Data Book

Data Transmission Circuits
Line Drivers, Receivers, Transceivers, UARTs

1993

TEXAS INSTRUMENTS

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Linear Products

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INTRODUCTION

In the 1993 *Data Transmission Circuits Data Book*, the Linear Products Division of Texas instruments presents technical information on various products for electronic media and electronic devices.

The Texas Instruments data transmission circuits represent technologies from classic bipolar through Advanced Low-Power Schottky (ALS), IMPACT™, LinBiCMOS™, CMOS, and BiMOS processes. The ALS and IMPACT oxide-isolated technologies provide the data transmission family with improved speed-power characteristics. LinBiCMOS technology features a step-function improvement in impedance, speed, power dissipation, and threshold stability.

This data book provides information on the following types of products:

- Data line drivers
- Data line receivers
- Data line transceivers
- Asynchronous communication elements (UARTs)

The data transmission line drivers, receivers, and transceivers, which support many popular data transmission standards, can connect electronic devices and systems at high data rates over significant cable lengths. The UARTs can control the sending and receipt of data through serial asynchronous data links.

Among new products offered by TI in the 1993 *Data Transmission Circuits Data Book* are numerous LinBiCMOS circuits for EIA RS-485, EIA-232, and IEEE 802.3 10BaseT data transmission standards. New packaging includes the shrink small-outline package (SSOP and DB) as well as surface-mount packages for popular mature products.

The data book is organized for quick location of a data sheet. The sequence is alphanumeric except for the SN prefixed parts; these data sheets are in base part number order, i.e., SN75ALS176 is located next to the SN75176B. The alphanumeric index provides a quick method of locating the data sheet for a known part number and indicates new products in this edition. The selection guide is grouped by industry standard and includes key features and the standard device footprint of the products in each category. The cross-reference guide lists other manufacturers' devices with the suggested TI replacement. Ordering information and mechanical data are in the last section of the data book.

An applications section has been added in this edition of the data book. This section is a reprint of material developed for the popular Linear Applications seminar series presented around the world. In this section are answers to the most commonly asked questions regarding data line circuits and applications.

While this data book offers design and specification data only for data transmission products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
LITERATURE RESPONSE CENTER
P.O. Box 809066
DALLAS, TEXAS 75380-9066

or telephone the Texas Instruments Literature Response number: 1-800-477-8924.

We sincerely believe the new 1993 *Data Transmission Circuits Data Book* will be a valuable addition to your collection of technical literature.

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†New devices added to this volume

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† UART – Universal Asynchronous Receivers/Transmitters
‡ FIFO – First In First Out

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uA9637A	uA9637AC	2–985
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SIGNETICS	SUGGESTED TI REPLACEMENT	PAGE NO.
AM26LS31	AM26LS31	2–13
AM26LS32	AM26LS32A	2–21
AM26LS33	AM26LS33A	2–21
MC1488	SN75188	2–737
MC1489	MC1489	2–751
MC1489A	MC1489A	2–751

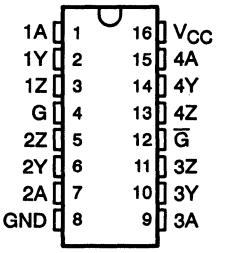
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

2 Line Drivers, Receivers, Transceivers

SLLS103B – D3636, DECEMBER 1990 – REVISED JANUARY 1993

- **Meets EIA Standard RS-422-A and CCITT Recommendation V.11**
- **Low Power, I_{CC} = 100 μA Typ**
- **Operates From a Single 5-V Supply**
- **High Speed, $t_{PLH} = t_{PHL}$ = 7 ns Typ**
- **Low Pulse Distortion ($t_{sk(p)}$ = 0.5 ns Typ)**
- **High Output Impedance In Power-Off Conditions**
- **Direct Replacement for National Semiconductor DS26C31**
- **Improved Replacement for AM26LS31**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

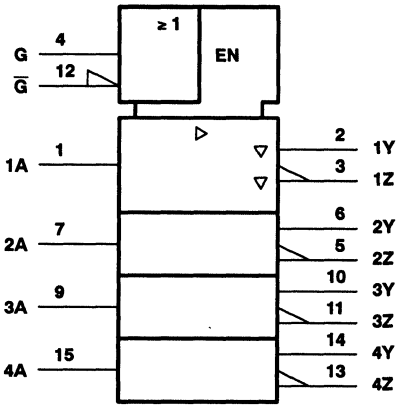
H = high level X = irrelevant
L = low level Z = high impedance (off)

description

The AM26C31C and AM26C31I are quadruple complementary-output line drivers designed to meet the requirements of EIA Standard RS-422-A and CCITT V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

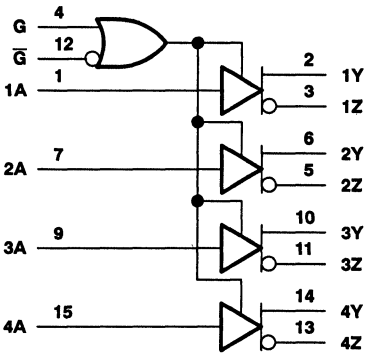
The AM26C31C is characterized for operation from 0°C to 70°C, and the AM26C31I is characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to 7 V
Input or output clamp current, I_{IK} or I_{OK} ..... ±20 mA
Output current, I_O ..... ±150 mA
V_{CC} current ..... 200 mA
GND current ..... −200 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: AM26C31C ..... 0°C to 70°C
AM26C31I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−20	mA
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	AM26C31C	0		70	°C
	AM26C31I	−40		85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_O = -20$ mA	2.4	3.4		V
V_{OL}	Low-level output voltage	$I_O = 20$ mA		0.2	0.4	V
$\|V_{OD}\|$	Differential output voltage	$R_L = 100\ \Omega$	2	3.1		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	$R_L = 100\ \Omega$			±0.4	V
V_{OC}	Common-mode output voltage	$R_L = 100\ \Omega$			3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡	$R_L = 100\ \Omega$			±0.4	V
I_I	Input current	V_I at V_{CC}, V_{IH}, V_{IL}, or GND			±1	μA
$I_{O(off)}$	Driver output curent with power off	$V_{CC} = 0$, $V_O = 6$ V			100	μA
		$V_{CC} = 0$, $V_O = -0.25$ V			−100	
I_{OS}	Driver output short-circuit current	$V_O = 0$	−30		−150	mA
I_{OZ}	Off-state (high-impedance state) output current	$V_O = 2.5$ V			20	μA
		$V_O = 0.5$ V			−20	μA
I_{CC}	Quiescent supply current	$I_O = 0$, $V_I = 0$ V or 5 V			100	μA
		$I_O = 0$, $V_I = 2.4$ V or 0.5 V, See Note 2		1.5	3	mA
C_i	Input capacitance			6		pF

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 2: Measured per input. All other inputs are at 0 V or 5 V.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 1 and 2, S1 is open		7	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			7	12	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PLH} - t_{PHL}\|$)			0.5	4	ns
t_{rD}, t_{fD}	Differential output rise and fall times	See Figures 1 and 4, S1 is open		5	10	ns
t_{PZH}	Output enable time to high level	See Figures 1 and 3, S1 is closed		10	19	ns
t_{PZL}	Output enable time to low level			10	19	ns
t_{PHZ}	Output disable time from high level			7	16	ns
t_{PLZ}	Output disable time from low level			7	16	ns
C_{pd}	Power dissipation capacitance (see Note 3)	No load		100		pF

NOTE 3: C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} V_{CC}^2 f$ where P_D is in watts, C_{pd} is in farads, V_{CC} is in volts, and f is in hertz.

PARAMETER MEASUREMENT INFORMATION

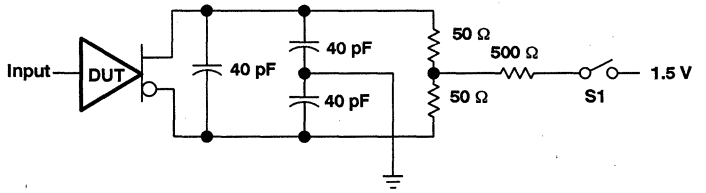


Figure 1. Test Circuit

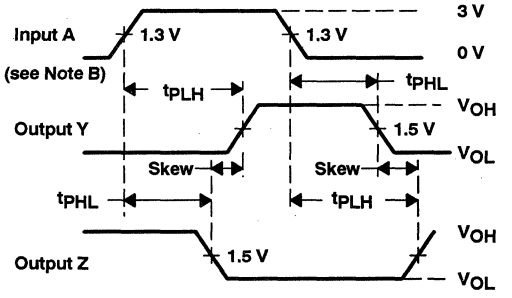


Figure 2. Propagation Delay Times and Skew Waveforms

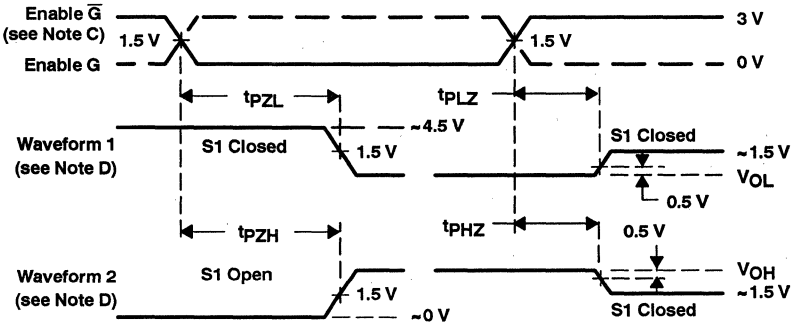


Figure 3. Enable and Disable Time Waveforms

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.
B. When measuring propagation delay times and skew, switch S1 is open.
C. Each enable is tested separately.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PARAMETER MEASUREMENT INFORMATION

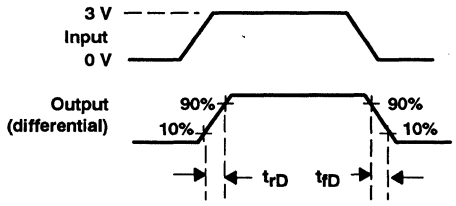
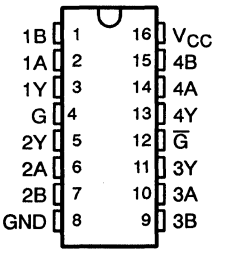


Figure 4. Differential Output Rise and Fall Times

SLLS104B – D3634, DECEMBER 1990 – REVISED DECEMBER 1992

- **Meets EIA Standards RS-422-A, RS-423-A, and CCITT Recommendation V.11**
- **Low Power, I_{CC} = 9 mA Typ**
- **±7-V Common-Mode Range With ±200-mV Sensitivity**
- **Input Hysteresis . . . 60 mV Typical**
- **t_{pd} = 19 ns (Typ)**
- **Operates From a Single 5-V Supply**
- **3-State Outputs**
- **Input Fail-Safe Circuitry**
- **Improved Replacement for AM26LS32**

D, N, OR NS† PACKAGE
(TOP VIEW)



† The NS package is available in left-ended taped and reeled (order device AM26C32CNSLE).

description

The AM26C32C and AM26C32I are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

The AM26C32 is manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32 while still maintaining ac and dc performance.

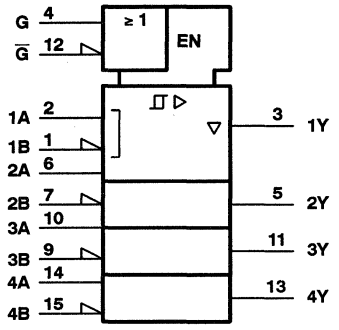
The AM26C32C is characterized for operation from 0°C to 70°C, and the AM26C32I is characterized from −40°C to 85°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES G	ENABLES $\overline{G}$	OUTPUT
$V_{ID} \geq V_{T+}$	H	X	H
	X	L	H
$V_{T-} \leq V_{ID} \leq V_{T+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{T+}$	H	X	L
	X	L	L
X	L	H	Z

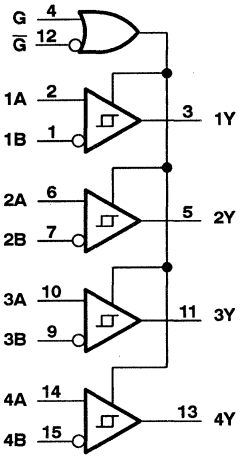
H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

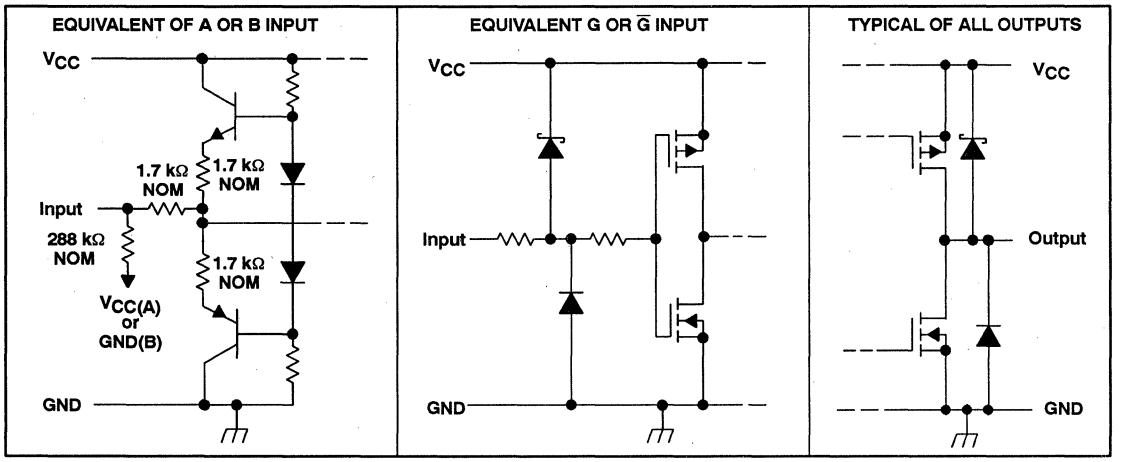
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I: A or B inputs ..... −11 V to 14 V
G or $\overline{G}$ inputs ..... 7 V
Output voltage, V_O ..... 7 V
Output current, I_O ..... ±25 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: AM26C32C ..... 0°C to 70°C
AM26C32I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to network ground terminal. Currents into the device are positive and currents out of the device are negative.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
NS	625 mW	5.0 mW/°C	400 mW	325 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode input voltage, V_{IC}				±7	V
High-level output current, I_{OH}				−6	mA
Low-level output current, I_{OL}				6	mA
Operating free-air temperature, T_A	AM26C32C	0		70	°C
	AM26C32I	−40		85	

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

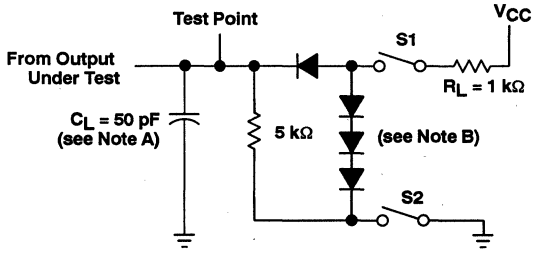
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Differential input high-threshold voltage	$V_O = V_{OH}$ min,	$I_{OH} = -440\ \mu A$			0.2	V
V_{T-}	Differential input low-threshold voltage	$V_O = 0.45$ V,	$I_{OL} = 8$ mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Enable input clamp voltage	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV,	$I_{OH} = -6$ mA	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV,	$I_{OL} = 6$ mA		0.2	0.3	V
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{CC}$ or GND			±0.5	±5	μA
I_I	Line input current	$V_I = 10$ V,	Other input at 0 V			1.5	mA
		$V_I = -10$ V,	Other input at 0 V			−2.5	
I_{IH}	High-level enable current	$V_I = 2.7$ V				20	μA
I_{IL}	Low-level enable current	$V_I = 0.4$ V				−100	μA
r_i	Input resistance	One input to ac ground			17		kΩ
I_{CC}	Supply current	$V_{CC} = 5.5$ V	All outputs disabled		9	14	mA
			All outputs enabled		12		

switching characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

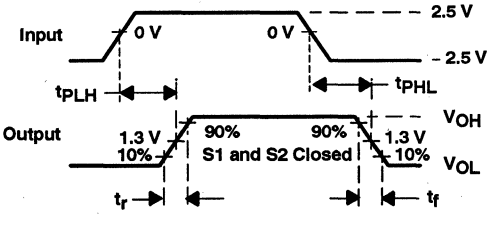
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 1	10	19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	19	30	ns
t_f	Output fall time			4	9	ns
t_r	Output rise time			4	9	ns
t_{PZH}	Output enable time to high level			13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level			13	22	ns
t_{PLZ}	Output disable time from low level			13	22	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

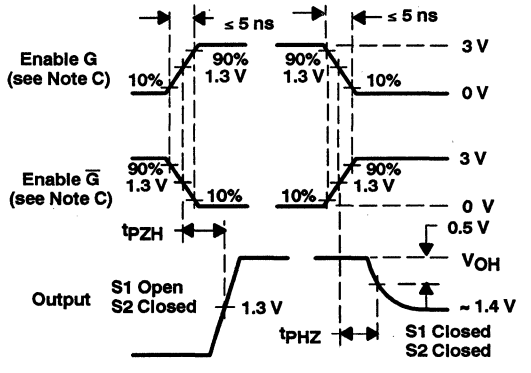
PARAMETER MEASUREMENT INFORMATION



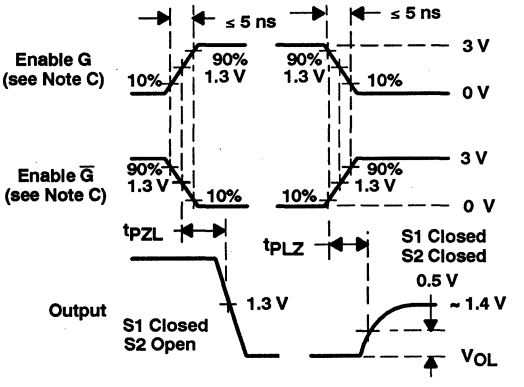
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

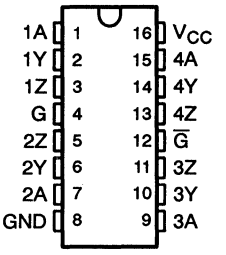
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 1. Test Circuit and Voltage Waveforms

SLLS114 – D2433, JANUARY 1979 – REVISED MAY 1990

- **Meets EIA Standard RS-422-A**
- **Operates From a Single 5-V Supply**
- **TTL Compatible**
- **Complementary Outputs**
- **High Output Impedance in Power-Off Conditions**
- **Complementary Output Enable Inputs**

D OR N PACKAGE
(TOP VIEW)



description

The AM26LS31C is a quad complementary-output line driver designed to meet the requirements of EIA Standard RS-422-A Federal Standard 1020. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

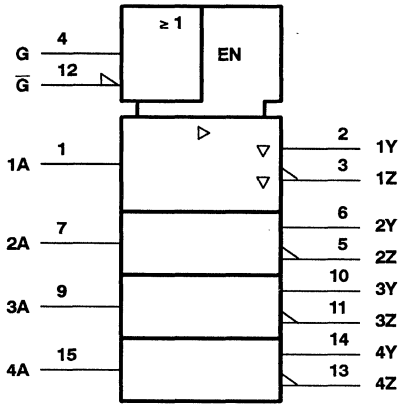
The AM26LS31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

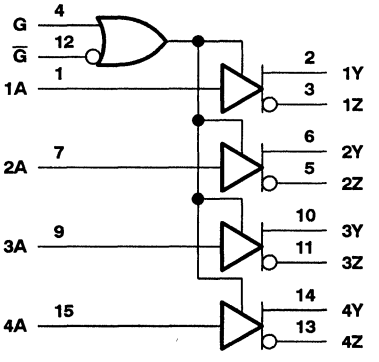
H = high level
L = low level
X = irrelevant
Z = high impedance (off)

logic symbol†

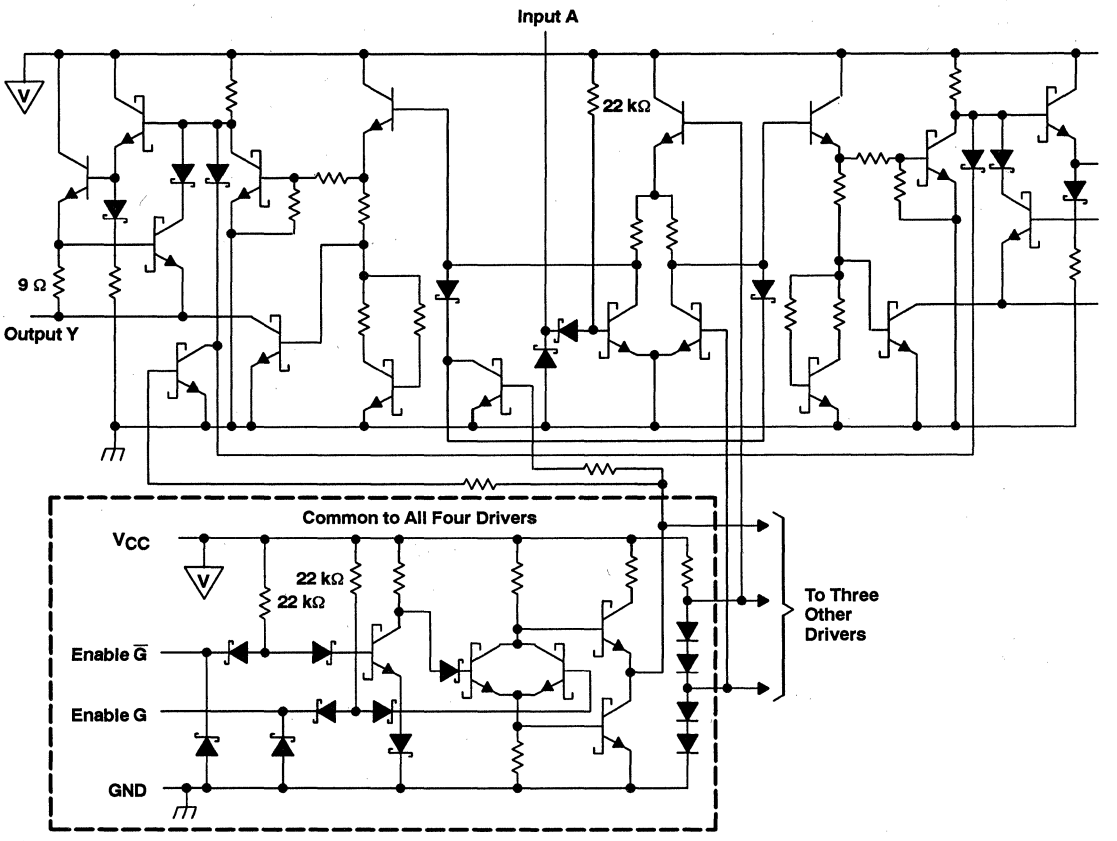


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output offstate voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

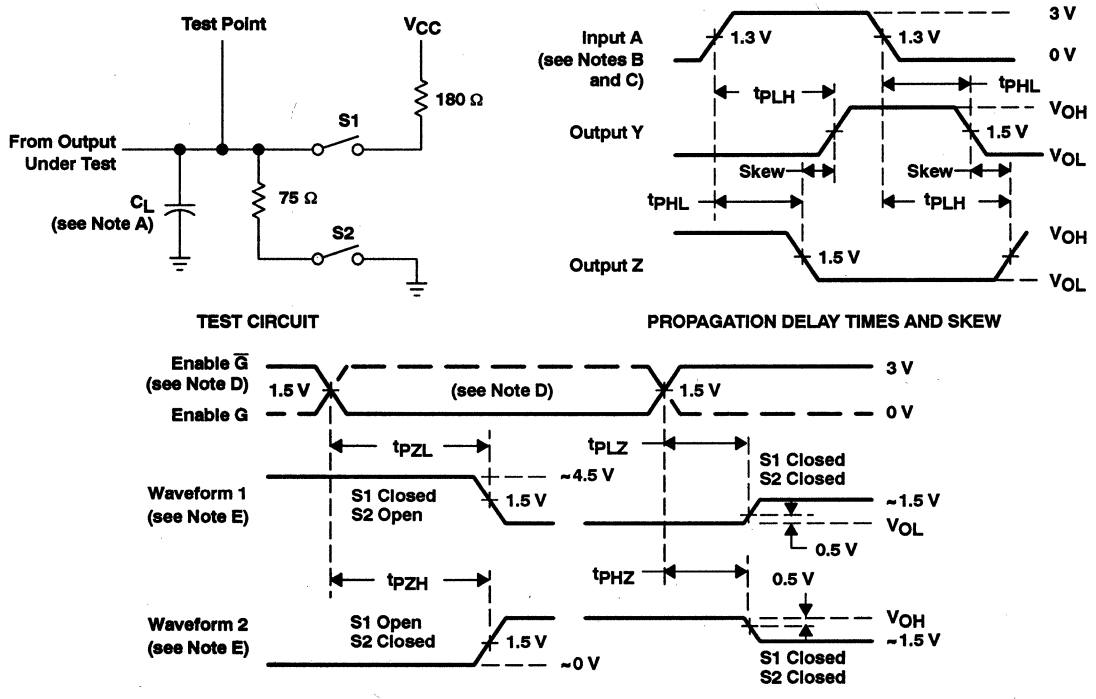
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −20 mA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 20 mA				0.5	V
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 4.75 V	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V				−0.36	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.25 V		−30		−150	mA
I_{CC}	Supply current	V_{CC} = 5.25 V,	All outputs disabled		32	80	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1	S1 and S2 open,		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				14	20	ns
	Output-to-output skew				1	6	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, See Figure 1	R_L = 75 Ω,		2.5	40	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, See Figure 1	R_L = 180 Ω,		37	45	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, See Figure 1	S1 and S2 closed,		21	30	ns
t_{PLZ}	Output disable time from low level				23	35	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.
C. When measuring propagation delay times and skew, switches S1 and S2 are open.
D. Each enable is tested separately.
E. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

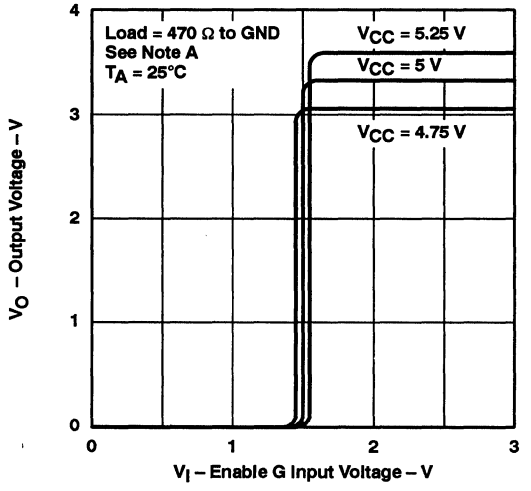


Figure 2

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

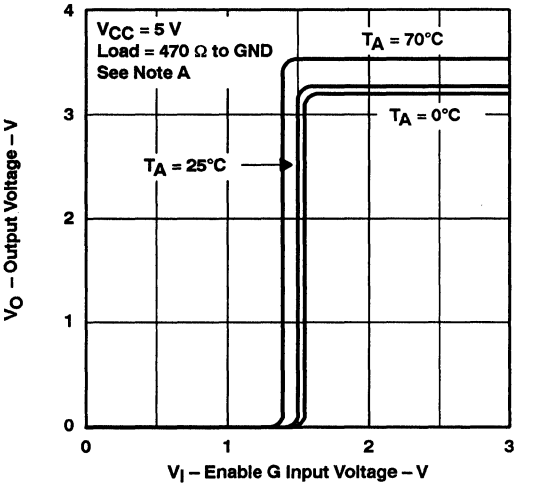


Figure 3

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

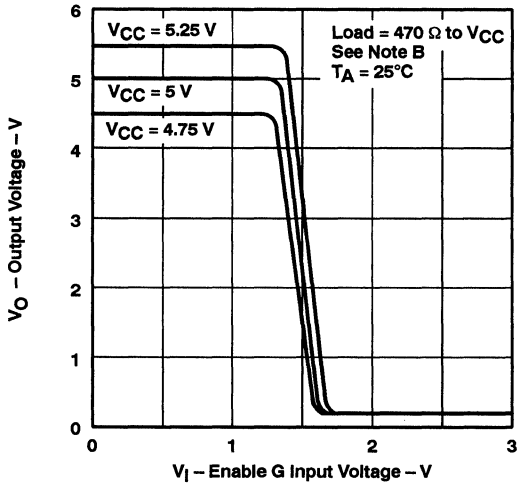


Figure 4

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

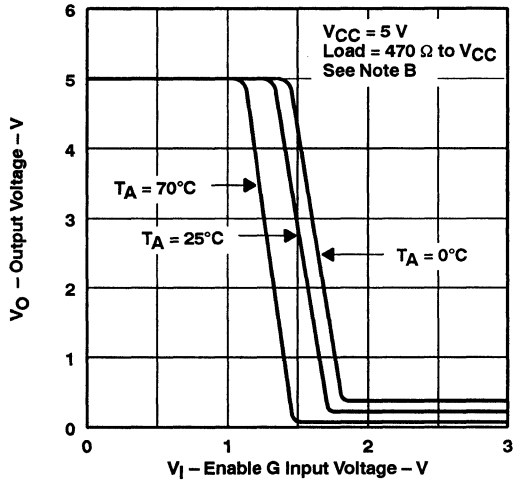


Figure 5

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

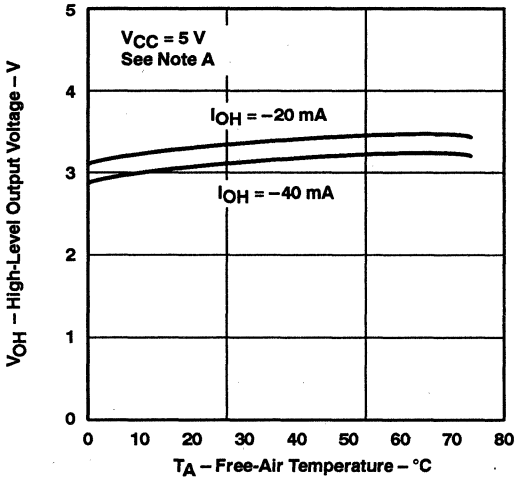


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

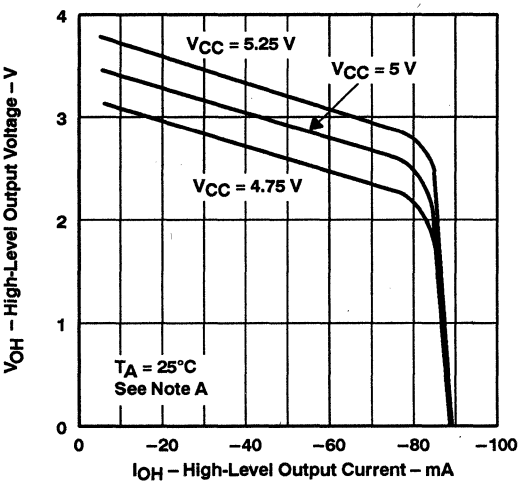


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

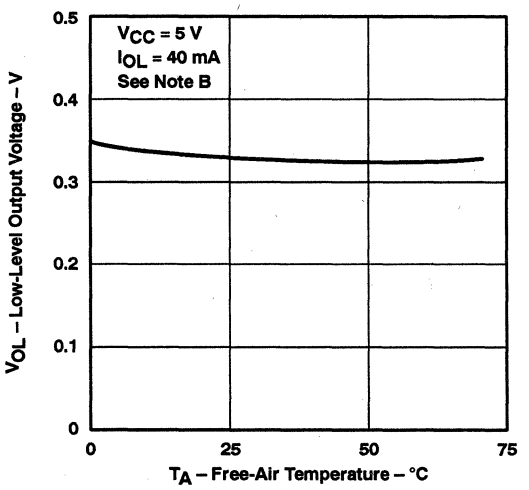


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

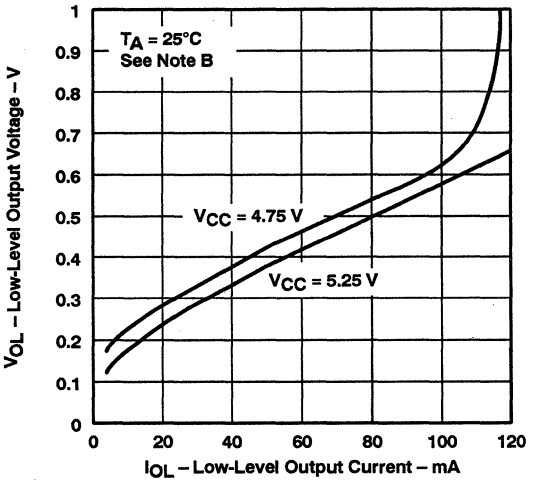


Figure 9

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

TYPICAL CHARACTERISTICS

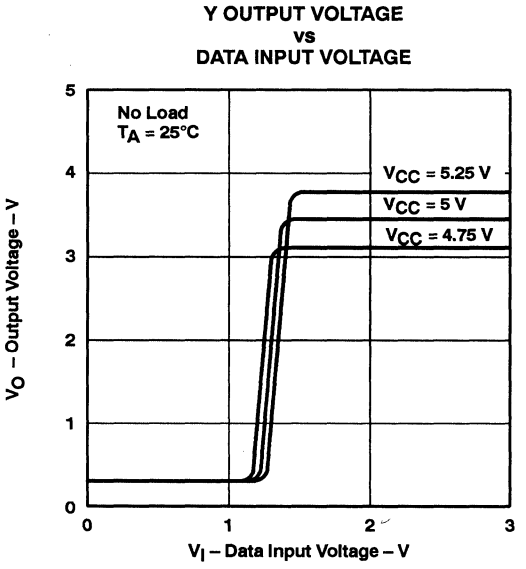


Figure 10

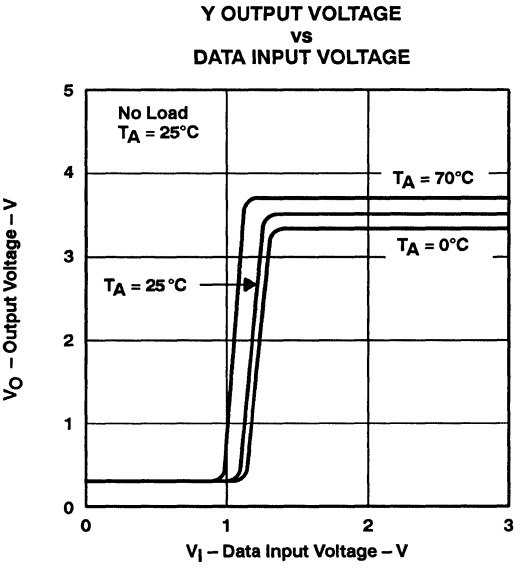


Figure 11

SLLS115A – D2434, OCTOBER 1980 – REVISED MARCH 1993

- **AM26LS32A Meets EIA Standards RS-422-A and RS-423-A**
- **AM26LS32A Has ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS32A Has ±15-V Common-Mode Range With ±500-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32 and AM26LS33**

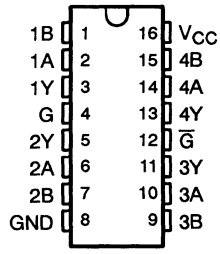
description

The AM26LS32A and AM26LS33A are quad line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection direct to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

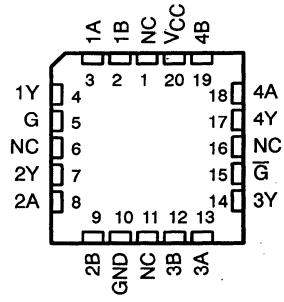
Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplilfication to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of −55°C to 125°C.

AM26LS32AC, AM26LS33AC . . . D OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



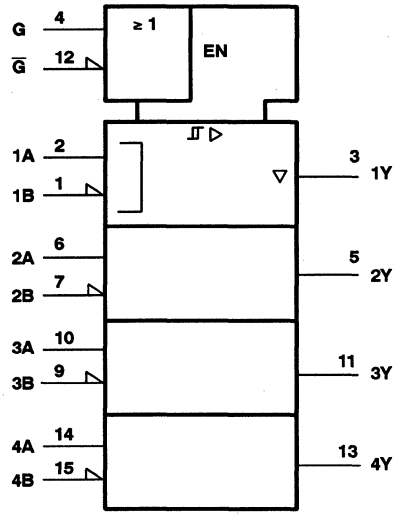
NC – No internal connection

FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

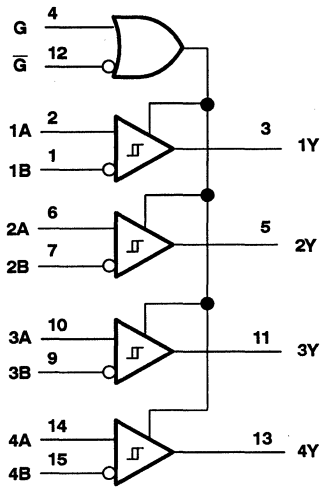
H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

logic symbol†

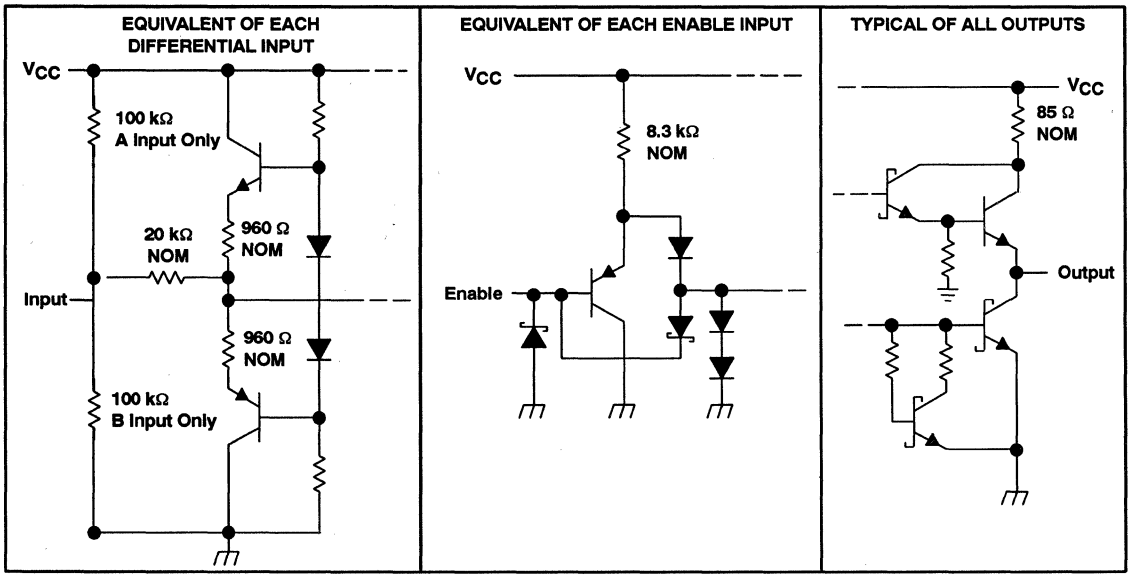


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		AM26LS32AC AM26LS33AC	AM26LS32AM AM26LS33AM	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, any differential input		±25	±25	V
Differential input voltage (see Note 2)		±25	±25	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		AM26LS32AC AM26LS33AC			AM26LS32AM AM26LS33AM			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM			±7			±7	V
	AM26LS33AC, AM26LS33AM			±15			±15	
High-level output current, I_{OH}				−440			−440	µA
Low-level output current, I_{OL}				8			8	mA
Operating free-air temperature, T_A		0		70	−55		125	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

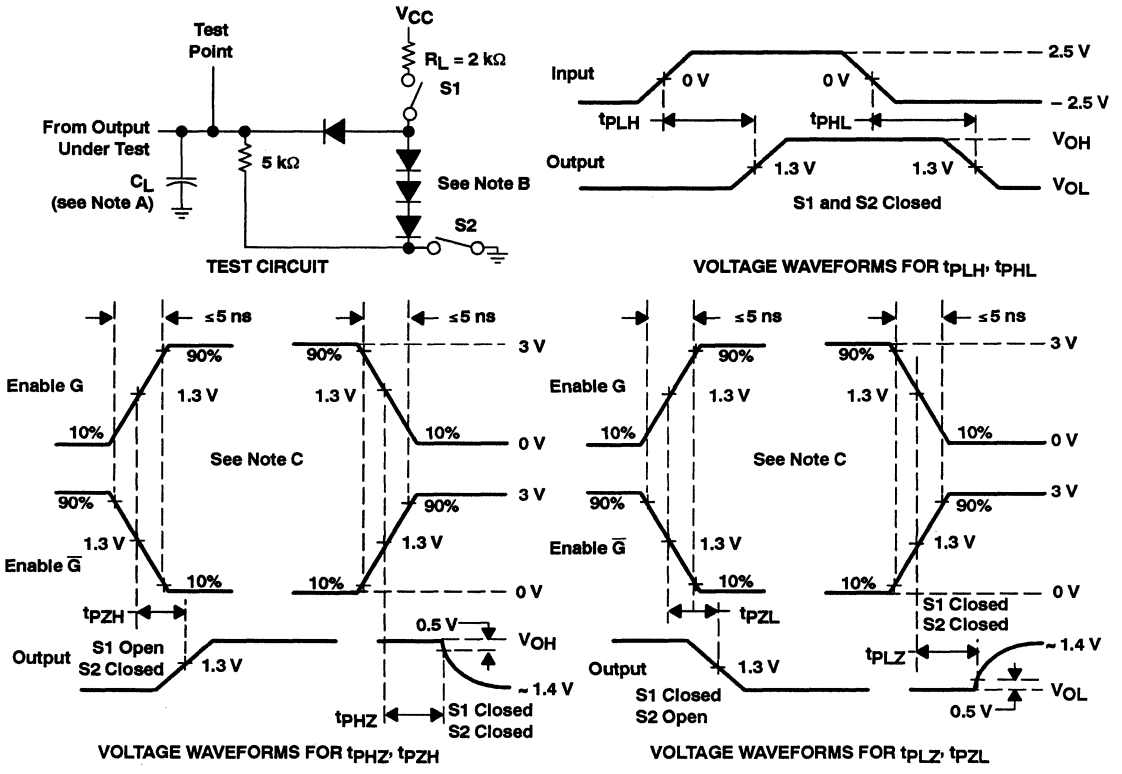
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshhold voltage	$V_O = V_{OH}$min, $I_{OH} = -440\ \mu A$		AM26LS32A			0.2	mV
				AM26LS33A			0.5	
V_{T-}	Negative-going threshhold voltage	$V_O = 0.45$ V, $I_{OL} = 8$ mA		AM26LS32A	−0.2‡			V
				AM26LS33A	−0.5‡			
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{IK}	Enable input clamp voltage	V_{CC} = MIN, $I_I = -18$ mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, $V_{I(\overline{G})} = 0.8$ V,	$V_{ID} = 1$ V, $I_{OH} = -440\ \mu A$	'32AC, '33AC	2.7			V
				'32AM, '33AM	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, $V_{I(\overline{G})} = 0.8$ V,	$V_{ID} = -1$ V,	$I_{OL} = 4$ mA			0.4	V
				$I_{OL} = 8$ mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX		$V_O = 2.4$ V			20	μA
				$V_O = 0.4$ V			−20	
I_I	Line input current	$V_I = 15$ V,	Other input at −10 V to 15 V				1.2	mA
		$V_I = -15$ V,	Other input at −15 V to 10 V				−1.7	
$I_{I(EN)}$	Enable input current	$V_I = 5.5$ V					100	μA
I_{IH}	High-level enable current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level enable current	$V_I = 0.4$ V					−0.36	mA
r_i	Input resistance	$V_{IC} = -15$ V to 15 V,	One input to ac ground		12	15		kΩ
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−15		−85	mA
I_{CC}	Supply current	V_{CC} = MAX,	All outputs disabled			52	70	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$, and $V_{IC} = 0$.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			22	35	ns
t_{PZH}	Output enable time to high level	$C_L = 15$ pF, See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level			20	25	ns
t_{PHZ}	Output disable time from high level	$C_L = 5$ pF, See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level			30	40	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 1

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT†

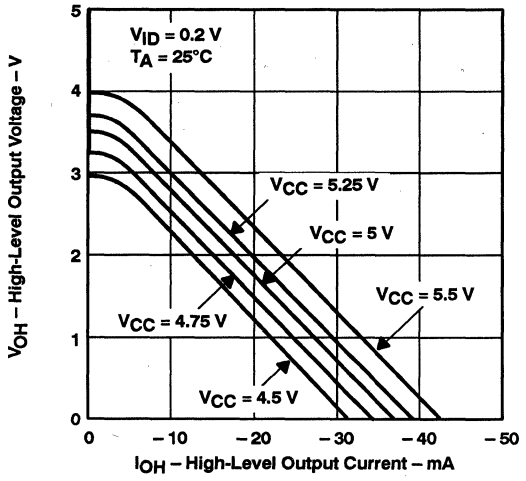


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

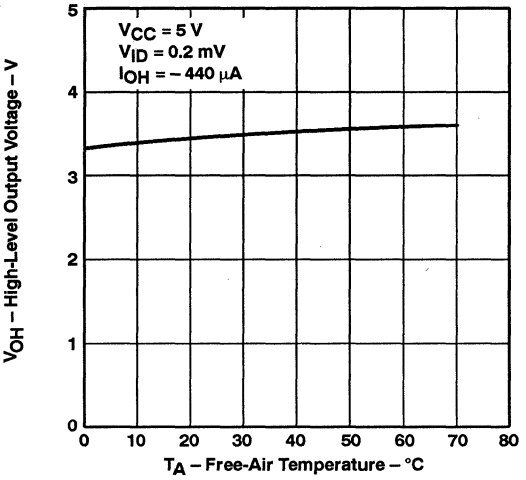


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

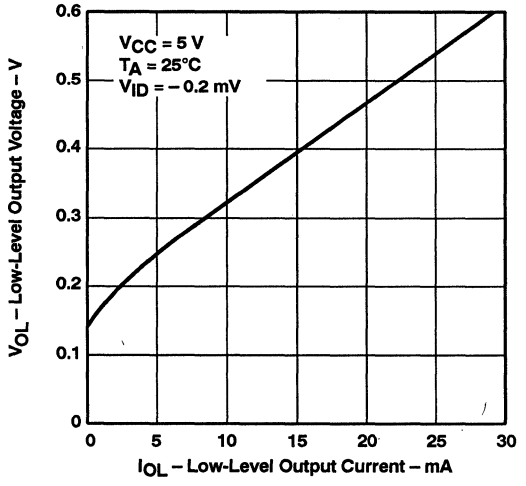


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

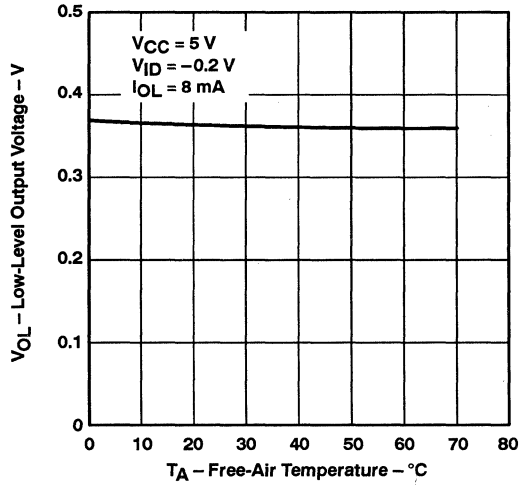


Figure 5

† V_{CC} = 5.5 V and V_{CC} = 4.5 V applies to M suffix devices only.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

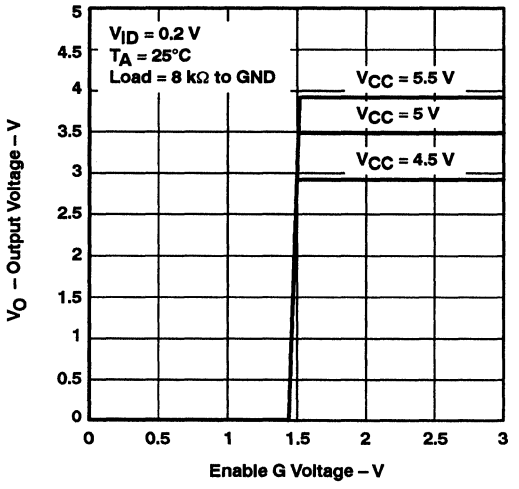


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

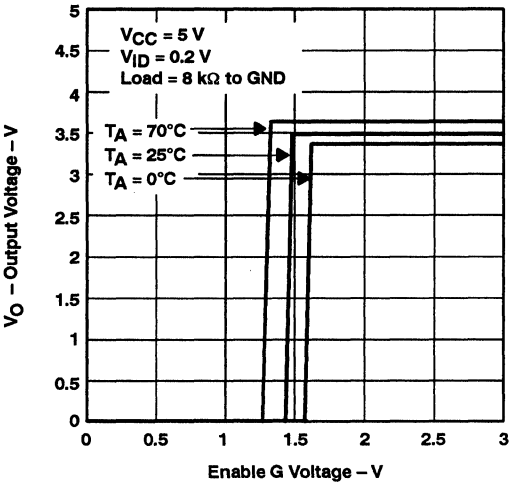


Figure 7

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

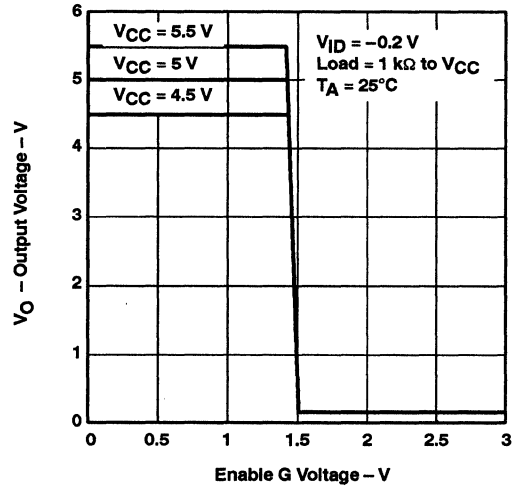


Figure 8

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

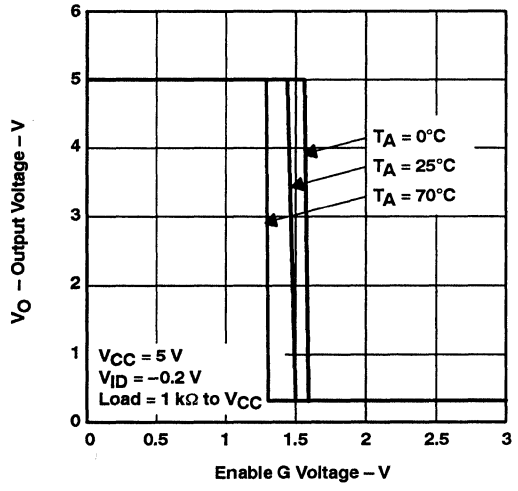


Figure 9

TYPICAL CHARACTERISTICS

AM26LS32A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

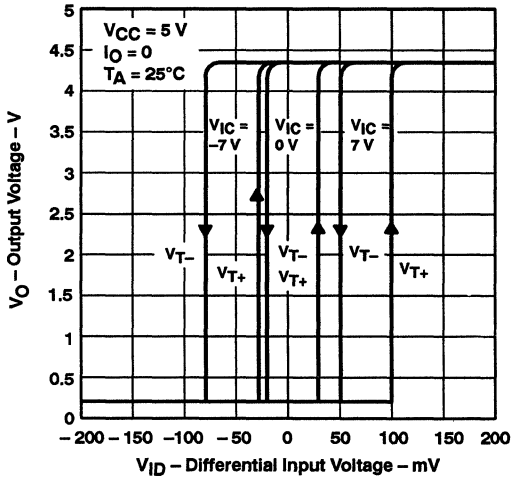


Figure 10

AM26LS33A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

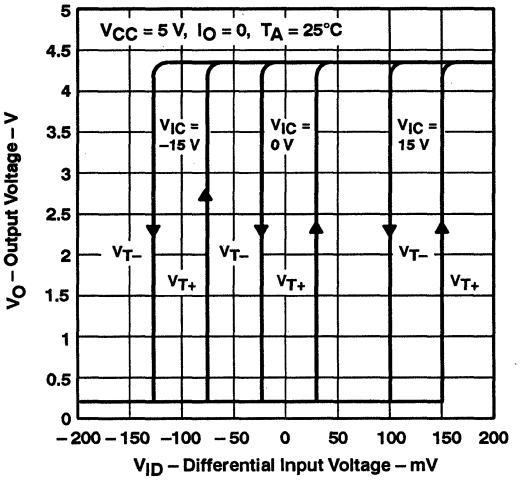
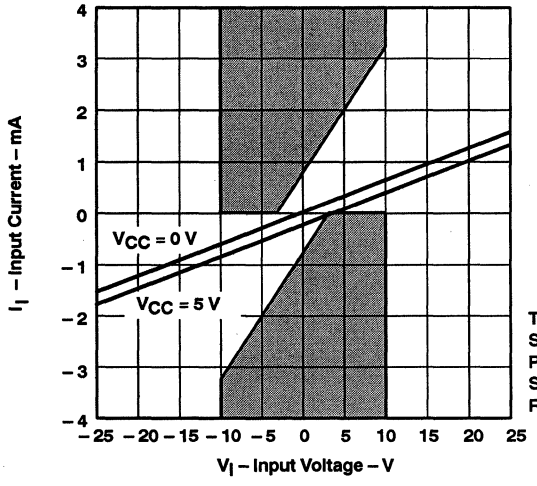


Figure 11

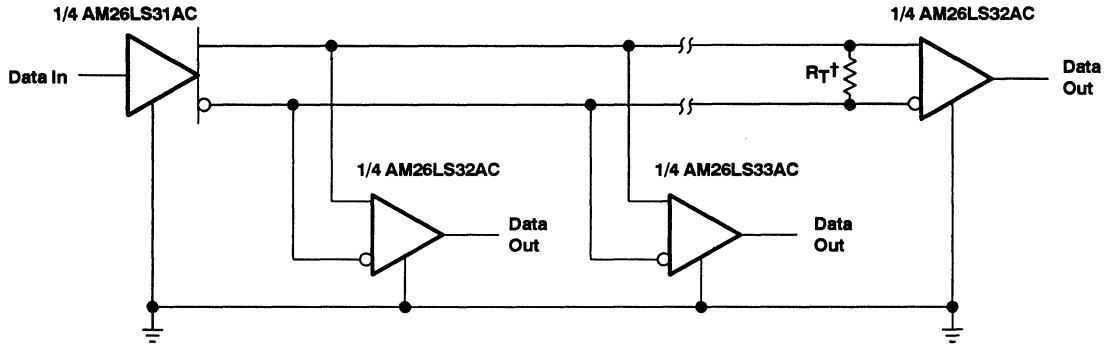
INPUT CURRENT
vs
INPUT VOLTAGE



The Unshaded Area Shows Requirements of Paragraph 4.2.1 of EIA Standards RS-422-A and RS-423-A

Figure 12

APPLICATION INFORMATION



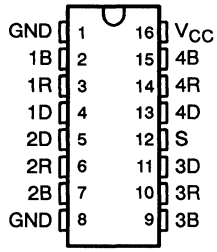
† R_T equals the characteristic impedance of the line.

Figure 13. Circuit With Multiple Receivers

SLLS116A – D2298, JANUARY 1977 – REVISED JANUARY 1993

- **Schottky Circuitry for High Speed, Typical Propagation Delay Time . . . 12 ns**
- **Drivers Feature Open-Collector Outputs for Party-Line (Data Bus) Operation**
- **Driver Outputs Can Sink 100 mA at 0.8 V Maximum**
- **PNP Inputs for Minimal Input Loading**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26S10 and AM26S11**

D OR N PACKAGE
(TOP VIEW)



description

The AM26S10C and AM26S11C are quadruple bus transceivers utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use pnp transistors to reduce the input loading.

The driver of the AM26S10C is inverting; the driver of the AM26S11C is noninverting. Each device has two ground connections for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10C and AM26S11C are characterized for operation over the temperature range of 0°C to 70°C.

Function Tables

AM26S10C
(transmitting)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

AM26S11C
(transmitting)

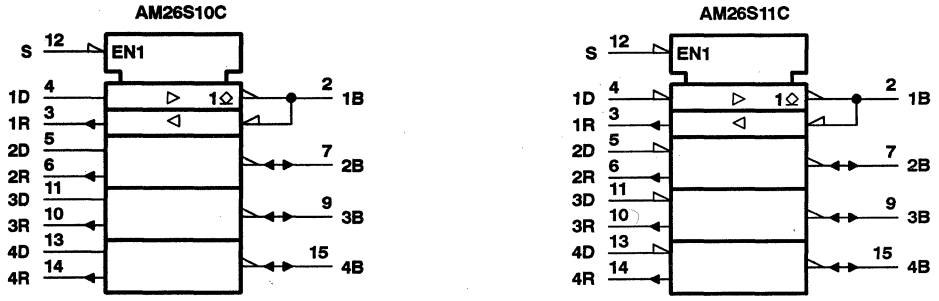
INPUTS		OUTPUTS	
S	D	B	R
L	H	H	L
L	L	L	H

AM26S10C AND AM26S11C
(receiving)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

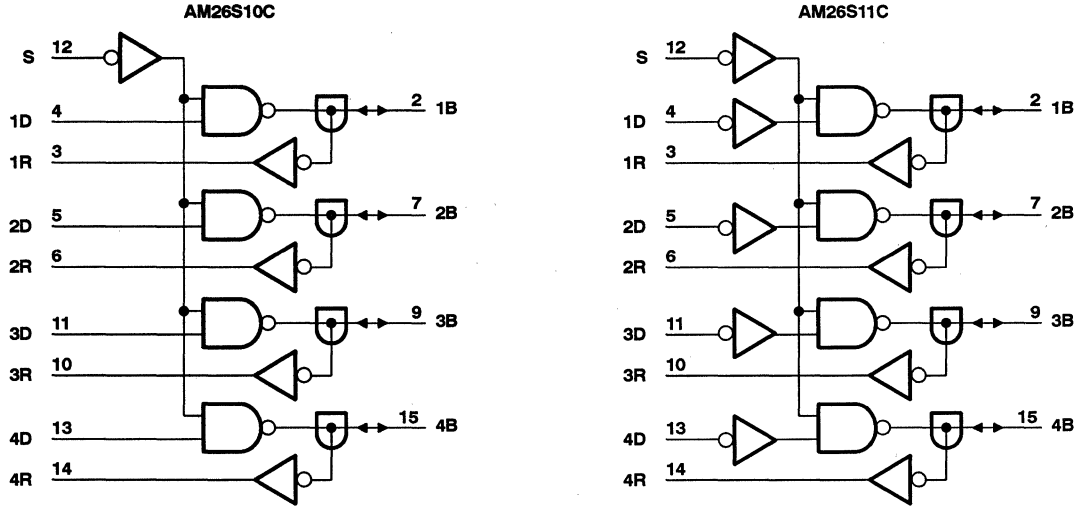
H = high level, L = low level, X = irrelevant

logic symbols†

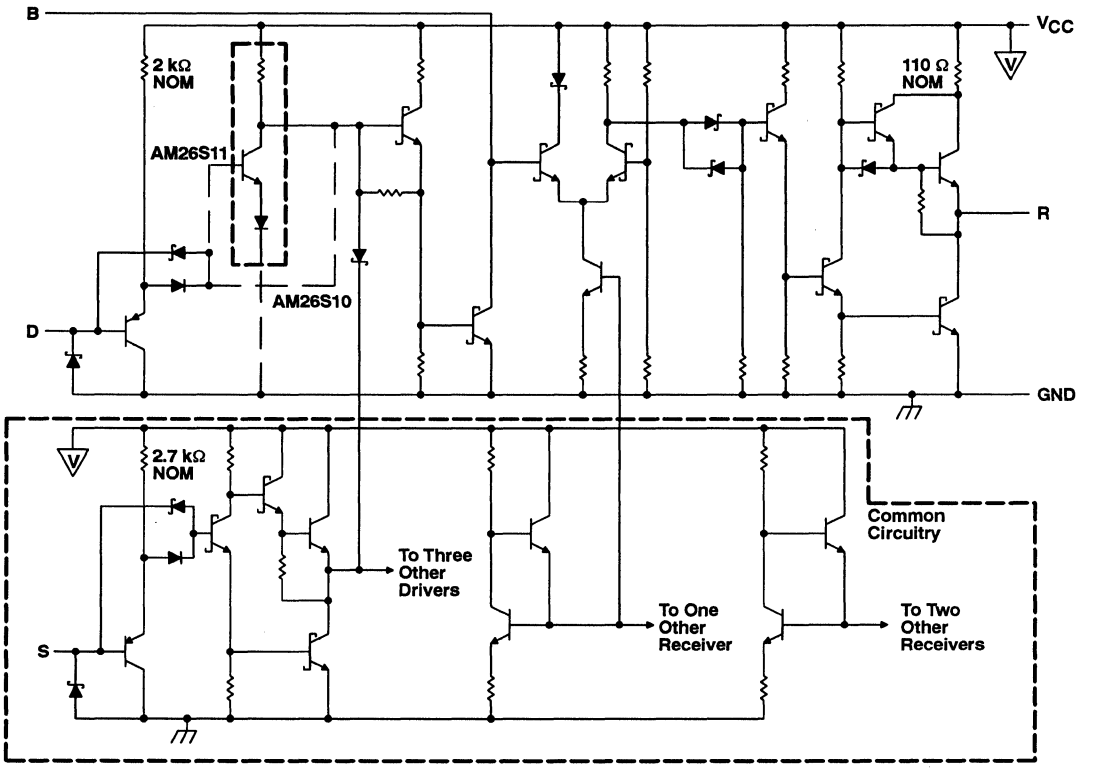


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



schematic (each transceiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Driver or strobe input voltage range, V_I ..... −0.5 V to 5.5 V
Bus voltage range, driver output off, V_O ..... −0.5 V to 5.25 V
Driver or strobe input current range, I_I ..... −30 mA to 5 mA
Driver output current, I_O ..... 200 mA
Receiver output current, I_O ..... 30 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-levael input voltage, V_{IH}	D or S	2			V
	B	2.25			
Low-level input voltage, V_{IL}	D or S			0.8	V
	B			1.75	
Receiver high-level output current, I_{OH}				−1	mA
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			20	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range

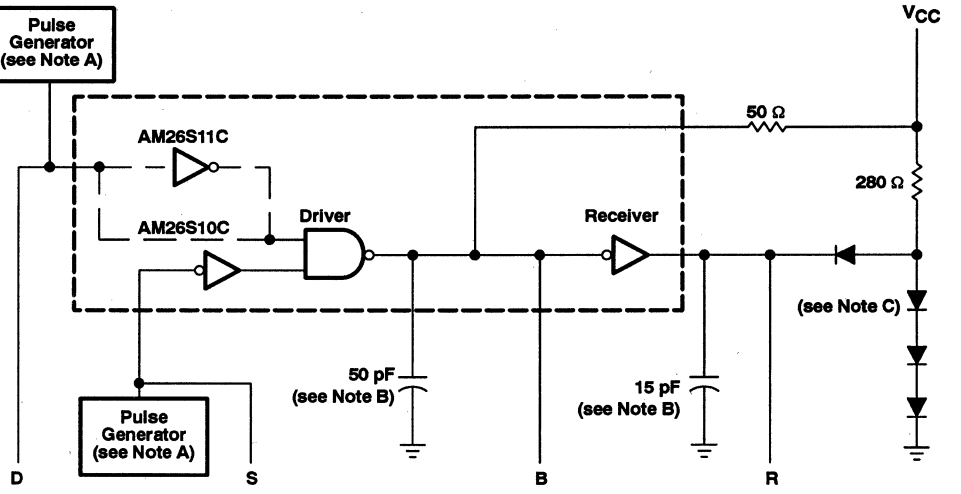
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D or S	V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	R	V_{CC} = 4.75 V, I_{OH} = −1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.7	3.4		V
V_{OH}	Low-level output voltage	R	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5	V
		B			I_{OL} = 40 mA		0.33	0.5	
					I_{OL} = 70 mA		0.42	0.7	
					I_{OL} = 100 mA		0.51	0.8	
$I_{O(off)}$	Off-stage output current	B	V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = 5.25 V,	V_O = 0.8 V			−50	μA
				V_{CC} = 5.25 V,	V_O = 4.5 V			100	
				V_{CC} = 0,	V_O = 4.5 V			100	
I_{IH}	High-level input current	D	V_{CC} = 5.25 V,	V_I = 2.7 V				30	μA
		S						20	
I_I	Input current at maximum input voltage	D or S	V_{CC} = 5.25 V,	V_I = 5.5 V				100	μA
I_{IL}	Low-level input current	D	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.54	mA
		S						−0.36	
I_{OS}	Short-circuit output current‡	R	V_{CC} = 5.25 V			−18		−60	mA
I_{CC}	Supply current		V_{CC} = 5.25 V, All driver outputs low	Strobe at 0 V,	No load,		45	70	mA
								80	

† All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

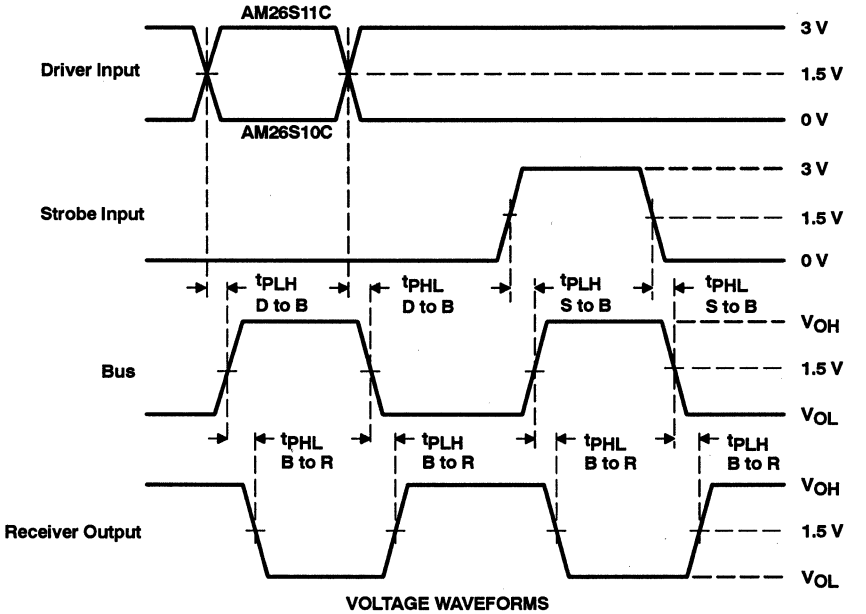
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	AM26S10C			AM26S11C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		10	15		12	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		12	19	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			14	18		15	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					13	18		14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R			10	15		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		10	15	
t_{TLH}	Transition time, low-to-high-level output		B		4	10		4	10		ns
t_{THL}	Transition time, high-to-low-level output				2	4		2	4		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns.
B. Includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

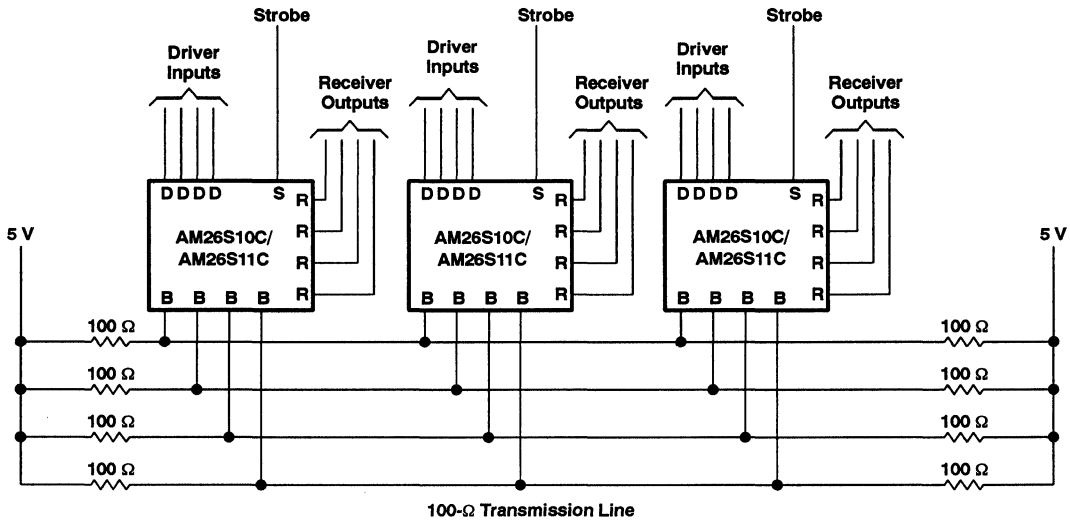
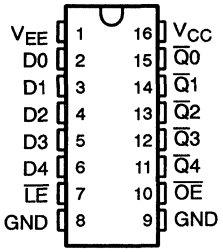


Figure 2. Party-Line System

SLLS035B – D3058, NOVEMBER 1987 – REVISED FEBRUARY 1993

- **ECL Control Inputs**
- **3-State Outputs**
- **10K ECL Input Compatible**
- **Direct Replacement for National Semiconductor DP8480**

N PACKAGE
(TOP VIEW)



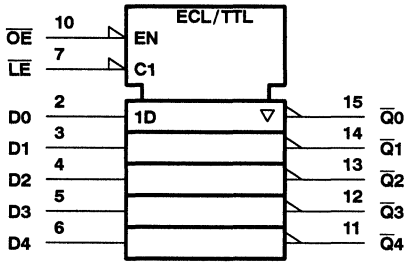
description

This circuit translates ECL-input levels to TTL-output levels and provides an inverting transparent latch. The 3-state outputs are designed to drive highly capacitive loads. All inputs operate at ECL levels.

If latch enable ($\overline{LE}$) is low, the latches are transparent and the $\overline{Q}$ outputs follow the complement of the D inputs. If $\overline{LE}$ is high, the outputs are latched. If output enable ($\overline{OE}$) is high, the outputs are in the high-impedance state, as they are during power up and power down.

The DP8480 is characterized for operation from 0°C to 75°C.

logic symbol†

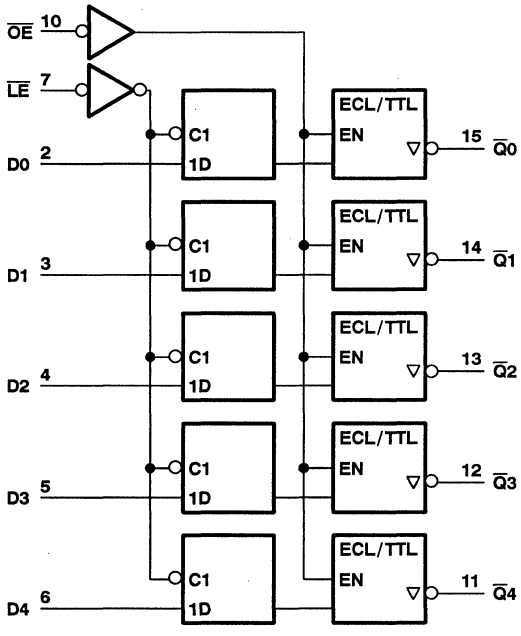


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each latch/translator)

$\overline{OE}$	$\overline{LE}$	D	$\overline{Q}$
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	X	Q_0

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Supply voltage, V_{EE} ..... −8 V
Input voltage range, V_I ..... 0 V to V_{EE}
Output voltage, V_O ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 75°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 75°C$ POWER RATING
N	1150 mW	9.2 mW/°C	690 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{EE}		−4.68	−5.20	−5.72	V
High-level Input voltage, V_{IH} (see Note 1)	T_A = 0°C	−1145		−840	mV
	T_A = 25°C	−1105		−810	
	T_A = 75°C	−1045		−720	
Low-level Input voltage, V_{IL} (see Note 1)	T_A = 0°C	−1870		−1490	mV
	T_A = 25°C	−1850		−1475	
	T_A = 75°C	−1830		−1450	
Pulse duration, $\overline{LE}$ low, t_w (see Figure 1)		5			ns
Setup time, data before $\overline{LE}\uparrow$, t_{su} (see Figure 1)		3			ns
Hold time, data after $\overline{LE}\uparrow$, t_h (see Figure 1)		3			ns
Operating free-air temperature, T_A		0		75	°C

NOTE 1: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −10 mA		V_{CC}−2			V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA			0.2	0.5	V
I_{IH}	High-level input current	$V_{IH} = V_{IH}$ max			75	350	µA
I_{IL}	Low-level input current	$V_{IL} = V_{IL}$ min			50	85	µA
I_{OSH}	High-state short-circuit output current	V_{OSH} = 0,	See Note 2	−70	−150		mA
I_{OSL}	High-state short-circuit output current	V_{OSL} = 2.5 V,	See Note 2	70	150		mA
I_{OZ}	High-impedance state output current	V_O = 0 to 5 V			±1	±50	µA
I_{CC}	Supply current from V_{CC}	Outputs open,	Inputs = V_{IL}		16	35	mA
I_{EE}	Supply current from V_{EE}	Outputs open,	Inputs = V_{IL}		−30	−50	mA

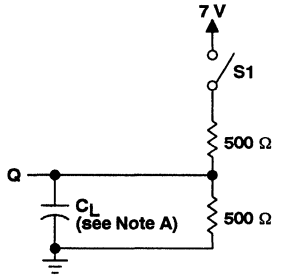
† Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
NOTE 2: During testing of I_{OSH} or I_{OSL}, only one output should be tested at a time and the current should be limited to a maximum of ±120 mA.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

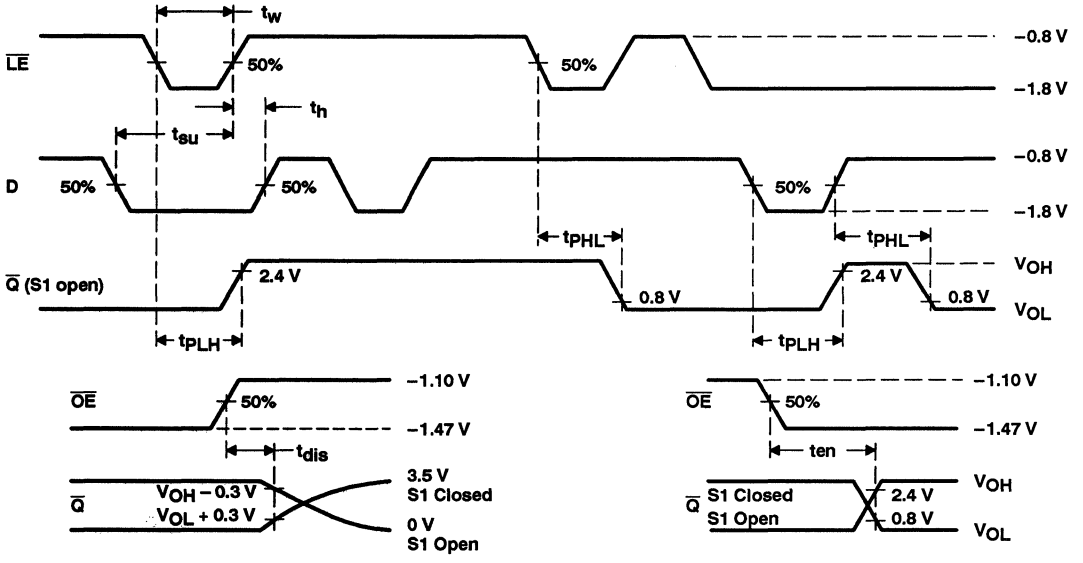
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{LE}$ input	C_L = 50 pF, See Figure 1	4	10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{LE}$ input		4	11	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from D input		3.5	10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from D input		3.5	11	15	ns
t_{en}	Output enable time from $\overline{OE}$ input		6	12	25	ns
t_{dis}	Output disable time from $\overline{OE}$ input		4.5	8	22	ns

† Typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C, and with all channels switched simultaneously.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



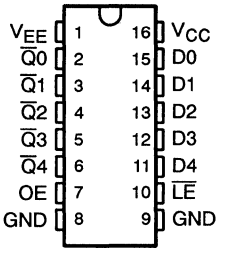
NOTES: A. C_L includes probe and jig capacitance.
B. ECL input rise times and fall time are 2 ns ± 0.2 ns from 20% to 80%.

Figure 1. Load Circuit and Voltage Waveforms

SLLS036B – D3059, NOVEMBER 1987 – REVISED FEBRUARY 1993

- **ECL Control Inputs**
- **10K ECL Compatible**
- **Propagation Delay . . . 4 ns Typ**
- **Direct Replacement for National Semiconductor DP8481**

N PACKAGE
(TOP VIEW)



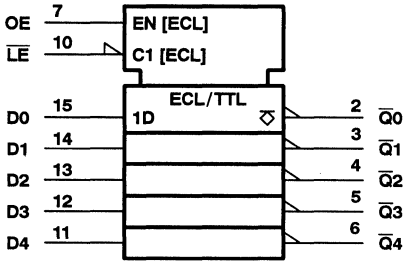
description

This circuit translates TTL-input levels to ECL-output levels and provides a 5-bit transparent latch. The outputs are gated by output enable (OE) and can be wire-OR connected. The latch enable ($\overline{LE}$) and OE inputs are ECL.

If latch enable ($\overline{LE}$) is low, the latches are transparent and the $\overline{Q}$ outputs follow the complement of the D inputs. If $\overline{LE}$ is high, the outputs are latched. If output enable (OE) is low, the outputs are forced to the low level.

The DP8481 is characterized for operation from 0°C to 75°C.

logic symbol†

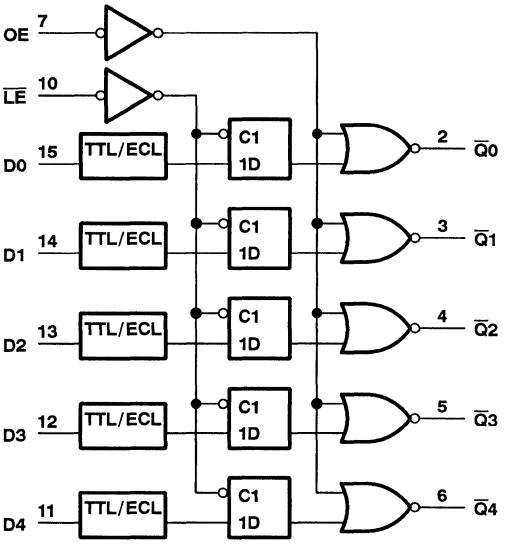


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each latch/translator)

OE	$\overline{LE}$	D	$\overline{Q}$
H	L	H	L
H	L	L	H
H	H	X	Q_0
L	X	X	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Supply voltage, V_{EE} ..... −8 V
Input voltage range, V_I: OE or $\overline{LE}$ input ..... 0 V to V_{EE}
D inputs ..... −1 V to 5.5 V
Output current, I_O ..... −50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating temperature range, T_A ..... 0°C to 75°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 75°C$ POWER RATING
N	1150 mW	9.2 mW/°C	690 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{EE}		−4.68	−5.20	−5.72	V
High-level input voltage, V_{IH} (TTL-level D inputs)		2			V
Low-level input voltage, V_{IL} (TTL-level D inputs)				0.8	V
High-level input voltage, V_{IH} (ECL-level OE and $\overline{LE}$ inputs) (see Note 1)	$T_A = 0°C$	−1145		−840	mV
	$T_A = 25°C$	−1105		−810	
	$T_A = 75°C$	−1045		−720	
Low-level input voltage, V_{IL} (ECL-level OE and $\overline{LE}$ inputs) (see Note 1)	$T_A = 0°C$	−1870		−1490	mV
	$T_A = 25°C$	−1850		−1475	
	$T_A = 75°C$	−1830		−1450	
Pulse duration, $\overline{LE}$ low, t_w (see Figure 1)		5			ns
Setup time, t_{su}	Data before $\overline{LE}\uparrow$ (see Figure 1)	5			ns
	Data before OE↑ (see Note 2 and Figure 1)	5.5			
Hold time, data after $\overline{LE}\uparrow$, t_h (see Figure 1)		1			ns
Operating free-air temperature, T_A		0		75	°C

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.
2. This setup time applies when operating in the transparent mode ($\overline{LE}$ is low) and it is necessary that valid data be available at the output immediately after the outputs are enabled.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D0–D4	$I_I = -12$ mA			−0.8	−1.2	V
I_{IH}	High-level input current	D0–D4	$V_I = 2.5$ V			1	40	μA
		OE, $\overline{LE}$	$V_I = -0.8$ V				200	
I_{IL}	Low-level input current	D0–D4	$V_I = 0.5$ V			−50	−200	μA
		OE, $\overline{LE}$	$V_I = -1.8$ V				150	
V_{OH}	High-level output voltage (see Notes 1 and 3)		$V_{EE} = -5.2$ V,	$T_A = 0°C$	−1000		−840	mV
			$V_{EE} = -5.2$ V,	$T_A = 25°C$	−960		−810	
			$V_{EE} = -5.2$ V,	$T_A = 75°C$	−900		−720	
$V_{OH(C)}$	Critical high-level output voltage (see Notes 1 and 3)		$V_{EE} = -5.2$ V,	$T_A = 0°C$	−1020			mV
			$V_{EE} = -5.2$ V,	$T_A = 25°C$	−980			
			$V_{EE} = -5.2$ V,	$T_A = 75°C$	−920			
V_{OL}	Low-level output voltage (see Notes 1 and 3)		$V_{EE} = -5.2$ V,	$T_A = 0°C$	−1870		−1665	mV
			$V_{EE} = -5.2$ V,	$T_A = 25°C$	−1850		−1650	
			$V_{EE} = -5.2$ V,	$T_A = 75°C$	−1830		−1625	
$V_{OL(C)}$	Critical low-level output voltage (see Notes 1 and 3)		$V_{EE} = -5.2$ V,	$T_A = 0°C$			−1645	mV
			$V_{EE} = -5.2$ V,	$T_A = 25°C$			−1630	
			$V_{EE} = -5.2$ V,	$T_A = 75°C$			−1605	
I_{CC}	Supply current from V_{CC}		$V_{CC} = 5.5$ V				20	mA
I_{EE}	Supply current from V_{EE}		$V_{EE} = -5.7$ V				−90	mA

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated one minimum, is used in this data sheet for logic levels only.

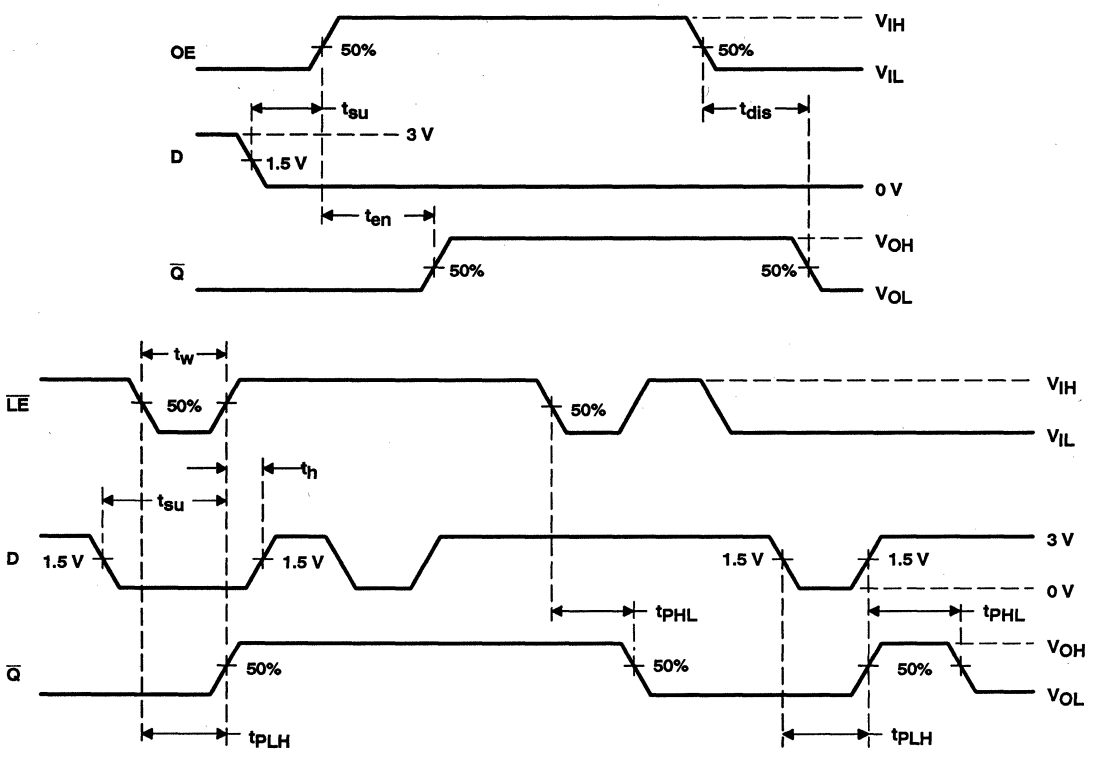
3. V_{OH} and V_{OL} are tested using the outer-limit values V_{IH} max and V_{IL} min. The critical values $V_{OH(C)}$ and $V_{OL(C)}$ are tested using the inner-limit values V_{IH} min and V_{IL} max. The latter values ensure the noise margins of 155-mV high and 125-mV low associated with 10K ECL.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{LE}$ input	$R_L = 50\ \Omega$ to −2 V, See Figure 1	1.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{LE}$ input		1.5	4	6	ns
t_{PLH}	Propagation delay time, low-to-high-level output from D input		2.5	4	7.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output from D input		2.5	4	7.5	ns
t_{en}	Output enable time from OE input		1	3	4	ns
t_{dis}	Output disable time from OE input		1	3	4	ns

† Typical values are at $V_{CC} = 5$ V, $V_{EE} = -5.2$ V, $T_A = 25°C$.

PARAMETER MEASUREMENT INFORMATION



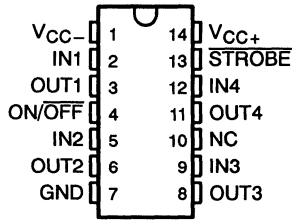
NOTE A: ECL input rise and fall times at OE and $\overline{LE}$ are 2 ns ± 0.2 ns from 20% to 80%. TTL input rise and fall times at D inputs are 3 ns maximum measured between 10% and 90%.

Figure 1. Switching Time Waveforms

SLLS048C – D3297, APRIL 1989 – REVISED MARCH 1993

- **Low Supply Voltage . . . ±5 V to ±15 V**
- **Supply Current . . . 500 μA Typ**
- **Zero Supply Current When Shut Down**
- **Outputs Can Be Driven ±30 V**
- **Output Open When Off (3-State)**
- **10-mA Output Drive**
- **Output of Several Devices Can Be Paralleled**
- **Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Std RS-232-C)**
- **Designed to Be Interchangeable With Linear Technology LT1030**

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	LT1030CD	LT1030CN

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LT1030CDR).

description

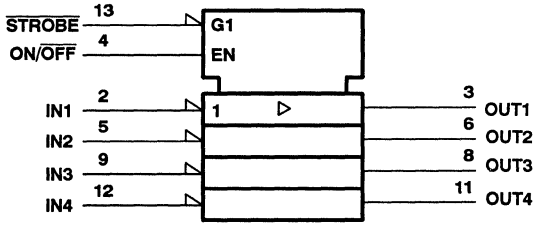
The LT1030C is an EIA-232 line driver that operates over a ±5-V to ±15-V supply voltage range on low supply current. The device can be shut down to zero supply current. Current limiting fully protects the outputs from externally-applied voltages of ±30 V. Since the output swings to within 200 mV of the positive supply and to within 1 V of the negative supply, supply voltage requirements are minimized.

A major advantage of the LT1030C is the high-impedance output state when the device is off or powered down. This feature allows several different drivers on the same bus.

The divide can be used as an EIA-232 driver, micropower interface, or level translator, among others.

The LT1030C is characterized for operation from 0°C to 70°C.

logic symbol†

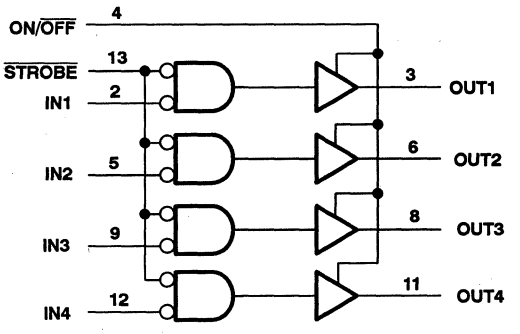


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Terminal Functions

PIN NAME	PIN NO	DESCRIPTION
GND	7	Ground pin
IN1, IN2, IN3, IN4	2, 5, 9, 12	Logic inputs. Operate properly on TTL or CMOS levels. Output valid from $V_I = V_{CC-} + 2$ V to 15 V. Connect to 5 V when not used.
ON/OFF	4	Shuts down entire circuit. Cannot be left open. For normally on operation, connect between 5 V and 10 V. If V_{IL} is at or near 0.8 V, significant settling time may be required.
OUT1, OUT2, OUT3, OUT4	3, 6, 8, 11	Line driver outputs
STROBE	13	Forces all outputs low. Drive with 3 V. Strobe terminal input impedance is approximately 2 kΩ to GND. Leave open when not used.
V_{CC+}	14	Positive supply
V_{CC-}	1	Negative supply

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) ..... 0 V to 15 V
Supply voltage range, V_{CC-} ..... 0 V to −15 V
Input voltage range, logic inputs, V_I ..... V_{CC-} to 25 V
Input voltage range at ON/$\overline{OFF}$, V_I ..... 0 V to 12 V
Output voltage range (any output) ..... V_{CC+} − 30 V to V_{CC-} + 30 V
Duration of output short circuit to ±30 V at (or below) 25°C (see Note 2) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	−5	−15	V
High-level input voltage, V_{IH} (see Note 3)	2	15	V
Low-level input voltage, V_{IL} (see Note 3)		0.8	V
Operating free-air temperature, T_A	0	70	°C

NOTE 3: These V_{IH} and V_{IL} specifications apply only for inputs IN1–IN4. For operating levels for ON/$\overline{OFF}$, see Figure 2.

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	I_O = −2 mA, T_A = 25°C	V_{CC+}−0.3	V_{CC+}−0.1		V
V_{OM-}	Maximum negative peak output voltage swing	I_O = 2 mA, T_A = 25°C		V_{CC-}+0.9	V_{CC-}+1.4	V
I_{IH}	High-level input current	$V_I \geq 2$ V, T_A = 25°C		2	20	µA
I_{IL}	Low-level input current	$V_I \leq 0.8$ V, T_A = 25°C		10	20	µA
I_I	Input current, ON/$\overline{OFF}$	V_I = 0		−0.1	−10	µA
		V_I = 5 V		30	65	
I_O	Output current	T_A = 25°C	5	12		mA
I_{OZ}	Off-state output current	V_O = ±15 V, T_A = 25°C, ON/$\overline{OFF}$ at 0.4 V		±2	±100	µA
I_{CC}	Supply current (all outputs low)	$V_I \geq$ at 2.4 V, I_O = 0		500	1000	µA
$I_{CC(off)}$	Off-state supply current	ON/$\overline{OFF}$ at 0.4 V			10	µA
		ON/$\overline{OFF}$ at 0.1 V		10	150	

operating characteristics, $V_{CC\pm}$ = ±5 V to ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ, C_L = 51 pF	4	15	30	V/µs

† All typical values are at $V_{CC\pm}$ = ±12 V, T_A = 25°C.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

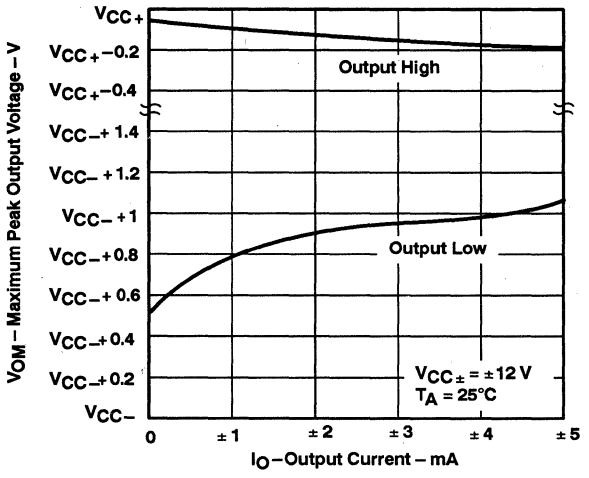


Figure 1

ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE
vs
FREE–AIR TEMPERATURE

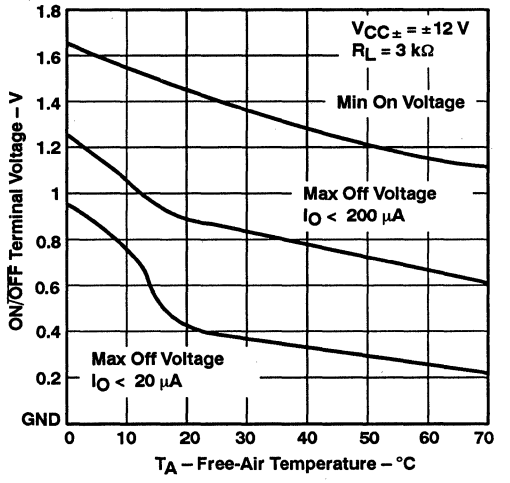


Figure 2

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
FREE-AIR TEMPERATURE

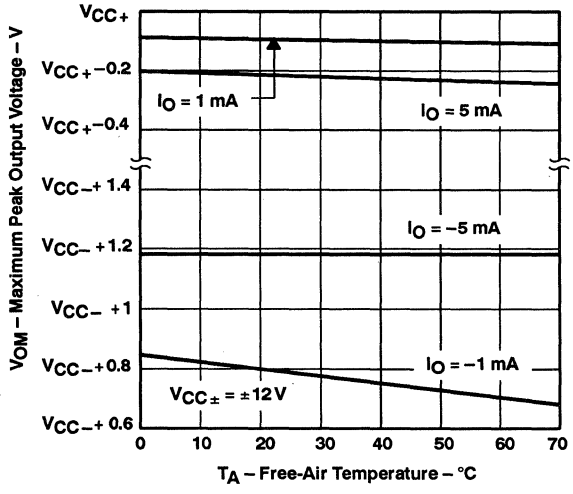


Figure 3

ON/$\overline{\text{OFF}}$ TERMINAL CURRENT
vs
ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE

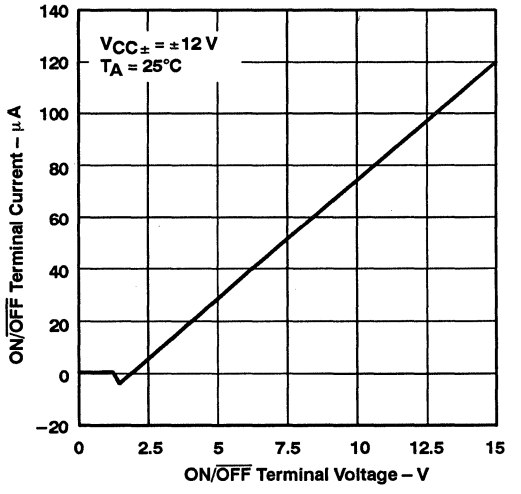


Figure 4

TYPICAL CHARACTERISTICS

OUTPUT CURRENT LIMIT
vs
FREE-AIR TEMPERATURE

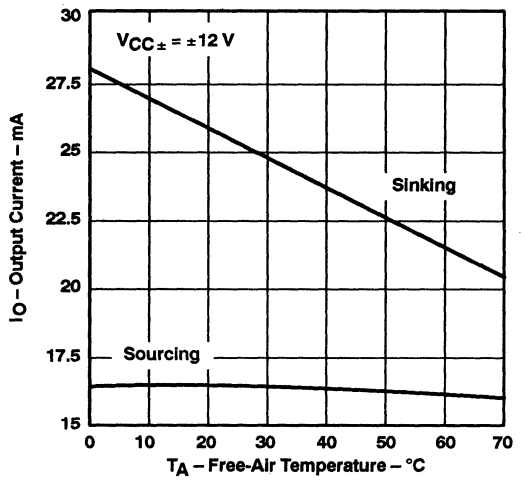


Figure 5

OFF-STATE OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

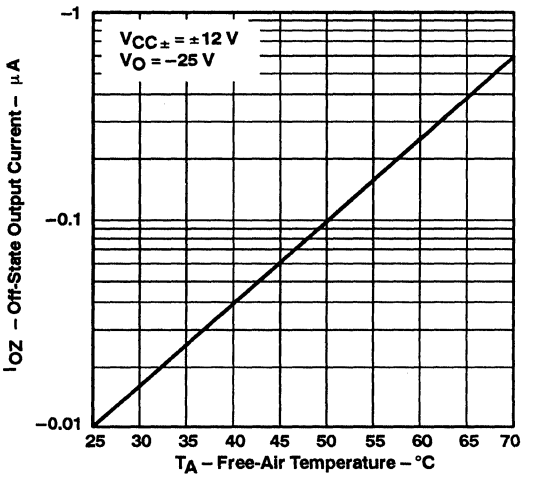


Figure 6

OFF-STATE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

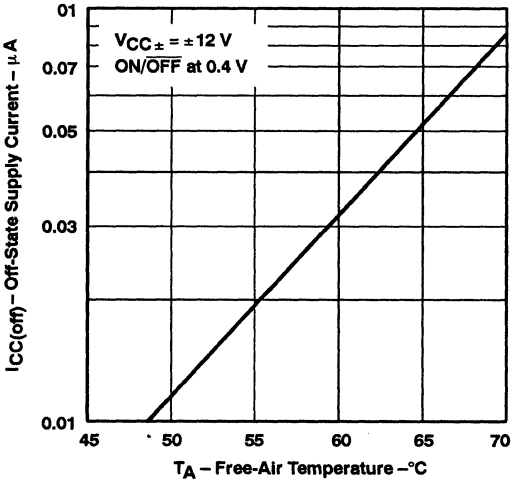


Figure 7

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

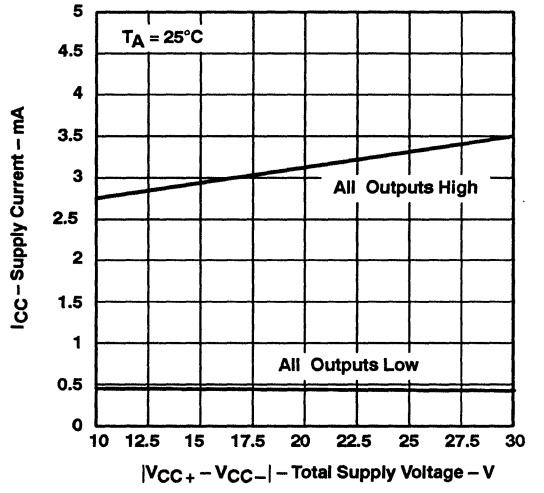


Figure 8

TYPICAL CHARACTERISTICS

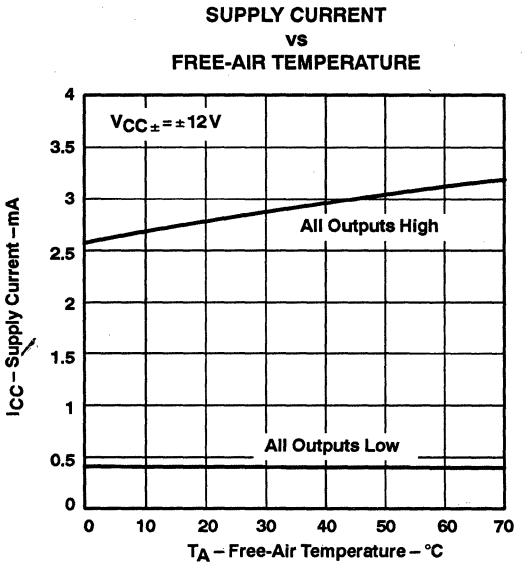


Figure 9

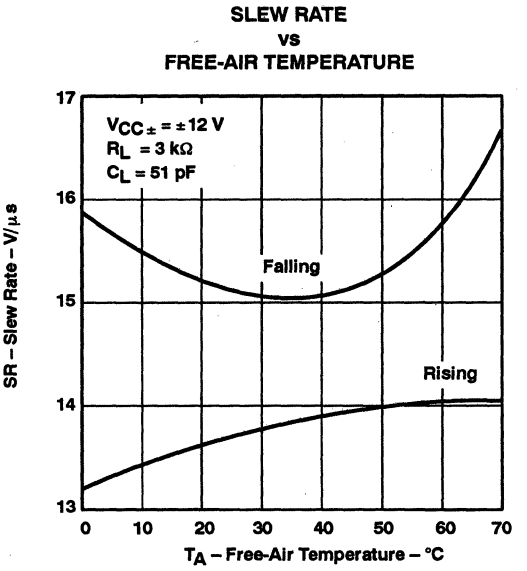


Figure 10

APPLICATION INFORMATION

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030C will draw high current from V_{CC+} to GND if V_{CC-} is open circuited or pulled above ground. If this is possible, connecting a diode from V_{CC-} to GND will prevent the high-current state. Any low-cost diode can be used (see Figure 11).

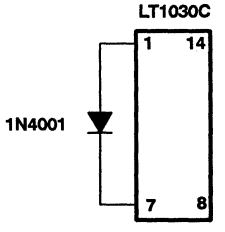
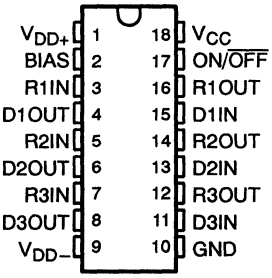


Figure 11. Connecting a Diode From V_{CC-} to GND

SLLS105B – D3627, FEBRUARY 1991 – REVISED JANUARY 1992

- **Meets All EIA-232-D (Revision of RS-232-C) Specifications**
- **Three Independent Drivers and Receivers Per Package**
- **EIA-232 Inputs and Outputs Withstand ±30 V**
- **3-State Outputs**
- **All Outputs Are Short-Circuit Protected**
- **Virtually Zero Supply Current When Shutdown**
- **Output of Several Devices Can Be Paralleled**
- **Operates From ±5-V to ±15-V Supplies**
- **Designed to Be Interchangeable With Linear Technology LT1039**

DW OR N PACKAGE
(TOP VIEW)



description

The LT1039 is a triple EIA-232 line transceiver designed to meet the requirements of Standard EIA-232-D. All outputs are fully protected against an overload or short to ground. A major advantage of the LT1039 is high-impedance output states when the device is off or powered down. This feature allows several different devices to be connected together on the same bus.

The bias pin provides a receiver to be kept alive when the LT1039 is shutdown (ON/$\overline{\text{OFF}}$ = low).

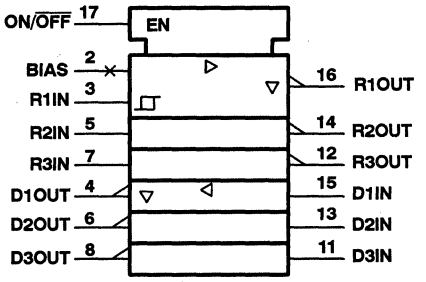
The LT1039 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	LT1039CDW	LT1039CN

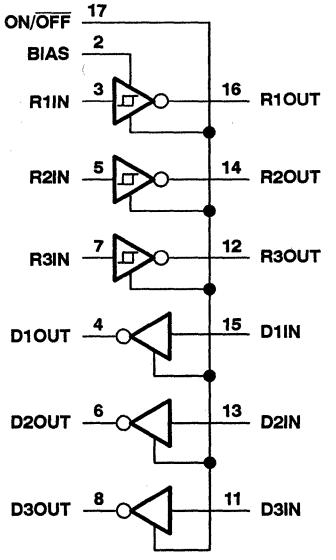
The DW package is available taped and reeled. Add the suffix R to the device type (i.e., LT1039CDWR).

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
BIAS	2	Keeps receiver 1 alive while the LT1039 is in the shutdown mode. Leave BIAS open when not in use.
D1IN, D2IN, D3IN	15, 13, 11	Line driver inputs. Operate properly on TTL or CMOS levels. Output valid from $V_I = (V_{DD-}) + (2 \text{ to } 15 \text{ V})$. Connect to 5 V when not used.
D1OUT, D2OUT, D3OUT	4, 6, 8	Line driver outputs
GND	10	Ground
ON/$\overline{\text{OFF}}$	17	Shuts down entire circuit. Cannot be left open. If V_{IL} is at or near 0.8 V, significant settling time may be required.
R1IN, R2IN, R3IN	3, 5, 7	Receiver inputs. Input impedance is normally 30 kΩ. Accepts EIA-232 voltage levels and has 0.4 V of hysteresis to provide noise immunity.
R1OUT, R2OUT, R3OUT	16, 14, 12	Receiver outputs with TTL/CMOS voltage levels
V_{DD+}	1	Positive supply voltage for driver
V_{DD-}	9	Negative supply voltage for driver
V_{CC}	18	5-V supply voltage for receivers

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD+} (see Note 1) ..... 0 V to 15 V
Supply voltage range, V_{DD-} ..... 0 V to −15 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range, driver input ..... V_{DD-} to 25 V
receiver input ..... ±30 V
Input voltage range, ON/$\overline{\text{OFF}}$ ..... 0 V to 12 V
Output voltage range, driver output ..... V_{DD+} −30 V to V_{DD-} + 30 V
Duration of output short circuit at (or below) T_A = 25°C (to ±30 V, see Note 2) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the GND terminal.
2. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD+}	5	12	15	V
Supply voltage, V_{DD-}	−5	−12	−15	V
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH} (see Note 3)	2			V
Low-level input voltage, V_{IL} (see Note 3)			0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 3: V_{IH} and V_{IL} specifications apply only for inputs D1IN to D3IN.

DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, $V_{DD\pm}$ = ±11.4 V to ±12.6 V, ON/$\overline{OFF}$ at 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	Load = 3 kΩ to GND	V_{DD+} −0.4	V_{DD+} −0.4		V
V_{OM-}	Maximum negative peak output voltage swing			V_{DD-} +1.0	V_{DD-} +1.5	
I_{IH}	High-level input current	$V_I \geq 2$ V		1	20	µA
I_{IL}	Low-level input current	$V_I \leq 0.8$ V		5	20	µA
		V_I = 0			15	
		V_I = 5 V			80	
		Sourcing current, V_O = 0	5	15		
		Sinking current, V_O = 0	−5	−15		
I_{OZ}	Off-state output current	V_O = ±18 V, V_I = 0, ON/$\overline{OFF}$ at 0.4 V		±10	±200	µA
I_{CC}	Supply current	I_O = 0		4	8	mA
$I_{CC(off)}$	Off-state supply current	ON/$\overline{OFF}$ at 0.4 V		1	100	µA
SR	Slew rate	R_L = 3 kΩ, C_L = 51 pF	4	15	30	V/µs

† All typical values are at $V_{DD\pm}$ = ±12 V, T_A = 25°C.

RECEIVER SECTION

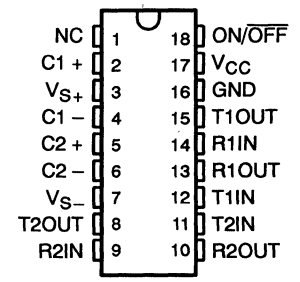
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, ON/$\overline{\text{OFF}}$ at 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T-}	Negative-going input threshold voltage				0.5	1.3		V
V_{T+}	Positive-going input threshold voltage					1.7	2.8	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				0.1	0.4	1	V
V_{OL}	Low-level output voltage	I_O = −1.6 mA				0.4	0.5	V
V_{OH}	High-level output voltage	I_O = 160 μA			3.5	4.8		V
I_{OS}	Short-circuit output current	Sinking current,	$V_O = V_{CC}$		−10			mA
		Sourcing current,	V_O = 0		0.5	1		
I_{OZ}	Off-state (high-impedance state) output current	V_O = 0 to V_{CC},	V_I = 0,	ON/$\overline{\text{OFF}}$ at 0.4 V		±1	±10	μA
I_{CC}	Supply current	I_O = 0				4	7	mA
$I_{CC(off)}$	Off-state supply current	ON/$\overline{\text{OFF}}$ at 0.4 V				1	100	μA

† All typical values ground are at V_{CC} = 5 V, T_A = 25°C.

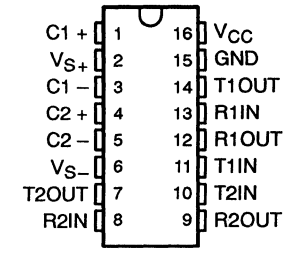
- **Operates With Single 5-V Power Supply**
- **Generates ±9-V Supply Voltages With Only 1-μF Capacitors**
- **Designed to Avoid Latch-Up**
- **CMOS Comparable Low Power . . . 60 mW**
- **Features Superior to CMOS:**
  - **Improved Speed . . . Operates Over 64K Baud**
  - **Improved Protection . . . Outputs Can Be Forced to ±30 V Without Damage**
  - **3-State Outputs Are at High Impedance When Off**
- **Power Additional EIA-232 Drivers . . . 10 mA**
- **1-μA Supply Current in Shutdown**
- **Available With or Without Shutdown**
- **Suitable for ANSI/EIA-232-D-1986 Applications (Revision of EIA Std RS-232-C)**
- **Designed to Be Interchangeable With Linear Technology LT1080 and LT1081**

LT1080C, LT1080I . . . DW OR N PACKAGE
(TOP VIEW)



NC – No internal connection

LT1081C, LT1081I . . . DW OR N PACKAGE
(TOP VIEW)



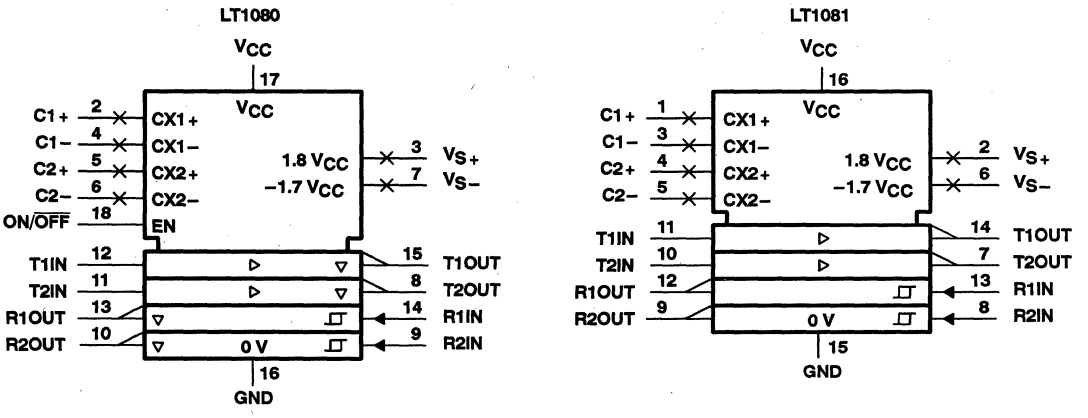
description

The LT1080 and LT1081 are dual driver/receivers that include a charge pump to supply EIA-232 voltage levels from a single 5-V supply. These interface-optimized devices are designed to avoid latch-up and provide a realistic balance between CMOS levels of power dissipation and real-world requirements for ruggedness. The driver outputs are fully protected against overload and can be shorted to ±30 V. Unlike CMOS devices, the advanced architecture of the LT1080 and LT1081 does not load the signal line when shut down or when the power is off. Both the receiver and EIA-232 outputs are put into a high-impedance state. An advanced output stage allows driving higher capacitive loads at higher speeds with exceptional resistance to ESD.

Applications for these devices include portable computers, battery-powered EIA-232 systems, power-supply generators, terminals, and modems.

The LT1080C and LT1081C are characterized for operation from 0°C to 70°C. The LT1080I and LT1081I are characterized for operation from –40°C to 85°C.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Terminal Functions

PIN NAME	PIN NO.†	I/O	DESCRIPTION
C1+ C1–	2 [1] 4 [3]		External capacitor C1
C2+ C2–	5 [4] 6 [5]		External capacitor C2
GND	16 [15]		Ground pin
ON/$\overline{\text{OFF}}$	18	I	Controls the operation mode and is TTL/CMOS compatible. A low logic level places the device in the shutdown mode, which reduces input supply current to near zero and places both driver and receiver outputs in a high-impedance state. This input is not available on the LT1081.
R1IN	14 [13]	I	Receiver input. Accepts EIA-232 voltage levels (±30 V) and has hysteresis to provide noise immunity.
R2IN	9 [8]	I	Same as R1IN
R1OUT	13 [12]	O	Receiver output with TTL/CMOS voltage levels. Output is in a high-impedance state when in the shutdown mode or when V_{CC} = 0 to allow bus operation. Fully short-circuit protected to GND or V_{CC} with power on, power off, or in the shutdown mode.
R2OUT	10 [9]	O	Same as R1OUT
T1IN	12 [11]	I	EIA-232 driver input pin. Input is TTL/CMOS compatible. Unused inputs should be tied to V_{CC}.
T2IN	11 [10]	I	Same as T1IN
T1OUT	15 [14]	O	Driver output with EIA-232 voltage levels. Outputs are in a high-impedance state when in the shutdown mode or when V_{CC} = 0 to allow bus operation. Fully short-circuit protected to GND or V_{CC} with power on, power off, or in the shutdown mode.
T2OUT	8 [7]	O	Same as T1OUT
V_{S+}	3 [2]		Positive supply for EIA-232 drivers. Requires an external capacitor (1-μF) for charge storage.
V_{S-}	7 [6]		Negative supply for EIA-232 drivers. Requires an external capacitor (1-μF) for charge storage.
V_{CC}	17 [16]		Input supply pin. Supply current drops to near zero in the shutdown mode. Driver and receiver outputs are in a high-impedance state when V_{CC} = 0.

† Pin numbers in brackets are for the LT1081.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Positive output supply voltage ..... 12 V
Negative output supply voltage ..... −12 V
Input voltage range: Driver ..... ±12 V
Receiver ..... ±30 V
ON/$\overline{OFF}$ ..... GND to 12 V
Output voltage range: T1OUT, T2OUT ..... V_{S-} + 30 V to V_{S+} − 30 V
R1OUT, R2OUT ..... −0.3 V to V_{CC} + 0.3 V
Duration of output short circuit at (or below) 25°C: V_{S+} ..... 30 s
V_{S-} ..... 30 s
Driver or receiver output ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: LT1080C, LT1081C ..... 0°C to 70°C
LT1080I, LT1081I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	LT1080C, LT1081C			LT1080I, LT1081I			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High-level input voltage, V_{IH} (T1IN, T2IN)	2		5.5	2		5.5	V
Low-level input voltage, V_{IL} (T1IN, T2IN)			0.8			0.8	V
Operating free-air temperature, T_A	0		70	−40		85	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, V_I = 3 V (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OM+}	Positive-peak output voltage	R_L = 3 kΩ to GND			5	7.5		V
V_{OM-}	Negative-peak output voltage	R_L = 3 kΩ to GND			−5	−6.5		V
I_{IH}	High-level input current	V_I = 2 V to 5.5 V				5	20	μA
I_{IL}	Low-level input current	V_I ≤ 0.8 V				−5	−20	μA
I_{OHS}	Output short-circuit current (sourcing)	V_I = 0,	V_O = 0,	T_A = 25°C	−7	12		mA
I_{OLS}	Output short-circuit current (sinking)	V_I = 2 V,	V_O = 0,	T_A = 25°C	7	−12		mA
I_{OZ}	High-impedance output current	Shutdown mode,	V_O = ±30 V				100	μA

receiver section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage		LT1080C, LT1081C		1.7	2.4	V
			LT1080I, LT1081I		1.7	3	
V_{T-}	Negative-going input threshold voltage		LT1080C, LT1081C	0.8	1.3		V
			LT1080I, LT1081I	0.2	1.3		
V_{hys}	Input hysteresis			0.1	0.4	1	V
r_i	Input resistance	T_A = 25°C		3	5	7	kΩ
V_{OH}	High-level output voltage	I_{OH} = −160 μA,	V_{CC} = 5 V	3.5	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.2	0.4	V
I_{OSH}	Output short-circuit current (sourcing)	V_I = 3 V,	V_O = 0, T_A = 25°C	−0.6	−1		mA
I_{OSL}	Output short-circuit current (sinking)	V_I = 3 V,	V_O = V_{CC}, T_A = 25°C	10	20		mA
I_{OZ}	High-impedance output current	Shutdown mode,	V_O = 0 to V_{CC}			10	μA

power supply section, V_{CC} = 5 V, driver outputs low (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{S+}	Supply output voltage	I_S = 0,	T_A = 25°C	8	9		V
		I_S = 10 mA,	T_A = 25°C	7	8		
		I_S = 15 mA,	T_A = 25°C	6.5	7.5		
V_{S-}	Supply output voltage	I_S = 0,	T_A = 25°C	−7.5	−8.5		V
		I_S = 10 mA,	T_A = 25°C	−5.5	−6.5		
		I_S = 15 mA,	T_A = 25°C	−5	−6		
I_{CC}	Supply current				10	22	mA
$I_{CC(off)}$	Off-state supply current (LT1080)	ON/$\overline{OFF}$ at 0.4 V				100	μA
I_I	Input current (ON/OFF) (LT1080)	V_I = 5 V				80	μA
		V_I = 0 V				−15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

operating characteristics over recommended range of supply voltage, V_I = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ,	C_L = 560 pF,	See Note 2	4	15	30	V/μs
$t_{r(supply)}$	Supply rise time (see Note 3)	C1–C4 = 1 μF				1		ms

NOTES: 2. Meets EIA-232-D specifications for capacitive loads greater than 560 pF.
3. Time from either shutdown input ON/$\overline{OFF}$ (LT1080) goes active high or V_{CC} power on (LT1081) until the output voltages reach V_{S+} ≥ 6 V and V_{S-} ≤ −6 V.

TYPICAL CHARACTERISTICS†

HIGH- AND LOW-LEVEL
DRIVER OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

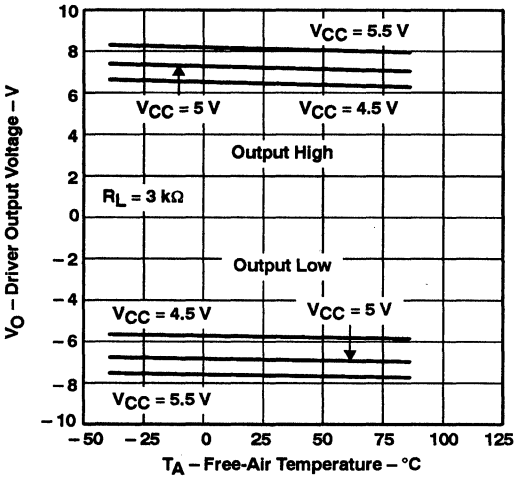


Figure 1

HIGH-IMPEDANCE
DRIVER OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

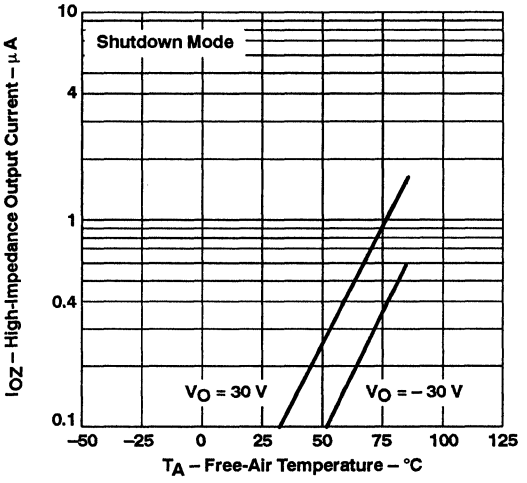


Figure 2

POSITIVE-GOING AND NEGATIVE-GOING
RECEIVER INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

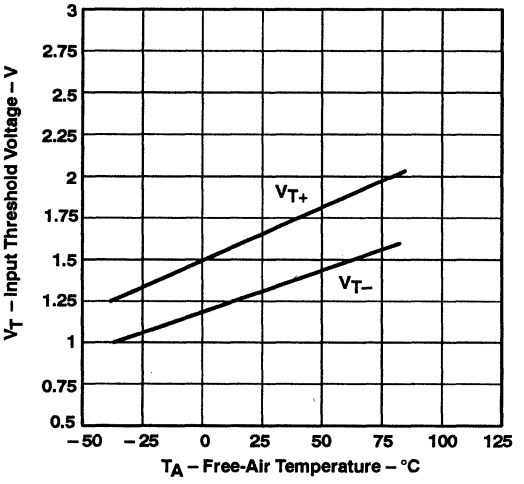


Figure 3

RECEIVER SOURCE CURRENT
AND SINK CURRENT
vs
FREE-AIR TEMPERATURE

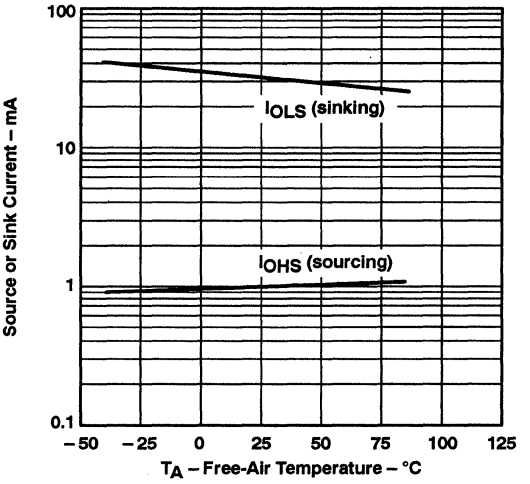


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY OUTPUT VOLTAGE vs OUTPUT CURRENT

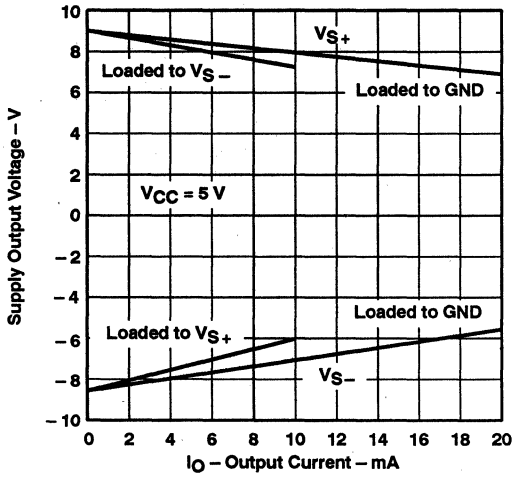


Figure 5

SUPPLY OUTPUT VOLTAGE vs ELAPSED TIME

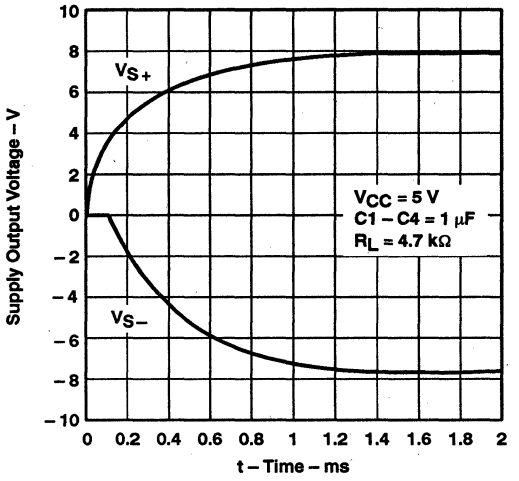


Figure 6

ON/$\overline{\text{OFF}}$ INPUT CURRENT vs INPUT VOLTAGE

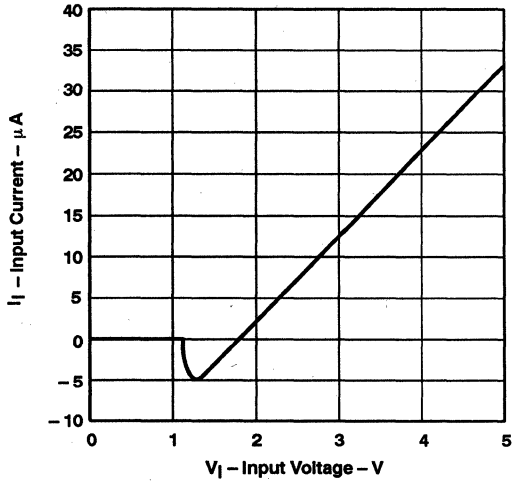


Figure 7

ON/$\overline{\text{OFF}}$ INPUT VOLTAGE vs FREE-AIR TEMPERATURE

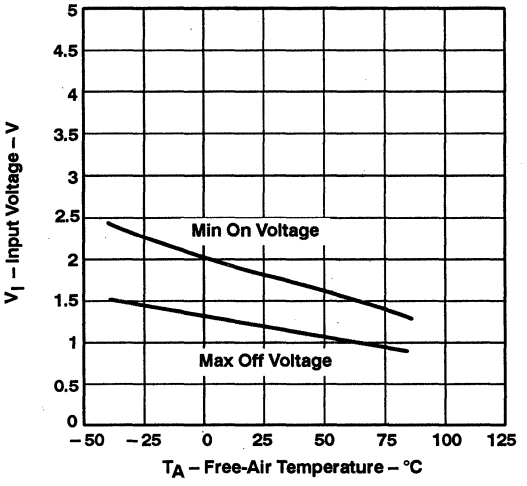


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OFF-STATE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

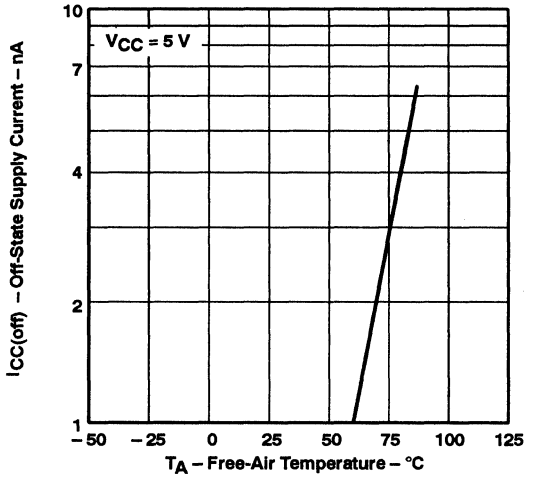


Figure 9

DRIVER and RECEIVER PULSE RESPONSE

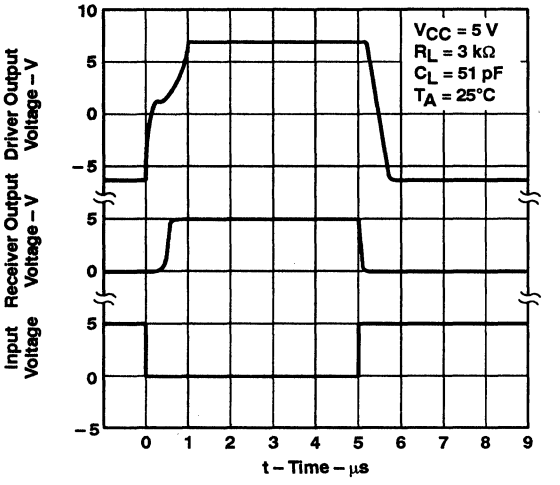


Figure 10

ON/$\overline{OFF}$ TO DRIVER OUTPUT PULSE RESPONSE

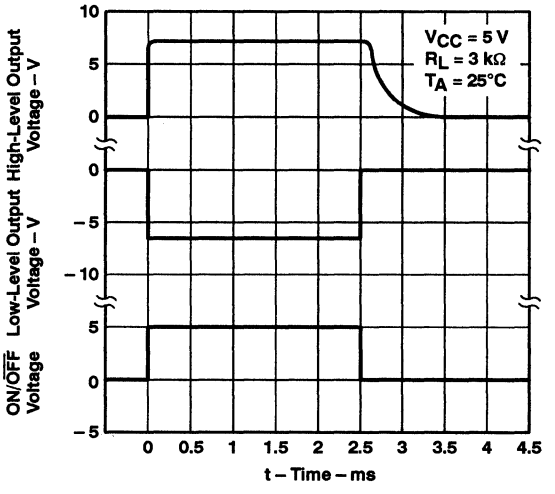


Figure 11

ON/$\overline{OFF}$ TO RECEIVER PULSE RESPONSE

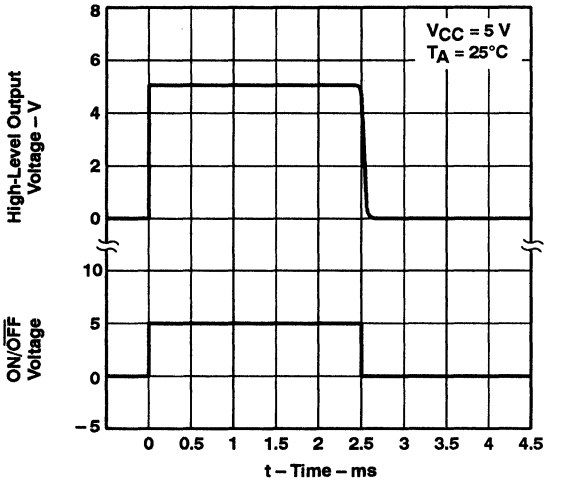


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

The driver output stage of the LT1080 offers significantly improved protection over older bipolar and CMOS designs (see Figures 13 and 14). In addition to limiting current, the driver output can be externally forced to ±30 V without damage, excessive current flow, or supply disruption. Some drivers have diodes connected between the outputs and the supplies, allowing externally applied voltages to cause excessive supply voltage to develop.

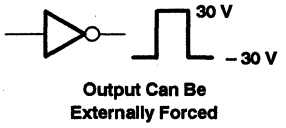


Figure 13. LT1080/LT1081 Driver

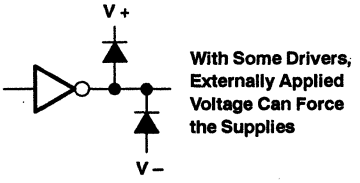


Figure 14. Older EIA-232 Drivers and CMOS Drivers

Placing the LT1080 in the shutdown mode (pin 18 low) puts both the driver and receiver outputs in a high-impedance state. This allows for bus operation and transceiver applications (see Figures 15–17). The shutdown mode also drops input supply current (V_{CC}) to near zero for power-conscious systems.

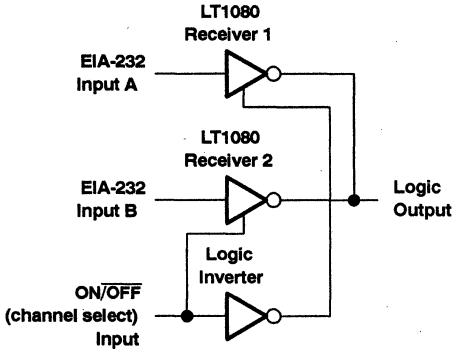


Figure 15. Sharing a Receiver Line

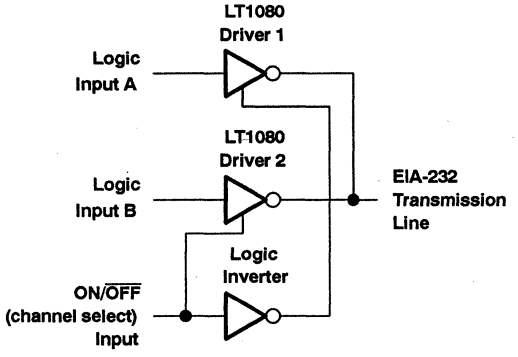


Figure 16. Sharing a Transmitter Line

APPLICATION INFORMATION

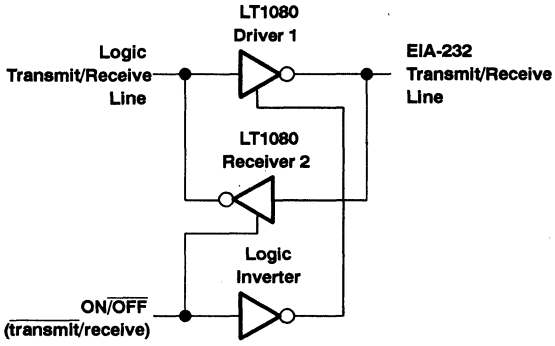
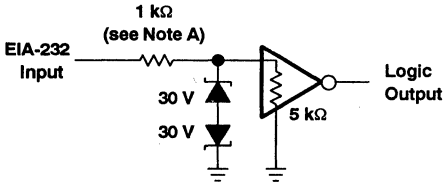


Figure 17. Transceiver

To protect against receiver input overloads in excess of ±30 V, a voltage clamp can be placed on the data line and still maintain EIA-232 compatibility (see Figure 18).

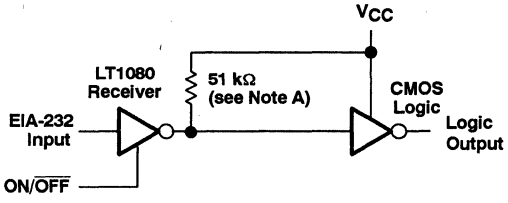
When driving CMOS logic from a receiver that will be used in the shutdown mode and when there is no other active receiver on the line, a 51-kΩ resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high-impedance state (see Figure 19).

The generated driver supplies (V_{S+} and V_{S-}) may be used to power external circuitry such as other EIA-232 drivers or operational amplifiers (see Figure 20). They should be loaded with care, since excessive loading can cause the generated supply voltages to drop, causing the EIA-232 driver output voltages to fall below EIA-232 requirements. See Figure 5 for a comparison of generated supply voltage versus supply current.



NOTE A: A PTC thermistor will allow continuous overload of greater than ± 100 V.

Figure 18. Input Overload Protection



NOTE A: Forces logic input state when V_I is low.

Figure 19. Forcing a Definite Logic Level

APPLICATION INFORMATION

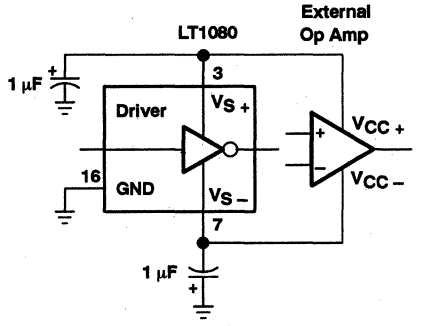
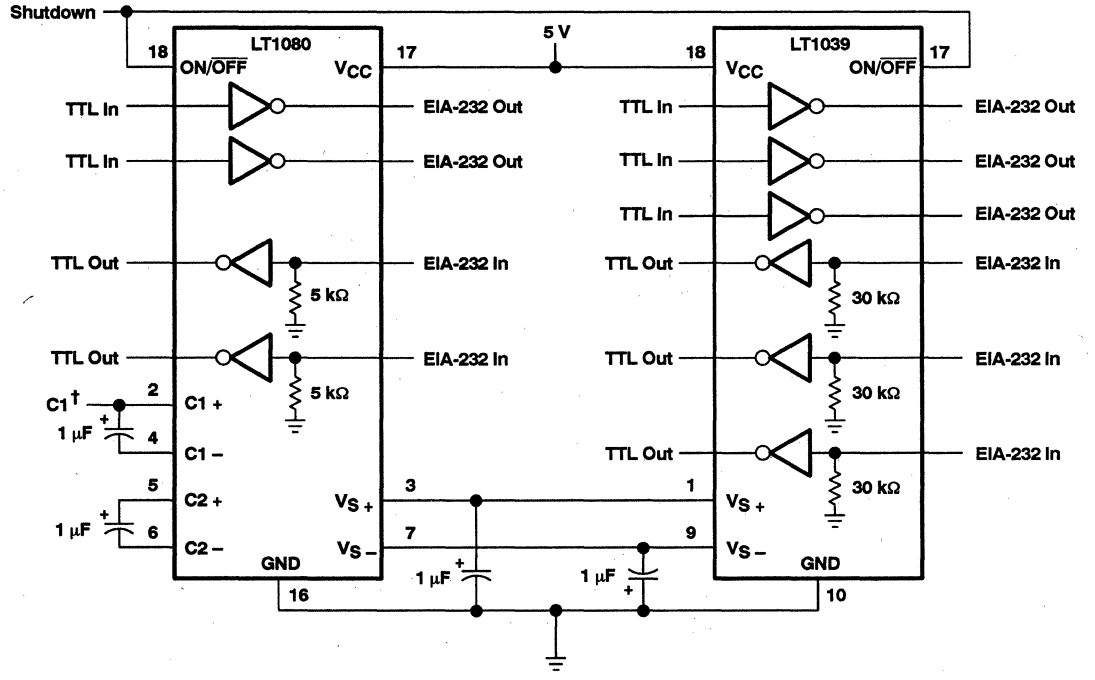


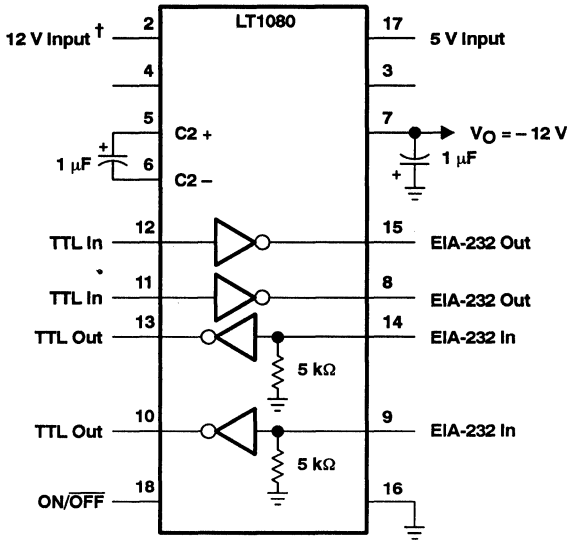
Figure 20. Powering External Circuitry



† In applications in which a separate second positive supply is available (such as 5 V and 12 V), the 12-V supply may be connected to pin 2 and C1 deleted. The power circuitry will then invert the 12-V supply. The 5-V supply is still needed to power the biasing circuitry and receivers.

Figure 21. Supporting an LT1039 (Triple Driver/Receiver)

APPLICATION INFORMATION

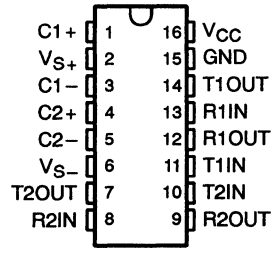


† C1 + used on LT1081

Figure 22. Operating With 5 V and 12 V

- **Operates With Single 5-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Two Drivers and Two Receivers**
- **±30-V Input Levels**
- **Low Supply Current . . . 8 mA Typ**
- **Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Standard RS-232-C)**
- **Designed to be Interchangeable With Maxim MAX232**
- **Applications**
  - **EIA-232 Interface**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**
- **ESO Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**

D, DW, OR N PACKAGE
(TOP VIEW)

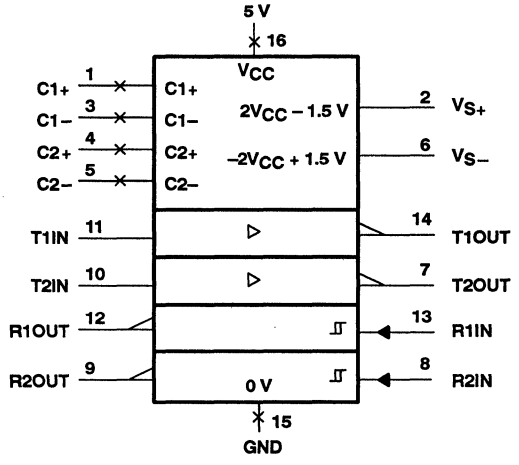


description

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

The MAX232 is characterized for operation from 0°C to 70°C. The MAX232I is characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 6 V
Positive output supply voltage range, V_{S+} . . . . . V_{CC} −0.3 V to 15 V
Negative output supply voltage range, V_{S-} . . . . . −0.3 V to −15 V
Input voltage range: Driver . . . . . −0.3 V to V_{CC} + 0.3 V
Receiver . . . . . ±30 V
Output voltage range: T1OUT, T2OUT . . . . . V_{S-} −0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT . . . . . −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT . . . . . unlimited
Operating free-air temperature range: MAX232 . . . . . 0°C to 70°C
MAX232I . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH} (T1IN,T2IN)	2			V
Low-level input voltage, V_{IL} (T1IN, T2IN)			0.8	V
Receiver input voltage, R1IN, R2IN			±30	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND		5	7		V
		R1OUT, R2OUT	I_{OH} = −1 mA		3.5			
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND			−7	−5	V
		R1OUT, R2OUT	I_{OL} = 3.2 mA				0.4	
V_{T+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{T-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis	R1IN, R2IN	V_{CC} = 5 V		0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5,	T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	T1OUT, T2OUT	$V_{S+} = V_{S-} = 0$,	V_O = ± 2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0				200	µA
I_{CC}	Supply current		V_{CC} = 5.5 V, T_A = 25°C	All outputs open,		8	10	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low-to-high-level output	See Figure 2			500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high-to-low-level output	See Figure 2			500		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ,	See Figure 3			30	V/µs
SR(tr)	Driver transition region slew rate	See Figure 4			3		V/µs

APPLICATION INFORMATION

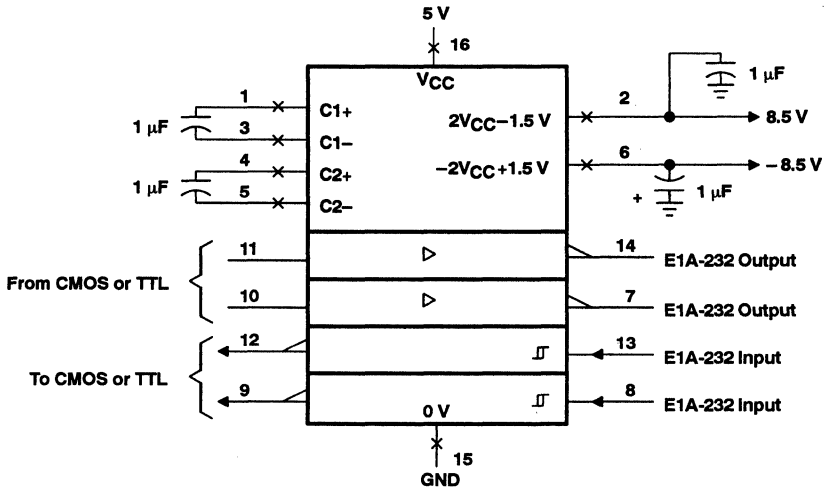
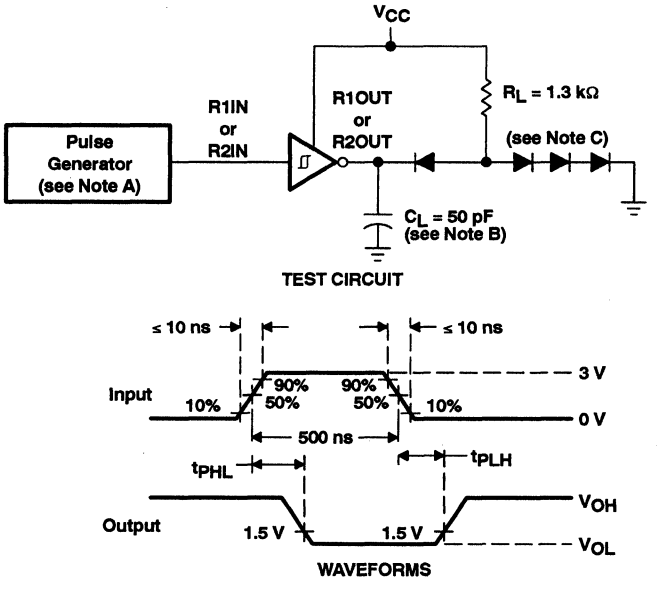


Figure 1. Typical Operating Circuit

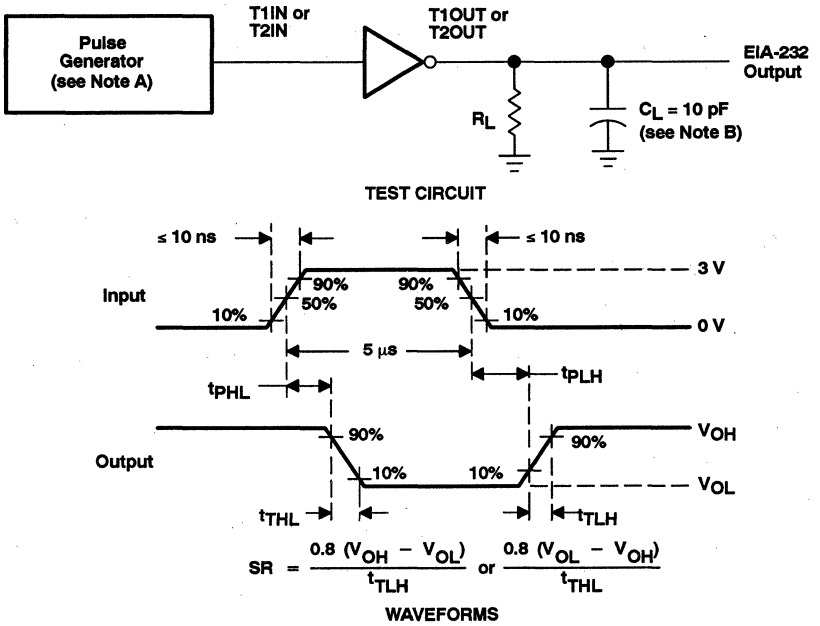
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

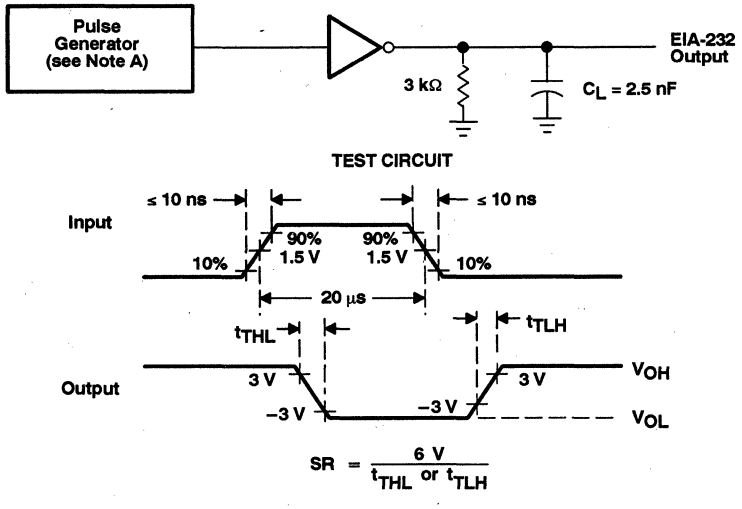
Figure 2. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5-μs input)



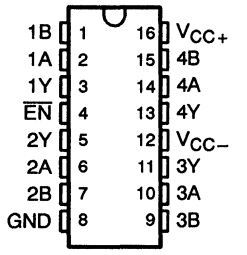
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 4. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20-μs input)

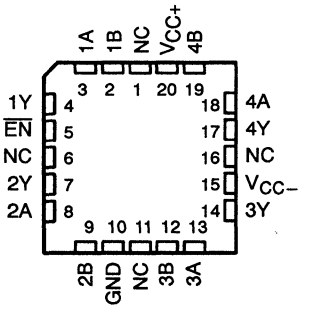
SLLS012B – D3006, FEBRUARY 1986 – REVISED FEBRUARY 1993

- **Four Independent Receivers With Common Enable Input**
- **High Input Sensitivity . . . 25 mV Max**
- **High Input Impedance**
- **MC3450 and MC3550 Have 3-State Outputs**
- **MC3452 Has Open-Collector Outputs**
- **Glitch-Free Power-Up/Power-Down Operation**

MC3450, MC3452 . . . D OR N PACKAGE
MC3550, MC3552 . . . J PACKAGE
(TOP VIEW)



MC3550, MC3552 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

THE MC3452 IS NOT RECOMMENDED FOR NEW DESIGN

description

The MC3450, MC3550, MC3452, and MC3552 are quad differential line receivers designed for use in balanced and unbalanced digital data transmission. The MC34/3550 and MC34/3552 are the same except that the MC3450 and MC3550 have 3-state outputs whereas the MC3452 and MC3552 have open-collector outputs, which permit the wire-AND function with similar output devices. The 3-state and open-collector outputs permit connection directly to a bus-organized system.

The MC3450, MC3550, MC3452, and MC3550 are designed for optimum performance when used with either the MC3453 or MC3553 quad differential line driver or SN75109A, SN75110A, and SN75112 dual differential drivers.

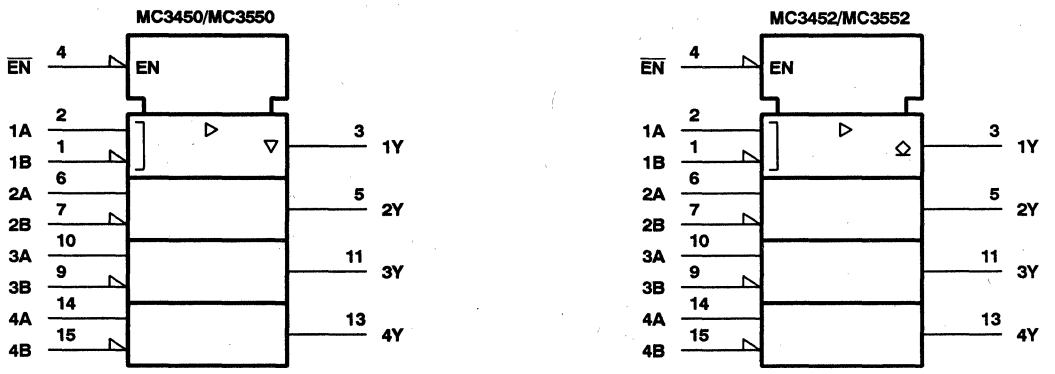
The MC3450 and MC3452 are characterized for operation from 0°C to 70°C. The MC3550 and MC3552 are characterized for operation over the full military temperature range of −55°C to 125°C.

FUNCTION TABLE

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{EN}$	OUTPUT Y
$V_{ID} \geq 25$ mV	L	H
-25 mV $< V_{ID} < 25$ mV	L	?
$V_{ID} \leq 25$ mV	L	L
X	H	Z

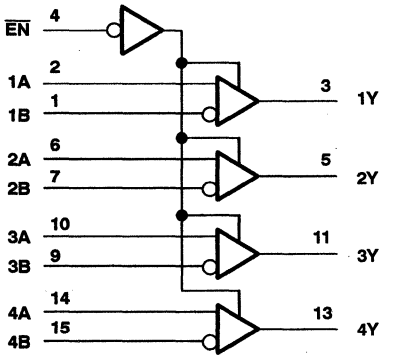
H = high level, L = low level, ? = indeterminate,
X = impedance (off)

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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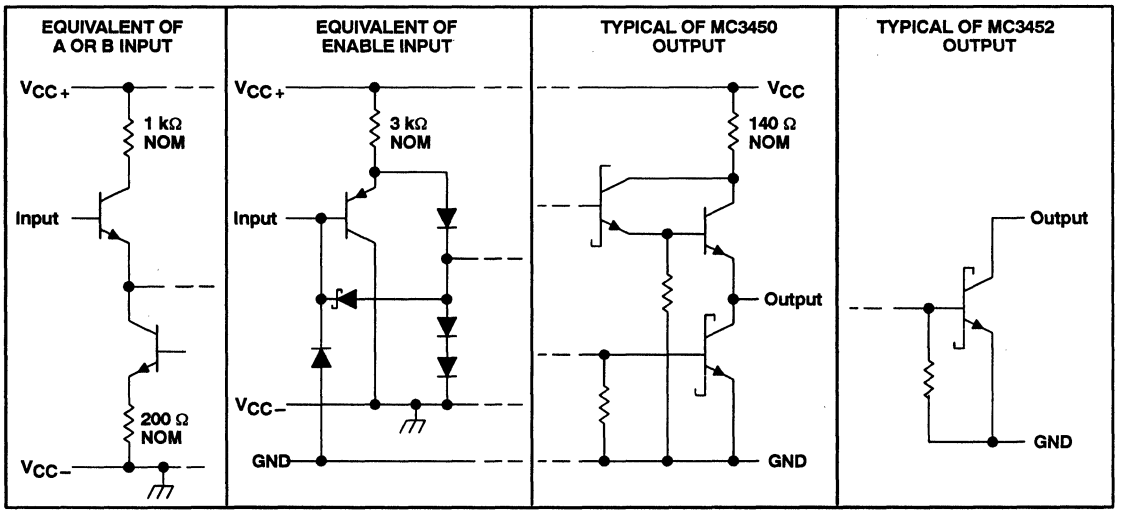
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 7 V
Supply voltage, V_{CC-} ..... –7 V
Differential input voltage (see Note 2) ..... ±6 V
Common-mode input voltage (see Note 3) ..... ±5 V
Enable input voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	$T_A \geq 25°C$	4.5	5	5.5	V
	$T_A < 25°C$	4.75	5	5.5	
Supply voltage, V_{CC-}	$T_A \geq 25°C$	−4.5	−5	−5.5	V
	$T_A < 25°C$	−4.75	−5	−5.5	
High-level enable input voltage, V_{IH}		2			V
Low-level enable input voltage, V_{IL}				0.8	V
Low-level output current, I_{OL}				−16	mA
Differential input voltage, V_{ID} (see Note 4)		−5†		5	V
Common-mode input voltage, V_{IC} (see Note 4)		−3†		3	V
Input voltage range, any different input to GND		−5†		3	V
Operating free-air temperature, T_A	MC3450, MC3452	0		70	°C
	MC3550, MC3552	−55		125	

† The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

NOTE 4: The recommended combinations of input voltages fall within the shaded area of Figure 1.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES

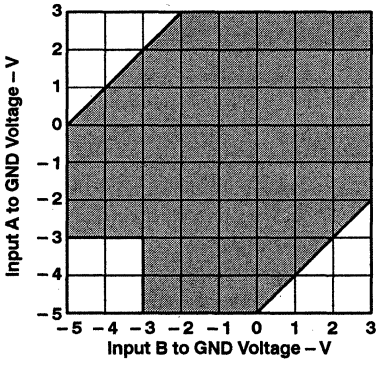


Figure 1

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = MAX (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MC3450, MC3550			MC3452, MC3552			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ±4.75 V, V_{ID} = 25 mV, $\overline{EN}$ at 0.8 V, I_{OH} = −400 µA, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ±4.75 V, V_{ID} = −25 mV, $\overline{EN}$ at 2 V, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V			0.5			0.5	V
I_{OH}	High-level output current		$V_{CC\pm}$ = ±4.75 V, V_{OH} = 5.25 V						250	µA
I_{IH}	High-level input current	A inputs	V_{ID} = −2 V		30	75		30	75	µA
		B inputs	V_{ID} = −2 V		30	75		30	75	
		$\overline{EN}$	V_{IH} = 2.4 V			40			40	µA
			V_{IH} = 5.25 V			1			1	mA
I_{IL}	Low-level input current	A inputs	V_{ID} = 2 V			−10			−10	µA
		B inputs	V_{ID} = 2 V			−10			−10	
		$\overline{EN}$	V_{IL} = 0.4 V			−1.6			−1.6	mA
I_{OZ}	High-impedance state output current		V_O = 2.4 V			40				µA
			V_O = 0.4 V			−40				
I_{OS}	Short-circuit output current‡		V_{ID} = 25 mV, V_O = 0, $\overline{EN}$ at 0.8 V	−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		A inputs at GND, B inputs at 3 V, $\overline{EN}$ at 3 V			60			60	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high					−30			−30	mA

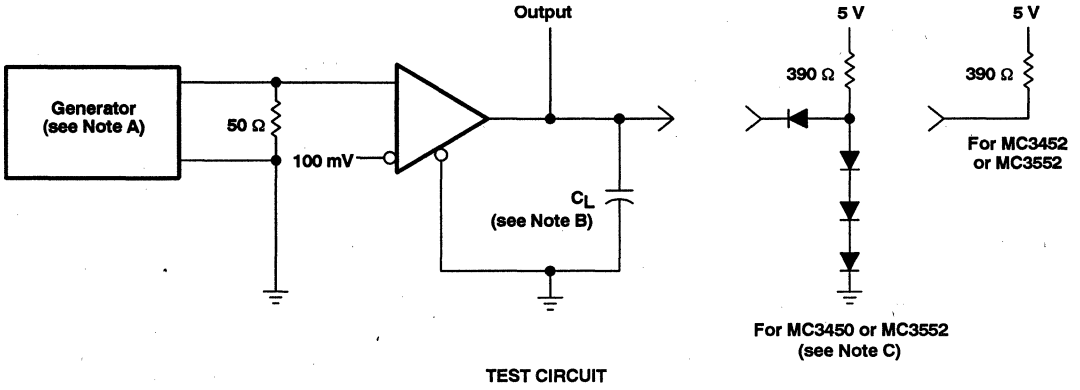
† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

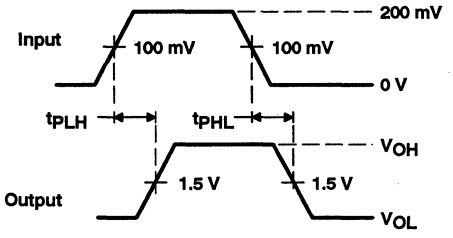
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MC3450, MC3550			MC3452, MC3552			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	A and B	Y	C_L = 50 pF, See Figure 2		17	25				ns
			C_L = 15 pF, See Figure 2					19	25	
t_{PHL}	A and B	Y	C_L = 50 pF, See Figure 2		17	25				ns
			C_L = 15 pF, See Figure 2					19	25	
t_{PZH}	$\overline{EN}$	Y	C_L = 50 pF, See Figure 2			21				ns
t_{PZL}	$\overline{EN}$	Y				27				
t_{PHZ}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 3			18				ns
t_{PLZ}	$\overline{EN}$	Y				29				
t_{PLH}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 4						25	ns
t_{PHL}	$\overline{EN}$	Y	C_L = 15 pF, See Figure 4						25	ns

† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



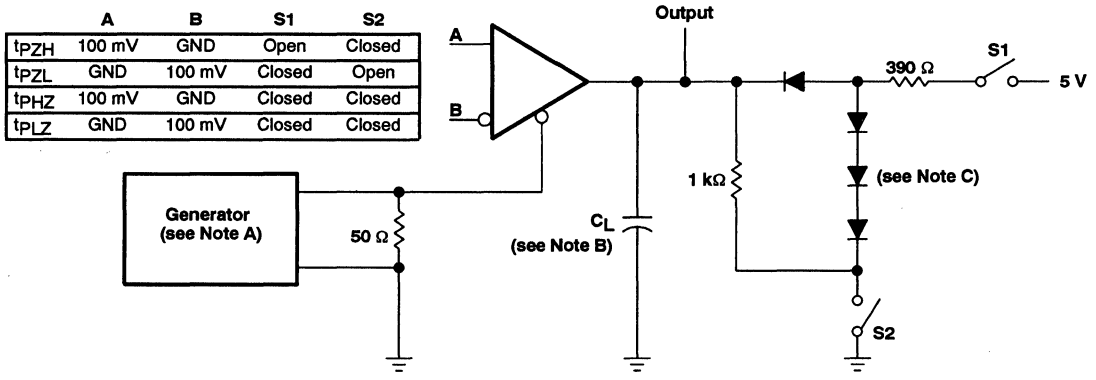
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

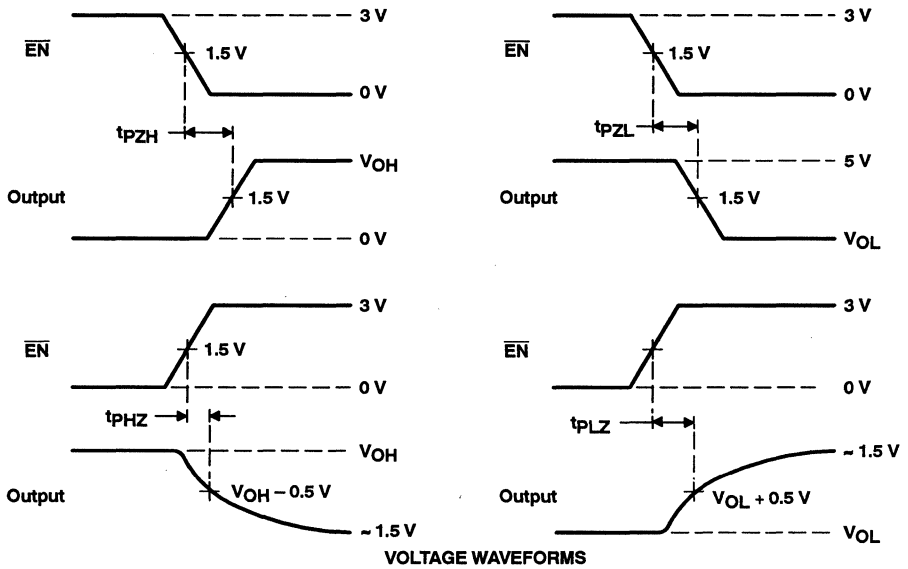
Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

	A	B	S1	S2
t_{PZH}	100 mV	GND	Open	Closed
t_{PZL}	GND	100 mV	Closed	Open
t_{PHZ}	100 mV	GND	Closed	Closed
t_{PLZ}	GND	100 mV	Closed	Closed



TEST CIRCUIT

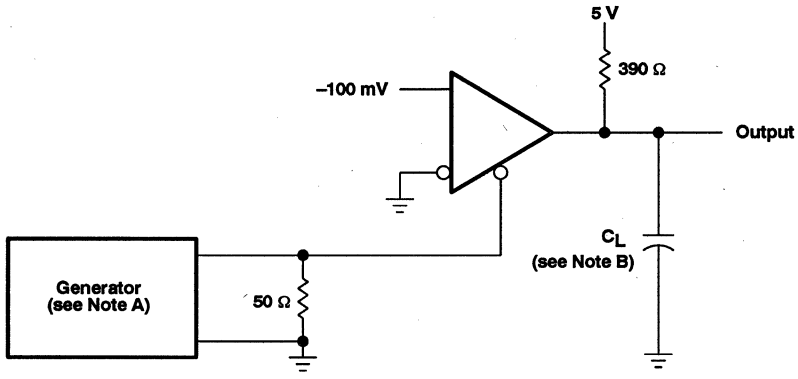


VOLTAGE WAVEFORMS

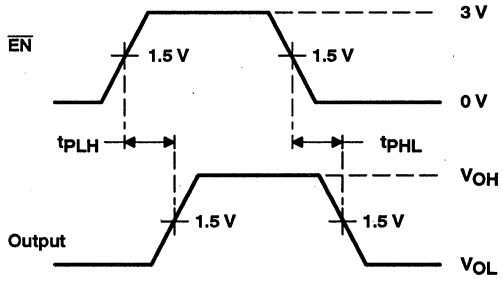
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 3. MC3450 and MC3550 Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

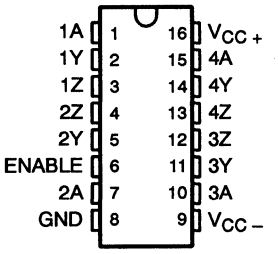
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 4. MC3452 and MC3552 Test Circuit and Voltage Waveforms

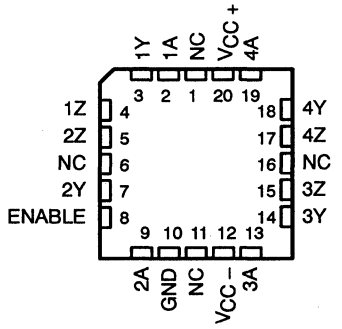
SLLS119A – D3000, FEBRUARY 1986 – REVISED FEBRUARY 1993

- **Similar to a Dual Version of SN55/75110A Line Driver**
- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range −3 V to 10 V**
- **Glitch-Free Power-Up/Power-Down Operation**
- **TTL-Input Compatibility**
- **Common-Enable Circuit**
- **Designed to Be Interchangeable With Motorola MC3453 and Military-Temperature-Range Version of MC3553**

D, J, OR N . . . PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The MC3453 and MC3553 feature four line drivers with a common-enable input. When the ENABLE input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel input. When the ENABLE is low, all channel outputs are nonconductive (transistors biased to cutoff). This minimizes loading in party-line systems where a large number of drivers share the same line.

The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltages on the line without affecting driver performance.

All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused outputs should be grounded.

FUNCTION TABLE

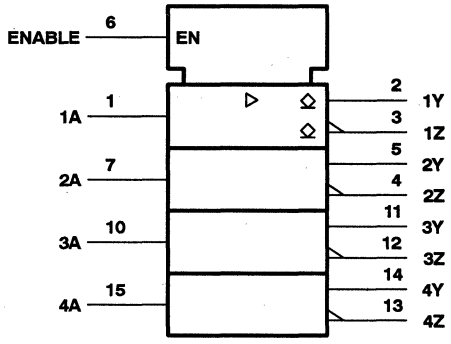
LOGIC INPUT	ENABLE INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = low logic level, H = high logic level

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400 mV of noise margin when interfaced with Series 54/74 TTL.

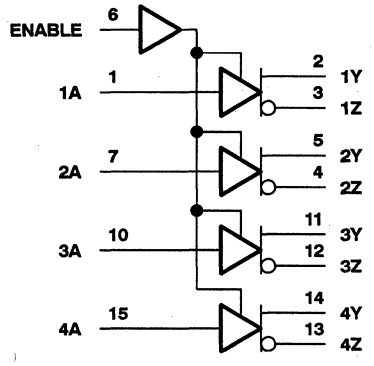
The MC3453 is characterized for operation from 0°C to 70°C. The MC3553 is characterized for operation over the full military temperature range of −55°C to 125°C.

logic symbol†

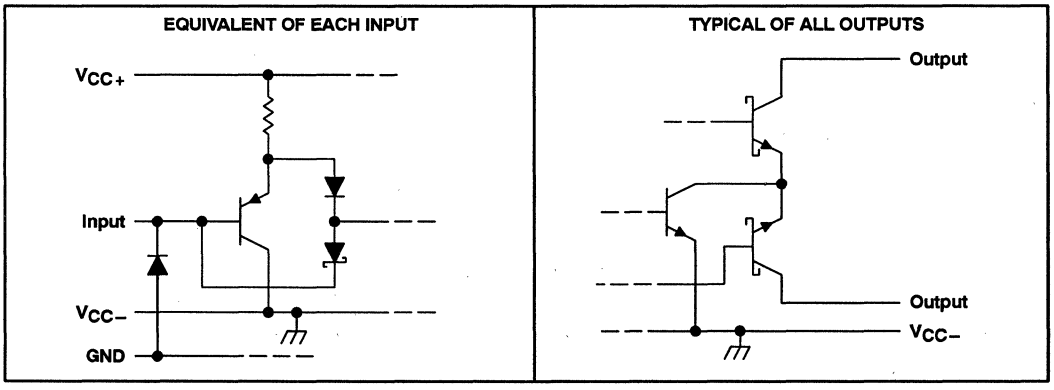


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 7 V
Supply voltage, V_{CC-} ..... –7 V
Input voltage (any input) ..... 5.5 V
Output voltage range (any output) ..... –5 V to 12 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: MC3453 ..... 0°C to 70°C
MC3553 ..... –55°C to 125°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC+}	$T_A \ge 25°C$	4.5	5	5.5	V
	$T_A < 25°C$	4.75	5	5.5	
Supply voltage, V_{CC-}	$T_A \ge 25°C$	−4.5	−5	−5.5	V
	$T_A < 25°C$	−4.75	−5	−5.5	
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		0		0.8	V
Common-mode output voltage range	V_{OCR+}	0		10	V
	V_{OCR-}	0		−3	V
Operating free-air temperature, T_A	MC3453	0		70	°C
	MC3553	−55		125	

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = MAX (unless otherwise noted)

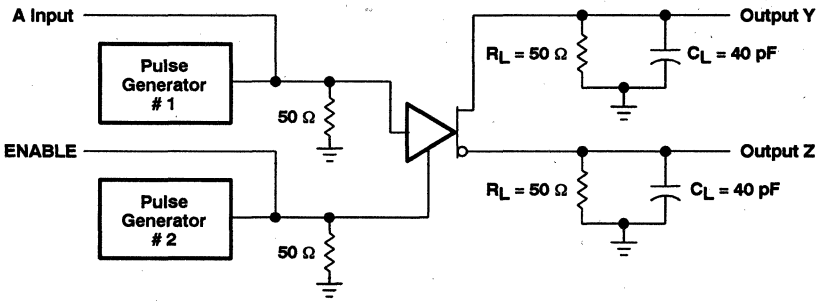
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -12$ mA				−0.9	−1.5	V
$I_{O(on)}$	On-state output current	V_{CC+} = MAX	V_{CC-} = MAX			11	15	mA
		V_{CC+} = MIN,	V_{CC-} = MIN		6.5	11		
$I_{O(off)}$	Off-state output current	V_{CC+} = MIN,	V_{CC-} = MIN,	V_O = 10 V			100	μA
I_{IH}	High-level input current	V_I = 2.4 V					40	μA
		$V_I = V_{CC+}$ max					1	mA
I_{IL}	Low-level input current	V_I = 0.4 V					−1.6	mA
I_{CC+}	Supply current from V_{CC+}	A inputs at 0.4 V	ENABLE at 2 V			33	50	mA
			ENABLE at 0.4 V			33	50	
I_{CC-}	Supply current from V_{CC-}	A inputs at 0.4 V	ENABLE at 2 V			−68	−90	mA
			ENABLE at 0.4 V			−31	−40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, and T_A = 25°C.

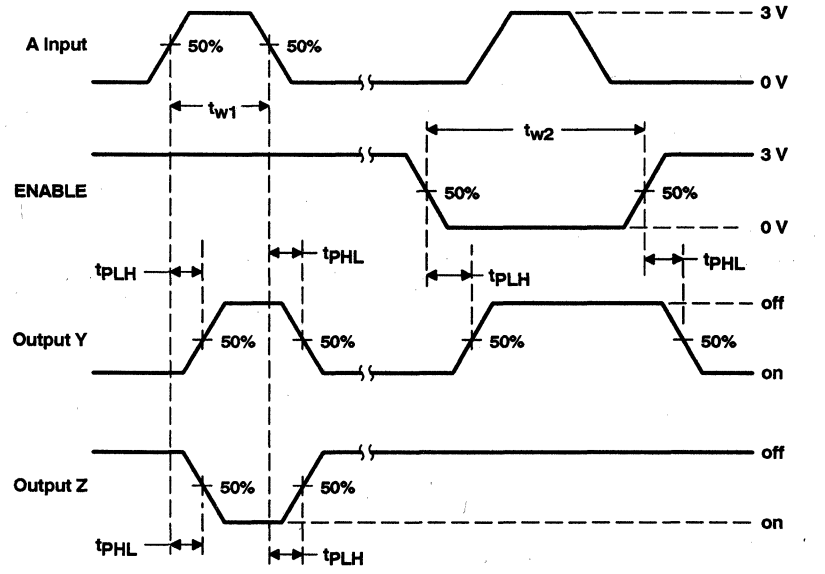
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, R_L = 50 Ω, C_L = 40 pF, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	A	Y or Z	See Figure 1		9	15	ns
t_{PHL}	Propagation delay time, high-to-low level output	A	Y or Z			7	15	ns
t_{PLH}	Propagation delay time, low-to-high level output	ENABLE	Y or Z			14	25	ns
t_{PHL}	Propagation delay time, high-to-low level output	ENABLE	Y or Z			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{w1} = 200 ns, PRR ≤ 1 MHz, t_{w2} = 1 μs, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

- **Meets EIA Standards RS-422-A and RS423-A and Federal Standards 1020 and 1030**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **Operates From Single 5-V Supply**
- **Designed to Be Interchangeable With Motorola MC3486**

description

The MC3486 is a monolithic quad differential line receiver designed to meet the specifications of EIA Standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

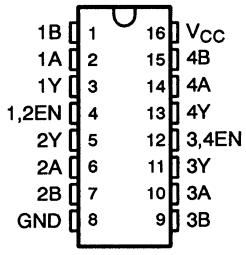
The MC3486 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

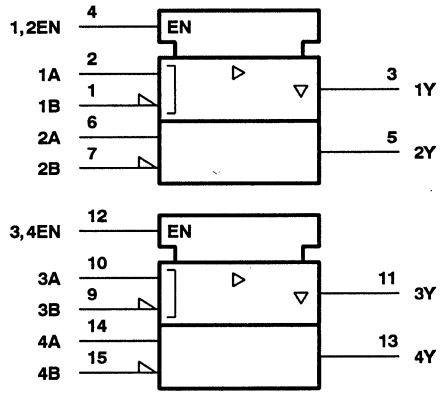
DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \leq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z

H = high level, L = low level, Z = high-impedance (off), ? = indeterminate

D OR N PACKAGE
(TOP VIEW)

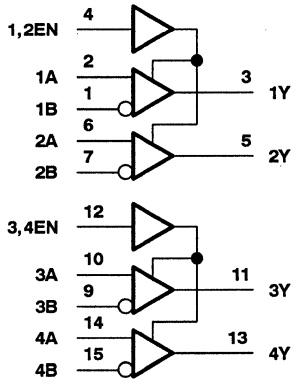


logic symbol†

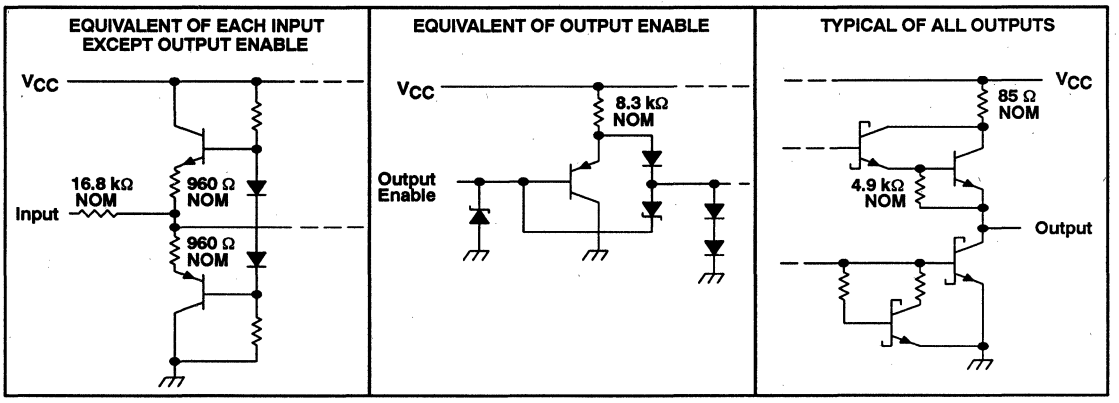


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 8 V
Input voltage, A or B inputs ..... ±15 V
Differential input voltage (see Note 2) ..... ±25 V
Enable input voltage ..... 8 V
Low-level output current ..... 50 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±6	V
High-level enable input voltage, V_{IH}	2			V
Low-level enable input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{T+}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = −8 mA		−0.2†		V
V_{IK}	Enable-input clamp voltage	I_I = −10 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 0.4 V, See Note 3 and Figure 1	I_O = −0.4 mA,		2.7		V
V_{OL}	Low-level output voltage	V_{ID} = −0.4 V See Note 3 and Figure 1	I_O = 8 mA,			0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V,	V_{ID} = −3 V,	V_O = 2.7 V		40	μA
		V_{IL} = 0.8 V,	V_{ID} = 3 V,	V_O = 0.5 V		−40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 5.25 V, Other inputs at 0 V		V_I = −10 V		−3.25	mA
				V_I = −3 V		−1.5	
				V_I = 3 V		1.5	
				V_I = 10 V		3.25	
I_{IH}	High-level enable input current	V_I = 5.25 V				100	μA
		V_I = 2.7 V				20	
I_{IL}	Low-level enable input current	V_I = −0.5 V				−100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 V,	V_O = 0,	See Note 4	−15	−100	mA
I_{CC}	Supply current	V_{IL} = 0				85	mA

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 3. Refer to EIA Standards RS-422-A and RS-423-A for exact conditions.
4. Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output	See Figure 2		28	35	ns
t_{PLH}	Propagation delay time, low-to-high level output			27	30	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

PARAMETER MEASUREMENT INFORMATION

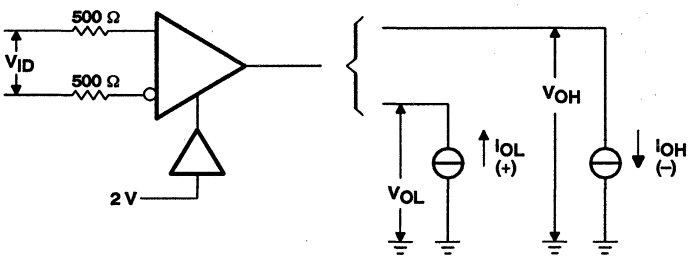


Figure 1. V_{OH}, V_{OL}

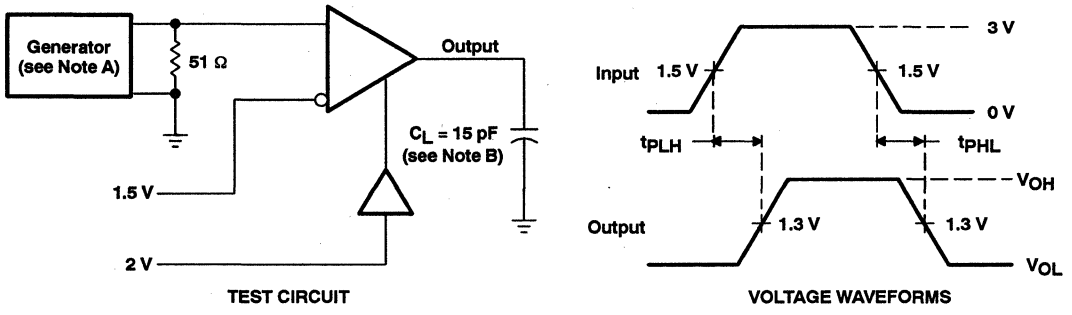


Figure 2. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

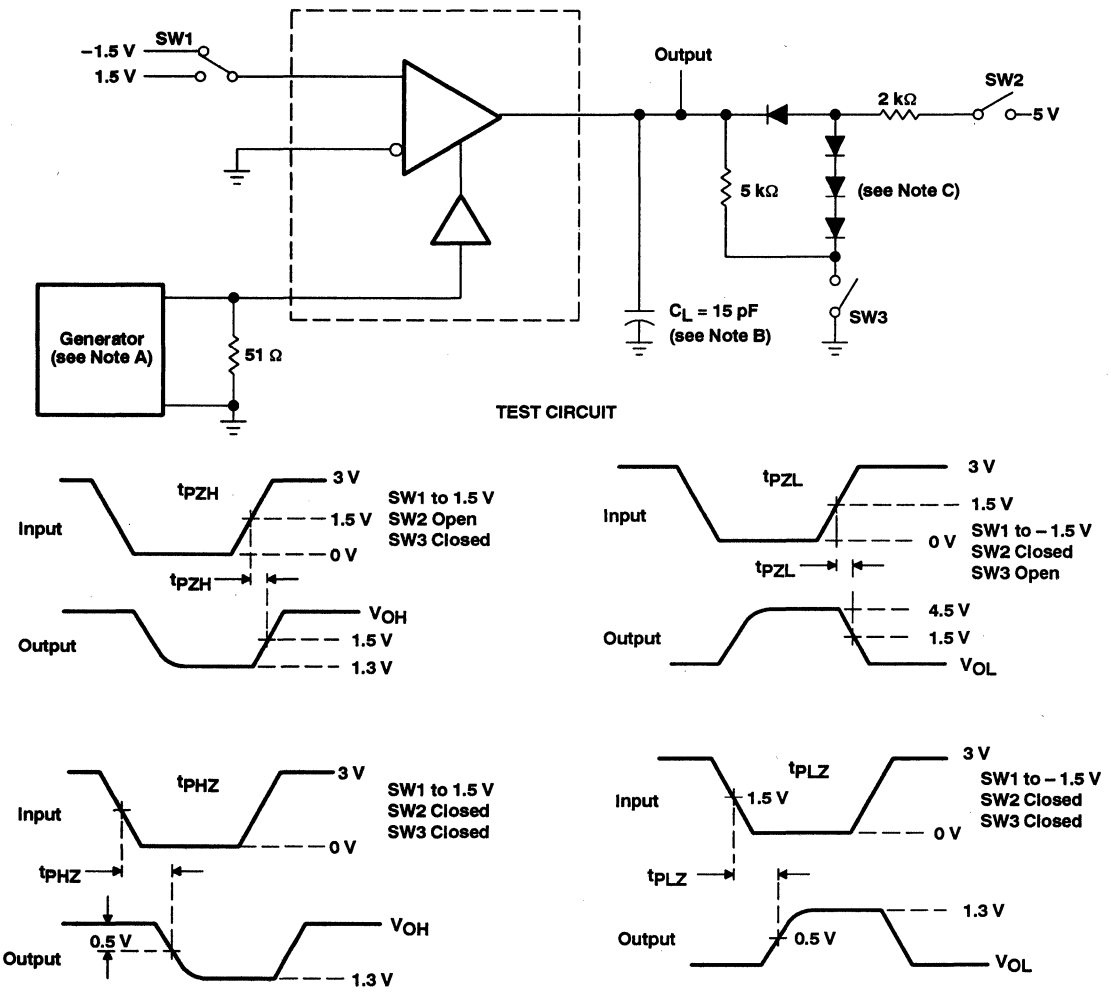
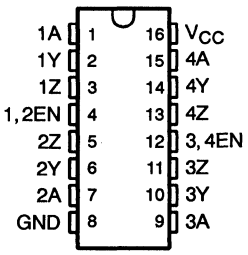


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

- **Meets EIA Standard RS-422-A and Federal Standard 1020**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**
- **Designed to Be Interchangeable With Motorola MC3487**

D, J, OR N PACKAGE
(TOP VIEW)



description

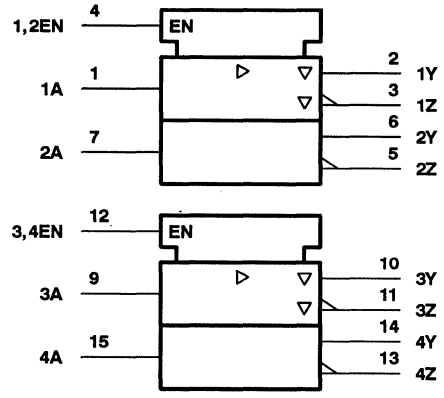
The MC3487 offers four independent differential line drivers designed to meet the specifications of EIA Standard RS-422-A and Federal Standard 1020. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low. The outputs are capable of source or sink currents of 48 mA.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

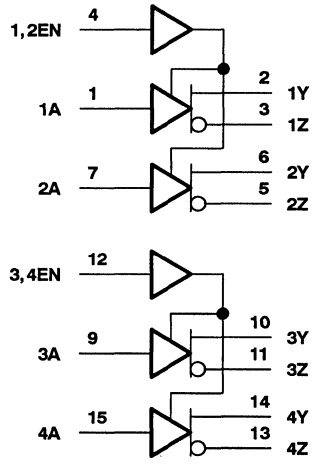
The MC3487 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

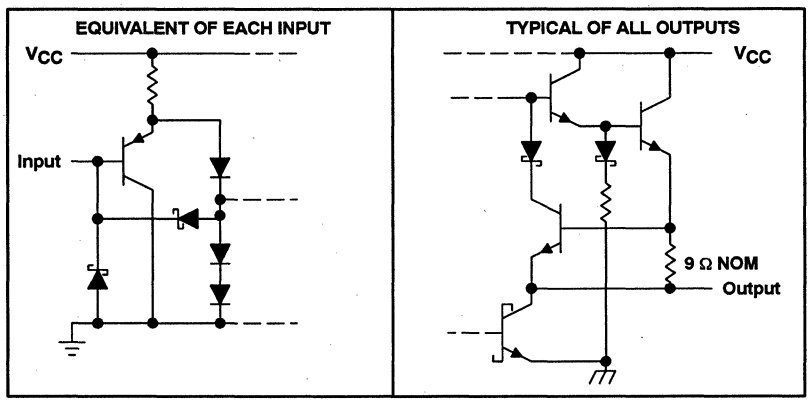


FUNCTION TABLE
(each driver)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-impedance	High-impedance

H = TTL high level, L = TTL low level, X = irrelevant

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 8 V
Input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{IL} = 0.8$ V,	$V_{IH} = 2$ V,	$I_{OH} = -20$ mA	2.5		V
V_{OL}	Low-level output voltage	$V_{IL} = 0.8$ V,	$V_{IH} = 2$ V,	$I_{OL} = 48$ mA		0.5	V
$\lvert V_{OD}\rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1		2		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage†	$R_L = 100\ \Omega$,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	$R_L = 100\ \Omega$,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage†	$R_L = 100\ \Omega$,	See Figure 1			±0.4	V
I_O	Output current with power off	$V_{CC} = 0$	$V_O = 6$ V			100	μA
			$V_O = -0.25$ V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	$V_O = 2.7$ V			100	μA
			$V_O = 0.5$ V			−100	
I_I	Input current at maximum input voltage	$V_I = 5.5$ V				100	μA
I_{IH}	High-level input current	$V_I = 2.7$ V				50	μA
I_{IL}	Low-level input current	$V_I = 0.5$ V				−400	μA
I_{OS}	Short-circuit output current§	$V_I = 2$ V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

† $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
‡ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
§ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended range of operating free-air temperature, $V_{CC} = 5$ V

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$C_L = 15$ pF,	See Figure 2		20	ns
t_{PHL}	Propagation delay time, high-to-low level output				20	ns
	Skew				6	ns
t_{tD}	Differential-output transition time	$C_L = 15$ pF,	See Figure 3		20	ns
t_{PZH}	Output enable time to high level	$C_L = 50$ pF,	See Figure 4		30	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				25	ns
t_{PLZ}	Output disable time from low level				30	ns

PARAMETER MEASUREMENT INFORMATION

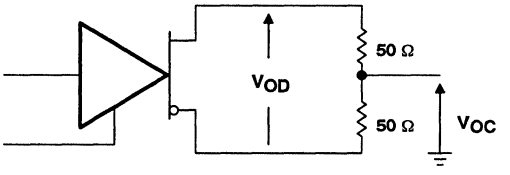
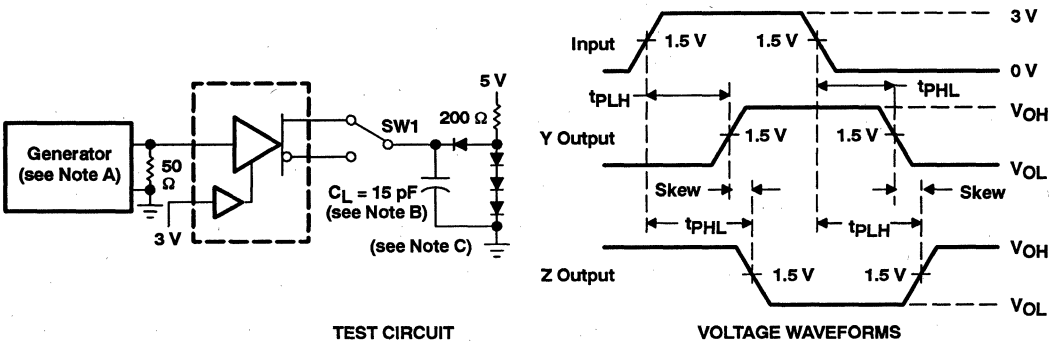


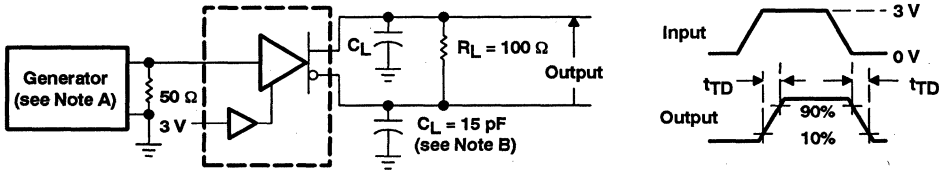
Figure 1. Differential and Common-Mode Output Voltages

PARAMETER MEASUREMENT INFORMATION



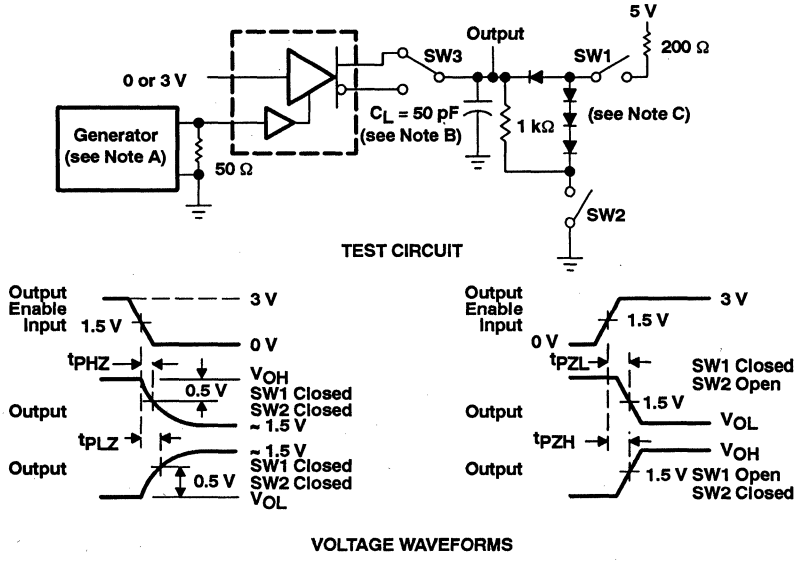
TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 2. Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. Test Circuit and Voltage Waveforms



TEST CIRCUIT

VOLTAGE WAVEFORMS

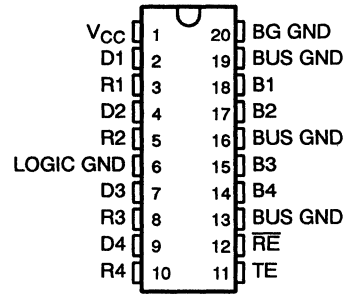
Figure 4. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

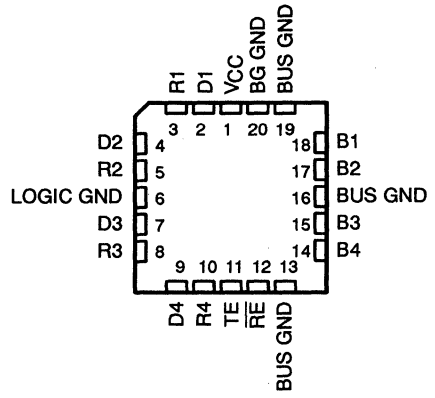
SLLS034B – D3077, JANUARY 1988 – REVISED SEPTEMBER 1989

- **High-Speed Quad Transceiver**
- **Fully Compatible With IEEE Std. 896.1 – 1987 Futurebus Requirements**
- **Drives Load Impedances as Low as 10 Ω**
- **High-Speed Advanced Low-Power Schottky Circuits**
- **Low Power Dissipation . . . 81 mW Max per Channel**
- **High-Impedance PNP Inputs**
- **BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Low Bus-Port Capacitance**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allows Wired-OR Connections**
- **Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3893**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way data communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0° to 70°C.

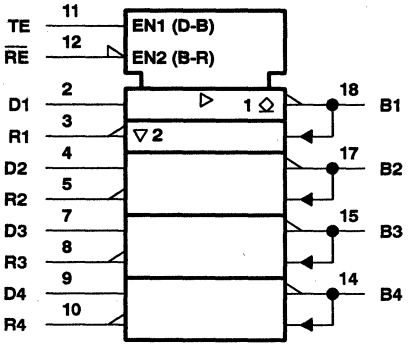
BTL is a trademark of National Semiconductor Corporation.

FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS	
TE	$\overline{RE}$	D→B	B→R
L	L	D	R
L	H	D	D
H	L	T	R
H	H	T	D

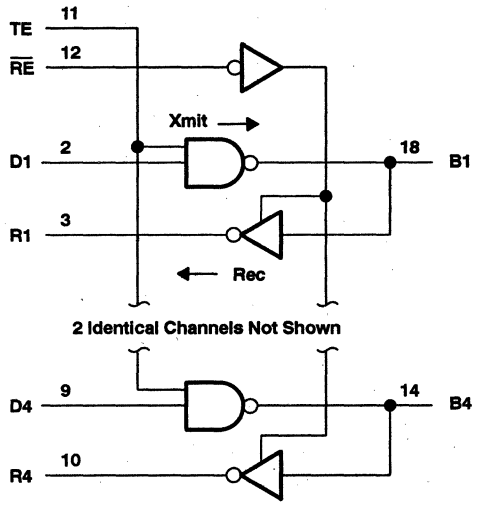
H = high level, L = low level, R = receive,
T = transmit, D = disable
Direction of data transmission is from Dn to Bn, direction of data reception is from Bn to Rn.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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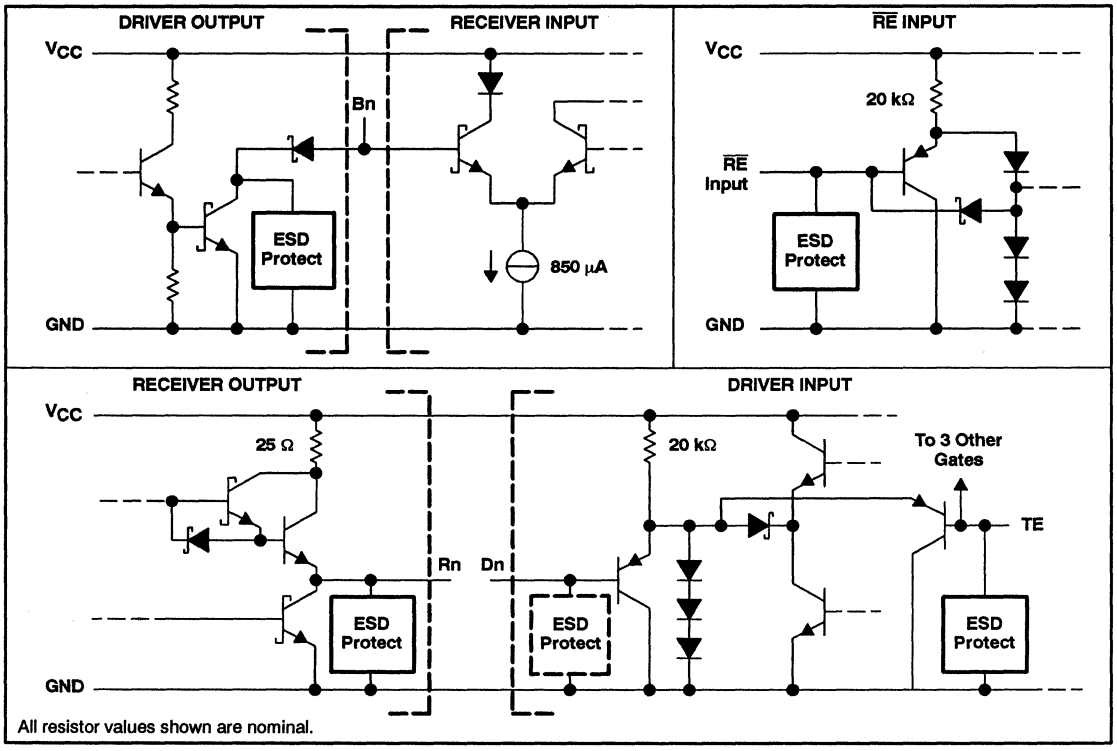
schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Control input voltage ..... 5.5 V
Driver input voltage ..... 5.5 V
Driver output voltage ..... 2.5 V
Receiver input voltage ..... 2.5 V
Receiver output voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: N package ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FN	1400 MW	11.2 MW/°C	896 MW
N	1150 MW	9.2 MW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, DE, or $\overline{RE}$		$I_I = -18$ mA			−1.5	V
V_T	Receiver input threshold voltage at Bn			1.426		1.674	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, $I_{OH} = -1$ mA	2.5			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, $I_{OL} = 20$ mA			0.5	V
		Bn	Dn at 2.4 V, TE at 2.4 V, See Figure 1, $V_L = 2$ V, $R_L = 10\ \Omega$	0.75		1.2	
I_{IH}	High-level input current	Dn, TE or $\overline{RE}$	$V_I = V_{CC}$			40	μA
		Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, Dn at 0.8 V, TE at 0.8 V			100	
I_{IL}	Low-level input current at Dn, TE or $\overline{RE}$		$V_I = 0.4$ V			−400	μA
I_{OS}	Short-circuit output at Rn		Rn at 0 V, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−70		−200	mA
I_{CC}	Supply current					65	mA
$C_{o(B)}$	Driver output capacitance		$V_{CC} = 5$ V, $T_A = 25°C$		6.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{PLH}	Propagation delay time low-to-high-level output	Dn	Bn	Dn at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{TLH}	Transition time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	0.5	5	ns
t_{THL}	Transition time, high-to-low-level output				0.5	5	
	Skew between driver channels†	Dn	Bn	TE at 3 V, V_L = 2 V		1	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V	2	8	ns
t_{PHL}	Propagation delay time, high-to-low-level output				2	8	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		6	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		12	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		6	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		12	ns
	Skew between receiver channels†	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V		1	ns

† Skew is the difference between the propagation delay time (t_{PLH} or t_{PHL}) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both t_{PLH} and t_{PHL}.

PARAMETER MEASUREMENT INFORMATION

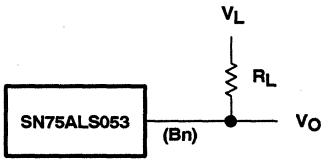
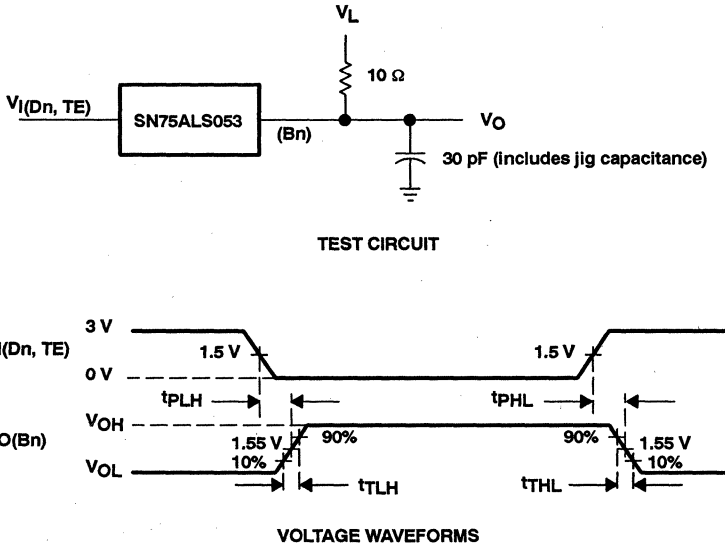


Figure 1. Driver Low-Level-Output-Voltage Test Circuit



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 2. Driver Test Circuit and Voltage Waveforms

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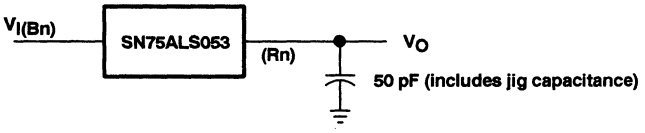
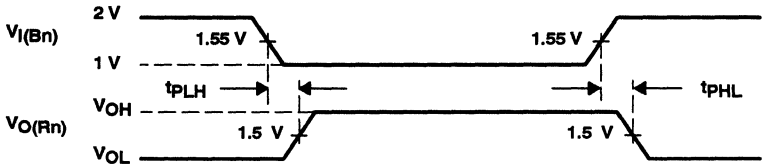
PARAMETER MEASUREMENT INFORMATION



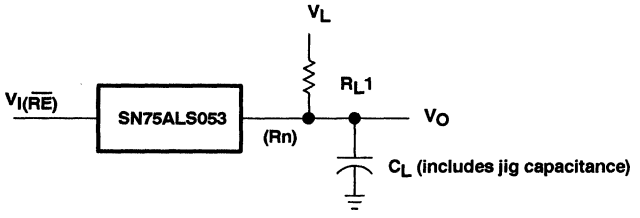
TEST CIRCUIT



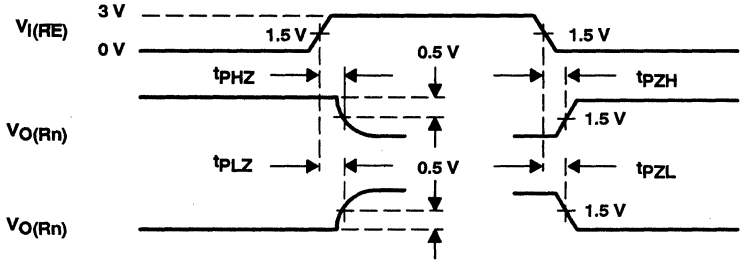
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

Figure 3. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

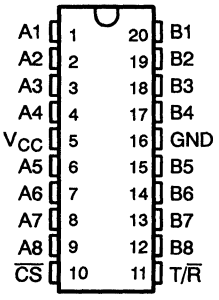
Figure 4. Test Circuit and Voltage Waveforms From $\overline{RE}$ to Rn

SLLS028D – D3025, AUGUST 1987 – REVISED MARCH 1993

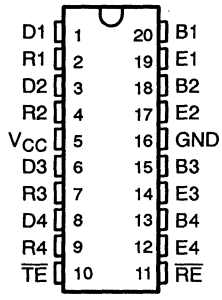
SUITABLE FOR IEEE STANDARD 896 APPLICATIONS†

- **SN55ALS056 and SN75ALS056 are Octal Transceivers**
- **SN55ALS057 and SN75ALS057 are Quad Transceivers**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation:**
  SN55' Devices . . . 60 mW/Channel Max
  SN75' Devices . . . 52.5 mW/Channel Max
- **High-Impedance PNP Inputs**
- **Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allow Wired-OR Connections**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3896, DS3897**

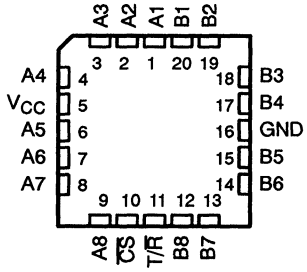
SN55ALS056 . . . J OR W PACKAGE
SN75ALS056 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS057 . . . J OR W PACKAGE
SN75ALS057 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS056 . . . FK PACKAGE
(TOP VIEW)



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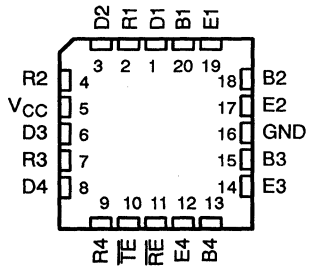


† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

description

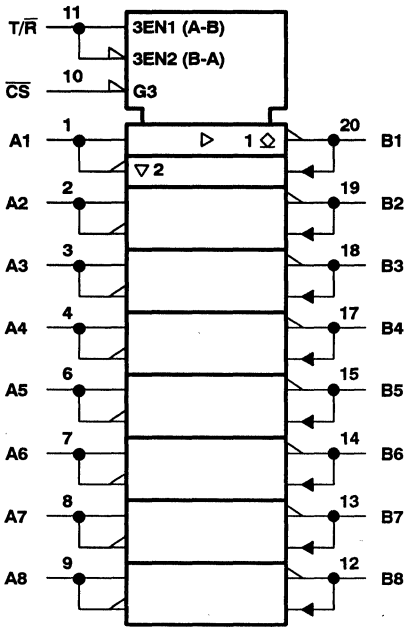
The SN55ALS056 and SN75ALS056 are 8-channel, monolithic, high-speed, advanced low-power Schottky devices designed for 2-way data communication in a densely populated backplane. The SN55ALS057 and SN75ALS057 are 4-channel versions with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En).

These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

The SN55ALS056 and SN55ALS057 are characterized over the full military operating range of −55°C to 125°C. The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS056



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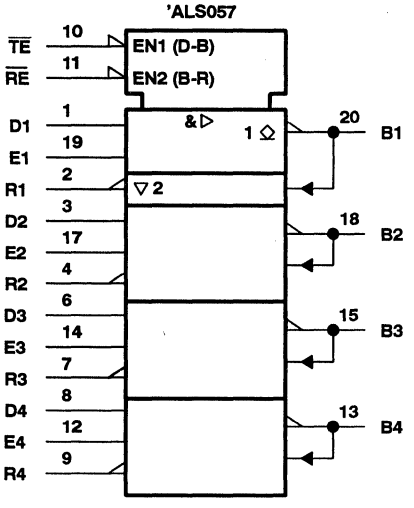
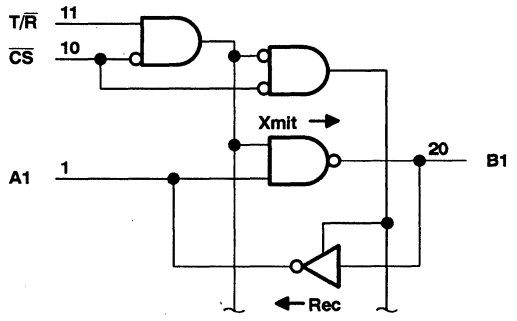
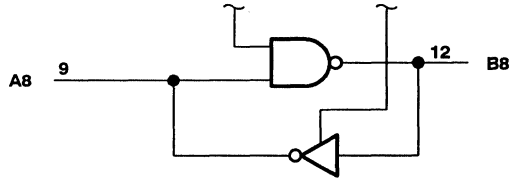


logic diagrams (positive logic)

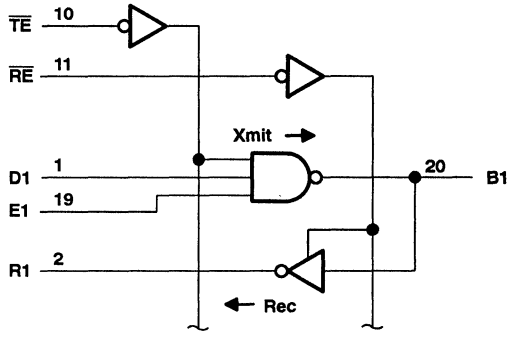
'ALS056



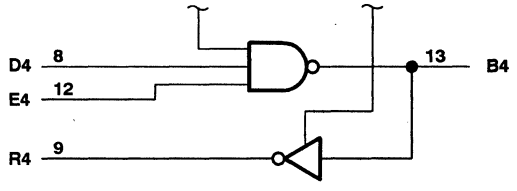
6 Identical Channels Not Shown



'ALS057



2 Identical Channels Not Shown



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Tables

'ALS056
TRANSMIT/RECEIVE

CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ↔ B
L	H	T (A → B)
L	L	R (B → A)
H	X	D

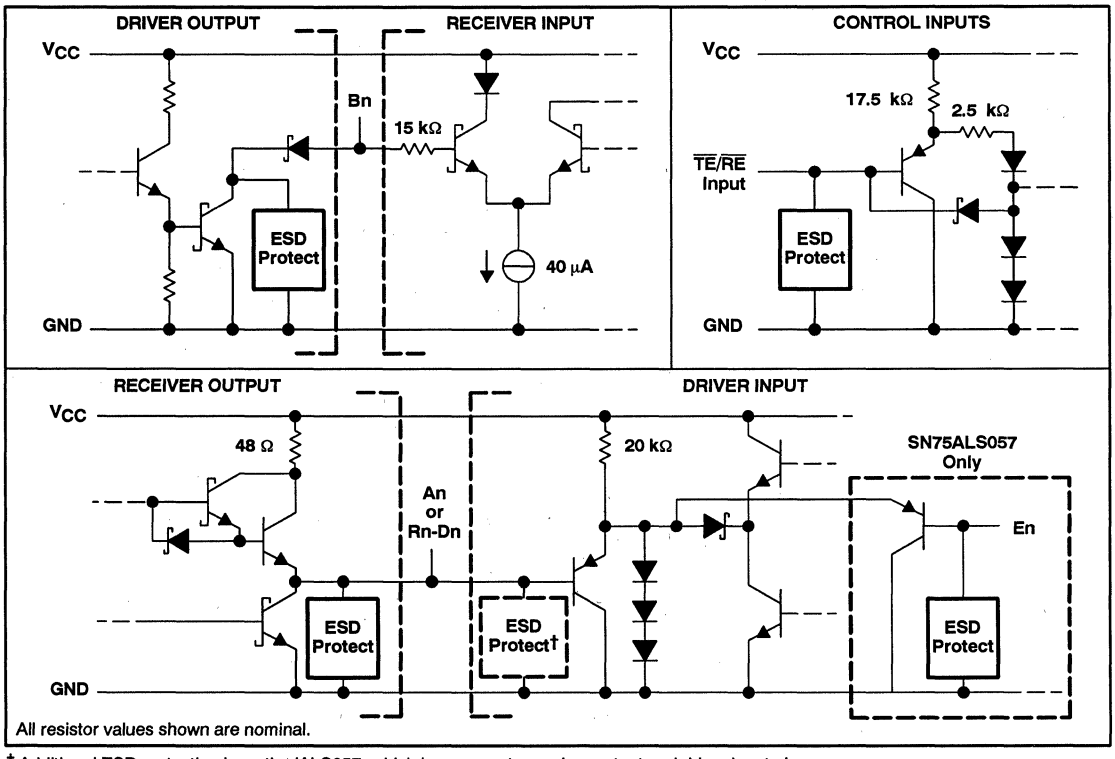
'ALS057
TRANSMIT/RECEIVE

CONTROLS			CHANNELS	
$\overline{TE}$	$\overline{RE}$	En	D → B	B → R
L	L	L	D	R
L	L	H	T	R
L	H	L	D	D
L	H	H	T	D
H	L	X	D	R
H	H	X	D	D

H = high level, L = low level, R = receive, T = transmit, D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the 'ALS056 and from Dn to Bn for the 'ALS057. Direction of data reception is from Bn to An for the 'ALS056 and from Bn to Rn for the 'ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



All resistor values shown are nominal.

† Additional ESD protection is on the 'ALS057, which has separate receiver output and driver input pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Control input voltage ..... 5.5 V
Driver input voltage ..... 5.5 V
Driver output voltage ..... 2.5 V
Receiver input voltage ..... 2.5 V
Receiver output voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55ALS05_ ..... −55°C to 125°C
SN75ALS05_ ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 300 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package ..... 300 °C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55ALS05_	4.5	5	5.5	V
	SN75ALS05_	4.75	5	5.25	
High-level driver and control input voltage, V_{IH}		2			V
Low-level driver and control input voltage, V_{IL}				0.8	V
Bus termination voltage		1.9		2.1	V
Operating free-air temperature, T_A	SN55ALS05_	−55		125	°C
	SN75ALS05_	0		70	

SN55ALS056 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_T	Receiver input threshold voltage at Bn		V_{CC} = 5 V,	T_A = 25°C	1.45		1.65	V
			V_{CC} = 5 V,	T_A = –55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at An		V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, I_{OH} = –400 μA	Bn at 1.2 V, T/$\overline{R}$ at 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	An	V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, I_{OL} = 16 mA	Bn at 2 V, T/$\overline{R}$ at 0.8 V,			0.5	V
		Bn	V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, See Figure 1	An at 2 V, T/$\overline{R}$ at 2 V,	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$ or $\overline{CS}$	V_I = V_{CC} = 5.5 V				40	μA
		Bn	V_{CC} = 5.5 V, An at 0.8 V,	V_I = 2 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 5.5 V,	V_I = 0.4 V			–400	μA
I_{OS}	Short-circuit output current at An		V_{CC} = 5.5 V, Bn at 1.2 V, T/$\overline{R}$ at 0.8 V	An at 0 V, $\overline{CS}$ at 0.8 V,	–35		–125	mA
I_{CC}	Supply current		V_{CC} = 5.5 V				85	mA
$C_{o(B)}$	Driver output capacitance					4.5		pF

SN75ALS056 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		I_I = –18 mA				–1.5	V
V_T	Receiver input threshold voltage at Bn				1.426		1.674	V
V_{OH}	High-level output voltage at An		Bn at 1.2 V, T/$\overline{R}$ at 0.8 V,	$\overline{CS}$ at 0.8 V, I_{OH} = –400 μA	2.4			V
V_{OL}	Low-level output voltage	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V,	$\overline{CS}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	An at 2 V, T/$\overline{R}$ at 2 V, R_L = 18.5 Ω,	$\overline{CS}$ at 0.8 V, V_L = 2 V, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$ or $\overline{CS}$	V_I = V_{CC}				40	μA
		Bn	V_I = 2 V, An at 0.8 V,	V_{CC} = 0 or 5.25 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_I = 0.4 V				–400	μA
I_{OS}	Short-circuit output current at An		An at 0 V, $\overline{CS}$ at 0.8 V,	Bn at 1.2 V, T/$\overline{R}$ at 0.8 V	–40		–120	mA
I_{CC}	Supply current						75	mA
$C_{o(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SN55ALS057 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_T	Receiver input threshold voltage at Bn		V_{CC} = 5 V,	T_A = 25°C	1.45		1.65	V
			V_{CC} = 5 V,	T_A = –55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at Rn		V_{CC} = 4.5 V, RE at 0.8 V,	Bn at 1.2 V, I_{OH} = – 400 µA	2.4			V
V_{OL}	Low-level output voltage	Rn	V_{CC} = 4.5 V, $\overline{RE}$ at 0.8 V,	Bn at 2 V, I_{OL} = 16 mA			0.5	V
		Bn	V_{CC} = 4.5 V, En at 2 V, See Figure 1	Dn at 2 V, $\overline{TE}$ at 0.8 V,	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC} = 5.5 V				40	µA
		Bn	V_{CC} = 5.5 V, Dn at 0.8 V, $\overline{TE}$ at 0.8 V	V_I = 2 V, En at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 5.5 V,	V_I = 0.4 V			– 400	µA
I_{OS}	Short-circuit output current at Rn		V_{CC} = 5.5 V, Bn at 1.2 V,	Rn at 0 V, $\overline{RE}$ at 0.8 V	– 435		– 125	mA
I_{CC}	Supply current		V_{CC} = 5.5 V				45	mA
$C_{o(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SN75ALS057 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		I_I = –18 mA				–1.5	V
V_T	Receiver input threshold voltage at Bn				1.43		1.65	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, I_{OH} = – 400 µA	$\overline{RE}$ at 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, I_{OL} = 16 mA	$\overline{RE}$ at 0.8 V,			0.5	V
		Bn	Dn at 2 V, $\overline{TE}$ at 0.8 V, R_L = 18.5 Ω,	En at 2 V, V_L = 2 V, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC}				40	µA
		Bn	V_I = 2 V, Dn at 0.8 V, $\overline{TE}$ at 0.8 V	V_{CC} = 0 or 5.25 V, En at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_I = 0.4 V				– 400	µA
I_{OS}	Short-circuit output current at Rn		Rn at 0 V, $\overline{RE}$ at 0.8 V	Bn at 1.2 V,	– 40		– 120	mA
I_{CC}	Supply current						40	mA
$C_{o(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN55ALS056 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-input level	An	Bn	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 2	25°C			10	ns
					Full range			40	
t_{PHL}	Propagation delay time high-to-low-input level				25°C			12	
					Full range			15	
t_{PLH}	Propagation delay time, low-to-high-input level	$\overline{CS}$	Bn	An and $T/\overline{R}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 2	25°C			18	ns
					Full range			30	
t_{PHL}	Propagation delay time, high-to-low-input level				25°C			20	
					Full range			22	
t_{PLH}	Propagation delay time, low-to-high-input level	$T/\overline{R}$	Bn	$\overline{CS}$ at 0.8 V V_L = 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 3	25°C			18	ns
					Full range			37	
t_{PHL}	Propagation delay time, high-to-low-input level				25°C			18	
					Full range			21	
t_{PHL}	Propagation delay time, low-to-high-input level	An	Bn	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, V_L = 2 V, See Figure 2	25°C	1	3	8	ns
					Full range	1		33	
t_{PLH}	Propagation delay time, high-to-low-input level				25°C	1	3	10	
					Full range	1		13	

SN75ALS056 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-output level	An	Bn	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 not connected, C_L = 30 pF, See Figure 2			19	ns
t_{PHL}	Propagation delay time high-to-low-output level						18	
t_{PLH}	Propagation delay time, low-to-high-output level	$\overline{CS}$	Bn	An and $T/\overline{R}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, C_L = 30 pF, R_L2 not connected, See Figure 2			24	ns
t_{PHL}	Propagation delay time, high-to-low-output level						20	
t_{PLH}	Propagation delay time, low-to-high-output level	$T/\overline{R}$	Bn	V_I(An) = 5 V, $\overline{CS}$ at 0.8 V, R_L1 = 18 Ω, C_L = 30 pF, R_L2 not connected, V_L = 2 V, See Figure 3			25	ns
t_{PHL}	Propagation delay time, high-to-low-output level						35	
t_{TLH}	Transition time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 2 V, V_L = 2 V, C_L = 30 pF, R_L1 = 18 Ω, R_L2 not connected, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

† Full range is –55°C to 125°C.
‡ Typical values are at V_{CC} = 5 V.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN55ALS056 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, R_L1 = 500 Ω, C_L = 50 pF,	T/$\overline{R}$ at 0.8 V, R_L2 = 500 Ω, See Figure 4	25°C		20	ns
						Full range		22	
t_{PHL}	Propagation delay time, high-to-low-level output					25°C		18	
						Full range		20	
t_{PLZ}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, R_L1 = 500 Ω, C_L = 50 pF, See Figure 5	T/$\overline{R}$ at 0.8 V, R_L2 = 500 Ω, V_L = 5 V,	25°C		20	ns
						Full range		22	
t_{PZL}	Output enable time to low level					25°C		13	
						Full range		14	
t_{PHZ}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, V_L = 0, R_L1 = R_L2 = 500 Ω,	T/$\overline{R}$ at 0.8 V, C_L = 50 pF, See Figure 5	25°C		12	ns
						Full range		13	
t_{PZH}	Output enable time to high level			Bn at 0.8 V, R_L1 not connected, C_L = 50 pF,	T/$\overline{R}$ at 0.8 V, R_L2 = 500 Ω, See Figure 5	25°C		14	
						Full range		22	
t_{PLZ}	Output disable time from low level	T/$\overline{R}$	An	Bn at 2 V, V_L = 5 V, R_L2 = 500 Ω, See Figure 3	$\overline{CS}$ at 0.8 V, R_L1 = 500 Ω, C_L = 50 pF,	25°C		17	ns
						Full range		20	
t_{PZL}	Output enable time to low level					25°C		25	
						Full range		40	
t_{PHZ}	Output disable time from high level	T/$\overline{R}$	An	Bn at 0.8 V, V_L = 0, R_L2 = 500 Ω, See Figure 3	$\overline{CS}$ at 0.8 V, R_L1 = 500 Ω, C_L = 50 pF,	25°C		12	ns
						Full range		13	
t_{PZH}	Output enable time to high level			Bn at 0.8 V, R_L1 open, C_L = 50 pF,	$\overline{CS}$ at 0.8 V, R_L2 = 500 Ω, See Figure 3	25°C		15	
						Full range		22	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An	V_L = 5 V, R_L2 = 500 Ω, See Figure 6	R_L1 = 500 Ω, C_L = 50 pF,	25°C	4		ns
						Full range	2		

† Full range is –55°C to 125°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN75ALS056 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					18	
t_{PLZ}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL}	Output enable time to low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		8	ns
t_{PZH}	Output enable time to high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ See Figure 5		17	ns
t_{PLZ}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		20	ns
t_{PZL}	Output enable time to low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		40	ns
t_{PHZ}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		17	ns
t_{PZH}	Output enable time to high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		15	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, V_L = 5 V, See Figure 6	3		ns

switching characteristics over recommended ranges of supply voltages and operating free-air temperature

SN55ALS057 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C			12	
					Full range			15	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C			17	
					Full range			19	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 2	25°C	1	3	8	ns
					Full range	1		33	
t_{THL}	Transition time, high-to-low-level output				25°C	1	3	10	ns
					Full range	1		13	

† Full range is −55°C to 125°C.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

SN75ALS057 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 not connected, C_L = 30 pF, See Figure 2			19	ns
t_{PHL}	Propagation delay time, high-to-low-level output						18	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 not connected, C_L = 30 pF, See Figure 2			24	ns
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, $\overline{TE}$ at 0.8 V, R_L1 = 18 Ω, R_L2 not connected, C_L = 30 pF, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltages and operating free-air temperature (continued)

SN55ALS057 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 4	25°C		20	ns
					Full range		22	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		18	
					Full range		20	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 5	25°C		15	ns
					Full range		17	
t_{PZL}	Output enable time to low level				25°C		13	
					Full range		14	
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 5	25°C		12	ns
					Full range		13	
t_{PZH}	Output enable time to high level			Bn at 0.8 V, $\overline{TE}$ at 2 V, R_L1 not connected, R_L2 = 500 Ω, C_L = 50 pF, See Figure 5	25°C		14	
					Full range		15	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	V_L = 5 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 6	25°C	4		ns
					Full range	2		

† Full range is −55°C to 125°C.

SN75ALS057 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					18	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 30 pF, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		17	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 30 pF, R_L1 not connected, R_L2 = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	$\overline{TE}$ at 2 V, $\overline{RE}$ at 0.8 V, V_L = 0, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 6	3		ns

switching characteristics over recommended ranges of supply voltages and operating free-air temperature (continued)

SN55ALS057 driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 7	25°C		25	ns
					Full range		35	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		25	
					Full range		44	

† Full range is −55°C to 125°C.

SN75ALS057 driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 7		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					40	

PARAMETER MEASUREMENT INFORMATION

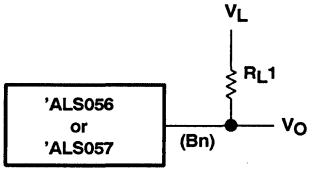
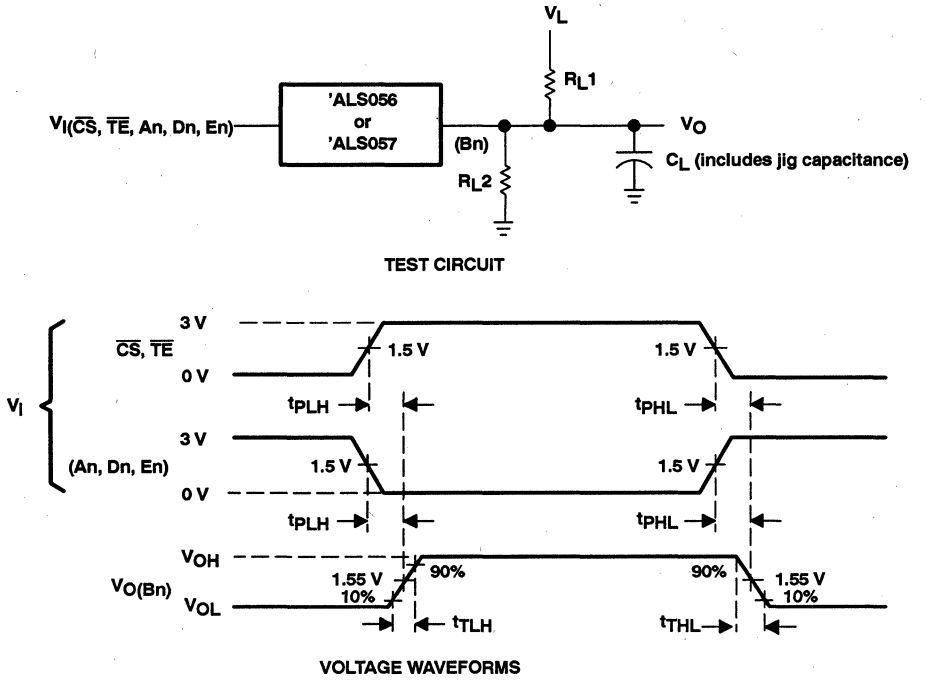


Figure 1. Driver Low-Level-Output-Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 2. Driver Test Circuit and Voltage Waveforms

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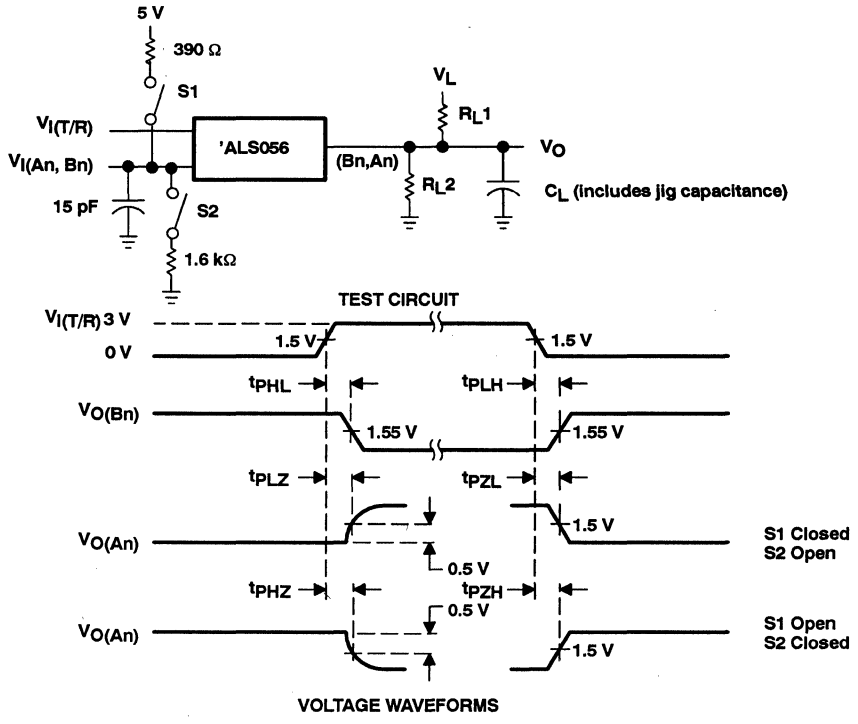
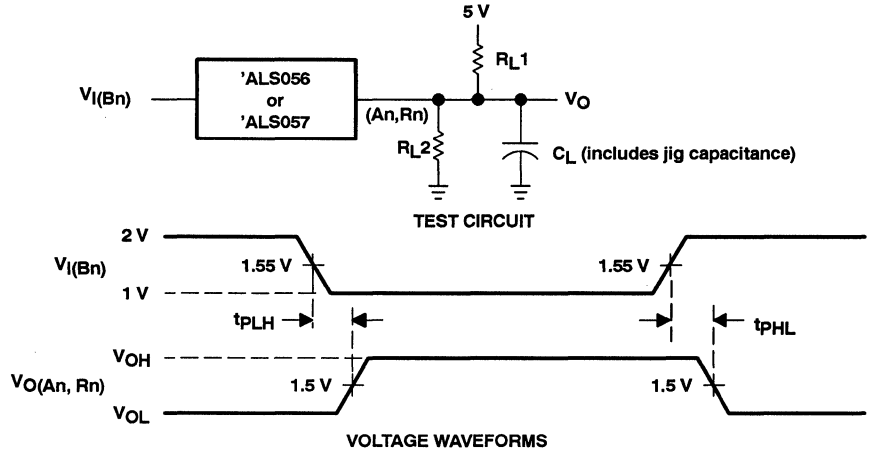
PARAMETER MEASUREMENT INFORMATION



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

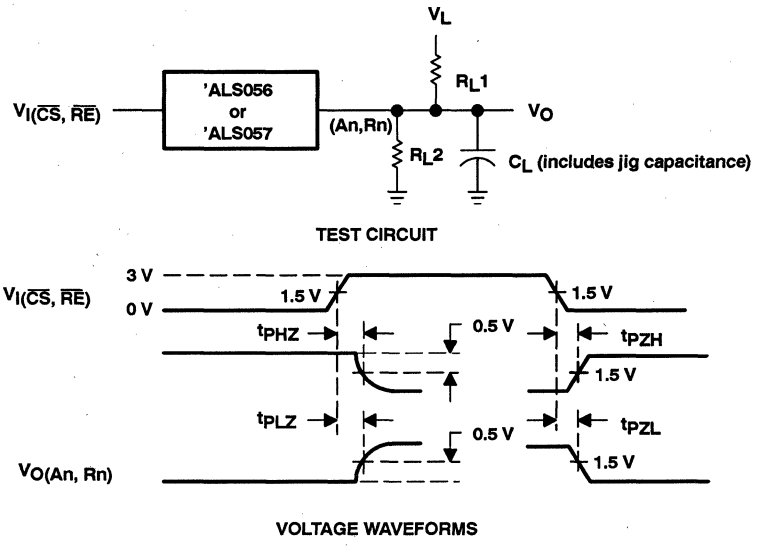
Figure 3. Propagation Delay From T/$\overline{R}$ to An or Bn Test Circuit and Voltage Waveforms



NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

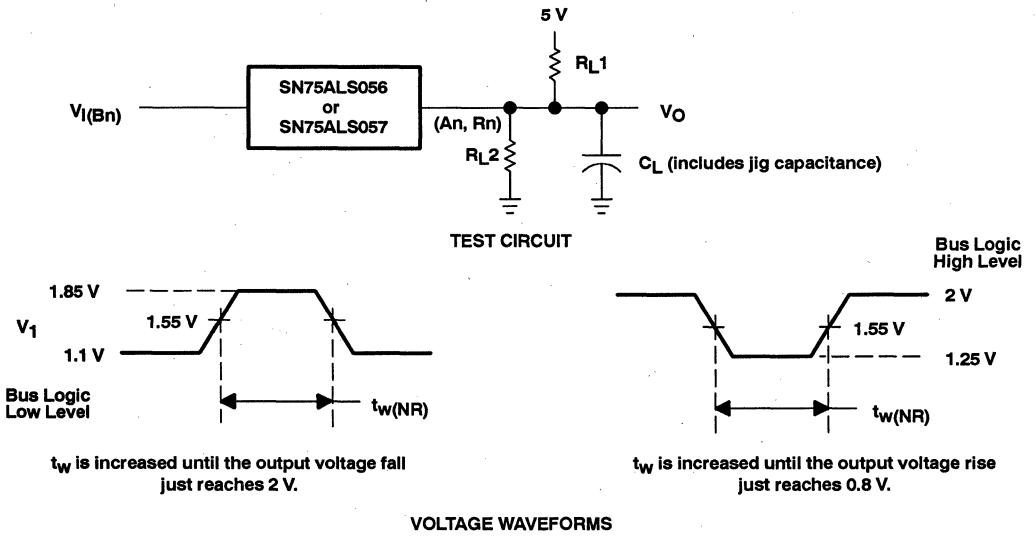
Figure 4. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

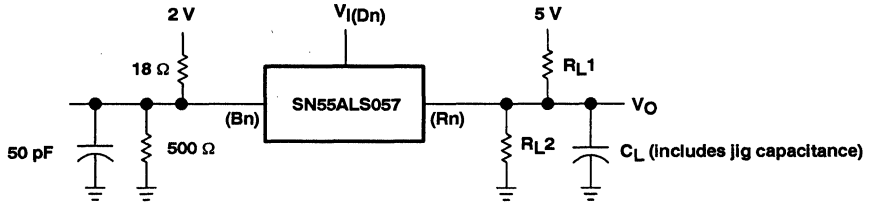
Figure 5. Propagation Delay From $\overline{CS}$ to An or $\overline{RE}$ to Rn Test Circuit and Voltage Waveforms



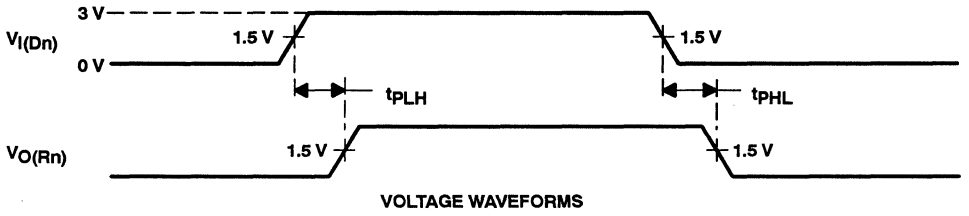
NOTE: $t_r = t_f \leq 2$ ns from 10% to 90%

Figure 6. Receiver Noise Immunity Test Circuit and Voltage Waveforms

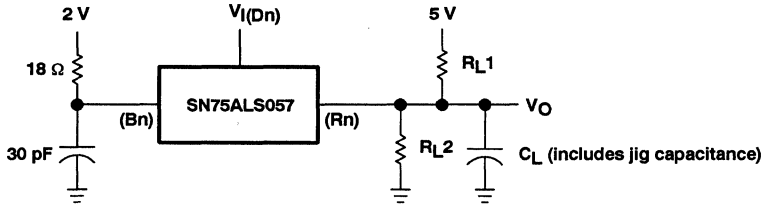
PARAMETER MEASUREMENT INFORMATION



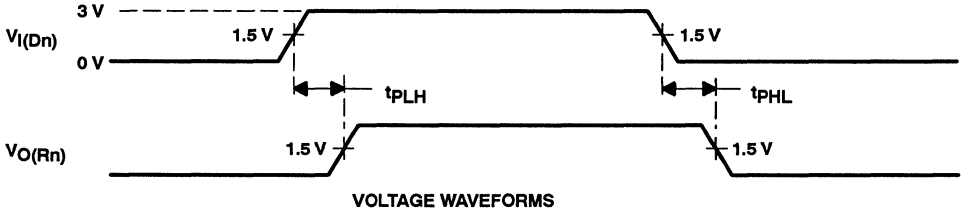
TEST CIRCUIT



VOLTAGE WAVEFORMS



TEST CIRCUIT



VOLTAGE WAVEFORMS

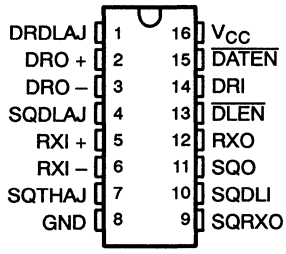
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 7. Driver Plus Receiver Delay Times Test Circuits and Voltage Waveforms

SLLS026C – D2959, JANUARY 1987 – REVISED JULY 1990

- **IEEE 802.3 1BASE5 Driver and Receiver**
- **On-Chip Receiver Squelch With Adjustable Threshold**
- **Adjustable Squelch Delay**
- **Direct TTL-Level Squelch Output**
- **Squelch Circuit Allows for External Noise Filtering**
- **Two Driver-Enable Options**
- **On-Chip Start-of-Idle Detection and Disable**
- **Driver Provides 2 V Minimum into a 50-Ω Differential Load to Allow for Use With Doubly-Terminated Lines and Multipoint Architectures**
- **On-Chip Driver Slew-Rate Control for Very Closely Matched Output Rise and Fall Times**

N PACKAGE
(TOP VIEW)



Function Tables

DRIVER

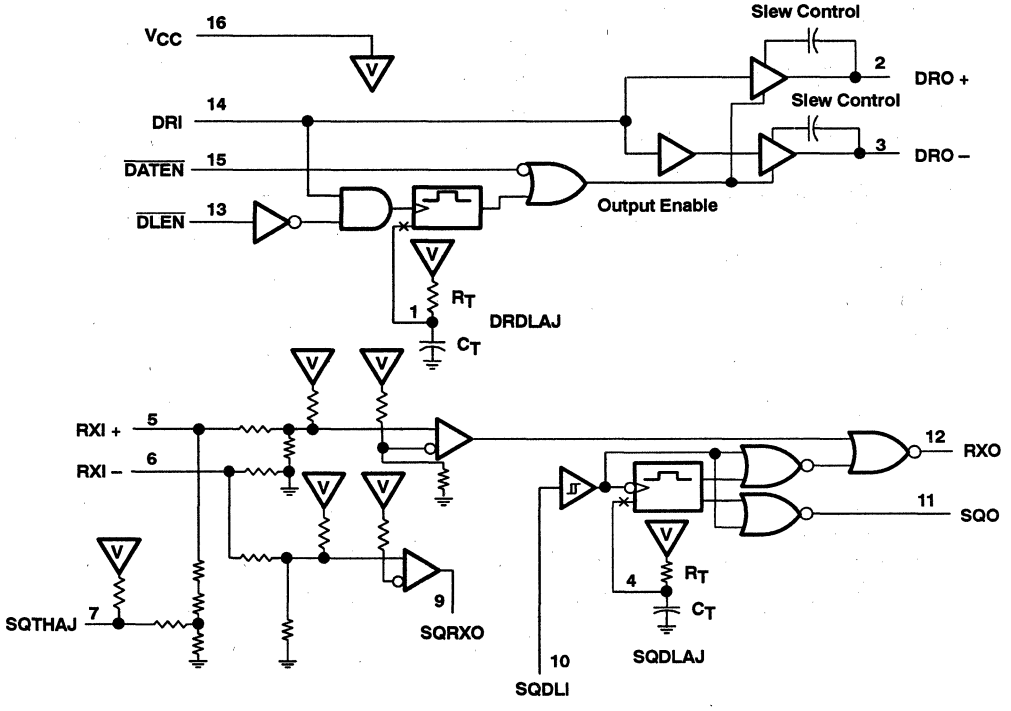
INPUTS			OUTPUTS	
DRI	DATEN	DLEN	DRO +	DRO –
L	L	X	L	H
H	L	X	H	L
X	H	H	Z	Z
H	H	L	H †	L †
L	H	L	L ‡	H ‡

RECEIVER§

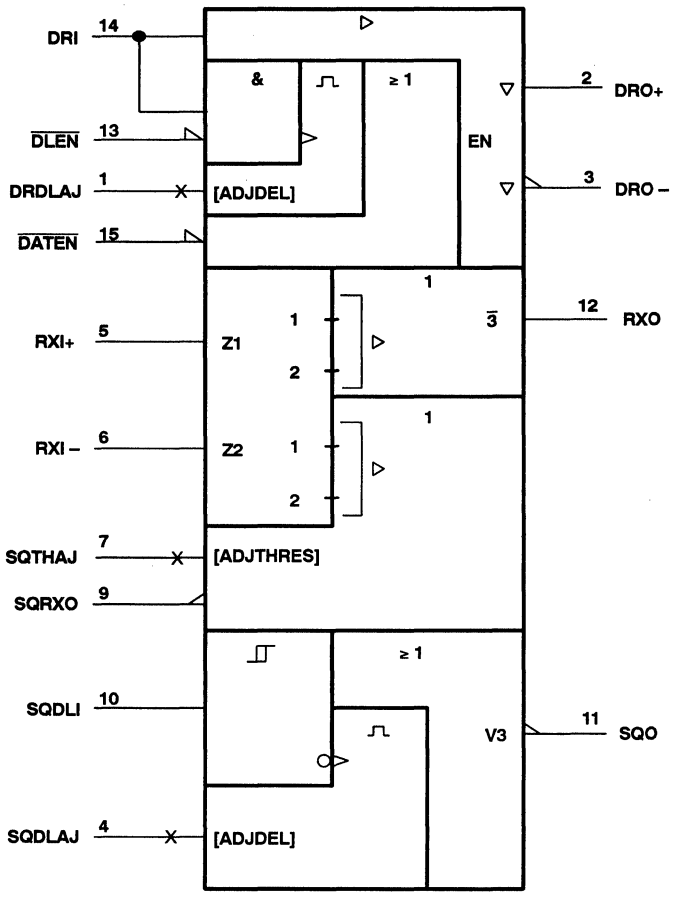
CONDITION	INPUTS		OUTPUTS	
	RXI +	RXI –	RXO	SQO
No active signal ¶	X	X	H	H
Active signal ¶	L	H	L	L
	H	L	H	L

† This condition is valid during the time period set by DRDLAJ following a rising transition on DRI. Following this, if no subsequent positive transition occurs on DRI, the outputs will go to the high-impedance state.
‡ This condition is valid if it occurs within the enable time set by DRDLAJ after a rising transition on DRI. Otherwise, the outputs will be in the high-impedance state.
§ Pins 9 and 10 are tied together.
¶ An active signal is one that has an amplitude greater than the threshold level set by SQTHAJ.

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN75061 is a single-channel driver/receiver pair designed for use in IEEE 802.3, 1BASE5 applications as well as other general data communications circuits. The SN75061 offers the system designer both a driver and a receiver that are easily configured for use with a variety of controllers and data encoder/decoders.

The receiver features a full analog squelch circuit with an adjustable threshold and a programmable squelch delay. Internal nodes of the squelch circuitry are brought out to external connections to allow for the insertion of noise filtering circuitry of the designer's choice.

As with the receiver, the driver offers a variety of implementation options. Driver enabling may be controlled directly by an external logic input or by use of an on-chip one-shot that is retriggered as long as data is being sent to the driver. The driver will then automatically go to the high-impedance state when end-of-packet occurs. The driver features internal slew-rate control for optimal matching of rise and fall times allowing for reduction of driver-induced jitter.

receiver

The SN75061 receiver implements full analog squelch functions by integrating both a separate, parallel squelch receiver with an externally programmable threshold, and a programmable one-shot. The output of the squelch receiver and the input to the high-level dc-triggered one-shot are brought out to external connections. These pins can be shorted for direct implementation or used for the insertion of noise-filtering circuitry of the implementer's design. The receiver one-shot can be effectively bypassed by applying a high logic level to SQDLI. The squelch threshold may be set externally by applying an external voltage set to a level that is −2 times the desired threshold voltage. If SQTHAJ is left open, the squelch receiver will default to its internal preset value of −600 mV. The receiver also outputs a high logic squelch signal when there is no active data present at the receiver inputs. When no data is present on the transmission line, the receiver output assumes a high level. The unsquelch duration is set externally with an R-C combination at SQDLAJ.

driver

The driver offers a variety of implementation options. Driver enabling may be controlled directly by an active-low external logic input on $\overline{\text{DATEN}}$ or by use of another on-chip one-shot that retriggers with positive-going transitions on the driver input line. If no positive transition occurs within the pulse duration set by an external R-C combination, the one-shot times out and the driver is automatically put into a high-impedance state. When operating in the delay-enable mode, the 2-bit-time high-level start-of-idle pulse prescribed by IEEE 802.3 1BASE5 causes the one-shot to time out and automatically place the driver outputs in the high-impedance state. This delay time is also adjustable for use in other applications. The driver implements an output slew-rate control that is internally set for nominally 40 mV/ns. (This is roughly a 100-ns peak-to-peak differential transition time.) The driver outputs are capable of driving a 50-Ω differential load with a minimum output level of 2 V. Short-circuit output current is greater than 100 mA.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
$\overline{\text{DATEN}}$	15	Driver data enable. When low, driver outputs are in an active state. When high, the driver outputs are in a high-impedance state if $\overline{\text{DLEN}}$ is also high.
$\overline{\text{DLEN}}$	13	Driver delay enable. When this signal is low and $\overline{\text{DATEN}}$ is high, the driver outputs are active for a period of time set by DRDLAJ after a positive-going transition on DRI. If there is no active data on DRI, the outputs are in a high-impedance state.
DRDLAJ	1	Driver delay adjust is a connection for the external R-C combination that determines the duration of the driver output active state after a positive transition on DRI when $\overline{\text{DLEN}}$ is low and $\overline{\text{DATEN}}$ is high.
DRI	14	Driver data input
DRO+	2	Noninverting driver output
DRO−	3	Inverting driver output
GND	8	Ground. Common for all voltages
RXI+	5	Noninverting receiver input
RXI−	6	Inverting receiver input
RXO	12	Main receiver input
SQDLAJ	4	Squelch delay adjust is a connection for an external R-C combination that determines the duration of the receiver unsquelch after a negative-going transition on SQDLI.
SQDLI	10	Squelch delay input is the input to the one-shot that controls the duration of the receiver unsquelch period. The main receiver output remains unsquelched as long as SQDLI is held high. Timing of the unsquelch period begins on the high-to-low transition of SQDLI.
SQO	11	Squelch output is high while the receiver is squelched.
SQRXO	9	Squelch receiver output is high only when the differential receiver input exceeds the threshold set by SQTHAJ.
SQTHAJ	7	Squelch receiver threshold adjust. The voltage at this input determines the threshold of the squelch receiver in a ratio of −2, SQTHAJ to threshold. If left open, the squelch receiver threshold defaults to −600 mV.
V_{CC}	16	Supply-voltage input

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage (any logic input) ..... 7 V
Receiver differential input voltage ..... ±25 V
Receiver input voltage ..... ±15 V
Driver output voltage ..... −0.5 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 1150 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Driver high-level input voltage, V_{IH}	2			V
Driver low-level input voltage, V_{IL}			0.8	V
Receiver common-mode input voltage, V_{IC} (see Note 2)	−2.5		5	V
Driver high-level output current, I_{OH}			−150	mA
Driver low-level output current, I_{OL}			150	mA
External timing resistance, R_{ext}	5		260	kΩ
External timing capacitance, C_{ext}	No restriction			
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, in which the less-positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{T+} and V_{T-}.

electrical characteristics over recommended operating free-air and supply voltage range (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OD}	Differential-output voltage	R_L = 50 Ω		2	2.4	3.3	V
		R_L = 115 Ω				3.65	
ΔV_{OD}	Change in differential-output voltage for a change in logic input state					50	mV
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V		±100		−35	μA
I_{OS}	Short-circuit output current	V_O = 0 or 6 V,	V_I = 0.8 V or 2.5 V			±300	mA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V	V_{OC} = 10 V			100	μA
			V_{OC} = 0			−100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air and supply voltage range (unless otherwise noted) (continued)

receiver

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, squelch delay		I_I = −18 mA				−1.5	V
V_{T+}	Positive-going threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			50	mV
V_{T-}	Negative-going threshold voltage		V_O = 0.5 V,	I_O = 16 mA	−50‡			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{IC}	Common-mode input voltage						5	V
V_{OH}	High-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 0.8 V	I_{OH} = −400 μA,	2.7			V
		SQO			2.7	3.5		
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = −0.7 V,	I_{OH} = −20 μA, SQDLAJ open	2.7	4.65		
V_{OL}	Low-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 2 V	I_{OL} = 8 mA			0.45	V
		SQO		I_{OL} = 16 mA			0.5	
				I_{OL} = 8 mA		0.35	0.5	
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = 50 mV	I_{OL} = 8 mA			0.45	
				I_{OL} = 16 mA			0.5	
I_{IH}	High-level input current	SQDLI	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current		V_I = 0.5 V				−35	μA
I_{OS}	Short-circuit output current	RXO	V_{CC} = 5.25 V,	V_O = 0	−15		−85	mA
		SQO			−15		−100	
		SQRXO	V_{CC} = 5 V,	V_O = 0	−0.8	−1	−1.2	
r_i	Input resistance					10		kΩ
$V_{T-(sq)}$	Squelch preset threshold voltage		V_{CC} = 5 V, SQTHAJ open	V_{IC} = 1.5 V to 3.5 V	−525	−600	−675	mV
				V_{IC} = −2.5 V to 1.5 V or 3.5 V to 5 V	−500		−700	mV
	Ratio of SQTHAJ input voltage to actual squelch threshold voltage		SQTHAJ at 200 mV to 4 V		−1.9		−2.1	

driver and receiver

				MIN	TYP†	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.25 V, No load	Driver outputs disabled,			70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{T+} and V_{T-}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

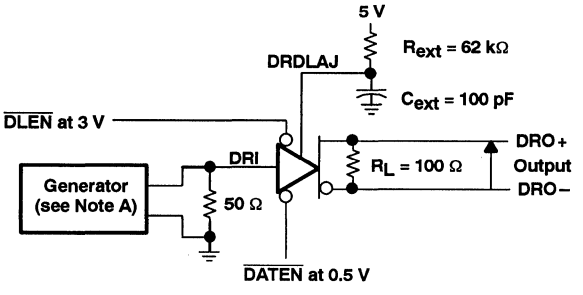
driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Differential-output slew rate	V_O = −2 V to 2 V, R_L =100 Ω (differential), See Figure 1	28	40	52	mV/ns
t_{dD}	Differential-output delay time (t_{dD+} and t_{dD-})	C_1 = 15 pF, R_L =100 Ω (differential), See Figure 2			160	ns
$t_{dD+} - t_{dD-}$	Differential-output delay time difference	R_L =100 Ω (differential), See Figure 2			5	ns
t_{PHZ}	Disabled time from $\overline{DATEN}$	See Figure 3, 4, and 5			220	ns
t_{PLZ}					300	ns
t_{PHZ}	Enable time from $\overline{DATEN}$				220	ns
t_{PLZ}					290	ns
t_{PZH}	Enable time from $\overline{DLEN}$				250	ns
$t_{w(en)}$	Enable pulse duration time (with DLEN low)	C_{ext} = 100 pF, R_{ext} = 62 kΩ, See Figure 6	2	2.5	3	µs

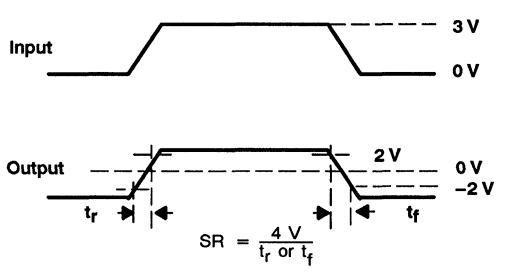
receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en(RX)}$	Receiver enable time	Squelch off, See Figure 7		117		ns
t_{PLH}	Propagation delay time, low-to high level output	Squelch off, See Figure 8		20	35	ns
t_{PHL}	Propagation delay time, high-to-low level output	Squelch off, See Figure 8		22	35	ns
$t_{d(unsq)}$	Unsquelch delay time	C_{ext} = 50 pF, R_{ext} = 51 kΩ, See Figure 9	1	1.2	1.45	µs
		C_{ext} = 15 pF, R_{ext} = 6.8 kΩ, See Figure 9			180	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 1. Driver Slew Rate Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

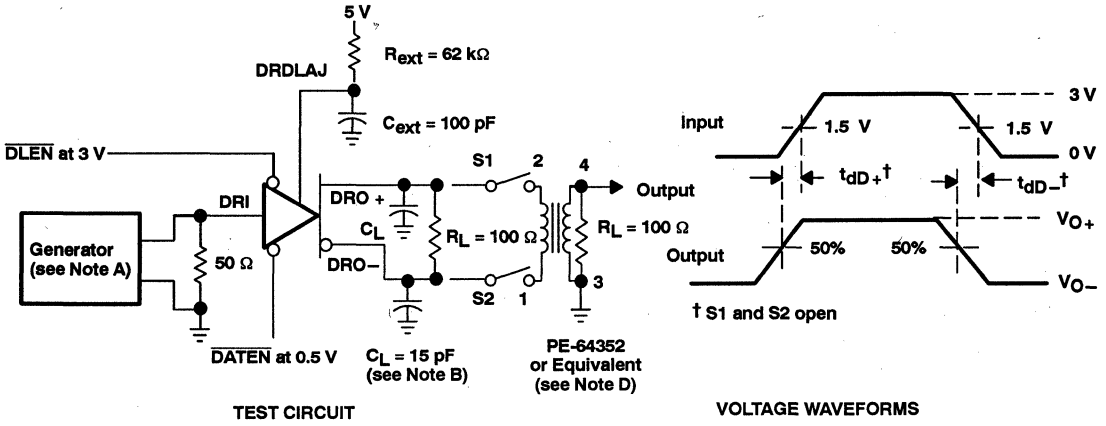


Figure 2. Driver Differential Delay Times Test Circuit and Voltage Waveforms

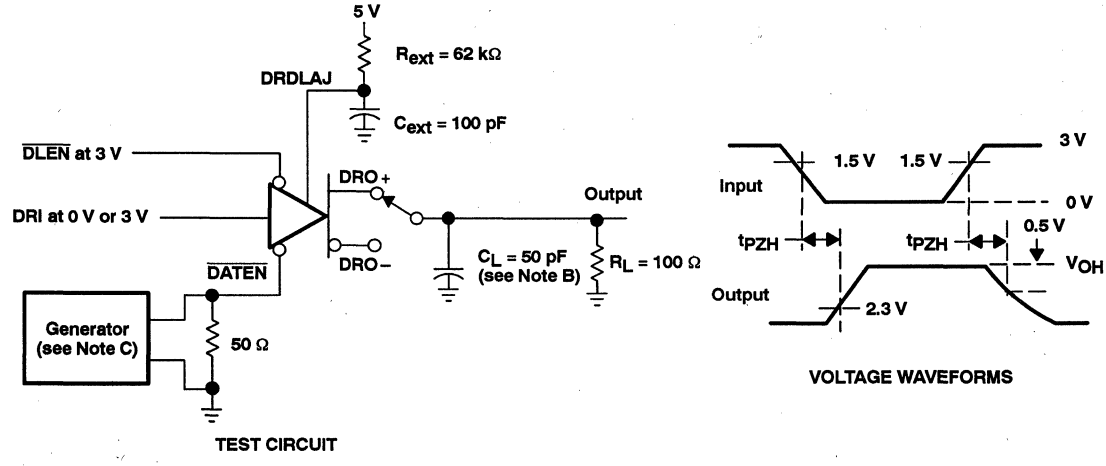


Figure 3. Driver Enable and Disable Time Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
D. When measuring differential-output delay time difference, switches S1 and S2 are closed. (Isolation transformer from Pulse Engineering P/N PE-64352).

PARAMETER MEASUREMENT INFORMATION

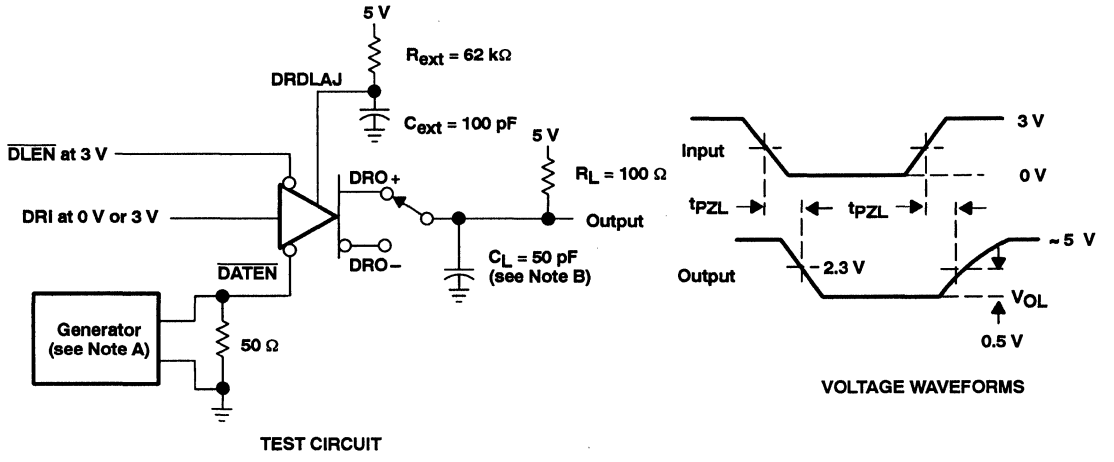


Figure 4. Driver Enable and Disable Time Test Circuit and Voltage Waveforms

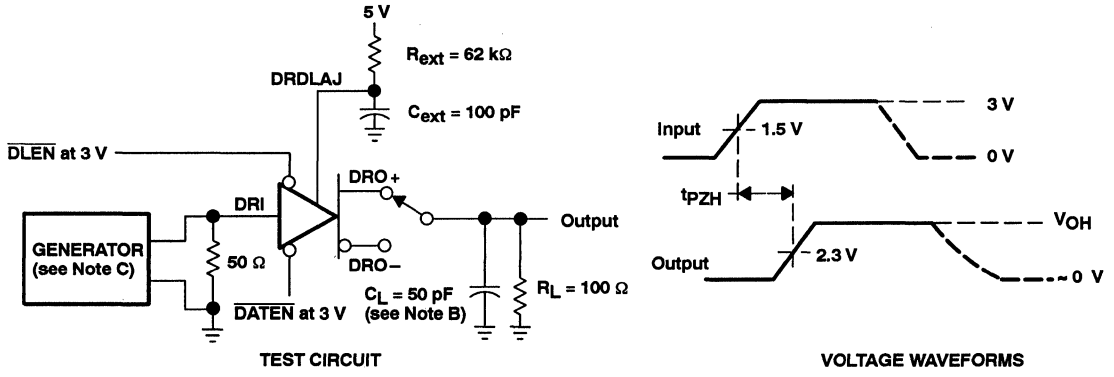


Figure 5. Enable Times From Delay Enable Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

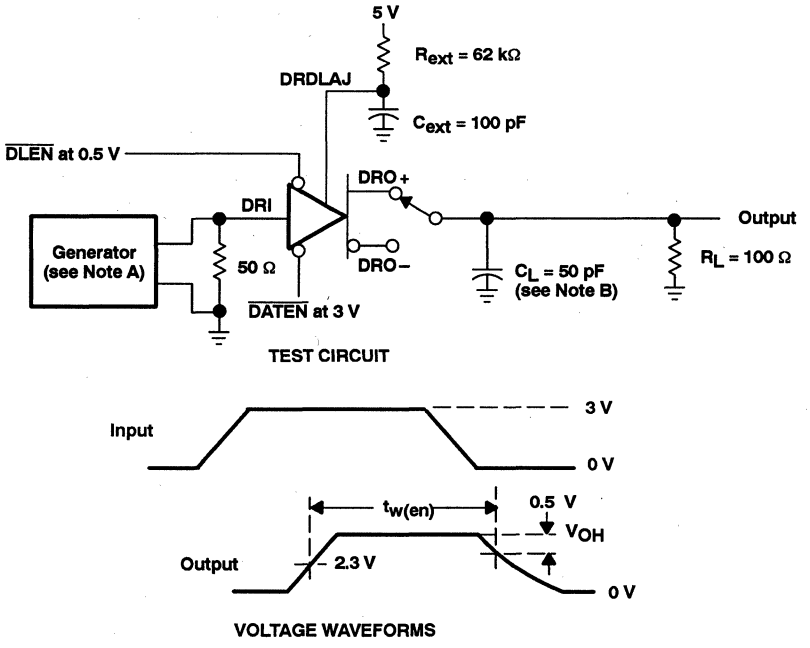


Figure 6. Enable Pulse Duration With Delay Enable Low Test Circuit and Voltage Waveforms

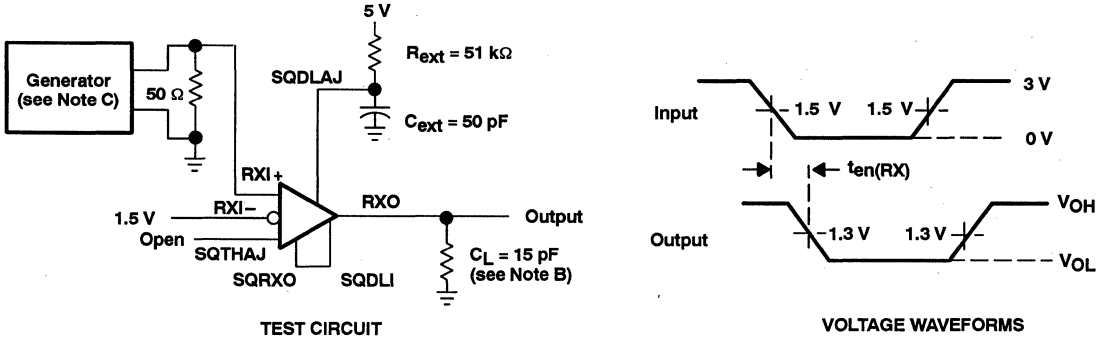
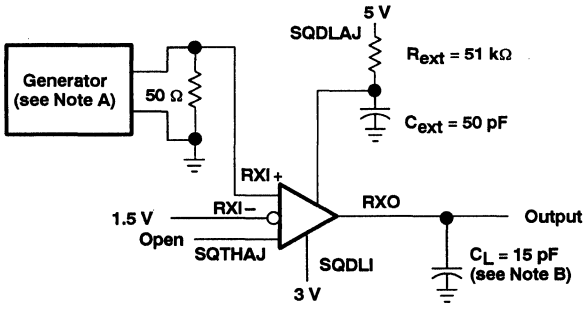


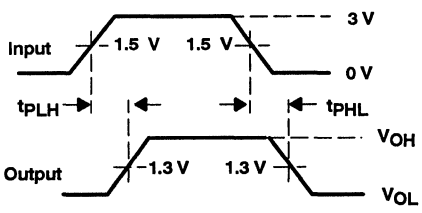
Figure 7. Receiver Enable (Unsquelch) Time Test Circuit and Voltage Waveforms

NOTES: D. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
E. C_L includes probe and jig capacitance.
F. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

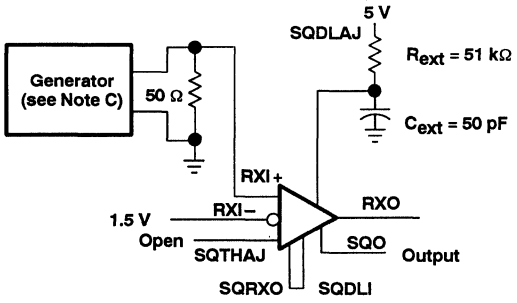


TEST CIRCUIT

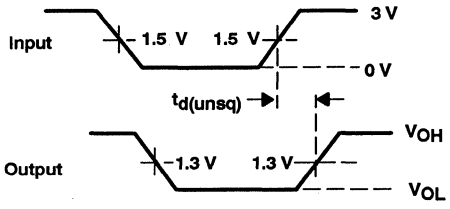


VOLTAGE WAVEFORMS

Figure 8. Receiver Propagation Delay Time Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

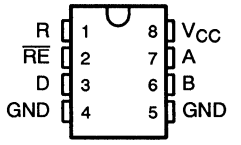
Figure 9. Unsquelch Duration Time Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 100 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

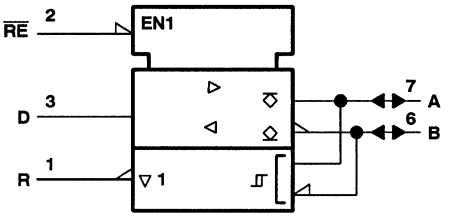
SLLS061 – D3407, JANUARY 1990

- **Bidirectional Transceiver**
- **Designed for Multipoint Transmission in Noisy Environments Such as Automotive Applications**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±10 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

D OR P PACKAGE
(TOP VIEW)



logic symbol†

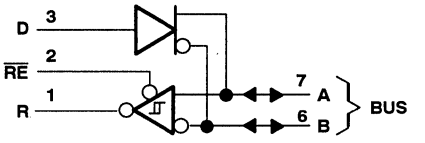


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN65076B and SN75076B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for noisy environments, where a low-impedance termination to ground is required.

logic diagram (positive logic)



The SN65076B and SN75076B combine a differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The receiver has an active-low enable. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

Function Tables

DRIVER

INPUT	OUTPUTS	
D	A	B
H	H	L
L	L†	H†

† These levels assume that the open-collector outputs (A) and the open-emitter outputs (B) are connected to a pullup and pulldown resistor, respectively.

RECEIVER

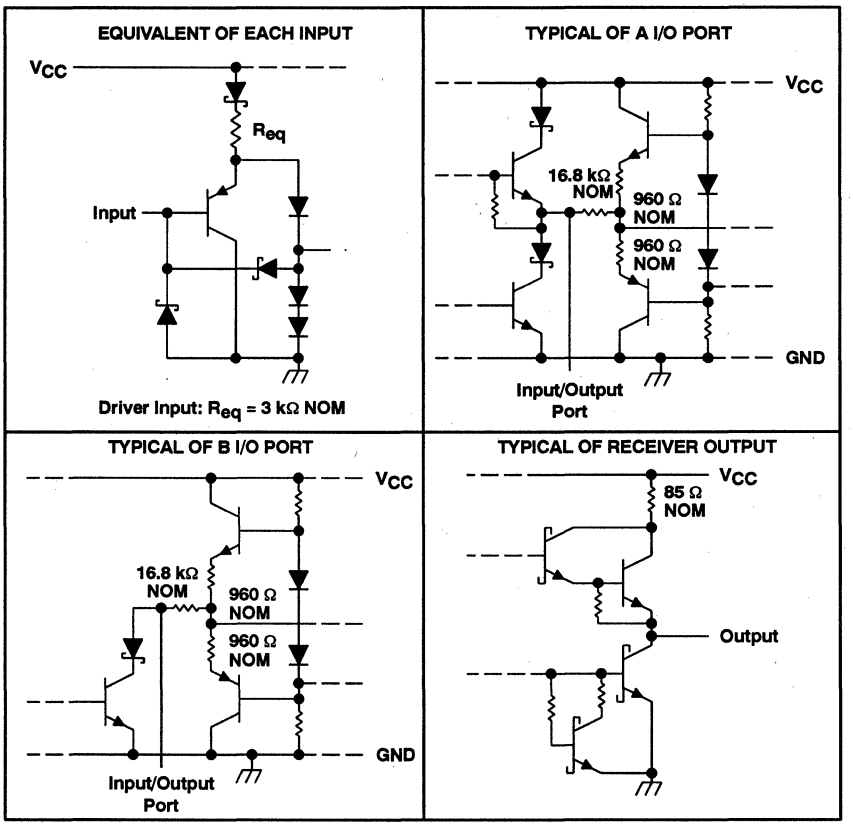
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	L
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	H
X	H	Z

H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

description (continued)

The driver is designed to handle loads up to 10 mA of sink and source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C in the P package and 170°C in the D package. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65076B is characterized for operation from −40°C to 105°C and the SN75076B is characterized for operation from 0°C to 70°C.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65076B ..... −40°C to 105°C
SN75076B ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}					12	V
					−7	
High-level input voltage, V_{IH}		D and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}		D and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)					±12	V
High-level output current, I_{OH}		Driver (A)			−10	mA
		Receiver			−400	µA
Low-level output current, I_{OL}		Driver (B)			10	mA
		Receiver			8	
Operating free-air temperature, T_A	SN65076B		−40		105	°C
	SN75076B		0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA			−1.5	V
V_O	Output voltage	$V_I = 2$ V, $I_O = 0$		0	6	V
V_{OD1}	Differential output voltage	$I_O = 0$		1.5	6	V
V_{OD2}	Differential output voltage	See Figure 1		1.5	5	V
I_O	Output current	$V_I = 0.8$ V	$V_O = 12$ V		1	mA
			$V_O = -7$ V		−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V			20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V			−400	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V			−250	mA
		$V_O = 0$			−150	
		$V_O = V_{CC}$			250	
		$V_O = 12$ V			250	
I_{CC}	Supply current (total package)	No load			30	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Differential-output turn-on time	See Figure 3		60	90	ns
t_{off}	Differential-output turn-off time			75	110	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, V_I = −7 V,	V_I = 12 V, See Note 3			1 −0.8	mA
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load				30	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
NOTE 3: This applies for both power on and power off.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{ID} = 0 to 3 V, See Figure 4		21	35	ns
t_{PHL}	Propagation delay time, high-to-low level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 5		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	See Figure 5		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

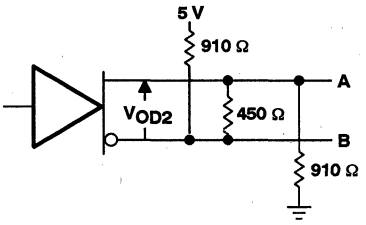


Figure 1. Driver V_{OD2}

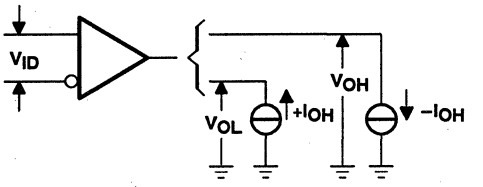
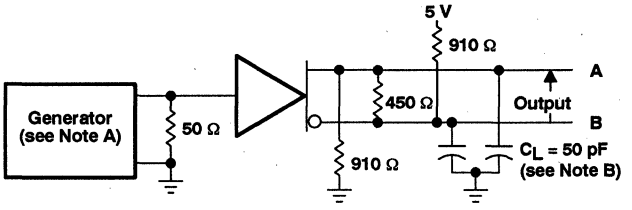
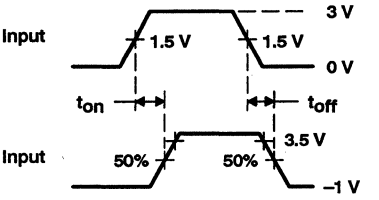


Figure 2. Receiver V_{OH} and V_{OL}

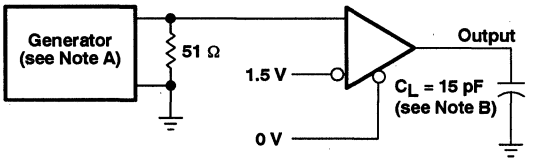


TEST CIRCUIT

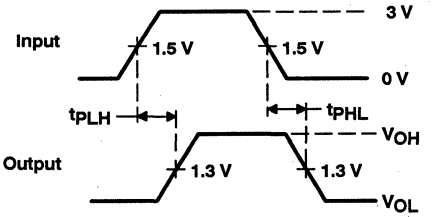


VOLTAGE WAVEFORMS

Figure 3. Driver Differential-Output Delay Times



TEST CIRCUIT



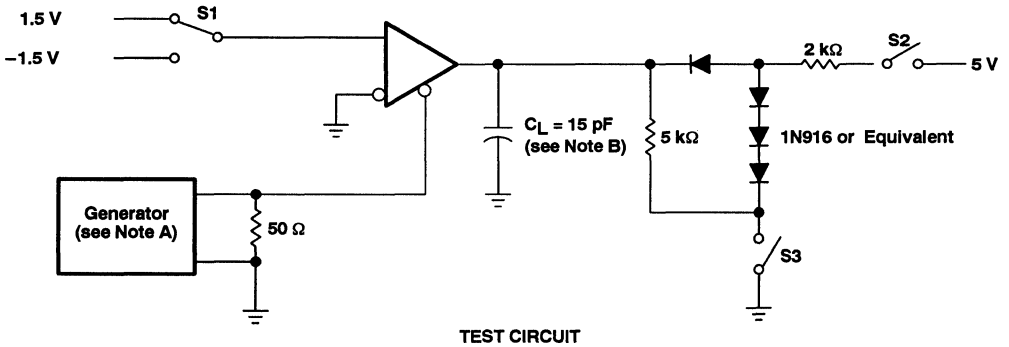
VOLTAGE WAVEFORMS

Figure 4. Receiver Test Circuit and Voltage Waveforms Propagation Delay Times

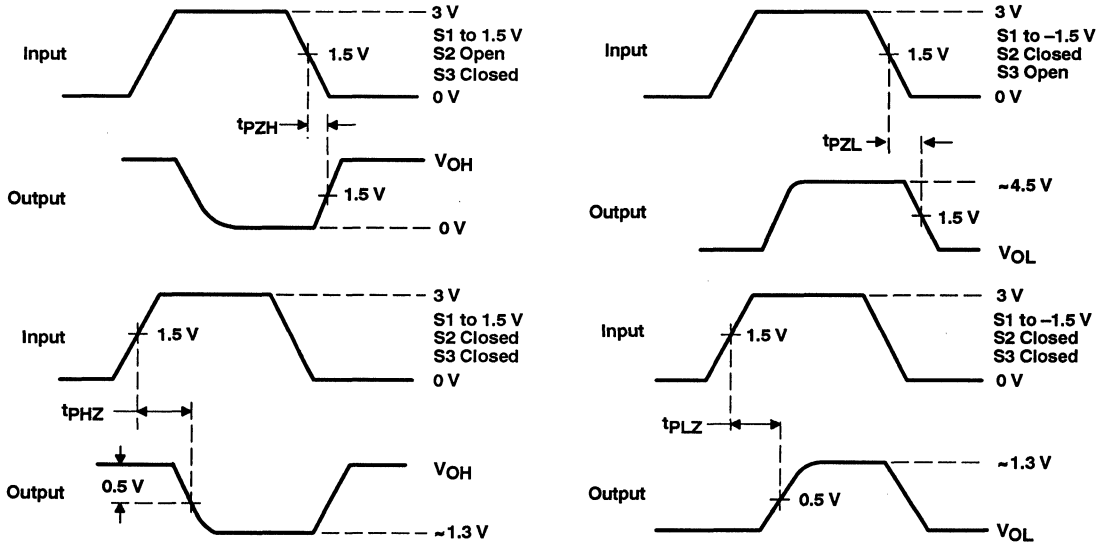
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Receiver Output Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

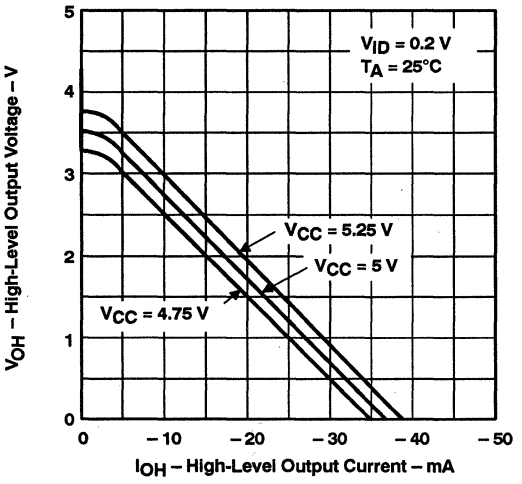


Figure 6

RECEIVER HIGH-LEVEL OUTPUT†
vs
FREE-AIR TEMPERATURE

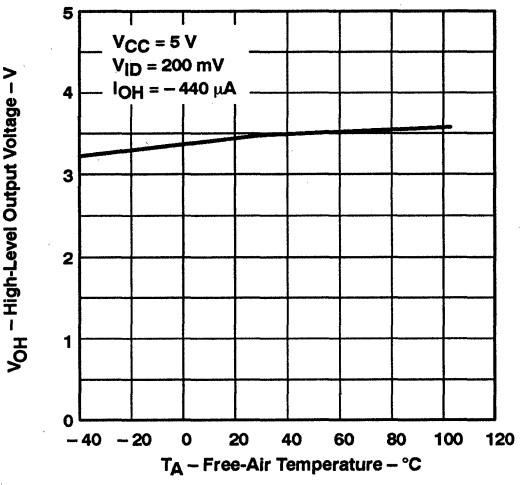


Figure 7

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

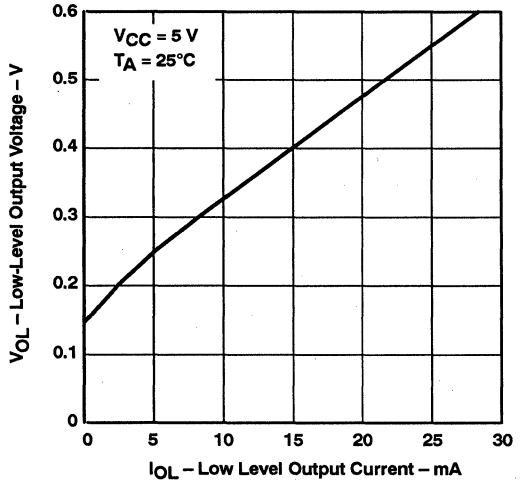


Figure 8

RECEIVER LOW-LEVEL OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

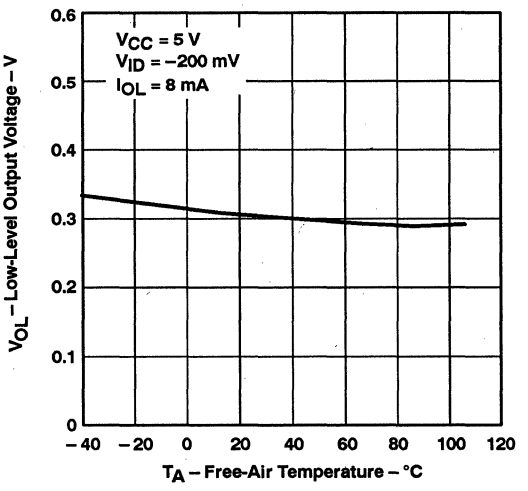


Figure 9

† Only the 0°C to 70°C portion of the curve applies for the SN75076B.

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

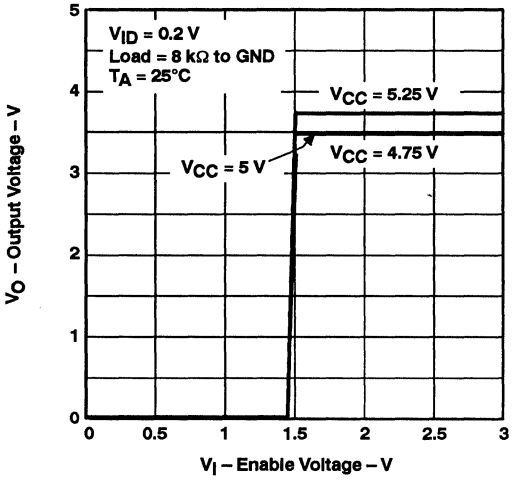


Figure 10

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

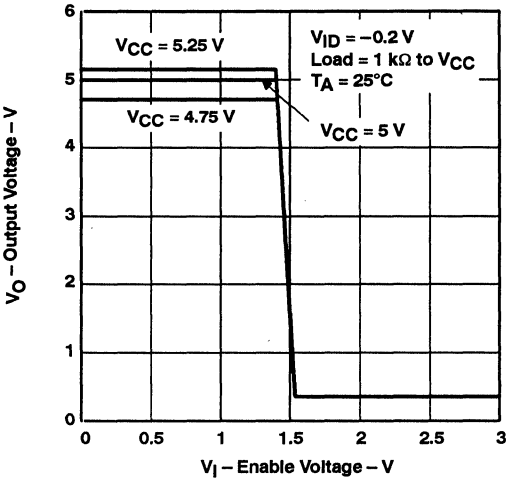


Figure 11

APPLICATION INFORMATION

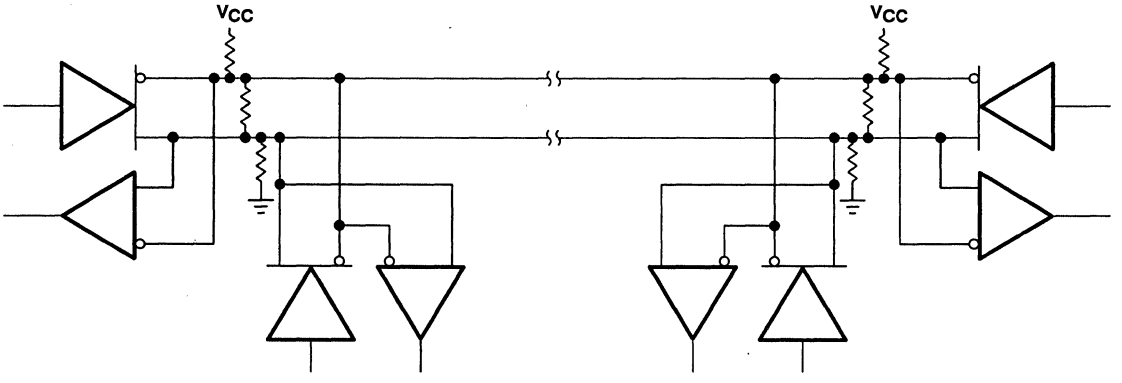
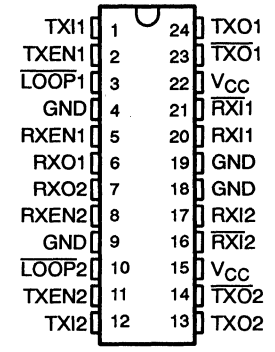


Figure 12. Typical Application Circuit

SLLS054A – D3279, APRIL 1989 – REVISED FEBRUARY 1993

- **Compatible With IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988**
- **Interdevice Loop-Back Paths for System Testing**
- **Squelch Function Implemented on the Receiver Inputs**
- **Drivers Will Drive a Balanced 78-Ω Load**
- **Transformer Coupling Not Required in System**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Isolated Ground Pins for Reduced Noise Coupling**
- **Fault-Condition Protection Built Into the Device**
- **Driver Inputs Are Level-Shifted ECL Compatible**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN75ALS085 is a monolithic, high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device drive a 78-Ω balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs will rise to full-amplitude output levels within 25 ns. The output amplitude is maintained for the remainder of the packet. After the last positive packet edge is transmitted into the driver, the driver will maintain a minimum of 70% full differential output for a minimum of 200 ns, then decay down to a minimum level for the reset (idle) condition within 8 μs. Disabling the driver by taking the driver enable low will also force the output into the idle condition after the normal 8-μs timeout. While operating, the driver is able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers power up in the idle state to ensure that no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This ensures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shutdown and line-idle conditions. The RXO outputs default to a high level and the RXEN outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch will become active within 50 ns when the input squelch threshold is exceeded. RXEN will be driven high when the squelch circuit is allowing data to pass through the receiver. The receiver squelch circuit can also withstand a set of fault conditions while operating without causing permanent damage to the device.

description (continued)

The purpose of the loop functions is to provide a means by which system data path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When $\overline{\text{LOOP1}}$ is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored and a path from TXI1 to RXO1 is established. When $\overline{\text{LOOP1}}$ is taken back high, driver 1 and receiver 1 revert back to their normal operation. When $\overline{\text{LOOP2}}$ is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective receiver enable output (RXEN) will reflect the status of TXEN1.

Function Tables

RECEIVER – $\overline{\text{LOOP}}$ = H

			OUTPUTS	
RXI		PREVIOUS RXEN	RXEN	RXO
V_{ID} = 1315 mV to –175 mV,	t_w < 25 ns	L	L	H
V_{ID} = –275 mV to –1315 mV,	t_w > 50 ns	X	H	L
V_{ID} = 318 mV to 1315 mV,	t_w < 142 ns	H	H	H
V_{ID} = 318 mV to 1315 mV,	t_w > 187 ns	X	L	H

DRIVER – $\overline{\text{LOOP}}$ = H

TXI	TXEN	PREVIOUS TXO	OUTPUT TXO
L	L	Idle	Idle
H	L	Idle	Idle
↓	H	Idle	L
L	H	Active	L
H < 260 µs	H	Active	H
H > 8 µs	H	Active	Idle
L	L > 8 µs	Active	Idle
H < 260 ns	L > 8 µs	Active	Idle
H < 260 ns	L < 260 ns	Active	H
H > 8 µs	L < 260 ns	Active	Idle
L	L < 260 ns	Active	L

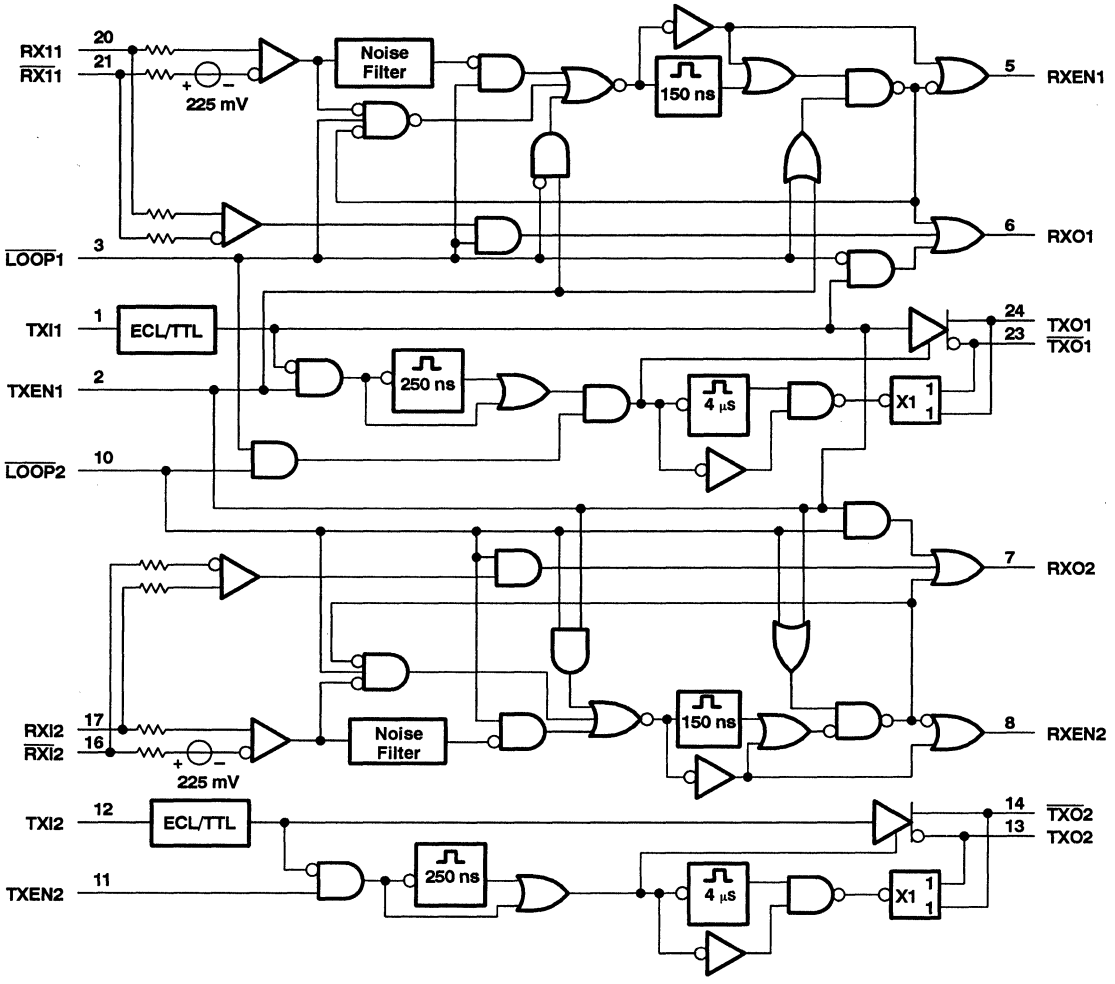
H = $V_I \geq V_T$ max, L = $V_I \leq V_T$ min

LOOP

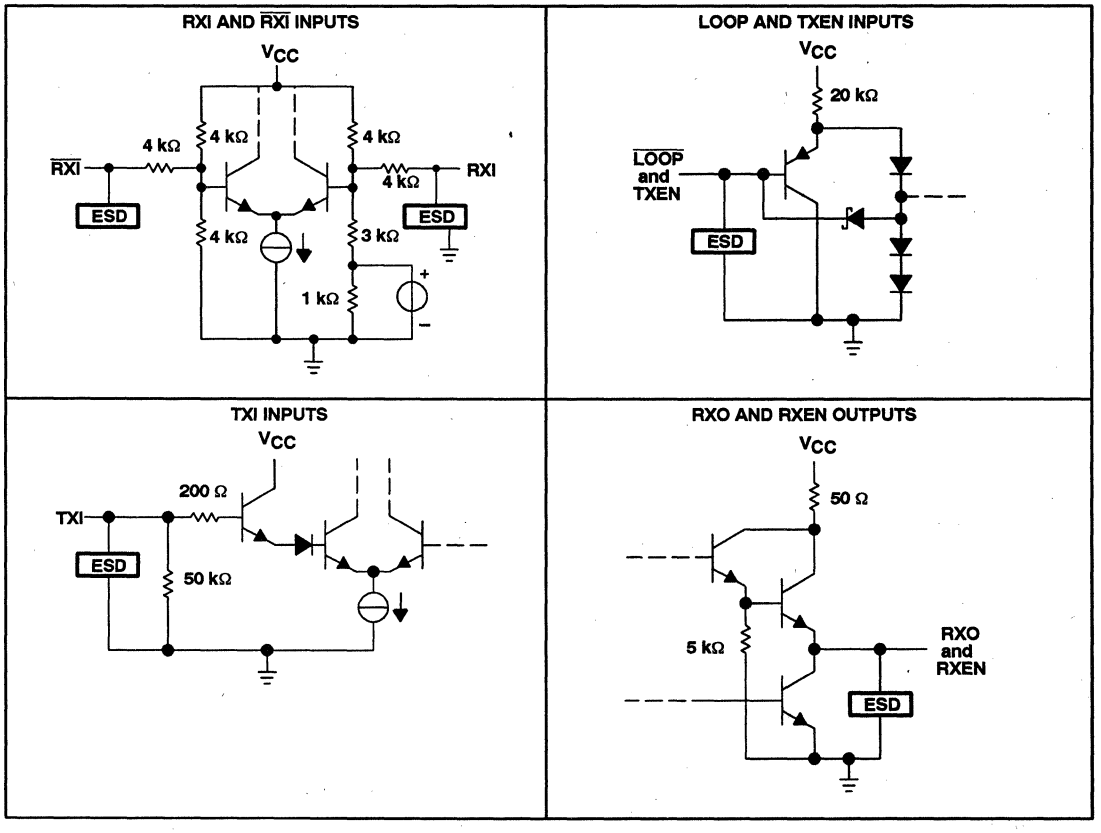
INPUTS						OUTPUTS				
$\overline{\text{LOOP1}}$	$\overline{\text{LOOP2}}$	TXI1	TXEN1	RXI1	RXI2	RXO1	RXO2	RXEN1	RXEN2	TXO1
L	L	L	H	X	X	L	L	H	H	Idle
L	L	H	H	X	X	H	H	H	H	Idle
L	L	X	L	X	X	H	H	L	L	Idle
L	H	L	H	X	Normal	L	Normal	H	Normal	Idle
L	H	H	H	X	Normal	H	Normal	H	Normal	Idle
L	H	X	L	X	Normal	H	Normal	L	Normal	Idle
H	L	L	H	Normal	X	Normal	L	Normal	H	Idle
H	L	H	H	Normal	X	Normal	H	Normal	H	Idle
H	L	X	L	Normal	X	Normal	H	Normal	L	Idle
H	H	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

H = high level, L = low level, X = don't care

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
TXI and $\overline{LOOP}$ input voltage ..... 5.5 V
TXO and $\overline{TXO}$ output voltage ..... 16 V
RXI and $\overline{RXI}$ input voltage ..... 16 V
RXO and RXEN output voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
NT	1250 mW	10.0 mW/°C	800 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode voltage at RXI inputs, V_{IC}	1		4.2	V
Differential voltage between RXI inputs, V_{ID}	± 318		± 1315	mV
High-level input voltage, $\overline{LOOP}$ and TXEN, V_{IH}	2			V
Low-level input voltage, $\overline{LOOP}$ and TXEN, V_{IL}			0.8	V
High-level output current, RXO and RXEN, I_{OH}			– 0.4	mA
Low-level output voltage, RXO and RXEN, I_{OL}			16	mA
Setup time, driver mode, TXEN high before TXI↓, t_{su1} (see Figure 8)	10			ns
Setup time, loop mode, $\overline{LOOP}$ low before TXEN↑, t_{su2} (see Figure 10)	15			ns
Setup time, loop mode, TXEN high before TXI↓, t_{su3} (see Figure 10)	10			ns
Hold time, loop mode, TXEN high after TXI↑, t_{h1} (see Figure 9)	10			ns
Hold time, loop mode, $\overline{LOOP}$ low after TXEN↓, t_{h2} (see Figure 9)	15			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Clamp voltage at all inputs		I_I = –18 mA			–1.5	V
V_T	Driver input (TXI) threshold voltage		T_A = 0°C	V_{CC} = 4.75 V	3.202	3.752	V
				V_{CC} = 5 V	3.389	3.998	
				V_{CC} = 5.25 V	3.577	4.244	
			T_A = 25°C	V_{CC} = 4.75 V	3.213	3.797	V
				V_{CC} = 5 V	3.400	4.043	
				V_{CC} = 5.25 V	3.588	4.289	
			T_A = 70°C	V_{CC} = 4.75 V	3.239	3.849	V
				V_{CC} = 5 V	3.426	4.095	
				V_{CC} = 5.25 V	3.614	4.341	
V_{IDT}	Receiver differential input threshold voltage					–275	mV
V_{OC}	Driver output (TXO) common-mode voltage	Idle	TXEN at 0.8 V, $\overline{LOOP}$2 at 2 V,	$\overline{LOOP}$1 at 2 V, See Figure 1	1	4.2	V
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 3.2 V,	1	4.2	
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 4.4 V,	1	4.2	
V_{OD}	Driver output (TXO) differential voltage	Idle	TXEN at 0.8 V, $\overline{LOOP}$2 at 2 V,	$\overline{LOOP}$1 at 2 V, See Figure 1		±40	mV
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 3.2 V,	–600	1315	
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 4.4 V,	600	1315	
V_{OH}	High-level output voltage	RXO, RXEN	I_{OH} = –0.4 mA		2.4		V
V_{OL}	Low-level output voltage	RXO, RXEN	I_{OL} = 16 mA			0.5	V
I_{IH}	High-level input current	TXEN, $\overline{LOOP}$	V_I = 2 V			20	µA
		TXI	V_I = 4.5 V			400	
		$\overline{RXI}$, RXI	V_{ID} = –0.5 V,	V_{IC} = 1 V to 4.2 V		1000	
I_{IL}	Low-level input current	TXEN, $\overline{LOOP}$	V_I = 0.8 V			–200	mA
		TXI	V_I = 3.1 V			100	
			V_I = 0.3 V		4	10	
		$\overline{RXI}$, RXI	V_{ID} = 0.5 V,	V_{IC} = 1 V to 4.2 V		1000	
I_{OD}	Driver differential output current	Idle	TXEN at 0.8 V, $\overline{LOOP}$2 at 2 V,	$\overline{LOOP}$1 at 2 V, See Figure 2		±4	mA
I_{OS}	Short-circuit output current†	RXO, RXEN	V_O at 0 V, RXI at 2 V	$\overline{RXI}$ at 3 V,	–40	–150	mA
I_{CC}	Supply current		$\overline{LOOP}$2 at 2 V, TXI at 4.5 V,	TXEN at 2 V, Outputs open		225	mA

† Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†			MIN	MAX	UNIT
Driver fault condition current	TXO shorted to $\overline{\text{TXO}}$,	Current measured in short			150	mA
	TXO at 0 V,	$\overline{\text{TXO}}$ is open,	Current measured at TXO		150	
	TXO is open,	$\overline{\text{TXO}}$ at 0,	Current measured at $\overline{\text{TXO}}$		150	
	TXO at 0 V,	$\overline{\text{TXO}}$ at 0 V,	Current measured at TXO and $\overline{\text{TXO}}$		150	
	TXO at 16 V,	$\overline{\text{TXO}}$ is open,	Current measured at TXO		150	
	TXO is open,	$\overline{\text{TXO}}$ at 16 V,	Current measured at TXO		150	
	TXO at 16 V,	$\overline{\text{TXO}}$ at 16 V,	Current measured at TXO and $\overline{\text{TXO}}$		150	
Receiver fault condition current	RXI shorted to $\overline{\text{RXI}}$,	Current measured in short			10	mA
	RXI at 0 V,	$\overline{\text{RXI}}$ is open,	Current measured at RXI		3	
	RXI is open,	$\overline{\text{RXI}}$ at 0 V,	Current measured at RXI		3	
	RXI at 0 V,	$\overline{\text{RXI}}$ at 0 V,	Current measured at RXI and $\overline{\text{RXI}}$		3	
	RXI at 16 V,	$\overline{\text{RXI}}$ at open,	Current measured at RXI		10	
	RXI at open,	$\overline{\text{RXI}}$ at 16 V,	Current measured at $\overline{\text{RXI}}$		10	
	RXI at 16 V,	$\overline{\text{RXI}}$ at 16 V,	Current measured at RXI and $\overline{\text{RXI}}$		10	

† Fault conditions should be measured on only one channel at a time.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		15	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		15	ns
t_{PIL}	Propagation delay time, idle-to-low level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 4		25	ns
t_{PIL}	Propagation delay time, idle-to-low level output	TXEN	TXO, $\overline{TXO}$	TXI at 3.2 V, See Figure 5		25	ns
t_w	Output pulse duration from low-to-high level to 70% output level		TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6	260	8000	ns
$V_{OD(U)}$	Driver output differential undershoot voltage	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6		–100	mV
t_{skew}	Driver caused signal skew $t_{PLH} - t_{PHL}$	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		±3	ns
t_r	Rise time, TXO, $\overline{TXO}$			TXEN at 2 V, See Figure 3	1	5	ns
t_f	Fall time, TXO, $\overline{TXO}$			TXEN at 2 V, See Figure 3	1	5	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, See Figure 11		15	ns
t_{PHL}	Propagation delay time, high-to-low level output	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, See Figure 10		15	ns
t_{PLH}	Start-up delay time, low-to-high level output	$\overline{RXI}$, RXI	RXEN	V_{IC} = 1 V to 4.2 V, V_{ID} = –500 mV, See Figure 12		55	ns
t_{PHL}	Shutdown delay time, high-to-low level output	$\overline{RXI}$, RXI	RXEN	V_{IC} = 1 V to 4.2 V, V_{ID} = 500 mV, See Figure 12	142	181	ns
t_{skew}	Receiver caused signal skew ($t_{PLH} - t_{PHL}$)	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, V_{ID} = 500 mV, See Figure 10		±3	ns
t_w	Pulse duration at $\overline{RXI}$ and RXI (to not activate squelch)			V_{IC} = 1 V to 4.2 V, V_{ID} = –175 mV, See Figure 11	25		ns
t_w	Pulse duration at $\overline{RXI}$ and RXI (to activate squelch)			V_{IC} = 1 V to 4.2 V, V_{ID} = –275 mV, See Figure 11		50	ns
t_{r1}	Rise time, RXO			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 10	1	8	ns
t_{r2}	Rise time, RXEN			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 12	1	8	ns
t_{f1}	Fall time, RXO			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 10	1	8	ns
t_{f2}	Fall time, RXEN			V_{IC} = 2.5 V, V_{ID} = ±500 V, See Figure 12	1	8	ns
t_{valid}	RXO valid after RXEN high			See Figure 10	–10	15	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

loop

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t_{PLH}	Propagation delay time, low-to-high level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 14		50	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 14		50	ns

PARAMETER MEASUREMENT INFORMATION

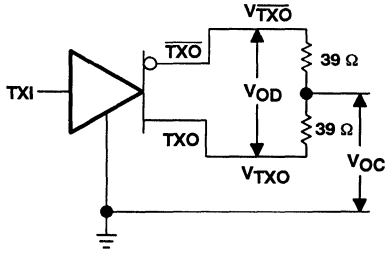


Figure 1

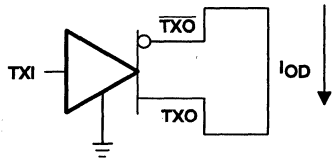
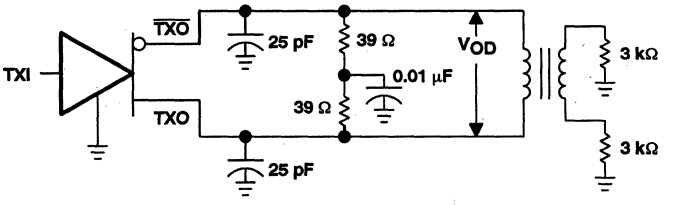
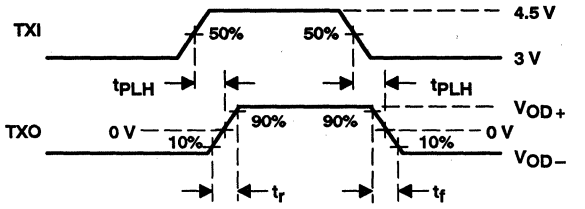


Figure 2

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



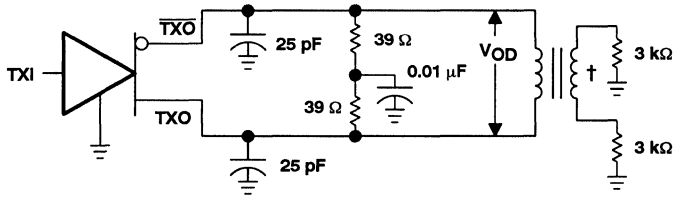
VOLTAGE WAVEFORMS

TRANSFORMER SPECIFICATIONS

Turns Ratio	1:1
Magnetizing Inductance	26 to 30 μH
Winding Resistance	0.6 Ω Max
Rise Time 10% to 90%	5 ns Max
Interwinding Capacitance	25 pF
Leakage Inductance	0.25 μH Max
Inductive Q	1250 Min

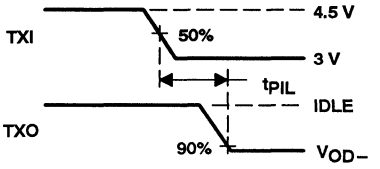
Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† See Figure 3

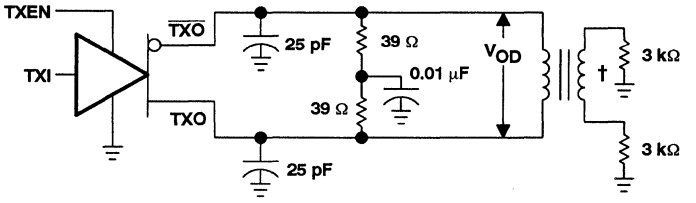
TEST CIRCUIT



VOLTAGE WAVEFORMS

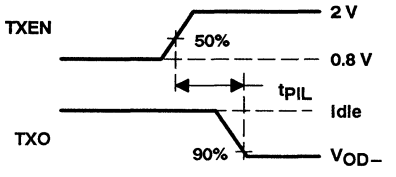
NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 4. Test Circuit and Voltage Waveforms



† See Figure 3

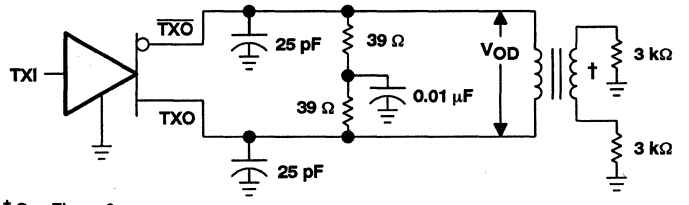
TEST CIRCUIT



VOLTAGE WAVEFORMS

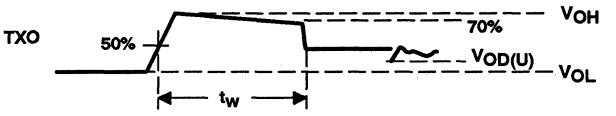
Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† See Figure 3

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6. Test Circuit and Voltage Waveforms

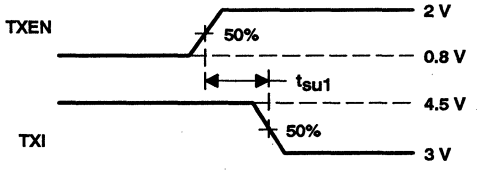


Figure 7

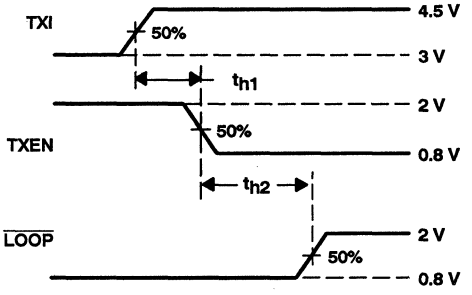


Figure 8

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

PARAMETER MEASUREMENT INFORMATION

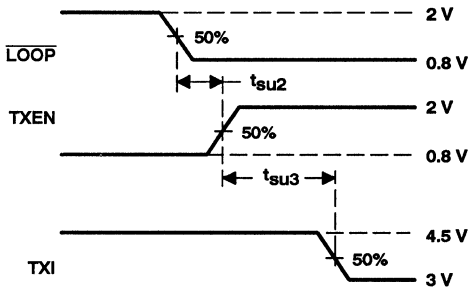
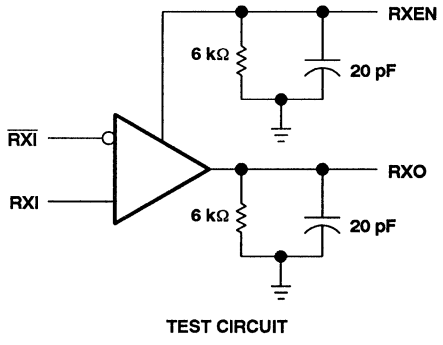
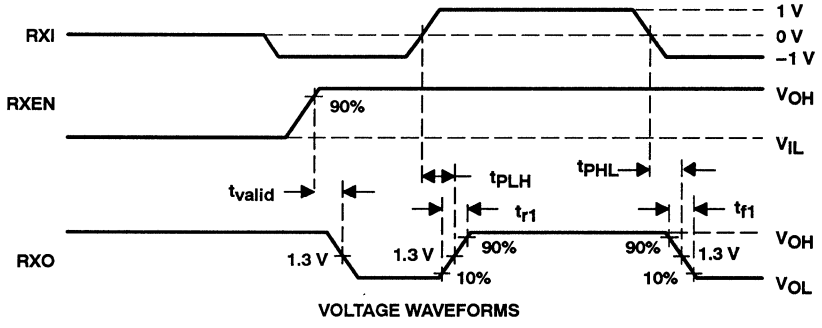


Figure 9



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 10. Test Circuit and Voltage Waveforms

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

PARAMETER MEASUREMENT INFORMATION

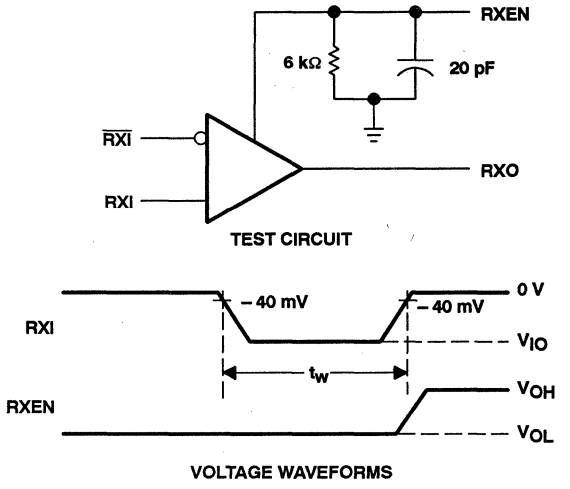


Figure 11. Test Circuit and Voltage Waveforms

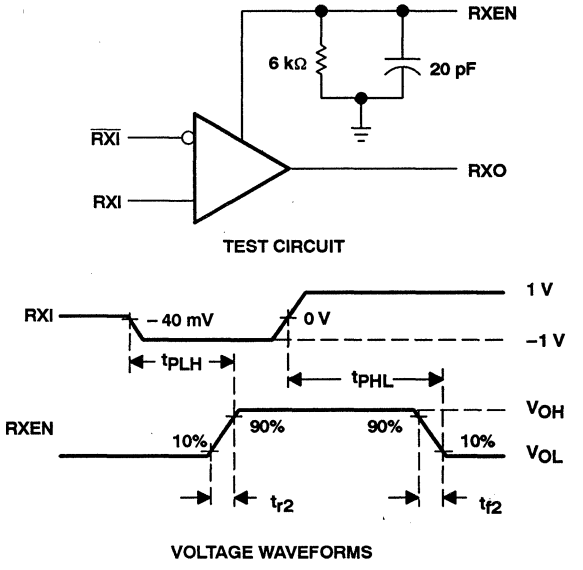


Figure 12. Test Circuit and Voltage Waveforms

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

PARAMETER MEASUREMENT INFORMATION

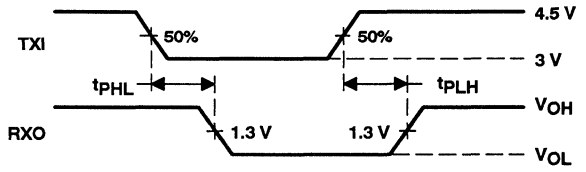


Figure 13

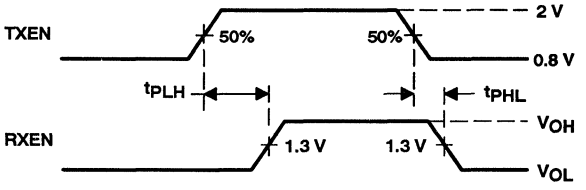
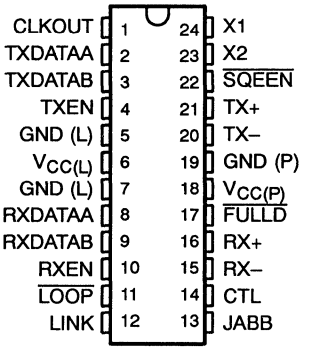


Figure 14

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

- **Compliant With IEEE STD 802.3I, Type 10BASE-T**
- **Differential (Twisted-Pair) I/O Driver/Receiver**
- **High-Speed Receiver . . . t_{pd} = 50 ns Max**
- **Receiver Squelch Circuit Integrity Improved With Noise Filter**
- **Jabber Control Prevents Network Lockup**
- **Collision Detection for Multiple-User Networks**
- **Data Link Integrity Monitored With Link Test Pulse**
- **Externally Addressable Test Register Controls Signal Quality Error Testing**
- **CMOS and Raised ECL Compatible**
- **24-Pin, 300-mil Dual-In-Line Package**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC086 is a single-channel differential driver/receiver interface device for the medium attachment unit (MAU) used in 10-MHz twisted-pair Ethernet applications. The device uses a 5-V supply and is designed to interface with two pairs of telephone-grade twisted-pair cables coupled through isolation transformers. The functional components of the device include a differential receiver and driver, receiver squelch with noise filter, jabber controls, collision detection, data link monitor, and signal quality error (SQE) testing. The LinBiCMOS™ process technology is used in the device design to ensure analog precision, low power, and high-speed operation.

The device contains an elaborate receiver-squelch circuit† that provides an improved level of noise rejection by qualifying the incoming signal stream with three different criteria. First, the signal is compared to a set threshold voltage level. Then, the pulse duration is compared to a set time window. Last, the signal must follow a set pattern of positive and negative pulses before the circuit finally opens the receiver channel to the incoming data packet.

The jabber control is designed to prevent a defective controller from locking up the network by limiting the data packet transmission time to 20 to 30 ms. When a packet length exceeds 20 to 30 ms, the driver is turned off for about 600 ms. The driver-enable input must be made inactive by the controller during this period before the jabber control will release the driver. The JABB output is active (high) when a jabber condition exists.

Collision detection is used to arbitrate access to the multiuser network. This detection is done logically by monitoring the receive line for a valid signal during a driver transmission. When a collision is detected, this device informs the controller with an active-high CTL output. After a valid packet transmission, the device also performs a signal quality error test causing the CTL output to go active (high). This test is disabled when the $\overline{\text{SQEEN}}$ input goes inactive (high).

The device tests data-link integrity during the idle state by periodically driving the driver line with a unipolar pulse called a link-test pulse. The receiver looks for this link-test pulse on the receive line. A failed line link is indicated by a high-impedance state at the LINK output. This output drives an LED for monitoring if needed.

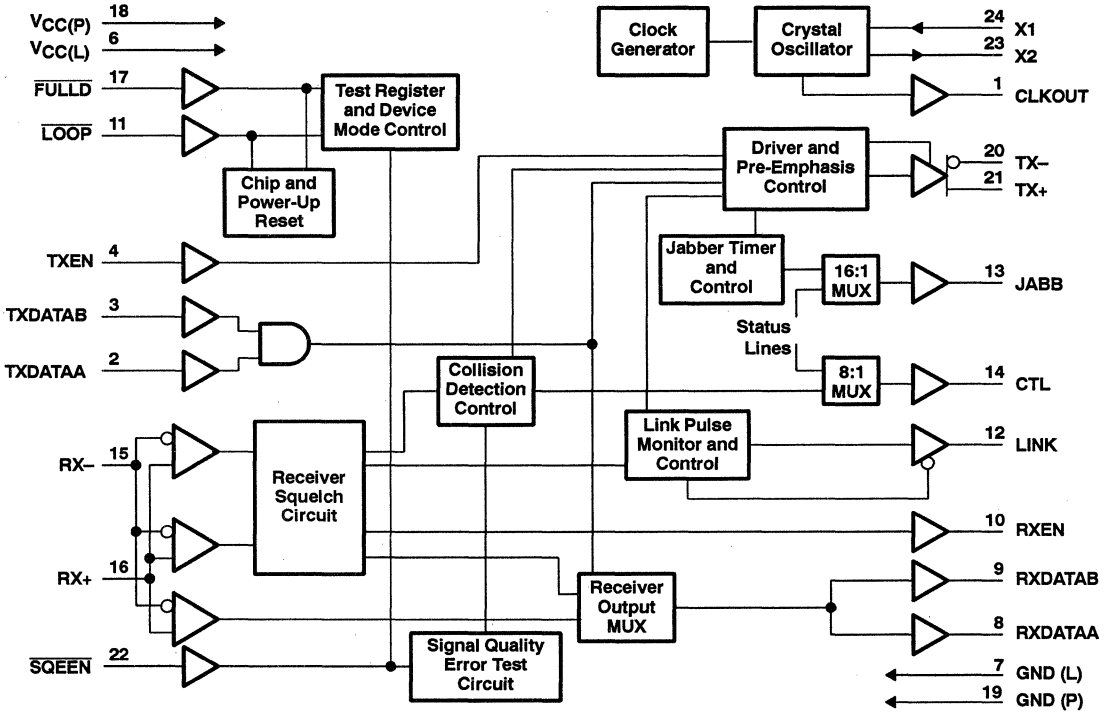
† Embodies technology covered by one or more Digital Equipment Corporation Patents.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

An internal test register is externally controlled with inputs $\overline{\text{FULLD}}$ and $\overline{\text{LOOP}}$ to select the device testing mode. When in the test mode, serial test-mode control patterns are clocked into the test register through input $\overline{\text{SQEEN}}$. These control patterns select various modes to test the internal circuits.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

NAME	PIN LEVEL	PIN NO.	I/O	DESCRIPTION
CLKOUT	CMOS	1	O	Clock output. This 10-MHz buffered clock is provided for driving other interface devices.
CTL	CMOS	14	O	Control. In normal mode, CTL high indicates a collision. In test mode, status lines are muxed out.
$\overline{\text{FULLD}}$	TTL	17	I	Full-duplex mode. When active (low), the device is placed in the full-duplex operating mode for simple point-to-point communication applications. In the full-duplex mode, the receiver and driver are both active with collision detection disabled. After $\overline{\text{LOOP}}$ and $\overline{\text{FULLD}}$ go active (low), in that order, a device reset is initiated and while both are active (low), test select data is clocked into the test register using a 100-ns clock at the X1 input. This terminal is held inactive (high) due to an internal pullup resistor.
GND (L)	GROUND	5 7		Logic grounds. These terminals provide a ground return for the CMOS core logic.
GND (P)	GROUND	19		Power ground. This provides a ground return for the input and output buffers, driver (transmitter), and receiver circuits.
JABB	CMOS	13	O	Jabber control. When a jabber condition exists during normal mode operation, this signal goes active (high) to report jabber-control status to the controller. In the test mode, this provides a multiplexed signal for internal timer and counter functions.
LINK	CMOS	12	O	Link status. This 3-state output indicates the status of the receiver and interface link. When driving an LED (with anode to resistor to V_{CC}), a high-impedance level indicates a failed link and the LED is off. A momentary high level indicates the device is receiving valid data and the LED is blinking on and off. A continuous low level indicates the device is receiving valid link pulses but no data, and the LED is on.
$\overline{\text{LOOP}}$	TTL	11	I	Loop-back mode. When the device is in the normal operating mode (not test mode) and $\overline{\text{LOOP}}$ is active (low), the driver (transmit) data is directed to the receive data path to put the device in the loop-back mode and the driver is turned off. After $\overline{\text{LOOP}}$ and $\overline{\text{FULLD}}$ go active (low), in that order, a device reset is initiated and while both are active (low), test select data is clocked into the test register using a 100-ns clock at the X1 input. This terminal is held inactive (high) due to an internal pullup resistor.
RX+		16	I	Differential receiver inputs
RX–		15	I	
RXEN	CMOS	10	O	Receiver squelch status. This provides squelch status information to the controller. When active (high), this signal indicates that the data path is valid or open from the receive channel through the device. An inactive (low) indicates that the receive channel is squelched or closed. This signal is capable of driving an LED monitor.
RXDATAA RXDATAB	CMOS ECL	8 9	O O	Received-data serial outputs. These provide a choice of logic levels and serial data either from the differential receiver input (RX+ and RX–) or data from the controller (TXDATAA or TXDATAB) when in the loop-back mode. When the receiver is idle, these output levels are normally high. These terminals are held inactive (high) due to an internal pullup resistor.
$\overline{\text{SQEEN}}$	TTL	22	I	Signal-quality error-test enable. In normal operating mode, this enables the SQE test function performed at the end of a data packet transmission. In the test mode, $\overline{\text{SQEEN}}$ is used (with X1 clock) as a serial data input port to load test patterns or selections into the test register. This terminal is held inactive (high) due to an internal pullup resistor.
TX+		21	O	Differential driver outputs
TX–		20	O	
TXEN	TTL	4	I	Transmitter (driver) enable. When TXEN is active (high), serial data at the TXDATA inputs starts and stops the driver. When TXEN is inactive (low), the driver begins transmitting an idle signal independent of the TXDATA inputs.
TXDATAA TXDATAB	CMOS ECL	2 3	I I	Transmit-data inputs. A choice of logic-level inputs provide Manchester-encoded serial data to the driver. Internal pullup resistors are included.
$V_{CC(L)}$	SUPPLY	6		V_{CC} logic power supply. This provides power to the CMOS core logic.
$V_{CC(P)}$	SUPPLY	18		V_{CC} power supply. This provides power to the input and output buffers, drivers, and receivers.
X1 X2	CMOS	24 23	I O	Crystal input/output. X1 provides an input from an external 10-MHz crystal or another external clock source if the crystal is disconnected. X2 provides an oscillator output.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 5.5 V
Output voltage range at any output, V_O ..... −0.5 V to 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to device ground pins GND(L) and GND(P) shorted together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
High-level output voltage, V_{IH}	TXDATAA, X1		3.15			V
	TXDATAB (see Figure 1)	$T_A = 0°C$	$0.984V_{CC}-0.922$		$0.984V_{CC}-0.763$	
		$T_A = 25°C$	$0.984V_{CC}-0.877$		$0.984V_{CC}-0.727$	
		$T_A = 70°C$	$0.984V_{CC}-0.825$		$0.984V_{CC}-0.645$	
	TXEN, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, $\overline{\text{SQEEN}}$		2			
Low-level output voltage, V_{IH}	TXDATAA, X1				0.8	V
	TXDATAB (see Figure 1)	$T_A = 0°C$	$0.75V_{CC}-0.590$		$0.750V_{CC}-0.375$	
		$T_A = 25°C$	$0.75V_{CC}-0.550$		$0.750V_{CC}-0.350$	
		$T_A = 70°C$	$0.75V_{CC}-0.531$		$0.750V_{CC}-0.324$	
	TXEN, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, $\overline{\text{SQEEN}}$				0.8	
Differential input voltage, V_{ID}			0.586		2.8	V
Common-mode input voltage, V_{IC}			1.8		3.2	V
Operating free-air temperature, T_A			0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

drivers

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	CLKOUT, RXDATAA, RXEN, JABB, CTL	I_{OH} = −12 mA		3.7			V
		RXDATAB	See Figure 1	T_A = 0°C	0.984 V_{CC}−0.922		0.984 V_{CC}−0.763	V
				T_A = 25°C	0.984 V_{CC}−0.877		0.984 V_{CC}−0.727	
				T_A = 70°C	0.984 V_{CC}−0.825		0.984 V_{CC}−0.645	
V_{OL}	Low-level output voltage	CLKOUT, RXDATAA, RXEN, JABB, CTL	I_{OL} = 16 mA				0.5	V
		RXDATAB	See Figure 1	T_A = 0°C	0.750 V_{CC}−0.590		0.750 V_{CC}−0.375	V
				T_A = 25°C	0.750 V_{CC}−0.550		0.750 V_{CC}−0.350	
				T_A = 70°C	0.750 V_{CC}−0.531		0.750 V_{CC}−0.324	
		LINK	I_{OL} = 12 mA				0.5	V
V_{OD}	Differential-output voltage (peak)		See Figure 2		2.2		2.8	V
V_{OD}	Differential-output voltage (step)		See Figure 2		1.53		1.982	V
	Common-mode driver impedance	TX+, TX–			2	5	8	Ω

receivers

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	TXDATAA, TXEN, $\overline{LOOP}$, $\overline{FULLD}$, $\overline{SQEEN}$	V_I = 5.25 V			20	μA
		X1				100	
		TXDATAB	V_{IH} = MAX			400	
I_{IL}	Low-level input current	TXDATAA, TXEN, $\overline{LOOP}$, $\overline{FULLD}$, $\overline{SQEEN}$	V_I = 0			−20	μA
		X1				−100	
		TXDATAB	V_{IL} = MIN			−400	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

drivers and receivers

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$V_{CC(L)}$, $V_{CC(P)}$	$V_{CC(L)}$ = 5.25 V, $V_{CC(P)}$ = 5.25 V			180	mA

switching characteristics

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time	RX+, RX–	RXEN	See Figure 4			5 bit times	
t_{pd2}	Propagation delay time at startup	RX+, RX–	RXDATAA or RXDATAB high	See Figure 4			75	ns
$t_{sk(o)}$	Output skew time	RXEN high	RXDATAA or RXDATAB low	See Figure 4			±10	ns
t_{pd3}	Propagation delay time after startup	RX+, RX–	RXDATAA or RXDATAB high	See Figure 4			50	ns
$t_{sk(p)}$	Pulse skew time ($\lvert t_{PLH4} - t_{PHL4} \rvert$)	RX+, RX–	RXDATAA or RXDATAAB	See Figure 4		2		ns
t_{pd4}	Propagation delay time	RX+, RX–	RXEN low	See Figure 5	155		250	ns
t_{pd5}	Propagation delay time	TXDATA or TXDATAB	TX+, TX–	See Figure 6			75	ns
$t_{sk(p)}$	Pulse skew time ($\lvert t_{PLH5} - t_{PHL5} \rvert$)	TXDATAA or TXDATAB	TX+, TX–	See Figure 6		2		ns
t_{pd6}	Propagation delay time in loop mode	TXDATAA or TXDATAB	RXDATAA, RXDATAB	See Figure 7			50	ns
t_{pd7}	Propagation delay time in loop mode	TXEN high	RXEN high	See Figure 7			50	ns
t_{pd8}	Propagation delay time in loop mode	$\overline{\text{LOOP}}$ low	RXEN low	See Figure 7			30	ns
t_{pd10}	Propagation delay time	TXEN low	RXEN low	See Figure 8			350	ns
t_{pd11}	Propagation delay time	TXEN low	TX+, TX– high	See Figure 8			50	ns
t_{p1}	Precompensation pulse duration		TX+, TX–	See Figure 6	45		55	ns
t_{p2}	Receiver link-beat minimum pulse duration			See Figure 9	80		120	ns
t_{en1}	Enable time	TXDATAA or TXDATAB	TX+, TX–	See Figure 6			75	ns
t_{en2}	Enable time	TXEN	TX+, TX–	See Figure 6			75	ns
t_{dis1}	Disable time, caused by TXDATAA or TXDATAB high or TXEN low	TX+, TX– high	TX+, TX– at 585-mV level	See Figure 8	250			ns
t_{pd12}	Propagation delay time to looped RXEN	TXEN high	RXEN high	See Figure 6			100	ns
t_{pd13}	Propagation delay time for looped back data	TXDATAA or TXDATAB	RXDATAA RXDATAB	See Figure 6			75	ns

timing requirements

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Setup time, test mode, $\overline{\text{SQEEN}}$ before X1↑, t_{su1}	See Figure 10	30			ns
Setup time, test mode, $\overline{\text{LOOP}}$ low before FULLD↓, t_{su2}	See Figure 10	25			ns
Hold time, test mode, $\overline{\text{SQEEN}}$ after X1↑, t_{h1}	See Figure 10	25			ns

PARAMETER MEASUREMENT INFORMATION

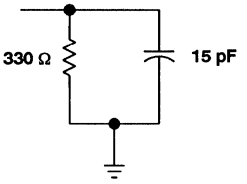


Figure 1. ECL Load Circuit

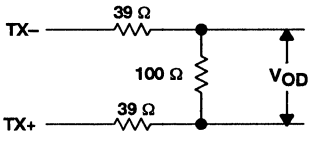


Figure 2. Differential Load Circuit

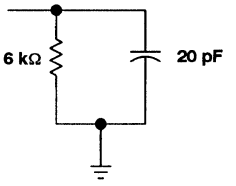


Figure 3. CMOS Load Circuit

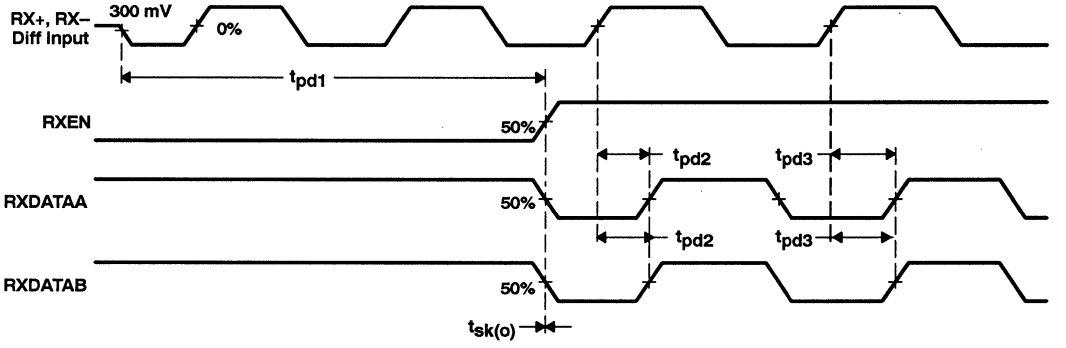


Figure 4. Receiver Startup Waveforms

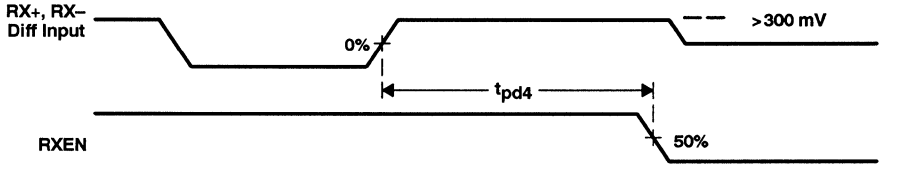


Figure 5. Receiver Shutdown Waveforms

PARAMETER MEASUREMENT INFORMATION

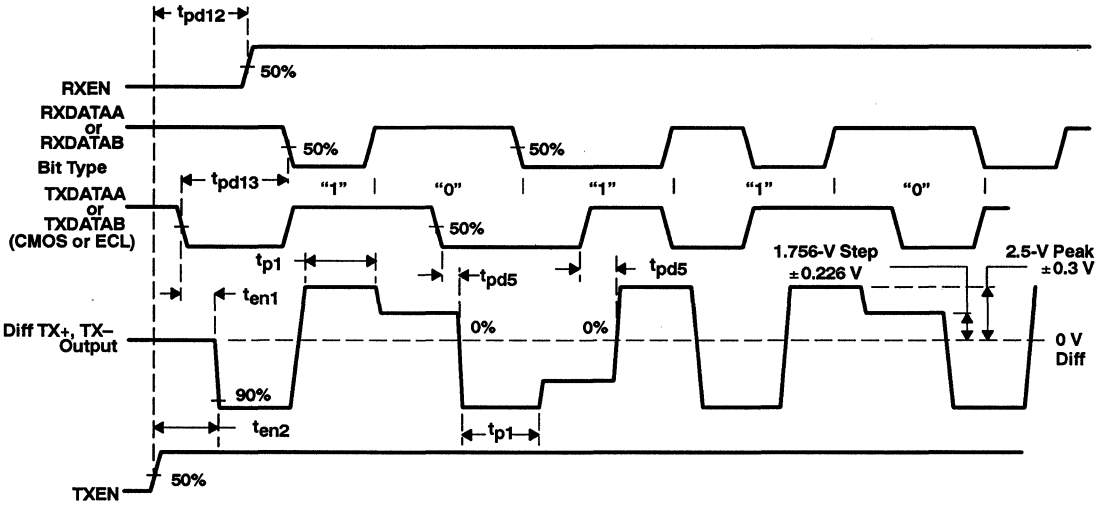


Figure 6. Driver Startup Waveforms

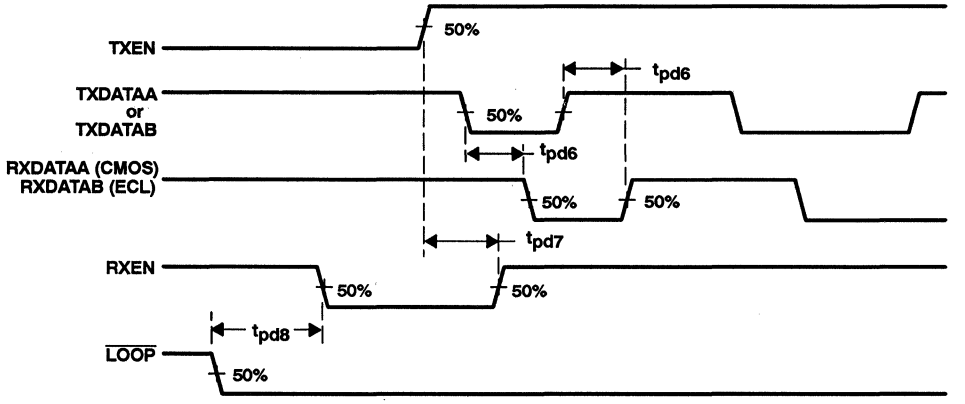


Figure 7. Propagation Delay Waveforms in Loop Mode

PARAMETER MEASUREMENT INFORMATION

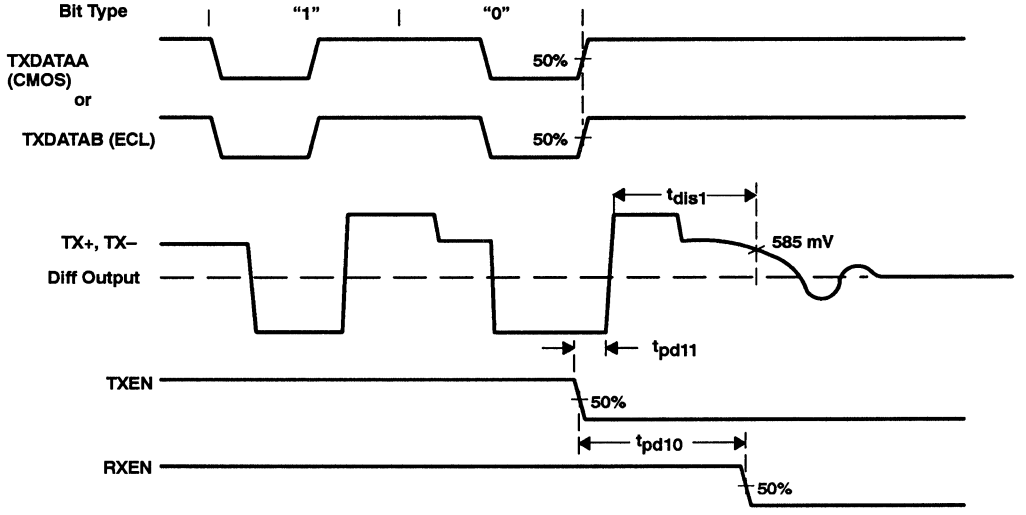


Figure 8. Driver Shutdown Waveforms

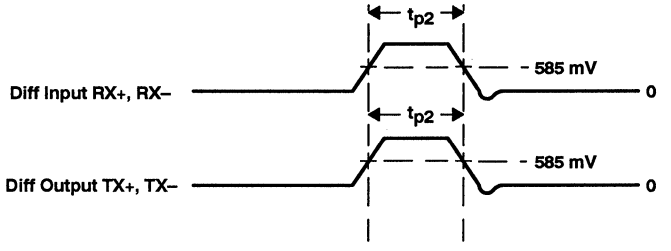


Figure 9. Link Beat Pulse Duration Waveform

PARAMETER MEASUREMENT INFORMATION

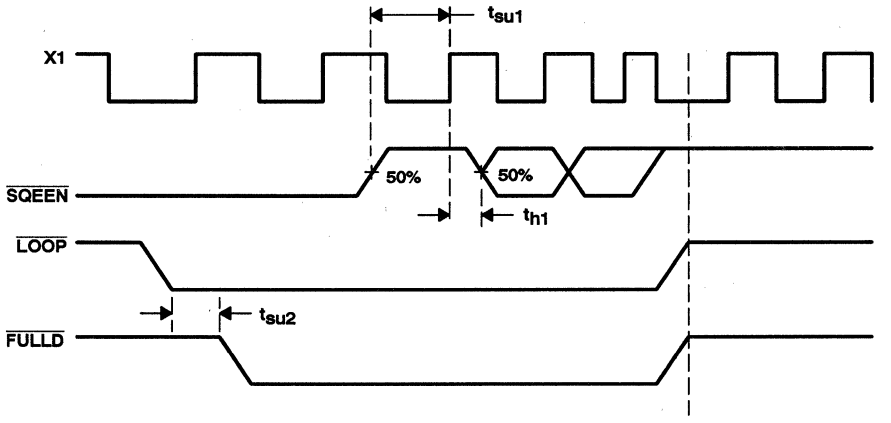
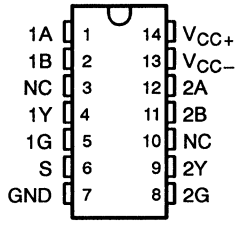


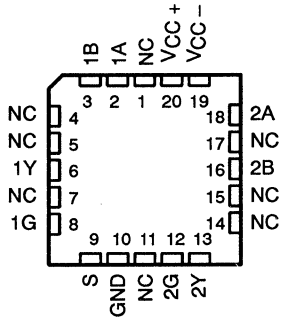
Figure 10. Setup and Hold Time Waveforms

- **High Speed**
- **Standard Supply Voltage**
- **Dual Channels**
- **High Common-Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Differential Common-Mode Input Voltage Range of ±3 V**
- **Strobe Inputs for Receiver Selection**
- **Gate Inputs for Logic Versatility**
- **TTL Drive Capability**
- **High dc Noise Margin**
- **'107A and '107B Have Totem-Pole Outputs**
- **'108A and '108B Have Open-Collector Outputs**
- **B Versions Have Diode-Protected Input for Power-Off Condition**

SN55107A, SN55107B, SN55108A, SN55108B . . . J OR W PACKAGE
SN75107A, SN75107B, SN75108A, SN75108B . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55107A, SN55107B, SN55108A, SN55108B . . . FK PACKAGE
(TOP VIEW)



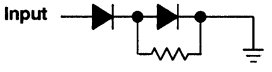
NC – No internal connection

THE SN75108B IS NOT RECOMMENDED FOR NEW DESIGN

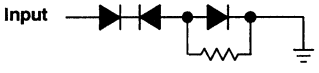
description

These circuits are TTL-compatible high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and are replacements for the SN55107, SN55108, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the A and B versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the B versions. These diodes are useful in certain party-line systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



A Version

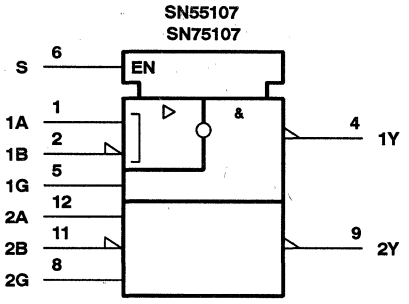


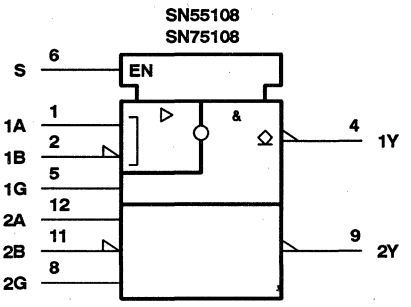
B Version

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 V.

The SN55107A, SN55107B, SN55108A, and SN55108B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75107A, SN75107B, SN75108A, and SN75108B are characterized for operation from 0°C to 70°C.

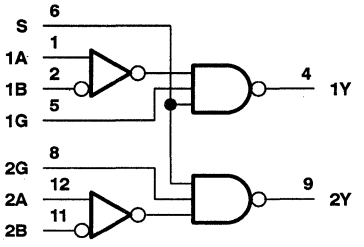
logic symbols†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

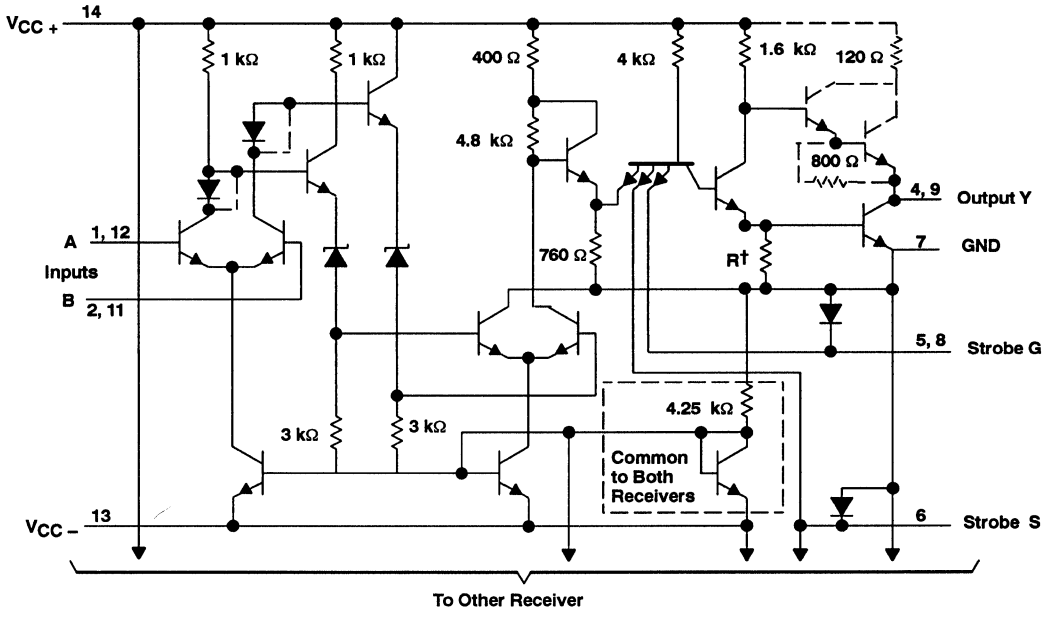


FUNCTION TABLE

DIFFERENTIAL INPUTS A – B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	X	X	H
-25 mV $< V_{ID} < 25$ mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



Pin numbers shown are for D, J, N, and W packages.
† R = 1 kΩ for '107A and '107B, 750 Ω for '108A and '108B.
NOTES: 1. Resistor values shown are nominal.
2. Components shown with dashed lines in the output circuitry are applicable to the '107A and '107B only. Diodes in series with the collectors of the differential input transistors are short circuited on '107A and '108A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 3)	7 V
Supply voltage, V_{CC-}	–7 V
Differential input voltage (see Note 4)	±6 V
Common-mode input voltage (see Note 5)	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range: SN55'	–55°C to 125°C
SN75'	0°C to 70°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package	260°C

NOTES: 3. All voltage values, except differential voltages, are with respect to network ground terminal.
4. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
5. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN5510_A,B)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN7510_A,B)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

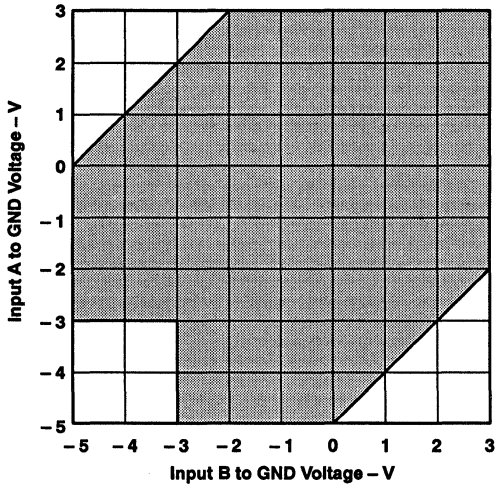
recommended operating conditions (see Note 6)

	SN55107A, SN55107B SN55108A, SN55108B			SN75107A, SN75107B SN75108A, SN75108B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
High-level input voltage between differential inputs, V_{IDH} (see Note 7)	0.025		5	0.025		5	V
Low-level input voltage between differential inputs, V_{IDL} (see Note 7)	−5†		−0.025	−5†		−0.025	V
Common-mode input voltage, V_{IC} (see Notes 7 and 8)	−3†		3	−3†		3	V
Input voltage, any differential input to GND (see Note 8)	−5†		3	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	0		0.8	V
Low-level output current, I_{OL}			−16			−16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for input voltage levels only.

NOTES: 6. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
7. The recommended combinations of input voltages fall within the shaded area of the figure shown.
8. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

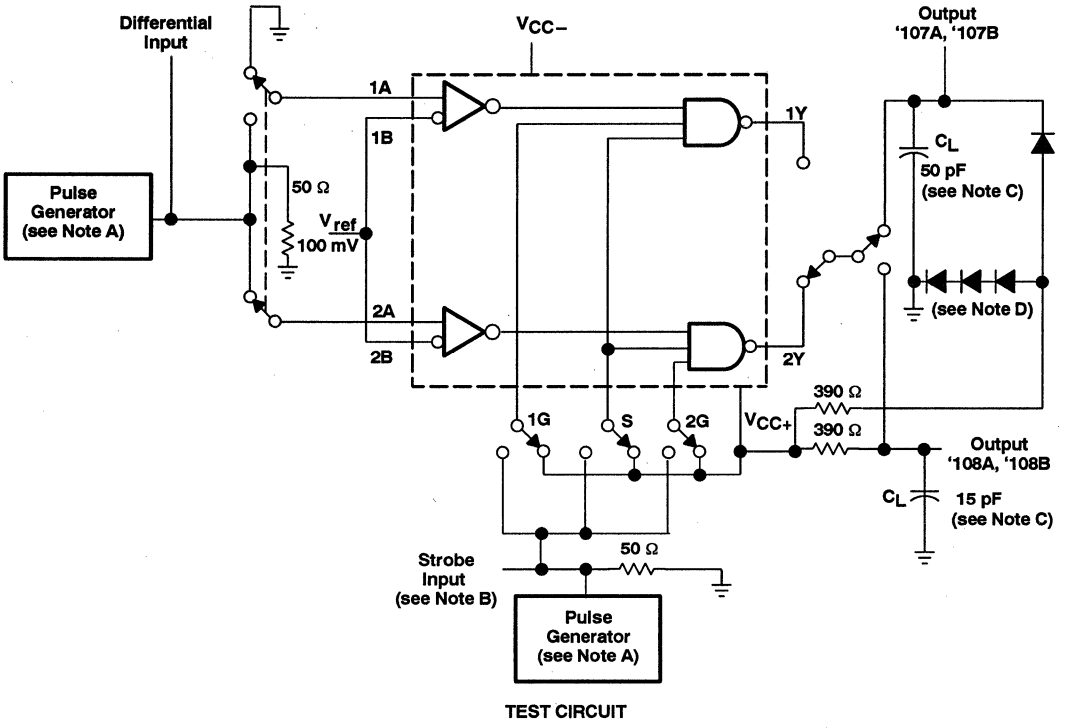
PARAMETER			TEST CONDITIONS†		'107A, '107B MIN	'107A, '107B TYP‡	'107A, '107B MAX	'108A, '108B MIN	'108A, '108B TYP‡	'108A, '108B MAX	UNIT
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 0.8 V, V_{IDH} = 25 mV, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V		2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, V_{IDL} = −25 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4			0.4	V
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(G)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(G)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(G)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current§		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

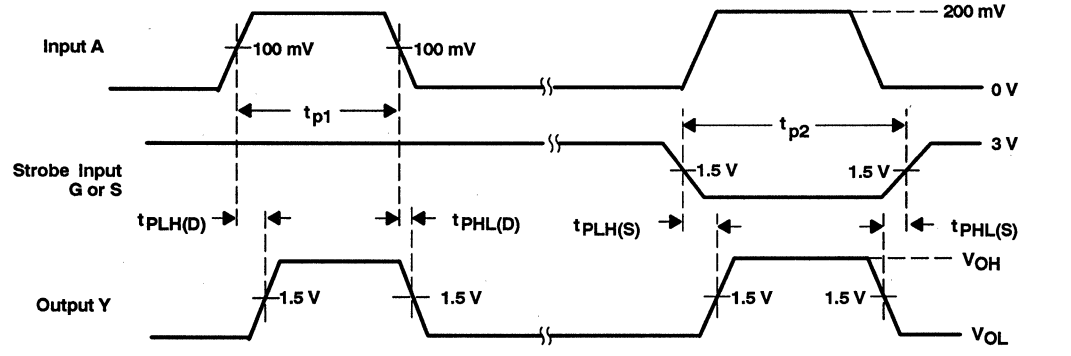
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C, R_L = 390 Ω (see Figure 1)

PARAMETER		TEST CONDITIONS	'107A, '107B MIN	'107A, '107B TYP	'107A, '107B MAX	'108A, 108B MIN	'108A, 108B TYP	'108A, 108B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S	C_L = 50 pF		10	15				ns
		C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S	C_L = 50 pF		8	15				ns
		C_L = 15 pF					13	20	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns, t_f = 10 ± 5 ns, t_{pd1} = 500 ns, PRR ≤ 1 MHz, t_{pd2} = 1 μs, PRR ≤ 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

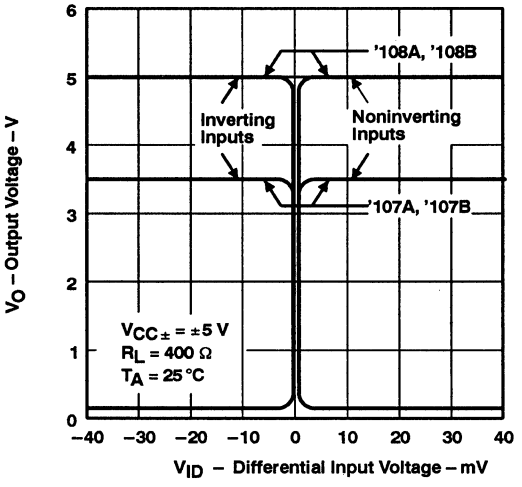


Figure 2

HIGH-LEVEL INPUT CURRENT INTO 1A OR 2A
vs
FREE-AIR TEMPERATURE

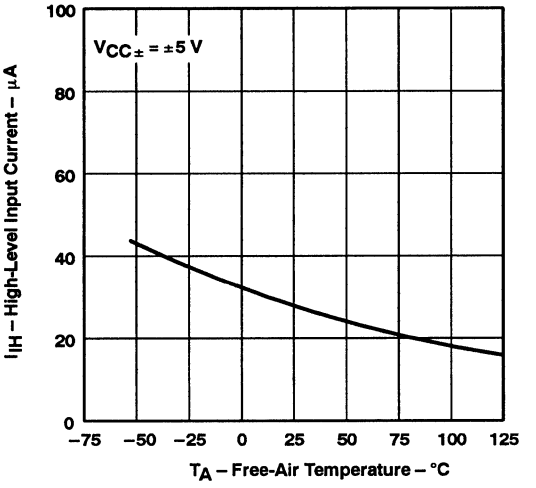


Figure 3

SUPPPLY CURRENT, OUTPUTS HIGH
vs
FREE-AIR TEMPERATURE

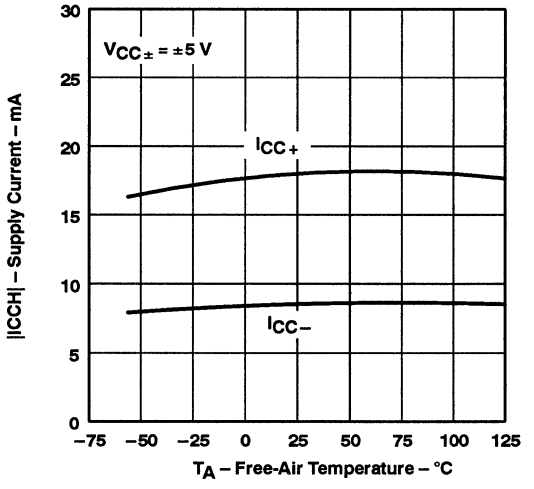


Figure 4

PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

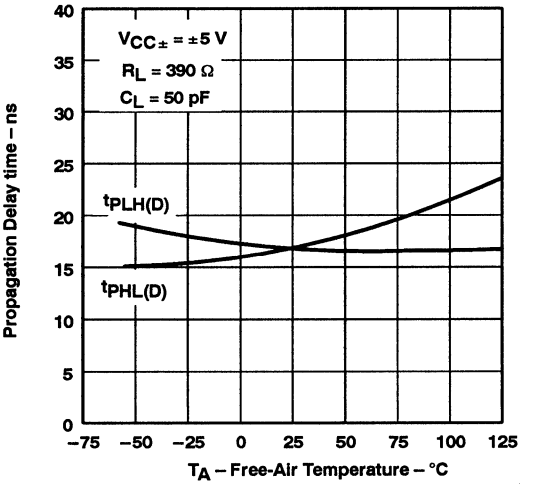


Figure 5

† Values below 0°C and above 70°C apply to SN55' only.

TYPICAL CHARACTERISTICS†

PROPAGATION TIME, LOW-TO-HIGH LEVEL (DIFFERENTIAL INPUTS) vs FREE-AIR TEMPERATURE

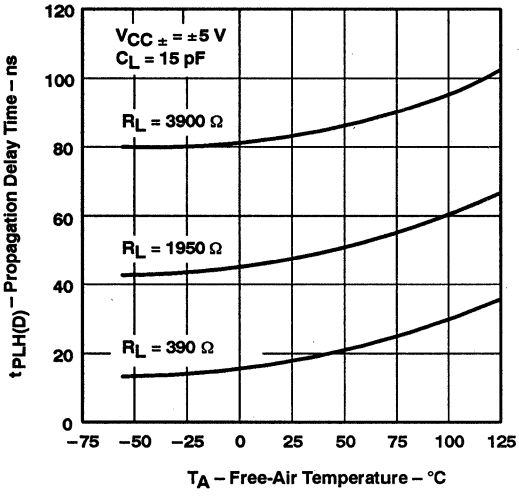


Figure 6

PROPAGATION TIME, LOW-TO-HIGH LEVEL (DIFFERENTIAL INPUTS) vs FREE-AIR TEMPERATURE

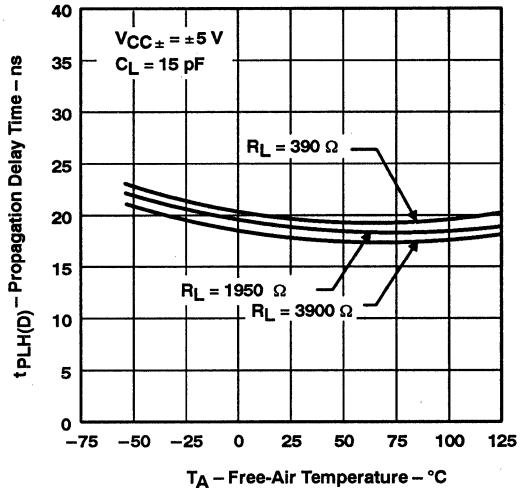


Figure 7

'108A, '108B PROPAGATION DELAY TIME (STROBE INPUTS) vs FREE-AIR TEMPERATURE

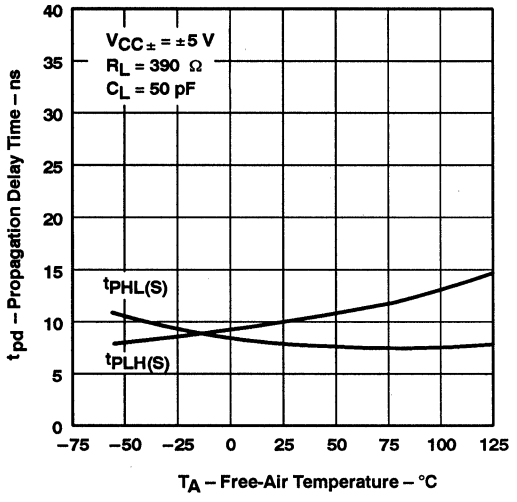


Figure 8

'108A, '108B PROPAGATION DELAY TIME (STROBE INPUTS) vs FREE-AIR TEMPERATURE

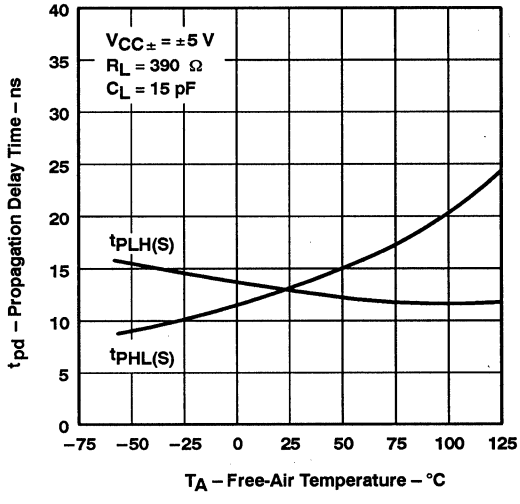


Figure 9

† Values below 0°C and above 70°C apply to SN55' only.

APPLICATION INFORMATION

basic balanced-line transmission system

The '107A, '107B, '108A, and '108B dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately 30 + 1.3 L ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \sim 1/2 I_{O(on)} \cdot R_T$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \sim I_{O(on)} \cdot R_T$$

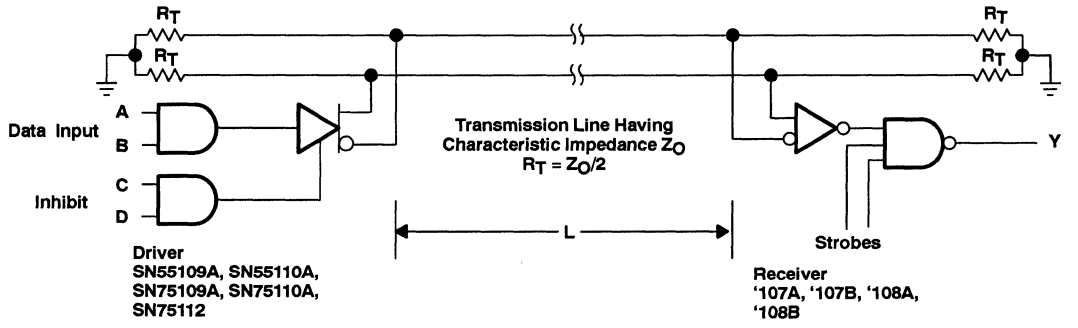


Figure 10. Typical Differential Data Line

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION INFORMATION

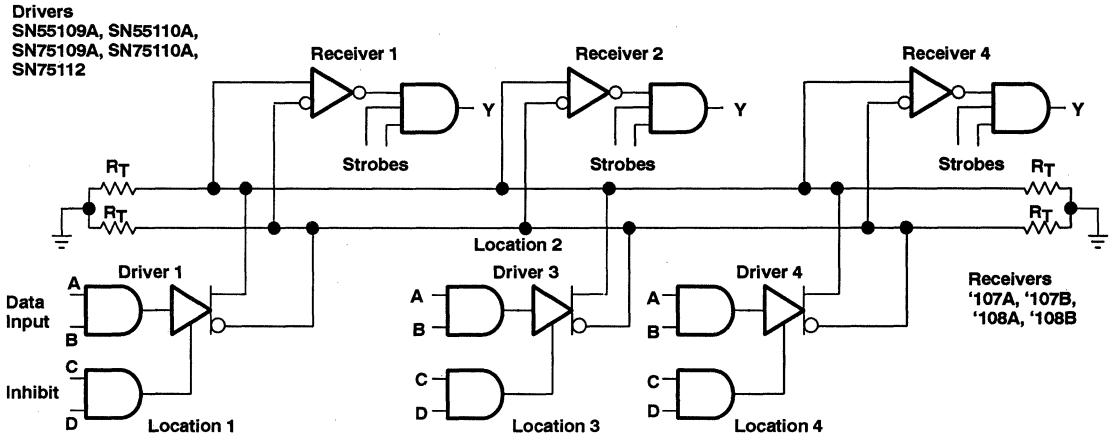


Figure 11. Typical Differential Party Line

unbalanced or single-line systems

These dual-line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 V to 3 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers may be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

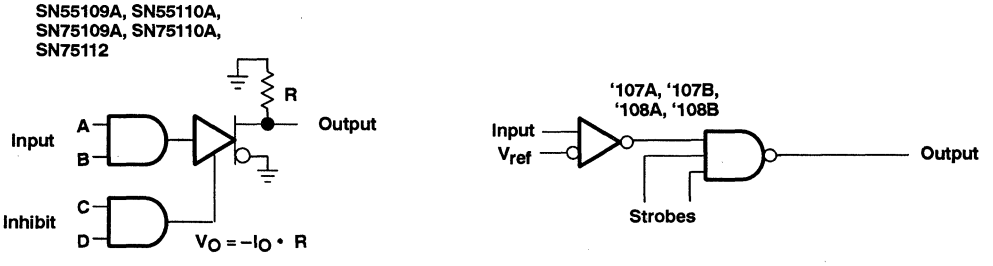


Figure 12. Single-Ended Operation

APPLICATION INFORMATION

'108A, '108B dot-AND output connections

The '108A, '108B line receivers feature an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

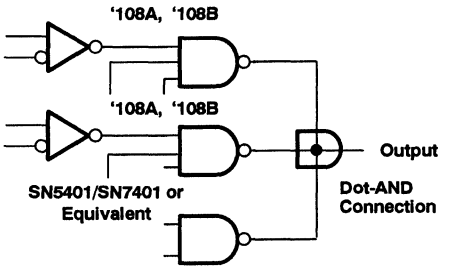


Figure 13. Dot-AND Connection

increasing common-mode input voltage range of receiver

The common-mode voltage range or CMVR is defined as the range of voltage applied simultaneously to both input terminals that if exceeded does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 V, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio. These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors that will be compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance, therefore reducing the versatility of the receiver.

The ability of the receiver to operate with approximately ±15 V common-mode voltage at the inputs has been checked using the circuit shown in Figure 14. The resistors R1 and R2 provide a voltage divider network. Dividers with three different values presenting a 5-to-1 attenuation were used so as to operate the differential inputs at approximately ±3 V common-mode voltage. Careful matching of the two attenuators is needed so as to balance the overdrive at the input stage. The resistors used are shown in Table 1.

Table 1

Attenuator 1:	R1 = 2 kΩ,	R2 = 0.5 kΩ
Attenuator 2:	R1 = 6 kΩ,	R2 = 1.5 kΩ
Attenuator 3:	R1 = 12 kΩ,	R2 = 3 kΩ

Table 2. Typical Propagation Delays for Receiver With Attenuator Test Circuit Shown in Figure 14

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (ns)
'107A,'107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
'108A,'108B	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

Table 2 shows some of the typical switching results obtained under such conditions.

APPLICATION INFORMATION

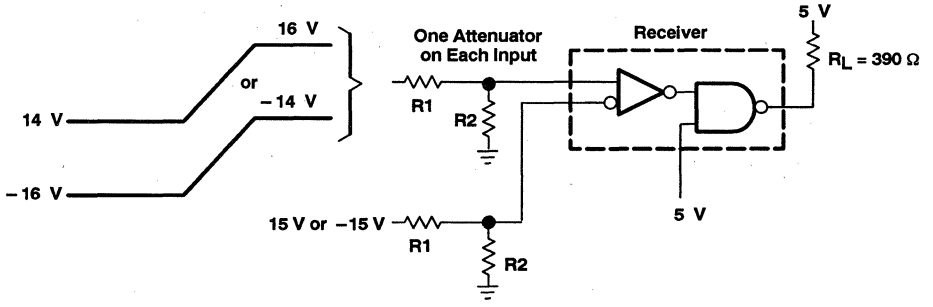


Figure 14. Common-Mode Circuit for Testing Input Attenuators With Results Shown In Table 2

Two methods of terminating a transmission line to reduce reflections are:

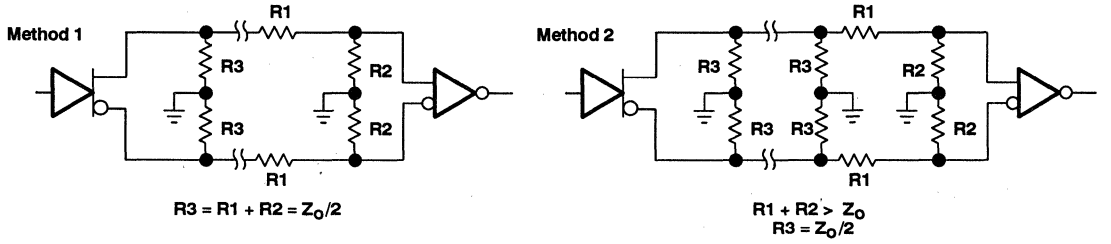


Figure 15. Termination Techniques

The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

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APPLICATION INFORMATION

For party-line operation, method 2 should be used as follows:

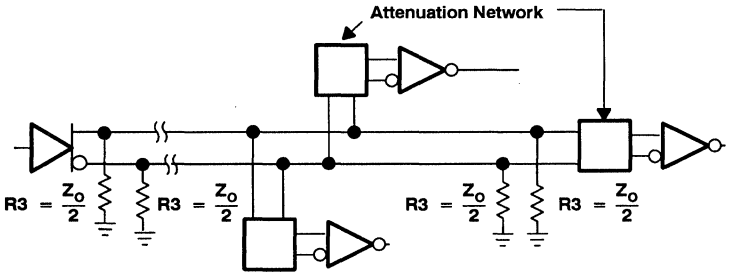


Figure 16. Party-Line Termination Technique

To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table 1.

furnace control using the SN75108A

The furnace control circuit in Figure 17 is an example of the possible use of the SN55107A Series in areas other than what would normally be considered electronic systems. Basically, the operation of this control is as follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the heat on relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the heat on relay is off. There is also a safety switch in the bonnet that shuts the furnace down if the temperature there exceeds desired limitations. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

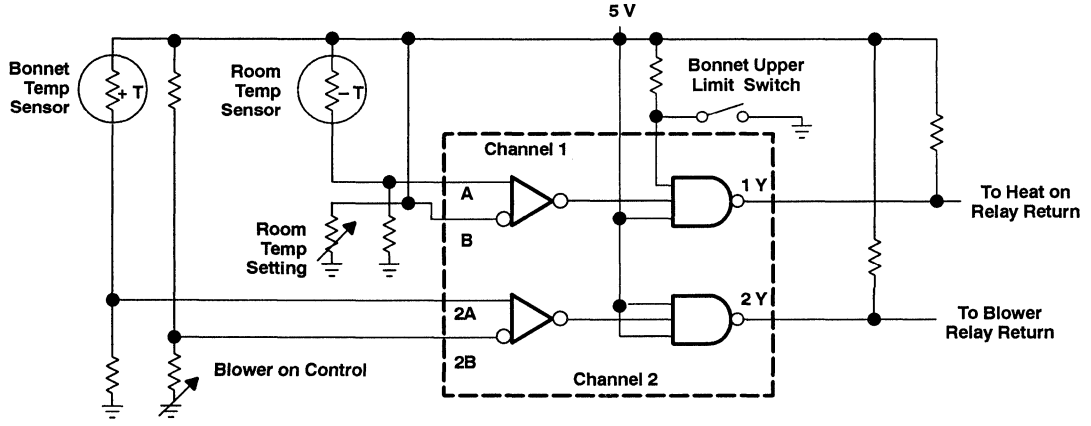


Figure 17. Furnace Control Using SN75108A

APPLICATION INFORMATION

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters [shown in Figure 18(a)] restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 18(b).

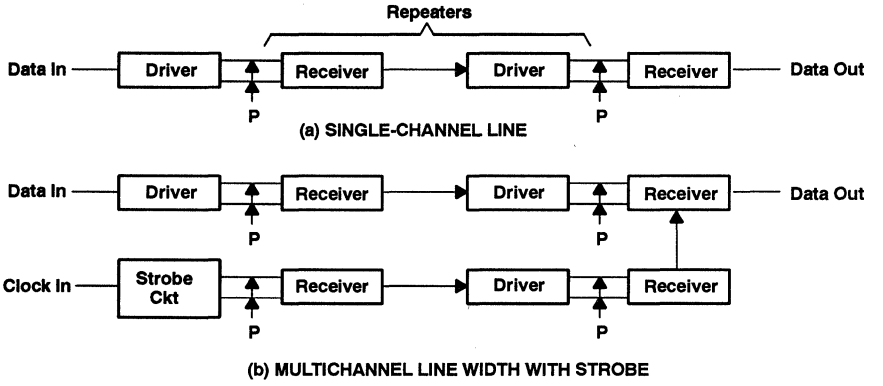


Figure 18. Receiver-Driver Repeaters

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse-width control.

As a differential comparator, a '107A or '108A may be connected so as to compare the noninverting input terminal with the inverting input as shown in Figure 19. Thus the output will be high or low resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

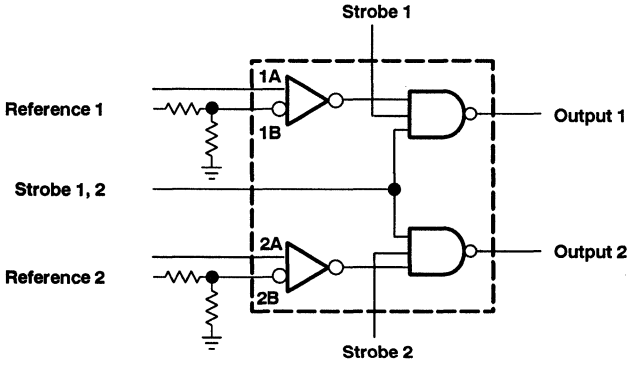
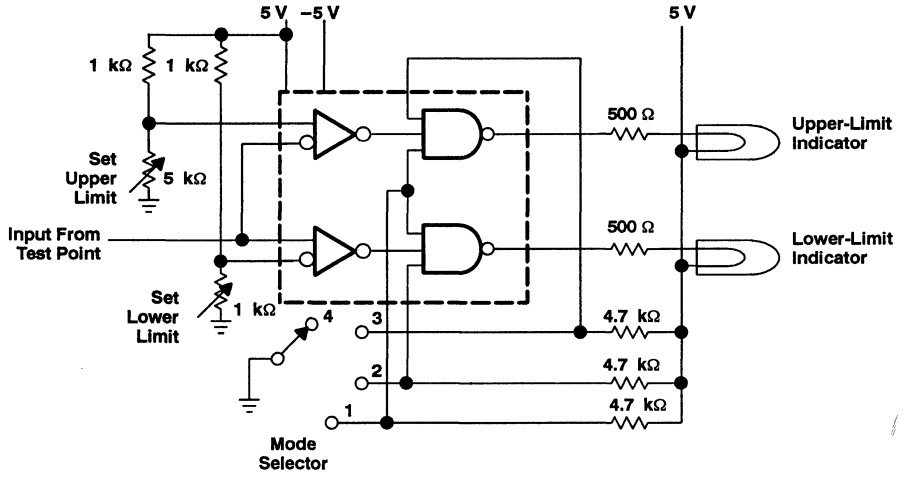


Figure 19. SN55107A Series Receiver as a Dual Differential Comparator

APPLICATION INFORMATION

window detector

The window detector circuit in Figure 20 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time – such as detecting whether a voltage or signal has exceeded its limits or window. Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the upper and lower limits test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	Off
2	Test for Upper Limit
3	Test for Lower Limit
4	Test for Upper and Lower Limits

Figure 20. Window Detector Using SN75108A

APPLICATION INFORMATION

temperature controller with zero-voltage switching

The circuit in Figure 21 switches an electric-resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the '108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is ANDed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

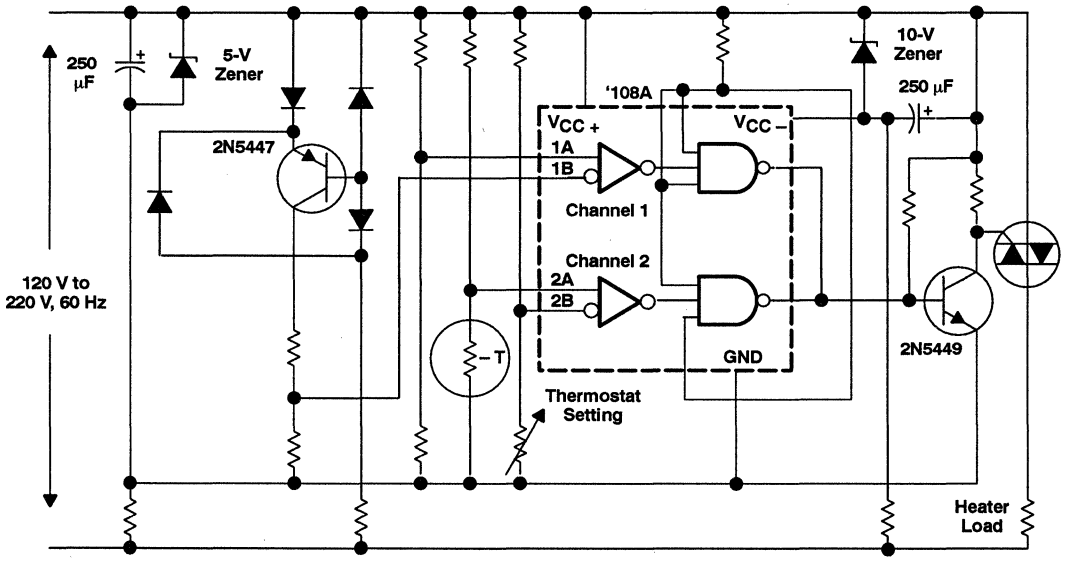
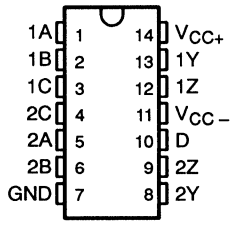


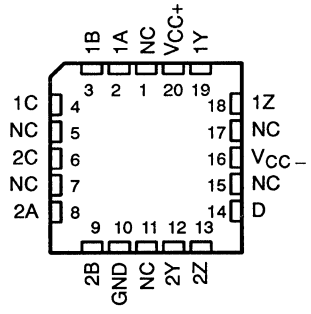
Figure 21. Zero-Voltage Switching Temperature Controller

- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Speed**
- **Standard Supply Voltages**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range −3 V to 10 V**
- **TTL-Input Compatibility**
- **Inhibitor Available for Driver Selection**
- **Glitch-Free During Power Up/Power Down**
- **SN75112 Complies With Requirements of CCITT Recommendation V.35**

SN55109A, SN55110A . . . J OR W PACKAGE
SN75109A, SN75110A, SN75112 . . . D OR N PACKAGE
(TOP VIEW)



SN55109A, SN55110A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE SN75109A IS NOT RECOMMENDED FOR NEW DESIGN

description

The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current is nominally 6 mA for the '109A, 12 mA for the '110A, and 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

AVAILABLE OPTIONS

T_A	PACKAGE				CERAMIC FLATPACK (W)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	SN75109AD SN75110AD SN75112D		SN75109AJ SN75110AJ SN75112J	SN75109AN SN75110AN SN75112N	
−55°C to 125°C		SN55109AFK SN55110AFK	SN55109AJ SN55110AJ	SN55109AJ SN55110AJ	SN55109AW SN55110AW

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75109ADR).

description (continued)

The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400-mV noise margin when interfaced with TTL Series 54/74.

The SN55109A and SN55110A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75109A, SN75110A, and SN75112 are characterized for operation from 0°C to 70°C.

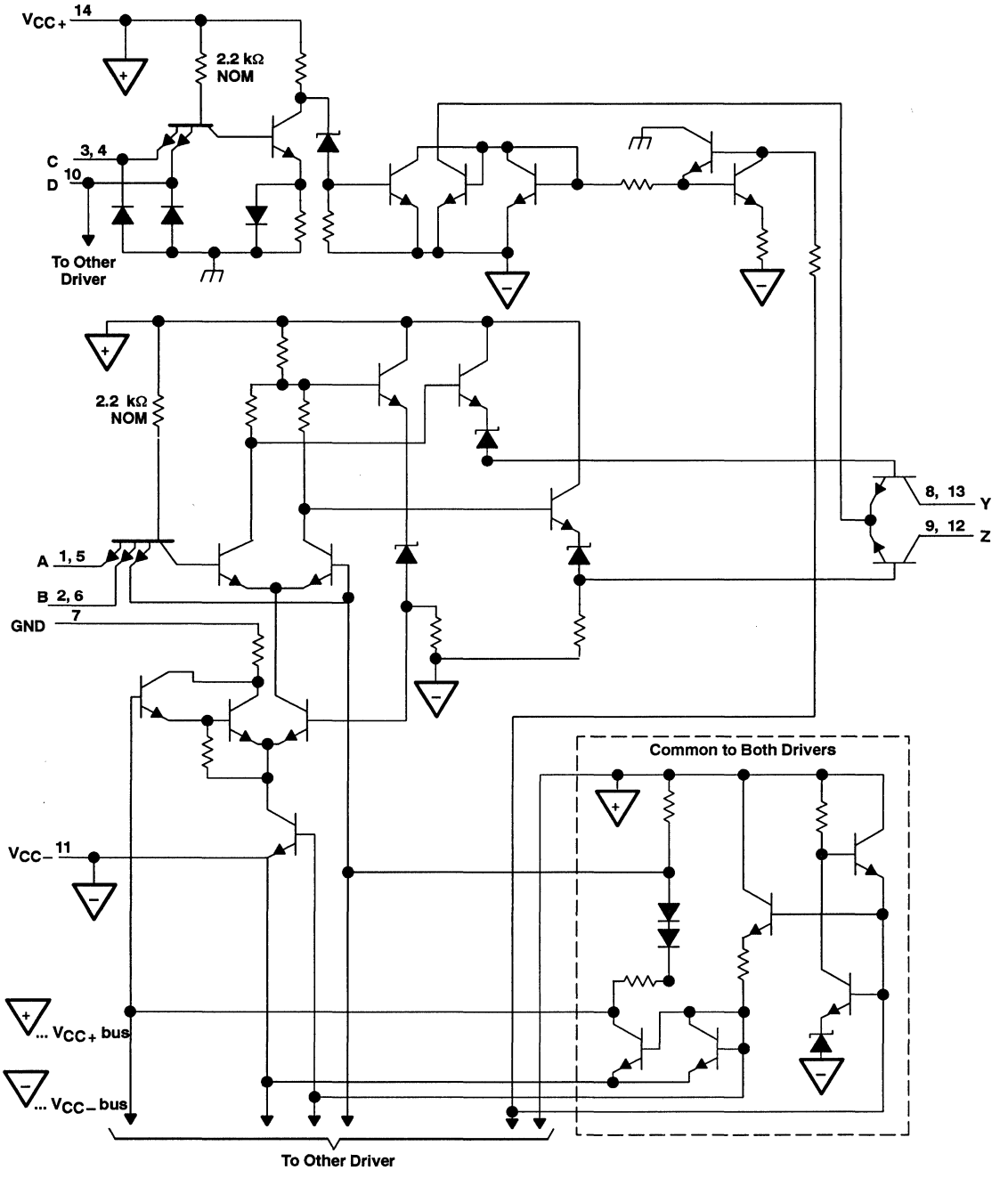
FUNCTION TABLE
(each driver)

LOGIC INPUTS		ENABLE INPUTS		OUTPUTS†	
A	B	C	D	Y	Z
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	On	Off
X	L	H	H	On	Off
H	H	H	H	Off	On

H = high level, L = low level, X = irrelevant

† When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)



Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55109A SN55110A	SN75109A SN75110A	SN75112	UNIT
Supply voltage, V_{CC+} (see Note 1)		7	7	7	V
Supply voltage, V_{CC-}		−7	−7	−7	V
Input voltage, V_I		5.5	5.5	5.5	V
Output voltage range		−5 to 12	−5 to 12	−5 to 12	V
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package		260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In the FK, J, or W package, SN55109A and SN55110A chips are either silver glass or alloy mounted, and SN75109A, SN75110A, and SN75112 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions (see Note 3)

	SN55109A, SN55110A			SN75109A, SN75110A, SN75112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive common-mode output voltage	0		10	0		10	V
Negative common-mode output voltage	0		−3	0		−3	V
High-level input voltage, V_{IH}	2			2			V
Low-level output current, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55109A, SN75109A			SN55110A, SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_L = −12 mA		−0.9	−1.5		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		6	7		12	15		27	36	mA
			V_{CC} = MIN to MAX, V_O = −1 V to 1 V							24	28	32	
			$V_{CC\pm}$ = MIN, V_O = −3 V	3.5	6		6.5	12		18	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100			100	μA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1			1	mA
		D input				2			2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40			40	μA
		D input				80			80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3			−3	mA
		D input				−6			−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		18	30		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−18	−30		−34	−50		−65	−100	
$I_{CC+(off)}$	Supply current from V_{CC-} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		18			21			30		mA
$I_{CC-(off)}$	Supply current from $V_{CC\pm}$ with driver inhibited				−10			−17			−32		

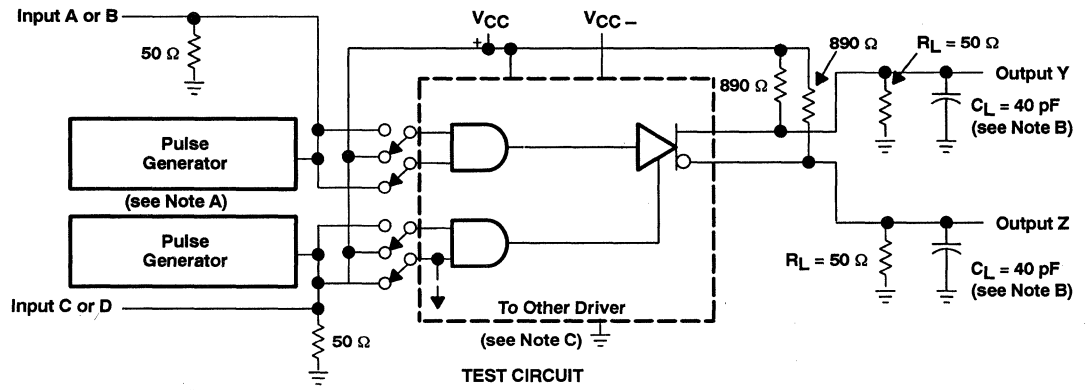
† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

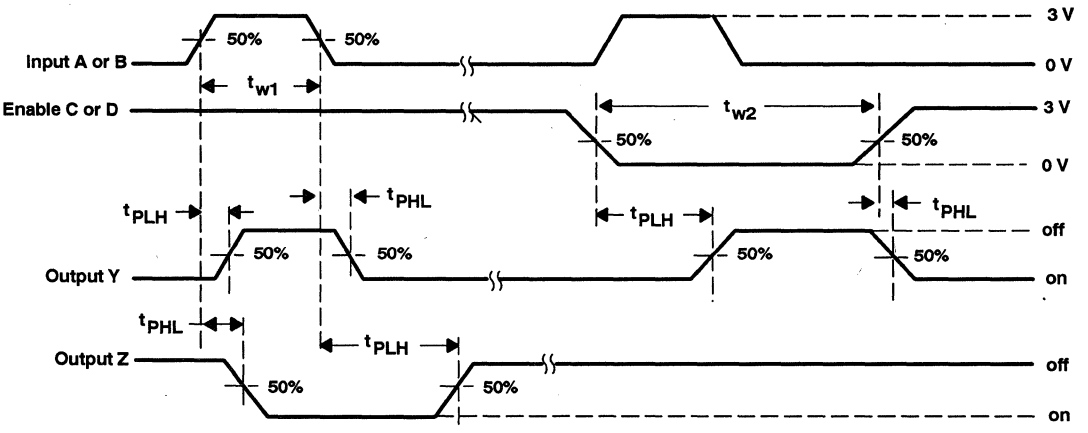
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}					9	15	ns
t_{PLH}	C or D	Y or Z			16	25	ns
t_{PHL}					13	25	ns

† t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{w1} = 500 ns, PRR ≤ 1 MHz, t_{w2} = 1 µs, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.
C. For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

**ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE**

SN55109A, SN75109A

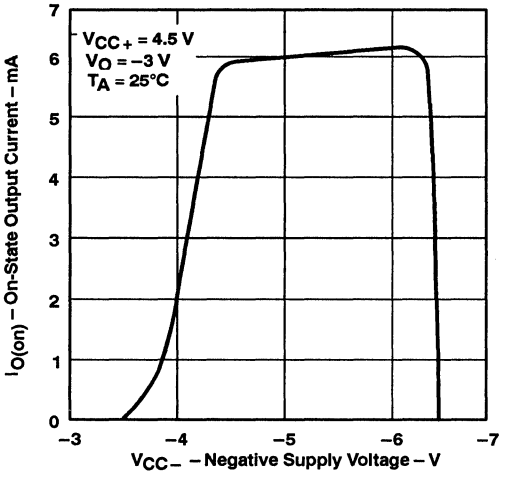


Figure 2

SN55110A, SN75110A

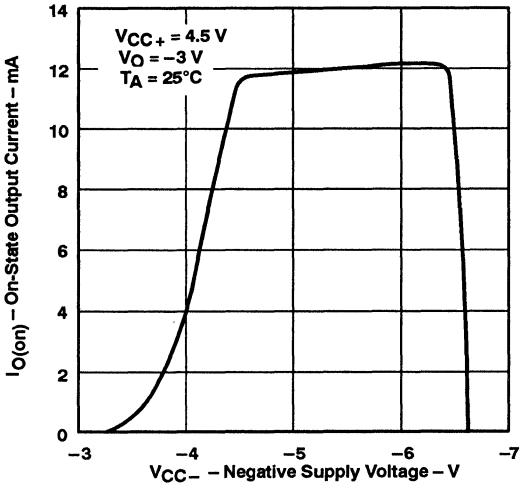


Figure 3

SN75112

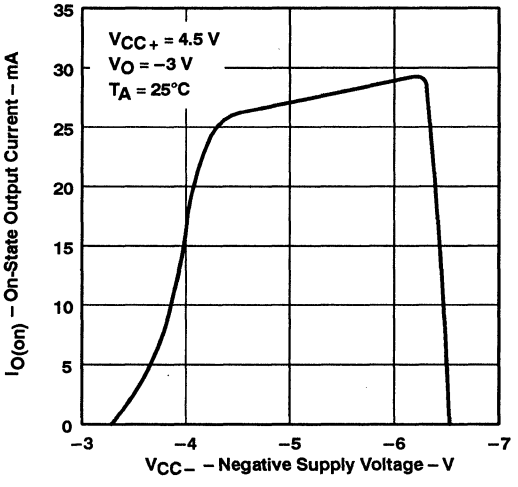


Figure 4

APPLICATION INFORMATION

special pulse-control circuit

Figure 5 shows a circuit that may be used as a pulse generator output or in many other testing applications.

INPUT	OUTPUTS	
A	Y	Z
High	Off	On
Low	On	Off

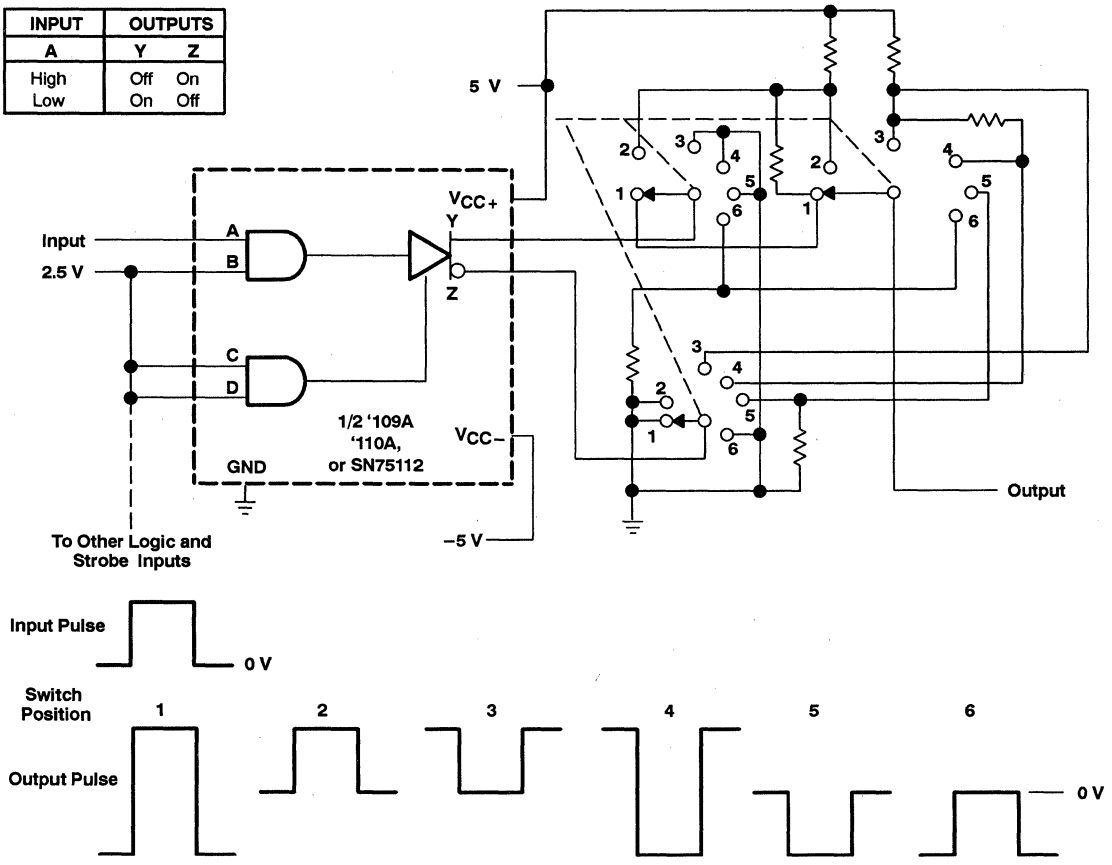


Figure 5. Pulse-Control Circuit

APPLICATION INFORMATION

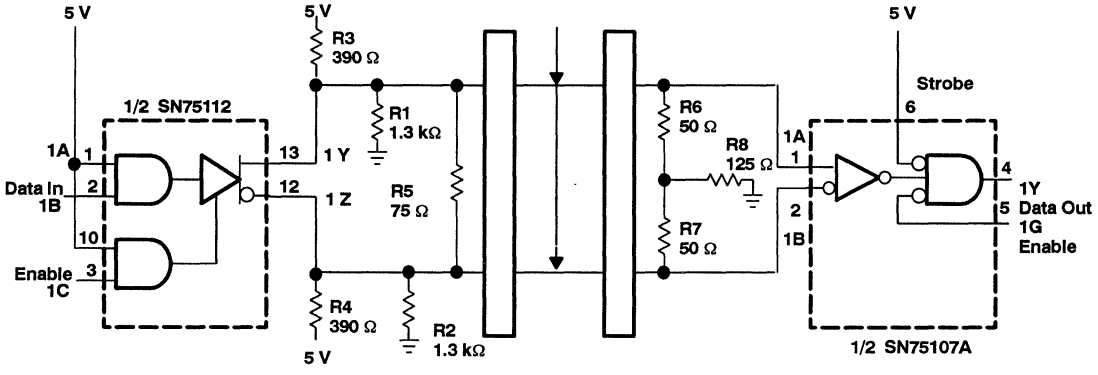
using the SN75112 as a CCITT recommendation V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 1 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and summarized in Table 1.

Table 1. CCITT V.35 Electrical Requirements

	MIN	MAX	UNIT
GENERATOR			
Source impedance, Z_{source}	50	150	Ω
Resistance to ground, R	135	165	Ω
Differential output voltage, V_{OD}	440	660	MV
10% to 90% rise time, t_r		40	ns
or		0.01 × ui †	
Common-mode output voltage, V_{CC}	– 0.6	0.6	V
LOAD (RECEIVER)			
Input impedance, Z_I	90	110	Ω
Resistance to ground, R	135	165	Ω

† ui = unit interval or minimum signal element pulse width

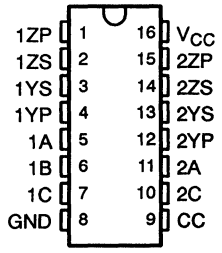


All resistors are 5%, 1/4 W.

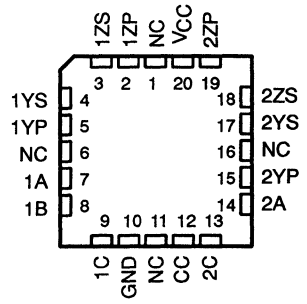
Figure 6. CCITT Recommendation V.35 Interface Using the SN75112 and SN75107A

- **Choice of Open-Collector, Open-Emitter, or 3-State Outputs**
- **High-Impedance Output State for Party-Line Applications**
- **Single-Ended or Differential AND/NAND Outputs**
- **Single 5-V Supply**
- **Dual Channel Operation**
- **Compatible With TTL**
- **Short-Circuit Protection**
- **High-Current Outputs**
- **Common and Individual Output Controls**
- **Clamp Diodes at Inputs and Outputs**
- **Easily Adaptable to SN55114 and SN75114 Applications**
- **Designed for Use With SN55115 and SN75115**

SN55113 . . . J OR W PACKAGE
SN75113 . . . D OR N PACKAGE
(TOP VIEW)



SN55113 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55113 and SN75113 dual differential line drivers with 3-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. Individual controls are provided for each output pair, as well as a common control for both output pairs. If any output is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins.

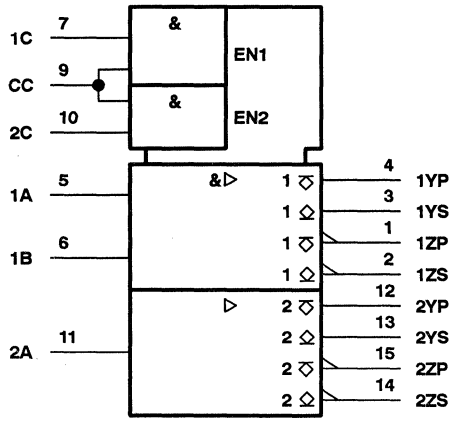
The SN55113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75113 is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B†	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

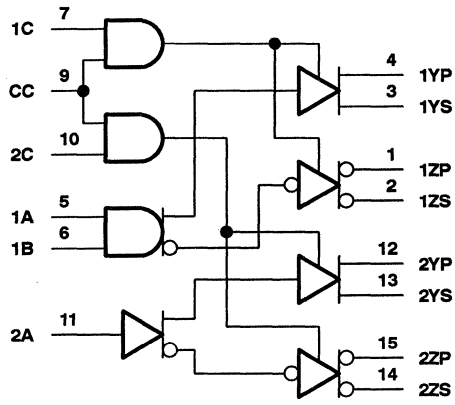
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)
† B input and 4th line of function table are applicable only to driver number 1.

logic symbol†

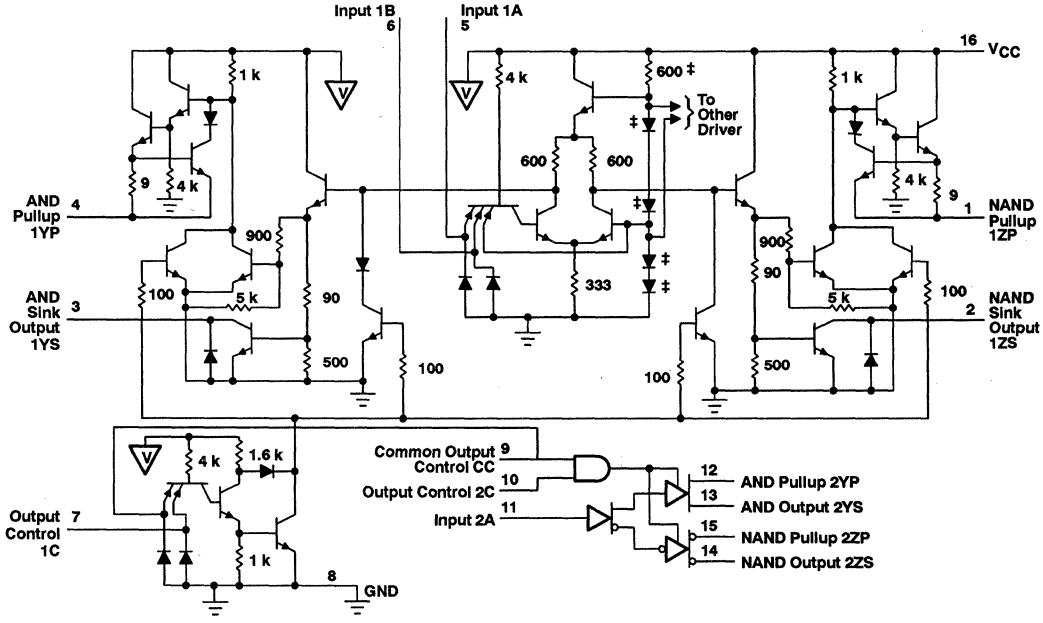


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic



▽ ... V_{CC} bus

‡ These components are common to both drivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Off-state voltage applied to open-collector outputs ..... 12 V
Continuous total power dissipation (see Note 2) ..... See Dissipation Rating Table
Operating free-air temperature range: SN55113 ..... −55°C to 125°C
SN75113 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package ..... 300°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the J, FK, and W packages, SN55113 chips are alloy mounted; SN75113 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

	SN55113			SN75113			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

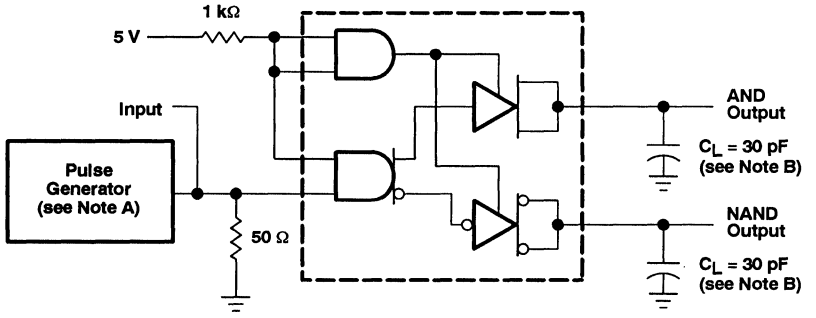
PARAMETER			TEST CONDITIONS†			SN55113			SN75113			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 40 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.23	0.4		0.23	0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX,	I_O = − 40 mA			−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25 V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10			±10	μA
				T_A = MAX	V_O = 0			−150			−20	
					V_O = 0.4 V			±80			±20	
					V_O = 2.4 V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
		CC						2			2	
I_{IH}	High-level input current	A, B, C	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
		CC						80			80	
I_{IL}	Low-level input current	A, B, C	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
		CC						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0	T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)		All inputs at 0 V, T_A = 25°C	No load,	V_{CC} = MAX		47	65		47	65	mA
					V_{CC} = 7 V		65	85		65	85	

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

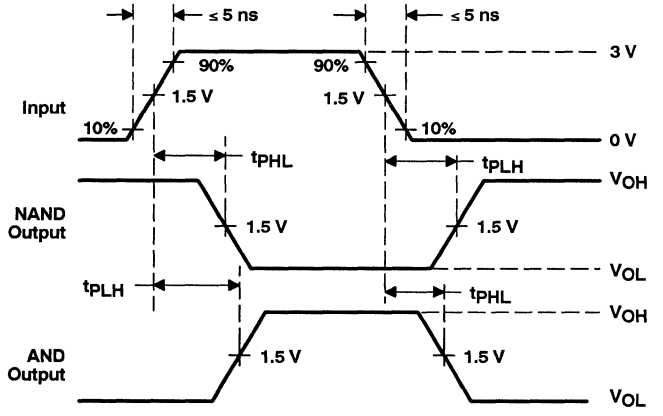
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55113			SN75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 1		13	20		13	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	ns
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 2		7	15		7	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 3		14	30		14	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 2		10	20		10	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 3		17	35		17	35	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

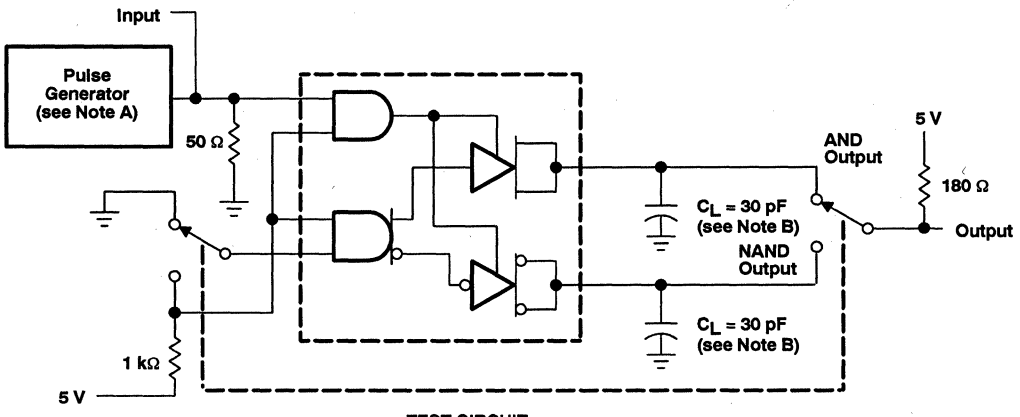


VOLTAGE WAVEFORMS

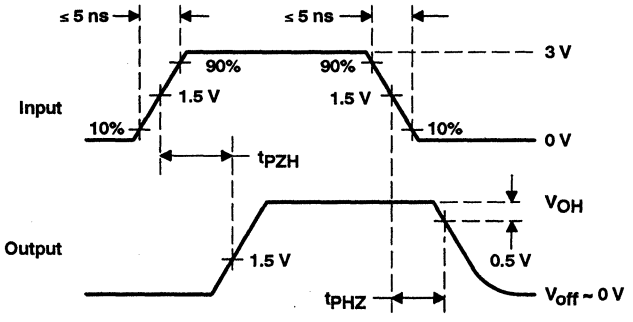
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms t_{PLH} and t_{PHL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

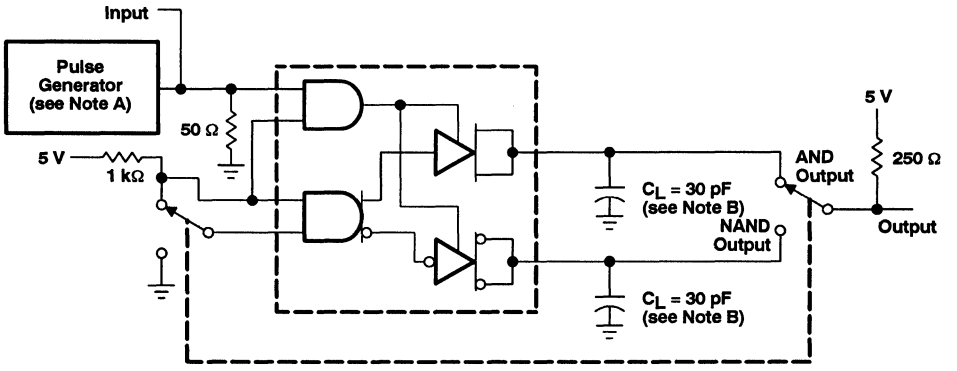


VOLTAGE WAVEFORMS

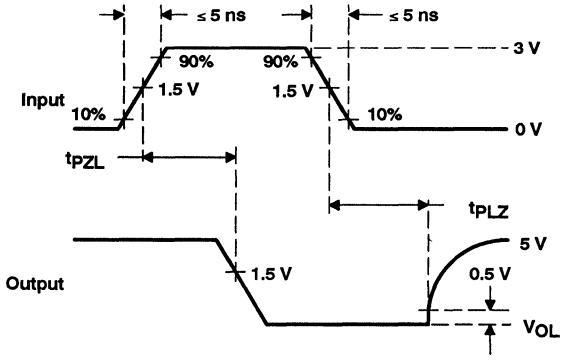
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: C. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns.
D. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

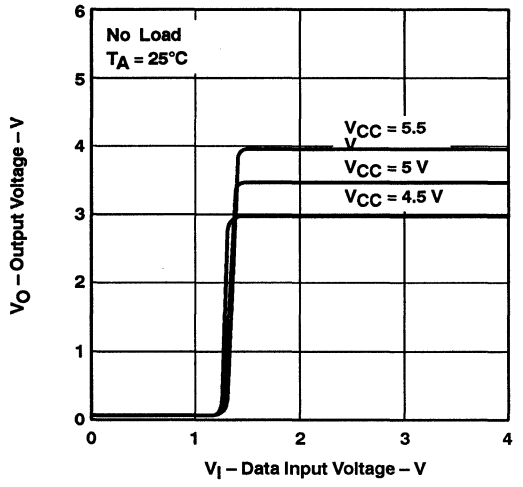


Figure 4

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

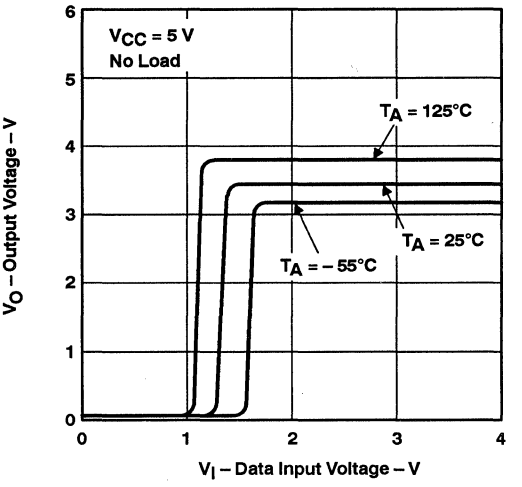


Figure 5

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

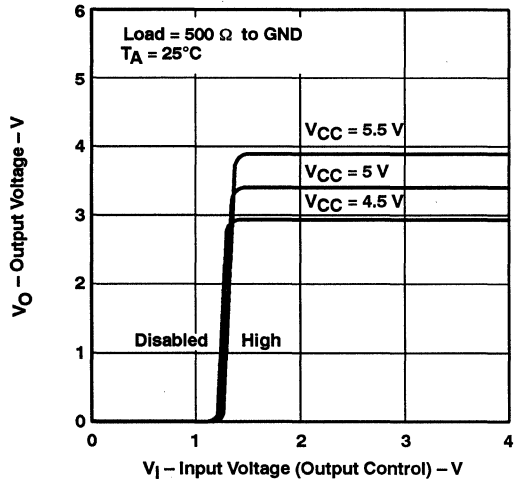


Figure 6

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

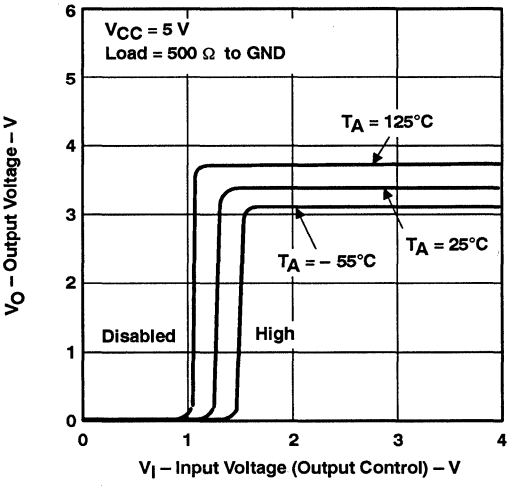


Figure 7

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

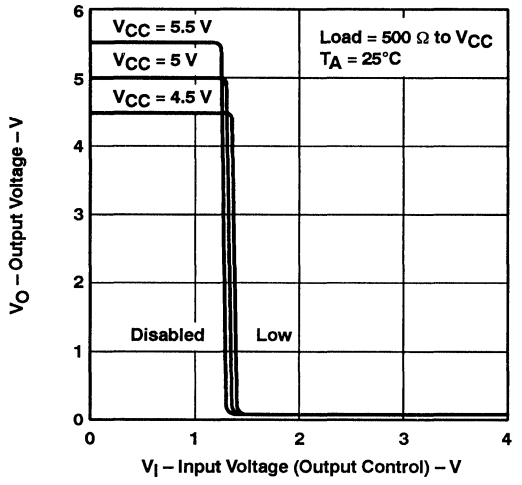


Figure 8

OUTPUT VOLTAGE
vs
OUTPUT CONTROL VOLTAGE

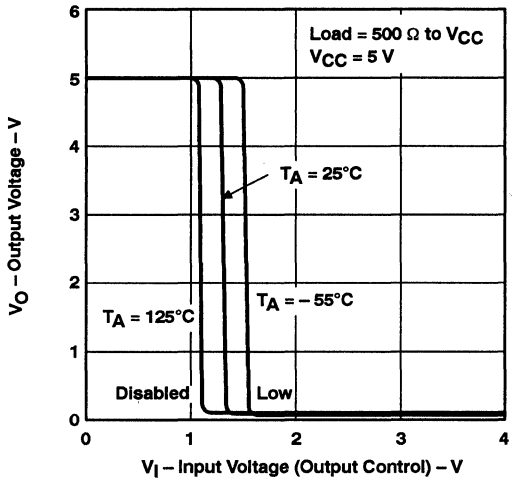


Figure 9

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

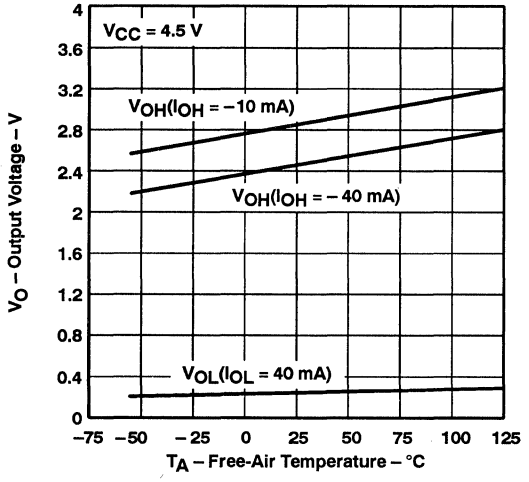


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

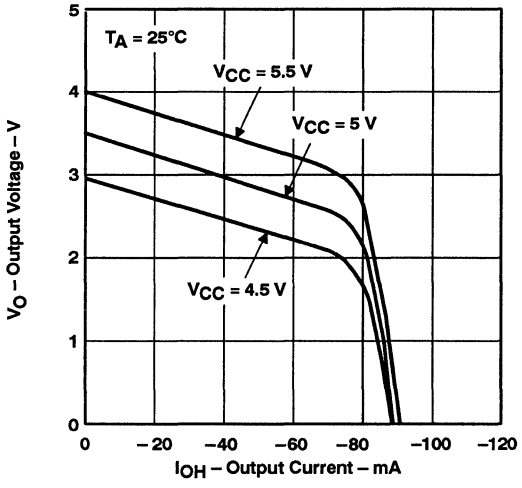


Figure 11

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

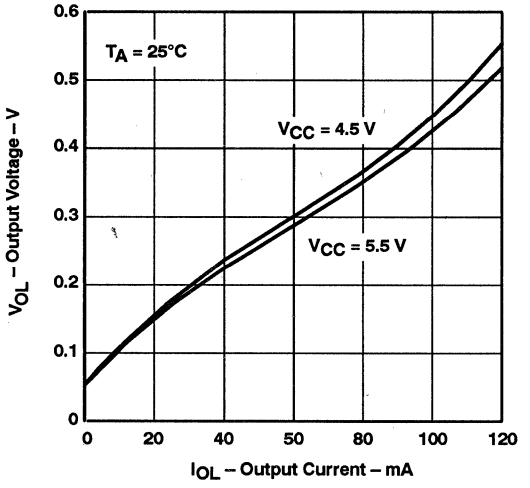


Figure 12

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

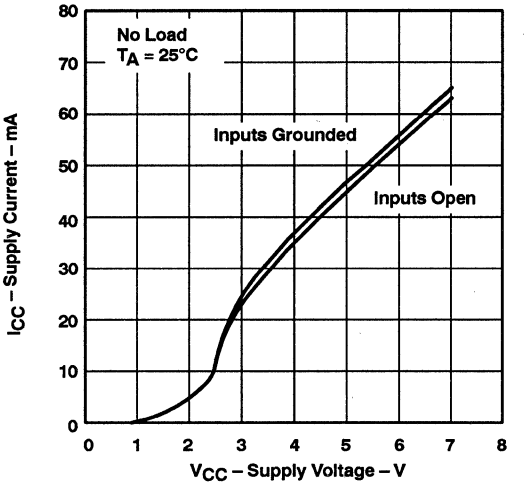


Figure 13

SUPPLY CURRENT
(BOTH DRIVERS)
vs
OUTPUT CURRENT

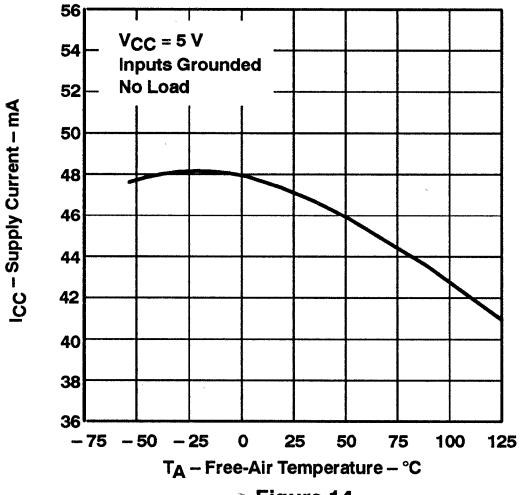


Figure 14

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

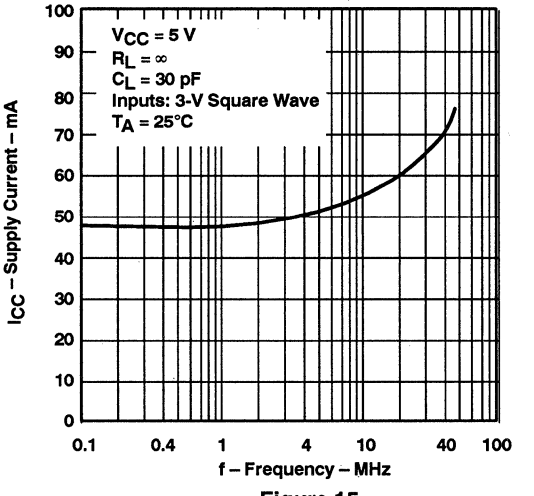


Figure 15

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

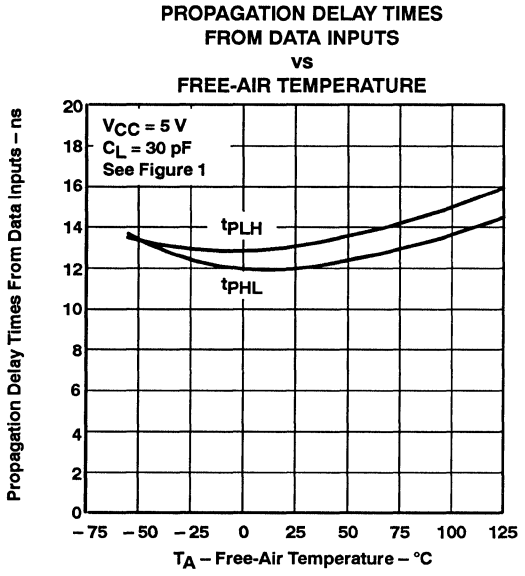


Figure 16

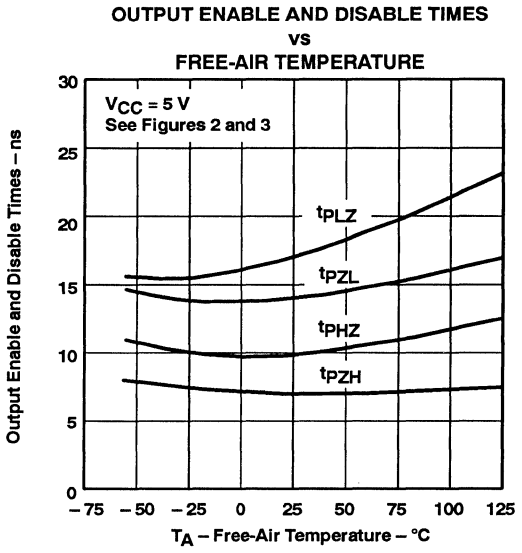
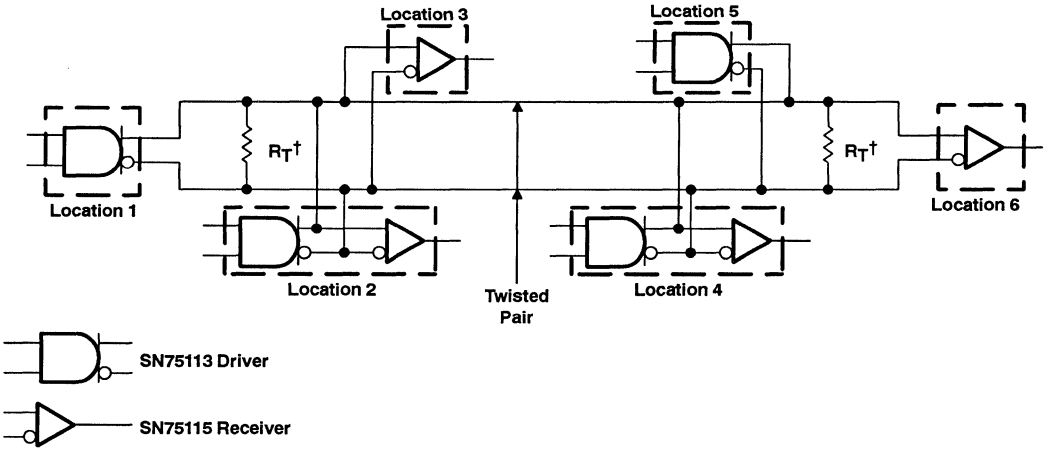


Figure 17

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



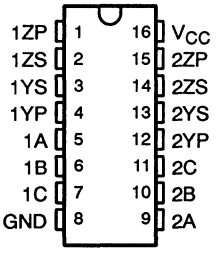
† $R_T = Z_O$. A capacitor may be connected in series with R_T to reduce power dissipation.

Figure 18. Basic Party-Line or Data-Bus Differential Data Transmission

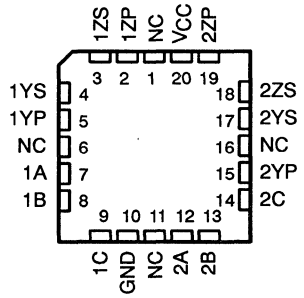
SLLS071A – D1315, SEPTEMBER 1973 – REVISED FEBRUARY 1993

- **Choice of Open-Collector, Open-Emitter, or Totem-Pole Outputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Single 5-V Supply**
- **Dual-Channel Operation**
- **TTL Compatible**
- **Short-Circuit Protection**
- **High-Current Outputs**
- **Triple Inputs**
- **Clamp Diodes at Inputs and Outputs**
- **Designed for Use With SN55115 and SN75115 Differential Line Receivers**
- **Designed to Be Interchangeable With Fairchild 9614 Line Driver**

SN55114 . . . J OR W PACKAGE
SN75114 . . . D OR N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y	Z
H	L	H	H	L
All other inputs combinations			L	H

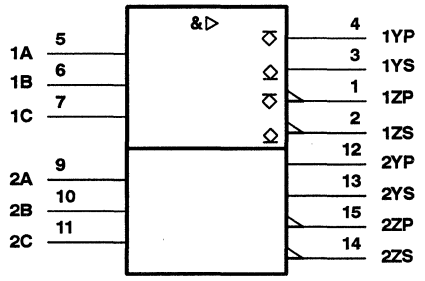
H = high level, L = low level

description

The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with the high-current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL-compatible output levels, these devices may also be used as TTL expanders or phase splitters.

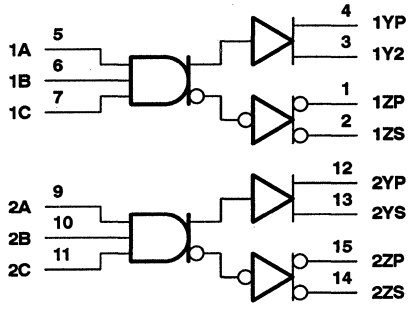
The SN55114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75114 is characterized for operation from 0°C to 70°C.

logic symbol†

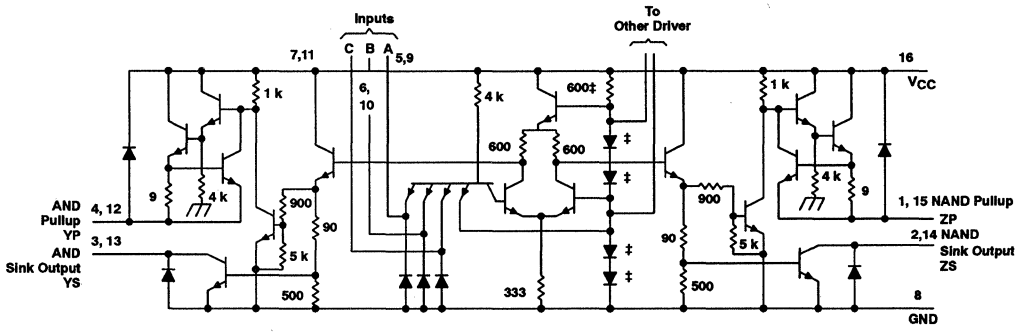


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic (each driver)



‡ These components are common to both drivers. Resistor values shown are nominal and in ohms.
Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55114	SN75114	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Off-state voltage applied to open-collector outputs	12	12	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 MW

† In the FK, J, and W packages, SN55114 chips are either silver glass or alloy mounted.

recommended operating conditions

	SN55114			SN75114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN55114			SN75114			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V,		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA	2	3		2	3		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output clamp voltage	V_{CC} = 5 V, I_O = 40 mA,		T_A = 25°C		6.1	6.5		6.1	6.5	V
		V_{CC} = MAX, I_O = −40 mA,		T_A = 25°C		−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	Off-state open collector output current	V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25 V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX, V_O = 0,		T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)	All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		37	50		37	50	mA
				V_{CC} = 7 V		47	65		47	70	

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

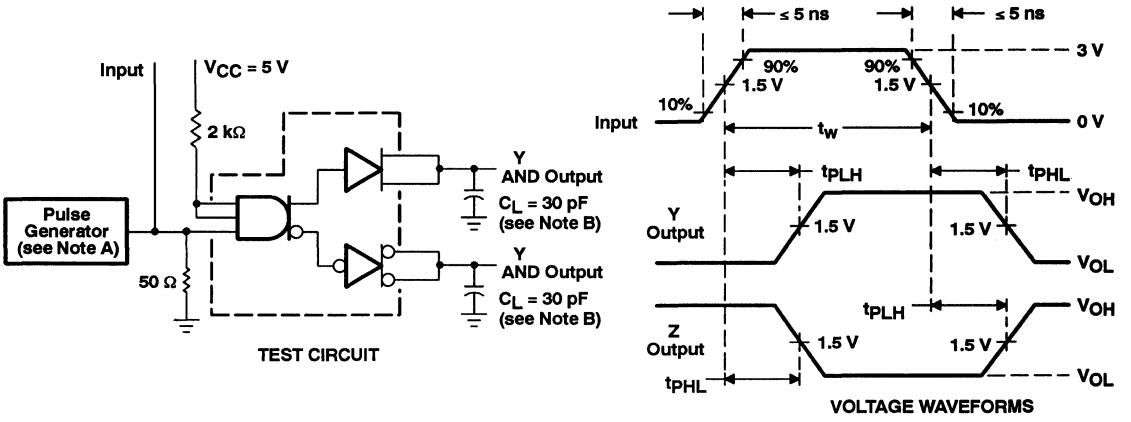
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.

§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55114			SN75114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	20		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20		11	30	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 500 Ω, PRR ≤ 500 kHz, t_w ≤ 100 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

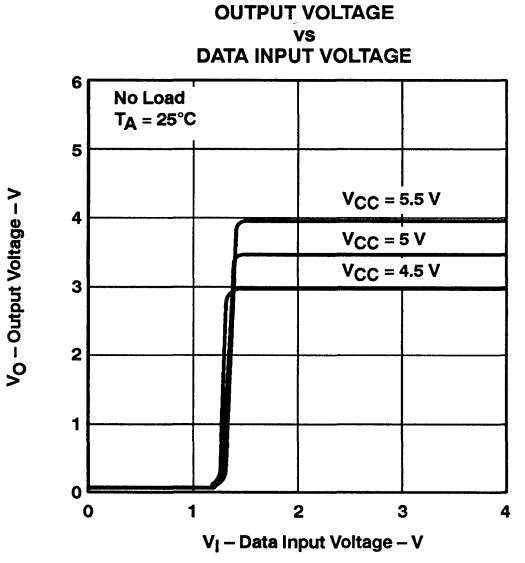


Figure 2

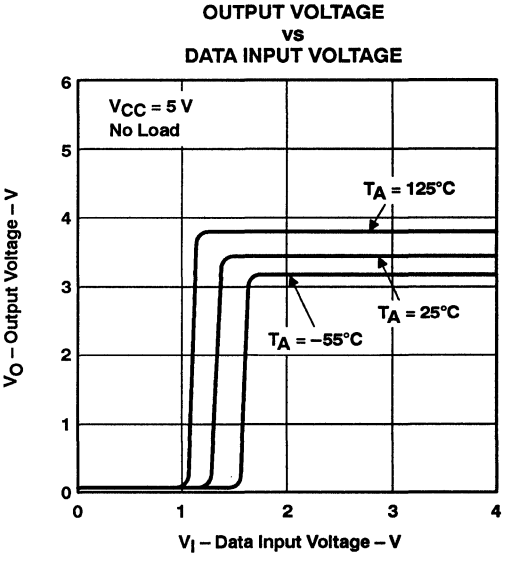


Figure 3

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

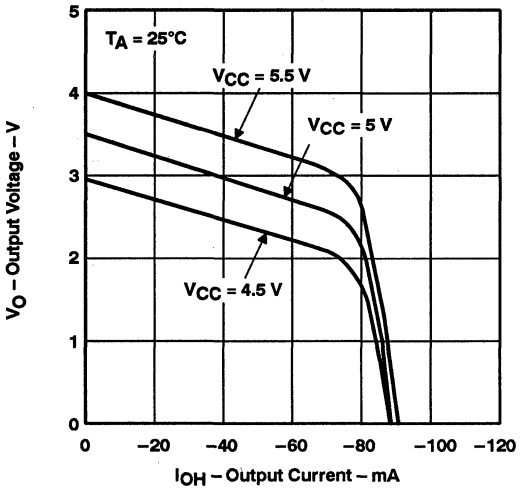


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

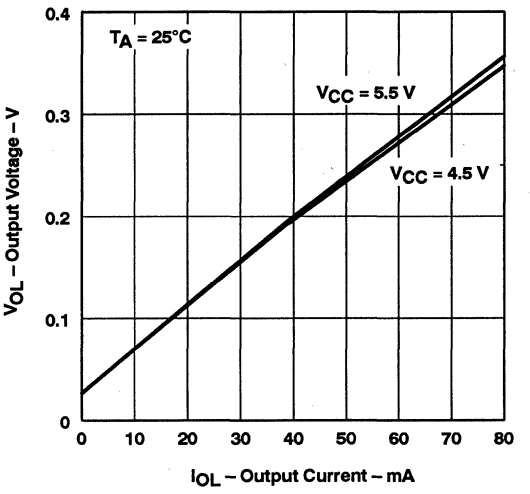


Figure 5

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

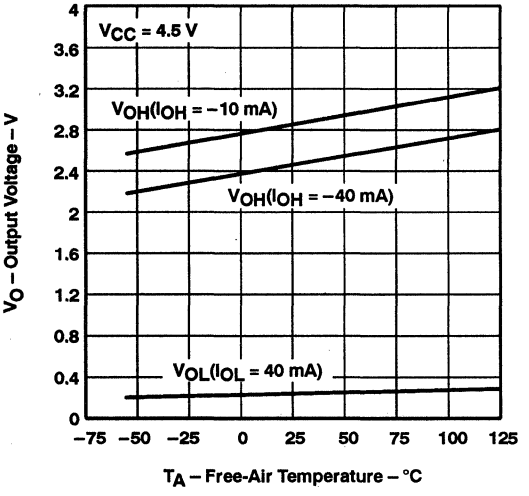


Figure 6

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

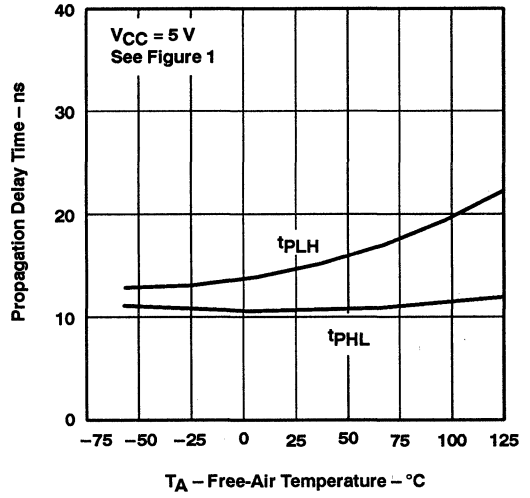


Figure 7

† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

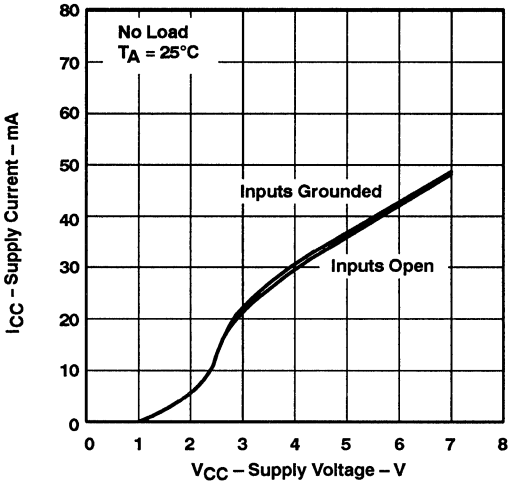


Figure 8

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

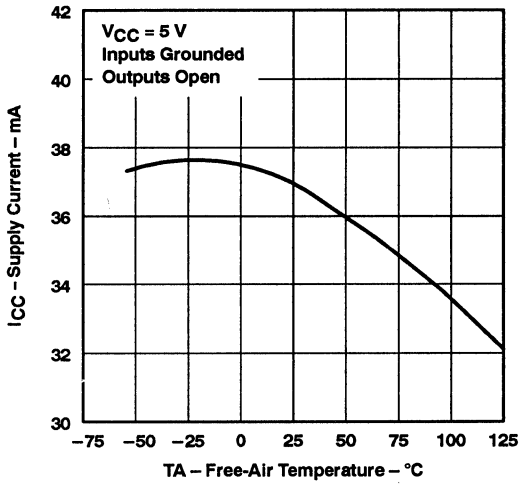


Figure 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

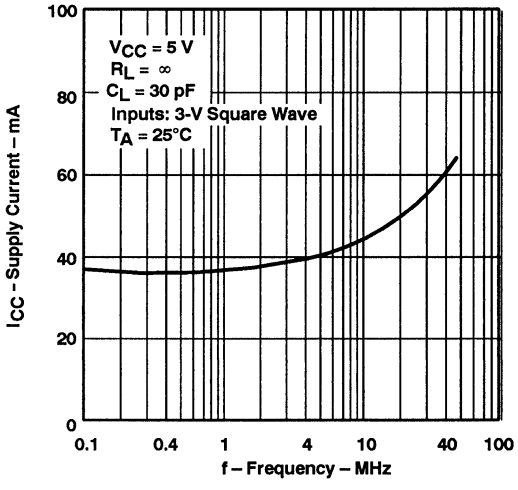
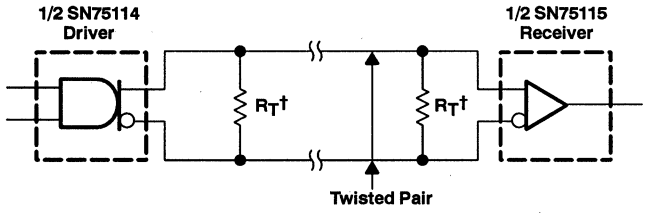


Figure 10

† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION†



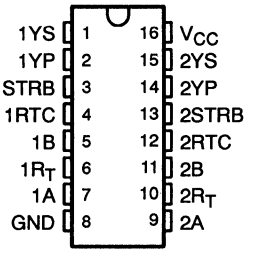
† $R_T = Z_O$. A capacitor may be connected in series with R_T to reduce power dissipation.

Figure 11. Basic Party-Line or Data-Bus Differential Data Transmission

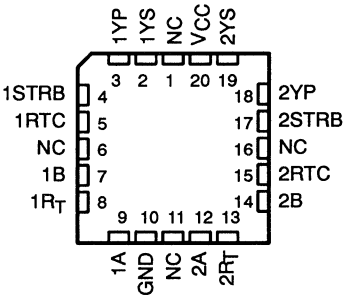
SLLS072A – D1315, SEPTEMBER 1973 – REVISED FEBRUARY 1993

- **Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs**
- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual-Channel Operation**
- **TTL Compatible**
- **±15-V Common-Mode Input Voltage Range**
- **Optional-Use Built-In 130-Ω Line-Terminating Resistor**
- **Individual Frequency Response Controls**
- **Individual Channel Strobes**
- **Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers**
- **Designed to Be Interchangeable With Fairchild 9615 Line Receivers**

SN55115 . . . J OR W PACKAGE
SN75115 . . . D OR N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay. The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

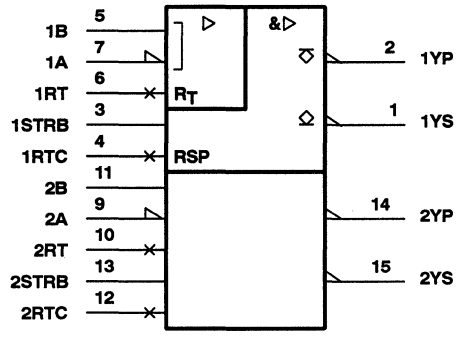
FUNCTION TABLE

STRB	DIFF INPUT (A AND B)	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

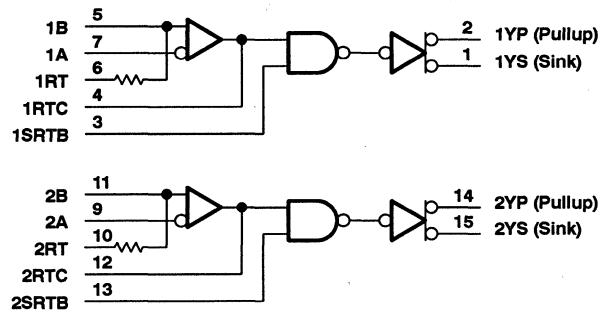
$H = V_I \geq V_{IH}$ min or V_{ID} more positive than V_{T+} max
$L = V_I \leq V_{IL}$ max or V_{ID} more negative than V_{T-} max
X = irrelevant

The SN55115 is characterized for operation over the full military range of −55°C to 125°C. The SN75115 is characterized for operation from 0°C to 70°C.

logic symbol†

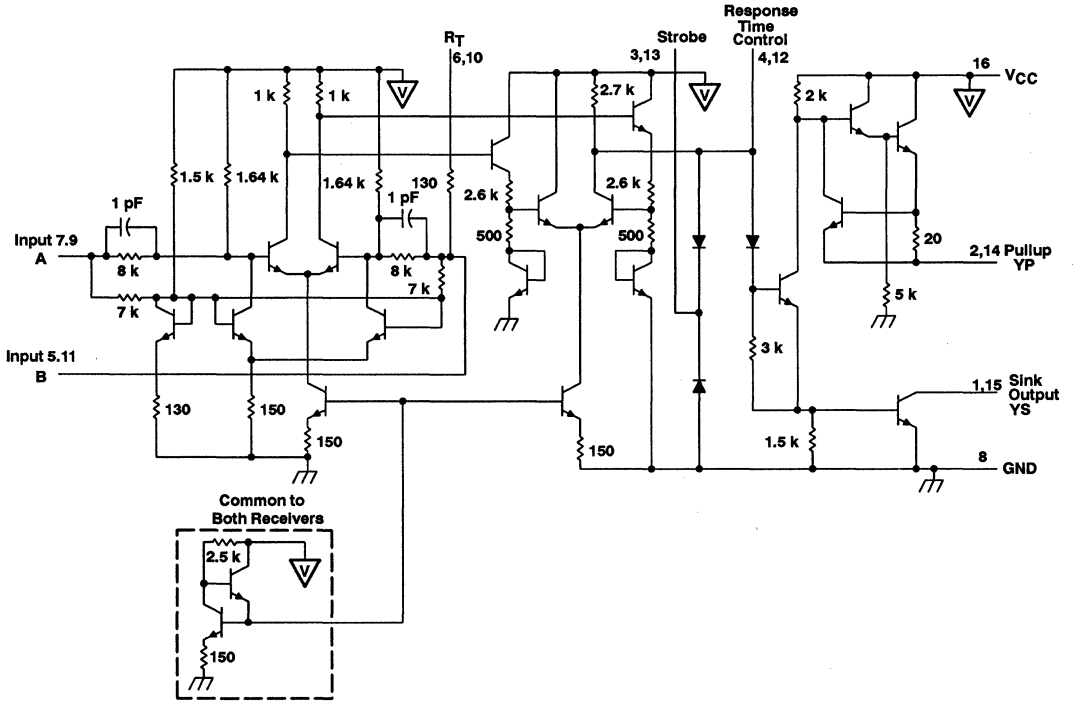


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each receiver)



Resistor values are nominal and in ohms.
Pin numbers shown are for D, J, N, and W packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55115	SN75115	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage at A, B, and R_T	±25	±25	V
Input voltage at STRB	5.5	5.5	V
Off-state voltage applied to open-collector outputs	14	14	V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTE 1: All voltage values, except differential input voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK, J, and W packages, SN55115 chips are either silver glass or alloy mounted. SN75115 chips are glass mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at STRB, V_{IH}	2.4			2.4			V
Low-level input voltage at STRB, V_{IL}			0.4			0.4	V
High-level output current, I_{OH}			−5			−5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55115			SN75115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}§	Positive-going threshold voltage	V_O = 0 .4 V, I_{OL} = 15 mA, V_{IC} = 0				500			500	mV
V_{T-}§	Negative-going threshold voltage	V_O = 2 .4 V, I_{OH} = −5 mA, V_{IC} = 0		−500¶			−500¶			mV
V_{ICR}	Common-mode input voltage range	V_{ID} = ±1 V		+15 to −15	+24 to −19		+15 to −15	+24 to −19		V
V_{OH}	High-level ouput voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OH} = −5 mA	T_A = MIN	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V, Other input at 5.5 V	T_A = MIN			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = MAX			−0.7			−0.7	
I_{SH}	High-level strobe current	V_{CC} = MIN, V_{ID} = −0.5 V, V_{strobe} = 4.5 V	T_A = 25°C			2			5	µA
			T_A = MAX			5			10	
I_{SL}	Low-level strobe current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{strobe} = 0.4 V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
$I_{(RTC)}$	Response-time-control current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MIN, V_{OH} = 12 V, V_{ID} = −4.5 V	T_A = 25°C			100				µA
			T_A = MAX			200				
		V_{CC} = MIN, V_{OH} = 5.25 V, V_{ID} = −4.75 V	T_A = 25°C						100	
			T_A = MAX						200	
R_T	Line-terminating resistance	V_{CC} = 5 V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Supply-circuit output current#	V_{CC} = MAX, V_{ID} = −0.5 V, V_O = 0	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply current (both receivers)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{IC} = 0	T_A = 25°C		32	50		32	50	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Differential voltages are at the B input terminal with respect to the A input terminal.

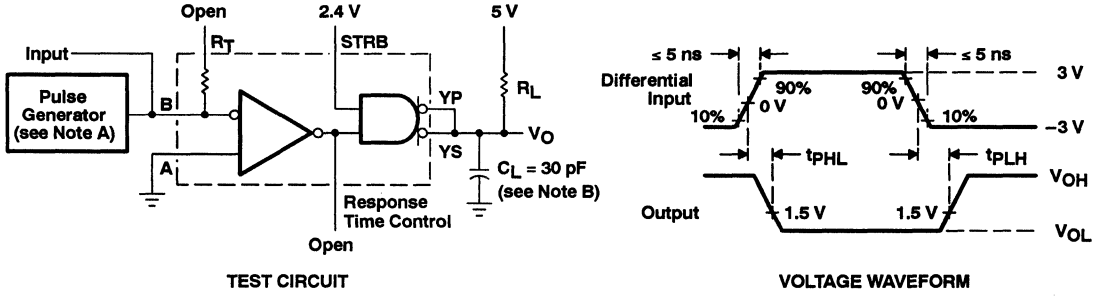
¶ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55115			SN75115			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3.9 kΩ, See Figure 1		18	50		18	75	ns
t_{PHL}	Propagation delay time, high-to-low level output	R_L = 390 Ω, See Figure 1		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORM

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w ≤ 100 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

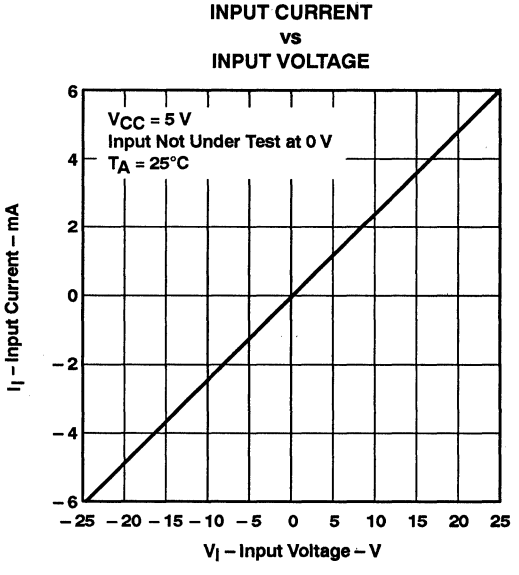


Figure 2

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

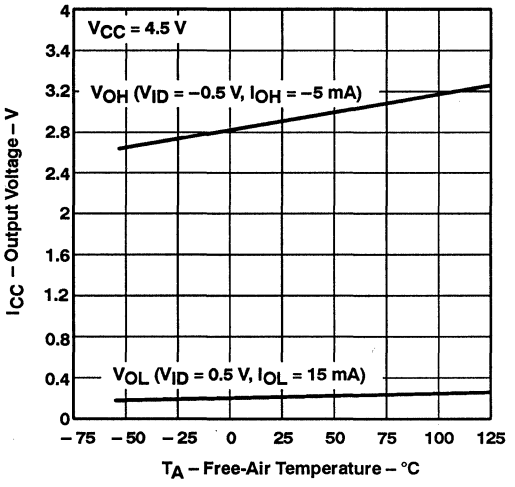


Figure 3

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

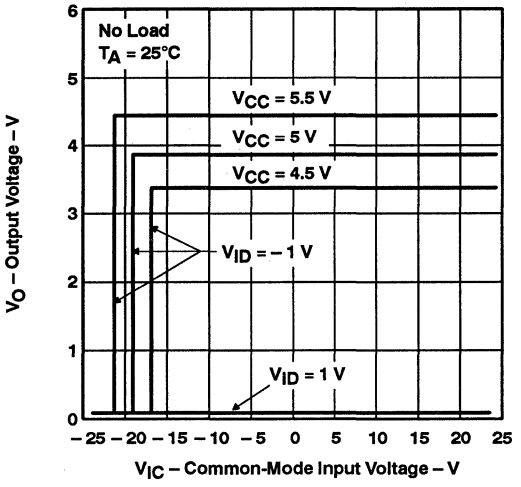


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

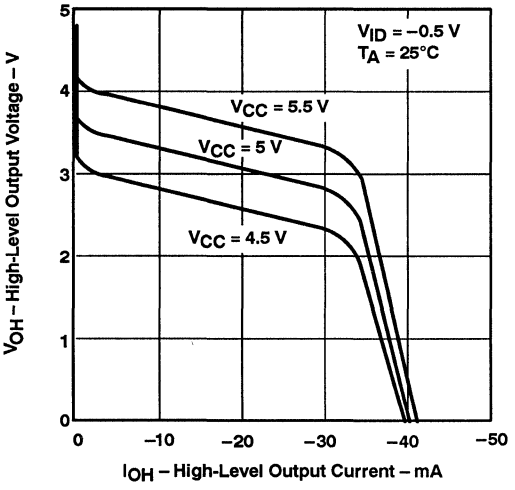


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

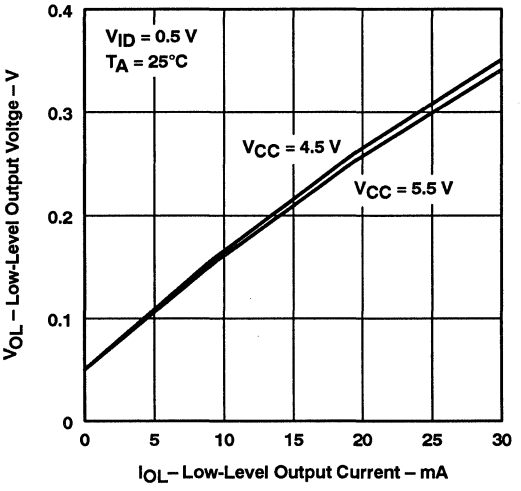


Figure 6

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

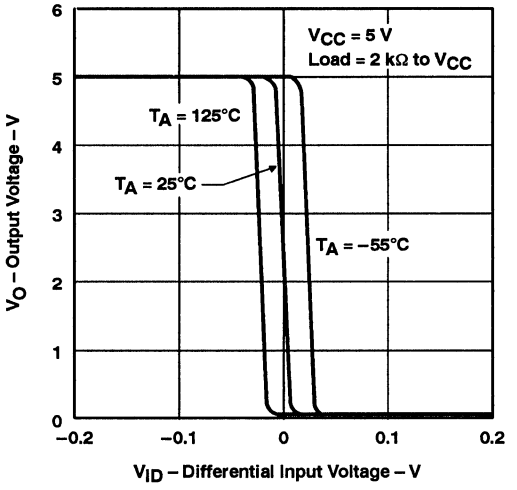


Figure 7

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

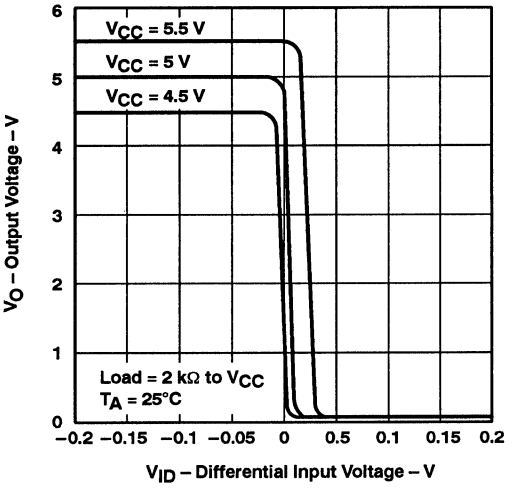


Figure 8

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

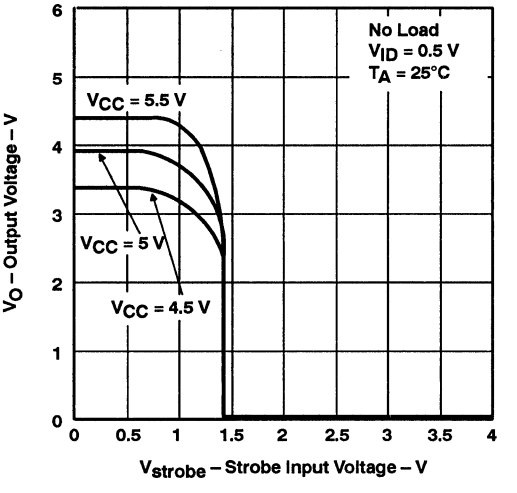


Figure 9

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

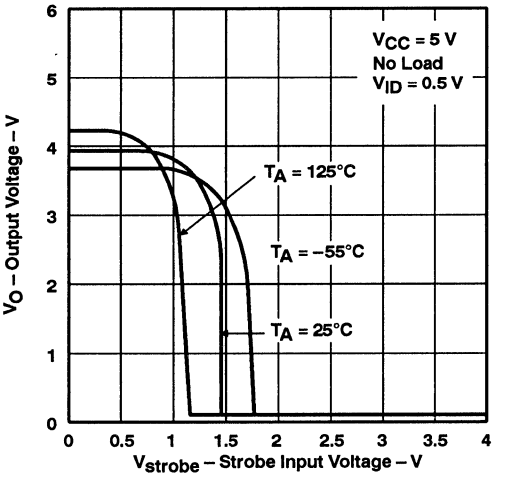


Figure 10

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
SUPPLY VOLTAGE

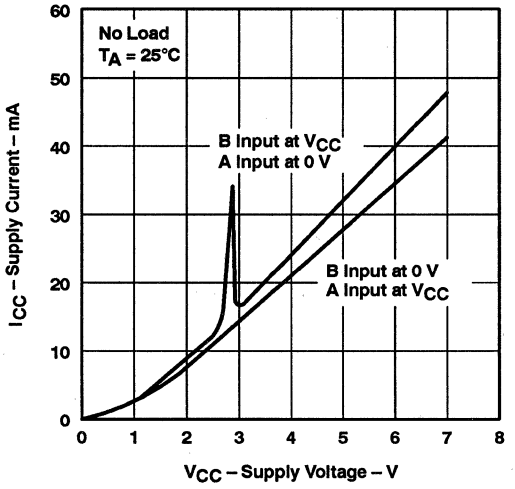


Figure 11

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
FREE-AIR TEMPERATURE

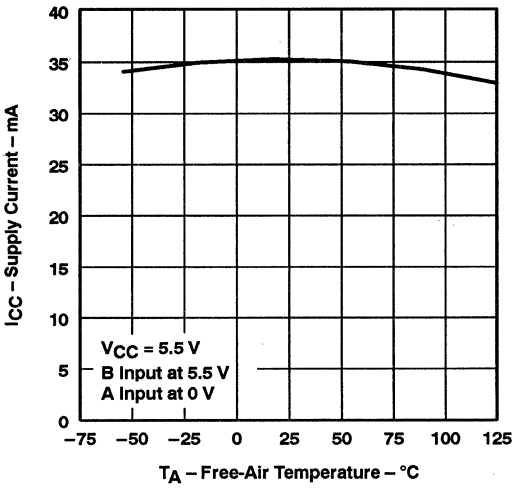


Figure 12

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

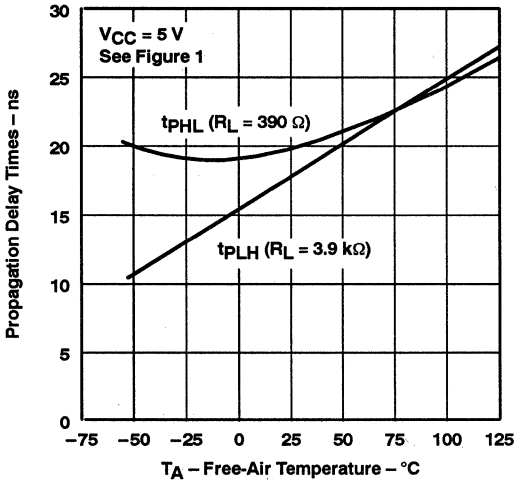


Figure 13

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

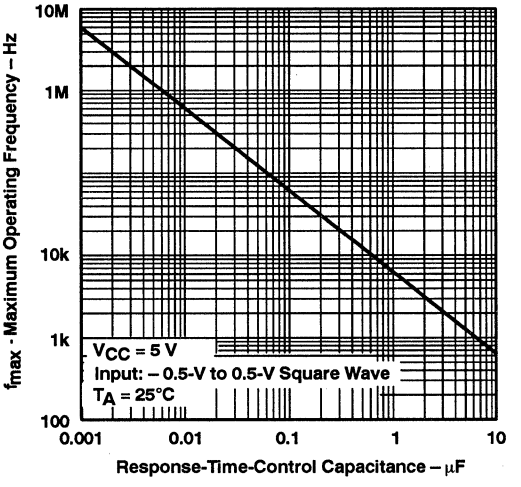
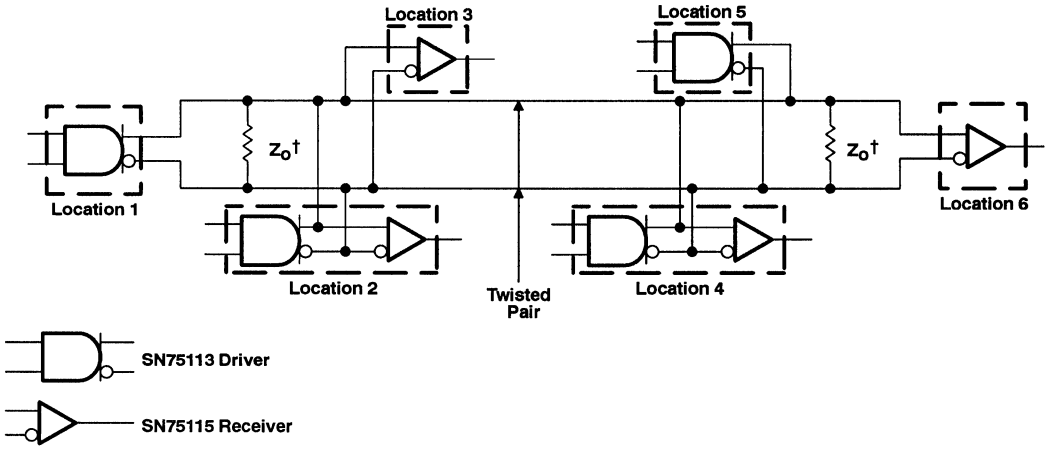


Figure 14

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



† A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 15. Basic Party-Line or Data-Bus Differential Data Transmission

SLLS073A – D2143, MAY 1976 – REVISED FEBRUARY 1993

features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe ('116, SN75117) or Enable (SN75118, SN75119)
- Designed for Party-Line (Data-Bus) Applications
- Choice of Ceramic or Plastic Packages

additional features of the SN55116/SN75116

- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency Response Control

additional features of the SN75117

- Driver Output Internally Connected to Receiver Input

The SN75118 is an SN75116 With 3-State Receiver Output Circuitry
The SN75119 is an SN75117 With 3-State Receiver Output Circuitry

description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a 3-state differential line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver inputs and receiver outputs are TTL compatible. The driver employed is similar to the SN55113/SN75113 3-state line driver, and the receiver is similar to the SN55115/SN75115 line receiver.

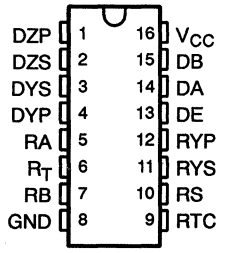
The '116 and SN75118 circuits offer all the features of the SN55113/SN75113 driver and the SN55115/SN75115 receiver combined. The driver performs the dual input AND and NAND functions when enabled or presents a high impedance to the load when in the disabled state. The driver output stages are similar to TTL totem-pole outputs, but have the current-sink portion separated from the current-sourcing portion and both are brought out to adjacent package pins. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink pins together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the '116 and SN75118 features a differential-input circuit having a common-mode voltage range of ±15 V. An internal 130-Ω resistor is also provided, which may optionally be used for terminating the transmission line. A frequency response control pin allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the '116 also has an output strobe and a split totem-pole output. The receiver of the SN75118 has an output-enable for the 3-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the V_{CC} and ground pins.

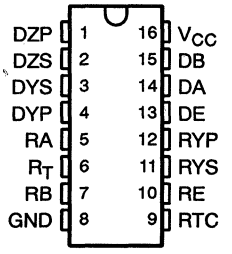
The SN75117 and SN75119 circuits provide the basic driver and receiver functions of the '116 and SN75118, but use a package that is only half as large. The SN75117 and SN75119 are intended primarily for party-line or bus-organized systems as the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input, and the SN75117 receiver has an output strobe while the SN75119 receiver has a 3-state-output enable. These devices do not, however, provide output connection options, line termination resistors, or receiver frequency-response controls.

The SN55116 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75116, SN75117, SN75118, and SN75119 are characterized for operation from 0°C to 70°C.

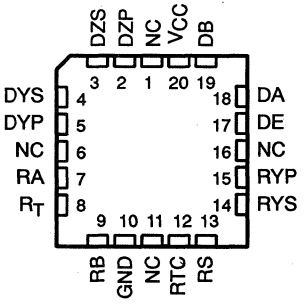
SN55116 . . . J PACKAGE
SN75116 . . . D OR N PACKAGE
(TOP VIEW)



SN75118 . . . D OR N PACKAGE
(TOP VIEW)

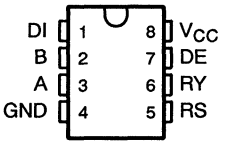


SN55116 . . . FK PACKAGE
(TOP VIEW)

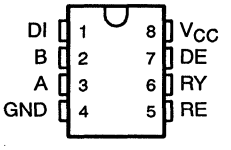


NC – No internal connection

SN75117 . . . D OR P PACKAGE
(TOP VIEW)



SN75119 . . . D OR P PACKAGE
(TOP VIEW)



Function Tables

'116, SN75118
DRIVER

INPUTS			OUTPUTS	
DE	DA	DB	DY	DZ
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

SN75117, SN75119
DRIVER

INPUTS		OUTPUTS	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

'116, SN75118
RECEIVER

RS/RE	DIFF INPUT	OUTPUTS RY	
		'116	SN75118
L	X	H	Z
H	L	H	H
H	H	L	L

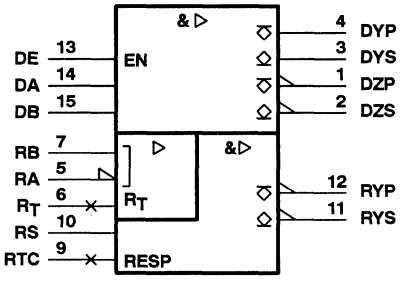
SN75117, SN75119
RECEIVER

INPUTS			OUTPUT RY	
A	B	RS/RE	SN75117	SN75119
H	L	H	H	H
L	H	H	L	L
X	X	L	H	Z

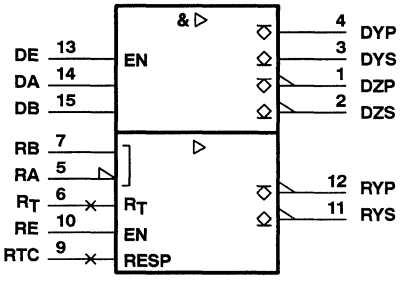
H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max)
L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max)
X = irrelevant
Z = high impedance (off)

logic symbols†

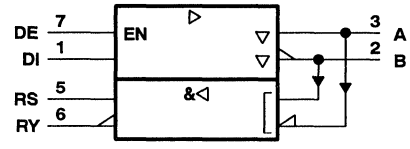
'116



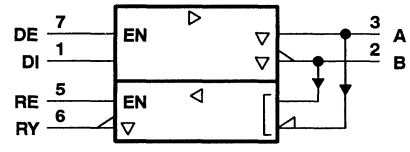
SN75118



SN75117



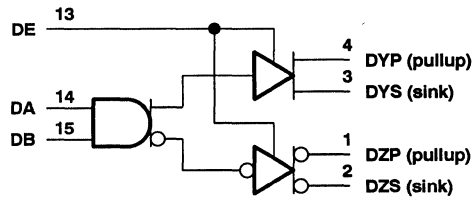
SN75119



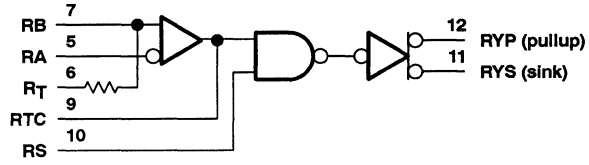
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

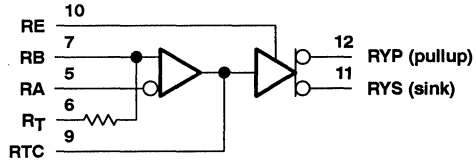
'116 AND SN75118



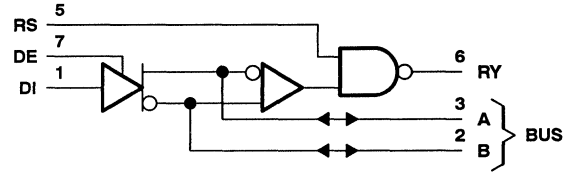
'116 Receiver



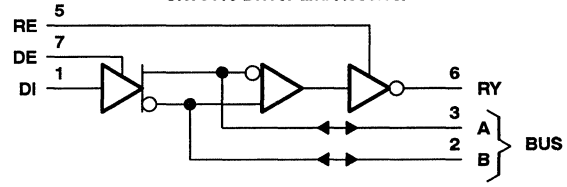
SN75118 Receiver



SN75117 Driver and Receiver



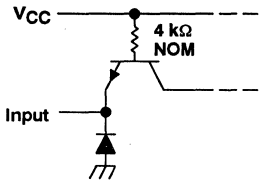
SN75119 Driver and Receiver



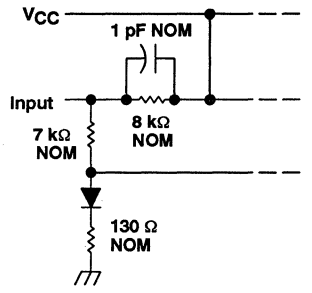
Pin numbers shown for the SN55116 are for the J package, those shown for the SN75118 are for the N package, those shown for SN75117 and SN75119 are for the P package.

schematics of inputs and outputs

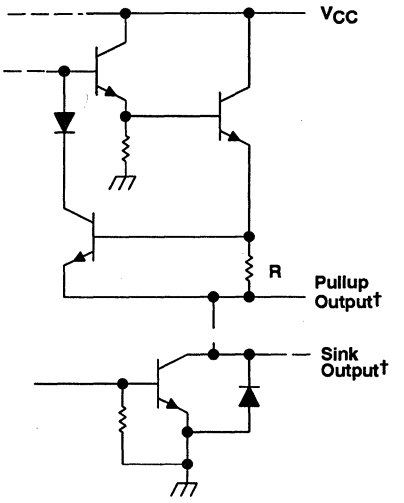
EQUIVALENT OF EACH DRIVER INPUT AND EACH RE AND RS INPUT



EQUIVALENT OF EACH RECEIVER INPUT (EXCLUDING ENABLES AND STROBES)



TYPICAL OF ALL OUTPUTS



Driver output R = 9 Ω NOM
Receiver output R = 20 Ω NOM
†On SN75117 and SN75119, common outputs replace the separate pullup and sink outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		'116, SN75118	SN75117, SN75119	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I	DA, DB, DE, DI, RE, RS	5.5	5.5	V
	RA, RB, RT	±25		
	A and B		0 to 6	
Off-state voltage applied to open-collector outputs		12		V

	SN55116	SN75116 THRU SN75119	UNIT
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 50	−65 to 50	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package		260	°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the FK and J packages, SN55116 chip is alloy mounted and SN75116 through SN75119 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	725 mW	5.8 mW/°C	464 mW	—
D (16 pin)	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

PARAMETER		SN55116			SN75'			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High-level input voltage, V_{IH}	All inputs except differential inputs	2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}	Drivers			−40			−40	mA
	Receivers			−5			−5	
Low-level output current, I_{OL}	Drivers			40			40	mA
	Receivers			15			15	
Receiver input voltage, V_I	'116, '118			±15			±15	V
	'117, '119	0		6	0		6	
Common-mode receiver input voltage, V_{ICR}	'116, '118			±15			±15	V
	'117, '119	0		6	0		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{IH} = 2 V	T_A = 25°C (SN55116) T_A = 0°C to 70°C (SN75')	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3		2	3		
				T_A = −55°C to 125°C (SN55')	I_{OH} = −10 mA	2			2			
					I_{OH} = −40 mA	1.8			1.8			
V_{OL}	Low-level output voltage		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.4			0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX,	I_O = −40 mA,	DE at 0.8 V			−1.5			−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55116			200				
					SN75'			20				
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX,	V_O = 0 to V_{CC},	DE at 0.8 V, T_A = 25°C			±10				μA
			V_{CC} = MAX, DE at 0.8 V, T_A = MAX	V_O = 0	SN55116			−300				
				V_O = 0.4 V to V_{CC}	SN55116			±150				
				V_O = 0 to V_{CC}	SN75'			±20				
I_I	Input current at maximum input voltage	Driver or enable input	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0,	T_A = 25°C	−40		−120	−40		−120	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX,	T_A = 25°C			42	60	42		60	mA

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

driver section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 13			14	30	ns
t_{PHL}	Propagation delay time, high-to-low level output				12	30	
t_{PZH}	Output enable time to high level	R_L = 180 Ω,	See Figure 14		8	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω,	See Figure 15		17	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω,	See Figure 14		16	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω,	See Figure 15		20	35	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER			TEST CONDITIONS†			'116, SN75118 MIN	'116, SN75118 TYP‡	'116, SN75118 MAX	SN75117, SN75119 MIN	SN75117, SN75119 TYP‡	SN75117, SN75119 MAX	UNIT
V_{T+}	Positive-going threshold voltage§		V_O = 0.4 V, See Note 3	I_{OL} = 15 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4			0.5			0.5	V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5			1			1	
V_{T-}	Negative-going threshold voltage§		V_O = 2.4 V, See Note 3	I_{OL} = −5 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4	−0.5¶			−0.5¶			V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5	−1¶			−1¶			
V_I	Input voltage range#		V_{CC} = 5 V,	V_{ID} = −1 V or 1 V,	See Note 3	15 to −15			6 to 0			V
V_{OH}	High-level output voltage		I_{OH} = −5 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = −0.5 V, See Notes 4 and 6	2.4			2.4			V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = −1 V, See Note 5	2.4			2.4			
V_{OL}	Low-level output voltage		I_{OL} = 15 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = 0.5 V, See Notes 4 and 7			0.4			0.4	V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = 1 V, See Note 5			0.4			0.4	
$I_{i(rec)}$	Receiver input current		V_{CC} = MAX, See Note 3	V_I = 0,	Other input at 0 V		−0.5	−0.9		−0.5	−1	mA
				V_I = 0.4 V,	Other input at 2.4 V		−0.4	−0.7		−0.4	−0.8	
				V_I = 2.4 V,	Other input at 0.4 V		0.1	0.3		0.1	0.4	
I_I	Input current at maximum input voltage	Strobe	V_{CC} = MIN, V_{strobe} = 4.5 V	V_{ID} = −0.5 V,	'116, SN75117			5			5	μA
		Enable	V_{CC} = MAX,	V_I = 5.5 V	SN75118, SN75119			1			1	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Differential voltages are at the B input terminal with respect to the A input terminal. Neither receiver input of the SN75117 or SN75119 should be taken negative with respect to GND.

¶ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Input voltage range is the voltage range that, if exceeded at either input, will cause the receiver to cease functioning properly.

NOTES: 3. Measurement of these characteristics on the SN75117 and SN75119 requires the driver to be disabled with the driver enable at 0.8 V.

4. This applies with the less positive receiver input grounded.
5. For '116 and SN75118, this applies with the more positive receiver input at 15 V or the more negative receiver input at – 15 V. For SN75117 and SN75119, this applies with the more positive receiver input at 6 V.
6. For SN55116, V_{ID} = −1 V.
7. For SN55116, V_{ID} = 1 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

receiver section

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V	SN75118, SN75119			40			40	μA
I_I	Low-level input current	Strobe	V_{CC} = MAX, V_{strobe} = 0.4 V	V_{ID} = 0.5 V, See Notes 4 and 7	'116, SN75117			−2.4			−2.4	mA
		Enable	V_{CC} = MAX,	V_I = 0.4 V	SN75118, SN75119			−1.6			−1.6	
$I_{(RC)}$	Response-time-control current (RTC)		V_{CC} = MAX, RC at 0 V,	V_{ID} = 0.5 V, See Notes 4 and 7	T_A = 25°C	−1.2						mA
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V, V_{ID} = −1 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55116,			200				
					SN75_			20				
I_{OZ}	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, RE at 0.4 V	T_A = 25°C	SN75118, SN75119			±10			±10	μA
				T_A = MAX	SN75118			±20				
					SN75119						±20	
R_T	Line-terminating resistance		V_{CC} = 5 V		T_A = 25°C	77		167				Ω
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_{ID} = −0.5 V,	V_O = 0, See Notes 4 and 6	T_A = 25°C	−15		−80	−15		−80	mA
I_{CC}	Short current (driver and receiver combined)		V_{CC} = MAX, See Notes 4 and 7	V_{ID} = 0.5 V,	T_A = 25°C		42	60		42	60	mA

† Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Not more than one output should be shorted at a time.

NOTES: 4. This applies with the less positive receiver input grounded.

6. For SN55116, V_{ID} = −1 V.

7. For SN55116, V_{ID} = 1 V.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

receiver section

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		R_L = 400 Ω,	See Figure 16		20	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output					17	75	ns
t_{PZH}	Output enable time to high level	SN75118 and SN75119 only	R_L = 480 Ω,	See Figure 14		9	20	ns
t_{PZL}	Output enable time to low level		R_L = 250 Ω,	See Figure 15		16	35	ns
t_{PHZ}	Output disable time from high level		R_L = 480 Ω,	See Figure 14		12	30	ns
t_{PLZ}	Output disable time from low level		R_L = 250 Ω,	See Figure 15		17	35	ns

TYPICAL CHARACTERISTICS

DRIVER OUTPUT VOLTAGE
vs
DRIVER INPUT VOLTAGE

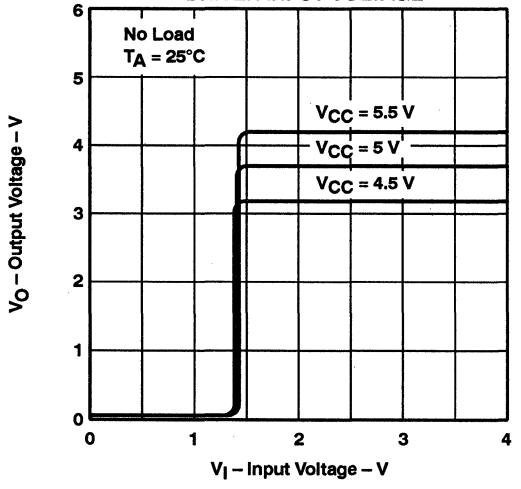


Figure 1

DRIVER OUTPUT VOLTAGE
vs
DRIVER INPUT VOLTAGE

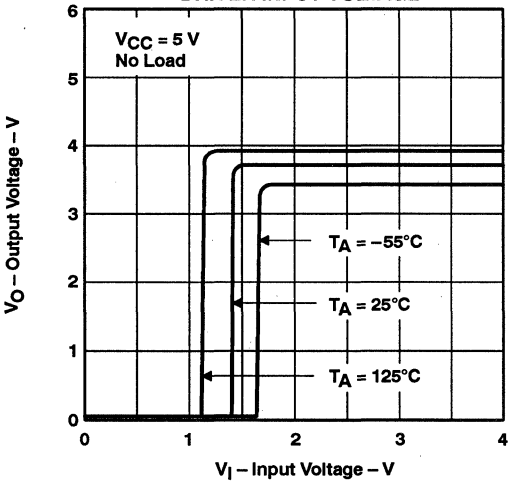


Figure 2

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

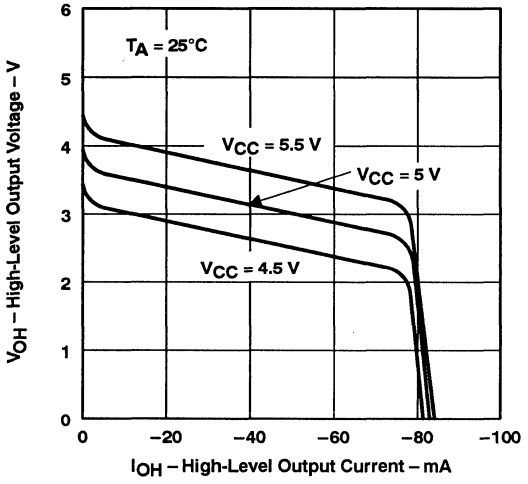


Figure 3

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

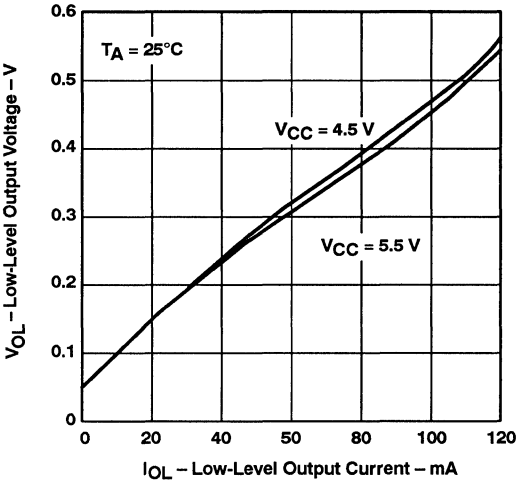


Figure 4

DRIVER PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE†

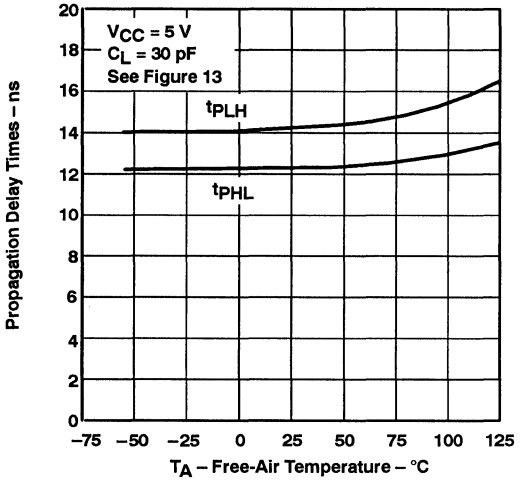


Figure 5

DRIVER OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE†

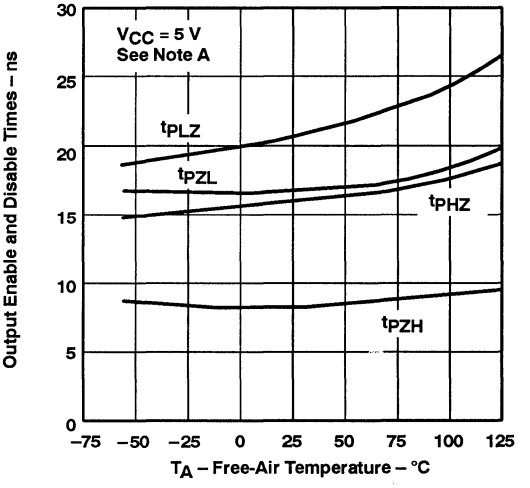


Figure 6

† Data for temperatures below 0°C and above 70°C are applicable to SN55116.
NOTE A: For t_{PZH} and t_{PHZ}: R_L = 180 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

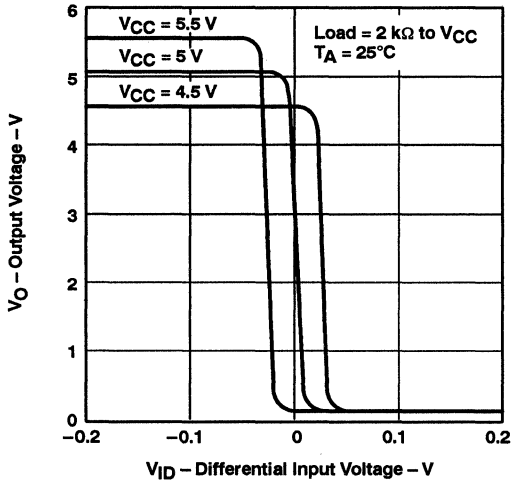


Figure 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE†

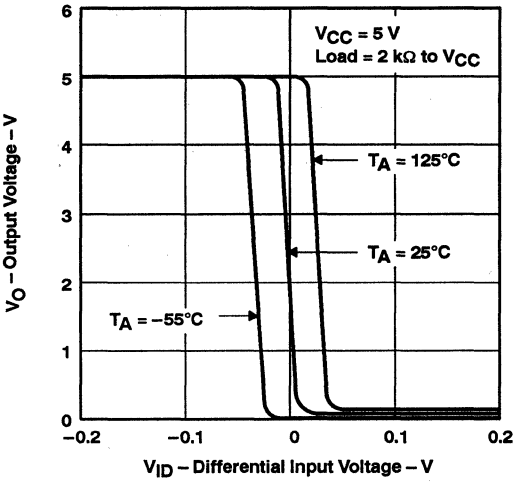


Figure 8

RECEIVER PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE†

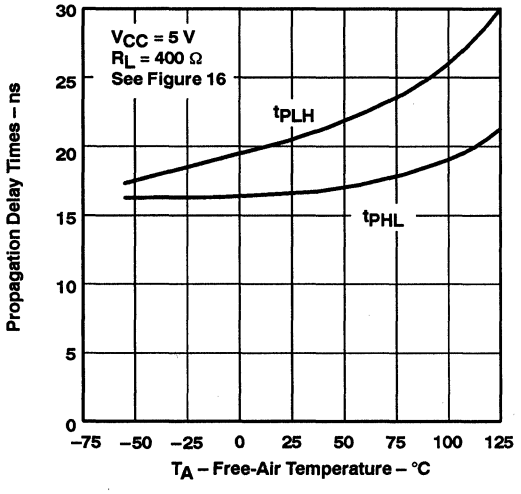


Figure 9

RECEIVER OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE†

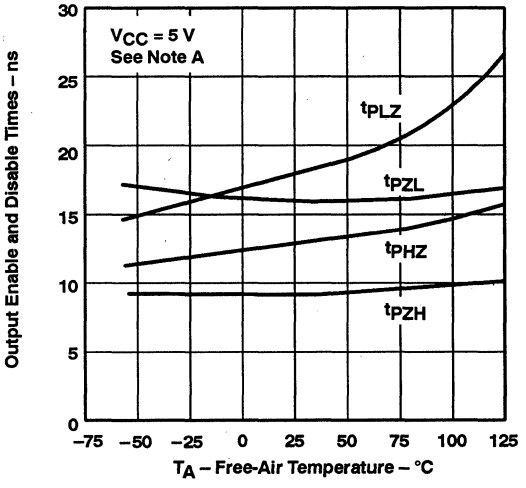


Figure 10

† Data for temperatures below 0°C and above 70°C are applicable to SN55116.
NOTE A: For t_{PZH} and t_{PHZ} :R_L= 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

**SUPPLY CURRENT (DRIVER AND RECEIVER)
vs
SUPPLY VOLTAGE**

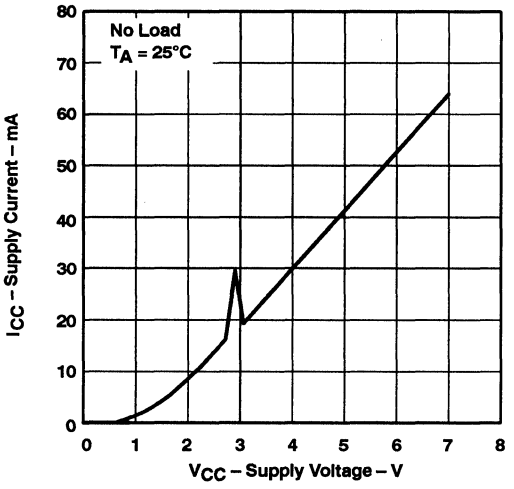


Figure 11

**SUPPLY CURRENT (DRIVER AND RECEIVER)
vs
FREE-AIR TEMPERATURE†**

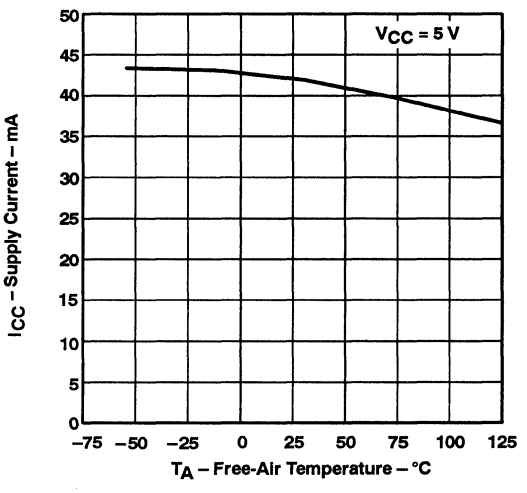


Figure 12

† Data for temperatures below 0°C and above 70°C are applicable to SN55116.

PARAMETER MEASUREMENT INFORMATION

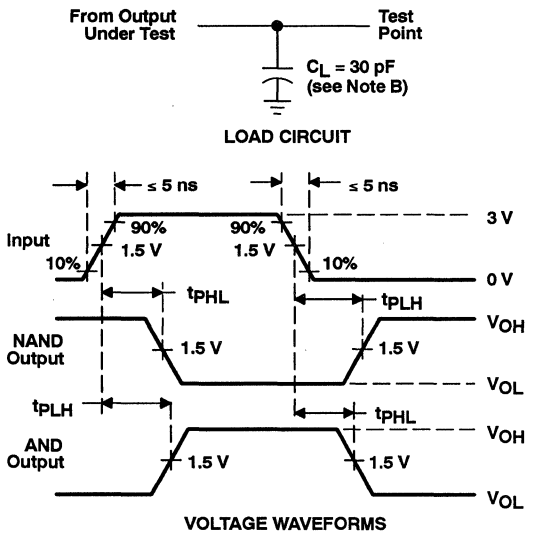


Figure 13. t_{PLH} and t_{PHL} (drivers only)

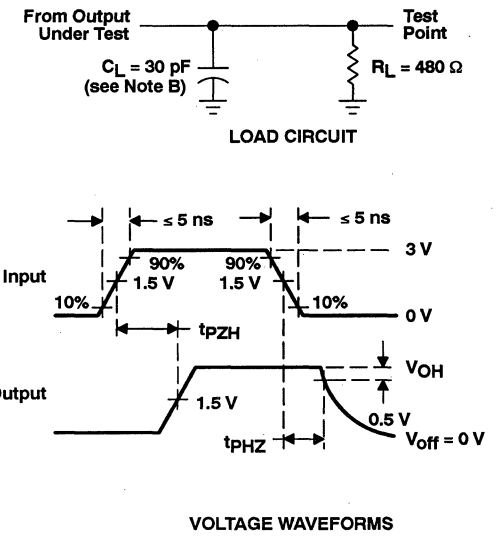


Figure 14. t_{PZH} and t_{PHZ}

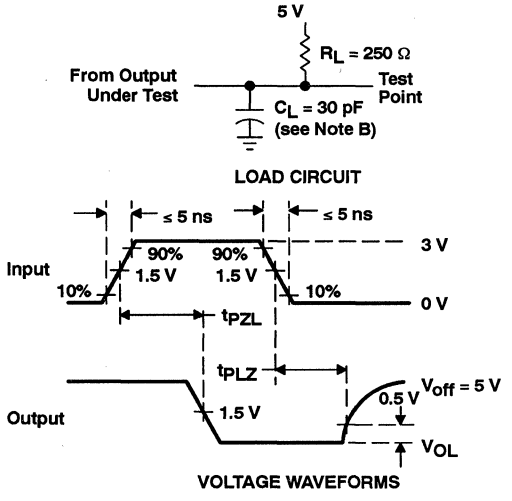


Figure 15. t_{PZL} and t_{PLZ}

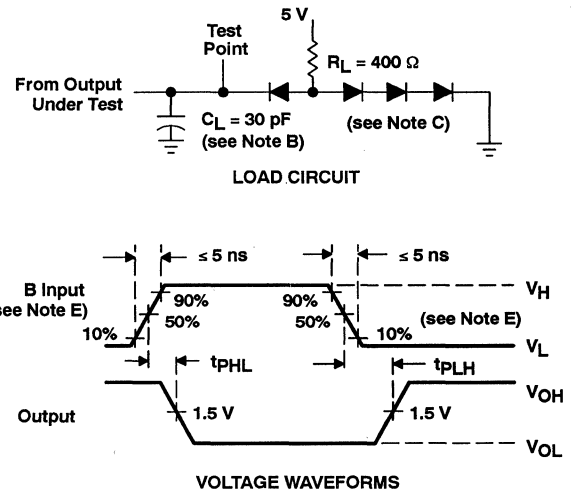


Figure 16. t_{PLH} and t_{PHL} (receivers only)

NOTES: A. Input pulses are supplied by generators having the following characteristics Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. When testing the '116 and SN75118 receiver sections, the response-time control and the termination resistor pins are left open.
E. For '116 and SN75118, V_H = 3 V, V_L = – 3 V, the A input is at 0 V.
For SN75117 and SN75119, V_H = 3 V, V_L = 0, the A input is at 1.5 V.

SLLS074A – D1334, SEPTEMBER 1973 – REVISED FEBRUARY 1993

- **Designed for Digital Data Transmission Over 50-Ω to 500-Ω Coaxial Cable, Strip Line, or Twisted Pair**
- **High Speed**
  t_{pd} = 20 ns Max at C_L = 15 pF
- **TTL Compatible With Single 5-V Supply**
- **2.4-V Output at I_{OH} = −75 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **Designed for Use With Triple Line Receivers SN55122, SN75122**
- **Designed to Be Interchangeable With Signetics N8T13**

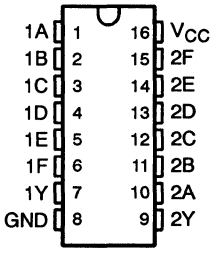
description

The SN55121 and SN75121 dual line drivers are designed for digital data transmission over lines having impedances from 50 to 500 Ω. They are also compatible with standard TTL logic and supply voltage levels.

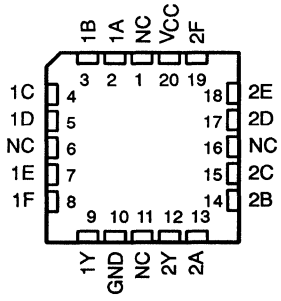
The low-impedance emitter-follower outputs of the SN55121 and SN75121 will drive terminated lines such as coaxial cable or twisted pairs. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55121 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75121 is characterized for operation from 0°C to 70°C.

SN55121 . . . J PACKAGE
SN75121 . . . D OR N PACKAGE
(TOP VIEW)



SN55121 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

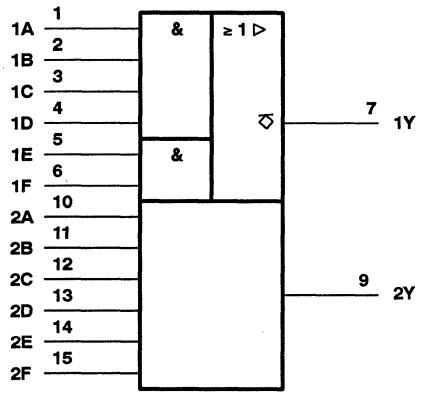
THE SN75121 IS NOT RECOMMENDED FOR NEW DESIGN

FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

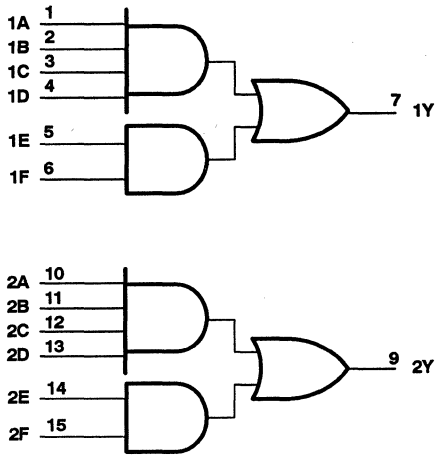
H = high level L = low level X = irrelevant

logic symbol†

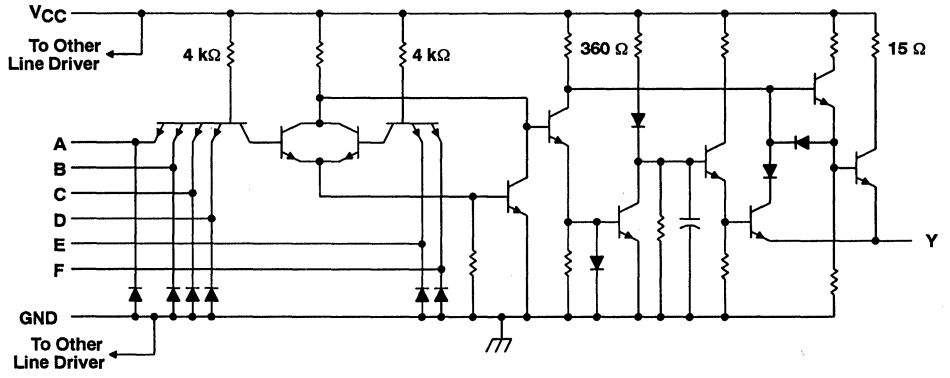


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



schematic (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55121	SN75121	UNIT
Supply voltage, V_{CC} (see Note 1)	6	6	V
Input voltage	6	6	V
Output voltage	6	6	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

NOTE 1: All voltage values are with respect to both ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

† In the FK and J packages, SN55121 chips are either silver glass or alloy mounted.

recommended operating conditions

	SN55121			SN75121			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−75			−75	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)}$	Breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = −75 mA,	See Note 2	2.4		V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 2	V_{OH} = 2 V,	−100	−250	mA
I_{OL}	Low-level output current	V_{IL} = 0.8 V,	V_{OL} = 0.4 V,	See Note 2		−800	μA
$I_{O(off)}$	Off-state output current	V_{CC} = 3 V,	V_O = 3 V			500	μA
I_{IH}	High-level output current	V_I = 4.5 V				40	μA
I_{IL}	Low-level output current	V_I = 0.4 V			−0.1	−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5 V,	T_A = 25°C			−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

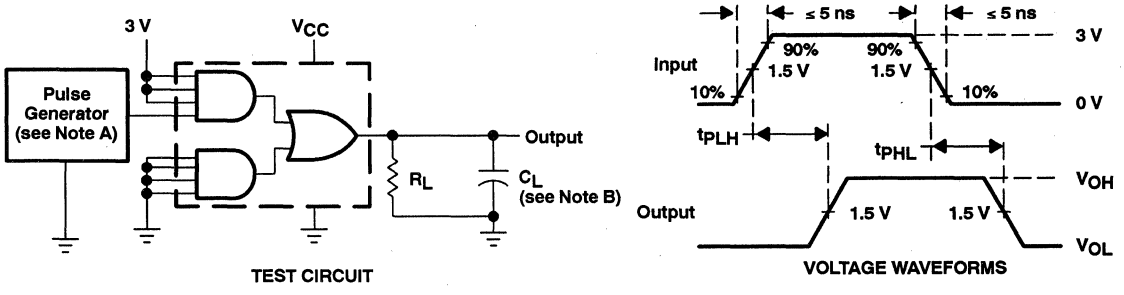
† Not more than one output should be shorted at a time.

NOTE 2: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 37 Ω,	C_L = 15 pF,	See Figure 1		11	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					8	20	
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 37 Ω,	C_L = 1000 pF,	See Figure 1		22	50	ns
t_{PHL}	Propagation delay time, high-to-low level output					20	50	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generators have the following characteristics: Z_O ≈ 50 Ω, t_w = 200 ns, duty cycle ≤ 50%, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

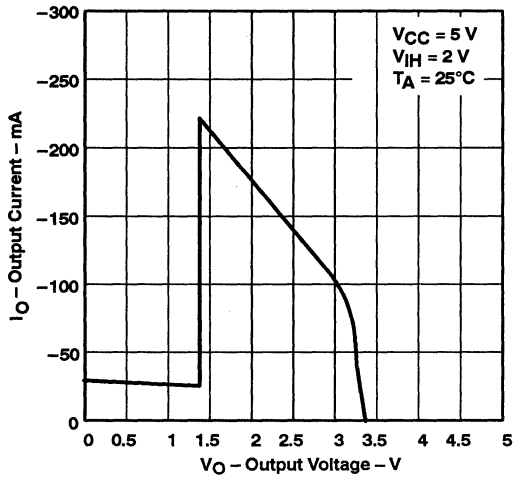


Figure 2

APPLICATION INFORMATION

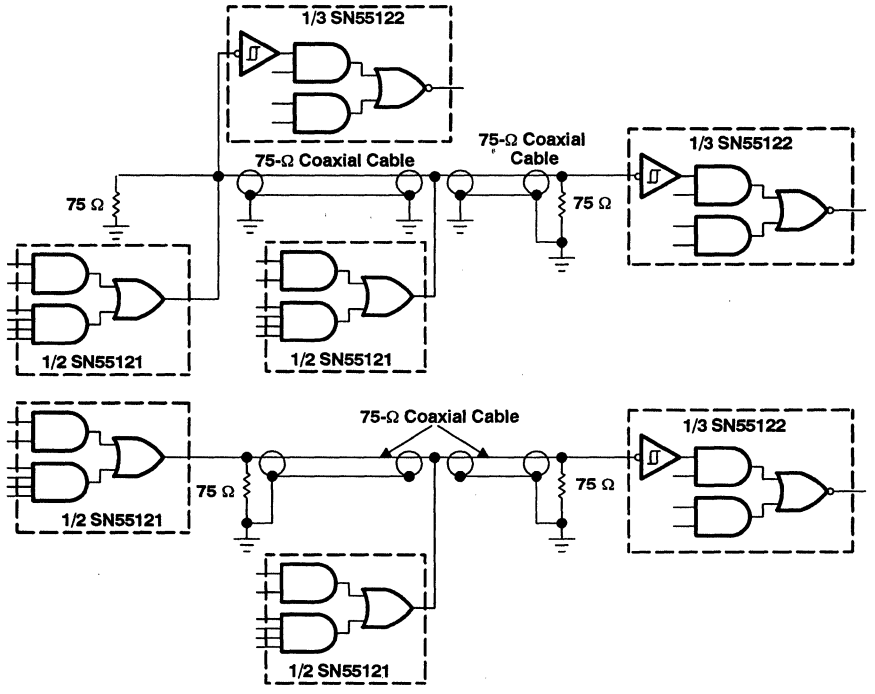
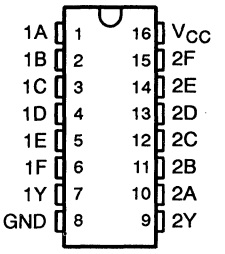


Figure 3. Single-Ended Party Line Circuits

SLLS030A – D1334, SEPTEMBER 1987 – REVISED AUGUST 1989

- **Permits Digital Data Transmission Over Coaxial Cable, Strip Line, or Twisted Pair**
- **Operates With 50-Ω to 500-Ω Transmission Lines**
- **TTL Compatible With 5-V Supply**
- **2.4-V Output at I_{OH} = –75 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **IMPACT™ Low-Power Schottky Technology**
- **Improved Replacement for the SN75121 and Signetics 8T13**
- **Glitchless Power Up/Power Down**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **High Speed . . . Maximum Propagation Delay Time of 14 ns at C_L = 15 pF**

D OR N PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGN

description

The SN75ALS121 dual line driver is designed for digital data transmission over lines having impedances from 50 to 500 Ω. It is compatible with standard TTL logic and supply voltage levels.

FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level, L = low level, X = irrelevant

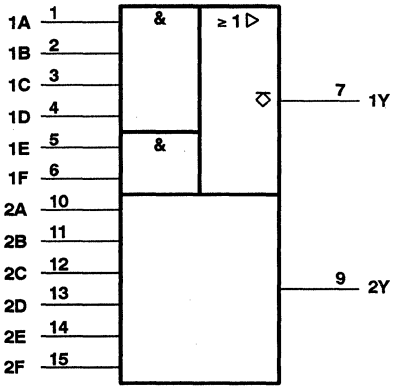
The low-impedance emitter-follower outputs drive terminated lines such as coaxial cable, strip line, or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All inputs are in conventional TTL configuration. Gating can be used during power-up and power-down sequences to ensure that no noise is introduced on the line.

The SN75ALS121 employs the IMPACT™ process to achieve fast switching speeds, low power dissipation, and reduced input current requirements.

The SN75ALS121 is characterized for operation from 0°C to 70°C.

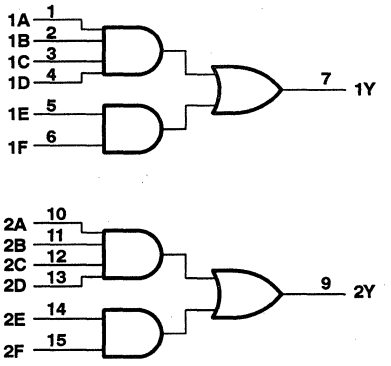
IMPACT is a trademark of Texas Instruments Incorporated.

logic symbol†

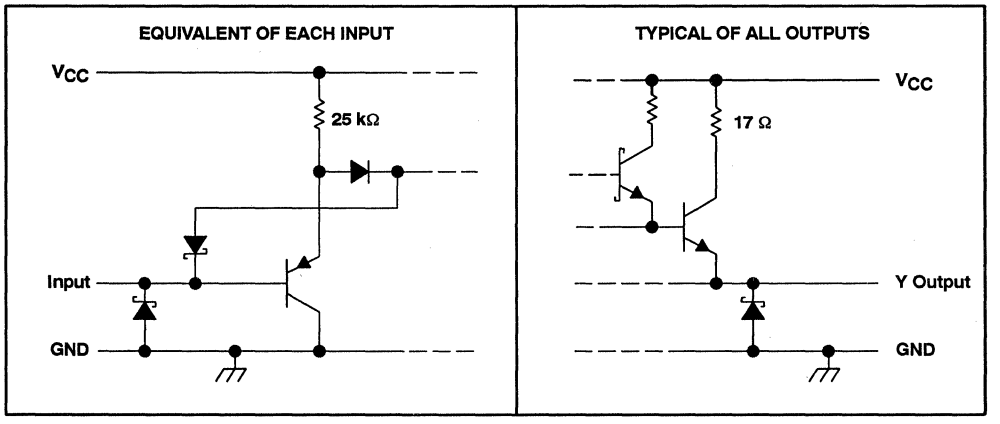


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Input voltage ..... 6 V
Output voltage ..... 6 V
Continuous total dissipation at (or below) 25°C free air temperature ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 75	mA
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = –12 mA				– 1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = –75 mA,	See Note 2	2.4	3.2		V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 2	V_{OH} = 2 V,	– 100	– 200	– 250	mA
I_{OL}	Low-level output current	V_{IL} = 0.8 V,	V_{OL} = 0.4 V,	See Note 2			– 800	µA
$I_{O(off)}$	Off-state output current	V_{CC} = 3 V,	V_O = 3 V				500	µA
I_{IH}	High-level input current	V_I = 4.5 V					40	µA
I_{IL}	Low-level input current	V_I = 0.4 V					– 250	µA
I_{OS}	Short-circuit output current	V_{CC} = 5 V				– 5	– 30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	No load		9	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	No load		13	30	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

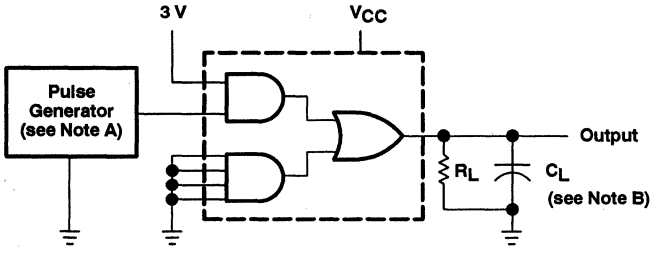
NOTE 2: The output voltage and current limits are ensured for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

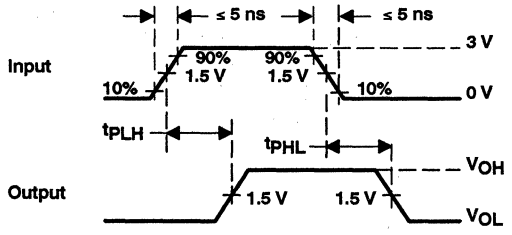
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω,	C_L = 15 pF,	See Figure 1		6	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					4	14	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω,	C_L = 1000 pF,	See Figure 1		18	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output					29	50	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 200 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

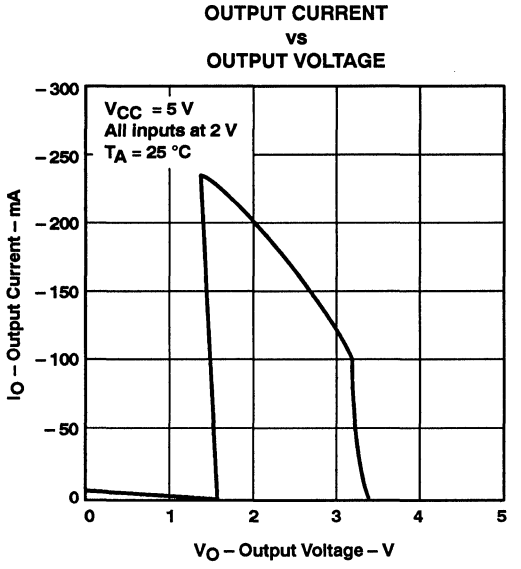
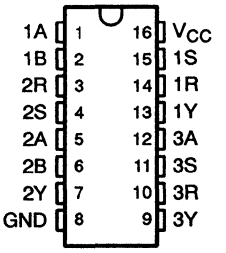


Figure 2

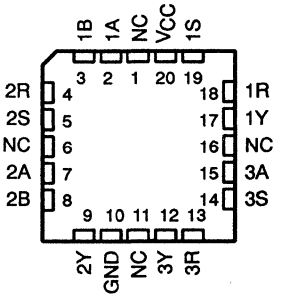
SLLS075A – D1334, SEPTEMBER 1973 – REVISED FEBRUARY 1993

- **Designed for Digital Data Transmission Over Coaxial Cable, Strip Line, or Twisted Pair**
- **Designed for Operation With 50-Ω to 500-Ω Transmission Lines**
- **TTL Compatible**
- **Single 5-V Supply**
- **Built-Input Threshold Hysteresis**
- **High-Speed . . . Typical Propagation Delay Time = 20 ns**
- **Independent Channel Strobes**
- **Input Gating Increases Application Flexibility**
- **Fanout to 10 Series 54/74 Standard Loads**
- **Can Be Used With Dual Line Drivers SN55121 and SN75121**
- **Interchangeable With Signetics N8T14**

SN55122 . . . J PACKAGE
N8T14, SN75122 . . . D OR N PACKAGE
(TOP VIEW)



SN55122 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE N8T14 AND SN75122 ARE NOT RECOMMENDED FOR NEW DESIGN

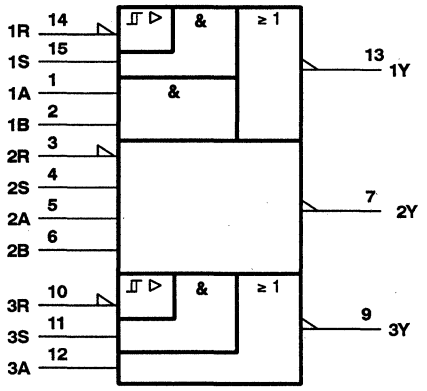
description

The N8T14, SN55122, and SN75122 are triple line receivers that are designed for digital data transmission over lines having impedances from 50 Ω to 500 Ω. They are also compatible with standard TTL-logic and supply voltage levels.

The N8T14, SN55122, and SN75122 have receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. The high impedance of this input presents a minimum load to the driver and allows termination of the transmission line in its characteristic impedance to minimize line reflection. An open line will affect the receiver input as would a low-level voltage. The receiver can withstand a level of −0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

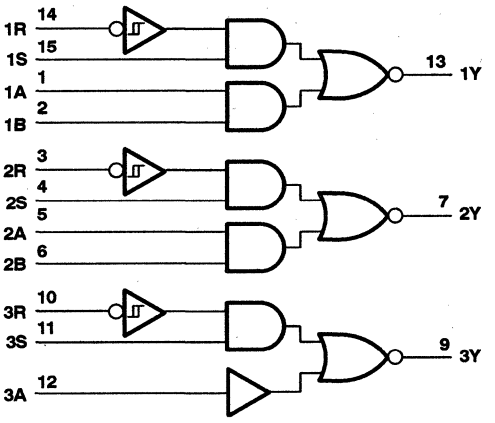
The SN55122 is characterized for operation over the full military temperature range of −55°C to 125°C. The N8T14 and SN75122 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram

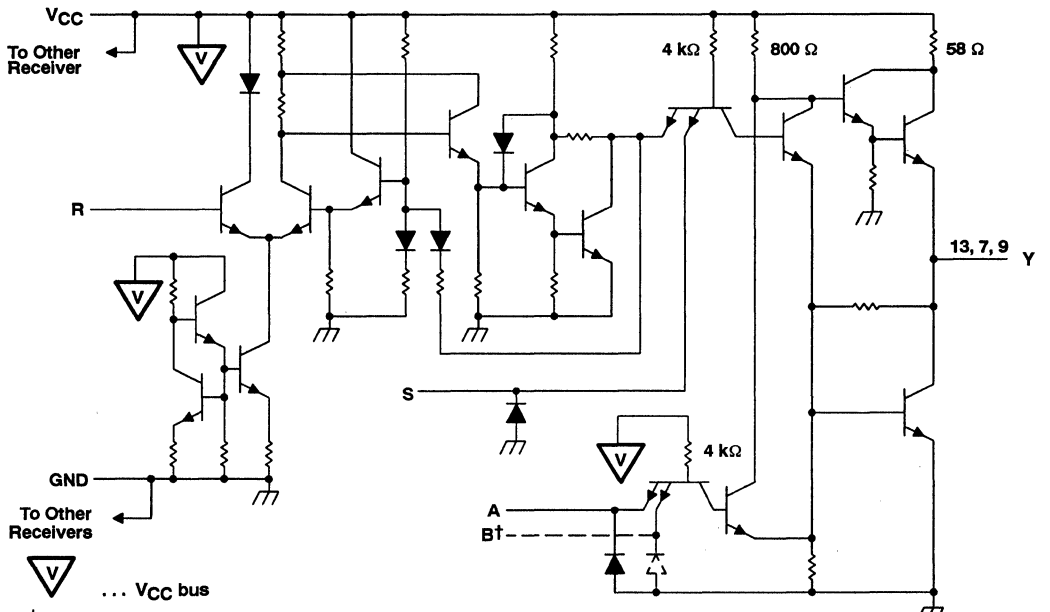


FUNCTION TABLE

INPUTS				OUTPUT
A	B‡	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

‡ B input and last two lines of the function table are applicable to receivers 1 and 2 only.
H = high level, L = low level, X = irrelevant

schematic diagram (each receiver)



† B input is provided on receivers 1 and 2 only.
Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Input voltage: R input ..... 6 V
A, B, or S input ..... 5.5 V
Output voltage ..... 6 V
Output current ..... ±100 mA
Continuous total power dissipation (see Note 2) ..... See Dissipation Rating Table
Operating free-air temperature range: SN55122 ..... −55°C to 125°C
N8T14, SN75122 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The SN55122 chips are alloy mounted, and the SN75122 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A, B, R, or S	2			V
Low-level input voltage, V_{IL}	A, B, R, or S			0.8	V
High-level output current, I_{OH}				−500	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN55122	−55		125	°C
	SN75122	0		70	

electrical characteristics over recommended operating free-air temperature, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

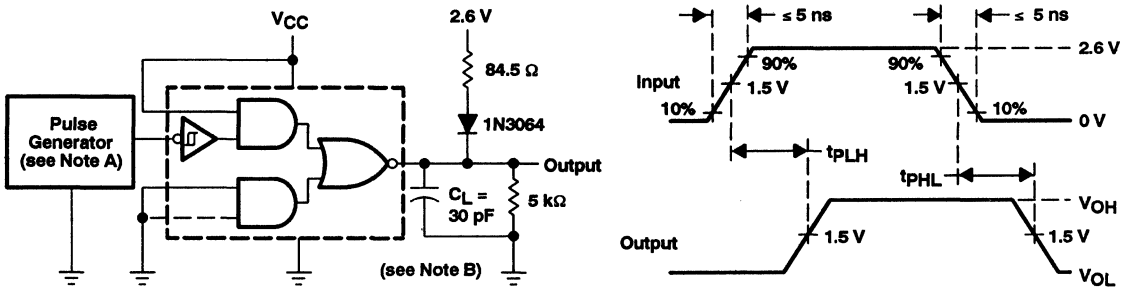
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	R	V_{CC} = 5 V,	T_A = 25°C,	See Figures 2 and 4	0.3	0.6		V
V_{IK}	Input clamp voltage	A, B, or S	V_{CC} = 5 V,	I_I = −12 mA				−1.5	V
$V_{I(BR)}$	Input breakdown voltage	A, B, or S	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage		V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = −500 μA	2.6			V
			$V_{I(A)}$ = 0, $V_{I(R)}$ = 1.45 V,	$V_{I(B)}$ = 0, I_{OH} = −500 μA,	$V_{I(S)}$ = 2 V, See Note 3	2.6			
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 16 mA			0.4	V
			$V_{I(A)}$ = 0, $V_{I(R)}$ = 1.45 V,	$V_{I(B)}$ = 0, I_{OL} = 16 mA,	$V_{I(S)}$ = 2 V, See Note 4			0.4	
I_{IH}	High-level input current	A, B, or S	V_I = 4.5 V					40	μA
		R	V_I = 3.8 V					170	
I_{IL}	Low-level input current	A, B, or S	V_I = 0.4 V,	V_{IR} = 0.8 V		−0.1		−1.6	mA
I_{OS}‡	Short-circuit output current		V_{CC} = 5 V,	T_A = 25°C		−50		−100	mA
I_{CCH}	High-level supply current		V_{CC} = MAX,	All inputs at 0.8 V,	Outputs open			72	mA
I_{CCL}	Low-level supply current		V_{CC} = MAX,	All inputs at 2 V,	Outputs open			100	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. The receiver input is high immediately before being reduced to 1.45 V.
4. The receiver input is low immediately before being increased to 1.45 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 200 ns, duty cycle = 50%, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

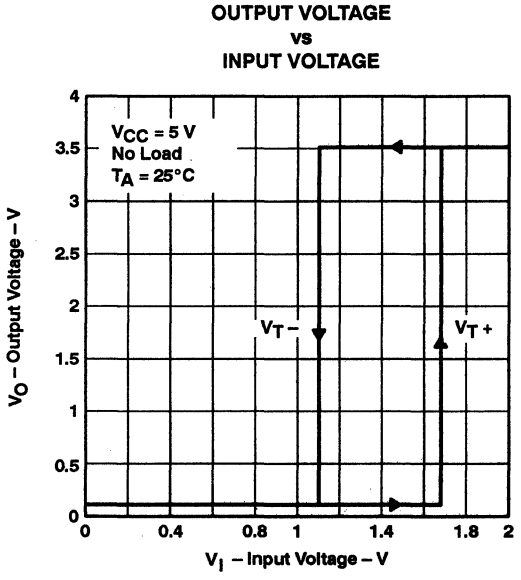


Figure 2

APPLICATION INFORMATION

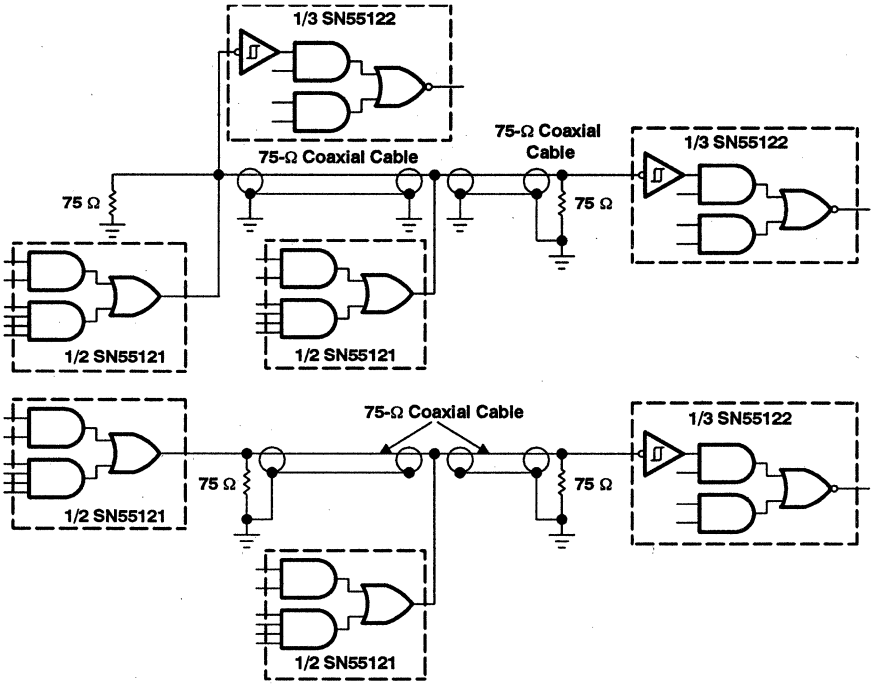
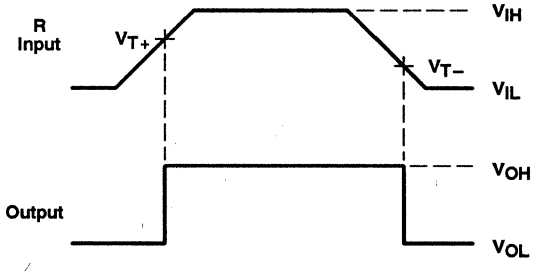


Figure 3. Single-Ended Party Line Circuits



NOTE: The high gain and built-in hysteresis of the SN55122 and SN75122 line receivers enable them to be used as Schmitt triggers in squaring pulses.

Figure 4. Pulse Squaring

SLLS086A – D1322, SEPTEMBER 1973 – REVISED JANUARY 1993

- **Meets IBM System 360 input/Output interface Specifications**
- **Operates From Single 5-V Supply**
- **TTL Compatible**
- **3.11-V Output at I_{OH} = −59.3 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **Designed for Use With Triple Line Receiver SN75124**
- **Designed to Be Interchangeable With Signetics N8T13 and N8T23**

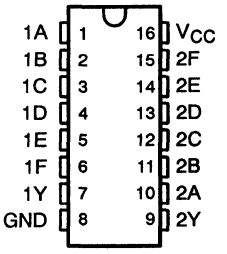
description

The N8T13, N8T23, and SN75123 are dual line drivers specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the N8T13, N8T23, and SN75123 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The N8T13, N8T23, and SN75123 are characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

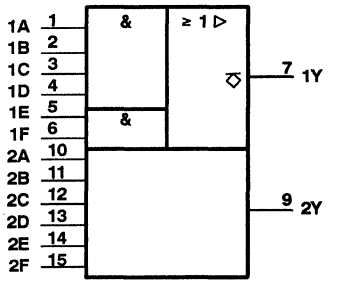


FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

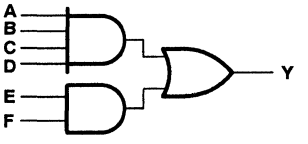
H = high level, L = low level, X = irrelevant

logic symbol†

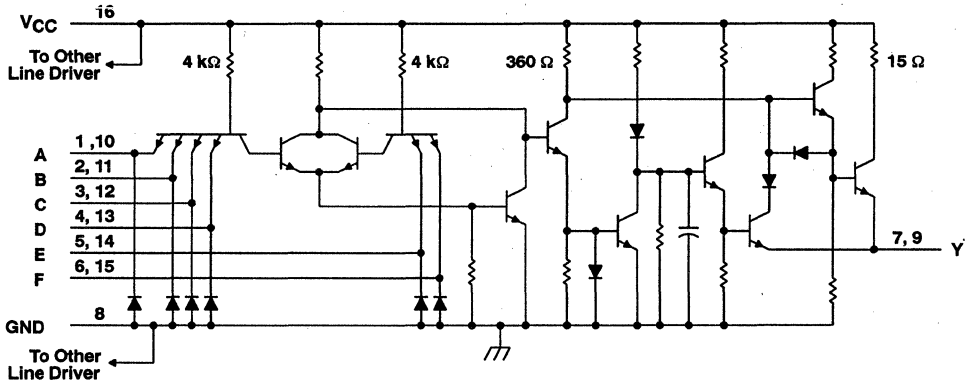


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Output voltage, V_O ..... 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): D package .... 950 mW
N package ... 1150 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–100	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{CC} = 5 V, I_{OH} = −59.3 mA,	V_{IH} = 2 V, See Note 3	T_A = 25°C	3.11		V
				T_A = 0°C to 70°C	2.9		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = −240 μA,	See Note 3		0.15	V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−250	mA
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V			40	μA
I_{IH}	High-level input current	V_I = 4.5 V				40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1	−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5 V,	T_A = 25°C			−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

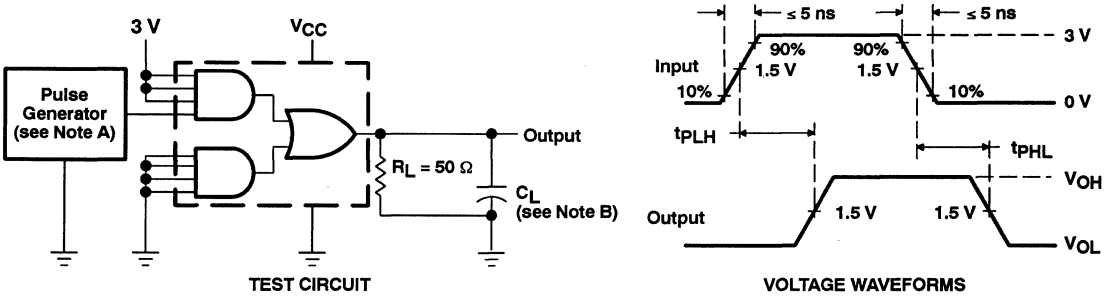
† Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω,	C_L = 15 pF,	See Figure 1		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω,	C_L = 100 pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	25	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω; t_w = 200 ns, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

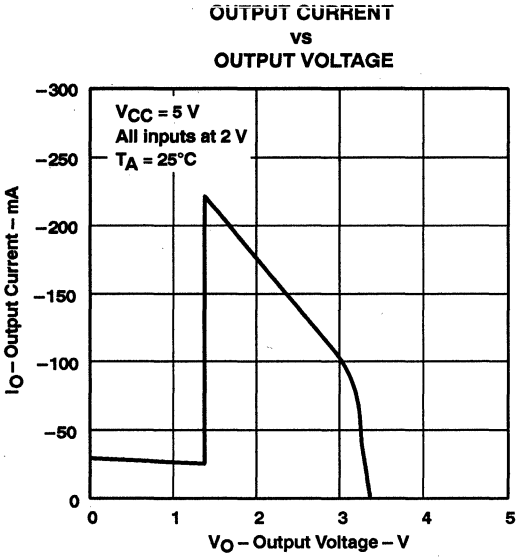


Figure 2

APPLICATION INFORMATION

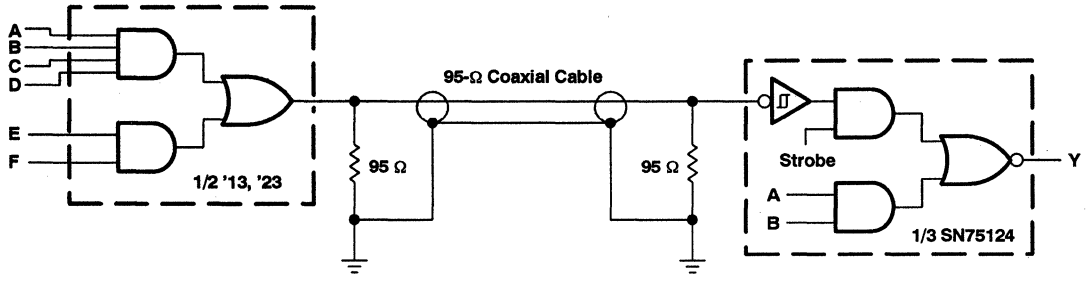
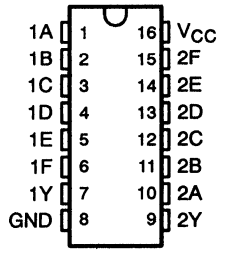


Figure 3. Unbalanced Line Communication Using '13, '23, and '124

SLLS031B – D1332, SEPTEMBER 1987 – REVISED FEBRUARY 1993

- **Meets IBM 360 Input Interface Specifications**
- **Permits Digital Data Transmission Over Coaxial Cable, Strip Line, or Twisted Pair**
- **TTL Compatible With 5-V Supply**
- **3.11-V Output at I_{OH} = – 59.3 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **IMPACT™ Low-Power Schottky Technology**
- **Improved Replacement for the SN75123 and Signetics 8T13**
- **Glitchless Power-Up/Power-Down Protection**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **High Speed . . . Maximum Propagation Delay Time of 14 ns at C_L = 15 pF**

D PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGN

description

The SN75ALS123 dual line driver is specifically designed to meet the input interface specifications for the IBM System 360. It is compatible with standard TTL logic and supply voltage levels. The low-impedance, emitter-follower outputs drive terminated lines such as coaxial cable, strip line, or twisted pair. The uncommitted output allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All inputs are in conventional TTL configuration. Gating can be used during power-up and power-down sequences to ensure that no noise is introduced on the line.

The SN75ALS123 employs the IMPACT™ process to achieve fast switching speeds, low power dissipation, and reduced input current requirements.

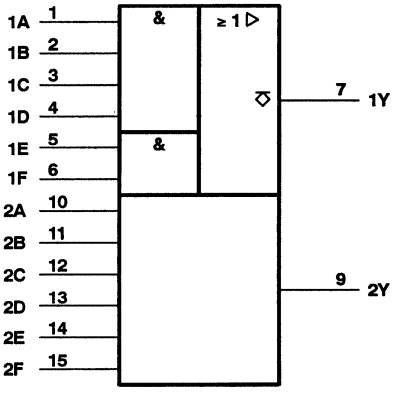
The SN75ALS123 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

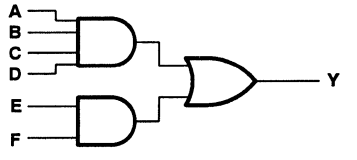
H = high level L = low level X = irrelevant

logic symbol†



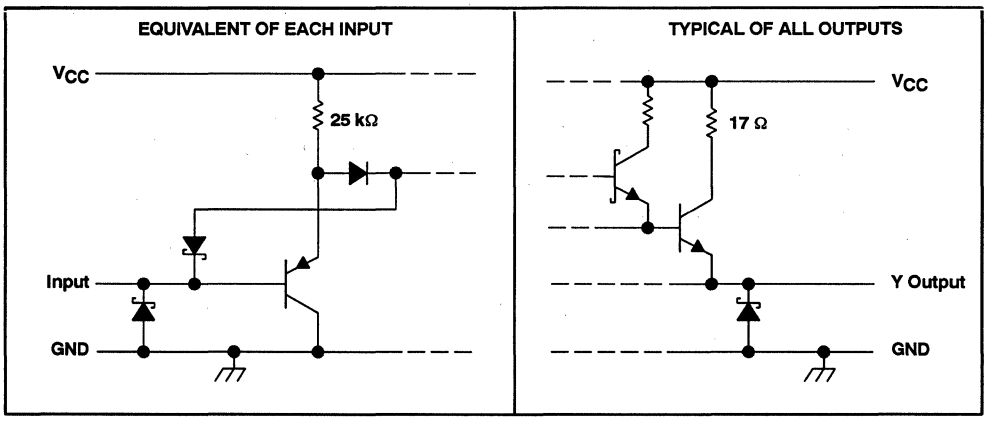
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



IMPACT is a trademark of Texas Instruments Incorporated.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Output voltage ..... 6 V
Continuous total dissipation at (or below) 25°C free air temperature (see Note 2) ..... 950 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate to 608 mW at 70°C at the rate of 7.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–100	mA
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = –12 mA				–1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage	V_{CC} = 5 V, See Note 3	V_{IH} = 2 V,	I_{OH} = –59.3 mA,	2.9			V
		V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 2 V, See Note 3	I_{OH} = –59.3 mA,	3.11	3.3		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = –240 µA,	See Note 3			0.15	V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	–100	–200	–250	mA
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V				40	µA
I_{IH}	High-level input current	V_I = 4.5 V					40	µA
I_{IL}	Low-level input current	V_I = 0.4 V					–250	µA
I_{OS}	Short-circuit output current	V_{CC} = 5 V				–5	–30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	No load		9	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	No load		13	30	mA

NOTE 3: The output voltage and current limits are ensured for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω,	C_L = 15 pF,	See Figure 1		4	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					5	14	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω,	C_L = 100 pF,	See Figure 1		8	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

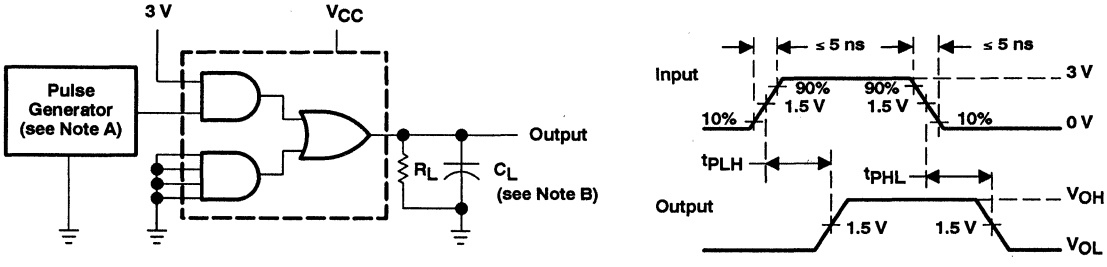


Figure 1. Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 200 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

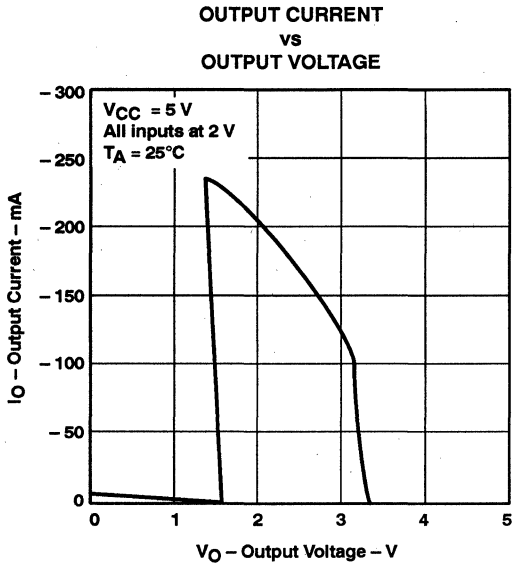


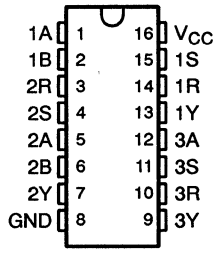
Figure 2

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SLLS058A – D1322, SEPTEMBER 1973 – REVISED JANUARY 1993

- **Meets IBM System 360 Input/Output Interface Specifications**
- **Operates From Single 5-V Supply**
- **TTL Compatible**
- **Built-In Input Threshold Hysteresis**
- **High Speed . . . Typical Propagation Delay Time = 20 ns**
- **Independent Channel Strobes**
- **Input Gating Increases Application Flexibility**
- **Designed for Use With Dual Line Driver SN75123**
- **Designed to Be Interchangeable With Signetics N8T24**

D OR N PACKAGE
(TOP VIEW)



description

The SN75124 triple line receiver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of −0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

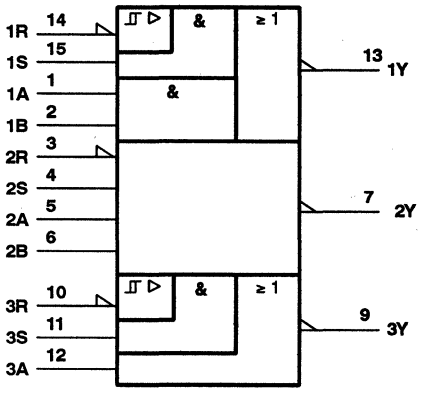
The SN75124 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

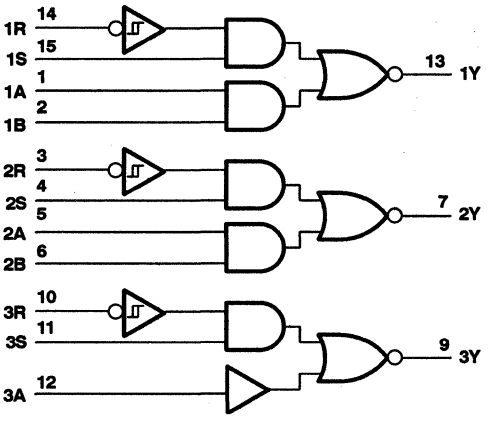
† B input and last two lines of the function table are applicable to receivers 1 and 2 only.

logic symbol†

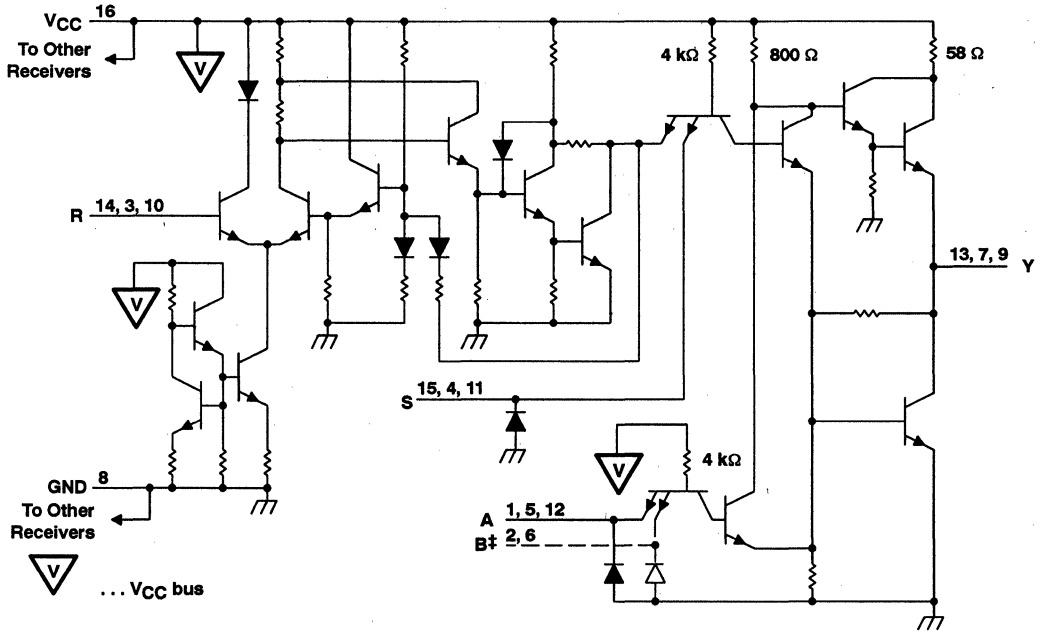


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematic (each receiver)



‡ B input is provided on receivers 1 and 2 only.
Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I: R input with V_{CC} applied ..... 7 V
R input with V_{CC} not applied ..... 6 V
A, B, or S input ..... 5.5 V
Output voltage, V_O ..... 7 V
Output current, I_O ..... ±100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 MW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A, B, or S	2			V
	R	1.7			
Low-level input voltage, V_{IL}	A, B, or S			0.8	V
	R			0.7	
High-level output current, I_{OH}				−800	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	R	V_{CC} = 5 V,	T_A = 25°C	0.2	0.5		V
V_{IK}	Input clamp voltage	A, B, or S	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	A, B, or S	V_{CC} = 5 V,	I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		$V_{IH} = V_{IH}$min, I_{OH} = −800 μA,	$V_{IL} = V_{IL}$max, See Note 2	2.6			V
V_{OL}	Low-level output voltage		$V_{IH} = V_{IH}$min, I_{OL} = 16 mA,	$V_{IL} = V_{IL}$max, See Note 2			0.4	V
I_I	Input current at maximum input voltage	R	V_I = 7 V				5	mA
			V_I = 6 V,	V_{CC} = 0			5	
I_{IH}	High-level input current	A, B, or S	V_I = 4.5 V				40	μA
		R	V_I = 3.11 V				170	
I_{IL}	Low-level input current	A, B, or S	V_I = 0.4 V,	V_{IR} = 0.8 V	−0.1		−1.6	mA
I_{OS}	Short-circuit output current†				−50		−100	mA
I_{CC}	Supply current		All inputs = 0.8 V				72	mA
			All inputs = 2 V				100	

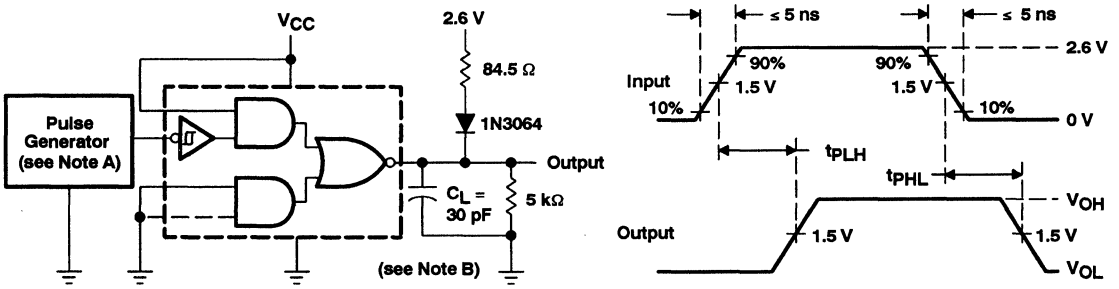
† Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 2: The output voltage and current limits are characterized for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \sim 50\ \Omega$, PRR ≤ 5 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
RECEIVER INPUT VOLTAGE

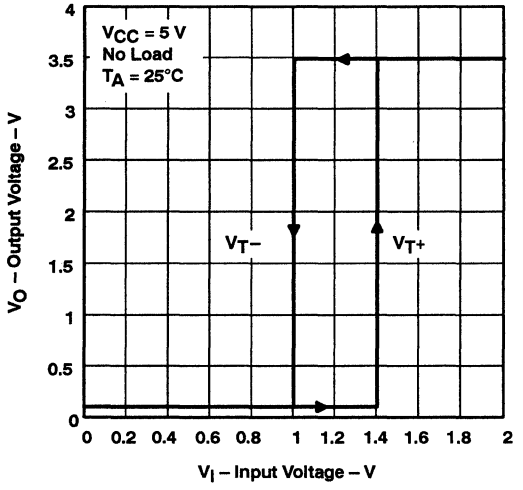


Figure 2

APPLICATION INFORMATION

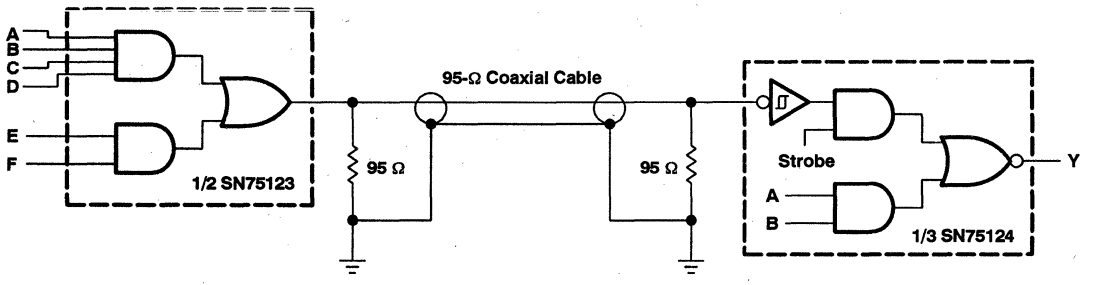


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

TEXAS INSTRUMENTS
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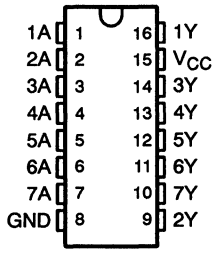
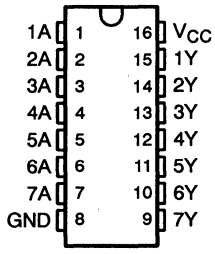
SLLS108A – D239, JANUARY 1977 – REVISED FEBRUARY 1993

- **Meets IBM 360/370 I/O Specification**
- **Input Resistance . . . 7 kΩ to 20 kΩ**
- **Output Compatible With TTL**
- **Schottky-Clamped Transistors**
- **Operates From Single 5-V Supply**
- **High Speed . . . Low Propagation Delay**
- **Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low**
- **Seven Channels in One 16-Pin Package**
- **Standard V_{CC} and Ground Positioning on SN75127**

SN75125 . . . D OR N PACKAGE
(TOP VIEW)



SN75127 . . . D OR N PACKAGE
(TOP VIEW)



THE SN75125 IS NOT RECOMMENDED FOR NEW DESIGN

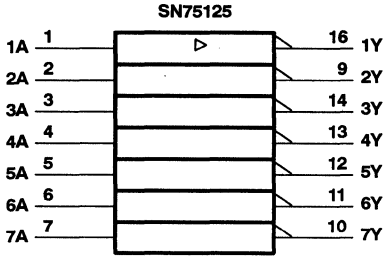
description

The SN75125 and SN75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky-clamped transistors allow for low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

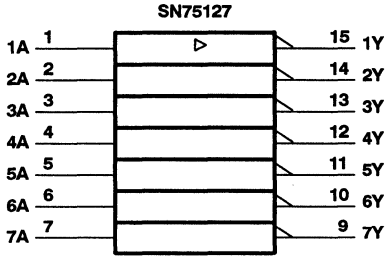
The SN75125 and SN75127 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75125

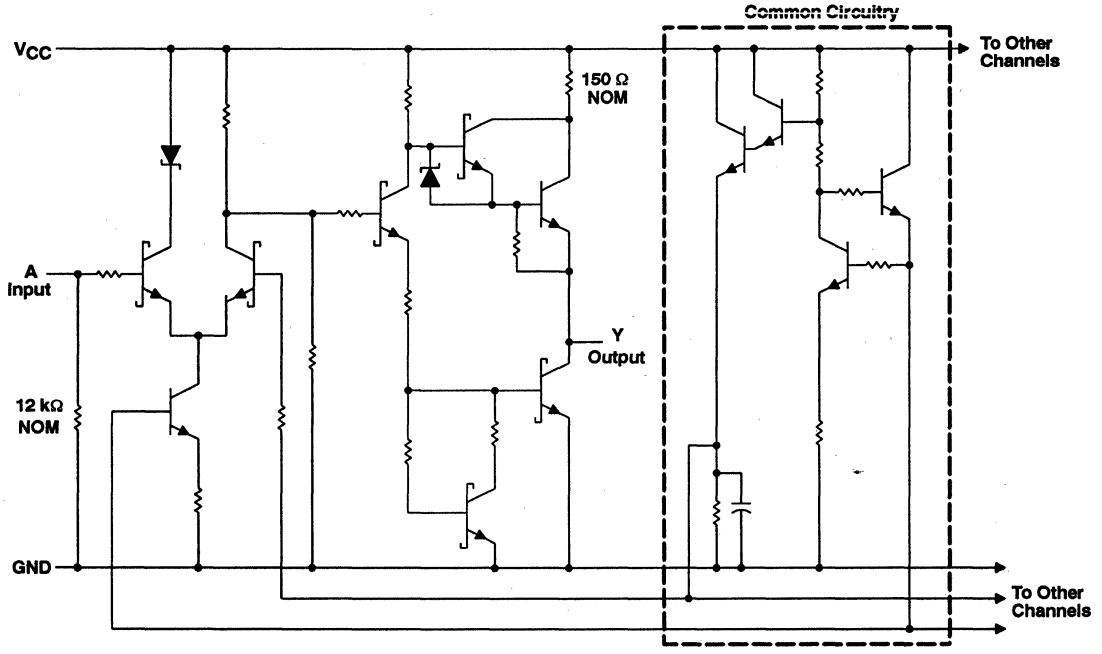


SN75127



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range: SN75125 ..... −0.15 V to 7 V
SN75127 ..... −2 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1050 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	1.7			V
Low-level input voltage, V_{IL}			0.7	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

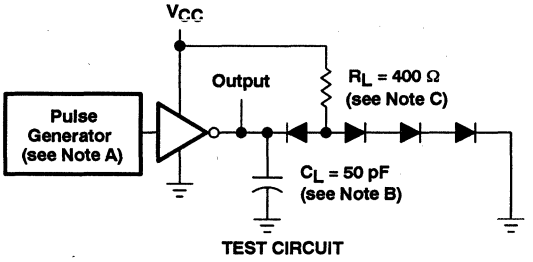
PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	V_{IL} = 0.7 V,	I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	V_{IH} = 1.7 V,	I_{OL} = 16 mA		0.4	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = 3.11 V			0.3	0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0.15 V				30	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.5 V,	V_O = 0		−18		−60	mA
r_i	Input resistance	V_{CC} = 4.5 V, 0 V, or open,		ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V,	I_{OH} = −0.4 mA,	All inputs at 0.7 V		15	25	mA
		V_{CC} = 5.5 V,	I_{OL} = 16 mA,	All inputs at 4 V		28	47	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

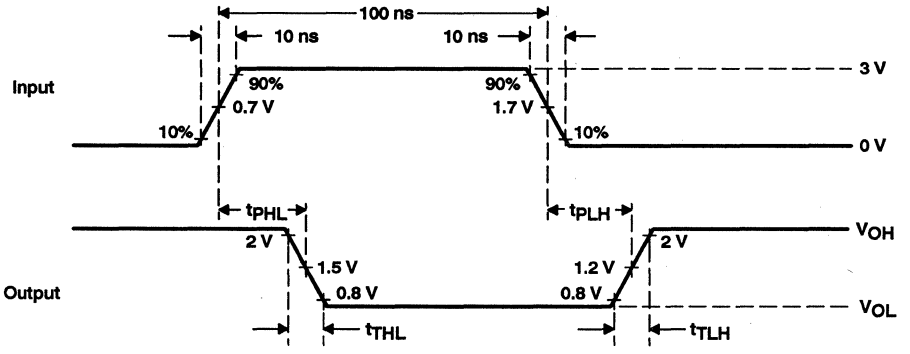
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times		0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output		1	7	12	ns
t_{THL}	Transition time, high-to-low-level output		1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \sim 50\ \Omega$, PRR ≤ 5 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 1. Tests Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

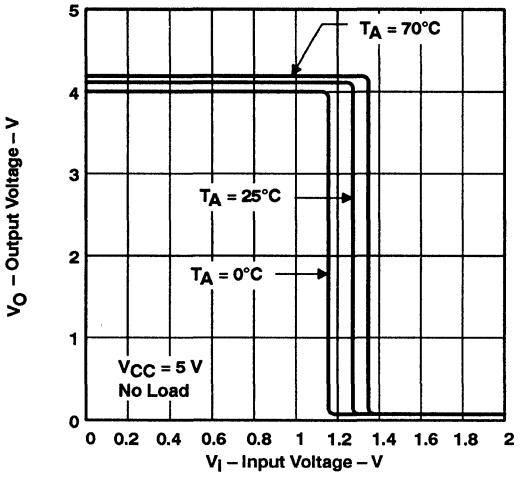


Figure 2

VOLTAGE TRANSFER CHARACTERISTICS

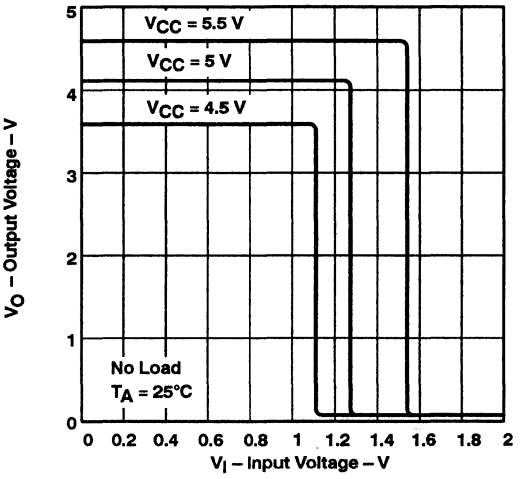


Figure 3

INPUT CURRENT
vs
INPUT VOLTAGE

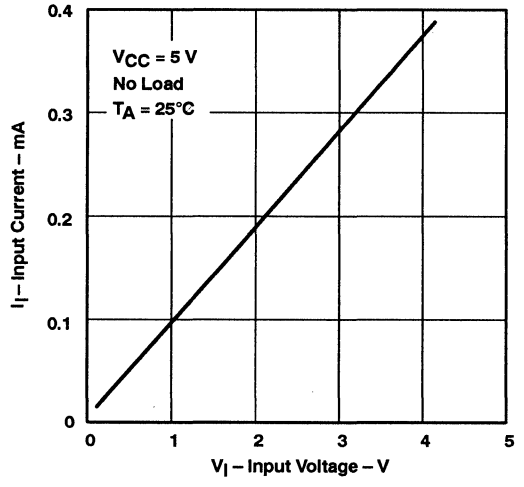


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

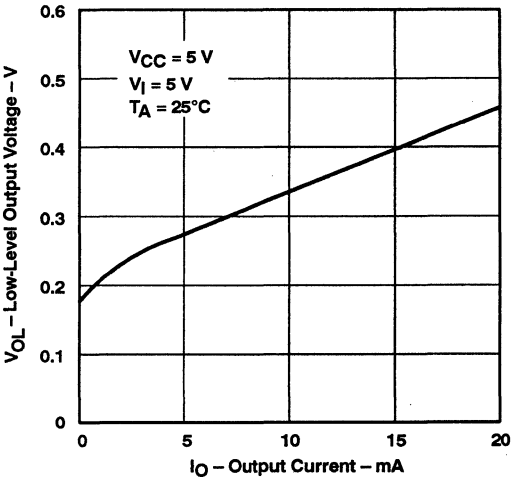


Figure 5

TYPICAL CHARACTERISTICS

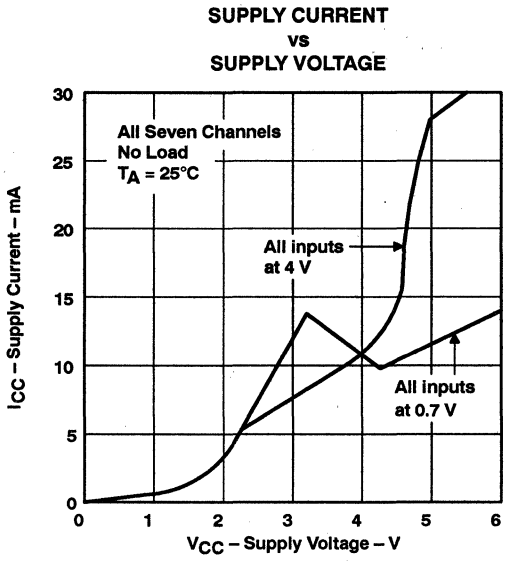
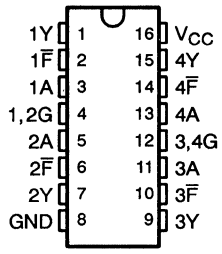


Figure 6

SLLS060A – D3405, FEBRUARY 1990 – REVISED FEBRUARY 1993

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN55ALS126 and SN75ALS126)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −59.3 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Dual Common Enable**
- **Individual Fault Flags**
- **Designed to Replace the MC3481**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS	
G	A	Y	F̄
L	X	L	H
H	H	H	H
H	H	S	L

H = high level,
L = low level,
X = irrelevant,
S = shorted to ground

description

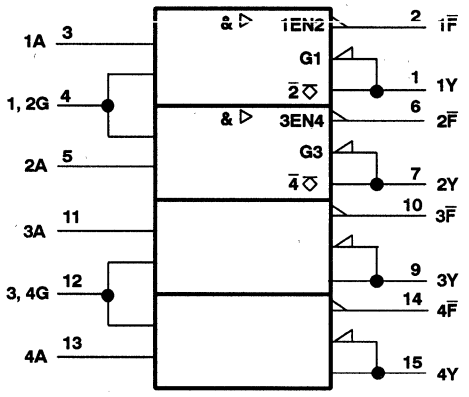
The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specification A22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75126 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75126 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

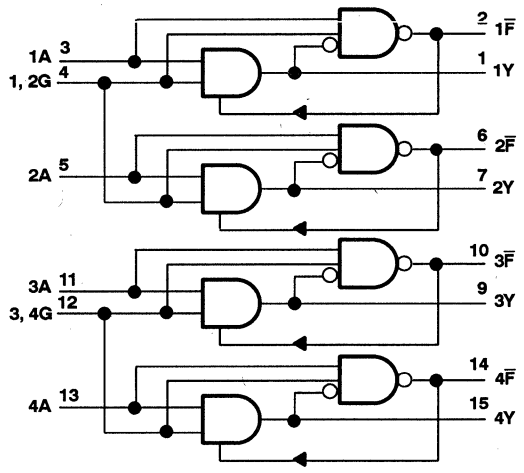
The SN75126 is characterized for operation from 0°C to 70°C.

logic symbol†

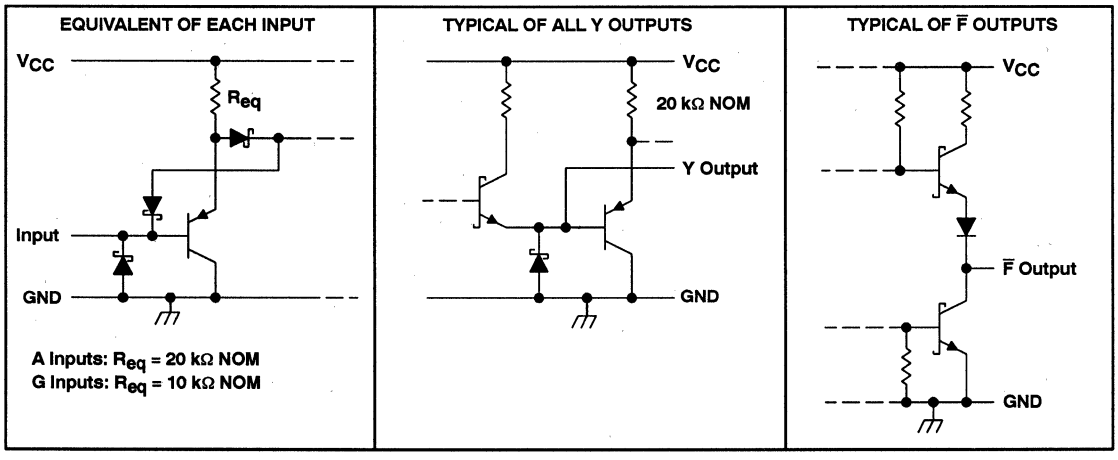


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

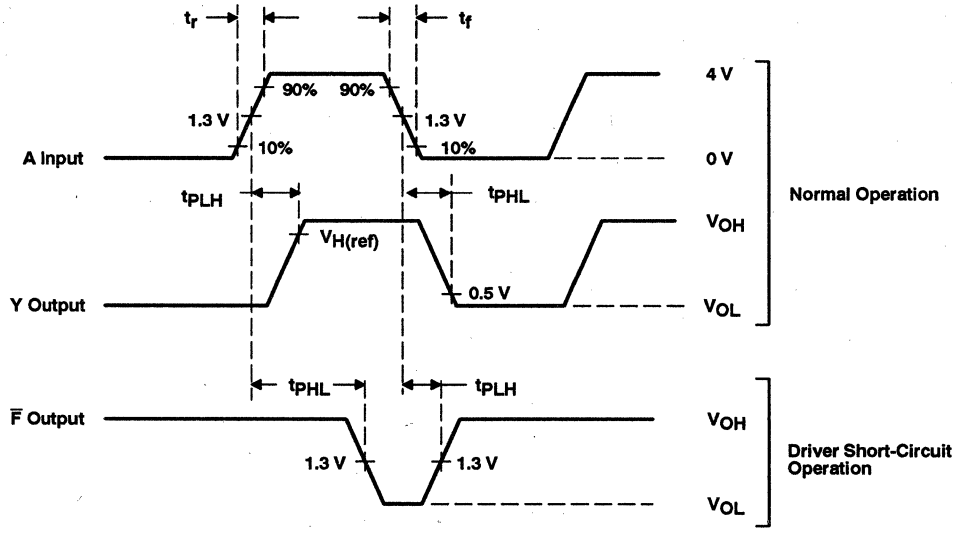
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = −59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = −41 mA,	V_{IH} = 2 V	3.9		
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OH} = −400 μA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = −240 μA,	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = −1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, V_{IH} = 2 V	I_{OL} = 8 mA,	Y at 0 V,		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_I = 0,	V_O = 3.11 V		100	μA
		Y	V_{CC} = 0,	V_I = 0,	*V_O = 3.11 V		200	
I_I	Input current	A	V_{CC} = 4.5 V,	V_I = 5.5 V			100	μA
		G					200	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_I = 2.7 V			20	μA
		G					40	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_I = 0.4 V			−250	μA
		G					−500	
I_{OS}	Short-circuit output current	Y	V_{CC} = 5.5 V,	V_O = 0,	V_{IH} = 2.7 V		−5	mA
		$\overline{F}$	V_{CC} = 5.5 V,	V_O = 0		−15	−100	
		Y	V_{CC} = 5.95 V,	V_O = 0,	V_{IH} = 2.7 V		−5	
		$\overline{F}$	V_{CC} = 5.95 V,	V_O = 0		−15	−110	
$I_{CC(H)}$	Supply current, all outputs high		V_{CC} = 5.5 V,	No load,	V_{IH} = 2 V		70	mA
			V_{CC} = 5.95 V,	No load,	V_{IH} = 2 V		80	
$I_{CC(L)}$	Supply current, Y outputs low		V_{CC} = 5.5 V,	No load,	V_{IL} = 0.8 V		55	mA
			V_{CC} = 5.95 V,	No load,	V_{IL} = 0.8 V		70	

switching characteristics at T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.11 V, See Figures 1 and 2		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					37	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{H(ref)}$ = 3.9 V, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output					45	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2		60	ns
t_{PHL}	Propagation delay time, high-to-low-level output					100	ns

PARAMETER MEASUREMENT INFORMATION



NOTE: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O ≈ 50 Ω.

Figure 1. Input and Output Voltage Waveforms

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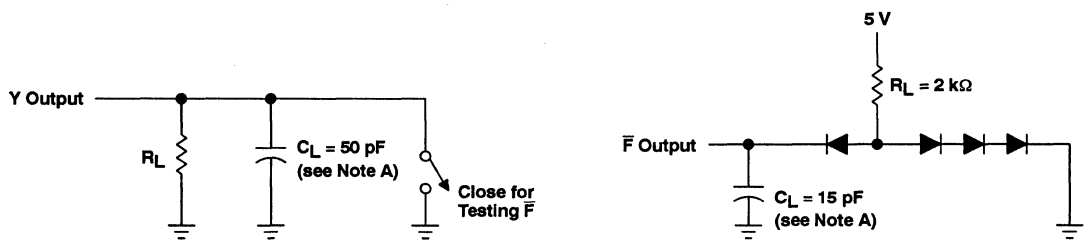
PARAMETER MEASUREMENT INFORMATION

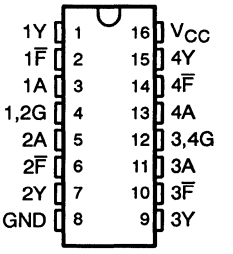


NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75ALS130)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = –60 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Advanced Low-Power Schottky Circuitry**
- **Dual Common Enable**
- **Individual Fault Flags**
- **Designed to Be an Improved Replacement for the MC3481**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS	
G	A	Y	F̄
L	X	L	H
H	H	H	H
H	H	S	L

H = high level, L = low level,
X = irrelevant,
S = shorted to GND

description

The SN75ALS126 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = – 59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75ALS126 is compatible with standard TTL logic and supply voltages

The SN75ALS126 employs the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75ALS126 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75127, SN75128, or SN75129 line receivers.

The SN75ALS126 is characterized for operation from 0°C to 70°C.

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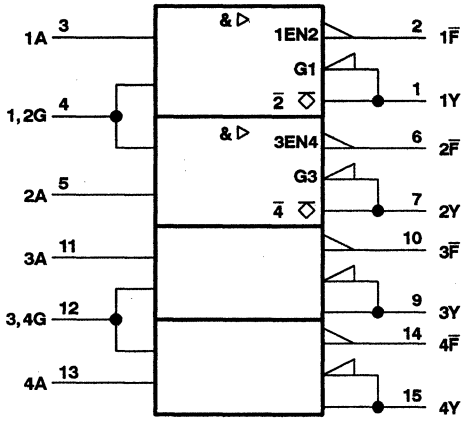
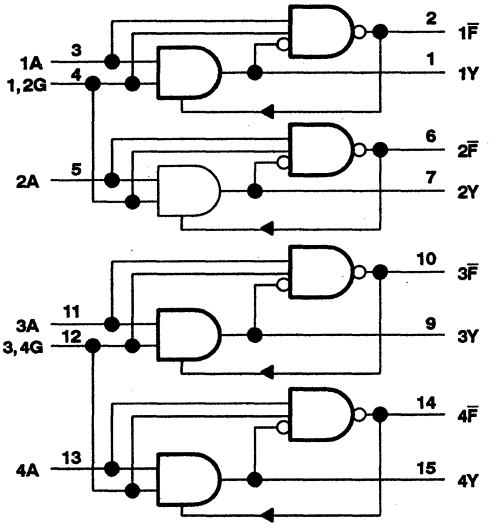
logic symbol†

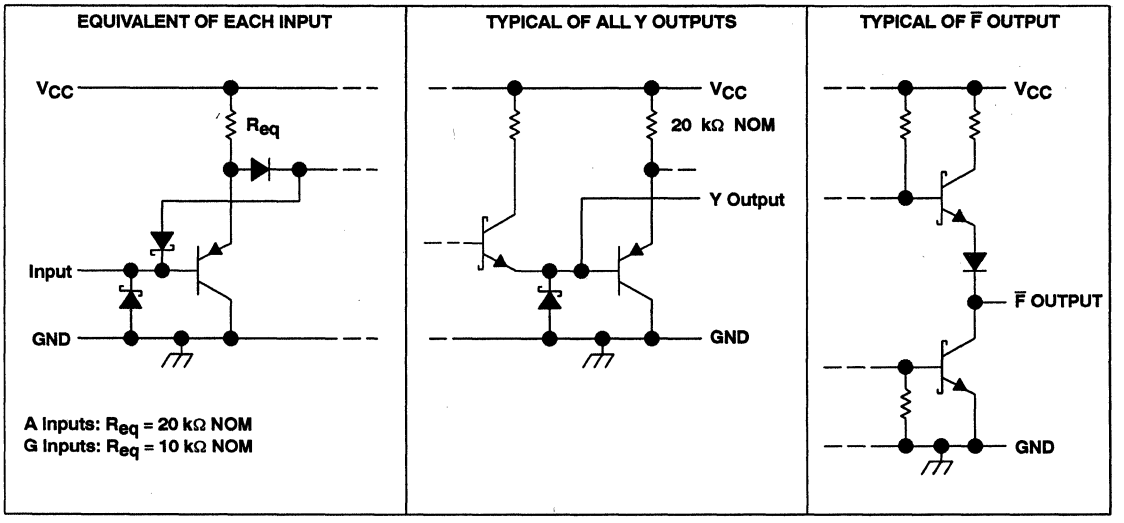


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 59.3	mA
Operating free-air temperature, T_A	0		70	°C

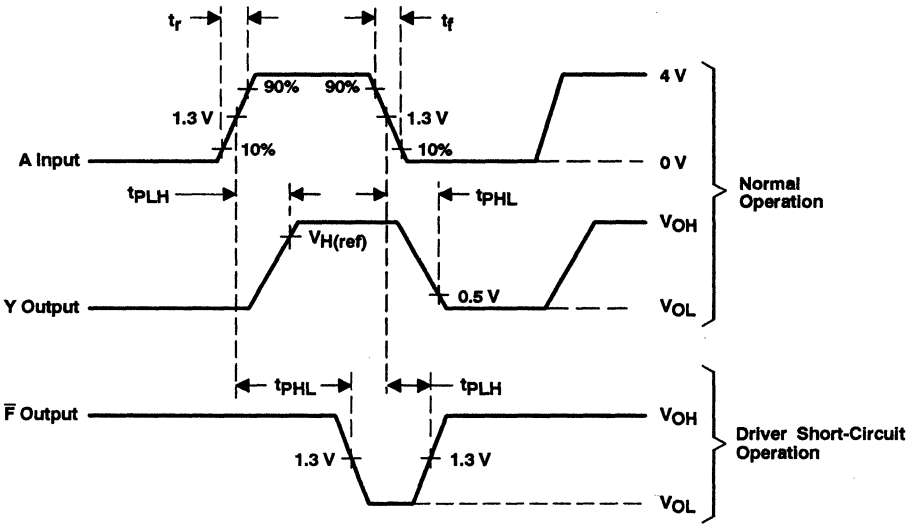
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = – 59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = – 41 mA,	V_{IH} = 2 V	3.9		
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OH} = – 400 μA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = – 240 μA	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = – 1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OL} = 8 mA,	Y at 0 V		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_{IL} = 0,	V_O = 3.11 V		100	μA
		Y	V_{CC} = 0 V,	V_{IL} = 0,	V_O = 3.11 V		200	
I_I	Input current	A	V_{CC} = 4.5 V,	V_I = 5.5 V			100	μA
		G					400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_I = 2.7 V			20	μA
		G					80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_I = 0.4 V			– 250	μA
		G					–1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V,	V_O = 0,	V_{IH} = 2.7 V		–5	mA
		$\overline{F}$	V_{CC} = 5.5 V,	V_O = 0		–15	–100	
		Y	V_{CC} = 5.95 V,	V_O = 0,	V_{IH} = 2.7 V		–5	
		$\overline{F}$	V_{CC} = 5.95 V,	V_O = 0		–15	–110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V,	No load,	V_{IH} = 2.7 V		25	mA
			V_{CC} = 5.95 V,	No load,	V_{IH} = 2.7 V		27	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V,	No load,	V_{IL} = 0.4 V		45	mA
			V_{CC} = 5.95 V,	No load,	V_{IL} = 0.4 V		47	

switching characteristics over recommended operating free-air temperature range

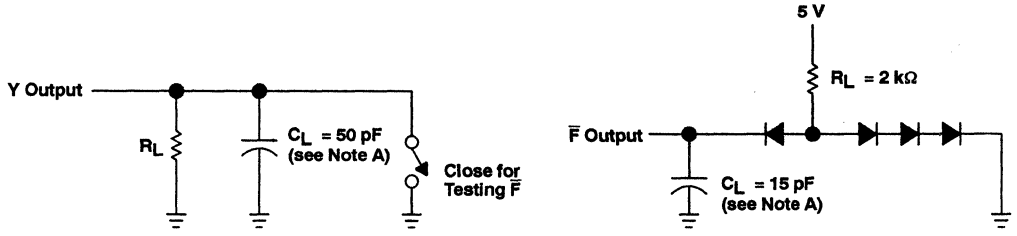
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, See Figures 1 and 2	C_L = 50 pF, $V_{H(ref)}$ = 3.11 V,		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output						28	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times					0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, See Figures 1 and 2	C_L = 50 pF, $V_{H(ref)}$ = 3.9 V,		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output						34	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						75	ns

PARAMETER MEASUREMENT INFORMATION



NOTE: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O ≈ 50 Ω.

Figure 1. Input and Output Voltage Waveforms



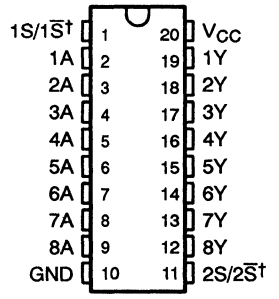
NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits

SLLS076A – D2305, JANUARY 1977 – REVISED MARCH 1993

- **Meets IBM 360/370 I/O Specification**
- **Input Resistance . . . 7 kΩ to 20 kΩ**
- **Output Compatible With TTL**
- **Schottky-Clamped Transistors**
- **Operates From a Single 5-V Supply**
- **High Speed . . . Low Propagation Delay**
- **Ratio Specification . . . t_{PLH} /t_{PHL}**
- **Common Strobe for Each Group of Four Receivers**
- **SN75128 . . . Active-High Strobes**
  SN75129 . . . Active-Low Strobes

N PACKAGE
(TOP VIEW)



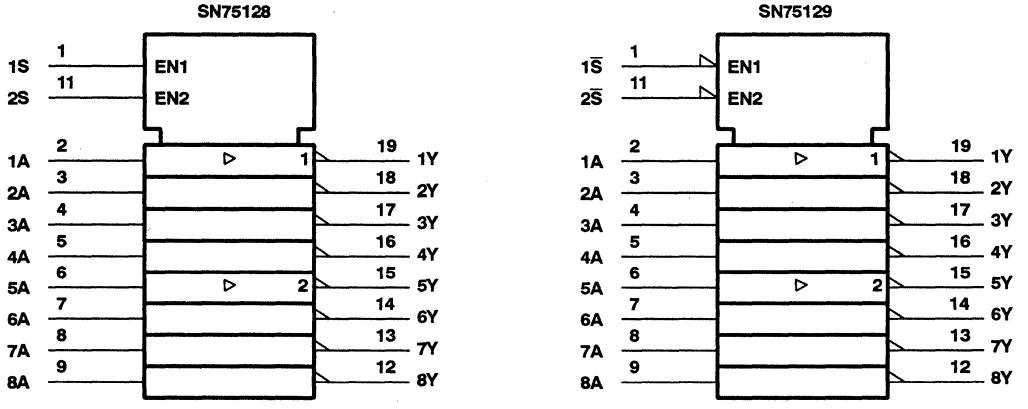
† S and S̄ for SN75128 and SN75129, respectively

description

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four devices. The SN75128 has active-high strobes; the SN75129 has active-low strobes. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

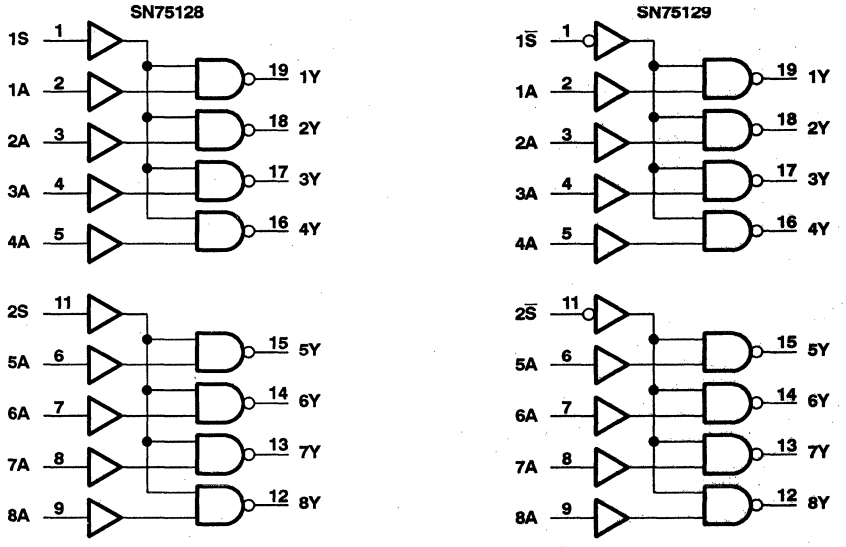
The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

logic symbols†

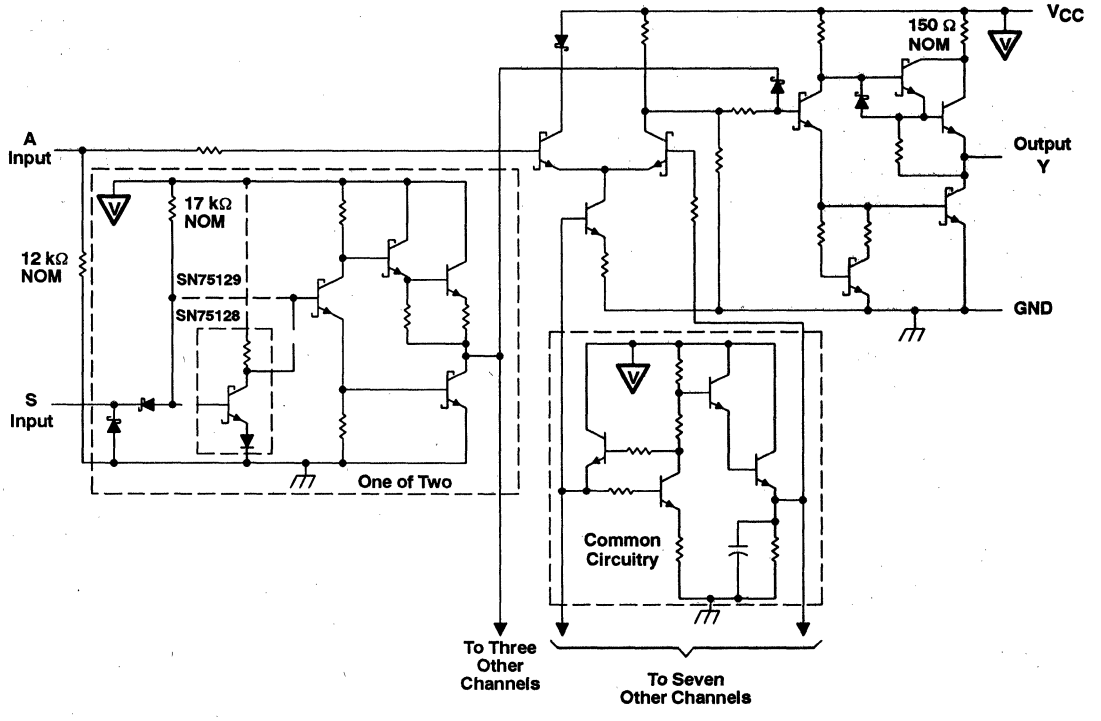


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, A, V_I ..... −0.15 V to 7 V
Input voltage, S, V_I ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	A	1.7			V
	S	2			
Low-level input voltage, V_{IL}	A			0.7	V
	S			0.7	
High-level output current, I_{OH}				−0.4	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

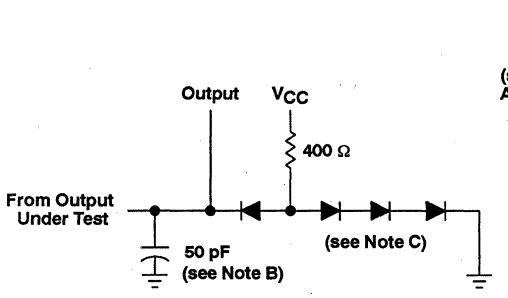
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	V_{IL} = 0.7 V,	I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	V_{IH} = 1.7 V,	I_{OL} = 16 mA		0.4	0.5	V
V_{IK}	Input clamp voltage	S	V_{CC} = 4.5 V,	I_I = −18 mA				−1.5	V
I_{IH}	High-level input current	A	V_{CC} = 5.5 V,	V_I = 3.11 V			0.3	0.42	mA
		S	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	A	V_{CC} = 5.5 V,	V_I = 0.15 V				30	μA
		S	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.4	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V,	V_O = 0		−18		−60	mA
r_i	Input resistance		V_{CC} = 4.5 V,	0 V or open,	ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	SN75128	V_{CC} = 5.5 V,	Strobe at 2.4 V,	All A inputs at 0.7 V		19	31	mA
		SN75129	V_{CC} = 5.5 V,	Strobe at 0.4 V,	All A inputs at 0.7 V		19	31	
		SN75128	V_{CC} = 5.5 V,	Strobe at 2.4 V,	All A inputs at 4 V		32	53	
		SN75129	V_{CC} = 5.5 V,	Strobe at 0.4 V,	All A inputs at 4 V		32	53	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

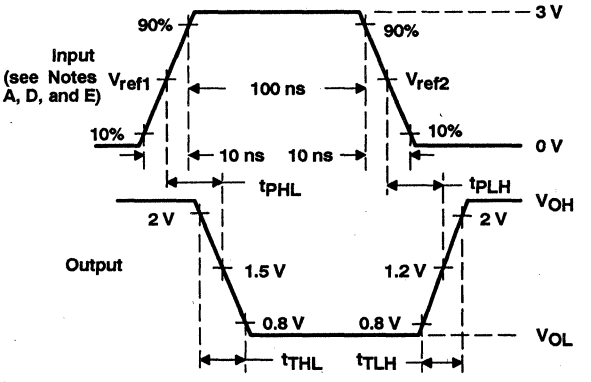
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	S			26	40		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output			1	7	12	1	7	12	ns
t_{THL}	Transition time, high-to-low-level output			1	3	12	1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR ≤ 5 MHz.
B. Includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. The strobe inputs of SN75129 are in phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

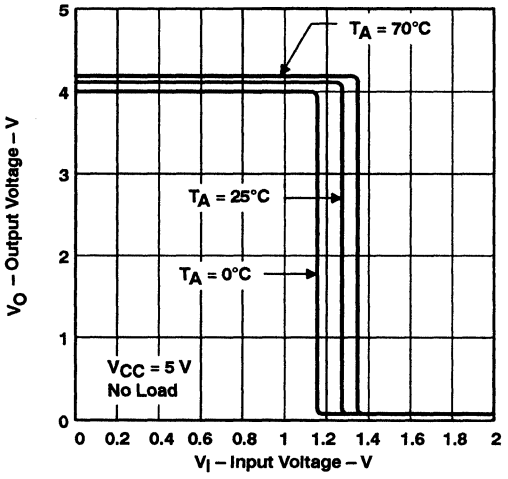


Figure 2

VOLTAGE TRANSFER CHARACTERISTICS
FROM A INPUTS

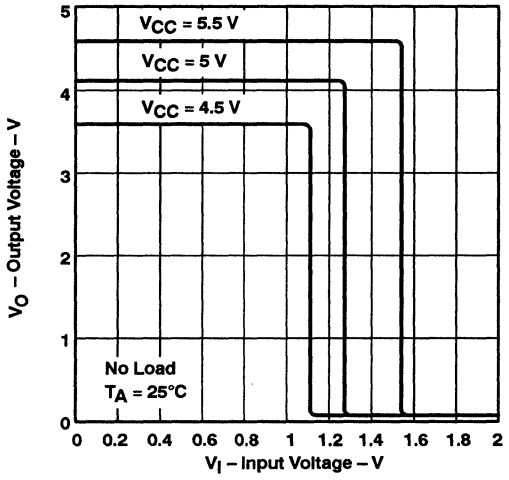


Figure 3

INPUT CURRENT
vs
INPUT VOLTAGE

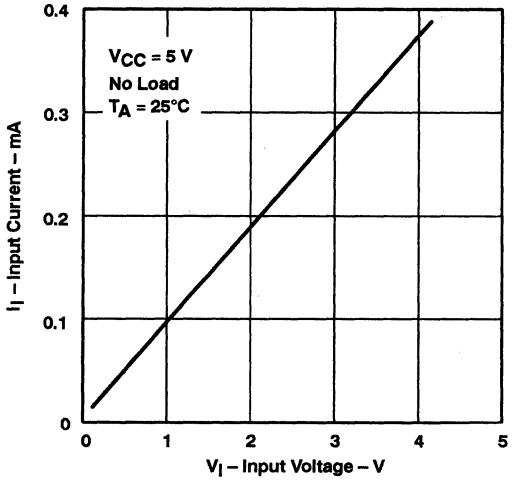


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

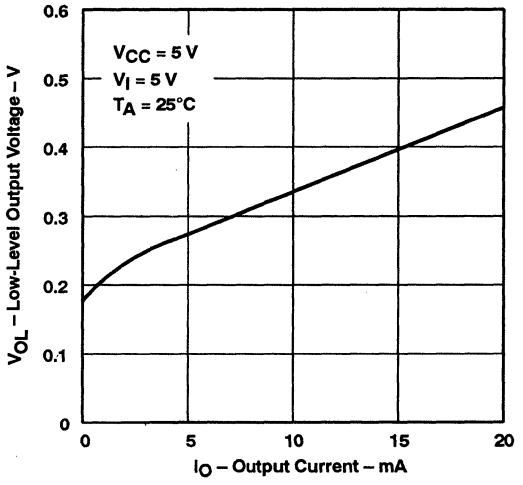
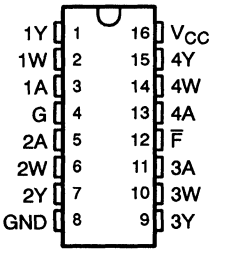


Figure 5

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75ALS130)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −59.3 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Common Enable and Common Fault Flag**
- **Designed to Be an Improved Replacement for the MC3485**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS		
G†	A	Y	F	W
L	X	L	H	H
X	L	L	H	H
H	H	H	H	L
H	H	S	L	H

H = high level, L = low level, X = irrelevant,
S = shorted to ground

† G and F are common to the four drivers. If any of the four Y outputs is shorted, the fault flag will respond.

description

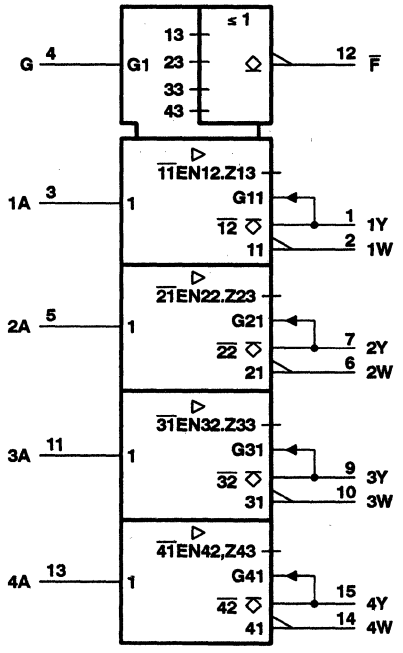
The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.5 V) and temperature (0°C to 70°C). Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75130 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into the off (low) state and signals a fault condition by causing the fault-flag output to go low.

The SN75130 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

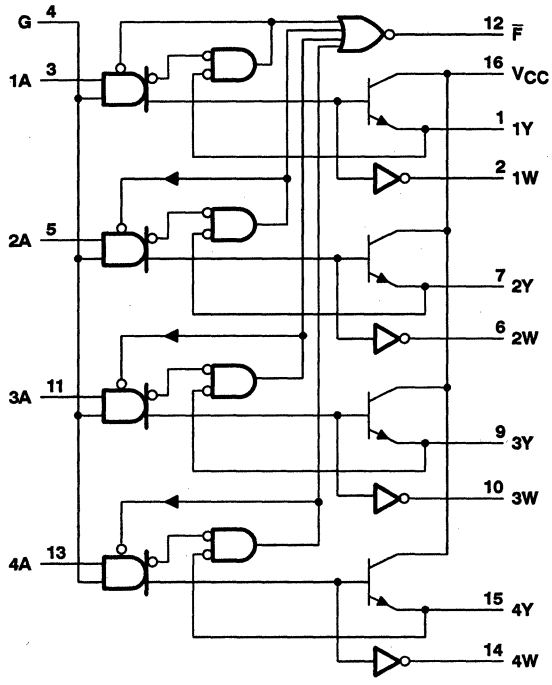
The SN75130 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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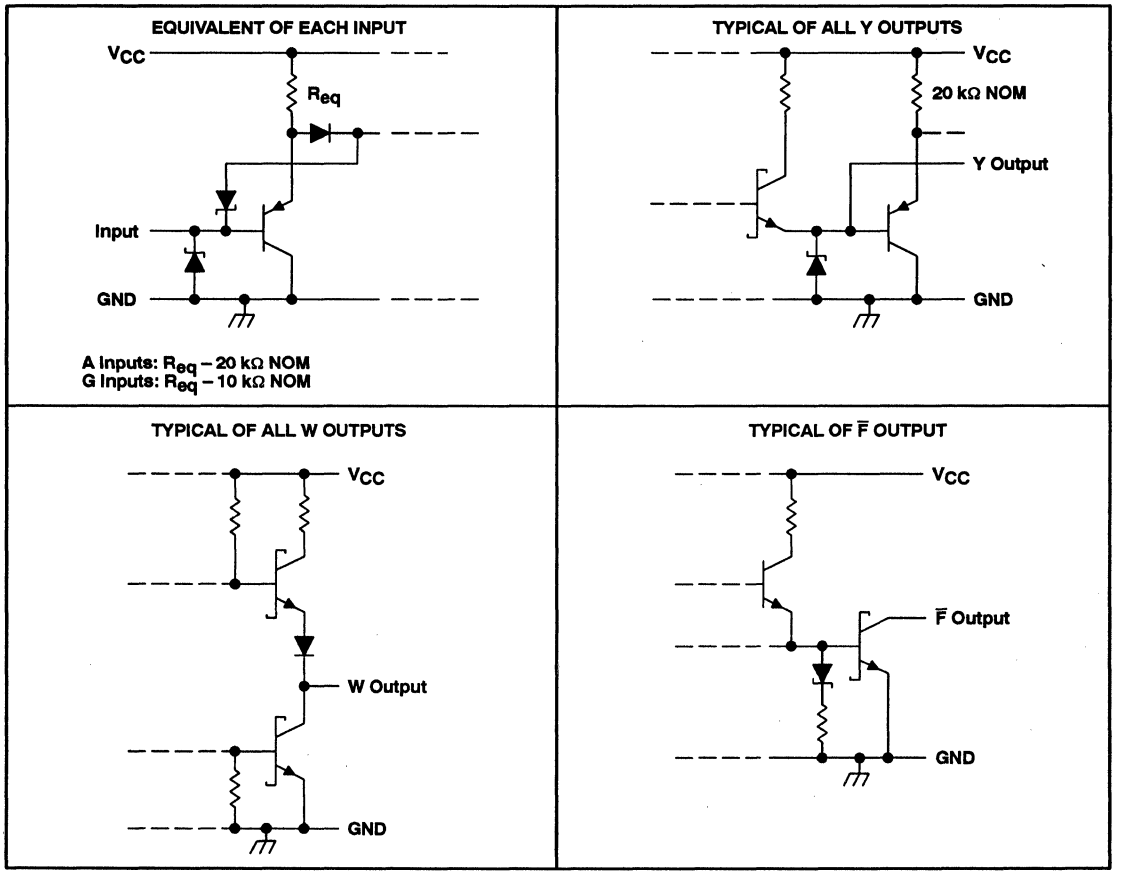
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

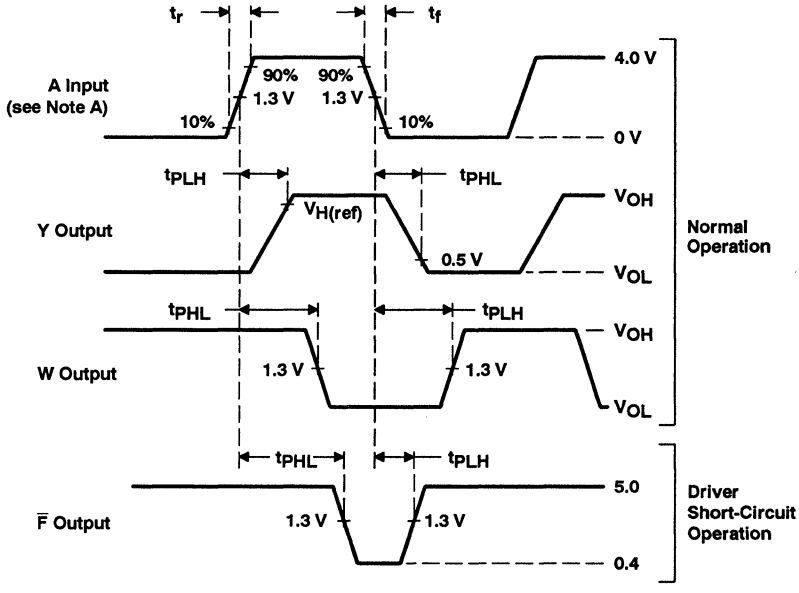
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = −59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = −41 mA,	V_{IH} = 2 V	3.9		
		W	V_{CC} = 4.5 V,	I_{OH} = −400 μA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = −240 μA,	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = −1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OL} = 8 mA,	Y at 0 V		0.5	
		W	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_{IL} = 0,	V_O = 3.11 V		100	μA
		Y	V_{CC} = 0,	V_{IL} = 0,	V_O = 3.11 V		200	
I_{OH}	High-level output current	$\overline{F}$	V_{CC} = 5.95 V,	V_{OH} = 5.95 V			100	μA
I_I	Input current	A	V_{CC} = 4.5 V,	V_{IH} = 5.5 V			100	μA
		G					400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_{IH} = 2.7 V			20	μA
		G					80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_{IL} = 0.4 V			250	μA
		G					−1000	
I_{OS}	Short-circuit output	Y	V_{CC} = 5.5 V,	V_O = 0			−5	mA
		W				−15	−100	
		Y	V_{CC} = 5.95 V,	V_O = 0			−5	
		W				−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V,	V_I = 2 V			75	mA
			V_{CC} = 5.95 V,	V_I = 2 V			85	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V,	V_I = 0.8 V			55	mA
			V_{CC} = 5.95 V,	V_I = 0.8 V			70	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, Input f = 1 MHz,	$V_{H(ref)}$ = 3.11 V, R_L = 50 Ω, See Figures 1 and 2		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output						37	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times					0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.59 V, C_L = 50 pF, Input f = 5 MHz,	$V_{H(ref)}$ = 3.9 V, R_L = 90 Ω, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						45	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	W	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						28	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		60	ns
t_{PHL}	Propagation delay time, high-to-low-level output						100	ns

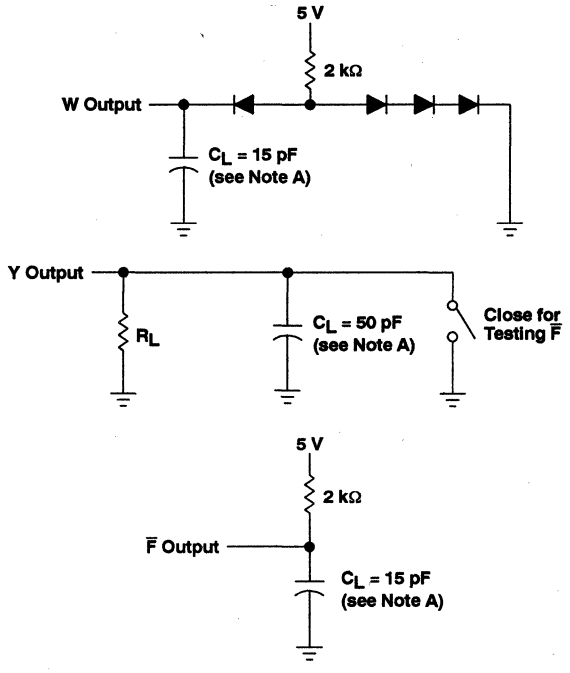
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.

Figure 1. Input and Output Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



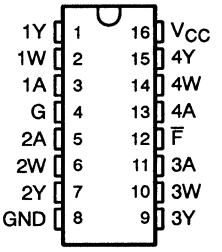
NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits

SLLS024B – D2299, FEBRUARY 1986 – REVISED FEBRUARY 1993

- **Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75ALS126)**
- **Minimum Output Voltage of 3.11 V at I_{OH} = – 60 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Advanced Low-Power Schottky Circuitry**
- **Common Enable and Common Fault Flag**
- **Designed to Be an Improved Replacement for the MC3485**

D OR N PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGN

description

The SN75ALS130 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = – 59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75ALS130 is compatible with standard TTL logic and supply voltages.

FUNCTION TABLE

INPUTS		OUTPUTS		
G†	A	Y	F†	W
L	X	L	H	H
X	L	L	H	H
H	H	H	H	L
H	H	S	L	H

H = high level, L = low level,
X = irrelevant, S = shorted to ground
† G and F are common to the four drivers. If any of the four Y outputs is shorted, the fault flag will respond.

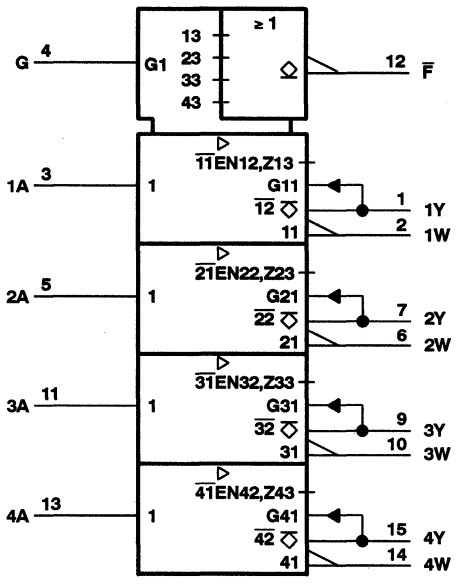
The SN75ALS130 employs the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75ALS130 can drive a 50-Ω load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the devices are used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75ALS130 is characterized for operation from 0°C to 70°C.

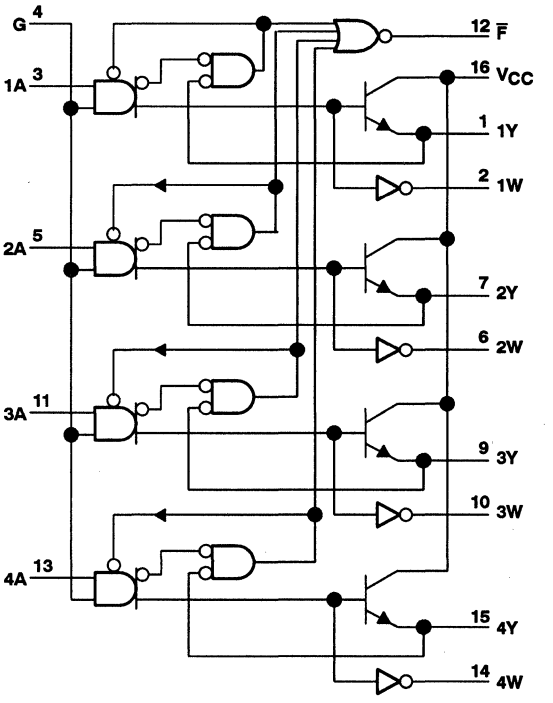
IMPACT is a trademark of Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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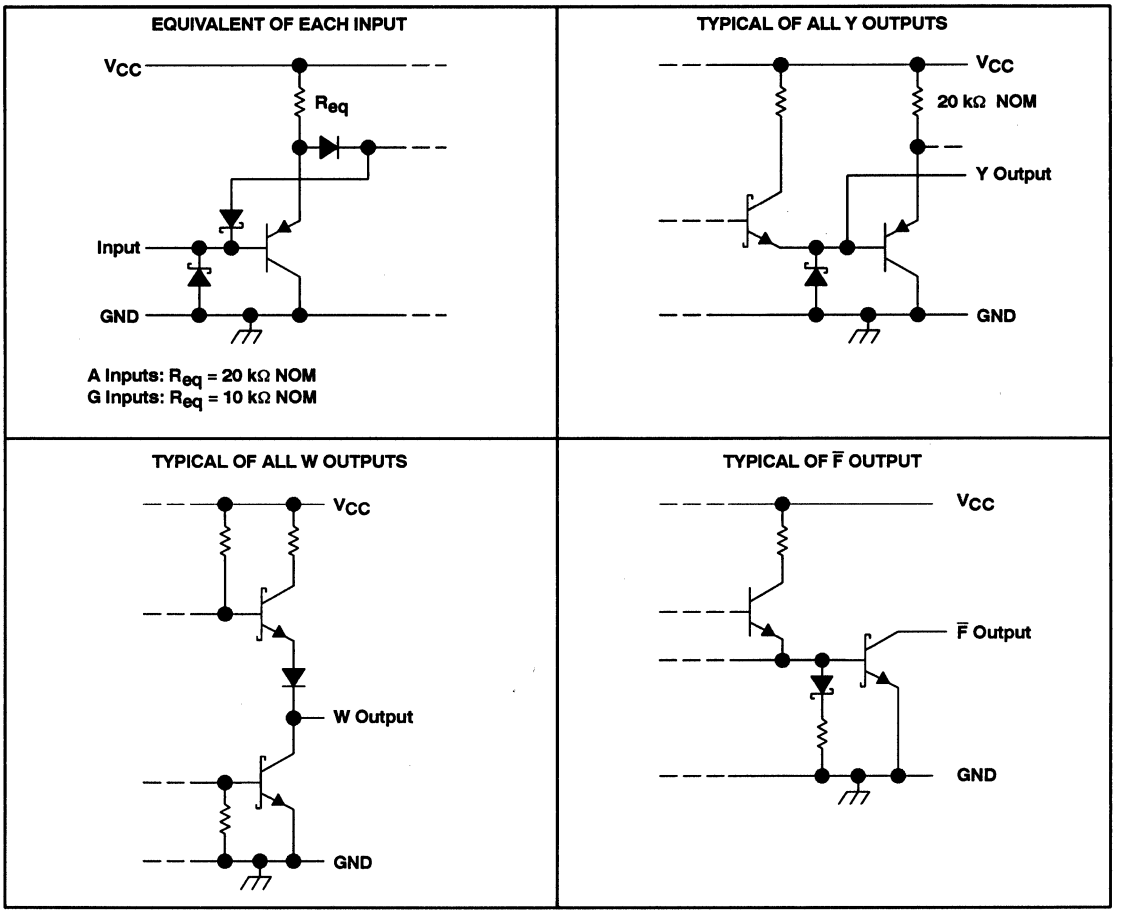
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 59.3	mA
Operating free-air temperature, T_A	0		70	°C

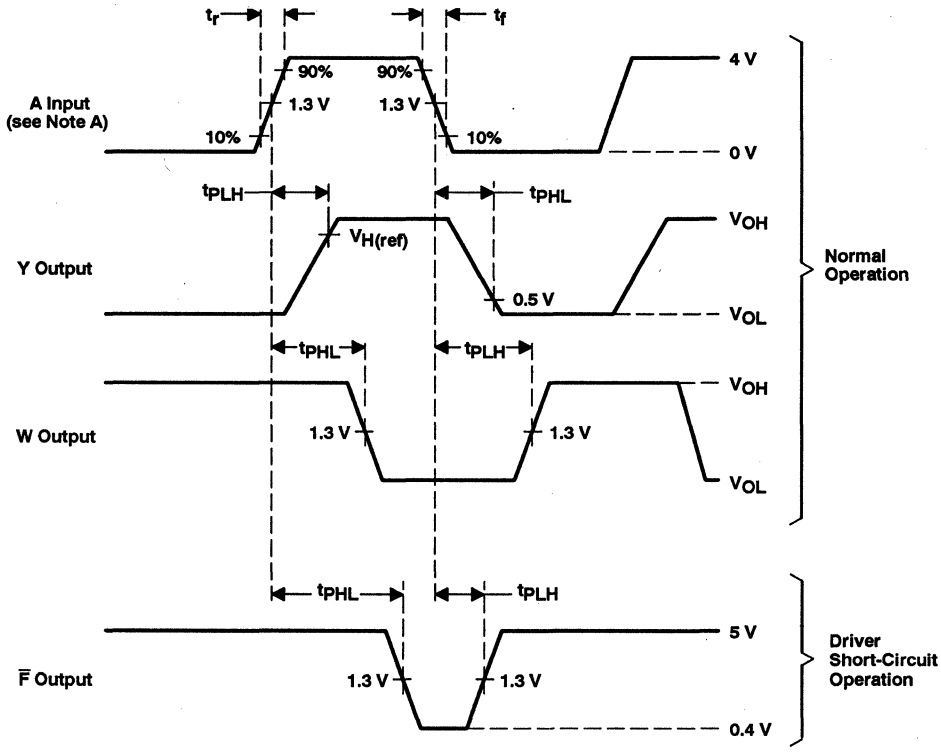
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V,	I_I = – 18 mA			–1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = – 59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = – 41 mA,	V_{IH} = 2 V	3.9		
		W	V_{CC} = 4.5 V,	I_{OH} = – 400 µA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = – 240 µA	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = –1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OL} = 8 mA,	Y at 0 V		0.5	
		W	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_{IL} = 0,	V_O = 3.11 V		100	µA
		Y	V_{CC} = 0,	V_{IL} = 0,	V_O = 3.11 V		200	
I_{OH}	High-level output current	$\overline{F}$	V_{CC} = 5.95 V,	V_{OH} = 5.95 V			100	µA
I_I	Input current	A	V_{CC} = 4.5 V,	V_{IH} = 5.5 V			100	µA
		G					400	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_{IH} = 2.7 V			20	µA
		G					80	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_{IL} = 0.4 V			250	µA
		G					–1000	
I_{OS}	Short-circuit output current	Y	V_{CC} = 5.5 V,	V_O = 0,	V_{IH} = 2.7 V		– 5	mA
		W	V_{CC} = 5.5 V,	V_O = 0		–15	–100	
		Y	V_{CC} = 5.95 V,	V_O = 0,	V_{IH} = 2.7 V		– 5	
		W	V_{CC} = 5.95 V,	V_O = 0		–15	–110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V,	No load,	V_{IH} = 2.7 V		30	mA
			V_{CC} = 5.95 V,	No load,	V_{IH} = 2.7 V		32	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V,	No load,	V_{IL} = 0.4 V		45	mA
			V_{CC} = 5.95 V,	No load,	V_{IL} = 0.4 V		47	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, Input f = 1 MHz,	R_L = 50 Ω, $V_{H(ref)}$ = 3.11 V, See Figures 1 and 2		30	ns
t_{PHL}	Propagation delay time, high-to-low-level output						28	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times					0.3	3	
t_{PLH}	Propagation delay time, low-to-high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, C_L = 50 pF, Input f = 5 MHz,	R_L = 90 Ω, $V_{H(ref)}$ = 3.9 V, See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output						34	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	W	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		34	ns
t_{PHL}	Propagation delay time, high-to-low-level output						21	ns
t_{PLH}	Propagation delay time, low-to-high-level output	A	$\overline{F}$	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						75	ns

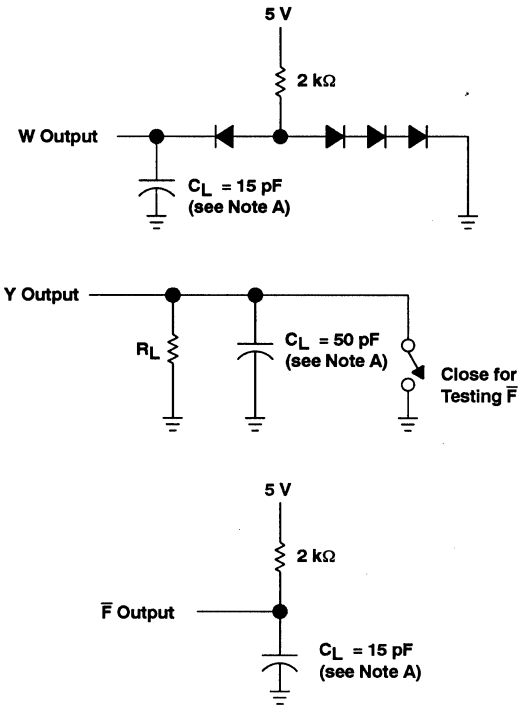
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O ~ 50 Ω.

Figure 1. Input and Output Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

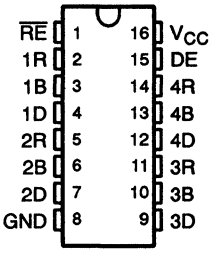


NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits

- **PNP Inputs for Minimal Input Loading (200 μA Maximum)**
- **High-Speed Schottky Circuitry**
- **3-State Outputs for Driver and Receiver**
- **Party-Line (Data-Bus) Operation**
- **Single 5-V Supply**
- **Driver Has 40-mA Current Sink Capability**
- **Designed to Be Functionally Interchangeable With Signetics N8T26, Also Called 8T26**

D OR N PACKAGE
(TOP VIEW)



description

The SN75136 is a quad transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have 3-state outputs. With pnp inputs, the input loading is reduced to a maximum input current of 200 μA.

The SN75136 is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER

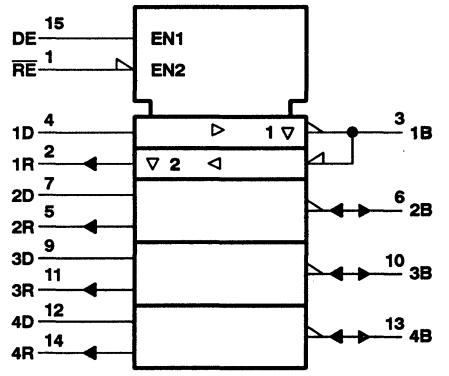
INPUTS		OUTPUT
D	DE	B
L	H	H
H	H	L
X	L	Z

RECEIVER

INPUTS		OUTPUT
B	$\overline{RE}$	R
L	L	H
H	L	L
X	H	Z

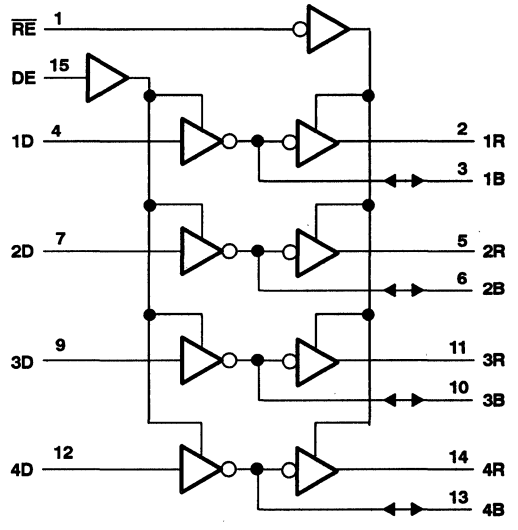
H = high level
L = low level
X = irrelevant
Z = high impedance

logic symbol†

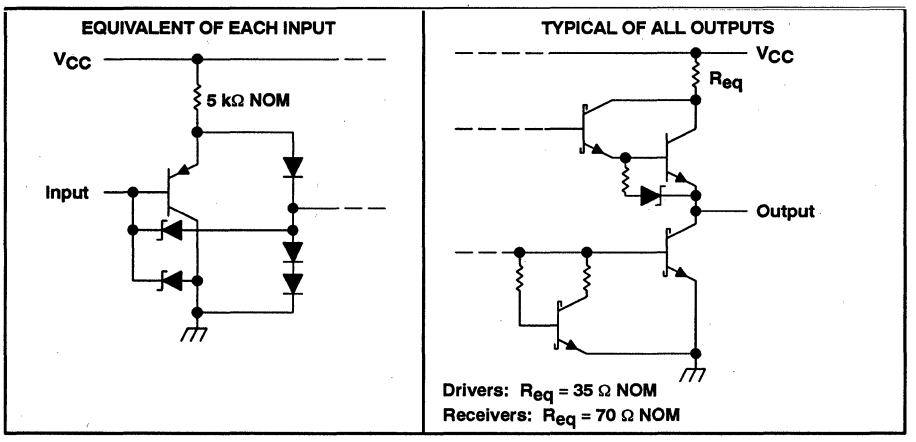


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	B, D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	B, D, DE, $\overline{RE}$			0.85	V
High-level output current, I_{OH}	Driver, B			–10	mA
	Receiver, R			–2	
Low-level output current, I_{OL}	Driver, B			40	mA
	Receiver, R			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	$I_I = -5$ mA					−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V,	V_{IL} = 0.85 V,	$I_{OH} = -10$ mA	2.6	3.1		V
		R	V_{IL} = 0.85 V,	$I_{OH} = -2$ mA		2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V,	I_{OL} = 40 mA				0.5	V
		R	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V,	$\overline{RE}$ at 2 V,	V_O = 2.6 V			100	μA
		R	$\overline{RE}$ at 2 V,	V_O = 0.5 V				−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V					25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V					−200	μA
I_{OS}	Short-circuit output current‡	B	V_{CC} = 5.25 V			−50		−150	mA
		R				−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V,	No load				87	mA

† All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡ Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	24	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		16	24	ns
t_{PZL}	Output enable time to low level					15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		9	24	ns
t_{PZL}	Output enable time to low level					31	38	

PARAMETER MEASUREMENT INFORMATION

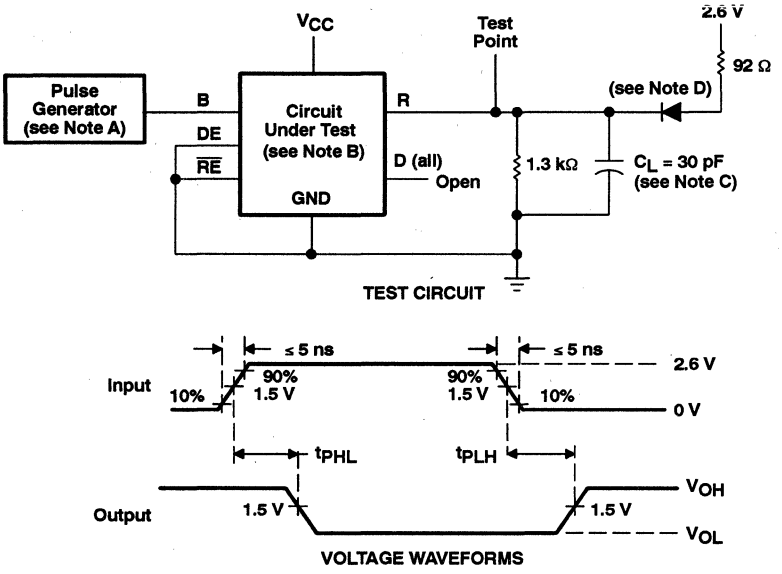


Figure 1. Propagation Delay Times From Bus to Receiver Output

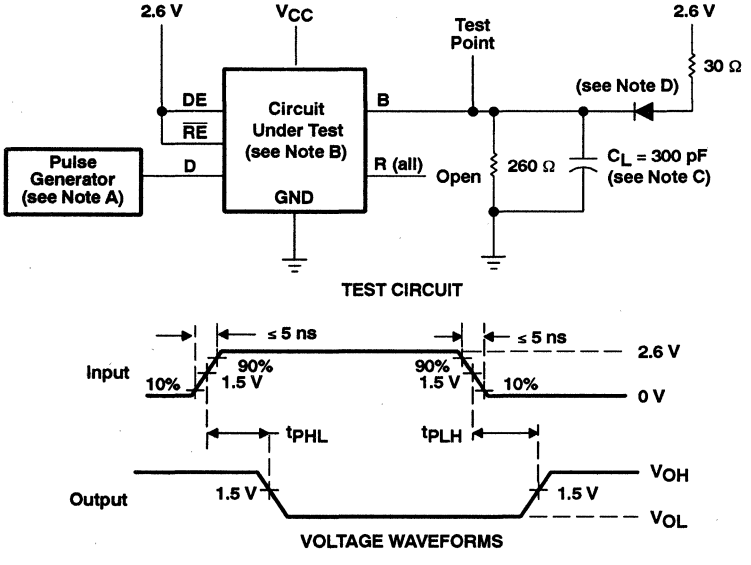


Figure 2. Propagation Delay Times From Driver Input to Bus

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR ≤ 10 MHz, duty cycle = 50%, Z_O ~ 50 Ω.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

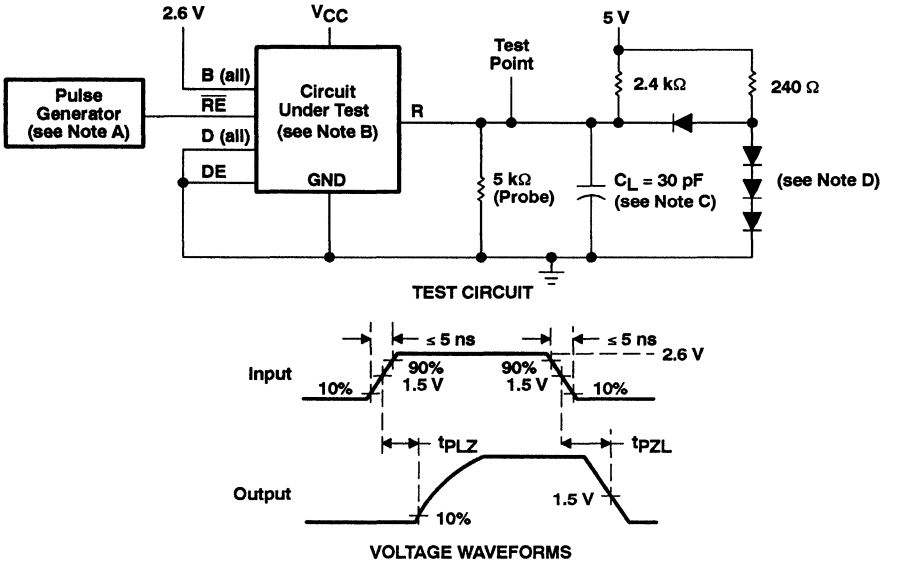


Figure 3. Receiver Test Circuit and Voltage Waveforms

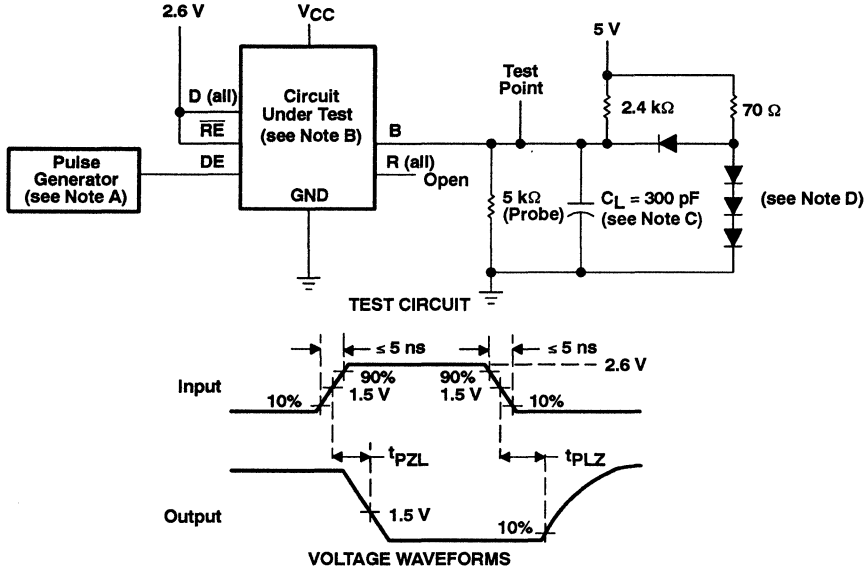


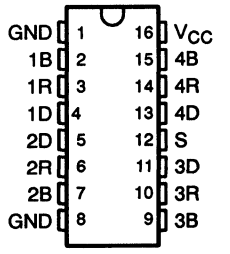
Figure 4. Driver Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR ≤ 5 MHz, duty cycle = 50%, $Z_O \sim 50\ \Omega$.
B. All inputs and outputs now shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

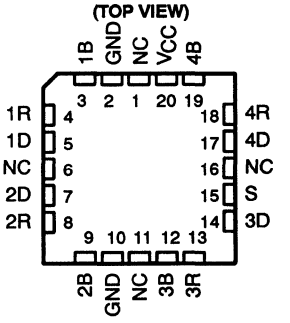
SLLS079A – D1663, SEPTEMBER 1973 – REVISED FEBRUARY 1993

- **Single 5-V Supply**
- **High-Input-Impedance, High-Threshold Receivers**
- **Common Driver Strobe**
- **TTL-Compatible Driver and Strobe Inputs With Clamp Diodes**
- **High-Speed Operation**
- **100-mA Open-Collector Driver Outputs**
- **Four Independent Channels**
- **TTL-Compatible Receiver Output**

SN55138 . . . J OR W PACKAGE
SN75138 . . . D OR N PACKAGE
(TOP VIEW)



SN55138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55138 and SN75138 quad bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver open-collector output is designed to handle loads of up to 100-mA open collector. The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

The receiver design also features a threshold of 2.3 V (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single 5-V supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero.

The SN55138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75138 is characterized for operation from 0°C to 70°C.

Function Tables

TRANSMITTING

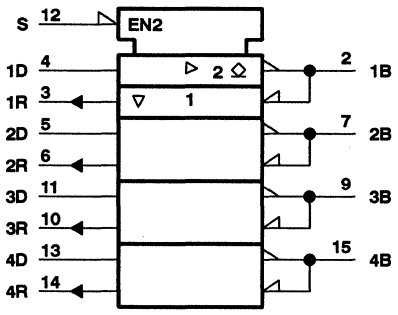
INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

RECEIVING

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

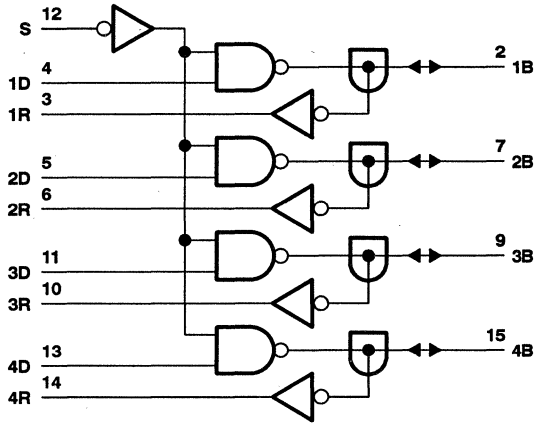
H = high level, L = low level, X = irrelevant

logic symbol†

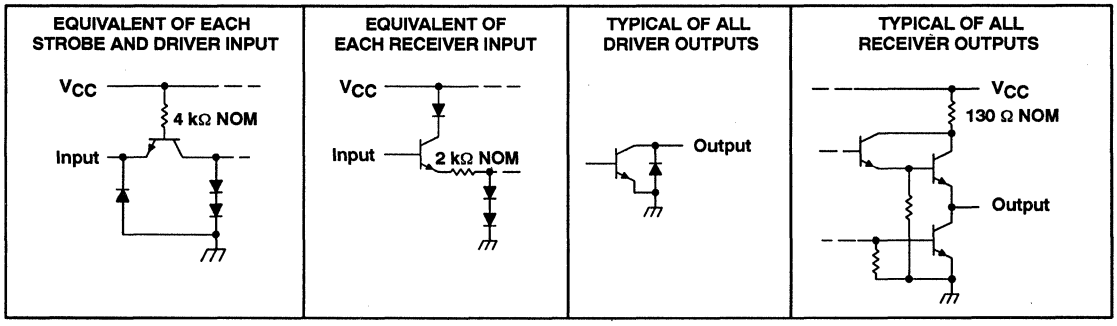


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55138	SN75138	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Driver off-state output voltage	7	7	V
Low-level output current into the driver output	150	150	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 125	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package		260	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

NOTE 1: All voltage values are with respect to both ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK and J packages, the SN55138 chip is alloy mounted.

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5		5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver or strobe	2			2			V
	Receiver	3.2			2.9			
Low-level input voltage, V_{IL}	Driver or strobe			0.8			0.8	V
	Receiver			1.5			1.8	
High-level output current, I_{OH}	Receiver output			−400			−400	μA
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	Driver or strobe	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Receiver	V_{CC} = MIN, $V_{IL(R)}$ = V_{IL} max,	$V_{IH(S)}$ = 2 V, I_{OH} = −400 µA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	Driver	V_{CC} = MIN, $V_{IL(S)}$ = 0.8 V,	$V_{IH(D)}$ = 2 V, I_{OL} = 100 mA			0.45			0.45	V
		Receiver	V_{CC} = MIN, $V_{IH(S)}$ = 2 V,	$V_{IH(R)}$ = V_{IH} min, I_{OL} = 16 mA			0.4			0.4	
I_I	Input current at maximum input voltage	Driver or strobe	V_{CC} = MAX,	V_I = V_{CC}			1			1	mA
I_{IH}	High-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 2.4 V			40			40	µA
		Receiver	V_{CC} = 5 V, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 4.5 V,		25	300		25	300	
I_{IL}	Low-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
		Receiver	V_{CC} = MAX, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 0.45 V,			−50			−50	µA
	Input current with power off	Receiver	V_{CC} = 0,	V_I = 4.5 V		1.1	1.5		1.1	1.5	mA
I_{OS}	Short-circuit output current§	Receiver	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	All driver outputs low	V_{CC} = MAX, $V_{I(S)}$ = 0.8 V	$V_{I(D)}$ = 2 V,		50	65		50	65	mA
		All driver outputs high	V_{CC} = MAX, $V_{I(S)}$ = 2 V, Receiver outputs open	$V_{I(R)}$ = 3.5 V,		42	55		42	55	

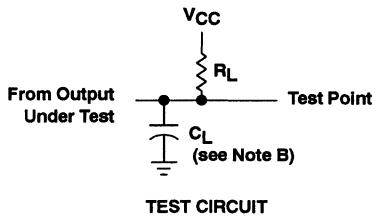
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

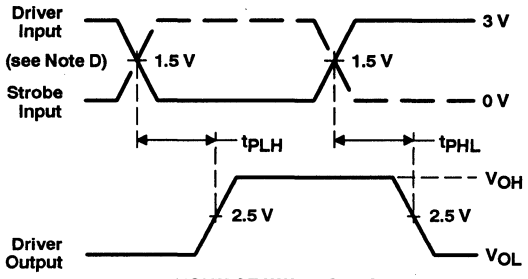
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Driver	Driver	C_L = 50 pF, See Figure 1	R_L = 50 Ω,		15	24	ns
t_{PHL}						14	24	
t_{PLH}	Strobe	Driver				18	28	ns
t_{PHL}						22	32	
t_{PLH}	Receiver	Receiver	C_L = 15 pF, See Figure 2	R_L = 400 Ω,		7	15	ns
t_{PHL}						8	15	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

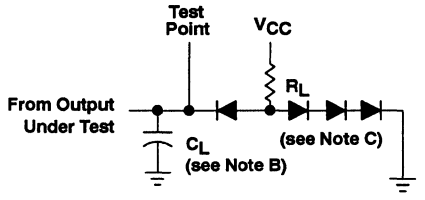


TEST CIRCUIT

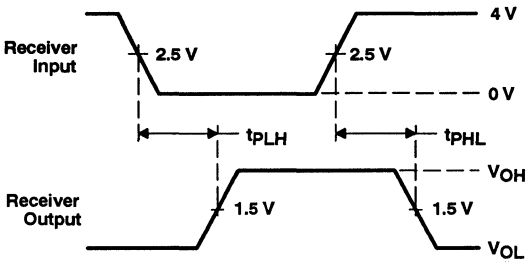


VOLTAGE WAVEFORMS

Figure 1. Propagation Delay Times From Data and Strobe Inputs



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Propagation Delay Times From Receiver Input

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 100 ns, PRR ≤ 1 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

TYPICAL CHARACTERISTICS†

DRIVER TRANSFER CHARACTERISTICS

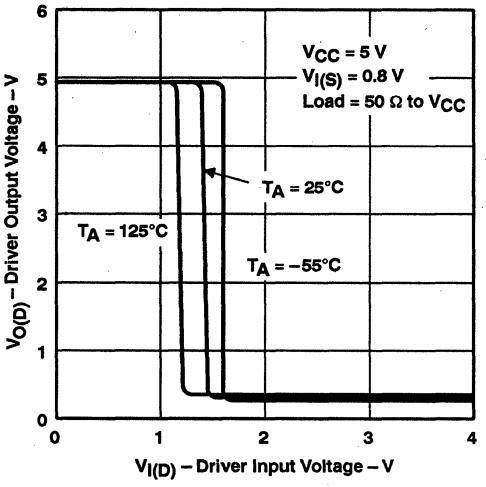


Figure 3

DRIVER TRANSFER CHARACTERISTICS

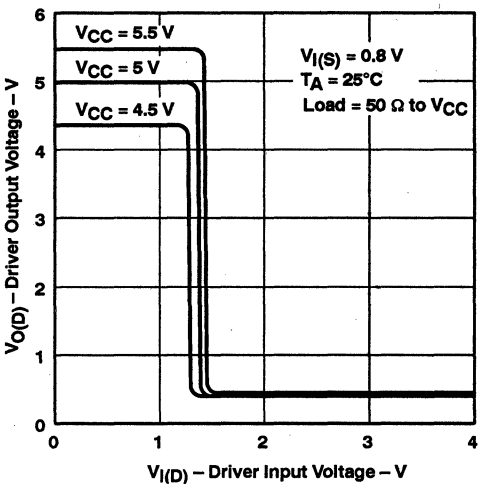


Figure 4

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

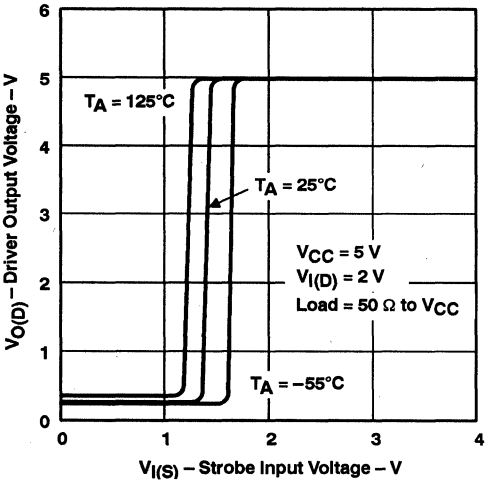


Figure 5

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

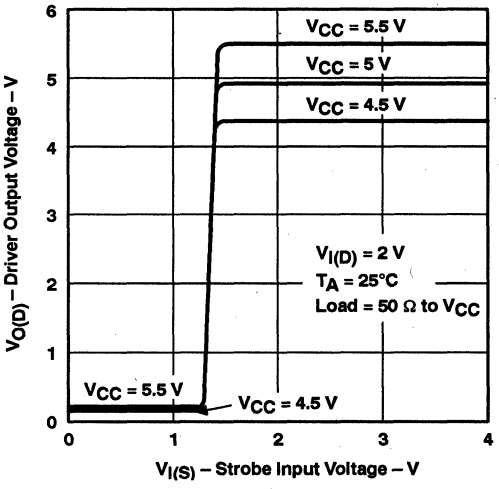


Figure 6

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

RECEIVER TRANSFER CHARACTERISTICS

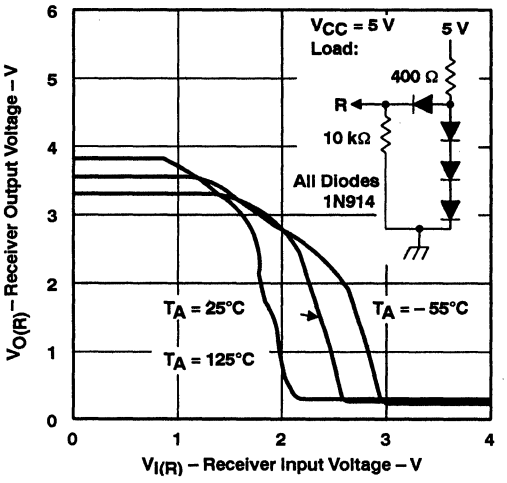


Figure 7

RECEIVER TRANSFER CHARACTERISTICS

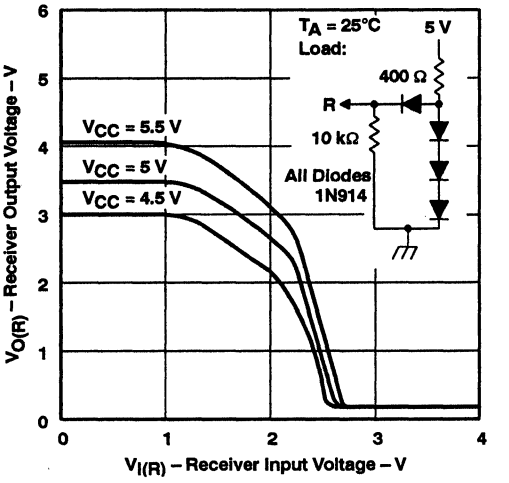


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (RECEIVER)

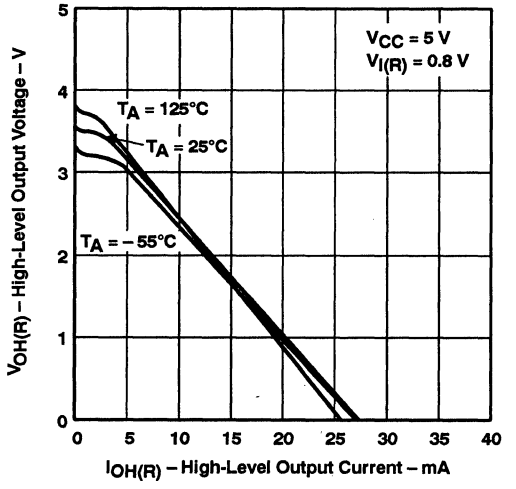


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (RECEIVER)

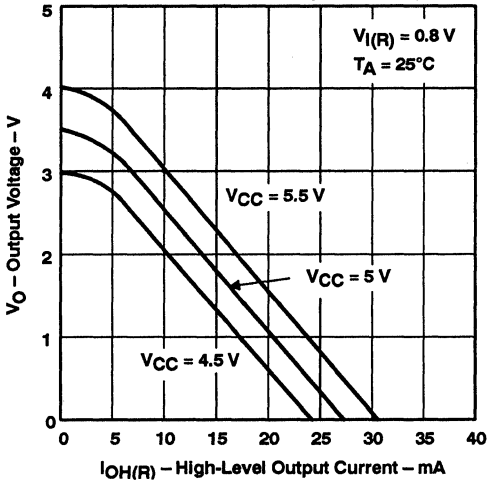


Figure 10

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

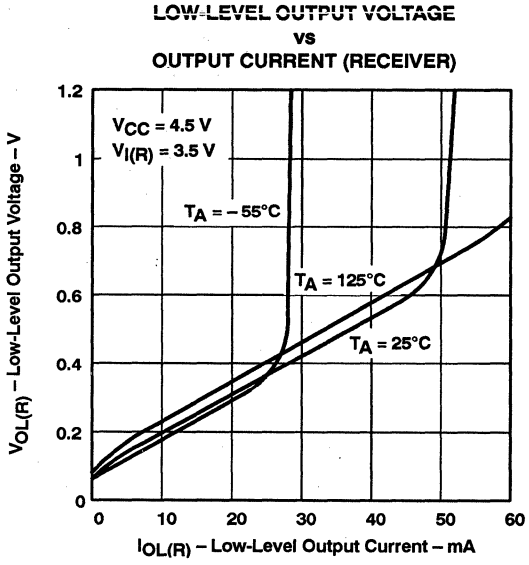


Figure 11

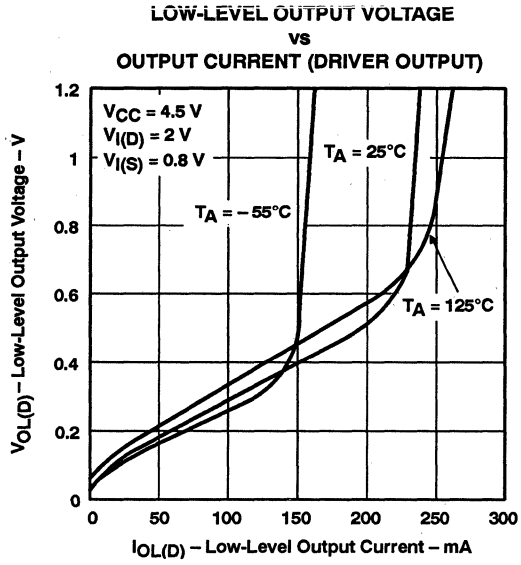


Figure 12

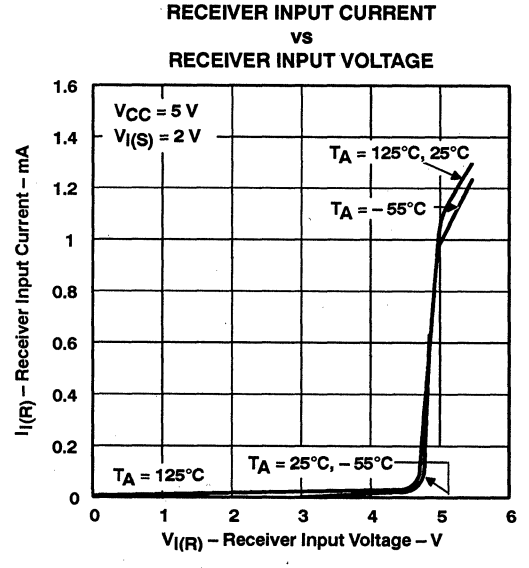


Figure 13

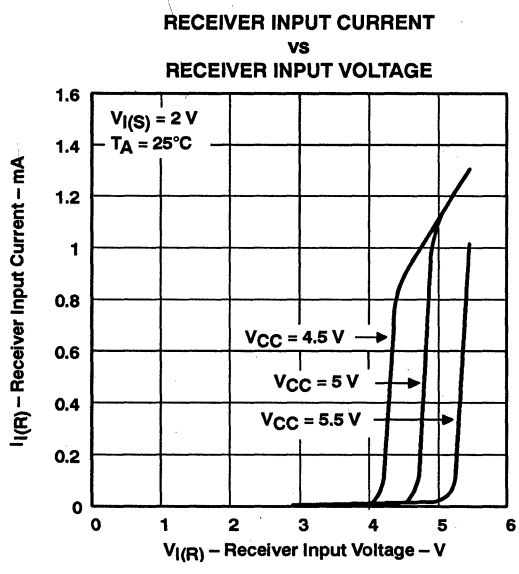


Figure 14

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE
(ALL DRIVER OUTPUTS LOW)

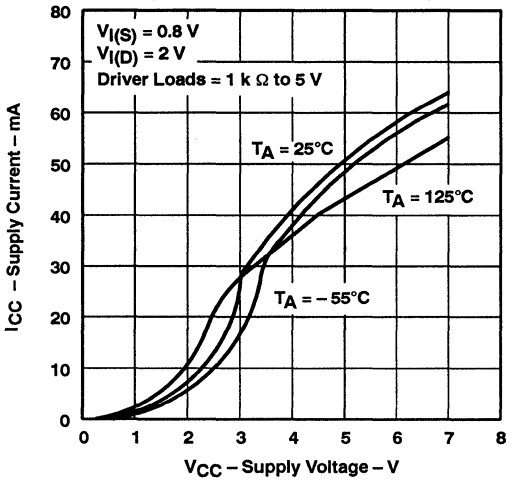


Figure 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

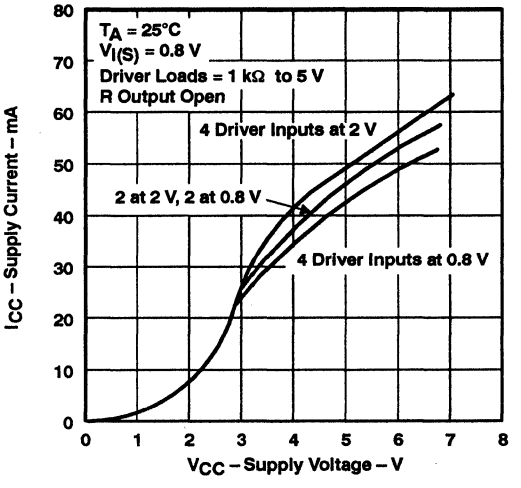


Figure 16

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

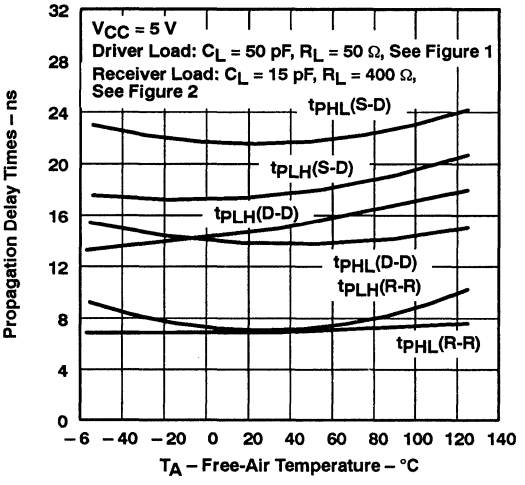


Figure 17

PROPAGATION DELAY TIMES
vs
SUPPLY VOLTAGE

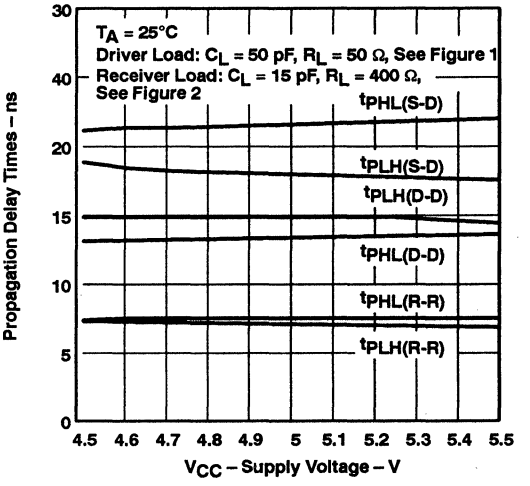


Figure 18

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS

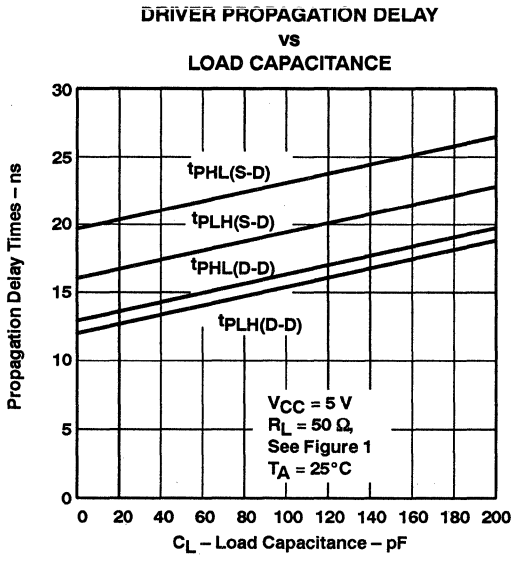


Figure 19

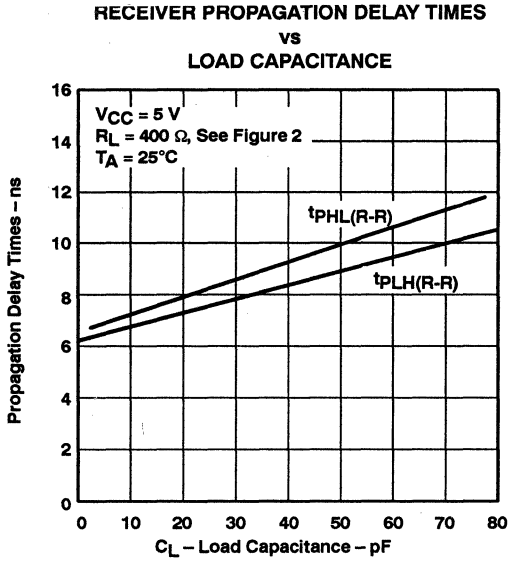


Figure 20

APPLICATION INFORMATION

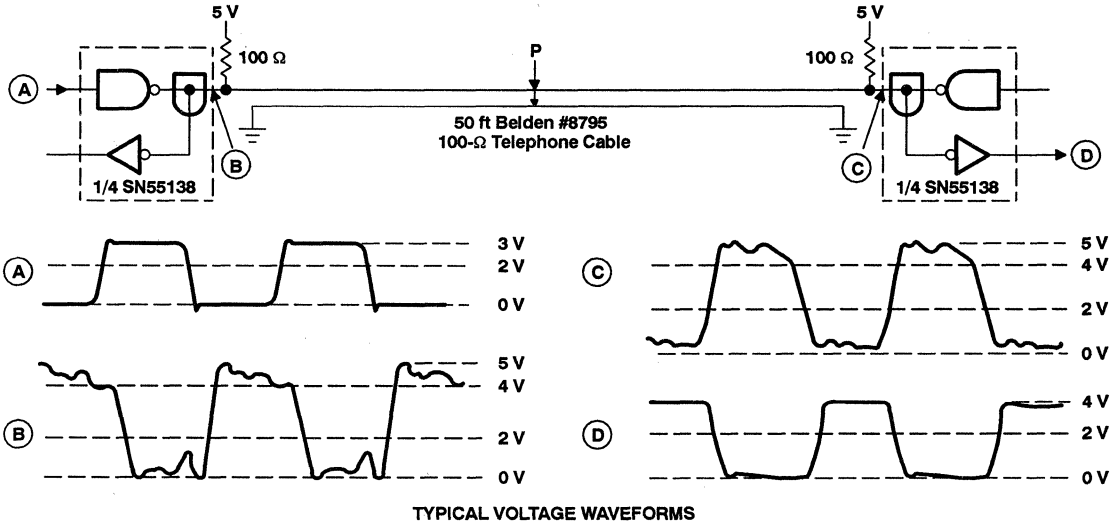
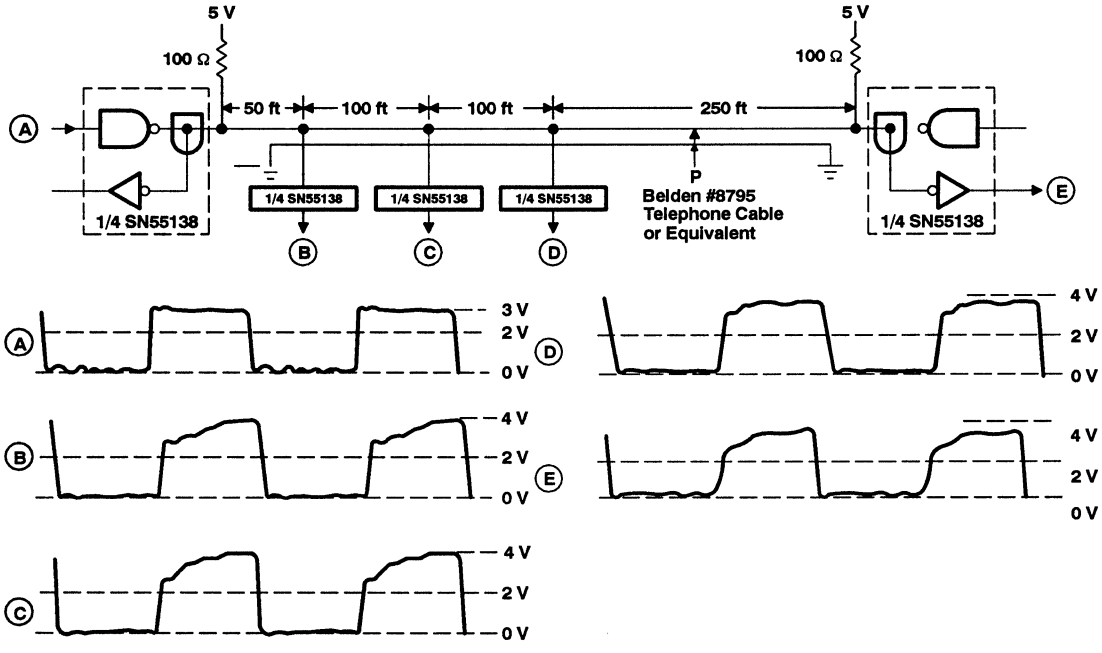


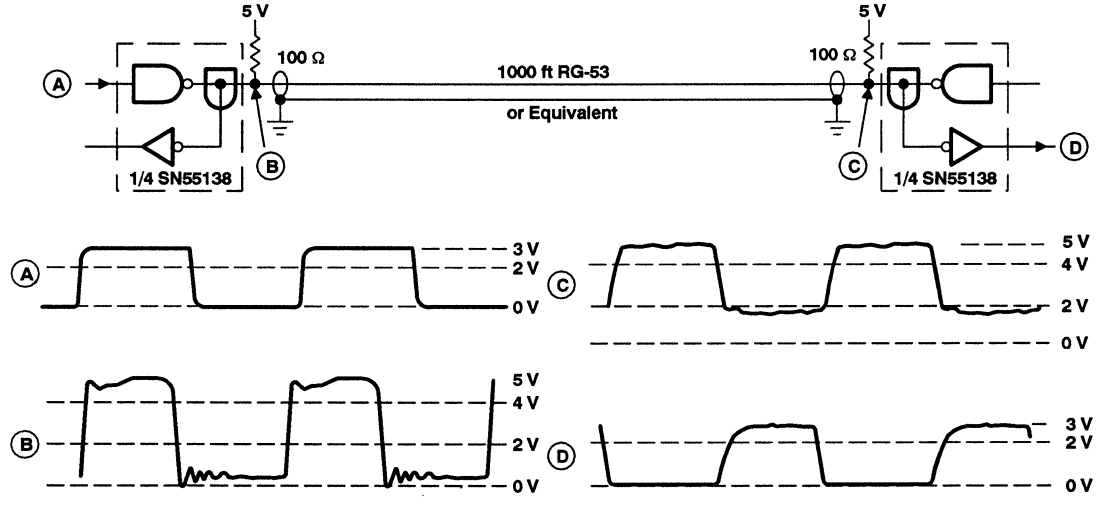
Figure 21. Point-to-Point Communication Over 50 Feet of Twisted Pair at 5 MHz

APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

Figure 22. Party-Line Communication on 500 Feet of Twisted Pair at 1 MHz



TYPICAL VOLTAGE WAVEFORMS

Figure 23. Point-to-Point Communication Over 1000 Feet of Coax at 1 MHz

SLLS080A – D2155, JANUARY 1977 – REVISED FEBRUARY 1993

- **Single 5-V Supply**
- **±100-mV Sensitivity**
- **For Application as:**
  Single-Ended Line Receiver
  Gated Oscillator
  Level Comparator
- **Adjustable Reference Voltage**
- **TTL Outputs**
- **TTL-Compatible Strobe**
- **Designed for Party-Line (Data-Bus) Applications**
- **Common Reference Pin**
- **Common Strobe**
- **SN75141 Has Diode-Protected Input Stage for Power-Off Condition**

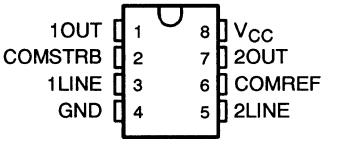
description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.5 V, making it possible to optimize noise immunity for a given system design. Due to their low input current (less than 100 μA), they are ideally suited for party-line (bus-organized) systems.

The SN75140 has a common reference voltage pin and a common strobe. The SN75141 is the same as the SN75140 except that the input stage is diode protected.

The SN75140 and SN75141 are characterized for operation from 0°C to 70°C.

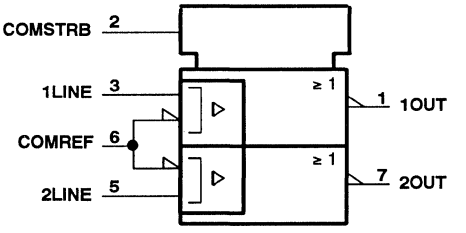
D, P, OR PS† PACKAGE
(TOP VIEW)



† The PS package is only available left-ended taped and reeled (order SN75140 PSLE).

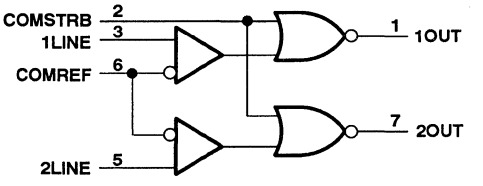
SN75141
NOT RECOMMENDED FOR NEW DESIGN

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

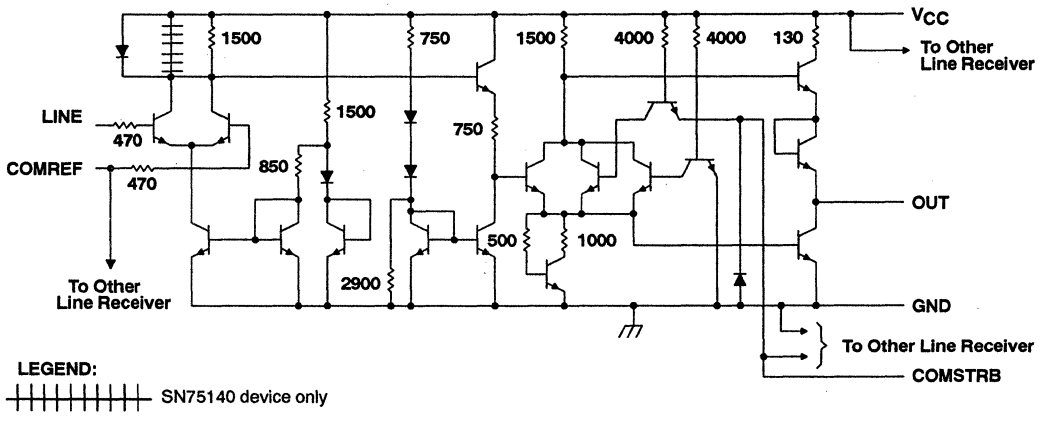


FUNCTION TABLE
(each receiver)

LINE INPUT	STROBE	OUTPUT
≤ V_{ref} – 100 mV	L	H
≥ V_{ref} + 100 mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Reference input voltage, V_{ref} ..... 5.5 V
Line input voltage range with respect to GND ..... −2 V to 5.5 V
Line input voltage with respect to V_{ref} ..... ±5 V
Strobe input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Unless otherwise specified, voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Reference input voltage, V_{ref}	1.5		3.5	V
High-level line input voltage, $V_{IH(L)}$	$V_{ref}+0.1$		$V_{CC}-1$	V
Low-level line input voltage, $V_{IL(L)}$	0		$V_{ref}-0.1$	V
High-level strobe input voltage, $V_{IH(S)}$	2		5.5	V
Low-level strobe input voltage, $V_{IL(S)}$	0		0.8	V

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

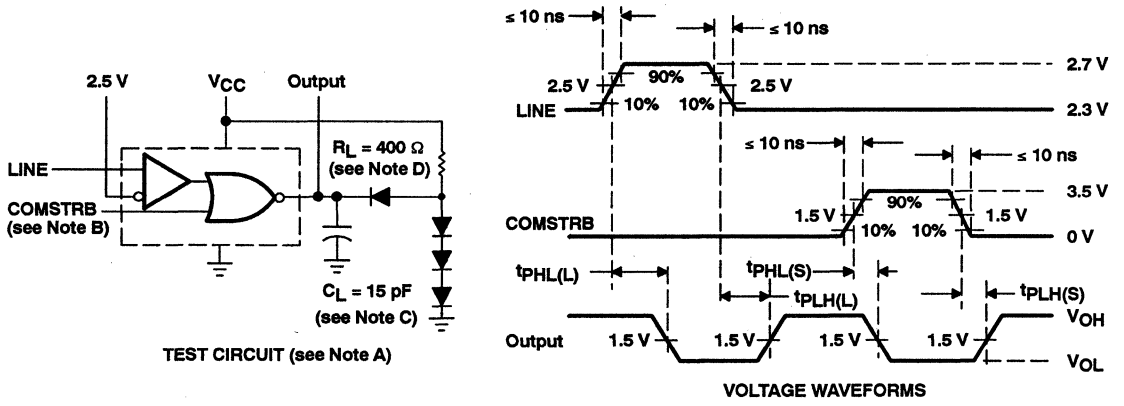
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Strobe input clamp voltage		$I_{I(S)}$ = −12 mA				−1.5	V
V_{OH}	High-level output voltage		$V_{IL(L)} = V_{ref}$ − 100 mV, I_{OH} = −400 µA	$V_{IL(S)}$ = 0.8 V,	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)} = V_{ref}$ + 100 mV, I_{OL} = 16 mA	$V_{IL(S)}$ = 0.8 V,			0.4	V
			$V_{IL(L)} = V_{ref}$ − 100 mV, I_{OL} = 16 mA	$V_{IH(S)}$ = 2 V,			0.4	
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V				1	mA
		COMSTRB					2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V				40	µA
		COMSTRB					80	
		LINE	$V_{I(L)}$ = 3.5 V,	V_{ref} = 1.5 V		35	100	
		Reference	$V_{I(L)}$ = 0,	V_{ref} = 3.5 V		35	100	
		COMREF				70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V				−1.6	mA
		COMSTRB					−3.2	
		LINE	$V_{I(L)}$ = 0,	V_{ref} = 1.5 V			−10	µA
		Reference	$V_{I(L)}$ = 1.5 V,	V_{ref} = 0			−10	
		COMREF					−20	
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V		−18		−55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0,	$V_{I(L)} = V_{ref}$ − 100 mV		18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0,	$V_{I(L)} = V_{ref}$ + 100 mV		20	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high-level output from LINE	C_L = 15 pF, R_L = 400 kΩ, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low-level output from LINE			22	30	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from COMSTRB			12	22	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from COMSTRB			8	15	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω.
B. Unused strobes are to be grounded.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

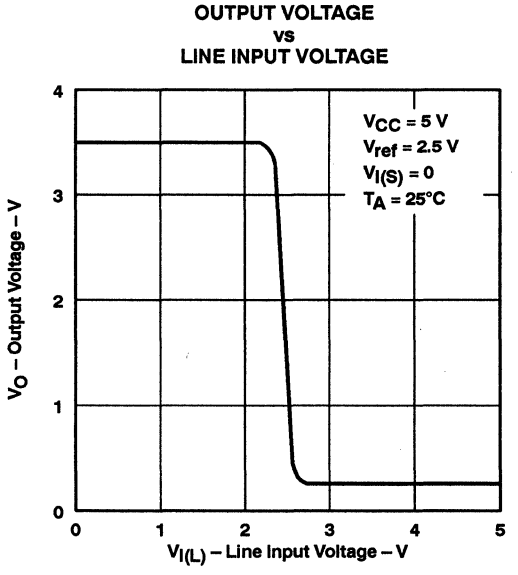


Figure 2

APPLICATION INFORMATION

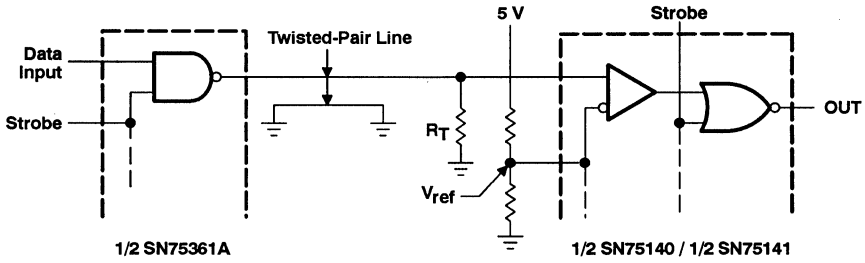
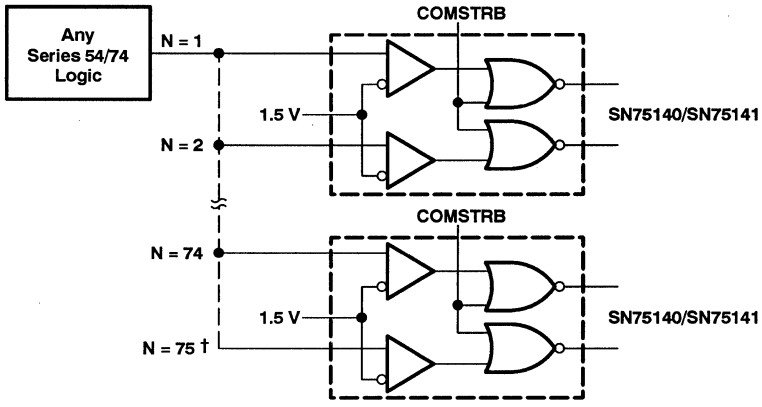


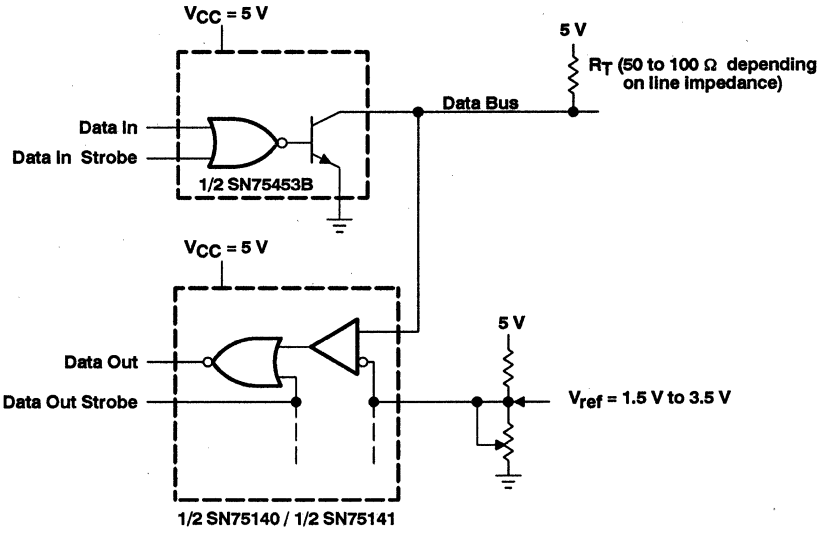
Figure 3. Line Receiver



† Although most Series 54/74 circuits have a 2.4-V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

Figure 4. High Fanout From Standard TTL Gate

APPLICATION INFORMATION



NOTE: Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package and only one power supply is required (5 V). Data In and Data Out terminals are TTL compatible.

Figure 5. Dual Bus Transceiver

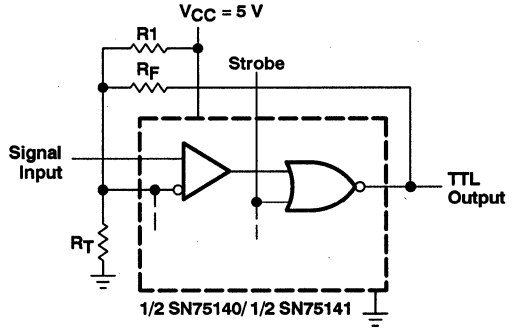
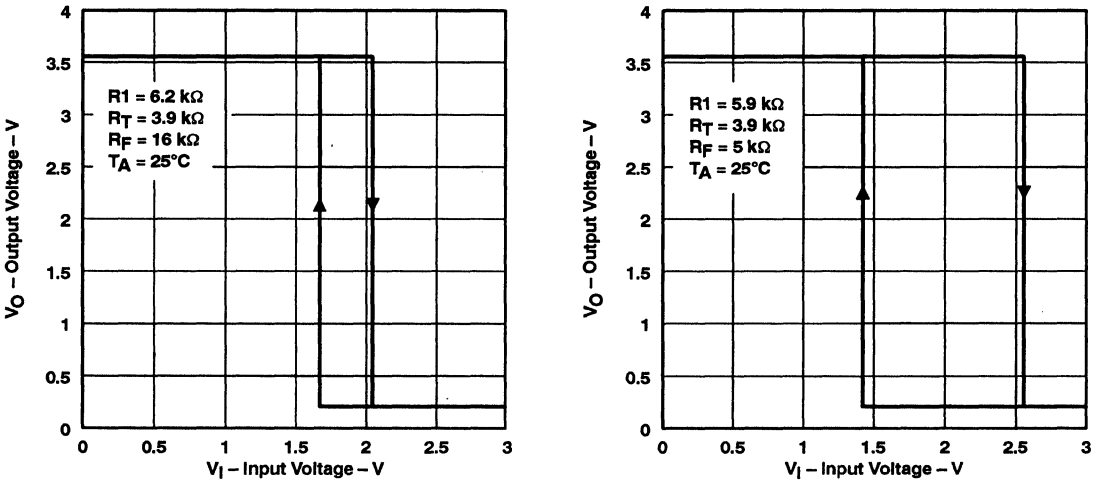


Figure 6. Schmitt Trigger

APPLICATION INFORMATION



NOTE: Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R_1, R_F, and R_T may be adjusted for the desired hysteresis and trigger levels.

Figure 7. Examples of Transfer Characteristics

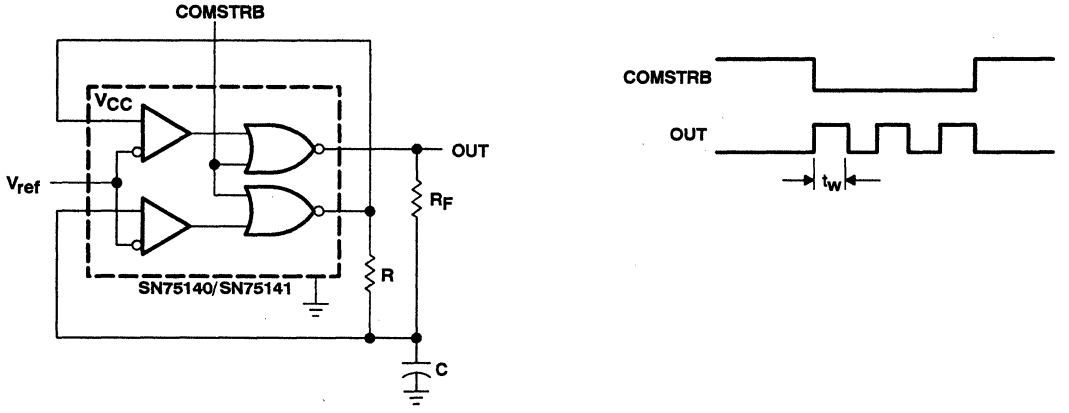


Figure 8. Gated Oscillator

APPLICATION INFORMATION

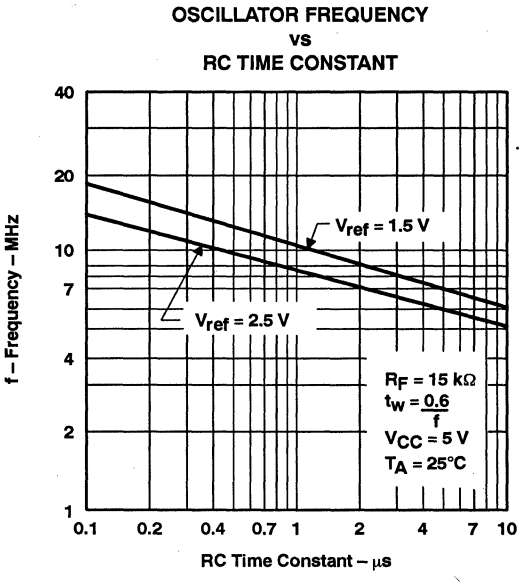
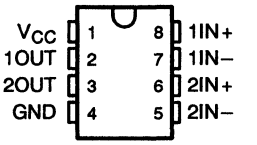


Figure 9

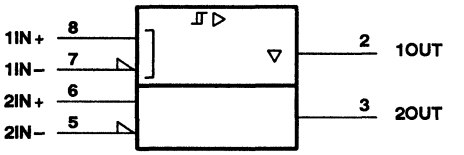
SLLS015A – D2609, FEBRUARY 1986 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets EIA Standards RS-232 and CCITT V.28 With External Components**
- **Meets Federal Standards 1020 and 1030**
- **Built-in 5-MHz Low-Pass Filter**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **8-Pin Dual-In-Line Package**
- **Pinout Compatible With the μA9637 and μA9639**

D OR P PACKAGE
(TOP VIEW)

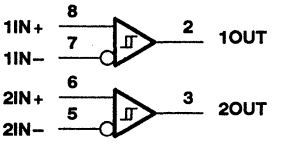


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

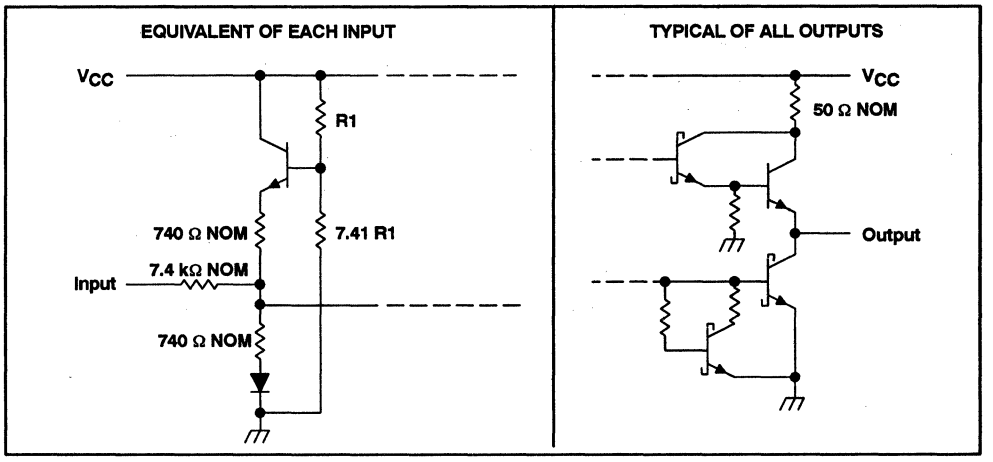


description

The SN75146 is a dual differential line receiver designed to meet EIA Standards RS-422-A and RS-423-A. The receiver is designed to have a constant impedance with input voltages of ±3 V to ±25 V allowing it to meet the requirements of EIA Standard RS-232-C and CCITT recommendation V.28 with the addition of an external bias resistor. This receiver is designed for low-speed operation below 355 kHz and has a built-in 5-MHz low-pass filter to attenuate high-frequency noise. The inputs are compatible with either a single-ended or a differential line system and the outputs are TTL compatible. This device operates from a single 5-V power supply and is supplied in both the 8-pin dual-in-line and small-outline packages.

The SN75146 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage ..... ±25 V
Differential input voltage (see Note 2) ..... ±25 V
Output voltage range (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

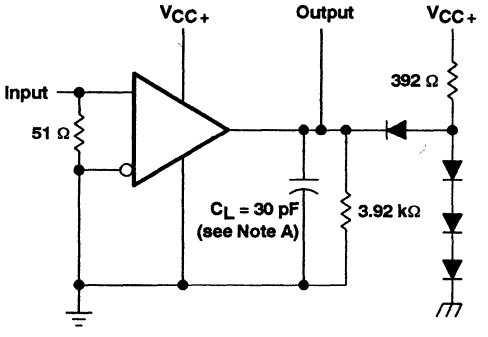
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2‡		0.2	V
		See Note 3		−0.4‡		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			70			mV
V_{IB}	Input bias voltage	I_I = 0		2		2.4	V
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
r_i	Input resistance	V_I = 3 V to 25 V or V_I = −3 V to −25 V, See Note 4		6	7.8	10.5	kΩ
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 5	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. r_i is defined by $\Delta V_I/\Delta I_I$.
5. The input not under test is grounded.

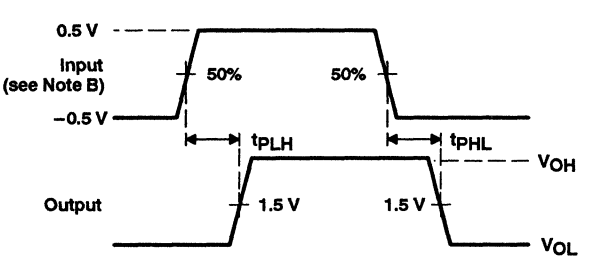
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	See Figure 1	100	150	300	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	150	300	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 300 kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

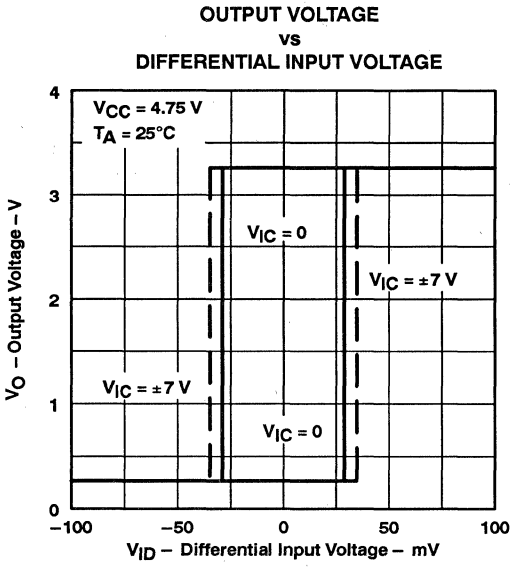


Figure 2

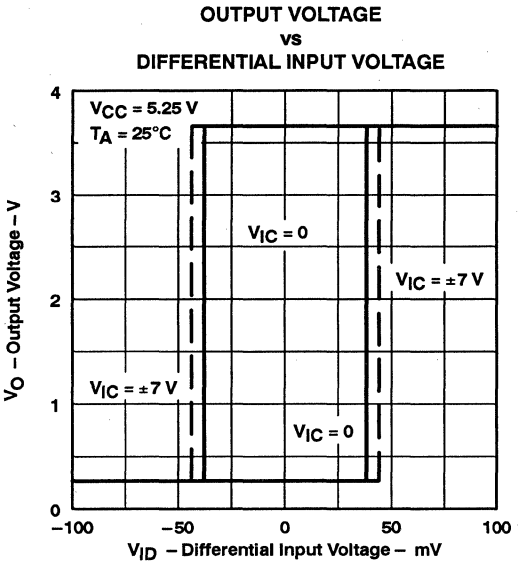
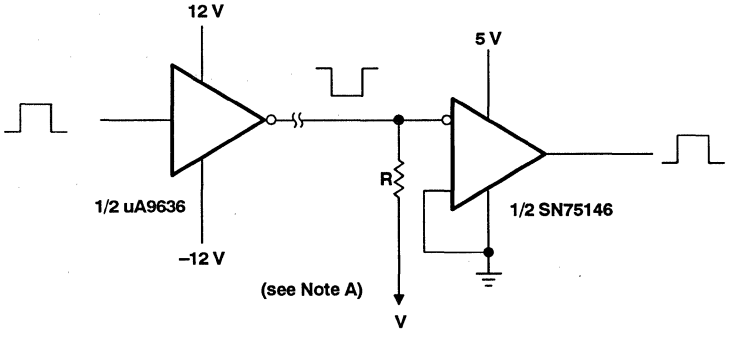


Figure 3

APPLICATION INFORMATION



NOTE A: In order to meet the input-impedance and open-circuit-input voltage requirements of RS-232-C and CCITT V.28 and ensure open-circuit-input fail-safe operation, R and V are selected to satisfy the following equations:

$$V = -1.1 - 3.3\,\frac{R}{r_i}\ \text{volts}$$

$$3\ \text{k}\Omega \le \frac{R(r_i)}{R + r_i} \le 7\ \text{k}\Omega$$

Figure 4. RS-232-C System Applications

APPLICATION INFORMATION

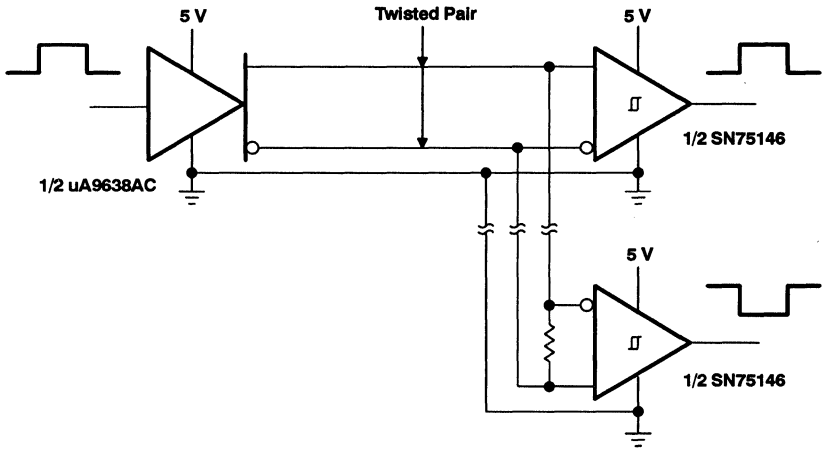


Figure 5. RS-422-A System Applications

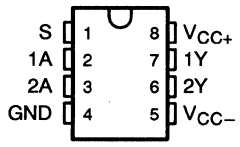
- **Satisfies Requirement of EIA Standard RS-232-C**
- **Withstands Sustained Output Short Circuit to Any Low-Impedance Voltage Between −25 V and 25 V**
- **2-μs Max Transition Time Through the 3-V to −3-V Transition Region Under Full 2500-pF Load**
- **Inputs Compatible With Most TTL Families**
- **Common Strobe Input**
- **Inverting Output**
- **Slew Rate Can Be Controlled With an External Capacitor at the Output**
- **Standard Supply Voltages . . . ±12 V**

description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL families. Operation is from 12-V and −12-V power supplies.

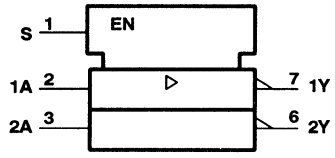
The SN75150 is characterized for operation from 0°C to 70°C.

D, P, OR PS† PACKAGE
(TOP VIEW)



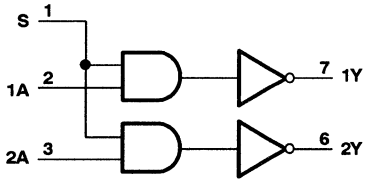
† The PS package is only available left-end taped and reeled, i.e., order device SN75150PSLE.

logic symbol‡

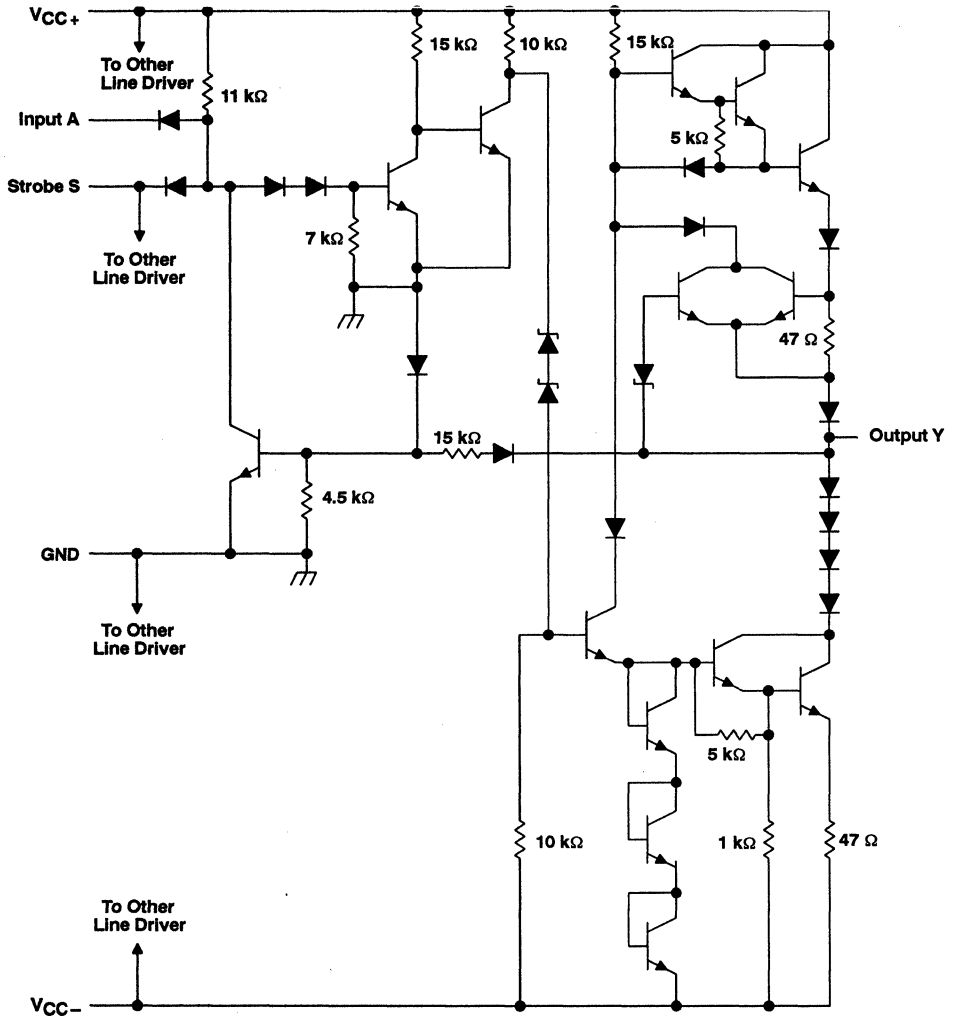


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each line driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} ..... −15 V
Input voltage, V_I ..... 15 V
Applied output voltage ..... ±25 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	10.8	12	13.2	V
Supply voltage, V_{CC-}	−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	0		0.8	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±13.2 V (unless otherwise noted)

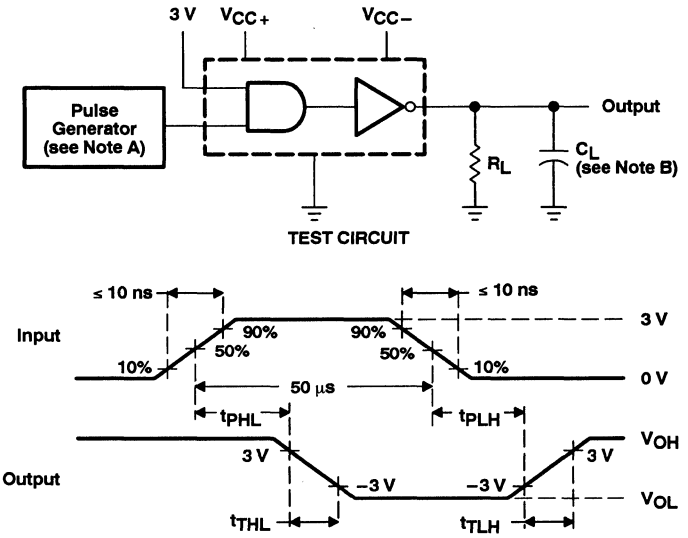
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC+} = 10.8 V, V_{IL} = 0.8 V,	V_{CC-} = −13.2 V, R_L = 3 kΩ to 7 kΩ	5	8		V
V_{OL}	Low-level output voltage (see Note 2)		V_{CC+} = 10.8 V, V_{IH} = 2 V,	V_{CC-} = −10.8 V, R_L = 3 kΩ to 7 kΩ		−8	−5	V
I_{IH}	High-level input current	Data input	V_I = 2.4 V			1	10	μA
		Strobe input				2	20	
I_{IL}	Low-level input current	Data input	V_I = 0.4 V			−1	−1.6	mA
		Strobe input				−2	−3.2	
I_{OS}	Short-circuit output current‡		V_O = 25 V			2	8	mA
			V_O = −25 V			−3	−8	
			V_O = 0,	V_I = 3 V	10	15	30	
			V_O = 0,	V_I = 0	−10	−15	−30	
I_{CCH+}	Supply current from V_{CC+}, high-level output		V_I = 0, T_A = 25°C	R_L = 3 kΩ,		10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	
I_{CCL+}	Supply current from V_{CC+}, low-level output		V_I = 3 V, T_A = 25°C	R_L = 3 kΩ,		8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	

† All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	C_L = 2500 pF,	R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	C_L = 15 pF,	R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

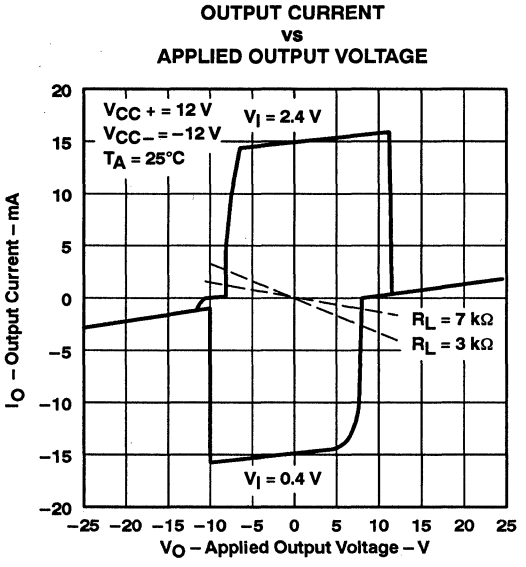


Figure 2

APPLICATION INFORMATION

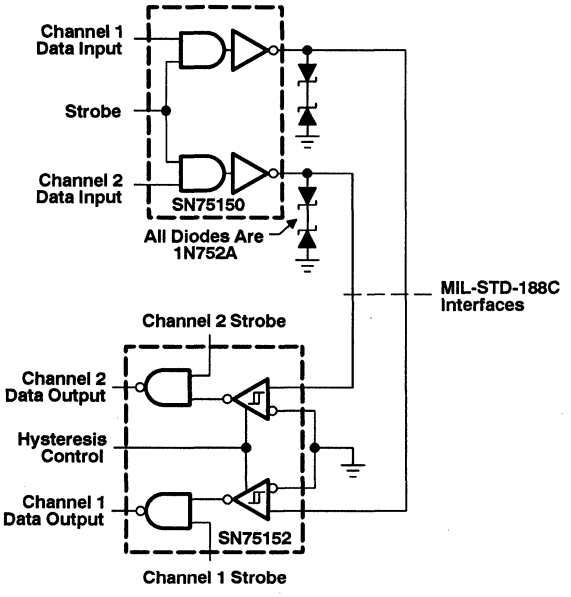
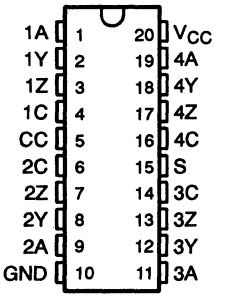


Figure 3. Dual-Channel Single-Ended Interface Circuit Meeting MIL-STD-188C, Paragraph 7.2.

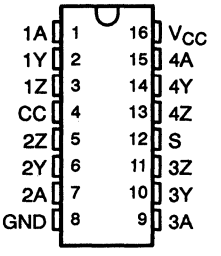
SLLS082A – D2453, DECEMBER 1978 – REVISED FEBRUARY 1993

- **Meets EIA Standard RS-422-A**
- **High-Impedance Output State for Party-Line Operation**
- **High Output Impedance in Power-Off Condition**
- **Low Input Current to Minimize Loading**
- **Single 5-V Supply**
- **40-mA Sink- and Source-Current Capability**
- **High-Speed Schottky Circuitry**
- **Low Power Requirements**

SN75151
DW OR N PACKAGE
(TOP VIEW)



SN75153
N PACKAGE
(TOP VIEW)



description

These line drivers are designed to provide differential signals with high current capability on balanced lines. These circuits provide strobe and enable inputs to control all four drivers, and the SN75151 provides an additional enable input for each driver. The output circuits have active pullup and pulldown and are capable of sinking or sourcing 40 mA.

The SN75151 and SN75153 meet all requirements of EIA Standard RS-422-A and Federal Standard 1020. They are characterized for operation from 0°C to 70°C.

SN75153
NOT RECOMMENDED FOR NEW DESIGN

Function Tables

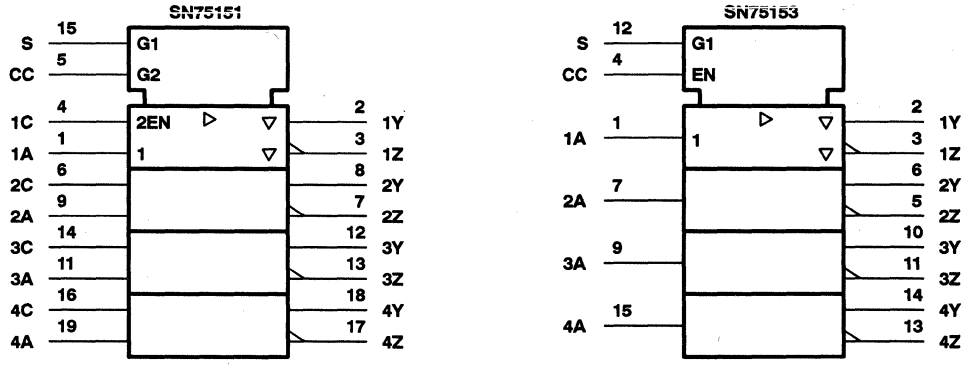
SN75151

INPUTS				OUTPUTS	
ENABLE CC	ENABLE C	STROBE S	DATA A	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

SN75153

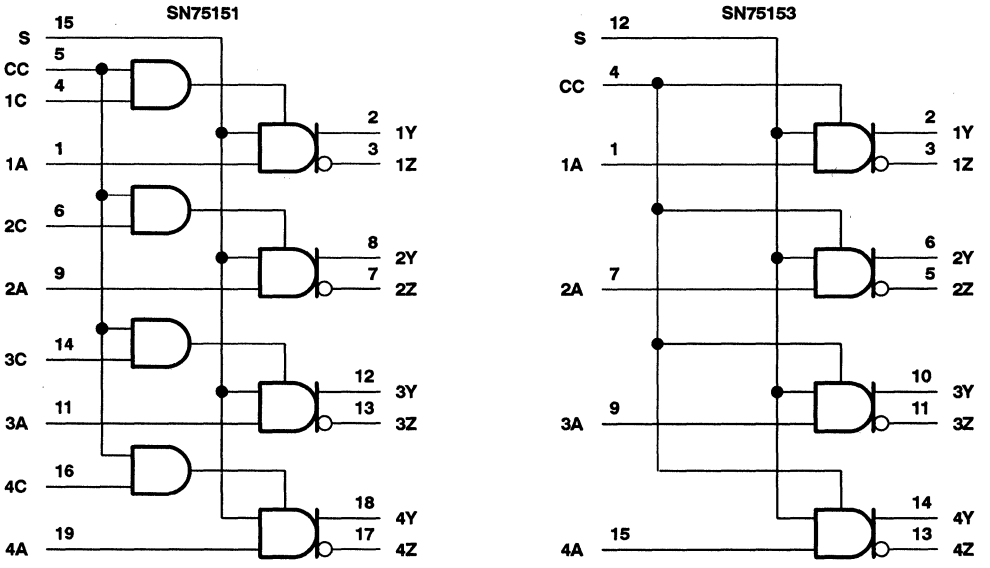
INPUTS			OUTPUTS	
ENABLE CC	STROBE S	DATA A	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

logic symbols†



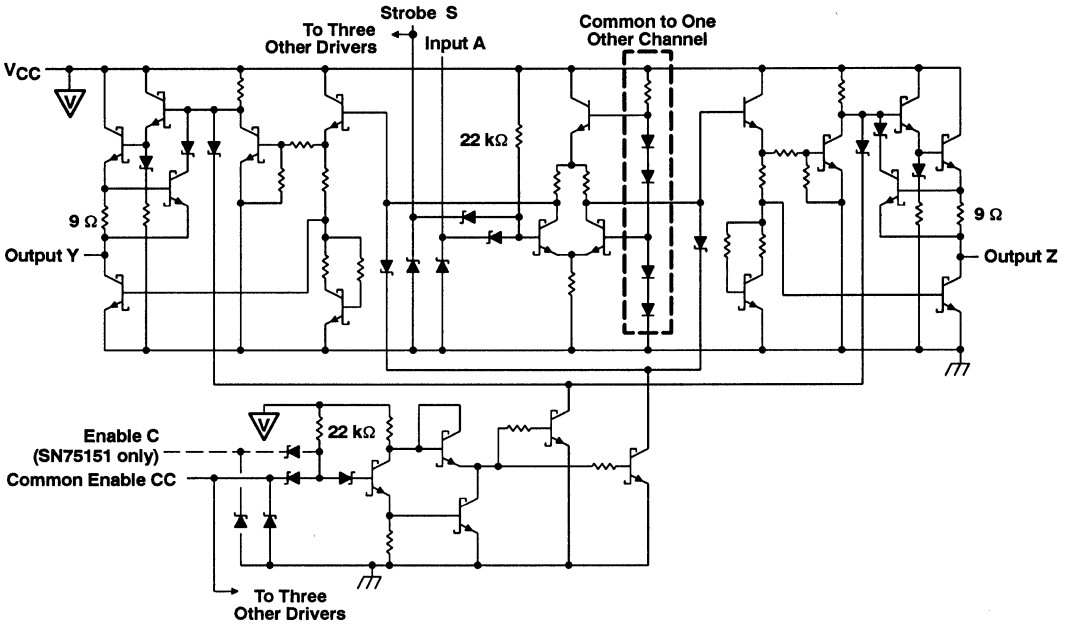
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	−0.25		6	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA	CC, S			−2	V
			All others		−0.9	−1.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −20 mA	2.5			V
			I_{OH} = −40 mA	2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = 40 mA	V_{IH} = 2 V,			0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MAX, I_O = 0			3.4	$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	2.8		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.01	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.8	3	V
		V_{CC} = MIN			1.6	3	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4	V
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX, Enable at 0.8 V	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
			V_O = V_{CC}			20	
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	C(SN75151), A			20	μA
			CC, S			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	C(SN75151), A			−0.36	mA
			CC, S			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−50	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load	Outputs disabled		30	60	mA
			Outputs enabled		60	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 2,	R_L = 100 Ω, Termination A		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, Termination B	See Figure 2,		13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				13	25	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, See Figure 2,	R_L = 100 Ω, Termination A		12	20	ns
t_{THL}	Transition time, high-to-low-level output				12	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, See Figure 3	R_L = 60 Ω,		18	35	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, See Figure 4	R_L = 111 Ω,		20	35	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, See Figure 3	R_L = 60 Ω,		19	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, See Figure 4	R_L = 111 Ω,		13	30	ns
	Overshoot factor	R_L = 100 Ω, Termination C	See Figure 2,			10	%

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

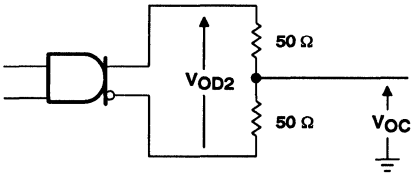
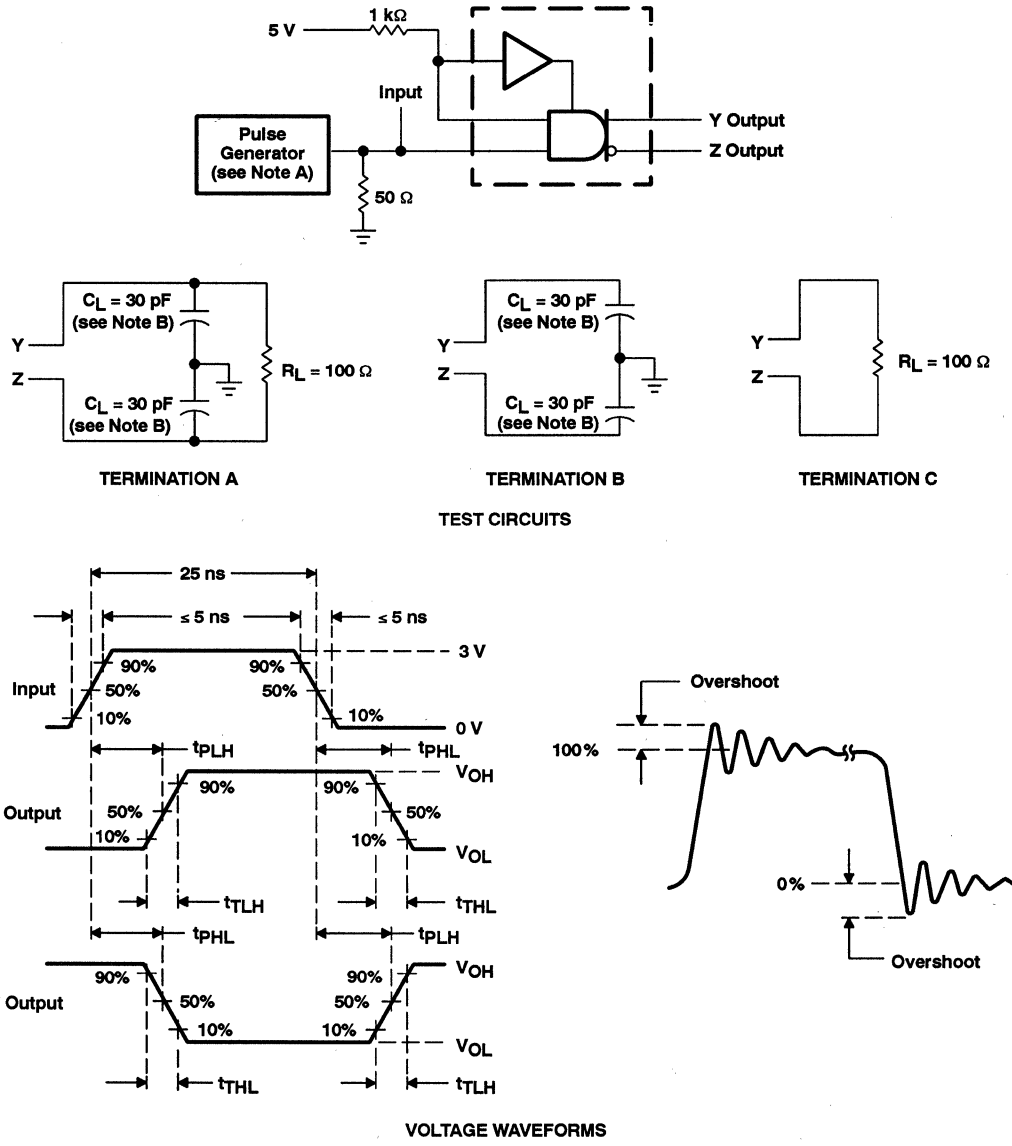


Figure 1. Differential and Common-Mode Output Voltages

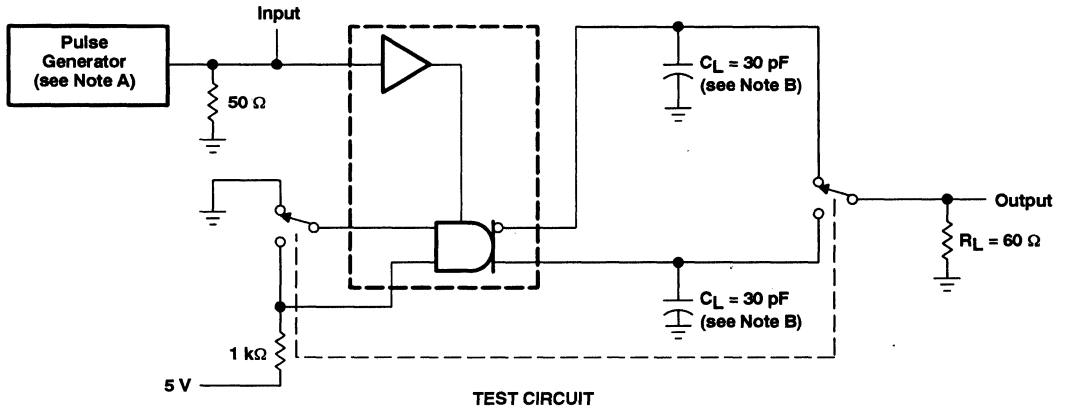
PARAMETER MEASUREMENT INFORMATION



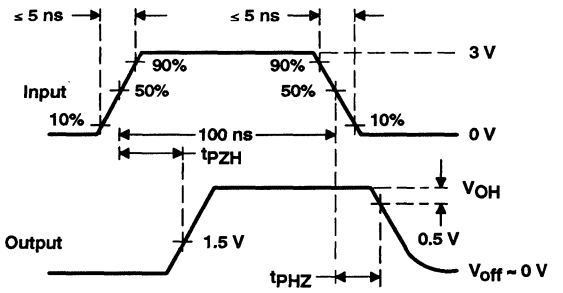
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuits, Voltage Waveforms, and Overshoot Factor

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

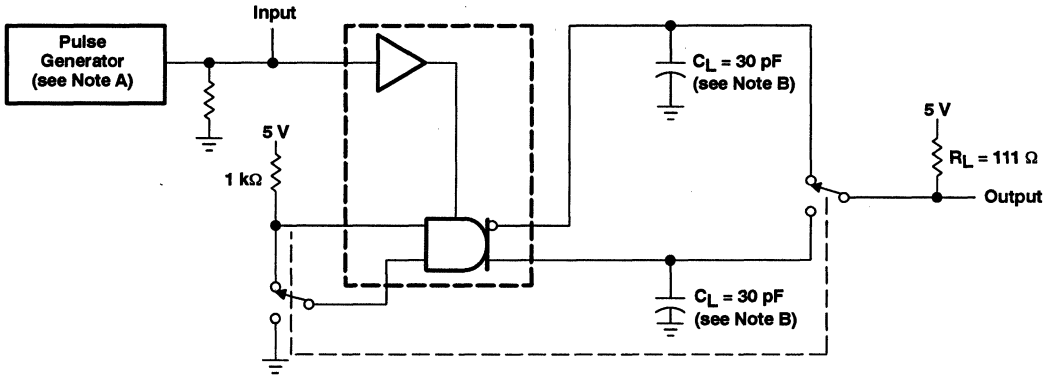


VOLTAGE WAVEFORMS

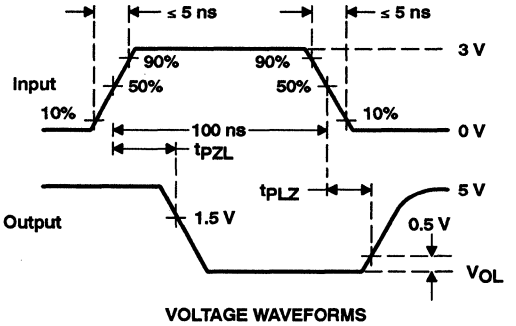
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

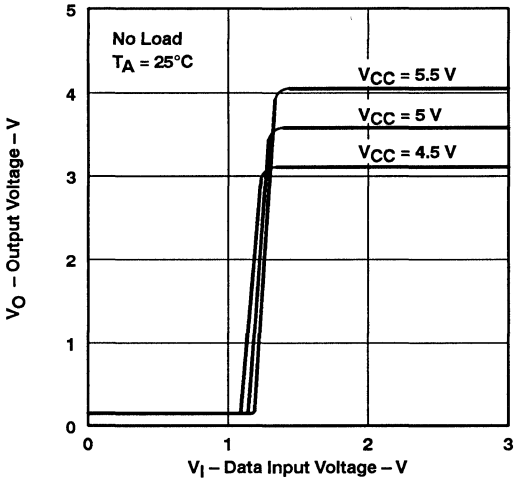
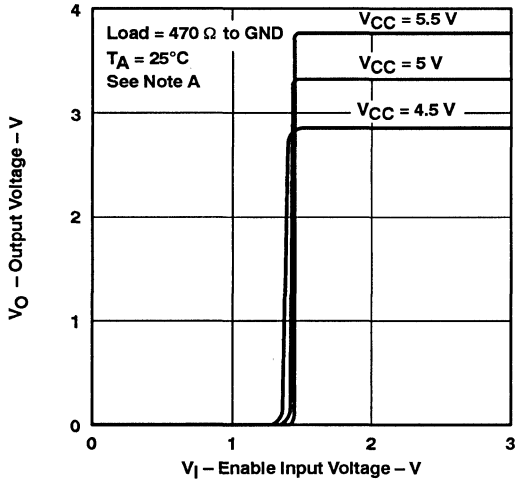


Figure 5

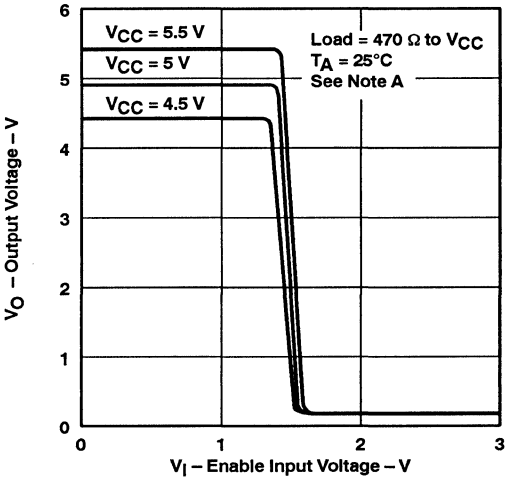
Y OR Z OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE



NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

Figure 6

Y OR Z OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE



NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

Figure 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

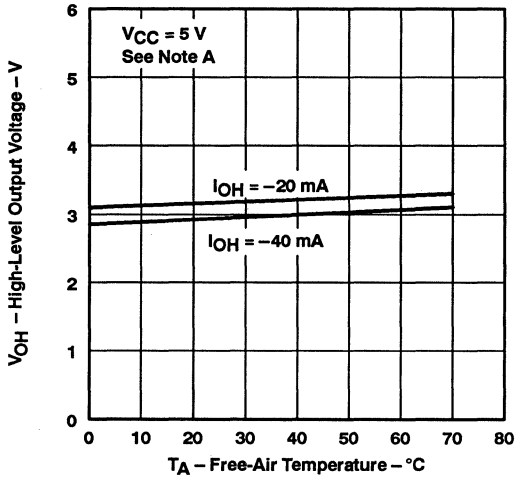


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

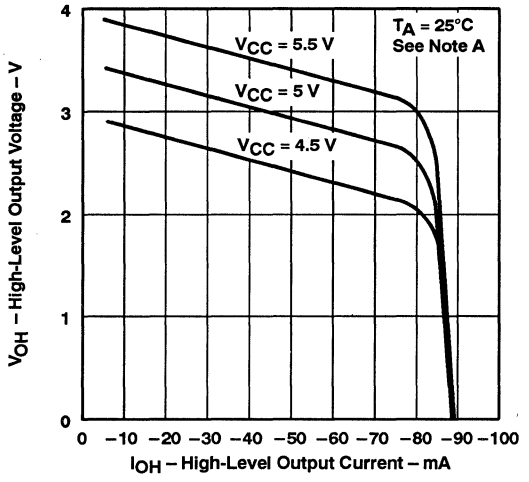


Figure 9

NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

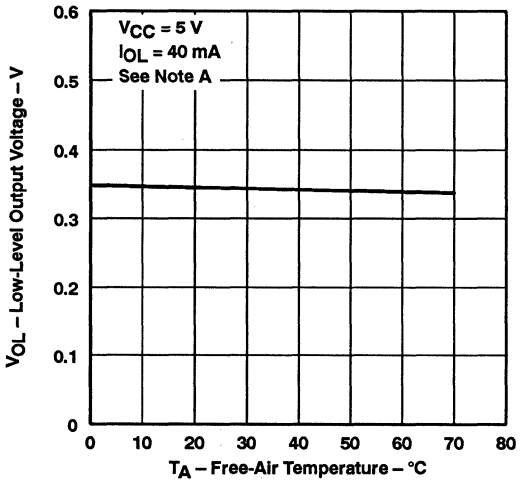


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

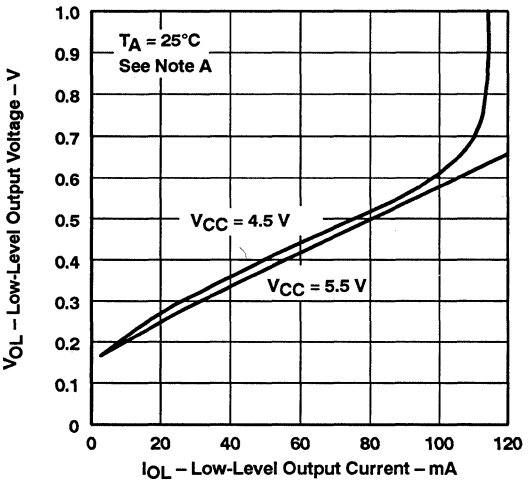


Figure 11

NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

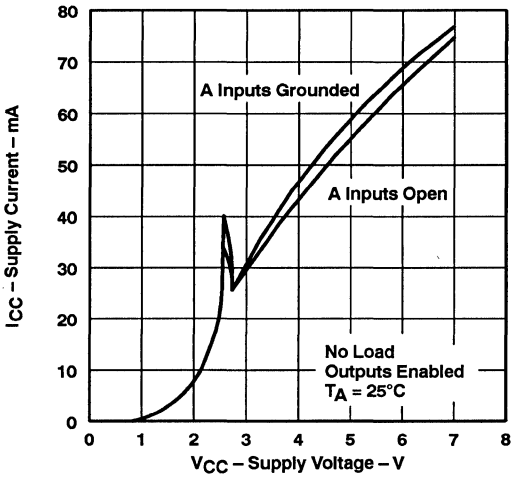


Figure 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

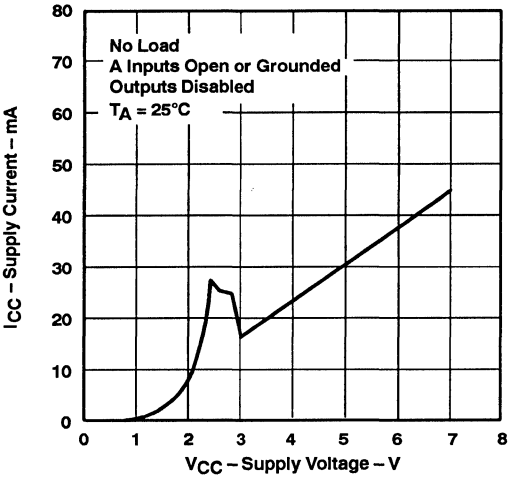
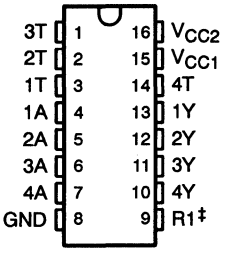


Figure 13

SLLS083A – D899, NOVEMBER 1970 – REVISED MARCH 1993

- **Satisfies Requirements of EIA Standard RS-232-C**
- **Input Resistance . . . 3 kΩ to 7 kΩ Over Full RS-232-C Voltage Range**
- **Input Threshold Adjustable to Meet Fail-Safe Requirements Without Using External Components**
- **Built-In Hysteresis for Increased Noise Immunity**
- **Inverting Output Compatible With TTL**
- **Output With Active Pullup for Symmetrical Switching Speeds**
- **Standard Supply Voltages . . . 5 V or 12 V**

D, N, OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled, i.e., order device SN75154NSLE.
‡ For function of R1, see schematic

description

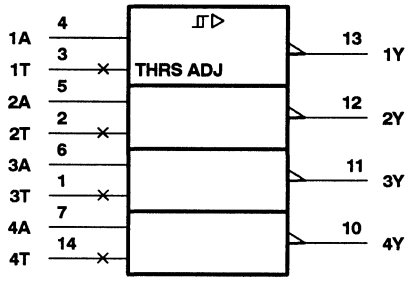
The SN75154 is a monolithic low-power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, even if power is being supplied via the alternate V_{CC2} terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

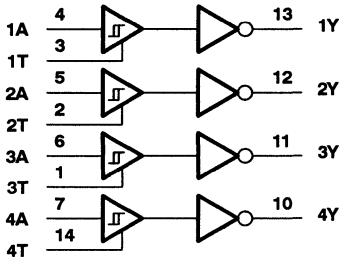
The SN75154 is characterized for operation from 0°C to 70°C.

logic symbol†

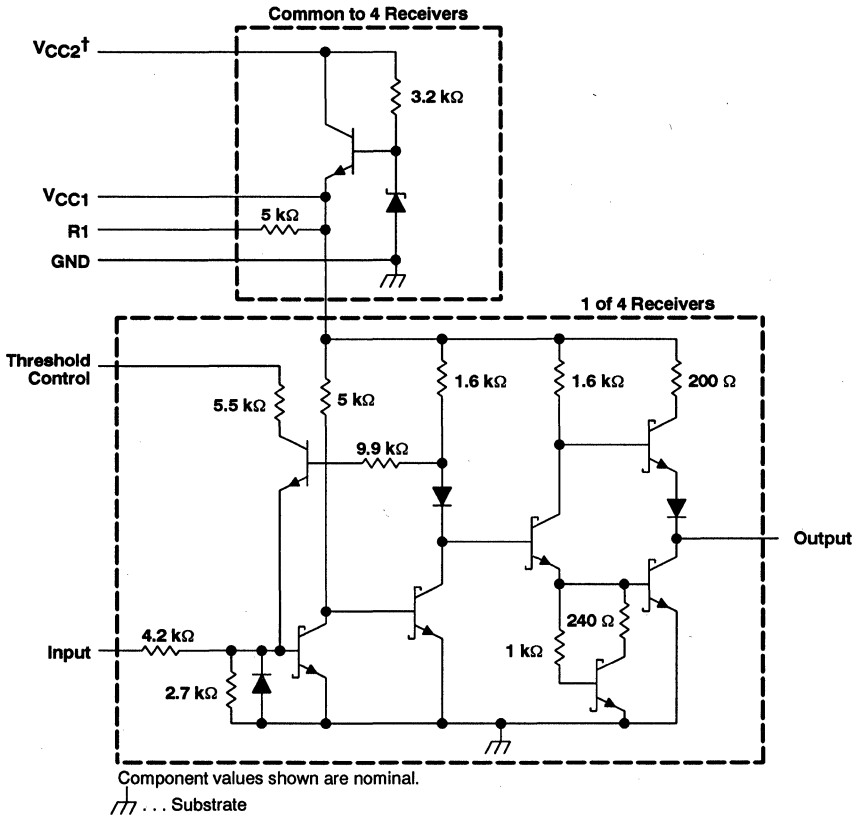


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematic



† When V_{CC1} is used, V_{CC2} may be left open or shorted to V_{CC1}. When V_{CC2} is used, V_{CC1} must be left open or connected to the threshold control pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage, V_{CC1} (see Note 1) ..... 7 V
Alternate supply voltage, V_{CC2} ..... 14 V
Input voltage, V_I ..... ±25 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage, V_{CC1}	4.5	5	5.5	V
Alternate supply voltage, V_{CC2}	10.8	12	13.2	V
High-level input voltage, V_{IH} (see Note 2)	3		15	V
Low-level input voltage, V_{IL} (see Note 2)	−15		−3	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

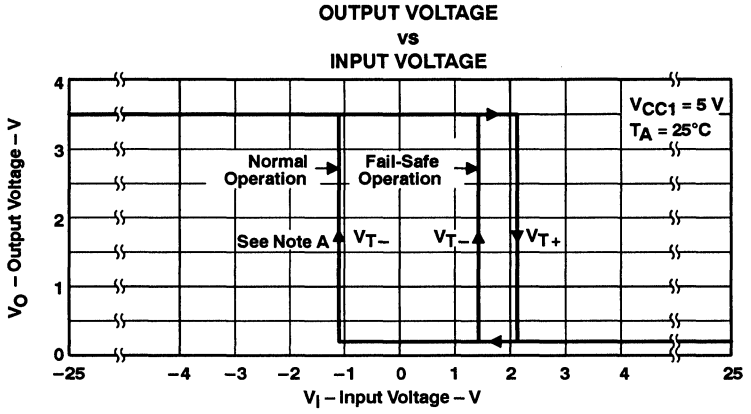
PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.29	0.4	V
r_i	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6	8	
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current‡		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

† All typical values are at V_{CC1} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		11		ns
t_{PHL}	Propagation delay time, high-to-low-level output				8		ns
t_{TLH}	Transition time, low-to-high-level output				7		ns
t_{THL}	Transition time, high-to-low-level output				2.2		ns

TYPICAL CHARACTERISTICS



NOTE A: For normal operation, the threshold controls are connected to V_{CC1}. For fail-safe operation, the threshold controls are open.

Figure 1

PARAMETER MEASUREMENT INFORMATION

dc test circuits†

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1}	V_{CC2}
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	V_{CC1}	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	V_{CC1}	I_{OH}	T	13.2 V
V_{IL} max, V_{T+} min (normal)	V_{OH}	–3 V	V_{CC1}	I_{OH}	5.5 V and T	Open
	V_{OH}	–3 V	V_{CC1}	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	V_{CC1}	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	V_{CC1}	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	V_{CC1}	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	V_{CC1}	I_{OL}	T	13.2 V

NOTES: A. Momentarily apply –5 V, then 0.8 V.
B. Momentarily apply 5 V, then GND.

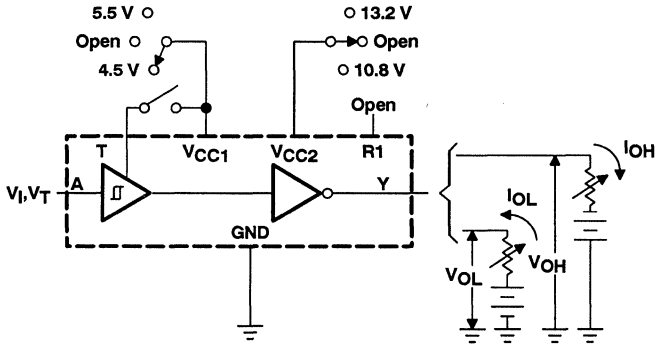
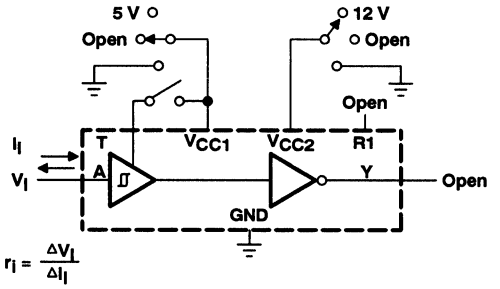


Figure 2. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

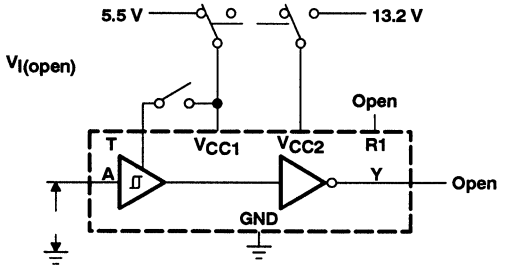
dc test circuits† (continued)



TEST TABLE

T	V_{CC1}	V_{CC2}
Open	5 V	Open
Open	GND	Open
Open	Open	Open
V_{CC1}	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
V_{CC1}	T	12 V
V_{CC1}	T	GND
V_{CC1}	T	Open

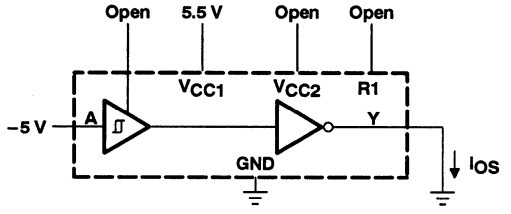
Figure 3. Input Resistance



TEST TABLE

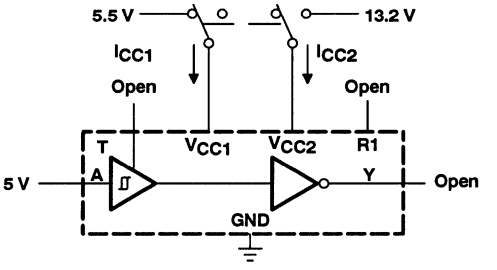
T	V_{CC1}	V_{CC2}
Open	5.5 V	Open
V_{CC1}	5.5 V	Open
Open	Open	13.2 V
V_{CC1}	T	13.2 V

Figure 4. Input Voltage (open)



Each output is tested separately.

Figure 5. Output Short-Circuit Current

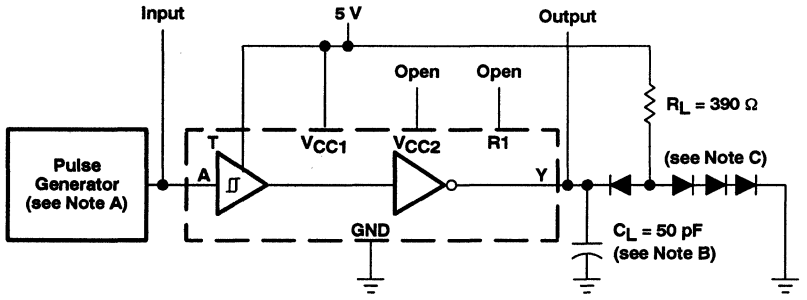


All four line receivers are tested simultaneously.

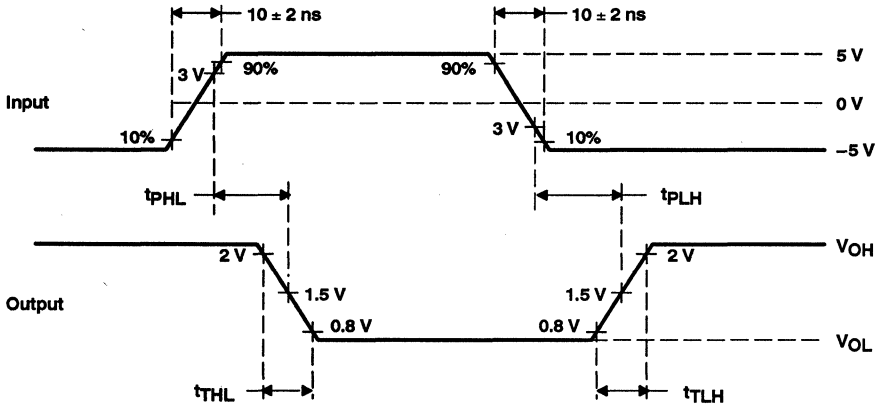
Figure 6. Supply Current

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_w \leq$ 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

Figure 6. Test Circuit and Voltage Waveforms

SLLS017B – D2951, JULY 1986 – REVISED MARCH 1993

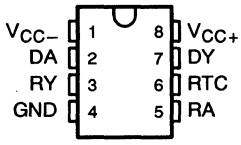
- **Meets EIA-Standard RS-232-C**
- **10-mA Current Limited Output**
- **Wide Range of Supply Voltage**
  V_{CC} = 4.5 V to 15 V
- **Low Power . . . 130 mW**
- **Built-In 5-V Regulator**
- **Response Control Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Power-Off Output Resistance . . . 300 Ω Typ**
- **Driver Input TTL Compatible**

description

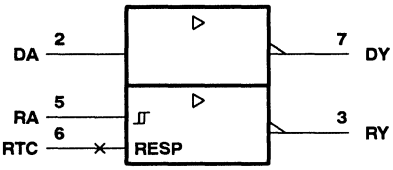
The SN75155 is a monolithic line driver and receiver that is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. A response control input is provided for the receiver. A resistor or a resistor and a bias voltage can be connected between the response control input and ground to provide noise filtering. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A.

The SN75155 is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
TOP VIEW

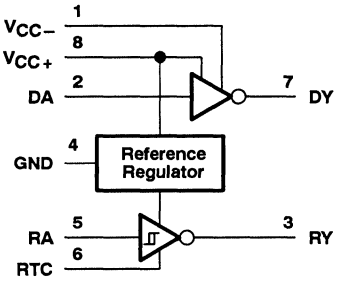


logic symbol†

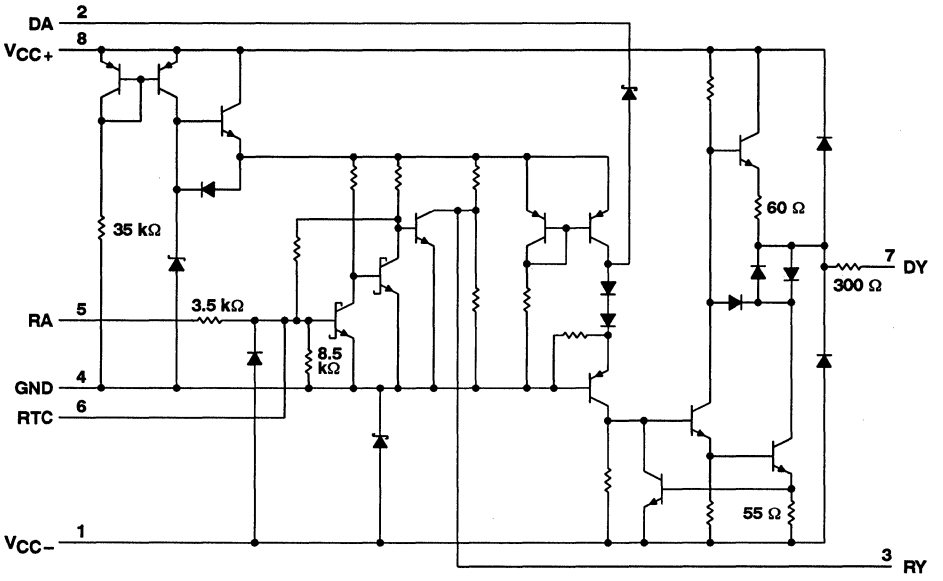


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} (see Note 1) ..... −15 V
Input voltage range: Driver ..... −15 V to 15 V
Receiver ..... −30 V to 30 V
Output voltage range (driver) ..... −15 V to 15 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	−4.5	−12	−15	V
Input voltage, driver, $V_{I(D)}$			±15	V
Input voltage, receiver, $V_{I(R)}$	−25		25	V
High-level input voltage, driver, V_{IH}	2			V
Low-level voltage, driver, V_{IL}			0.8	V
Response control current			±5.5	mA
Output current, receiver, $I_{O(R)}$			24	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CCH+}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = 2.3 V, Output open		6.3	8.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			9.1	11.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			10.4	14	
I_{CCL+}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = 0.6 V, Output open		2.5	3.4	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			3.7	5.1	
		V_{CC+} = 12V,	V_{CC-} = −12 V			4.1	5.6	
I_{CC+}	Supply current	V_{CC+} = 5 V,	V_{CC-} = 0	$V_{I(R)}$ = 2.3 V, $V_{I(D)}$ = 0		4.8	6.4	mA
		V_{CC+} = 9 V,	V_{CC-} = 0			6.7	9.1	
I_{CCH-}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = 2.3 V Output open		−2.4	−3.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			−3.9	−4.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			−4.8	−6.1	
I_{CCL-}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = 0.6 V, Output open		−0.2	−0.35	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			−0.25	−0.4	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			−0.27	−0.45	

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.2	3.7		V
			V_{CC+} = 9 V,	V_{CC-} = −9 V	6.5	7.2		
			V_{CC+} = 12 V,	V_{CC-} = −12 V	8.9	9.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	V_{CC+} = 5 V,	V_{CC-} = −5 V		−3.6	−3.2	V
			V_{CC+} = 9 V,	V_{CC-} = −9 V		−7.1	−6.4	
			V_{CC+} = 12 V,	V_{CC-} = −12 V		−9.7	−8.8	
I_{IH}	High-level input current	V_I = 7 V					5	μA
I_{IL}	Low-level input current	V_I = 0				−0.73	−1.2	mA
$I_{OS(H)}$	High-level short-circuit output current	V_I = 0.8 V, V_O = 0			−7	−12	−14.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = 2 V, V_O = 0			6.5	11.5	15	mA
r_o	Output resistance with power off	V_O = −2 V to 2 V				300		Ω

receiver section (see Figure 1)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshhold voltage				1.2	1.9	2..3	V
V_{T-}	Negative-going threshhold voltage				0.6	0.95	1.2	V
V_{hys}	Hystresis ($V_{T+} - V_{T-}$)				0.6			V
$V_{O(H)}$	High-level output voltage	V_I = 0.6 V, I_{OH} = 10 μA	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.7	4.1	4.5	V
			V_{CC+} = 12 V,	V_{CC-} = −12 V	4.4	4.7	5.2	
		V_I = 0.6 V, I_{OH} = 0.4 mA	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.1	3.4	3.8	
			V_{CC+} = 12 V,	V_{CC-} = −12 V	3.6	4	4.5	
$V_{O(L)}$	Low-level output voltage	V_I = 2.3 V,	I_{OL} = 24 mA			0.2	0.3	V
I_{IH}	High-level input current	V_I = 2 5 V			3.6	6.7	10	mA
		V_I = 3 V			0.43	0.67	1	mA
I_{IL}	Low-level input current	V_I = −25 V			−3.6	−6.7	−10	mA
		V_I = −3 V			−0.43	−0.67	−1	mA
I_{OS}	Short-circuit output current	V_I = 0.6 V				−2.8	−3.7	mA

† All typical values are at T_A = 25°C.

NOTE 2: The algebraic limit system, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only, e.g., if −8.8 V is the maximum, the typical value is a more negative value.

switching characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, C_L = 50 pF (unless otherwise noted)

driver section (see Figure 2)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3 kΩ			250	480	ns
t_{PHL}	Propagation delay time, high-to-low level output				80	150	
t_r	Output rise time	R_L = 3 kΩ			67	180	ns
		R_L = 3 kΩ to 7 kΩ,	C_L = 2500 pF		2.4	3	µs
t_f	Output fall time	R_L = 3 kΩ			48	160	ns
		R_L = 3 kΩ to 7 kΩ,	C_L = 2500 pF		1.9	3	µs

receiver section (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 400 Ω		175	245	ns
t_{PHL}	Propagation delay time, high-to-low level output			37	100	
t_r	Output rise time	R_L = 400 Ω		255	360	ns
t_f	Output fall time	R_L = 400 Ω		23	50	ns

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

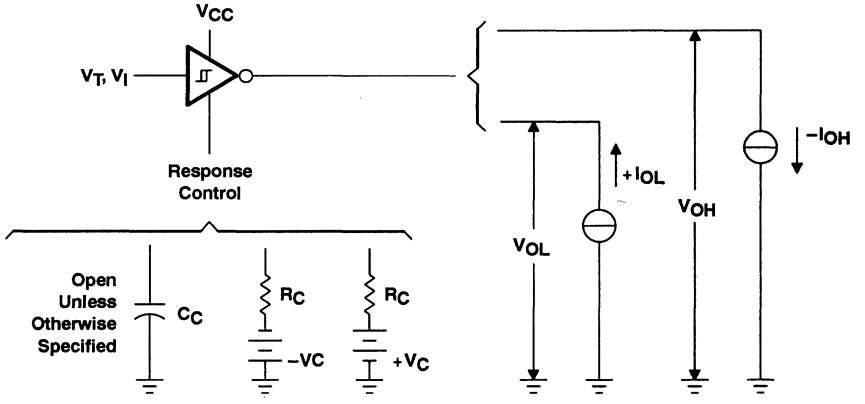


Figure 1. Receiver Section Test Circuit (V_{T+}, V_{T-}, V_{OH}, V_{OL})

PARAMETER MEASUREMENT INFORMATION

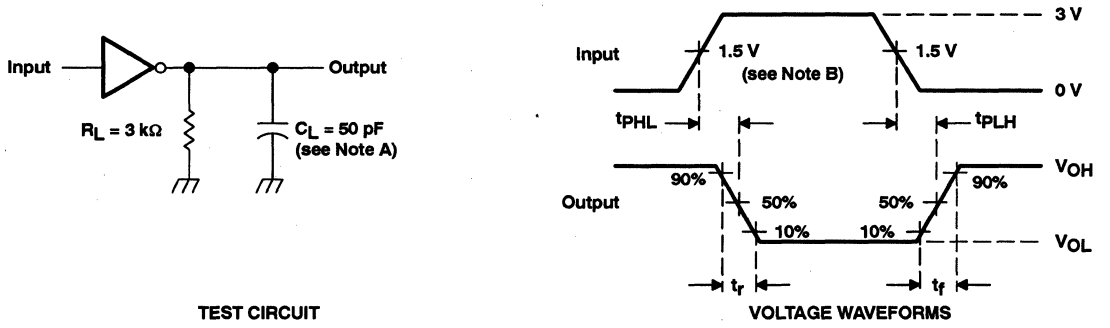


Figure 2. Driver Section Switching Test Circuit and Voltage Waveforms

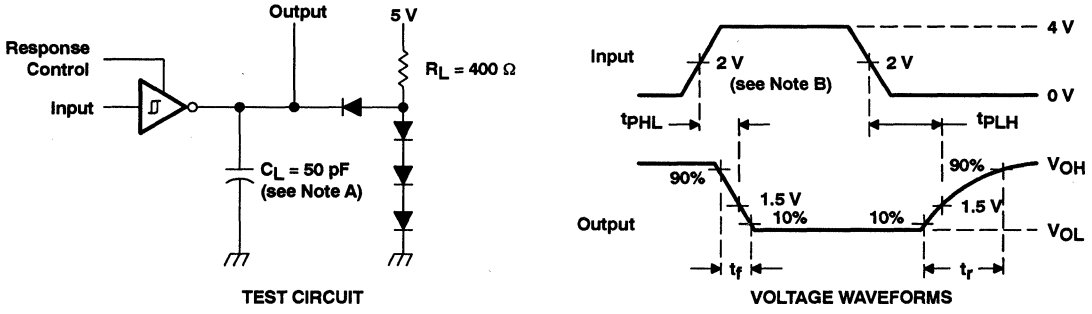


Figure 3. Receiver Section Switching Test Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, t_w = 1 μs, t_r ≤ 10 ns, t_f ≤ 10 ns.

TYPICAL CHARACTERISTICS (DRIVER)

VOLTAGE TRANSFER CHARACTERISTICS

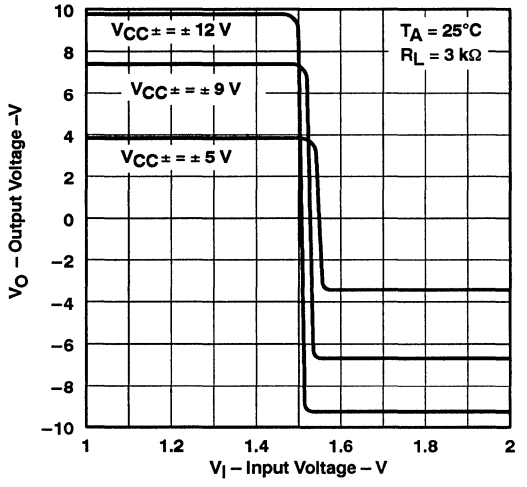


Figure 4

OUTPUT CURRENT vs OUTPUT VOLTAGE

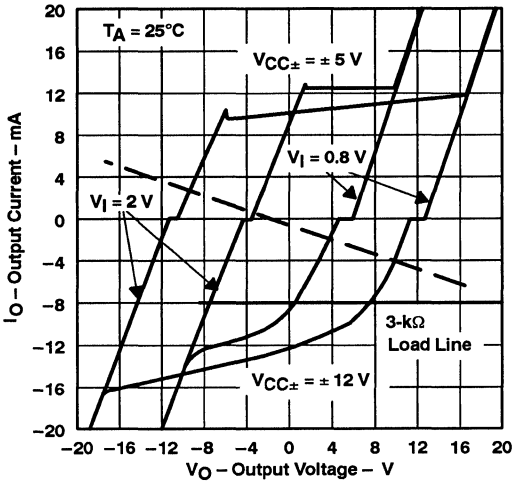


Figure 5

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

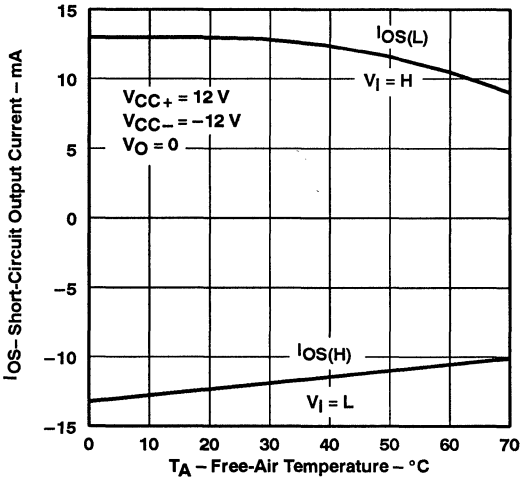


Figure 6

SLEW RATE vs LOAD CAPACITANCE

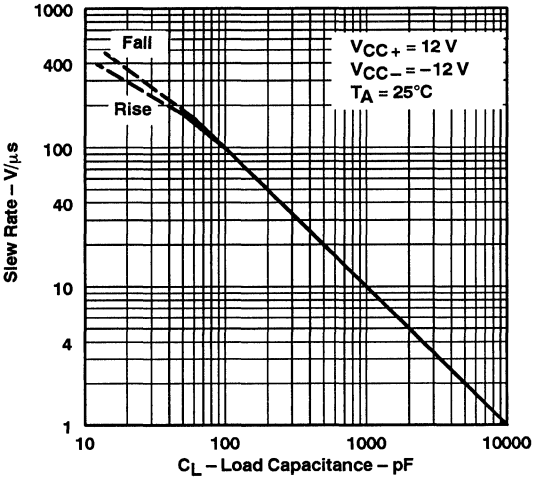


Figure 7

TYPICAL CHARACTERISTICS (RECEIVER)

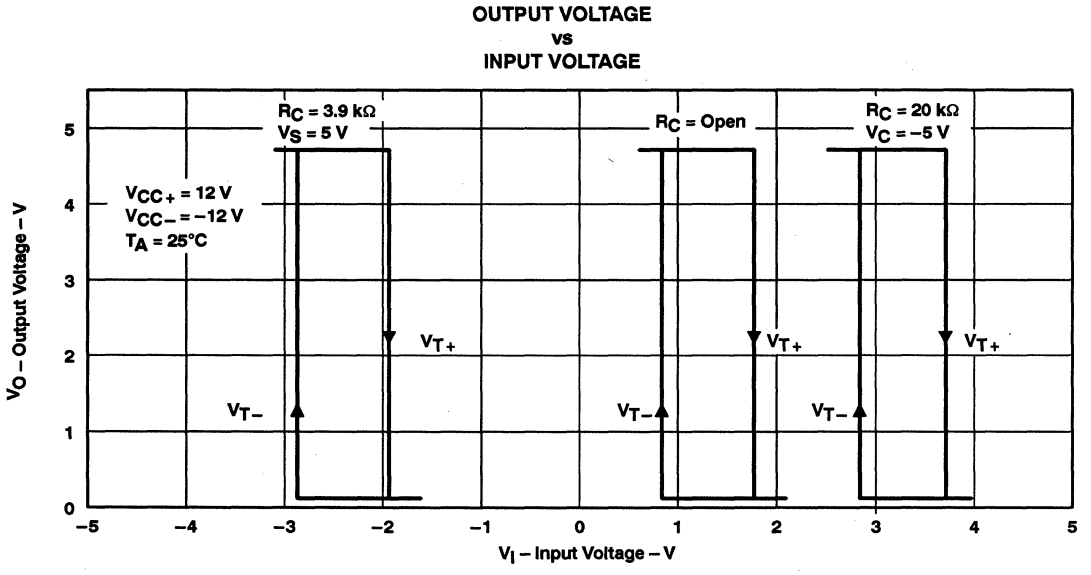


Figure 8

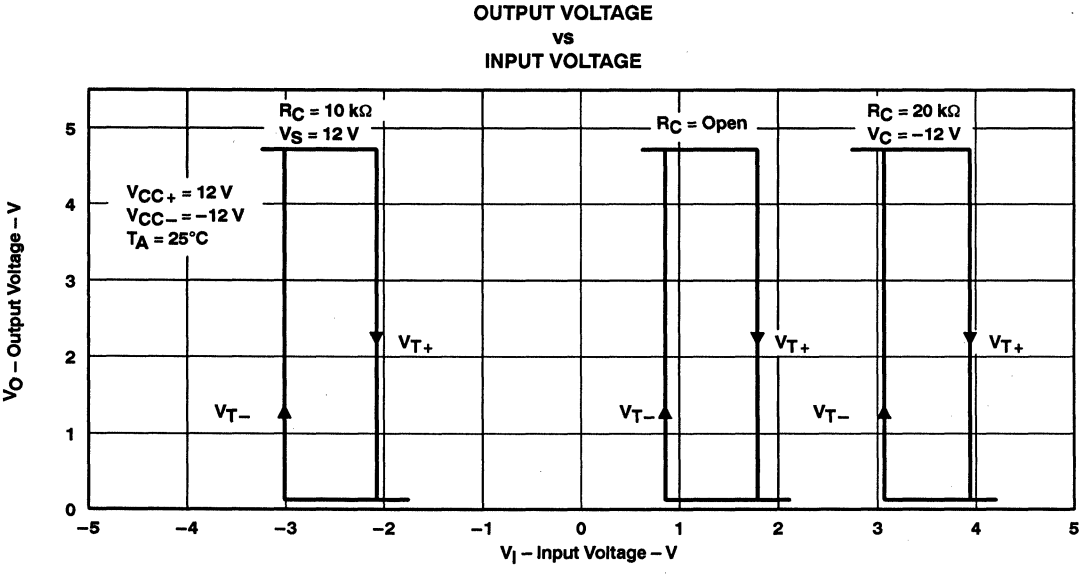


Figure 9

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TYPICAL CHARACTERISTICS (RECEIVER)

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

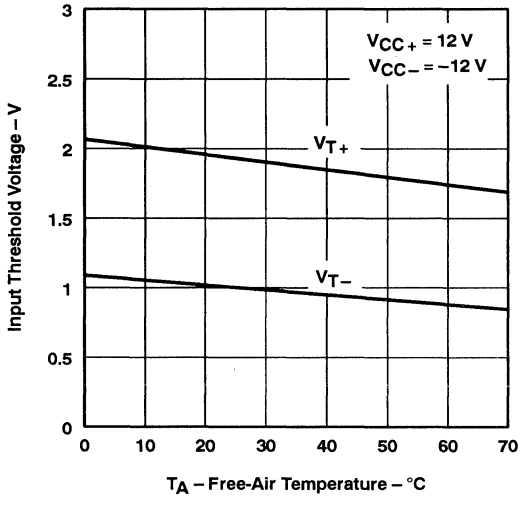


Figure 10

INPUT CURRENT vs INPUT VOLTAGE

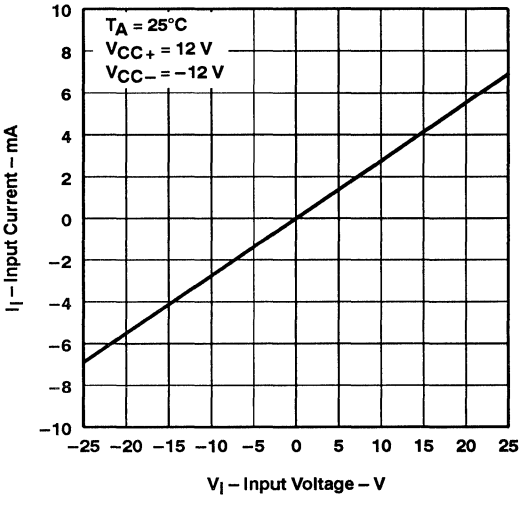


Figure 11

NOISE REJECTION

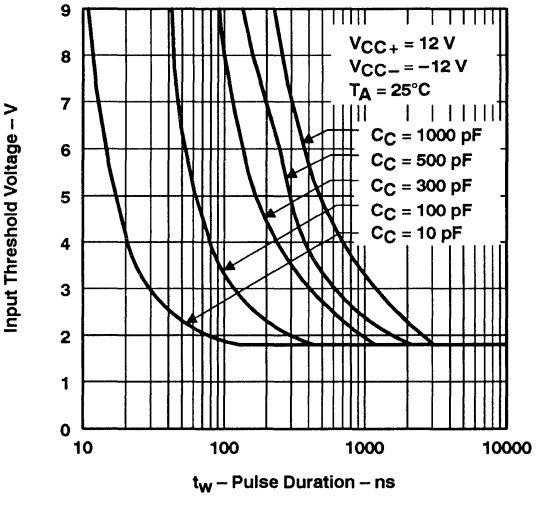


Figure 12

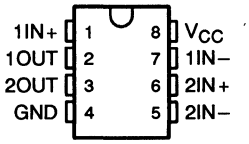
- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets Federal Standards 1020 and 1030**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line Package**
- **Similar to μA9637AC Except for Corner V_{CC} and GND Positions**

description

The SN75157 is a dual differential line receiver designed to meet EIA Standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5-V power supply and is supplied in an 8-pin dual-in-line package and small outline package.

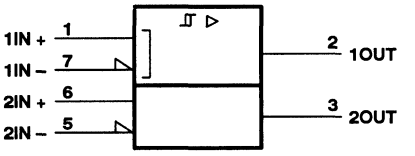
The SN75157 is characterized for operation from 0°C to 70°C.

D, P OR PS† PACKAGE
(TOP VIEW)



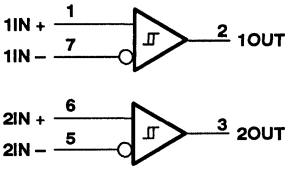
† The PS package is only available left-ended taped and reeled (order SN75157PSLE).

logic symbol‡

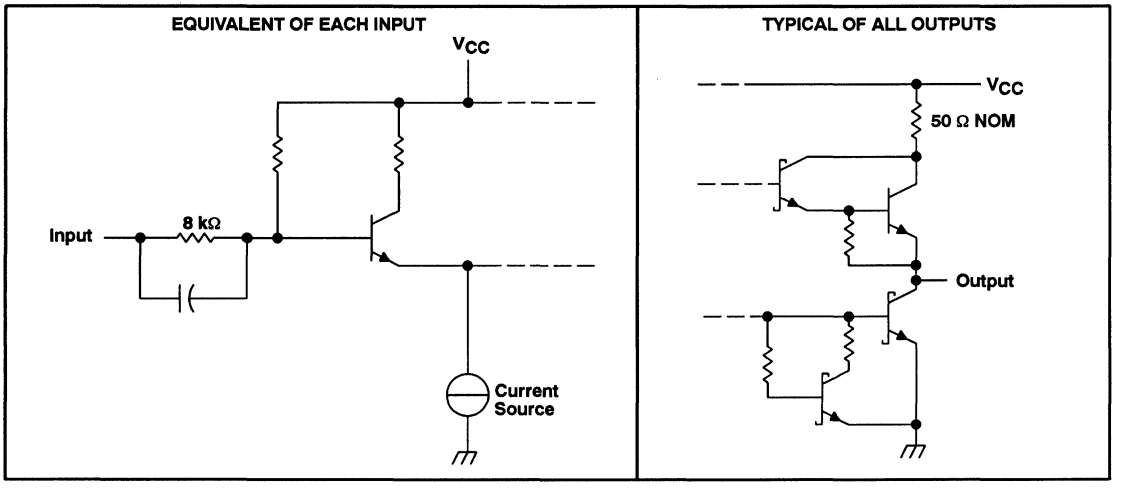


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Output voltage range (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)†

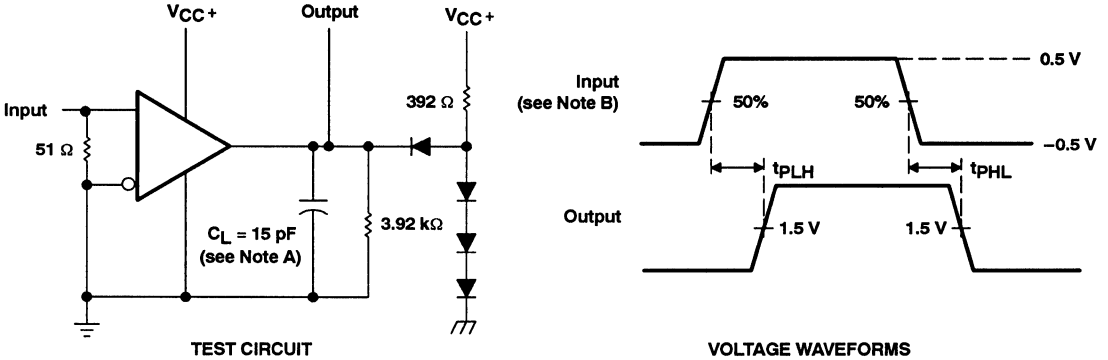
PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 3		−0.4		0.4	
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 4	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

† The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Only one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

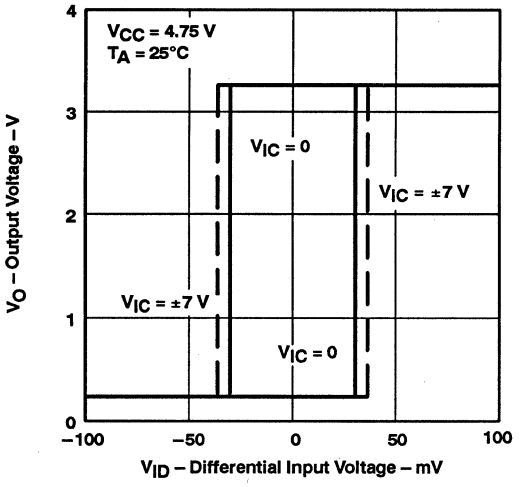


Figure 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

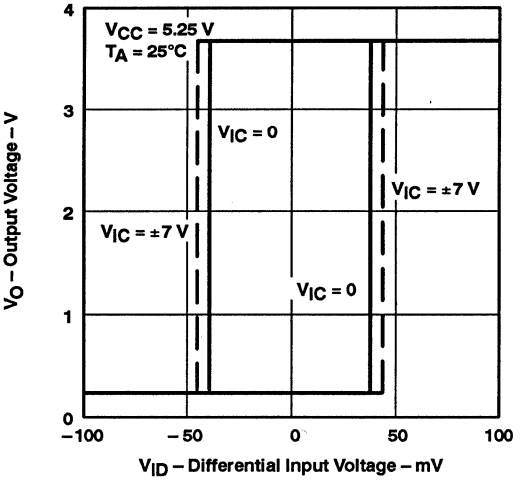


Figure 3

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

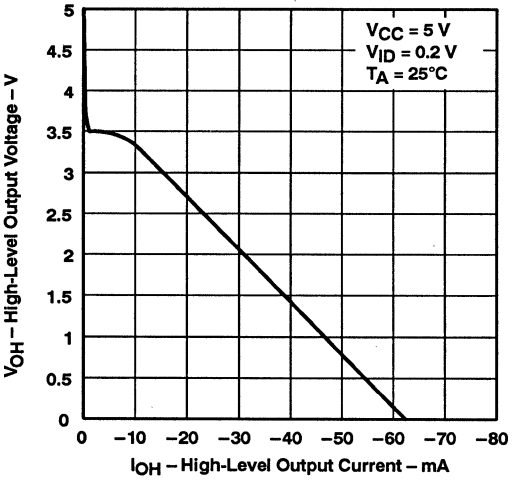


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

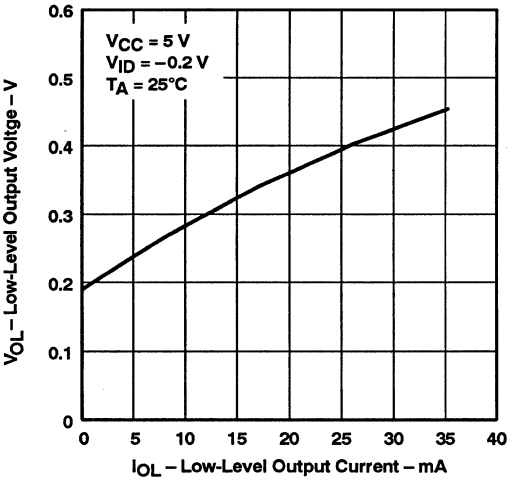


Figure 5

TYPICAL CHARACTERISTICS

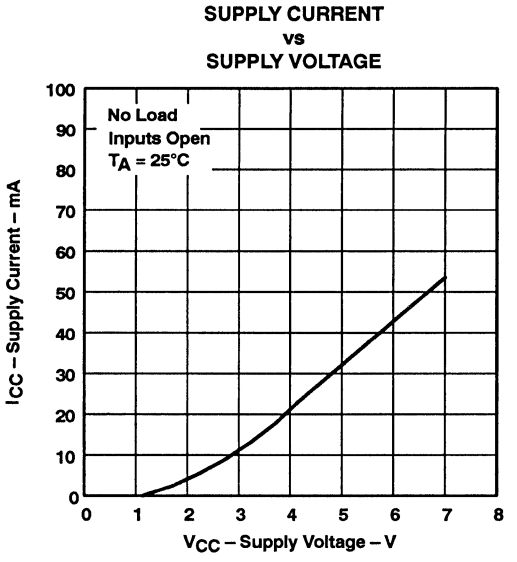


Figure 6

APPLICATION INFORMATION

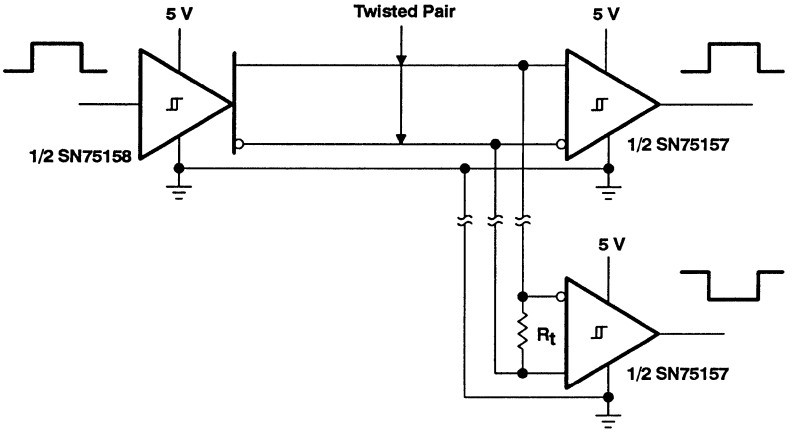
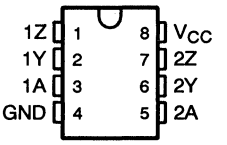


Figure 7. RS-422-A System Applications

SLLS085A – D2292, JANUARY 1977 – REVISED MARCH 1993

- **Meets EIA Standard RS-422-A**
- **Single 5-V Supply**
- **Balanced-Line Operation**
- **TTLCompatible**
- **High Output Impedance in Power-Off Condition**
- **High-Current Active-Pullup Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Input Clamp Diodes**

D, PS†, OR P PACKAGE
(TOP VIEW)



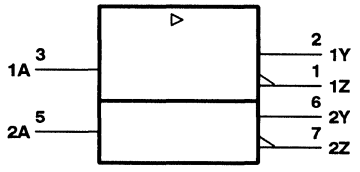
† The PS package is only available left-end taped and reeled, i.e., order SN75158PSLE.

description

The SN75158 is a dual differential line driver designed to satisfy the requirements set by the EIA Standard RS-422-A interface specifications. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

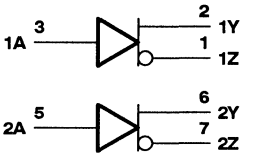
The SN75158 is characterized for operation from 0°C to 70°C.

logic symbol†

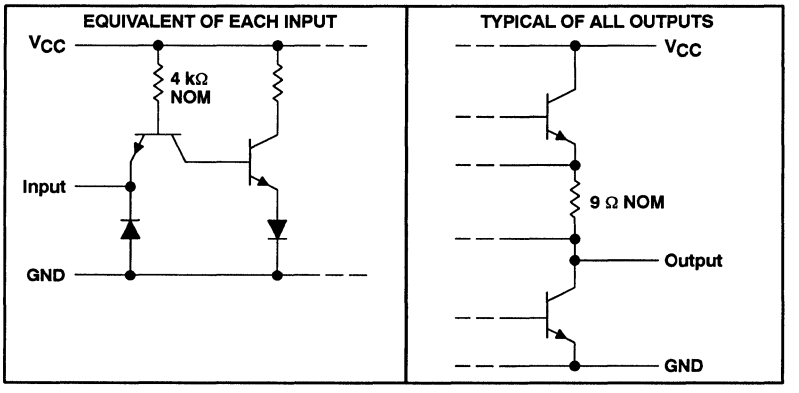


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values except differential output voltage V_{OD} are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA	2.4	3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.5	2 V_{OD2}	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	3		V
ΔV_{OD}	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.02	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.8	3	V
		V_{CC} = MIN			1.5	3	
ΔV_{OC}	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 to 6 V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load,	Inputs grounded, T_A = 25°C		37	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ ΔV_{OD} and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	See Figure 2, Termination A		4	20	ns
t_{TLH}	Transition time, high-to-low-level output			4	20	ns
	Overshoot factor	See Figure 2, Termination C			10%	

PARAMETER MEASUREMENT INFORMATION

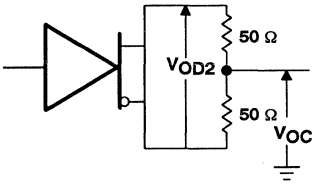
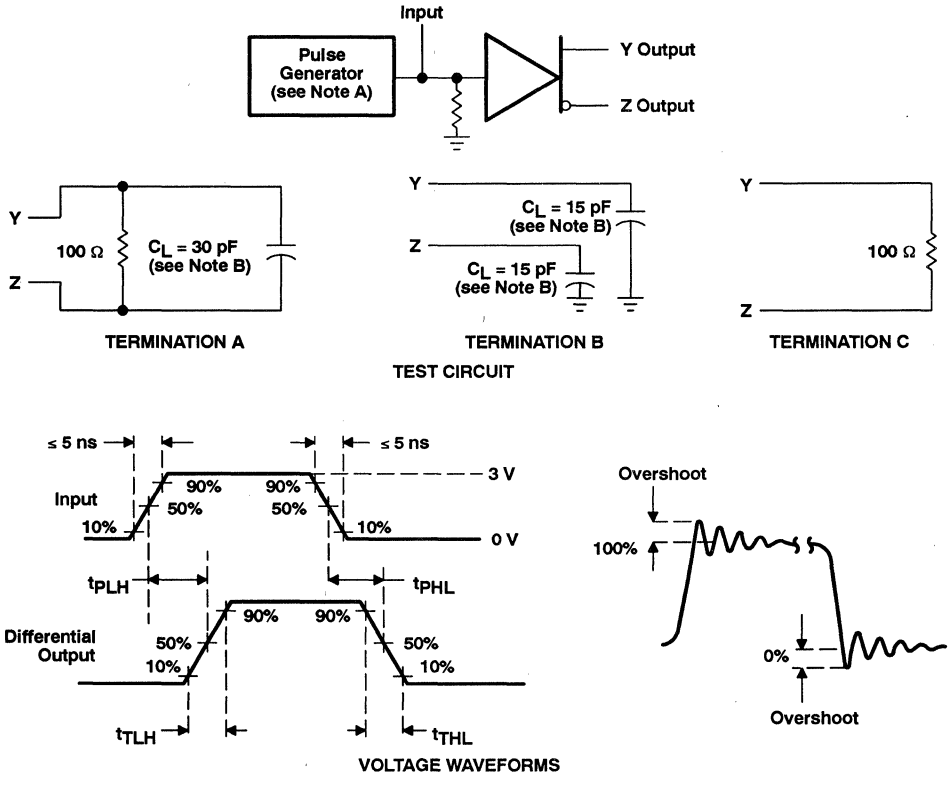


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 25 ns, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

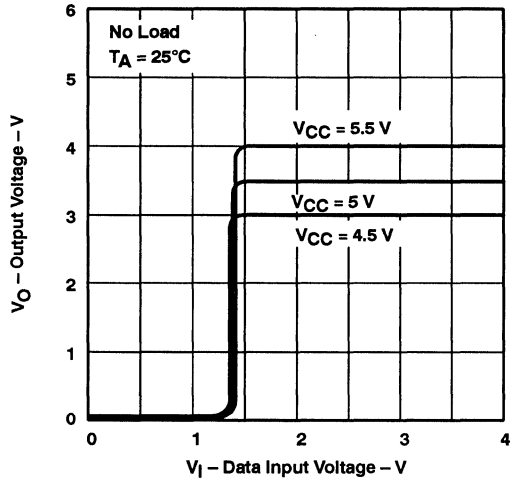


Figure 3

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

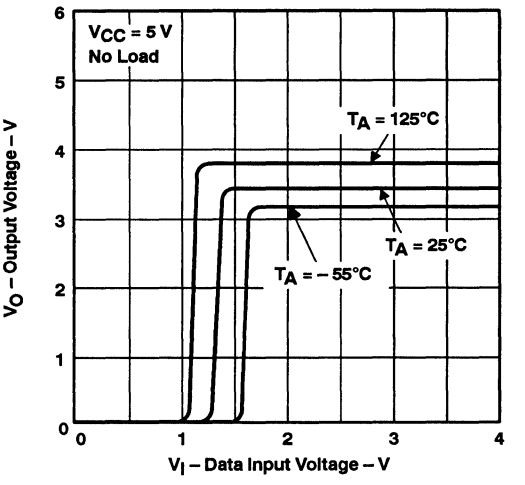


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

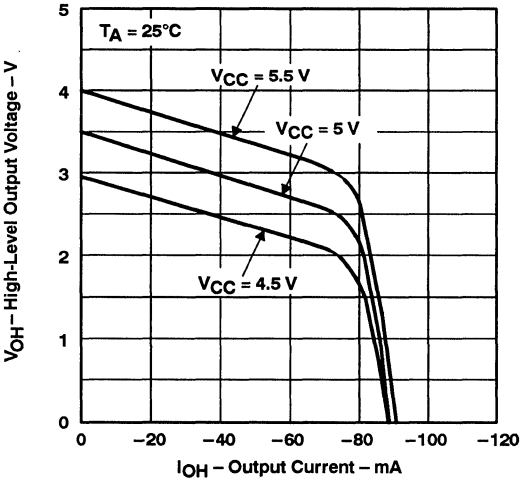


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

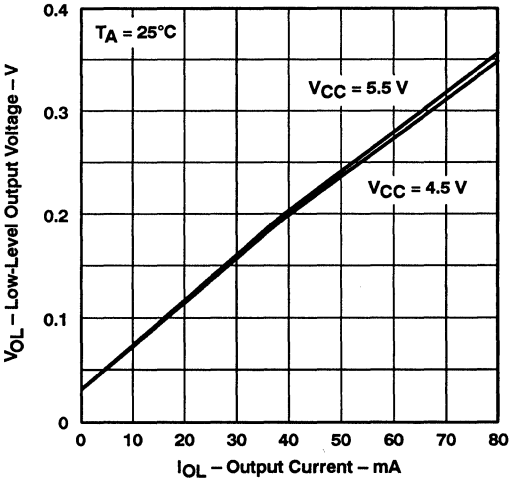


Figure 6

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

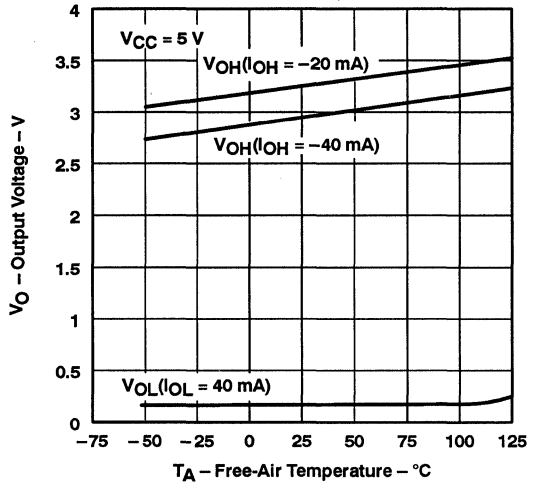


Figure 7

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

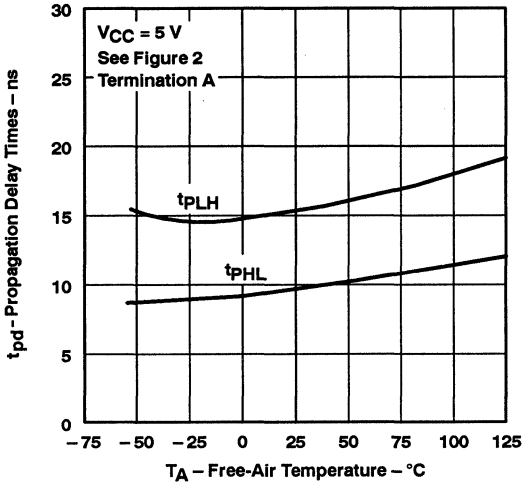


Figure 8

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

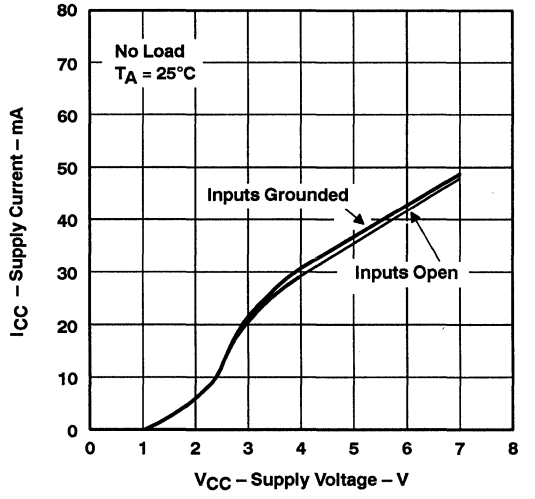


Figure 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

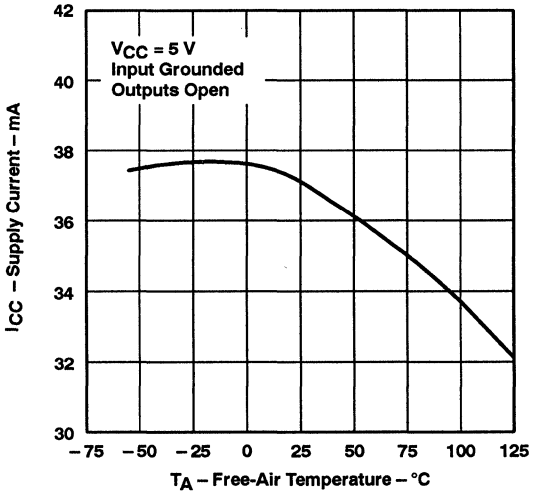


Figure 10

TYPICAL CHARACTERISTICS

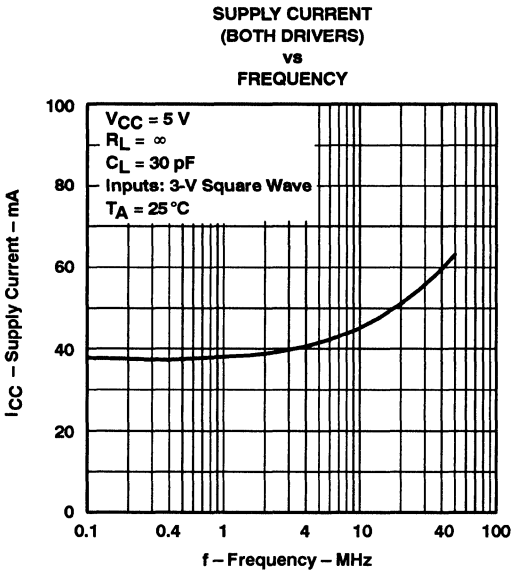
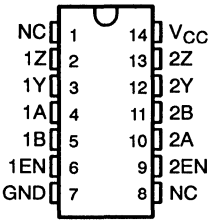


Figure 11

- **Meets EIA Standard RS-422-A**
- **Single 5-V Supply**
- **Balanced Line Operation**
- **TTL Compatible**
- **High-Impedance Output State for Party-Line Applications**
- **High-Current Active-Pullup Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Clamp Diodes at Inputs**

D OR N PACKAGE
(TOP VIEW)



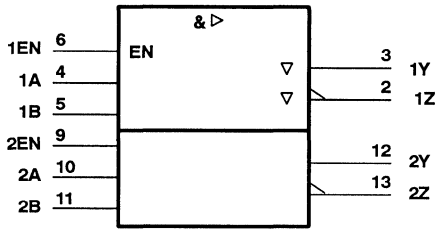
NC – No internal connection

description

The SN75159 dual differential line driver with 3-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

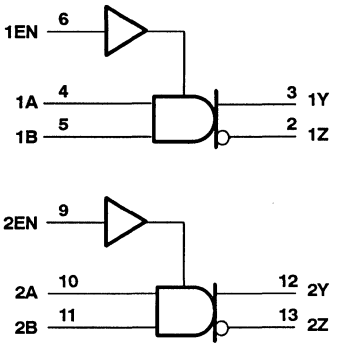
The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†

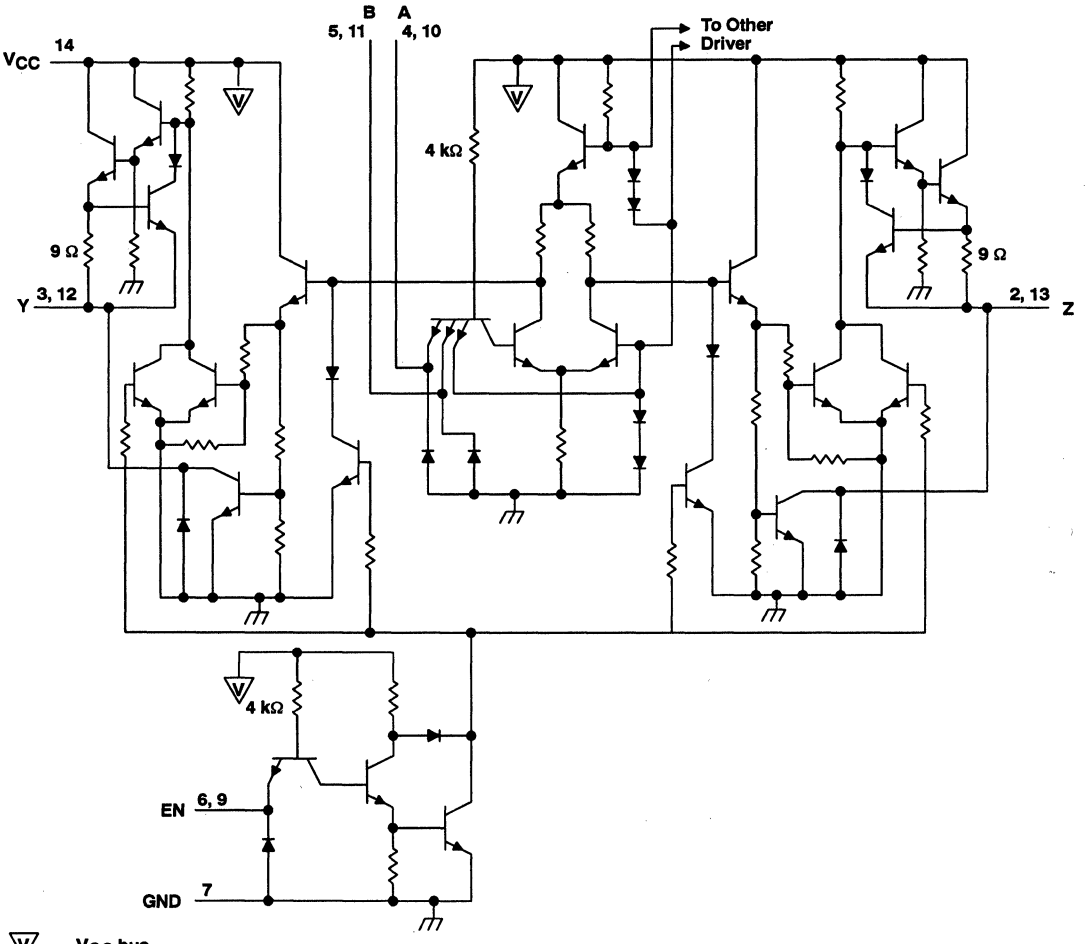


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



▽ . . . V_{CC} bus

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Off-state voltage applied to open-collector outputs ..... 12 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values except differential output voltage V_{OD} are with respect to the network ground terminal. V_{OD} is at the Y output with respect to the Z output.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output voltage, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA		2.4	3		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = 5.25 V,	I_O = −40 mA			−1.1	−1.5	V
V_O	Output voltage	V_{CC} = 4.75 V to 5.25 V,	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = 5.25 V,	I_O = 0			3.5	$\frac{2V_{OD}}{2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = 4.75 V			2	3		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	V_{CC} = 4.75 V	R_L = 100 Ω, See Figure 1			±0.02	±0.4	V
V_{OC}	Common-mode output voltage§	V_{CC} = 5.25 V				1.8	3	V
		V_{CC} = 4.75 V				1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡	V_{CC} = 4.75 V to 5.25 V				±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	μA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.25 V, Output controls at 0.8 V	T_A = 25°C	V_O = 0 to V_{CC}			±10	μA
			T_A = 70°C	V_O = 0			−20	
				V_O = 0.4 V			±20	
				V_O = 2.4 V			±20	
				V_O = V_{CC}			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, No load,	Inputs grounded, T_A = 25°C			47	65	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
¶ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, ,R_L = 100 Ω, See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10%	

† All typical values are at T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

PARAMETER MEASUREMENT INFORMATION

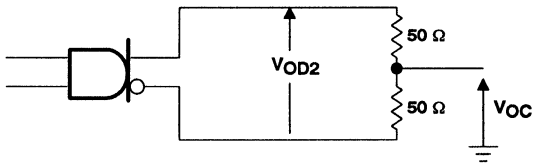
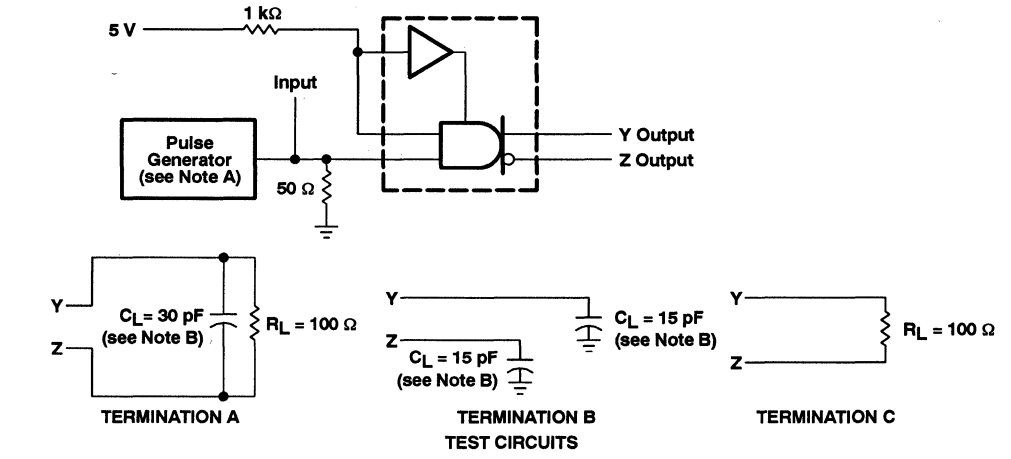
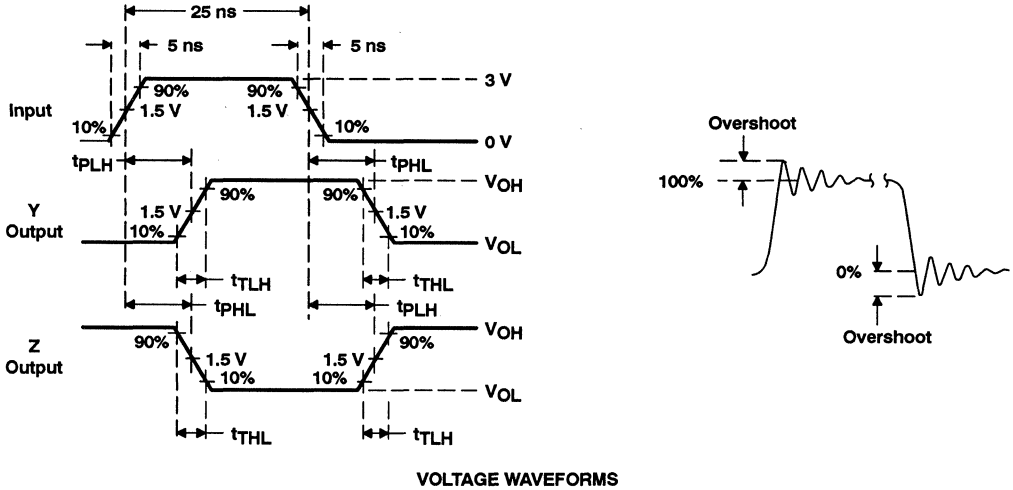


Figure 1. Differential and Common-Mode Output Voltages

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuits, Voltage Waveforms, and Overshoot Factor

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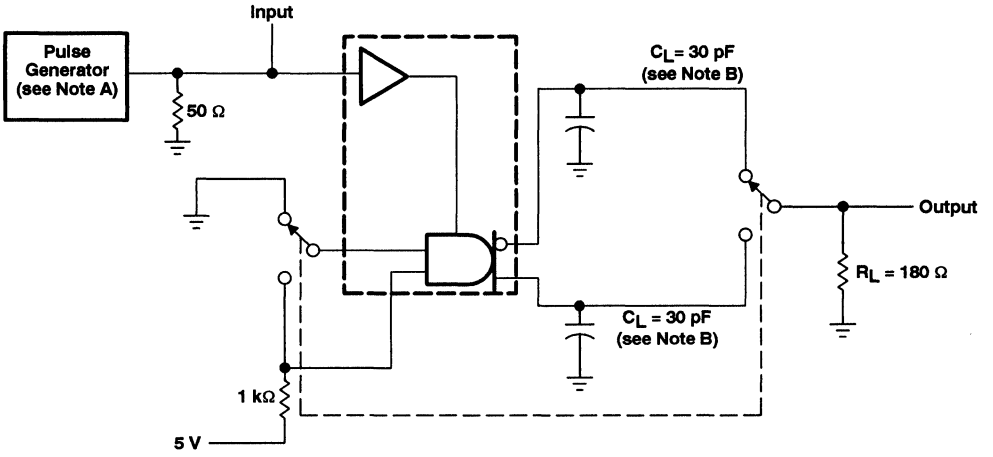
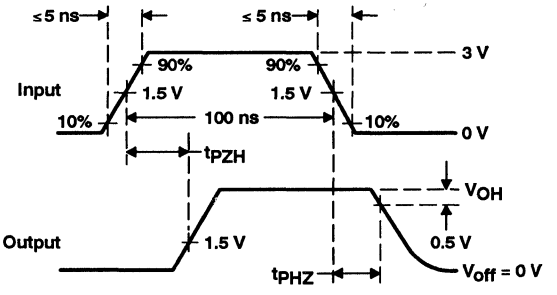
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

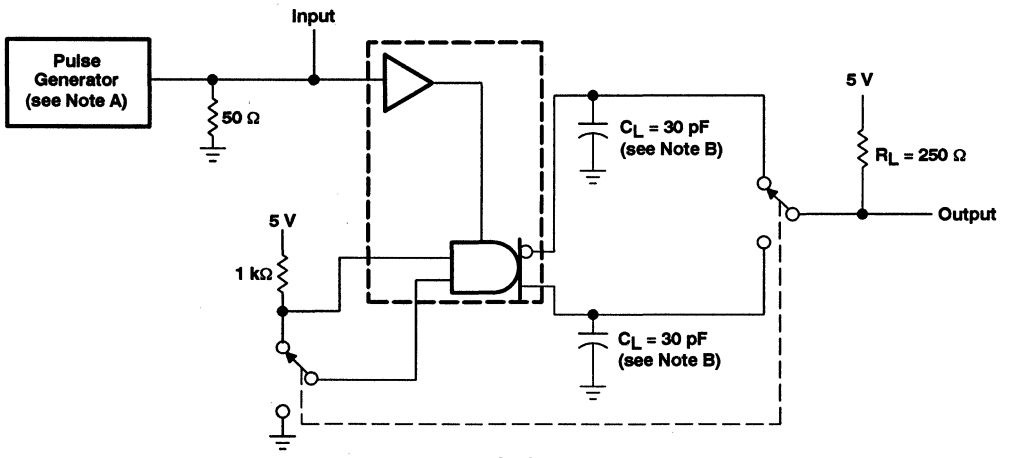


VOLTAGE WAVEFORMS

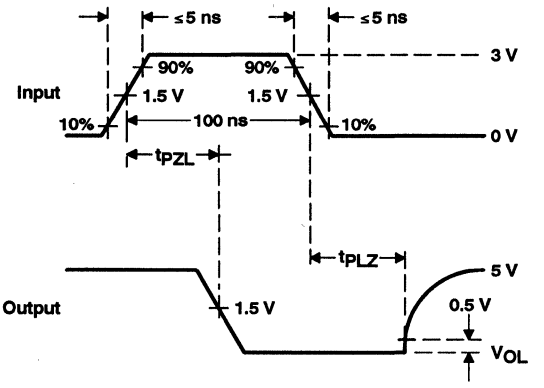
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltge Waveform

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

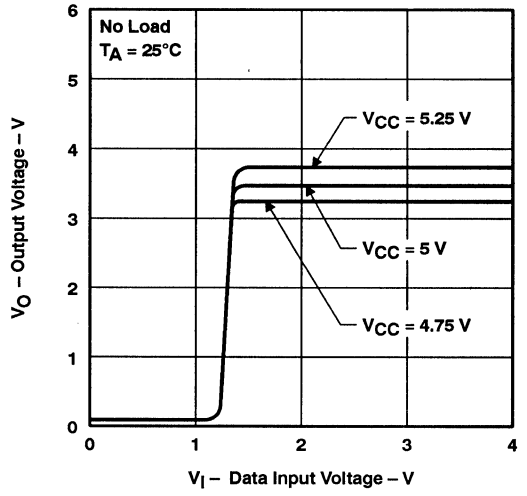


Figure 5

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

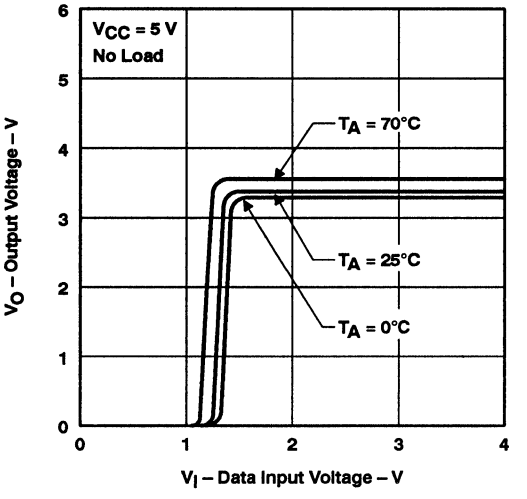


Figure 6

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

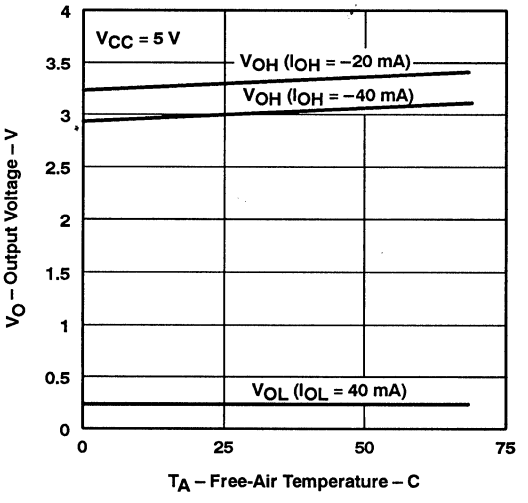


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

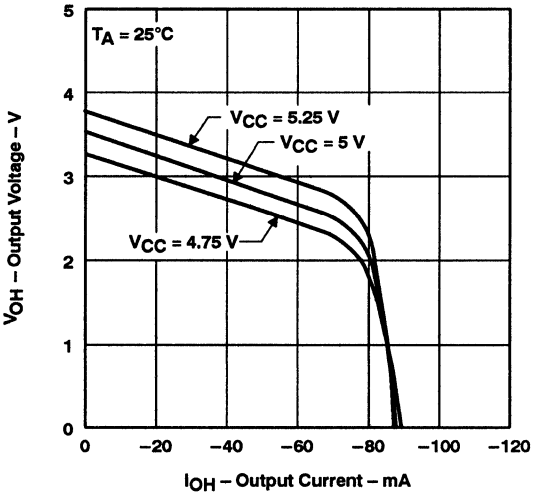


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

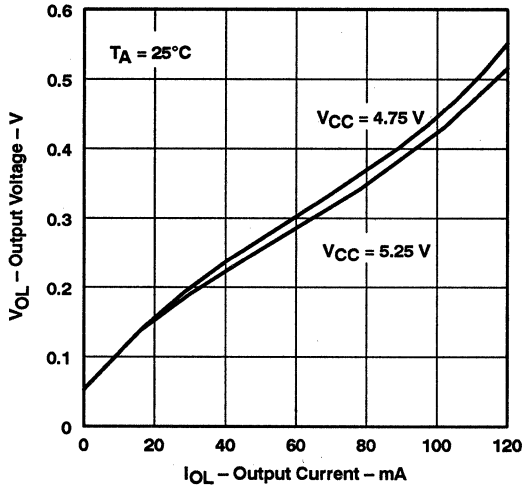


Figure 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

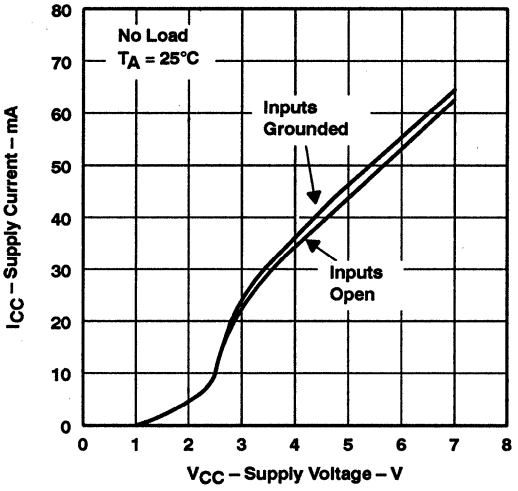


Figure 10

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

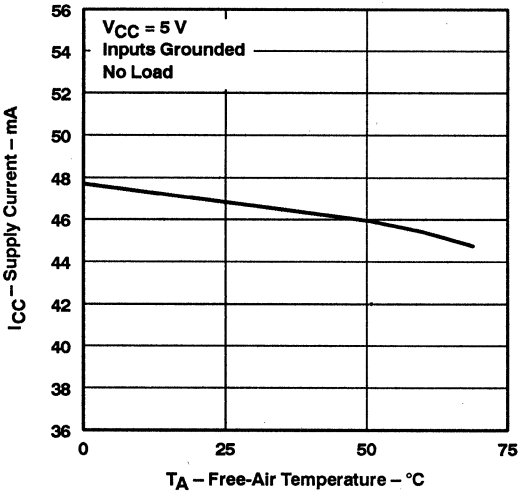


Figure 11

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

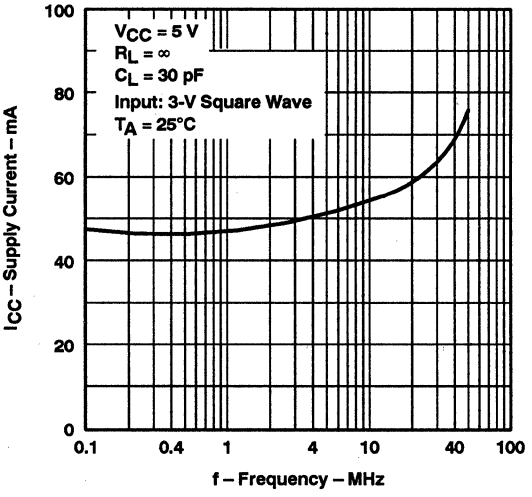


Figure 12

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

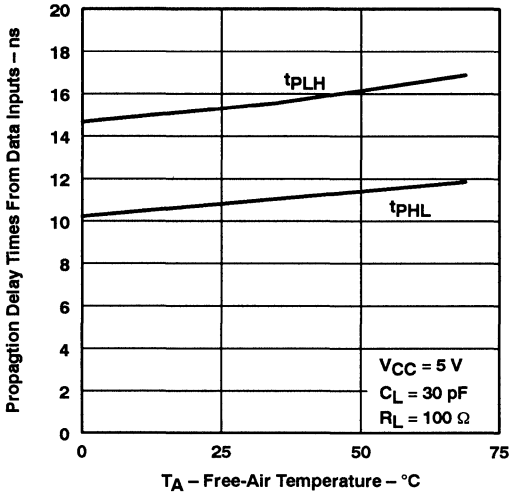


Figure 13

OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE

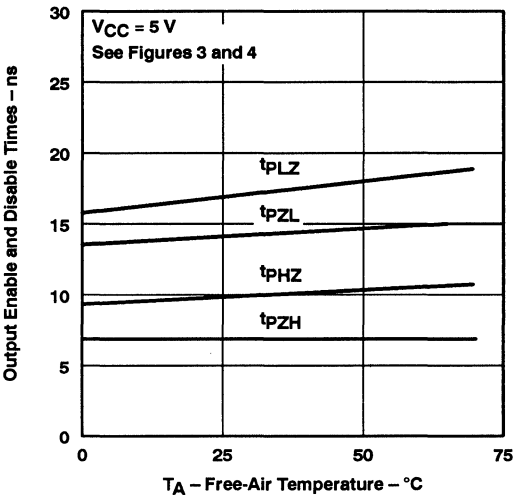
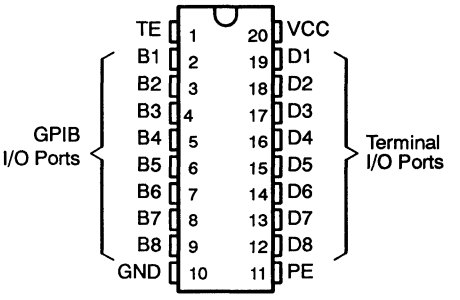


Figure 14

MEETS IEEE STANDARD 488-1978 (GPIB)

- **8-Channel Bidirectional Transceiver**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **High-Speed, Low-Power Schottky Circuitry**
- **Low-Power Dissipation . . . 72 mW Max Per Channel**
- **Fast Propagation Times . . . 22 ns Max**
- **High-Impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

DW OR N PACKAGE
(TOP VIEW)



description

The SN75160B 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low, and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

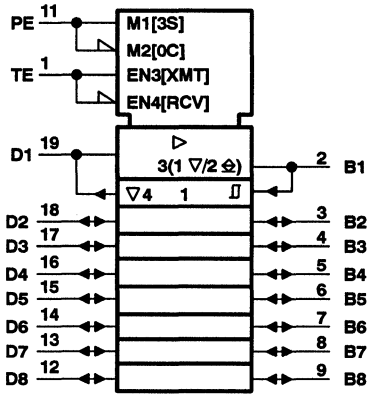
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high-impedance state

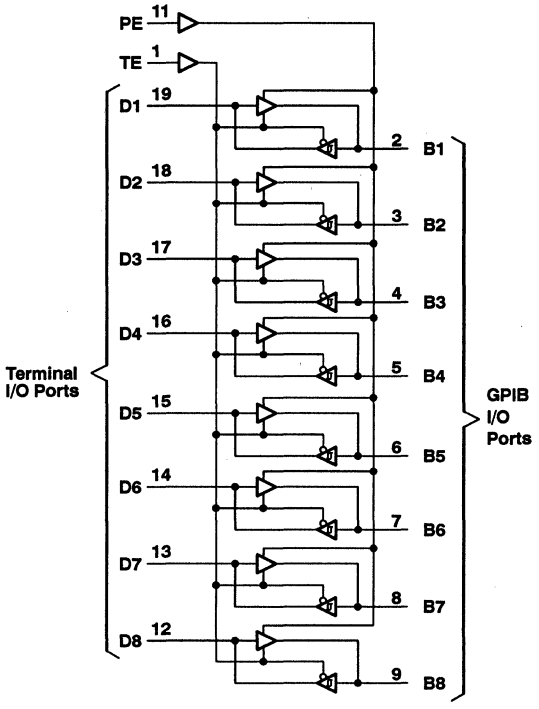
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

logic symbol†



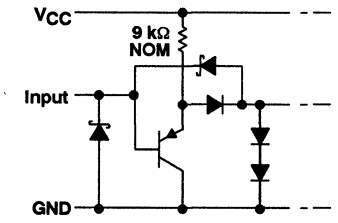
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏚ Designates passive-pullup outputs

logic diagram (positive logic)

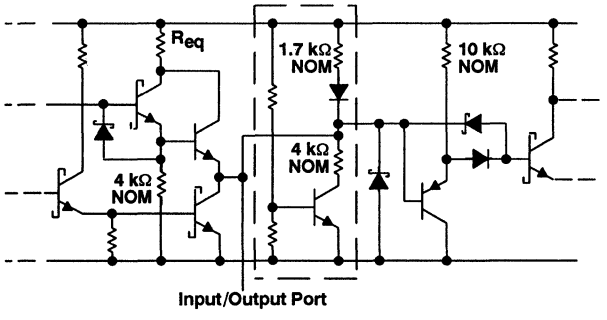


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	µA
High-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	See Figure 8		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			−40	
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propation delay time, low-to-high level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					14	20	
t_{PLH}	Propagation delay time, low-to-high level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					15	22	
t_{PZH}	Output enable time to high level	TE	BUS	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pullup enable time	PE	Bus	See Figure 5		15	22	ns
t_{dis}	Output pullup disable time					13	20	

PARAMETER MEASUREMENT INFORMATION

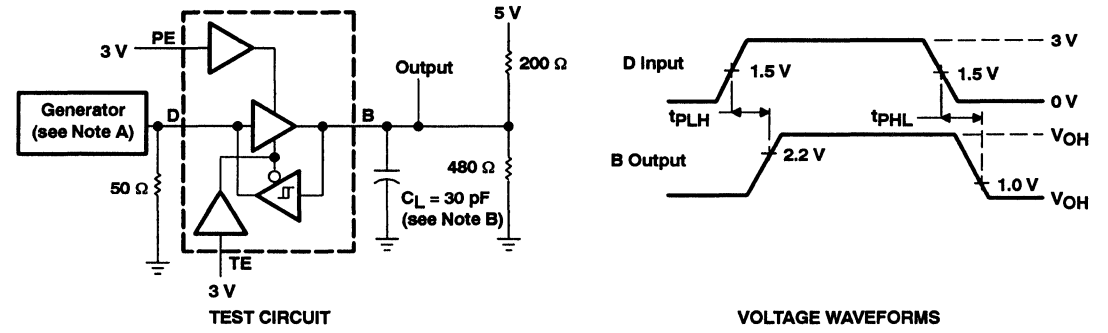


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

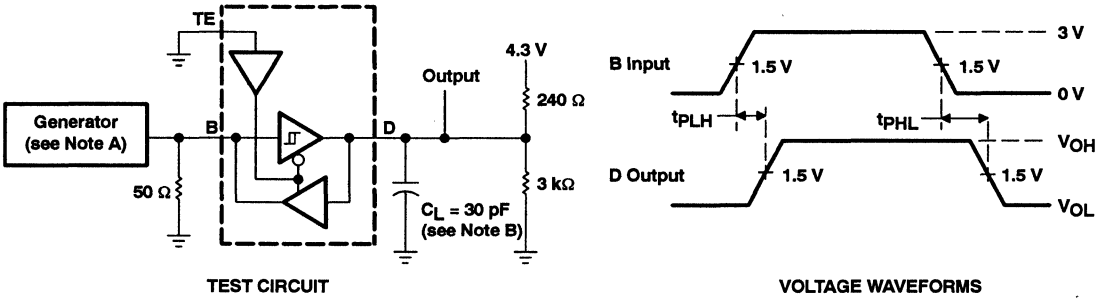


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

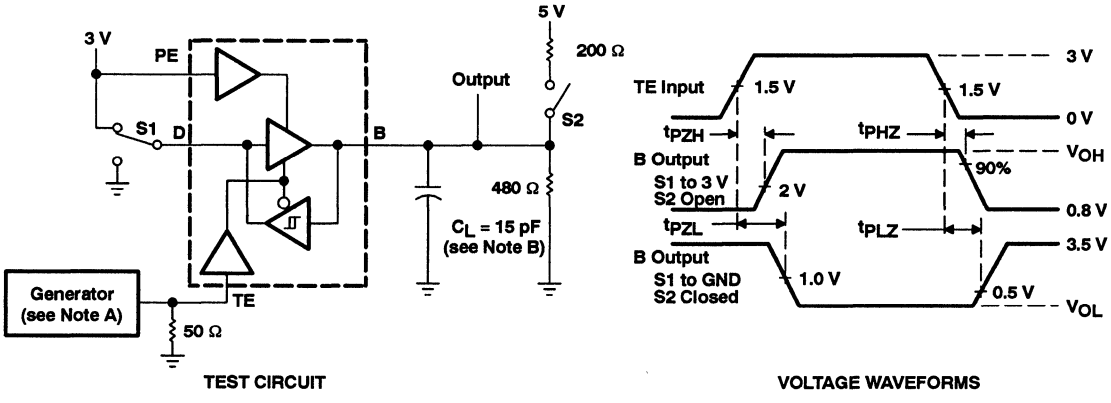


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

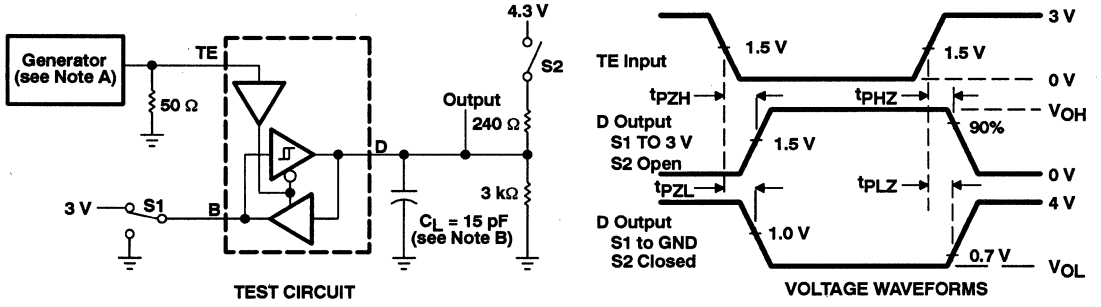


Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

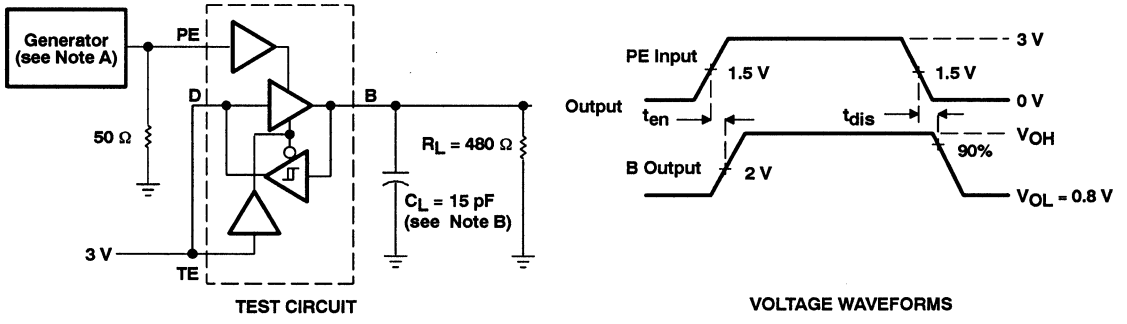


Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

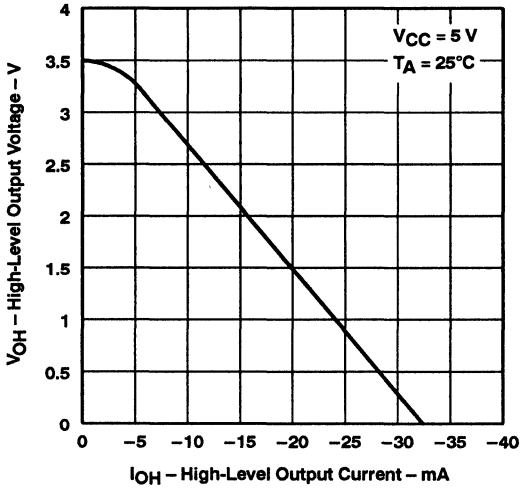


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

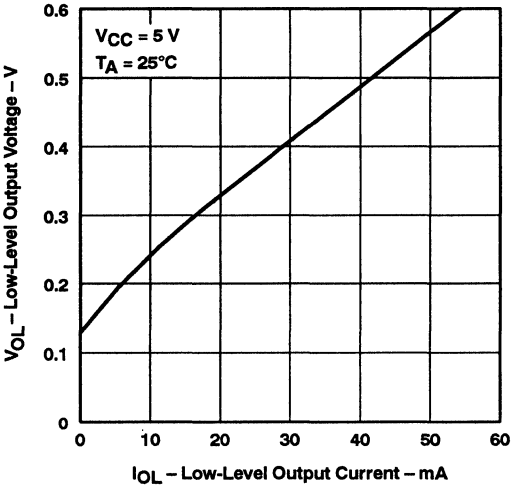


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

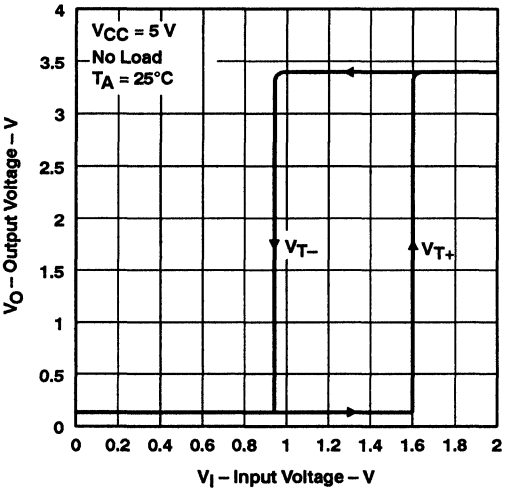


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

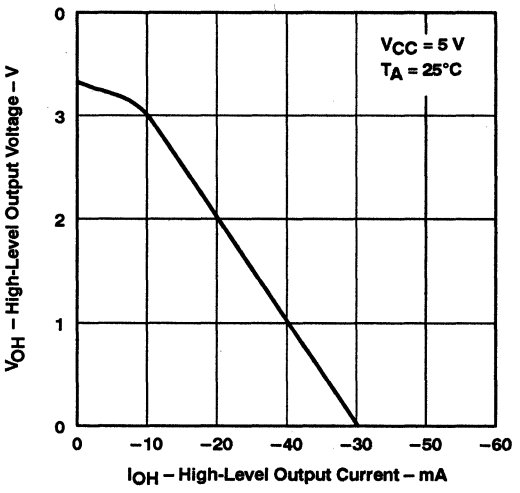


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

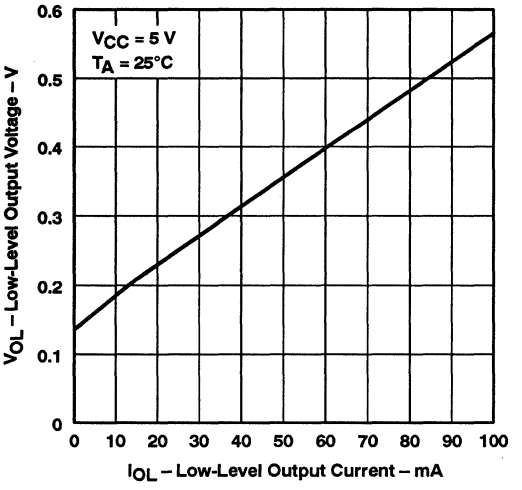


Figure 10

BUS OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

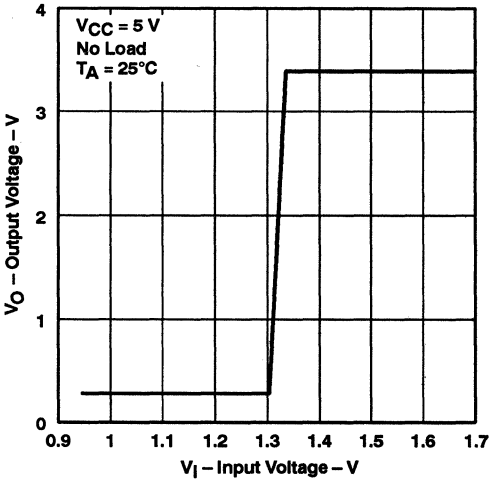


Figure 11

BUS CURRENT
vs
BUS VOLTAGE

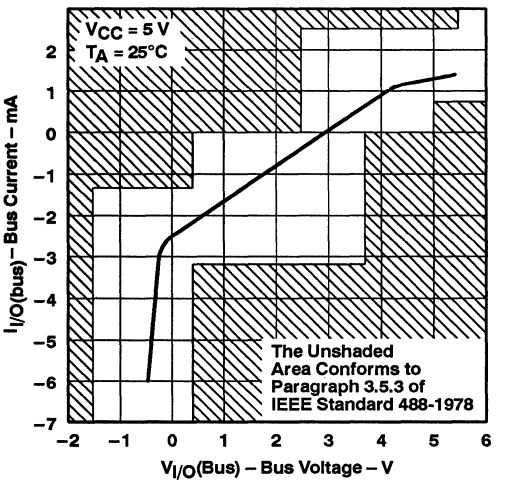


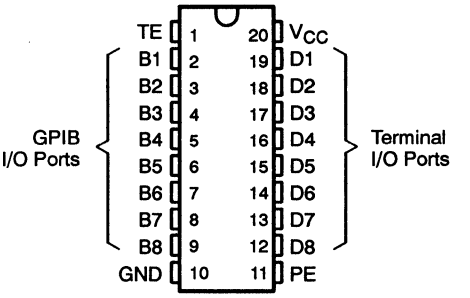
Figure 12

SLLS018C – D2525, JUNE 1986 – REVISED FEBRUARY 1993

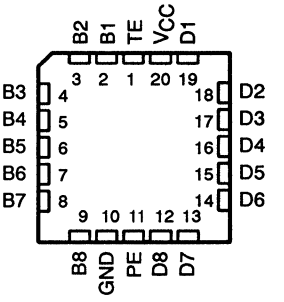
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation:
  - SN55ALS160 . . . 56 mW Max Per Channel
  - SN75ALS160 . . . 46 mW Max Per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance PNP Inputs
- Receiver Hysteresis:
  - SN55ALS160 . . . 550 mV Typ
  - SN75ALS160 . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch Free)

SN55ALS160 . . . J OR W PACKAGE
SN75ALS160 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS160 . . . FK PACKAGE
(TOP VIEW)



description

The SN55ALS160 and SN75ALS160 eight-channel general-purpose interface bus transceivers are monolithic, high-speed, advanced low-power Schottky devices designed for two-way data communications over single-ended transmission lines. They are designed to meet the requirements of IEEE Standard 488-1978. The transceivers feature driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low, and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN55ALS161, SN75ALS161, or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN55ALS160 is characterized for operation from −55°C to 125°C. The SN75ALS160 is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z‡
X	L	X	Z‡

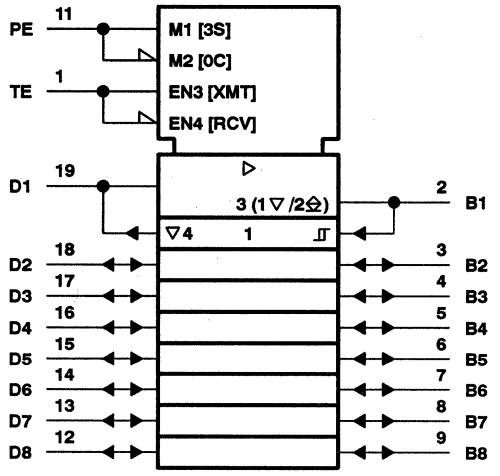
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant,
Z = high-impedance state
‡ This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

logic symbol†

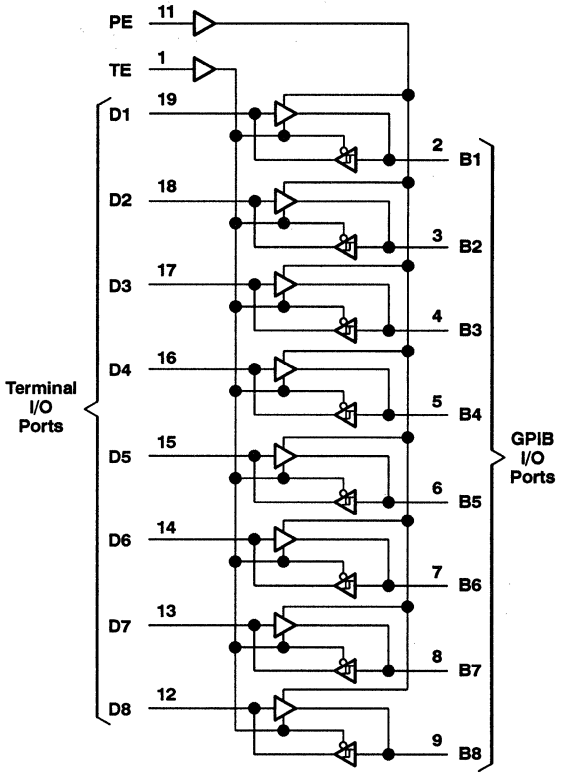


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

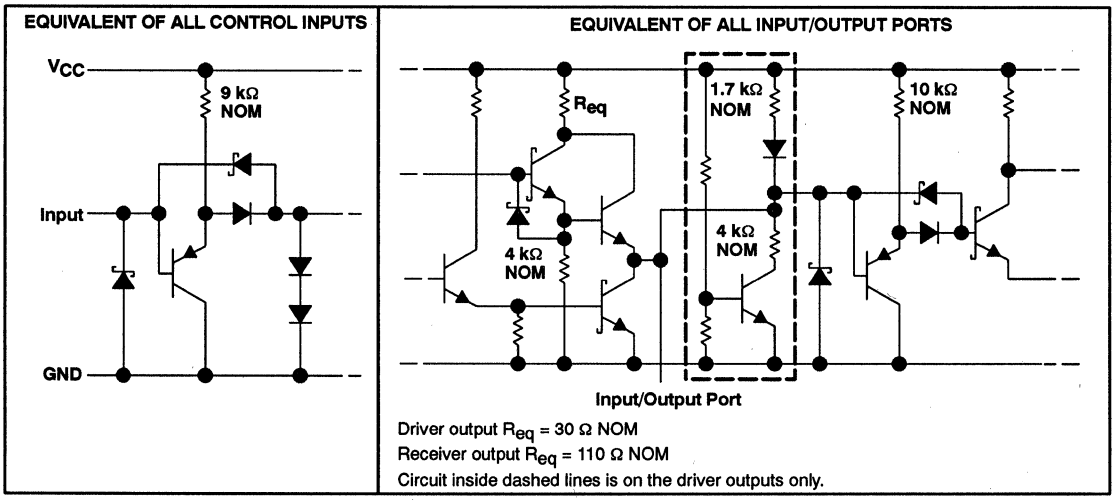
▽ Designates 3-state outputs

◇ Designates open-collector outputs

logic diagram (positive logic)



schematics of inputs and outputs



Driver output R_{eq} = 30 Ω NOM

Receiver output R_{eq} = 110 Ω NOM

Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55ALS160 ..... −55°C to 125°C
SN75ALS160 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package ..... 300°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS160 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and PE at $T_A = -55°C$ to 125°C	2			V
	Bus and terminal at $T_A = 25°C$ to 125°C	2			
	Bus and terminal at $T_A = -55°C$	2.1			
Low-level input voltage, V_{IL}	TE and PE at $T_A = -55°C$ to 125°C			0.8	V
	Bus and terminal at $T_A = 25°C$ to −55°C			0.8	
	Bus and terminal at $T_A = 125°C$			0.7	
High-level output current, I_{OH}	Bus ports with pullups active ($V_{CC} = 5$ V)			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		−55		125	°C

SN75ALS160 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55ALS160			SN75ALS160			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		I_I = −18 mA,	V_{CC} = MIN		−0.8	−1.5		−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus						0.4	0.65		V
		Bus	V_{CC} = 5 V,	T_A = −55°C and 25°C	0.4	0.55					
			V_{CC} = 5 V,	T_A = 125°C	0.25						
V_{OH}§	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V, V_{CC} = MIN	2.7	3.5		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V, V_{CC} = MIN	2.5	3.3		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V, V_{CC} = MIN		0.3	0.5		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V, V_{CC} = MIN		0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V,	V_{CC} = MAX		0.2	100		0.2	100	μA
I_{IH}	High-level input current	Terminal, PE, or TE	V_I = 2.7 V,	V_{CC} = MAX		0.1	20		0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V,	V_{CC} = MAX		−30	−100		−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled, V_{CC} = 5 V (SN55')	$I_{I(bus)}$ = 0	2.5	3	3.7	2.5	3	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled, V_{CC} = 5 V (SN55')	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5 −3.2			2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V			40			40	μA
I_{OS}	Short-circuit output current	Terminal	V_{CC} = MAX		−15	−35	−75	−15	−35	−75	mA
		Bus	V_{CC} = MAX		−25	−50	−125	−25	−50	−125	
I_{CC}	Supply current		No load, V_{CC} = MAX	Terminal outputs low and enabled		42	56		42	65	mA
				Bus outputs low and enabled		52	85		52	80	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30			30		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} applies to 3-state outputs only.

TEXAS INSTRUMENTS
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switching characteristics at V_{CC} = 4.75 V, 5 V, and 5.25 V, C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	See Figure 2	25°C		8	15	ns
					Full range			18	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		8	15	
					Full range			18	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3	25°C		24	30	ns
					Full range			41	
t_{PHZ}	Output disable time from high level				25°C		9	14	
					Full range			16	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t_{PLZ}	Output disable time from low level				25°C		12	19	
					Full range			24	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t_{PHZ}	Output disable time from high level				25°C		10	18	
					Full range			23	
t_{PZL}	Output enable time to low level				25°C		15	26	
					Full range			30	
t_{PLZ}	Output disable time from low level				25°C		15	24	
					Full range			31	
t_{en}	Output pullup enable time	PE	Bus	See Figure 5	25°C		16	24	ns
					Full range			25	
t_{dis}	Output pullup disable time				25°C		9	16	
					Full range			20	

† Full range is −55°C to 125°C.
‡ All typical values are at V_{CC} = 5 V.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pullup enable time	PE	Bus	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pullup disable time					6	12	

† Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

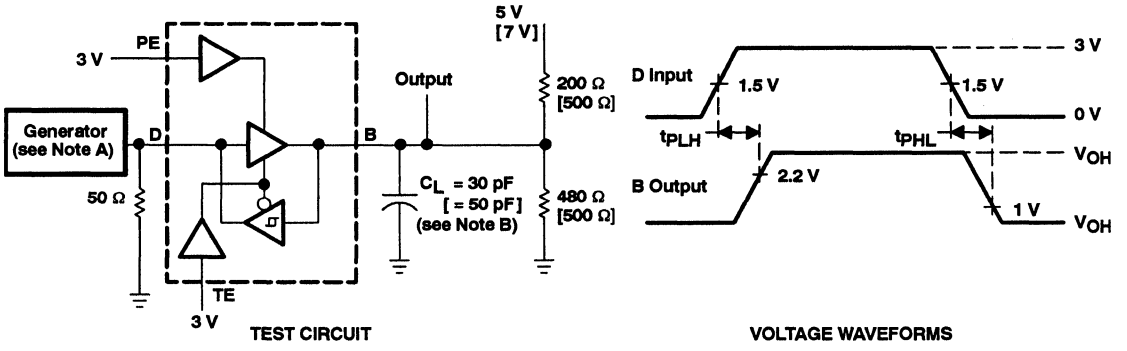


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

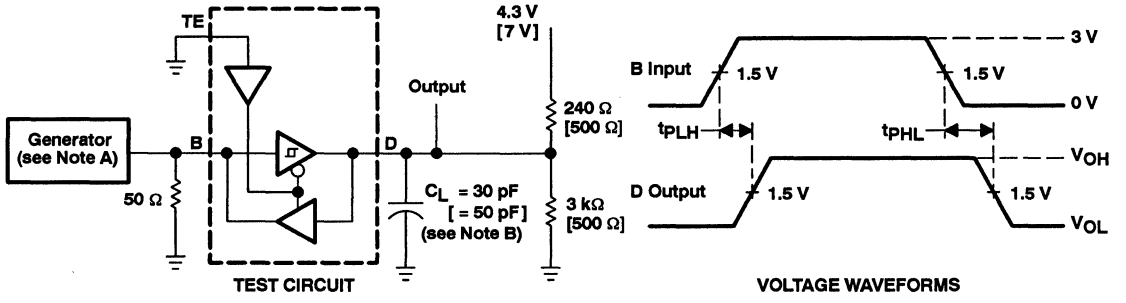


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

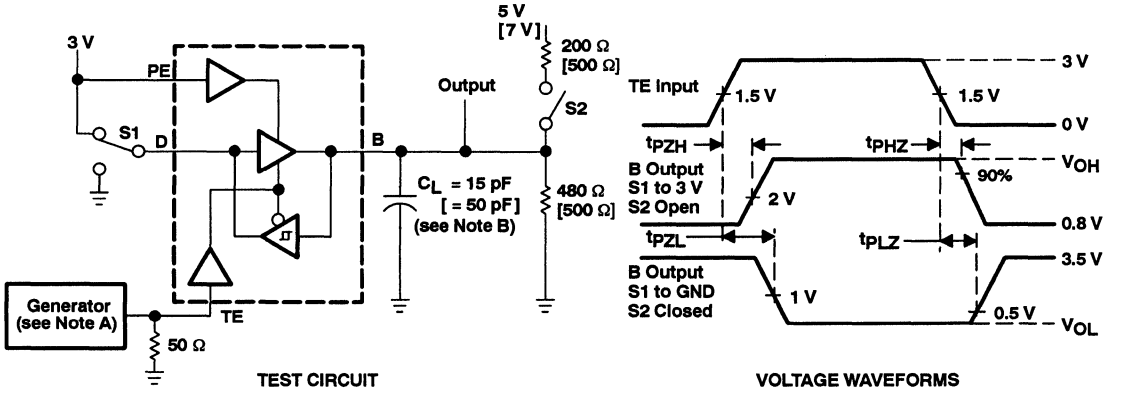


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

[ ] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

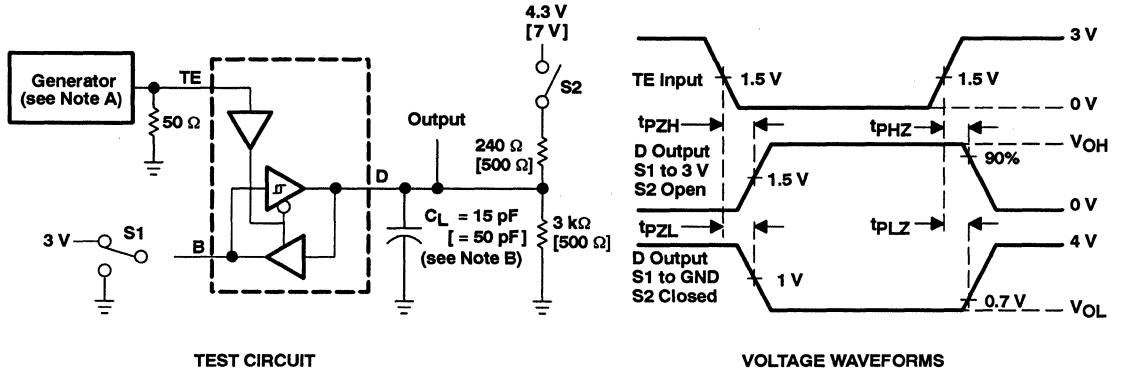


Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

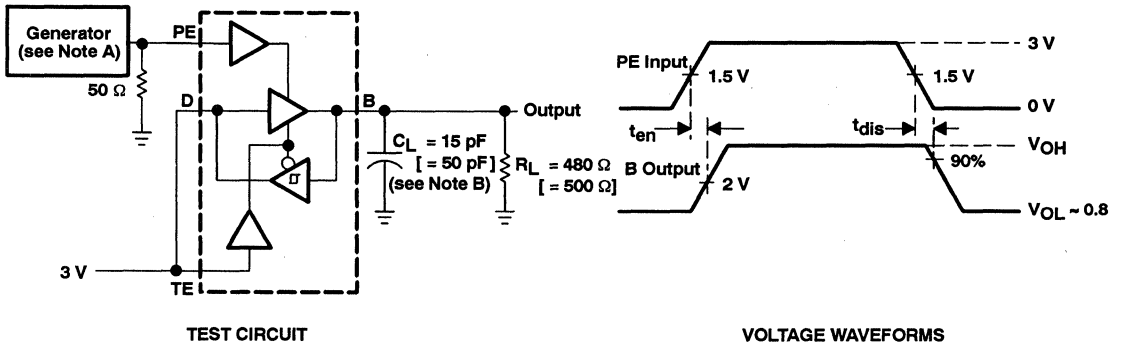


Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

[ ] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

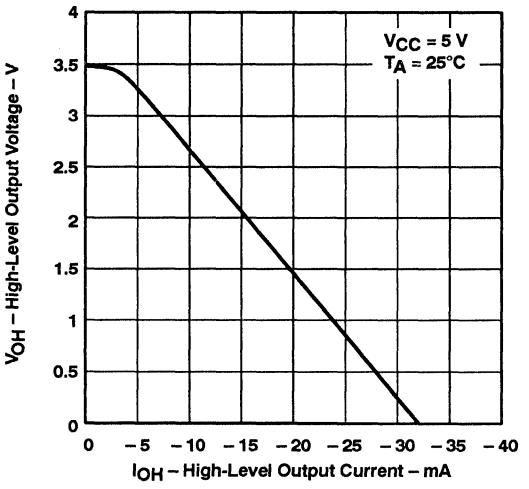


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

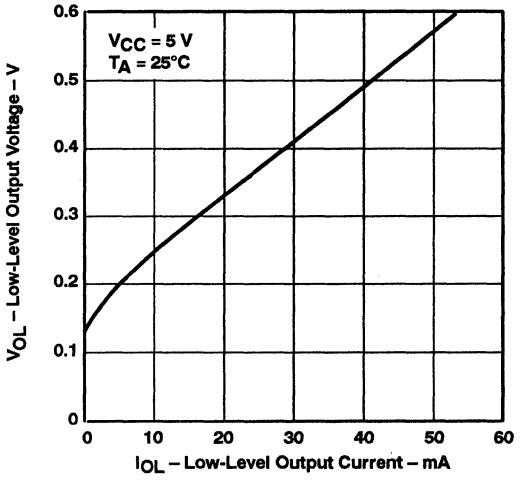


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

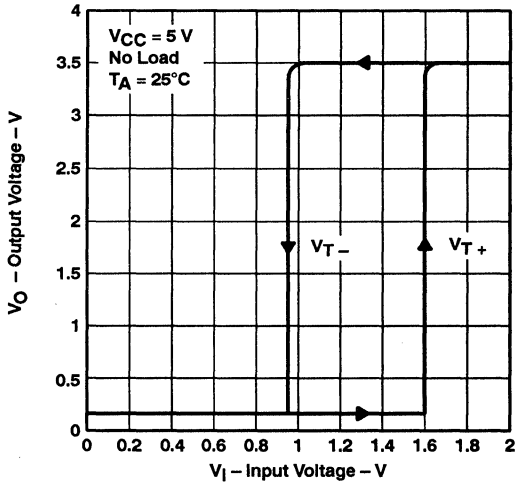


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

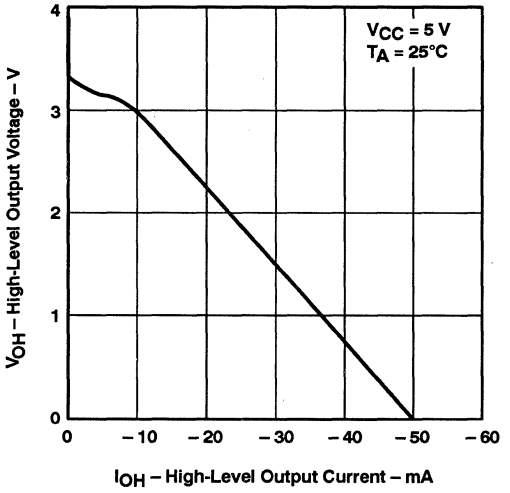


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

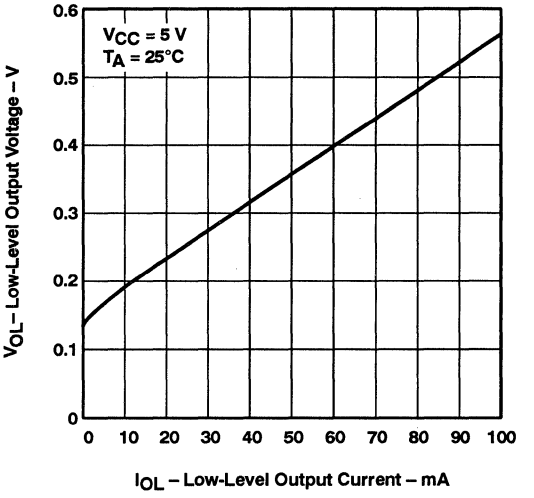


Figure 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

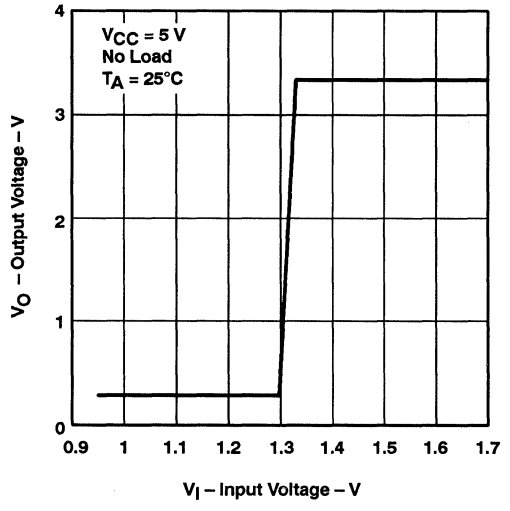


Figure 11

BUS CURRENT
vs
BUS VOLTAGE

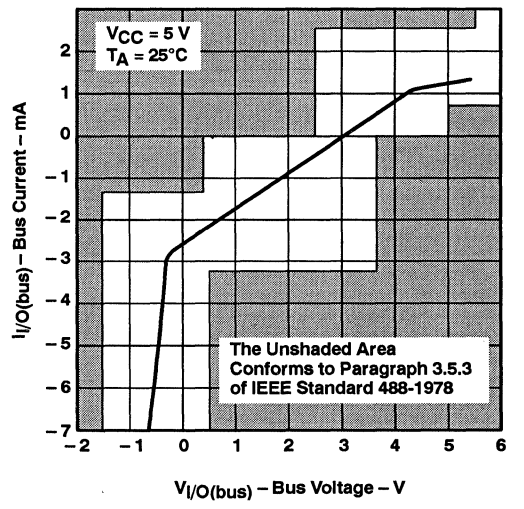


Figure 12

MEETS IEEE STANDARD 488-1978 (GPIB)

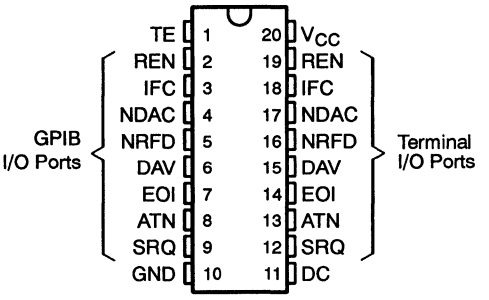
- **8-Channel Bidirectional Transceiver**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Designed to Implement Control Bus Interface**
- **SN75161B Designed for Single Controller**
- **SN75162B Designed for Multiple Controllers**
- **High-Speed, Low-Power Schottky Circuitry**
- **Low-Power Dissipation . . . 72 mW Max Per Channel**
- **Fast Propagation Times . . . 22 ns Max**
- **High-impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

description

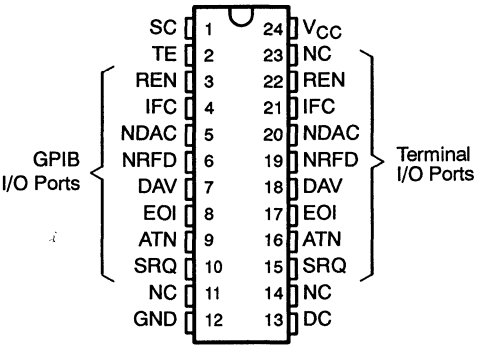
The SN75161B and SN75162B eight-channel, general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE-488 bus.

The SN75161B and SN75162B each features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power-up/down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power up and power down. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

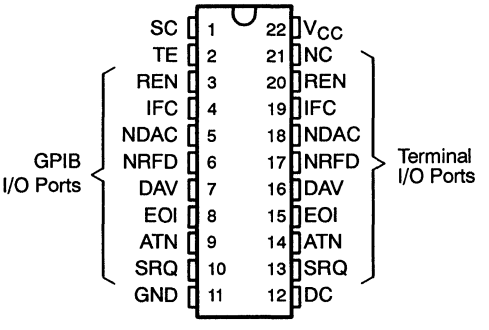
SN75161B . . . DW OR N PACKAGE
(TOP VIEW)



SN75162B . . . DW PACKAGE
(TOP VIEW)



SN75162B . . . N PACKAGE
(TOP VIEW)



NC – No internal connection

description (continued)

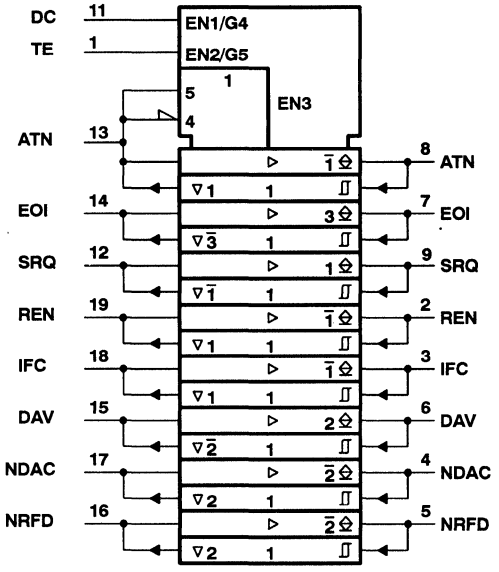
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

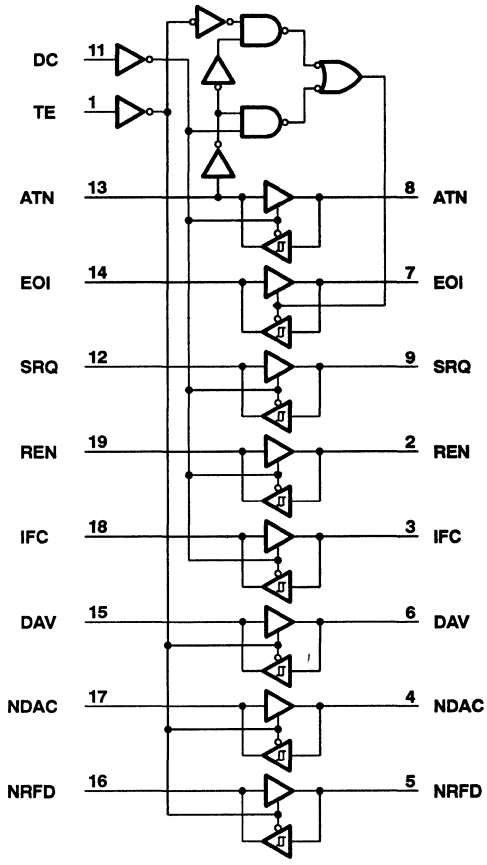
NAME	IDENTITY	CLASS
DC	Direction Control	
TE	Talk Enable	Control
SC	System Control (SN75162B only)	
ATN	Attention	
SRQ	Service Request	
REN	Remote Enable	Bus
IFC	Interface Clear	Management
EOI	End of Identity	
DAV	Data Valid	
NDAC	Not Data Accepted	Data
NRFD	Not Ready for Data	Transfer

logic symbol†

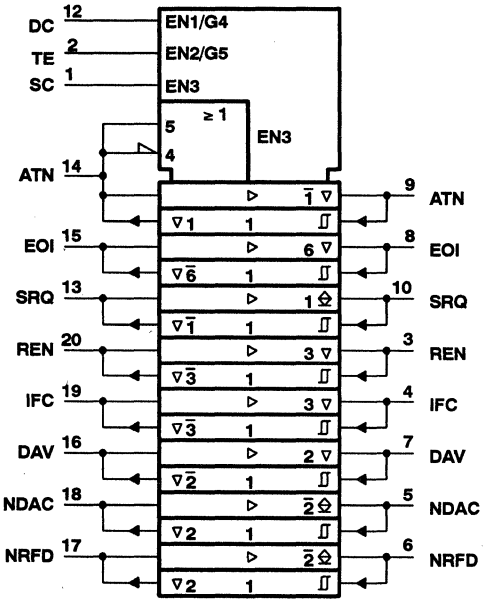


† This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

logic diagram (positive logic)

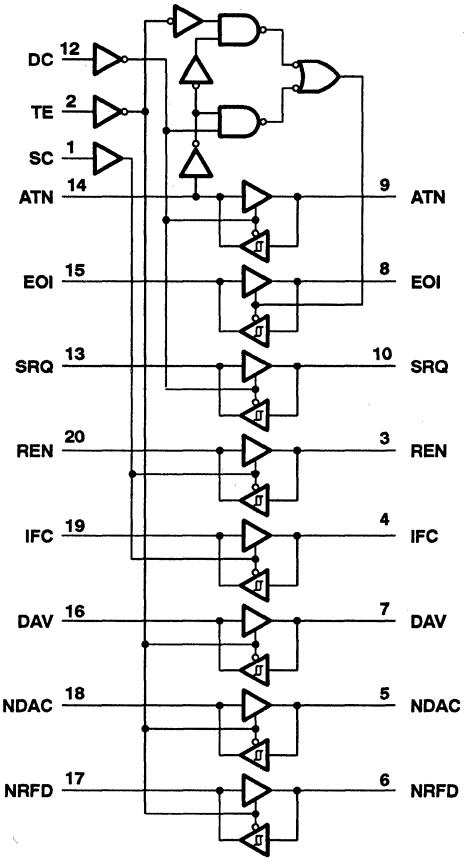


logic symbol†



†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

logic diagram (positive logic)



Pin numbers shown are for the N package.

Function Tables

SN75161B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162B RECEIVE/TRANSMIT

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

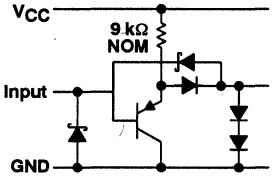
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

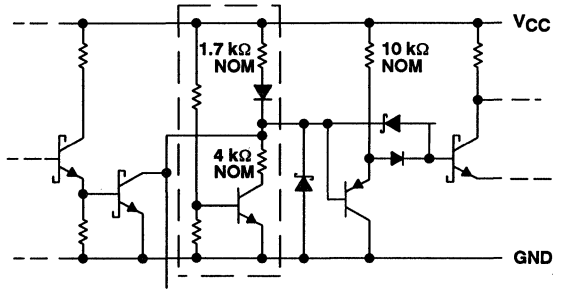
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

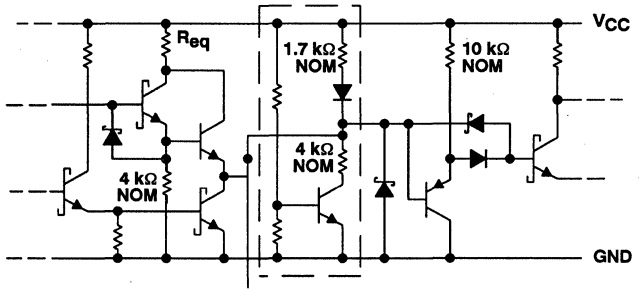


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, AND NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW (20 pin)	1125 mW	9.0 mW/°C	720 mW
DW (24 pin)	1350 mW	10.8 mW/°C	864 mW
N (20 pin)	1150 mW	9.2 mW/°C	736 mW
N (22 pin)	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level Input voltage, V_{IH}		2			V
Low-level Input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	See Figure 2		0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5	
							−3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load,	TE, DE, and SC low			110	mA
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0, $V_{I/O}$ = 0 to 2 V,	f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for 3-state outputs only.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					14	20	
t_{PLH}	Propagation delay time, low-to-high level output	Terminal	Bus (SRQ, NDAC NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low-to-high level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					15	22	
t_{PZH}	Output enable time to high level	TE,DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE,DC, or SC	Terminal	See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION

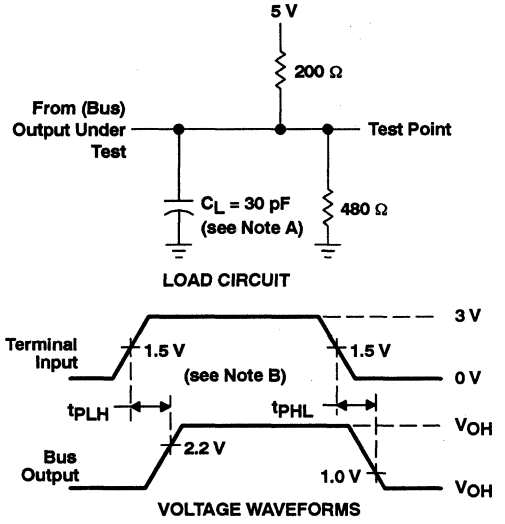


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

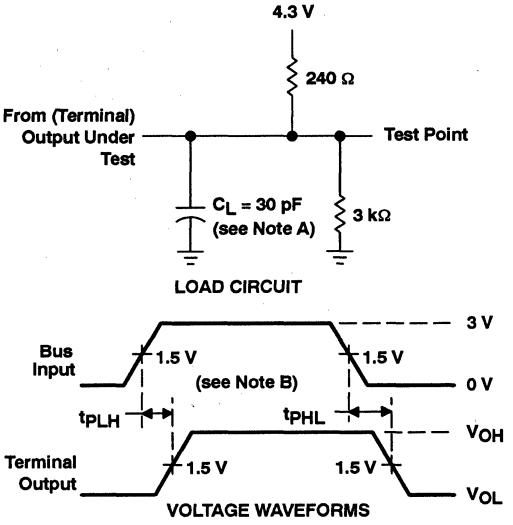
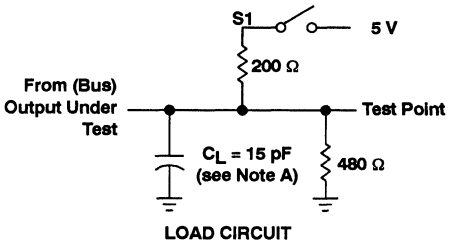
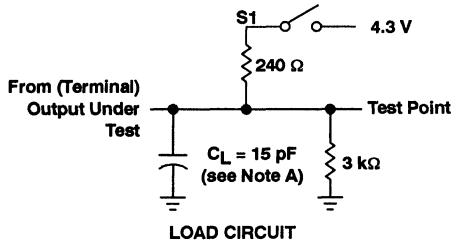


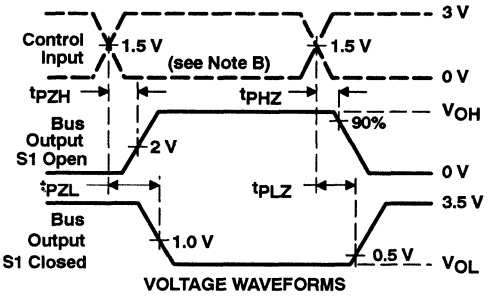
Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION







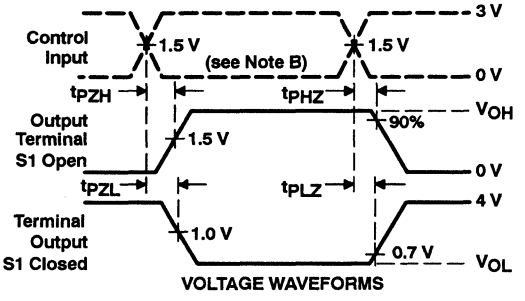


Figure 3. Bus Enable and Disable Times Load Circuit and Voltage Waveforms

Figure 4. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The Input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

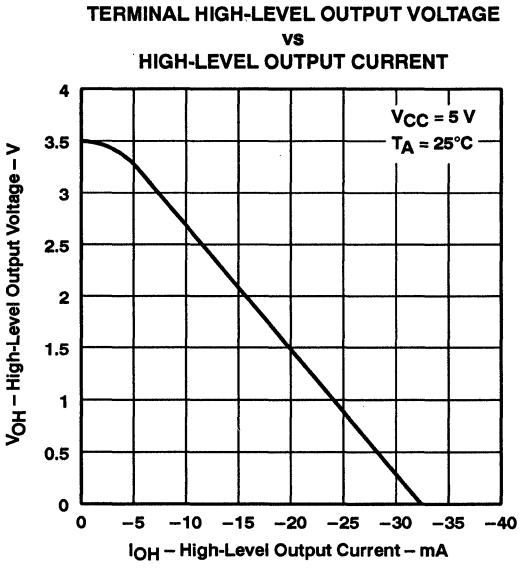


Figure 5

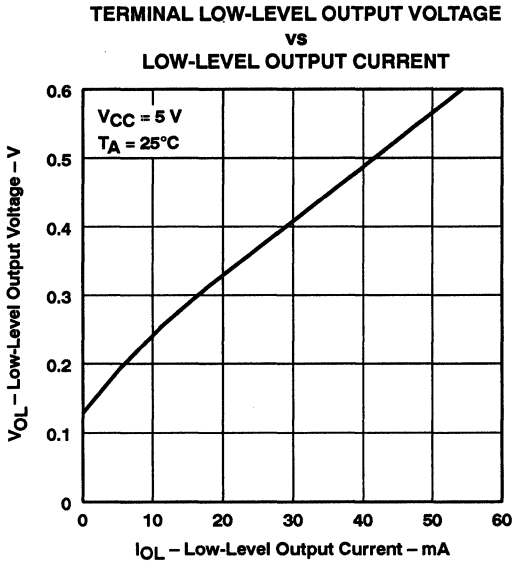


Figure 6

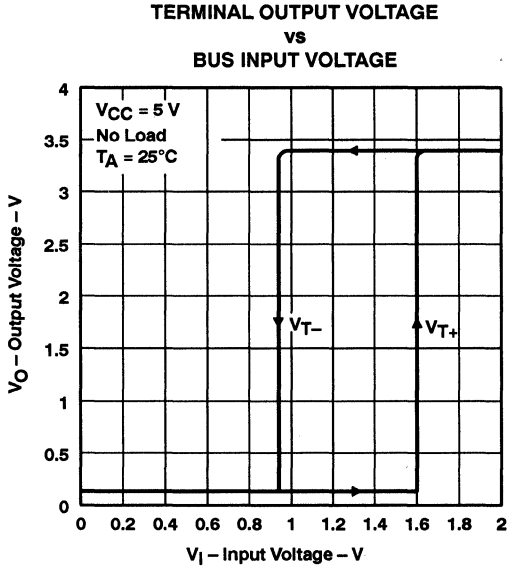


Figure 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

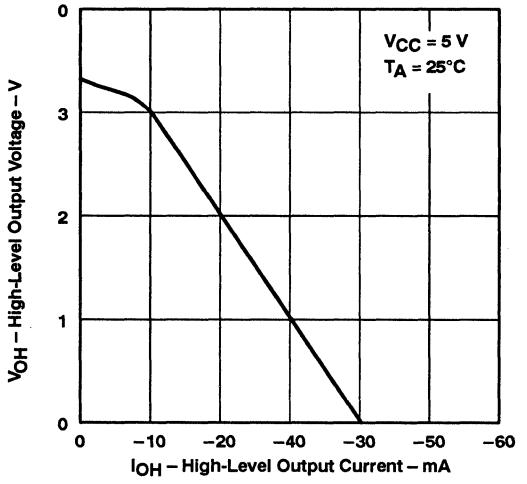


Figure 8

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

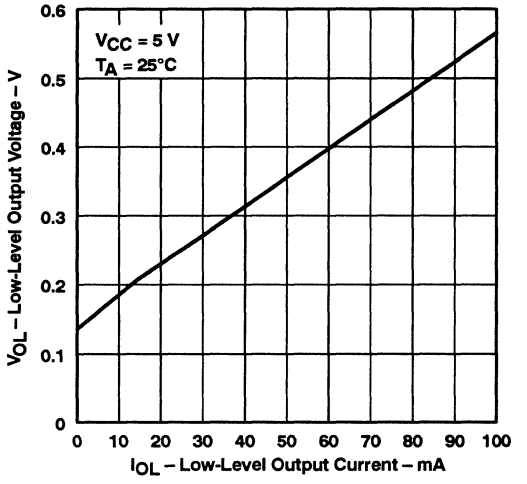


Figure 9

BUS OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

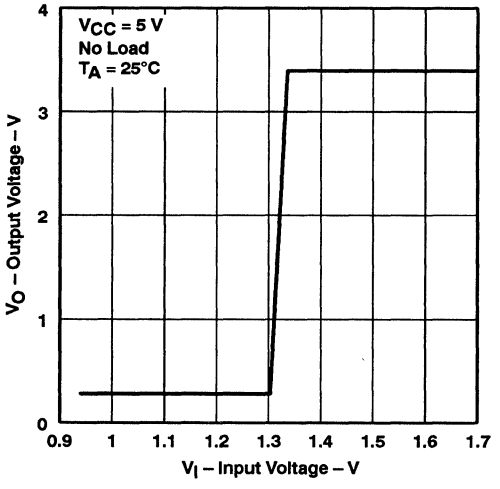


Figure 10

BUS CURRENT
vs
BUS VOLTAGE

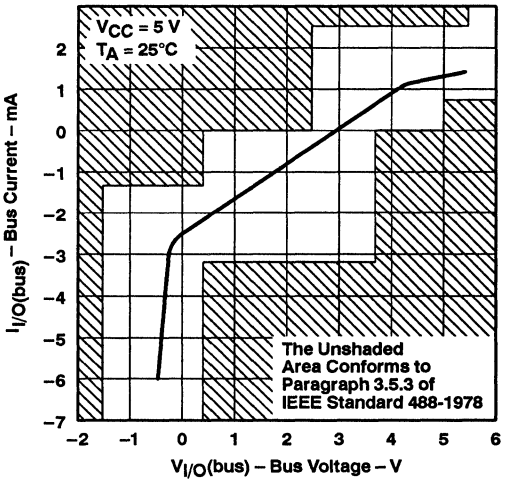


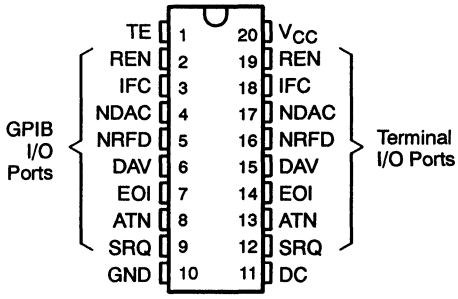
Figure 11

SLLS019C – D2618, JUNE 1986 – REVISED FEBRUARY 1993

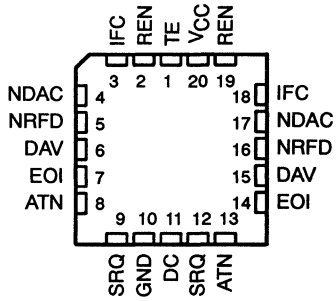
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low-Power Dissipation:
  SN55ALS161 . . . 59 mW Max Per Channel
  SN75ALS161 . . . 46 mW Max Per Channel
- Fast Propagation Times:
  SN55ALS161 . . . 25 ns Max
  SN75ALS161 . . . 20 ns Max
- High-impedance PNP Inputs
- Receiver Hysteresis:
  SN55ALS161 . . . 550 mV Typ
  SN75ALS161 . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch Free)

SN55ALS161 . . . J OR W PACKAGE
SN75ALS161 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS161 . . . FK PACKAGE
(TOP VIEW)



CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

description

The SN55ALS161 and SN75ALS161 eight-channel general-purpose interface bus transceivers are monolithic, high-speed, advanced low-power Schottky process devices designed to provide the bus-management and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN55ALS160 and SN75ALS160 octal bus transceivers, the 'ALS161 provides the complete 16-wire interface for the IEEE 488 bus.

The SN55ALS161 and SN75ALS161 feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.

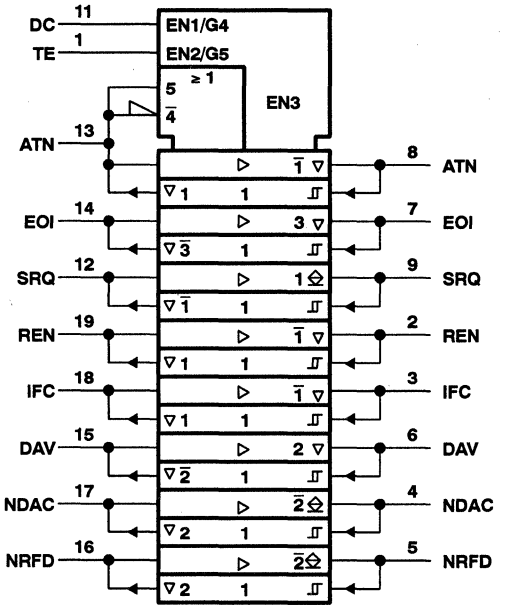
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV on the commercial part, 250 mV on the military part minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

† The transceivers are suitable for IEEE Standard 488 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

description (continued)

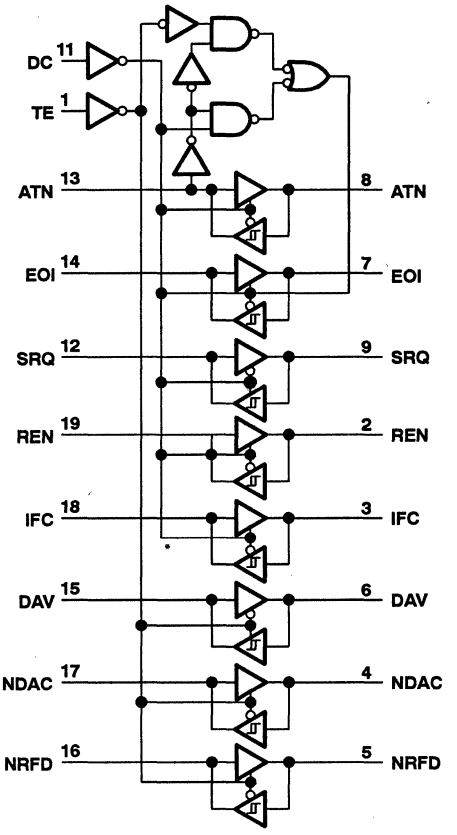
The SN5ALS161 is characterized for operation from −55°C to 125°C. The SN75ALS161 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏢ Designates passive-pullup outputs

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(controlled by DC)					(controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

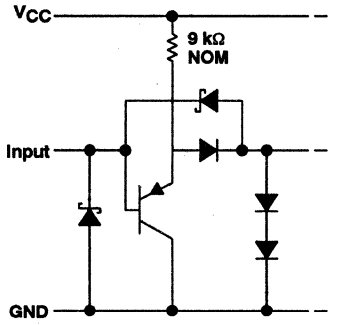
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

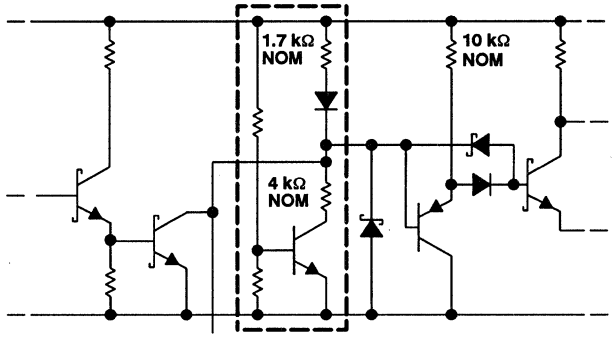
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

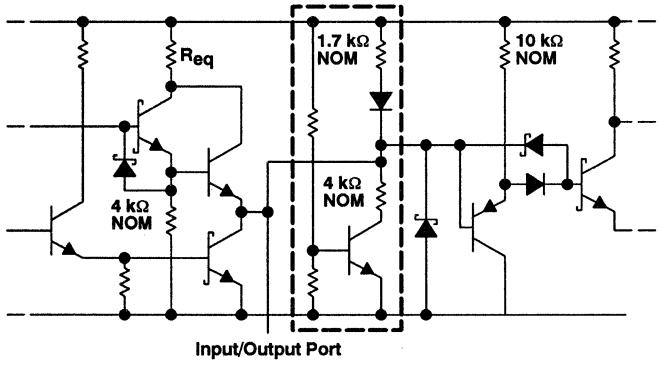


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55ALS161 ..... −55°C to 125°C
SN75ALS161 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and DC at $T_A = -55°C$ to 125°C	2			V
	Bus and terminal at $T_A = 25°C$ to 125°C	2			
	Bus and terminal at $T_A = -55°C$	2.1			
Low-level input voltage, V_{IL}	TE and DC at $T_A = -55°C$ to 125°C			0.8	V
	Bus and terminal at $T_A = 25°C$ to −55°C			0.8	
	Bus and terminal at $T_A = 125°C$			0.7	
High-level output current, I_{OH}	Bus ports with pullups active ($V_{CC} = 5$ V)			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		−55		125	°C

SN75ALS171 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN55ALS161			SN75ALS161			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		I_I = –18 mA				–0.8	–1.5		–0.8	–1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus							0.4	0.65		V
		Bus	V_{CC} = 5 V,	T_A = –55°C and 25°C		0.4	0.55					
			V_{CC} = 5 V,	T_A = 125°C		0.25						
V_{OH}§	High-level output voltage	Terminal	I_{OH} = – 800 µA			2.7	3.5		2.7	3.5		V
		Bus	I_{OH} = – 5.2 mA,	V_{CC} = 5 V (SN55')		2.2			2.2			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	V_{CC} = MIN			0.3	0.5		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	V_{CC} = MIN	T_A = –55°C and 25°C (SN55')		0.35	0.5		0.35	0.5	
					T_A = 25°C (SN55')		0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V,	V_{CC} = MAX			0.2	100		0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V,	V_{CC} = MAX			0.1	20		0.1	20	µA
I_{IL}	Low-level input current		V_I = 0.5 V,	V_{CC} = MAX			–30	–100		–10	–100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled, V_{CC} = 5 V (SN55')	$I_{I(bus)}$ = 0		2.5	3	3.7	2.5	3	3.7	V
				$I_{I(bus)}$ = –12 mA				–1.5			–1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled, V_{CC} = 5 V (SN55')	$V_{I(bus)}$ = –1.5 V to 0.4 V		–1.3			–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V		0		–3.2	0		–3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V				2.5 –3.2			2.5 –3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V		0		2.5	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V		0.7		2.5	0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V				40			40	µA
I_{OS}	Short-circuit output current	Terminal	V_{CC} = MAX			–15	–35	–75	–15	–35	–75	mA
		Bus				–25	–50	–125	–25	–50	–125	
I_{CC}	Supply current		No load,	TE and DC low,	V_{CC} = MAX		55	90		55	75	mA
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V,	f = 1 MHz		30			30		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} and I_{OS} apply to 3-state outputs only.

TEXAS INSTRUMENTS
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SN55ALS161 switching characteristics V_{CC} = 4.75 V, V_{CC} = 5 V, and V_{CC} = 5.25 V and C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus (Except SRQ, NDAC, and NRFD)	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus (NRFD, SRQ, NDAC)	See Figure 2	25°C			25	ns
					Full range			30	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	See Figure 2	25°C		10	15	ns
					Full range			18	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C		10	15	
					Full range			18	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, REN, IFC, and DAV)	See Figure 3	25°C		20	30	ns
					Full range			41	
t_{PHZ}	Output disable time from high level				25°C		8	14	
					Full range			16	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t_{PLZ}	Output disable time from low level				25°C		10	19	
					Full range			24	
t_{PZH}	Output enable time to high level	TE or DC	Bus (EOI)	See Figure 3	25°C		24	30	ns
					Full range			48	
t_{PHZ}	Output disable time from high level				25°C		13	19	
					Full range			25	
t_{PZL}	Output enable time to low level,				25°C		21	35	
					Full range			43	
t_{PLZ}	Output disable time from low level				25°C		13	20	
					Full range			27	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t_{PHZ}	Output disable time from high level				25°C		12	20	
					Full range			33	
t_{PZL}	Output enable time to low level				25°C		20	34	
					Full range			41	
t_{PLZ}	Output disable time from low level				25°C		13	24	
					Full range			35	

† Full range is −55°C to 125°C.
‡ All typical values are at V_{CC} = 5 V.

SN75ALS161 switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

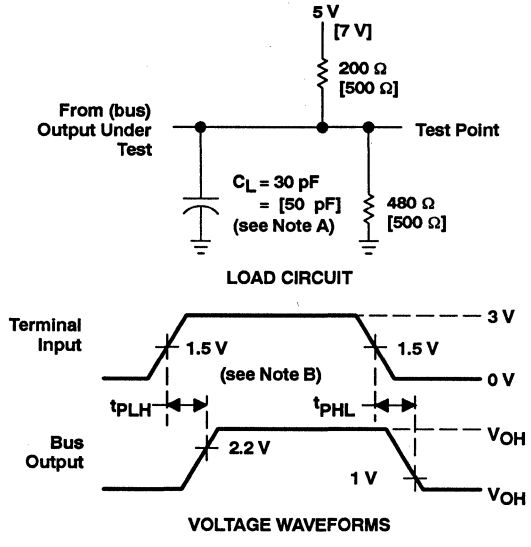


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

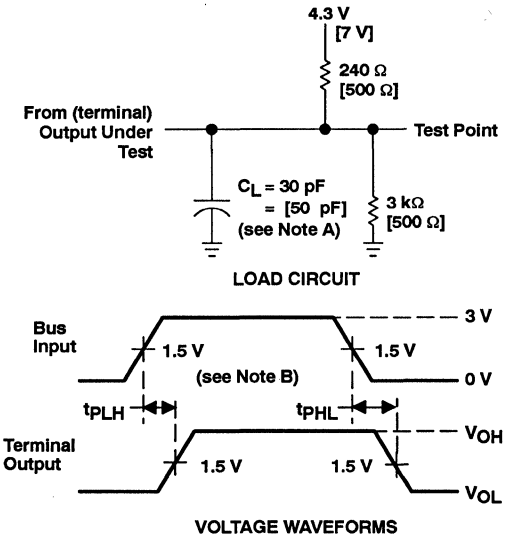


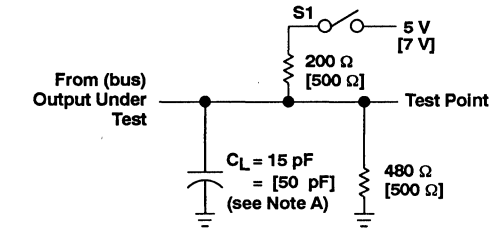
Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

[ ] denotes the SN55ALS161 military test conditions.

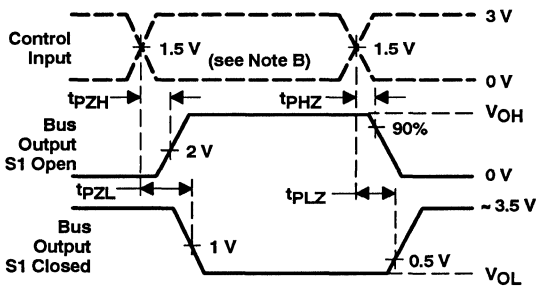
NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

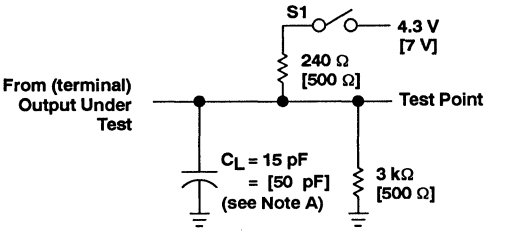


LOAD CIRCUIT

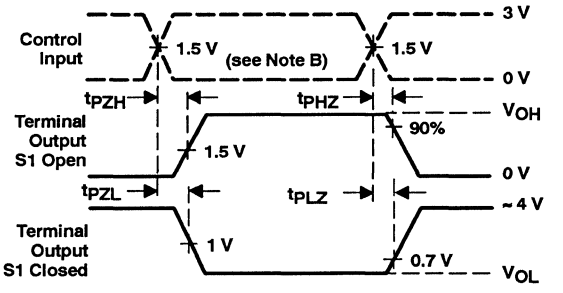


VOLTAGE WAVEFORMS

Figure 3. Bus Load Circuit and Voltage Waveforms



LOAD CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Terminal Load Circuit and Voltage Waveforms

[ ] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

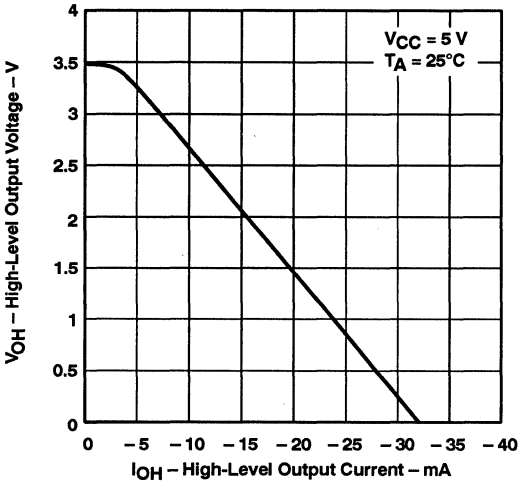


Figure 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

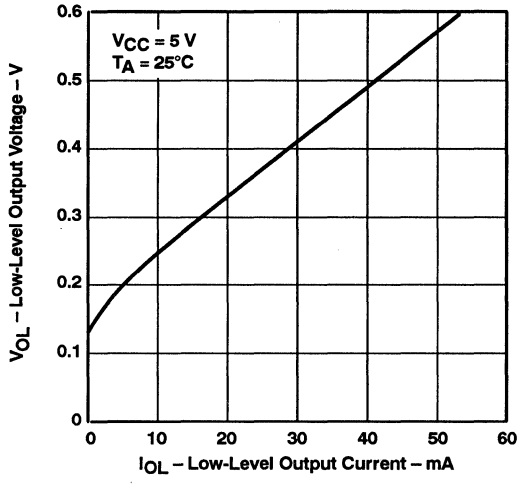


Figure 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

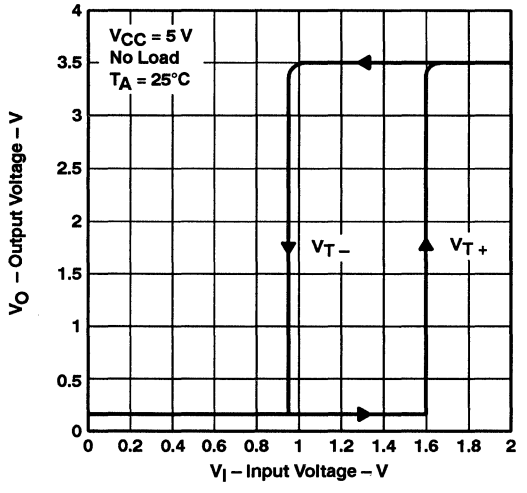


Figure 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

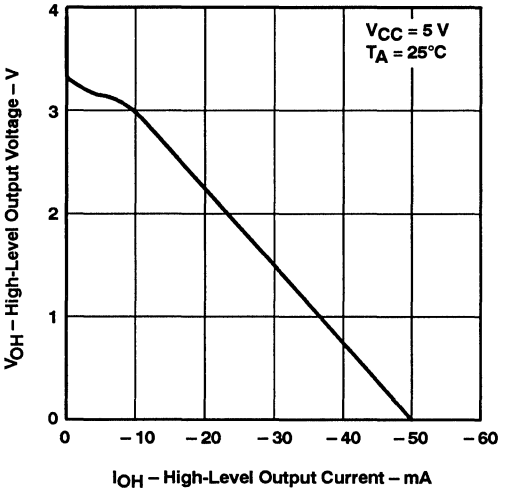


Figure 8

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

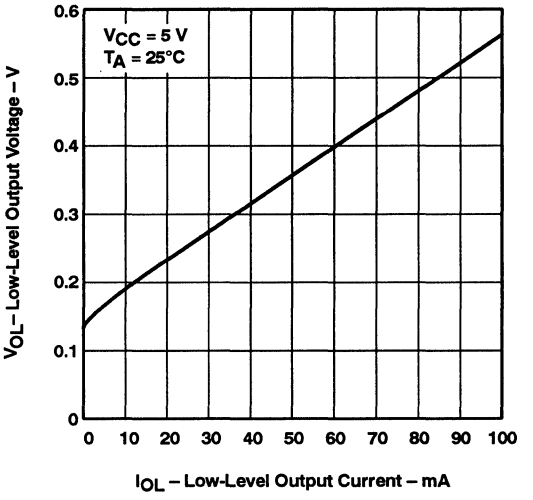


Figure 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

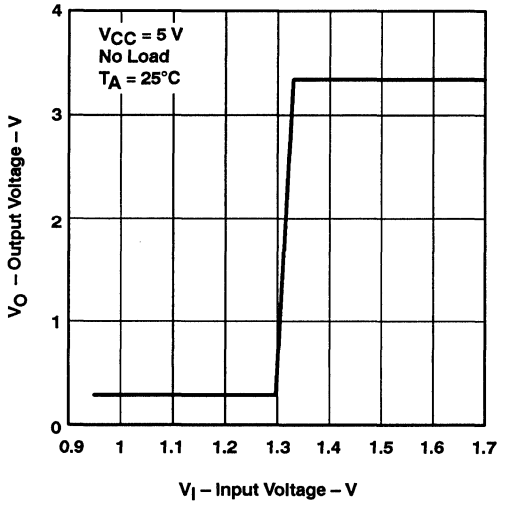


Figure 10

BUS CURRENT
vs
BUS VOLTAGE

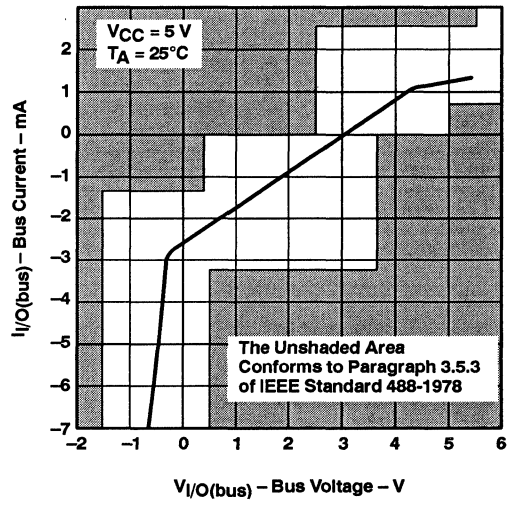


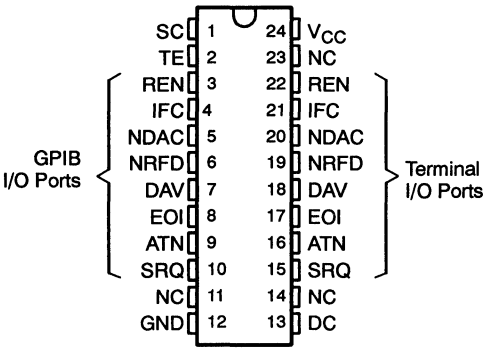
Figure 11

SLLS020B – D2618, JUNE 1986 – REVISED AUGUST 1989

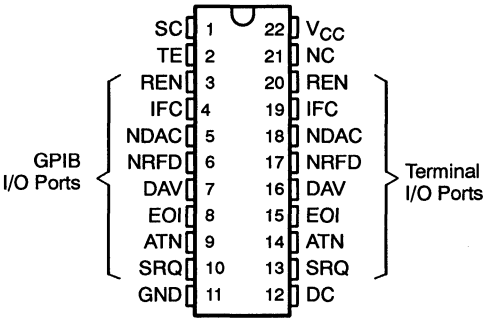
MEETS IEEE STANDARD 488-1978 (GPIB)

- **8-Channel Bidirectional Transceiver**
- **Designed to Implement Control Bus Interface**
- **Designed for Multicontrollers**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low-Power Dissipation . . . 46 mW Max per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**

DW PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



NC–No internal connection

description

The SN75ALS162 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

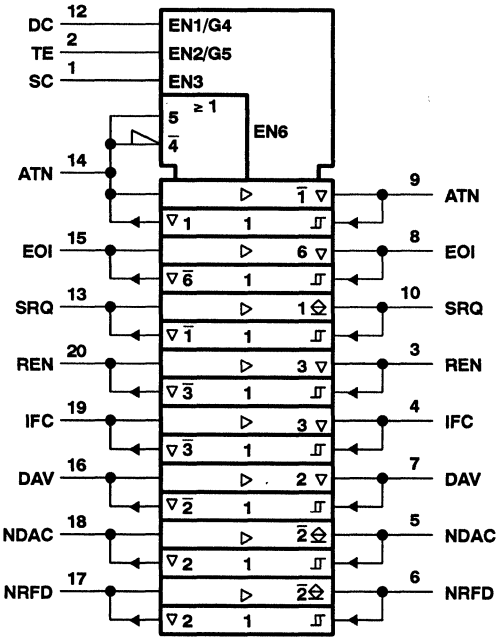
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS162 is characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

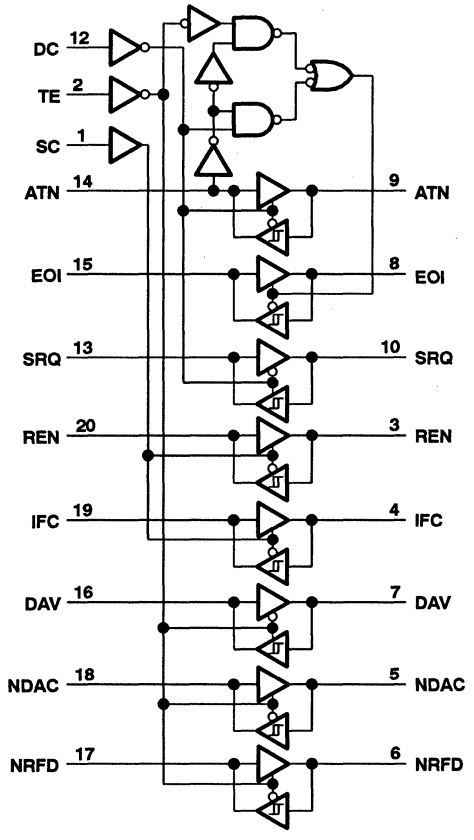
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	No Data Accepted	
NRFD	Not Ready for Data	

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
◇ Designates passive-pullup outputs

logic diagram (positive logic)



Pin numbers shown are for the N package.

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (controlled by DC)	SRQ (controlled by DC)	REN (controlled by SC)	IFC (controlled by SC)	EOI	DAV (controlled by TE)	NDAC (controlled by TE)	NRFD (controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

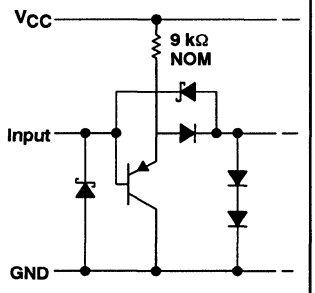
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

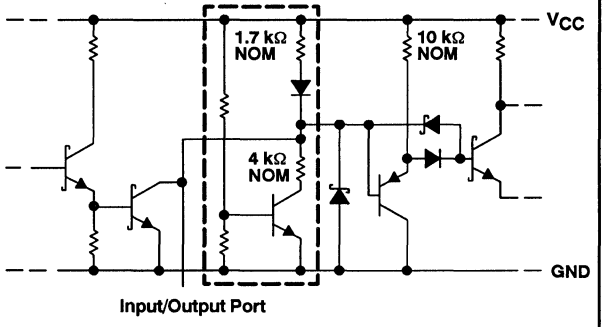
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

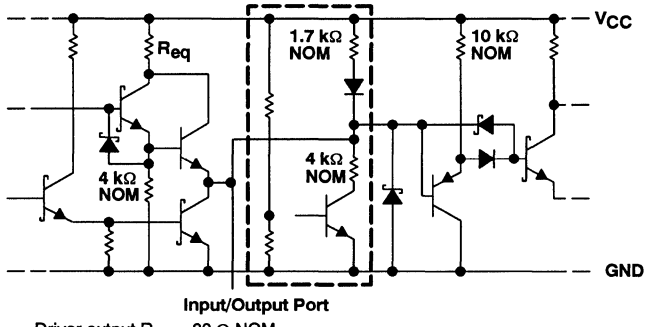


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM

Receiver output R_{eq} = 110 Ω NOM

Circuit inside dashed lines is on the driver outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
N	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			– 5.2	mA
	Terminal ports			– 800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	$I_{OH} = -800$ μA		2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OL} = 48$ mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5$ V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7$ V			0.1	20	μA
I_{IL}	Low-level input current		$V_I = 0.5$ V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)} = 0$	2.5	3.0	3.7	V
				$I_{I(bus)} = -12$ mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)} = -1.5$ V to 0.4 V	−1.3			mA
				$V_{I(bus)} = 0.4$ V to 2.5 V	0		−3.2	
				$V_{I(bus)} = 2.5$ V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)} = 3.7$ V to 5 V	0		2.5	
				$V_{I(bus)} = 5$ V to 5.5 V	0.7		2.5	
		Power off	$V_{CC} = 0$,	$V_{I(bus)} = 0$ to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load,	TE, DC, and SC low		55	75	mA
$C_{I/O(bus)}$	Bus-port capacitance		$V_{CC} = 0$ to 5 V,	$V_{I/O} = 0$ to 2 V, f = 1 MHz		30		pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ V_{OH} applies to 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

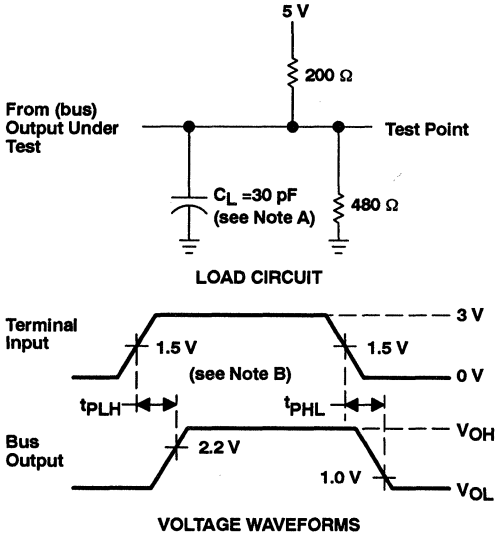


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

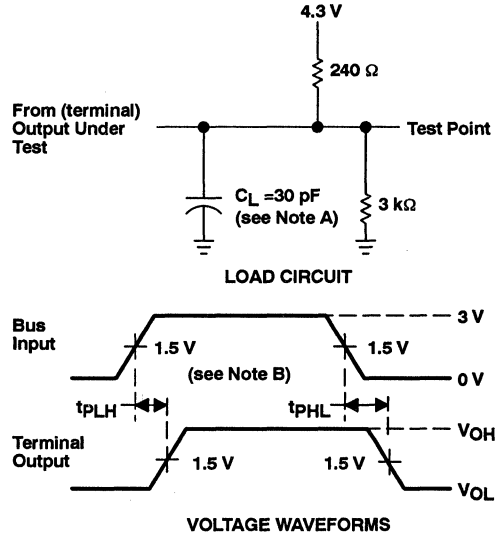


Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

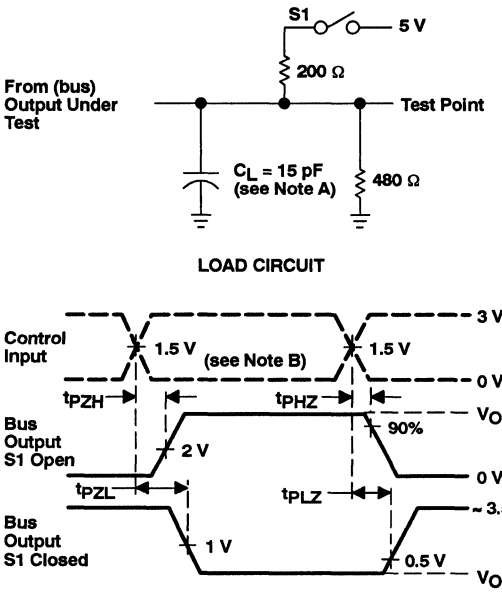


Figure 3. Bus Load Circuit and Voltage Waveforms

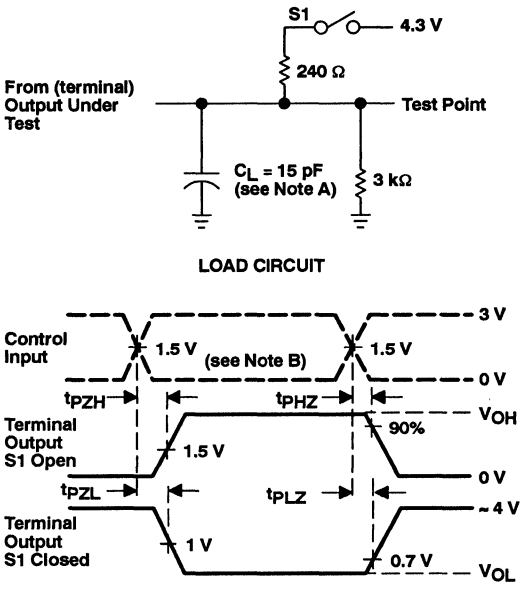


Figure 4. Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

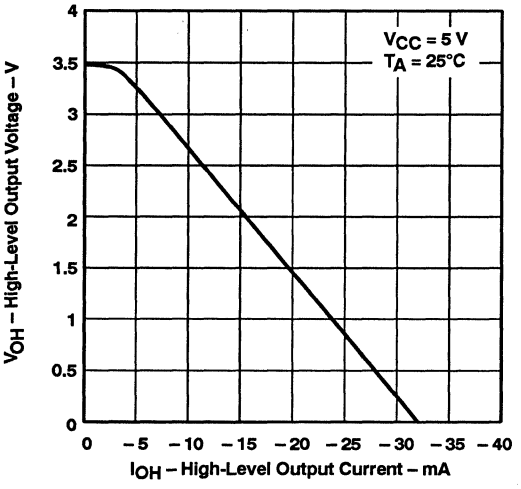


Figure 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

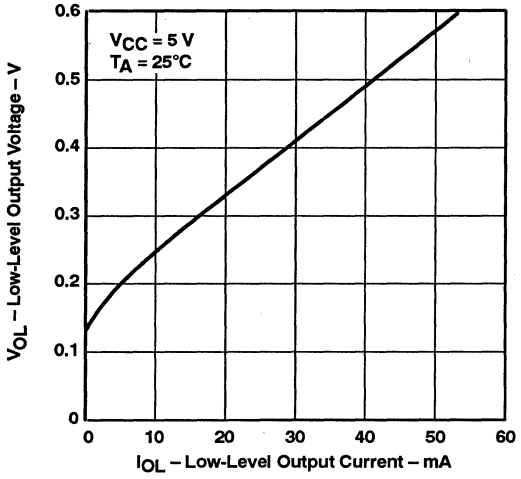


Figure 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

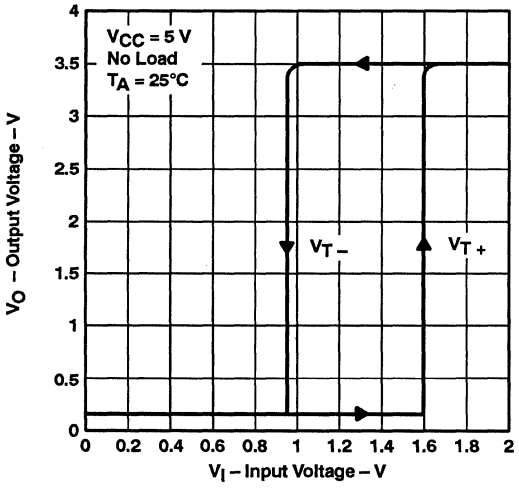


Figure 7

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

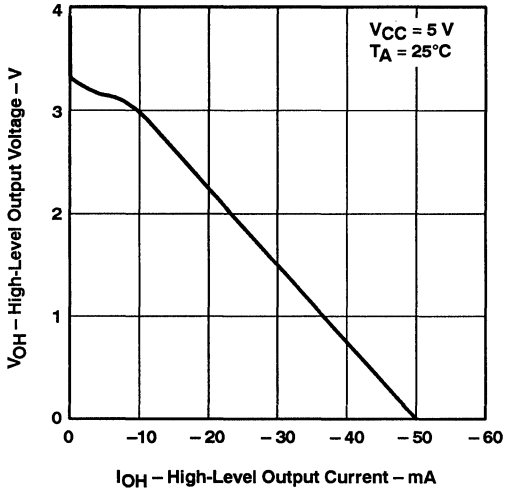


Figure 8

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

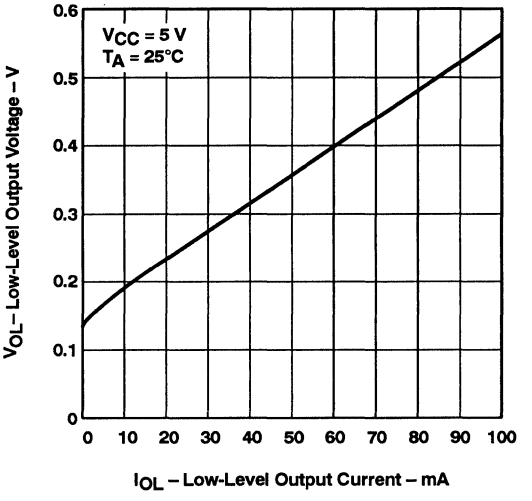


Figure 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

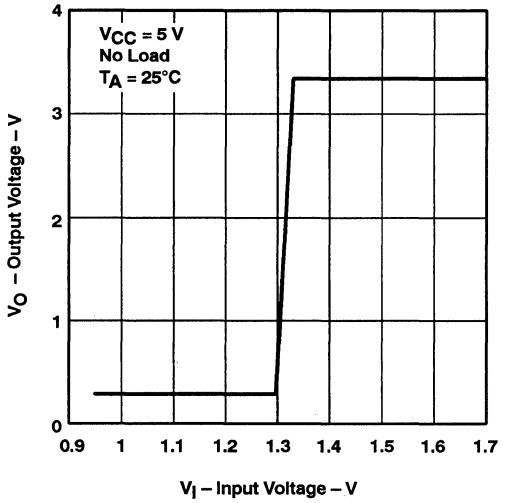


Figure 10

BUS CURRENT
vs
BUS VOLTAGE

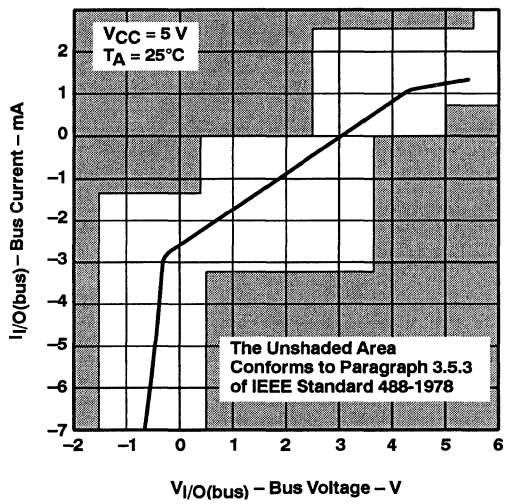
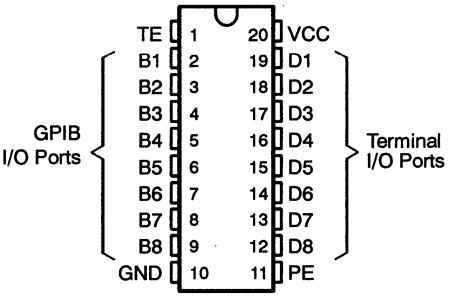


Figure 11

SLLS006A – D2611, OCTOBER 1985 – REVISED FEBRUARY 1993

- **8-Channel Bidirectional Transceivers**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **High-Speed Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 66 mW Max Per Channel**
- **High-impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

DW OR N PACKAGE
(TOP VIEW)



description

NOT RECOMMENDED FOR NEW DESIGN

The SN75163B octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state modes. If talk enable (TE) is high, these outputs have the characteristics of open-collector outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and 400 mV of hysteresis for increased noise immunity.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75163B is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

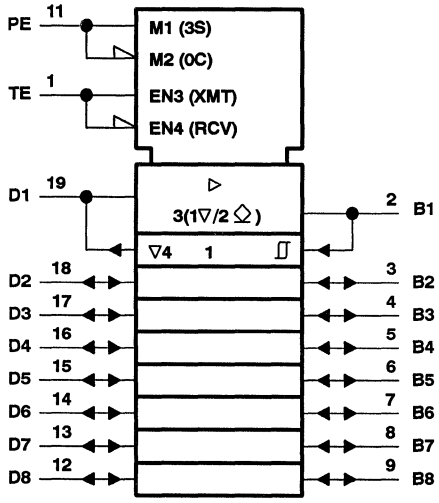
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	H	L
H	X	L	Z
L	H	L	L
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

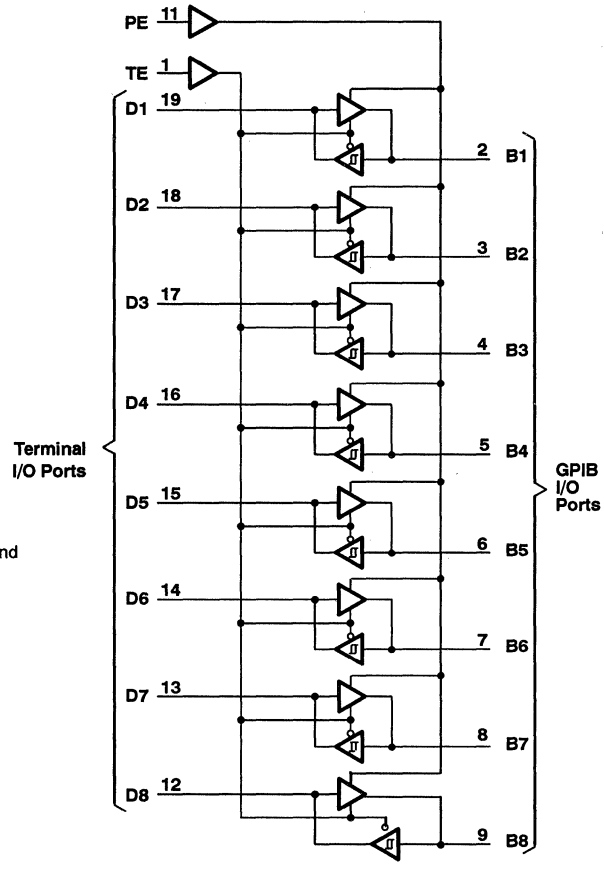
H = high level, L = low level, X = irrelevant, Z = high-impedance state

logic symbol†



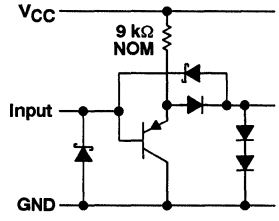
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
∇ Designates 3-state outputs
◇ Designates open-collector outputs

logic diagram (positive logic)

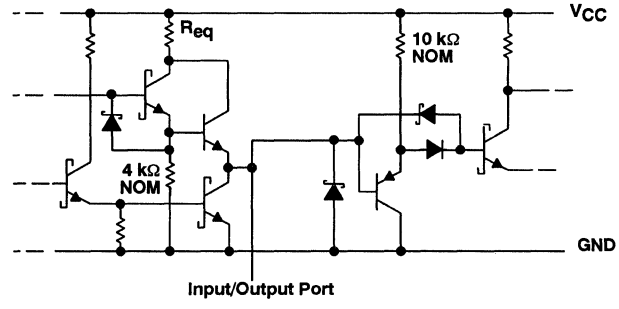


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total power dissipation (see Note 2) ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			–10	mA
	Terminal ports			–800	µA
High-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	See Figure 8		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	$I_{OH} = -800$ μA,	TE at 0.8 V	2.7	3.5		V
		Bus	$I_{OH} = -10$ mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16$ mA,	TE at 0.8 V		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA,	PE and TE at 2 V		0.4	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	$V_O = 5.5$ V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	$V_O = 2.7$ V			20	μA
				$V_O = 0.4$ V			−20	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5$ V			0.2	100	μA
I_{IH}	High-level input current	Terminal	$V_I = 2.7$ V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	$V_I = 0.5$ V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{IL}	Supply current		No load	Receivers low and enabled			80	mA
				Drivers low and enabled			100	
$C_{I/O(bus)}$	Bus-port capacitance		$V_{CC} = 5$ V to 0,	$V_{I/O} = 0$ to 2 V, f = 1 MHz		30		pF

† All typical values are at $V_{CC} = 5$, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	$C_L = 30$ pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	$C_L = 30$ pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pullup enable time	PE	Terminal	See Figure 5		15	22	ns
t_{dis}	Output pullup disable time					13	20	

PARAMETER MEASUREMENT INFORMATION

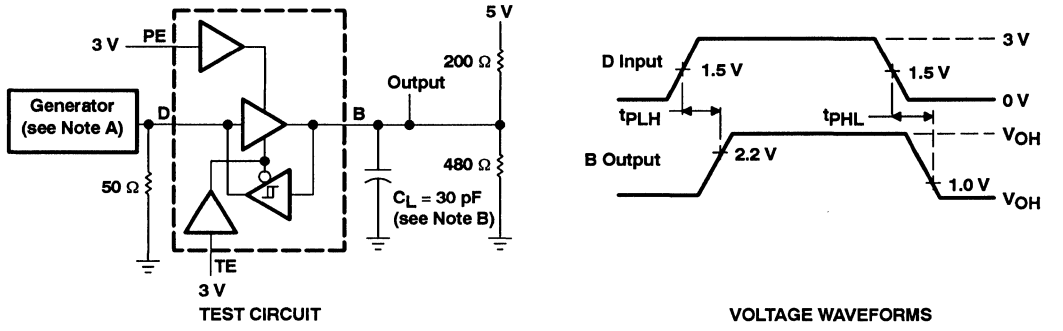


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

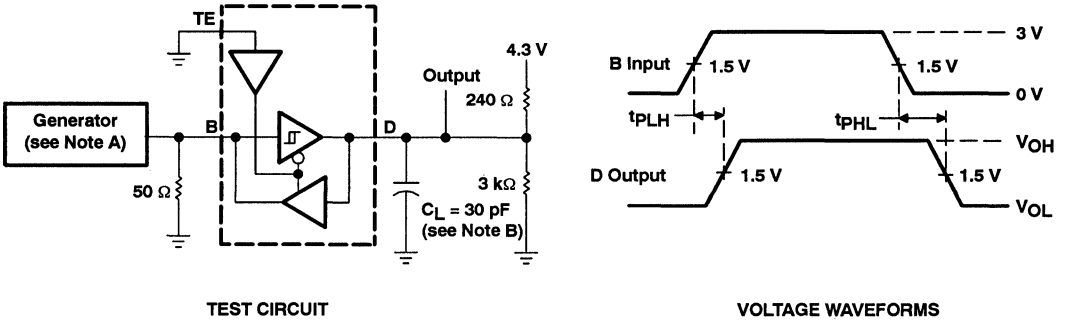


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

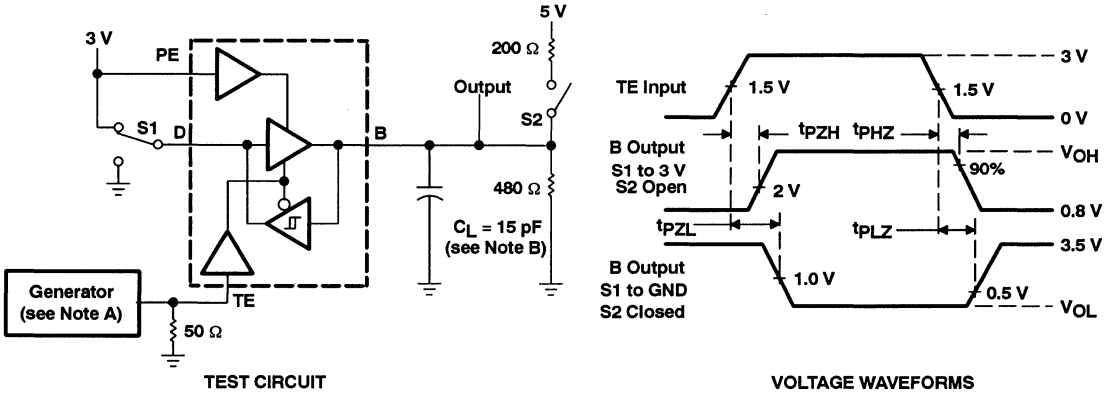


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

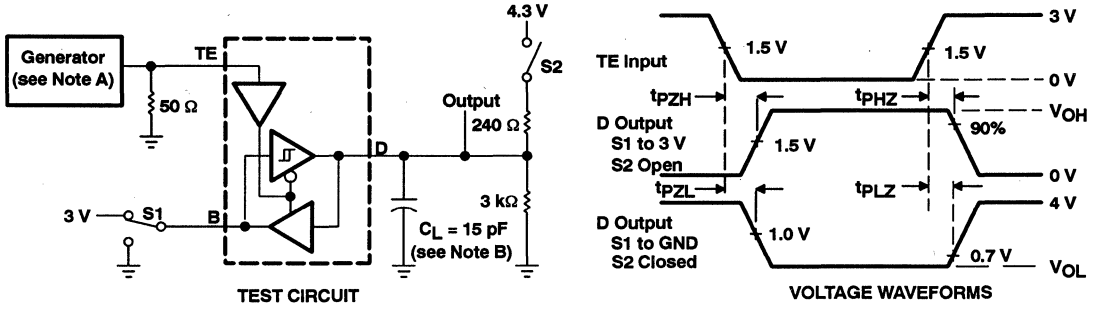


Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

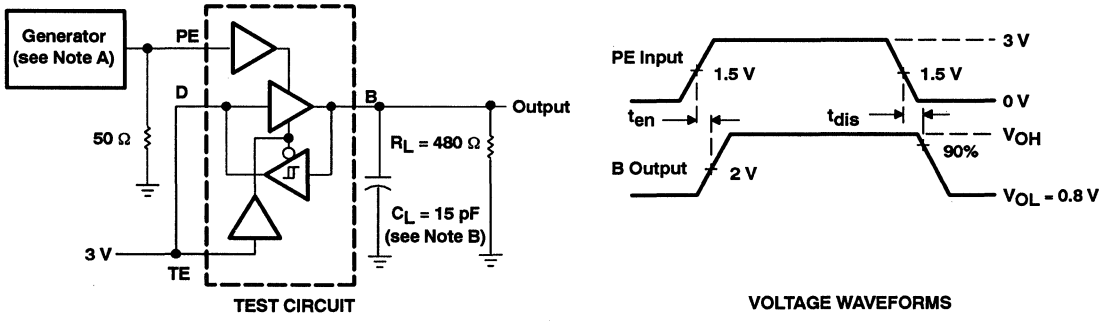


Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms

NOTES: C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

D. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

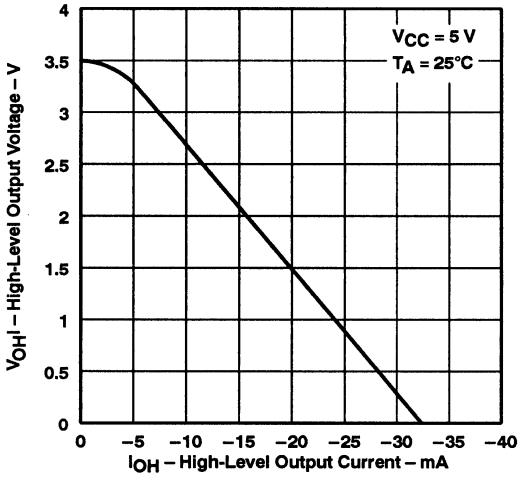


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

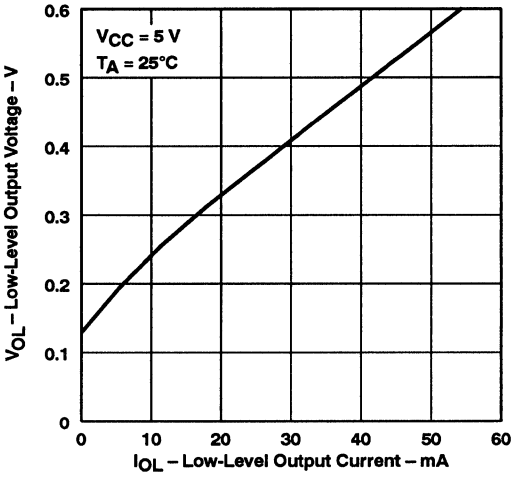


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

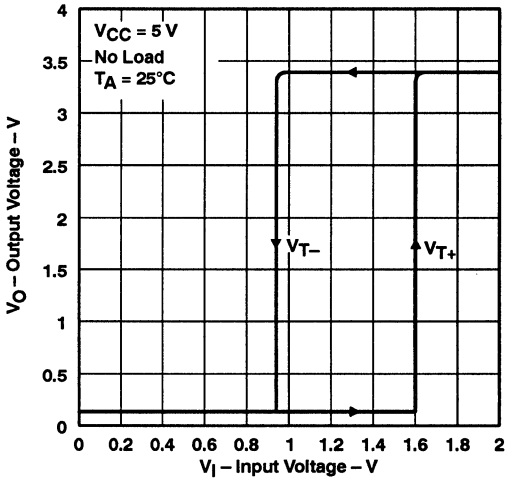


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

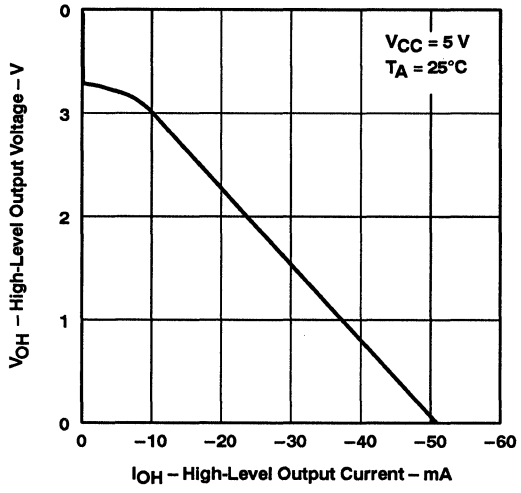


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

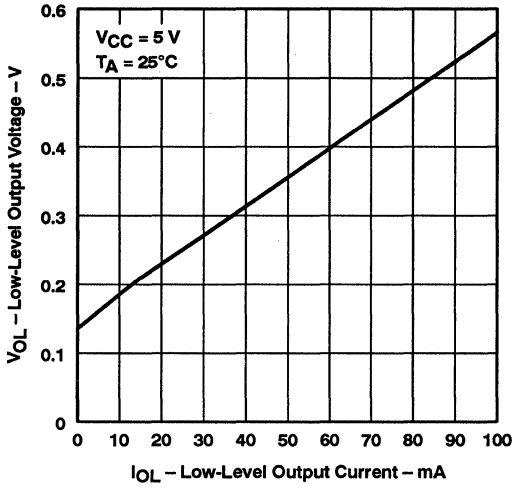


Figure 10

BUS OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

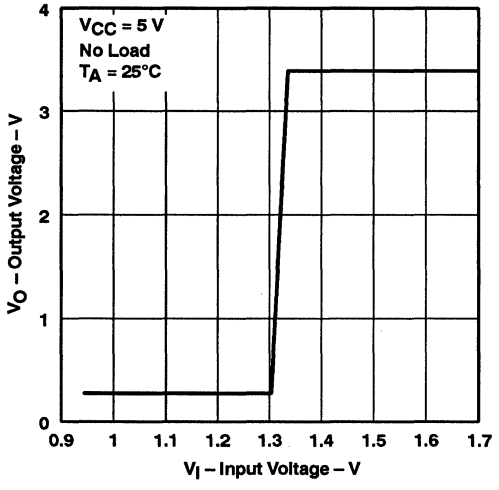
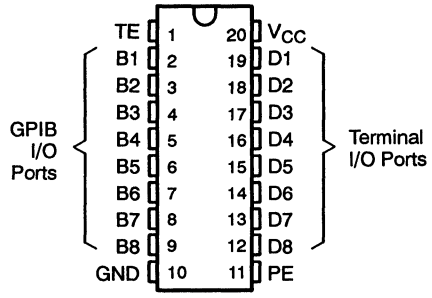


Figure 11

SLLS021D – D2611, JUNE 1986 – REVISED FEBRUARY 1993

- **8-Channel Bidirectional Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 46 mW Max per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**

DW OR N PACKAGE
(TOP VIEW)



description

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state mode. If talk enable (TE) is high, these outputs have the characteristics of open-collector outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and 400 mV minimum of hysteresis for increased noise immunity.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z
X	L	X	Z

EACH RECEIVER

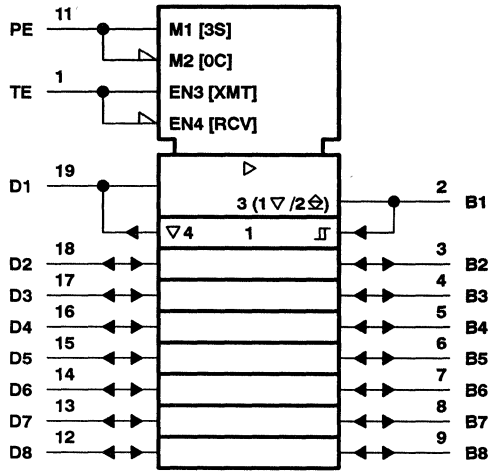
INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant,
Z = high-impedance state

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

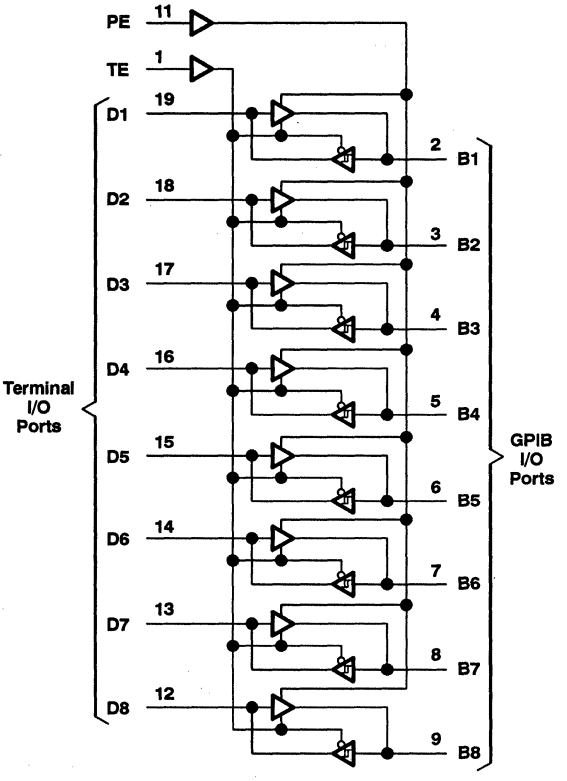
The SN75ALS163 is characterized for operation from 0°C to 70°C.

logic symbol†

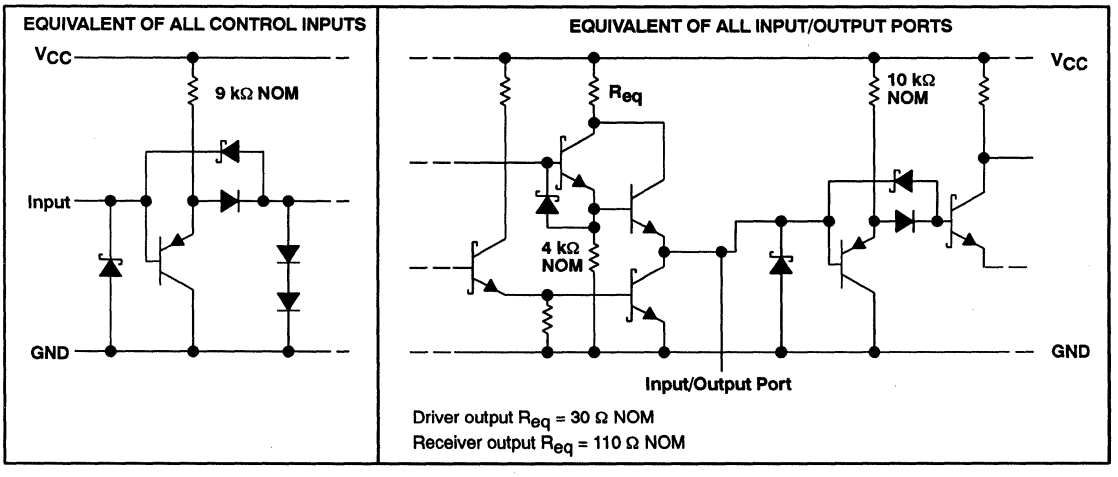


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates open-collector outputs

logic diagram (positive logic)



schematics of inputs and outputs



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTE: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			– 5.2	mA
	Terminal ports			– 800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA			–0.8	–1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = –800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = –5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V,	PE at 0.8 V, D and TE at 2 V			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.5 V			–100	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal, PE, or TE	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			–10	–100	μA
I_{OS}	Short-circuit output current	Terminal			–15	–35	–75	mA
		Bus			–25	–50	–125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	65	mA
				Bus outputs low and enabled		52	80	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pull-up enable time	PE	Bus	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pull-up disable time					6	12	

‡ Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

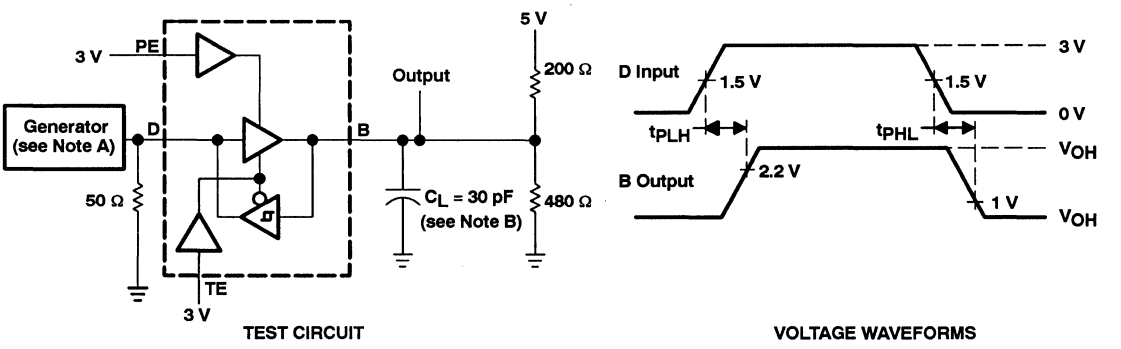


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

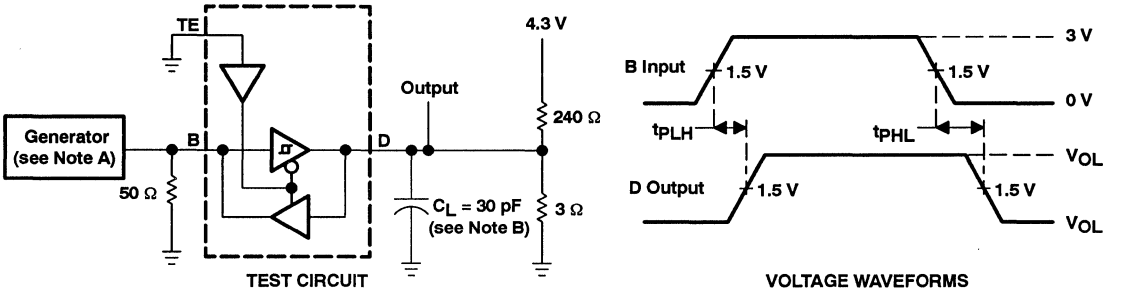


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

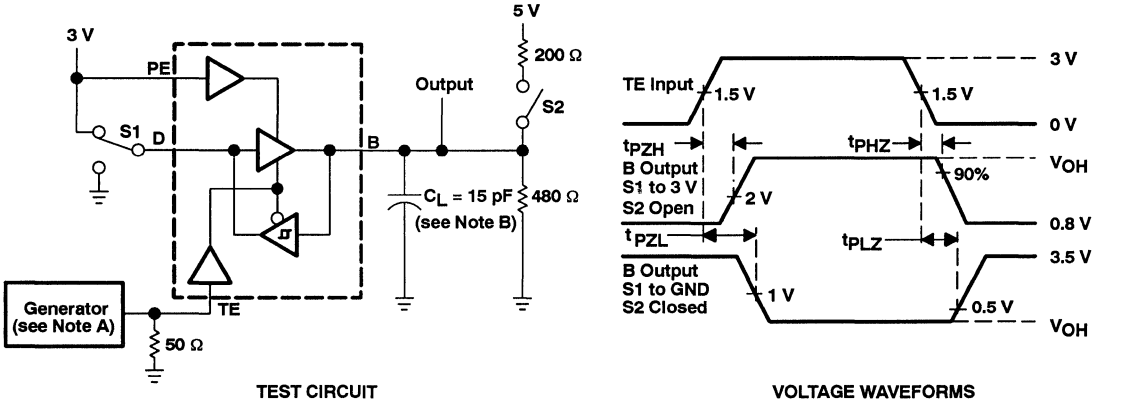
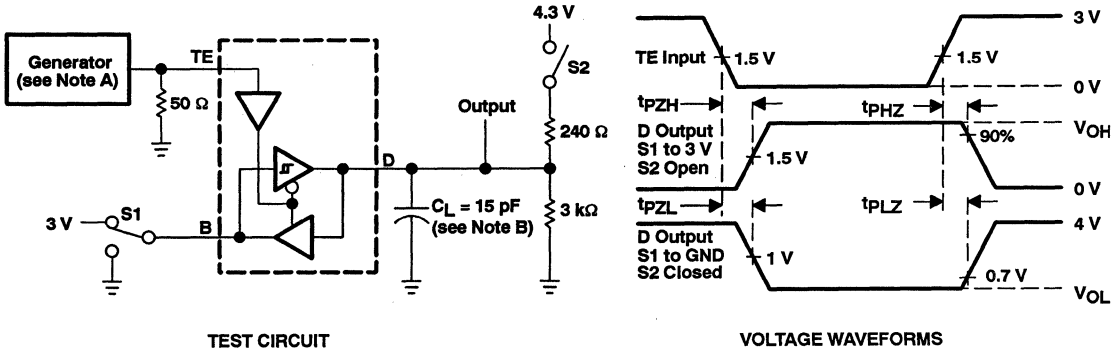


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

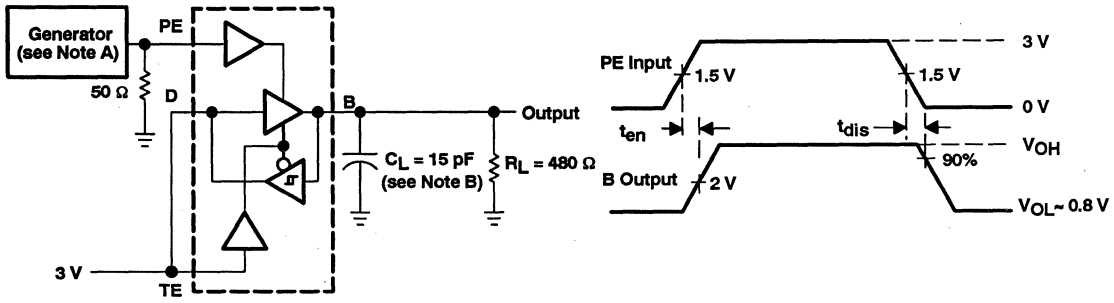
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

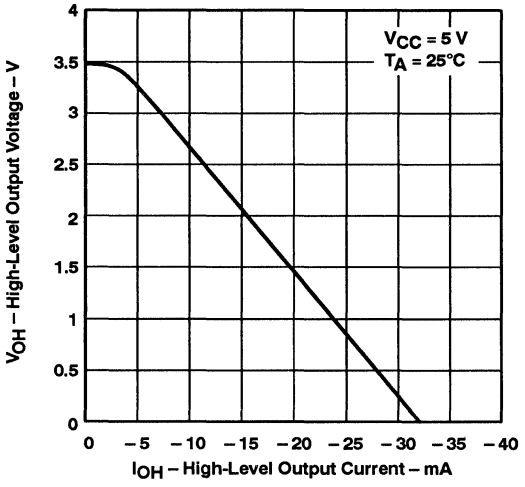


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

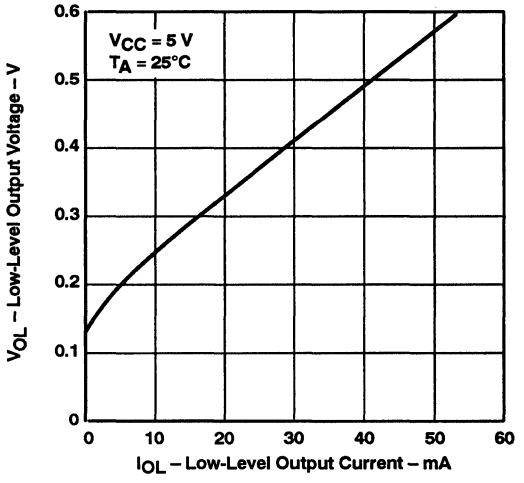


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

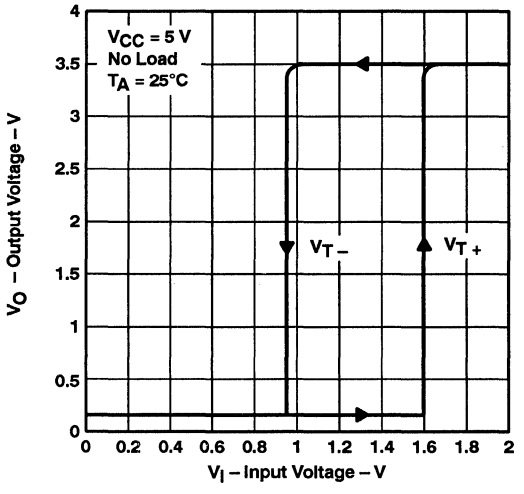


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

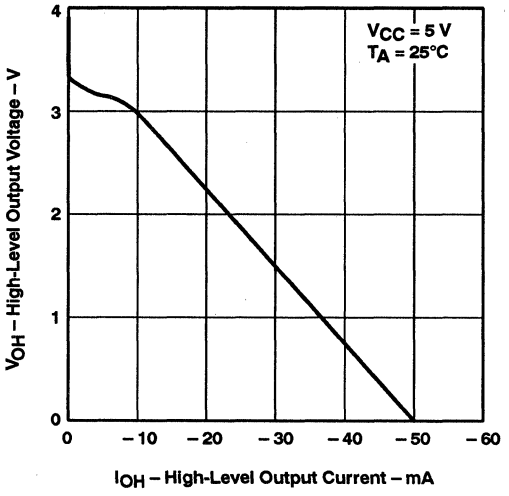


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

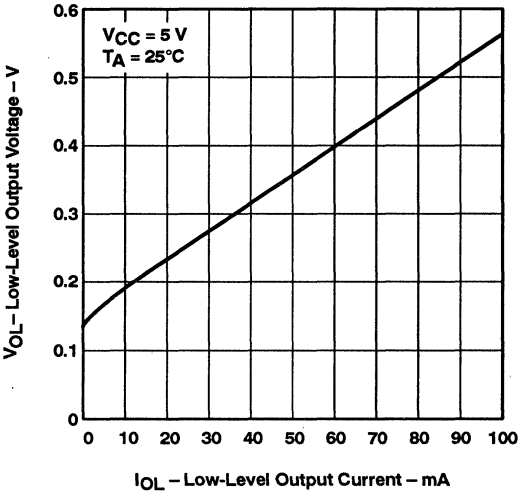


Figure 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

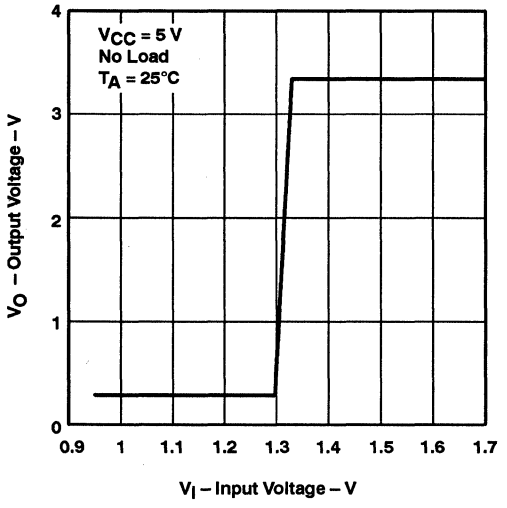
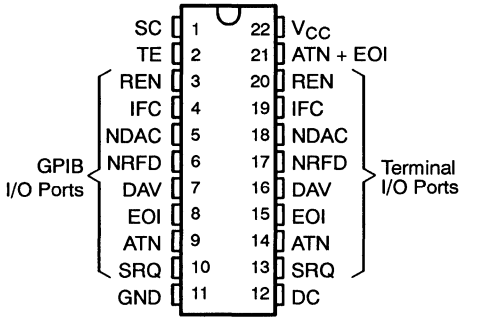


Figure 11

SLLS011A – D2908, OCTOBER 1985 – REVISED FEBRUARY 1993

- **8-Channel Bidirectional Transceiver**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **ATN+EOI (OR Function) Output to Simplify Board Layout**
- **Designed to Implement Control Bus Interface for Multiple Controllers**
- **Low-Power Dissipation . . . 72 mW Max Per Channel**
- **Fast Propagation Times . . . 22 ns Max**
- **High-impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

N PACKAGE
(TOP VIEW)



NC – No internal connection

NOT RECOMMENDED FOR NEW DESIGN

description

The SN75164B eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75164B provides the complete 16-wire interface for the IEEE-488 bus.

CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC TE SC	Direction Control Talk Enable System Control	Control
ATN SRQ REN IFC EOI	Attention Service Request Remote Enable Interface Clear End or Identify	Bus Management
ATN + EOI	ATN Logical or EOI	Logic
DAV NDAC NRFD	Data Valid Not Data Accepted Not Ready for Data	Data Transfer

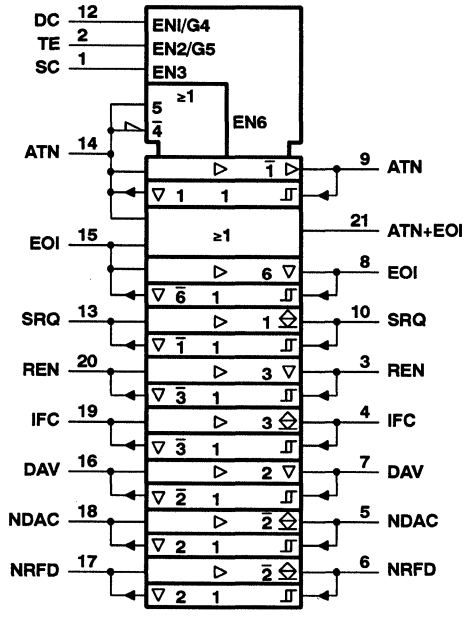
The SN75164B features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75164B is identical to the SN75162B with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.

description (continued)

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and an ensured hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

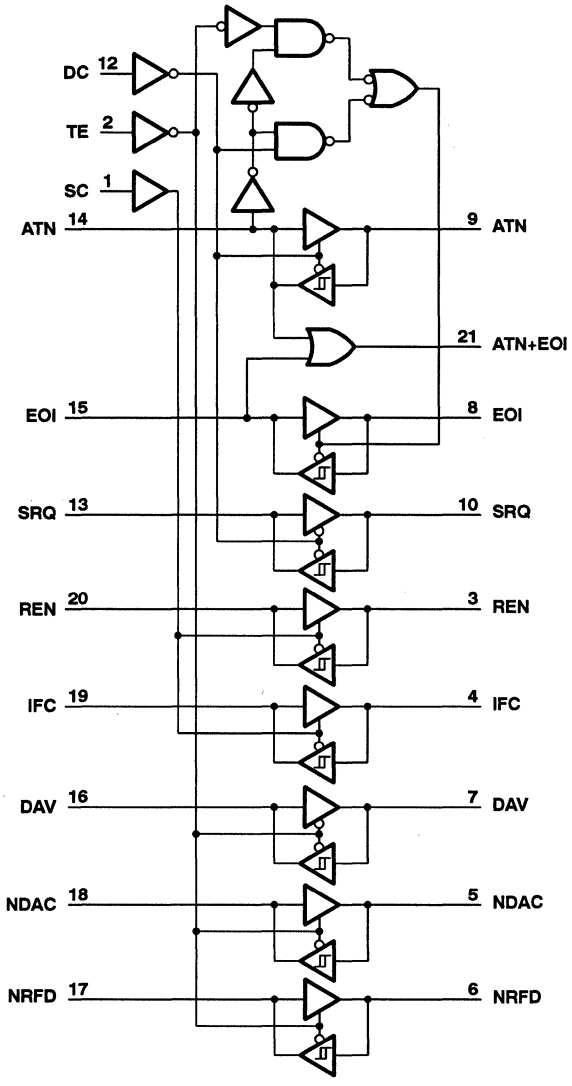
The SN75164B is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (controlled by DC)	SRQ (controlled by DC)	REN (controlled by SC)	IFC (controlled by SC)	EOI	DAV (controlled by TE)	NDAC (controlled by TE)	NRFD (controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

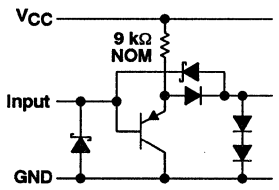
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

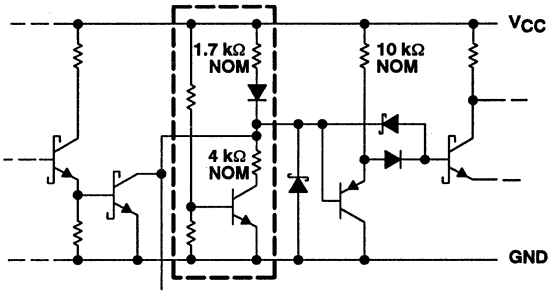
INPUTS		OUTPUT
ATN	EOI	ATN+EOI
H	X	H
X	H	H
L	L	L

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

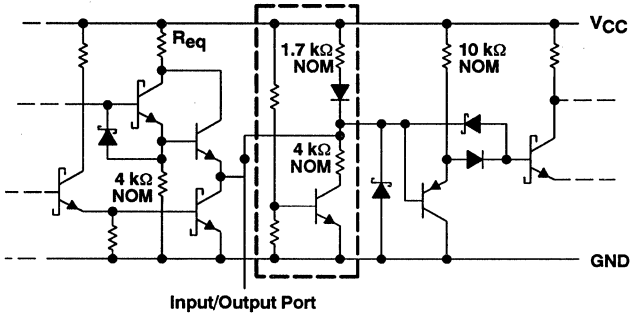


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



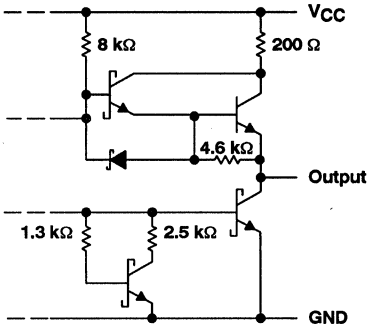
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF ALL I/O PORTS
EXCEPT SRQ, NDAC, AND NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

ATN+EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1700 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the N package at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level Input voltage, V_{IH}		2			V
Low-level Input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	µA
	ATN+EOI			−400	
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
	ATN+EOI			4	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA				−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	See Figure 8		0.4			V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 µA		2.7			V
		Bus	I_{OH} = −5.2 mA		2.5			
		ATN+EOI	I_{OH} = −400 µA		2.7			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA				0.5	V
		Bus	I_{OL} = 48 mA				0.5	
		ATN+EOI	I_{OL} = 4 mA				0.4	
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V				100	µA
		ATN+EOI	V_I = 5.5 V				200	
I_{IH}	High-level input current	Terminal, control	V_I = 2.7 V				20	µA
		ATN, EOI	V_I = 2.7 V				40	
I_{IL}	Low-level input current	Terminal, control	V_I = 0.5 V				−100	µA
		ATN, EOI	V_I = 0.5 V				−500	
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5		3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	µA
I_{OS}	Short-circuit output current	Terminal			−15		−75	mA
		Bus			−25		−125	
		ATN+EOI			−10		−100	
I_{CC}	Supply current		No load,	TE, DE, and SC low			120	mA
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for 3-state outputs only.
§ Except ATN and EOI terminal pins

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					14	20	
t_{PLH}	Propagation delay time, low-to-high level output	Terminal	Bus (SRQ, NDAC NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low-to-high level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low level output					15	22	
t_{PLH}	Propagation delay time, low-to-high level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PHL}	Propagation delay time, high-to-low level output	Terminal ATN or Terminal EOI	ATN+EOI	See Figure 3		14		ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 4			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE,DC, or SC	Terminal	See Figure 5			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION

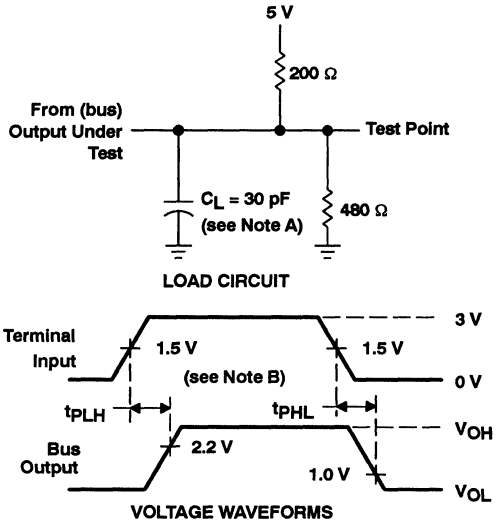


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

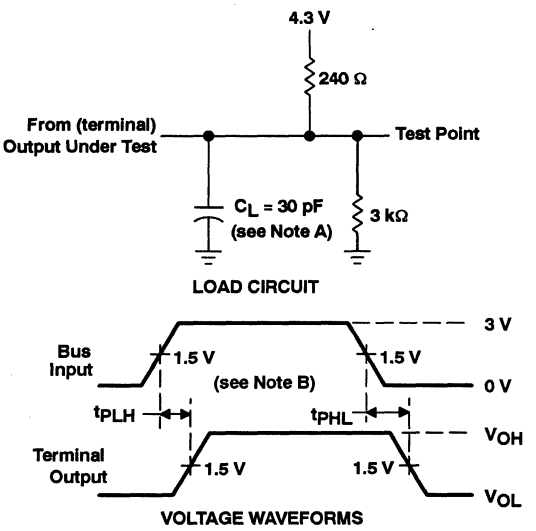
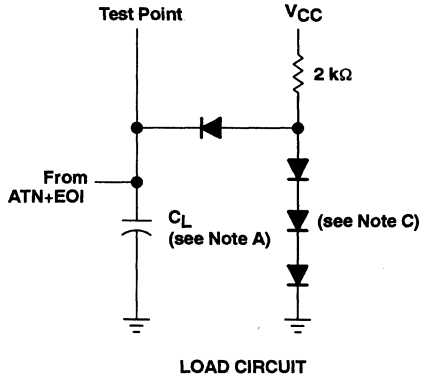


Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms



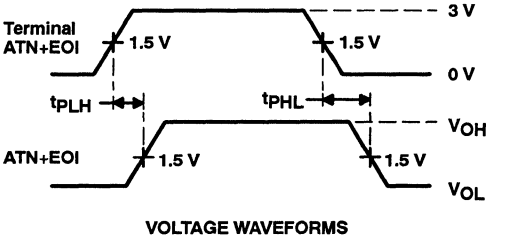


Figure 3. ATN+EOI Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

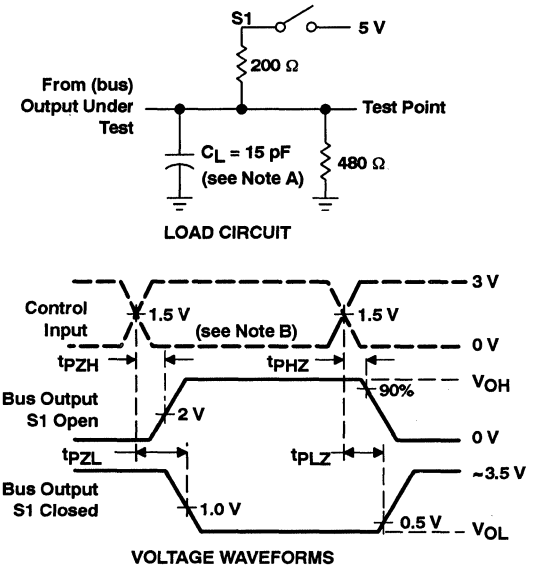


Figure 4. Bus Enable and Disable Times Load Circuit and Voltage Waveforms

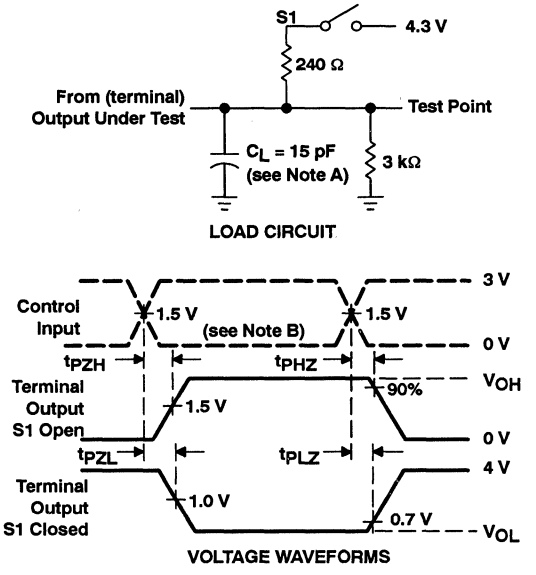


Figure 5. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

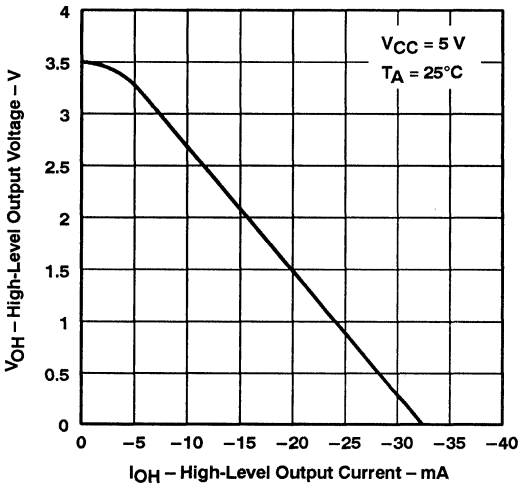


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

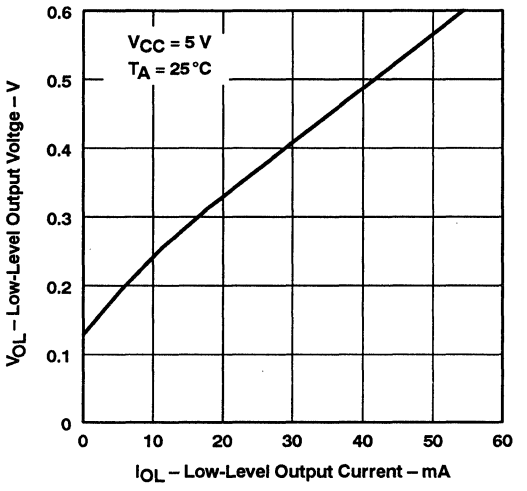


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

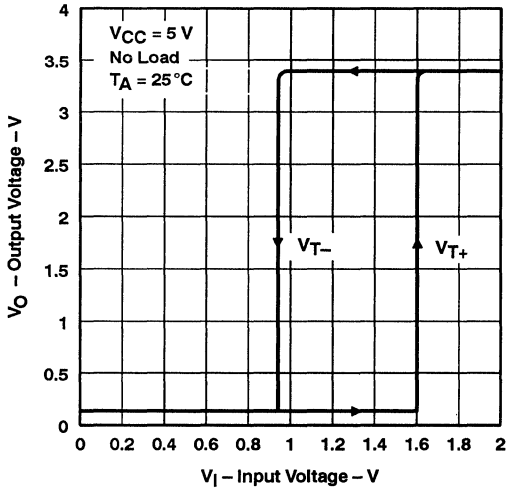


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

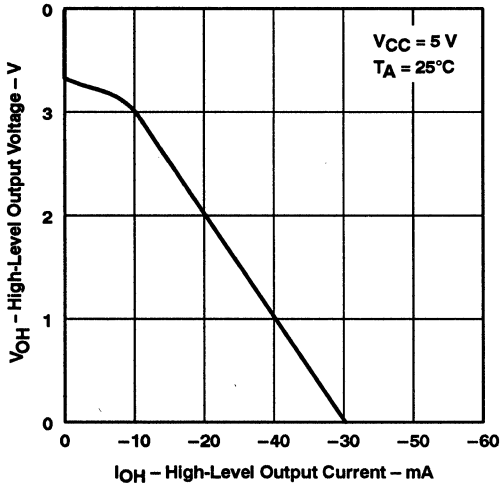


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

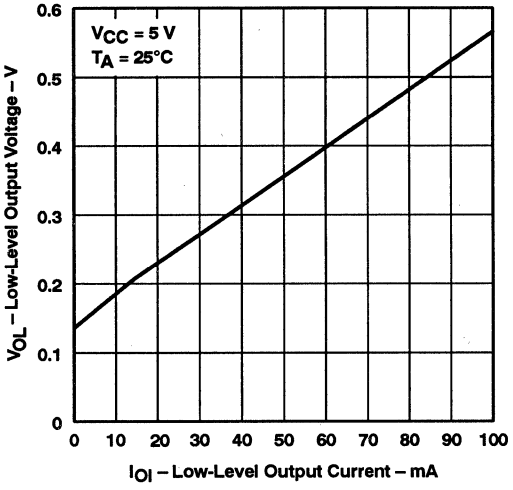


Figure 10

BUS OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

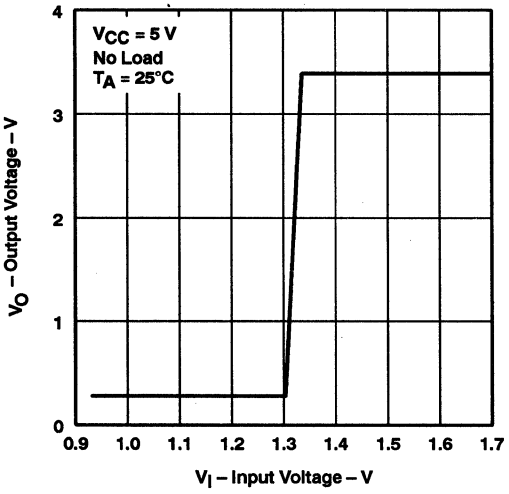


Figure 11

BUS CURRENT
vs
BUS VOLTAGE

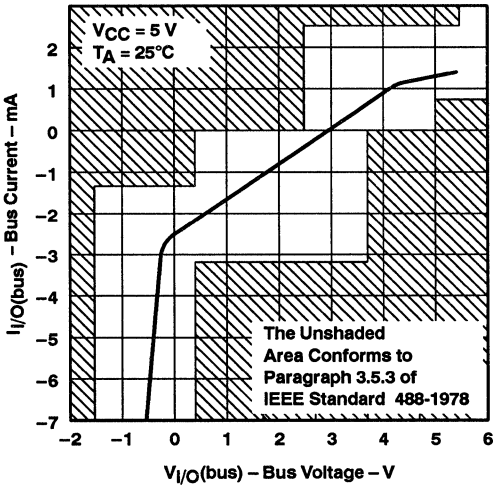
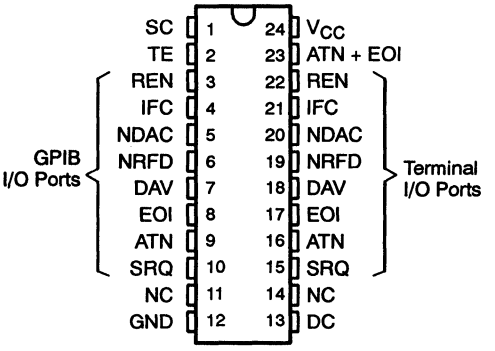


Figure 12

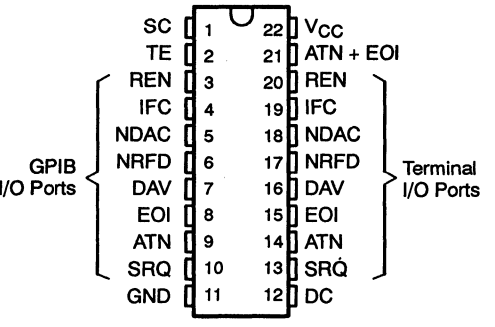
SLLS022B – D2908, JUNE 1986 – REVISED AUGUST 1989

- **8-Channel Bidirectional Transceiver**
- **Designed to Implement Control Bus Interface**
- **Designed for Multicontrollers**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low-Power Dissipation . . . 46 mW Max Per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**

DW PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75ALS164 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS164 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS164 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75ALS164 is identical to the SN75ALS162 with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to provide the ATN + EOI output, which is a standard totem-pole output.

NOT RECOMMENDED FOR NEW DESIGN

CHANNEL IDENTIFICATION TABLE

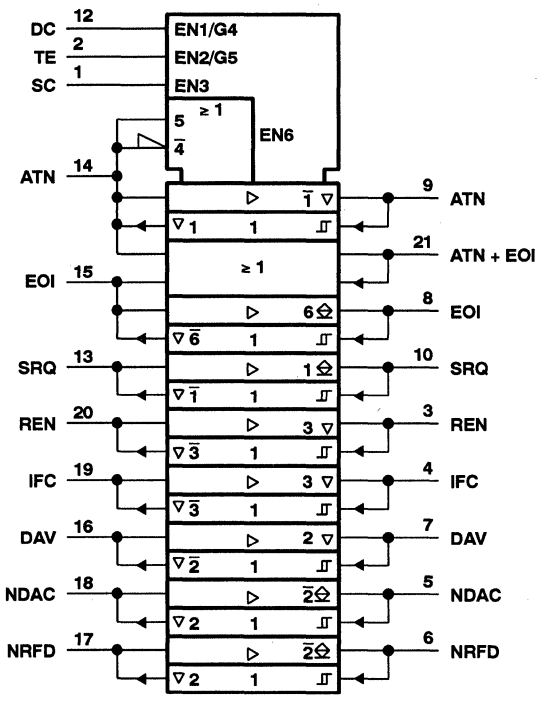
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
ATN+EOI	ATN Logical or EOI	Logic
DAV	Data Valid	Data Transfer
NDAC	No Data Accepted	
NRFD	Not Ready for Data	

description (continued)

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

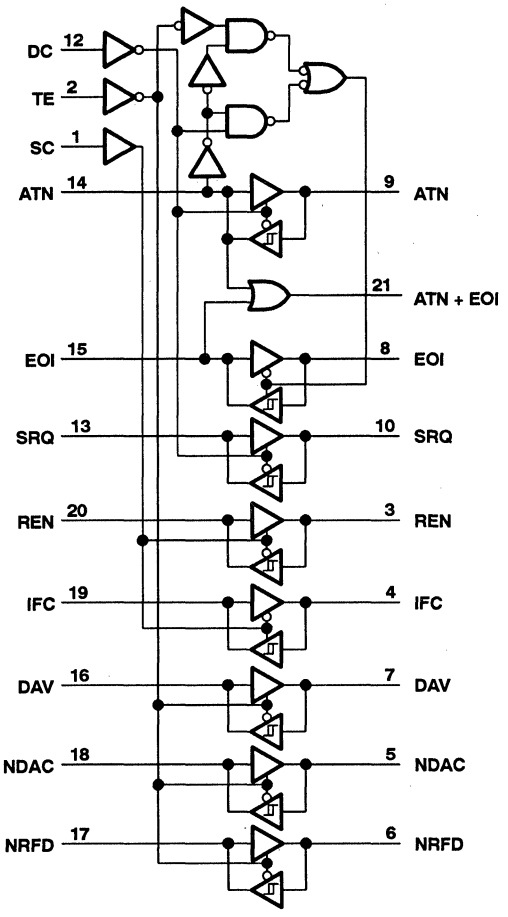
The SN75ALS164 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

logic diagram (positive logic)



Pin numbers shown are for the N package.

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (controlled by DC)	SRQ (controlled by DC)	REN (controlled by SC)	IFC (controlled by SC)	EOI	DAV (controlled by TE)	NDAC (controlled by TE)	NRFD (controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

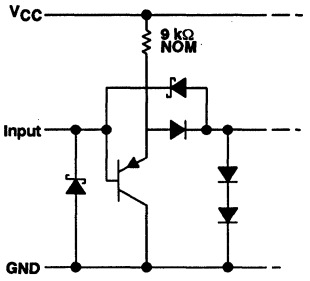
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

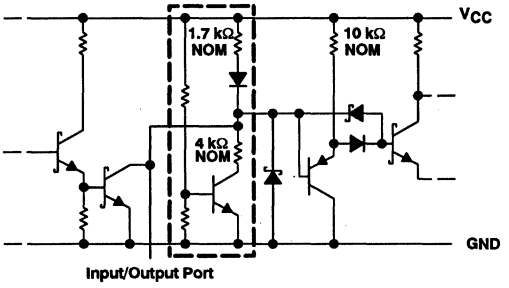
INPUTS		OUTPUT
ATN	EOI	ATN + EOI
H	X	H
X	H	H
L	L	L

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

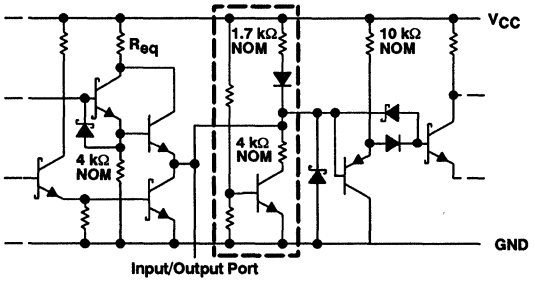


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



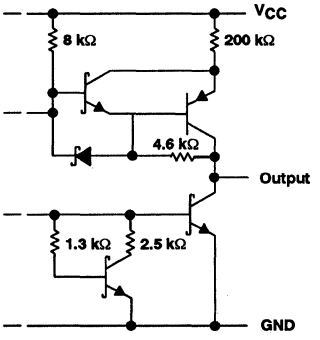
Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, AND NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.,

ATN + EOI OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
N	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			– 5.2	mA
	Terminal ports			– 800	µA
	ATN + EOI			– 400	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	mA
	ATN + EOI			4	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA			– 0.8	–1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = – 800 µA		2.7	3.5		V
		Bus	I_{OH} = – 5.2 mA		2.5	3.3		V
		ATN+EOI	I_{OH} = – 400 µA		2.7			V
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	V
		ATN+EOI	I_{OL} = 4 mA				0.4	V
I_I	Input current at maximum input voltage	Terminal§	V_I = 5.5 V			0.2	100	µA
		ATN, EOI	V_I = 5.5 V				200	µA
I_{IH}	High-level input current	Terminal control	V_I = 2.7 V			0.1	20	µA
		ATN, EOI	V_I = 2.7 V				40	µA
I_{IL}	Low-level input current	Terminal control	V_I = 0.5 V			–10	–100	µA
		ATN, EOI	V_I = 0.5 V				– 500	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = –12 mA			–1.5	V
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = –1.5 V to 0.4 V	–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		– 3.2	mA
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+ 2.5 – 3.2	mA
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	mA
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	mA
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			– 40	µA
I_{OS}	Short-circuit output current	Terminal			–15	– 35	– 75	mA
		Bus			– 25	– 50	–125	mA
		ATN + EOI			–10		–100	mA
I_{CC}	Supply current		No load,	TE, DC, and SC low		55	75	mA
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies for 3-state outputs only.
§ Except ATN and EOI terminals.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN+EOI	C_L = 15 pF, See Figure 3		3.5	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN+EOI	C_L = 15 pF, See Figure 3		7	15	ns
t_{PZH}	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

PARAMETER MEASUREMENT INFORMATION

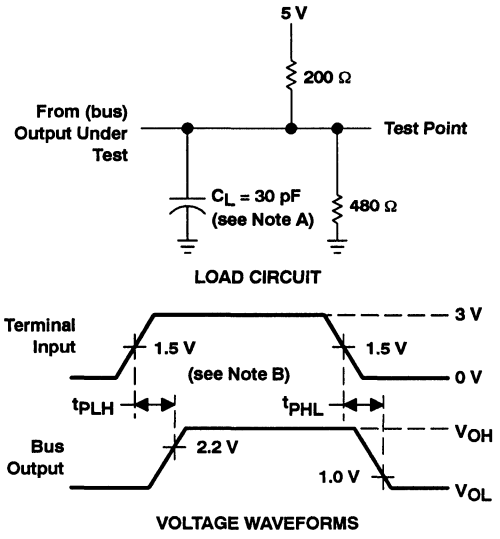


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

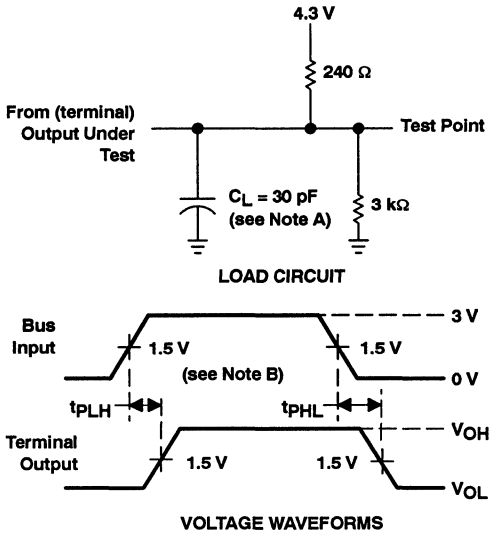
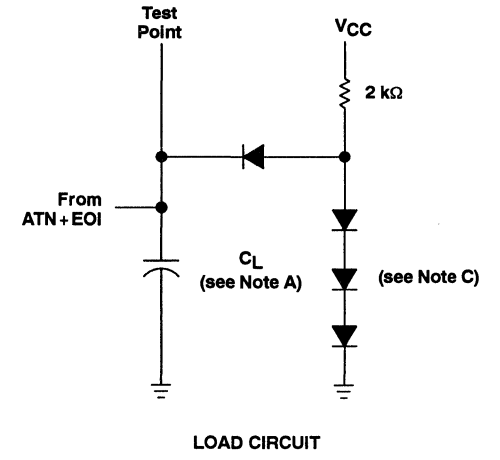


Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms



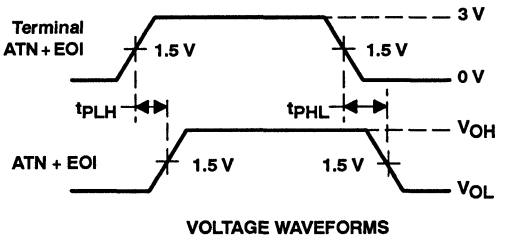
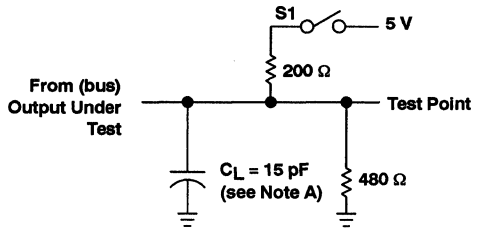


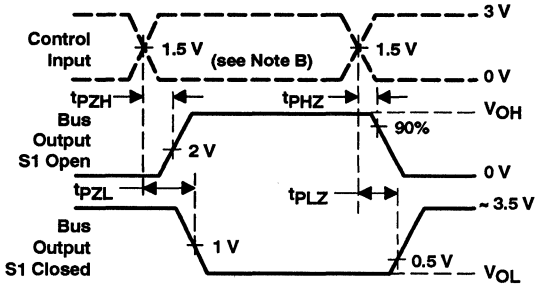
Figure 3. ATN + EOI Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
C. All diodes are 1N916 or 1N3064

PARAMETER MEASUREMENT INFORMATION

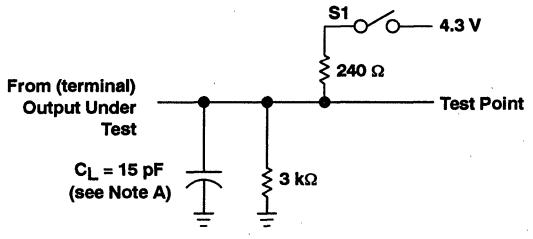


LOAD CIRCUIT

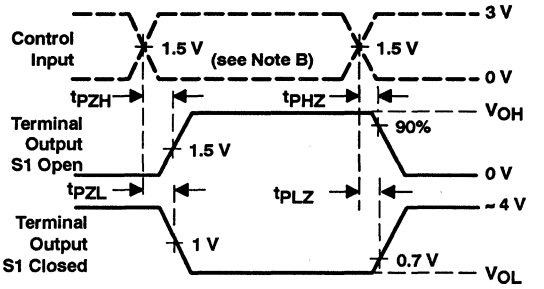


VOLTAGE WAVEFORMS

Figure 4. Bus Load Circuit and Voltage Waveforms



LOAD CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

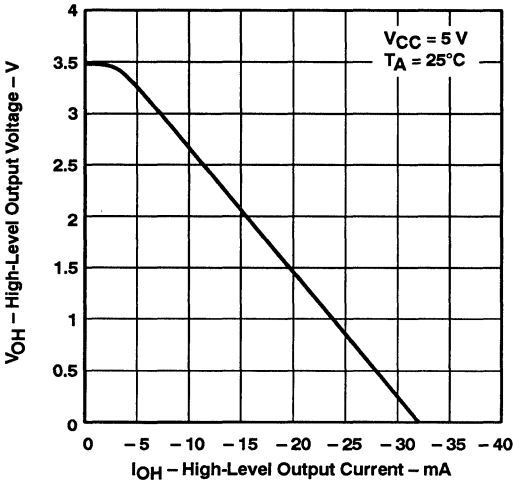


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

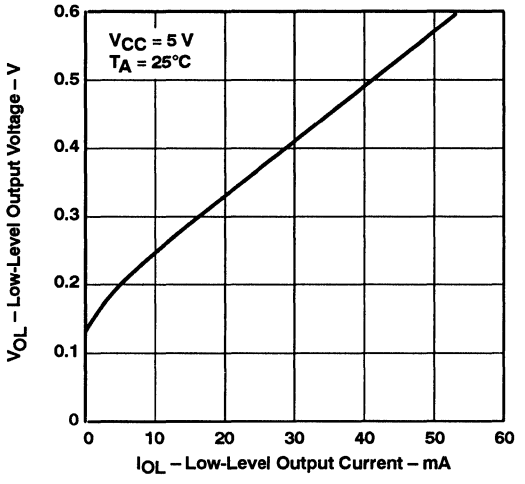


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

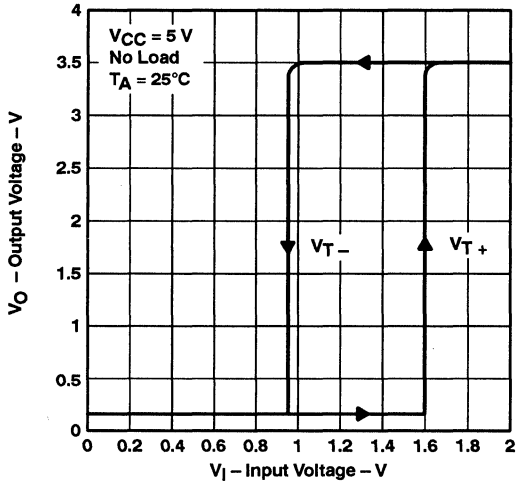


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

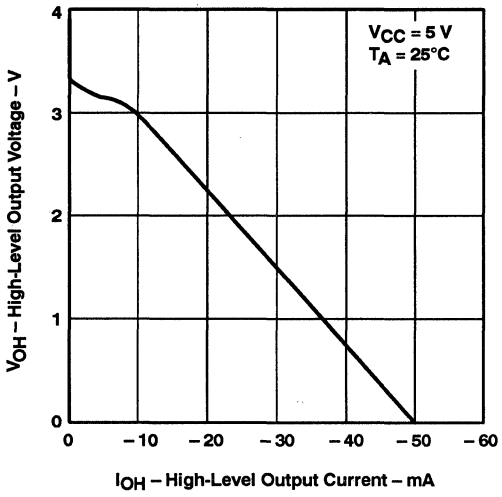


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

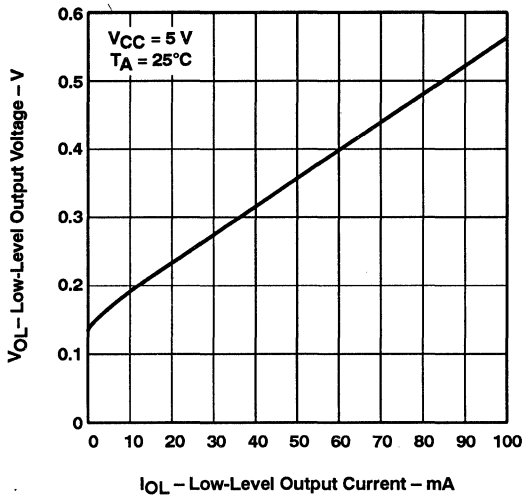


Figure 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

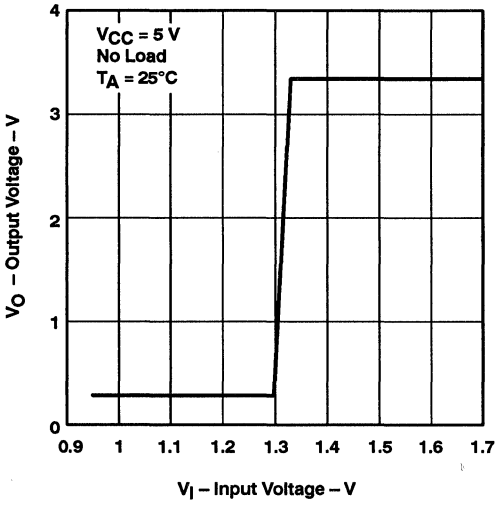


Figure 11

BUS CURRENT
vs
BUS VOLTAGE

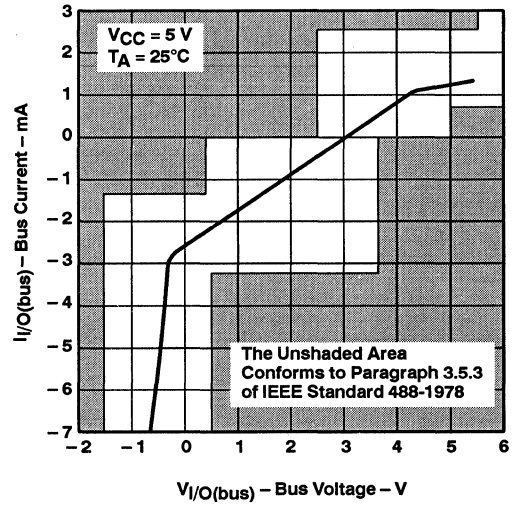


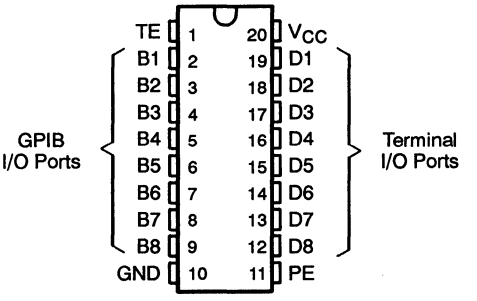
Figure 12

SLLS023B – D3011, JUNE 1986 – REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

- **8-Channel Bidirectional Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 46 mW Max Per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Driver and Receiver Can Be Disabled Simultaneously**

DW OR N PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGN

description

The SN75ALS165 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated ineither the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. Taking TE and PE low places both the drivers and receivers in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

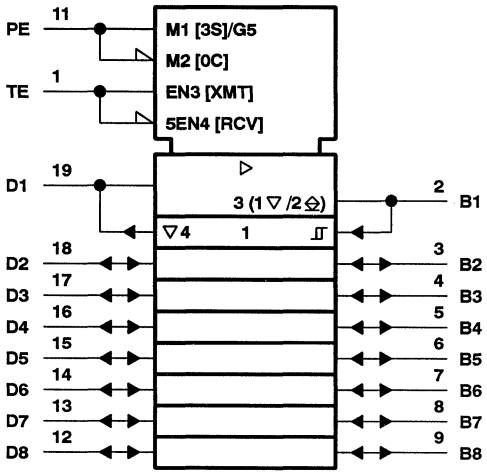
INPUTS			OUTPUT
B	TE	PE	D
L	L	H	L
H	L	H	H
X	H	X	Z
X	X	L	Z

H = high level, L = low level, X = irrelevant,
Z = high-impedance state
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

An active turn-off feature is incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

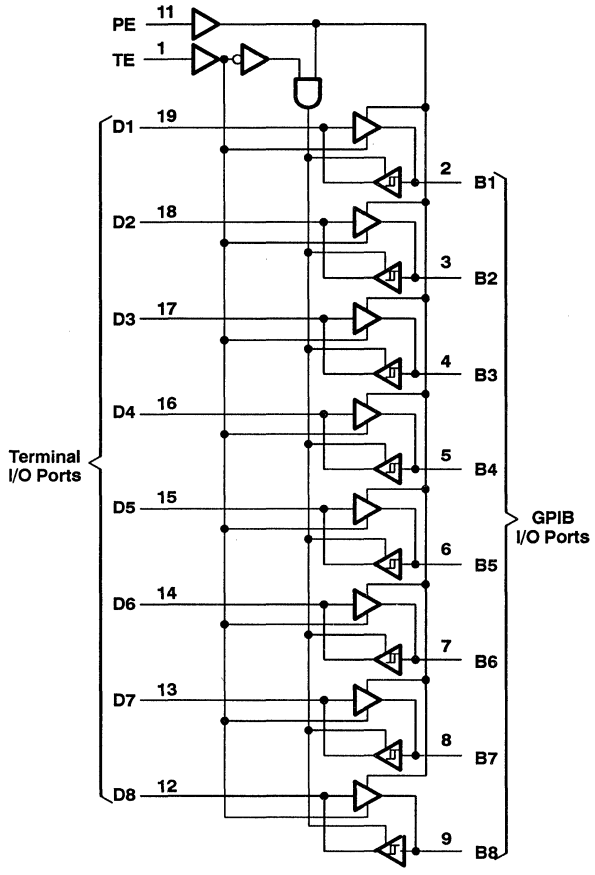
The SN75ALS165 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

logic diagram (positive logic)



TEXAS INSTRUMENTS
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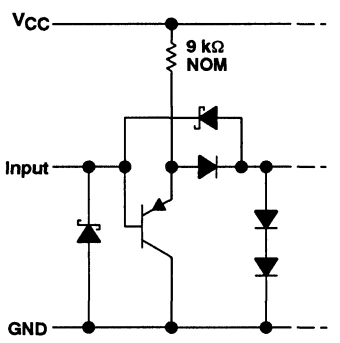
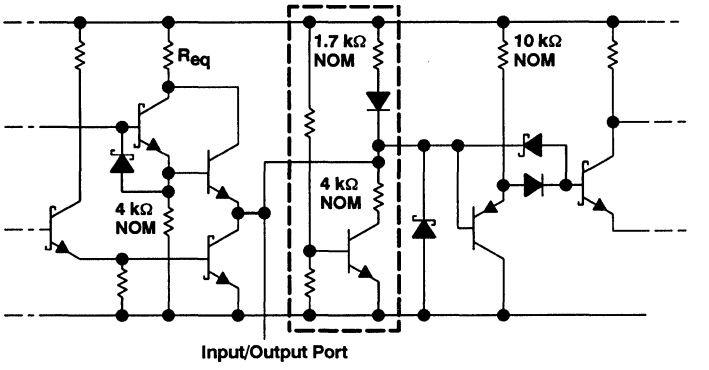
schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Low-level driver output current ..... 100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18$ mA			−0.8	1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	$I_{OH} = -800$ µA,	TE at 0.8 V	2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16$ mA,	TE at 0.8 V		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5$ V			0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7$ V			0.1	20	µA
I_{IL}	Low-level input current		$V_I = 0.5$ V			−10	−100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)} = 0$	2.5	3	3.7	V
				$I_{I(bus)} = -12$ mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)} = -1.5$ V to 0.4 V	−1.3			mA
				$V_{I(bus)} = 0.4$ V to 2.5 V	0		−3.2	
				$V_{I(bus)} = 2.5$ V to 3.7 V			2.5 −3.2	
				$V_{I(bus)} = 3.7$ V to 5 V	0		2.5	
				$V_{I(bus)} = 5$ V to 5.5 V	0.7		2.5	
		Power off	$V_{CC} = 0$,	$V_{I(bus)} = 0$ to 2.5 V			40	µA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	65	mA
				Bus outputs low and enabled		52	80	
$C_{I/O(bus)}$	Bus-port capacitance		$V_{CC} = 5$ V to 0,	$V_{I/O} = 0$ to 2 V, f = 1 MHz		30		pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ V_{OH} applies for 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pullup enable time	PE	Terminal	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pullup disable time					6	12	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

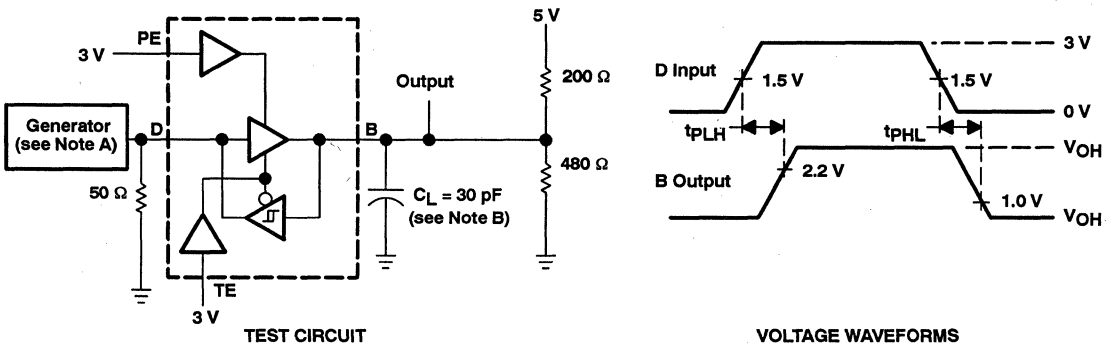


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

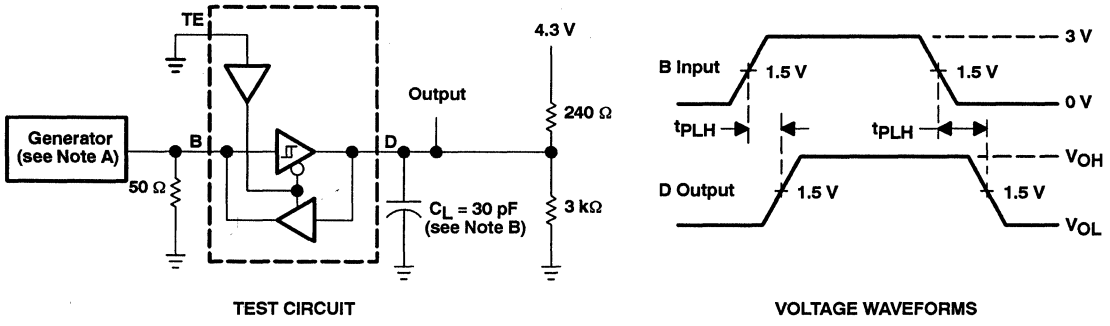


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

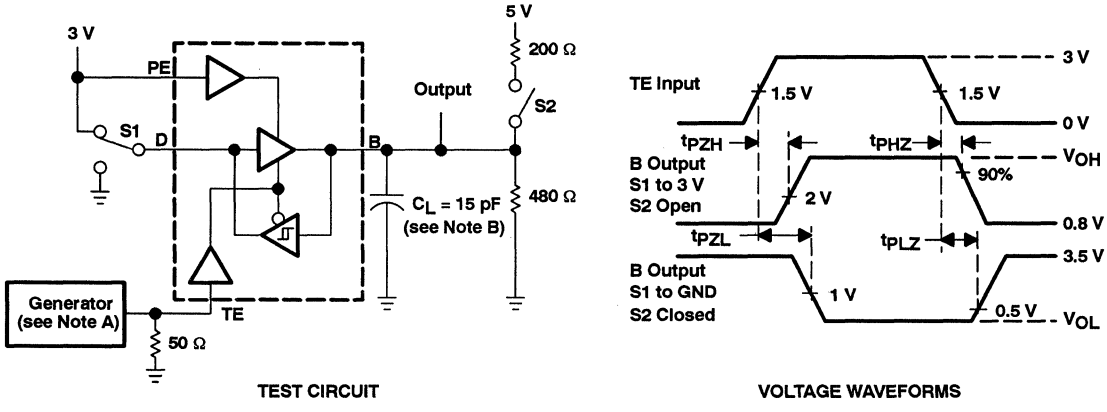
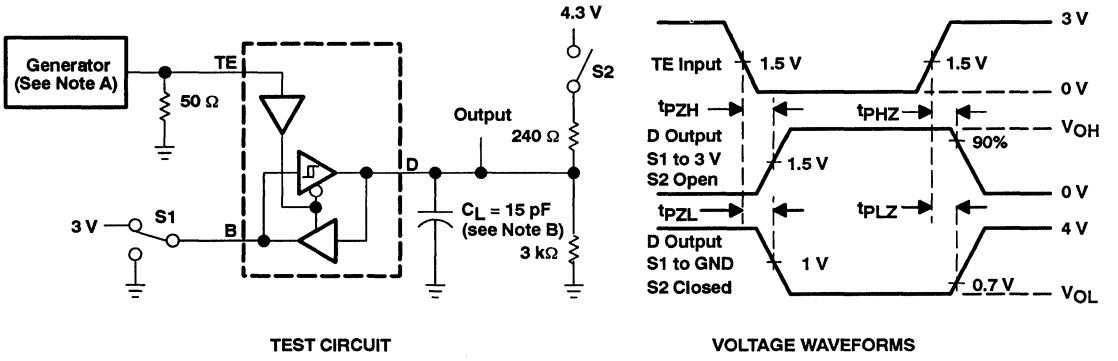


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

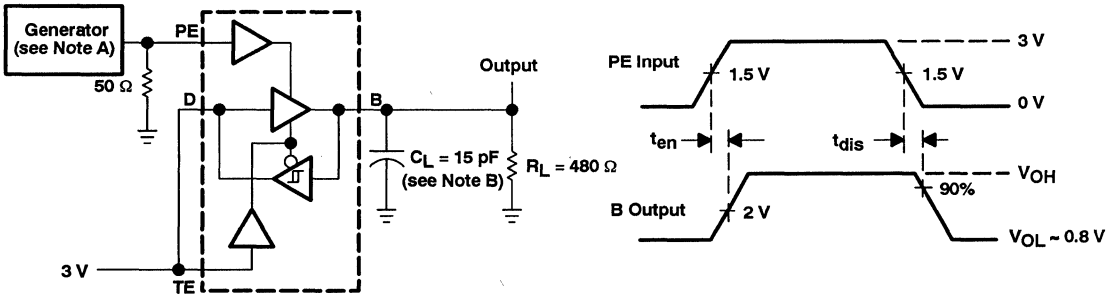
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

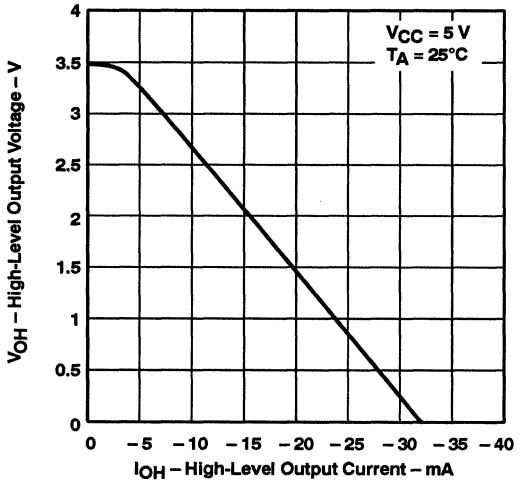


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

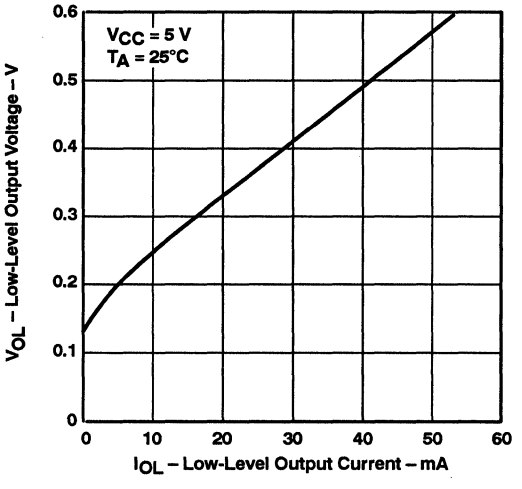


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

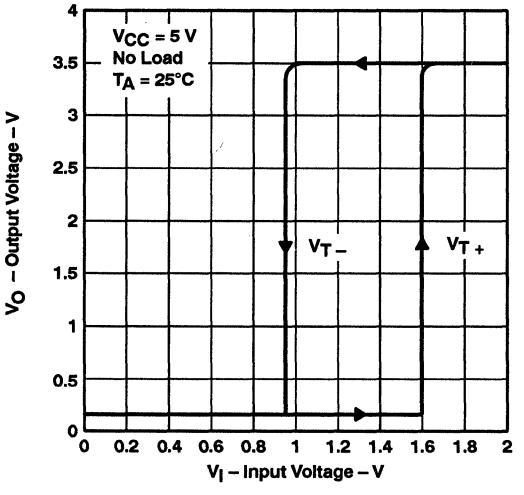


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

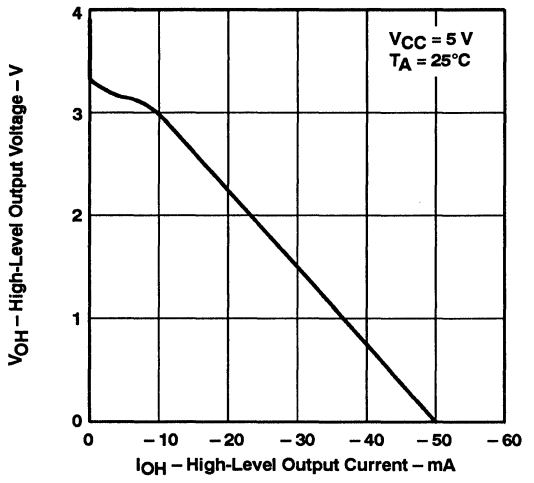


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

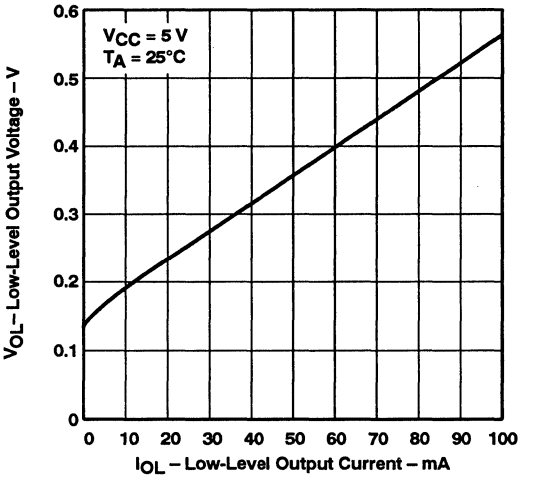


Figure 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

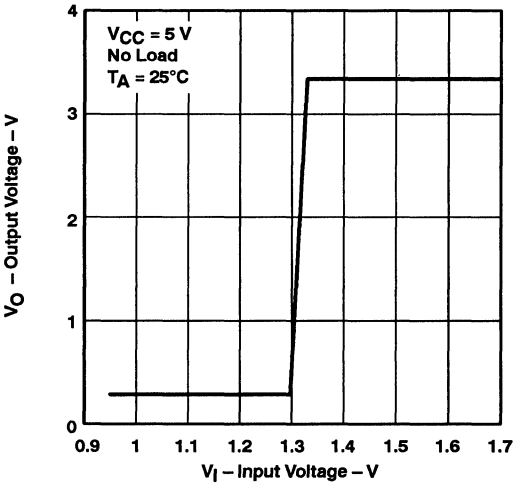


Figure 11

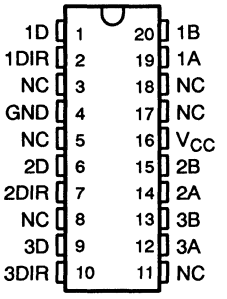
SLLS055B – D3040, AUGUST 1987 – REVISED FEBRUARY 1993

- Three Bidirectional Transceivers
- Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation In Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments
- Low Supply Current Requirements 90 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Features Independent Direction Controls for Each Channel

description

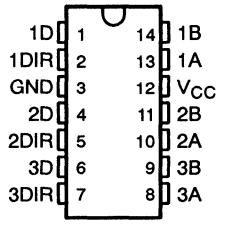
The SN75ALS170 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

DW PACKAGE
(TOP VIEW)



NC – No internal connection

J PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

INPUT D	DIR	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	DIR	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z
Open	L	H

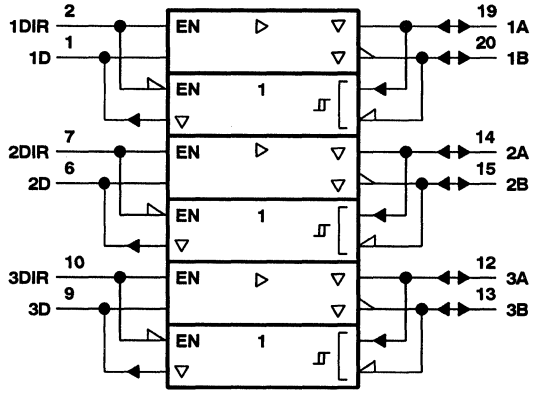
H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

description (continued)

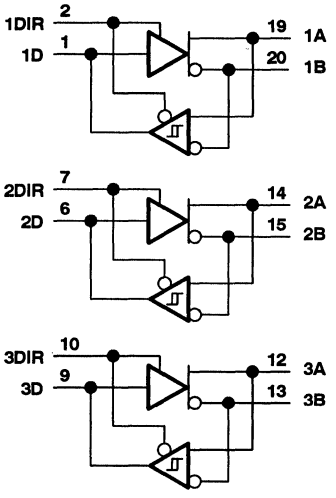
The SN75ALS170 operates from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS170 is characterized for operation from 0°C to 70°C.

logic symbol†



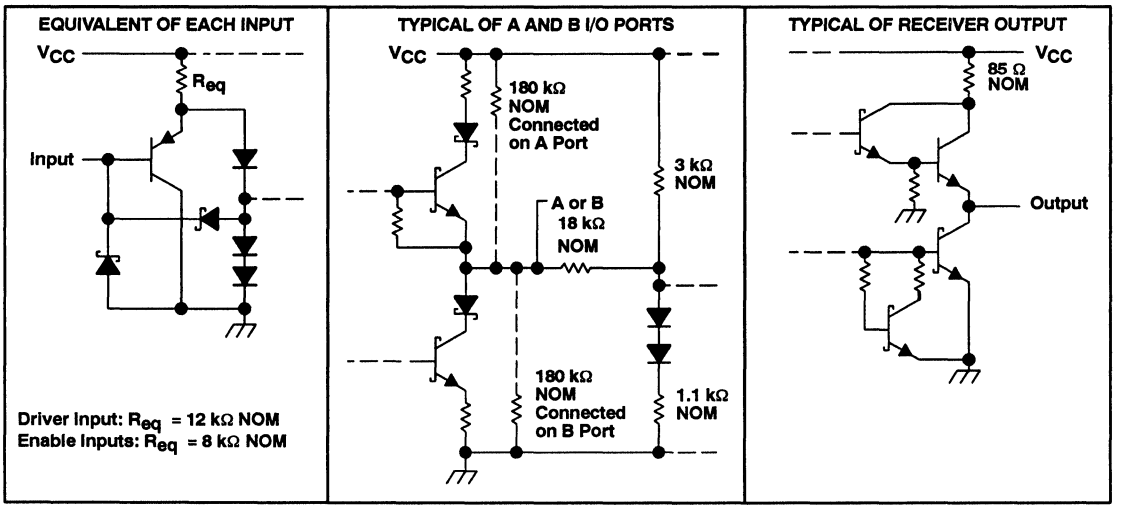
logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DIR	2			V
Low-level input voltage, V_{IL}	D, DIR			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -19$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2V_{OD1} or 2#			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 540 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current¶	V_O = −6 V				−250	mA
		V_O = 0 V				−150	
		$V_O = V_{CC}$				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short-circuit current should not exceed one second.
# The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4	3	8	13	
	Skew ($\lvert t_{dDH} - t_{dDL} \rvert$)	R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	6	ns
		R_{L1} = R_{L3} = 165 Ω C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4		1	6	
t_{tD}	Differential-output transition time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		R_{L1} = R_{L3} = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4	3	8	13	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_O	V_O
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 5	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 5	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 2.4 V				20	μA
		V_O = 0.4 V				−400	
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 6	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output		9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			2	6	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

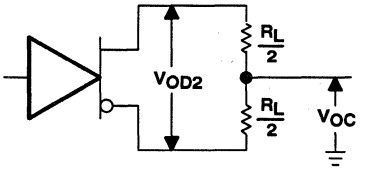


Figure 1. Driver V_{OD} and V_{OC}

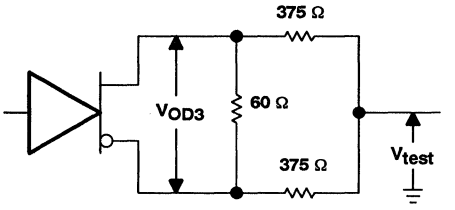
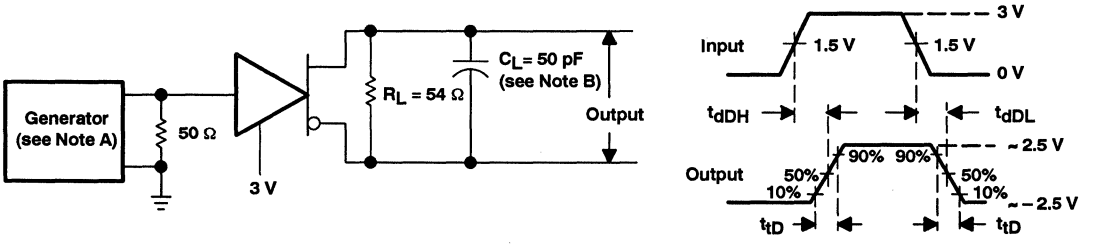


Figure 2. Driver V_{OD3}

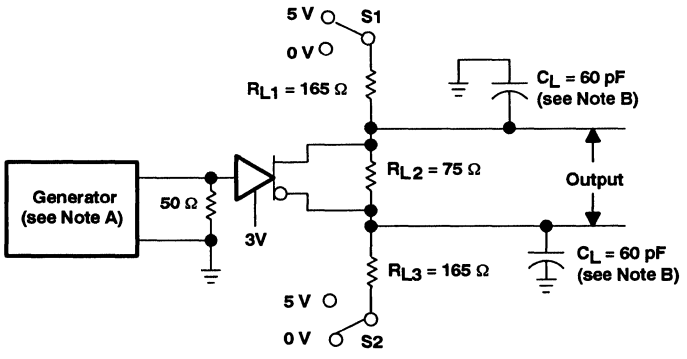


TEST CIRCUIT **VOLTAGE WAVEFORMS**

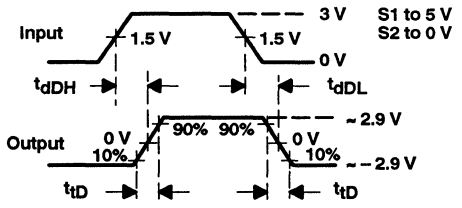
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

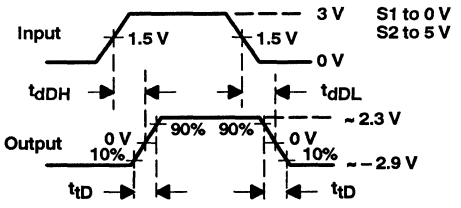
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load

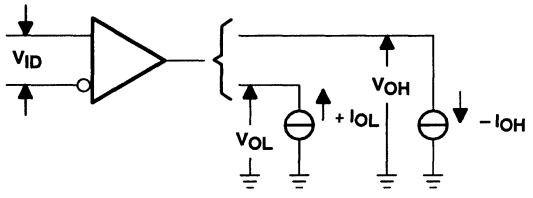
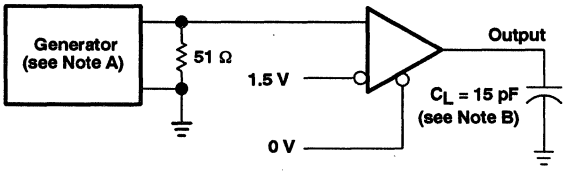
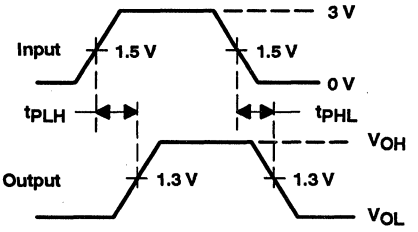


Figure 5. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs DRIVER HIGH-LEVEL OUTPUT CURRENT

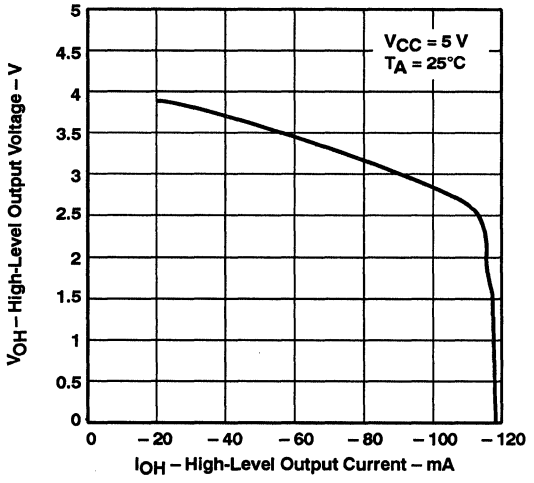


Figure 7

DRIVER LOW-LEVEL OUTPUT VOLTAGE vs DRIVER LOW-LEVEL OUTPUT CURRENT

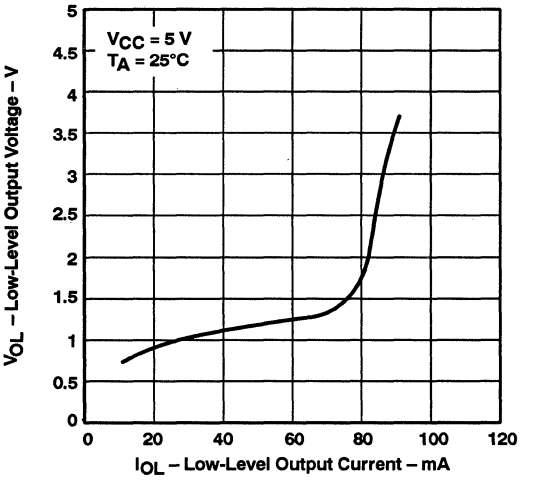


Figure 8

TYPICAL CHARACTERISTICS

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

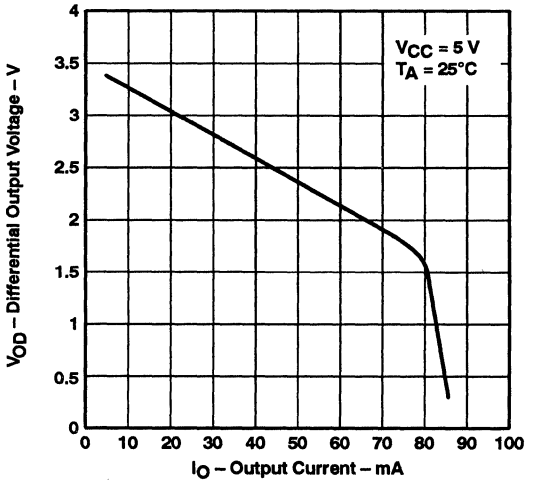


Figure 9

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

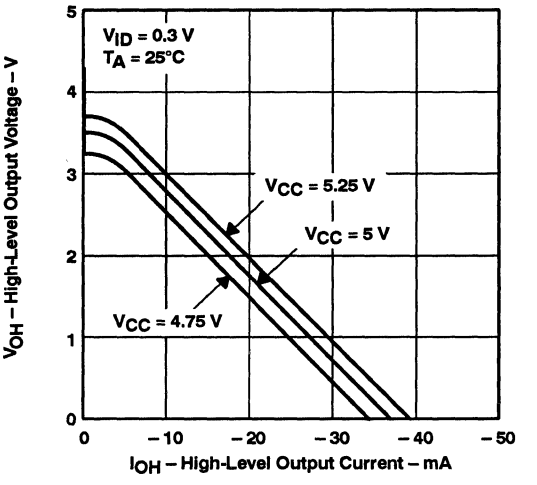


Figure 10

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

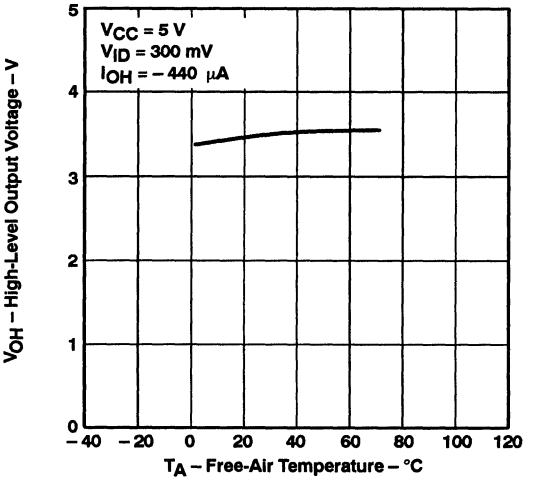


Figure 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

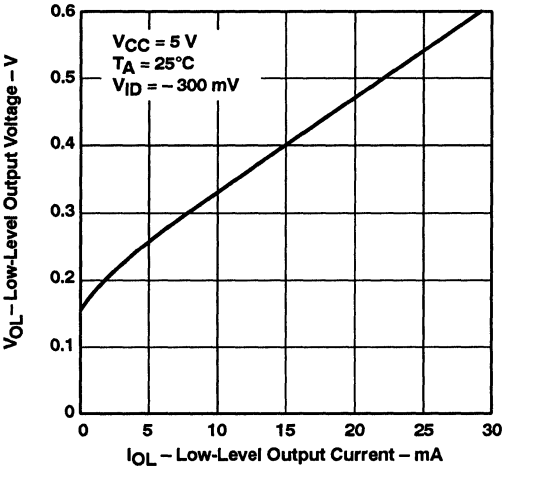


Figure 12

TYPICAL CHARACTERISTICS

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

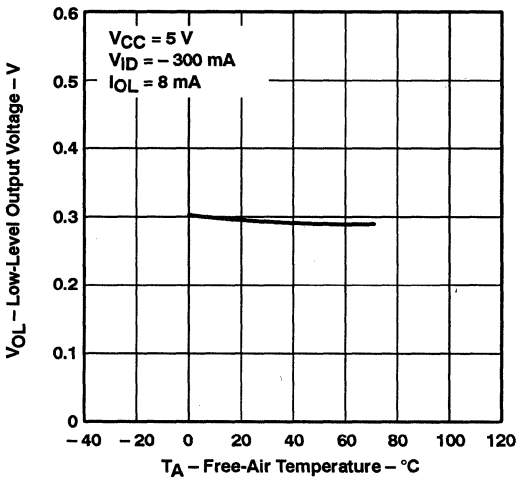


Figure 13

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

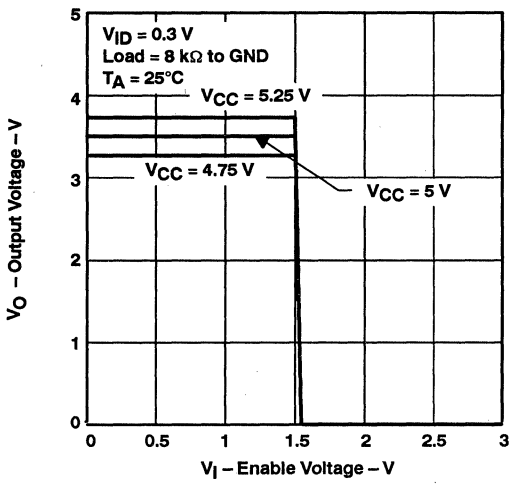


Figure 14

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

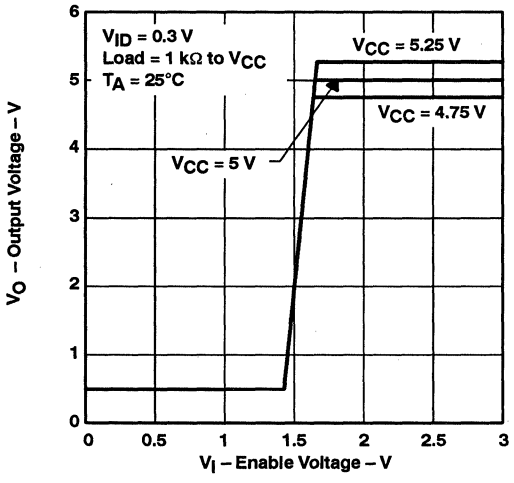
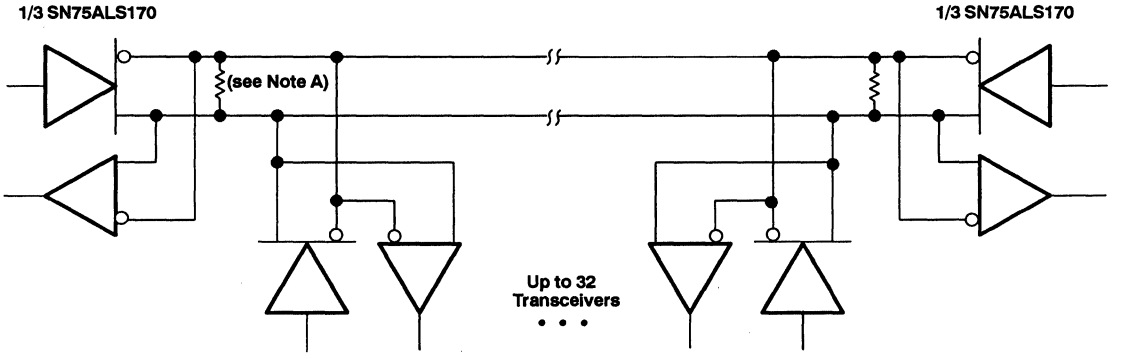


Figure 15

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

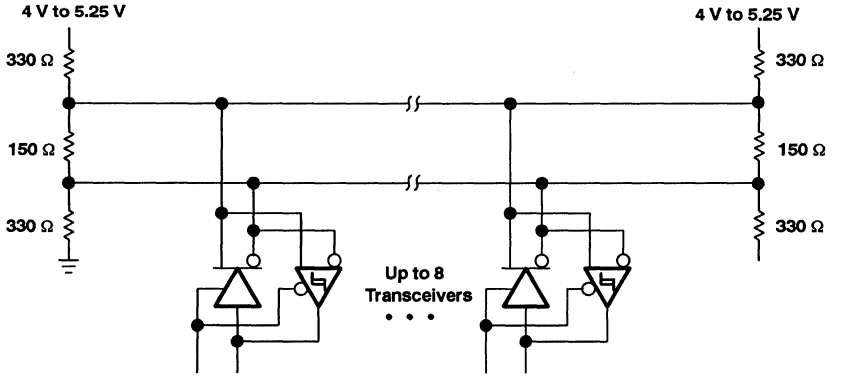


Figure 17. Typical Differential SCSI Application Circuit

APPLICATION INFORMATION

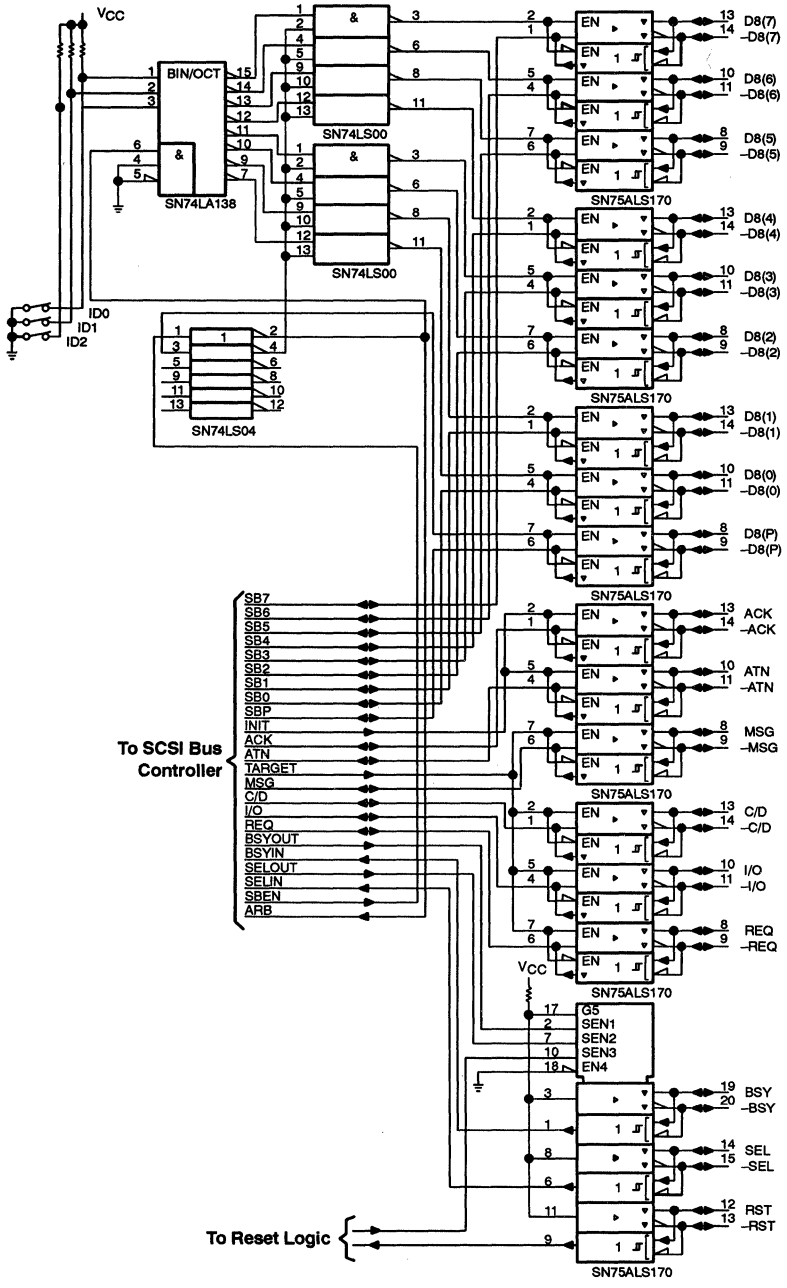
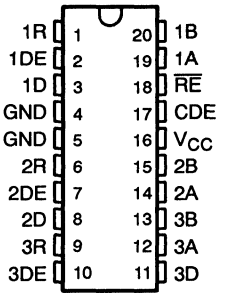


Figure 18. Typical Differential SCSI Bus Interface Implementation

SLLS056B – D3041, AUGUST 1987 – REVISED FEBRUARY 1993

- **Three Bidirectional Transceivers**
- **Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation in Both Serial and Parallel Applications**
- **Low Skew . . . 6 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Features Independent Driver Enables and Combined Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±300 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Low Supply Current Requirements 90 mA Max**

DW OR J PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

INPUT	ENABLE		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

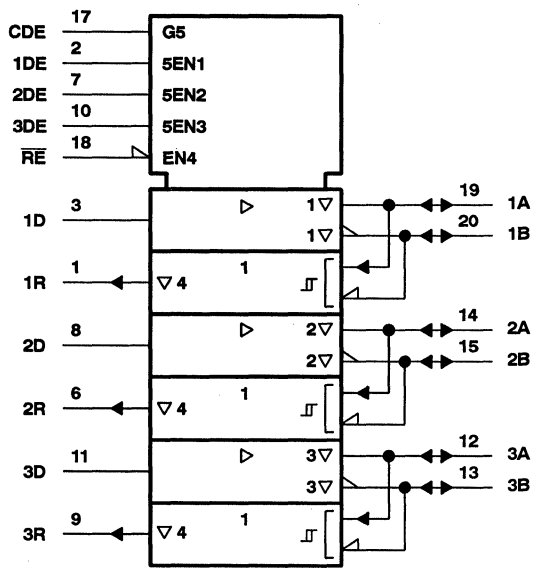
description

The SN75ALS171 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines, and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

The SN75ALS171 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

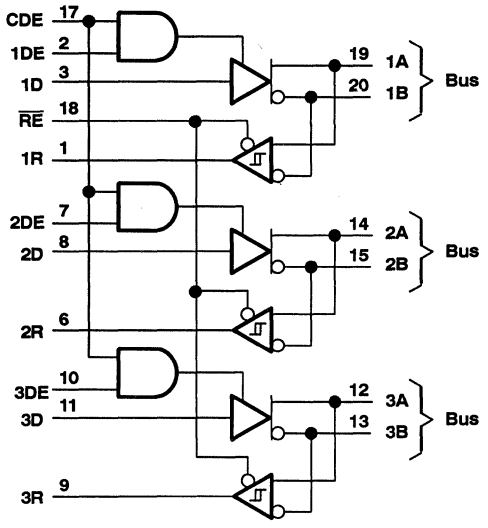
The SN75ALS171 is characterized for operation from 0°C to 70°C.

logic symbol†

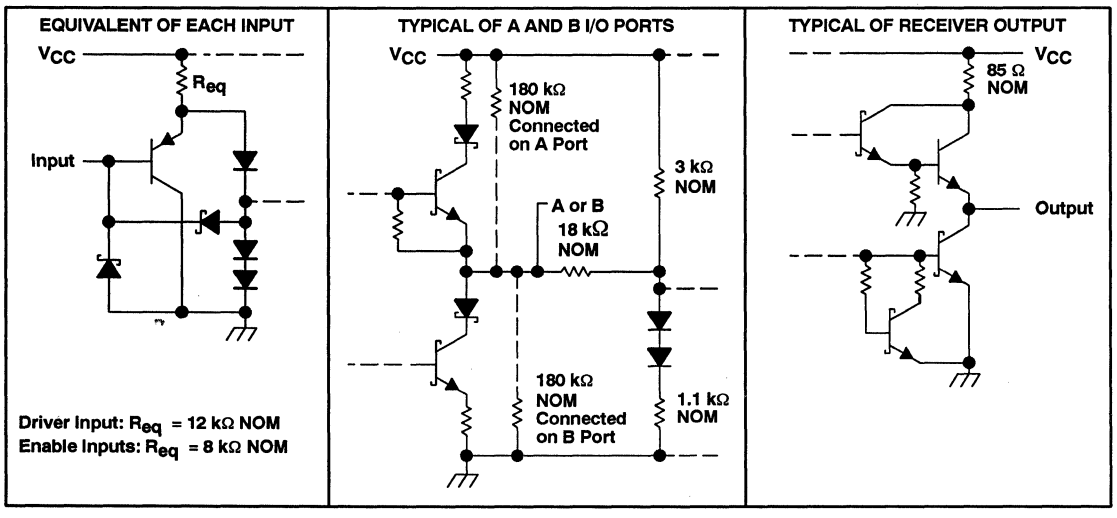


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, CDE, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, CDE, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2V_{OD1} or 2#	2.5	5	V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level enable-input current	D and DE	V_{IH} = 2.7 V			20	μA
		CDE				60	
I_{IL}	Low-level enable-input current	D and DE	V_{IL} = 0.4 V			−100	
		CDE				−900	
I_{OS}	Short-circuit output current¶	V_O = −6 V				−250	mA
		V_O = 0				−150	
		$V_O = V_{CC}$				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ Duration of the short-circuit current should not exceed one second.
# The minimum V_{OD2} with 100-W load is either 1/2 V_{OD2} or 2 V, whichever is greater.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω, See Figure	C_L = 50 pF,	3	8	13	ns
		$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	
	Skew ($\lvert t_{dDH} - t_{dDL} \rvert$)	R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	6	ns
		$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6		1	6	
t_{tD}	Differential-output transition time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
		$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		30	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4	3	8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5	3	8	13	ns
t_{PDE}	Differential-output enable time	$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 7	8	30	45	ns
t_{PDZ}	Differential-output disable time			5	10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta\lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta\lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 8	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 8	I_{OL} = 8 mA			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				60	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−300	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5V to 1.5 V, See Figure 9	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	19	ns
	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

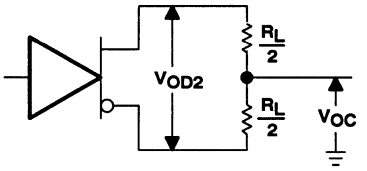


Figure 1. Driver V_{OD} and V_{OC}

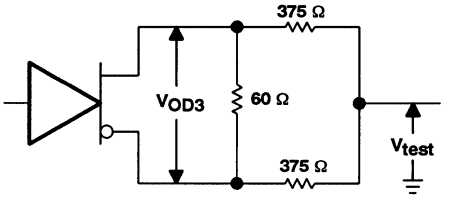
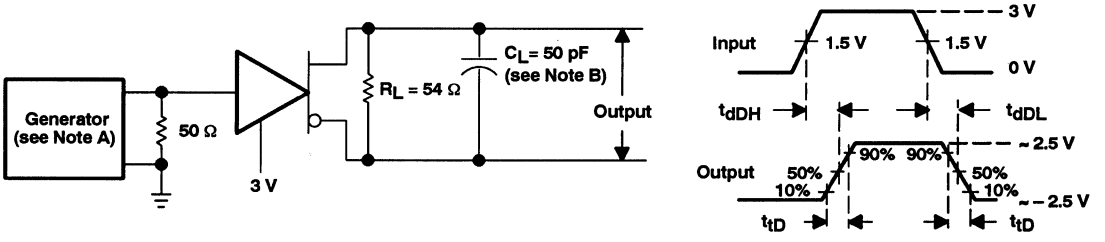


Figure 2. Driver V_{OD3}

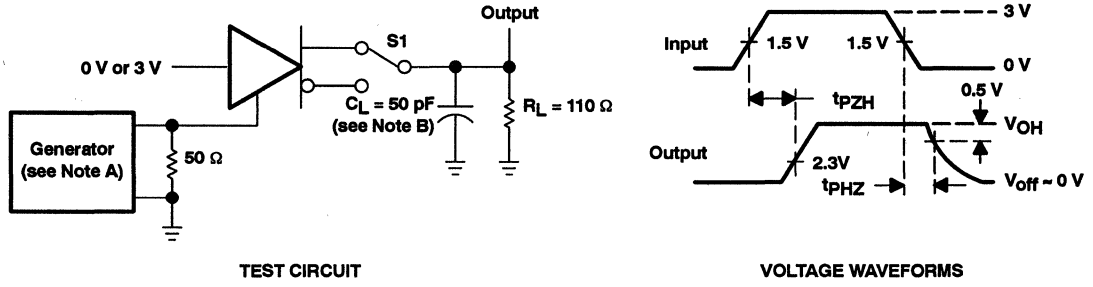


TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms

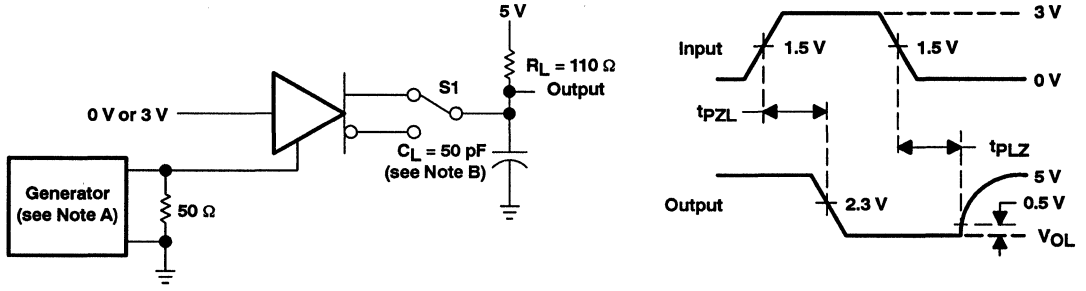
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms

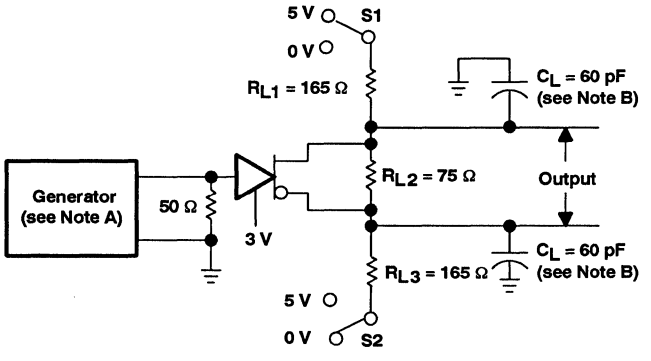


TEST CIRCUIT VOLTAGE WAVEFORMS

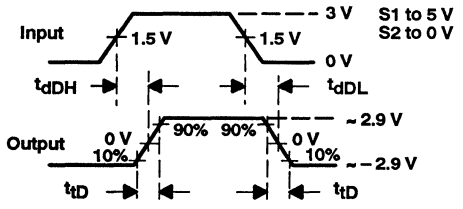
Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

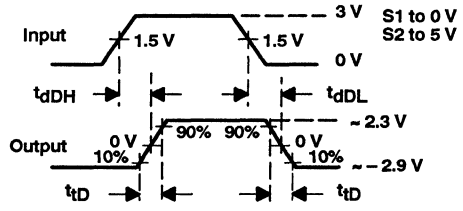
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

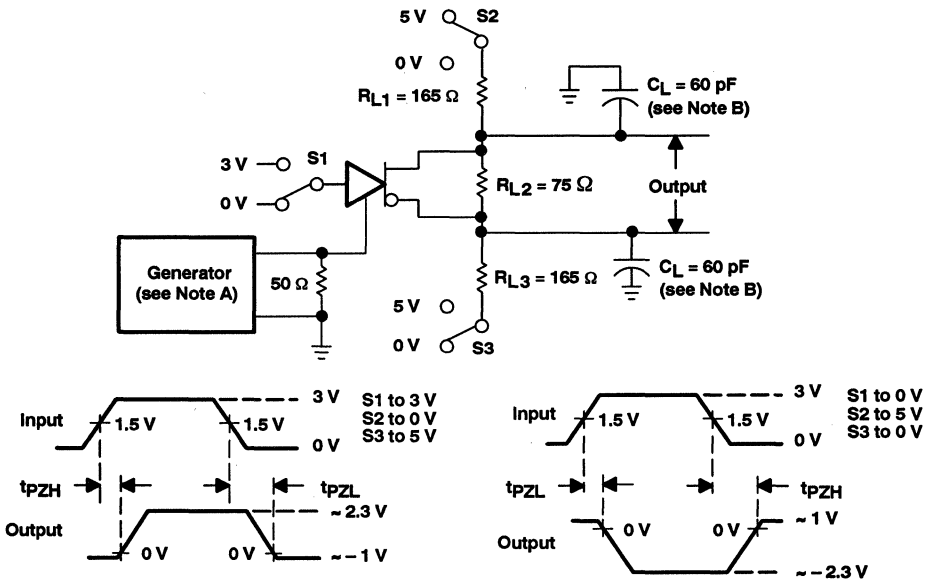


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Driver Differential-Enable and Disable Times With a Double-SCI Termination

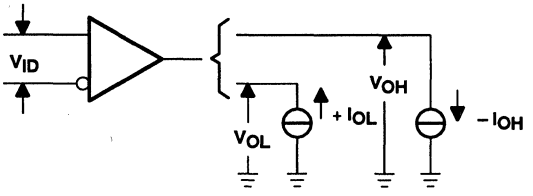


Figure 8. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

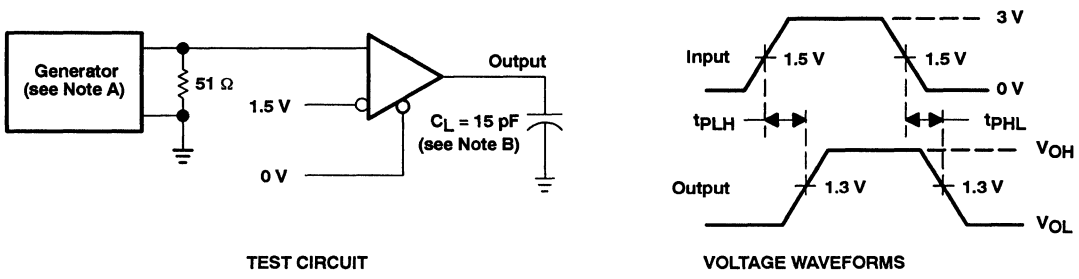


Figure 9. Receiver Test Circuit and Voltage Waveforms

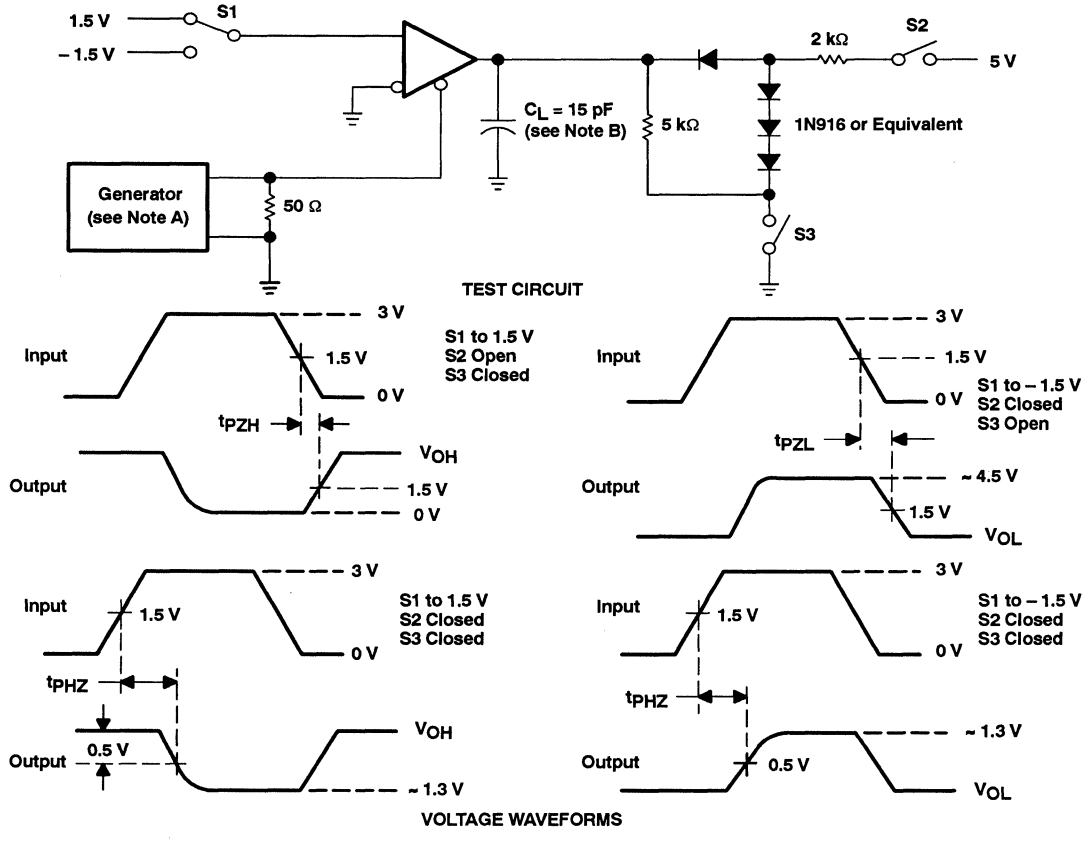


Figure 10. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

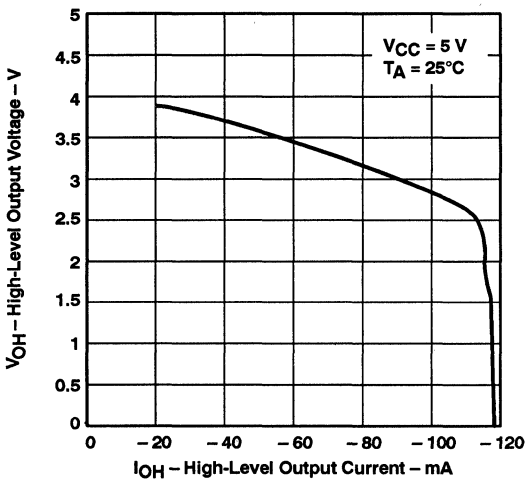


Figure 11

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

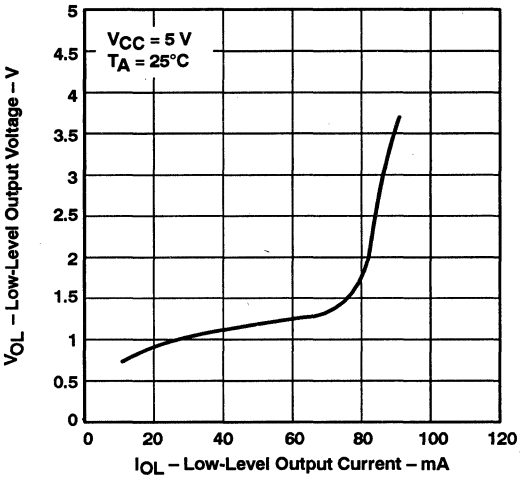


Figure 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

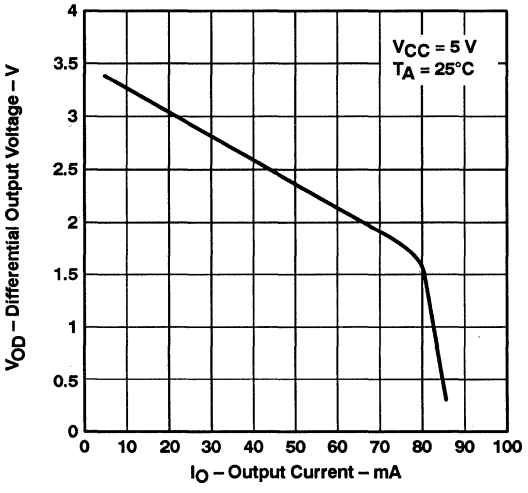


Figure 13

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

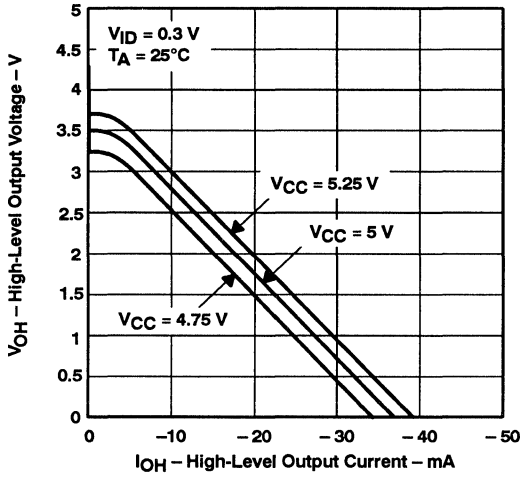


Figure 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

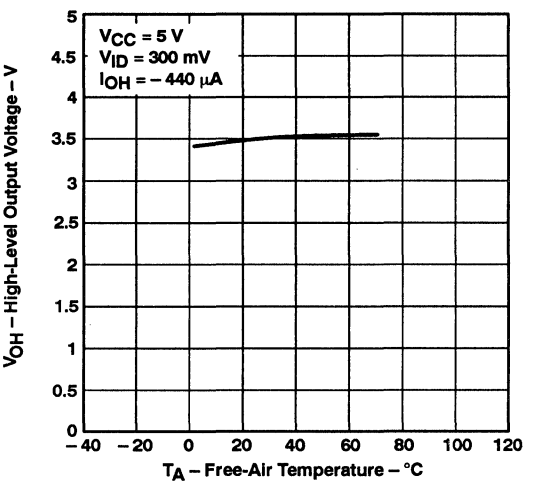


Figure 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

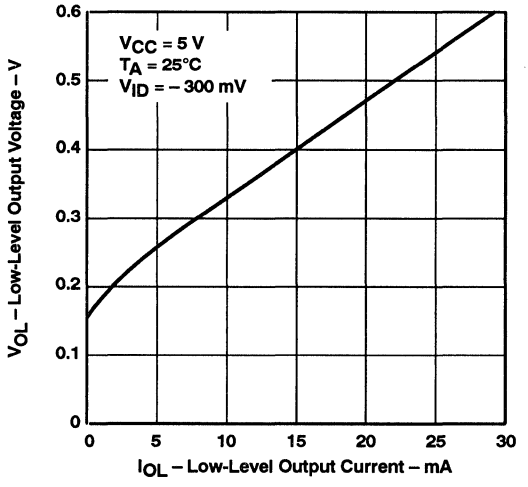


Figure 16

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

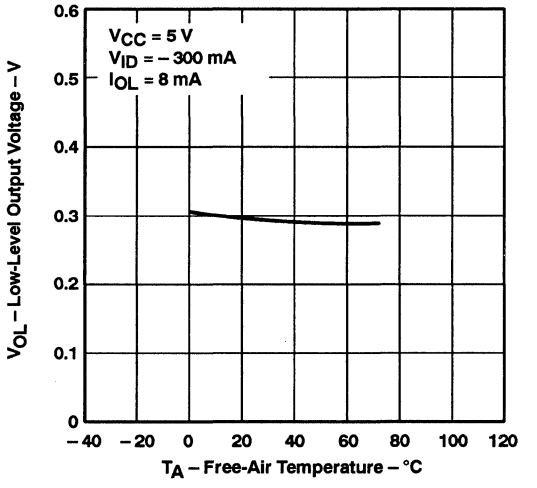


Figure 17

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

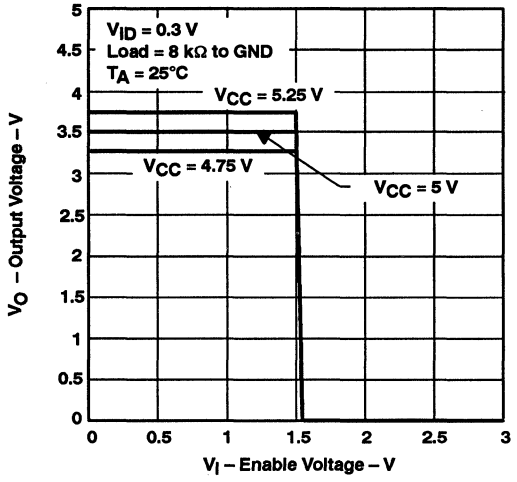


Figure 18

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

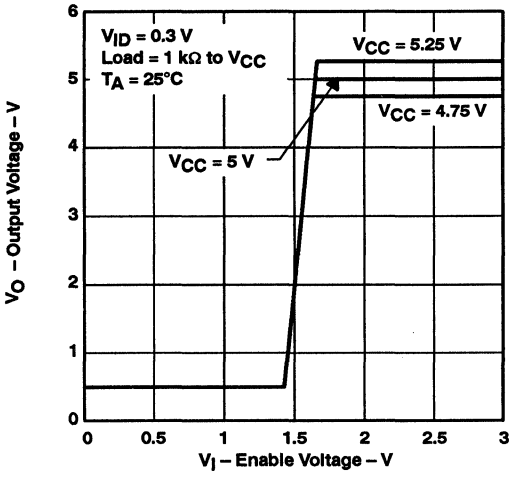
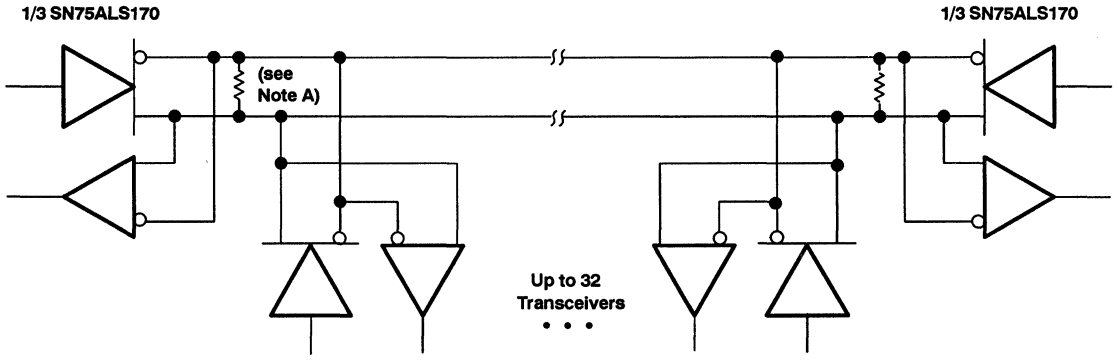


Figure 19

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 20. Typical Application Circuit

APPLICATION INFORMATION

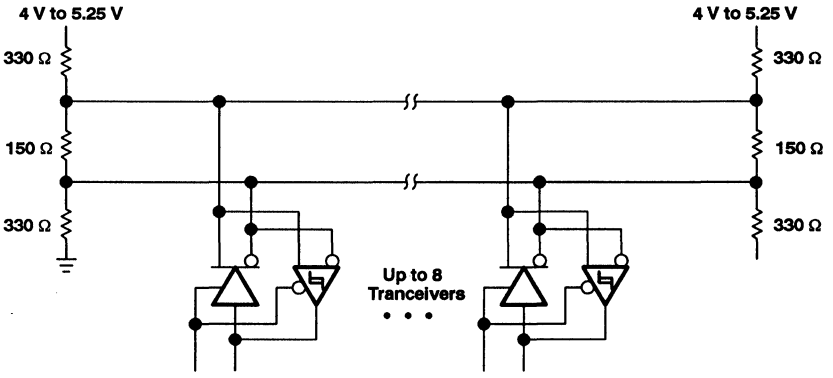


Figure 21. Typical Differential SCSI Application Circuit

APPLICATION INFORMATION

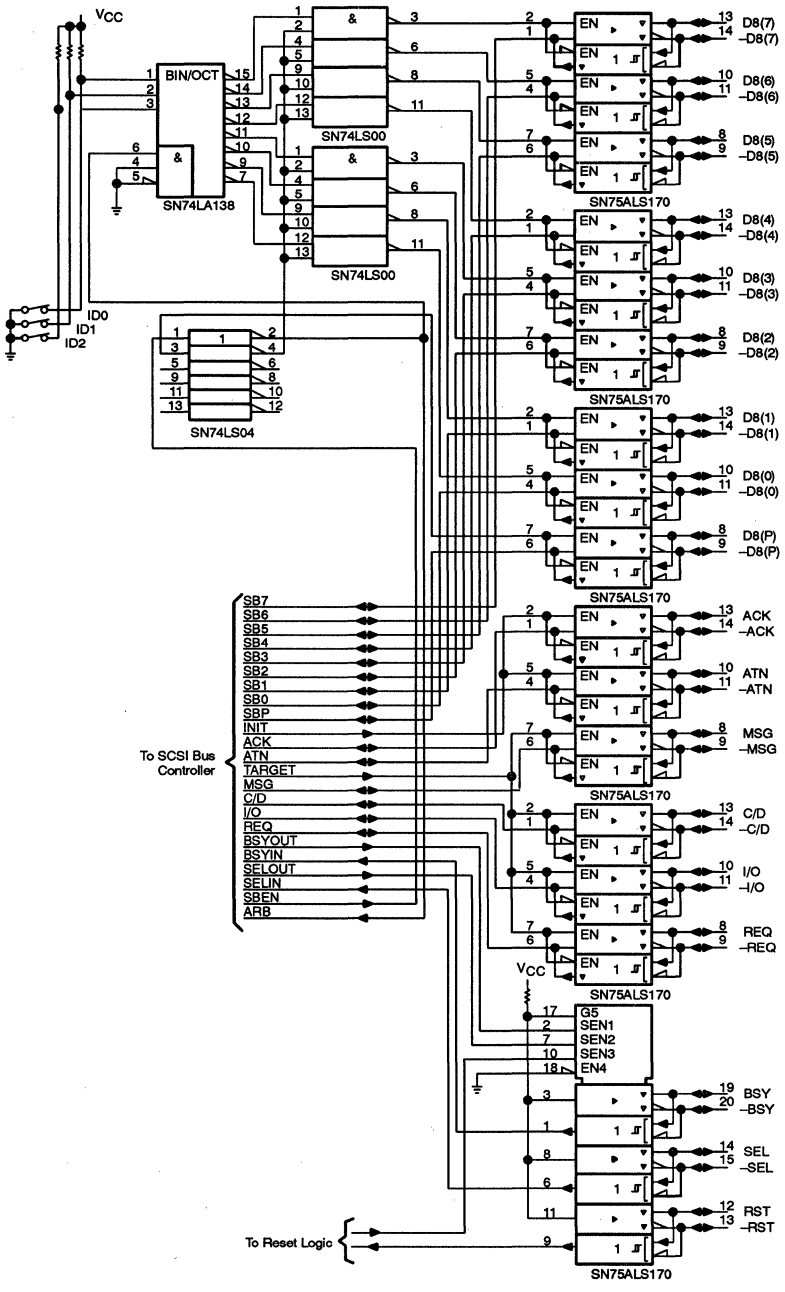
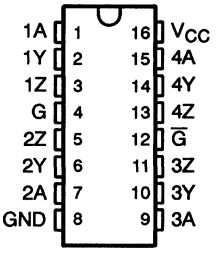


Figure 22. Typical Differential SCSI Bus Interface Implementation

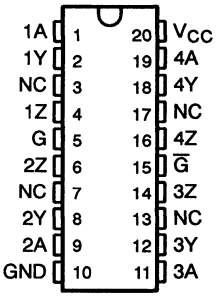
SLLS038A – D2596, OCTOBER 1980 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of −7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable With AM26LS31**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75172 is a monolithic quad differential line driver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

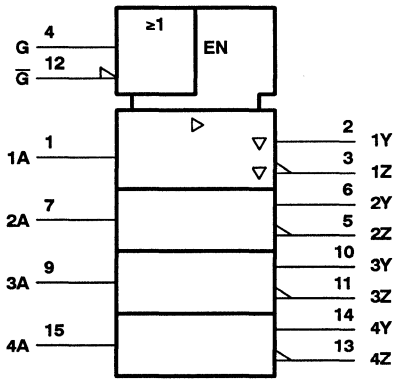
The SN75172 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

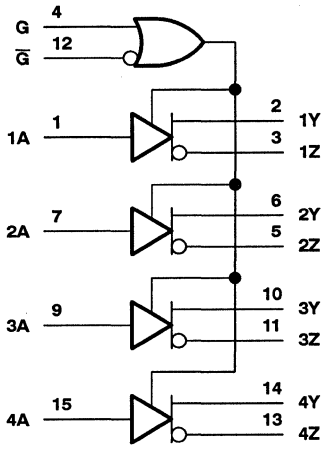
H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA					−1.5	V
V_O	Output voltage	$I_O = 0$			0		6	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = -33$ mA		3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = 33$ mA		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$			1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1		1/2 V_{OD1} or 2¶			V
		$R_L = 54\ \Omega$,	See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2			1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of diferential output voltage‡	$R_L = 54\ \Omega$ or $100\ \Omega$,		See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage§						+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡						±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V					±100	μA
I_{IH}	High-level input current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level input current	$V_I = 0.5$ V					−360	mA
I_{OS}	Short-circuit output current	$V_O = -7$ V					−180	mA
		$V_O = V_{CC}$					180	
		$V_O = 12$ V					500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTE 2: See Figure 3-5 of EIA Standard RS-485.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD2}\rvert$		V_t (Test Termination) Measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert, \lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert, \lvert I_{xb}\rvert$	I_{ia}, I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω,	See Figure 2		45	65	ns
t_{tD}	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level9	R_L = 110 Ω,	See Figure 3		18	30	ns

PARAMETER MEASUREMENT INFORMATION

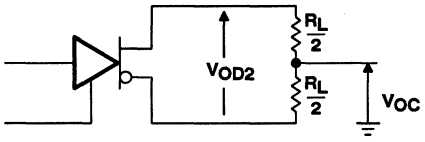


Figure 1. Differential and Common-Mode Output Voltages

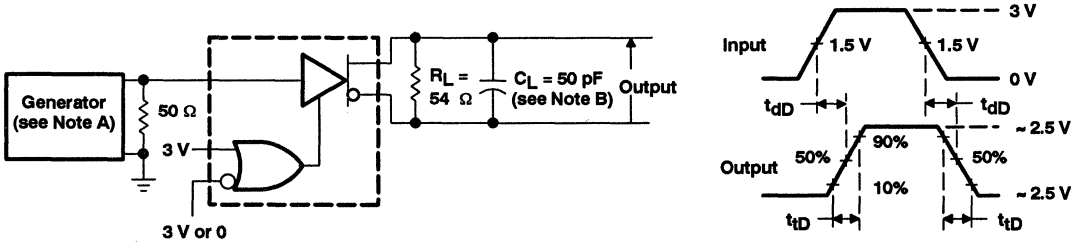
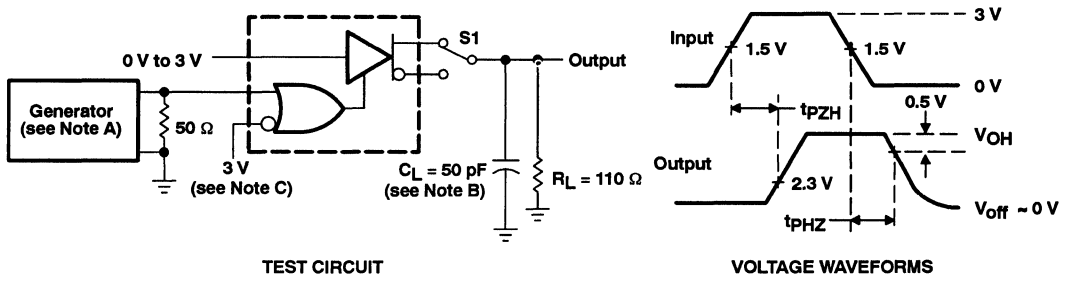


Figure 2. Differential-Output Test Circuit and Voltge Waveforms

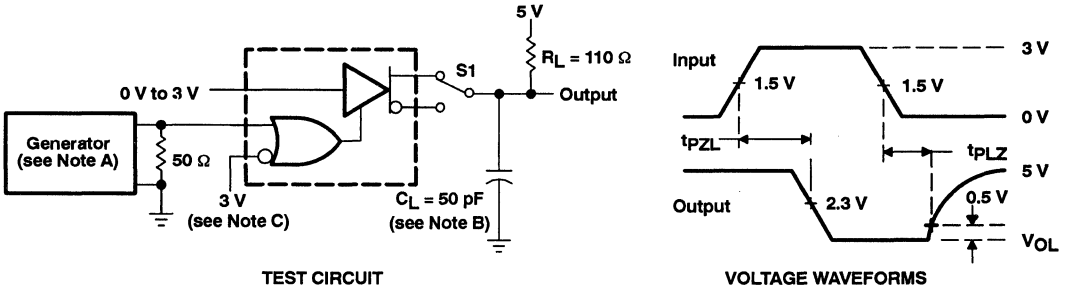
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Test Circuit and Voltage Waveforms

NOTES: C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.

D. C_L includes probe and stray capacitance.

E. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

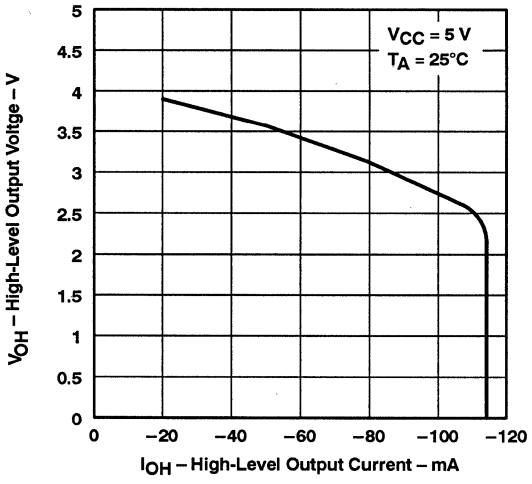


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

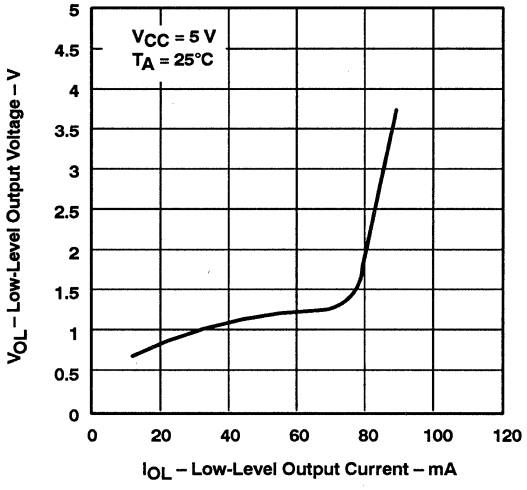


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

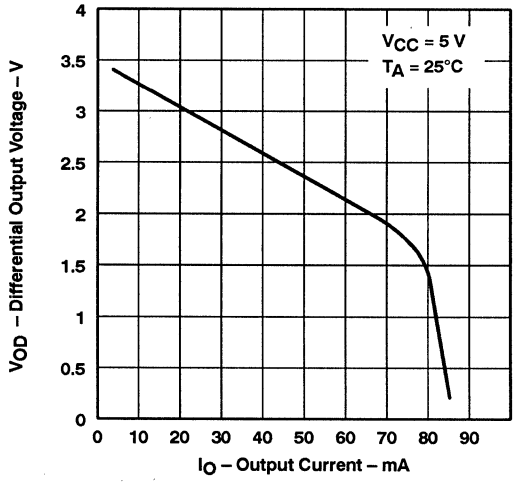


Figure 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

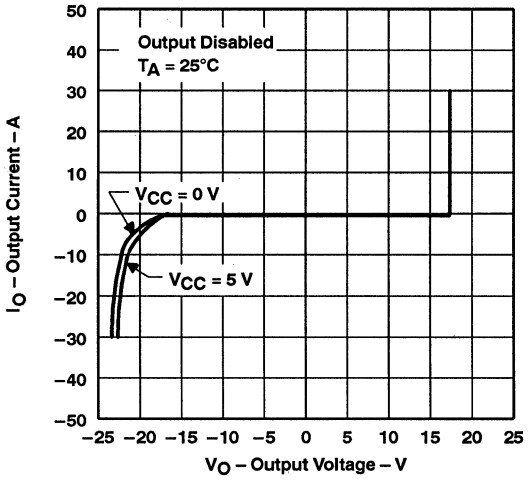


Figure 8

TYPICAL CHARACTERISTICS

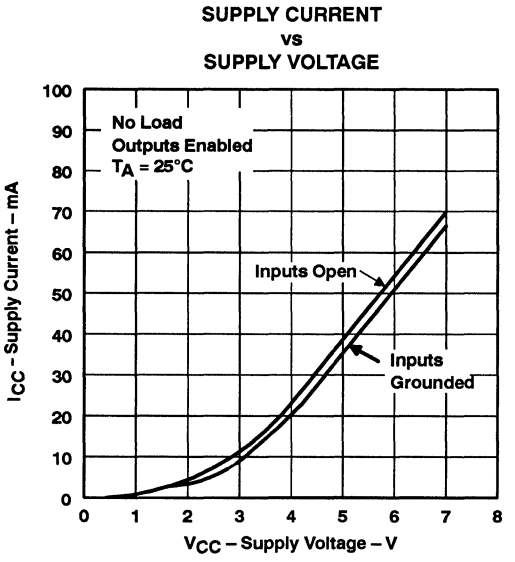


Figure 9

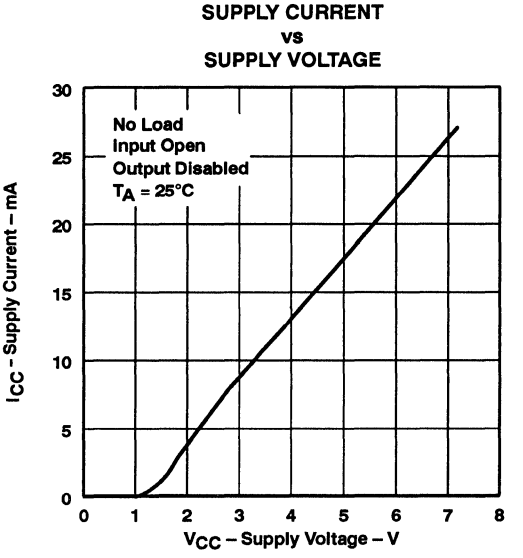
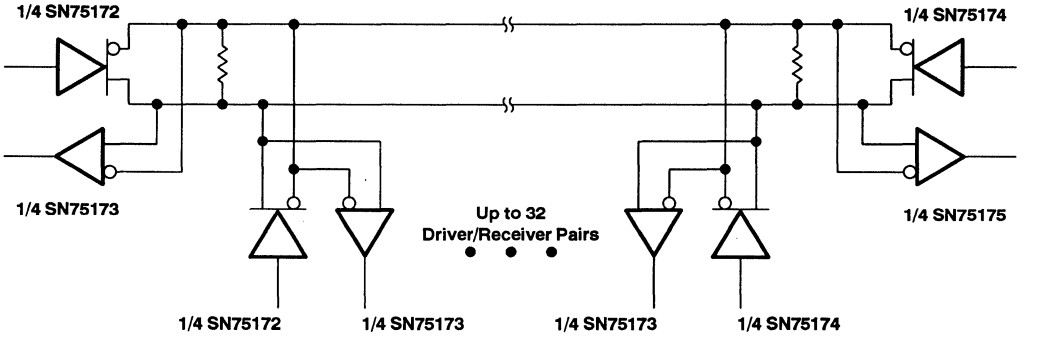


Figure 10

APPLICATION INFORMATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 11

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 20-MBaud Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 55 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Functionally Interchangeable With SN75172**

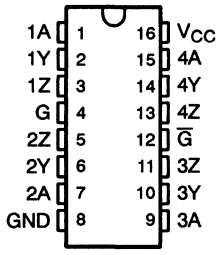
description

The SN65ALS172A and SN75ALS172A are quad line drivers with 3-state differential outputs. They are designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. These devices are optimized for balanced multipoint bus transmission at rates of up to 20-Mbaud. Each driver features wide positive and negative common-mode output voltage ranges making them suitable for party-line applications in noisy environments.

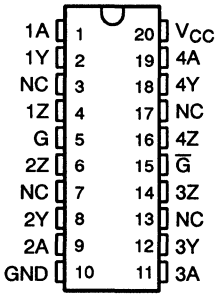
The SN65ALS172A and SN75ALS172A provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN65ALS172A is characterized for operation from −40°C to 85°C and the SN75ALS172A is characterized for operation from 0°C to 70°C.

SN75ALS172A . . . N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



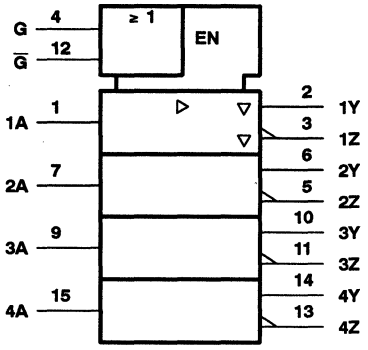
NC – No internal connection

FUNCTION TABLE
(each driver)

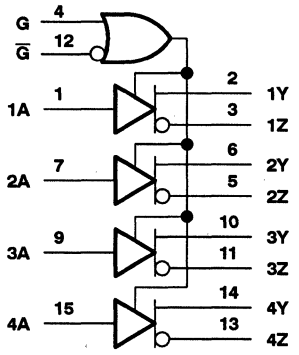
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

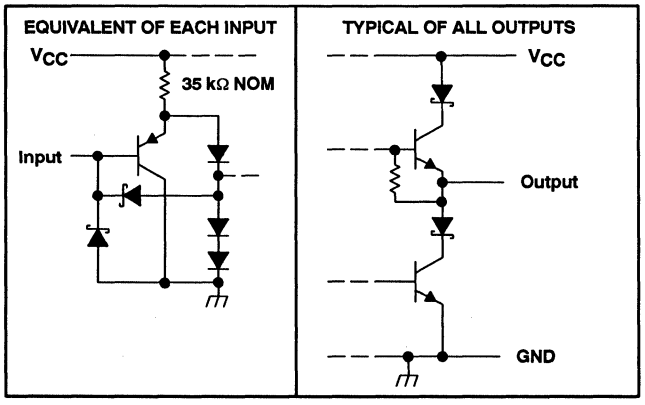


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −9 V to 14 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65ALS172A ..... −40°C to 85°C
SN75ALS172A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				+12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A	SN65ALS172A	−40		85	°C
	SN75ALS172A	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2V_{OD1} or 2¶			V
		R_L = 54 Ω		1.5	2.5	5	
$\lvert V_{OD3} \rvert$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage§					+3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		15	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4	10	30	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

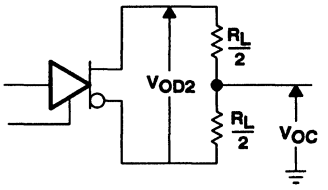
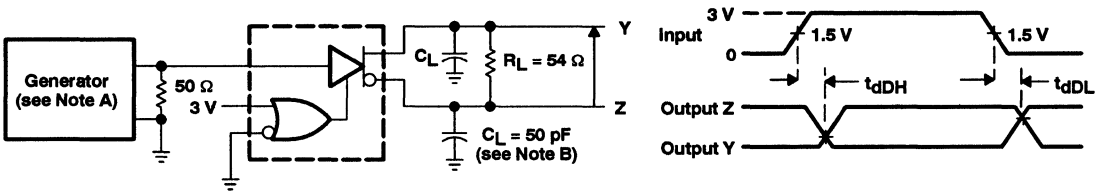


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 2. Differential Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

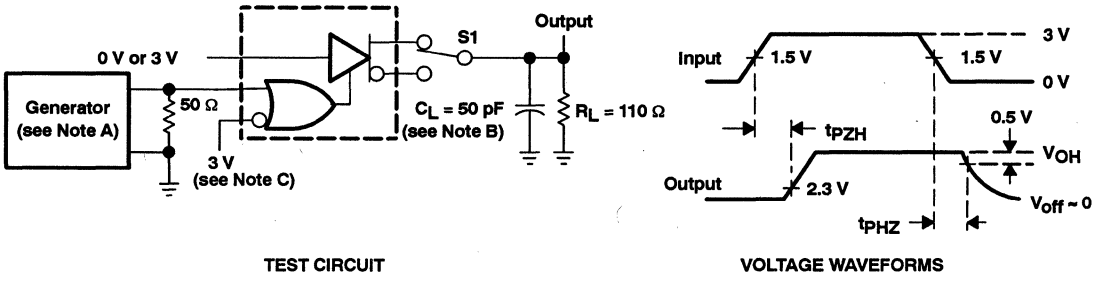


Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

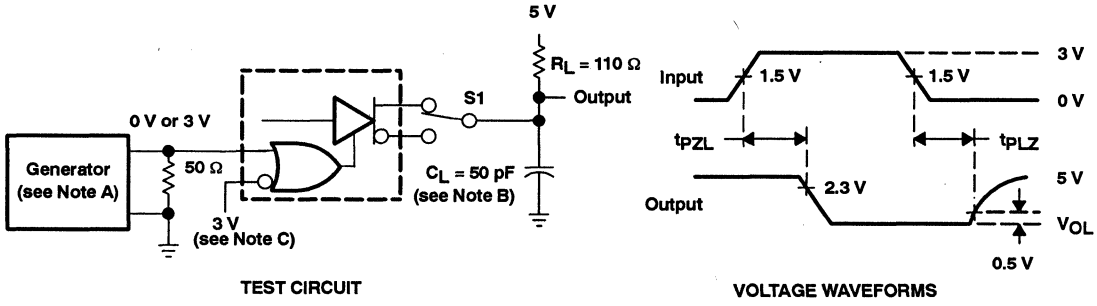


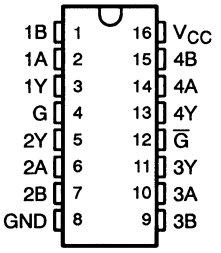
Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

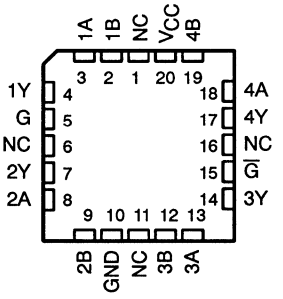
SLLS144A – D2600, OCTOBER 1980 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Plug In Replacement for AM26LS32**

D, J, OR N PACKAGE
(TOP VIEW)



SN55173 . . . FK PACKAGE
(TOP VIEW)



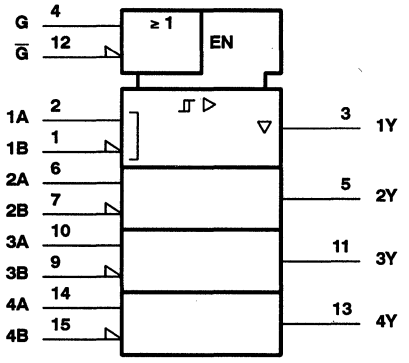
NC – No internal connection

description

The SN55173, SN65173, and SN75173 are monolithic quad differential line receivers with 3-state outputs. They are designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, RS-485, and several CCITT recommendations. The devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. The '173 devices feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 to 12 V. Fail-safe design ensures that if the inputs are open circuited, the outputs are always high. The SN65173 and SN75173 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers, and the SN55173 is designed for optimum performance when used with the SN55172 or SN55174 quad differential line drivers.

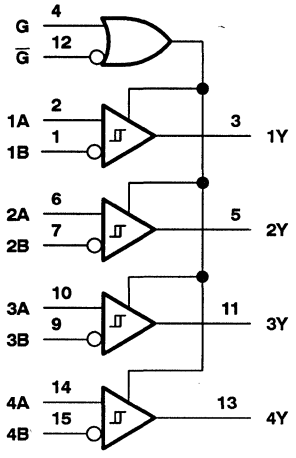
The SN55173 is characterized over the full military temperature range of −55°C to 125°C. The SN65173 is characterized for operation from −40°C to 85°C. The SN75173 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



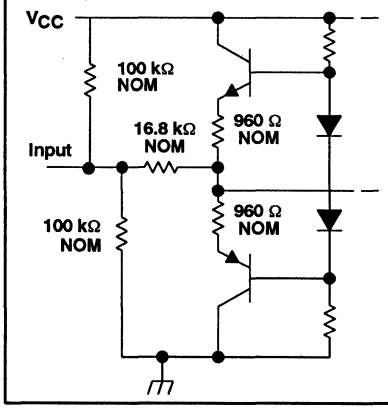
FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

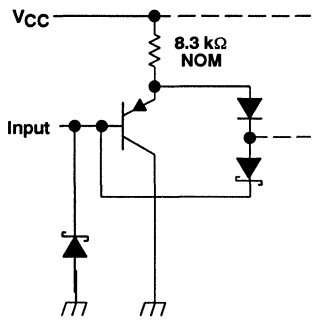
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs

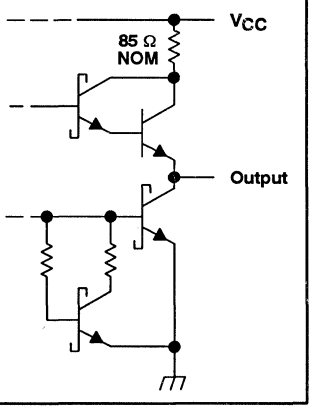
EQUIVALENT OF EACH A OR B INPUT



EQUIVALENT OF G OR $\overline{G}$ INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs ..... ±25 V
Differential input voltage (see Note 2) ..... ±25 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55173 ..... −55°C to 125°C
SN65173 ..... −40°C to 85°C
SN75173 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55173	4.5	5	5.5	V
	SN65173, SN75173	4.75	5	5.25	
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN55173	−55		125	°C
	SN65173	−40		85	
	SN75173	0		70	

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 16 mA		−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	See Figure 4				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	SN55173	2.5			V
				SN65173, SN75173	2.7			
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	See Figure 1	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current§				−15		−85	mA
I_{CC}	Supply current	Outputs disabled					70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to EIA Standards RS-422A and RS423-A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF,			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

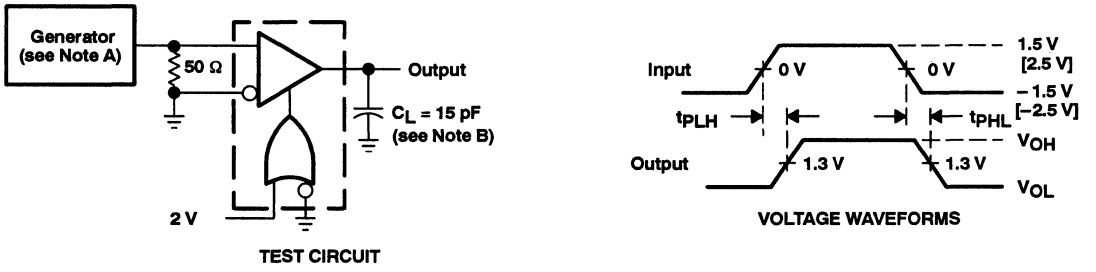


Figure 1. t_{PLH}, t_{PHL} Test Circuit and Voltage Waveforms

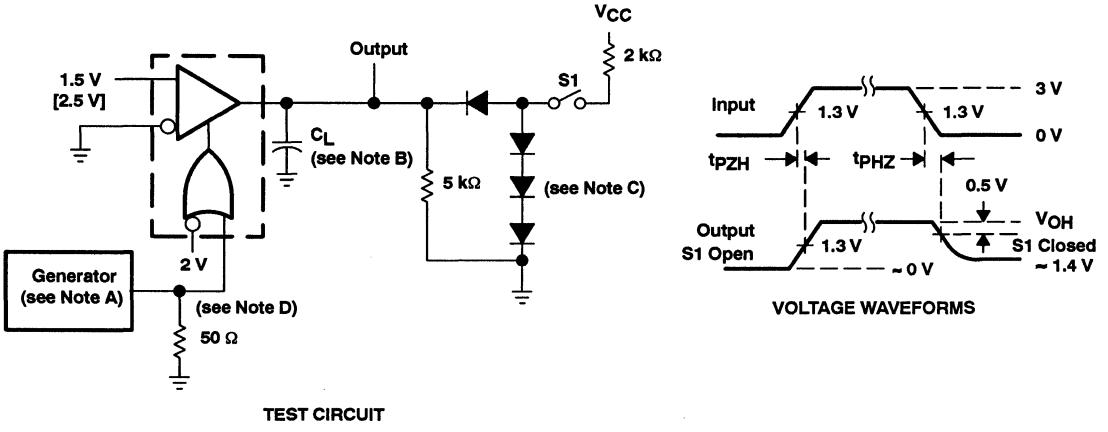


Figure 2. t_{PHZ}, t_{PZH} Test Circuit and Voltage Waveforms

[ ] represent voltages on the SN55173 only.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

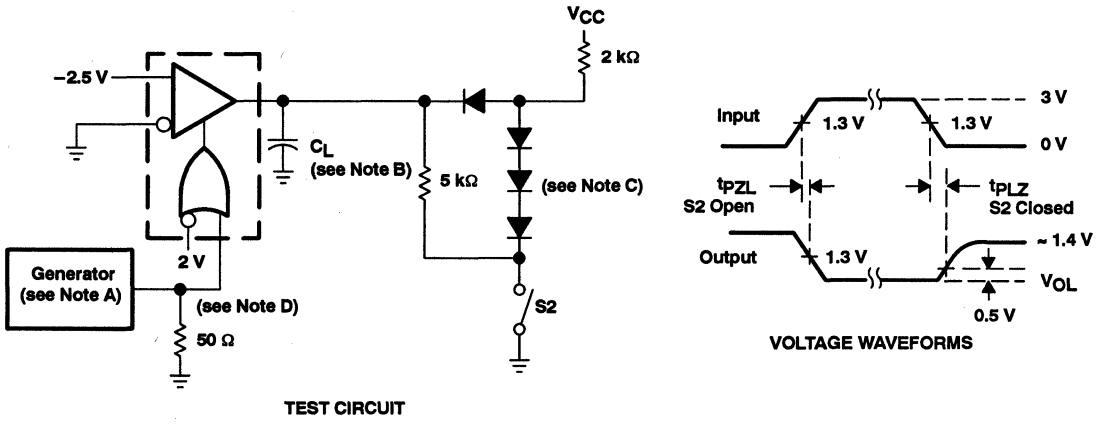


Figure 3. t_{PZL}, t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

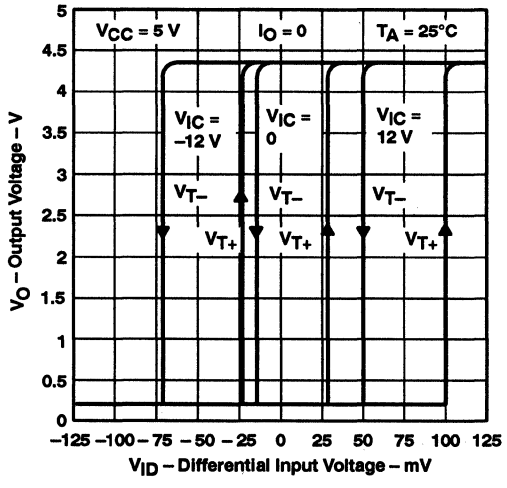


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

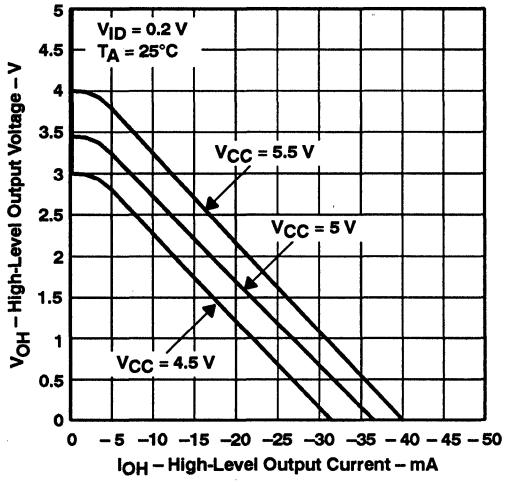


Figure 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

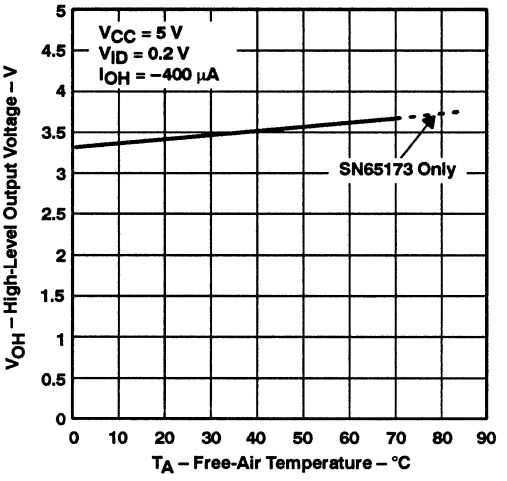


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

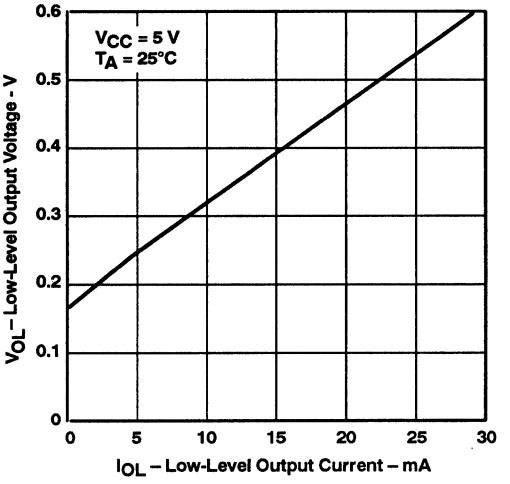


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

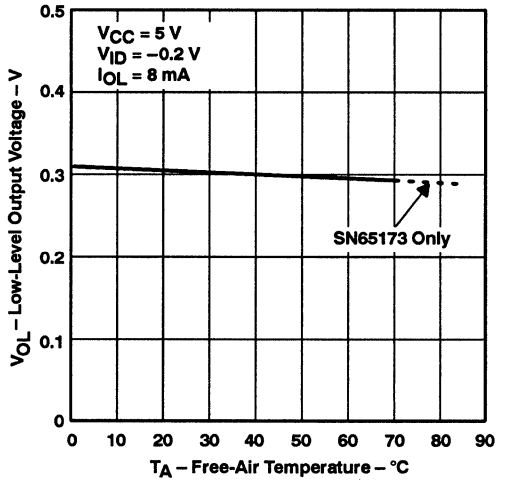


Figure 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

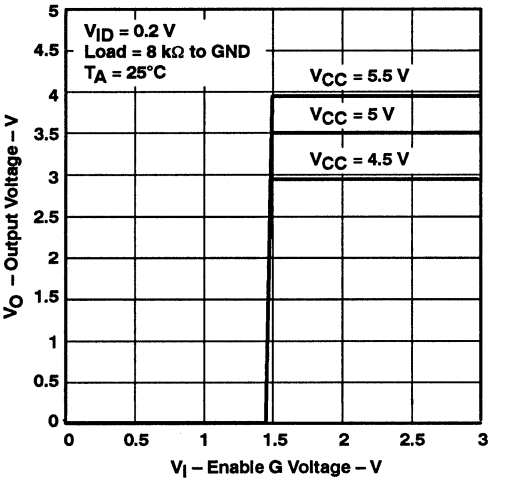


Figure 9

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

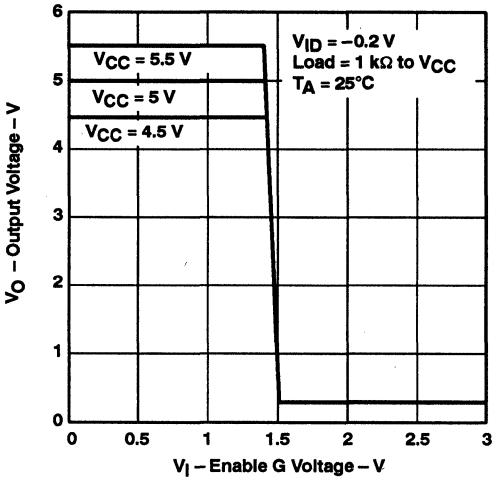


Figure 10

INPUT CURRENT
vs
INPUT VOLTAGE

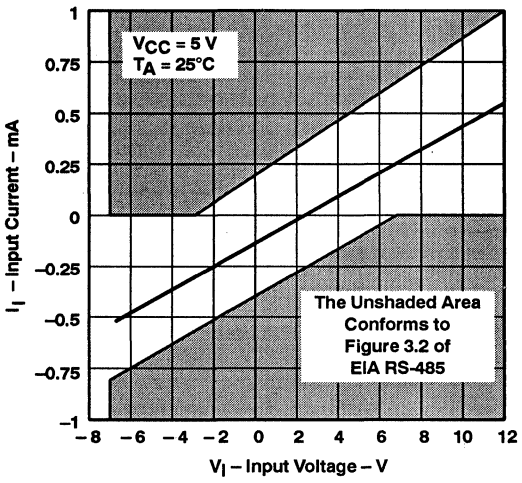
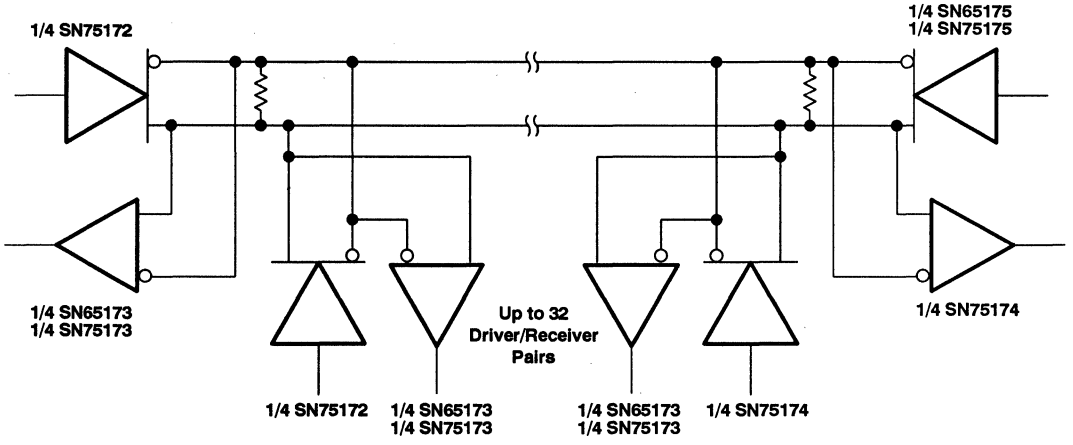


Figure 11

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 12. Typical Application Circuit

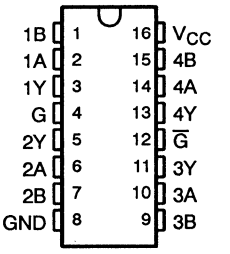
- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Log Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low Supply Current Requirement 27 mA Max**

description

The SN75ALS173 is a monolithic quad differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. The four receivers have an ORed pair of enables in common. Either G being high or $\overline{G}$ being low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

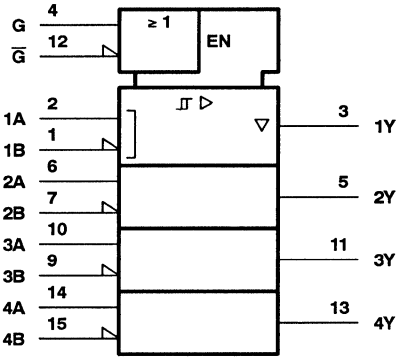
The SN75ALS173 is characterized for operation from 0°C to 70°C.

N OR NS† PACKAGE
(TOP VIEW)



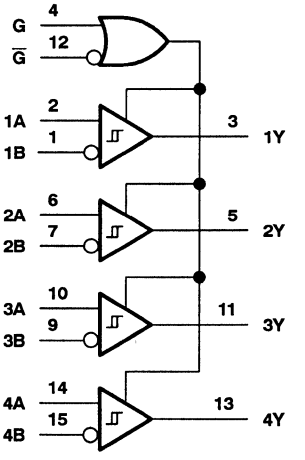
† The NS package is only available left-end taped and reeled (order device SN75ALS173 NSLE).

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

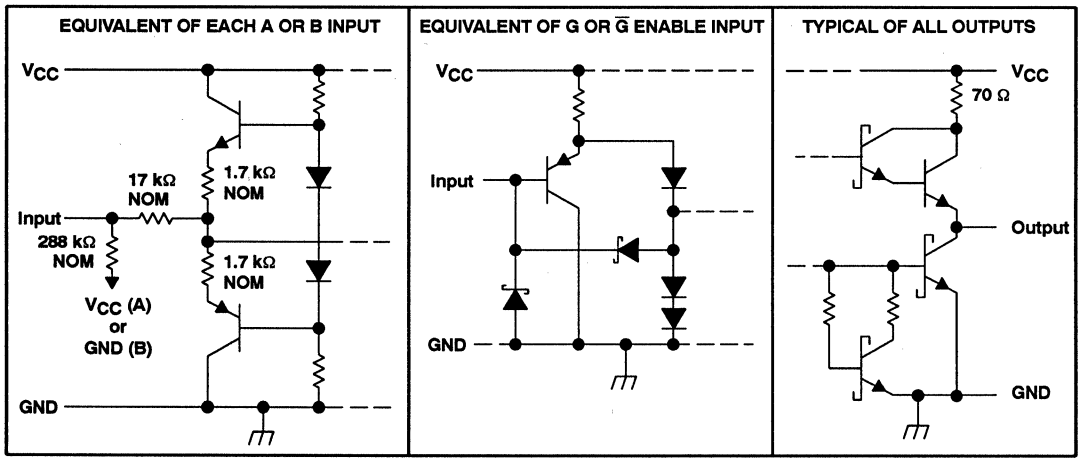


FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs, V_I ..... ±14 V
Differential input voltage, V_{ID} (see Note 2) ..... ±14 V
Enable input voltage ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$			0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage						200	mV
V_{T-}	Negative-going threshold voltage				−200‡			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{IK}	Input clamp voltage	G, $\overline{G}$	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 1				0.45	V
I_{OZ}	High-impedance-state output current		V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level input current	G, $\overline{G}$	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	G, $\overline{G}$	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		See Note 4		−15		−85	mA
I_{CC}	Supply current (total package)		No load, Outputs enabled			16	24	mA
			No load, Outputs disabled			18	27	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to EIA Standards RS-485 for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	V_{ID} = −2.5 V to 2.5 V, See Figure 2	9	18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output		9	18	27	ns
t_{PZH}	Output enable time to high level	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level	See Figure 4	6	13	21	ns
t_{PHZ}	Output disable time from high level	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level	See Figure 4	8	15	25	ns

PARAMETER MEASUREMENT INFORMATION

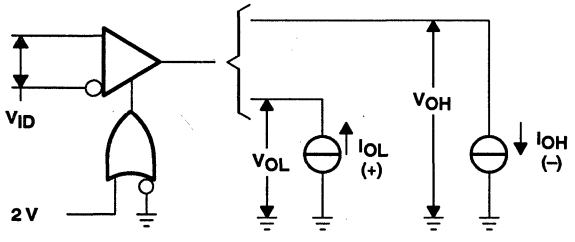


Figure 1. V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

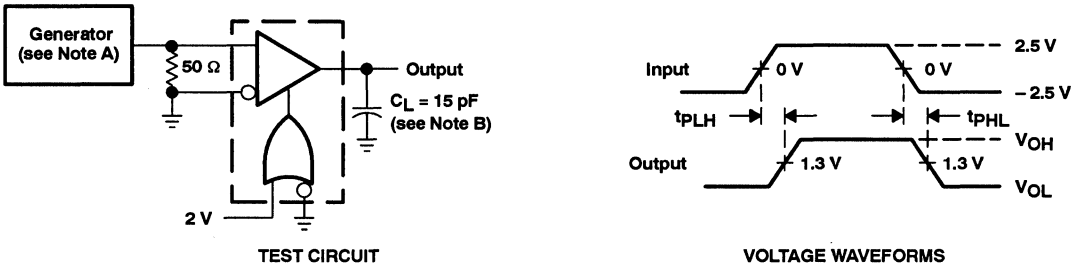


Figure 2. Test Circuit and Voltage Waveforms

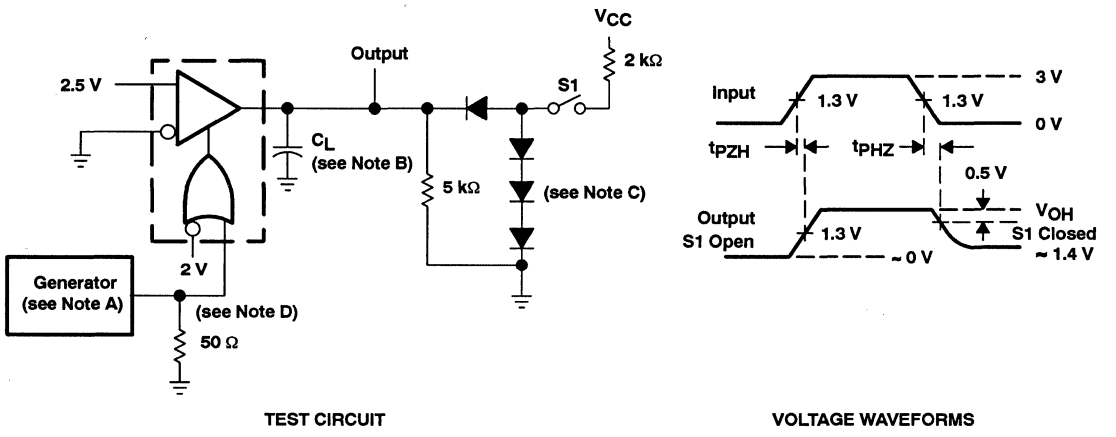


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

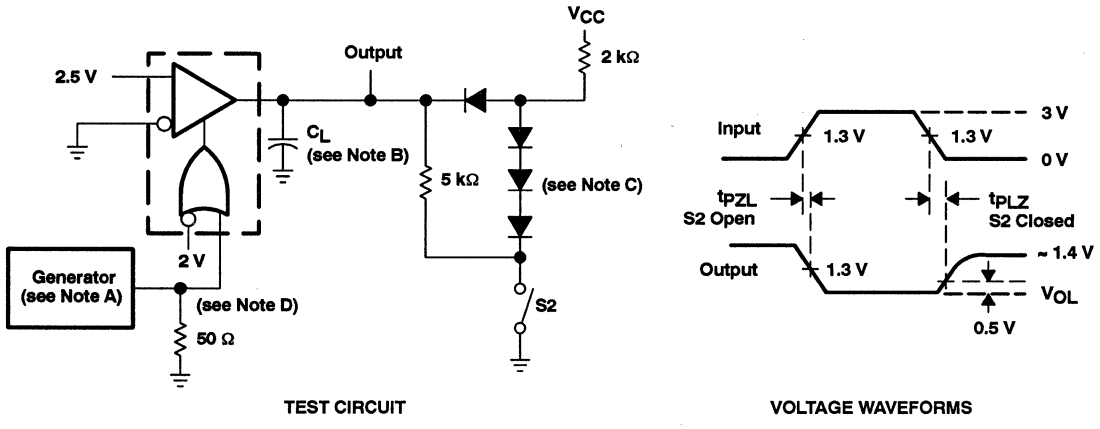


Figure 4. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TEXAS INSTRUMENTS
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- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High Enable**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable With MC3487**

description

The SN75174 is a monolithic quad differential line driver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

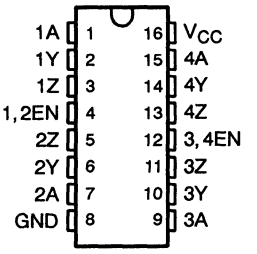
The SN75174 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

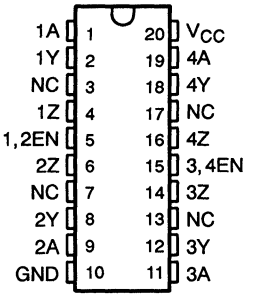
INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, X = irrelevant,
L = TTL low level,
Z = high impedance (off)

N PACKAGE
(TOP VIEW)

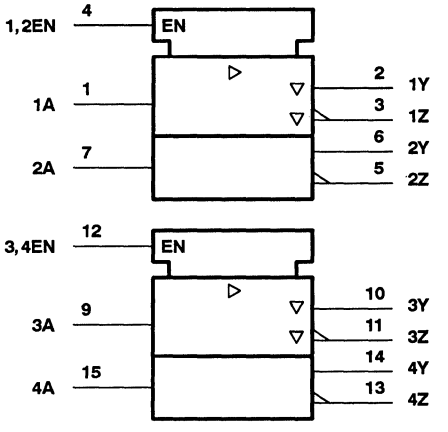


DW PACKAGE
(TOP VIEW)



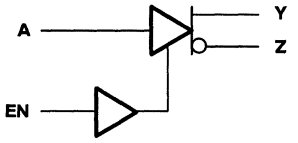
NC – No internal connection

logic symbol†

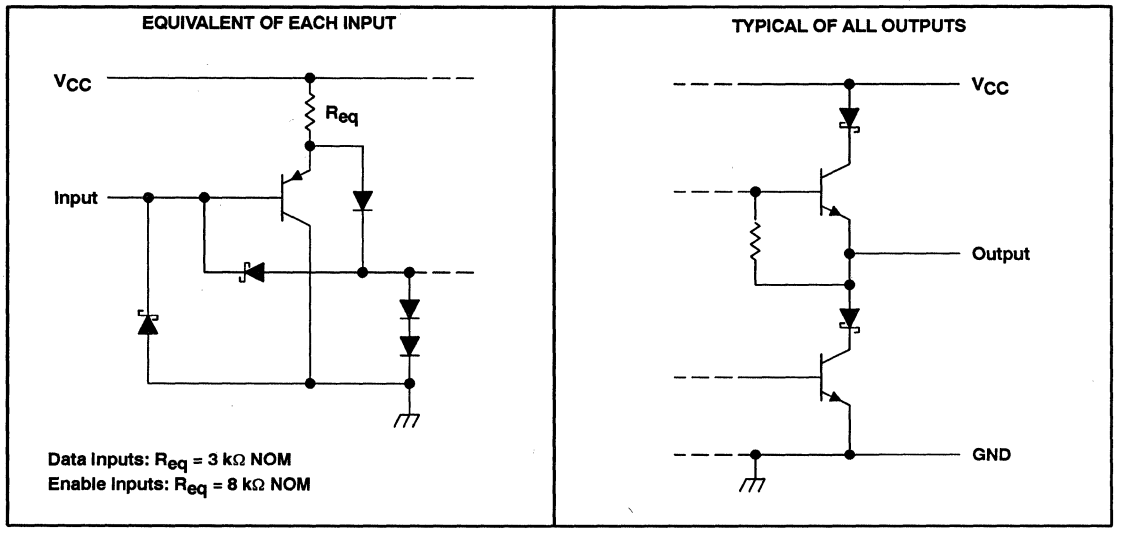


† This symbol is in accordance with ANSI/IEEE Std 91-984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended, operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 33 mA			1.1		V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5	6	6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2 V_{OD1} or 2§			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage§					+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

NOTE 2: See Figure 3.5 of EIA Standard RS-485.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω,	See Figure 2		45	65	ns
t_{tD}	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4		55	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3		75	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 3		18	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{Oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination) Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$,$\|I_{sb}\|$	
I_O	$\|I_{xa}\|$,$\|I_{xb}\|$	I_{ia},I_{ib}

PARAMETER MEASUREMENT INFORMATION

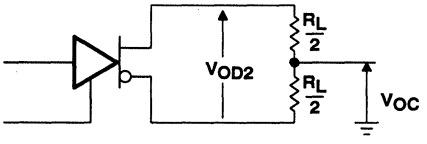
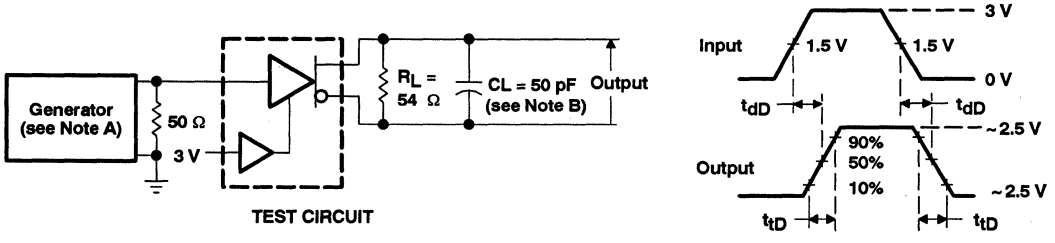


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

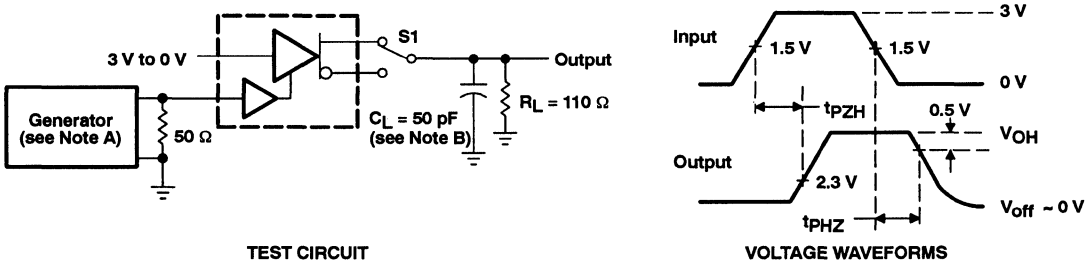


Figure 3. Test Circuit and Voltage Waveforms

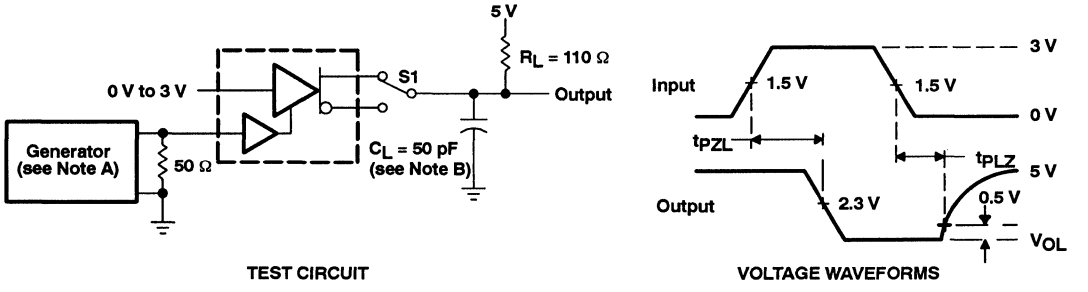


Figure 4. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

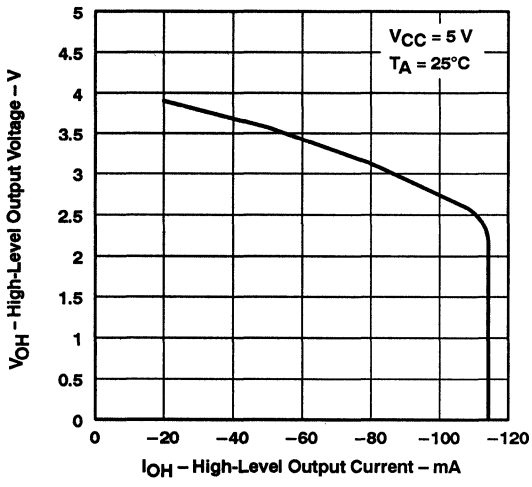


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

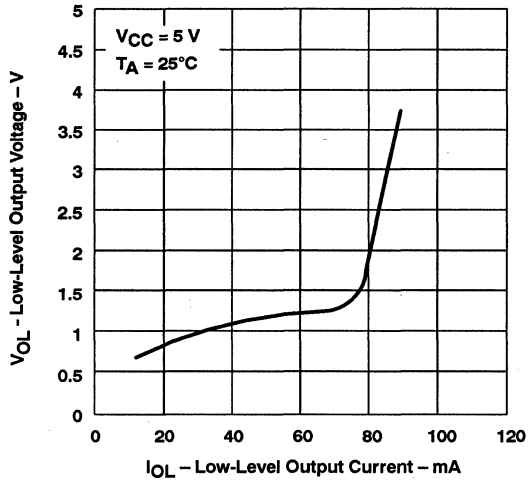


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

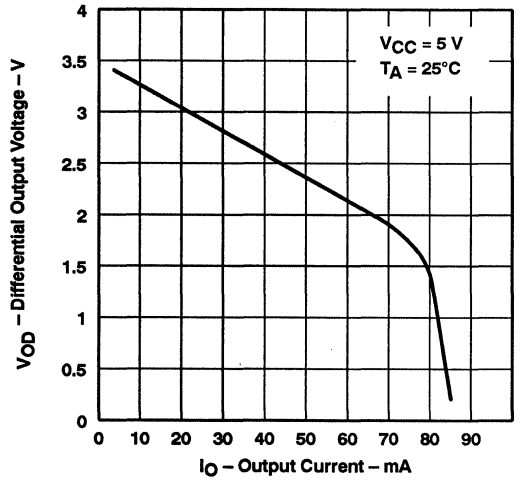


Figure 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

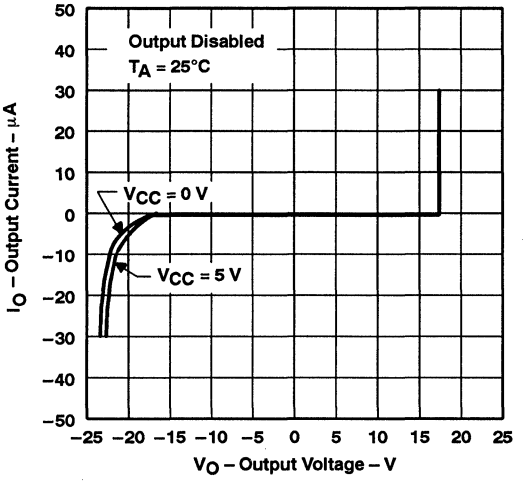


Figure 8

TYPICAL CHARACTERISTICS

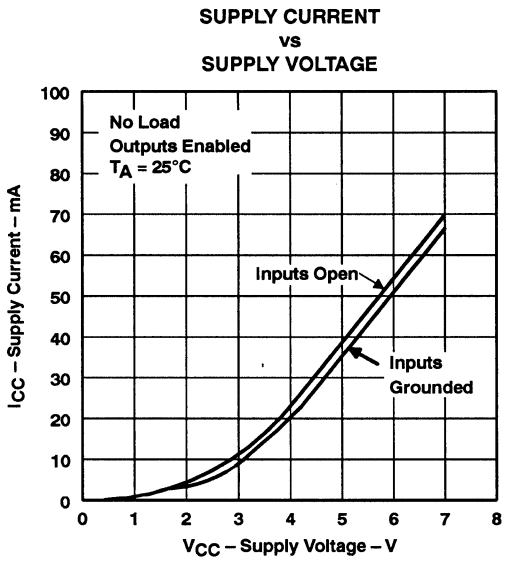


Figure 9

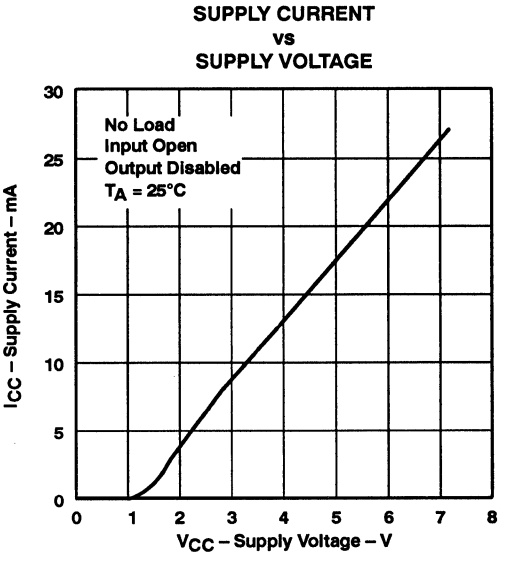
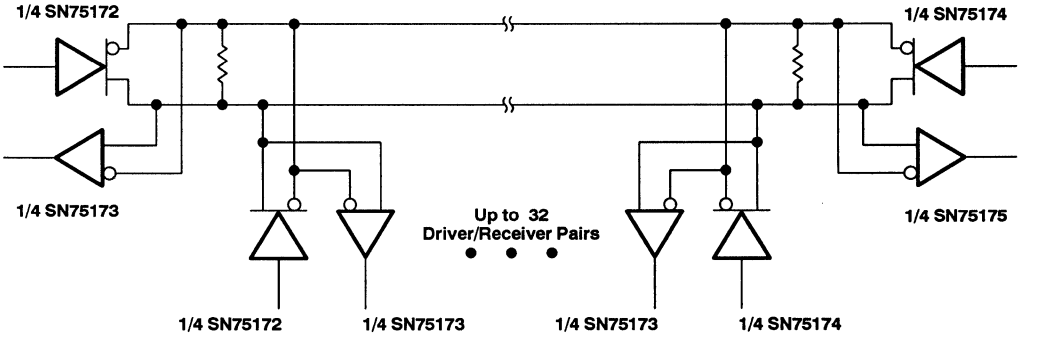


Figure 10

APPLICATION INFORMATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 11. Typical Application Circuit

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 20-MBaud Operation In Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments**
- **Low Supply Current Requirements 55 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Functionally Interchangeable With SN75174**

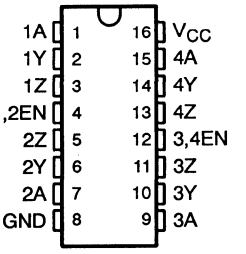
description

The SN65ALS174A and SN75ALS174A are quad line drivers with 3-state differential outputs. They are designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. These devices are optimized for balanced multipoint bus transmission at rates of up to 20 Mbaud. Each driver features wide positive and negative common-mode output voltage ranges making them suitable for party-line applications in noisy environments.

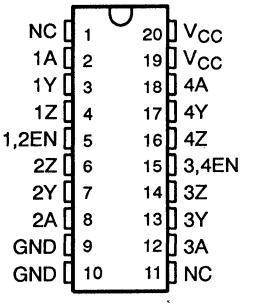
The SN65ALS174A and SN75ALS174A provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN65ALS174A is characterized for operation from −40°C to 85°C and the SN75ALS174A is characterized for operation from 0°C to 70°C.

SN75ALS174A . . . N PACKAGE
(TOP VIEW)



SN65ALS174A, SN75ALS174A . . . DW PACKAGE
(TOP VIEW)



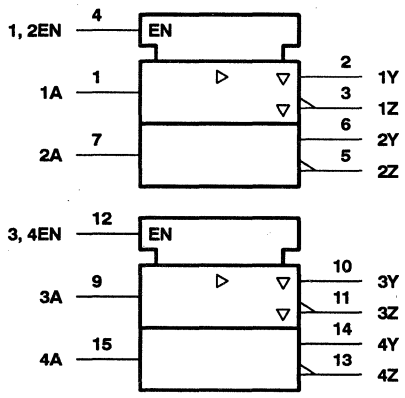
NC–No internal connection

FUNCTION TABLE
(each driver)

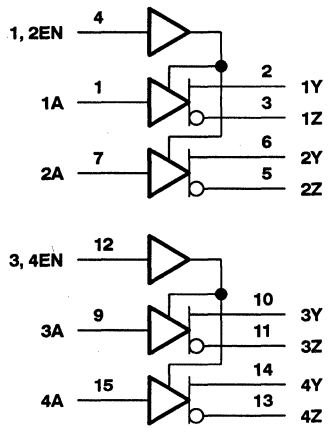
INPUT A	ENABLES	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

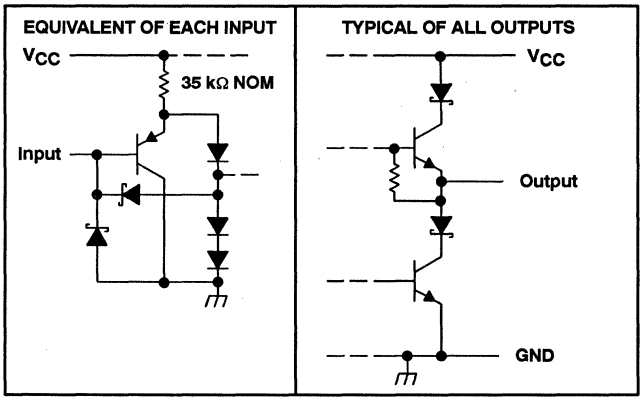


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −9 V to 14 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65ALS174A ..... −40°C to 85°C
SN75ALS174A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A	SN65ALS174A	−40		85	°C
	SN75ALS174A	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	$R_L = 100\ \Omega$	See Figure 1	1/2 V_{OD1} or 2¶			V
		$R_L = 54\ \Omega$		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$ or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage§					3 / −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	μA
I_{IH}	High-level input current	$V_I = 2.7$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−100	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V whichever is greater.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential-output delay time	$R_L = 54\ \Omega$,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 4	10	30	45	ns

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

PARAMETER MEASUREMENT INFORMATION

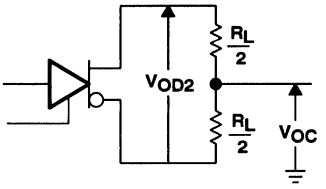
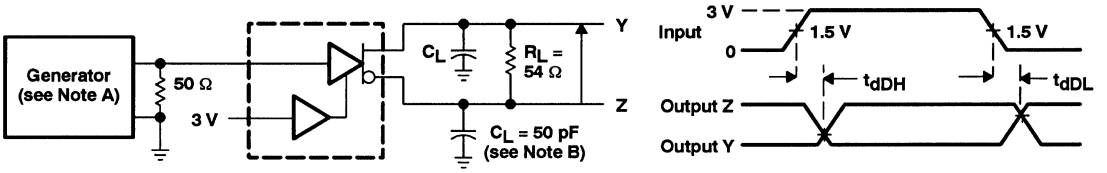


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Voltage Waveforms Delay and Transition Times

PARAMETER MEASUREMENT INFORMATION

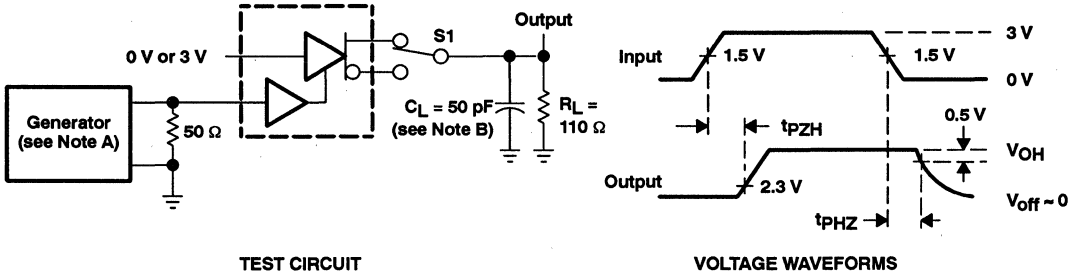


Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

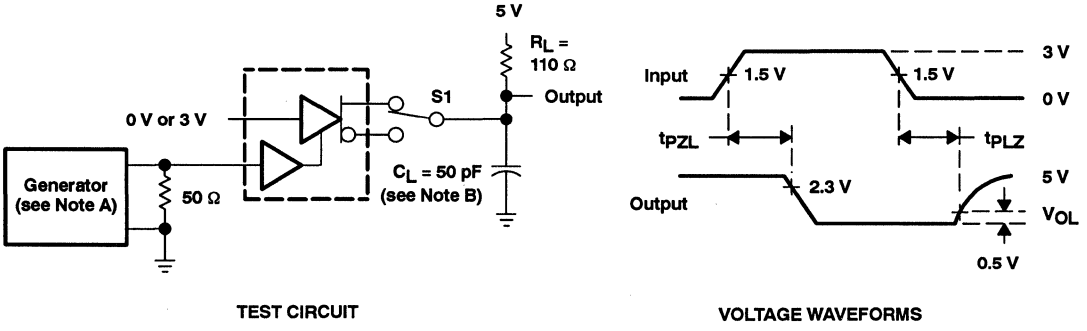


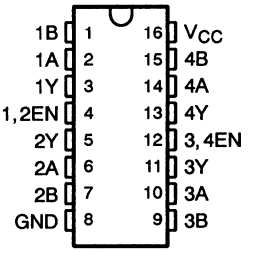
Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

SLLS145A – D2602, OCTOBER 1990 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines In Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low-Power Requirements**
- **Plug-In Replacement for MC3486**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

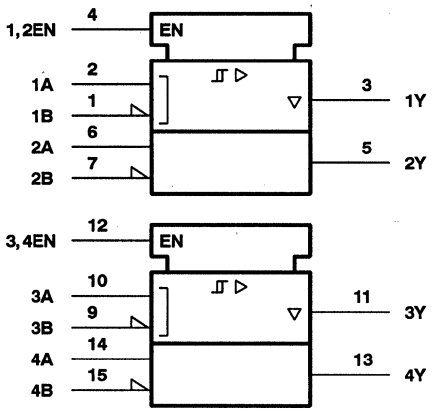
description

The SN65175 and SN75175 are monolithic quad differential line receivers with 3-state outputs. They are designed to meet the requirements of EIA Standards RS-422-A, RS-423A, RS-485, and several CCITT recommendations. These devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of ±12 V. The SN65175 and SN75175 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

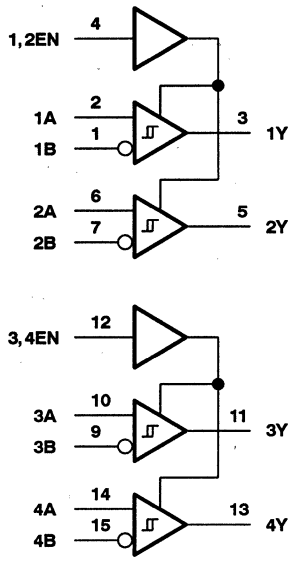
The SN65175 is characterized for operation from −40°C to 85°C. The SN75175 is characterized for operation from 0°C to 70°C.

logic symbol†

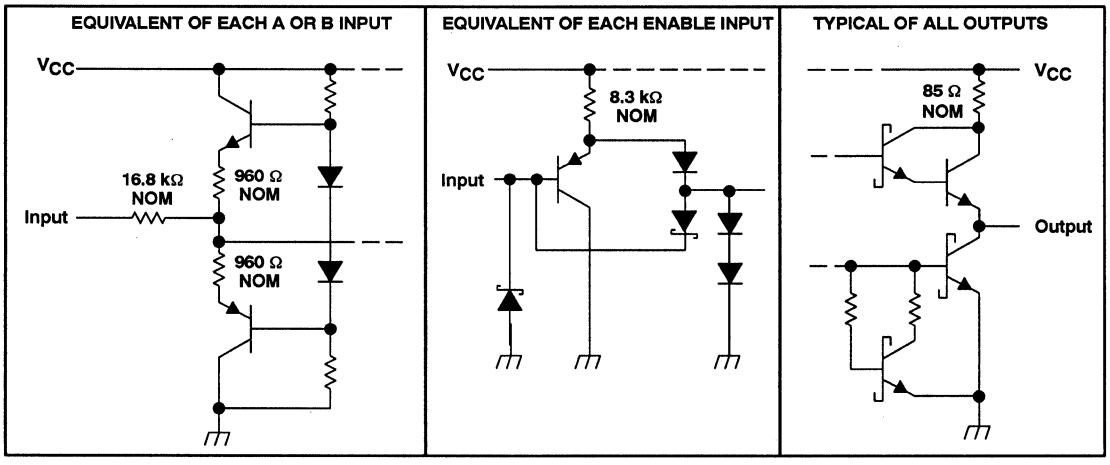


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs ..... ±25 V
Differential input voltage (see Note 2) ..... ±25 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65175 ..... −40°C to 85°C
SN75175 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... −260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65175	−40		85	°C
	SN75175	0		70	

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 16 mA		−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	See Figure 4				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	See Figure 1	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current§				−15		−85	mA
I_{CC}	Supply current	Outputs disabled					70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to EIA Standards RS-422A, RS423-A, and RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	35	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level	See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level			25	35	ns

PARAMETER MEASUREMENT INFORMATION

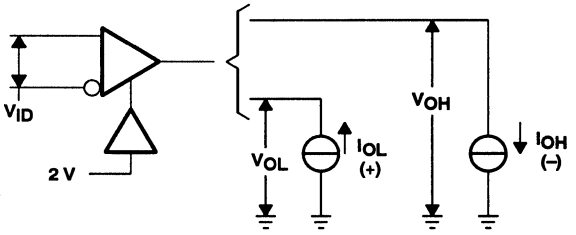


Figure 1. V_{OH}, V_{OL}

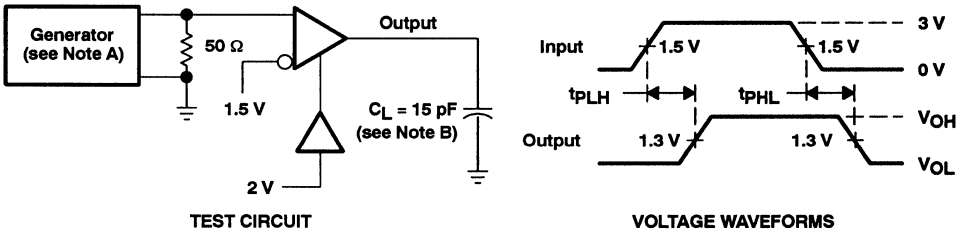


Figure 2. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

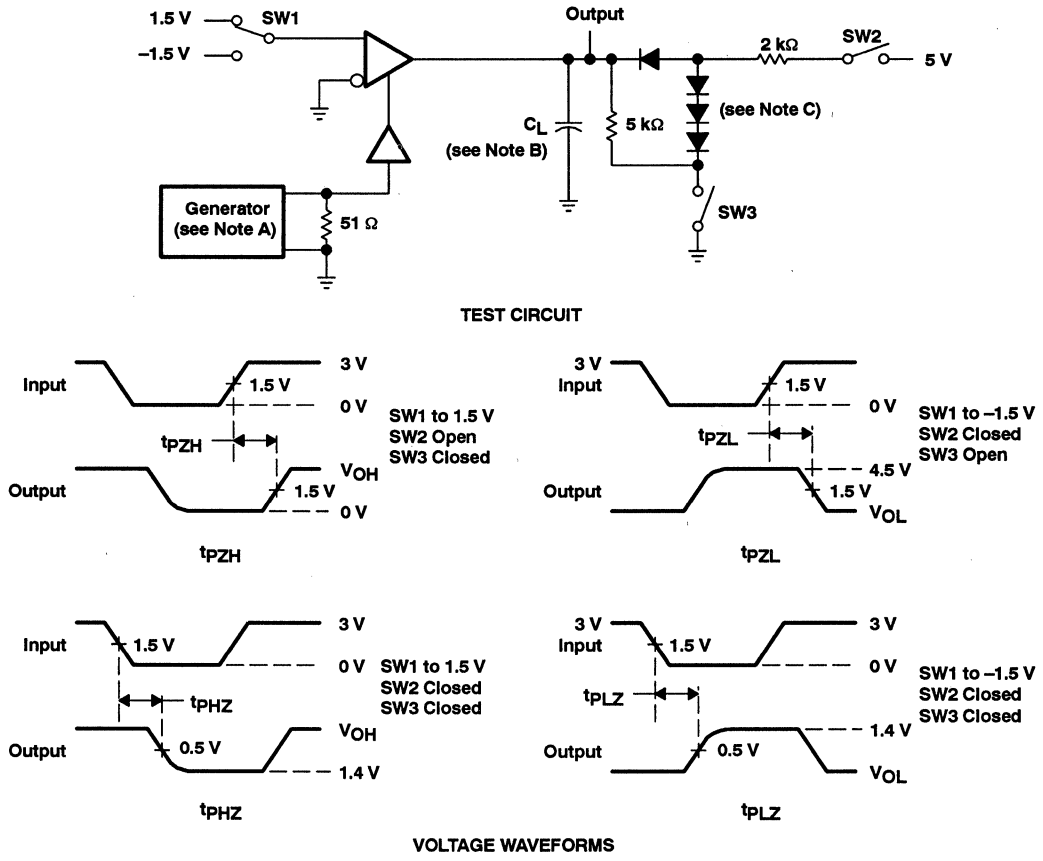


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_f ≤ 6 ns, t_r ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

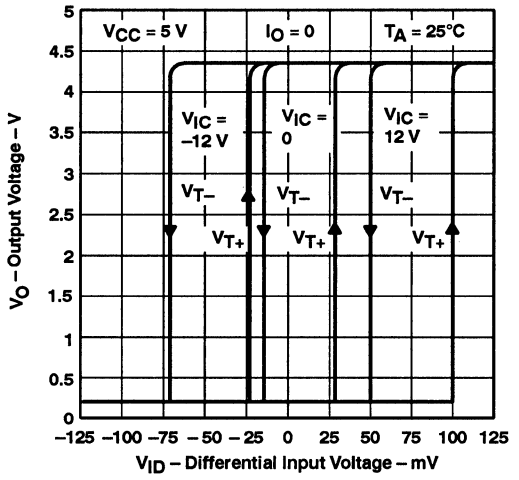


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

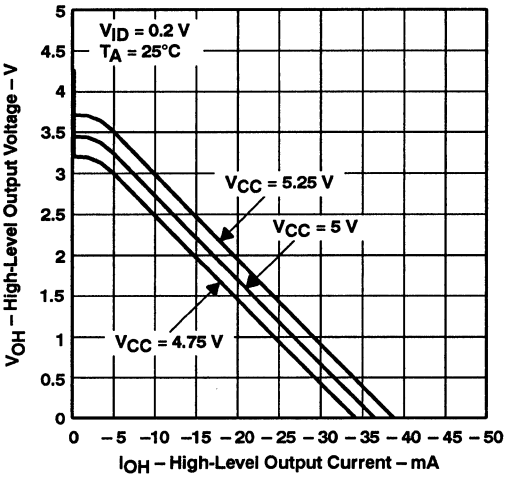


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

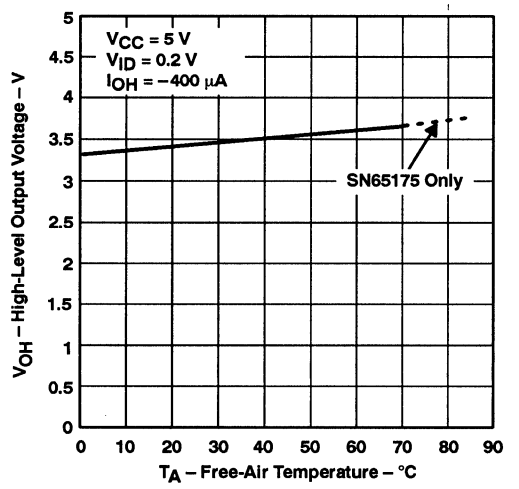


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

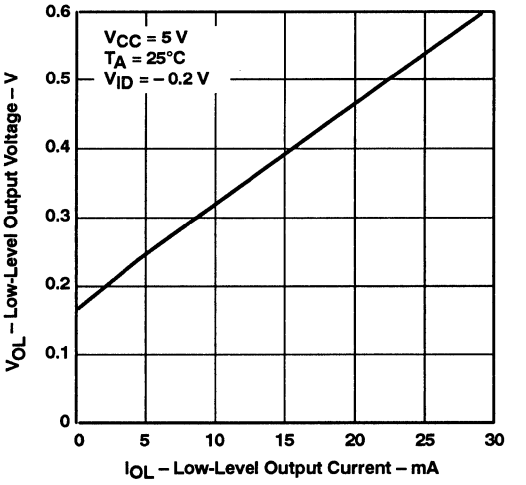


Figure 7

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

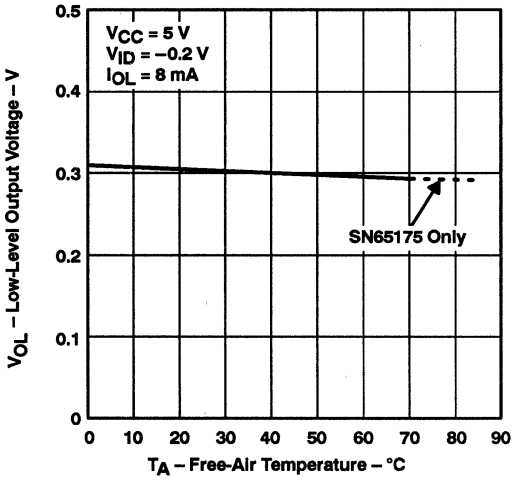


Figure 8

OUTPUT VOLTAGE vs ENABLE VOLTAGE

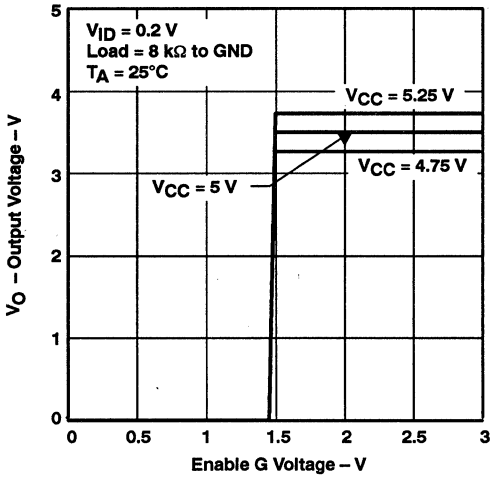


Figure 9

OUTPUT VOLTAGE vs ENABLE VOLTAGE

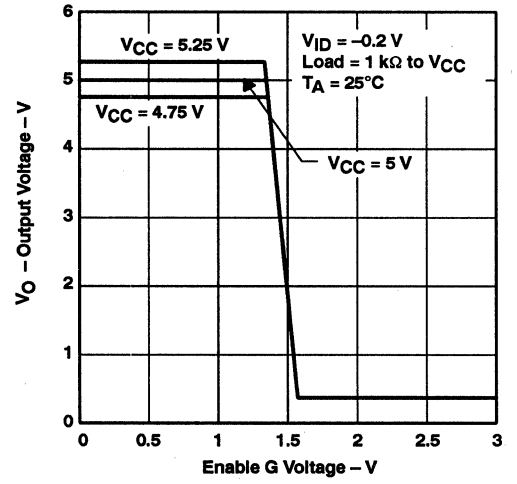


Figure 10

SUPPLY CURRENT (ALL RECEIVERS) vs SUPPLY VOLTAGE

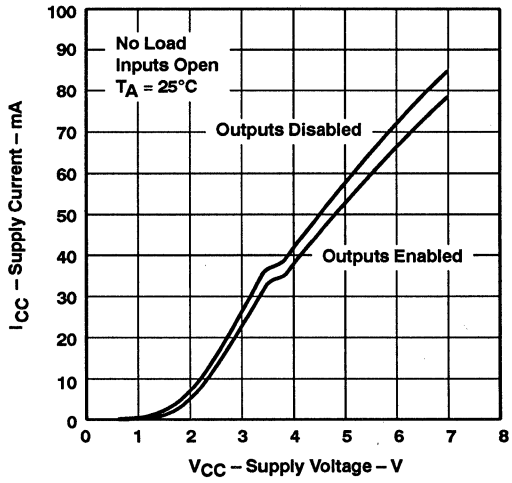


Figure 11

TYPICAL CHARACTERISTICS

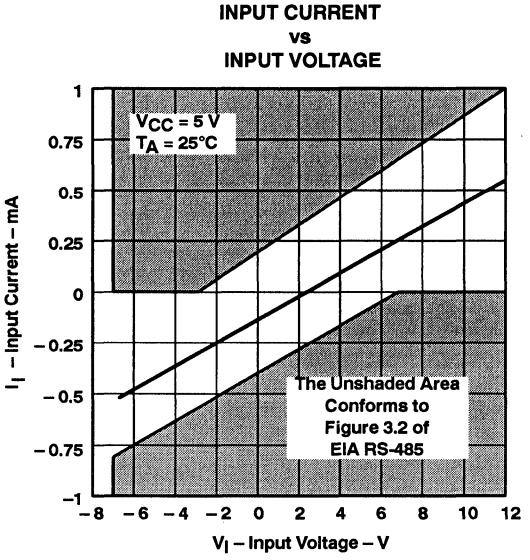


Figure 12

APPLICATION INFORMATION

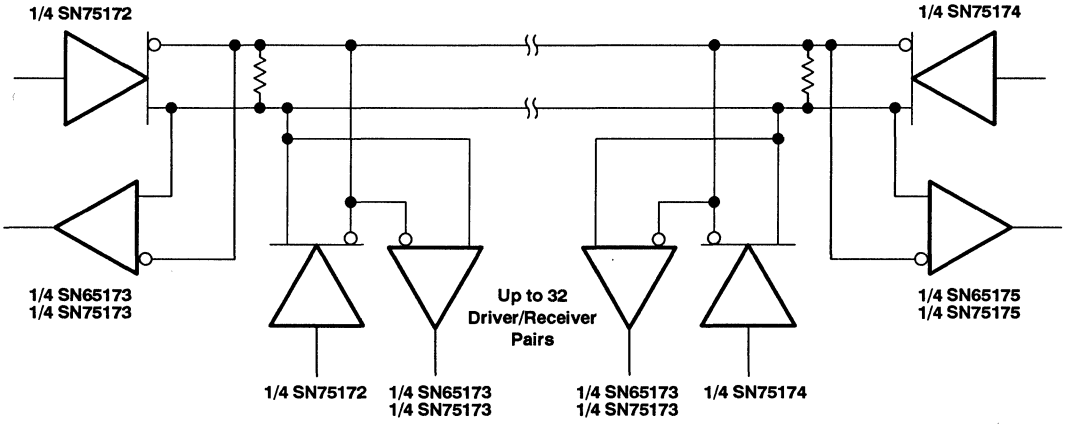


Figure 13. Typical Application Circuit

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

SLLS131B – D3910, SEPTEMBER 1991 – REVISED JANUARY 1993

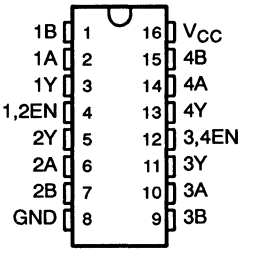
- **Meets EIA Standards RS-422-A, RS-423-A, and RS-485**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirement 27 mA Max**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**

description

The SN75ALS175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. Each of the two pairs of receivers has a common active-high enable. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

The SN75ALS175 is characterized for operation from 0°C to 70°C.

N OR NS† PACKAGE
(TOP VIEW)



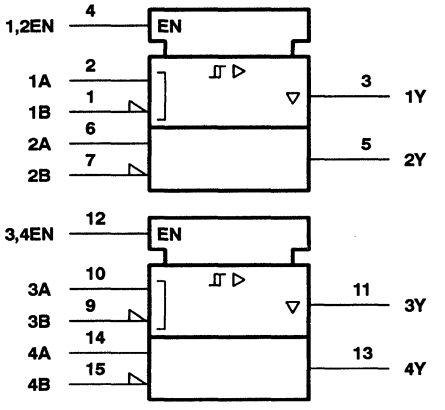
† The NS package is only available left-ende taped and reeled (order device SN75ALS175NSLE).

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A – B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open Circuit	H	H

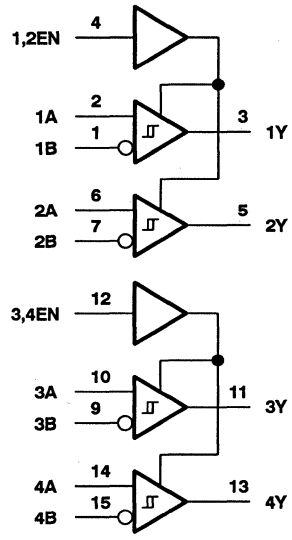
H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

logic symbol‡

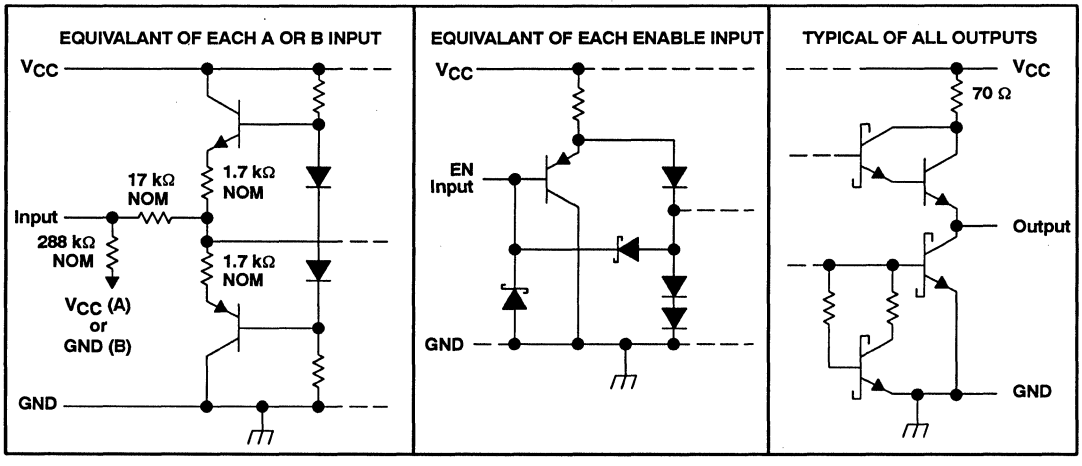


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs ..... ±14 V
Differential input voltage (see Note 2) ..... ±14 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level enable-input voltage, V_{IH}	2			V
Low-level enable-input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage						200	mV
V_{T-}	Negative-going threshold voltage				−200‡			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 1			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	$V_{IH(E)}$ = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	$V_{IL(E)}$ = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_O = 0,	See Note 4		−15		−85	mA
I_{CC}	Suply current (total package)	No load,	Outputs enabled			16	24	mA
		No load,	Outputs disabled			18	27	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
NOTES: 3. Refer to EIA Standards RS-485 for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	V_{ID} = −2.5 V to 2.5 V,		9	18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2	9	18	27	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level			6	13	21	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level			8	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

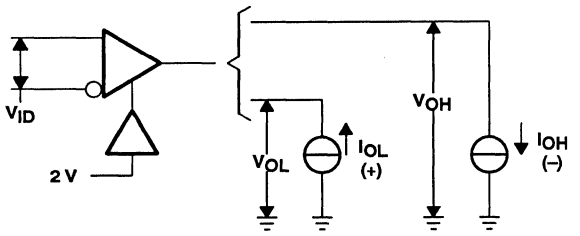
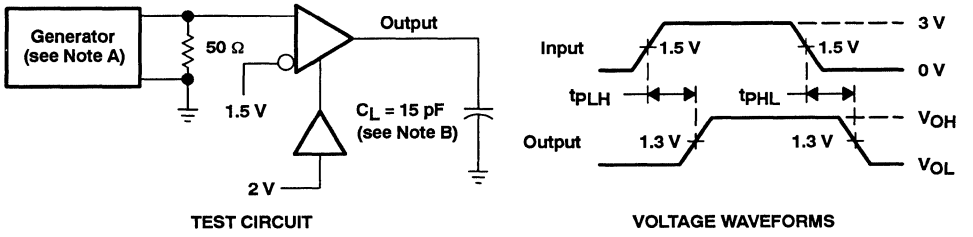


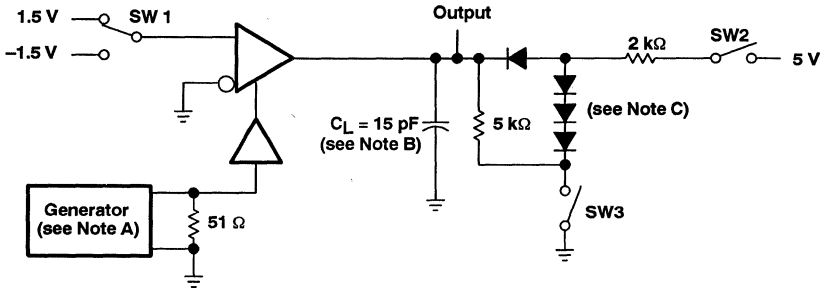
Figure 1. V_{OH}, V_{OL}



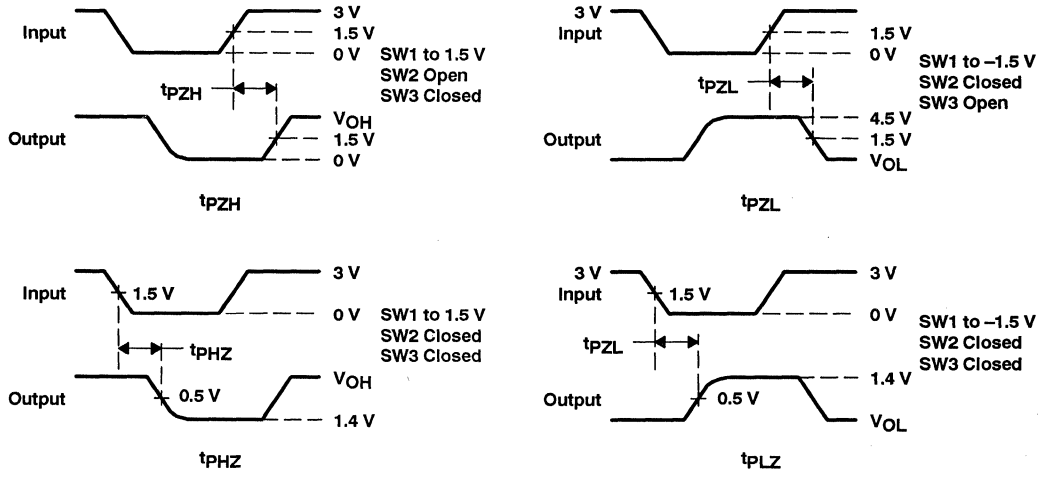
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.

Figure 2. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

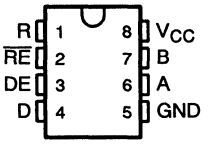
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 3. Enable and Disable Times

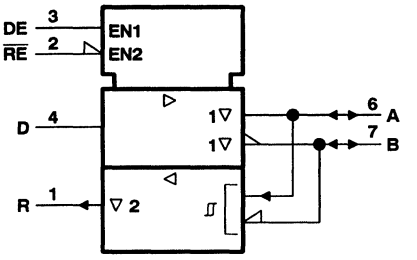
SLLS100 – D2619, JUNE 1984 – REVISED AUGUST 1989

- **Bidirectional Transceiver**
- **Meets EIA Standards RS-422-A and CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

D OR P PACKAGE
(TOP VIEW)

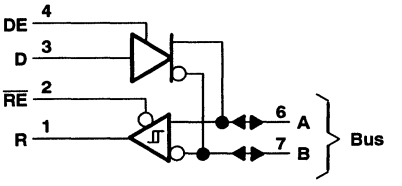


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meet EIA Standard RS-422-A and CCITT Recommendations V.11 and X.27.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

Function Tables

DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

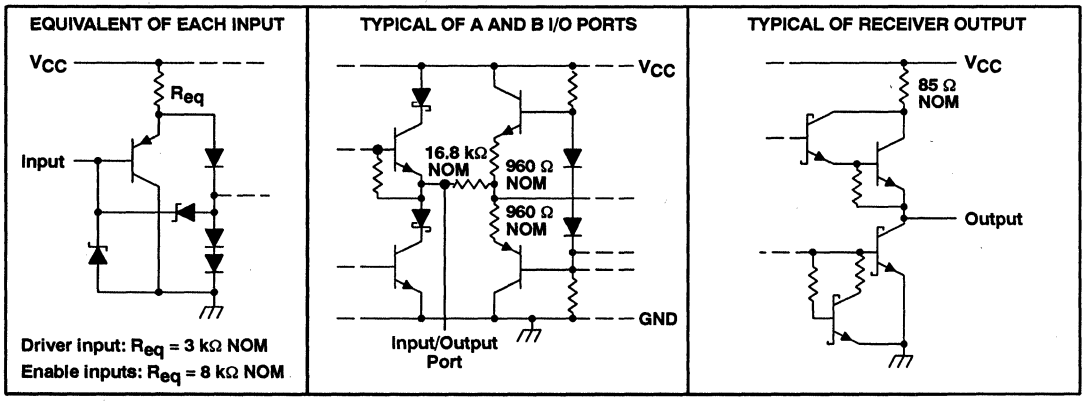
description (continued)

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission line applications employing the SN75172 and SN75174 quad differential line drivers and SN75173 and SN75175 quad differential line receivers.

The SN75176A is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{OH} = -33$ mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA			1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2	2.7		V
		R_L = 54 Ω,	See Figure 1	1.5	2.4		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡					±0.2	V
V_{OC}	Common-mode output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = V_{CC}$				250	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-422A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 60 Ω,	See Figure 3		40	60	ns
t_{tD}	Differential-output transition time				65	95	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		55	90	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		85	130	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	40	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Enable clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 3	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 3: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	30	ns
t_{PZL}	Output enable time to low level			12	30	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

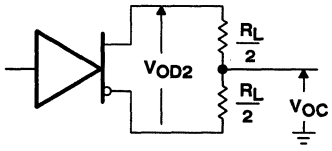


Figure 1. Driver V_{OD} and V_{OC}

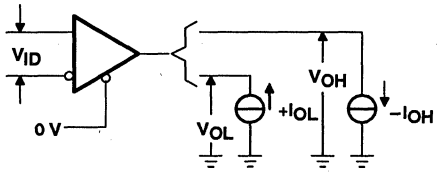
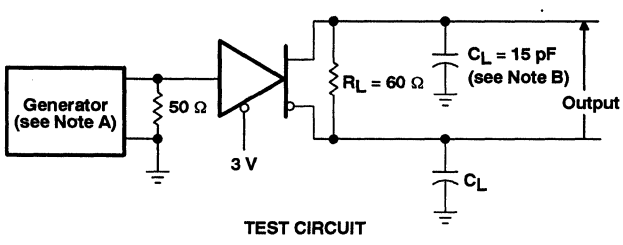


Figure 2. Receiver V_{OH} and V_{OL}



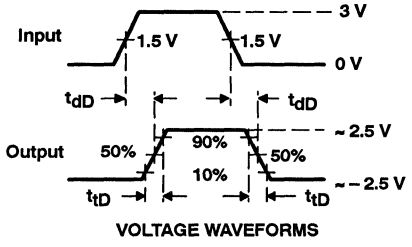
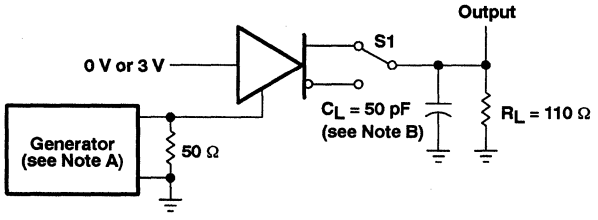


Figure 3. Driver Test Circuit and Voltage Waveforms



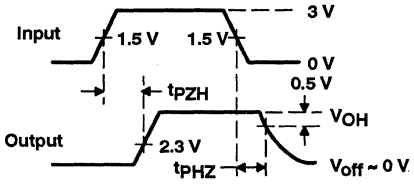
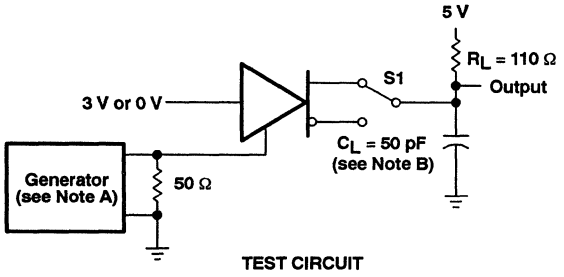


Figure 4. Driver Test Circuit and Voltage Waveforms



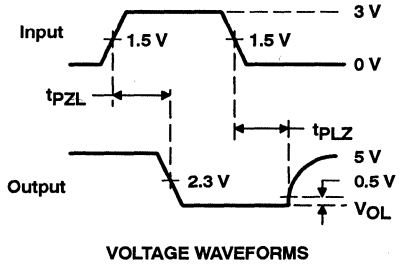


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

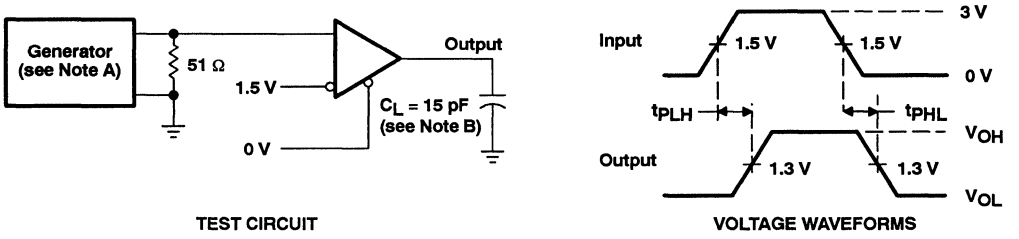


Figure 6. Receiver Test Circuit and Voltage Waveforms

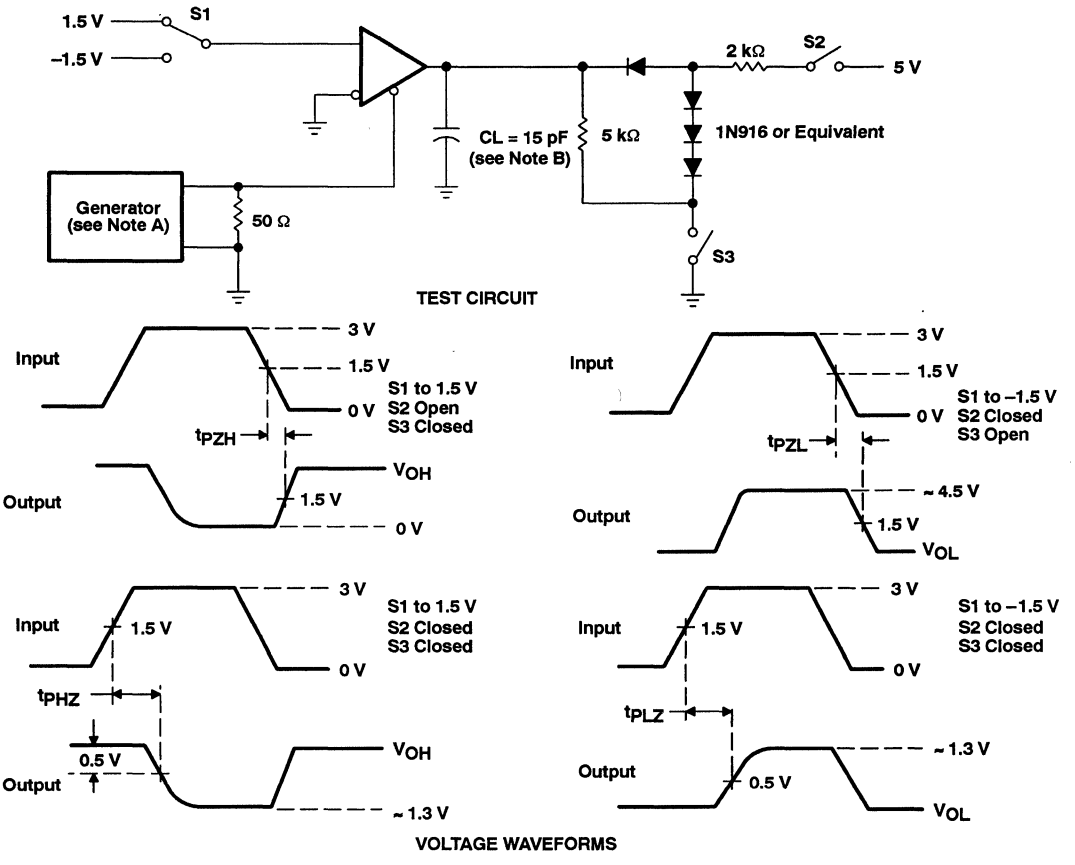


Figure 7. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

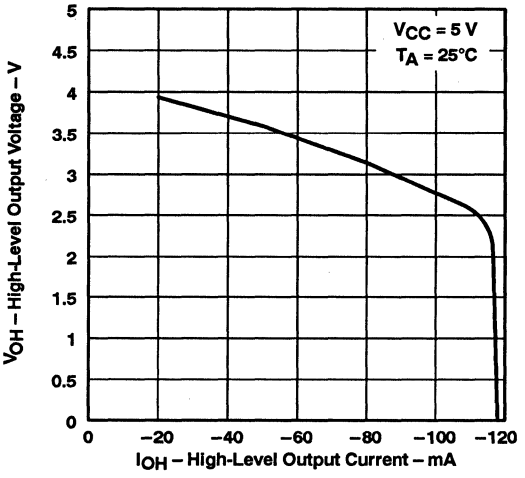


Figure 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

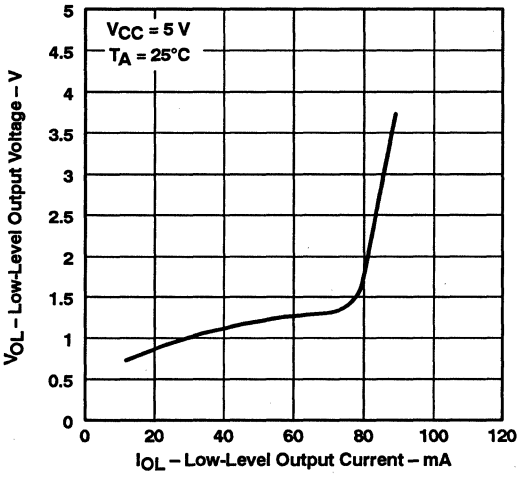


Figure 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

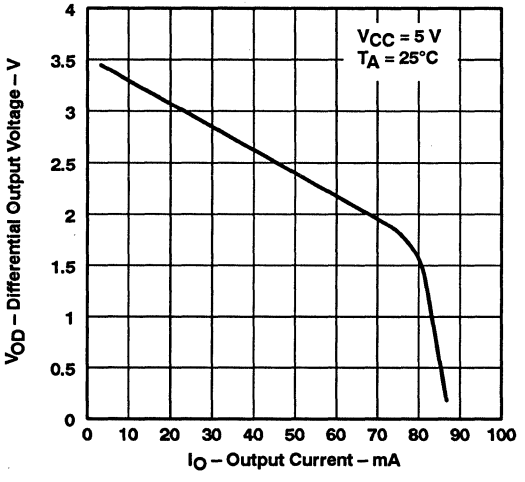


Figure 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

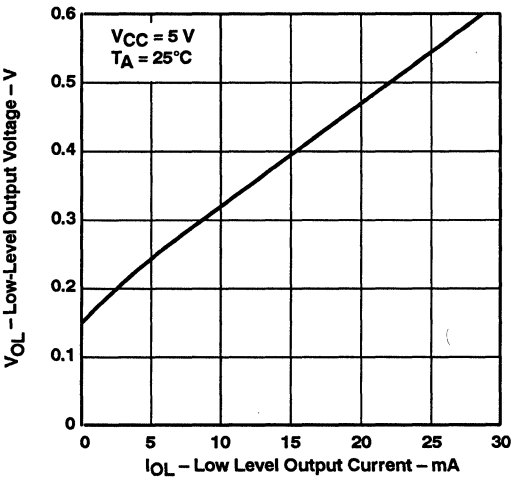


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

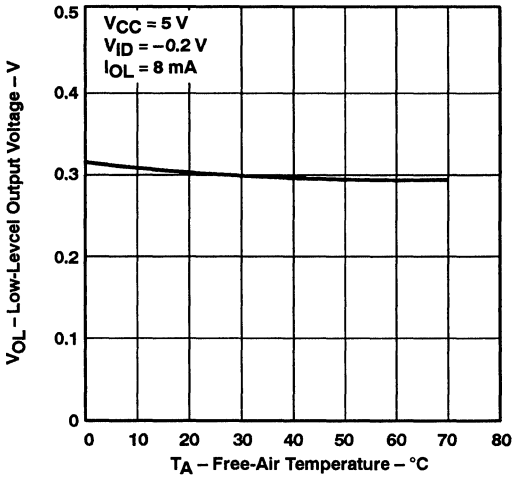


Figure 12

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

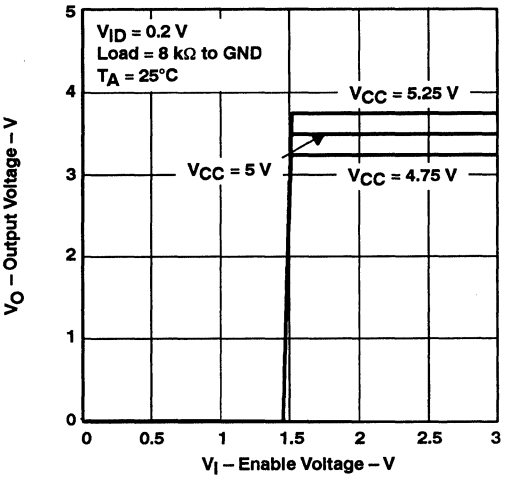


Figure 13

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

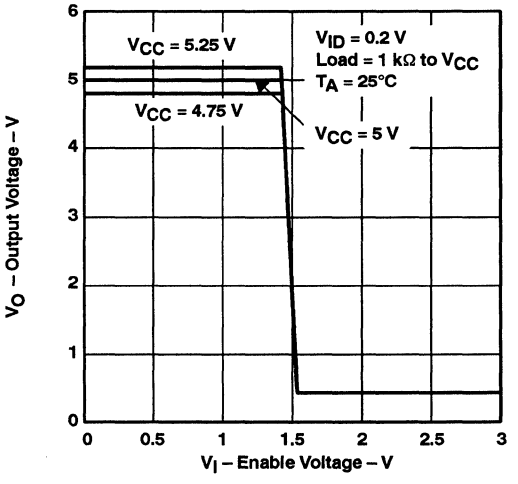


Figure 14

APPLICATION INFORMATION

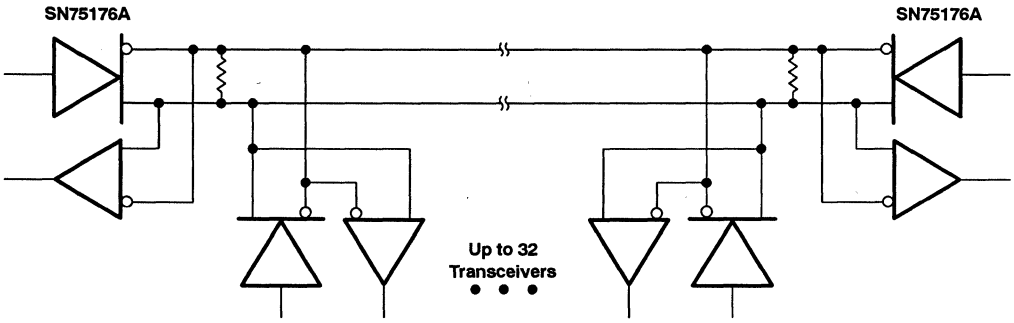
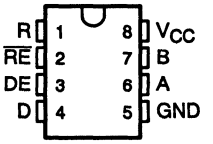


Figure 15. Typical Application Circuit

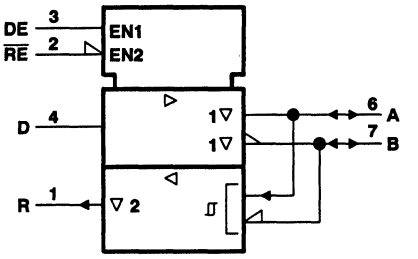
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)

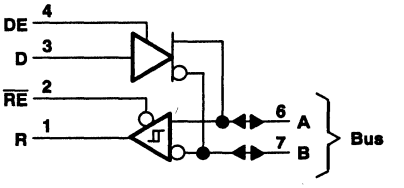


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

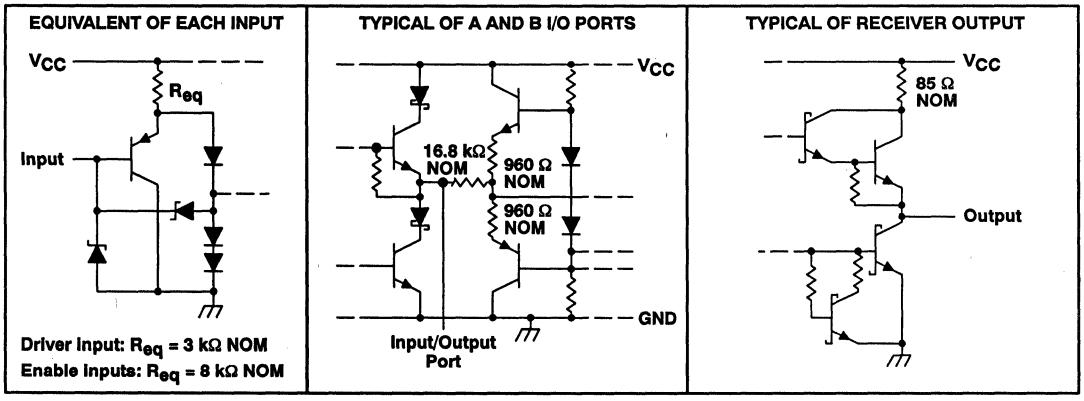
description (continued)

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B characterized for operation from −40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65176B ..... −40°C to 105°C
SN75176B ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	702 mW	396 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65176B	−40		105	°C
	SN75176B	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$		1.5	6	6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2 V_{OD1} or 2¶			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 5	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTES: 1. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
2. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics, V_{CC} = 5 V, R_L = 110 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω, See Figure 3		15	20	ns
t_{tD}	Differential-output transition time			20	30	ns
t_{PZH}	Output enable time to high level	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Enable clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 3: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

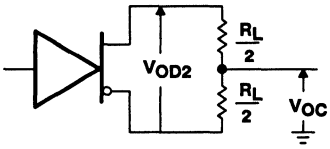


Figure 1. Driver V_{OD} and V_{OC}

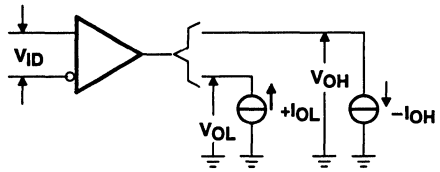
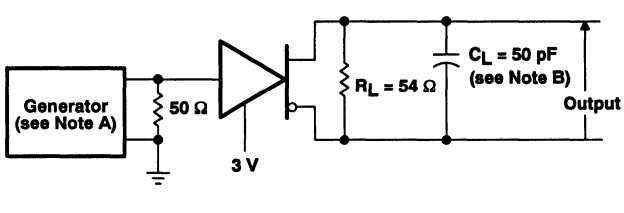
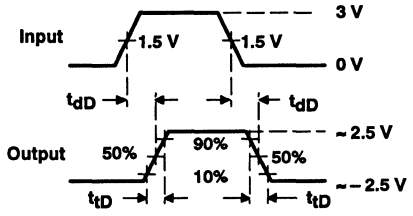


Figure 2. Receiver V_{OH} and V_{OL}

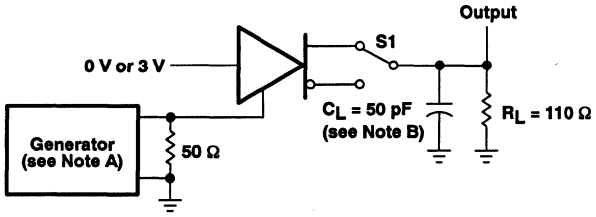


TEST CIRCUIT

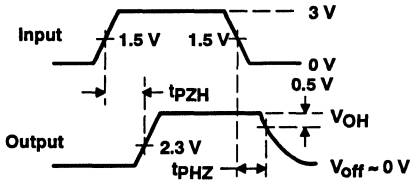


VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms

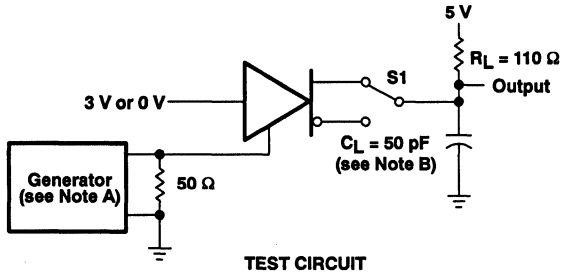


TEST CIRCUIT

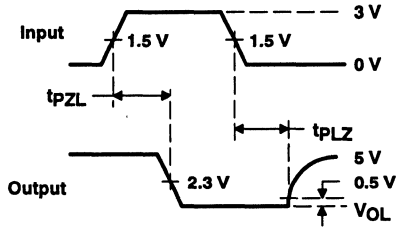


VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

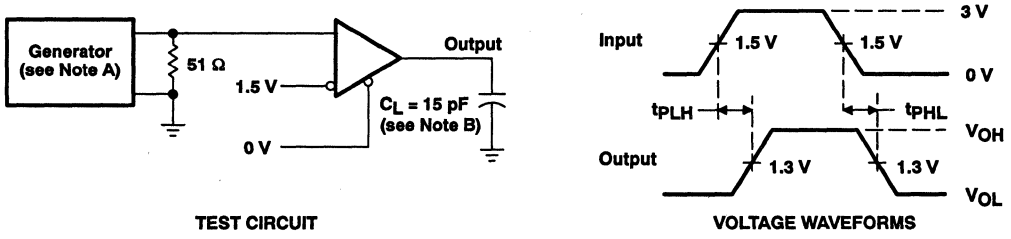


Figure 6. Receiver Test Circuit and Voltage Waveforms

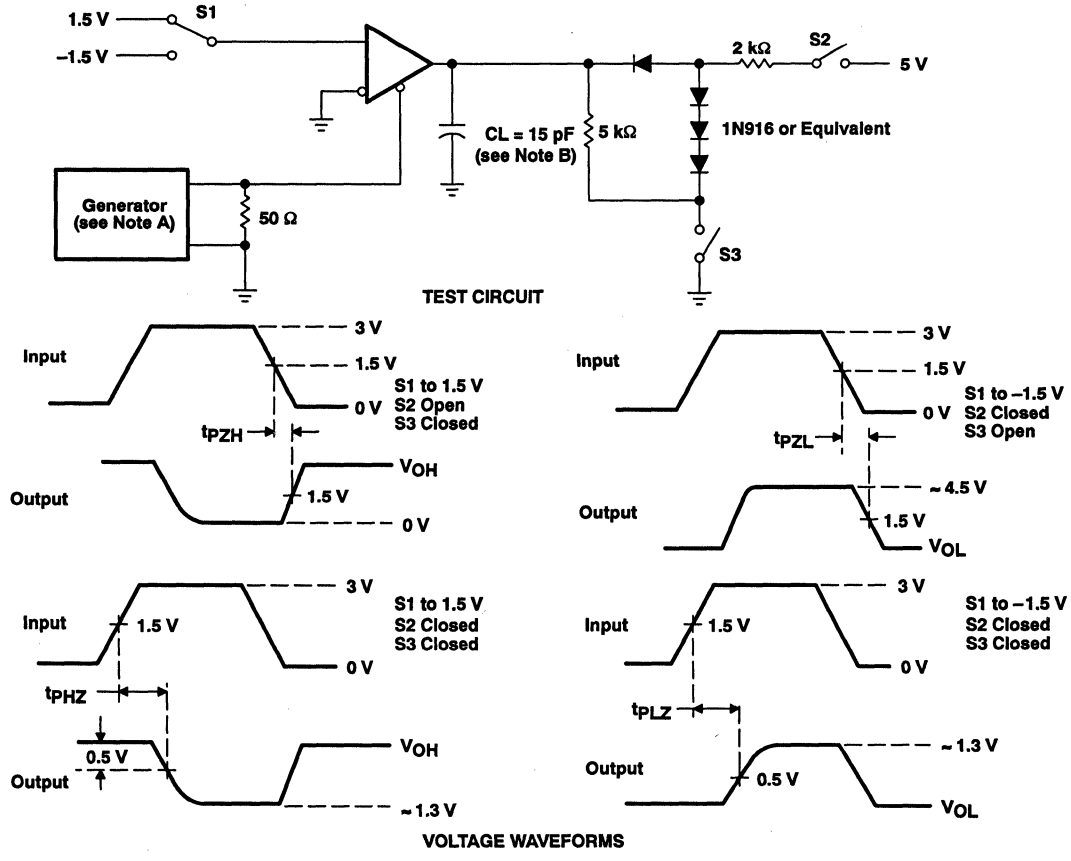


Figure 7. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

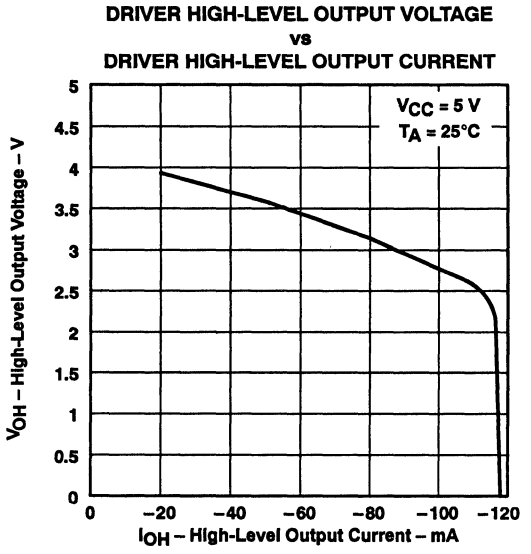


Figure 8

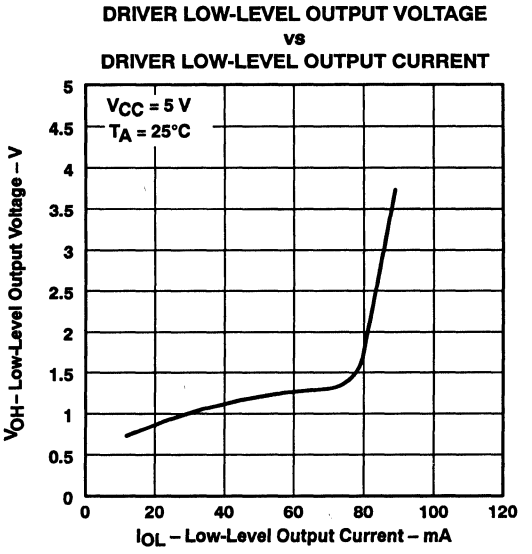


Figure 9

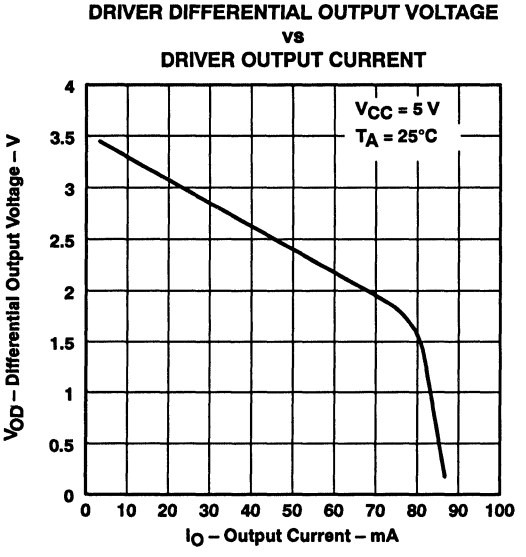


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

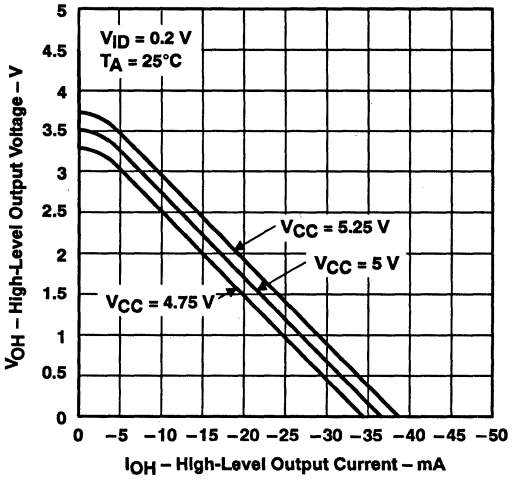


Figure 11

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

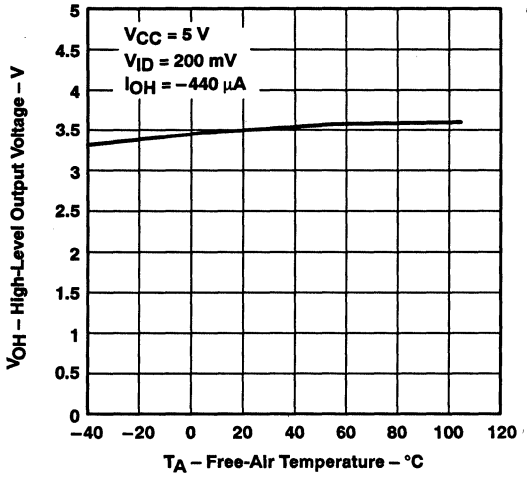


Figure 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

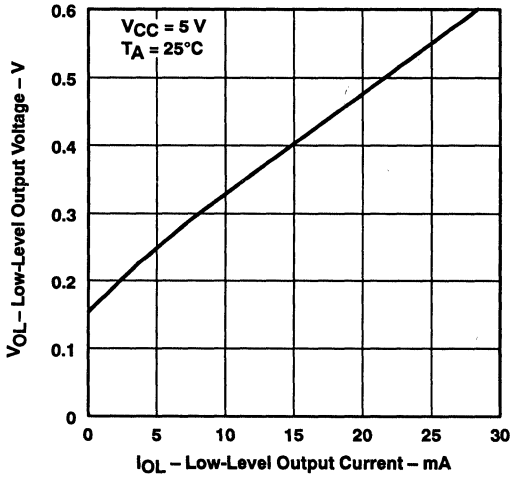


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

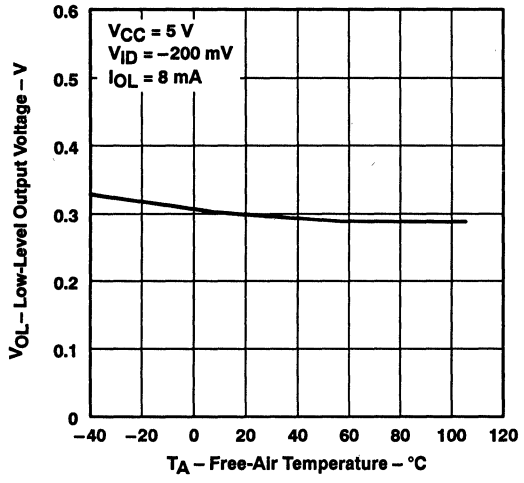


Figure 14

† Only the 0°C to 70°C portion of the curve applies to the SN75176B.

TYPICAL CHARACTERISTICS

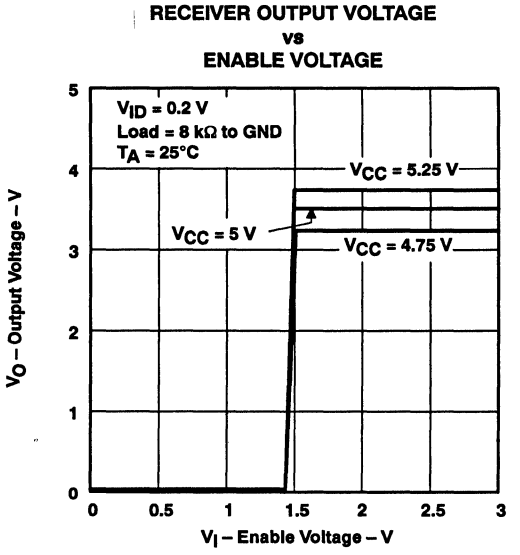


Figure 15

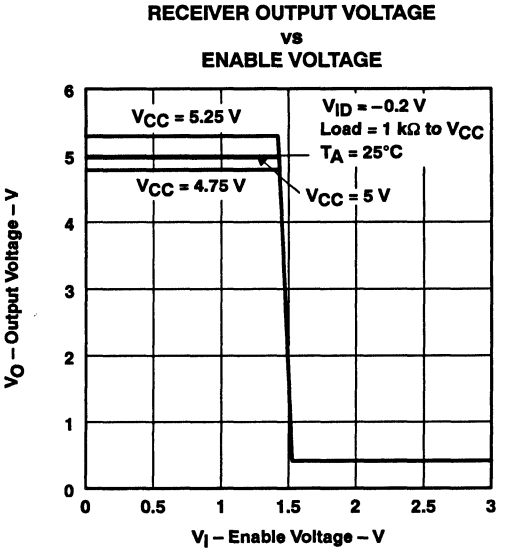


Figure 16

APPLICATION INFORMATION

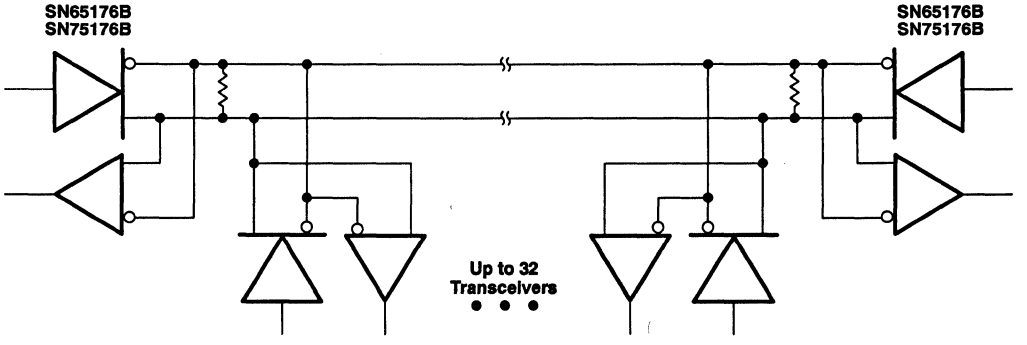


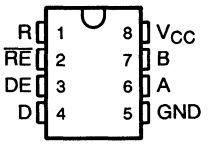
Figure 17. Typical Application Circuit

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

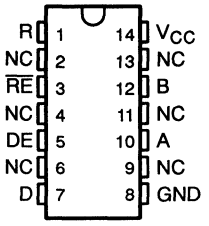
SGLS026 – D3272, MARCH 1989

- **Bidirectional Transceiver**
- **Suitable for Most EIA Standards RS-422-A and RS-485 Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

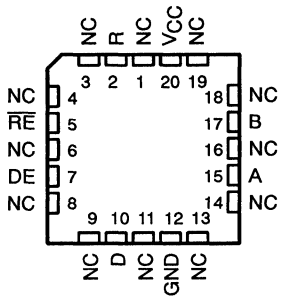
JG PACKAGE
(TOP VIEW)



W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN95176B differential bus transceiver is a monolithic integrated circuit designed for bi-directional data communication on multipoint bus transmission lines. The transceiver is suitable for most RS-422-A and RS-485 applications to the extent of the specified data sheet characteristics and operating conditions.

The SN95176B combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN95176B is characterized for operation from −40°C to 110°C.

Function Tables

DRIVER

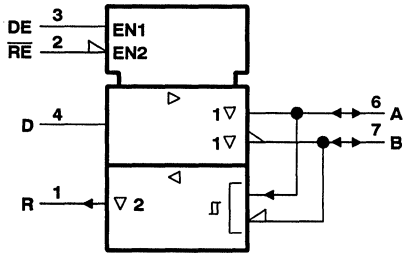
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

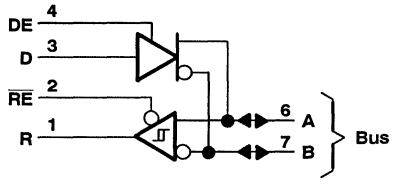
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†

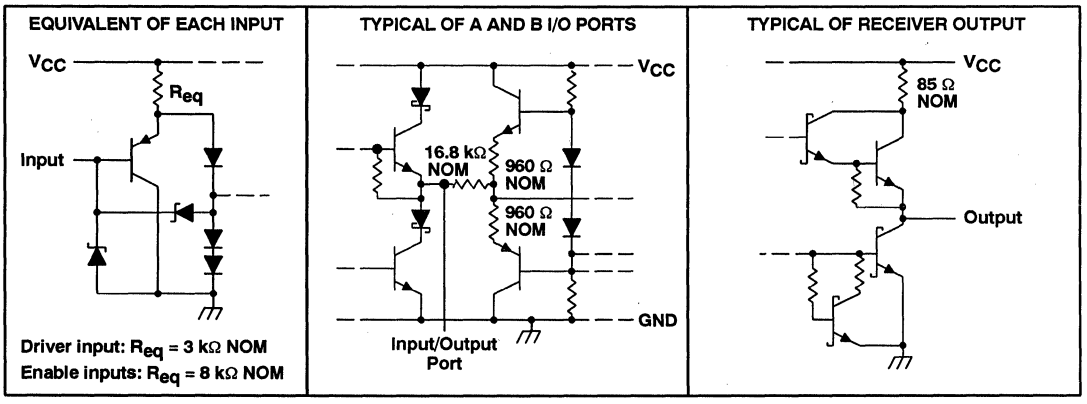


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JG package.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... −40°C to 110°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or W package ..... 300°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 110°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	336 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	320 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		−40		110	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	2			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 3			4		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	$R_L = 54\ \Omega$,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 4	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 12$ V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTES: 3. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
4. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	$R_L = 54\ \Omega$,	See Figure 3		15	22	ns
t_{tD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Enable clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

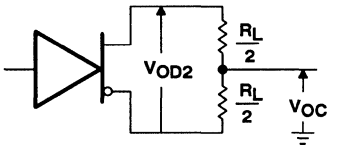


Figure 1. Driver V_{OD} and V_{OC}

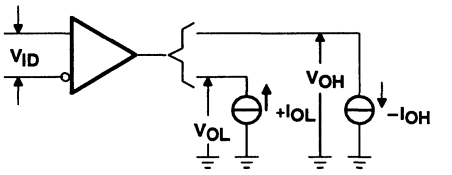


Figure 2. Receiver V_{OH} and V_{OL}

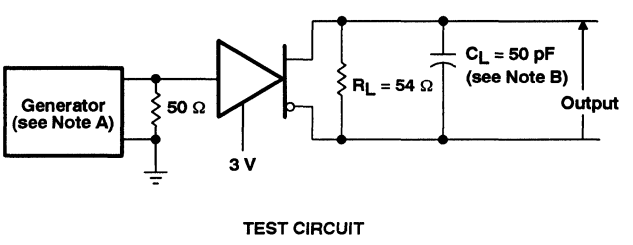


Figure 3. Driver Test Circuit and Voltage Waveforms

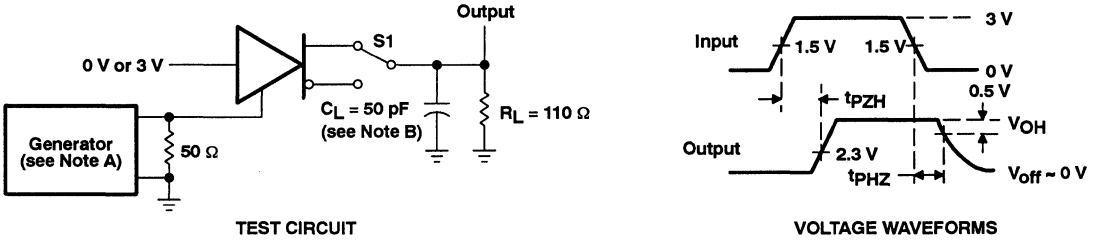


Figure 4. Driver Test Circuit and Voltage Waveforms

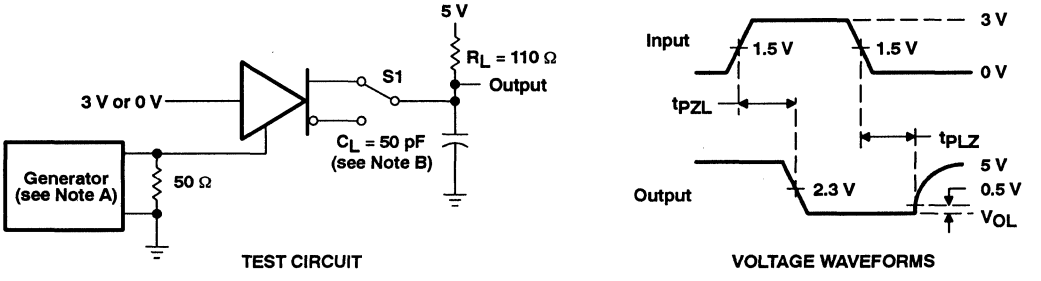


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Equivalent test circuits may be substituted for actual testing.

PARAMETER MEASUREMENT INFORMATION

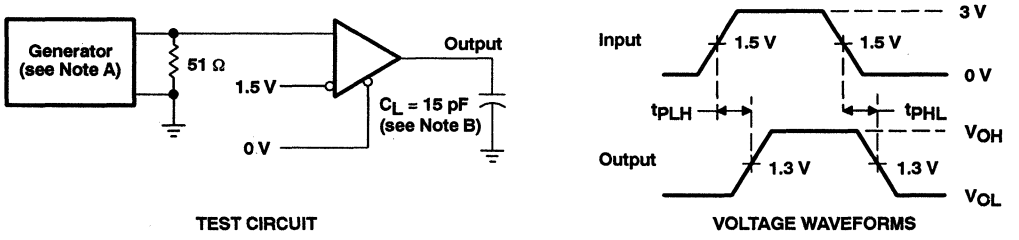


Figure 6. Receiver Test Circuit and Voltage Waveforms

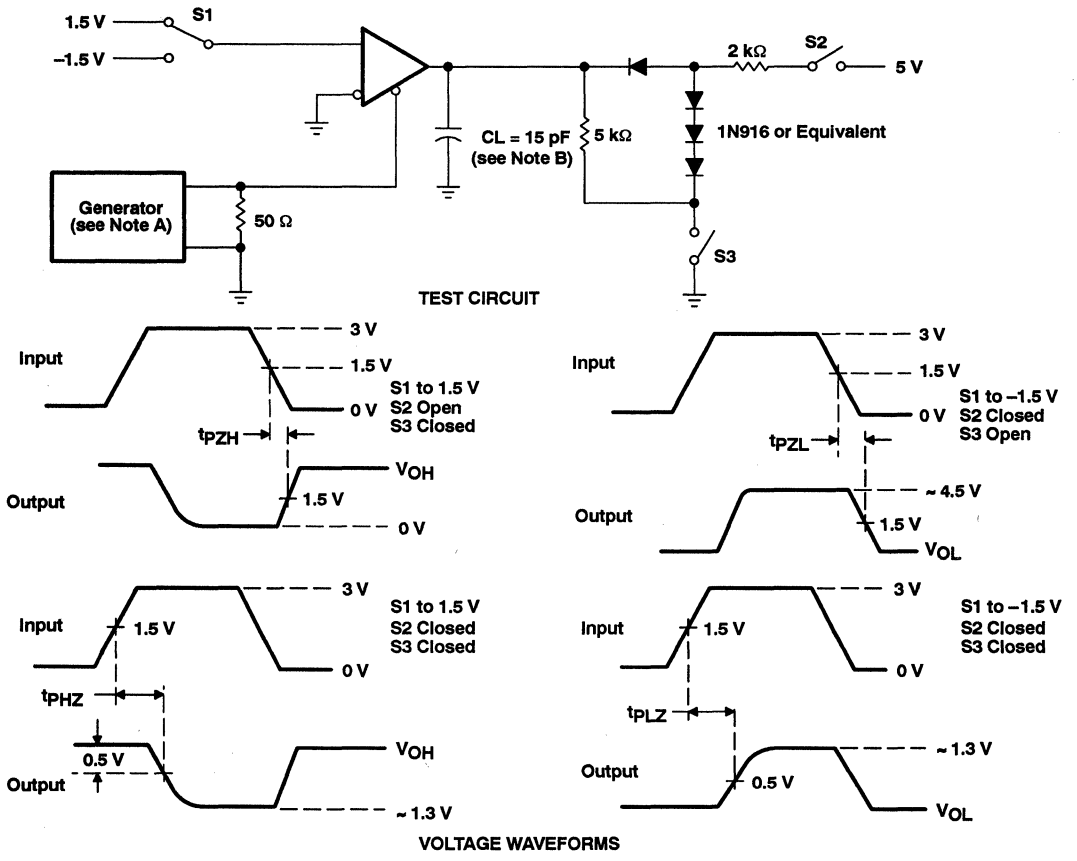


Figure 7. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. Equivalent test circuits may be substituted for actual testing.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

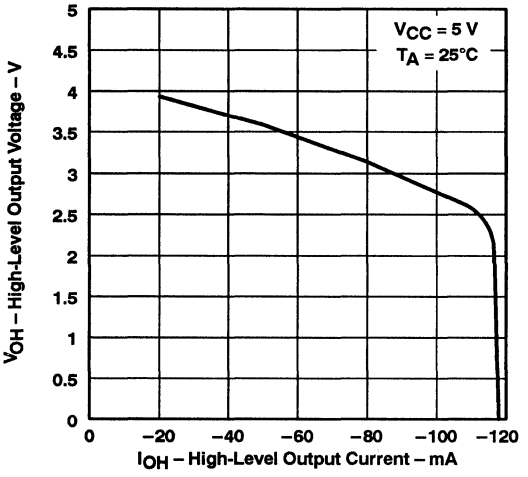


Figure 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

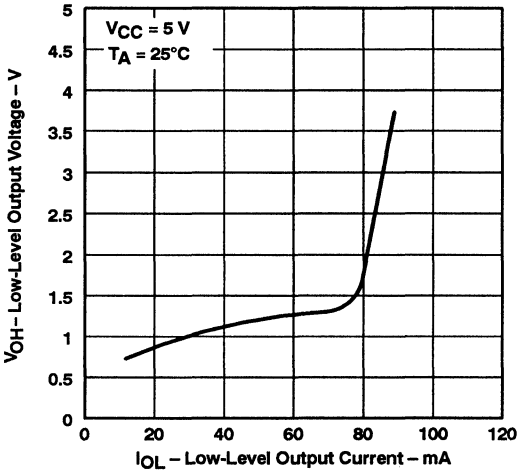


Figure 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

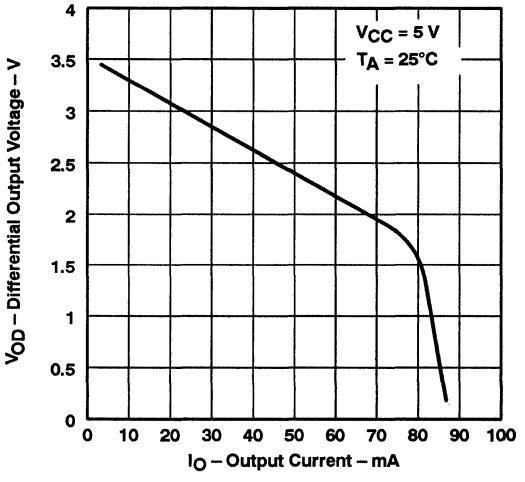


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

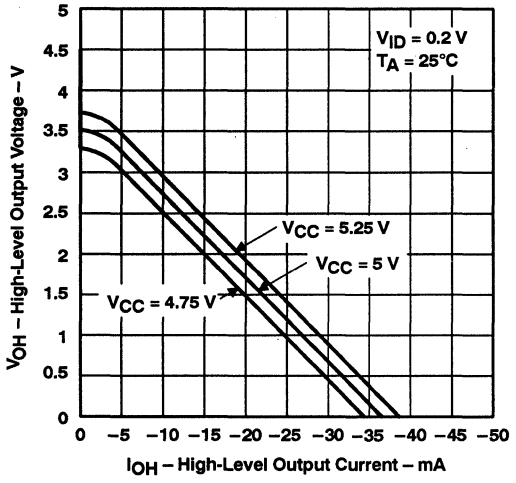


Figure 11

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

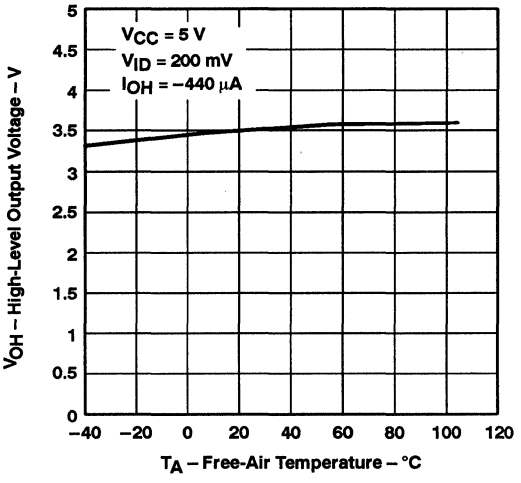


Figure 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

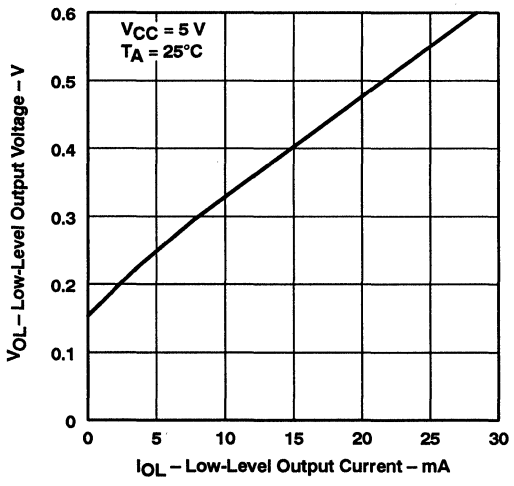


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

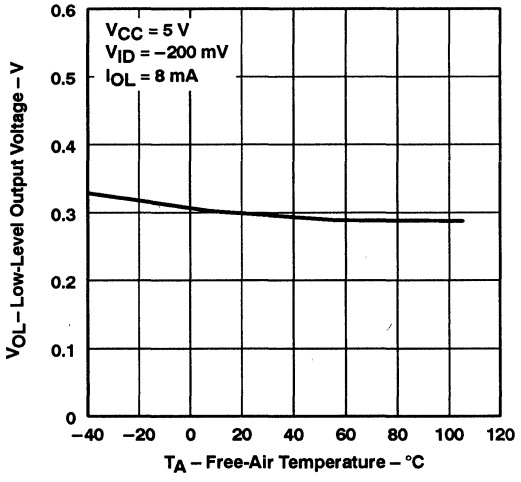


Figure 14

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

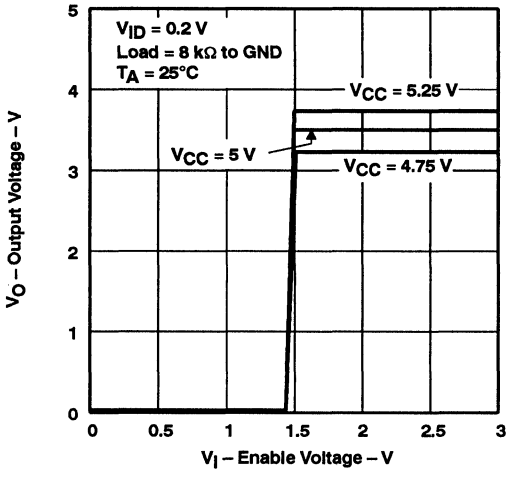


Figure 15

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

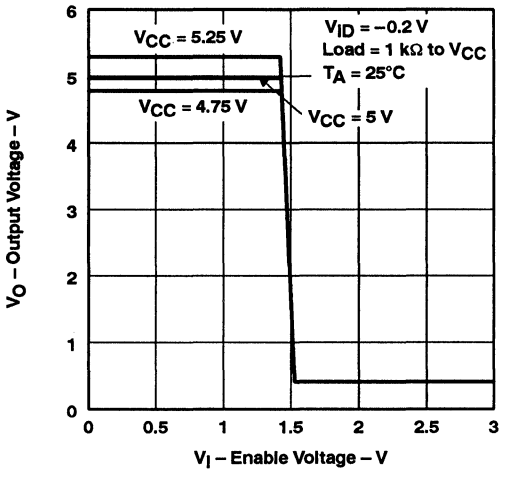


Figure 16

APPLICATION INFORMATION

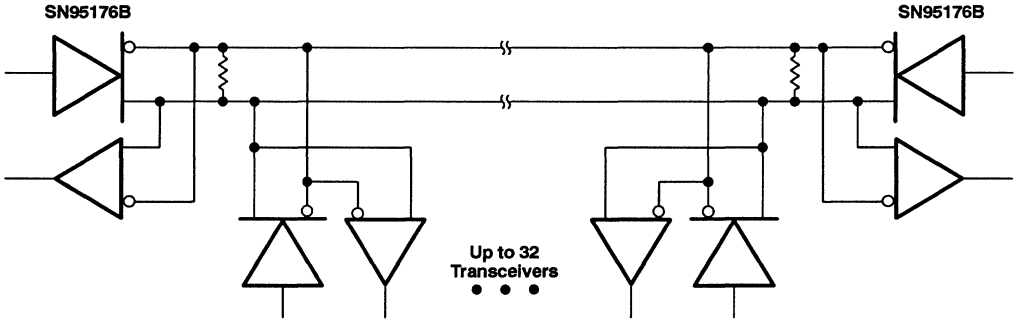


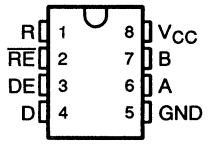
Figure 17. Typical Application Circuit

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

SLLS040D – D3042, AUGUST 1987 – REVISED AUGUST 1991

- **Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27**
- **Designed and Tested for Data Rates up to 35 MBaud**
- **SN65ALS176 Operating Temperature −40°C to 85°C**
- **Three Skew Limits Available:**
  'ALS176 . . . 10 ns
  'ALS176A . . . 7.5 ns
  'ALS176B . . . 5 ns
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Hysteresis**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Receiver Open-Circuit Fail-Safe Design**

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

T_A	$t_{sk(LIM)}$‡	PACKAGE	
		SMALL OUTLINE (D)†	PLASTIC DIP (P)
0°C to 70°C	10	SN75ALS176D	SN75ALS176P
	7.5	SN75ALS176AD	SN75ALS176AP
	5	SN75ALS176BD	SN75ALS176BP
−40°C to 85°C	10	SN65ALS176D	SN65ALS176P

† The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75ALS176DR).

‡ $t_{sk(LIM)}$ is the greater of 1) the difference between the maximum and minimum specified values of t_{PLH} (or t_{dDH}), and 2) the difference between the maximum and minimum specified values of t_{PHL} (or t_{dDL}). This is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device to device.

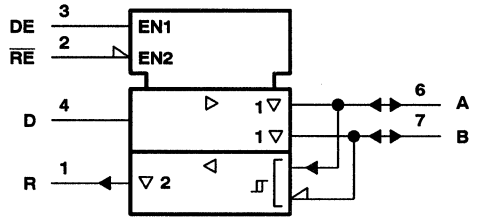
description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

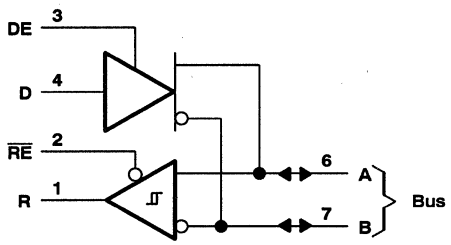
The SN65ALS176 is characterized for operation from −40°C to 85°C, and the SN75ALS176 series is characterized for operation from 0°C to 70°C.

logic symbol†

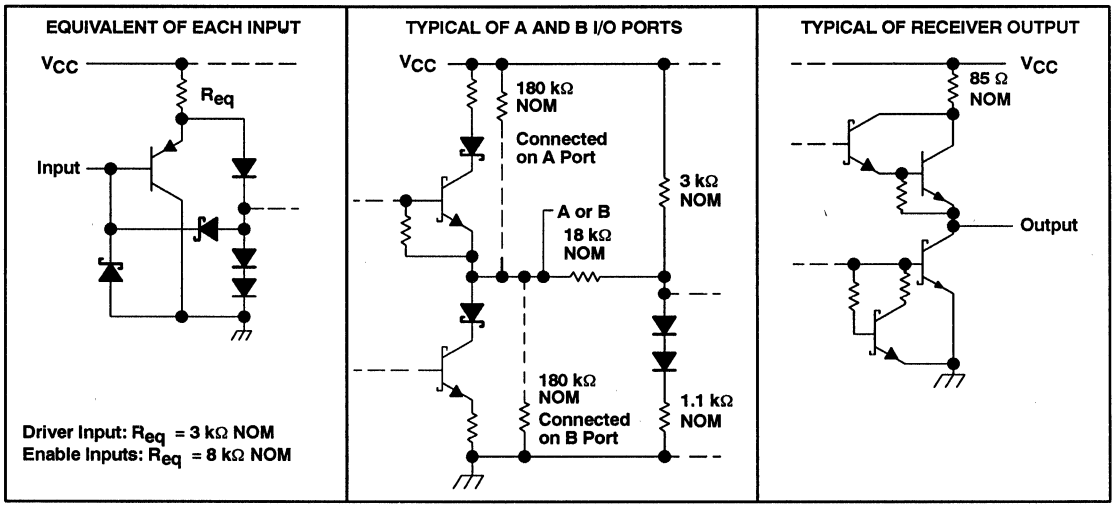


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −7 V to 12 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS176 ..... −40°C to 85°C
SN75ALS176 series ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS176	−40		85	°C
	SN75ALS176	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2¶			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Outputs disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −4 V	SN65ALS176			−250	mA
		V_O = −6 V	SN75ALS176				
		V_O = 0				−150	
		$V_O = V_{CC}$				250	
		V_O = 8 V					
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTE 3: This applies for both power on and power off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{dD}	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3			15	ns
$t_{sk(p)}$	Pulse skew ($\|t_{dDL} - t_{dDH}\|$)			0	2	ns
t_{tD}	Differential output transition time			8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{dD}	Differential output delay time	'ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3	3	8	13	ns
		'ALS176A		4	7	11.5	
		'ALS176B		5	8	10	
$t_{sk(p)}$	Pulse skew ($\|t_{dDL} - t_{dDH}\|$)				0	2	ns
t_{TD}	Differential output transition time				8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
V_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7			25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0	2	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		11	18	ns
t_{PZL}	Output enable time to low level			11	18	ns
t_{PHZ}	Output disable time from high level				50	ns
t_{PLZ}	Output disable time from low level				30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	9	14	19	ns
		'ALS176A		10.5	14	18	
		'ALS176B		11.5	13	16.5	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				0	2	ns
t_{PZH}	Output enable time to high level		C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level				20	35	ns
t_{PHZ}	Output disable time from high level				20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

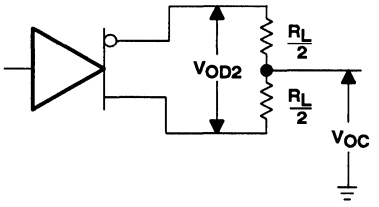


Figure 1. Driver V_{OD2} and V_{OC}

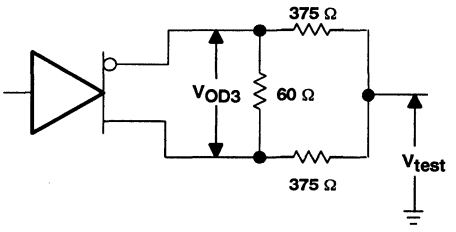
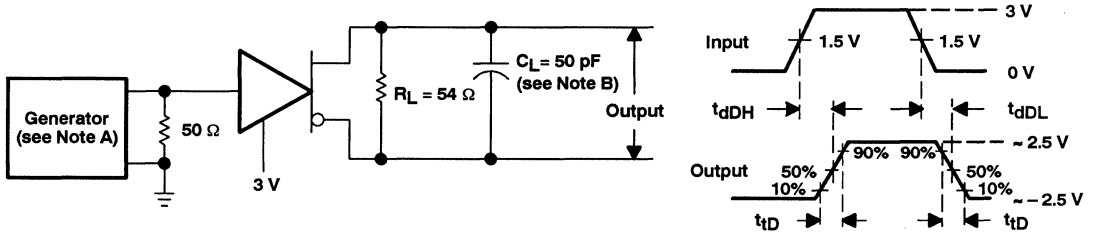


Figure 2. Driver V_{OD3}

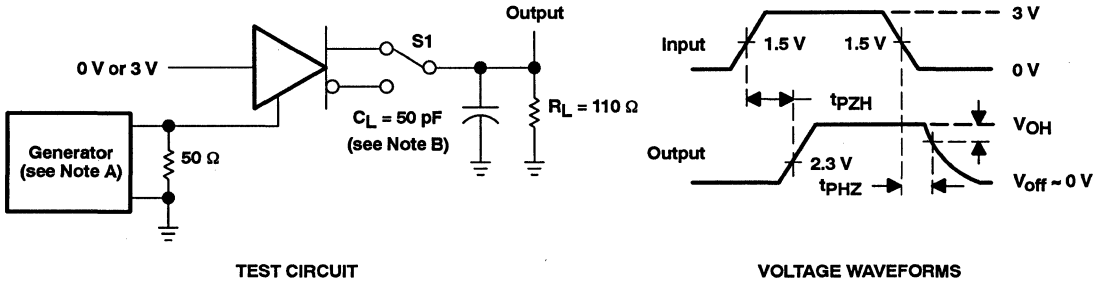


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. $t_{dD} = t_{dDH}$ or t_{dDL}

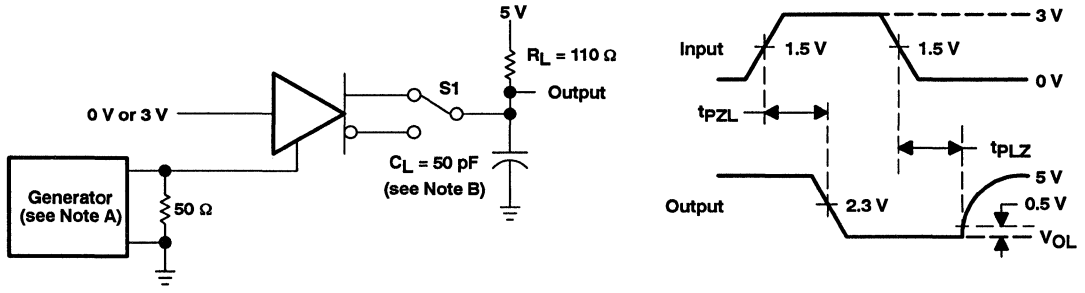
Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waeforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

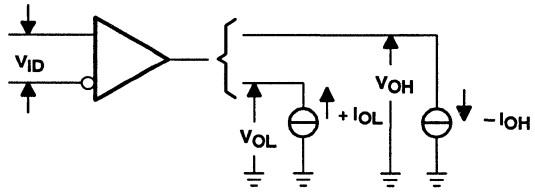


Figure 6. Receiver V_{OH} and V_{OL} Test Circuit

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PARAMETER MEASUREMENT INFORMATION

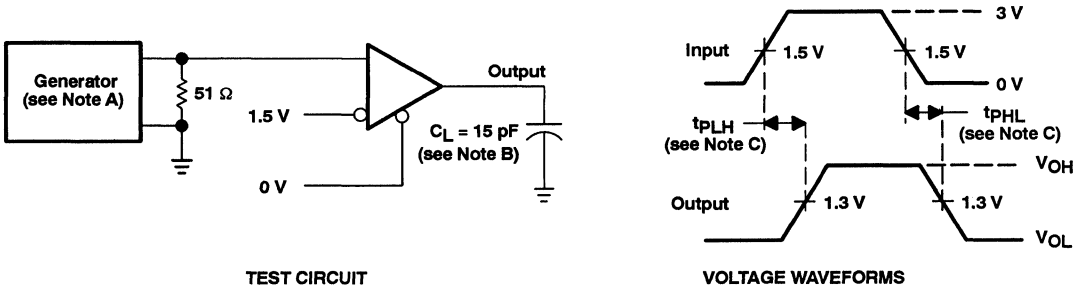


Figure 7. Receiver Test Circuit and Voltage Waveforms

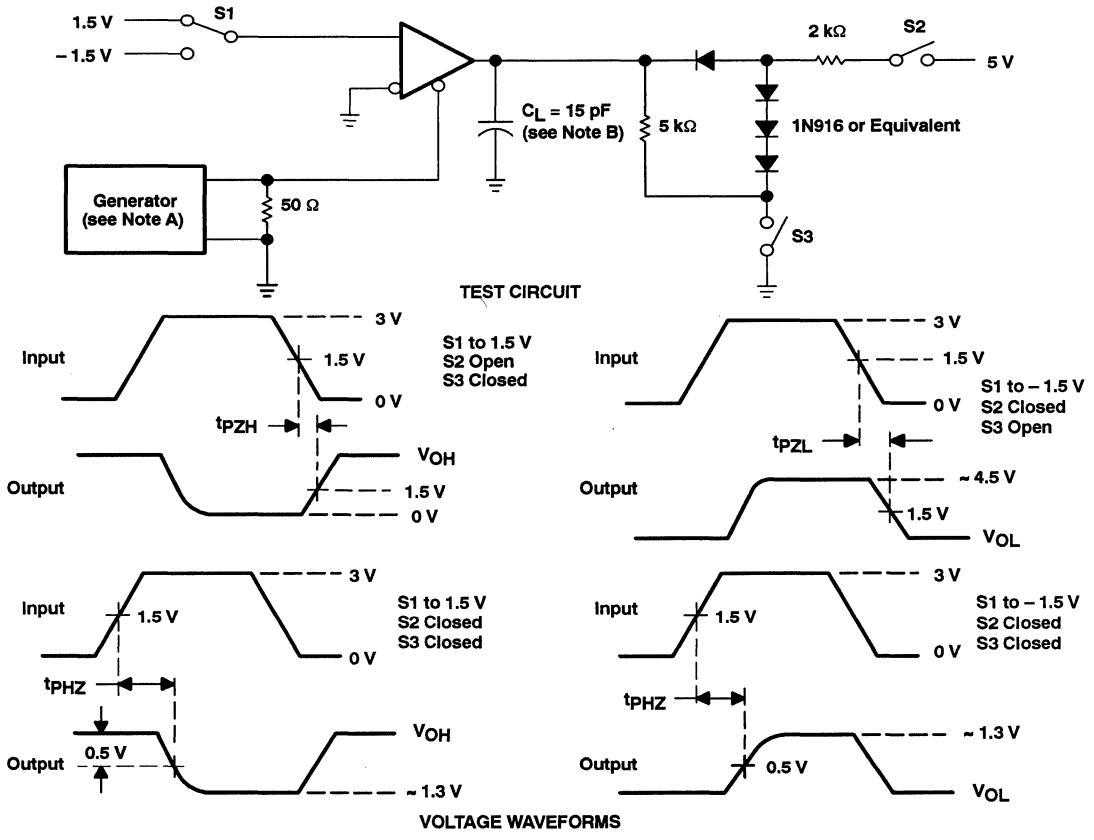


Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. $t_{pd} = t_{PLH}$ or t_{PHL}

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

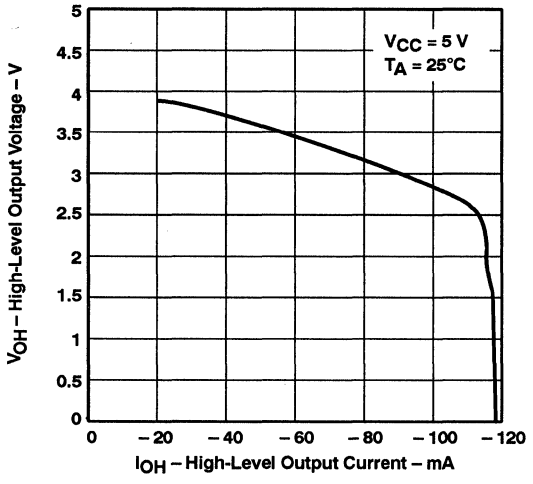


Figure 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

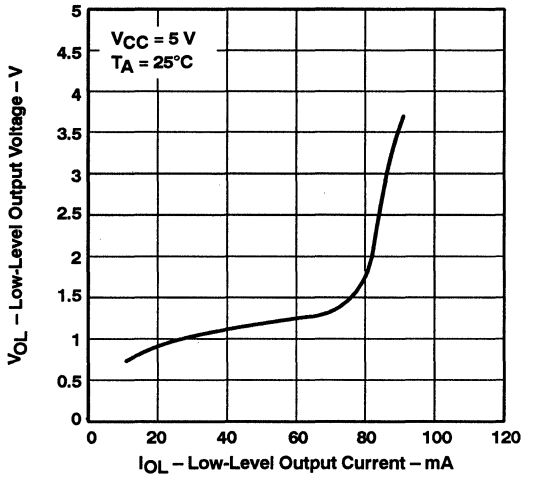


Figure 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

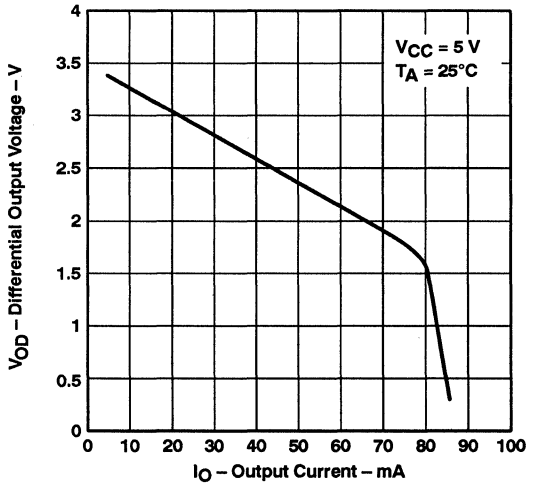


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

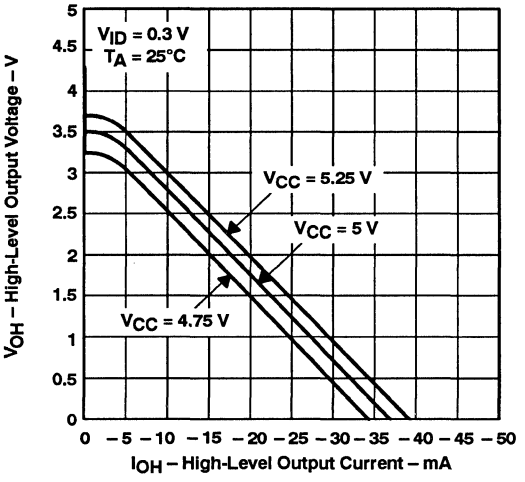


Figure 12

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

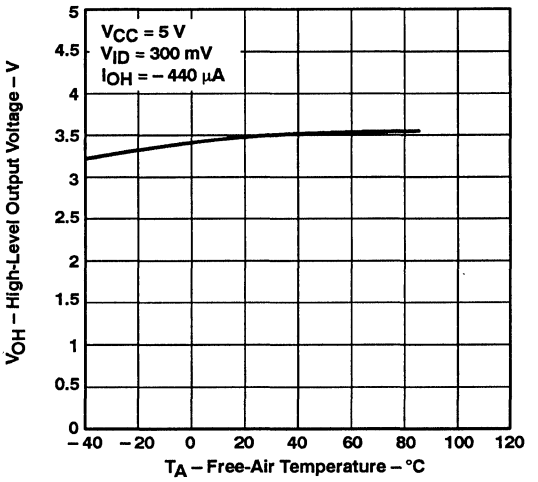


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

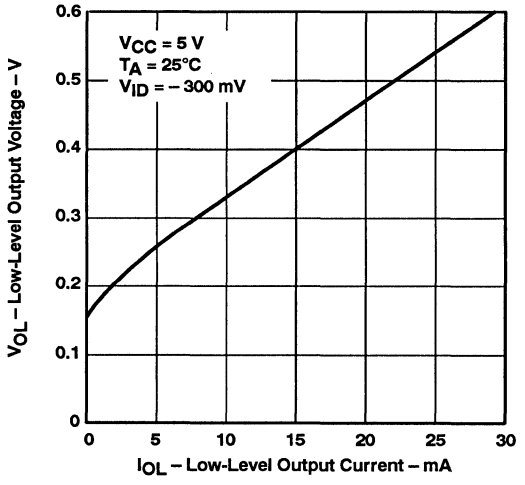


Figure 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

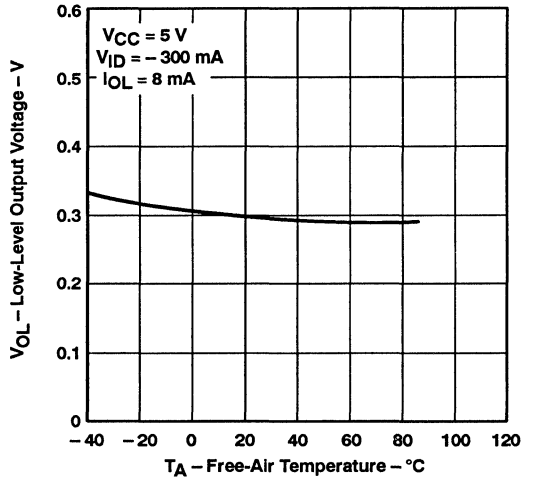


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

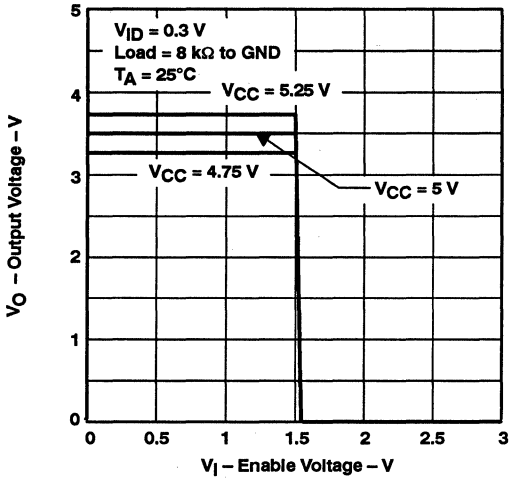


Figure 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

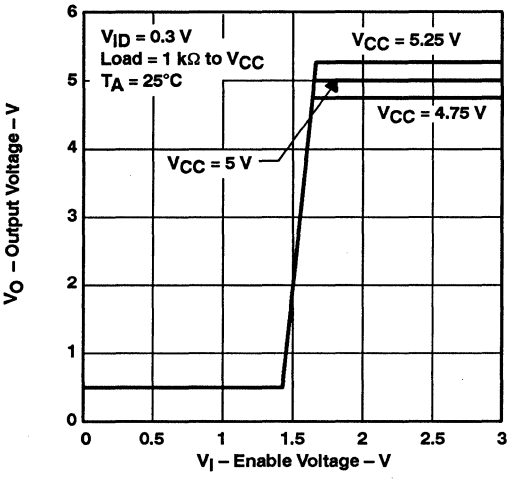
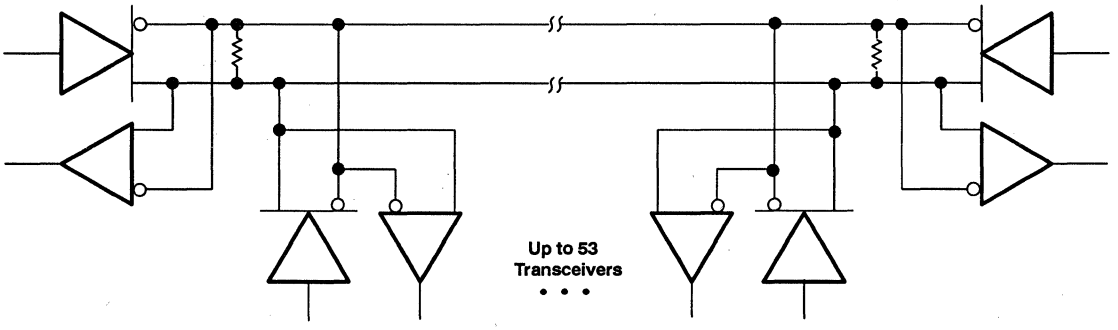


Figure 17

APPLICATION INFORMATION



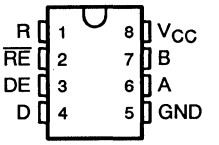
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

SLLS067B – D3502, AUGUST 1990 – REVISED FEBRUARY 1993

- **Bidirectional Transceiver**
- **Meets EIA Standard RS-485 and ISO 8482:1987(E)**
- **High-Speed Low-Power LinBiCMOS™ Circuitry**
- **Designed for High-Speed Operation In Both Serial and Parallel Applications**
- **Low Skew**
- **Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments**
- **Very Low Disabled Supply Current Requirements . . . 200 μA Maximum**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

D, JG, OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A–B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN55LBC176, SN65LBC176, and SN75LBC176 differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standard RS-485 and ISO 8482:1987(E).

The SN65LBC176 and SN75LBC176 combine a 3-state differential-line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party line applications. Very low device supply current can be achieved by disabling the driver and the receiver. Both the driver and receiver are available as cells in the Texas Instruments LinASIC™ Library.

These transceivers are suitable for RS-485 and ISO 8482:1987 (E) applications to the extent that they are specific in the operating conditions and characteristics section of this data sheet. Certain limits contained in the RS-485 and ISO 8482:1987 (E) are not met or cannot be tested over the entire military temperature range.

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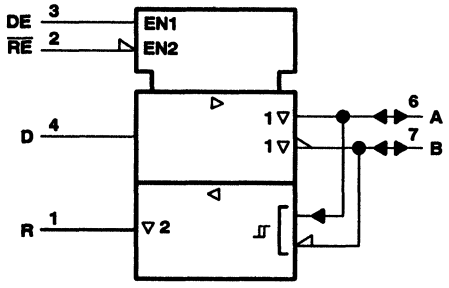
description (continued)

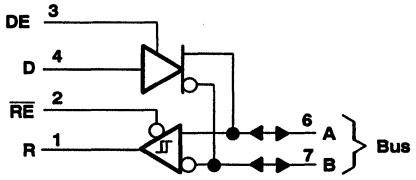
The SN55LBC176 is characterized for operation from −55°C to 125°C. The SN65LBC176 is characterized for operation from −40°C to 85°C, and the SN75LBC176 is characterized for operation from 0°C to 70°C.

logic symbol†

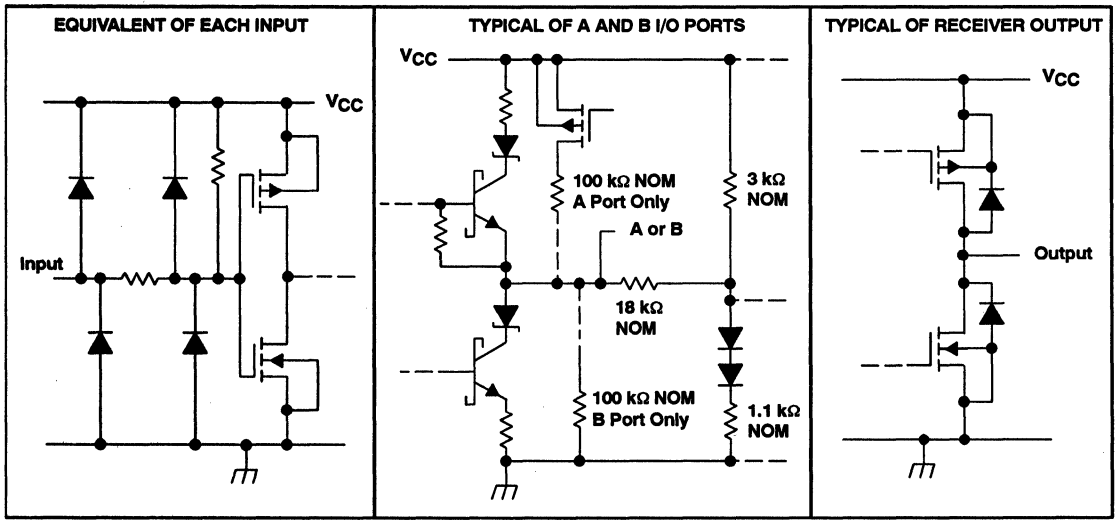


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55LBC176 ..... −55°C to 125°C
SN65LBC176 ..... −40°C to 85°C
SN75LBC176 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	336 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55LBC176	4.5	5	5.5	V
	SN65/75LBC176	4.75	5	5.25	
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN55LBC176	−55		125	°C
	SN65LBC176	−40		85	
	SN75LBC176	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0			0	6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0			1.5	6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 54 Ω, See Note 3	See Figure 1,	55LBC176	1.1		V
				65LBC176	1.1		
				75LBC176	1.5	5	
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V, See Note 3	See Figure 2,	55LCB176	1.1		V
				65LBC176	1		
				75LBC176	1.5	5	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage†	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage†					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V					
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled	55LBC176		1.75	mA
				65LBC176		1.5	
				75LBC176			
			Receiver and driver disabled	55LBC176		0.25	
				65LBC176		0.2	
				75LBC176			

† $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. This device meets the RS485 V_{OD} requirements above 0°C only.
4. This applies for both power on and off; refer to EIA standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage, operating free-air temperature

PARAMETER		TEST CONDITIONS		SN55LBC176		SN65LBC176 SN75LBC176			UNIT
				MIN	MAX	MIN	TYP†	MAX	
t_{dD}	Differential-output delay time	R_L = 54 Ω, See Figure 3	C_L = 50 pF,	8	31	8		25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{dDH} - t_{dDL} \rvert$)				6		0	6	ns
t_{PLH}	Propagation time, low-to-high-level single-ended output							26	ns
t_{PHL}	Propagation time, high-to-low-level single-ended output							26	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		65			60	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		65			60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		105			60	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		105			60	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	V_t (Test Termination Measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	
I_O	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) (see Figure 4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OL} = 8 mA,				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = −7 V				−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled	SN55LBC176			0.25	mA
				SN65LBC176			0.2	
				SN75LBC176				

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	SN55LBC176		SN65LBC176 SN75LBC176			UNIT
			MIN	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation time, low-to-high-level single-ended output	V_{ID} = −1.5 V to 1.5 V, See Figure 7	20	37	20		30	ns
t_{PHL}	Propagation time, high-to-low-level single-ended output		20	55	28		45	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{dDH} - t_{dDL} \rvert$)			22		10	18	ns
t_{PZH}	Output enable time to high level	See Figure 8		34			30	ns
t_{PZL}	Output enable time to low level			34			30	ns
t_{PHZ}	Output disable time from high level	See Figure 8		34			30	ns
t_{PLZ}	Output disable time from low level			34			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

PARAMETER MEASUREMENT INFORMATION

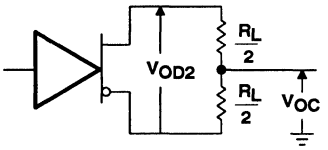


Figure 1. Driver V_{OD} and V_{OC}

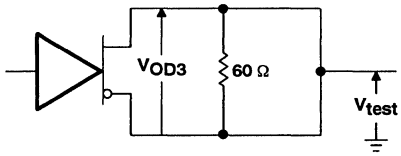


Figure 2. Driver V_{OD3}

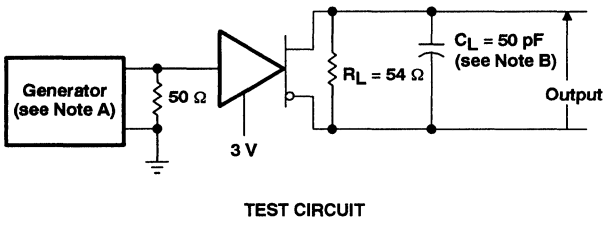


Figure 3. Driver Test Circuit and Voltage Waveforms

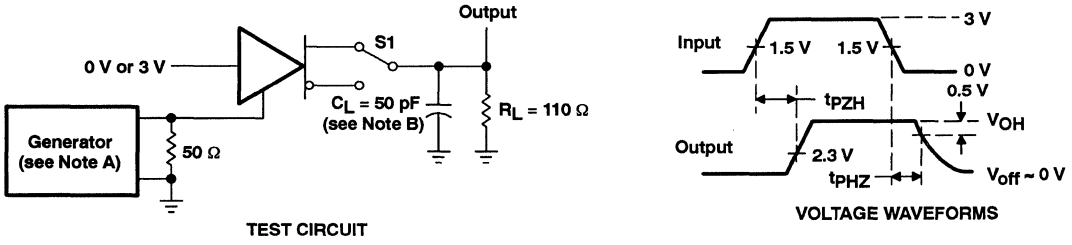


Figure 4. Driver Test Circuit and Voltage Waveforms

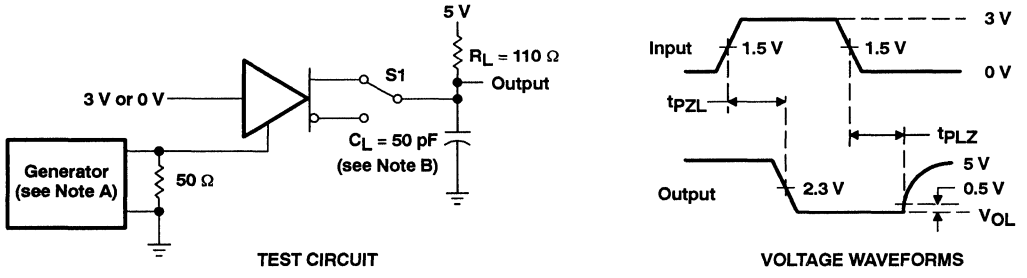


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

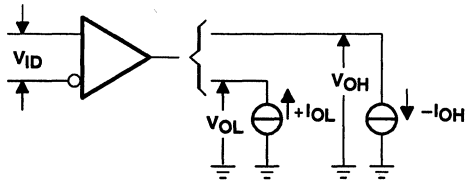


Figure 6. Receiver V_{OH} and V_{OL}

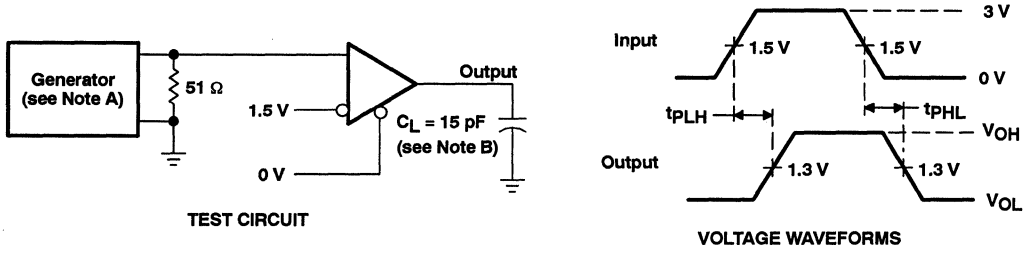


Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

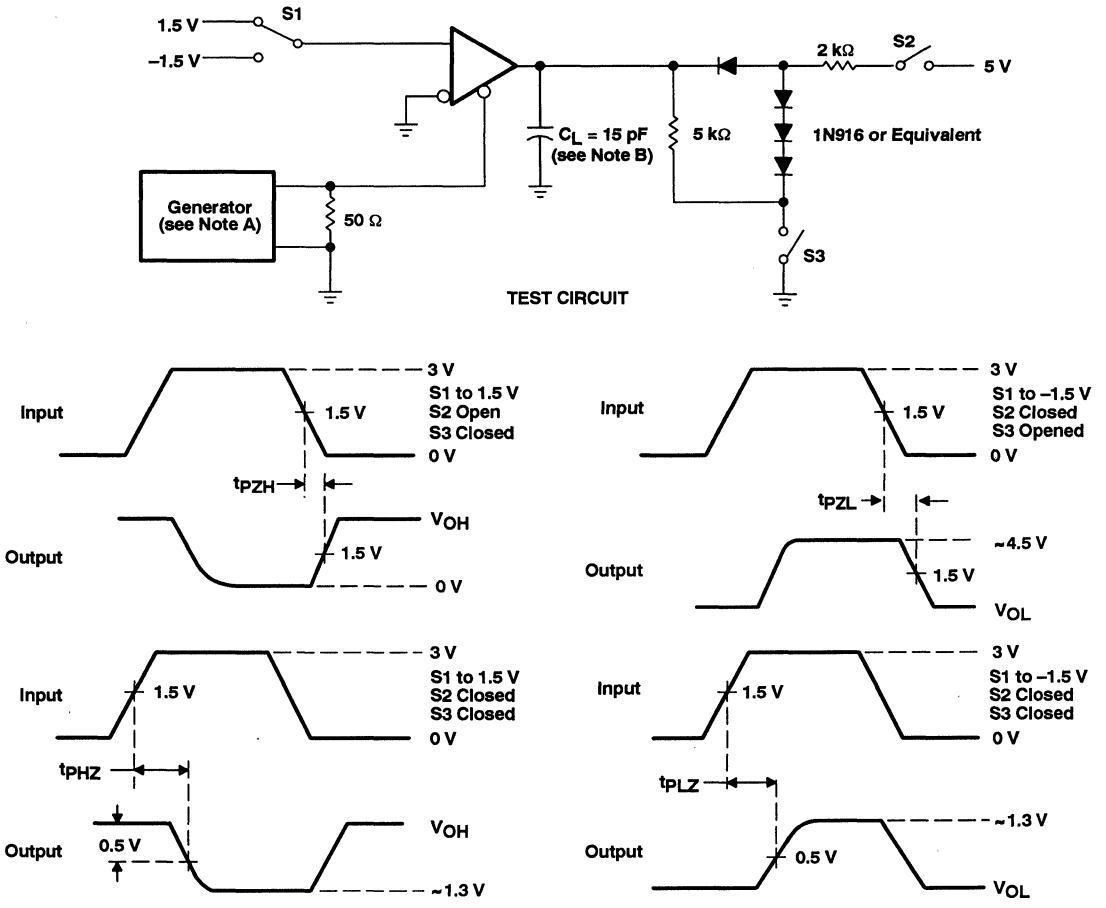


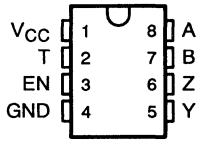
Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

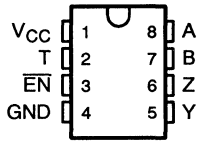
SLLS002C – D2606, JULY 1985 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Bus Voltage Range . . . –7 V to 12 V**
- **Positive and Negative Current Limiting**
- **Driver Output Capability . . . 60 mA Max**
- **Driver Thermal Shutdown Protection**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

SN75177B . . . D OR P PACKAGE
(TOP VIEW)



SN75178B . . . P PACKAGE
(TOP VIEW)



THE SN75177B IS NOT RECOMMENDED FOR NEW DESIGN

description

The SN75177B and SN75178B differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177B and SN75178B are identical except for the complementary enable inputs, which allow the devices to be used in pairs for bidirectional communication.

The SN75177B and SN75178B feature positive- and negative-current limiting 3-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –7 V to 12 V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The driver is designed to drive current loads up to 60 mA maximum.

The SN75177B and SN75178B are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176B bus transceiver.

Function Tables

SN75177B

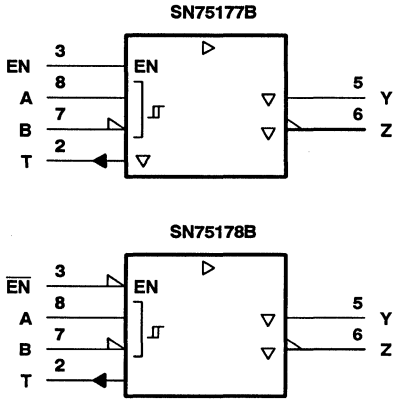
DIFFERENTIAL INPUTS	ENABLE	OUTPUTS		
A – B	EN	T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq 0.2$ V	H	L	L	H
X	L	Z	Z	Z

SN75178B

DIFFERENTIAL INPUTS	ENABLE	OUTPUTS		
A – B	$\overline{EN}$	T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq 0.2$ V	L	L	L	H
X	H	Z	Z	Z

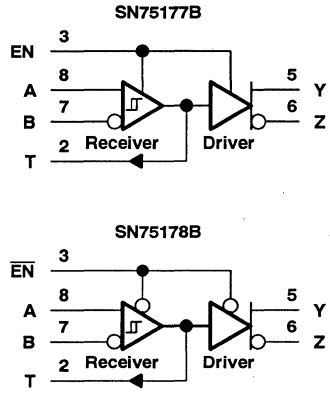
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = impedance (off)

logic symbols†

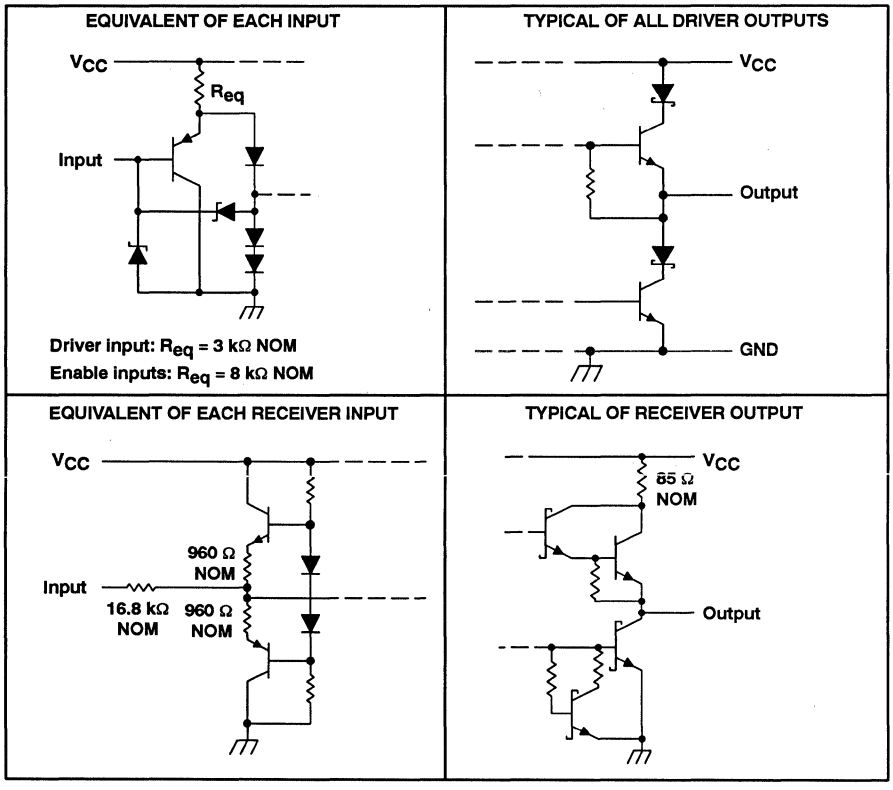


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Differential input voltage (see Note 2) ..... ±25 V
Enable input voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	EN or $\overline{EN}$	2			V
low-level input voltage, V_{IL}	EN or $\overline{EN}$			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2 V_{OD1} or 2§			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 3		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of diferential output voltage‡	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	$V_{CC} = 0$,	$V_O = -7$ V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	μA
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = V_{CC}$				250	
		$V_O = 12$ V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2, whichever is greater.
NOTE 3: See Figure 3.5 of EIA Standard RS-485.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	$R_L = 54\ \Omega$,	See Figure 3		15	20	ns
t_{tD}	Differential-output transition time				20	30	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination) Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{OS}\|$	$\|V_{OS}\|$
$\Delta\|V_{OC}\|$	$\|V_{OS} - \overline{V}_{OS}\|$	$\|V_{OS} - \overline{V}_{OS}\|$
I_{OS}	$\|I_{sa}\|$,$\|I_{sb}\|$	
I_O	$\|I_{xa}\|$,$\|I_{xb}\|$	I_{ia},I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Input clamp voltage at EN	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				20	μA
						−400	
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−200	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		57	70	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: Refer to EIA Standard RS-422 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 6		19	35	ns
t_{PHL}	Propagation delay time, high-to-low level output			30	40	
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 7		10	20	ns
t_{PZL}	Output enable time to high level			12	20	
t_{PHZ}	Output disable time from high level	C_L = 15 pF, See Figure 8		25	35	ns
t_{PLZ}	Output disable time from low level			17	25	

PARAMETER MEASUREMENT INFORMATION

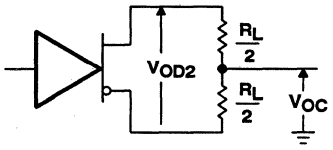


Figure 1. Driver V_{OD} and V_{OC}

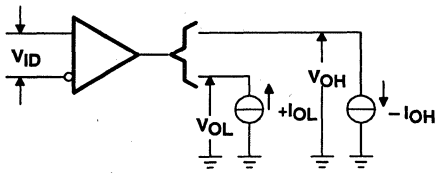


Figure 2. Receiver V_{OH} and V_{OL}

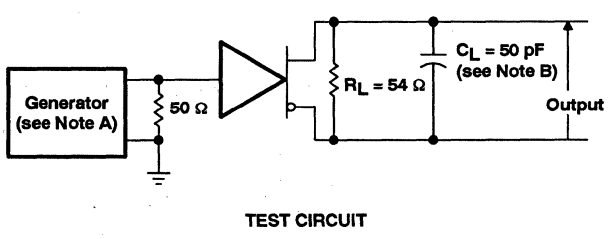


Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms

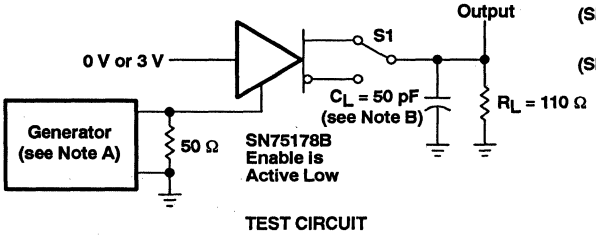


Figure 4. Driver Enable and Disable Times

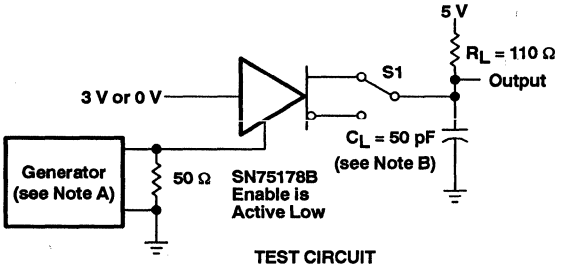


Figure 5. Driver Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

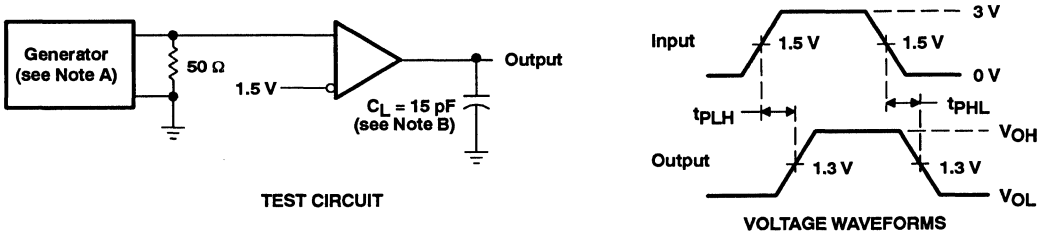


Figure 6. Receiver Propagation Delay Times

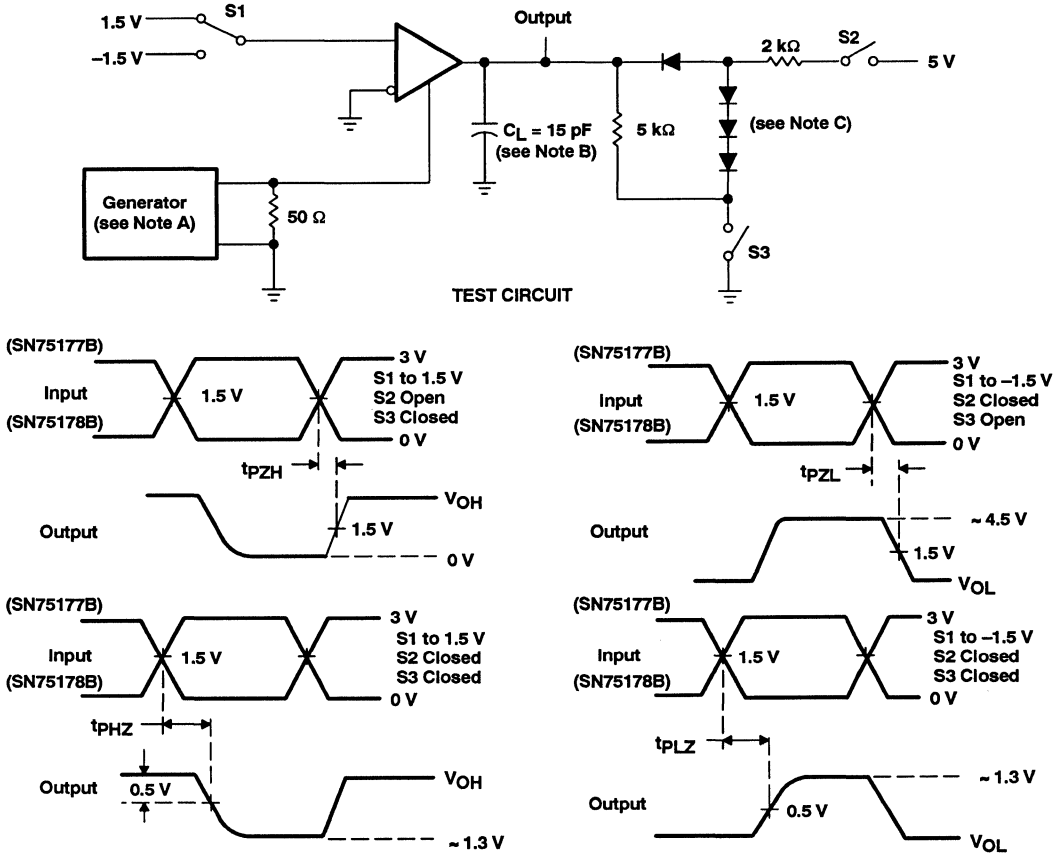


Figure 7. Receiver Output Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

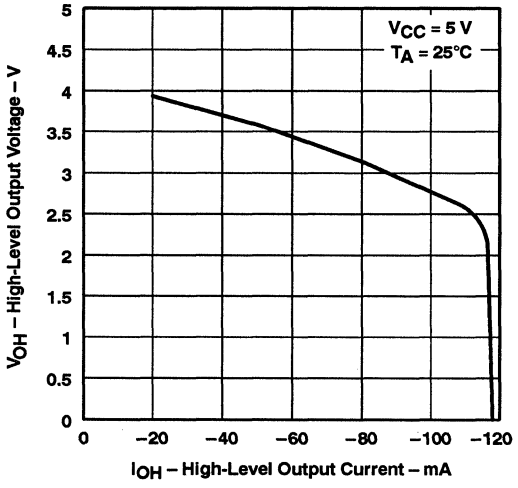


Figure 8

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

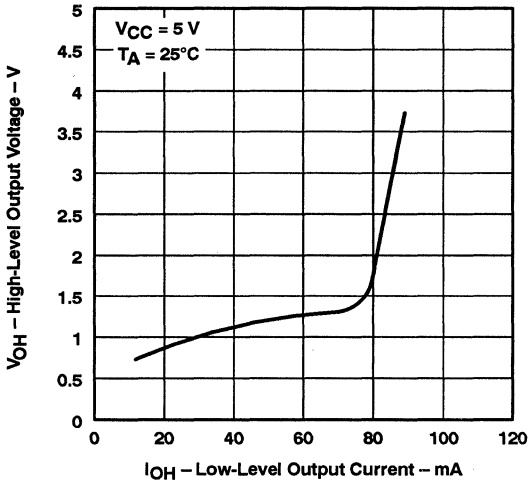


Figure 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

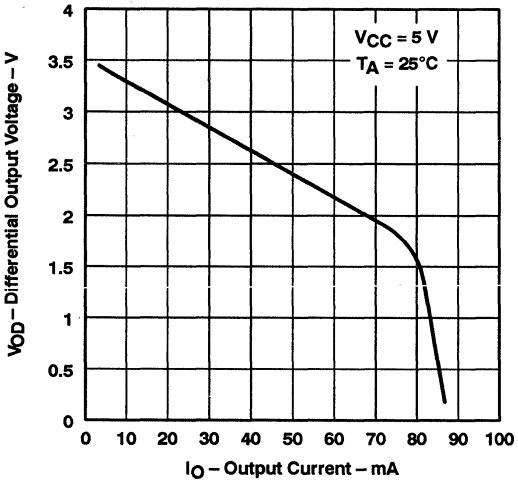


Figure 10

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

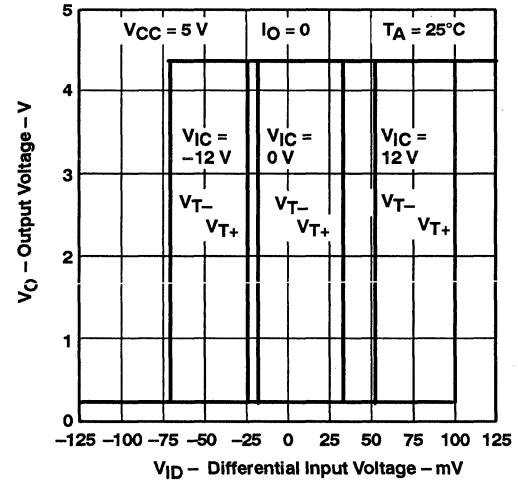


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

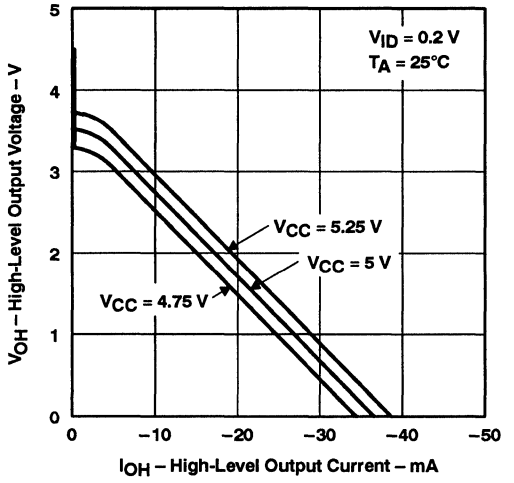


Figure 12

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

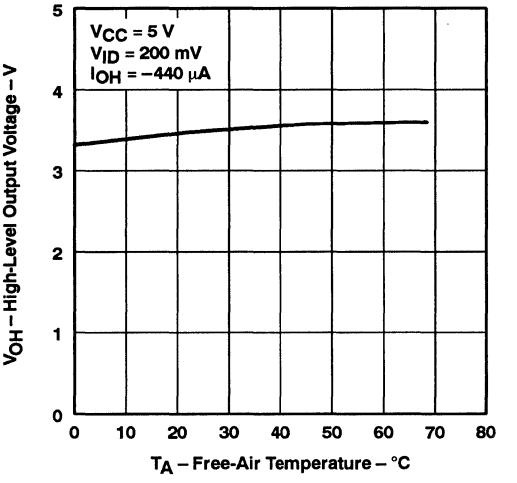


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

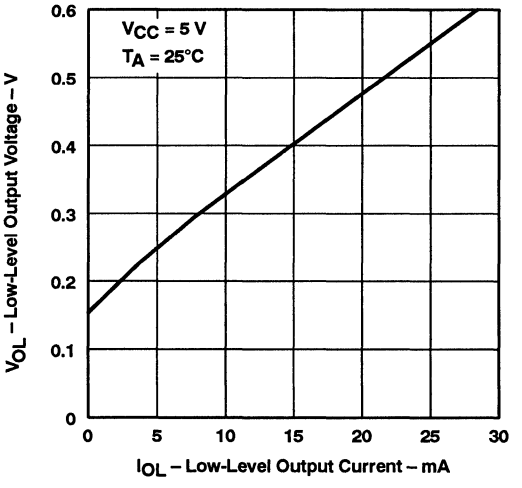


Figure 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

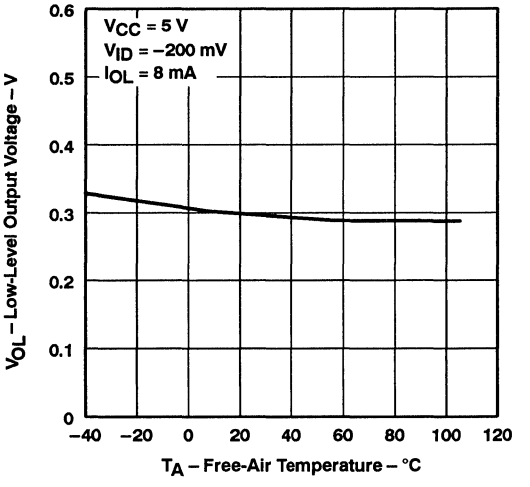
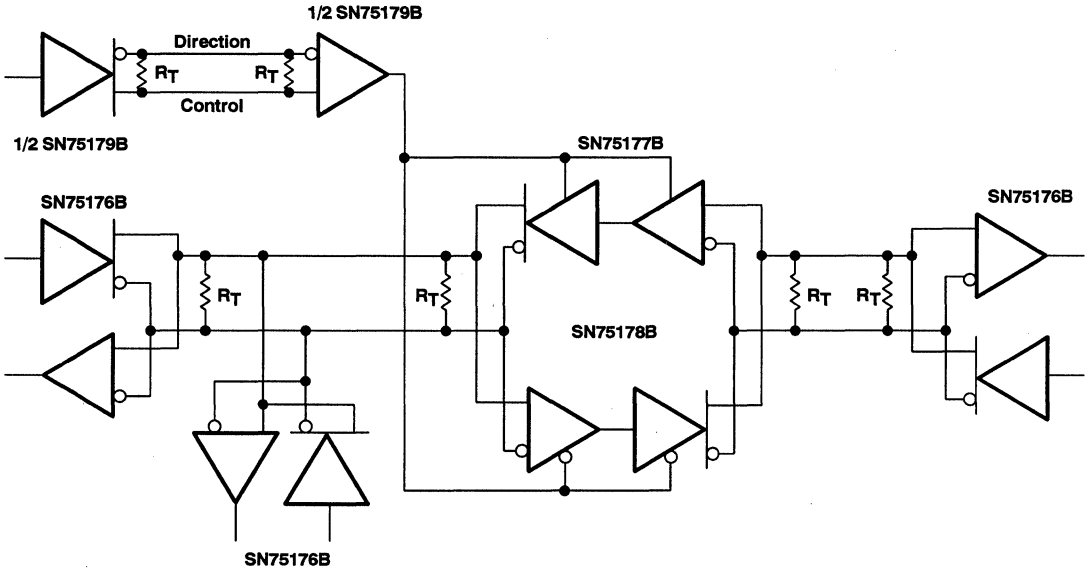


Figure 15

APPLICATION INFORMATION



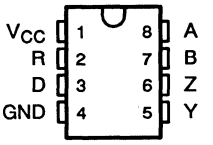
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

SLLS123B – D2845, JUNE 1984 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422A, RS423A, and CCITT Recommendations V.11 and X.27**
- **Bus Voltage Range . . . –7 V to 12 V**
- **Positive and Negative Current Limiting**
- **Driver Output Capability . . . 60 mA Max**
- **Driver Thermal Shutdown Protection**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

D OR P PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGN

description

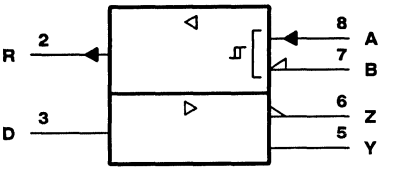
The SN75179A driver and bus receiver circuit is a monolithic integrated device designed for balanced transmission line applications, and meets EIA Standards RS-422A, RS-423A, and CCITT Recommendations V.11 and X.27. It is designed to improve the performance of data communications over long bus lines.

The SN75179A features positive- and negative-current limiting for the driver and receiver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

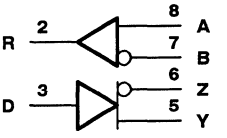
The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The device is designed to drive current loads of up to 60 mA maximum.

The SN75179A is characterized for operation from 0°C to 70°C.

logic symbol



logic diagram



Function Tables

DRIVER

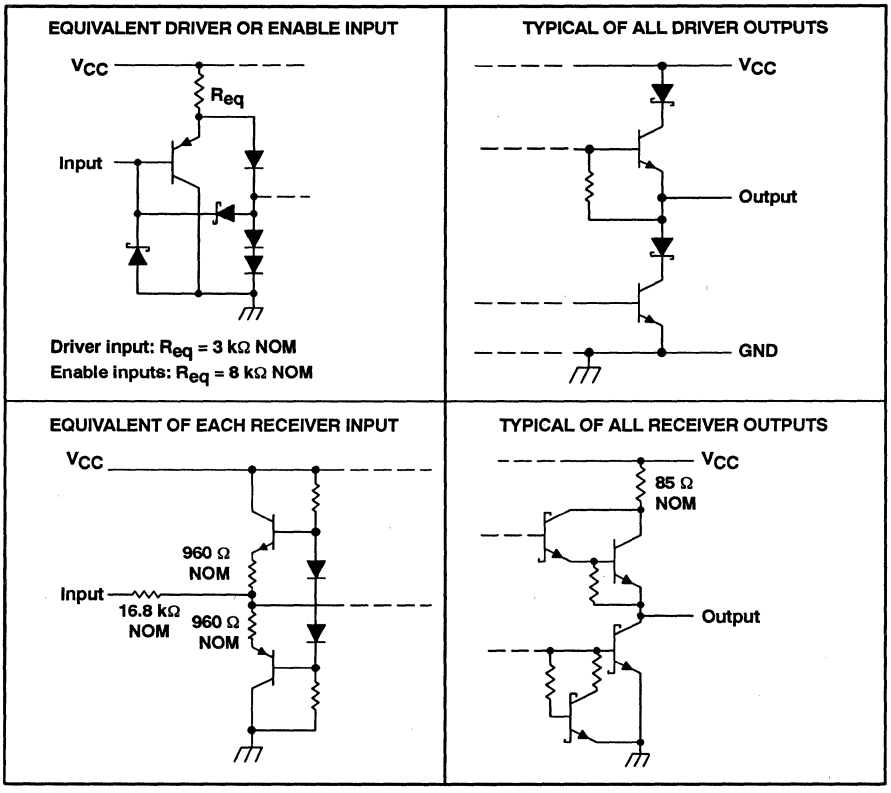
INPUT D	OUTPUTS Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

H = high level, L = low level, ? = indeterminate

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Differential input voltage (see Note 2) ..... ±25 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OH} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				2 V_{OD2}	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 13	2	2.7		V
		R_L = 54 Ω,	See Figure 13	1.5	2.4		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 13			±0.2	V
V_{OC}	Common-mode output voltage¶					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	µA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load				50	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

¶ In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 60 Ω, See Figure 3		40	60	ns
t_{tD}	Differential-output transition time			65	95	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	See Figure 9				50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 2			0.45	V
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 12 V				1	mA
			V_I = −7 V				−0.8	
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				−15		−85	mA
I_{CC}	Supply current (total package)	No load					50	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 3: Refer to EIA Standard RS-422A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 5		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			27	35	ns

PARAMETER MEASUREMENT INFORMATION

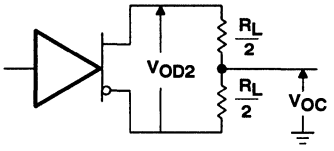


Figure 1. Driver V_{OD} and V_{OC}

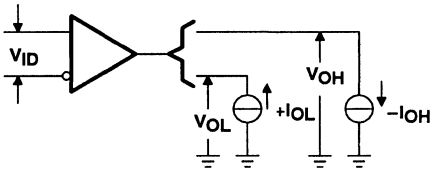
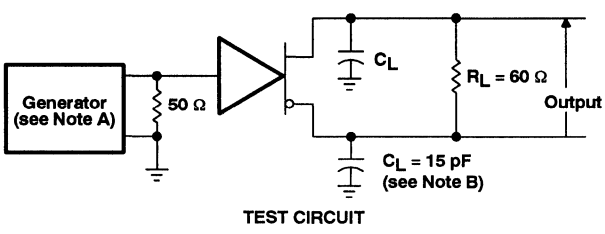


Figure 2. Receiver V_{OH} and V_{OL}



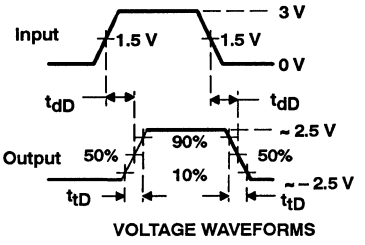
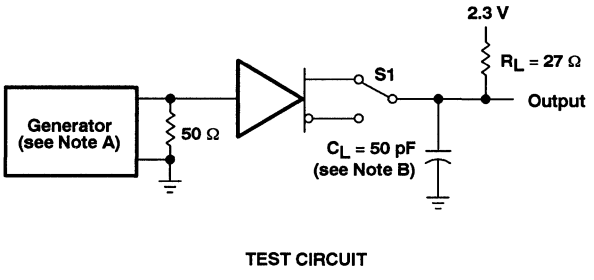


Figure 3. Driver Differential-Output Delay and Transition Times



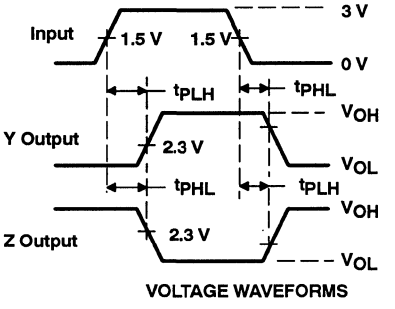
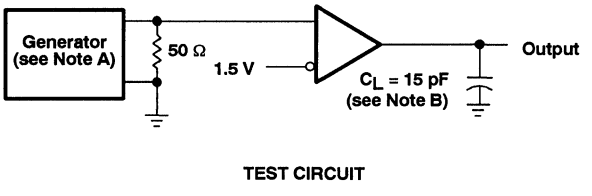


Figure 4. Driver Test Circuit and Voltage Waveforms



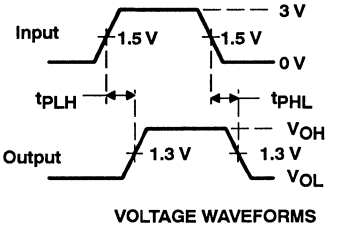


Figure 5. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs DRIVER HIGH-LEVEL OUTPUT CURRENT

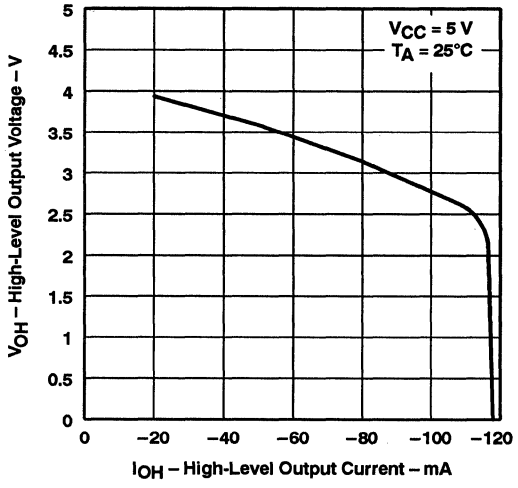


Figure 6

DRIVER LOW-LEVEL OUTPUT VOLTAGE vs DRIVER LOW-LEVEL OUTPUT CURRENT

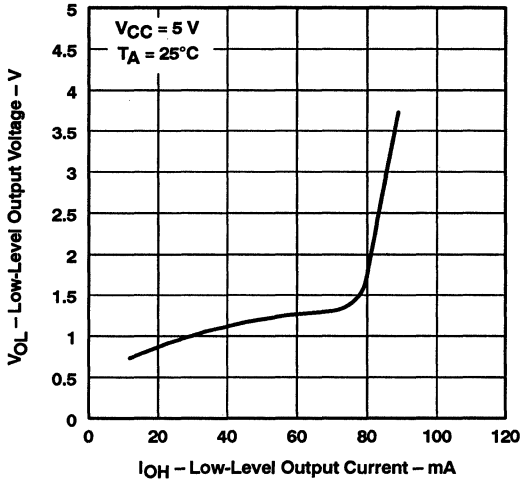


Figure 7

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs DRIVER OUTPUT CURRENT

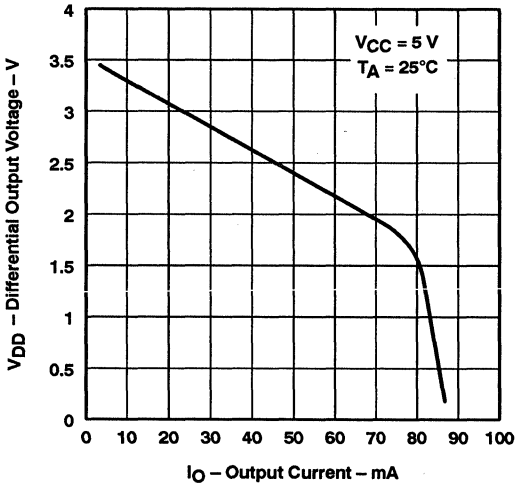


Figure 8

RECEIVER OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

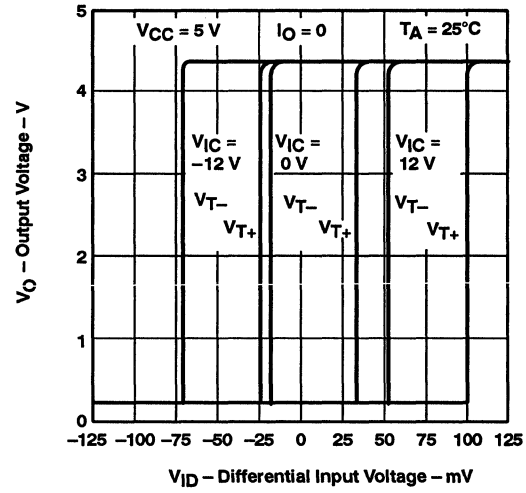


Figure 9

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

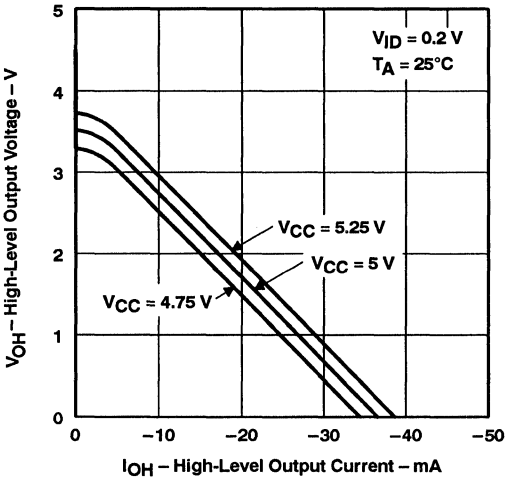


Figure 10

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

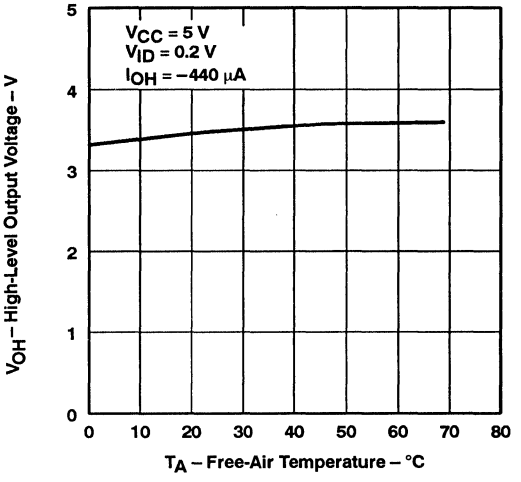


Figure 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

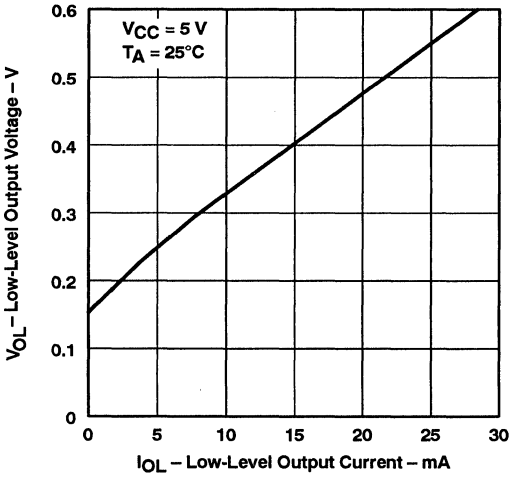


Figure 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

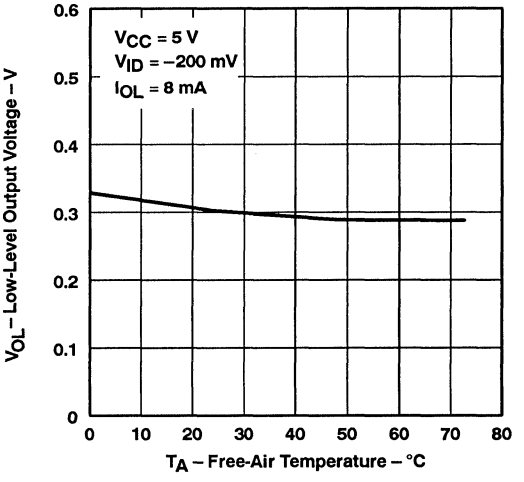


Figure 13

- **Meets EIA Standards RS-422-A, RS-485 and CCITT Recommendations V.11 and X.27**
- **Bus Voltage Range . . . –7 V to 12 V**
- **Positive and Negative Current Limiting**
- **Driver Output Capability . . . 60 mA Max**
- **Driver Thermal Shutdown Protection**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

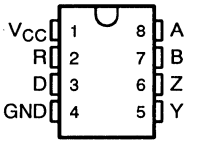
description

The SN65179B and SN75179B differential driver and receiver pair are monolithic integrated devices designed for balanced transmission line applications and meet EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. They are designed to improve the performance of full-duplex data communications over long bus lines.

The SN65179B and SN75179B driver outputs provide limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –7 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The SN65179B and SN75179B are designed to drive current loads of up to 60 mA maximum.

The SN65179B is characterized for operation from –40°C to 85°C. The SN75179B is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

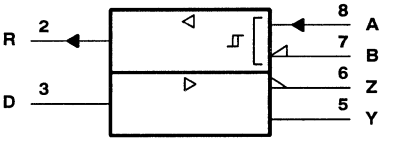
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

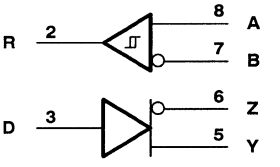
H = high level, L = low level,
? = indeterminate

logic symbol†

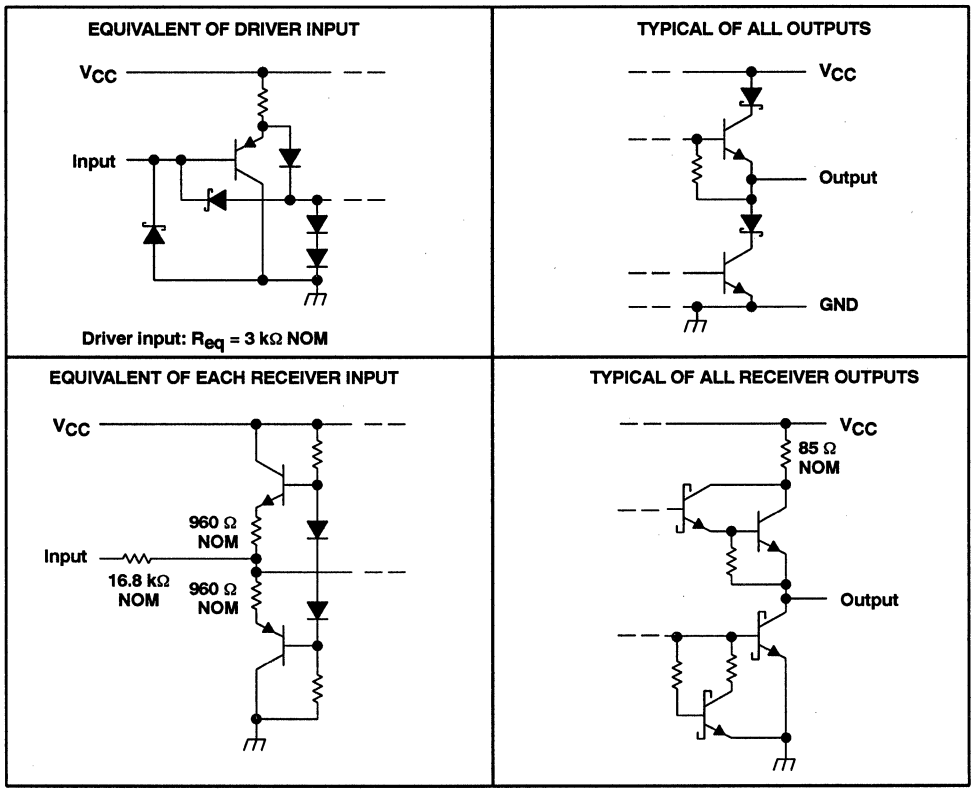


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Differential input voltage (see Note 2) ..... ±25 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65179B ..... −40°C to 85°C
SN75179B ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	TA ≤ 25°C POWER RATING	DERATING FACTOR	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65179B	−40		85	°C
	SN75179B	0		70	

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Low-level output voltage	R_L = 100 Ω,	See Figure 1	1/2V_{OD1} or 2¶			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See Note 3		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC} or 12 V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

¶ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.

NOTE 3: See EIA Standard RS-485, Figure 3.5, Test Termination Measurement 2.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
t_{tD}	Differential-output transition time				20	30	ns

Symbol Equivalents

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\|-\|\overline{V}_t\|\|$	$\|\|V_t\|-\|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os}-\overline{V}_{os}\|$	$\|V_{os}-\overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 2			0.45	V
I_I	Line input current	Other input at 0 V,	See Note 4	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				−15		−85	mA
I_{CC}	Supply current (total package)	No load				57	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: Refer to EIA Standard RS-422A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 4		30	40	ns

PARAMETER MEASUREMENT INFORMATION

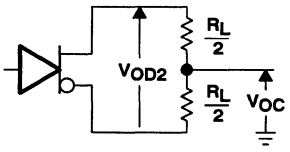


Figure 1. Driver V_{DD} and V_{OC}

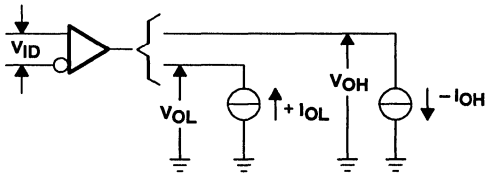


Figure 2. Receiver V_{OH} and V_{OL}

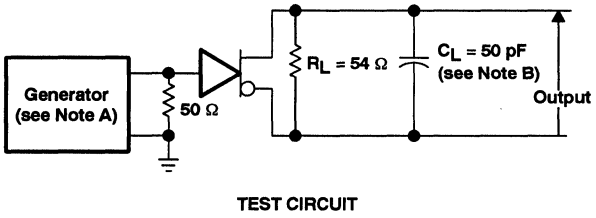


Figure 3. Driver Test Circuit and Voltage Waveforms

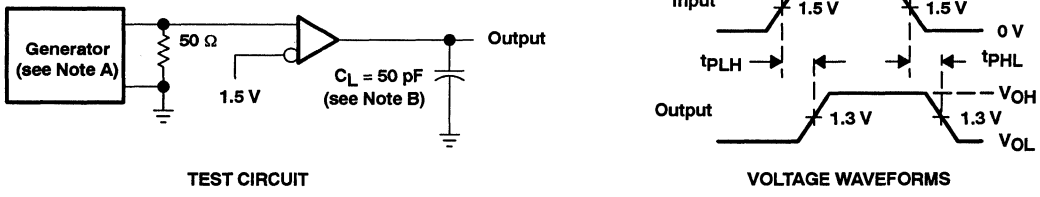


Figure 4. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

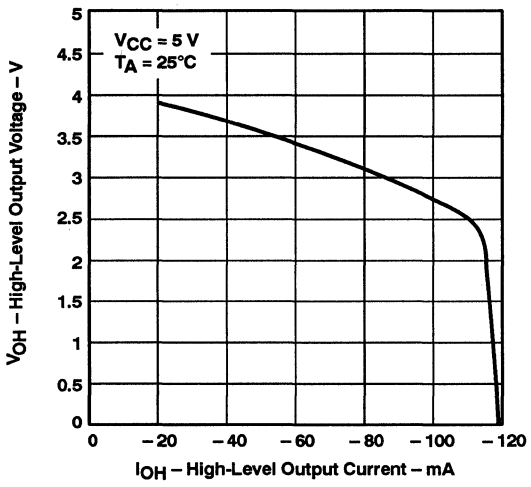


Figure 5

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

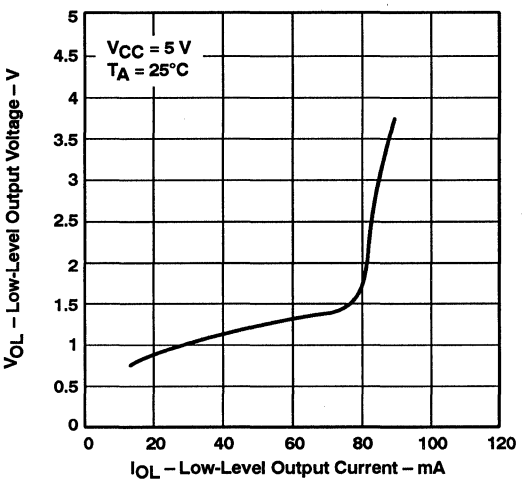


Figure 6

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

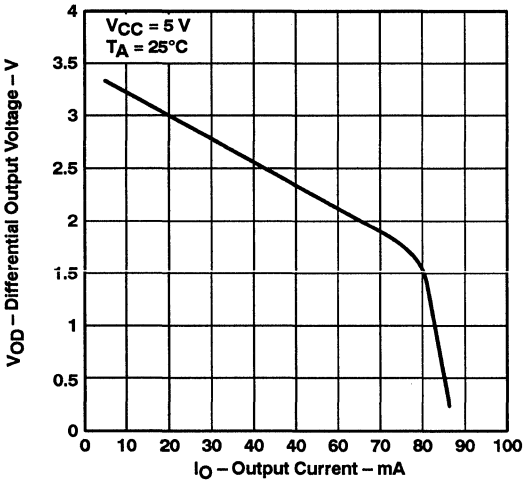


Figure 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

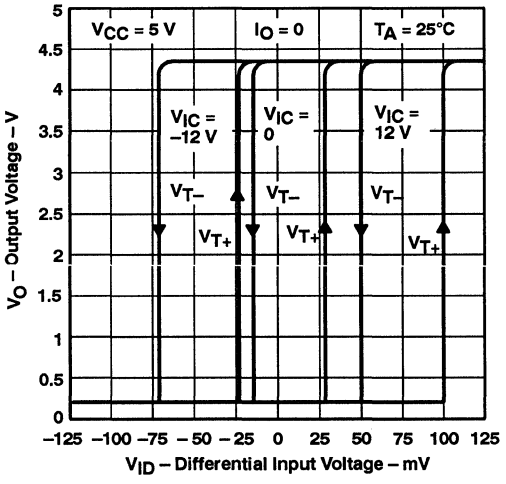


Figure 8

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

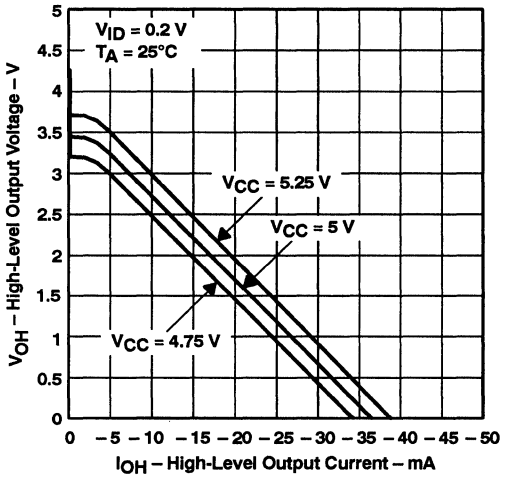


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

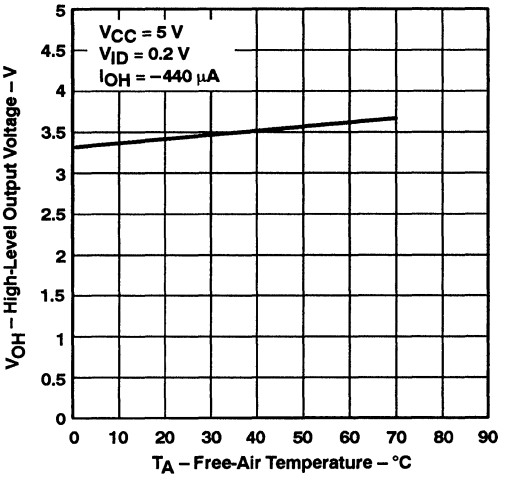


Figure 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

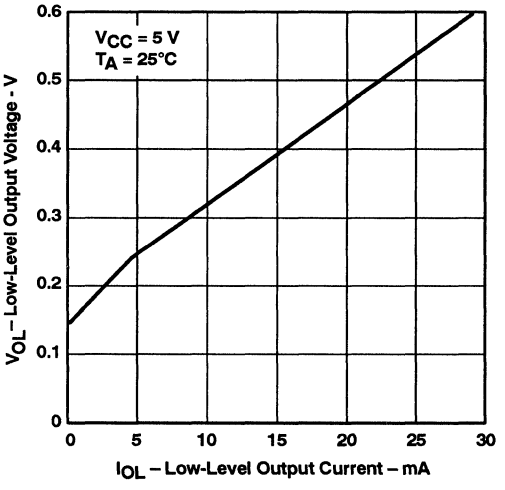


Figure 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

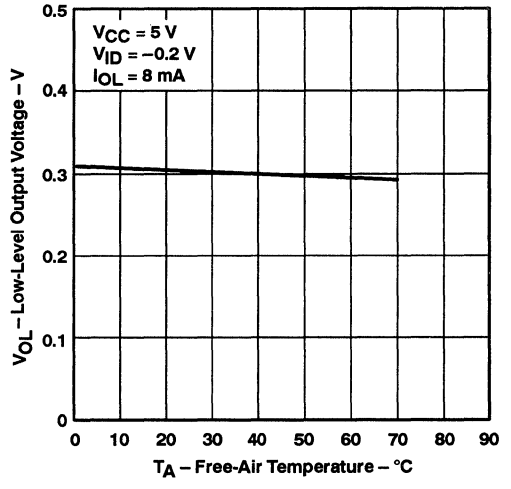


Figure 12

SLLS052C – D3043, AUGUST 1987 – REVISED FEBRUARY 1992

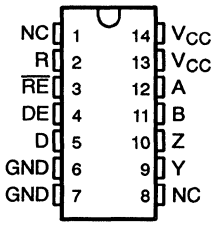
- **Meets EIA Standards RS-422A and RS-485† and CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation In Both Serial and Parallel Applications**
- **Low Skew Between Devices . . . 6 ns Max**
- **Low Supply Current Requirements 30 mA Max**
- **Individual Driver and Receiver I/O Pins With Dual V_{CC} and Dual GND**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

description

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver

D OR N PACKAGE
(TOP VIEW)



NC–No internal connection

Function Tables

DRIVER

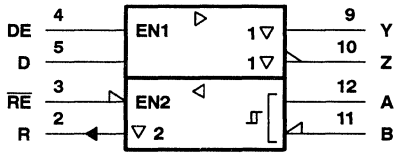
INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

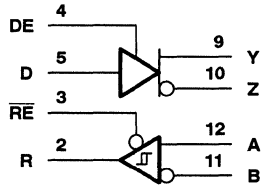
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



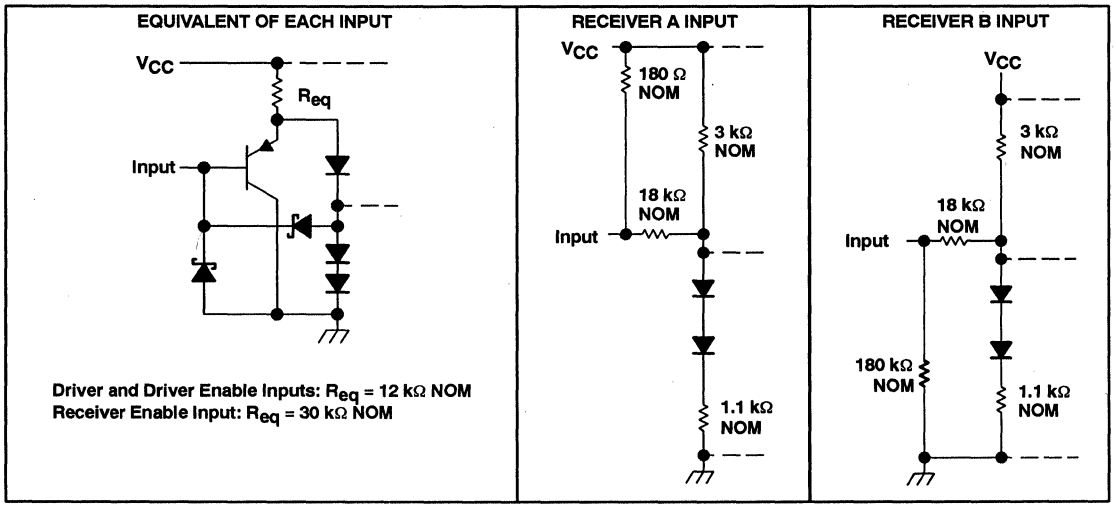
† These devices meet or exceed the requirements of EIA RS485 except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4.5 V to 8 V for the SN65ALS180.

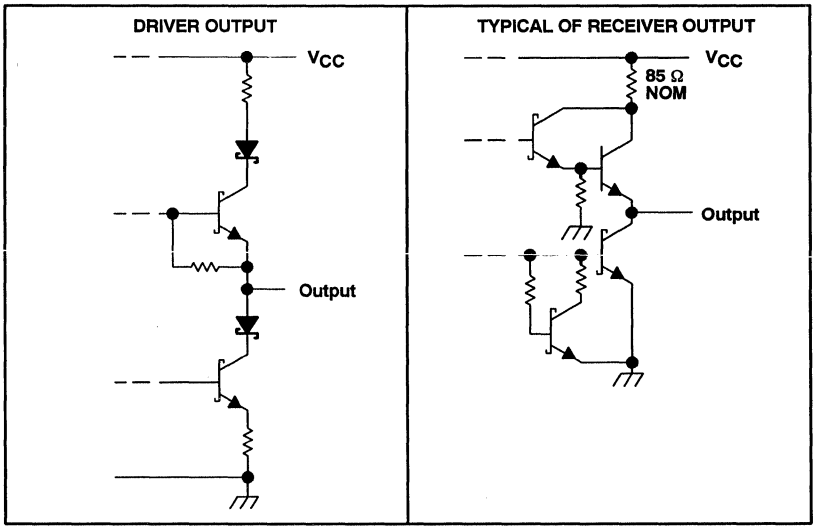
description (continued)

differential inputs are connected to separate pins for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from −40°C to 85°C. The SN75ALS180 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS180 ..... −40°C to 85°C
SN75ALS180 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12 −7	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS180	−40		85	°C
	SN75ALS180	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A/Y with respect to the inverting terminal B/Z.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2V_{OD1} or 2§			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current#	$V_O = -6$ V	SN75ALS180			−250	mA
		$V_O = -4$ V	SN65ALS180				
		$V_O = 0$	All			−150	
		$V_O = V_{CC}$	All				
		$V_O = 8$ V	All				
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
§ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
# Duration of the short circuit does not exceed one second for this test.
NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{dD}	Differential output delay time	$R_L = 54\ \Omega$, $C_L = 50$ pF, See Figure 3	3	8	13	ns
	Pulse skew ($\lvert t_{dDH} - t_{dDL} \rvert$)			1	6	ns
t_{tD}	Differential output transition time		3	8	13	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$, See Figure 5		19	24	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$, See Figure 4		8	13	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$, See Figure 5		8	13	ns

‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert VOD2 \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert VOD3 \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 7	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	19	ns
	Skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level				20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

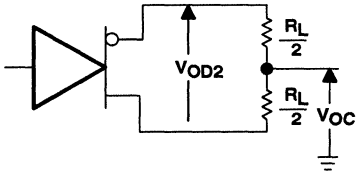


Figure 1. Driver V_{OD} and V_{OC}

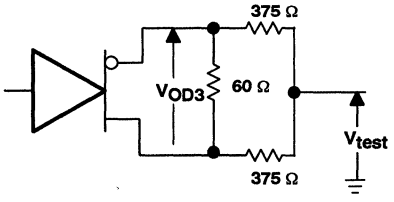
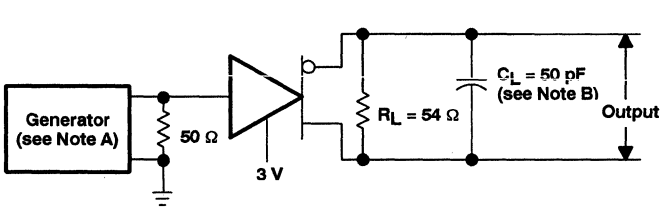
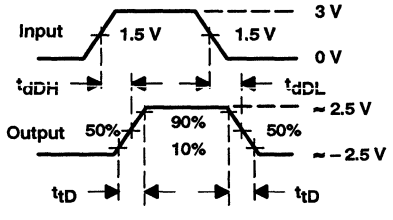


Figure 2. Driver V_{OD3}



TEST CIRCUIT

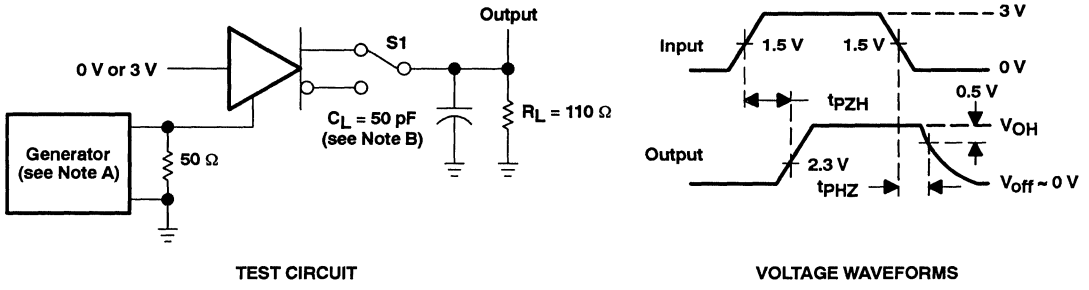


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

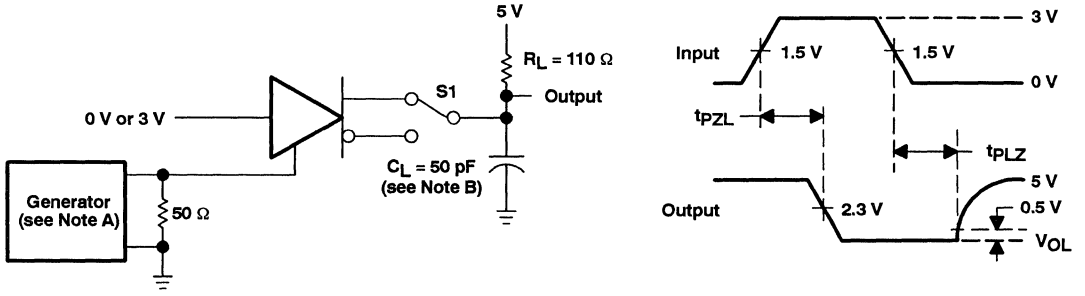
Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

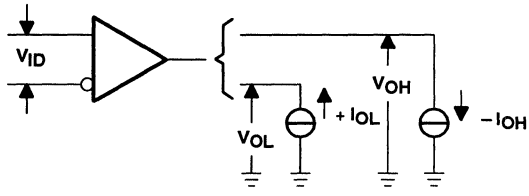


Figure 6. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

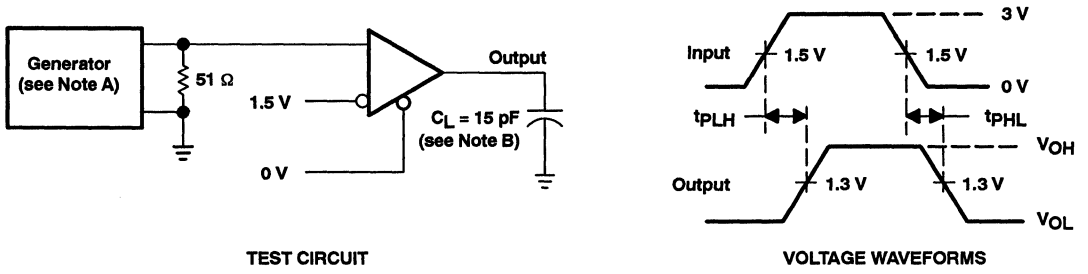


Figure 7. Receiver Test Circuit and Voltage Waveforms

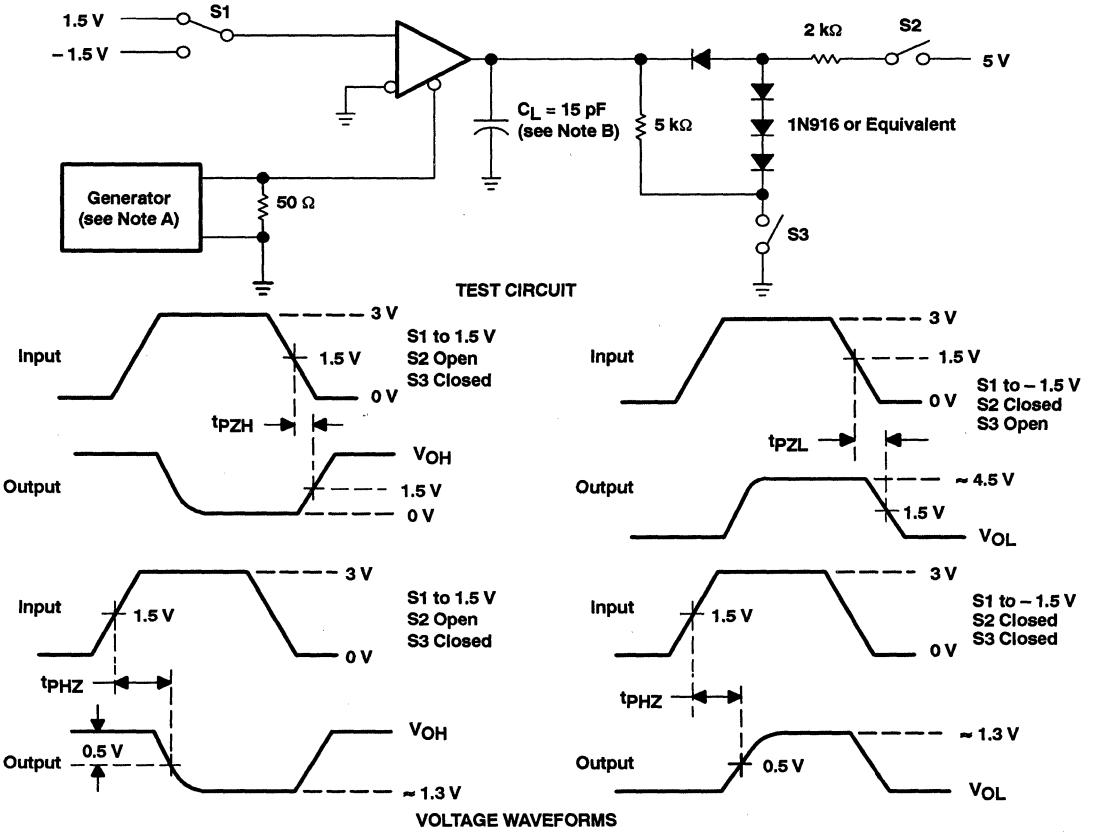


Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

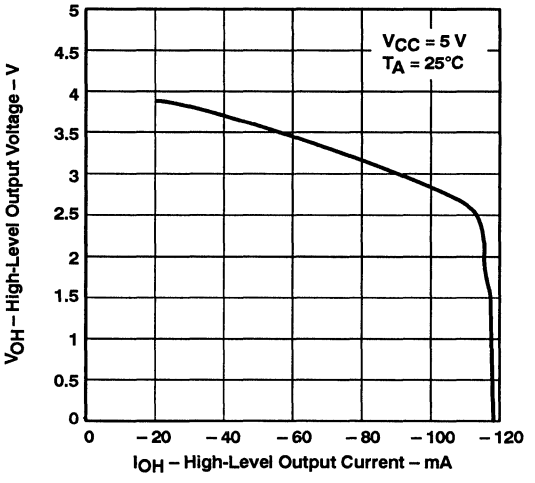


Figure 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

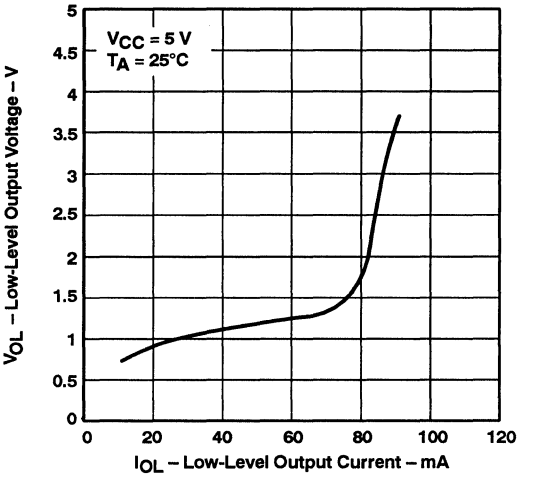


Figure 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

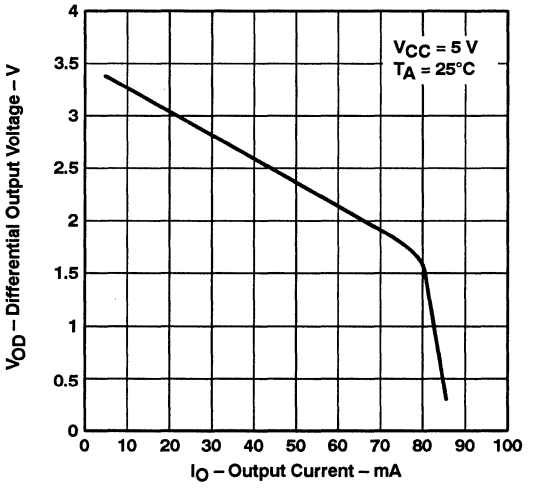


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

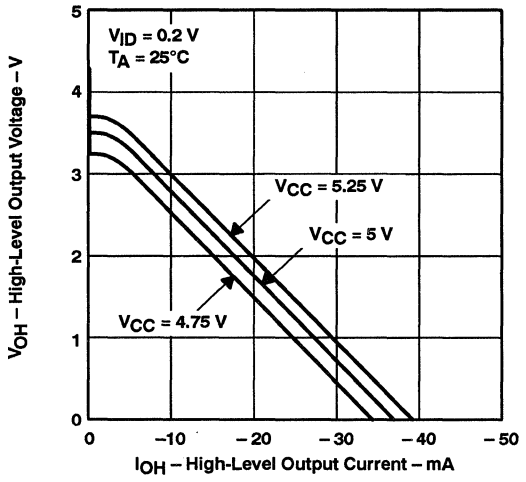


Figure 12

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

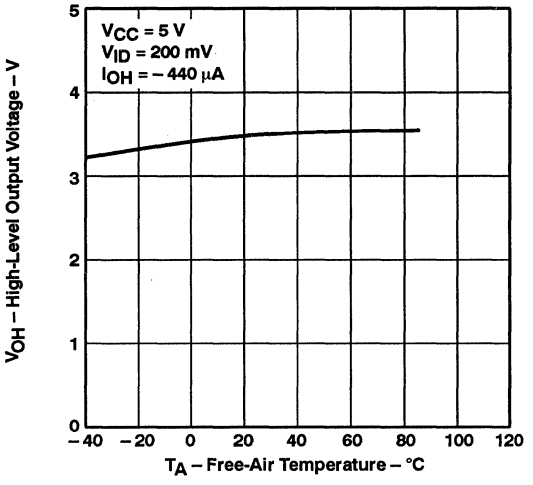


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

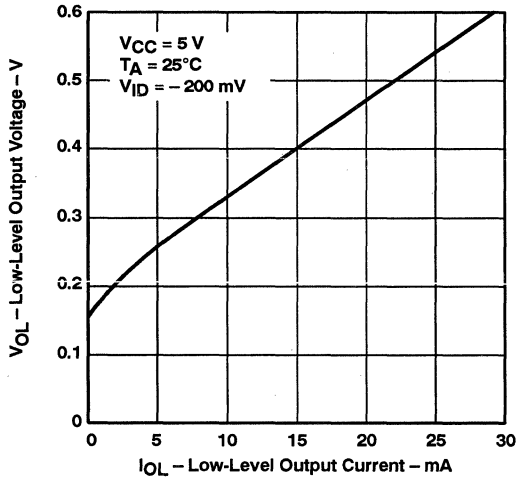


Figure 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

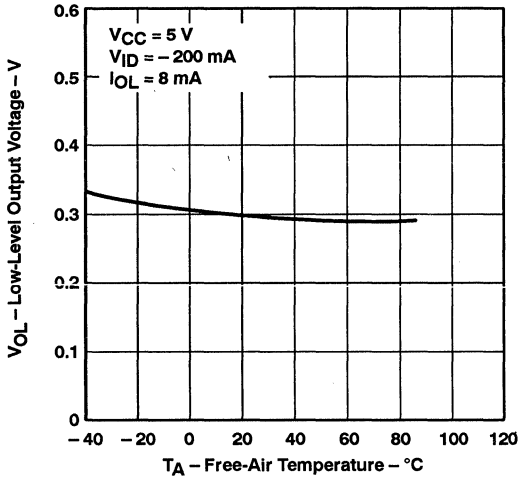


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

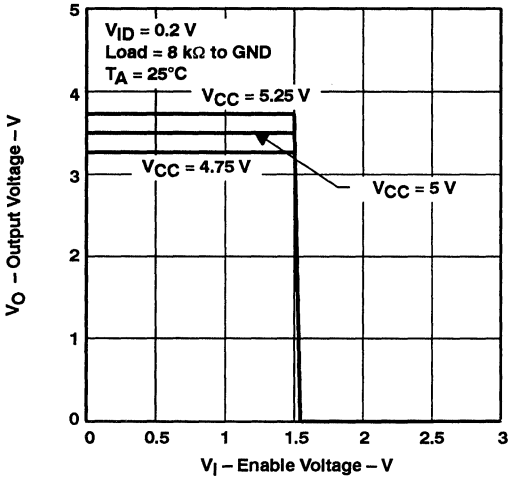


Figure 16

RECEIVER OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

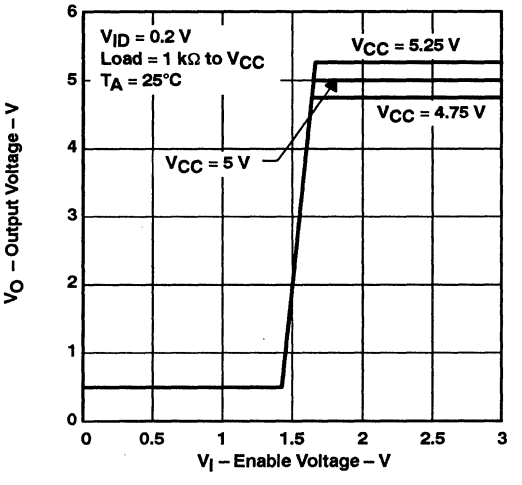
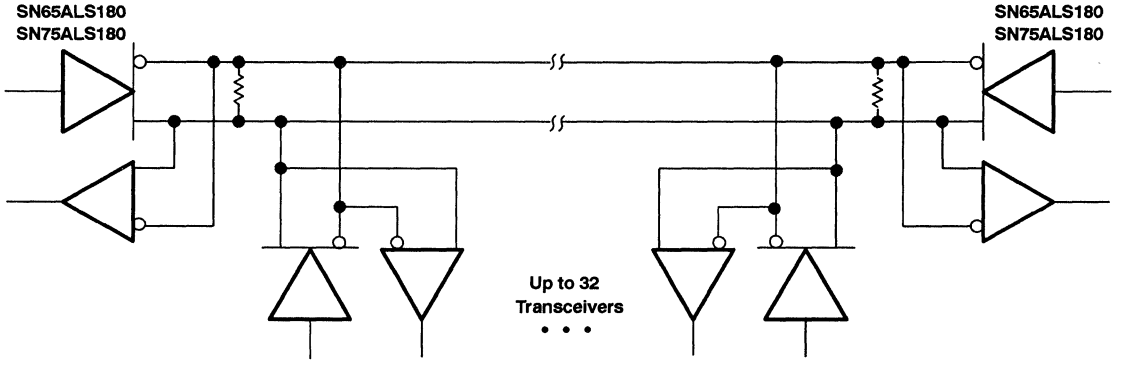


Figure 17

APPLICATION INFORMATION

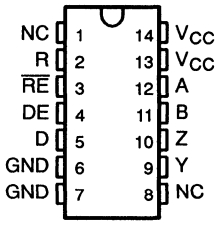


NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

- **Meets EIA Standards RS-422-A, RS-485, and CCITT Recommendations V.11 and X.27**
- **Low Supply Current Requirements 30 mA Max**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Common-Mode Output Voltage Range of −7 V to 12 V**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Receiver Common-Mode Input Voltage Range of ±12 V**
- **Operates From Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

N OR NS† PACKAGE
(TOP VIEW)



NC – No internal connection

† The NS package is only available in left-end taped and reeled (order device SN75ALS181NSLE).

description

The SN75ALS181 differential driver and receiver pair are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. The design provides for balanced transmission lines and meets EIA Standards RS-422-A and RS-485, and CCITT recommendations V.10, V.11, X.26, and X.27.

The SN75ALS181 combines a 3-state differential line driver and a differential input line receiver that operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage changes making the device suitable for party-line applications.

The SN75ALS181 is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

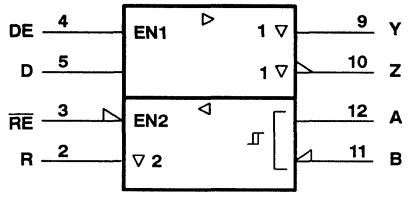
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

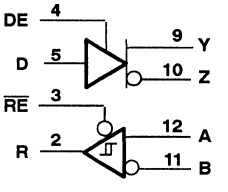
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

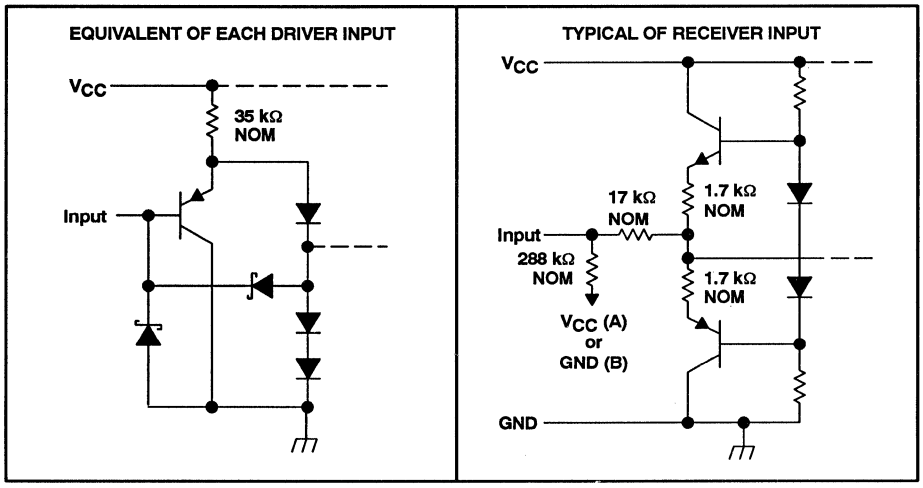


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

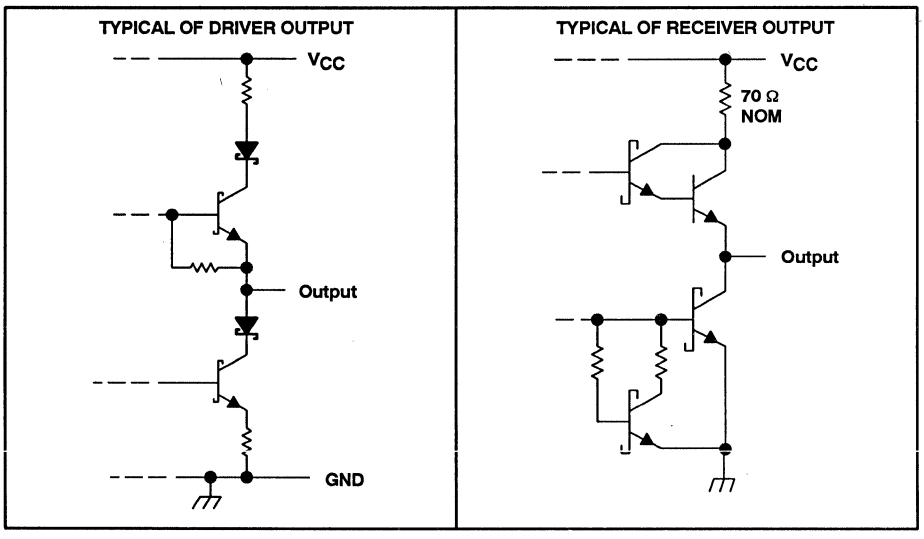
logic diagram (positive logic)



schematics of inputs



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, DE, $\overline{RE}$, and D inputs ..... 7 V
Output voltage range, driver ..... −9 V to 14 V
Input voltage range, receiver ..... −14 V to 14 V
Receiver differential input voltage range (see Note 2) ..... −14 V to 14 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	4.0 mW/°C	445 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode output voltage, V_{OC} (see Note 3)	Driver	−7		12	V
Common-mode input voltage, V_{IC} (see Note 3)	Receiver	−12		12	V
High-level input current, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input current, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 3: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this table for common-mode output voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2 V_{OD1}			V
				2			
$\|V_{OD2}\|$	Differential output voltage	R_L = 54 Ω		1.5	2.3	5	
$\|V_{OD3}\|$	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 4)	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V,	See Note 5			±100	μA
I_{IH}	High-level input current	V_{IH} = 2.4 V				20	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		$V_O = V_{CC}$				250	
		V_O = 12 V				250	
		V_O = 0 V				−150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		21	30	mA
			Outputs disabled		14	21	

NOTES: 4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5. This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential output delay time, t_{dDH} or t_{dDL}	R_L = 54 Ω,	C_L = 50 pF, See Figure 3	9	13	20	ns
$t_{sk(p)}$	Pulse skew ($\|t_{dDH} - t_{dDL}\|$)				1	8	
t_t	Differential output transition time			3	10	16	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		36	53	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		39	56	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		20	31	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		9	20	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage, differential input	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{T-}	Negative-going threshold voltage, differential input	V_O = 0.5 V,	I_O = 8 mA	See Note 8	−0.2			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = −7 V				−0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0 V		−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled			21	30	mA
			Outputs disabled			14	21	

NOTE 5: This applies for both power on and power off. Refer to EIA Standards RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (unless otherwise noted) (see Figure 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	V_{ID} = −1.5 V to 1.5 V	10	16	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V	10	16	25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)	V_{ID} = −1.5 V to 1.5 V		1	8	ns
t_{PZH}	Output enable time to high level			7	15	ns
t_{PZL}	Output enable time to low level			9	19	ns
t_{PHZ}	Output disable time from high level			18	27	ns
t_{PLZ}	Output disable time from low level			10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

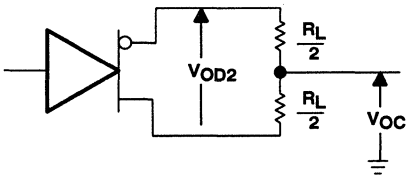


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

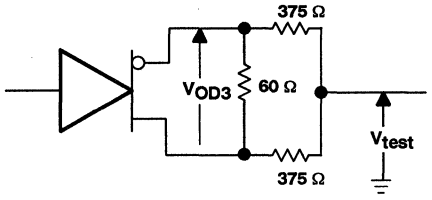
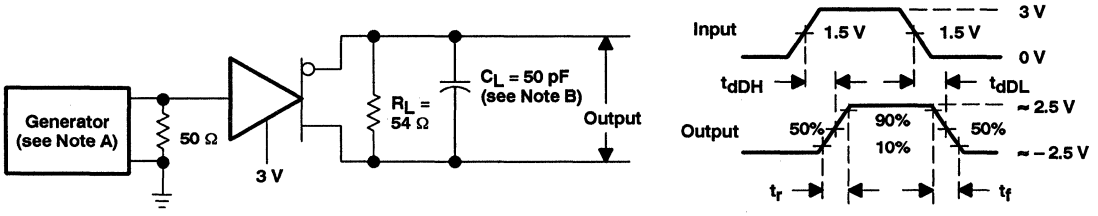


Figure 2. Driver Circuit, V_{OD3}

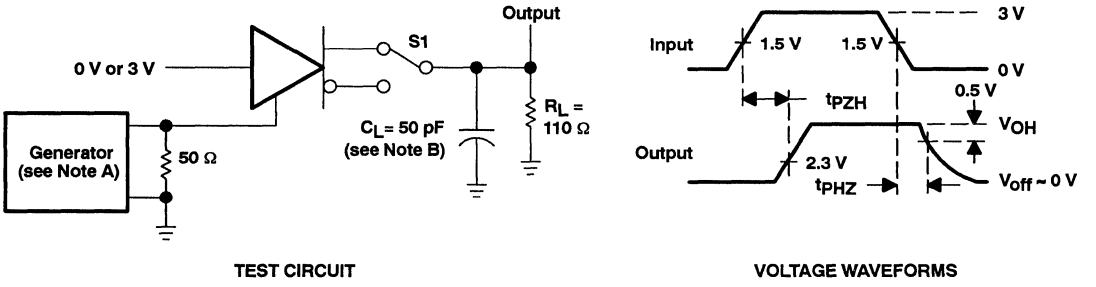


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

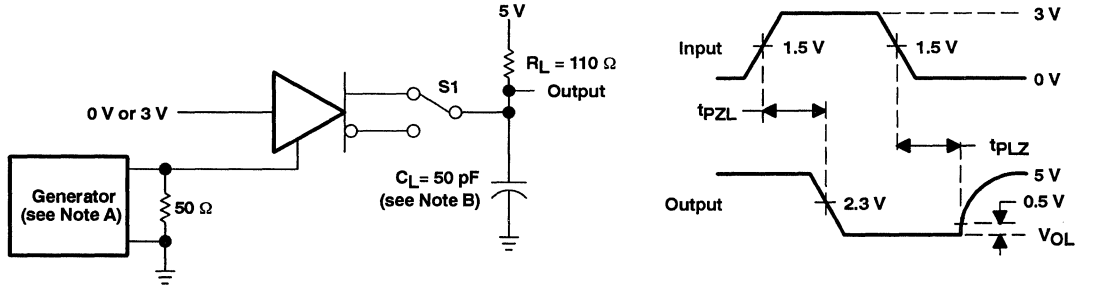
Figure 3. Driver Differential-Output Delay and Transition Times

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Enable and Disable Times



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. Driver Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f 3 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

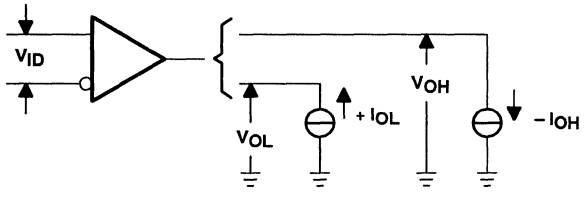


Figure 6. Receiver, V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

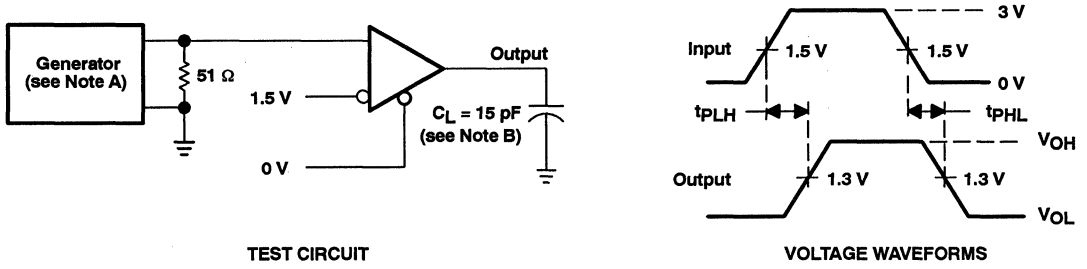


Figure 7. Receiver Propagation Delay Times

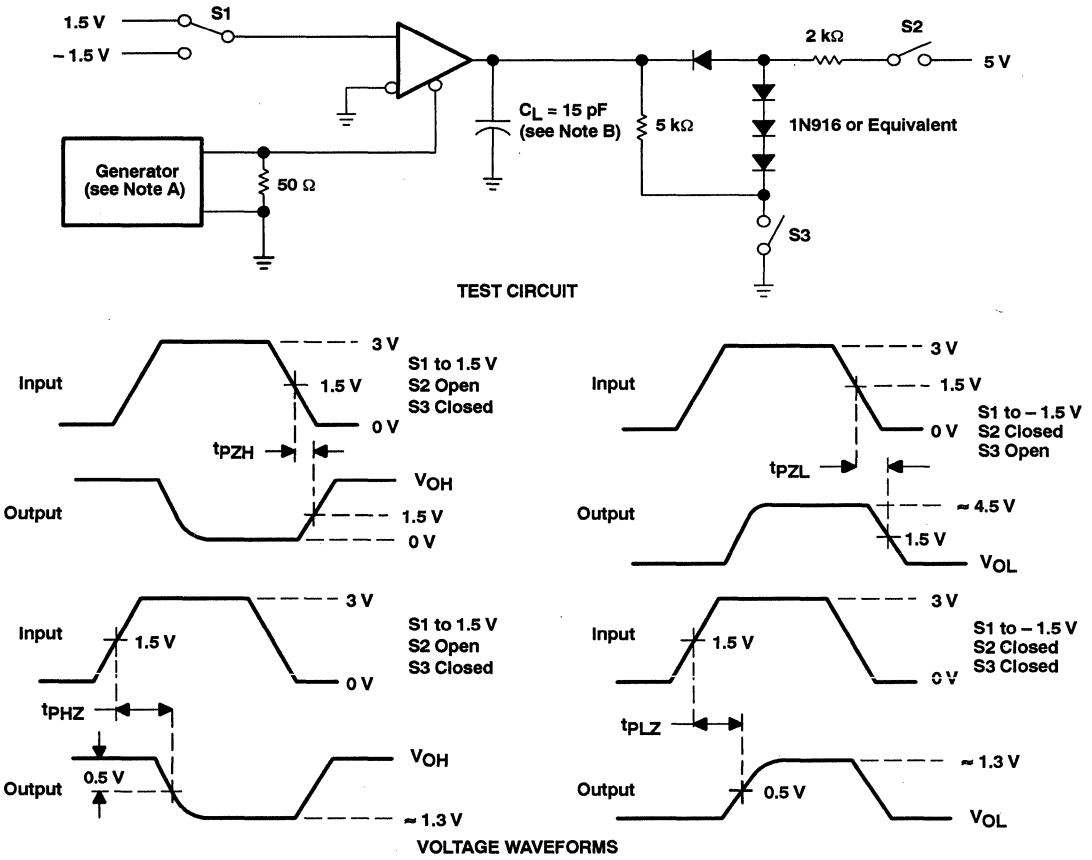


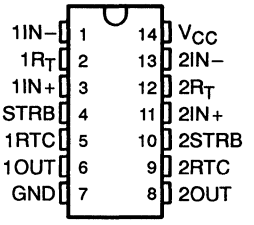
Figure 8. Receiver Output Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f 3 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

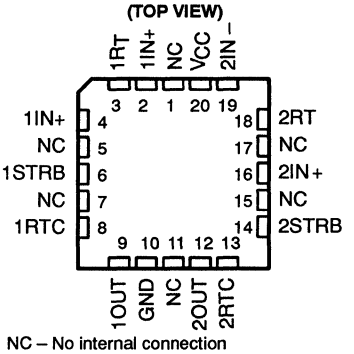
SLLS092A – D1292, OCTOBER 1972 – REVISED MARCH 1993

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **±15-V Common-Mode Input Voltage Range**
- **±15-V Differential Input Voltage Range**
- **Individual Channel Strobes**
- **Built-In Optional Line-Termination Resistor**
- **Individual Frequency Response Controls**
- **Designed for Use With Dual Differential Drivers SN55183 and SN75183**
- **Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A**

SN55182 . . . J OR W PACKAGE
DS8820A, SN75182 . . . D OR N PACKAGE
(TOP VIEW)



SN55182 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

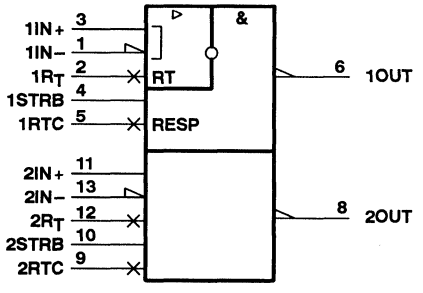
description

The DS8820A, SN55182, and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

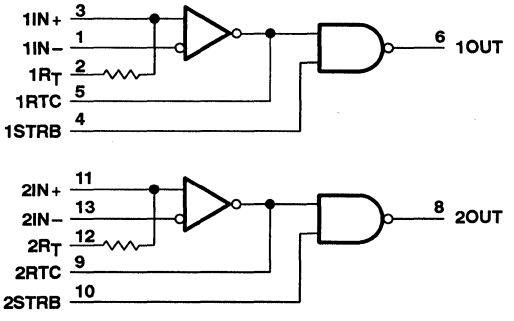
The SN55182 is characterized for operation over the full military temperature range of −55°C to 125°C. The DS8820A and SN75182 are characterized for operation from 0°C to 70°C.

logic symbol†

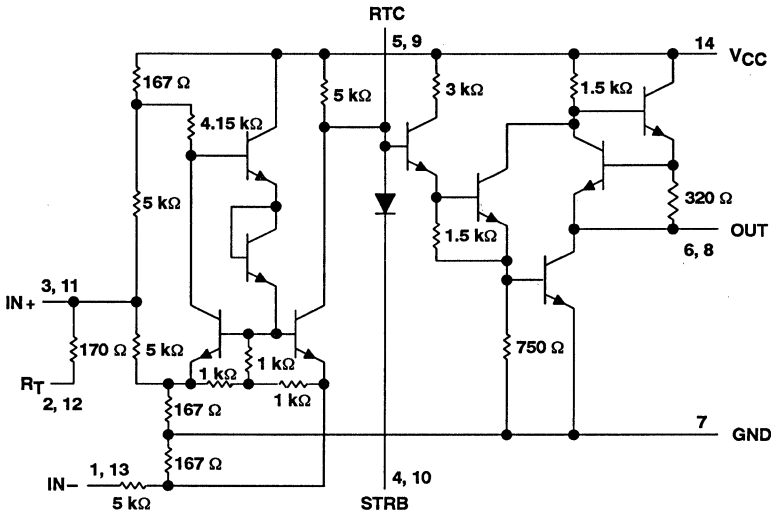


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are nominal.
Pin numbers shown are for the D, J, N, and W packages.

FUNCTION TABLE

STRB	V_{ID}	OUT
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55182	DS8820A SN75182	UNIT
Supply voltage, V_{CC1} (see Note 1)	8	8	V
Common-mode input voltage	±20	±20	V
Differential input voltage (see Note 2)	±20	±20	V
Strobe input voltage	8	8	V
Output sink current	50	50	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK, J, and W packages, SN55182 chips are alloy mounted.

recommended operating conditions

	SN55182			DS8820A, SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	V
High-level strobe input voltage, $V_{IH(STRB)}$	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, $V_{IL(STRB)}$	0		0.9	0		0.9	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

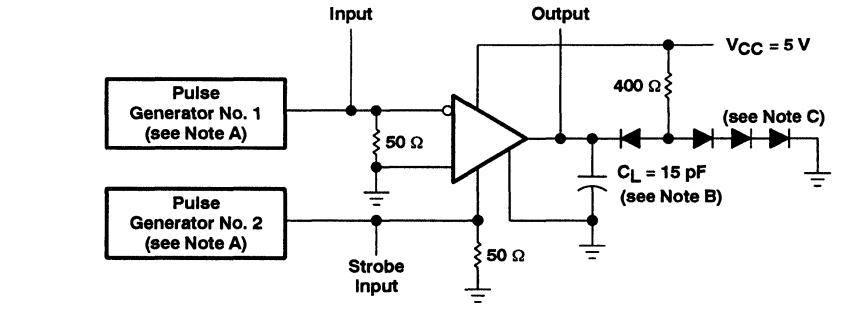
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going input threshold voltage		V_O = 2.5 V, I_{OH} = −400 μA	V_{IC} = −3 V to 3 V			0.5	V
				V_{IC} = −15 V to 15 V			1	
V_{T-}	Negative-going input threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA	V_{IC} = −3 V to 3 V			−0.5	V
				V_{IC} = −15 V to 15 V			−1	
V_{OH}	High-level output voltage		V_{ID} = 1 V, I_{OH} = −400 μA	V_{STRB} = 2.1 V,	2.5	4.2	5.5	V
			V_{ID} = −1 V, I_{OH} = −400 μA	V_{STRB} = 0.4 V,	2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = −1 V, I_{OL} = 16 mA	V_{STRB} = 2.1 V,		0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0			0	−0.5	
			V_{IC} = −15 V			−3	−4.2	
		Noninverting input	V_{IC} = 15 V			5	7	mA
			V_{IC} = 0			−1	−1.4	
			V_{IC} = −15 V			−7	−9.8	
$I_{STRB(H)}$	High-level strobe current		V_{STRB} = 5.5 V				5	μA
$I_{STRB(L)}$	Low-level strobe current		V_{STRB} = 0			−1	−1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		kΩ
R_T	Line terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	−2.8	−4.5	−6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = −1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = −0.5 V		6.8	10.2	
			V_{IC} = −15 V,	V_{ID} = −1 V		9.4	14	

† Unless otherwise noted, $V_{STRB} \geq 2.1$ V or open.
‡ All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

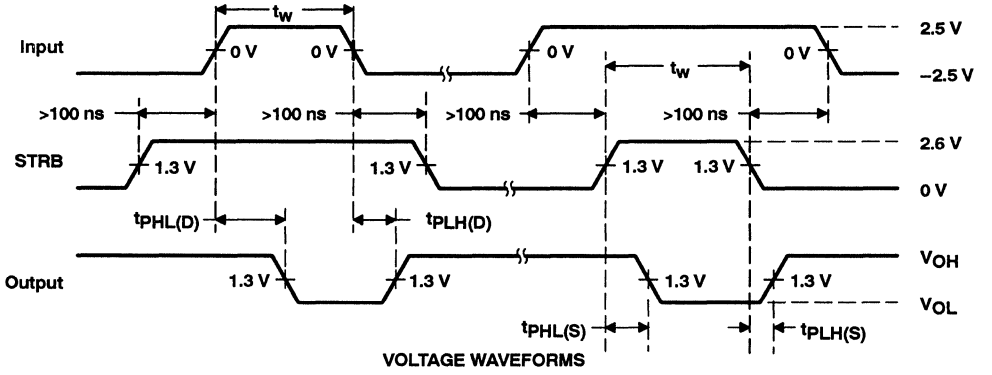
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, See Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output from differential input			31	45	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from STRB input			9	30	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from STRB input			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 0.5 \pm 0.1$ μs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

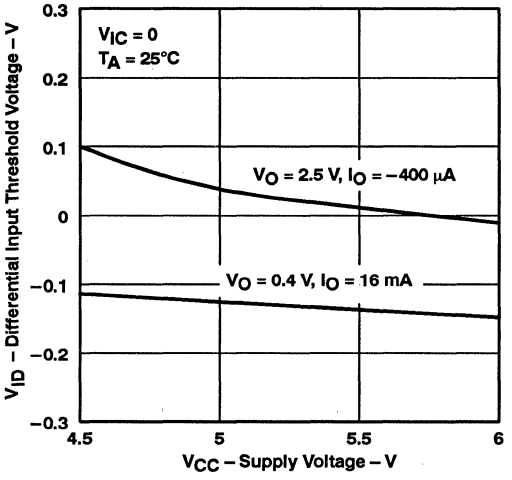


Figure 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

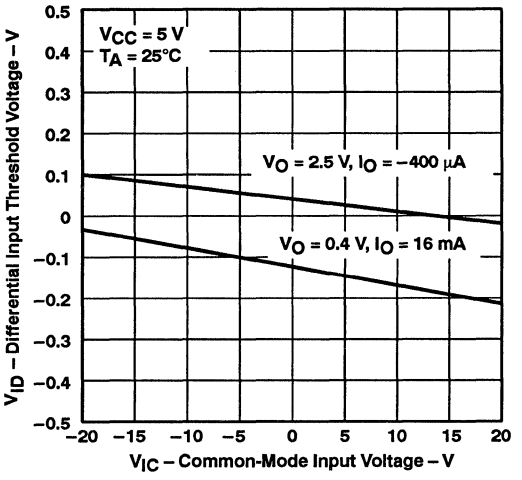


Figure 3

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

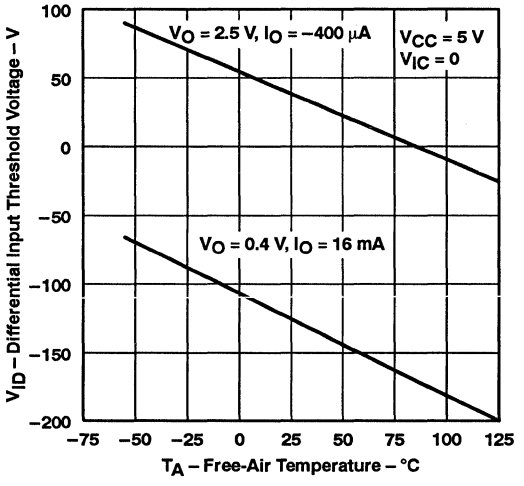


Figure 4

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

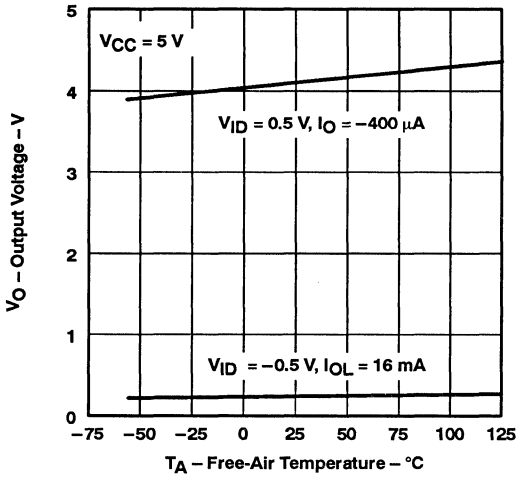


Figure 5

VOLTAGE TRANSFER CHARACTERISTICS

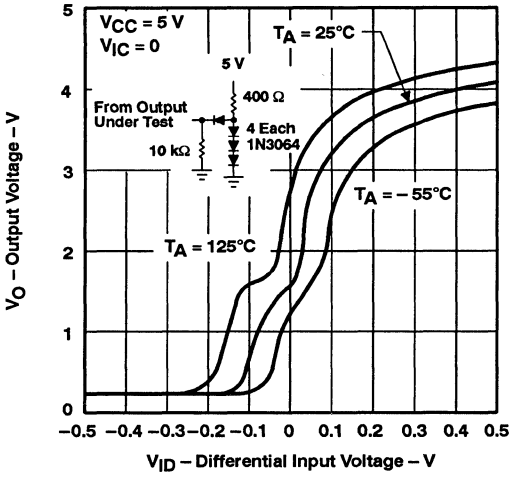


Figure 6

INPUT CURRENT
vs
INPUT VOLTAGE

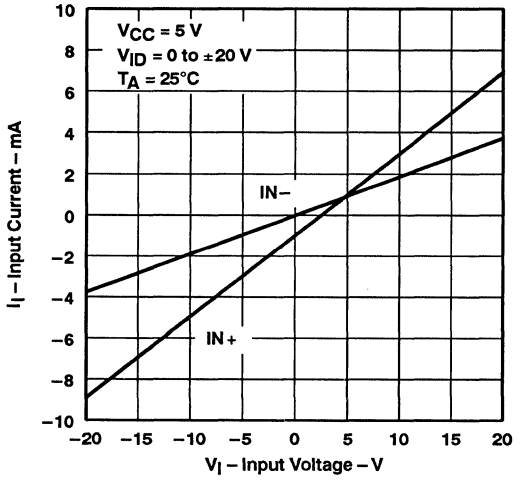


Figure 7

TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

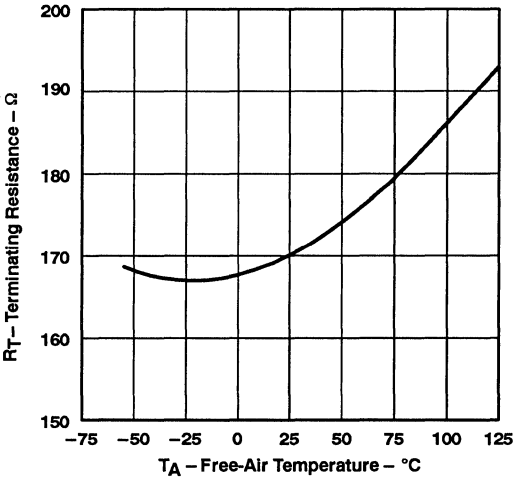


Figure 8

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

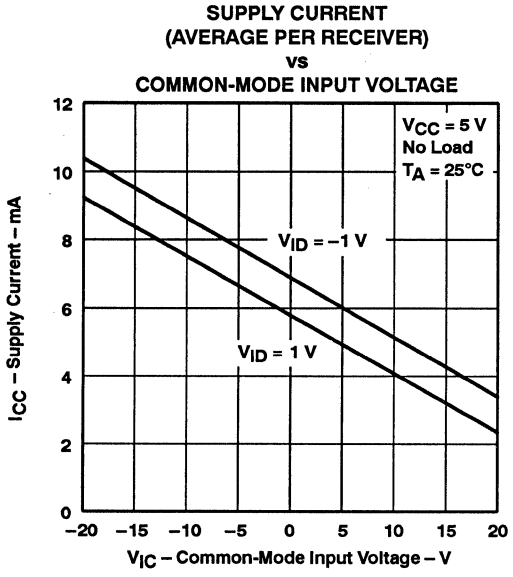


Figure 9

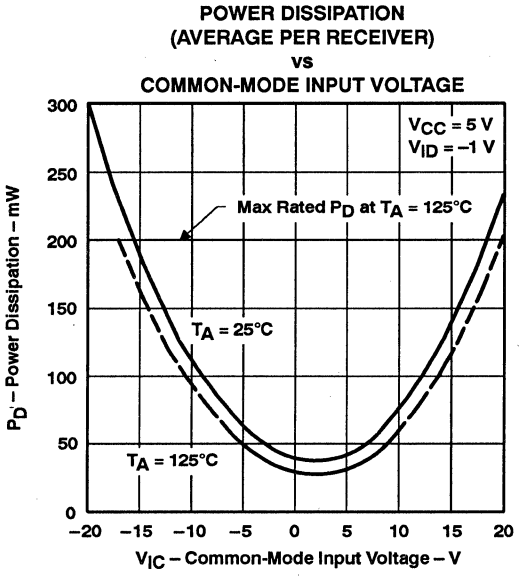
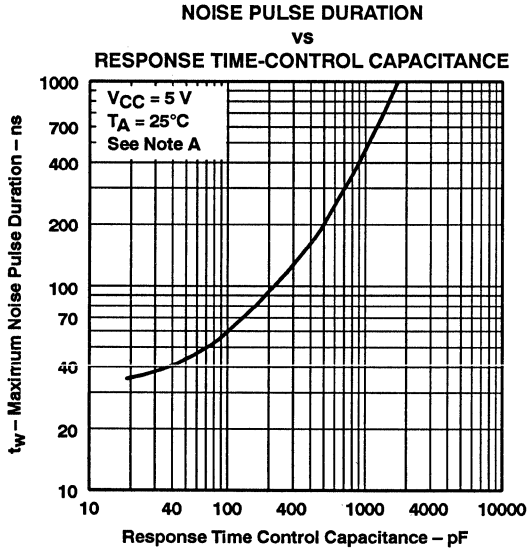
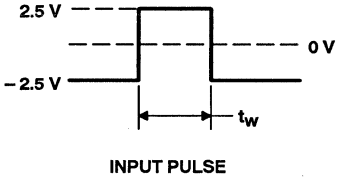


Figure 10





INPUT PULSE

NOTE A: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES FROM DIFFERENTIAL INPUT vs FREE-AIR TEMPERATURE

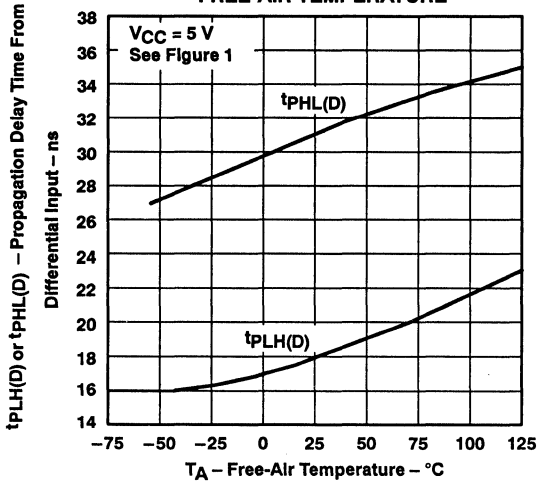


Figure 12

PROPAGATION DELAY TIMES FROM STROBE INPUT vs FREE-AIR TEMPERATURE

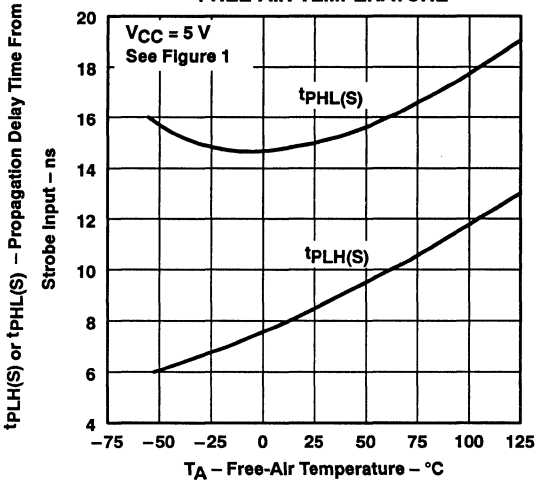
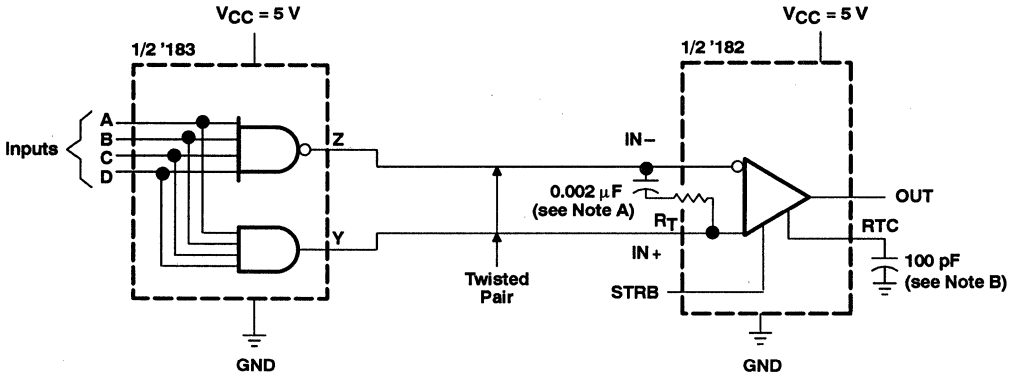


Figure 13

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\ (5 \times 10^6)\ (0.002 \times 10^{-6})}$$

$$Z_C \approx 16\ \Omega$$

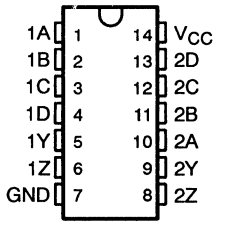
B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

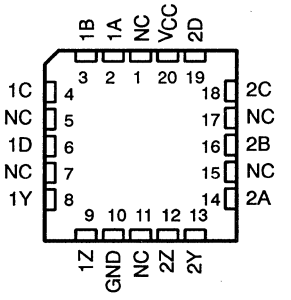
SLLS093A – D1292, OCTOBER 1972 – REVISED MARCH 1993

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **Short-Circuit Protection of Outputs**
- **Output Clamp Diodes to Terminate Line Transients**
- **High-Current Outputs**
- **Quad Inputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Designed for Use With Dual Differential Drivers SN55182 and SN75182**
- **Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830**

SN55183 . . . J OR W PACKAGE
DS8830, SN75183 . . . D OR N PACKAGE
(TOP VIEW)



SN55183 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

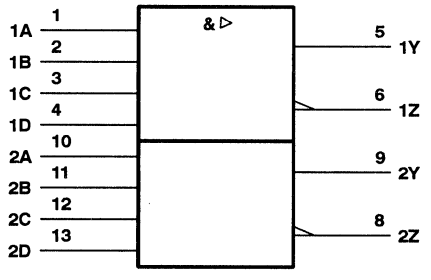
description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedances without high power dissipation. These devices may be used as TTL expander/phase splitters, as the output stages are similar to TTL totem-pole outputs.

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

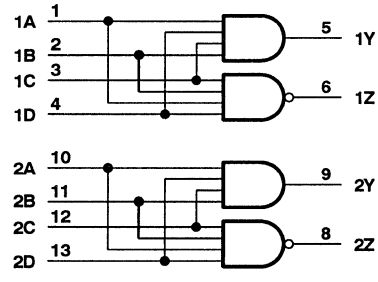
The SN55183 is characterized for operation over the full military temperature range of −55°C to 125°C. The DS8830 and SN75183 are characterized for operation from 0°C to 70°C.

logic symbol†



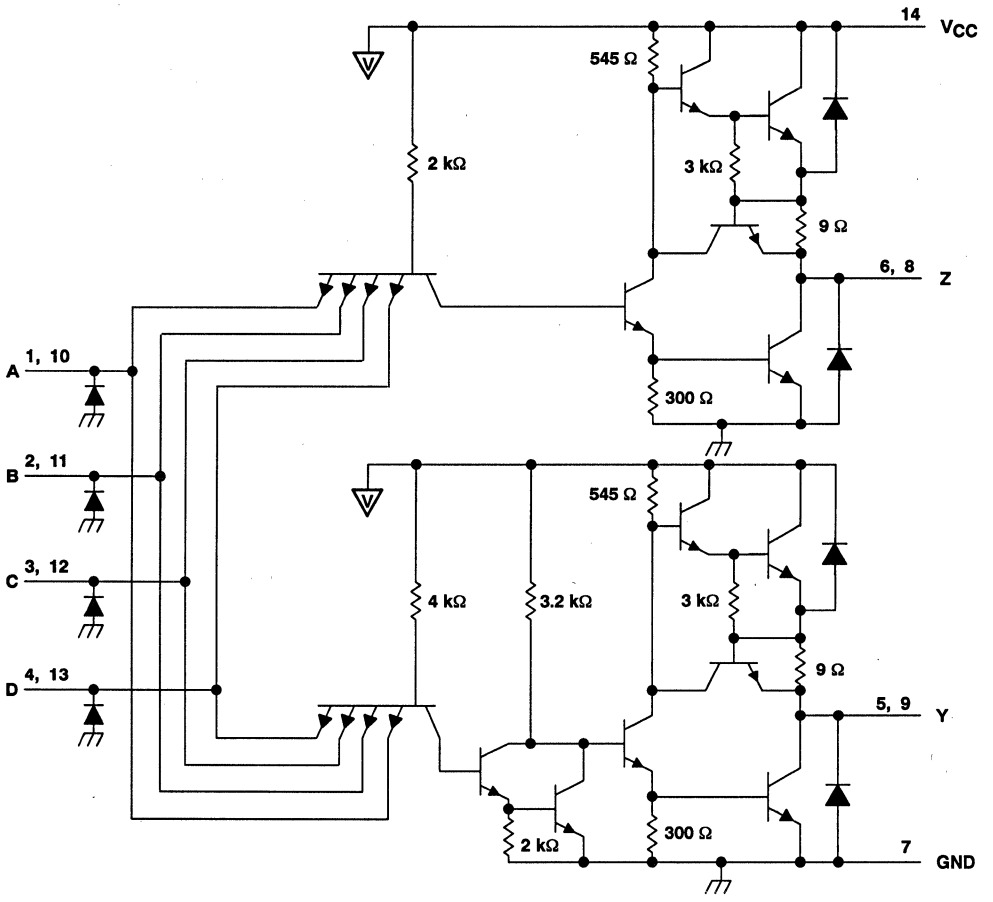
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



positive logic: $Y = ABCD$, $Z = \overline{ABCD}$

schematic (each driver)



Resistor values shown are nominal.
Pin numbers shown are for the D, N, J, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55183	DS8830 SN75183	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage	5.5	5.5	V
Duration of output short circuit (see Note 2)	1	1	s
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at a time.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK and J packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

recommended operating conditions

	SN55183			DS8830, SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

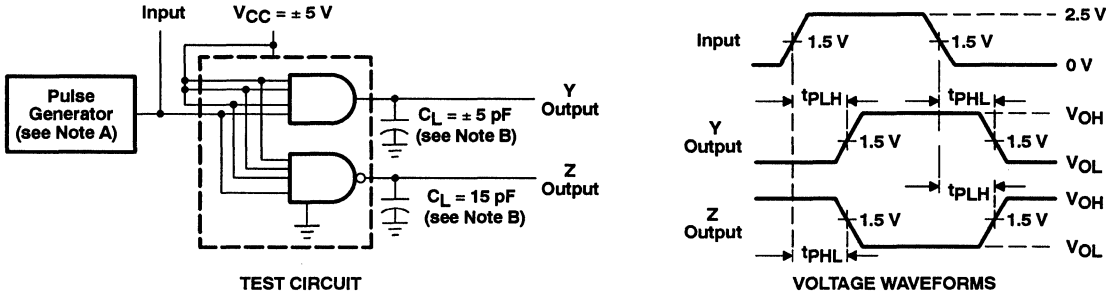
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Y (AND) output	V_{IH} = 2 V,	I_{OH} = −0.8 mA	2.4			V
			V_{IH} = 2 V,	I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IL} = 0.8 V,	I_{OL} = 32 mA		0.2		V
			V_{IL} = 0.8 V,	I_{OL} = 40 mA		0.22	0.4	
V_{OH}	High-level output voltage	Z (NAND) output	V_{IL} = 0.8 V,	I_{OH} = −0.8 mA	2.4			V
			V_{IL} = 0.8 V,	I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 32 mA		0.2		V
			V_{IH} = 2 V,	I_{OL} = 40 mA		0.22	0.4	
I_{IH}	High-level input current		V_{IH} = 2.4 V				120	μA
I_I	Input current at maximum input voltage		V_{IH} = 5.5 V				2	mA
I_{IL}	Low-level input current		V_{IL} = 0.4 V				−4.8	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V,	T_A = 125°C	−40	−100	−120	mA
I_{CC}	Supply current (average per driver)		V_{CC} = 5 V, No load	All inputs at 5 V,		10	18	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

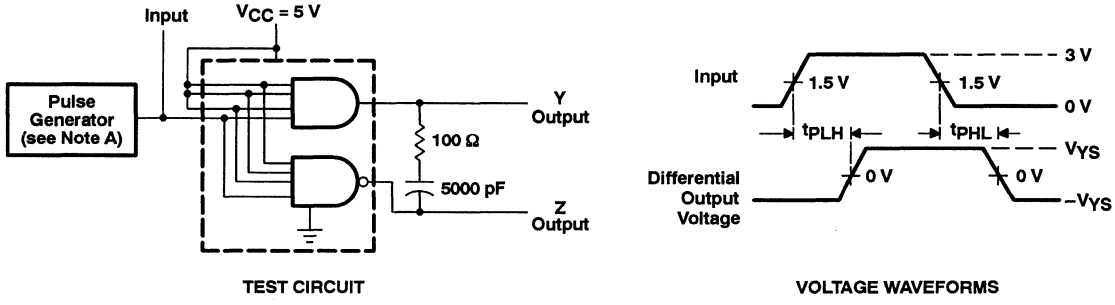
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Y output	AND gates	C_L = 15 pF, See Figure 1(a)		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Y output				12	18	ns
t_{PLH}	Propagation delay time, low-to-high-level Z output	NAND gates			6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Z output				6	8	
t_{PLH}	Propagation delay time, low-to-high-level differential output	Y output with respect to Z output	Z_L = 100 Ω in series with 5000 pF, See Figure 1(b)		9	16	ns
t_{PHL}	Propagation delay time, high-to-low-level differential output				8	16	ns

PARAMETER MEASUREMENT INFORMATION



(a) OUTPUTS Y AND Z



(b) DIFFERENTIAL OUTPUT

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, tr ≤ 10 ns, t_f ≤ 10 ns, t_w = 0.5 μS, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with R_{in} ≥ 1 MΩ.

Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS†

THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

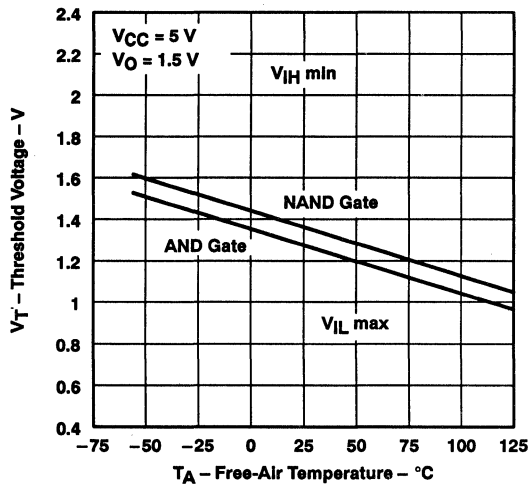


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

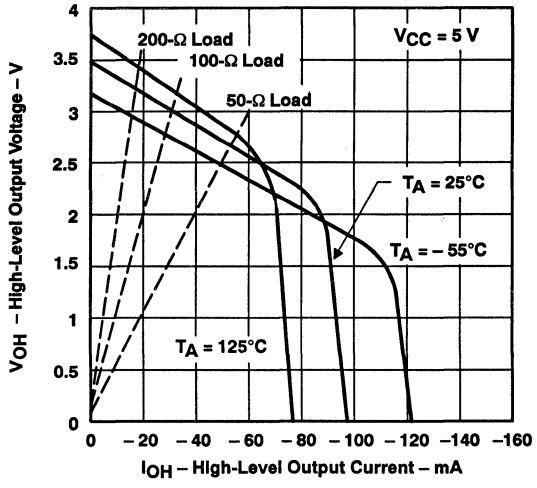


Figure 3

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

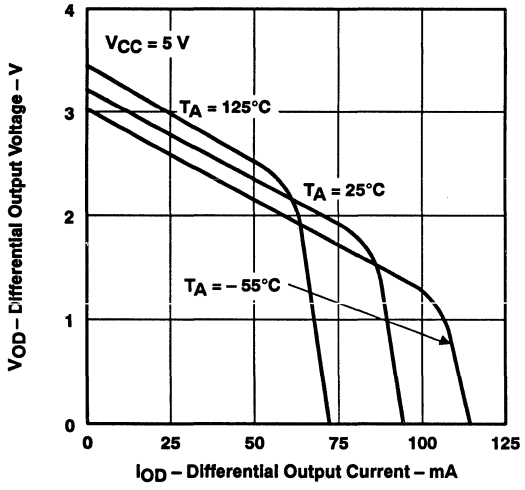


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

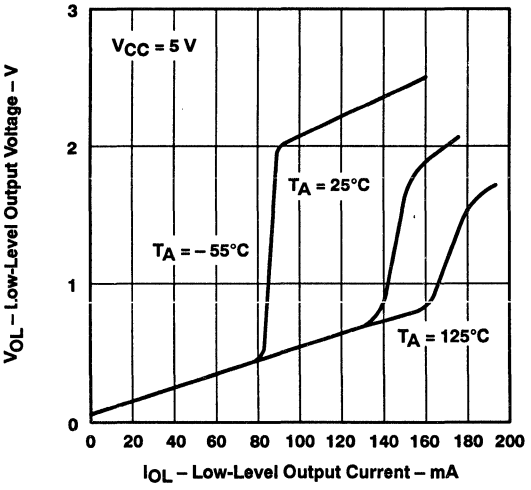


Figure 5

† Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME OF DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE

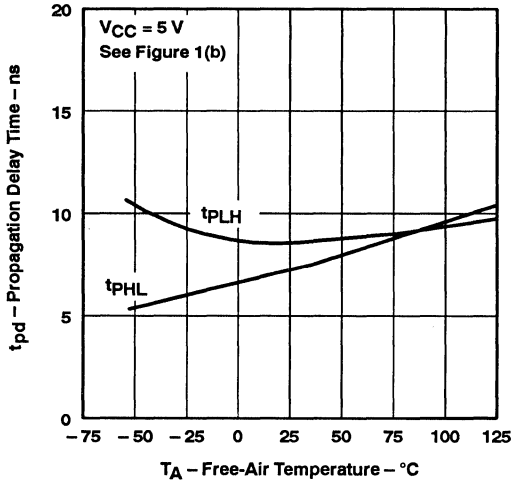


Figure 6

TOTAL POWER DISSIPATION (BOTH DRIVERS) vs FREQUENCY

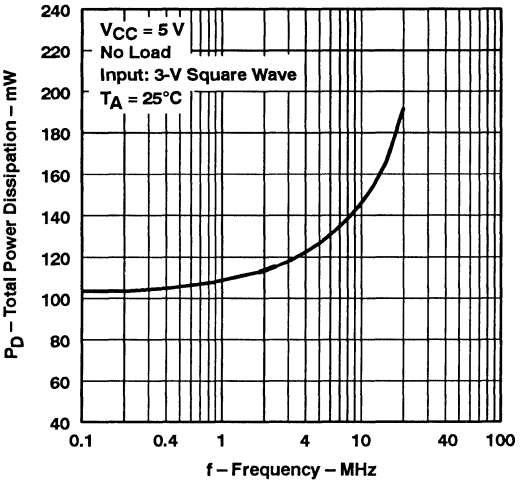
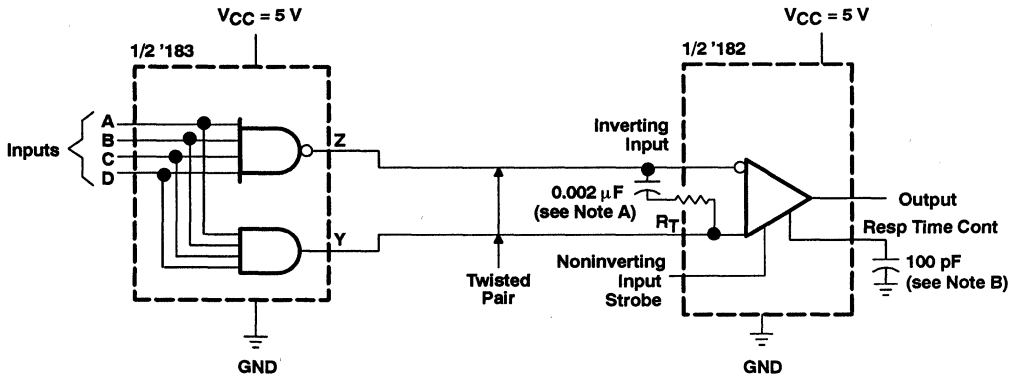


Figure 7

† Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\ (5 \times 10^6)\ (0.002 \times 10^{-6})}$$

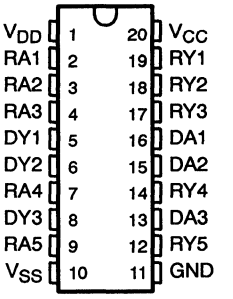
$$Z_C \sim 16\ \Omega$$

B. Use of a capacitor to control response time is optional.

Figure 8. Transmission of Digital Data Over Twisted-Pair Line

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Single Chip With Easy Interface Between UART and Serial Port Connector**
- **Less Than 9-mW Power Consumption**
- **Wide Driver Supply Voltage . . . 4.5 V to 13.2 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1100 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **ESD Protection Exceeds 500 V Per MIL-STD-883C, Method 3015**

DW OR N PACKAGE
(TOP VIEW)

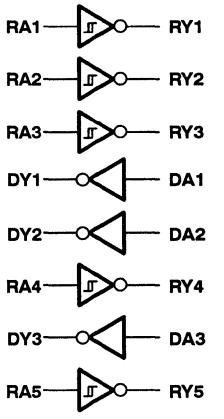


description

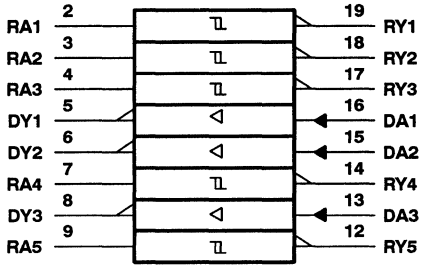
The SN65C185 and SN75C185 are low-power BI-MOS devices containing three independent drivers and five receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The SN65C185 and SN75C185 will typically replace one SN75188 and two SN75189 devices. These devices have been designed to conform to Standards ANSI/EIA-232-D-1986, which supersedes RS-232-C. The three drivers and five receivers of the SN65C185 and SN75C185 are similar to those of the SN75C188 quad drivers and SN75C189A quad receivers, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses that are shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C185 and SN75C185 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices will interface to single inputs of peripheral devices such as ACEs, UARTS, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C185 and SN75C185 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

logic diagram (positive logic)



logic symbol†

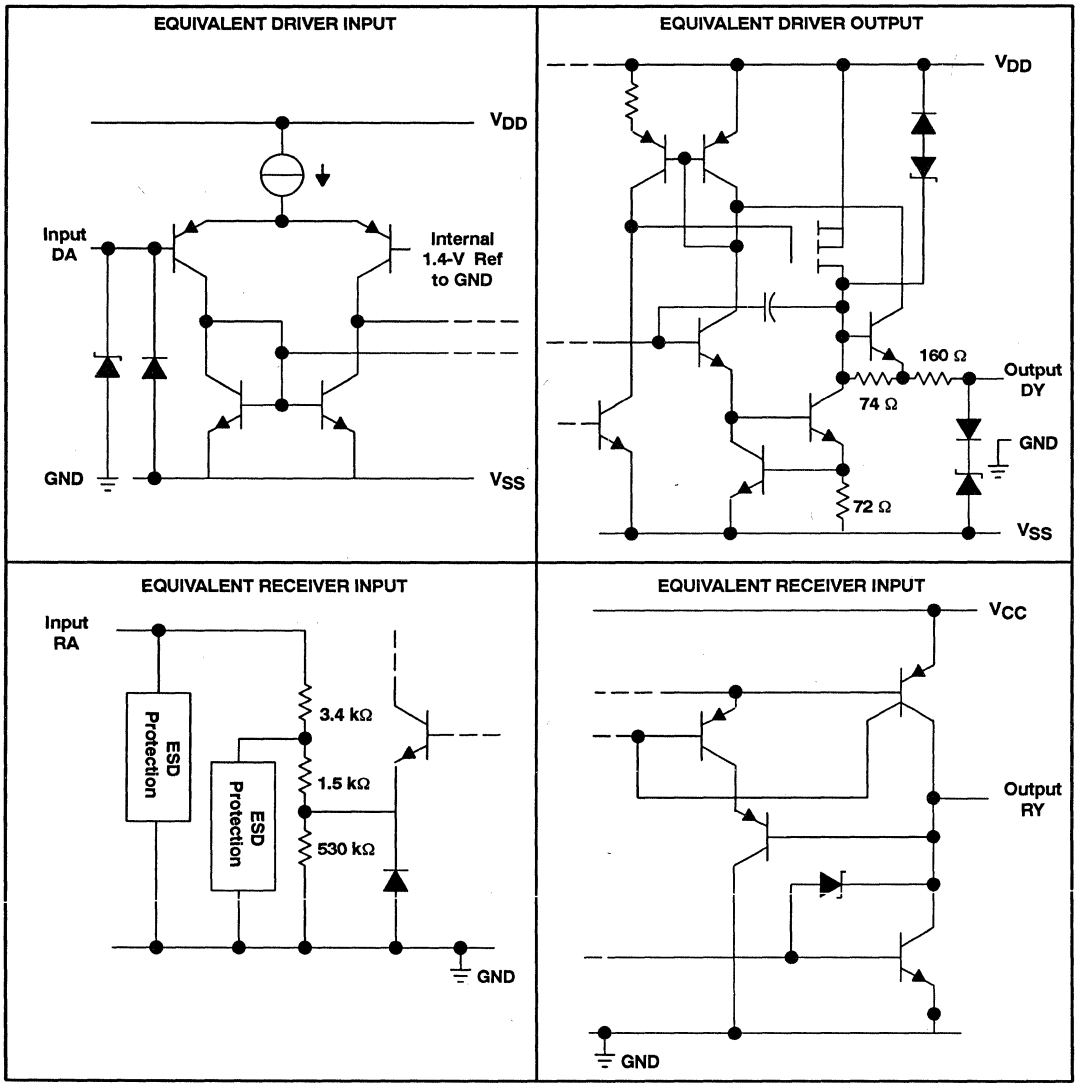


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description (continued)

The SN65C185 is characterized for operation from −40°C to 85°C. The SN75C185 is characterized for operation from 0°C to 70°C.

equivalent schematics of inputs and outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 13.5 V
Supply voltage, V_{SS} ..... −13.5 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range: Driver ..... V_{SS} to V_{DD}
Receiver ..... −30 V to 30 V
Output voltage range: Driver ..... V_{SS} − 6 V to V_{DD} + 6 V
Receiver ..... −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C185 ..... −40°C to 85°C
SN75C185 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	585 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	13.2	V
Supply voltage, V_{SS}		−4.5	−12	−13.2	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)	Driver	$V_{SS}+2$		V_{DD}	V
	Receiver	−25		25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
High-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C185	−40		85	°C
	SN75C185	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = −5 V		115	200	μA
			V_{DD} = 12 V,	V_{SS} = −12 V		115	200	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = −5 V		−115	−200	μA
			V_{DD} = 12 V,	V_{SS} = −12 V		−115	−200	
I_{CC}	Supply current from V_{CC}	No load All inputs at 0 or 5 V	V_{DD} = 5 V,	V_{SS} = −5 V			750	μA
			V_{DD} = 12 V,	V_{SS} = −12 V			750	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD}= 5 V,	V_{SS} = −5 V	4	4.5		V
			V_{DD} = 12 V,	V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD}= 5 V,	V_{SS} = −5 V		−4.4	−4	V
			V_{DD} = 12 V,	V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2					1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2					−1	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)	V_I = 0.8 V, See Figure 1	V_O = 0 or V_O = V_{SS},		−4.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)	V_I = 2 V, See Figure 1	V_O = 0 or V_O = V_{DD},		4.5	12	19.5	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, See Note 4	V_O = −2 V to 2 V,		300	400		Ω

† All typical values are at T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA-232-D.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high-to-low-level output (see Note 5)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,		1.2	3	µs
t_{PHL}	Propagation delay time, low-to-high-level output (see Note 5)				2.5	3.5	µs
t_{TLH}	Transition time, low-to-high-level output			0.53	2	3.2	µs
t_{THL}	Transition time, high-to-low-level output			0.53	2	3..2	µs
t_{TLH}	Transition time, low-to-high-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 2500 pF,		1	3	µs
t_{THL}	Transition time, high-to-low-level output (see Note 6)				1	3	µs
SR	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,	4	10	30	V/µs

NOTES: 5. t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and is measured at the 50% points.
6. Measured between 3-V and −3-V points of output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshhold voltage	See Figure 5			1.6	2.1	2.55	V
V_{T-}	Negative-going threshhold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				600	1100		mV
V_{OH}	High-level output voltage	V_I = 0.75 V,	I_{OH} = −20 μA,	See Figure 5 and Note 7	3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V		2.8	4.4		
			V_{CC} = 5 V		3.8	4.9		
			V_{CC} = 5.5 V		4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V,	I_{OL} = 3.2 mA,	See Figure 5		0.17	0.4	V
I_{IH}	High-level output current	V_I = 3 V			0.43	0.55	1	mA
		V_I = 25 V			3.6	4.6	8.3	
I_{IL}	Low-level output current	V_I = −3 V			−0.43	−0.55	−1	mA
		V_I = −25 V			−3.6	−5.0	−8.3	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V,	V_O = 0,	See Figure 4		−8	−15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC},	V_O = V_{CC},	See Figure 4		13	25	mA

† All typical values are at T_A = 25°C.

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs will remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 5 kΩ, See Figure 6	C_L = 50 pF,		3	4	μs
t_{PHL}	Propagation delay time, high-to-low-level output				3	4	μs
t_{TLH}	Transition time, low-to-high-level output				300	450	ns
t_{THL}	Transition time, high-to-low-level output				100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise (see Note 8)	R_L = 5 kΩ, See Figure 6	C_L = 50 pF,	1		4	μs

NOTE 8: The intent of this specification is that any input pulse of less than 1 μs will have no effect on the output, and any pulse duration of greater than 4 μs will cause the output to change state twice. Reaction to a pulse duration between 1 μs and 4 μs is uncertain.

PARAMETER MEASUREMENT INFORMATION

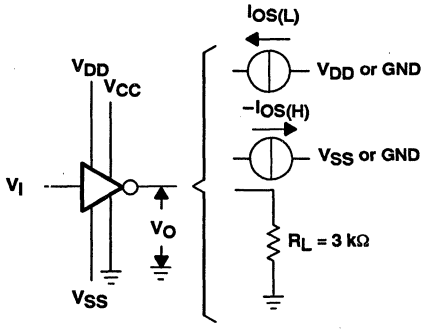


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

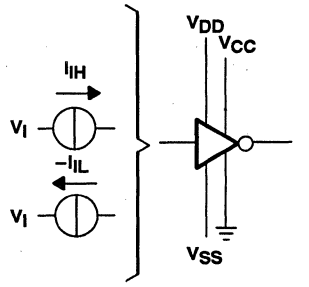
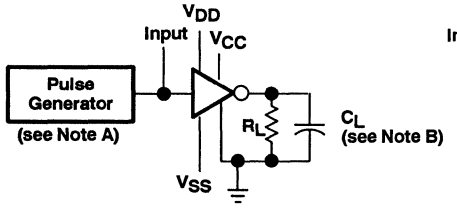
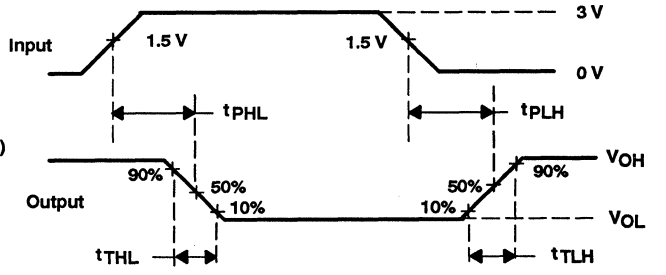


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

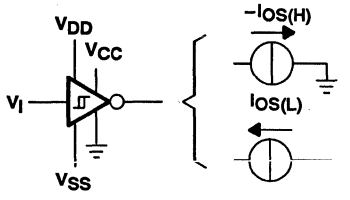


Figure 4. Receiver Test Circuit for $I_{OS(H)}$ and $I_{OS(L)}$

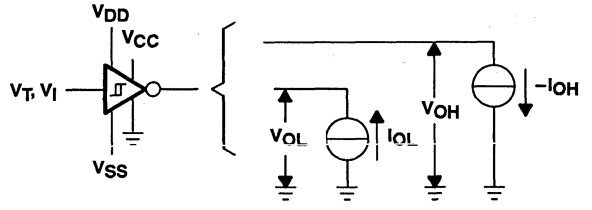
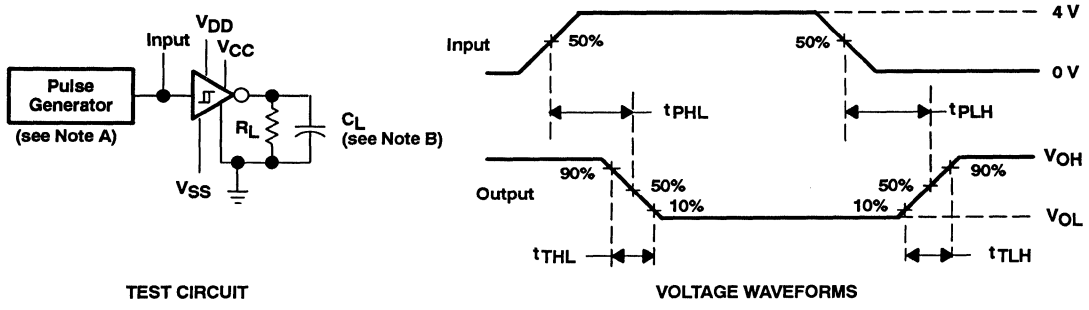


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

APPLICATION INFORMATION

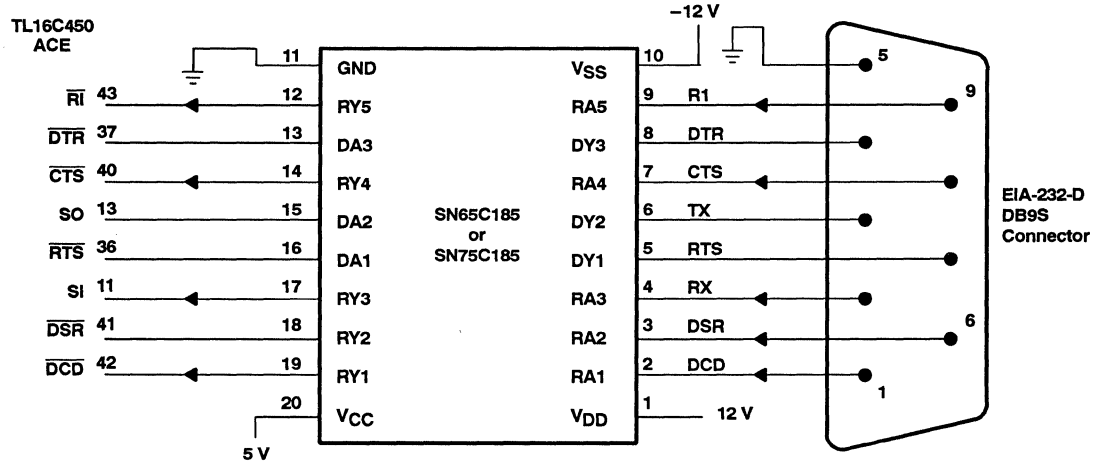


Figure 7. Typical Connection

SLLS068B – D3389, FEBRUARY 1990 – REVISED MARCH 1993

- **Meets Standards RS-232-C, EIA-232-D, and CCITT V.28**
- **Four Independent Drivers and Receivers**
- **Loopback Mode Functionally Self-Tests Drivers and Receivers Without Disconnection From Line**
- **Driver Slew Rate Limited to 30 V/μs Max**
- **Built-In Receiver 1-μs Noise Filter**
- **Internal Thermal Overload Protection**
- **EIA-232-D Inputs and Outputs Withstand ±30 V**
- **Low Supply Current . . . 2.5 mA Typ**
- **ESD Protection Exceeds 4000 V Per MIL-STD-833C Method 3015**

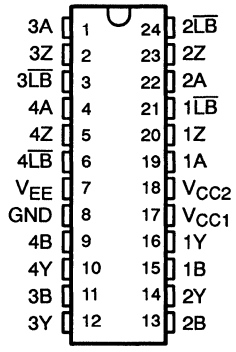
description

The SN75186 is a low-power bipolar device containing four driver/receiver pairs designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). Additionally, the SN75186 has a loopback mode that may be used by a data communication system to perform a functional self test on each driver/receiver pair, removing the need to locally disconnect cables and install a loopback connector. Flexibility of control is ensured by each driver/receiver pair having its own loopback control input. The SN75186 is designed to conform to standards RS-232-C, its revision ANSI/EIA-232-D-1986, and CCITT V.28.

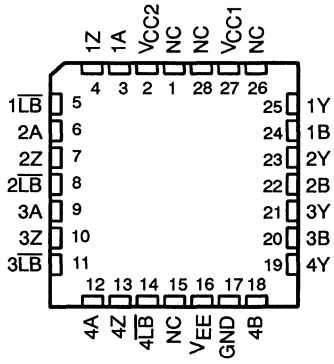
The maximum slew rate is limited to 30 V/μs at the driver outputs and drives a capacitive load of 2500 pF at 20 kBaud. The receivers have input filters that disregard input noise pulses shorter than 1 μs. The SN75186 is a robust device capable of withstanding ±30 V at driver outputs and at receiver inputs whether powered or unpowered. This device has an internal ESD protection rated at 4 kV to prevent functional failures.

The SN75186 is characterized for operation from 0°C to 70°C.

DW PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

EACH RECEIVER

LOOPBACK	INPUTS		OUTPUT
$\overline{LB}$	A	B†	Z
H	X	H	L
H	X	L	H
L	L	X	L
L	H	X	H

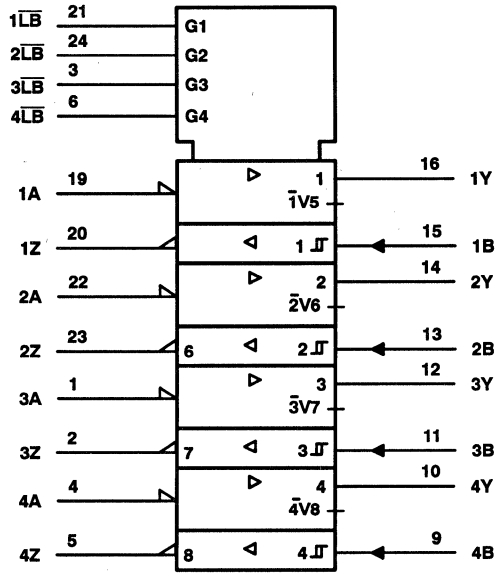
EACH DRIVER

LOOPBACK	INPUT	OUTPUT
$\overline{LB}$	A	Y†
H	H	L
H	L	H
L	X	L

† Voltages are RS-232-C, EIA-232-D, and V.28 levels

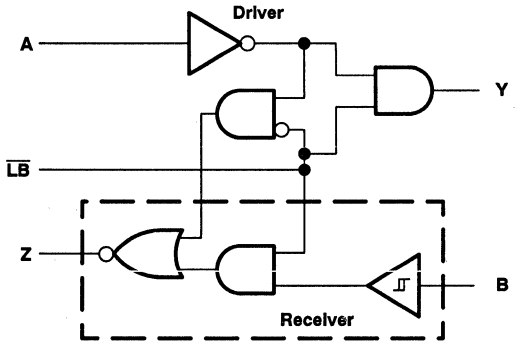
H = high level, L = low level, X = irrelevant

logic symbol†

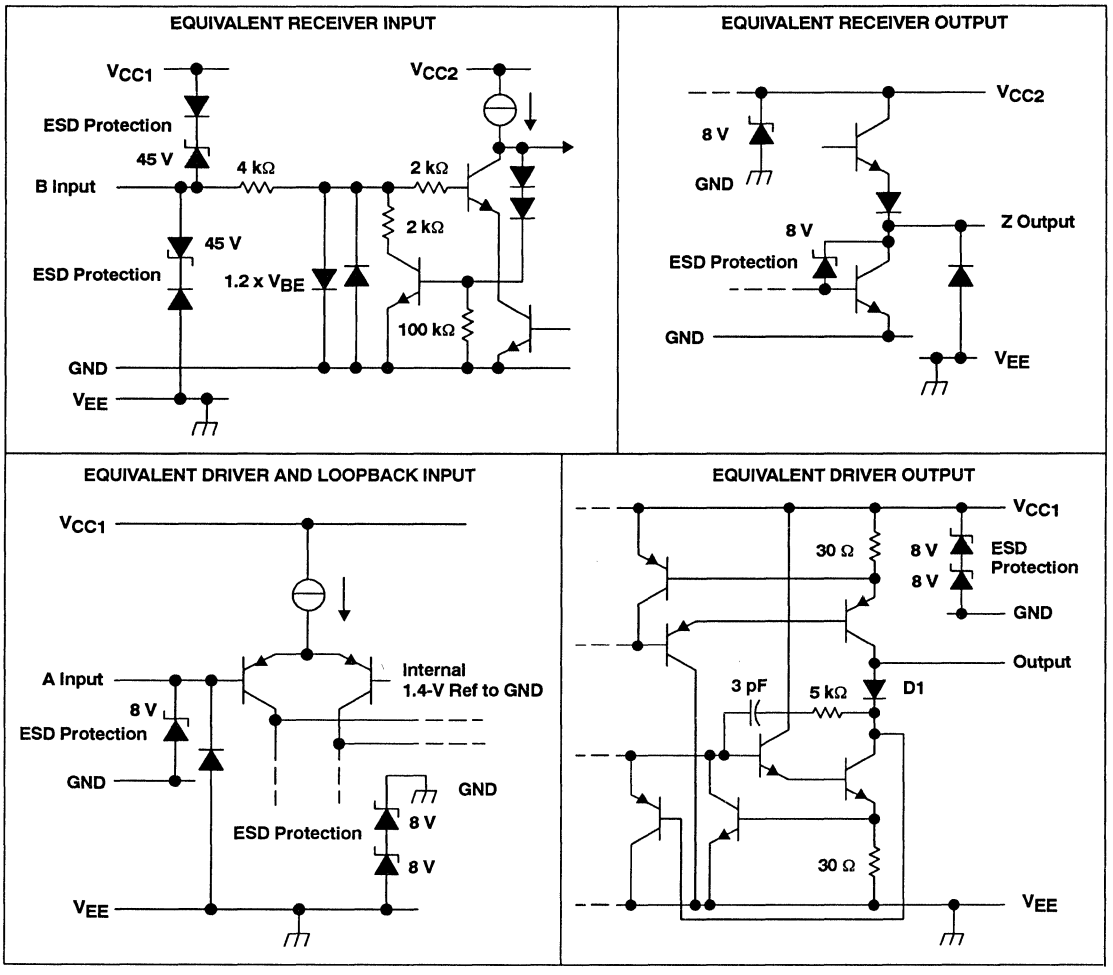


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

logic diagram, each driver/receiver pair (positive logic)



schematics of inputs and outputs



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 7 V
Supply voltage, V_{EE} ..... −15 V
Receiver input voltage range ..... −30 V to 30 V
Driver input voltage range ..... (V_{EE} + 2 V) to V_{CC1}
Loopback input voltage range ..... 0 V to 7 V
Driver output voltage range ..... −30 V to 30 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
FN	1400 mW	11.2 mW/°C	896 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
Supply voltage, V_{EE}		−10.8	−12	−13.2	V
Input voltage, V_I	Driver and loopback	0		V_{CC2}	V
Input voltage, V_I (see Note 2)	Receiver			±30	V
High-level input voltage, V_{IH}	Driver and loopback	2			V
Low-level input voltage, V_{IL}	Driver and loopback			0.8	V
Output voltage powered on or off, V_O	Driver			±30	V
High-level output current, I_{OH}	Receiver			−4	mA
Low-level output current, I_{OL}	Receiver			4	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 2: If all receiver inputs are held at ±30 V, the thermal dissipation limit of the package may be exceeded. The thermal shutdown may not protect the device, as this dissipation occurs in the receiver input resistors.

DRIVER SECTION

electrical characteristics over full recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ, V_{IL} = 0.8 V, See Figure 1	7			V
V_{OL}	Low-level output voltage‡	R_L = 3 kΩ, V_{IH} = 2 V, See Figure 1			–7	V
$V_{OH(LB)}$	High-level output voltage in loopback mode‡§¶	R_L = 3 kΩ, $\overline{LB}$ at 0.8 V, V_{IL} = 0.8 V			–7	V
I_{IH}	High-level input current (driver and loopback inputs)#	V_I = 5 V, See Figure 2			100	μA
I_{IL}	Low-level input current (driver and loopback inputs)#				–100	μA
$V_{OS(H)}$	High-level short-circuit output current	V_I = 0.8 V, V_O = 0, See Note 3 and Figure 1	–10	–20	–35	mA
$V_{OS(L)}$	Low-level short-circuit output current	V_I = 2 V, V_O = 0, See Note 3 and Figure 1	10	20	35	mA
I_{CC1}	Supply current from V_{CC1}	No load		2.5	4	mA
$I_{CC1(LB)}$	Supply current from V_{CC1} with loopback on	No load, $\overline{LB}$ at 0.8 V			10	mA
I_{EE}	Supply current from V_{EE}	No load		–2.5	–4	mA
$I_{EE(LB)}$	Supply current from V_{EE} with loopback on	No load, $\overline{LB}$ at 0.8 V			–10	mA
I_{CC2}	Supply current from V_{CC2}	No load, V_I = 0, See Note 5		–10	–100	μA
$I_{CC2(LB)}$	Supply current from V_{CC2} with loopback on	No load, See Note 5 LB at 0.8 V, V_I = 0,		–10	–100	μA
		V_{CC1} = V_{EE} = V_{CC2} = 0, V_O = –2 V to 2 V, See Note 4	0.3	5		kΩ

† All typical values are at T_A = 25°C.
‡ The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
§ This is the most positive level that the driver output will rise to when the device is in the loopback mode and the driver input is at a low level.
¶ The loopback mode should be entered only when the driver output is in the low (marking) state.
# Unused driver inputs should be tied to 0 V or V_{CC2}; unused loopback inputs should be tied to V_{CC2}.

NOTES: 3. Minimum $I_{OS(H)}$ and $I_{OS(L)}$ are specified at V_O = 0, as this more accurately describes the output current needed to dynamically drive capacitive lines. A minimum of ±10 mA is sufficient to drive 2500 pF in parallel with 3 kΩ at a slew rate of 4 V/μs (in accordance with EIA-232-D and V.28).
4. Test conditions are those specified by EIA-232-D.
5. Without a load and V_I = 0, the worst-case conditions, V_{CC2} sources a small current originating from V_{CC1} giving I_{CC2} supply current a negative sign. When a receiver has an output load, V_{CC2} sinks static and dynamic supply currents to meet load requirements.

switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		0.6	5	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.8	5	μs
t_{skew}	$\lvert t_{PLH} - t_{PHL} \rvert$	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF		0.2	1	μs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF	4		30	V/μs
$t_{pd(ILB)}$	Propagation delay time going into loopback mode‡	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 7		3	50	μs
$t_{pd(OLB)}$	Propagation delay time going out of loopback mode§	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 7		3	50	μs
$t_{pd(LB)}$	Propagation delay time in loopback mode¶	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 8		3	15	μs
t_{skew}	Skew time in loopback mode	R_L = 3 kΩ to 7 kΩ, See Note 6		4	10	μs

† All typical values are at T_A = 25°C.
‡ This is the delay between entering the loopback mode and when the data on the receiver output becomes valid.
§ This is the worst-case (rising or falling edges) total propagation delay between driver input and receiver output when in the loopback mode.
¶ This is the magnitude of the difference between the propagation delay time of the rising and falling edges of $t_{pd(LB)}$.
NOTE 6: Skew time is the magnitude of the difference between t_{PHL} and t_{PLH} and is measured with a 0 to 3-V input pulse.

RECEIVER SECTION

electrical characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5		1.3	2	2.5	V
V_{T-}	Negative-going threshold voltage	See Figure 5		0.5	1	1.7	V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5	1	1.5	V
V_{OH}	High-level output voltage	V_I = –3 V or inputs open,	I_{OH} = –20 μA	3.5			V
		I_{OH} = –4 mA,	See Note 7 and Figure 5	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 5	V_I = 3 V,			0.4	V
$I_{OS(H)}$	Short-circuit output current at high level	V_{OH} = 0,	See Figure 4		–20	–60	mA
$I_{OS(L)}$	Short-circuit output current at low level	$V_{OL} = V_{CC2}$,	See Figure 4		20	60	mA
r_{in}	Input resistance	$\lvert V_I \rvert \le 25$ V		3			kΩ
		$\lvert V_I \rvert$ = 3 V to 25 V				7	

NOTE 7: If the inputs are left unconnected, the receiver interprets this as a low input and the receiver outputs will remain in the high state.

switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 6			2	6	μs
t_{PHL}	Propagation delay time, high-to-low-level output				2	6	μs
t_{TLH}	Transition time, low-to-high level output‡	C_L = 50 pF,	See Figure 6		200	300	ns
t_{THL}	Transition time, high-to-low level output‡				50	300	ns
t_{skew}	$\lvert t_{PLH} - t_{PHL} \rvert$				0.1	1	μs
t_w	Maximum pulse duration assumed to be noise§	Pulse amplitude = 5 V		1	2	4	μs

† All typical values are at T_A = 25°C.
‡ Transition times are measured between 10% and 90% points on output waveform.
§ The receiver will ignore any positive- or negative-going pulse whose duration is less than the minimum value of t_w and accept any positive- or negative-going pulse whose duration is greater than the maximum value of t_w.

PARAMETER MEASUREMENT INFORMATION

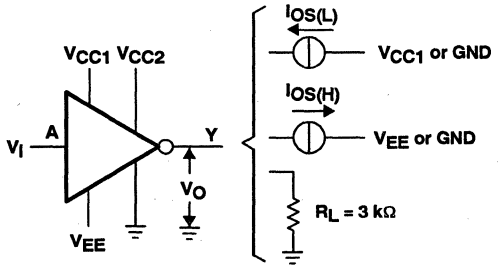


Figure 1. Driver Test Circuit, V_{OH}, V_{OL}, $I_{OS(L)}$, $I_{OS(H)}$

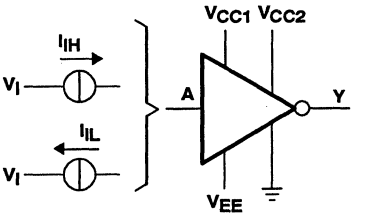
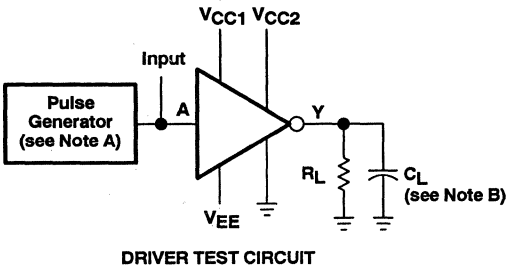


Figure 2. Driver and Loopback Test Circuit, I_{IL}, I_{IH}



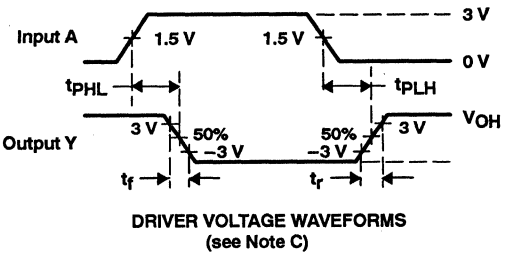


Figure 3. Driver Test Circuit and Voltage Waveforms

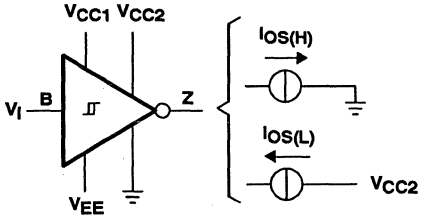


Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$

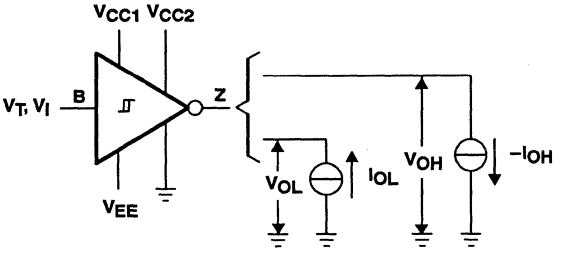


Figure 5. Receiver Test Circuit, V_T, V_{OL}, V_{OH}

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Slew rate = $\frac{6\ V}{t_r \text{ or } t_f}$

PARAMETER MEASUREMENT INFORMATION

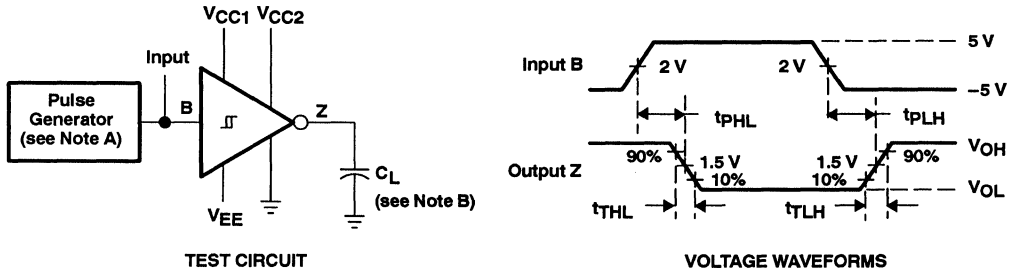


Figure 6. Receiver Propagation and Transition Times

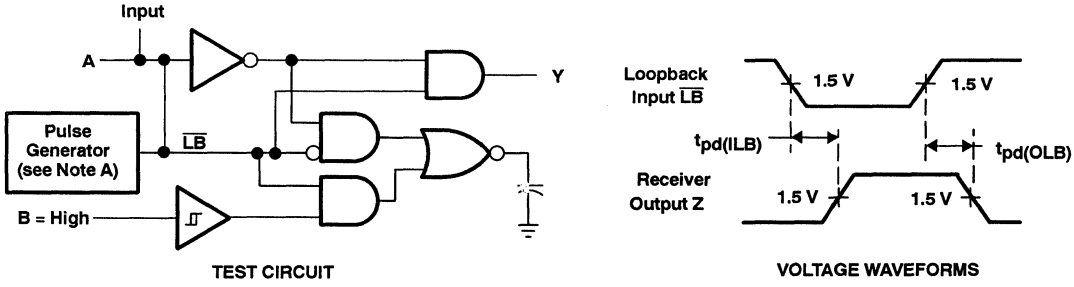


Figure 7. Loopback Entry and Exit Propagation Times

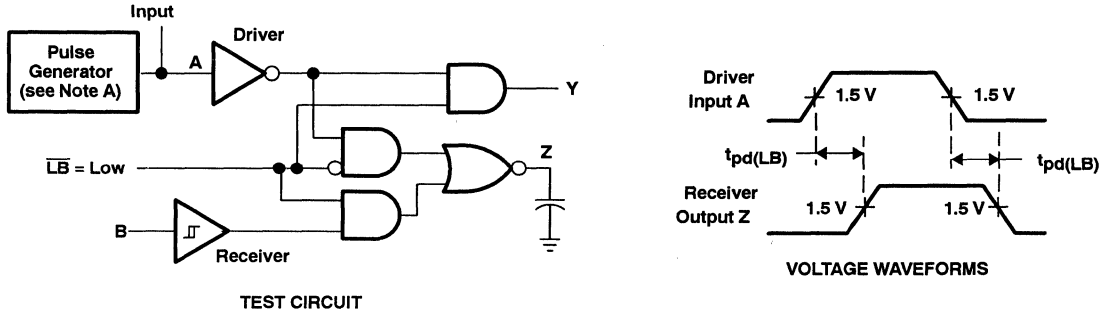


Figure 8. Loop Propagation Times in Loopback Mode

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PRINCIPLES OF OPERATION

In normal operation, the SN75186 acts as four independent drivers and receivers; the loopback mode is held off by keeping logic inputs $\overline{LB}$ high. Taking a particular $\overline{LB}$ input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, –5 V, or the EIA-232-D marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75186 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages that are greater than (V_{EE} + 7 V) and less than V_{EE} typically. For example, with V_{EE} = –12 V, line short circuits to voltages greater than –5 V and less than –12 V will be detected. The loopback mode should be entered only when the driver output is low, that is, the marking condition of EIA-232-D. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.

When in the loopback mode, approximately 95% of the SN75186 circuit is functionally checked. There exists some low probability of fault mechanisms in circuitry not checked in the loopback mode. To reduce the chances of undetected failure, the unchecked circuitry has been designed to be more robust than that within the loopback test loop. The areas where special attention has been paid are the receiver input potential divider and resistors, the driver output blocking diode (D1), and parts of the driver clamp circuit.

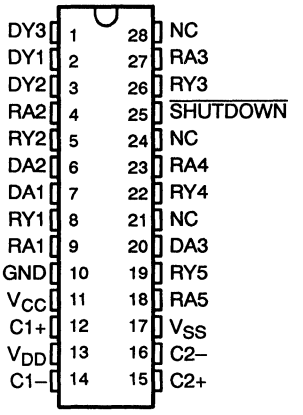
Protection of the SN75186 is achieved by means of driver output current limits and a thermal trip. Although this device will withstand ±30 V at its receiver input, package thermal dissipation limitations have to be taken into consideration if more than one receiver is connected simultaneously. This is due to the possible dissipation in the 3-kΩ minimum input resistors, which is not under the control of the thermal trip. Although the supply current is higher in the loopback mode than in normal operation, the total power dissipation is not sufficient under normal worst-case conditions (of receiver input V_I = 15 V + 10%, receiver output voltage = 2.4 V at 4 mA, driver load of 3 kΩ) to cause the thermal limiting circuitry to trip.

If the SN75186 goes into thermal trip, the output of the driver goes to a high-impedance state and the receiver output is held in a logic-high marking state. Both driver and receiver outputs maintain a marking state for the following circuit and do not allow indeterminate conditions to exist.

The standards specify a minimum driver output resistance to ground of 300 Ω when the device is powered off. To fully comply with EIA-232-D power-off fault conditions, many drivers need diodes in series with each supply voltage to prevent reverse current flow and driver damage. The SN75186 overcomes this need by providing a high-impedance driver output of typically 5 kΩ under power-off conditions through the use of the equivalent of these series diodes in the driver output circuit.

- **Single IC and Single 5-V Supply Interface for Serial Communication Ports**
- **Three EIA/TIA-E Drivers and Five Receivers Meet EIA/TIA-232-E-1991, EIA/TIA-562, and CCITT Recommendation V.28 Standards**
- **Switched-Capacitor Voltage Converter Eliminates Need for ±12-V Supplies**
- **Voltage Converter Operates With Low Capacitance . . . 0.1 μF Min**
- **ESD Protection on RS-232 Lines Exceeds 6 kV Per MIL-STD-883C, Method 3015**
- **Designed for Data Rates up to 120 kb/s Over 3-m Cable**
- **Available in Shrink Small-Outline 25-mil-Pitch Package**
- **Shutdown Mode to Save Power When Not in Use**
- **±30-V Receiver Input Voltage Range**
- **LinBiCMOS™ Process Technology**
- **Applications**
  - **Laptop or Notebook Computers**
  - **Portable Terminals**
  - **Single-Board Computers**
  - **Portable Test Equipment**

DB PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75LBC187 is a low-power LinBiCMOS™ device containing three independent drivers, five receivers, and a switched-capacitor voltage converter. The SN75LBC187 provides a single integrated circuit (IC) and single 5-V supply interface between the asynchronous communications element and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standards EIA/TIA-232-E-1991, EIA/TIA-562, and CCITT recommendation V.28.

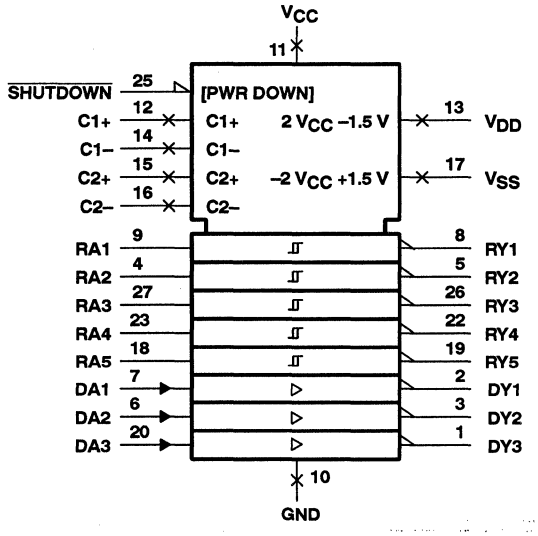
The switched-capacitor voltage converter of the SN75LBC187 uses four small external capacitors to generate the positive and negative voltages required by EIA-232 (and V.28) line drivers from a single 5-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage. The device also features a reduced power or shutdown mode that cuts the quiescent power to the IC when not transmitting data between the CPU and peripheral.

The SN75LBC187 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LBC187 is characterized for operation from 0°C to 70°C.

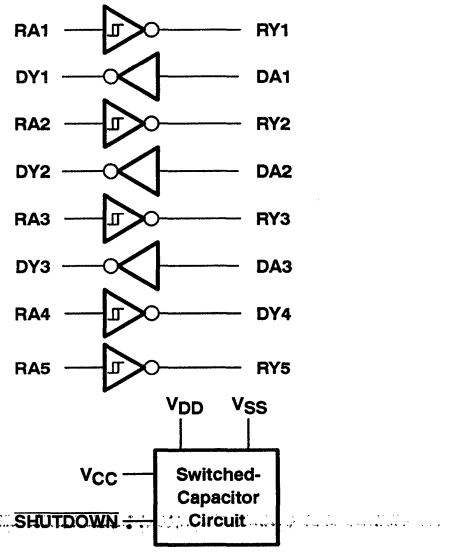
NOTE: This device includes circuit designs and process technologies that have patents pending.

LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... 0.3 V to 6 V
Positive output supply voltage range, V_{DD} ..... V_{CC} –0.3 V to 15 V
Negative output supply voltage range, V_{SS} ..... 0.3 V to –15 V
Input voltage range: RA ..... ±30 V
All other inputs ..... –0.3 V to V_{CC} + 3 V
Output voltage range: DY ..... –2 V_{CC} + 1.2 V to 2 V_{CC} – 1.2 V
All other outputs ..... –0.3 V to V_{CC} + 3 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	DA	2			V
	RA, $\overline{\text{SHUTDOWN}}$	2.4			
Low-level input voltage, V_{IL}	RA, DA, $\overline{\text{SHUTDOWN}}$			0.8	V
Receiver input voltage, V_I		−25		25	V
High-level output current, I_{OH}	RY			−1	mA
Low-level output current, I_{OL}	RY			3.2	mA
Output current, I_O	V_{DD}			±10	μA
	V_{SS}			±10	μA
C1, C2, C3, C4 charge pump capacitors		0.1	0.47		μF
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Receiver	I_O = −1 mA	3.5			V
		Driver	R_L = 3 kΩ to GND	5	7		
V_{OL}	Low-level output voltage	Receiver	I_O = 3.2 mA			0.4	V
		Driver	R_L = 3 kΩ to GND		−7	−5	
V_{T+}	Receiver positive-going input voltage threshold				1.7	2.4	V
V_{T-}	Receiver negative-going input voltage threshold			0.8	1.2		V
V_{hys}	Receiver input hysteresis ($V_{T+} - V_{T-}$)				0.5	1	V
r_i	Receiver input resistance		V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ
r_o	Driver output resistance		V_{CC} = 0, V_O = ±2 V	300			Ω
I_I	Input current (DA, $\overline{\text{SHUTDOWN}}$)		V_I = 0 to V_{CC}			±50	μA
I_{OS}	Driver output short-circuit current		V_O = 0	±10			mA
I_{CC}	Supply current		All outputs open, $\overline{\text{SHUTDOWN}}$ at 2.4 V		15	30	mA
			All outputs open, $\overline{\text{SHUTDOWN}}$ at 0.1 V			10	μA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Receiver	R_L = 5 kΩ, See Figure 1	C_L = 50 pF,		1.25	µs
		Driver	R_L = 3 kΩ, See Figure 2	C_L = 1200 pF,		1.25	µs
t_{PHL}	Propagation delay time, high-to-low-level output	Receiver	R_L = 5 kΩ, See Figure 1	C_L = 50 pF,		1.25	µs
		Driver	R_L = 3 kΩ, See Figure 2	C_L = 1200 pF,		1.25	µs
t_r	Rise time, driver output		R_L = 3 kΩ, V_O = −3 V to 3 V,	C_L = 50 pF, See Note 2	200		ns
			R_L = 3 kΩ, V_O = −3.3 V to 3.3 V,	C_L = 2500 pF, See Note 3		1.5	µs
t_f	Fall time, driver output		R_L = 3 kΩ, V_O = 3 V to −3 V	C_L = 50 pF,	200		ns
			R_L = 3 kΩ, V_O = 3.3 V to −3.3 V	C_L = 2500 pF,		1.5	µs

NOTES: 2. The 200 ns for the output to change from −3 V to 3 V (or vice versa) corresponds to the 30 V/µs maximum slew rate of EIA/TIA-232-E, EIA/TIA-562, and CCITT V.28.
3. The more stringent requirement for transition times comes from the EIA/TIA-562, which requires the rise and fall times to be measured from 3.3 V.

PARAMETER MEASUREMENT INFORMATION

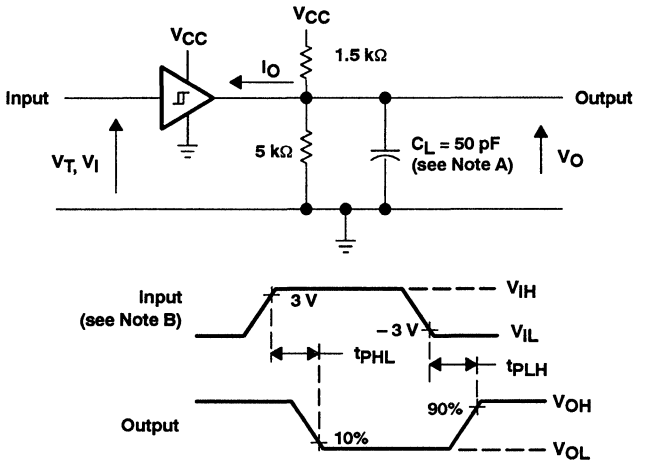


Figure 1. Receiver Test Circuit and Waveforms

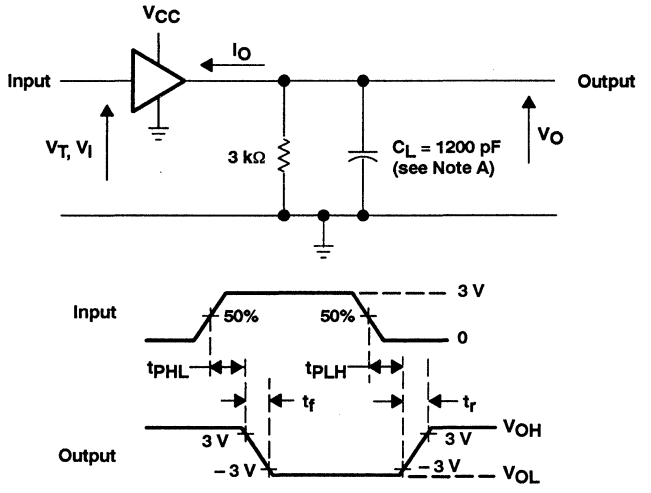
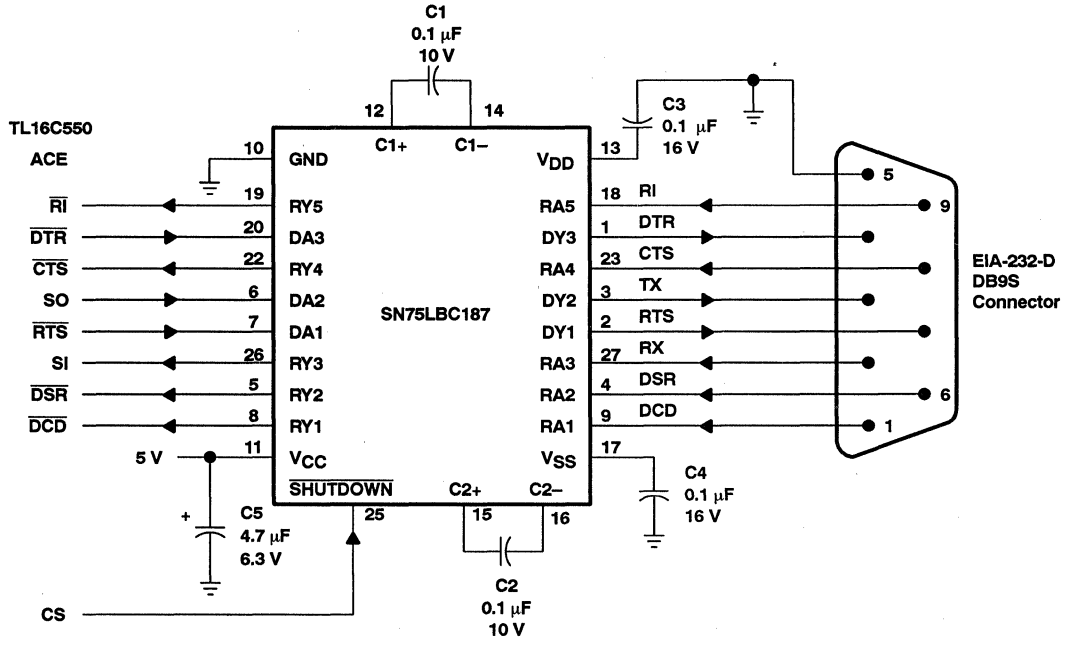


Figure 2. Driver Test Circuit and Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_W = 8.33 μs, PRR = 60 kHz, $t_r = t_f \leq 50$ ns.

APPLICATION INFORMATION

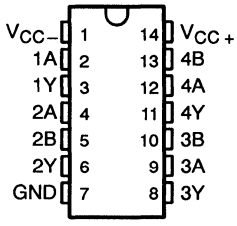


NOTE: C1, C2, C3, and C4 are Z5U-type ceramic-chip capacitors.

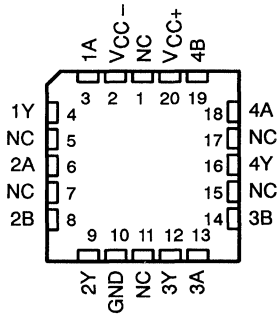
Figure 3. Typical SN75LBC187 Connection

- **Meets Specifications of EIA RS-232-C**
- **Designed to Be Interchangeable With Motorola MC1488**
- **Current-Limited Output: 10 mA Typ**
- **Power-Off Output Impedance: 300 Ω Min**
- **Slew Rate Control by Load Capacitor**
- **Flexible Supply Voltage Range**
- **Input Compatible With Most TTL Circuits**

SN55188 . . . J OR W PACKAGE
MC1488, SN75188 . . . D OR N PACKAGE
(TOP VIEW)



SN55188 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The MC1488, SN55188, and SN75188 are monolithic quad line drivers designed to interface data terminal equipment with data communications equipment in conformance with EIA Standard RS-232-C using a diode in series with each supply-voltage terminal as shown under typical applications.

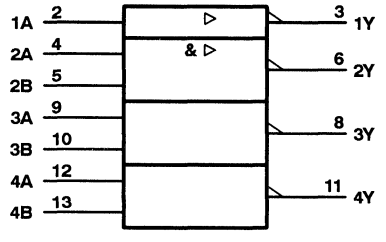
The and SN55188 is characterized for operation over the full military temperature range of –55°C to 125°C. The MC1488 and SN75188 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(drivers 2 through 4)

A	B	Y
H	H	L
L	X	H
X	L	H

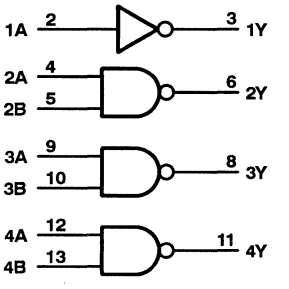
H = high level, L = low level,
X = irrelevant

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

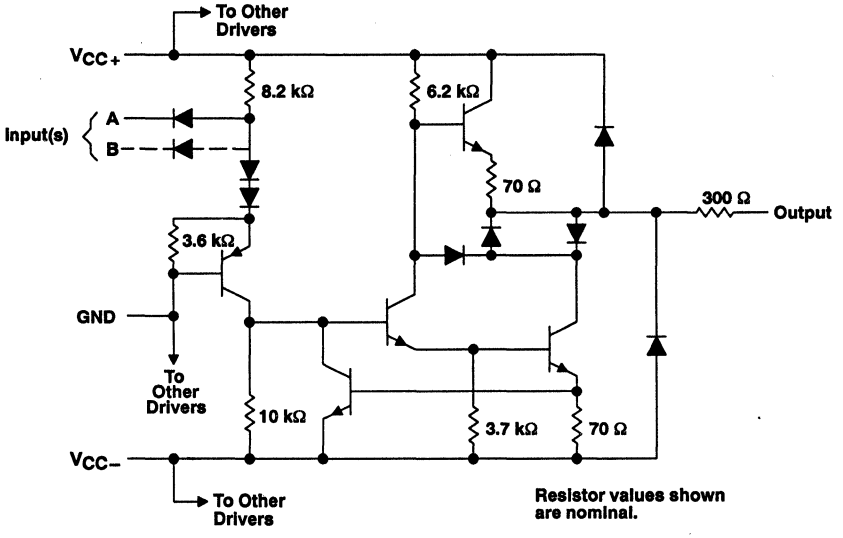
logic diagram (positive logic)



Positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 thru 4)

Pin numbers shown are for the D and N packages.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55188	MC1488 SN75188	UNIT
Supply voltage, V_{CC+}, at (or below) 25°C free-air temperature (see Notes 1 and 2)		15	15	V
Supply voltage, V_{CC-}, at (or below) 25°C free-air temperature (see Notes 1 and 2)		−15	−15	V
Input voltage range		−15 to 7	−15 to 7	V
Output voltage range		−15 to 15	−15 to 15	V
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300		

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the FK and J packages, SN55188 chips are alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

	SN55188			MC1488, SN75188			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	7.5	9	15	7.5	9	15	V
Supply voltage, V_{CC-}	−7.5	−9	−15	−7.5	−9	−15	V
High-level input voltage, V_{IH}	1.9			1.9			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 9$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55188			MC1488, SN75188			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7‡	−6		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5‡	−9		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10			10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6		−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level§	V_I = 0.8 V,	V_O = 0	−4.6	−9	−13.5	−6	−9	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level§	V_I = 1.9 V,	V_O = 0	4.6	9	13.5	6	9	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_O = −2 V to 2 V	V_{CC-} = 0,	300			300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20		15	20	mA
			All inputs at 0.8 V		4.5	6		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25		19	25	
			All inputs at 0.8 V		5.5	7		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34			34	
			All inputs at 0.8 V			12			12	
I_{CC-}	Supply current from I_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17		−13	−17	mA
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23		−18	−23	
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34			−34	
			All inputs at 0.8 V			−2.5			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576			576	

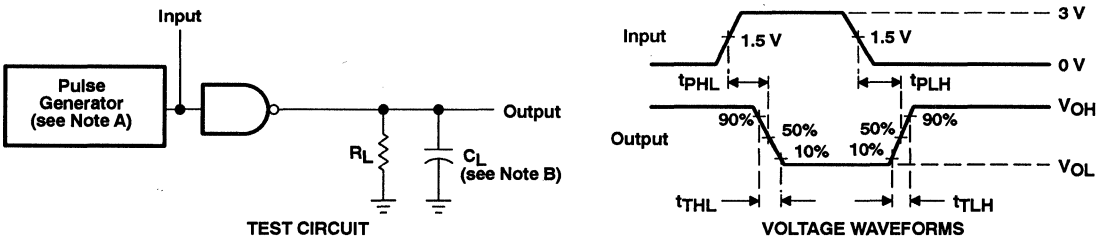
† All typical values are at T_A = 25°C.
‡ The algebraic convention in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more negative voltage.
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC\pm}$ = ±9 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ, See Figure 1	C_L = 15 pF,		220	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output				100	175	ns
t_{TLH}	Transition time, low-to-high-level output†				55	100	ns
t_{THL}	Transition time, high-to-low-level output†				45	75	ns
t_{TLH}	Transition time, low-to-high-level output‡	R_L = 3 kΩ to 7 kΩ, See Figure 1	C_L = 2500 pF,		2.5		µs
t_{THL}	Transition time, high-to-low-level output‡				3.0		µs

† Measured between 10% and 90% points of output waveform.
‡ Measured between 3 V and −3 V points on the output waveform (EIA RS-232-C conditions).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 µs, PRR ≤ 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

VOLTAGE TRANSFER CHARACTERISTICS

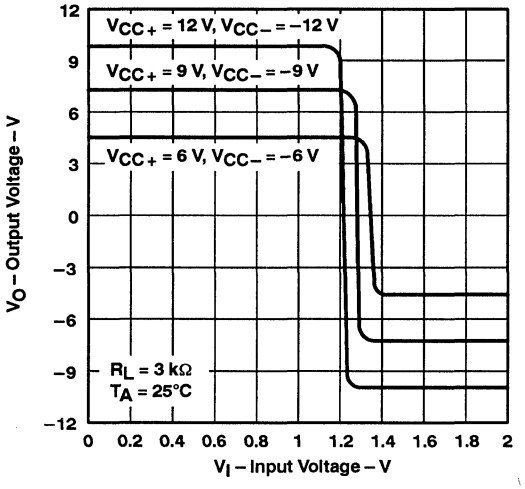


Figure 2

OUPUT CURRENT
vs
OUTPUT VOLTAGE

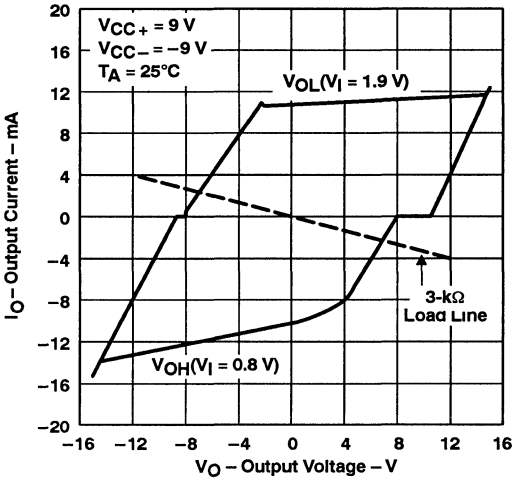


Figure 3

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

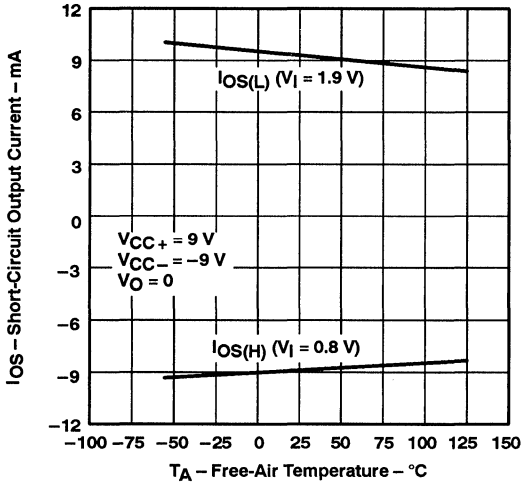


Figure 4

SLEW RATE
vs
LOAD CAPACITANCE

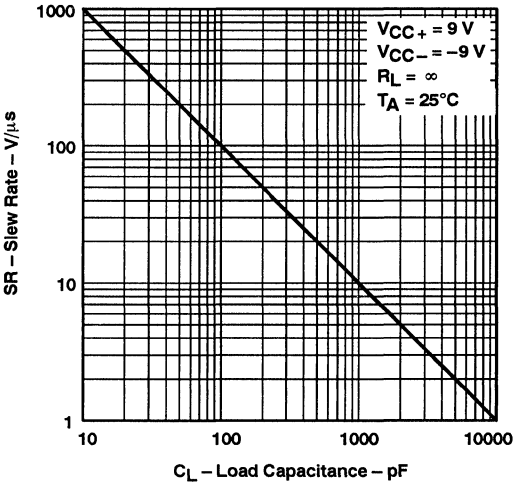


Figure 5

† Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

THERMAL INFORMATION†

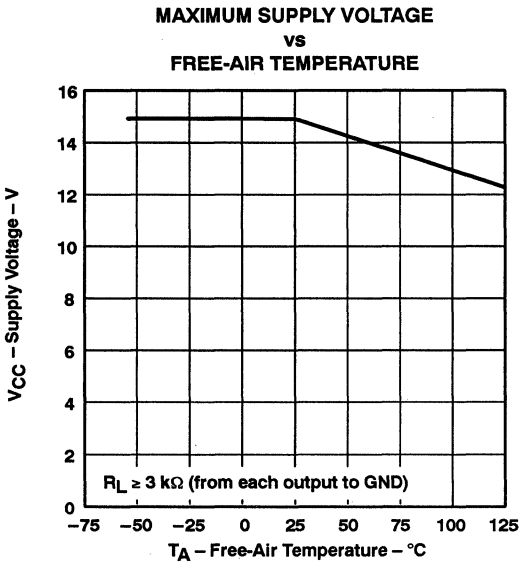


Figure 6

† Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

APPLICATION INFORMATION

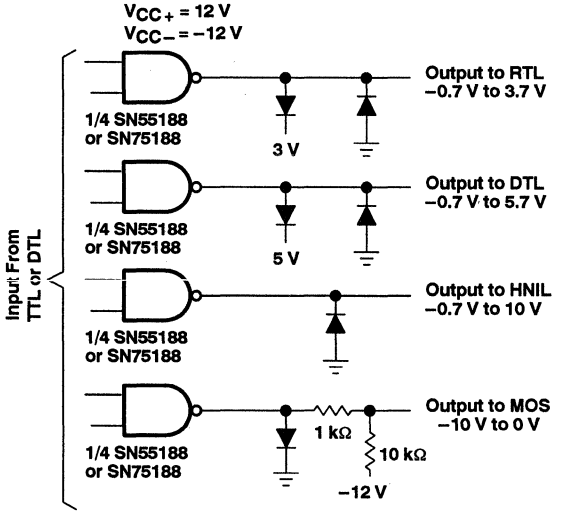


Figure 7. Logic Translator Applications

Diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to ± 15 V and the power supplies are at low and provide low-impedance paths to ground.

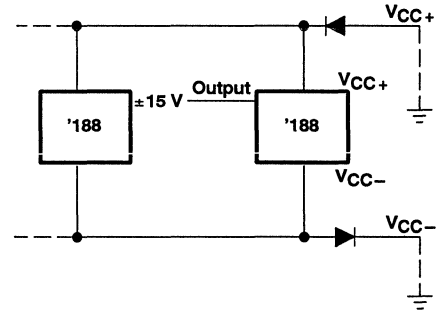
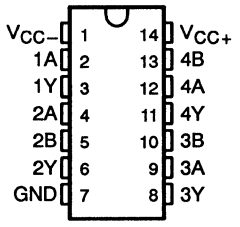


Figure 8. Power Supply Protection to Meet Power-Off Fault Conditions of EIA Standard RS-232-C

- **Bi-MOS Technology With TTL and CMOS Compatibility**
- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Very Low Quiescent Current . . . 95 μA Typ $V_{CC\pm}$ = ±12 V**
- **Current-Limited Output . . . 10 mA Typ**
- **CMOS-and TTL-Compatible Inputs**
- **On-Chip Slew Rate Limited to 30 V/μs max**
- **Flexible Supply Voltage Range**
- **Characterized at $V_{CC\pm}$ of ±4.5 V and ±15 V**
- **Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88**
- **ESD Protection Exceeds 1000 V Per MIL-Std-883C Method 3015**

D, DB†, OR N PACKAGE
(TOP VIEW)



† The DB package is only avalable left-end taped and reeled, i.e., order device SN75C188DBLE.

Function Tables

DRIVER 1

B	Y
H	L
L	H

DRIVERS 2 THRU 4

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level, X = don't care

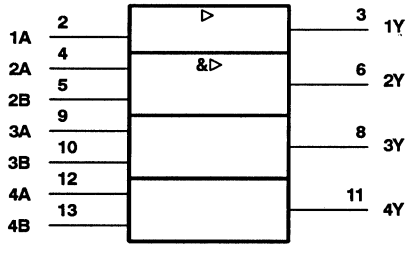
description

The SN65C188 and SN75C188 are monolithic, low-power, quad line drivers that interface data terminal equipment with data communications equipment. These devices are designed to conform to Standard ANSI/EIA-232-D-1986, which supercedes RS-232-C.

An external diode in series with each supply-voltage terminal is needed to protect the SN65C188 and SN75C188 under certain fault conditions to comply with EIA-232-D (refer to Application Information).

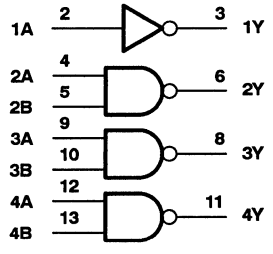
The SN65C188 is characterized for operation from −40°C to 85°C. The SN75C188 is characterized for operation from 0°C to 70°C.

logic symbol†



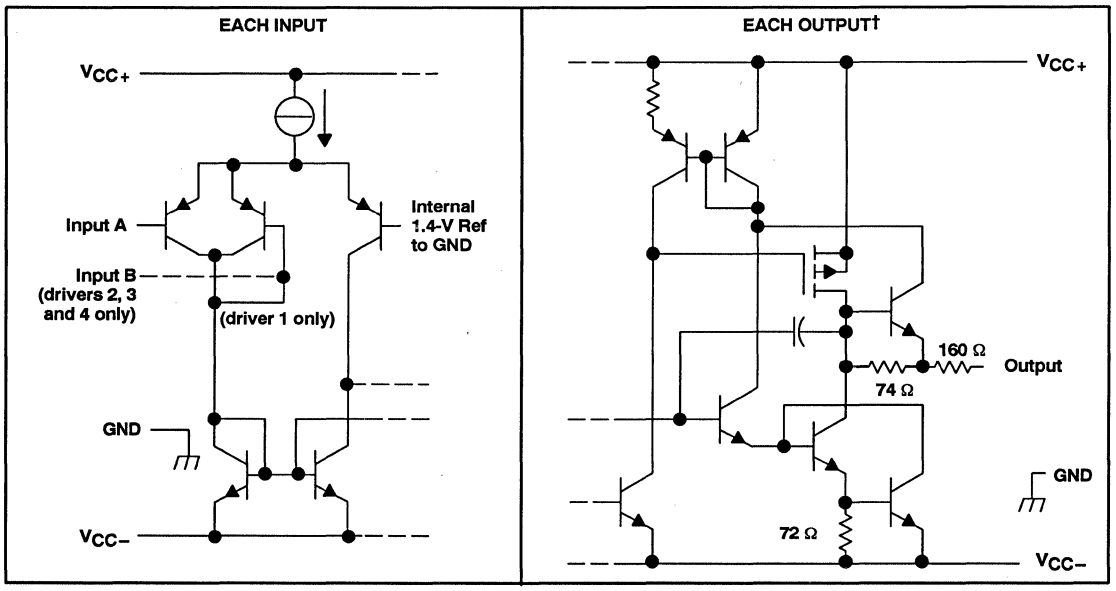
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 thru 4)

schematics of inputs and outputs



† All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} (see Note 1) ..... –15 V
Input voltage range, V_I ..... V_{CC-} to V_{CC+}
Output voltage range, V_O ..... V_{CC-} –6 V to V_{CC+} +6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C188 ..... –40°C to 85°C
SN75C188 ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 in.) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DB	525 mW	4.2 mW/°C	336 mW	273 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.5	12	15	V
Supply voltage, V_{CC-}		−4.5	−12	−15	V
Input voltage, V_I		V_{CC-}+2		V_{CC+}	V
High-level Input voltage, V_{IH}		2			V
Low-level Input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	SN65C188	−40		85	°C
	SN75C188	0		70	

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V	4			V
				V_{CC+} = 12 V, V_{CC-} = −12 V	10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V,	R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V			−4	V
				V_{CC+} = 12 V, V_{CC-} = −12 V			−10	
I_{IH}	High-level input current	V_I = 5 V					10	µA
I_{IL}	Low-level input current	V_I = 0					−10	µA
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{CC-}		−5.5	−10	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{CC+}		5.5	10	19.5	mA
I_{IL}	Output resistance, power off	V_{CC+} = 0 V,	V_{CC-} = 0,	V_I = −2 V to 2 V	300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 5 V, No load	V_{CC-} = −5 V,	All inputs at 2 V or 0.8 V		90	160	µA
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,	All inputs at 2 V or 0.8 V		95	160	
I_{CC-}	Supply current from V_{CC-}	V_{CC+} = 5 V, No load	V_{CC-} = −5 V,	All inputs at 2 V or 0.8 V		−90	−160	µA
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,	All inputs at 2 V or 0.8 V		−95	−160	

† All typical values are at T_A = 25°C.

‡ Not more than one output should be shorted at one time.

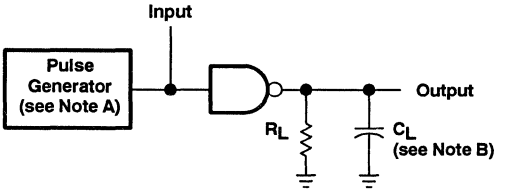
NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if a −4 V is a maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

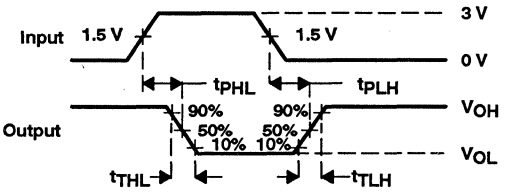
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output†	R_L = 3 kΩ, C_L = 15 pF, See Figure 1			3	µs
t_{PHL}	Propagation delay time, high-to-low-level output†				3.5	µs
t_{TLH}	Transition time, low-to-high-level output‡		0.53		3.2	µs
t_{THL}	Transition time, high-to-low-level output‡		0.53		3.2	µs
t_{TLH}	Transition time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		1.5	3	µs
t_{THL}	Transition time, high-to-low-level output§			1.5	3	µs
SR	Output slew rate§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	6	15	30	V/µs

† Measured at the 50% level
‡ Measured between the 10% and 90% points on the output waveform
§ Measured between the 3 V and −3 V points on the output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHZ, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

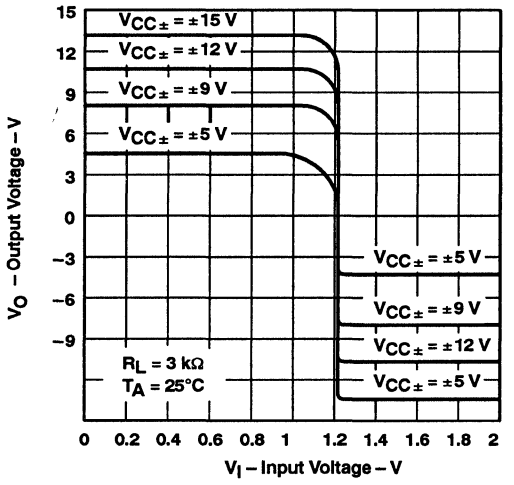


Figure 2

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

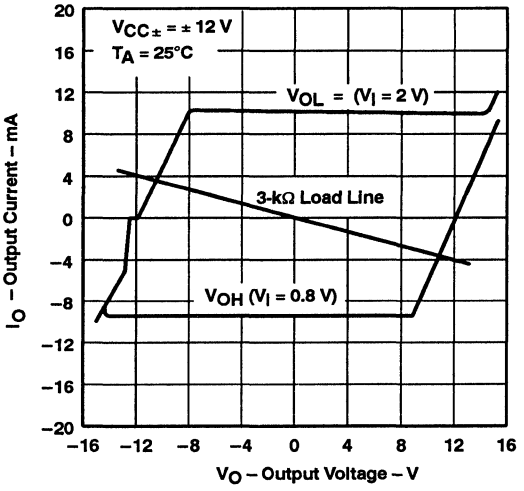


Figure 3

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE†

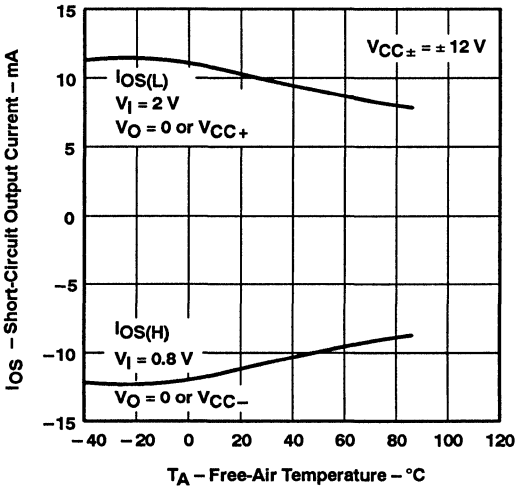


Figure 4

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

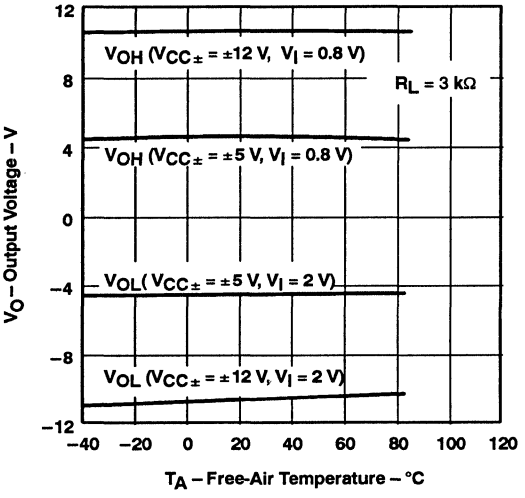


Figure 5

† Only the 0°C to 70°C portion of the curves applies to the SN75C188.

TYPICAL CHARACTERISTICS

INPUT CURRENT vs FREE-AIR TEMPERATURE†

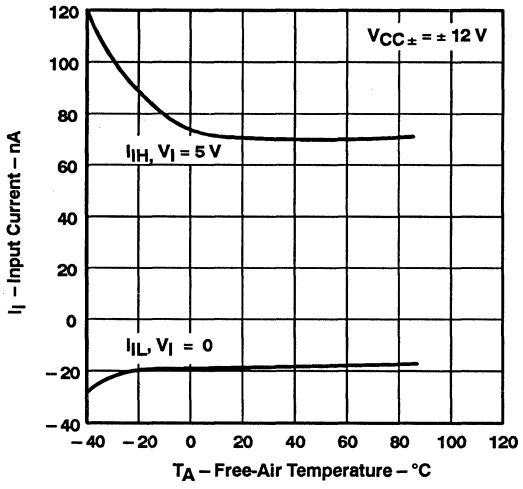


Figure 6

POWER-OFF OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE†

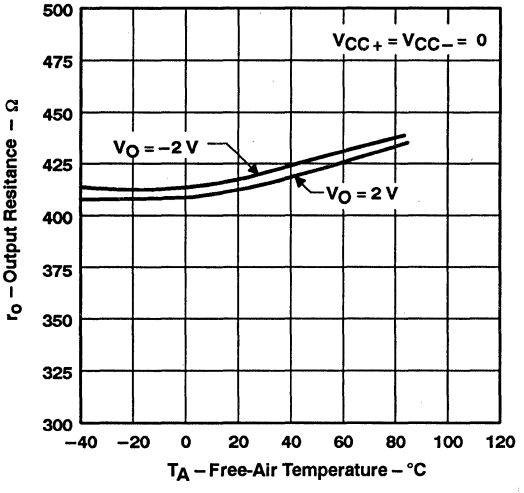


Figure 7

SUPPLY CURRENT vs FREE-AIR TEMPERATURE†

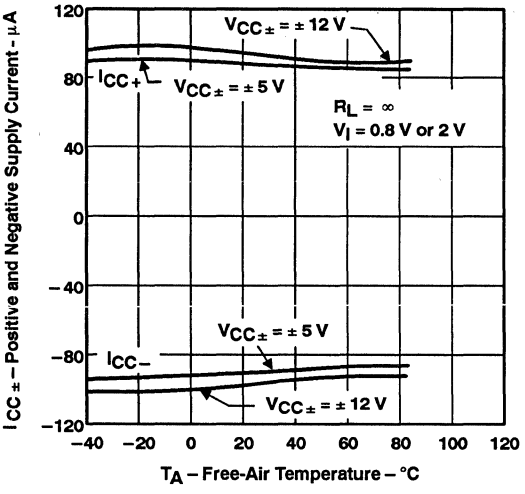


Figure 8

OUTPUT SLEW RATE vs FREE-AIR TEMPERATURE†

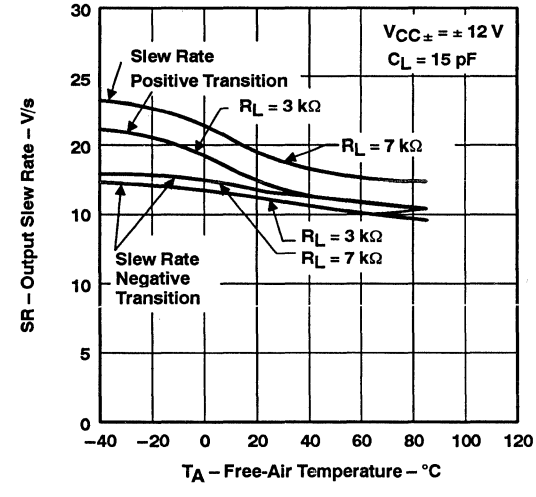


Figure 9

† Only the 0°C to 70°C portion of the curves applies to the SN75C188.

TYPICAL CHARACTERISTICS

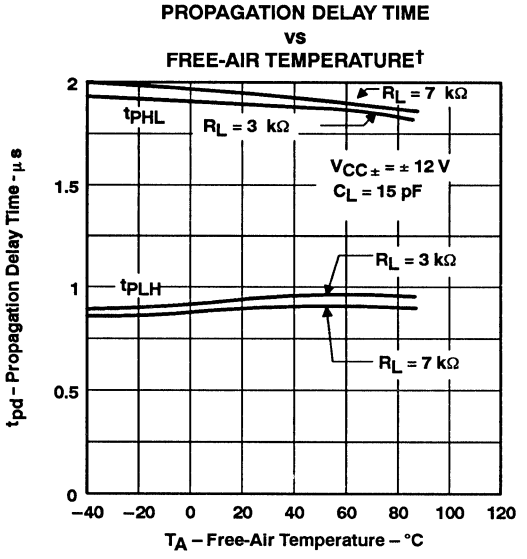


Figure 10

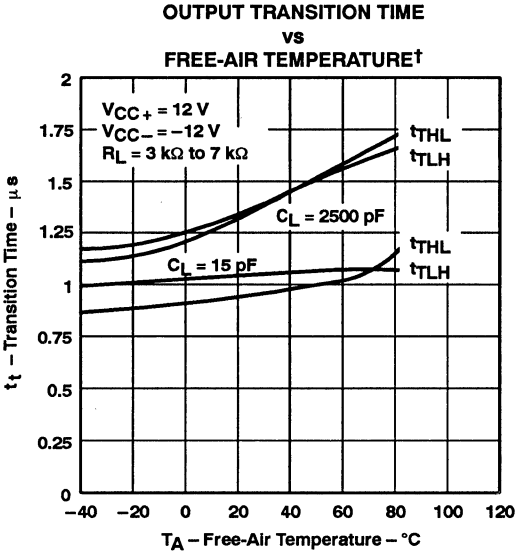


Figure 11

† Only the 0°C to 70°C portion of the curves applies to the SN75C188.

APPLICATION INFORMATION

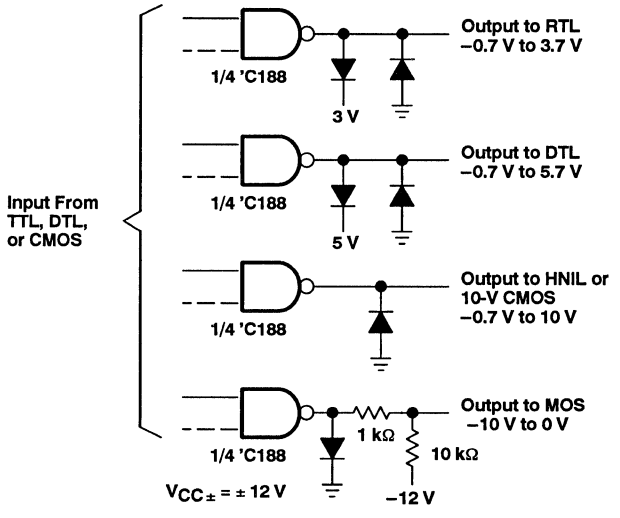
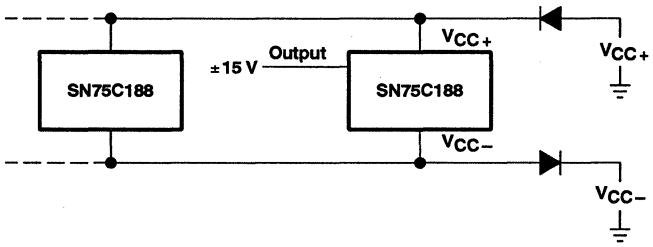


Figure 12. Logic Translator Applications

APPLICATION INFORMATION



NOTE: External diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN75C188 in the fault condition where the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to GND.

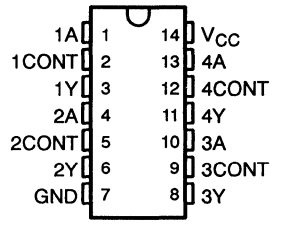
Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA-232-D

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SLLS095A – D1619, SEPTEMBER 1973 – REVISED MARCH 1993

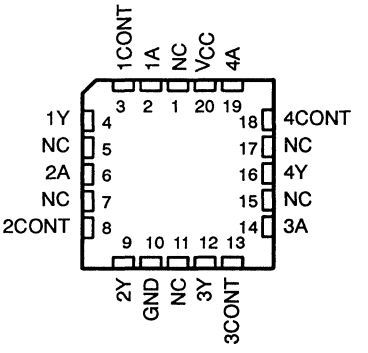
- **Input Resistance . . . 3 kΩ to 7 kΩ**
- **Input Signal Range . . . ±30 V**
- **Operates From Single 5-V Supply**
- **Built-In Input Hysteresis (Double Thresholds)**
- **Response Control Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Satisfies Requirements of EIA RS-232-C**
- **Fully Interchangeable With Motorola MC1489 and MC1489A**

SN55189, SN55189A . . . J OR W PACKAGE
MC1489, MC1489A, SN75189, SN75189A
D, N, OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled and for SN75189, i.e., order SN75189NSLE.

SN55189, SN55189A . . . FK PACKAGE
(TOP VIEW)



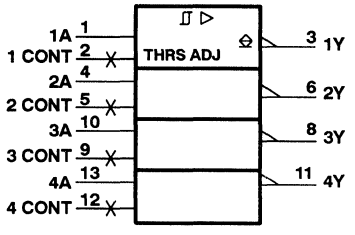
NC – No internal connection

description

These devices are monolithic low-power Schottky quad line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

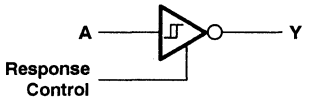
The SN55189 and SN55189A are characterized for operation over the full military temperature range of −55°C to 125°C. The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C.

logic symbol†

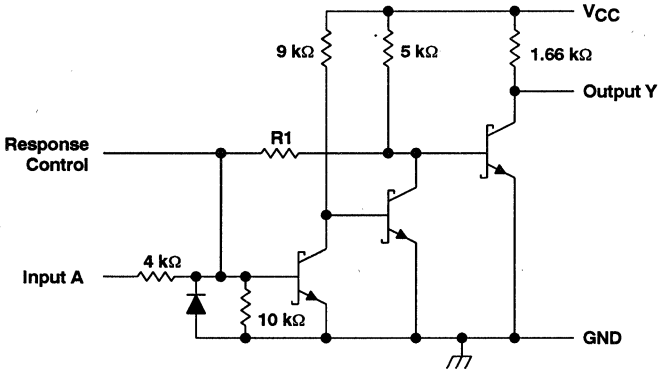


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



schematic (each receiver)



	MC1489 SN55189 SN75189	MC1489A SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55189 SN55189A	MC1489, MC1498A SN75189 SN75189A	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage	±30	±30	V
Output current	20	20	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package		260	°C

NOTE 1: All voltage values are with respect to network ground terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
NS	625 mW	4.0 mW/°C	445 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V ± 1% (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN55189 SN55189A			MC1489, MC1489A SN75189 SN75189A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	1	'89	T_A = 25°C	1	1.3	1.5	1	1.3	1.5	V
				T_A = 0°C to 70°C				0.9		1.6	
				T_A = −55°C to 125°C	0.6		1.9				
			'89A	T_A = 25°C	1.75	1.9	2.25	1.75	1.9	2.25	
				T_A = 0°C to 70°C				1.55		2.25	
				T_A = −55°C to 125°C	1.30		2.65				
V_{T-}	Negative-going threshold voltage	1	'89, '89A	T_A = 25°C	0.75	1.0	1.25	0.75	1.0	1.25	V
				T_A = 0°C to 70°C				0.65		1.25	
				T_A = −55°C to 125°C	0.35		1.6				
V_{OH}	High-level output voltage	1	V_I = 0.75 V, I_{OH} = −0.5 mA		2.6	4	5	2.6	4	5	V
			Input open, I_{OH} = −0.5 mA		2.6	4	5	2.6	4	5	
V_{OL}	Low-level output voltage	1	V_I = 3 V, I_{OL} = 10 mA			0.2	0.45		0.2	0.45	V
I_{IH}	High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
			V_I = 3 V		0.43			0.43			
I_{IL}	Low-level input current	2	V_I = −25 V		−3.6		−8.3	−3.6		−8.3	mA
			V_I = −3 V		−0.43			−0.43			
I_{OS}	Short-circuit output current	3				−3			−3		mA
I_{CC}	Supply current	2	V_I = 5 V, Outputs open			20	26		20	26	mA

† All characteristics are measured with the response control terminal open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	4	R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Propagation delay time, high-to-low-level output		R_L = 390 Ω		25	50	
t_{TLH}	Transition time, low-to-high-level output		R_L = 3.9 kΩ		120	175	ns
t_{THL}	Transition time, high-to-low-level output		R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION†

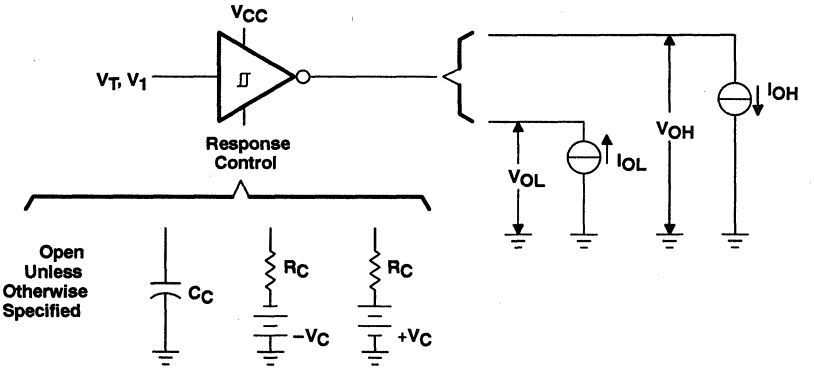
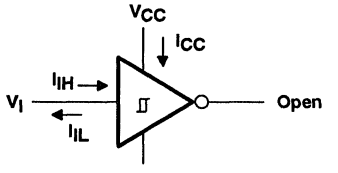


Figure 1. V_{T+}, V_{T-}, V_{OH}, V_{OL}



I_{CC} is tested for all four receivers simultaneously.

Figure 2. I_{IH}, I_{IL}, I_{CC}

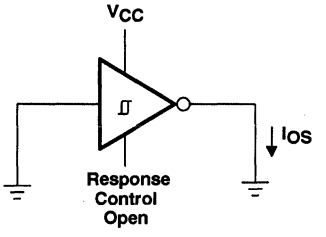
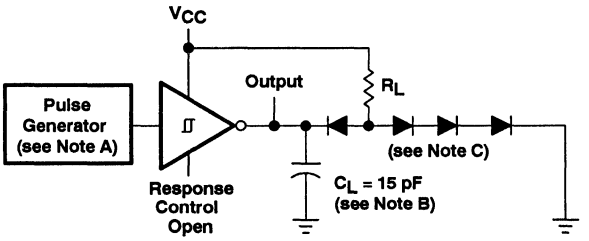


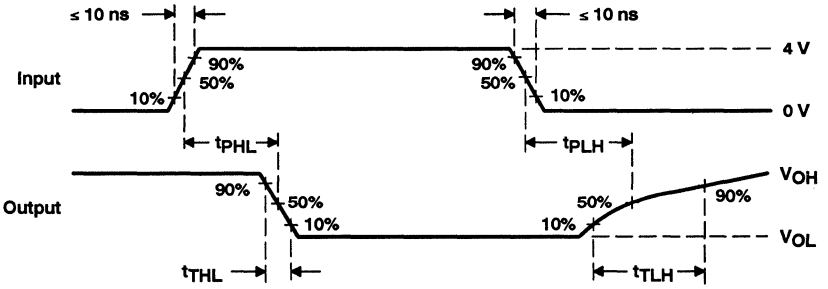
Figure 3. I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 500 ns.
B. C_L includes probe and jig capacitances.
C. All diodes are 1N3064 or equivalent.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE

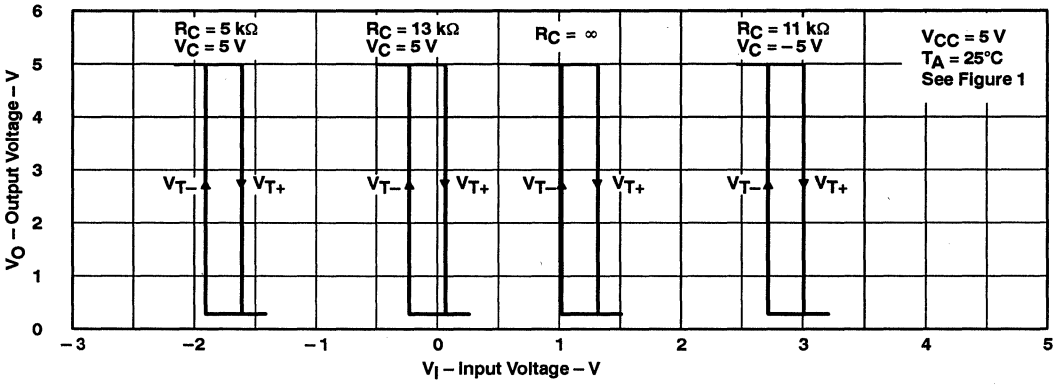


Figure 5

OUTPUT VOLTAGE vs INPUT VOLTAGE

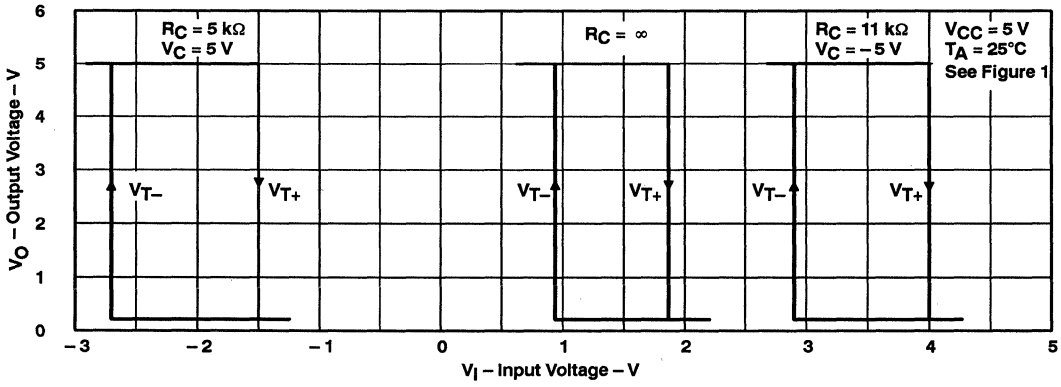


Figure 6

TYPICAL CHARACTERISTICS†

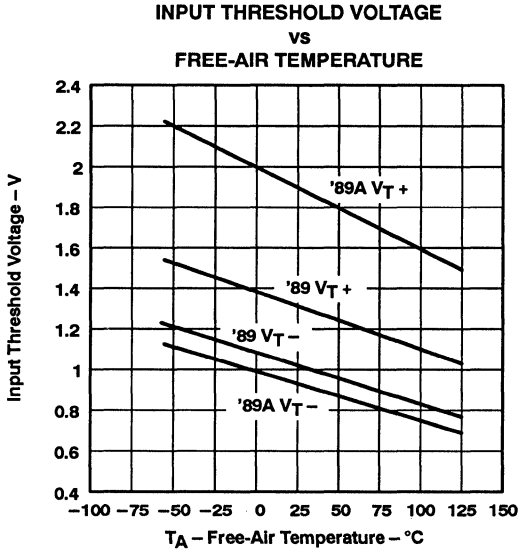


Figure 7

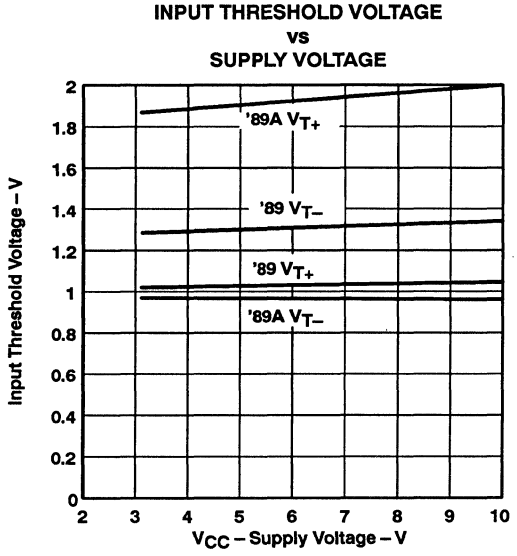


Figure 8

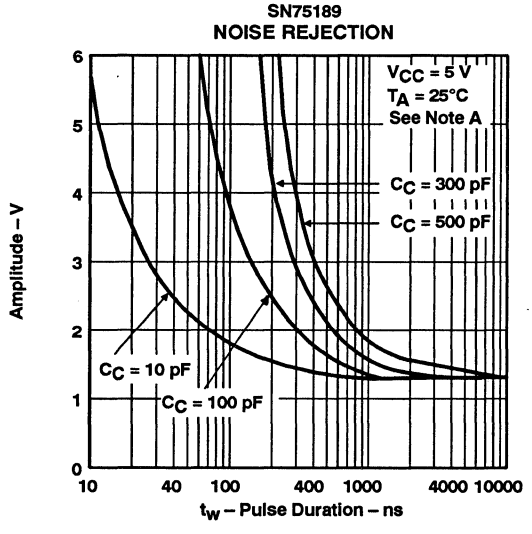


Figure 9

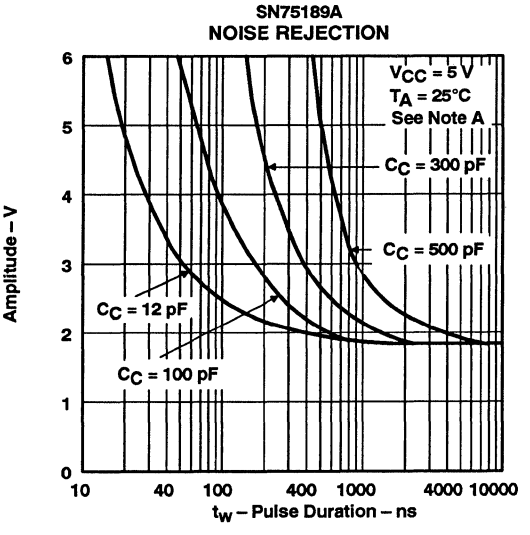


Figure 10

† Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.
NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change of the output level.

TYPICAL CHARACTERISTICS

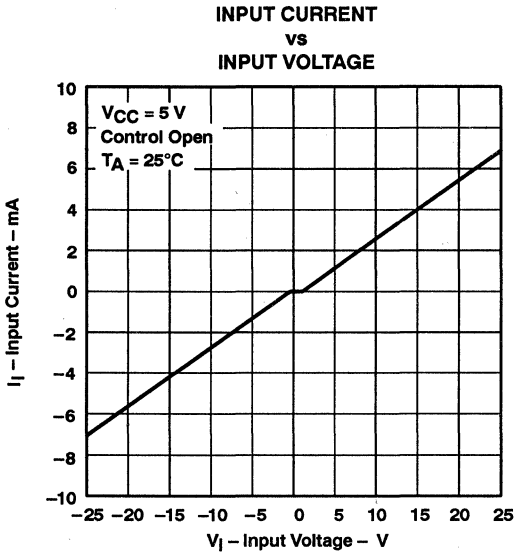
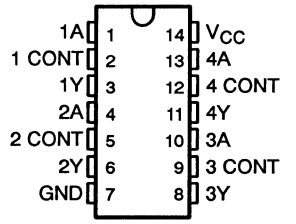


Figure 11

SLLS041C – D3144, OCTOBER 1988 – REVISED MARCH 1993

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Low Supply Current . . . 420 μA Typ**
- **Preset On-Chip Input Noise Filter**
- **Built-in Input Hysteresis**
- **Response and Threshold Control Inputs**
- **Push-Pull Outputs**
- **ESD Protection Exceeds 500 V Per MIL-STD-883C, Method 3015**
- **Functionally Interchangeable and Pin Compatible With Texas Instruments SN75189/SN75189A, Motorola MC1489/MC1489A, and National Semiconductor DS14C88A**

D, DB†, N, OR NS† PACKAGE
(TOP VIEW)



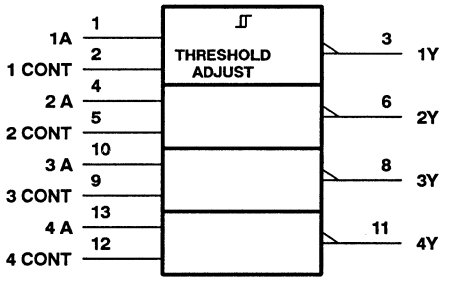
† The DB and NS packages are only available left-end taped and reeled, i.e., order SN_5C189ADBLE or SN_5C189ANSLE.

description

The SN65C189, SN65C189A, SN75C189, and SN75C189A are low-power bipolar quad line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform with Standard ANSI/EIA-232-D-1986, which supersedes RS-232-C.

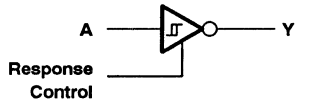
The SN65C189 and SN75C189 have a 0.33 V typical hysteresis compared with 0.97 V for the SN65C189A and SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response control pins. The output is in the high logic state if the input is left open circuited or shorted to ground.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each receiver)

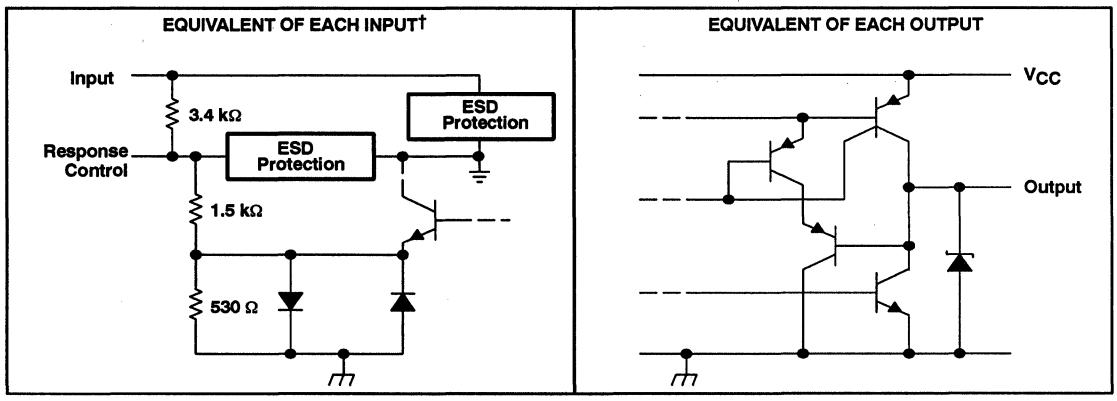


These devices have an on-chip filter that rejects input pulses of shorter than 1-μs minimum duration. An external capacitor may be connected from the control pins to ground to provide further input noise filtering for each receiver.

The SN65C189, SN75C189, SN65C189A, and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers will interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case or for other uses, it is recommended that the SN65C189, SN75C189, SN65C189A, and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C189 and SN65C189A are characterized for operation from −40°C to 85°C. The SN75C189 and SN75C189A are characterized for operation from 0°C to 70°C.

schematic of inputs and outputs



† All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I ..... −30 V to 30 V
Output voltage range ..... −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65C189, SN65C189A ..... −40°C to 85°C
SN75C189, SN75C189A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DB	525 mW	4.2 mW/°C	336 mW	273 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
NS	500 mW	4.0 mW/°C	320 mW	260 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)		−25		25	V
High-level output current, I_{OH}				−3.2	mA
Low-level output current, I_{OL}				3.2	mA
Response control current				±1	mA
Operating free-air temperature, T_A	SN65C189, SN65C189A	−40		85	°C
	SN75C189, SN75C189A	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

electrical characteristics over recommended free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	'C189	See Figure 1		1		1.5	V
		'C189A			1.6		2.25	
V_{T-}	Negative-going threshold voltage	'C189	See Figure 1		0.75		1.25	V
		'C189A			0.75	1	1.25	
V_{hys}	Input hysteresis	'C189	See Figure 1		0.15	0.33		V
		'C189A			0.65	0.97		
V_{OH}	High-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OH} = −20 μA	V_I = 0.75 V,	3.5			V
			V_I = 0.75 V,	I_{OH} = −3.2 mA	2.5			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OL} = 3.2 mA	V_I = 3 V,			0.4	V
I_{IH}	High-level input current		See Figure 2	V_I = 25 V	3.6		8.3	mA
				V_I = 3 V	0.43		1	
I_{IL}	Low-level input current		See Figure 2	V_I = −25 V	−3.6		−8.3	mA
				V_I = −3 V	−0.43		−1	
I_{OS}	Short-circuit output current		See Figure 3				−35	mA
I_{CC}	Supply current		V_I = 5 V, See Figure 2	No load,		420	700	μA

† All typical values are at T_A = 25°C.

NOTE 3: All characteristics are measured with response control terminal open.

switching characteristics, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 5 kΩ, C_L = 50 pF, See Figure 4			6	μs
t_{PHL}	Propagation delay time, high-to-low-level output				6	μs
t_{TLH}	Transition time, low-to-high-level output‡				500	ns
t_{THL}	Transition time, high-to-low-level output‡				300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§		1		6	μs

‡ Measured between 10% and 90% points of output waveform.

§ The intent of this specification is that any input pulse of less than 1 μs will have no effect on the output, and any pulse duration of greater than 6 μs will cause the output to change state twice. Reaction to a pulse duration between 1 μs and 6 μs is uncertain.

PARAMETER MEASUREMENT INFORMATION†

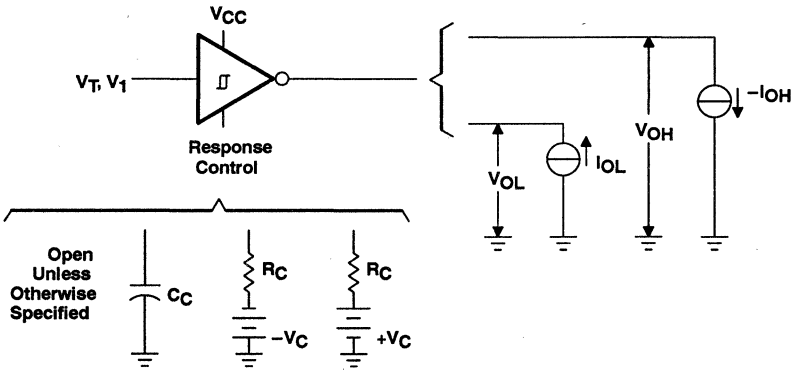


Figure 1. V_{T+}, V_{T-}, V_{OH}, V_{OL}

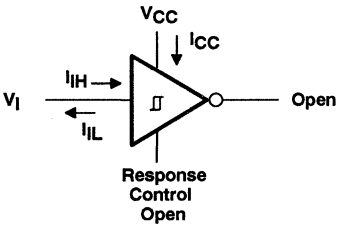


Figure 2. I_{IH}, I_{IL}, I_{CC}

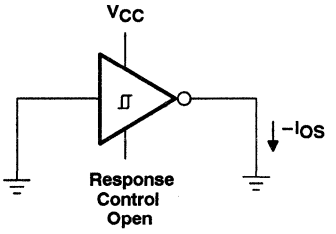


Figure 3. I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
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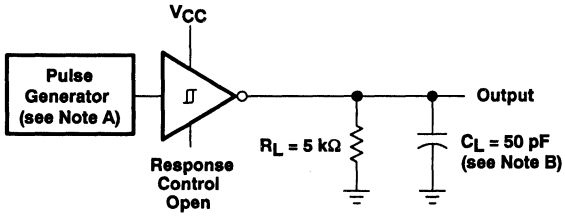
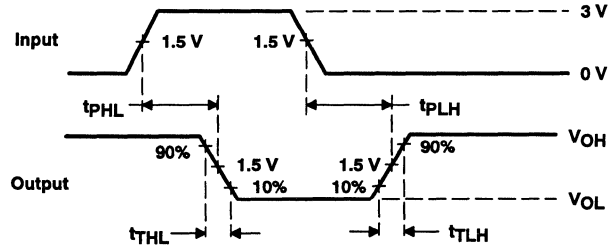
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 25 μs.
B. C_L includes probe and jig capacitances.

TYPICAL CHARACTERISTICS

SN75C189
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE†

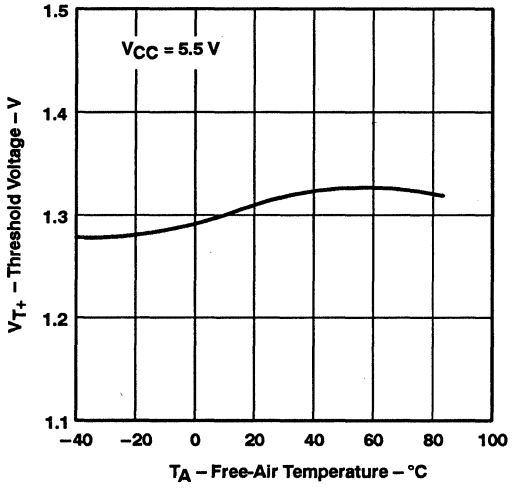


Figure 5

SN75C189A
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE†

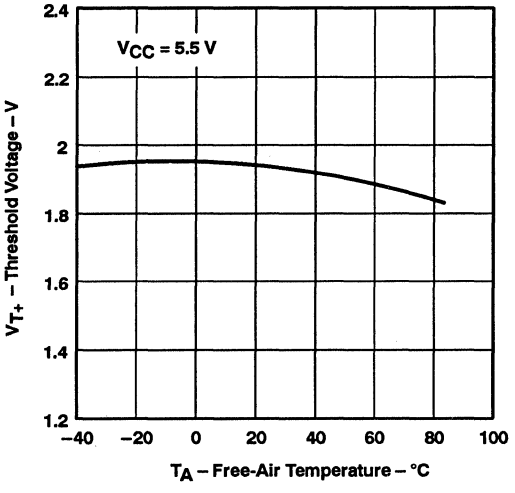


Figure 6

SN75C189
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE†

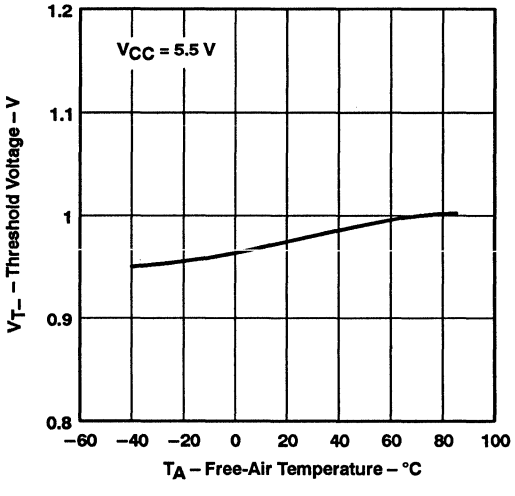


Figure 7

SN75C189A
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE†

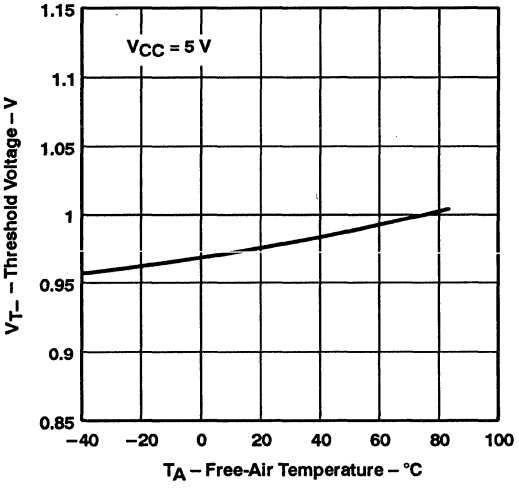


Figure 8

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

**SN75C189
INPUT HYSTERESIS
vs
FREE-AIR TEMPERATURE†**

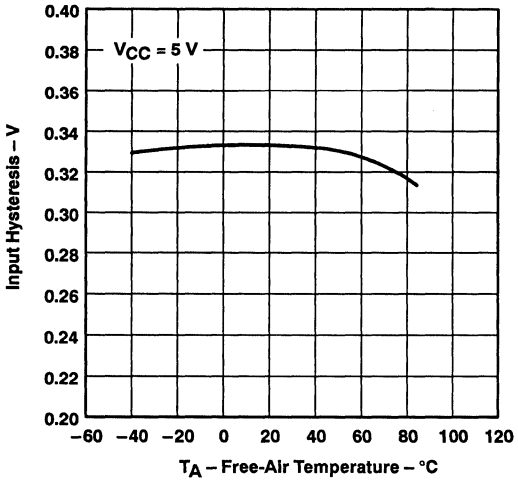


Figure 9

**SN75C189A
INPUT HYSTERESIS
vs
FREE-AIR TEMPERATURE†**

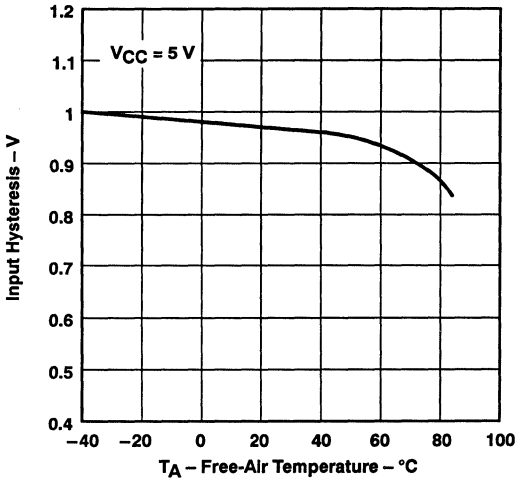


Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†**

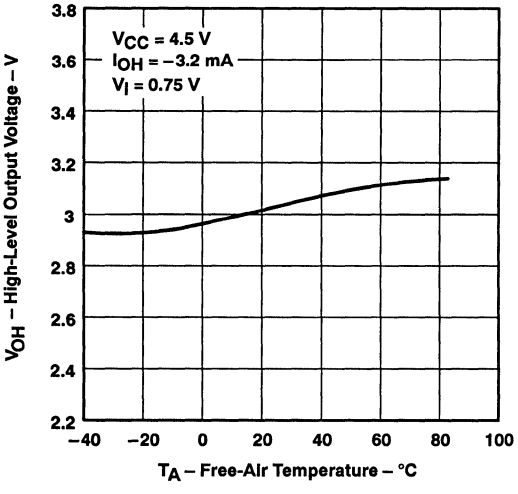


Figure 11

**LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†**

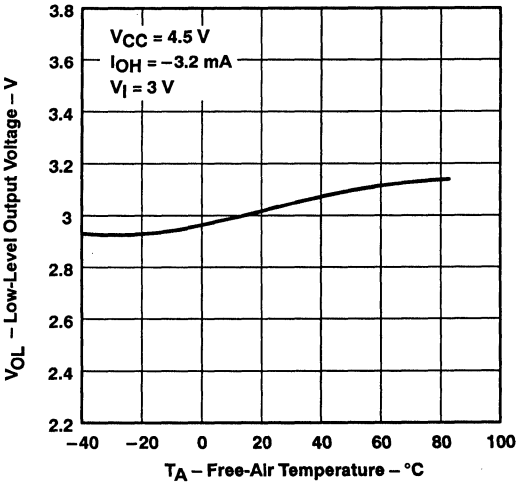


Figure 12

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

**SN75C189
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†**

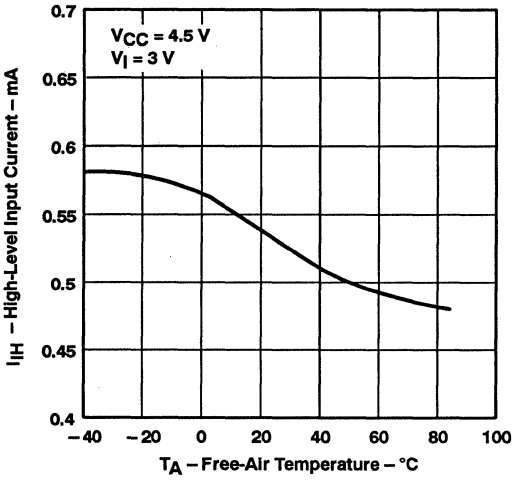


Figure 13

**SN75C189A
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†**

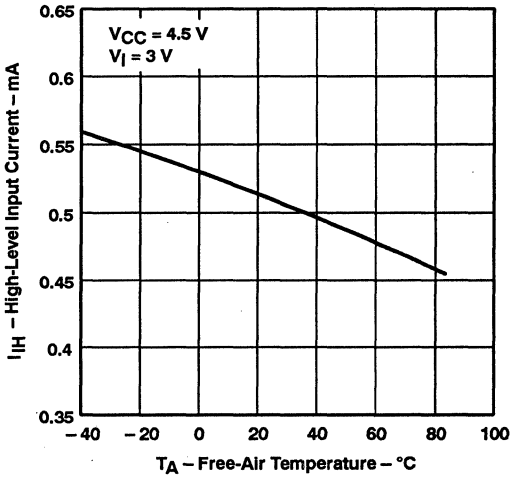


Figure 14

**SN75C189
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†**

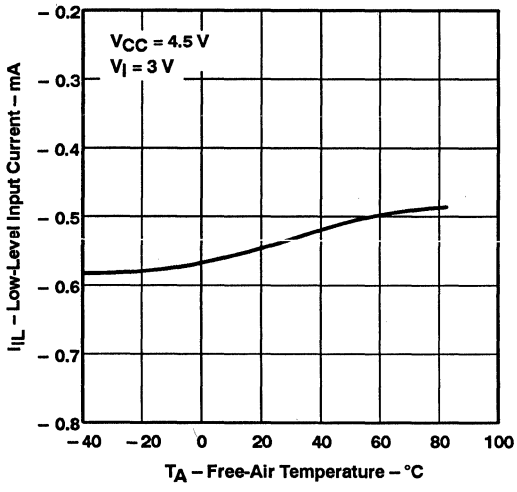


Figure 15

**SN75C189A
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†**

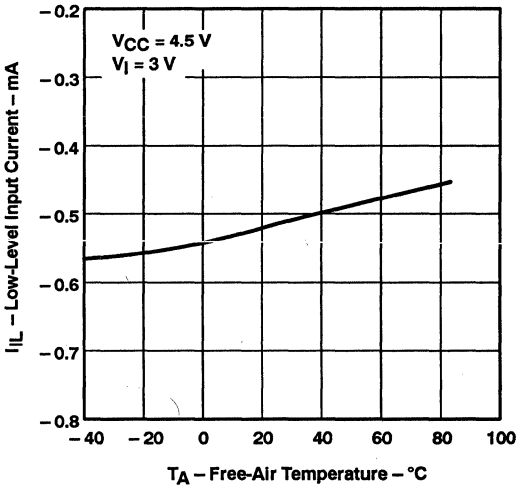


Figure 16

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

HIGH-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE†

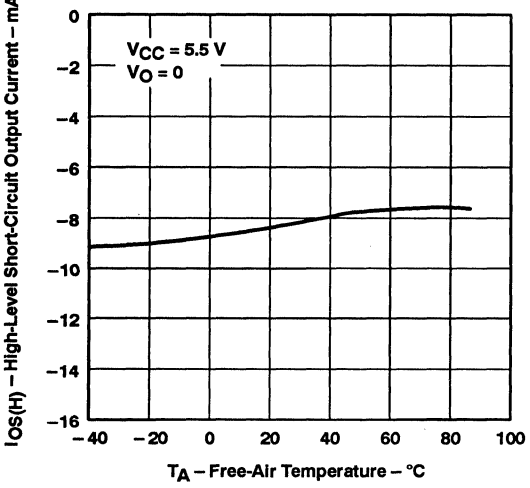


Figure 17

LOW-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE†

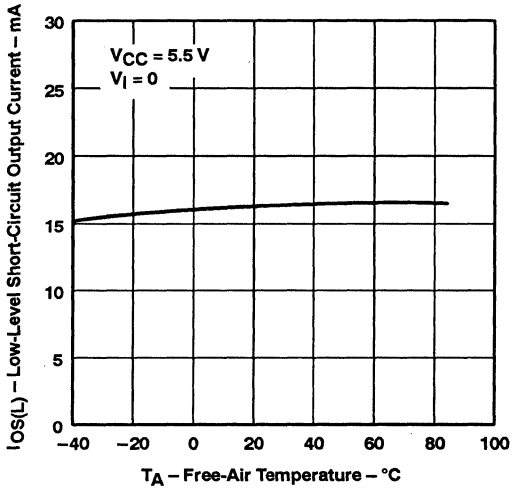


Figure 18

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE†

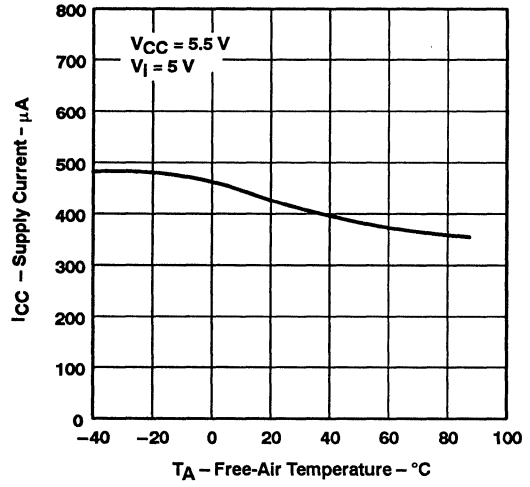


Figure 19

PROPAGATION DELAY TIME,
LOW-TO-HIGH LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†

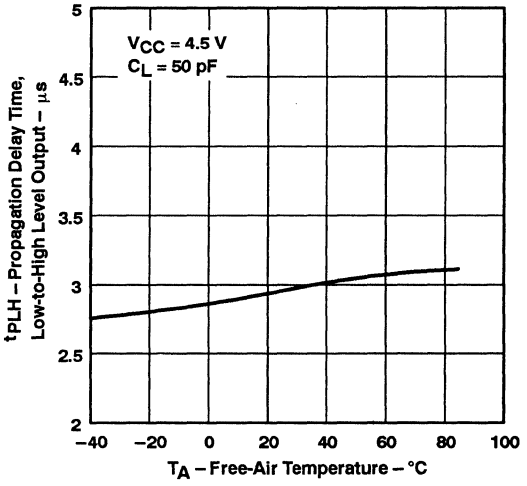


Figure 20

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†

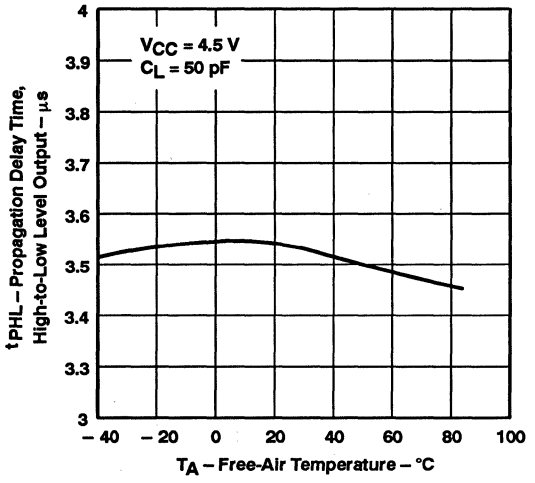


Figure 21

TRANSITION TIME,
LOW-TO-HIGH-LEVEL
vs
FREE-AIR TEMPERATURE†

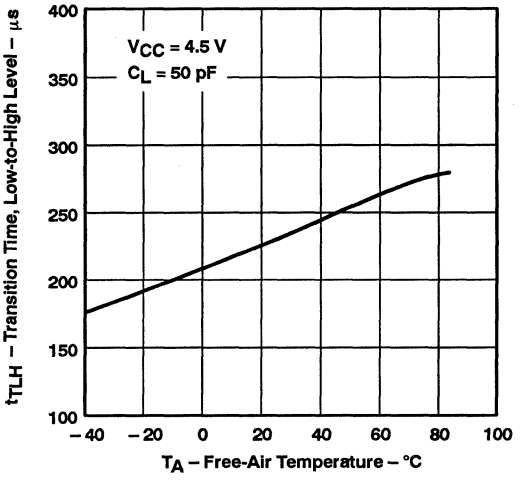


Figure 22

TRANSITION TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†

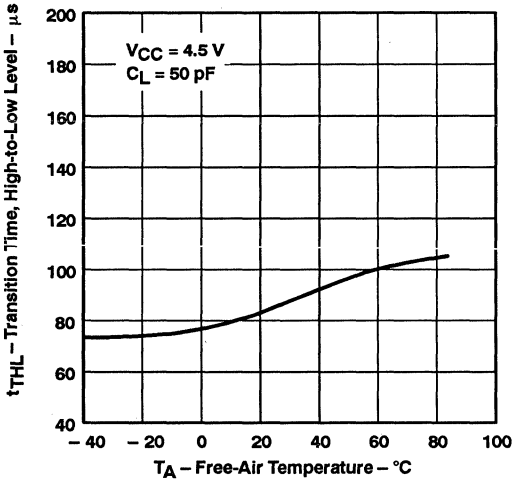


Figure 23

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

SLLS032A – D3068, DECEMBER 1987 – REVISED AUGUST 1989

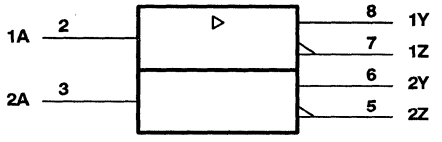
- **Meets EIA Standard RS-422-A**
- **High Speed, Low-Power ALS Design**
- **TTL-and CMOS-Input Compatibility**
- **Single 5-V Supply Operation**
- **Output Short-Circuit Protection**
- **Improved Replacement for the uA9638**

description

The SN75ALS191 is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in 8-pin packages.

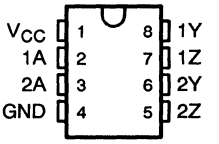
The SN75ALS191 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

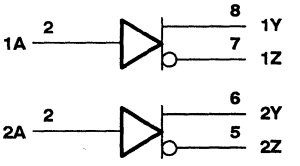
D OR P PACKAGE
(TOP VIEW)



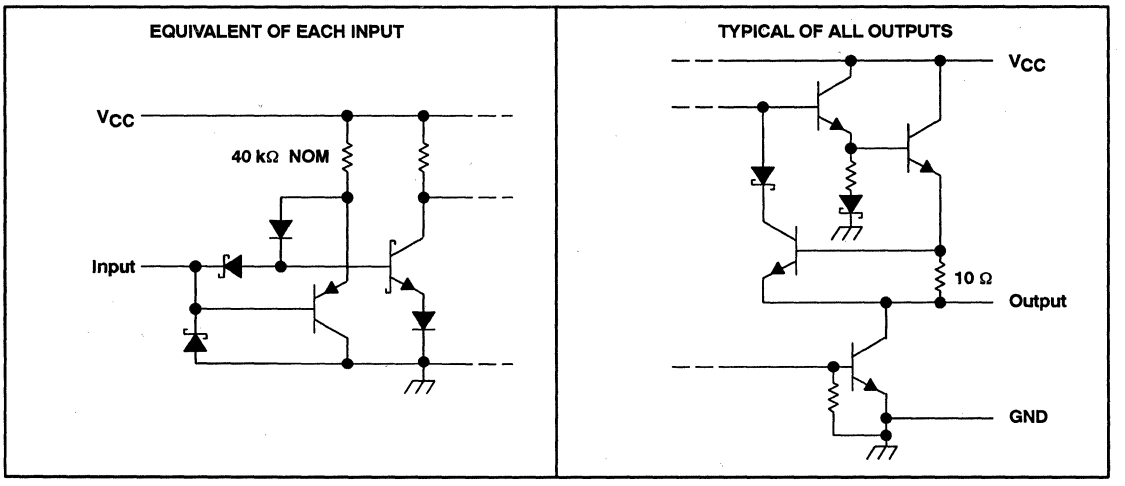
FUNCTION TABLE
(each driver)

INPUT	OUTPUTS	
A	Y	Z
H	H	L
L	L	H

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA				−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.5	3.3		
				I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 40 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0					2 V_{OD2}	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, See Figure 1		R_L = 100 Ω,	2			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡						±0.4	V
V_{OC}	Common-mode output voltage§						3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡						±0.4	V
I_O	Output current with power off	V_{CC} = 0		V_O = 6 V		0.1	100	μA
				V_O = −0.25 V		−0.1	−100	
				V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V					50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V					25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V					200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0			−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V, No load,		All inputs at 0 V		32	40	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $|V_{OD}|$ and $|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP#	MAX	UNIT
t_{dD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		3.5	7	ns
t_{tD}	Differential-output transition time			3.5	7	ns
	Skew			1.5	4	ns

Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

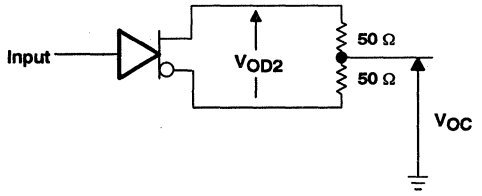
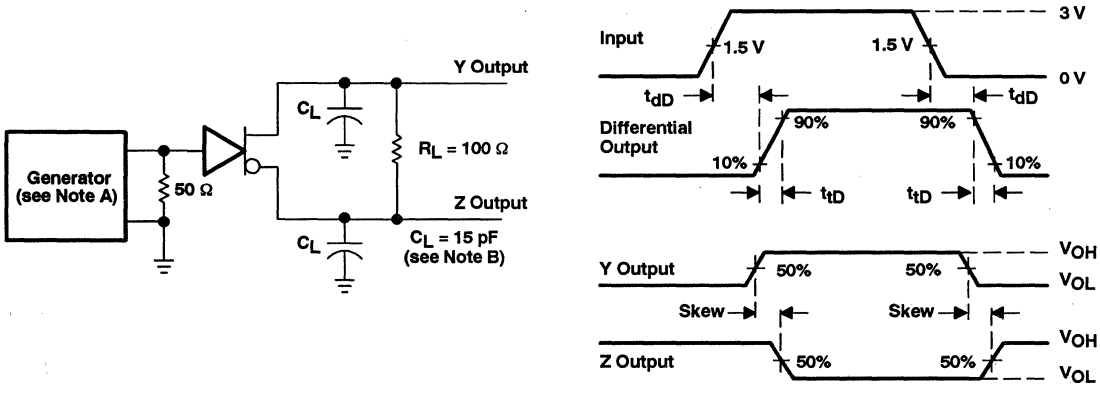


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

SLLS007B – D2904, JULY 1985 – REVISED MARCH 1993

- **Meets EIA Standard RS-422-A**
- **High-Speed, Low-Power ALS Design**
- **3-State TTL Compatible**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Complementary Output Enable Inputs**
- **Improved Replacement for the AM26LS31**

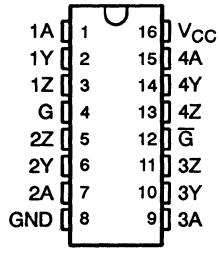
description

These quad differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

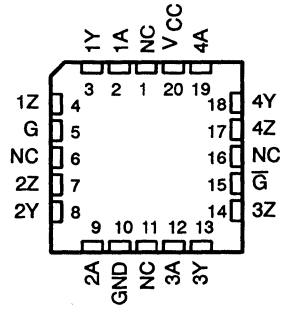
High-impedance inputs maintain input currents low, less than 1 μA for a high level and less than 100 μA for a low level. Complementary enable inputs, G and $\overline{G}$, allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quad line receiver. The SN55ALS192 is also capable of data rates in excess of 20 megabits per second and designed to operate with the SN55ALS193; however, it may be limited to a lower bit rate based on the temperature. Reference should be made to the Dissipation Rating Table and Figure 15.

The SN55ALS192 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75ALS192 is characterized for operation from 0°C to 70°C.

SN55ALS192 . . . J OR W PACKAGE
SN75ALS192 . . . D OR N PACKAGE
(TOP VIEW)



SN55ALS192 . . . FK PACKAGE
(TOP VIEW)



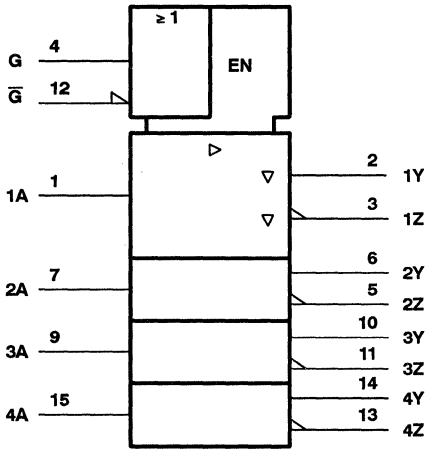
NC – No internal connection

FUNCTION TABLE
(each driver)

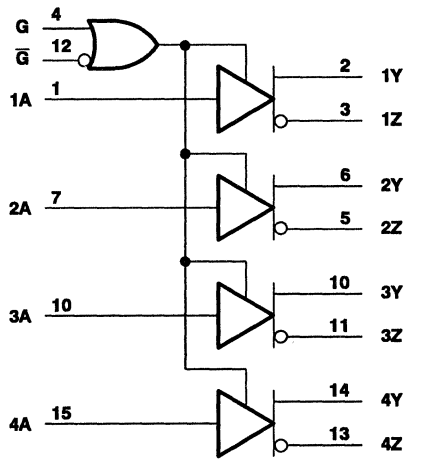
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	$\overline{Z}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
Z = high impedance (off), X = irrelevant

logic symbol†

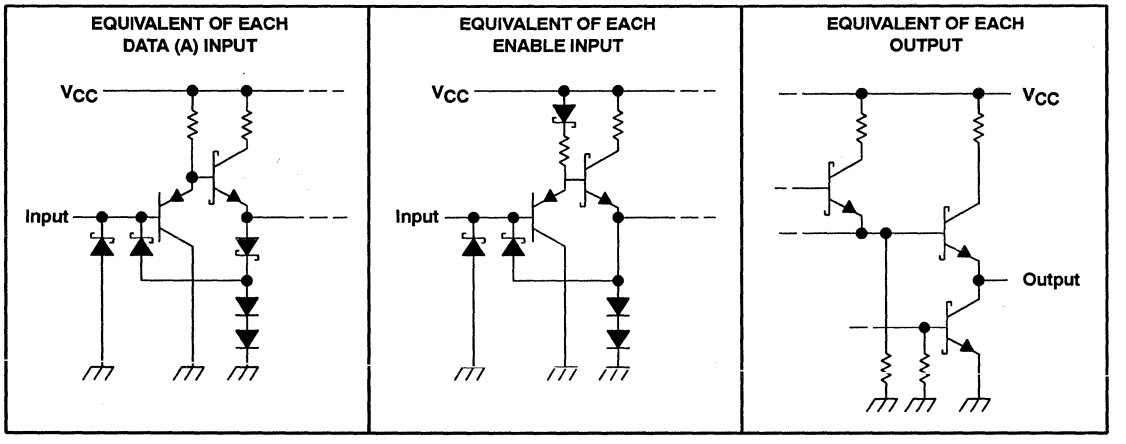


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Off-state output voltage ..... 6 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55ALS192 ..... – 55°C to 125°C
SN75ALS192 ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package ..... 260°C

NOTE 1: All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the J package, the SN55ALS192 chips are either alloy or silver glass mounted.

recommended operating conditions

	SN55ALS192			SN75ALS192			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			– 20			– 20	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55ALS192			SN75ALS192			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = –18 mA				–1.5			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = – 20 mA		2.4			2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA				0.5			0.5	V
V_O	Output voltage	V_{CC} = MAX, I_O = 0		0		6	0		6	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MIN, I_O = 0		1.5		6	1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2 V_{OD1} or 2§			1/2 V_{OD1} or 2§			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage¶	R_L = 100 Ω, See Figure 1				± 0.2			± 0.2	V
V_{OC}	Common-mode output voltage#					± 3			± 3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage¶					± 0.2			± 0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100			100	µA
			V_O = – 0.25 V			–100			–100	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX	V_O = 0.5 V			–20			–20	µA
			V_O = 2.5 V			20			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				– 200			– 200	µA
I_{OS}	Short-circuit output current‖	V_{CC} = MAX		– 30		–150	– 30		– 150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX, All outputs disabled			26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $|V_{OD}|$ and $|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
# In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
‖ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S1 and S2 open, C_L = 30 pF		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14	ns
	Output-to-output skew			3	6	ns
t_{PZH}	Output enable time to high level	S1 open and S2 closed		11	15	ns
t_{PZL}	Output enable time to low level	S1 closed and S2 open		16	20	ns
t_{PHZ}	Output disable time from high level	S1 open and S2 closed, C_L = 10 pF		8	15	ns
t_{PLZ}	Output disable time from low level	S1 and S2 closed, C_L = 10 pF		18	20	ns

PARAMETER MEASUREMENT INFORMATION

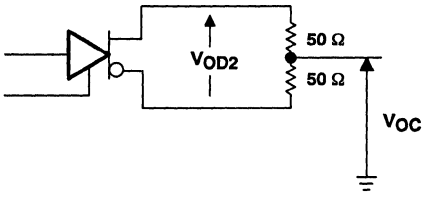
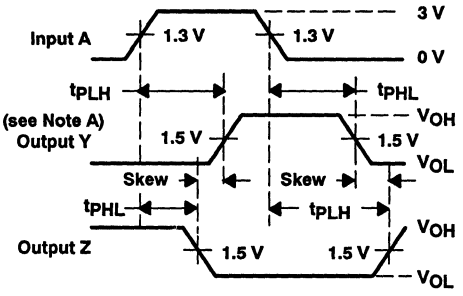
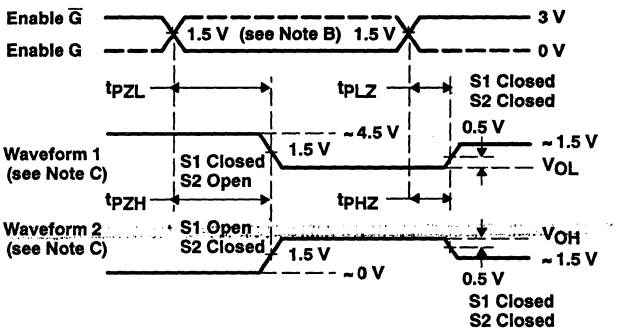


Figure 1. Differential and Common-Mode Output Voltages

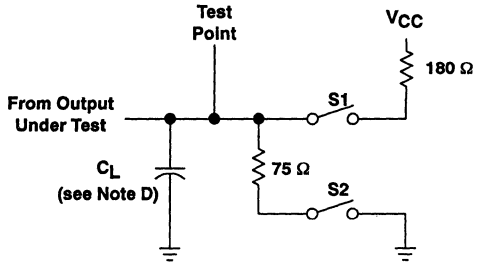


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

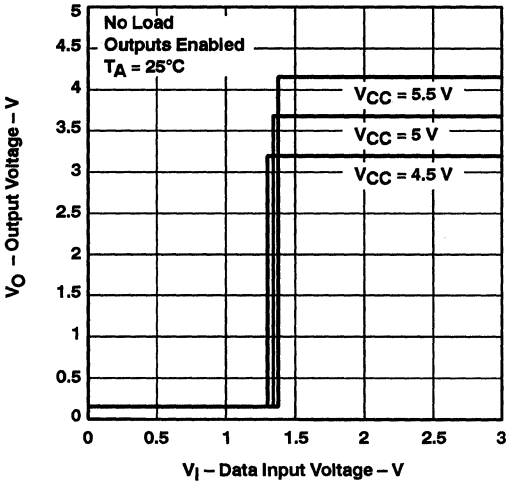


Figure 3

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

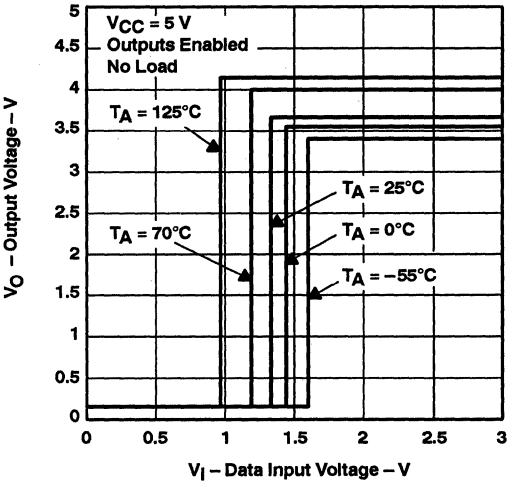


Figure 4

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

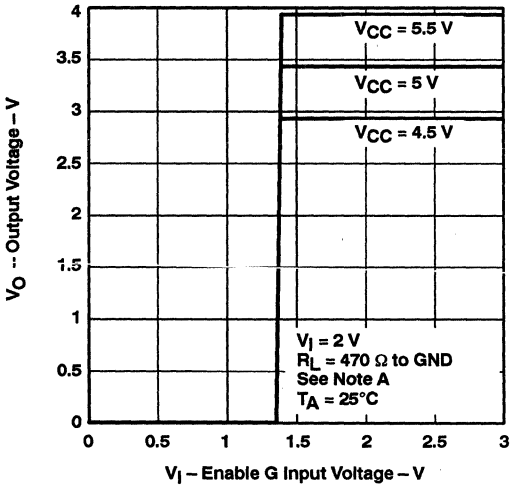


Figure 5

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

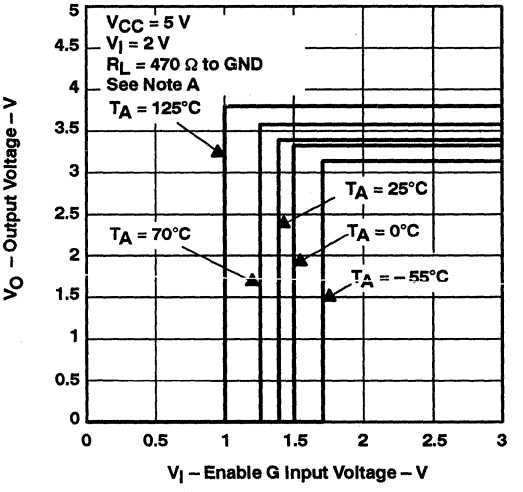


Figure 6

† Data for temperatures below 0°C and above 70°C and below 4.75 V and above 5.25 V, are applicable to SN55ALS192 circuits only.
NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

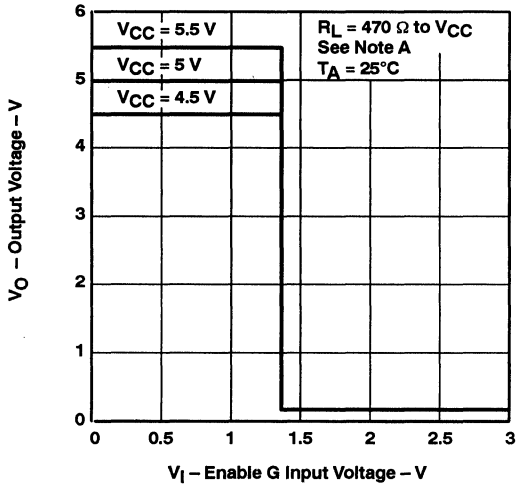


Figure 7

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

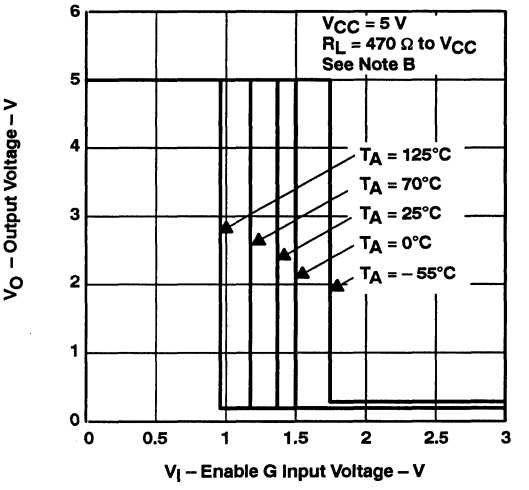


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

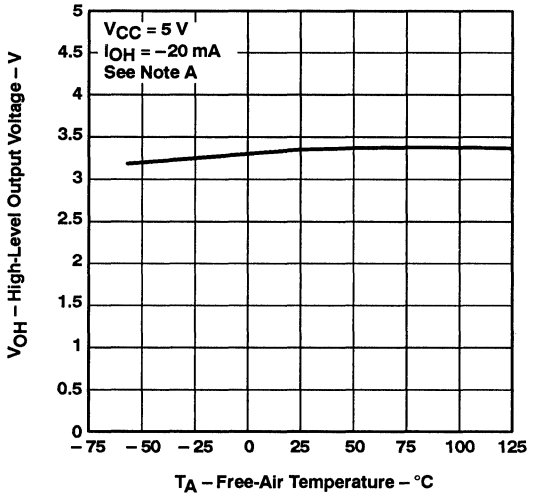


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

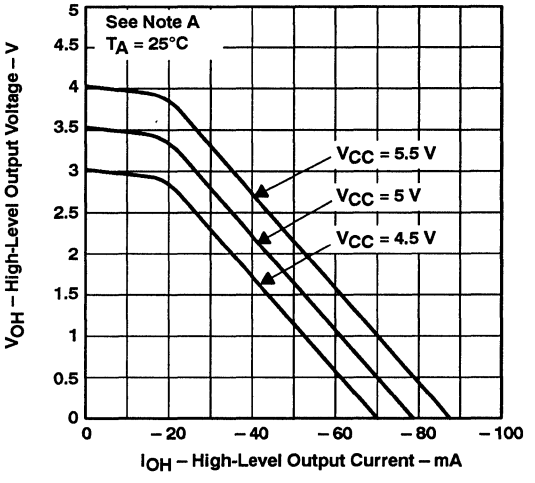


Figure 10

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS192 circuits only.

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
B. The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

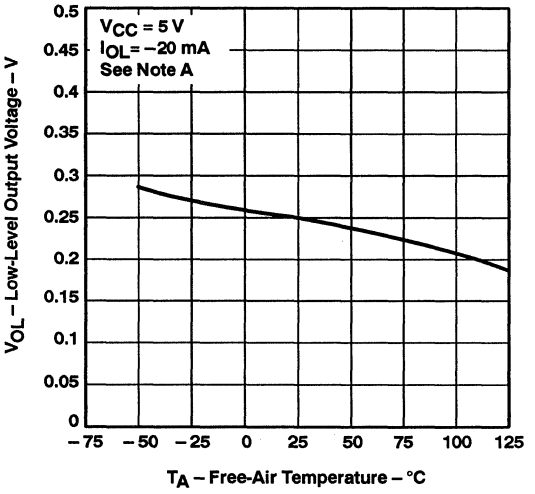


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-OUTPUT CURRENT

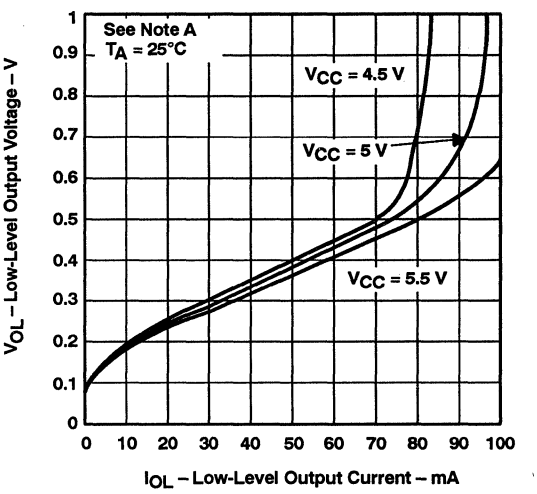


Figure 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

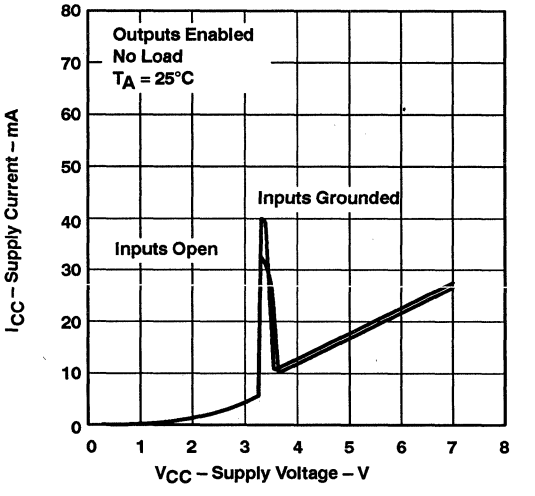


Figure 13

SUPPLY CURRENT
vs
SUPPLY CURRENT

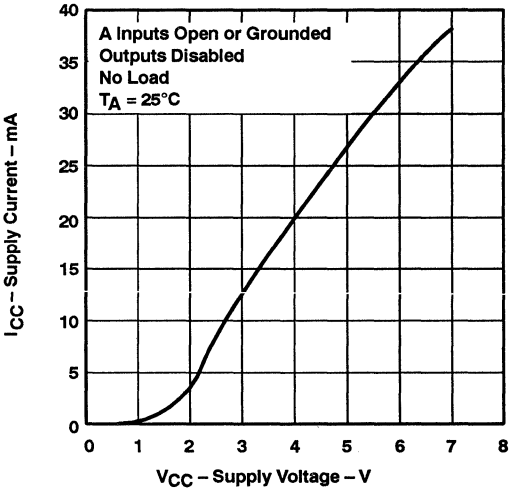


Figure 14

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS192 circuits only.
NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

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TYPICAL CHARACTERISTICS

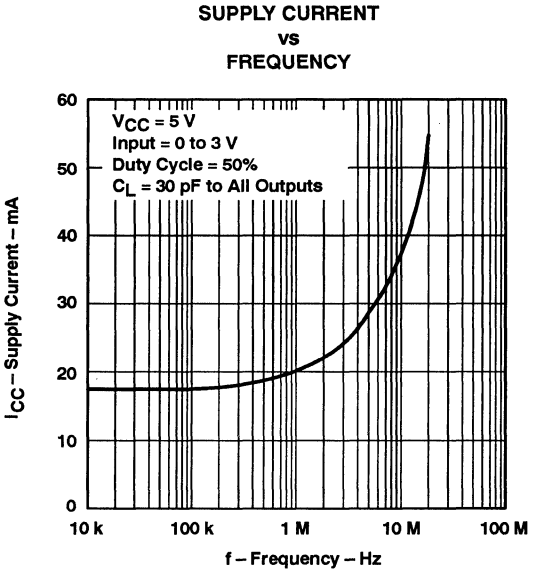
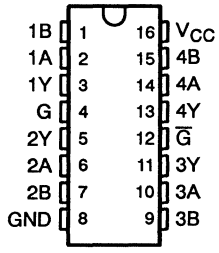


Figure 15

SLLS008C – D2931, JUNE 1986 – REVISED MARCH 1993

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −7 V to 7 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to AM26LS32A**

SN75ALS193 . . . J PACKAGE†
(TOP VIEW)



† For surface-mount package, see the SN75ALS197.

description

The SN75ALS193 is a monolithic quad line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. These devices meet the specifications of EIA Standards RS-422-A and RS-423-A. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high Input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of – 7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the ALS192 quad differential line driver.

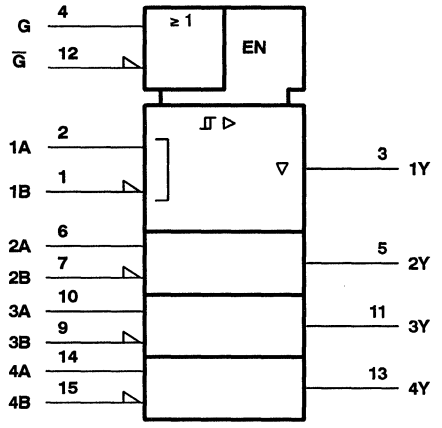
The SN75ALS193 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

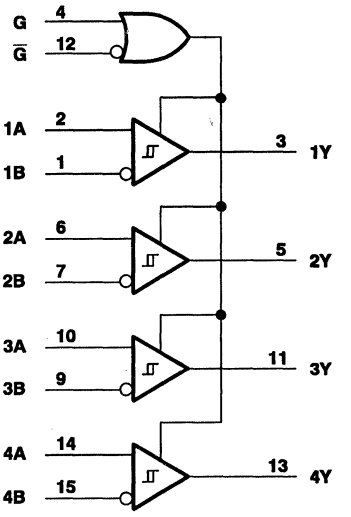
DIFFERENTIAL INPUTS	ENABLES		OUTPUT
A – B	G	$\overline{G}$	Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate
Z = high impedance (off)

logic symbol†

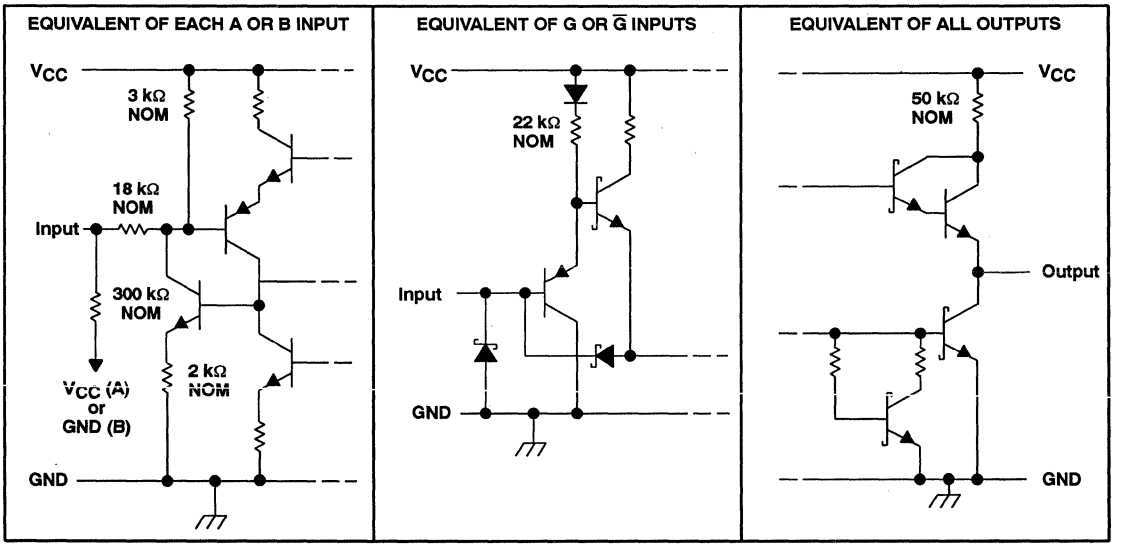


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds ..... 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditons is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the, corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW	N/A

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage					200	mV
V_{T-}	Negative-going threshold voltage			−200§			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −400 μA,	V_{ID} = 200 mV, See Figure 1	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_{CC} = MIN, V_I = 15 V		0.7	1.2	mA
			V_{CC} = MIN, V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V			20	μA
			V_{IH} = MAX			100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0,	V_{ID} = 3 V, See Note 4	−15	−78	−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled		22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
NOTES: 3. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V, C_L = 15 pF,	See Figure 2		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 3		13	25	
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

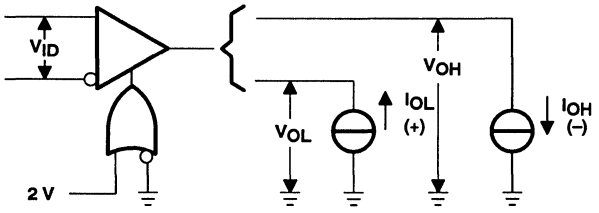
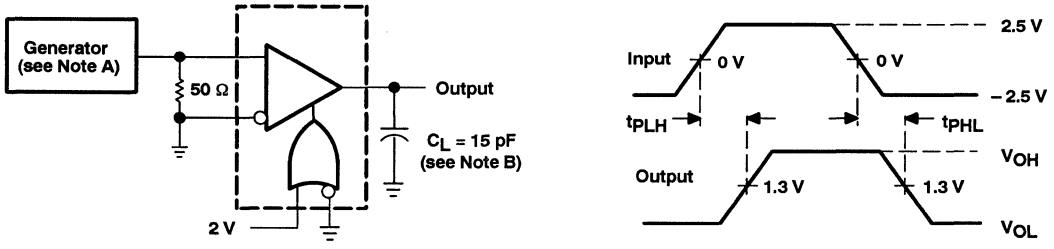


Figure 1. V_{OH}, V_{OL}

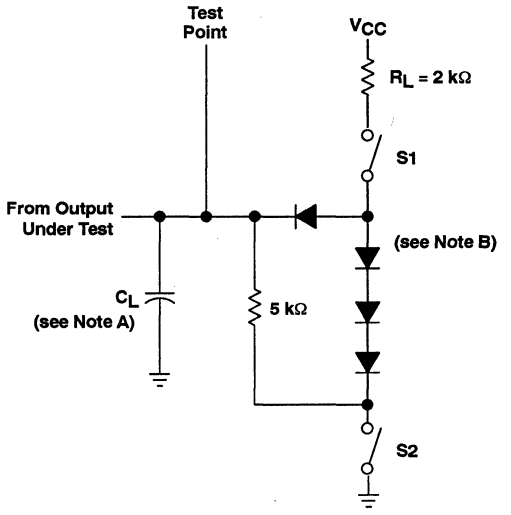


TEST CIRCUIT **VOLTAGE WAVEFORMS**

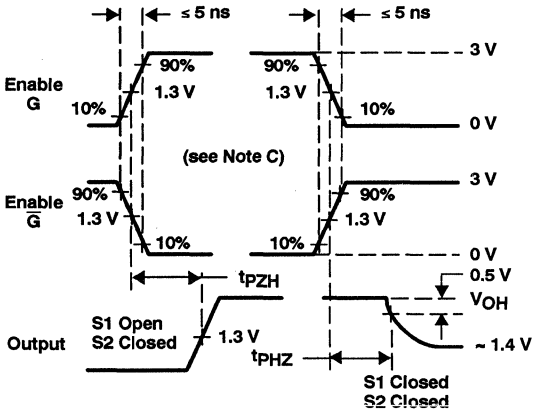
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

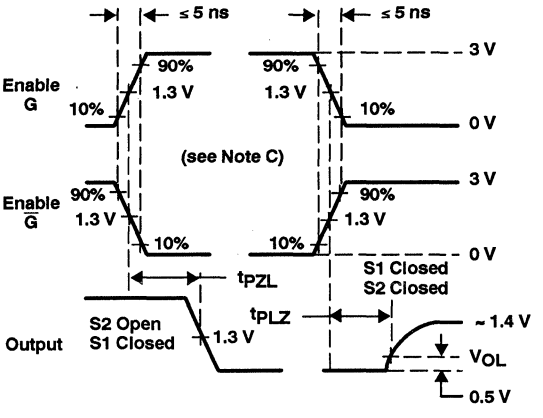
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

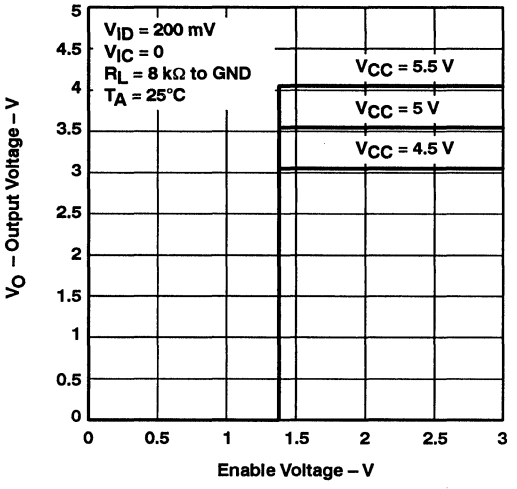


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

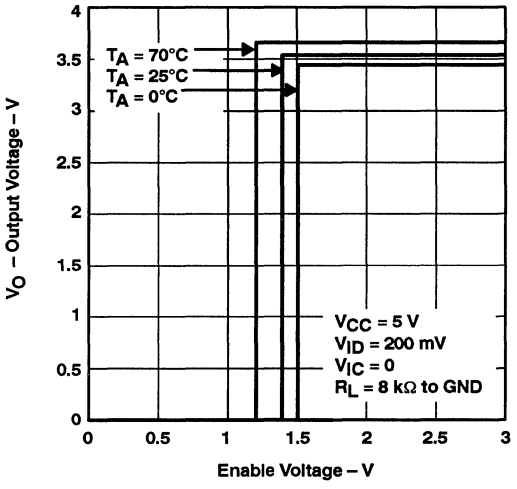


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

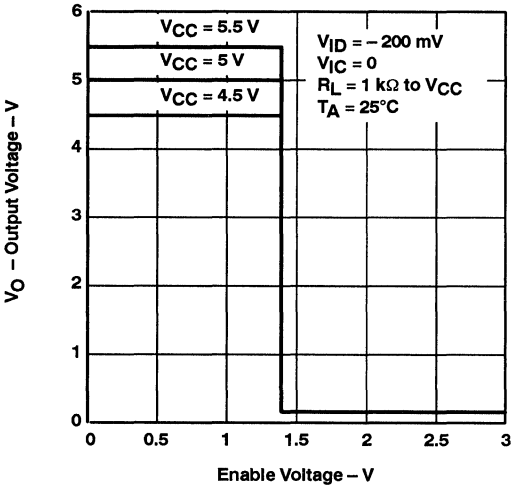


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

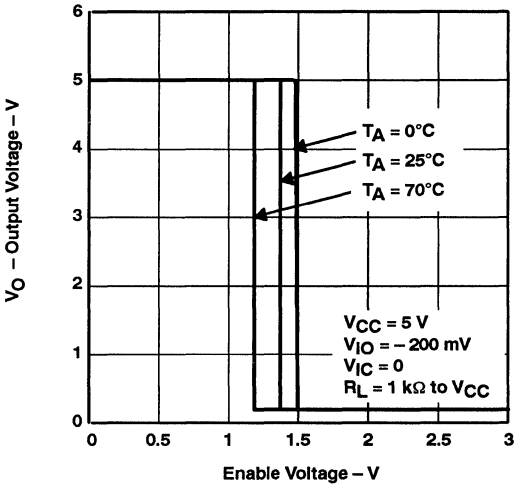


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

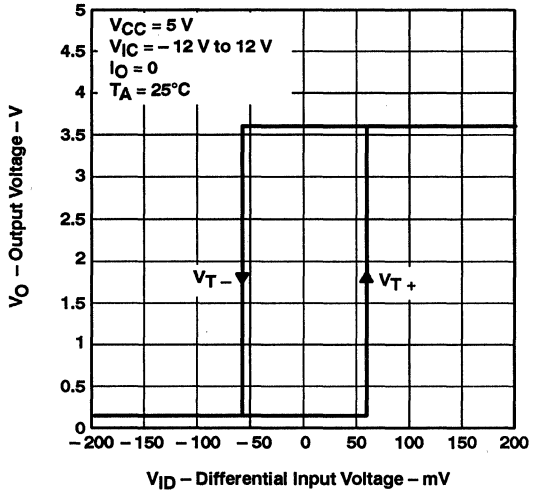


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

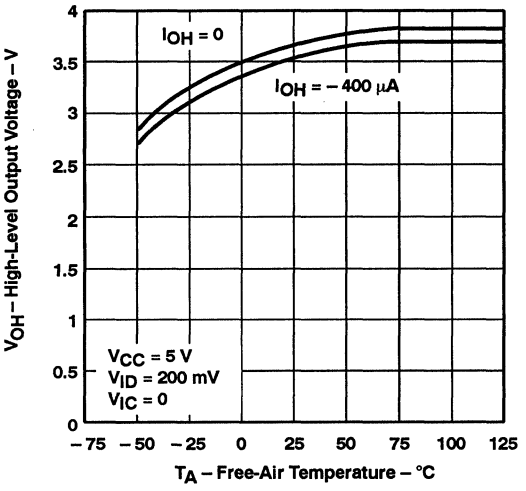


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

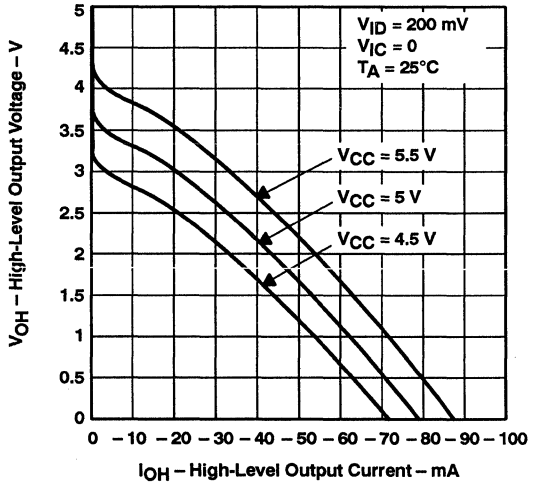


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

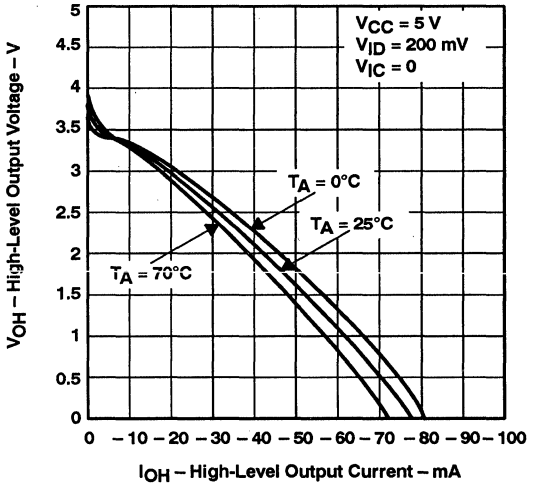


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

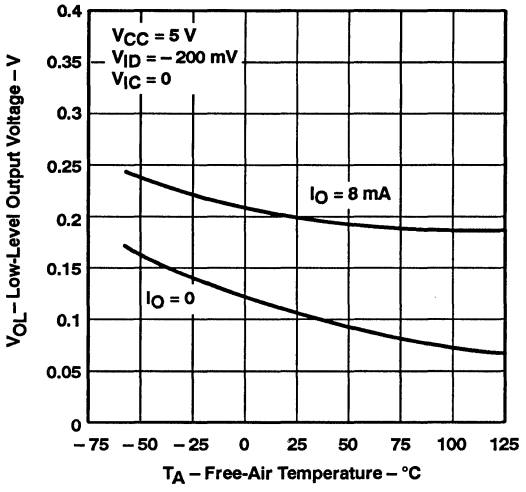


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

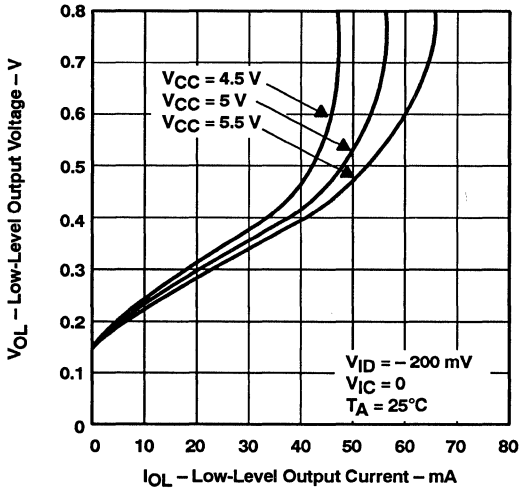


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

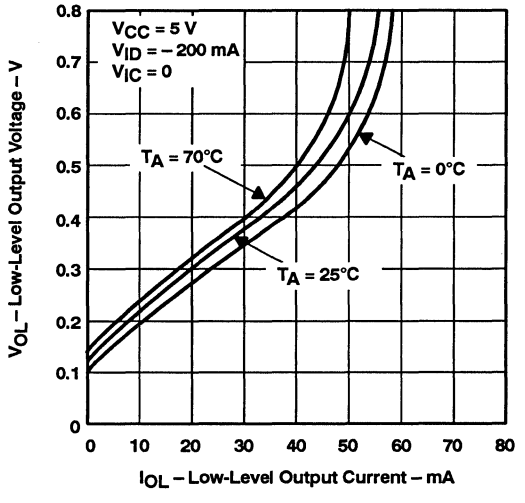


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

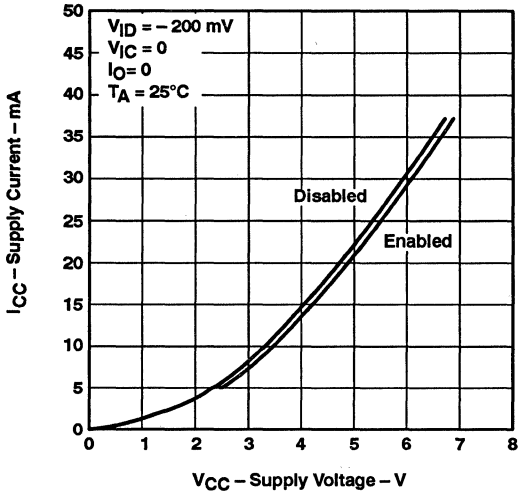


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

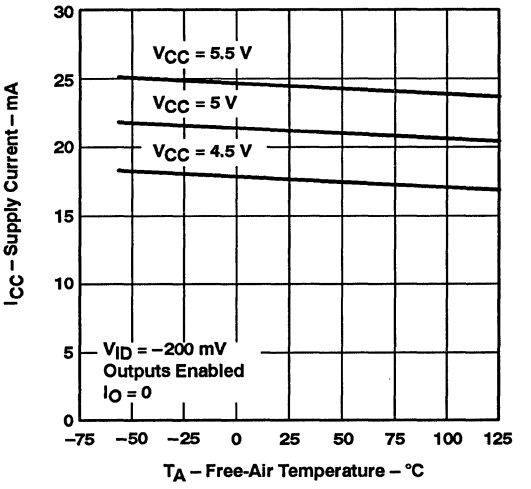


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

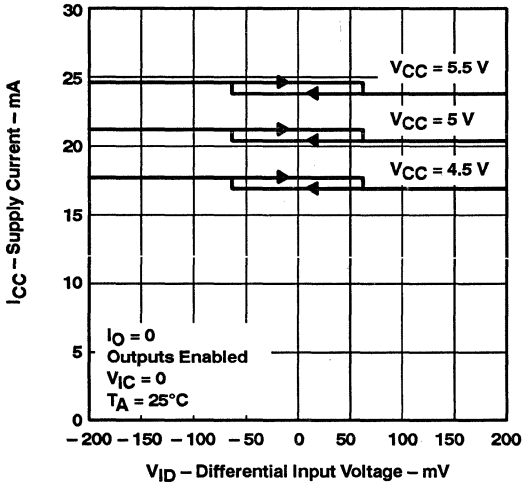


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

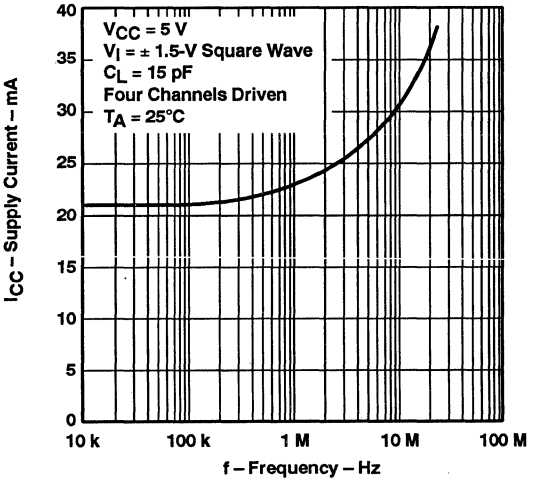


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

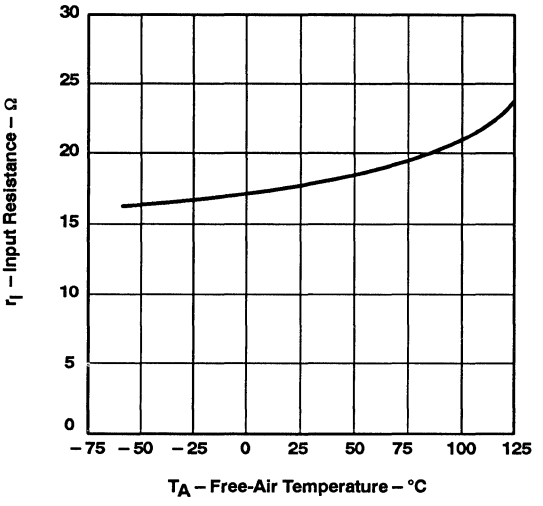


Figure 19

INPUT CURRENT
vs
INPUT VOLTAGE TO GND

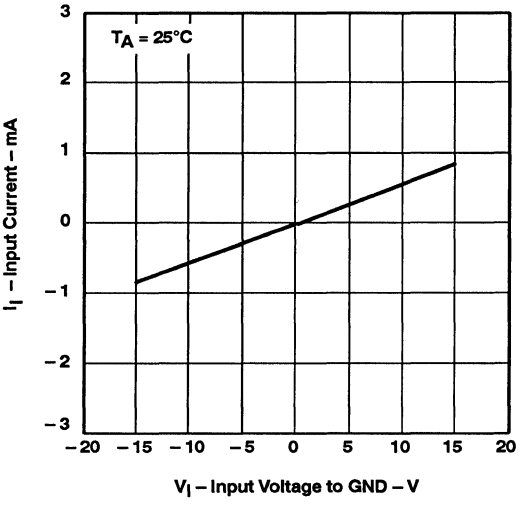


Figure 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

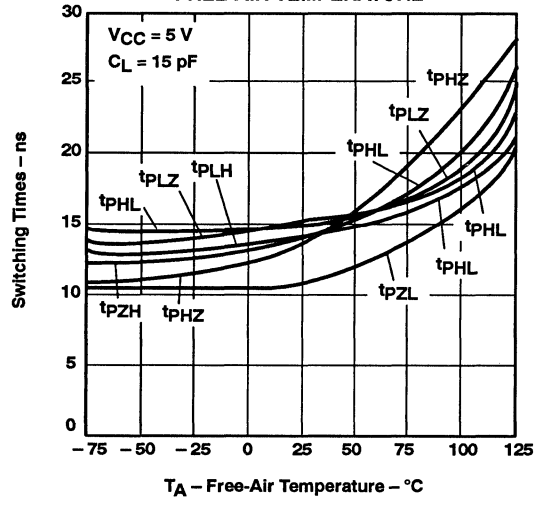


Figure 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

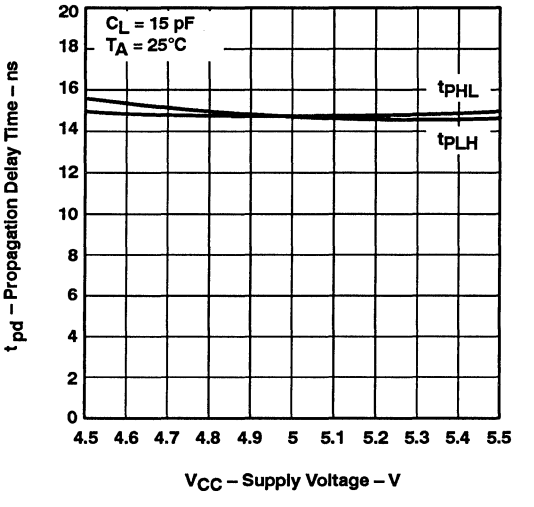
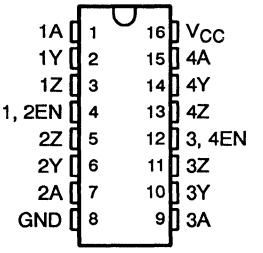


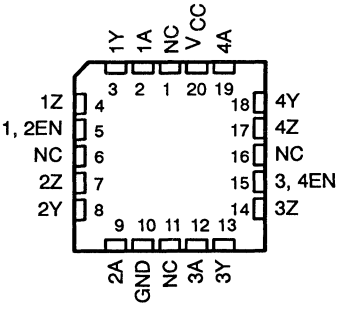
Figure 22

- **Meets EIA Standard RS-422-A**
- **High-Speed ALS Design**
- **3-State TTL-Compatible Outputs**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Two Pairs of Drivers Independently Enabled**
- **Designed as a Replacement for the MC3487 With Improvements: I_{CC} 50% Lower, Switching Speed 30% Faster, Full-Temperature-Range Version**

SN55ALS194 . . . J OR W PACKAGE
SN75ALS194 . . . D OR N PACKAGE
(TOP VIEW)



SN55ALS194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quad differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns and enable/disable times are typically less than 16 ns.

High-impedance inputs keep input currents low, less than 1 μA for a high level and less than 100 μA for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN55ALS194 and SN75ALS194 are capable of data rates in excess of 10 megabits per second and are designed to operate with the SN55ALS195 and SN75ALS195 quadruple line receivers.

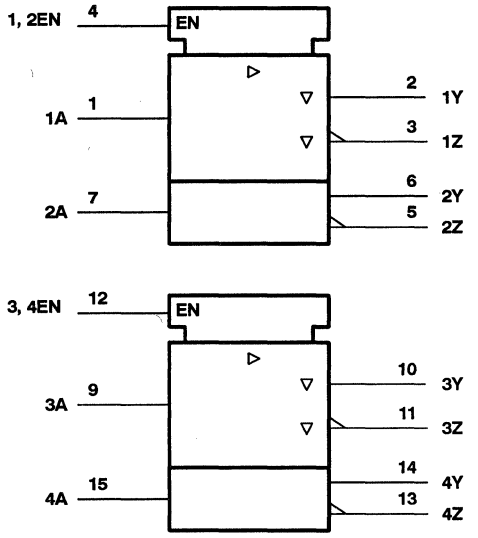
The SN55ALS194 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN75ALS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

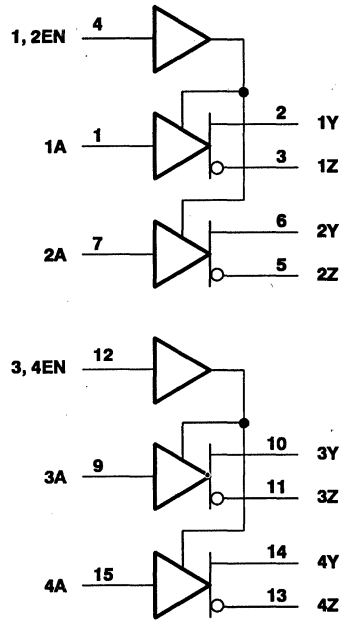
INPUT A	OUTPUT EN	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance

logic symbol†

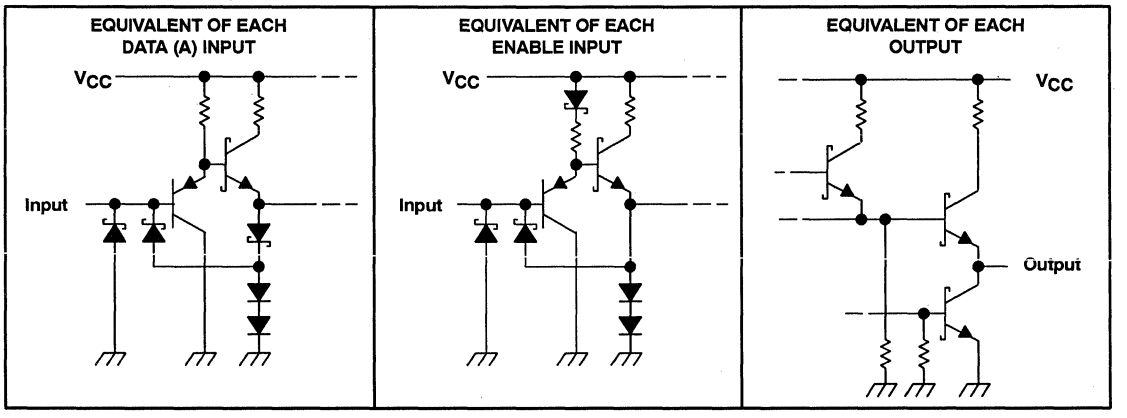


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55ALS194 ..... – 55°C to 125°C
SN75ALS194 ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions†

		SN55ALS194			SN75ALS194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	All inputs, T_A = 25°C	2			2			V
	A inputs, T_A = Full range	2			2			
	EN inputs, T_A = Full range	2.1			2			
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}				– 20			– 20	mA
Low-level output current, I_{OL}	T_A = 25°C			48			48	mA
	T_A = Full range			20			48	
Operating free-air temperature, T_A		– 55		125	0		70	°C

† Full range is T_A = – 55°C to 125°C for SN55ALS194 and T_A = 0°C to 70°C for SN75ALS194.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –20 mA	SN55ALS194	2.4			V
			SN75ALS194	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX			0.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage¶					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage¶					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6V			100	µA
			V_O = –0.25 V			–100	
I_{OZ}	High-impedance state output current	V_{CC} = MAX, Output enables at 0.8 V	V_O = 2.7 V			100	µA
			V_O = 0.5 V			–100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			100	µA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			50	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			–200	µA
I_{OS}	Short-circuit output current#	V_{CC} = MAX,	V_I = 2 V	–40		–140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX,	All outputs disabled		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, TA = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
# Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55ALS194			SN75ALS194			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		6	13		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	14		9	14	ns
	Output-to-output skew			3.5	6		3.5	6	ns
t_{tD}	Differential-output transition time	C_L = 15 pF, See Figure 3		8	14		8	14	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 4		9	12		9	12	ns
t_{PZL}	Output enable time to low level			12	20		12	20	ns
t_{PHZ}	Output disable time from high level			9	15		9	14	ns
t_{PLZ}	Output disable time from low level			12	15		12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$

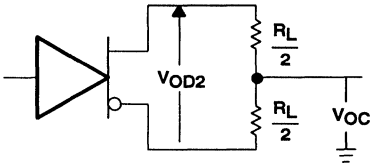


Figure 1. Driver V_{OD} and V_{OC}

PARAMETER MEASUREMENT INFORMATION

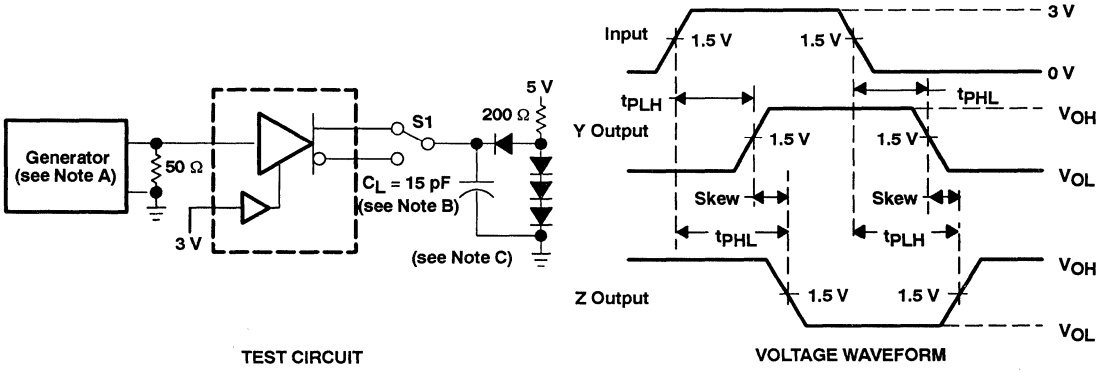


Figure 2. Test Circuit and Voltage Waveform

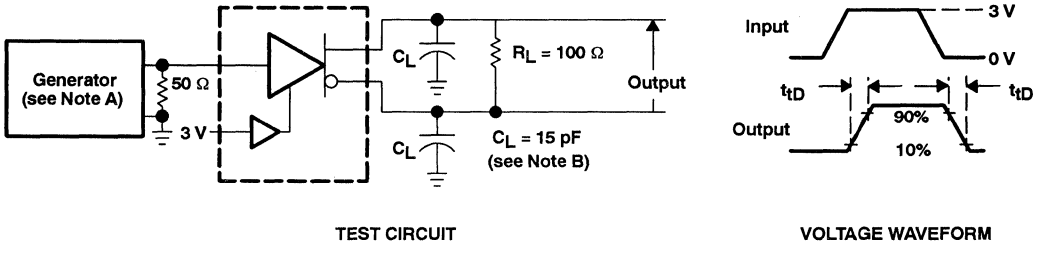
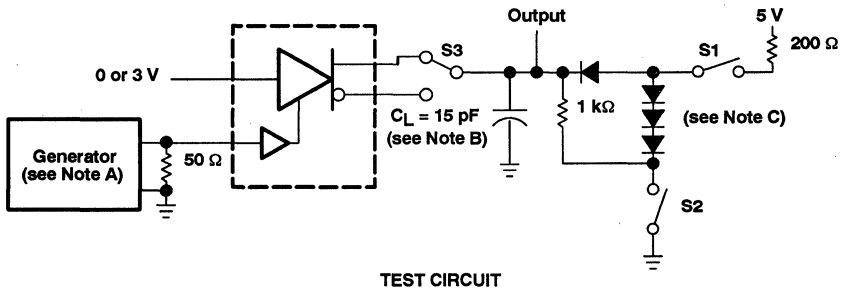


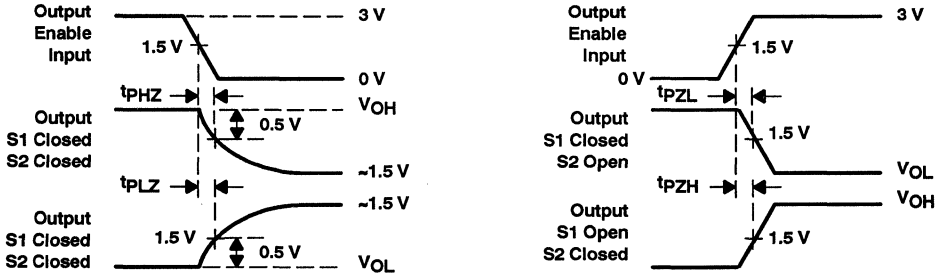
Figure 3. Differential-Output Test Circuit and Voltage Waveform

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O \sim 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

Figure 4. Driver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

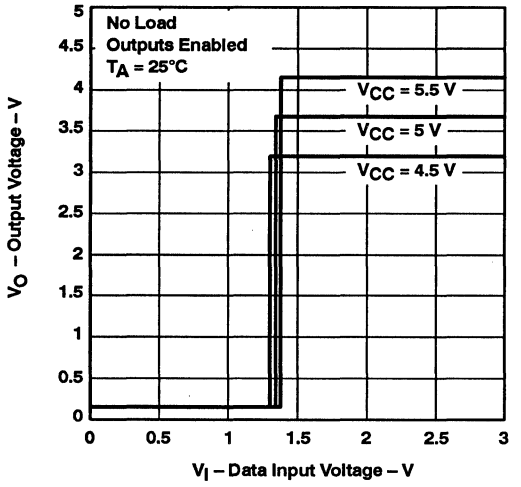


Figure 5

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

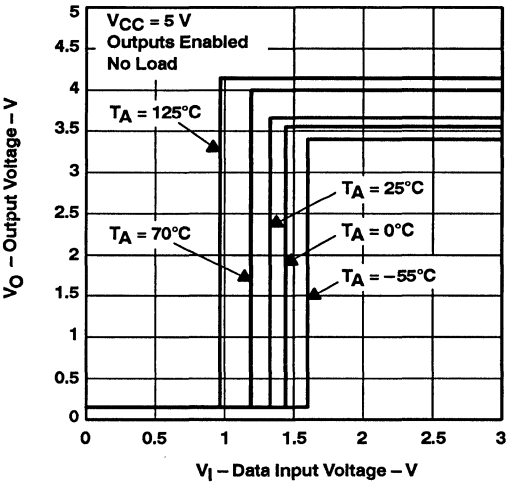


Figure 6

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

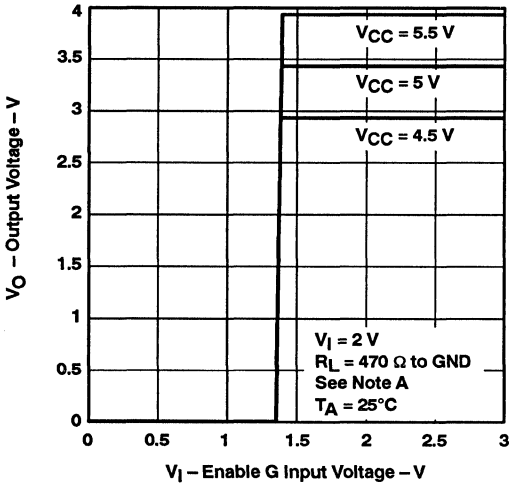


Figure 7

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

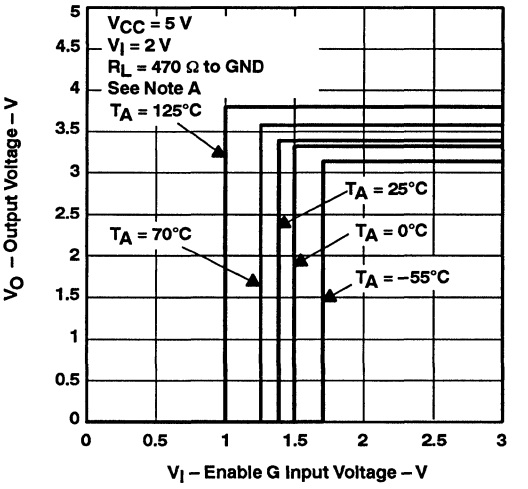


Figure 8

† Date for temperatures below 0°C and above 70°C are applicable to SN55ALS194 circuits only.
NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

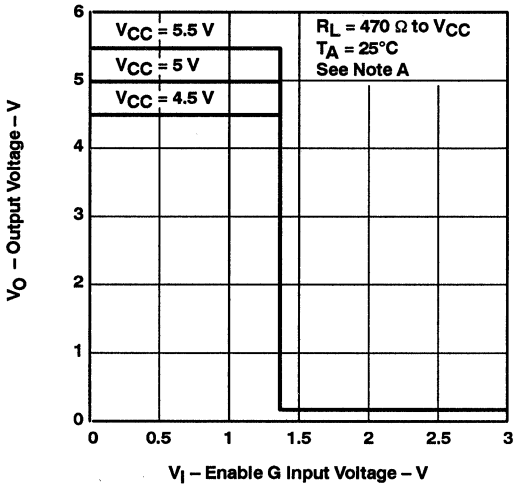


Figure 9

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

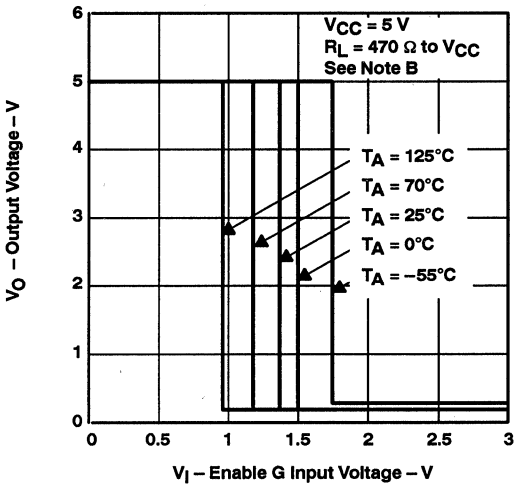


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

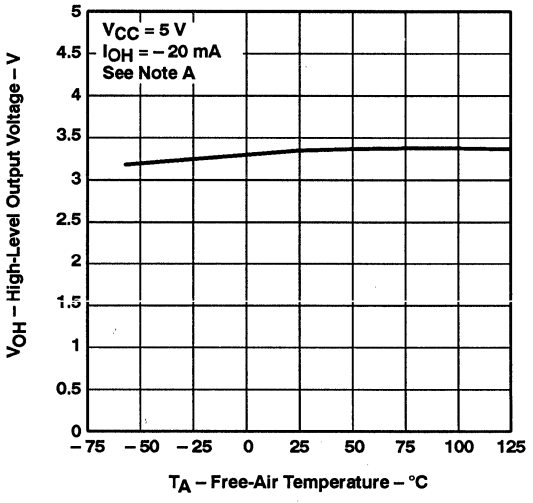


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

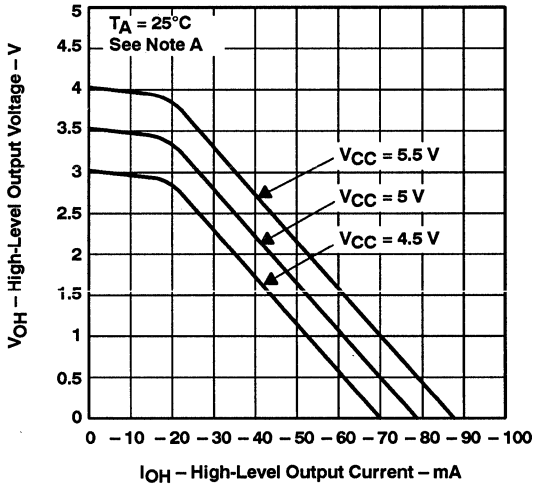


Figure 12

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.
B. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

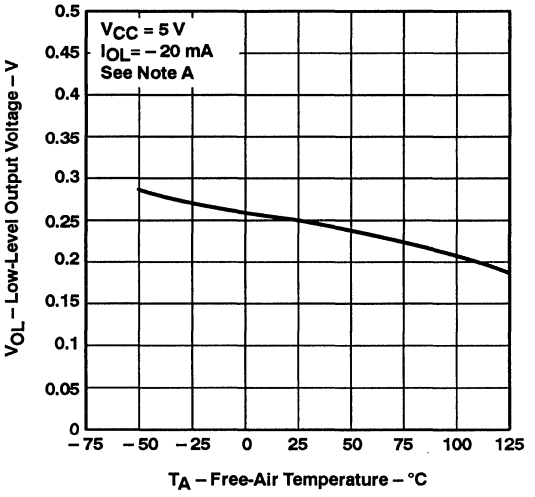


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

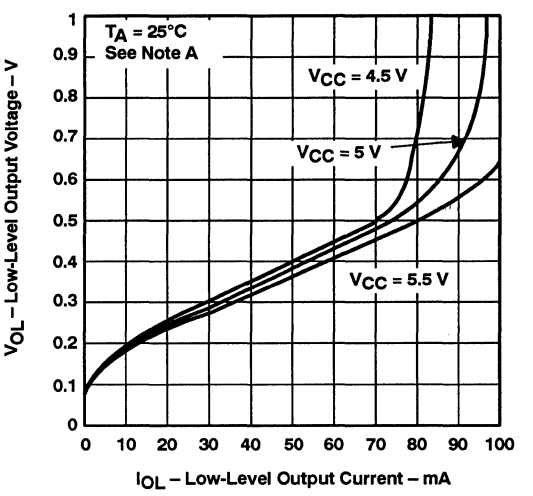


Figure 14

SUPPLY CURRENT vs SUPPLY VOLTAGE

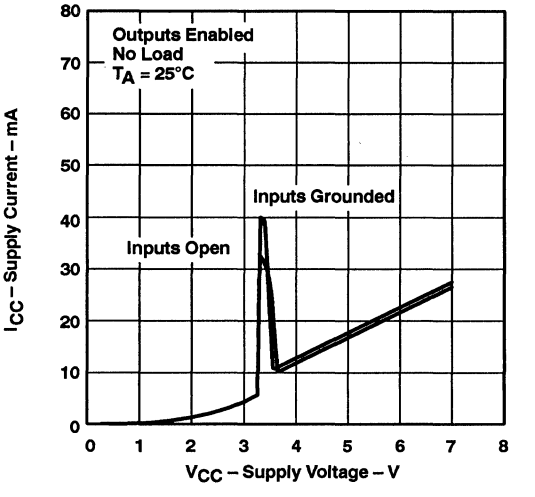


Figure 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

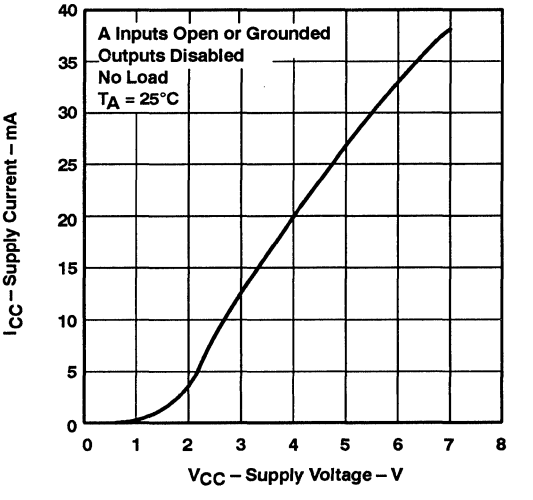


Figure 16

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.
NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

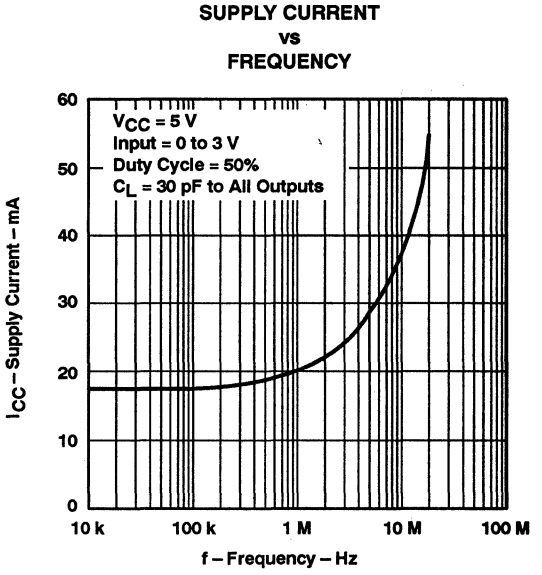
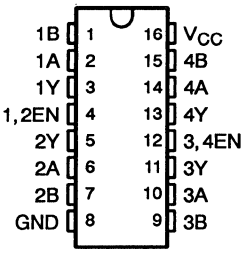


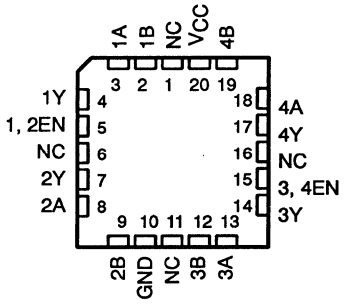
Figure 17

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **–7 V to 7 V Common-Mode Input Voltage Range With 200-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

SN55ALS195 . . . J OR W PACKAGE
SN75ALS195 . . . J PACKAGE
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

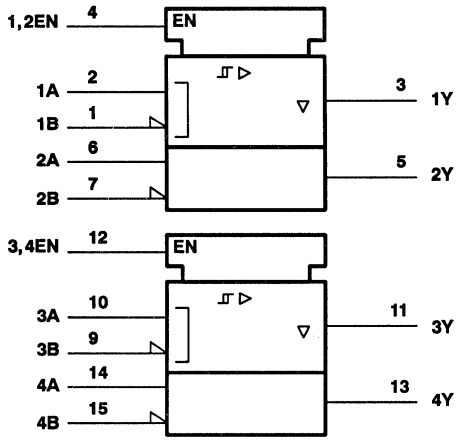
description

The SN55ALS195 and SN75ALS195 are monolithic quad line receivers with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of EIA Standards RS-422-A and RS-423-A. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The devices are optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of ± 7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quad differential line drivers.

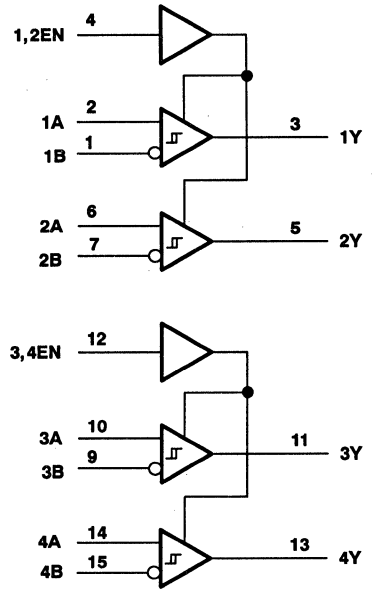
The SN55ALS195 is characterized for operation over the full military temperature range of – 55°C to 125°C. The SN75ALS195 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



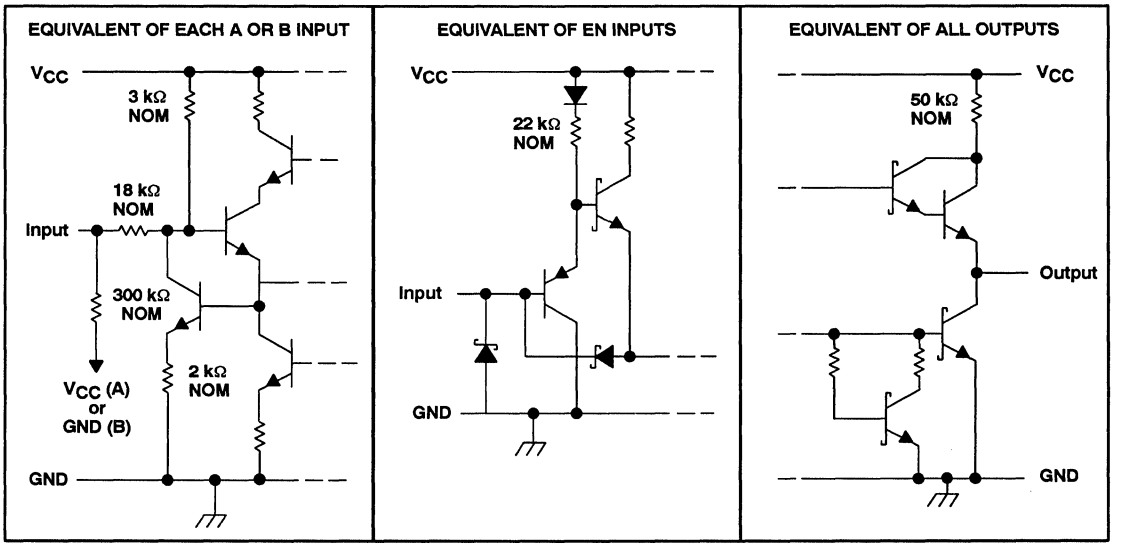
Pin numbers shown are for the J and W packages.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} <$ 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55ALS195 ..... – 55°C to 125°C
SN75ALS195 ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package ..... 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditons is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/°C	656 mW	N/A
W	1000 mW	8.0 mW/°C	690 mW	200 mW

recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Differential input voltage, V_{ID}			±12			±12	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage						200	mV
V_{T-}	Negative-going threshold voltage				−200§			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)					120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, See Figure 1	V_{ID} = 200 mV,	I_{OH} = −400 μA,	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA				0.45	V
			I_{OL} = 16 mA				0.5	
I_{OZ}	High-impedance state output current	V_{CC} = MAX, V_O = 2.7 V	V_{IL} = 0.8 V,	V_{ID} = −3 V,			20	μA
		V_{CC} = MAX, V_O = 0.5 V	V_{IL} = 0.8 V,	V_{ID} = 3 V,			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_{CC} = MIN,	V_I = 15 V		0.7	1.2	mA
			V_{CC} = MAX,	V_I = −15 V		−1	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V				20	μA
			V_{IH} = 5.25 V				100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V				−100	μA
	Input resistance				12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, See Note 4	V_{ID} = 3 V,	V_O = 0,	−15	−78	130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled			22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
NOTES: 3. Refer to EIA Standards RS-422-A and RS-423-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 V to 3 V, See Figure 2		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level			10	25	
t_{PHZ}	Output disable time from high level	See Figure 3		19	25	ns
t_{PLZ}	Output disable time from low level			17	22	

PARAMETER MEASUREMENT INFORMATION

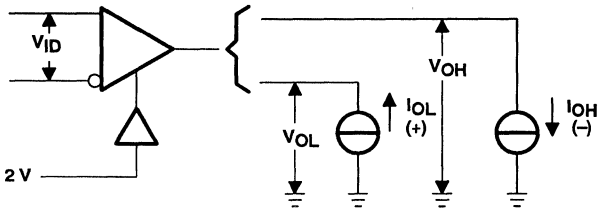
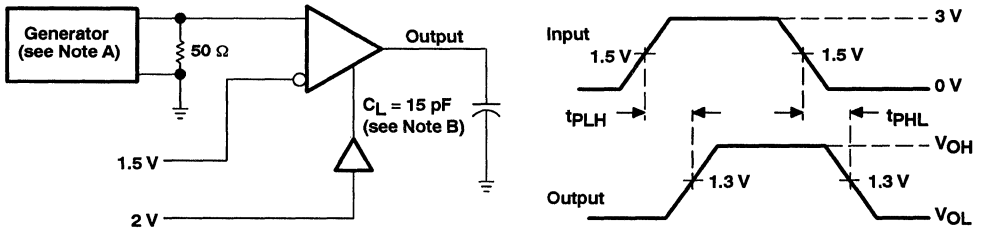


Figure 1. V_{OH}, V_{OL}

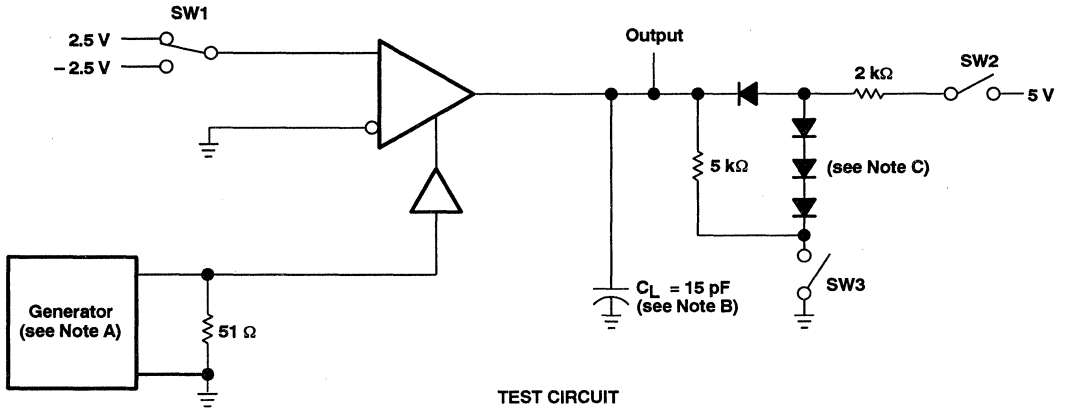


TEST CIRCUIT VOLTAGE WAVEFORMS

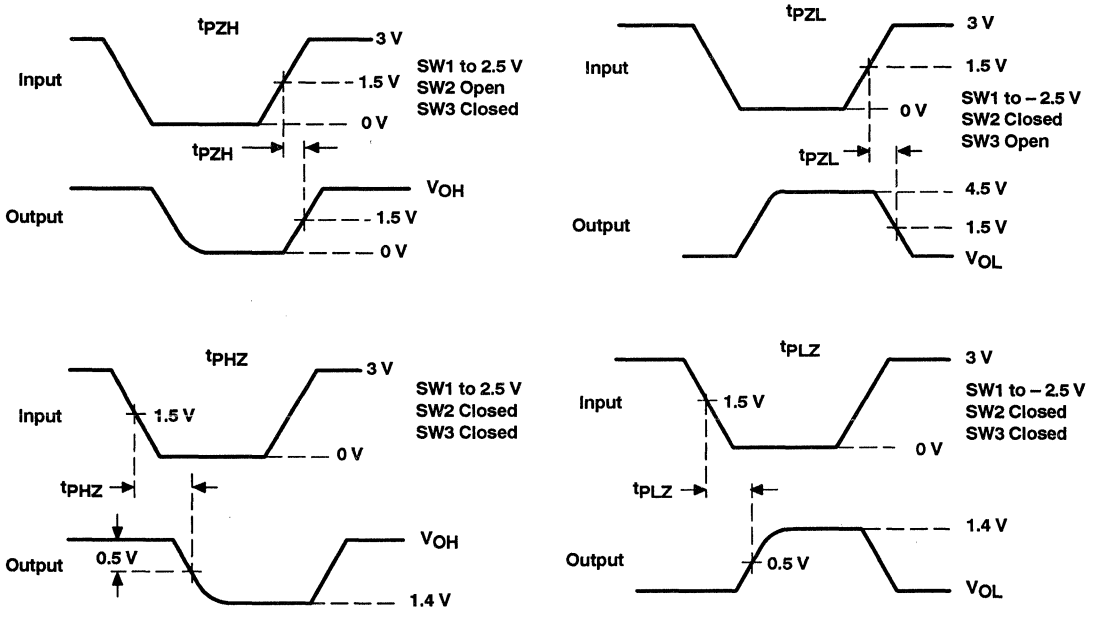
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

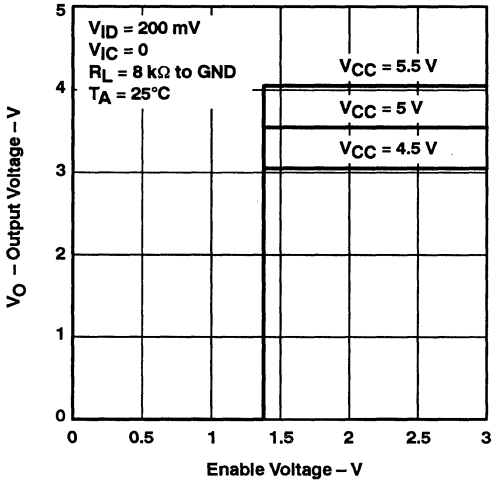


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

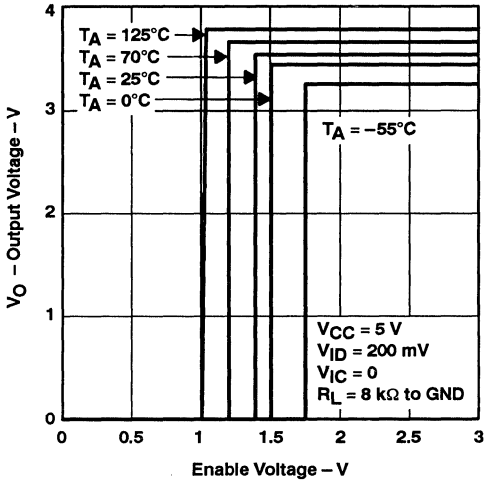


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

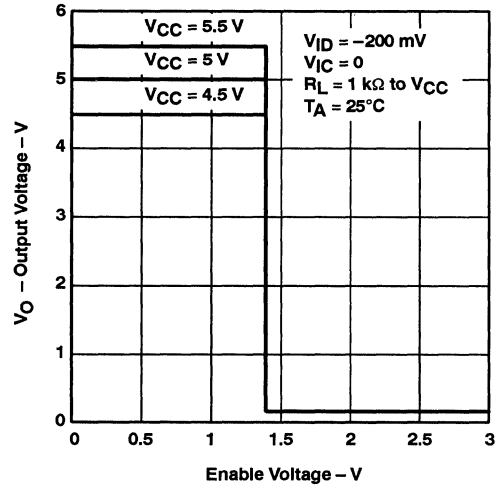


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

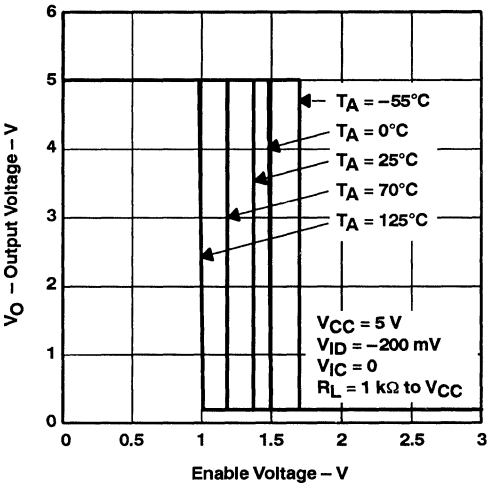


Figure 7

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

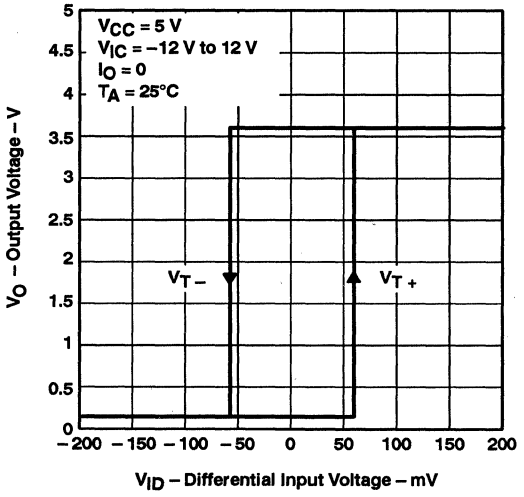


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

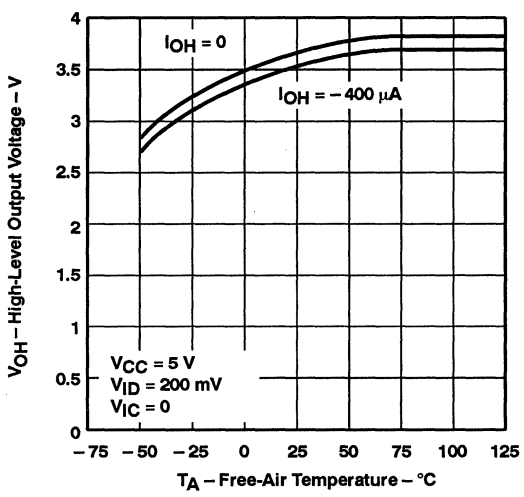


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

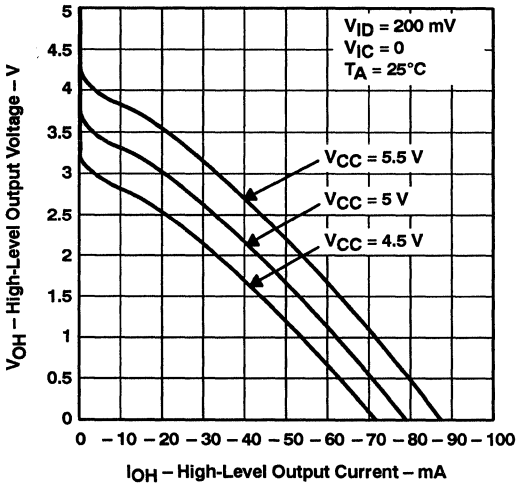


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

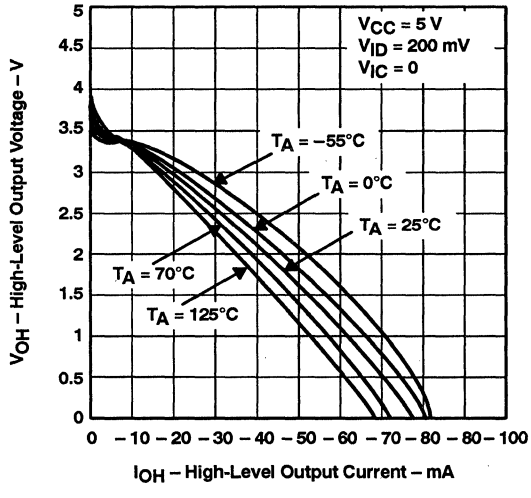


Figure 11

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

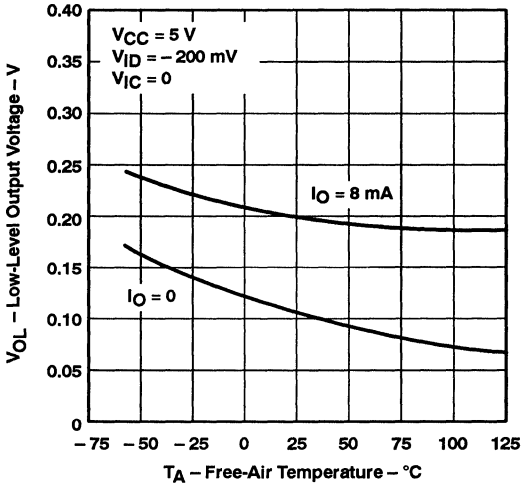


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

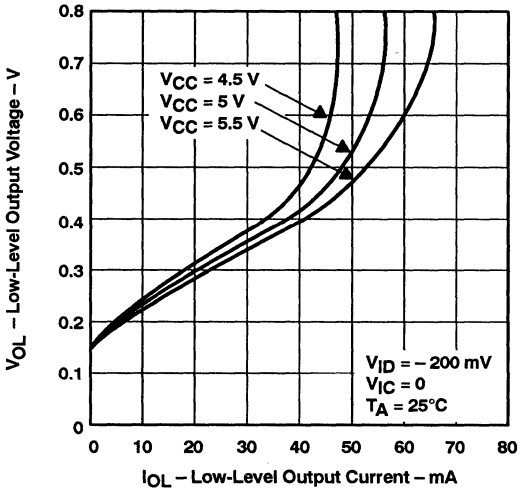


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

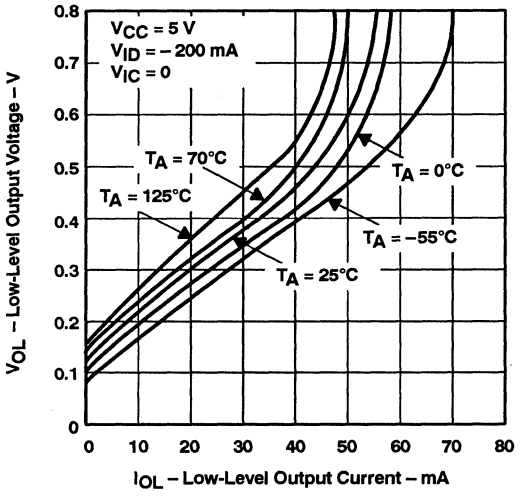


Figure 14

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

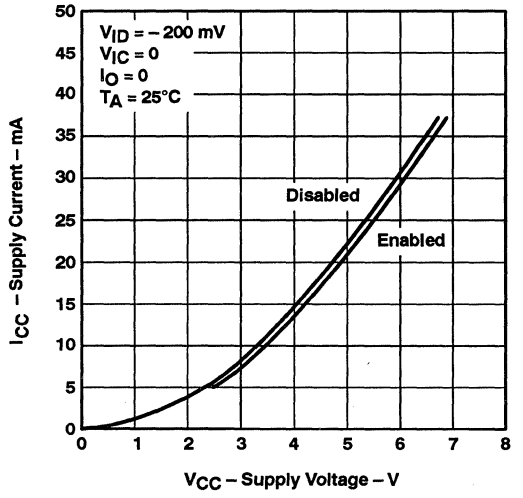


Figure 15

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

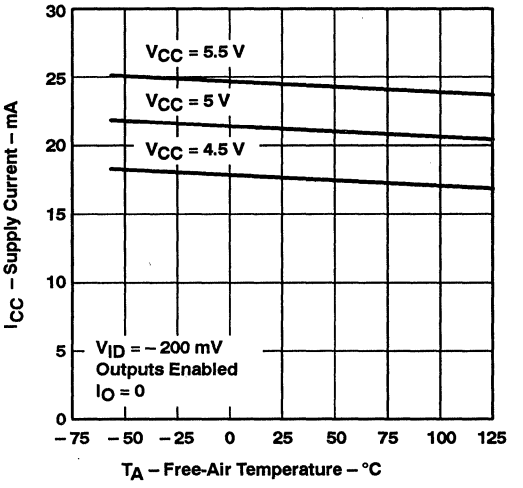


Figure 16

SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE

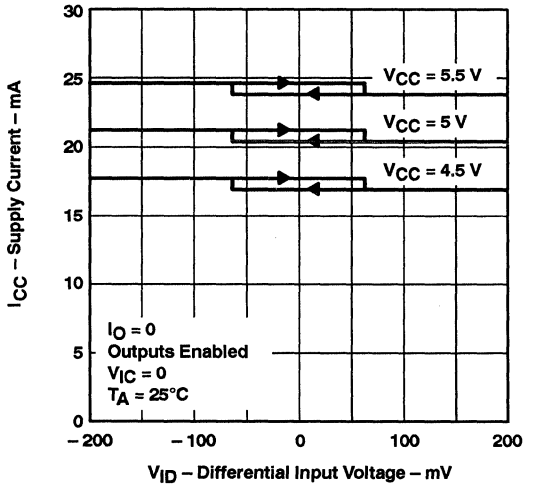


Figure 17

SUPPLY CURRENT vs FREQUENCY

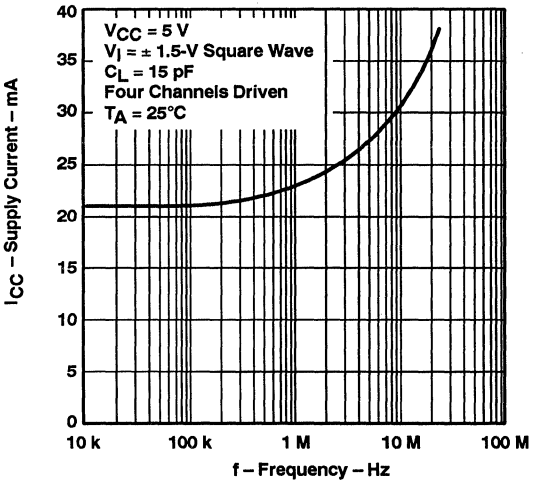


Figure 18

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

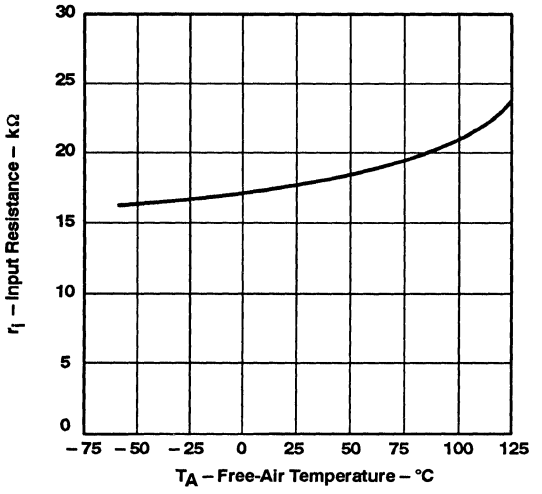


Figure 19

INPUT CURRENT
vs
INPUT VOLTAGE TO GND

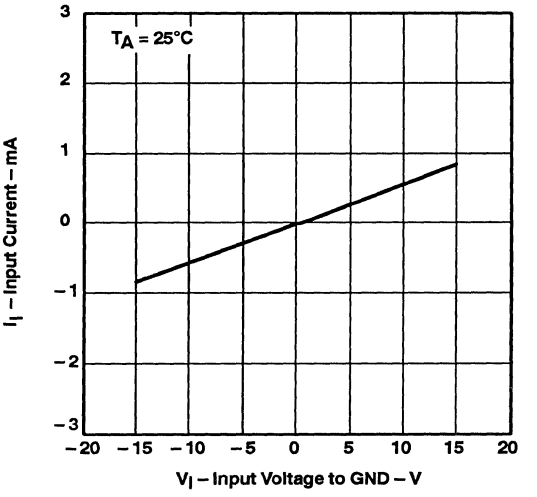


Figure 20

SWITCHING CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

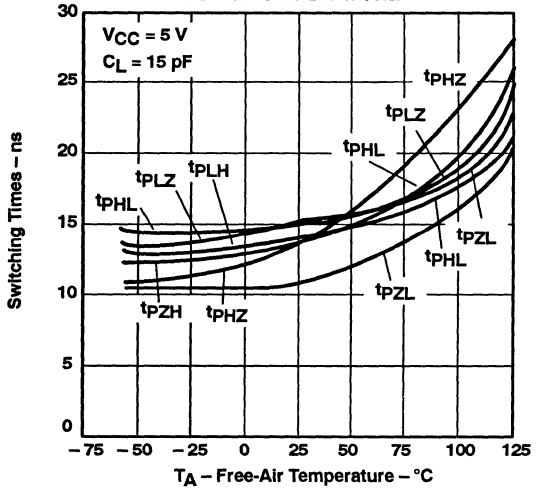


Figure 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

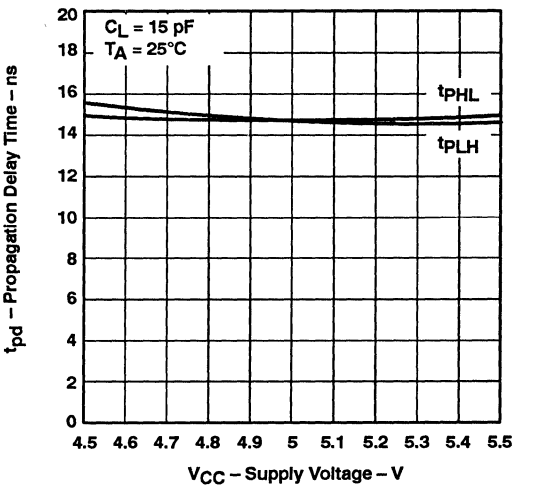


Figure 22

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −7 V to 7 V**
- **Input Sensitivity . . . ± 300 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to AM26LS32A**

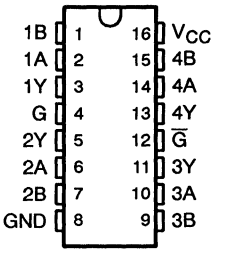
description

The SN75ALSI97 is a monolithic quad line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of CCITT Recommendations V.10, V.11, X.26, and X.27. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

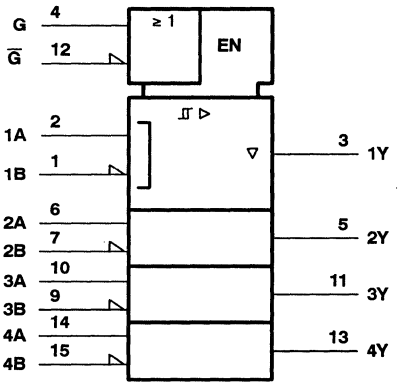
The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of −7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quad differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

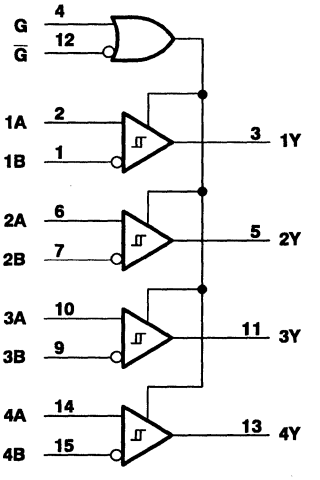


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

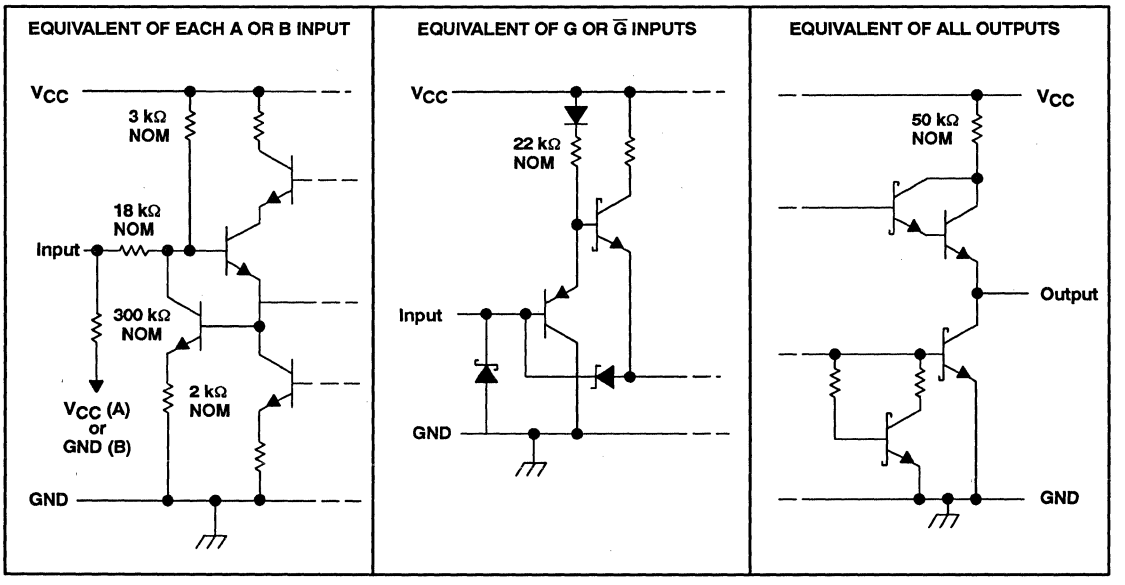


FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
-0.3 V $< V_{ID} <$ 0.3 V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate,
Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the, corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7	V
Differential input voltage, V_{ID}			± 12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					300	mV
V_{T-}	Negative-going threshold voltage			−300‡			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	See Figure 4			120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = −400 μA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	μA
			V_{OH} = 0.4 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	μA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current§	V_{ID} = 3 V,	V_O = 0	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 2		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

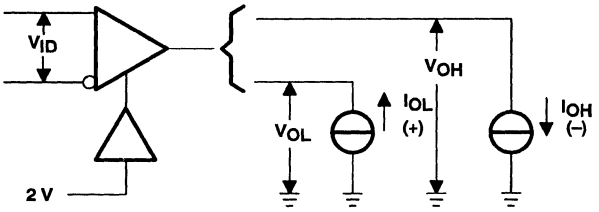
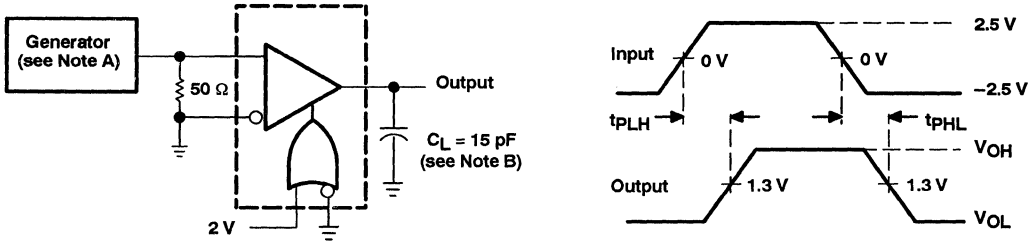


Figure 1. V_{OH}, V_{OL} Test Circuit

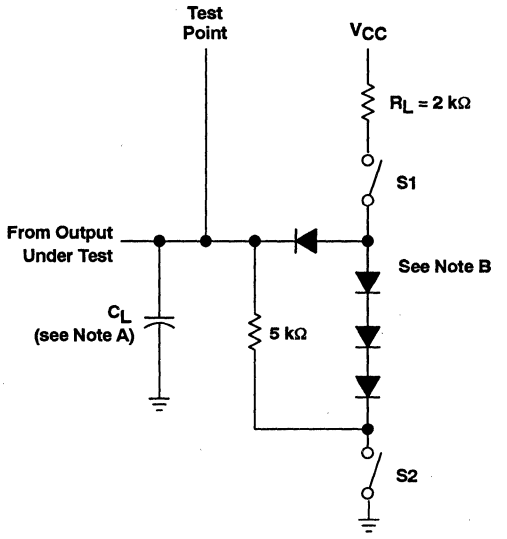


TEST CIRCUIT **VOLTAGE WAVEFORMS**

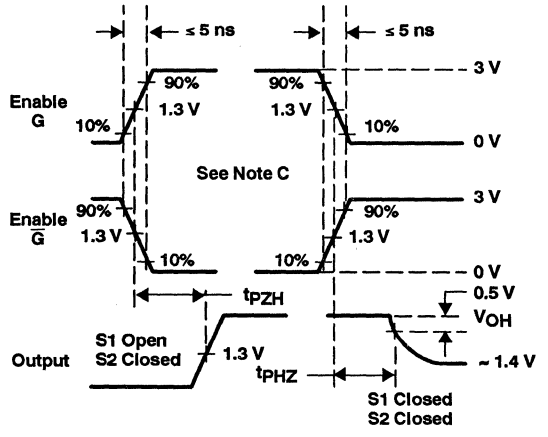
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. t_{PLH}, t_{PHL} Test Circuit and Voltage Waveforms

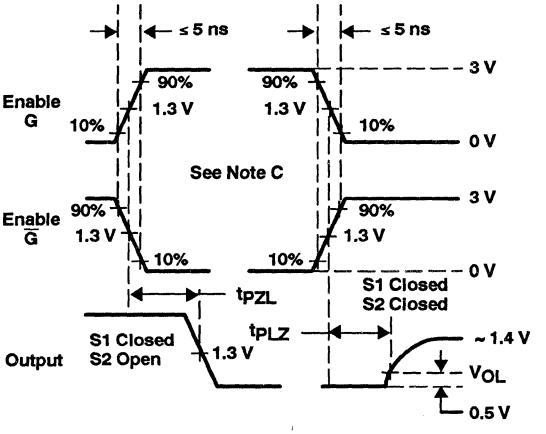
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 3. t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL} Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

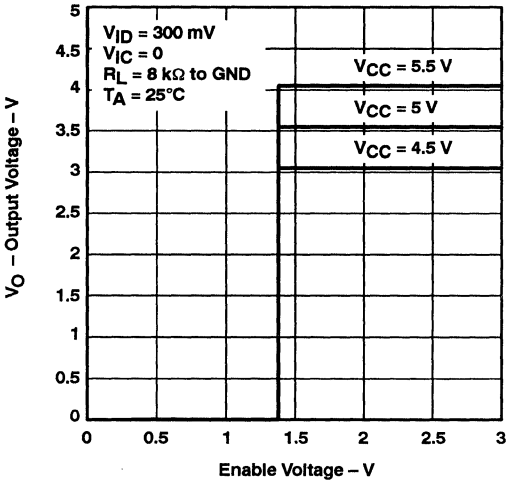


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

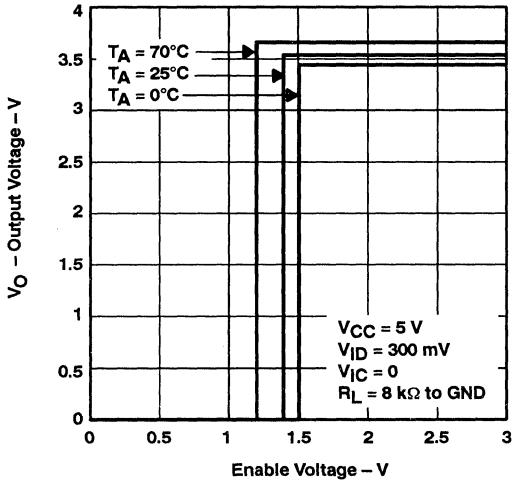


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

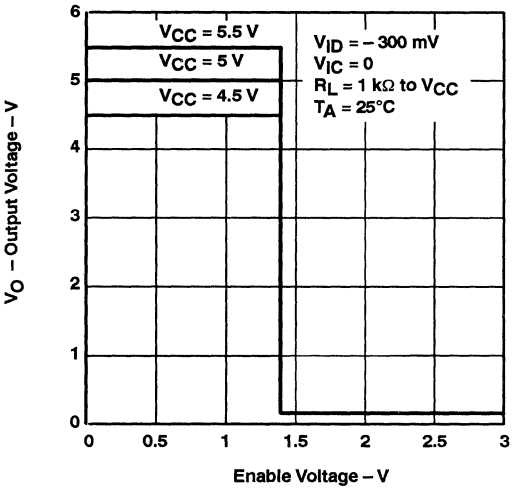


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

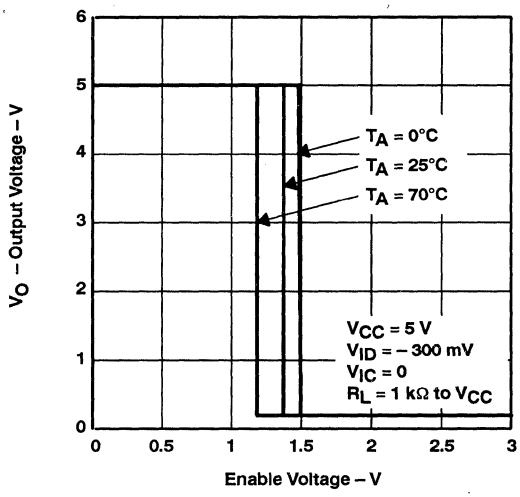


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

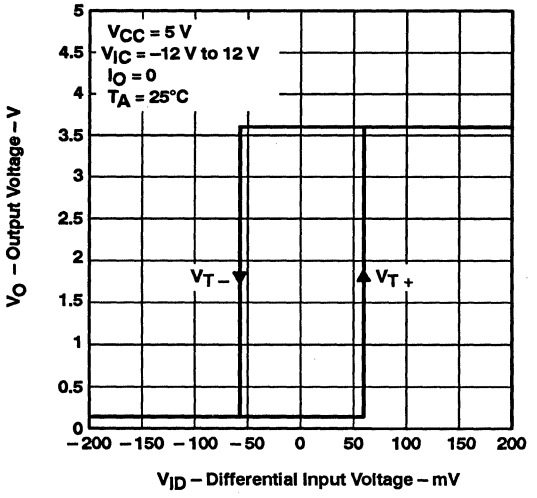


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

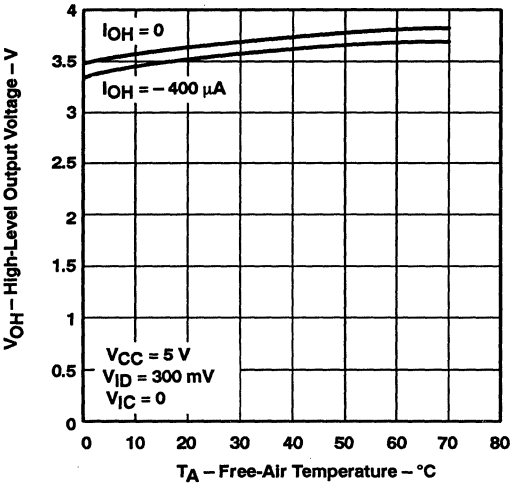


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

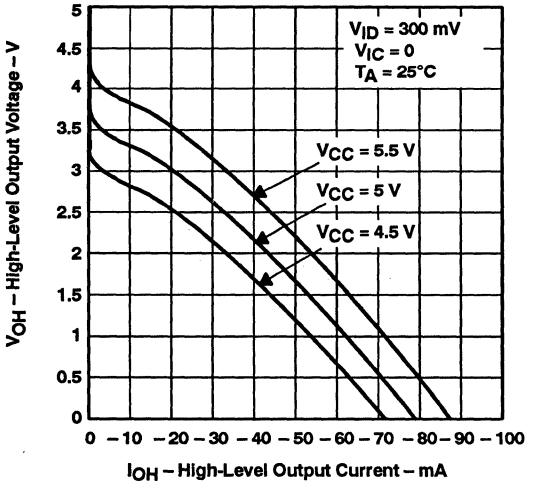


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

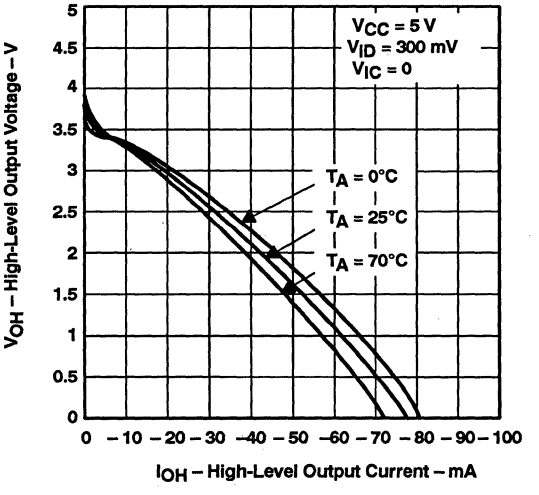


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

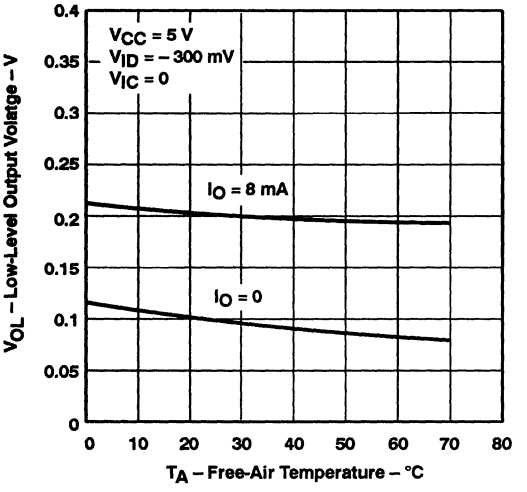


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

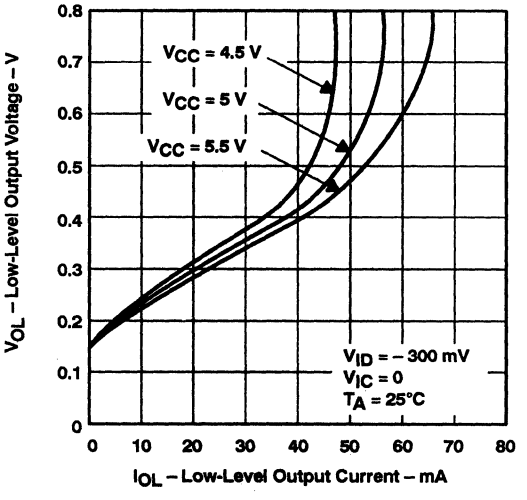


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

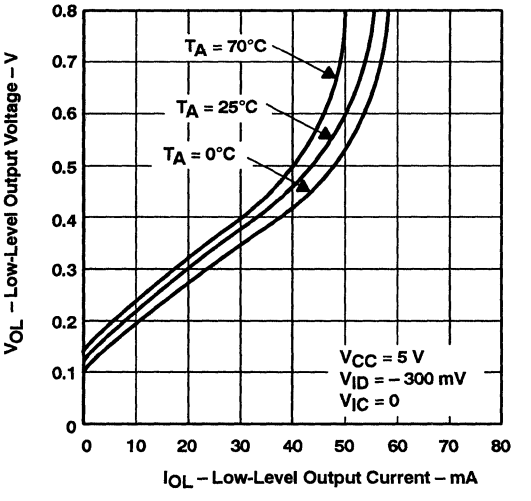


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

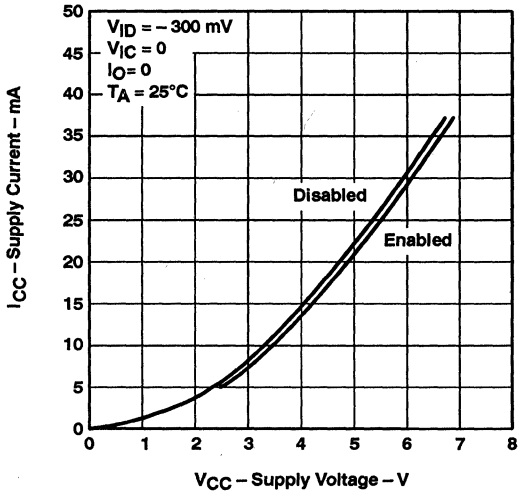


Figure 15

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

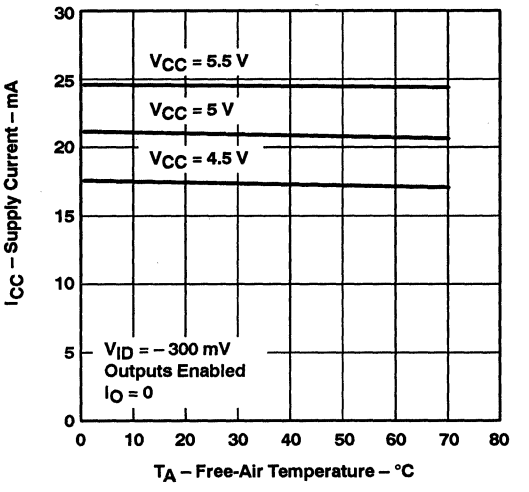


Figure 16

SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE

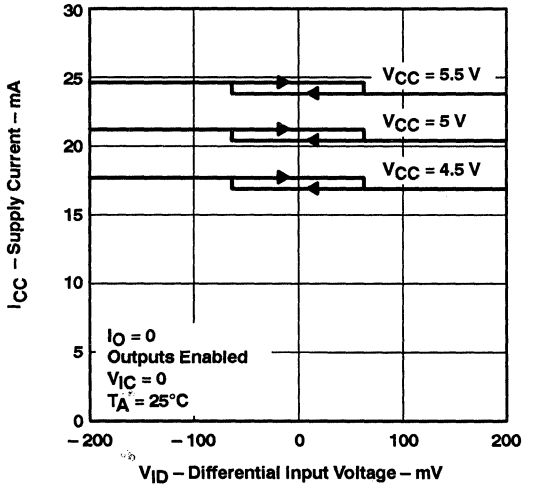


Figure 17

SUPPLY CURRENT vs FREQUENCY

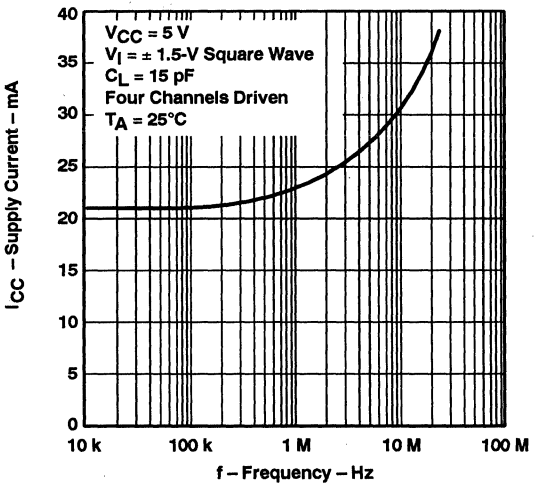


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

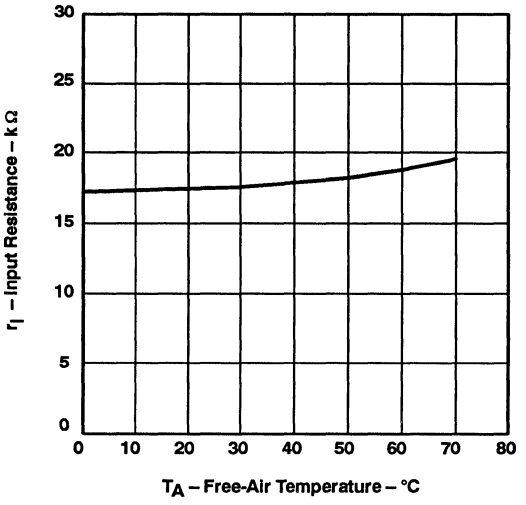


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

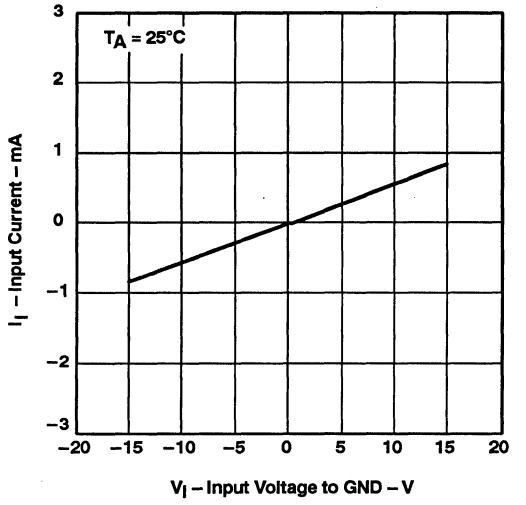


Figure 20

SWITCHING CHARACTERISTICS vs FREE-AIR TEMPERATURE

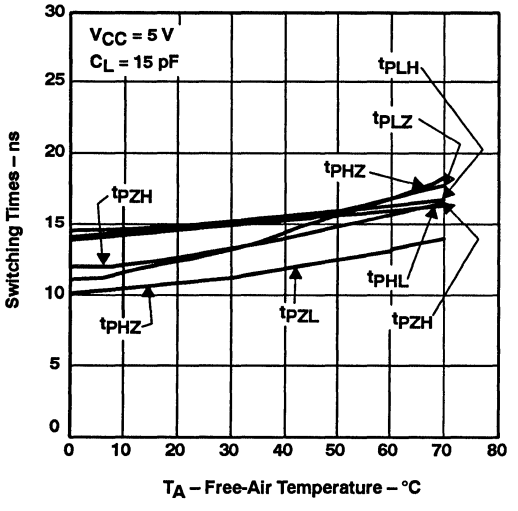


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

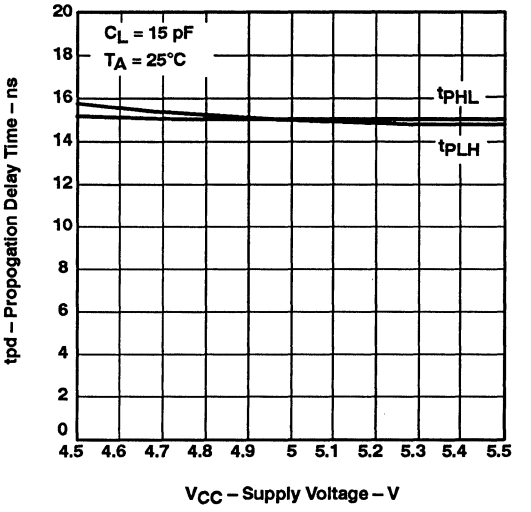


Figure 22

- **Meets EIA-232-D (Revision of RS-232-C)**
- **Very Low Supply Current**
- **Sleep Mode:**
  3-State Outputs in High-Impedance State
  Ultra-Low Supply Current . . . 17 μA Typ
- **Improved Functional Replacement for:**
  SN75188,
  Motorola MC1488,
  National Semiconductor DS14C88, and
  DS1488
- **CMOS- and TTL-Compatible Data Inputs**
- **On-Chip Slew-Rate Limit . . . 30 V/μs**
- **Output Current Limit . . . 10 mA Typ**
- **Wide Supply Voltage Range . . . ±4.5 V to ±15 V**
- **ESD Protection Exceeds 500 V Per MIL-STD-883C, Method 3015.2**

description

The SN65C198 and SN75C198 are monolithic low-power BI-MOS quad low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI/EIA-232-D-1986.

The sleep-mode input, $\overline{SM}$, can be used to switch the outputs to high impedance, which avoids the transmission of corrupted data during power up and allows significant system power savings during data-off periods.

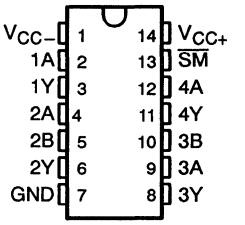
The SN65C198 is characterized for operation from −40°C to 85°C. The SN75C198 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

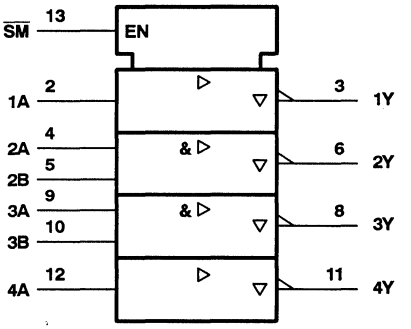
INPUTS			OUTPUT
$\overline{SM}$	A	B	Y
H	H	H	L
H	L	X	H
H	X	L	H
L	X	X	Z

H = high level, L = low level,
X = irrelevant,
Z = high impedance

D OR N PACKAGE
(TOP VIEW)

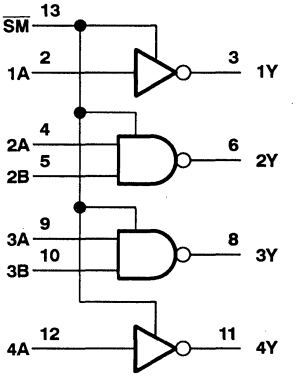


logic symbol†

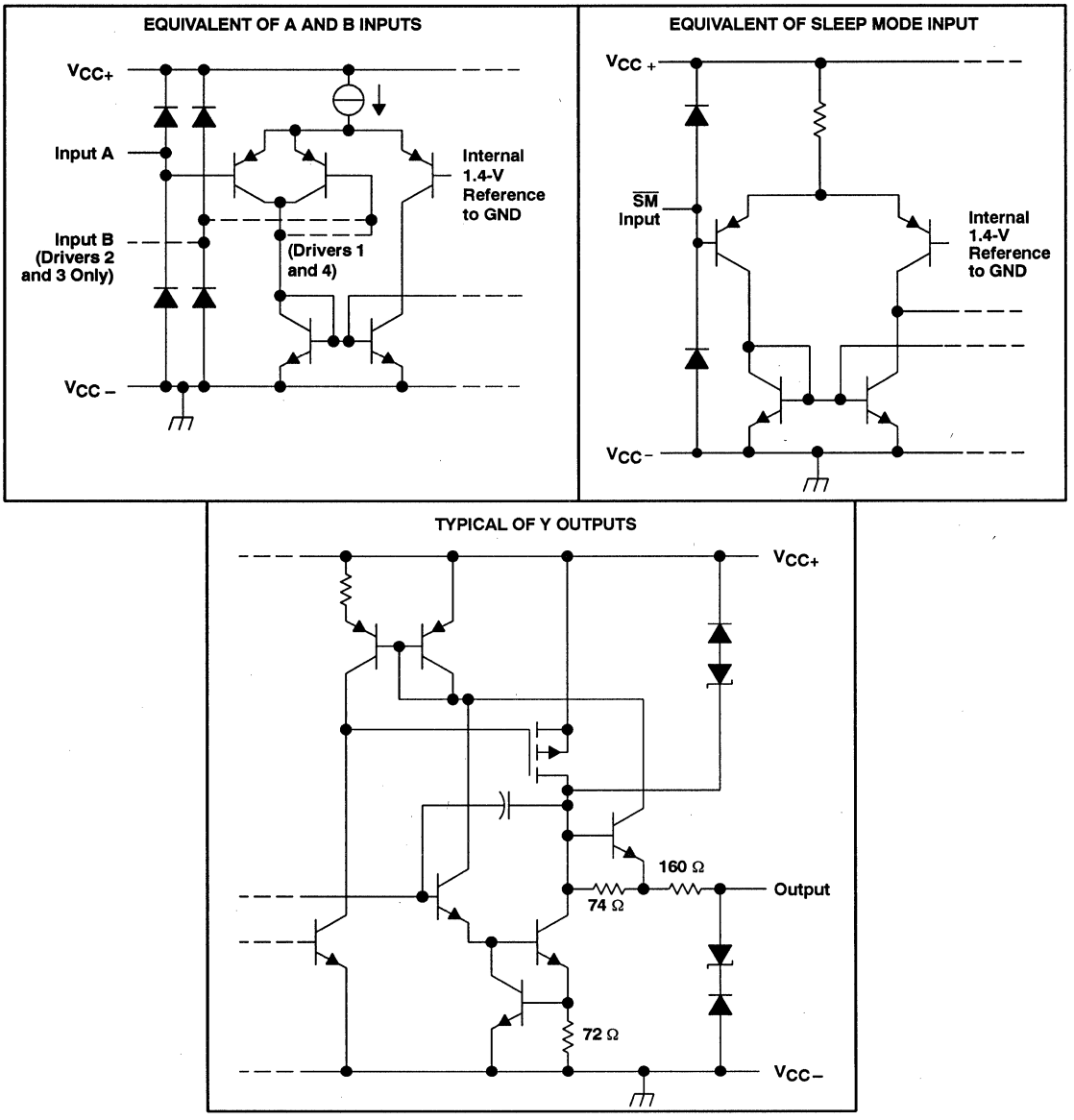


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} ..... −15 V
Input voltage range ..... −15 V to 15 V
Output voltage range ..... V_{CC-} −6 V to V_{CC+} + 6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65C198 ..... −40°C to 85°C
SN75C198 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}			4.5	12	15	V
Supply voltage, V_{CC-}			−4.5	−12	−15	V
Input voltage, V_I (see Figure 2)			V_{CC-}+2		V_{CC+}	V
High-level input voltage, V_{IH}			2			V
Low-level input voltage, V_{IL}	A and B inputs				0.8	V
	$\overline{SM}$ input				0.6	
Operating free-air temperature, T_A		SN65C198	−40		85	°C
		SN75C198	0		70	

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±12 V, $\overline{SM}$ at 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 0.8 V,	R_L = 3 kΩ	$V_{CC\pm}$ = ±5 V	4			V
				$V_{CC\pm}$ = ±12 V	10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V,	R_L = 3 kΩ	$V_{CC\pm}$ = ±5 V			−4	V
				$V_{CC\pm}$ = ±12 V			−10	
I_{IH}	High-level input current	V_I = 5 V					10	μA
I_{IL}	Low-level input current	V_I = 0 V					−10	μA
I_{OZ}	High-impedance-state output current	$\overline{SM}$ at 0.6 V		V_O = 12 V, $V_{CC\pm}$ = ±12 V			100	μA
				V_O = −12 V, $V_{CC\pm}$ = ±12 V			−100	
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{CC-}		−4.5	−10	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{CC+}		4.5	10	19.5	mA
r_o	Output resistance	$V_{CC\pm}$ = 0,	V_O = −2 V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	A and B inputs at 0.8 V or 2 V, No load		$V_{CC\pm}$ = ±5 V		90	160	μA
				$V_{CC\pm}$ = ±12 V		95	160	
		A and B inputs at 0.8 V or 2 V, R_L = 3 kΩ, $\overline{SM}$ at 0.6 V		$V_{CC\pm}$ = ±5 V		17	40	
				$V_{CC\pm}$ = ±12 V		17	40	
I_{CC-}	Supply current from V_{CC-}	A and B inputs at 0.8 V or 2 V, No load		$V_{CC\pm}$ = ±5 V		−90	−160	μA
				$V_{CC\pm}$ = ±12 V		−95	−160	
		A and B inputs at 0.8 V or 2 V, R_L = 3 kΩ, $\overline{SM}$ at 0.6 V		$V_{CC\pm}$ = ±5 V		−17	−40	
				$V_{CC\pm}$ = ±12 V		−17	−40	

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1			3	μs
t_{PHL}	Propagation delay time, high-to-low-level output§				3.5	μs
t_{TLH}	Transition time, low-to-high-level output¶		0.53	1	3.2	μs
t_{THL}	Transition time, high-to-low-level output¶		0.53	1	3.2	μs
t_{TLH}	Transition time, low-to-high-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 2		1.5		μs
t_{THL}	Transition time, high-to-low-level output#			1.5		μs
t_{PZH}	Output enable time to high level	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3			50	μs
t_{PHZ}	Output disable time from high level				10	μs
t_{PZL}	Output enable time to low level	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 4			15	μs
t_{PLZ}	Output disable time from low level				10	μs
SR	Output slew rate#	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	6	15	30	V/μs

† All typical values are at T_A = 25°C.
§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform
# Measured between 3-V and −3-V points of output waveform

PARAMETER MEASUREMENT INFORMATION

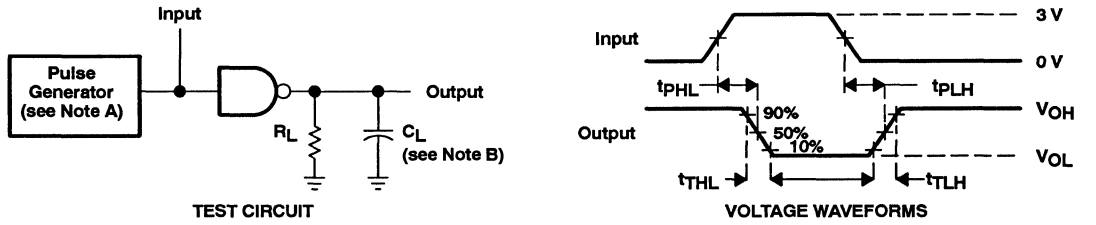


Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times

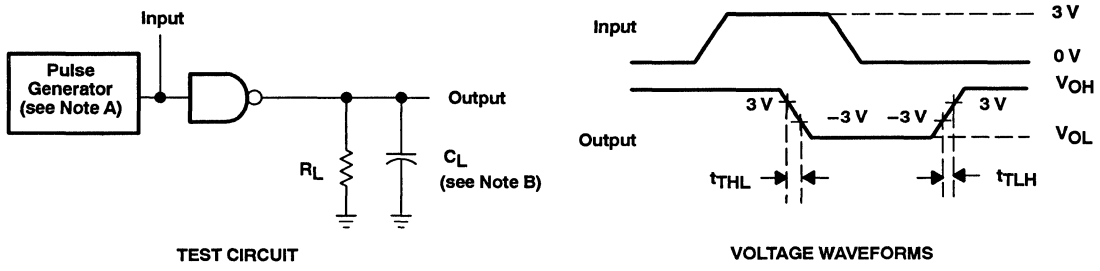


Figure 2. Test Circuit and Voltage Waveforms, Transition Times

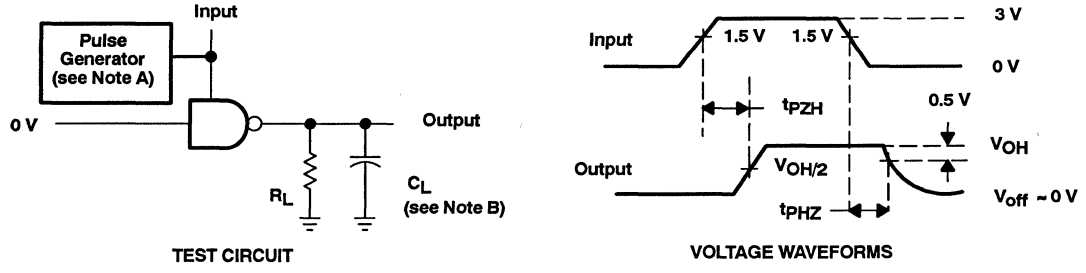


Figure 3. Driver Test Circuit and Voltage Waveforms

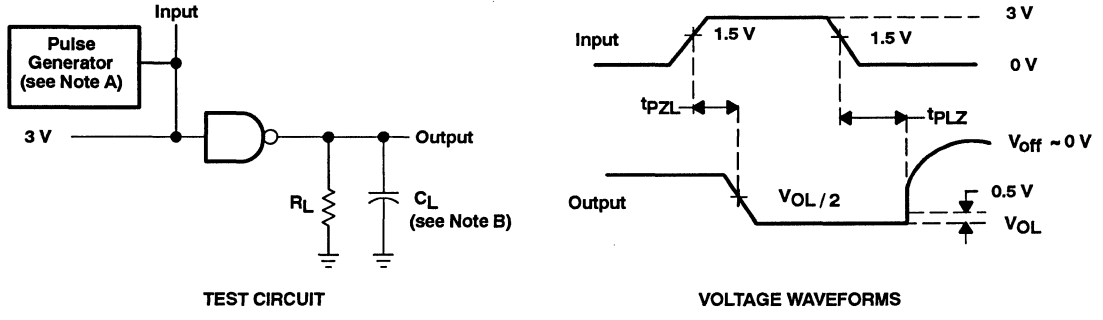


Figure 4. Driver Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

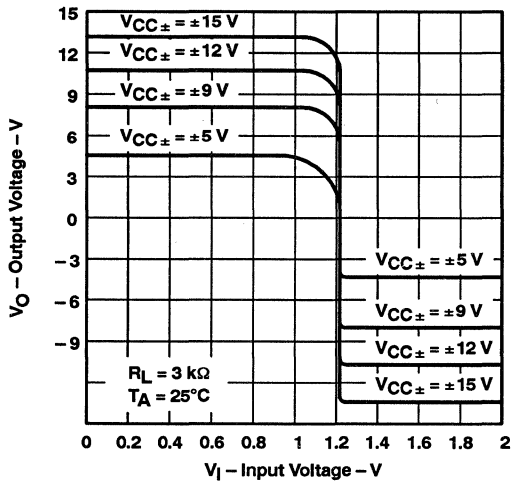


Figure 5

OUTPUT CURRENT vs OUTPUT VOLTAGE

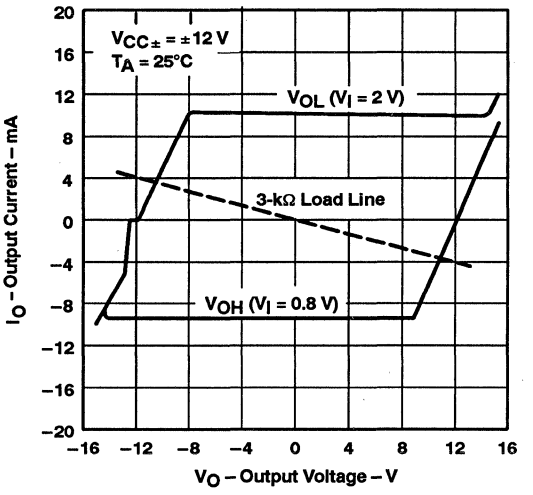


Figure 6

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE†

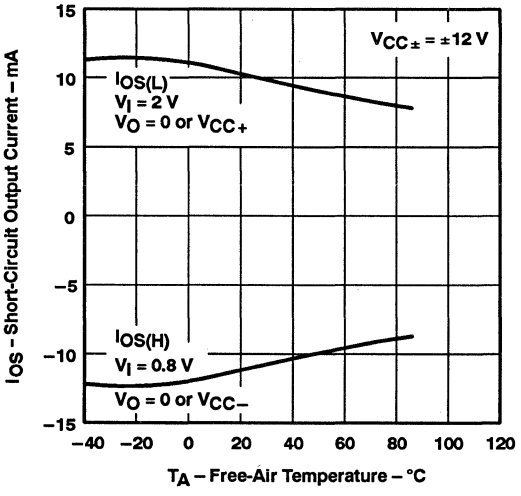


Figure 7

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE†

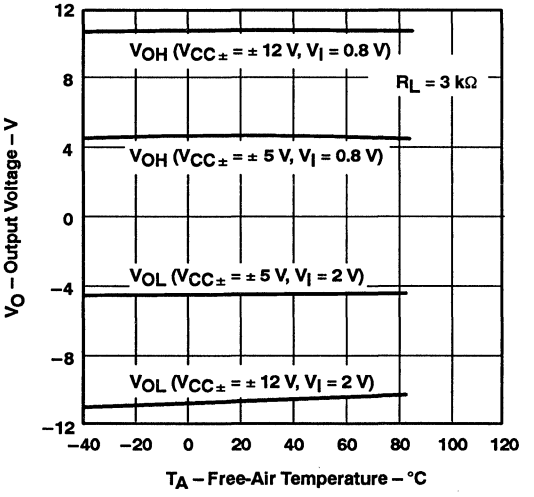


Figure 8

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

TYPICAL CHARACTERISTICS

INPUT CURRENT vs FREE-AIR TEMPERATURE†

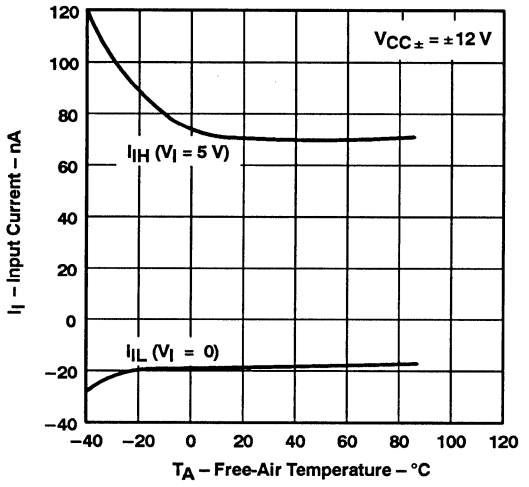


Figure 9

POWER-OFF OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE†

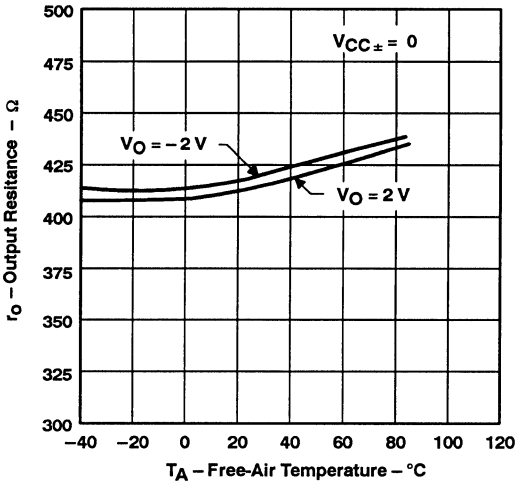


Figure 10

SUPPLY CURRENT vs FREE-AIR TEMPERATURE†

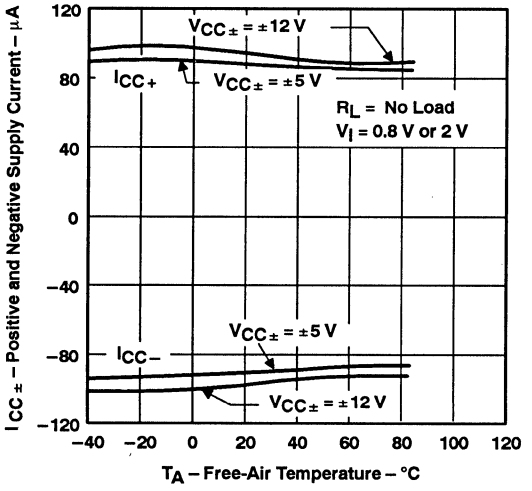


Figure 11

OUTPUT SLEW RATE vs FREE-AIR TEMPERATURE†

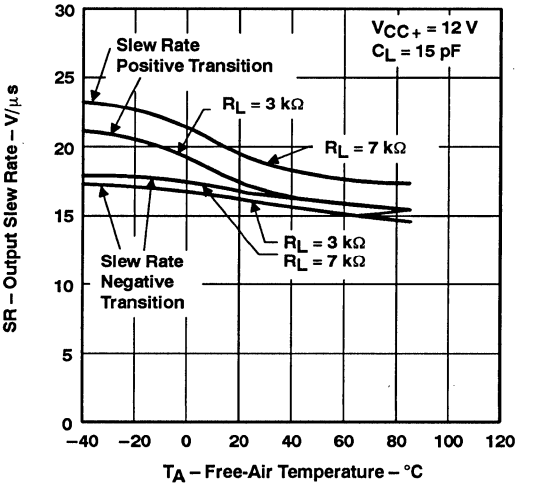


Figure 12

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE†

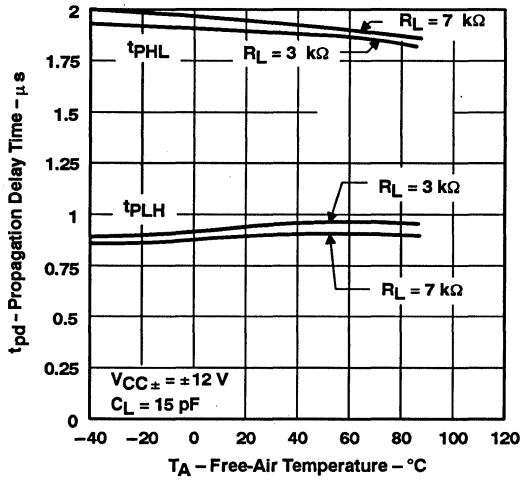


Figure 13

OUTPUT TRANSITION TIME
vs
FREE-AIR TEMPERATURE†

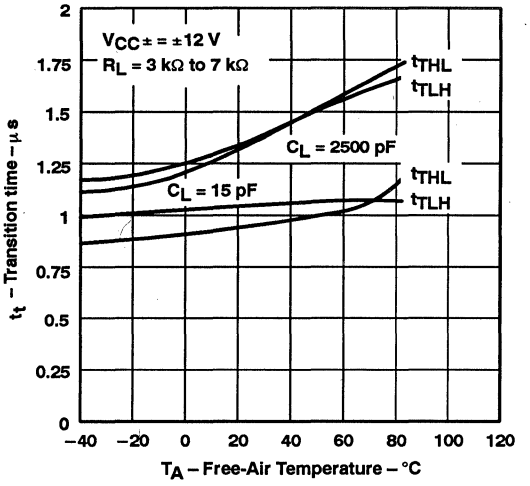


Figure 14

OUTPUT ENABLE TIME TO HIGH LEVEL
vs
FREE-AIR TEMPERATURE†

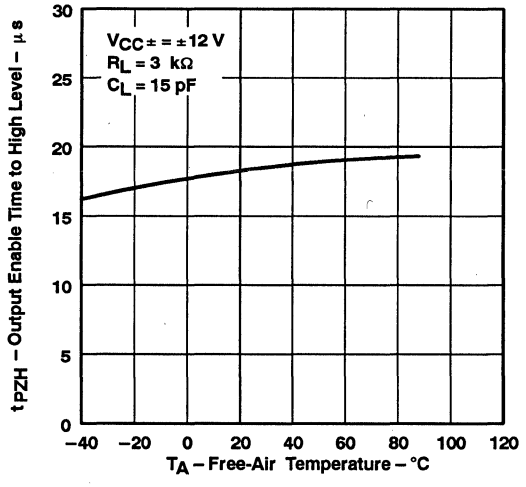


Figure 15

OUTPUT DISABLE TIME FROM HIGH LEVEL
vs
FREE-AIR TEMPERATURE†

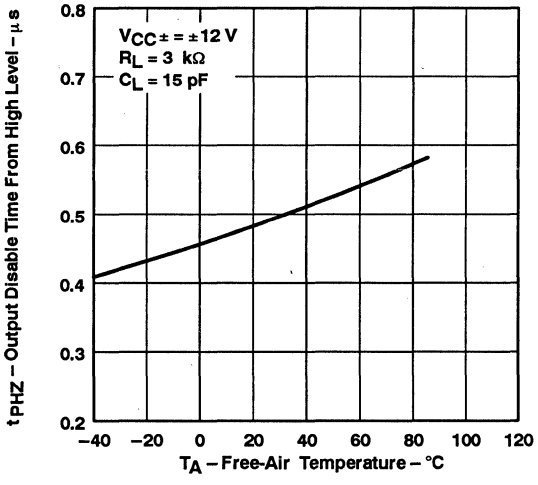


Figure 16

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

TYPICAL CHARACTERISTICS

OUTPUT ENABLE TIME TO LOW LEVEL vs FREE-AIR TEMPERATURE†

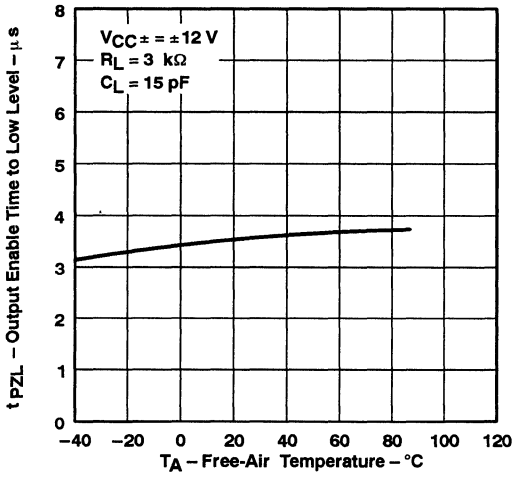


Figure 17

OUTPUT DISABLE TIME FROM LOW LEVEL vs FREE-AIR TEMPERATURE†

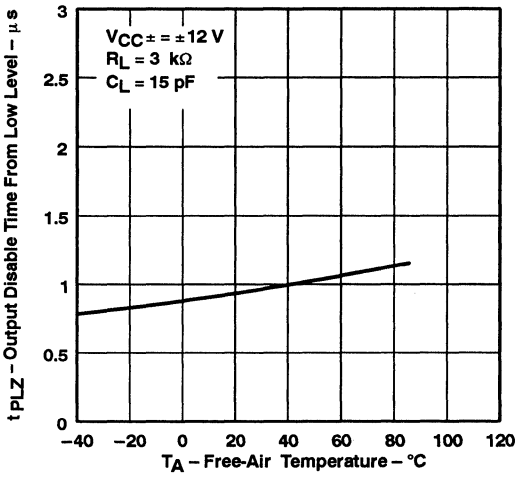


Figure 18

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

- **Meets CCITT Recommendations V.10, V.11, X.26, and X.27**
- **–7 V to 7 V Common-Mode Input Voltage Range With 300-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

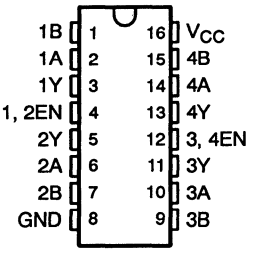
description

The SN75ALS199 is a monolithic quad line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of CCITT Recommendation V.10, V.11, X.26 and X.27.

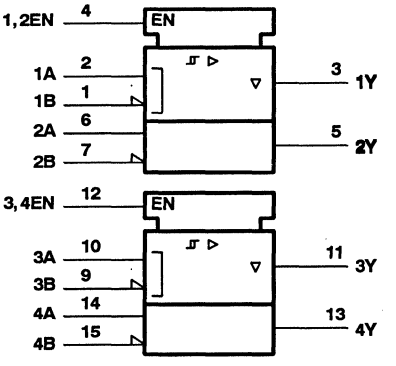
The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the ouptuts will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of ±7 V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

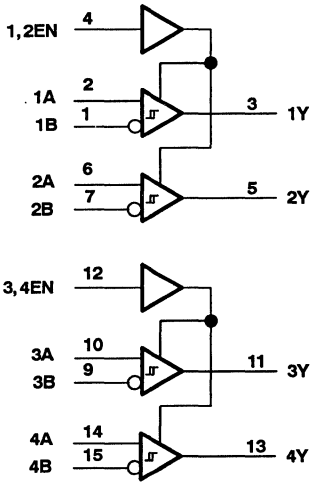


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

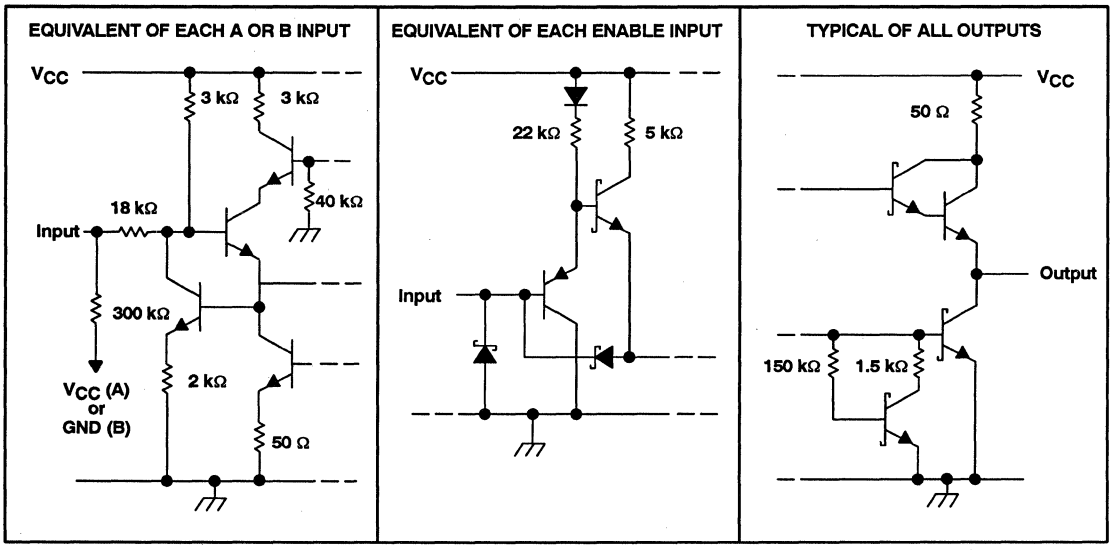


FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	EN	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	H
-0.3 V $< V_{ID} < 0.3$ V	H	?
$V_{ID} \leq -0.3$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,
? = indeterminate, Z = high impedance (off)

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Enable input voltage ..... 7 V
Low-level output current ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage					300	mV
V_{T-}	Negative-going threshold voltage			–300‡			mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				120		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = – 400 µA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = – 300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = – 3 V,	V_O = 2.7 V			20	µA
		V_{IL} = 0.8 V, V_{ID} = 3 V,	V_O = 0.5 V			–20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = –15 V		–1	–1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	µA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				–100	µA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current§	V_{ID} = 3 V,	V_O = 0	–15	–78	–130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to CCITT Recommendations V.10 and V.11 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = 0 V to 3 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

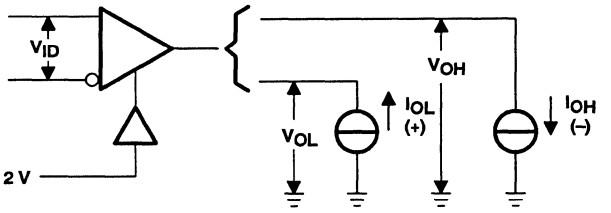
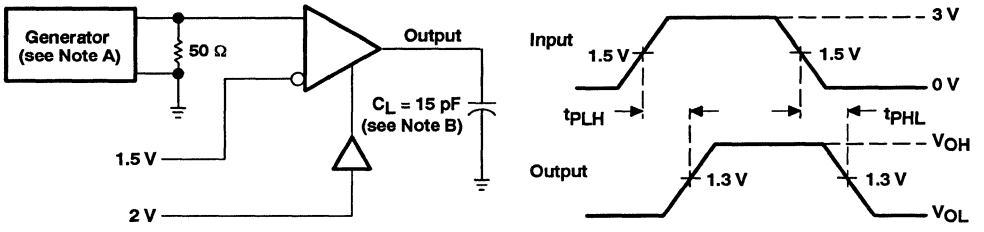


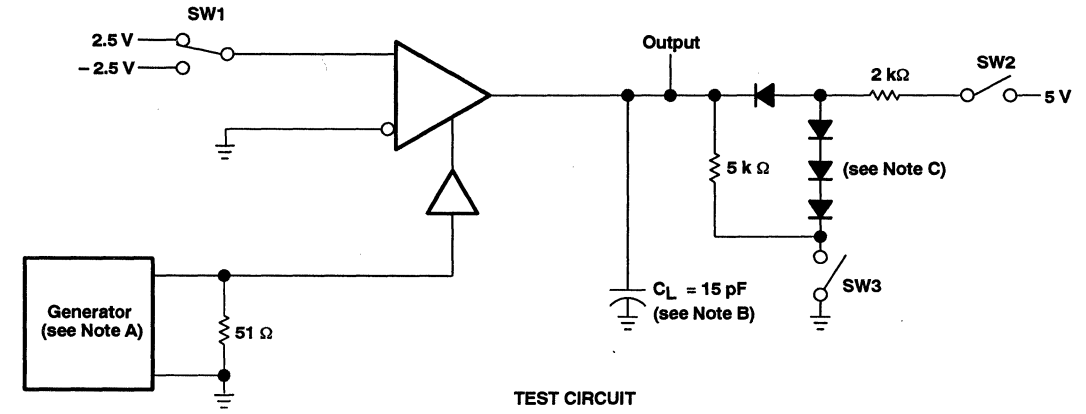
Figure 1. V_{OH}, V_{OL} Test Circuit



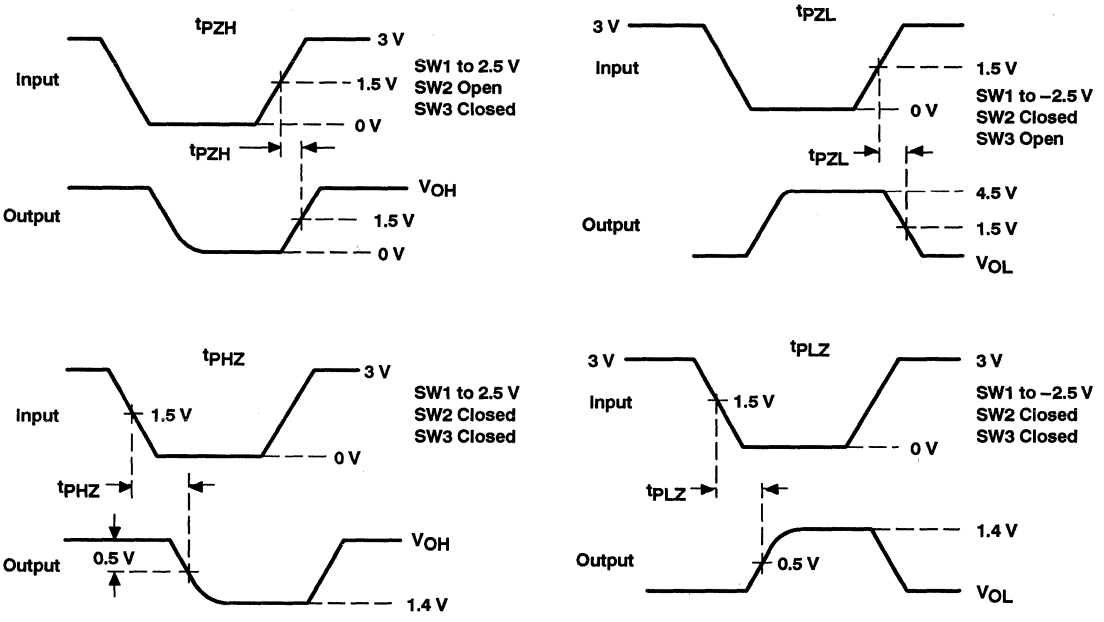
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

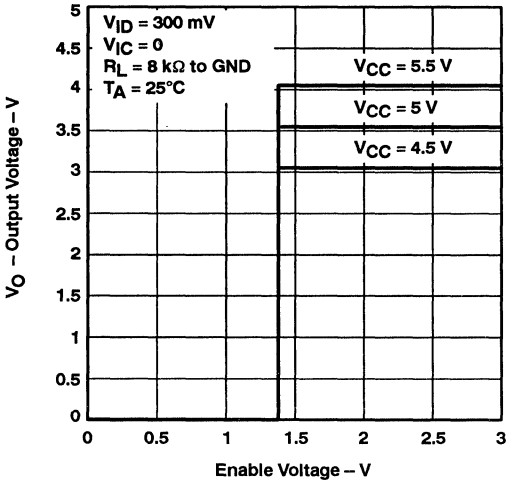


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

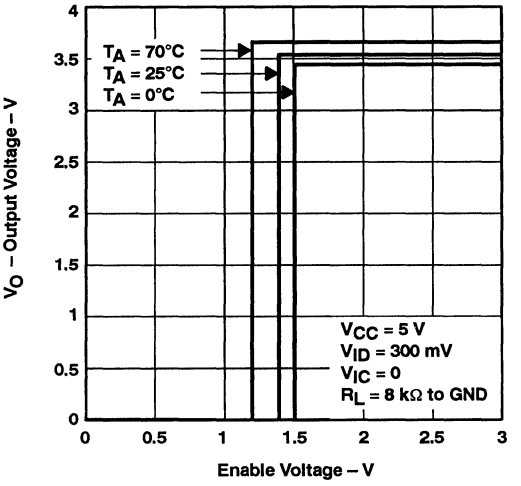


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

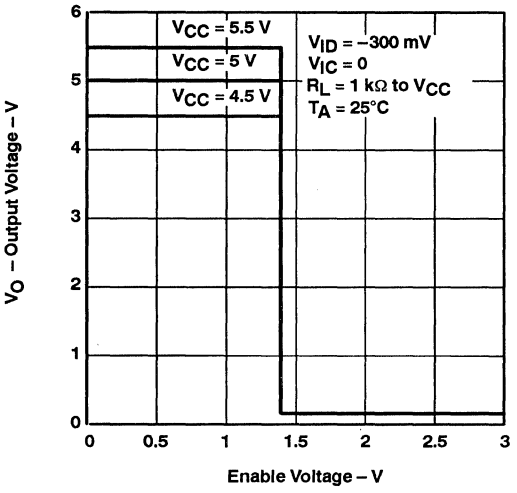


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

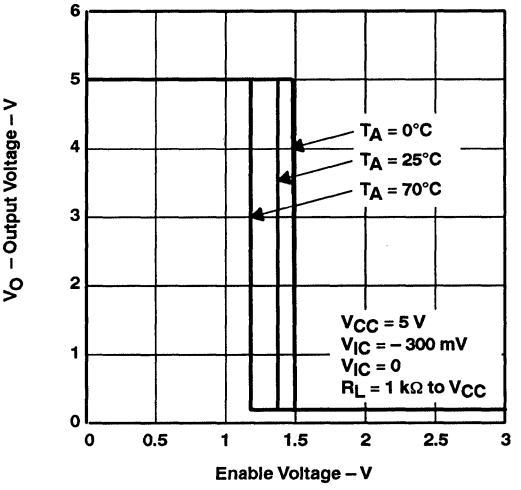


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

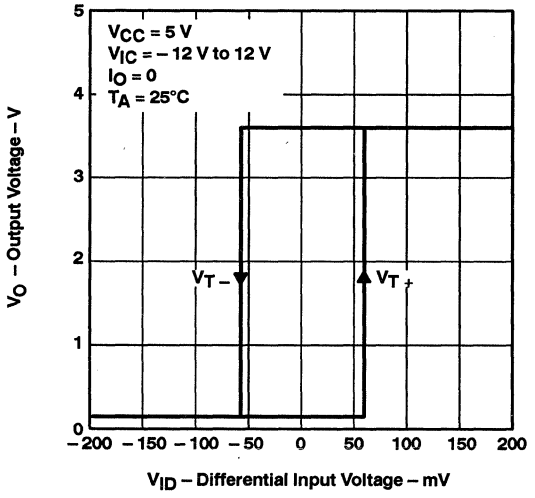


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

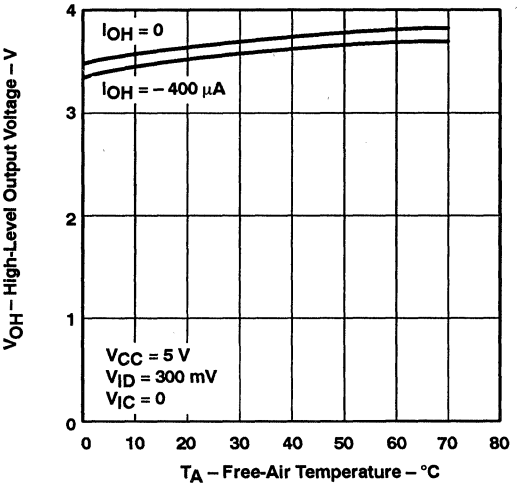


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

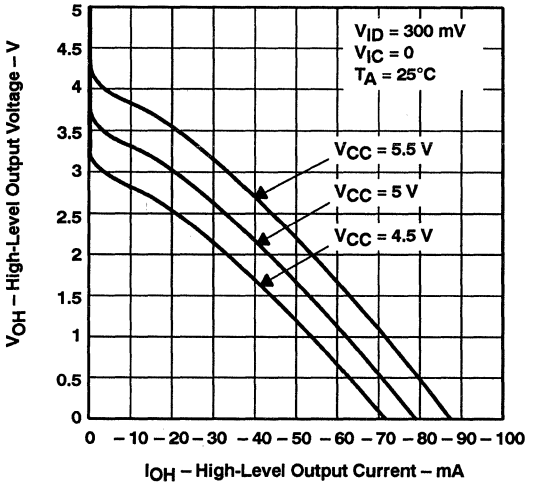


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

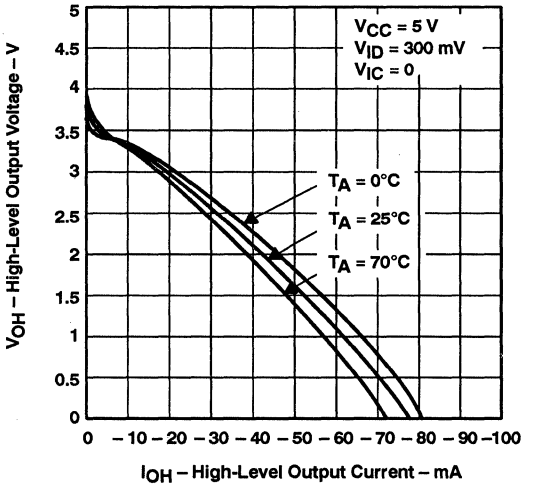


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

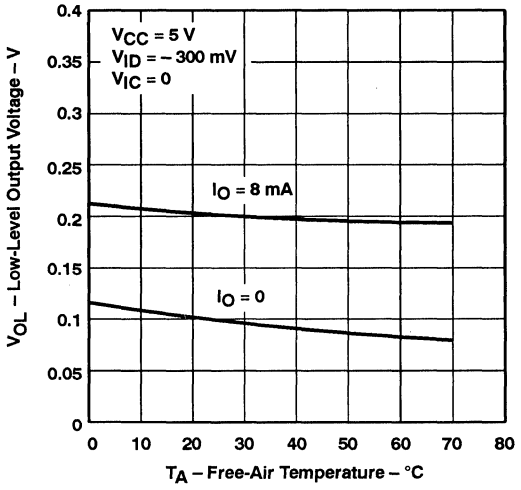


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

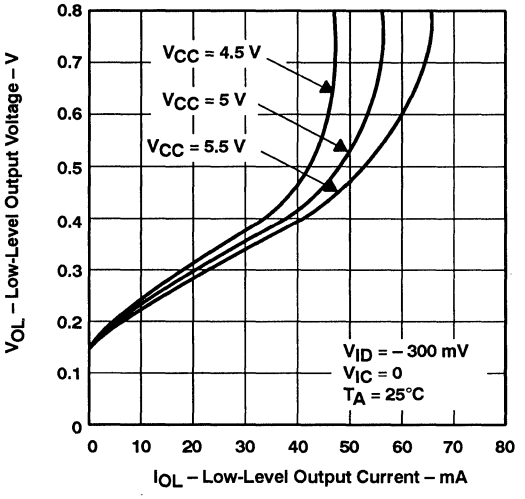


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

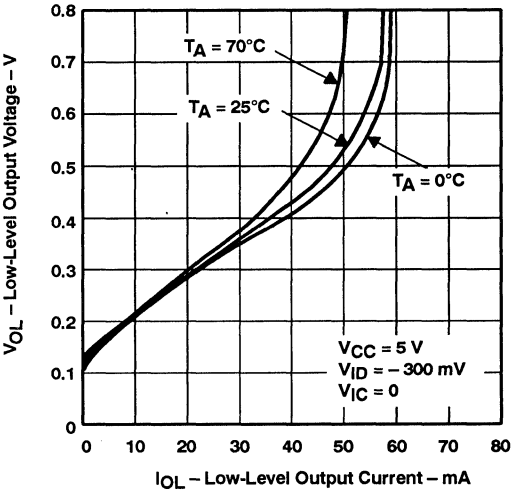


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

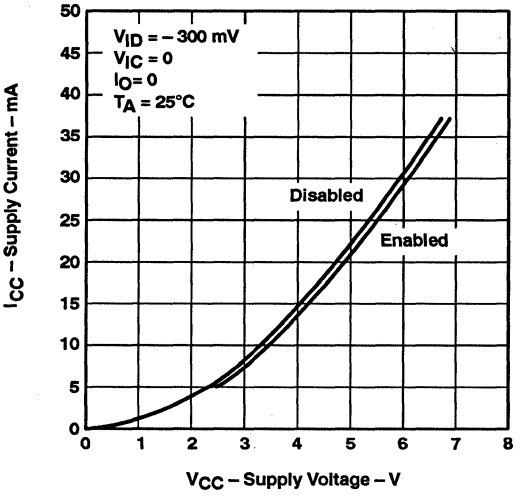


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

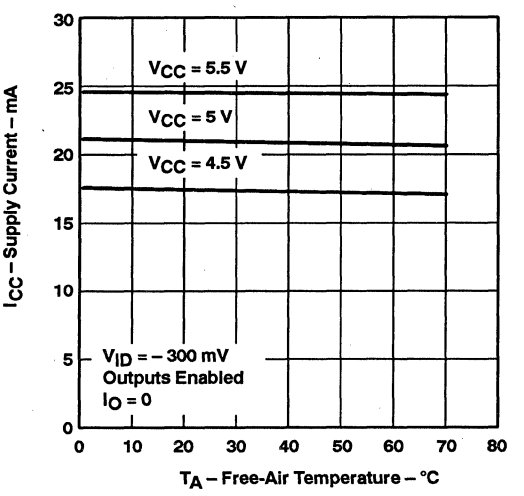


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

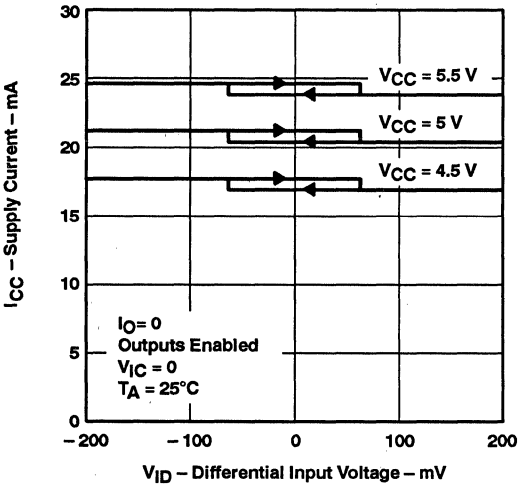


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

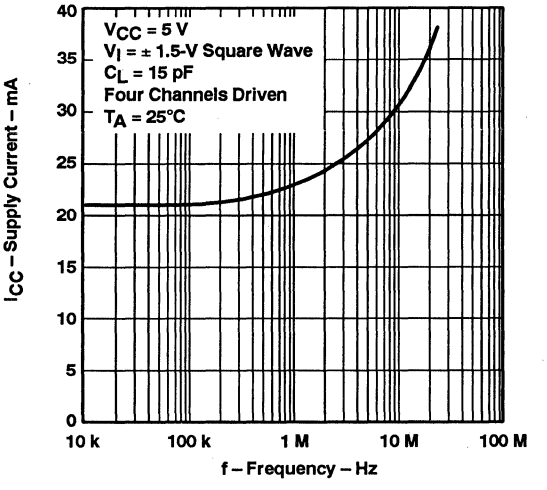


Figure 18

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TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

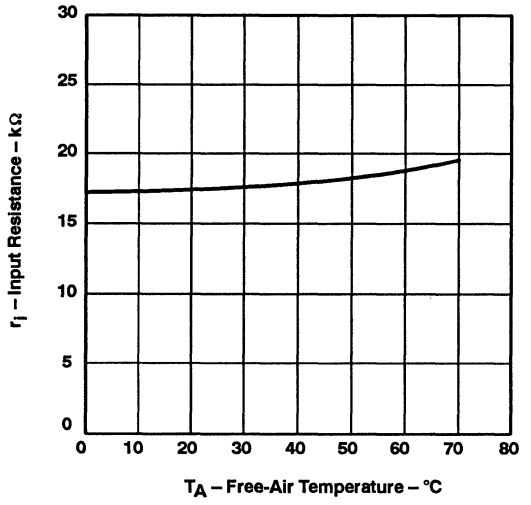


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

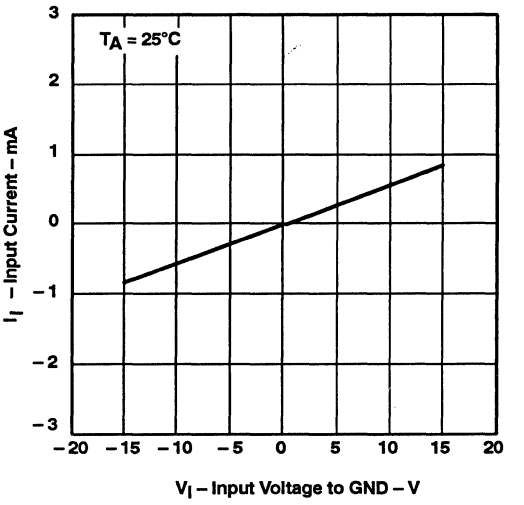


Figure 20

SWITCHING CHARACTERISTICS vs FREE-AIR TEMPERATURE

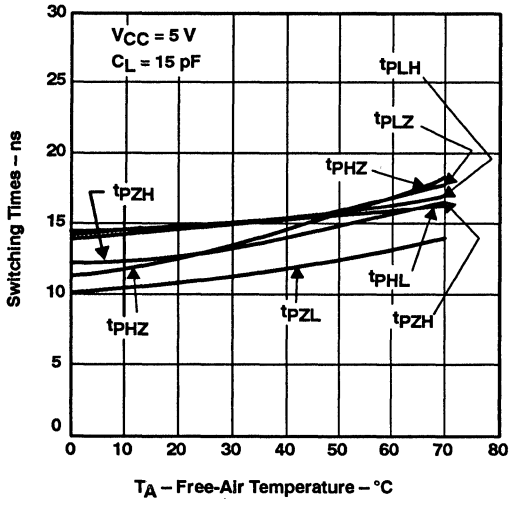


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

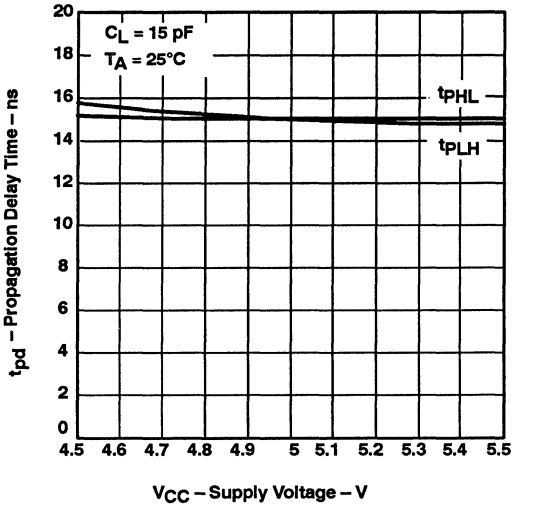
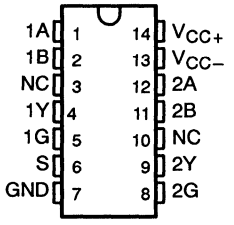


Figure 22

- **Plug-In Replacement for SN75107A and SN75107B With Improved Characteristics**
- **±10-mV Input Sensitivity**
- **TTL Compatible**
- **Standard Supply Voltages . . . ±5 V**
- **Differential Input Common-Mode Voltage Range of ±3 V**
- **Strobe Inputs for Channel Selection**
- **Totem-Pole Outputs**
- **SN75207B Has Diode-Protected Input Stage for Power-Off Condition**
- **Sense Amplifier for MOS Memories**
- **Dual Comparator**
- **High-Sensitivity Line Receiver**

D OR N PACKAGE
(TOP VIEW)

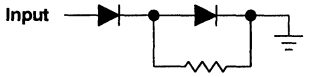


NC – No internal connection

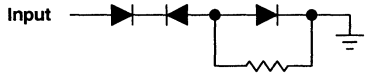
description

The SN75207 and SN75207B are pin-for-pin replacements for the SN75107A and SN75107B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pullup output.

The essential difference between the SN75207 and SN75207B can be seen in the schematics. Input protection diodes are in series with the collectors of the differential-input transistors of the SN75207B. These diodes are useful in certain party-line systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



SN75207



SN75207B

This would be a problem in specific systems that might have the transmission lines biased to some potential greater than 1.4 V.

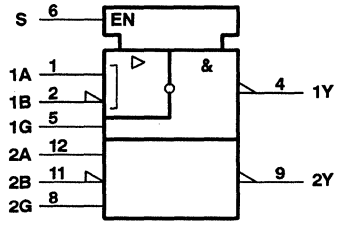
These devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} < 10$ mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

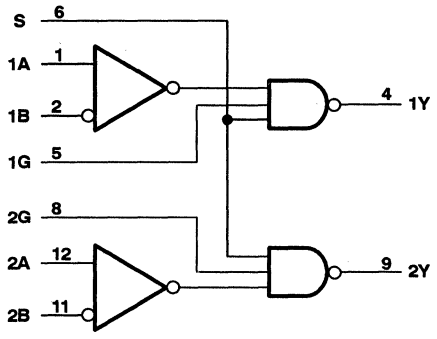
H = high level, L = low level, X = irrelevant

logic symbol†

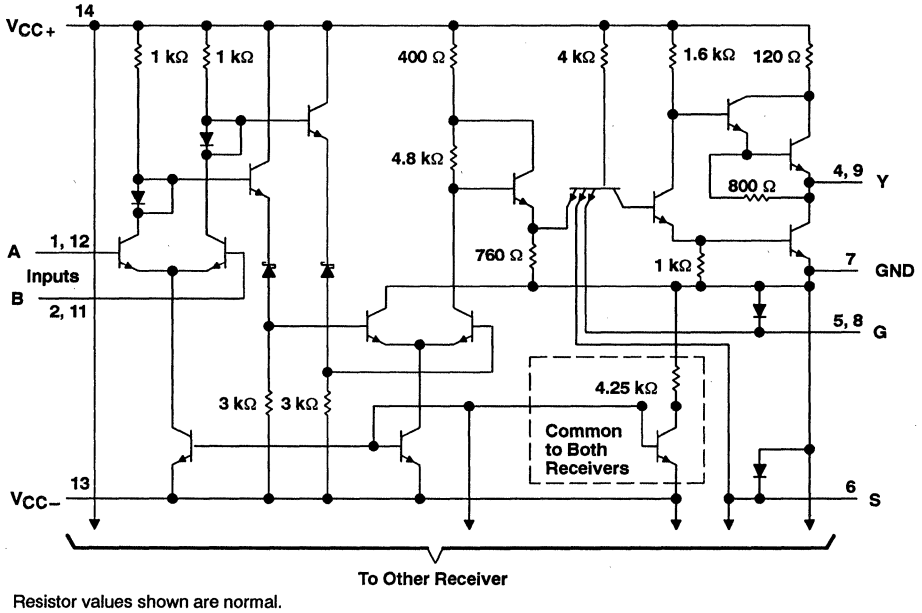


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are normal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

design characteristics

The '207 and '207B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. The dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 V. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to ensure 400 mV of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 mV typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10-mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 7 V
Supply voltage, V_{CC-} (see Note 1) ..... −7 V
Differential input voltage, V_{ID} (see Note 2) ..... ±6 V
Common-mode input voltage, V_{IC} (see Note 3) ..... ±5 V
Strobe input voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to ground terminal.
2. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

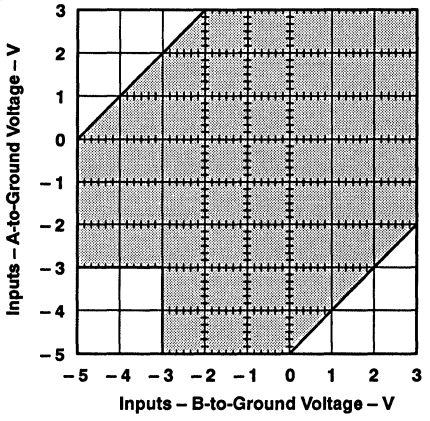
PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1050 mW	9.2 mW/°C	736 mW

recommended operating conditions (see Note 4)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level differential input voltage, V_{IDH} (see Note 5)	0.01		5	V
Low-level differential input voltage, V_{IDL}	−5†		−0.01	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	−3†		3	V
Input voltage, any differential input to ground (see Note 5)	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	V
Low-level output current, I_{OL}			−16	mA
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure shown.
6. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.



electrical characteristics over recommended free-air temperature range (unless otherwise noted)

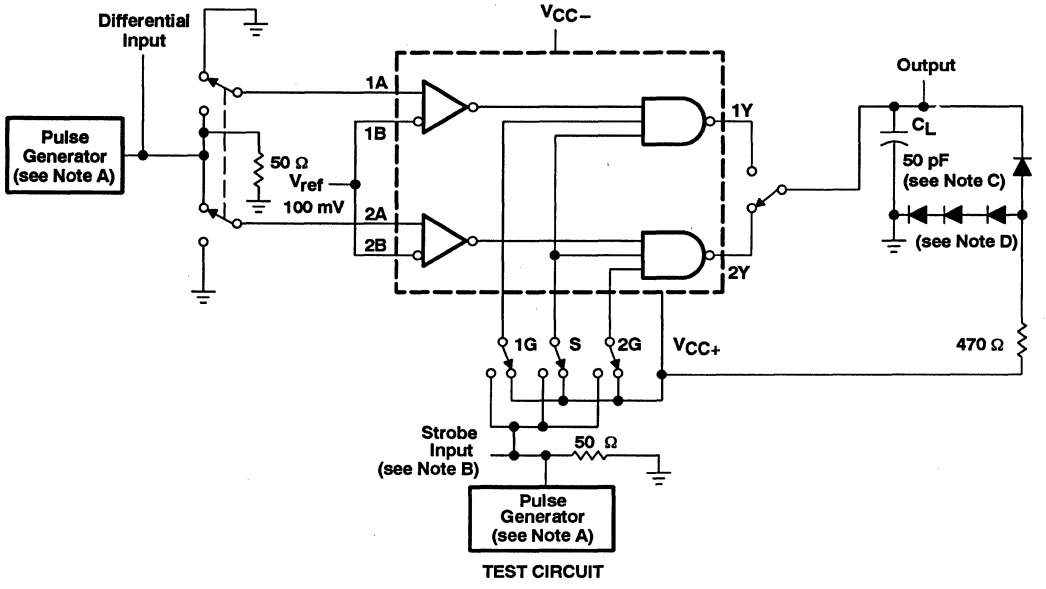
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	'207	$V_{CC\pm}$ = ± 5.25 V	V_{ID} = 5 V			30	75	µA
		'207B		V_{ID} = −5 V			30	75	
I_{IL}	Low-level input current	'207	$V_{CC\pm}$ = ± 5.25 V	V_{ID} = −5 V				−10	µA
		'207B		V_{ID} = 5 V				−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = 2.4 V				40	µA
			$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = ± 5.25 V				1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = ± 5.25 V,	$V_{IL(S)}$ = 0.4 V				−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = 2.4 V				80	µA
			$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = ± 5.25 V				2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = ± 5.25 V,	$V_{IL(S)}$ = 0.4 V				−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ± 4.75 V, I_{OH} = −400 µA,	$V_{IL(S)}$ = 0.8 V, V_{IC} = −3 V to 3 V	V_{IDH} = 10 mV,	2.4			V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ± 4.75 V I_{OL} = 16 mA,	$V_{IH(S)}$ = 2 V, V_{IC} = −3 V to 3 V	V_{IDL} = −10 mV,			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = ± 4.75 V,	V_{OH} = ±5.25 V				400	µA
I_{OS}	Short-circuit output current‡		$V_{CC\pm}$ = ± 5.25 V			−18		−70	mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = ± 5.25 V,	T_A = 25°C			18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = ± 5.25 V,	T_A = 25°C			−8.4	−15	mA

† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

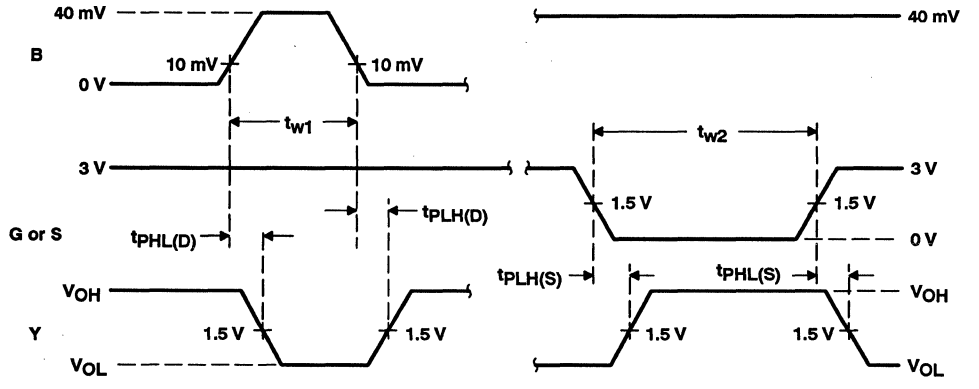
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high level output, from differential inputs A and B	R_L = 470 Ω, C_L = 50 pF, See Figure 1		35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low level output, from differential inputs A and B			20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high level output, from strobe input G or S			17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low level output, from strobe input G or S			17	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \le 5$ ns, $t_f \le 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 μs with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

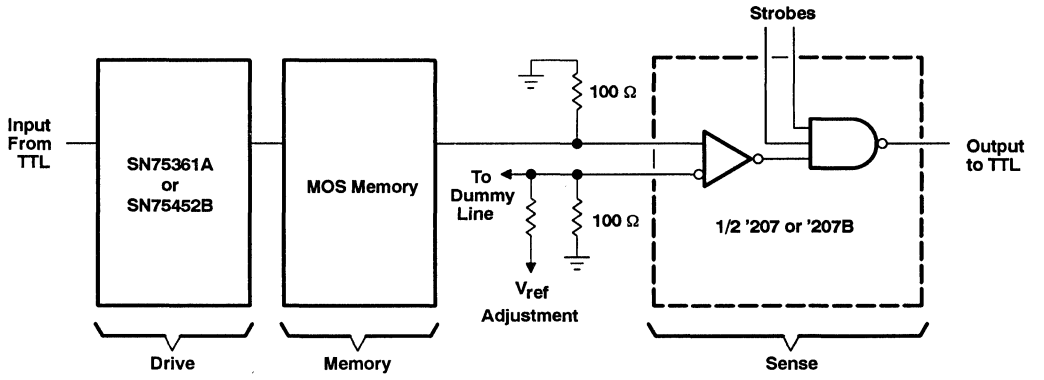
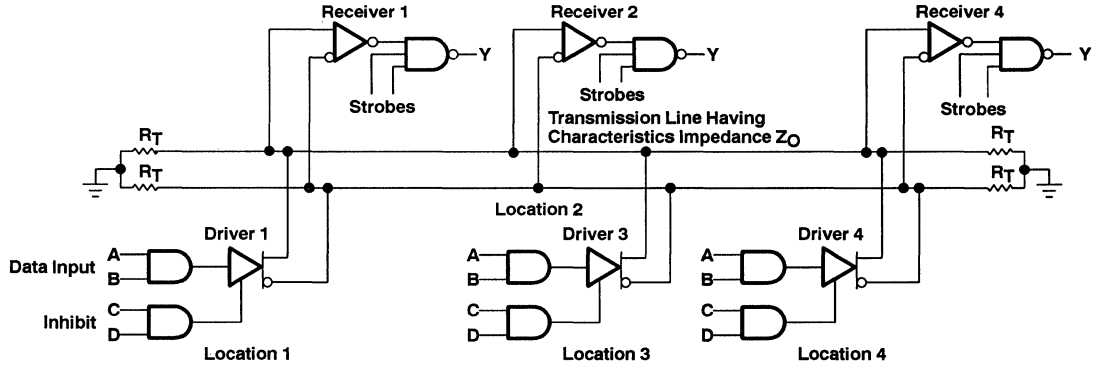


Figure 2. Mos Memory Sense Amplifier



Receivers are '207 or '207B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

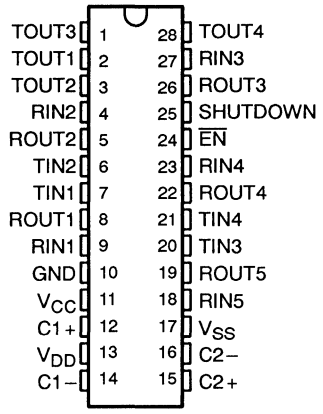
Figure 3. Data-Bus or Parity-Line System

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between –3 V and 3 V, preferably at GND. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

SLLS137C – D4027, MAY 1992 – REVISED APRIL 1993

- **Operates With Single 5-V Power Supply**
- **Meets EIA/TIA-232-E, 1991 Specifications (Revision of EIA-232-D and CCITT V.28)**
- **Improved Performance Replacement for MAX241**
- **ESD Protection on EIA/TIA-232 Pins Exceeds 6 kV ESD Per MIL-STD-883C, Method 3015**
- **Operates at Data Rates Up to 100 kb/s Over a 3-Meter Cable**
- **Low Power Shutdown Mode: ≤1 μA Typ**
- **LinBiCMOS™ Process Technology**
- **4 Drivers and 5 Receivers**
- **±30-V Input Levels**
- **3-State TTL/CMOS Receiver Outputs**
- **±9-V Output Swing With a 5-V Supply**
- **Applications**
  - **EIA-232 Interface**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC241† is a low-power LinBiCMOS™ line interface device containing four independent drivers and five receivers. It is designed to provide a plug-in replacement for the Maxim MAX241 with improved ESD protection and other key performance specifications. The SN75LBC241 provides a capacitive charge-pump voltage generator to produce EIA/TIA-232 voltage levels from a 5-V supply. The charge-pump oscillator frequency is 20 kHz. Each receiver converts EIA/TIA-232 inputs to 5-V TTL/CMOS levels. The receivers have a typical threshold of 1.2 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA/TIA-232 levels.

The SN75LBC241 includes a receiver 3-state control line and a low-power shutdown control line. Whenever, the $\overline{EN}$ line is high, the receiver outputs are placed in a high-impedance state. When $\overline{EN}$ is low, normal operation is enabled.

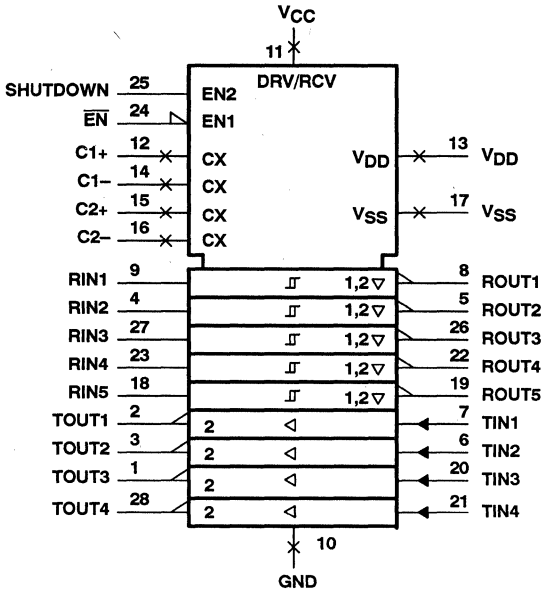
The shutdown mode reduces power dissipation to less than 5 μW typical. In this mode, receiver outputs are high impedance, driver outputs are turned off, and the charge-pump circuit is turned off. When the SHUTDOWN line is high, the shutdown mode is enabled. When the SHUTDOWN line is low, normal operation is enabled.

This device has been designed to conform to standard EIA/TIA-232-E, 1991 and CCITT V.28 specifications.

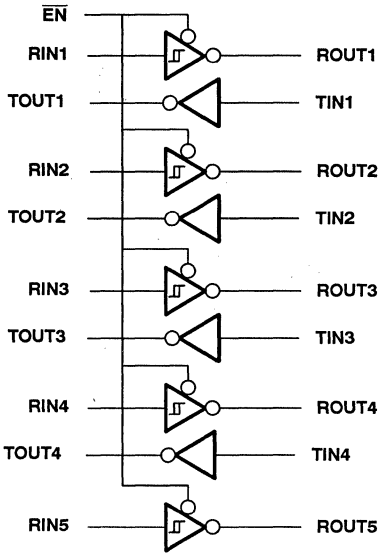
The SN75LBC241 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. Use of LinBiCMOS™ circuitry increases latch-up immunity in this device over an all-CMOS design. The SN75LBC241 is characterized for operation from 0°C to 70°C.

† Patent pending
LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Positive output supply voltage range, V_{DD} ..... V_{CC} − 0.3 V to 15 V
Negative output supply voltage range, V_{SS} ..... 0.3 V to −15 V
Input voltage range: Driver ..... −0.3 V to V_{CC} + 0.3 V
Receiver ..... ±30 V
Output voltage range: TOUT ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
ROUT ..... −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: TOUT ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1348 mW	10.8 mW/°C	863 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	TIN	2			V
	$\overline{EN}$, SHUTDOWN	2.4			
Low-level input voltage, V_{IL}	TIN, $\overline{EN}$, SHUTDOWN			0.8	V
External charge-pump capacitor	C1, C2 (see Figure 1)	1			μF
	C3, C4 (see Figure 1)	1			
External charge-pump capacitor voltage rating	C1, C3 (see Figure 1)	6.3			V
	C2, C4 (see Figure 1)	16			
Receiver input voltage, RIN				±30	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TOUT	R_L = 3 kΩ to GND,	See Note 2	5	9		V
		ROUT	I_{OH} = −1 mA		3.5			
V_{OL}	Low-level output voltage	TOUT	R_L = 3 kΩ to GND,	See Note 3		−9‡	−5	V
		ROUT	I_{OL} = 3.2 mA				0.4	
V_{T+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{T-}	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)	RIN	V_{CC} = 5 V			0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5 V,	T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	TOUT	$V_{DD} = V_{SS} = V_{CC}$ = 0,	V_O = ±2 V	300			Ω
I_{OS}	Short circuit output current§	TOUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short circuit input current	TIN	V_I = 0				200	μA
I_{CC}	Supply current		V_{CC} = 5.5 V, All output open	T_A = 25°C,		4	8	mA
			All outputs open, Shutdown pin high	T_A = 25°C,		1	10	μA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at one time.

NOTES: 2. Total I_{OH} drawn from TOUT1, TOUT2, TOUT3, TOUT4 and V_{DD} pins should not exceed 12 mA.

3. Total I_{OL} drawn from TOUT1, TOUT2, TOUT3, TOUT4 and V_{SS} pins should not exceed −12 mA.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low-to-high-level output	See Figure 2			500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high-to-low-level output	See Figure 2			500		ns
t_{PZH}	Receiver output enable time to high level	See Figure 5			100		ns
t_{PZL}	Receiver output enable time to low level	See Figure 5			100		ns
t_{PHZ}	Receiver output disable time from high level	See Figure 5			50		ns
t_{PLZ}	Receiver output disable time from low level	See Figure 5			50		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ,	See Figure 4			30	V/μs
$SR_{(tr)}$	Driver transition region slew rate	C_L = 2500 pF,	See Figure 4	4	6		V/μs

APPLICATION INFORMATION

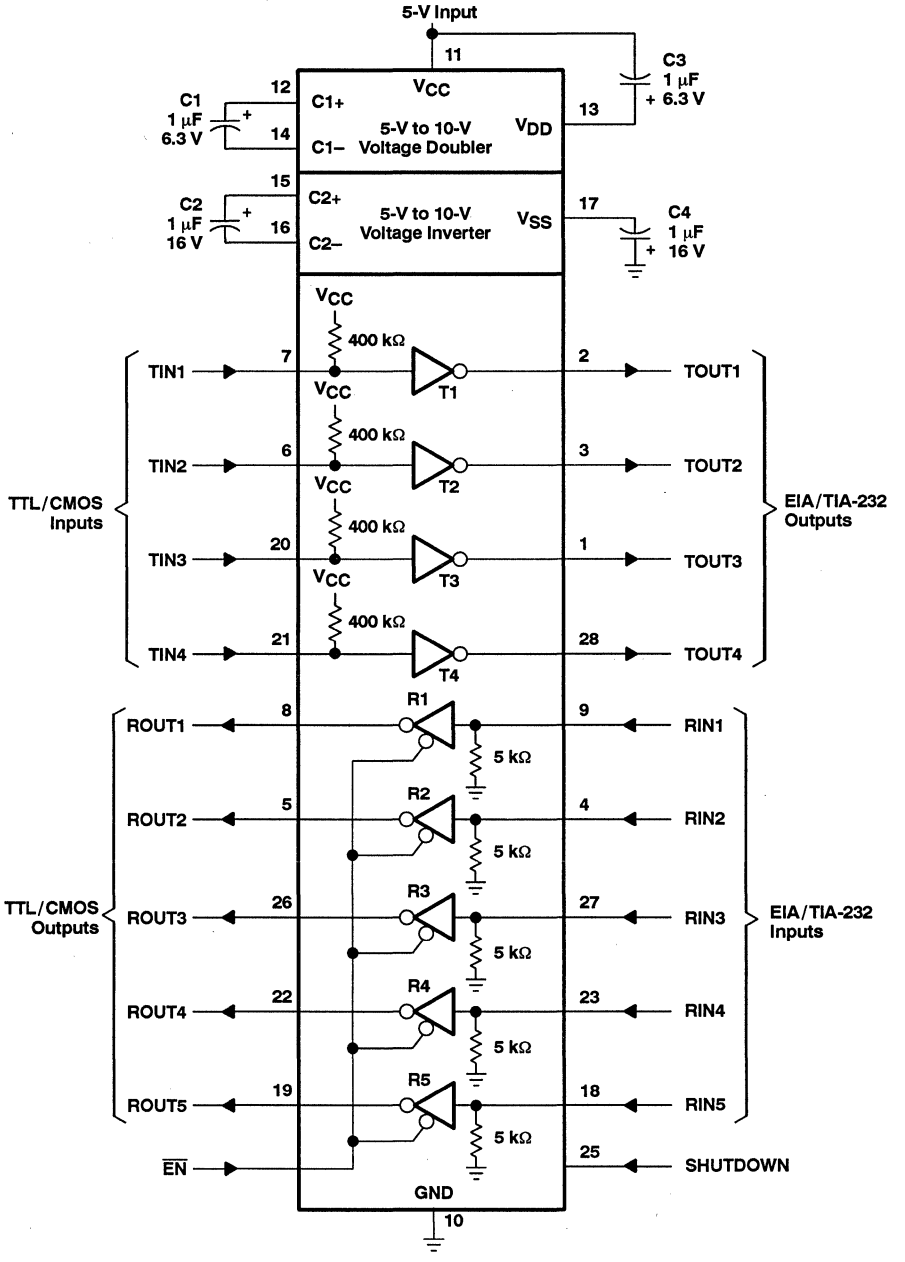


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION

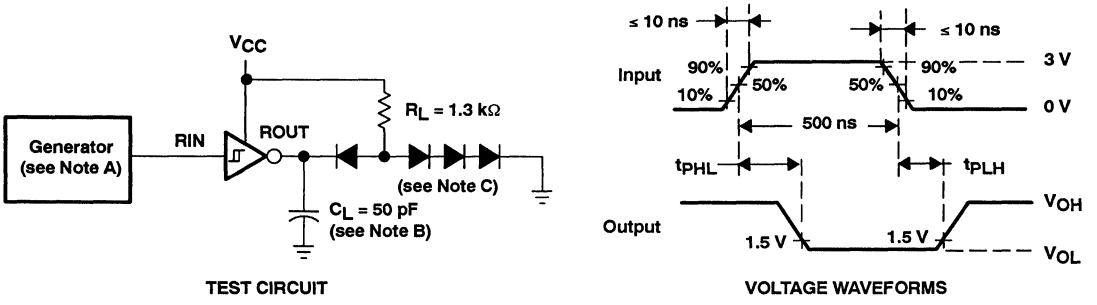


Figure 2. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement

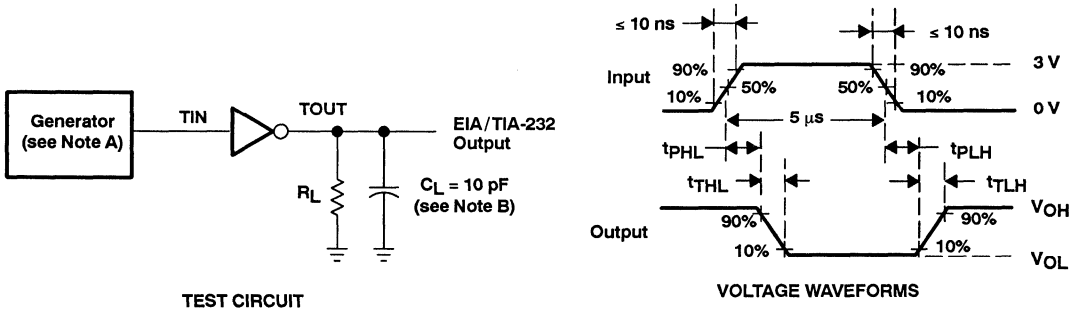


Figure 3. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5-μs Input)

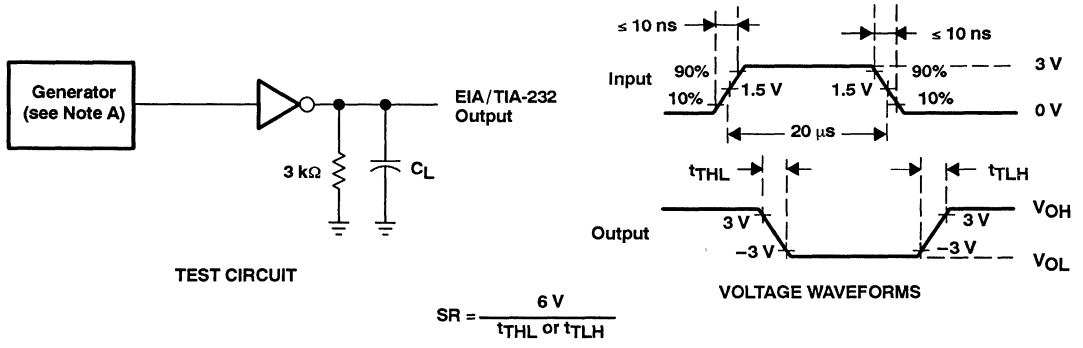


Figure 4. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20-μs Input)

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

PARAMETER MEASUREMENT INFORMATION

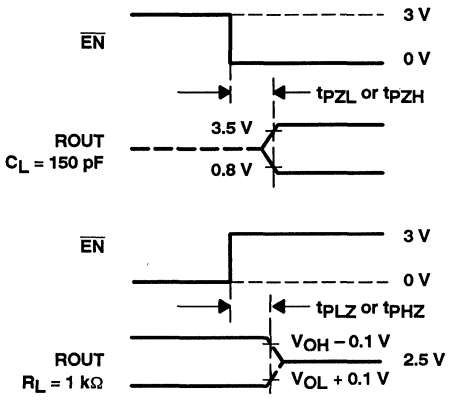
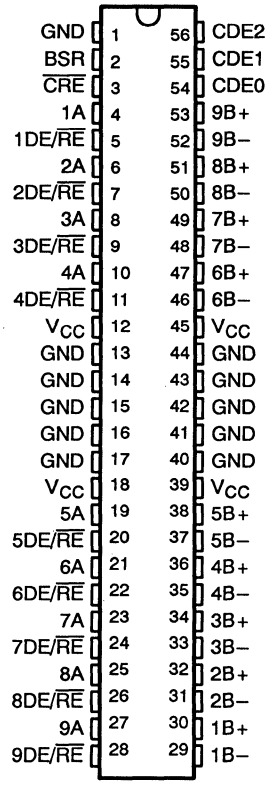


Figure 5. Receiver Output Enable and Disable Timing

SLLS133B – D4042, AUGUST 1992 – REVISED FEBRUARY 1993

- **9 Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI-2)**
- **Each Transceiver Meets EIA-RS-485 and ISO 8482:1987(E) Standards**
- **Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typical**
- **Thermal Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

DL PACKAGE
(TOP VIEW)



Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC976 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of Texas Instruments' LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential transceivers. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for both the Small Computer Systems Interface (SCSI) and the Intelligent Peripheral Interface (IPI-2) standard data interfaces. This part is ESD Class 1 (A) and Class 2 (B) per MIL-STD-883, Method 3015.

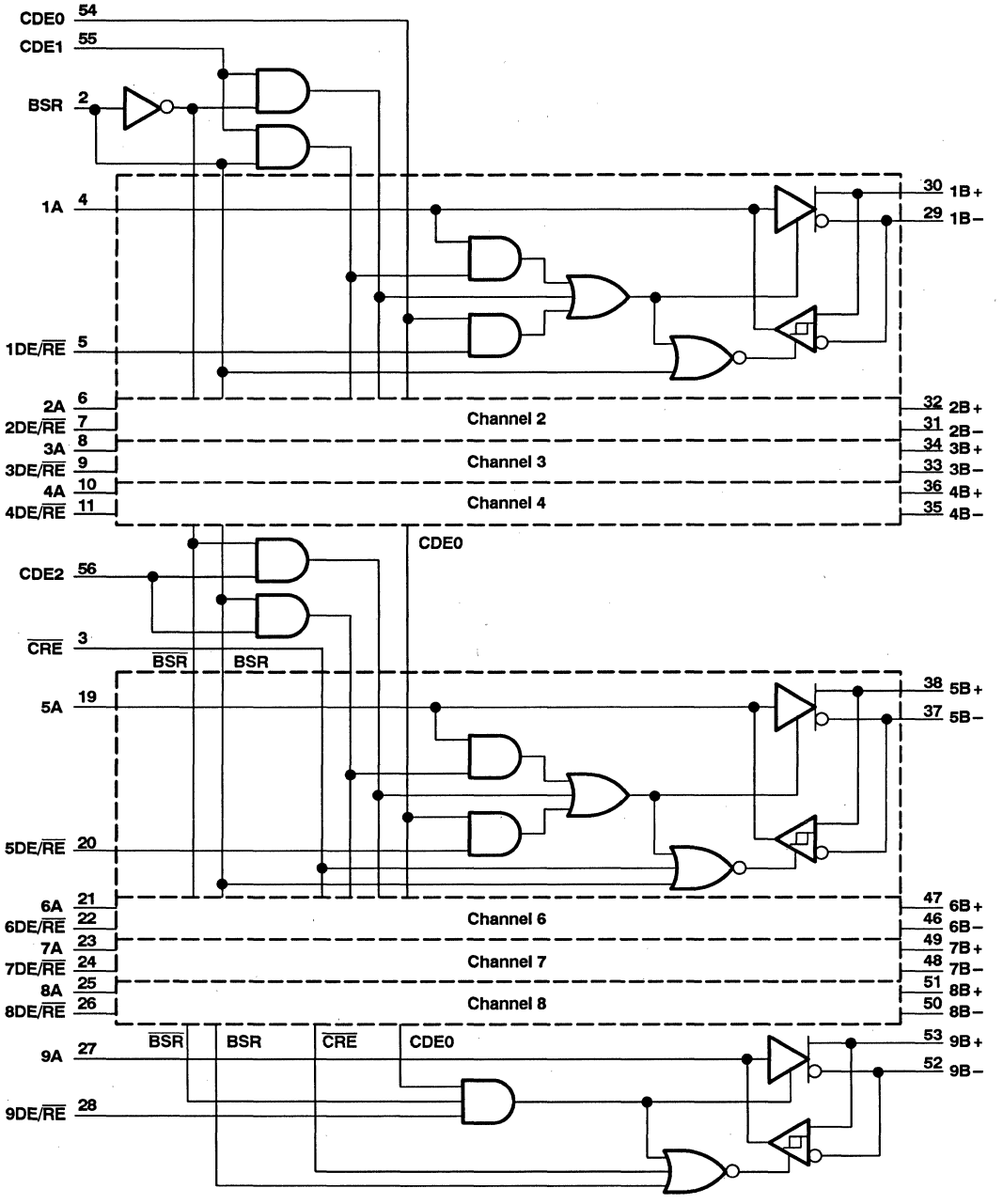
The SN75LBC976 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat sink pins. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed and testing of the SN75LBC976 is sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine channels conforms to the requirements of the EIA-RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.129-1986 (IPI), ANSI X3.131-1986 (SCSI-1), and the proposed SCSI-2 and SCSI-3 standards.

The SN75LBC976 is characterized for operation from 0°C to 70°C.

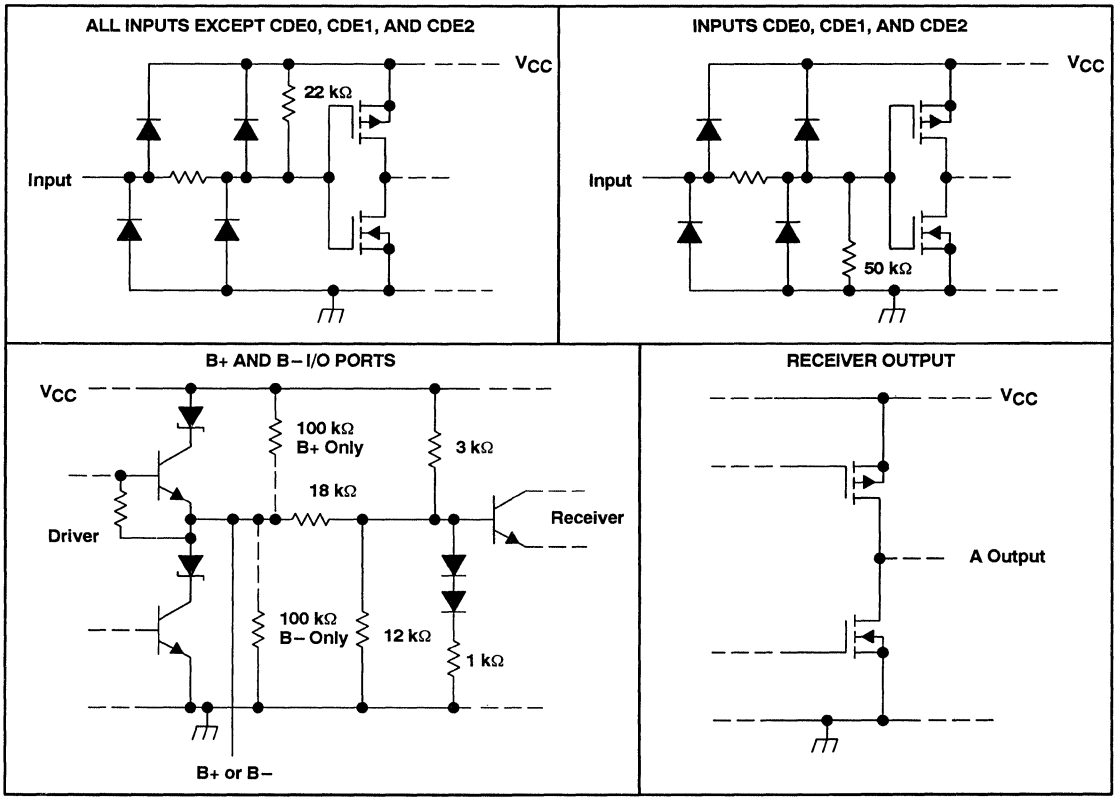
† Patent pending
LinASIC and LinBiCMOS are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)†



† For additional logic diagrams, see Application Information.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Bus voltage range	−10 V to 15 V
Data I/O and control (A-side) voltage range	−0.3 V to 7 V
Continuous power dissipation	internally limited
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values and with respect to the GND terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	B+ or B–			12	V
				–7	
High-level input voltage, V_{IH}	All except B+ and B–	2			V
Low-level input voltage, V_{IL}	All except B+ and B–			0.8	V
High-level output current, I_{OH}	B+ or B–			–60	mA
	A			–8	mA
Low-level output current, I_{OL}	B+ or B–			60	mA
	A			8	mA
Operating free-air temperature, T_A		0		70	°C

device electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	BSR, A, DE/$\overline{RE}$, and $\overline{CRE}$	See Figure 3	V_{IH} = 5 V			–100	µA
		CDE0, CDE1, and CDE2					100	µA
I_{IL}	Low-level input current	BSR, A, DE/$\overline{RE}$, and $\overline{CRE}$		V_{IL} = 0 V			–200	µA
		CDE0, CDE1, and CDE2			–50		50	µA
I_{CC}	Supply current	All drivers and receivers disabled	BSR and CDE0 at 5 V, Other inputs at 0 V			1.4	3	mA
		All receivers enabled	No load, V_{ID} = 5 V, All other inputs at 0 V			29	45	mA
		All drivers enabled	BSR at 0 V, No load, All other inputs at 5 V			4.8	10	mA
C_o	Bus port capacitance		B+ or B–			16		pF
C_{pd}	Power dissipation capacitance‡		One driver			460		pF
			One receiver			50		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_{pd} determines the no-load dynamic current consumption, $I_S = C_{pd} V_{CC} f + I_{CC}$.

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	V_{test} = –7 V to 12 V, See Figure 2	1	2		V
I_{OS}	Output short-circuit current	See Figure 1			±250	mA
I_{OZ}	High-impedance state output current	See receiver input current				

receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 3	I_{OH} = −8 mA,	2.5			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 3	I_{OL} = 8 mA,			0.8	V
V_{T+}	Positive-going threshold voltage	I_{OH} = −8 mA,	See Figure 3			0.2	V
V_{T-}	Negative-going threshold voltage	I_{OL} = 8 mA,	See Figure 3	−0.2			V
V_{hys}	Receiver input hysteresis ($V_{T+} - V_{T-}$)				45		mV
I_I	Receiver input current, B+ and B−	V_I = 12 V, Other input at 0 V,	V_{CC} = 5 V, See Figure 3		0.7	1	mA
		V_I = 12 V, Other input at 0 V,	V_{CC} = 0 V, See Figure 3		0.8	1	mA
		V_I = −7 V, Other input at 0 V,	V_{CC} = 5 V, See Figure 3		−0.5	−0.8	mA
		V_I = −7 V, Other input at 0 V,	V_{CC} = 0 V, See Figure 3		−0.4	−0.8	mA
I_{OZ}	High-impedance-state output current	See Figure 3	V_O = GND			−100	µA
			V_O = V_{CC}			50	

driver switching characteristics over recommended operating conditions (see Figure 4) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential delay time, high-to-low-level output (t_{dDH}) or low-to-high-level output (t_{dDL})			7.6		19.6	ns
		V_{CC} = 5 V,	T_A = 25°C	9.1		17.1	
		V_{CC} = 5 V,	T_A = 70°C	11.5		19.5	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		V_{CC} = 5 V,	See Note 2			8	
$t_{sk(p)}$	Pulse skew ($\lvert t_{dDL} - t_{dDH} \rvert$)				0	6	ns
t_t	Transistion time (t_r or t_f)				10		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: This specification applies to any 5°C band within the operating temperature range.

receiver switching characteristics over recommended operating conditions (see Figure 5) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, high-to-low-level output (t_{PLH}) or low-to-high-level output (t_{PHL})			21.5		33	ns
		V_{CC} = 5 V,	T_A = 25°C	22.6		31.6	
		V_{CC} = 5 V,	T_A = 70°C	23.4		32.4	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		V_{CC} = 5 V,	See Note 2			9	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				2	6	ns
t_t	Transition time (t_r or t_f)				3		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

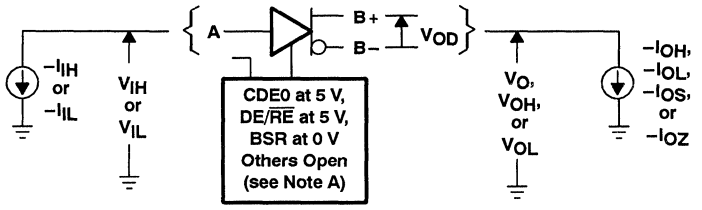
transceiver switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{enRX(L)}$	Enable time, transmit-to-receive to low-level output	See Figure 6		150	ns
$t_{enRX(H)}$	Enable time, transmit-to-receive to high-level output			150	ns
$t_{enTX(L)}$	Enable time, receive-to-transmit to low-level output			80	ns
$t_{enTX(H)}$	Enable time, receive-to-transmit to high-level output			80	ns
t_{su}	Setup time, CDE0, CDE1, CDE2, BSR, or $\overline{CRE}$ to active input(s) or output(s)		150		ns

thermal characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted,	No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance				12		°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: For the I_{OZ} test, the BSR input is at 5 V and all others are at 0 V.

Figure 1. Driver Test and Input Conditions

PARAMETER MEASUREMENT INFORMATION

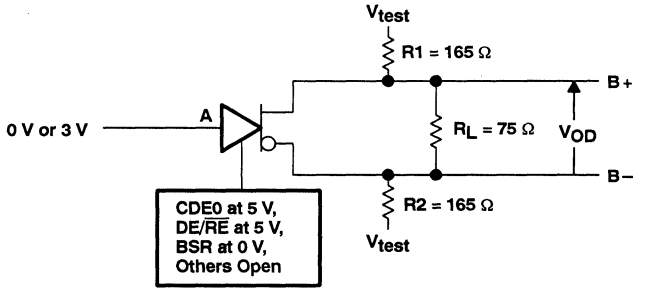
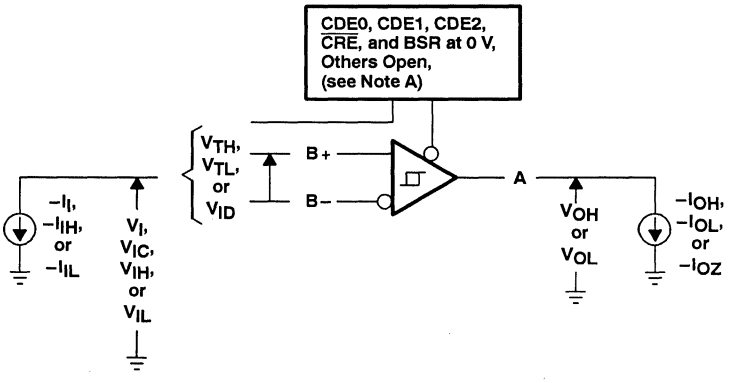


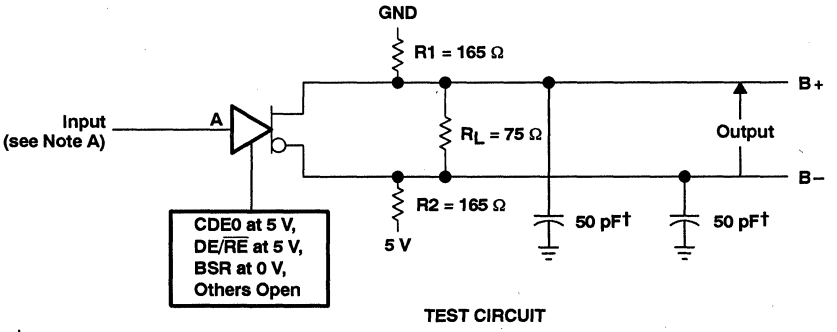
Figure 2. Driver V_{OD} Test Circuit



NOTE A: For the I_{OZ} measurement, BSR is at 5 V and CDE0, CDE1, and CDE2 are at 0 V.

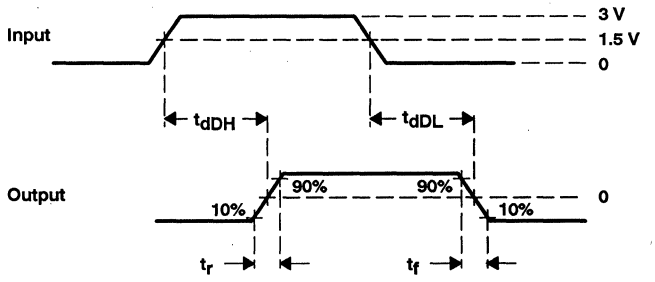
Figure 3. Receiver Test Circuit and Input Conditions

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

† Includes probe and jig capacitance.

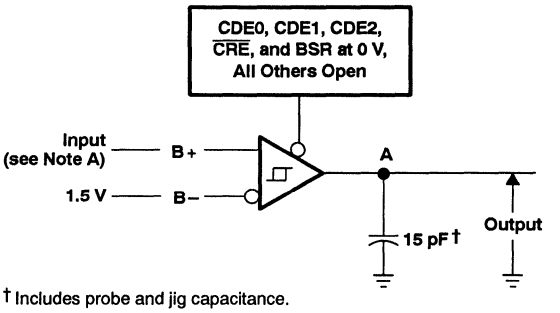


VOLTAGE WAVEFORMS

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

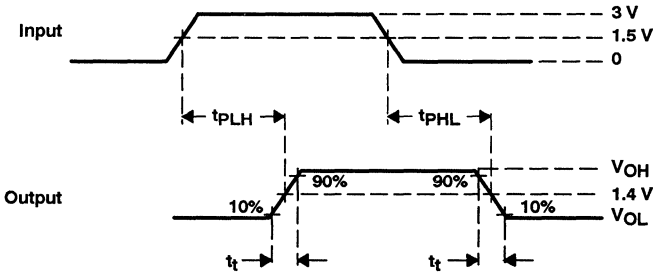
Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† Includes probe and jig capacitance.

TEST CIRCUIT

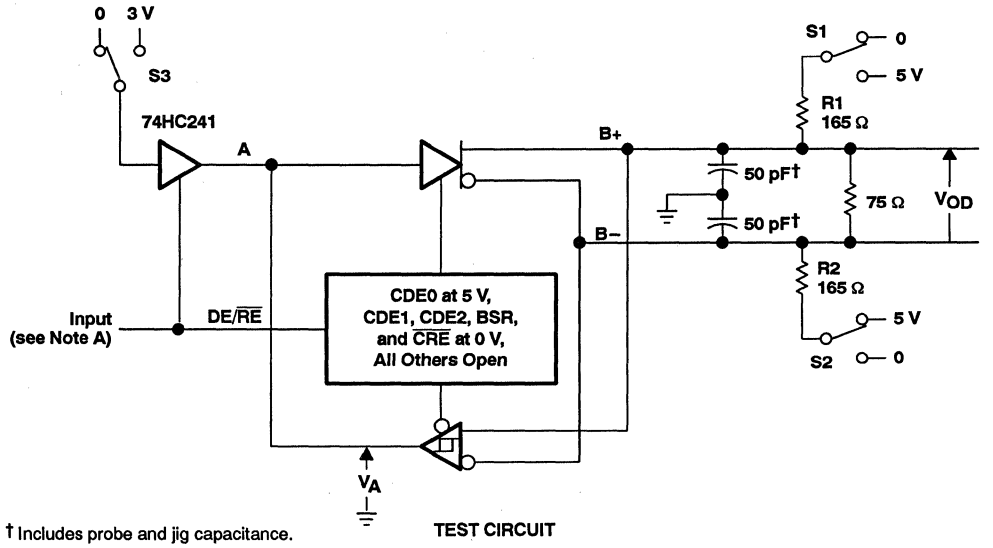


VOLTAGE WAVEFORMS

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

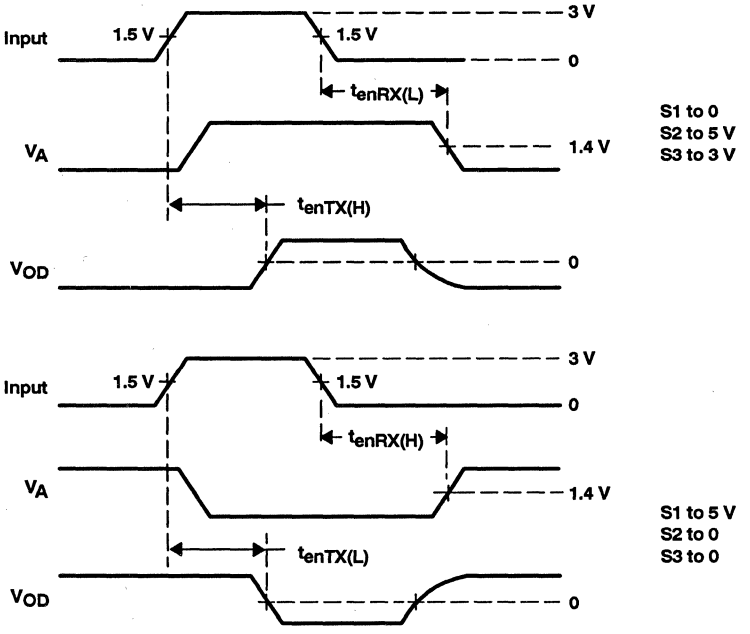
Figure 5. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† Includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 6. Enable and Disable Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

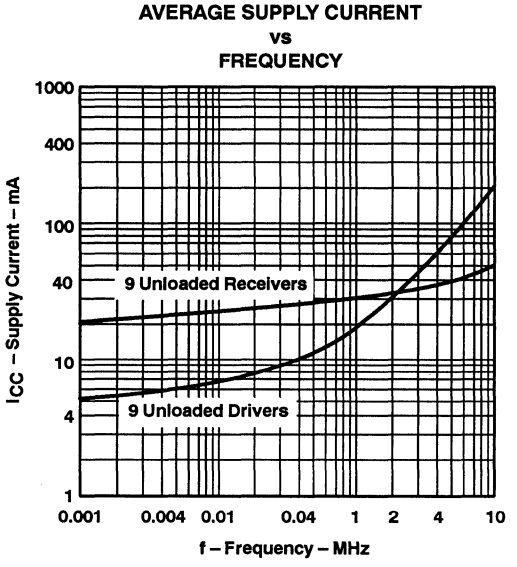


Figure 7

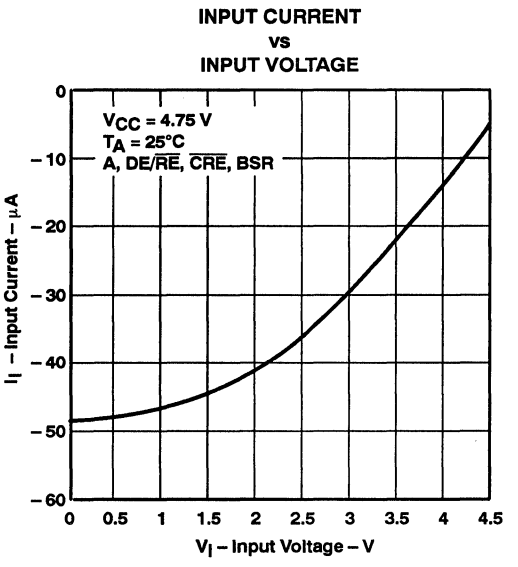


Figure 8

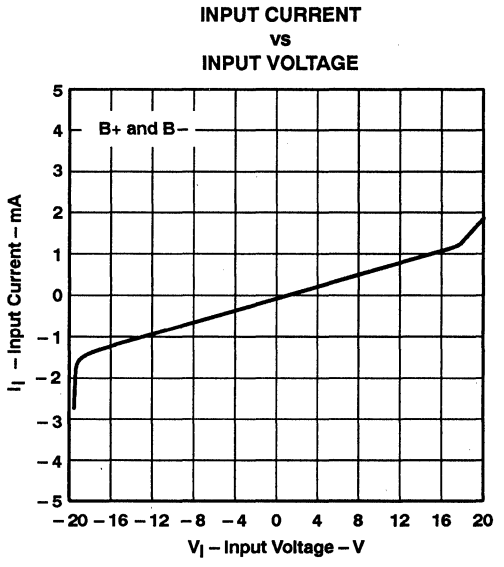


Figure 9

TYPICAL CHARACTERISTICS

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

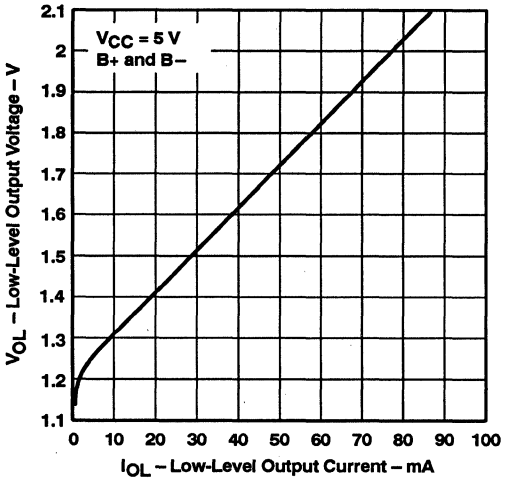


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

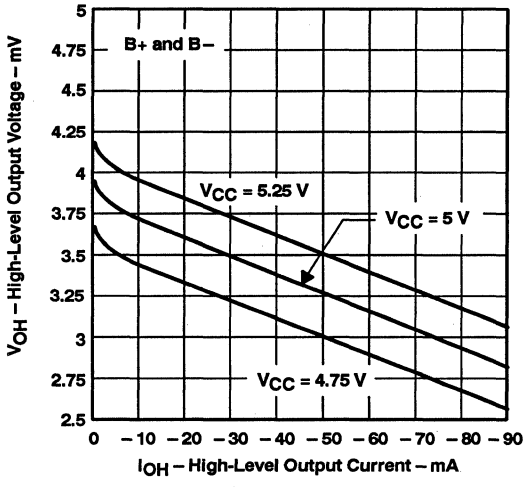


Figure 11

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

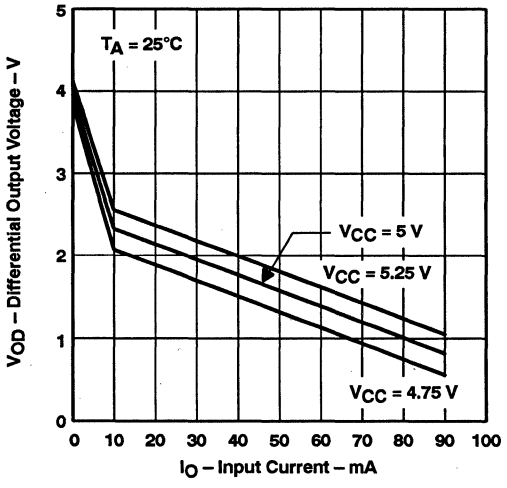


Figure 12

TYPICAL CHARACTERISTICS

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

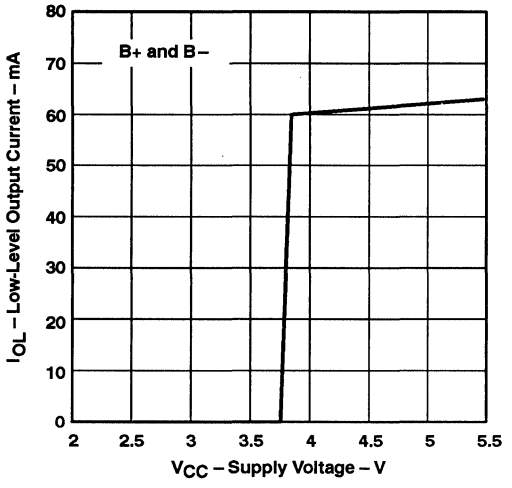


Figure 13

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

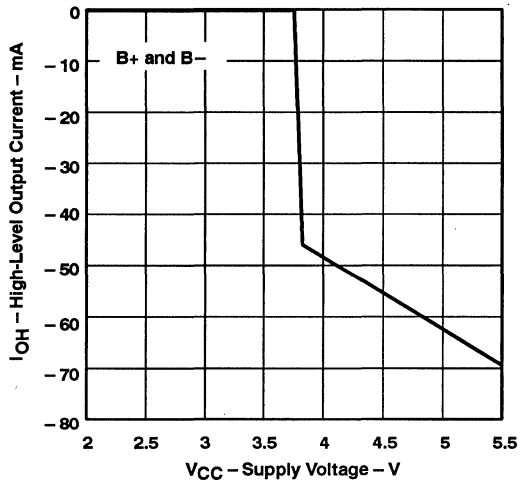


Figure 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

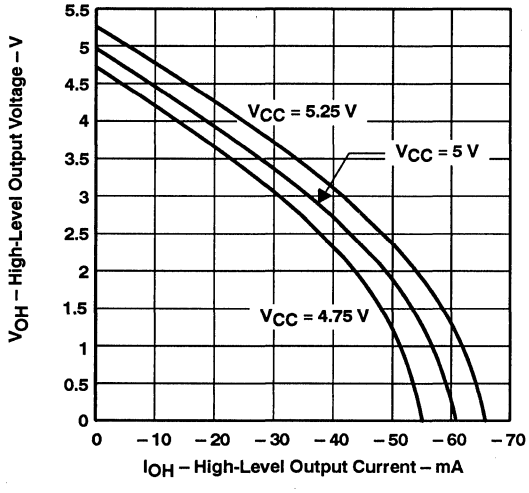


Figure 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

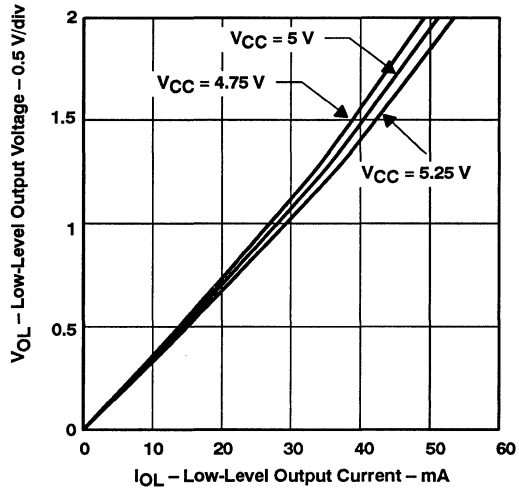


Figure 16

TYPICAL CHARACTERISTICS

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

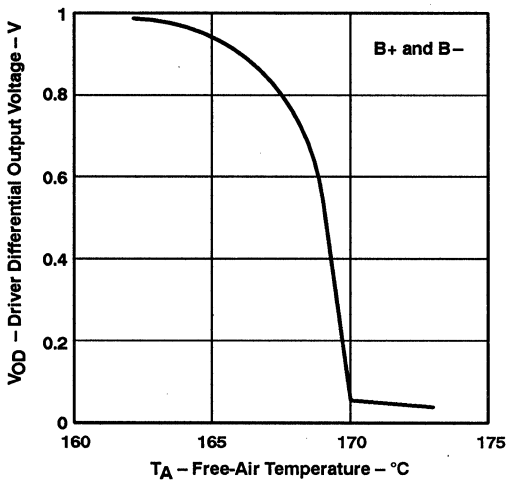


Figure 17

RECEIVER PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

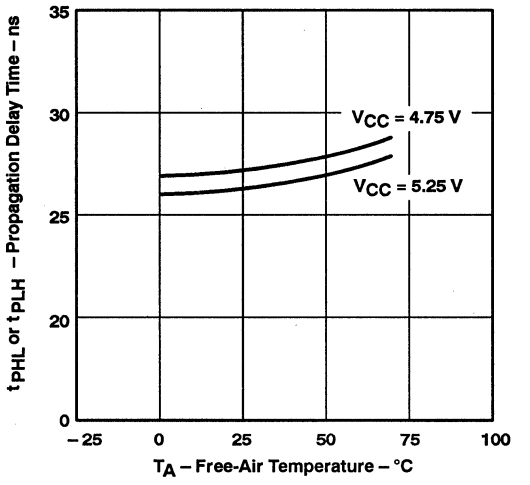


Figure 18

DRIVER PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

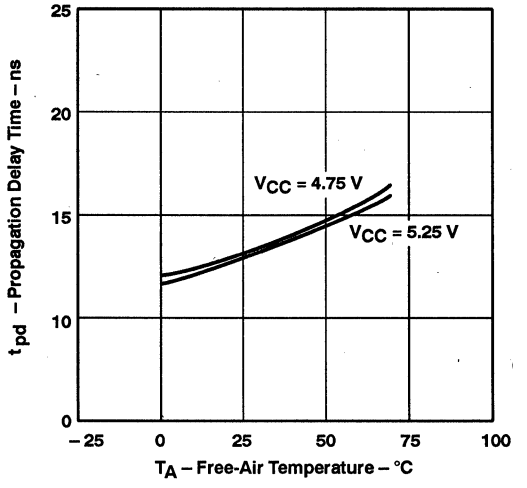


Figure 19

APPLICATION INFORMATION

Table 1. Typical Signal and Pin Assignments

SIGNAL	PIN	SCSI DATA	SCSI CONTROL	IPI DATA	IPI CONTROL
CDE0	54	DIFFSENSE	DIFFSENSE	V_{CC}	V_{CC}
CDE1	55	GND	GND	XMTA, XMTB	GND
CDE2	56	GND	GND	XMTA, XMTB	SLAVE/MASTER
BSR	2	GND	GND	GND, BSR	GND
$\overline{CRE}$	3	GND	GND	GND	V_{CC}
1A	4	DB0, DB8	ATN	AD7, BD7	NOT USED
1DE/$\overline{RE}$	5	DBE0, DBE8	INIT EN	GND	GND
2A	6	DB1, DB9	BSY	AD6, BD6	NOT USED
2DE/$\overline{RE}$	7	DBE1, DBE9	BSY EN	GND	GND
3A	8	DB2, DB10	ACK	AD5, BD5	SYNC IN
3DE/$\overline{RE}$	9	DBE2, DBE10	INIT EN	GND	GND
4A	10	DB3, DB11	RST	AD4, BD4	SLAVE IN
4DE/$\overline{RE}$	11	DBE3, DBE11	GND	GND	GND
5A	19	DB4, DB12	MSG	AD3, BD3	NOT USED
5DE/$\overline{RE}$	20	DBE4, DBE12	TARG EN	GND	GND
6A	21	DB5, DB13	SEL	AD2, BD2	SYNC OUT
6DE/$\overline{RE}$	22	DBE5, DBE13	SEL EN	GND	GND
7A	23	DB6, DB14	C/D	AD1, BD1	MASTER OUT
7DE/$\overline{RE}$	24	DBE6, DBE14	TARG EN	GND	GND
8A	25	DB7, DB15	REQ	AD0, BD0	SELECT OUT
8DE/$\overline{RE}$	26	DBE7, DBE15	TARG EN	GND	GND
9A	27	DBP0, DBP1	I/O	AP, BP	ATTENTION IN
9DE/$\overline{RE}$	28	DBPE0, DBPE1	TARG EN	XMTA, XMTB	V_{CC}

ABBREVIATIONS:

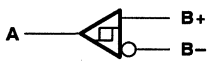
DBn, data bit n, where n = {0,1, . . . ,15}
DBEn, data bit n enable, where n = {0,1, . . . ,15}
DBP0, parity bit for data bits 0 through 7 or IPI bus A
DBPE0, parity bit enable for P0
P1, parity bit for data bits 8 through 15 or IPI bus B
PE1, parity bit enable for P1
ADn or BDn, IPI Bus A – Bit n (ADn) or Bus B – Bit n (BDn), where n = {0,1, . . . ,7}
AP or BP, IPI parity bit for bus A or bus B
XMTA or XMTB, transmit enable for IPI bus A or B
BSR, bit significant response
INIT EN, common enable for SCSI initiator mode
TARG EN, common enable for SCSI target mode

NOTE: Signal inputs are shown as active high. If only active-low inputs are available, logic inversion is accomplished by reversing the B+ and B– connecter pin assignments.

APPLICATION INFORMATION

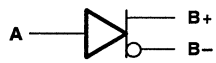
Function Tables

RECEIVER



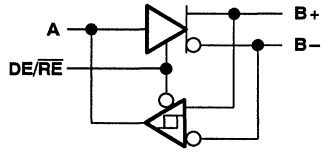
INPUTS		OUTPUT
B+†	B–†	A
L	H	L
H	L	H

DRIVER



INPUT	OUTPUTS	
A	B+	B–
L	L	H
H	H	L

TRANSCEIVER

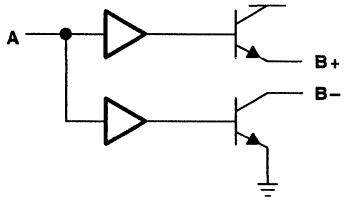


INPUTS				OUTPUTS		
DE/RE	A	B+†	B–†	A	B+	B–
L	–	L	H	L	–	–
L	–	H	L	H	–	–
H	L	–	–	–	L	H
H	H	–	–	–	H	L

DRIVER WITH ENABLE

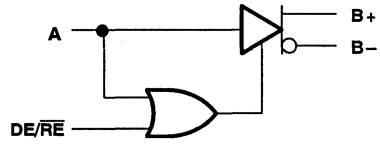
INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

WIRED-OR DRIVER



INPUT	OUTPUTS	
A	B+	B–
L	Z	Z
H	H	L

TWO-ENABLE INPUT DRIVER

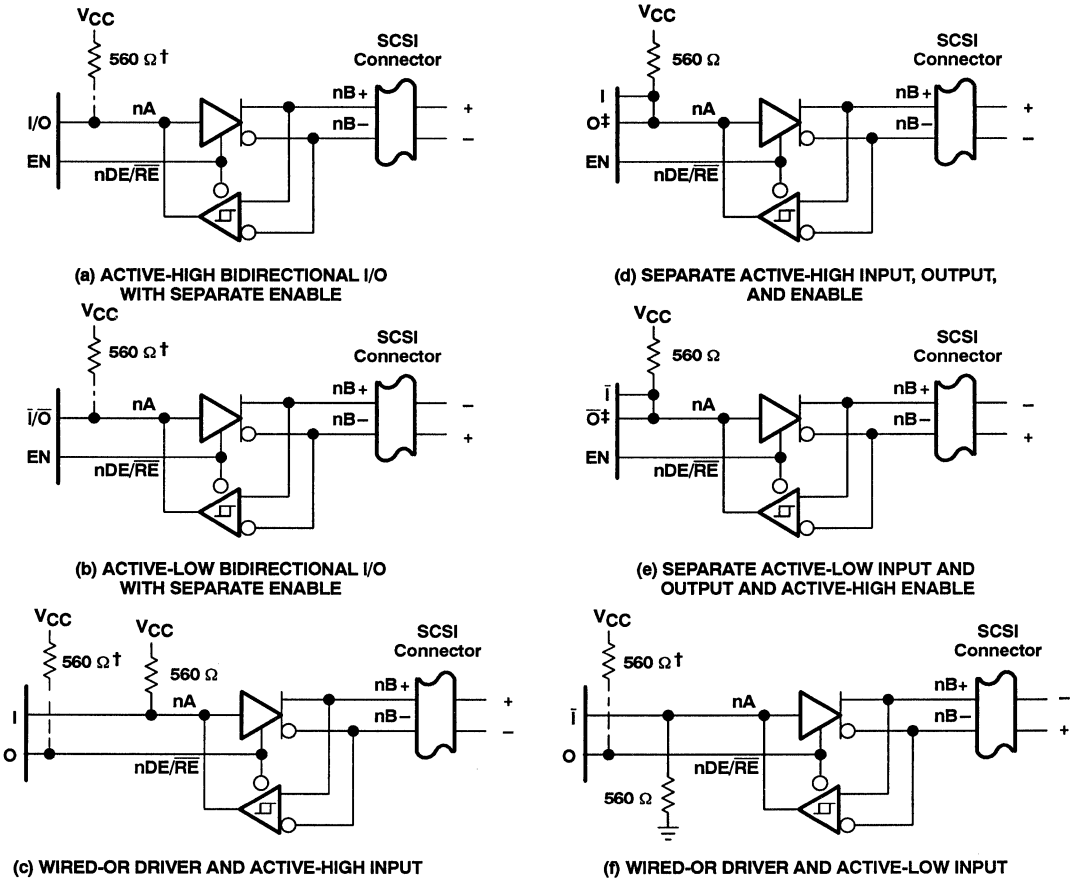


INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

APPLICATION INFORMATION



† If 0 is open drain
‡ Must be open-drain or 3-state output
NOTE: The BSR, $\overline{CRE}$, A, and DE/$\overline{RE}$ inputs have internal pullups. CDE0, CDE1, and CDE2 have internal pulldowns.

Figure 20. Typical SCSI Transceiver Connections

APPLICATION INFORMATION

channel logic configurations with control input logic

The following logic diagrams show the positive logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; BSR, CDE0, CDE1, CDE2, and $\overline{\text{CRE}}$, and are shown below the diagrams. Channel 1 is at the top and channel 9 at the bottom of the logic diagrams.

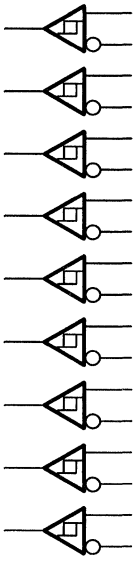


Figure 21. 00000

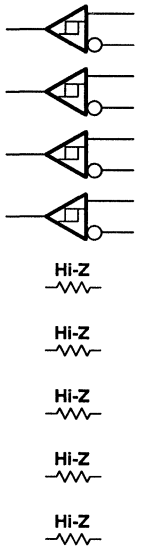


Figure 22. 00001

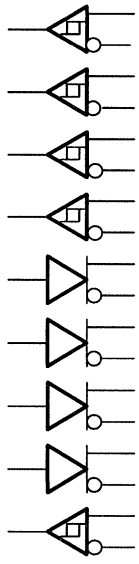


Figure 23. 00010

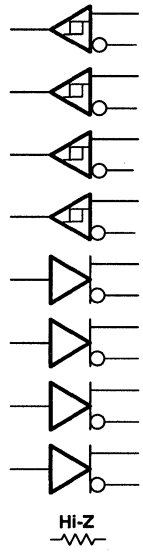


Figure 24. 00011

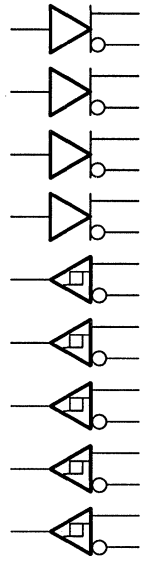


Figure 25. 00100

APPLICATION INFORMATION

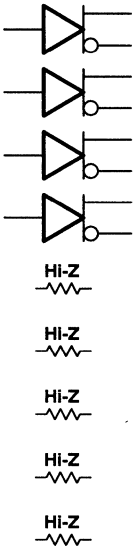


Figure 26. 00101

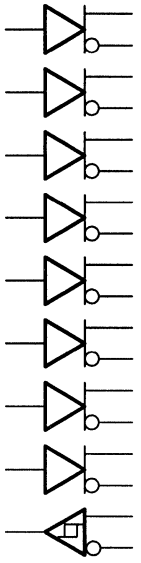


Figure 27. 00110

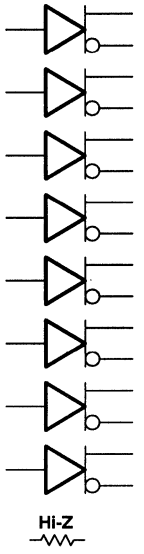


Figure 28. 00111

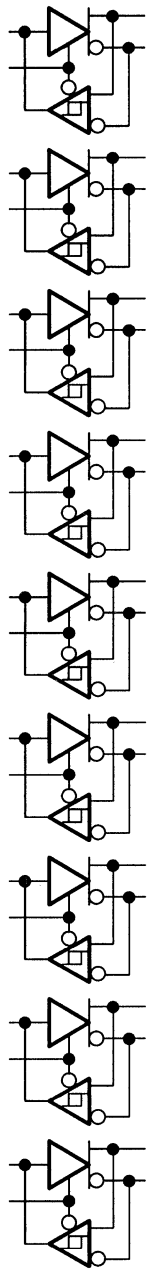


Figure 29. 01000

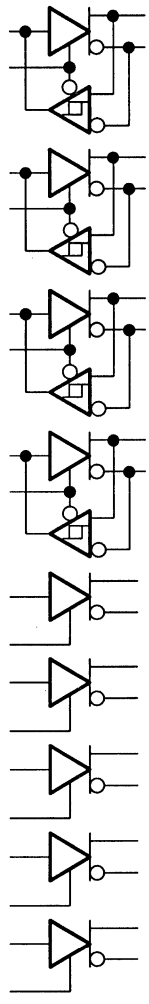


Figure 30. 01001

APPLICATION INFORMATION

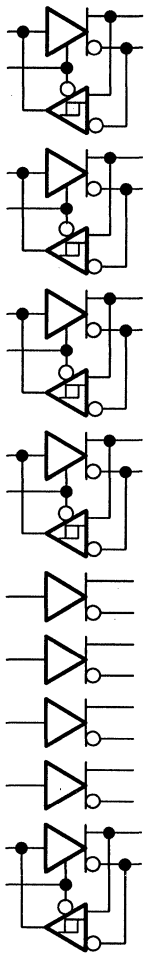


Figure 31. 01010

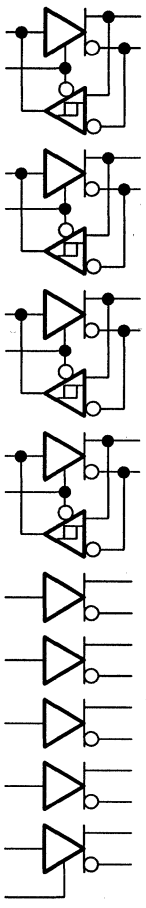


Figure 32. 01011

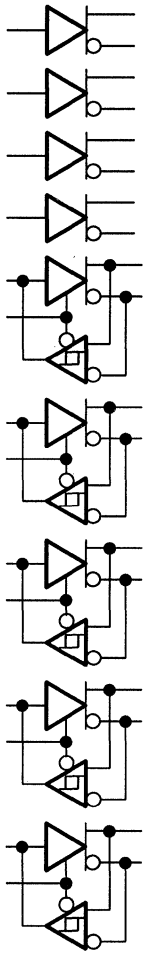


Figure 33. 01100

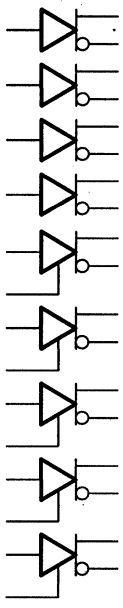


Figure 34. 01101

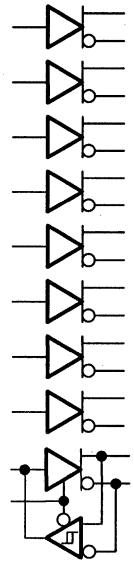


Figure 35. 01110

APPLICATION INFORMATION

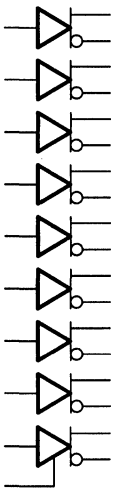


Figure 36. 01111

Figure 37. 10000 and 10001

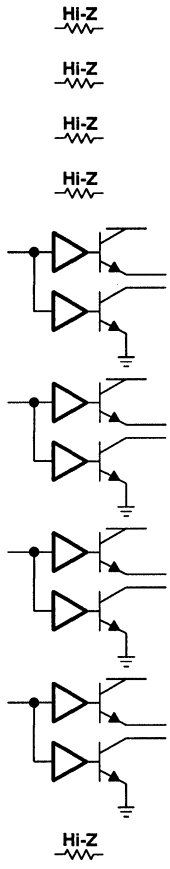


Figure 38. 10010 and 10011

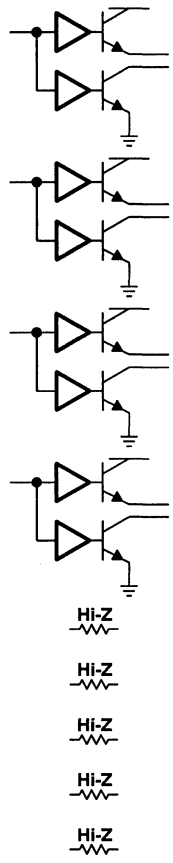


Figure 39. 10100 and 10101

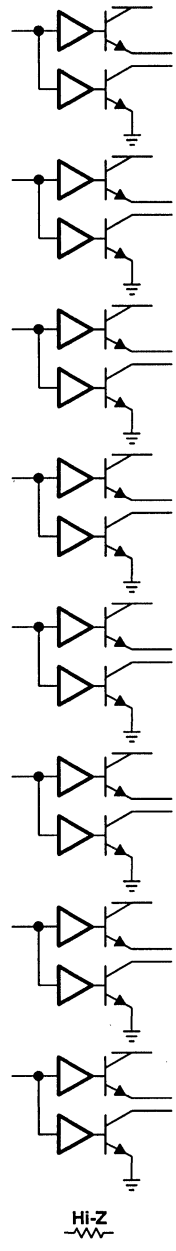


Figure 40. 10110 and 10111

APPLICATION INFORMATION

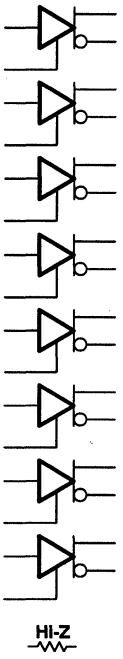


Figure 41. 11000 and 11001

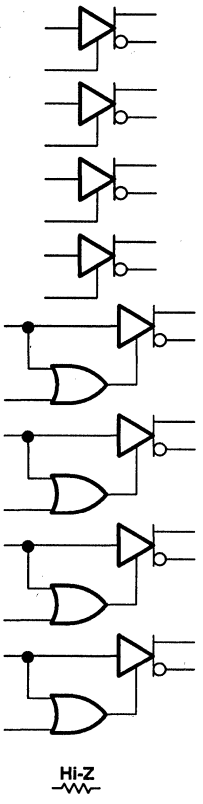


Figure 42. 11010 and 11011

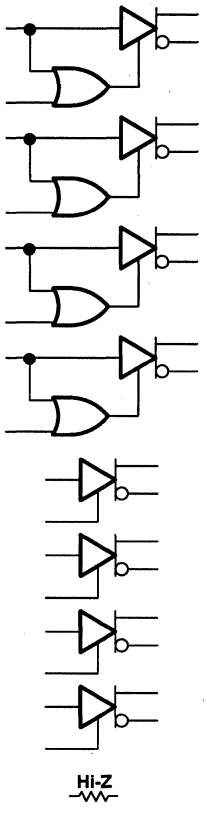


Figure 43. 11100 and 11101

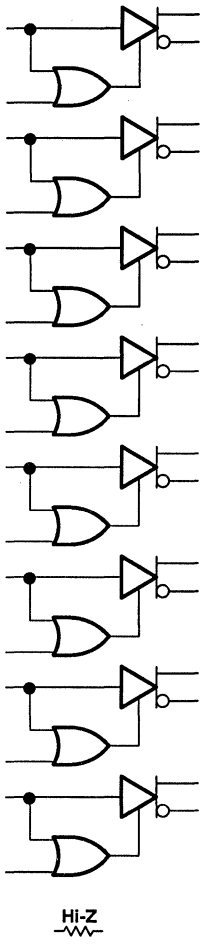
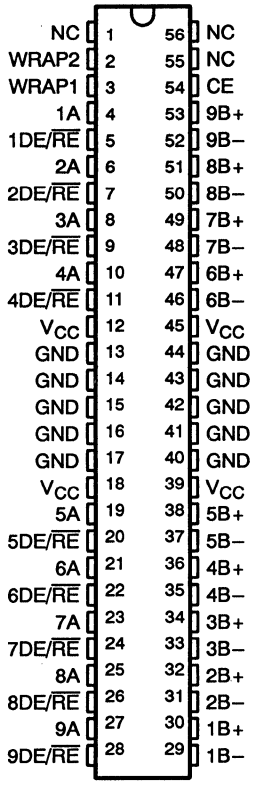


Figure 44. 11110 and 11111

SLLS134B – D4088, APRIL 1992 – REVISED FEBRUARY 1993

- **9 Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI)**
- **Each Transceiver Meets EIA-RS-485 and ISO 8482:1987(E) Standards**
- **Packaged In Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typ**
- **Thermal Shutdown Protection**
- **Power Up/Down Glitch Protection**
- **Positive and Negative Output Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

DL PACKAGE
(TOP VIEW)



Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC978 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of the Texas Instruments LinBiCMOS™ process technology allows the power reduction necessary to integrate nine differential balanced transceivers†. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for the Small Computer Systems Interface (SCSI) standard. The WRAP function allows in-circuit testing and wired-OR channels for the BSY, RST, and SEL signals of the SCSI bus.

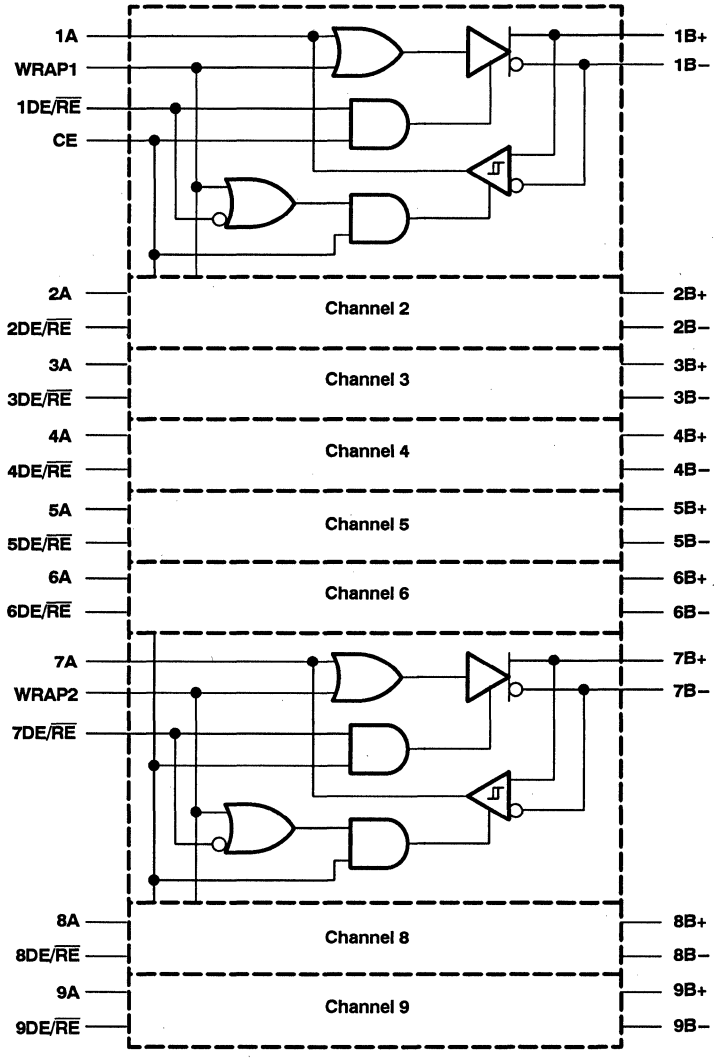
The SN75LBC978 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat sink pins. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed of the SN75LBC978 is sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine identical channels conforms to the requirements of the EIA-RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.131-1986 (SCSI-1) and the proposed SCSI-2 standards. This device conforms to ESD Class 1 (A) and Class 2 (B) per MIL-STD-883, Method 3015.

The SN75LBC978 is characterized for operation from 0°C to 70°C.

† Patent Pending
LinASIC and LinBiCMOS are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



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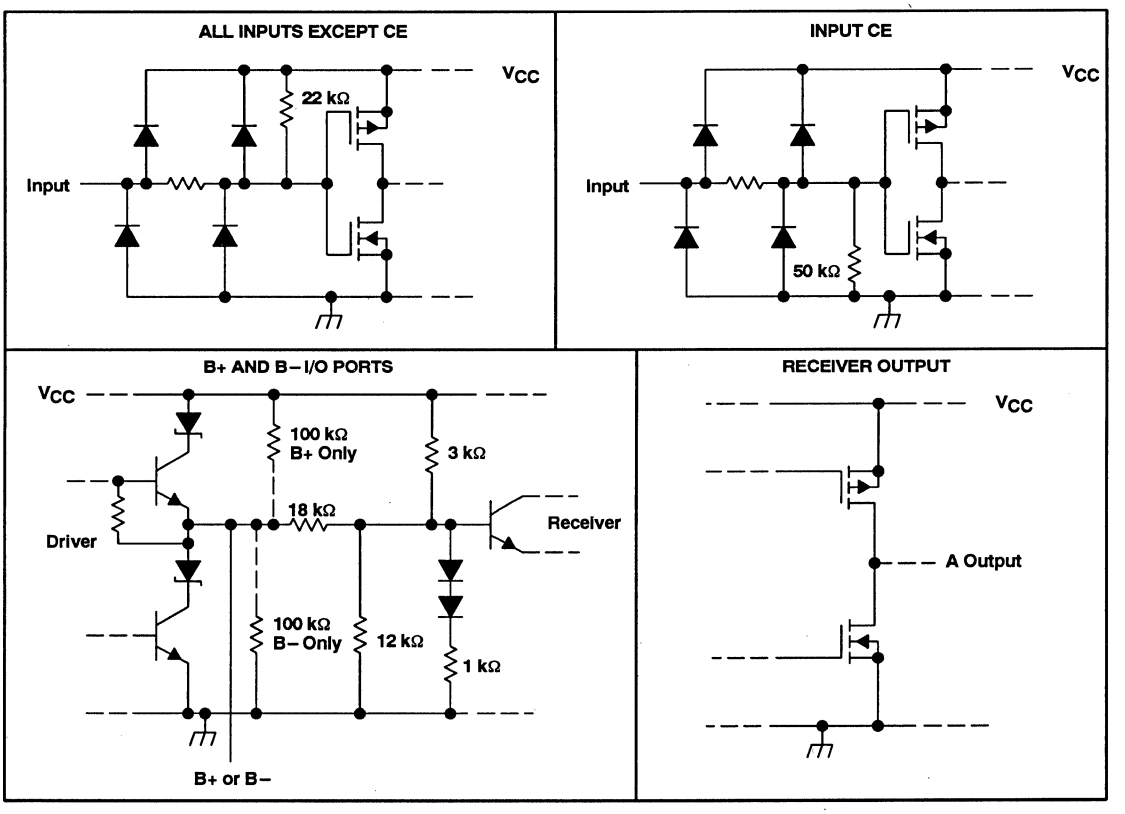
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Bus voltage range	−10 V to 15 V
Data I/O and control (A-side) voltage range	−0.3 V to 7 V
Continuous power dissipation	internally limited
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are dc and with respect to the GND terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	B+ or B–			12	V
				–7	
High-level input voltage, V_{IH}	All except B+ and B–	2			V
Low-level input voltage, V_{IL}	All except B+ and B–			0.8	V
High-level output current, I_{OH}	B+ or B–			–60	mA
	A			–8	mA
Low-level output current, I_{OL}	B+ or B–			60	mA
	A			8	mA
Operating free-air temperature, T_A		0		70	°C

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	V_{test} = –7 V to 12 V, See Figure 2	1	2		V
I_{OS}	Output short-circuit current	See Figure 1			±250	mA
I_{OZ}	High-impedance state output current	See receiver input current				

receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –8 mA	2.5			V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OL} = 8 mA			0.8	V
V_{T+}	Differential-input high-level threshold voltage		I_{OH} = –8 mA			0.2	V
V_{T-}	Differential-input low-level threshold voltage		I_{OL} = 8 mA	–0.2			V
V_{hys}	Receiver input hysteresis ($V_{T+} - V_{T-}$)				45		mV
I_I	Receiver input current	B+ and B–	V_I = 12 V, Other input at 0 V, V_{CC} = 5 V		0.7	1	mA
			V_I = 12 V, Other input at 0 V, V_{CC} = 0 V		0.8	1	mA
			V_I = –7 V, Other input at 0 V, V_{CC} = 5 V		–0.5	–0.8	mA
			V_I = –7 V, Other input at 0 V, V_{CC} = 0 V		–0.4	–0.8	mA
I_{OZ}	High-impedance state output current		V_O = GND			–100	µA
			V_O = V_{CC}			50	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

device electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	A, WRAP, DE/$\overline{RE}$	See Figure 3	V_{IH} = 5 V			−100	μA
		CE					50	μA
I_{IL}	Low-level input current	A, WRAP, DE/$\overline{RE}$		V_{IL} = 0 V			−200	μA
		CE			−50		50	μA
I_{CC}	Supply current	All drivers and receivers disabled	CE at 0 V			1.4	3	mA
		All receivers enabled	No load, CE at 5 V,	V_{ID} = 5 V, WRAP and DE/$\overline{RE}$ at 0 V		29	45	mA
		All drivers enabled	No load, WRAP at 0 V	CE and DE/$\overline{RE}$ at 5 V,		7	10	mA
C_o	Bus port capacitance		B+ or B−			19		pF
C_{pd}	Power dissipation capacitance‡		One driver			460		pF
			One receiver			40		pF

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential delay time, high-to-low-level output (t_{dDH}) or low-to-high-level output (t_{dDL})			11.8		26.4	ns
		V_{CC} = 5 V,	T_A = 25°C	14	18	22	
		V_{CC} = 5 V,	T_A = 70°C	18	22	26	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					15	ns
		V_{CC} = 5 V,	See Note 2			8	
$t_{sk(p)}$	Pulse skew ($\lvert t_{dDL} - t_{dDH} \rvert$)				0	6	ns
t_t	Transition time (t_r or t_f)				10		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_{pd} determines the no-load dynamic current consumption, $I_S = C_{pd} V_{CC} f + I_{CC}$.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

transceiver switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{en(TL)}$	Transmit-to-receive enable time to low-level output	See Figure 6		80	ns
$t_{en(TH)}$	Transmit-to-receive enable time to high-level output			80	ns
$t_{en(RL)}$	Receive-to-transmit enable time to low-level output			150	ns
$t_{en(RH)}$	Receive-to-transmit enable time to high-level output			150	ns
t_{su}	Setup time, WRAP1 or WRAP2 before active input(s) or output(s)		150		ns

thermal characteristics

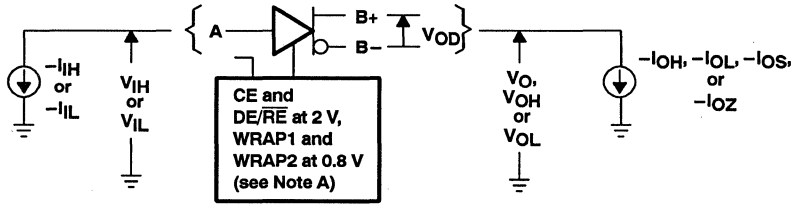
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, high-to-low-level output (t_{PHL}) or low-to-high-level output (t_{PLH})			19.5		30.7	ns
		V_{CC} = 5 V,	T_A = 25°C	20.2	24.7	29.2	
		V_{CC} = 5 V,	T_A = 70°C	21.1	25.6	30.1	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		V_{CC} = 5 V,	See Note 2			9	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				2	6	ns
t_t	Transition time (t_r or t_f)				3		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

PARAMETER MEASUREMENT INFORMATION



NOTE A: For the I_{OZ} test, the CE input is at 0.8 V.

Figure 1. Driver Test and Input Conditions

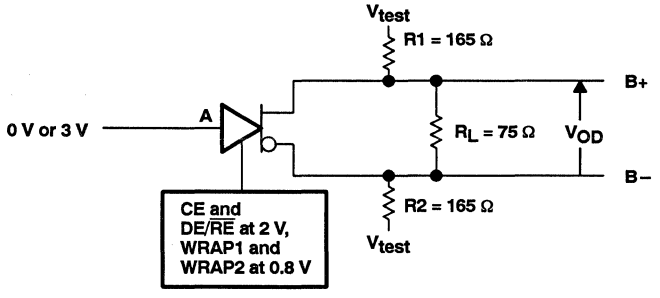
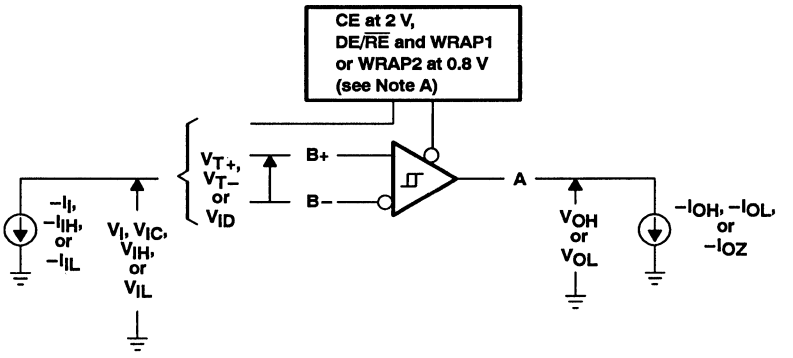


Figure 2. Driver V_{OD} Test Circuit

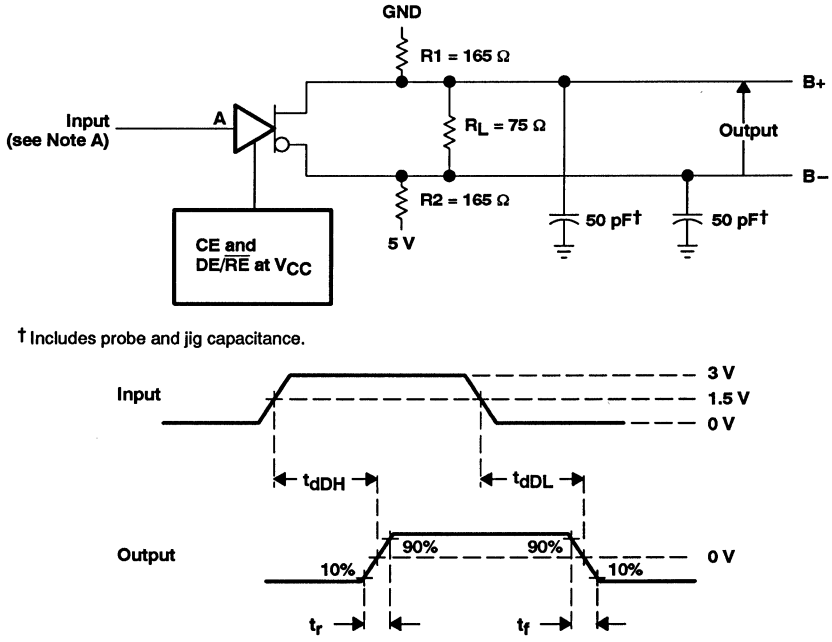
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



NOTE A: For the I_{OZ} measurement, CE is at 0.8 V.

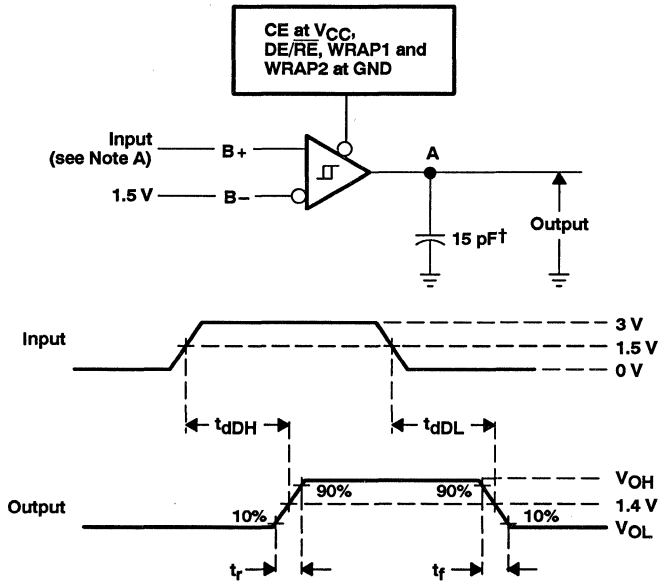
Figure 3. Receiver Test and Input Conditions



NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 4. Driver Propagation Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

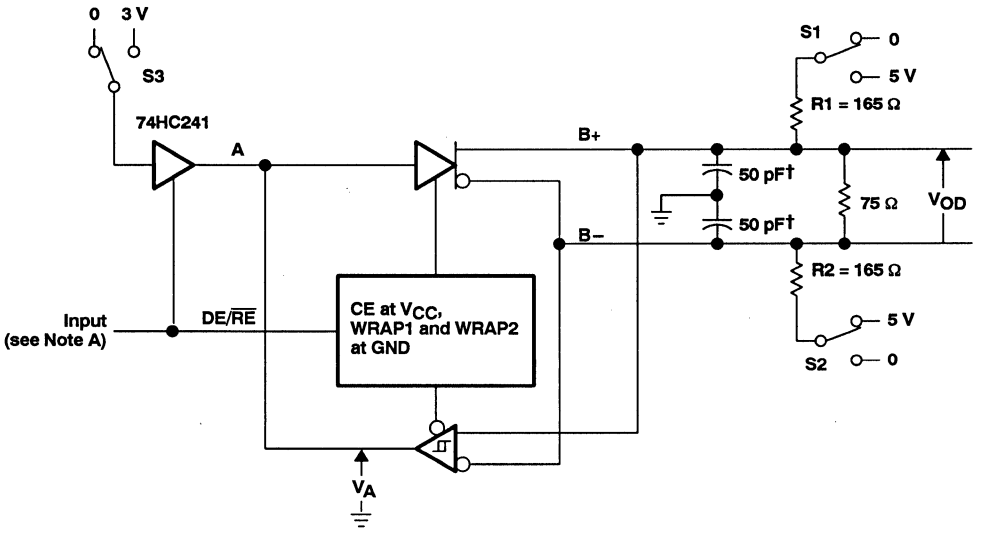


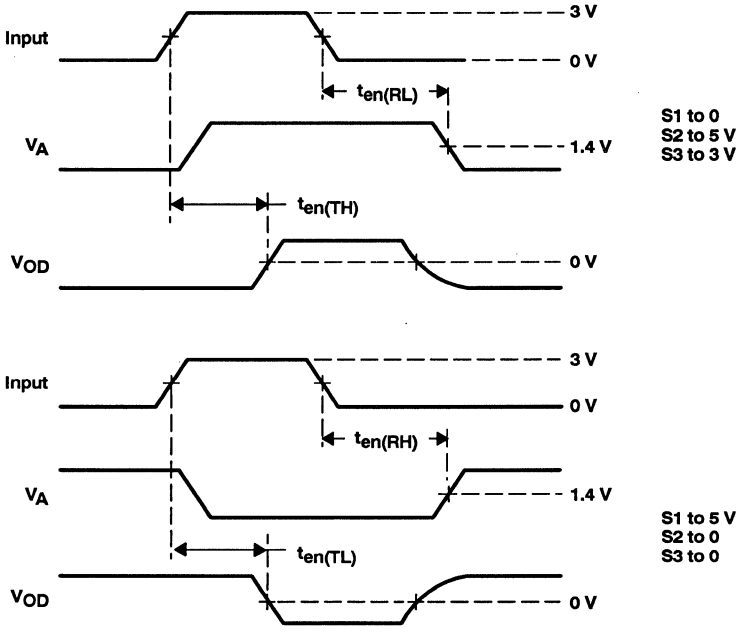
† Includes probe and jig capacitance.
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 5. Receiver Propagation Delay Time Test Circuit and Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION





† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

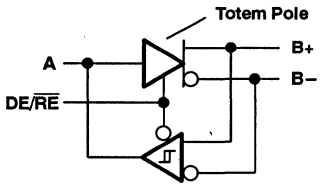
Figure 6. Enable and Disable Time Measurements

APPLICATION INFORMATION

Truth Tables for Possible Channel Functions

Table 1

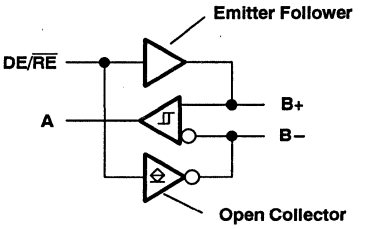
CE is high
WRAP1 or WRAP2 is low



INPUTS				OUTPUTS		
DE/$\overline{RE}$	A	B+†	B–†	A	B+	B–
L	X	L	H	L	Z	Z
L	X	H	L	H	Z	Z
H	L	X	X	Z	L	H
H	H	X	X	Z	H	L

Table 2

CE is high
WRAP1 or WRAP2 is high



INPUTS			OUTPUTS		
DE/$\overline{RE}$	B+	B–	A	B+	B–
L	L	H	L	Z	Z
L	H	L	H	Z	Z
H	X	X	H	H	L
H	X	X	H	H	L

H = high level, L = low level, X = irrelevant Z = high impedance

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

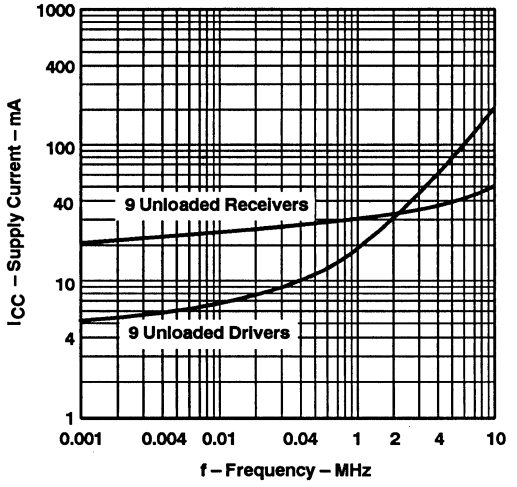


Figure 7

INPUT CURRENT
vs
INPUT VOLTAGE

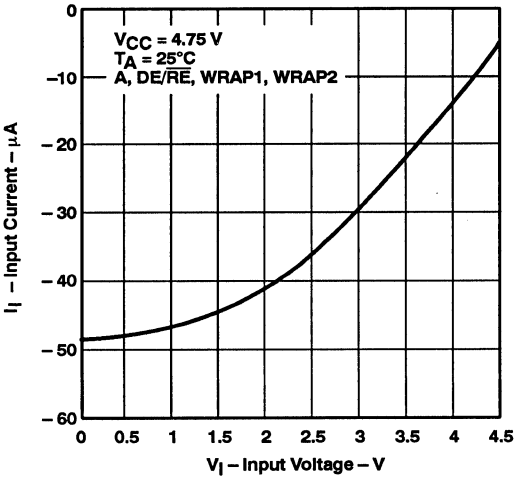


Figure 8

INPUT CURRENT
vs
INPUT VOLTAGE

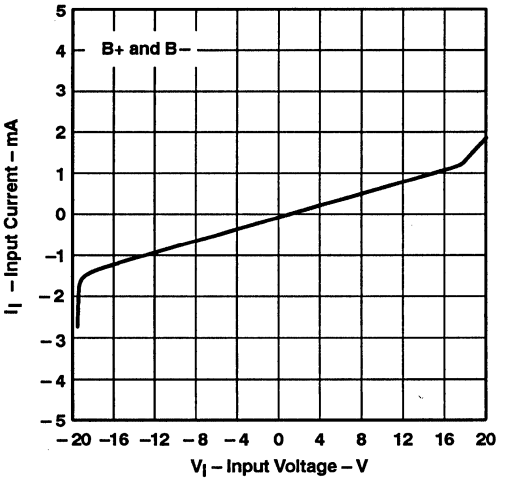


Figure 9

TYPICAL CHARACTERISTICS

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

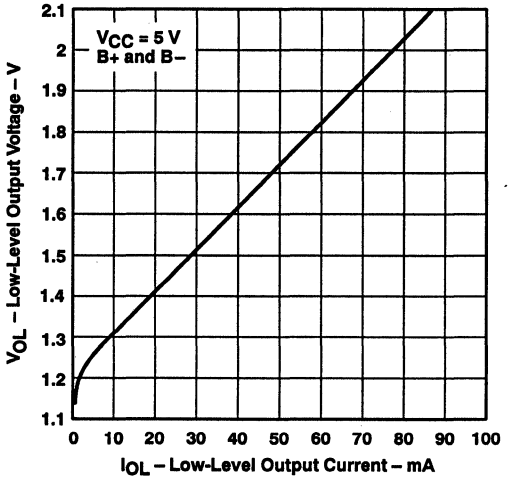


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

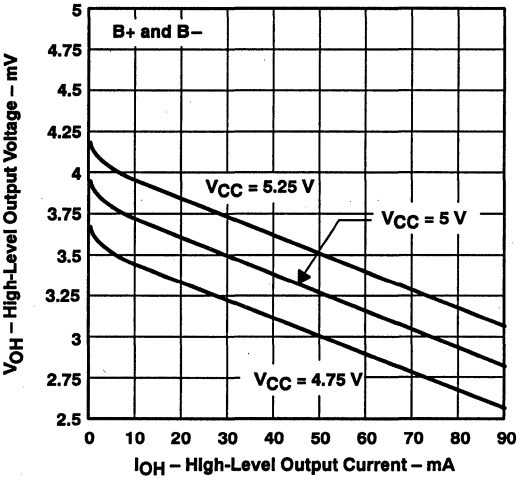


Figure 11

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

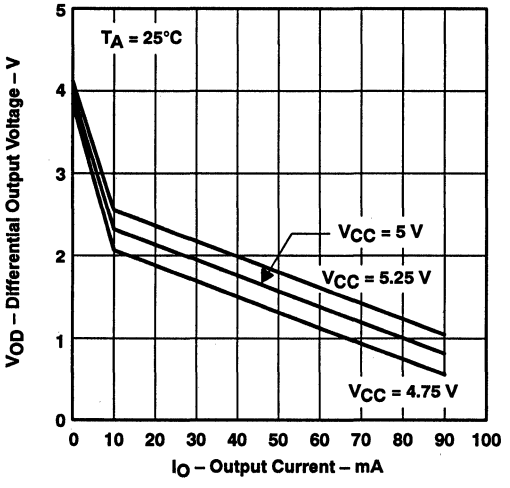


Figure 12

TYPICAL CHARACTERISTICS

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

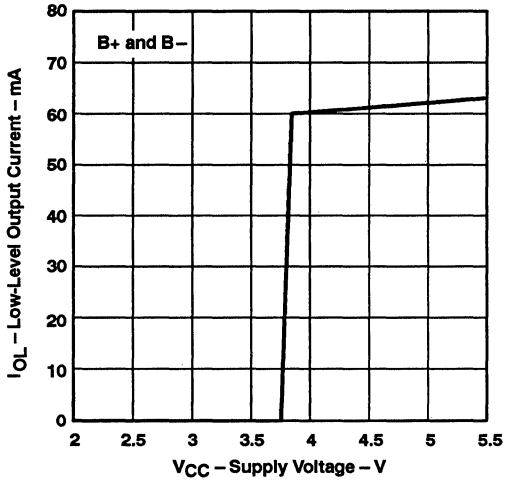


Figure 13

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

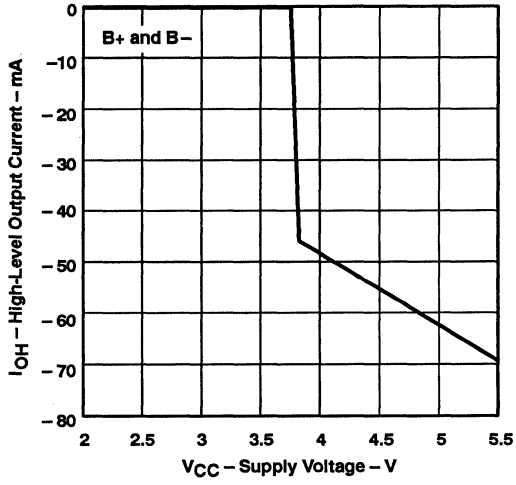


Figure 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

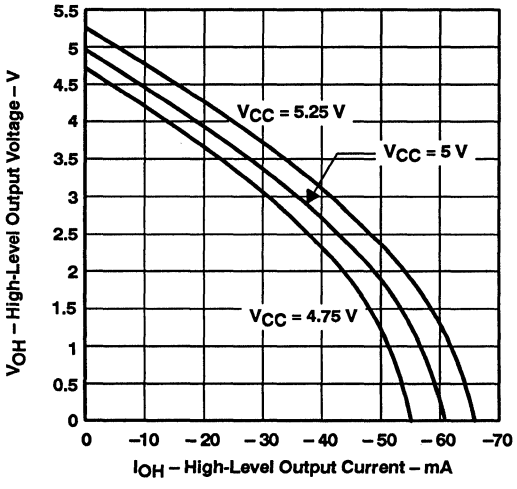


Figure 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

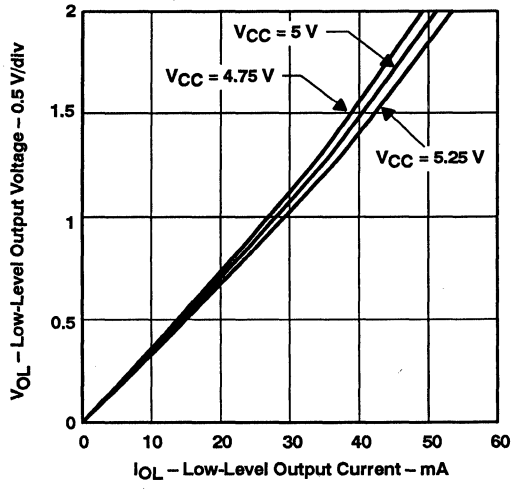


Figure 16

TYPICAL CHARACTERISTICS

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

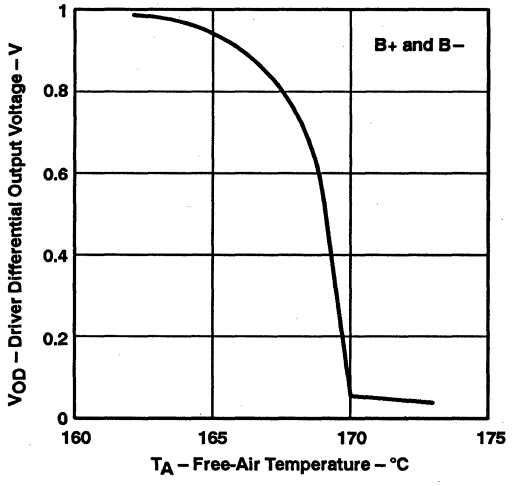


Figure 17

RECEIVER PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

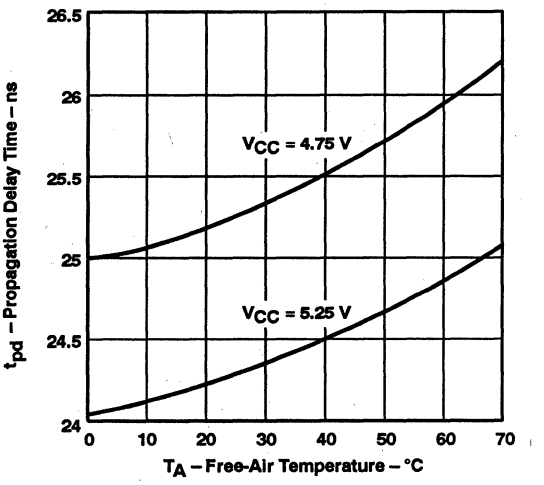


Figure 18

DRIVER PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

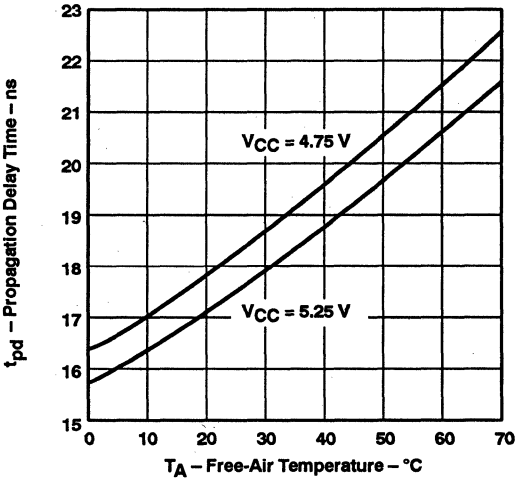
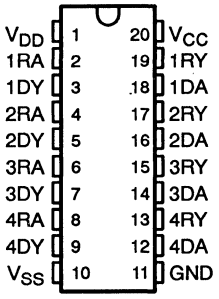


Figure 19

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Very Low Power Consumption 5 mW Typ**
- **Wide Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**

DW OR N PACKAGE
(TOP VIEW)



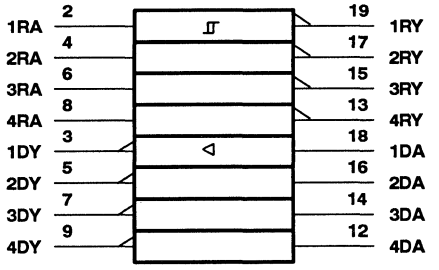
description

The SN65C1154 and SN75C1154 are low-power BI-MOS devices containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device has been designed to conform to Standards ANSI/EIA-232-D-1986 (which supersedes RS-232-C). The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses of shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

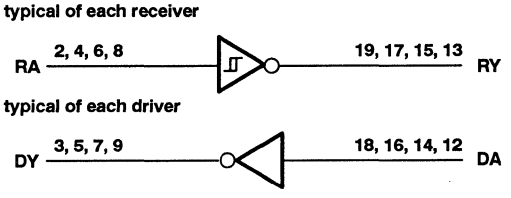
The SN65C1154 is characterized for operation from −40°C to 85°C. The SN75C1154 is characterized for operation from 0°C to 70°C.

logic symbol†

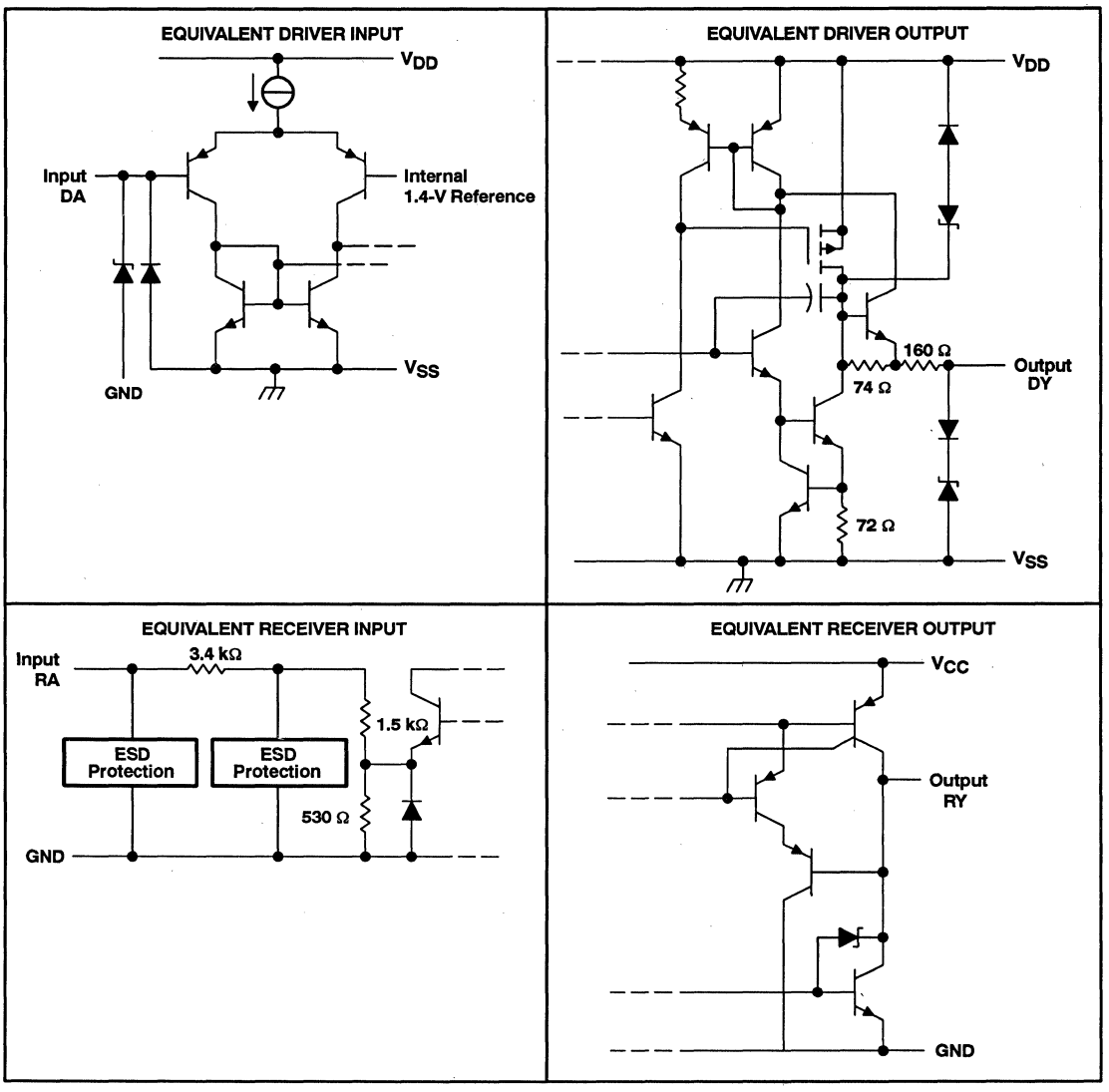


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} ..... −15 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range: Driver ..... V_{SS} to V_{DD}
Receiver ..... −30 V to 30 V
Output voltage range: Driver ..... (V_{SS} −6 V) to (V_{DD} + 6 V)
Receiver ..... −0.3 V to (V_{CC} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65C1154 ..... −40°C to 85°C
SN75C1154 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	920 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	15	V
Supply voltage, V_{SS}		−4.5	−12	−15	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I	Driver	V_{SS}+2		V_{DD}	V
	Receiver			±25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
High-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C1154	−40		85	°C
	SN75C1154	0		70	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
				V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
				V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				1	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1	μA
$I_{OS(H)}$	High-level short circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{SS},	See Figure 1	−7.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short circuit output current‡	V_I = 2 V,	V_O = 0 or V_{DD},	See Figure 1	7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = −5 V		115	250	μA
				V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	μA
				V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0,	V_O = −2 V to 2 V,	See Note 3	300	400		Ω

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at one time.
NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Test conditions are those specified by EIA-232-D.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output§	R_L = 3 to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	μs
t_{PHL}	Propagation delay time, high-to-low-level output§			2.5	3.5	μs
t_{TLH}	Transition time, low-to-high-level output¶		0.53	2	3.2	μs
t_{THL}	Transition time, high-to-low-level output¶		0.53	2	3.2	μs
t_{TLH}	Transition time, low-to-high-level output#	R_L = 3 to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	μs
t_{THL}	Transition time, high-to-low level output#			1	2	μs
SR	Output slew rate	R_L = 3 to 7 kΩ, C_L = 150 pF, See Figure 3	4	10	30	V/μs

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform.
# Measured between 3 V and −3 V points of output waveform (EIA-232-D conditions) with all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5			1.7	2.1	2.55	V
V_{T-}	Negative-going threshold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V,	I_{OH} = −20 μA,	See Figure 5 and Note 4	3.5			V
		V_I = 0.75 V, See Figure 5	I_{OH} = −1 mA,	V_{CC} = 4.5 V	2.8	4.4		
				V_{CC} = 5 V	3.8	4.9		
				V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V,	I_{OL} = 3.2 mA,	See Figure 5		0.17	0.4	V
I_{IH}	High-level input current	V_I = 25 V			3.6	4.6	8.3	mA
		V_I = 3 V			0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −25 V			−3.6	−5	−8.3	
		V_I = −3 V			−0.43	−0.55	−1	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V,	V_O = 0,	See Figure 4		−8	−15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC},	V_O = V_{CC},	See Figure 4		13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V		V_{DD} = 5 V, V_{SS} = −5 V		400	600	μA
				V_{DD} = 12 V, V_{SS} = −12 V		400	600	

† All typical values are at T_A = 25°C.

NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10%, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high-to-low-level output					3	4	μs
t_{TLH}	Transition time, low-to-high-level output					300	450	ns
t_{THL}	Transition time, high-to-low-level output					100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise‡	C_L = 50 pF,	R_L = 5 kΩ		1		4	μs

‡ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

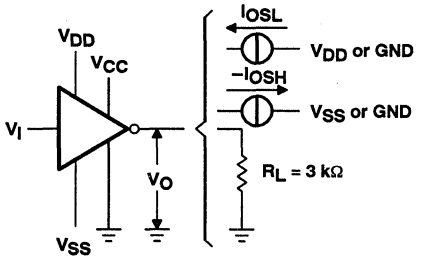


Figure 1. Driver Test Circuit V_{OH}, V_{OL}, I_{OSL}, I_{OSH}

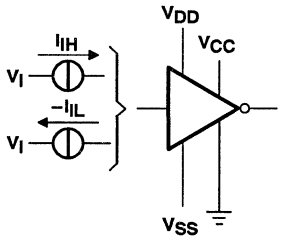
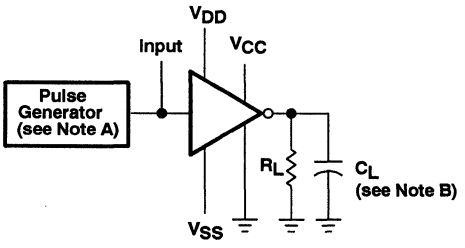
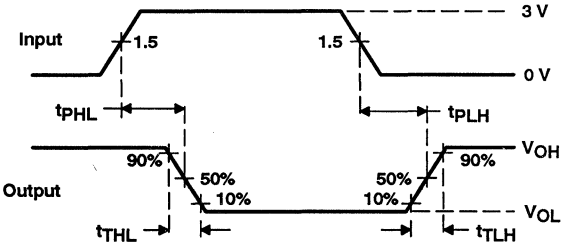


Figure 2. Driver Test Circuit, I_{IL}, I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

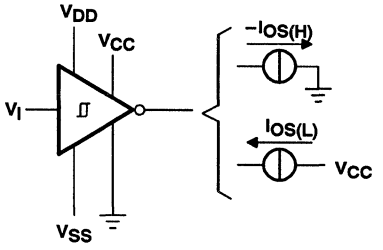


Figure 4. Receiver Test Circuit, I_{OSH}, I_{OSL}

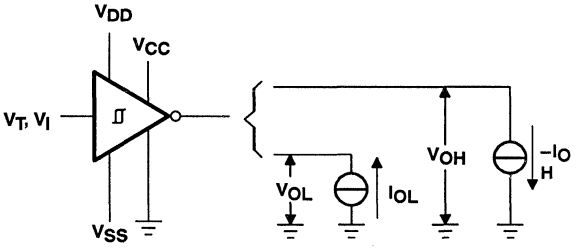


Figure 5. Receiver Test Circuit, V_T, V_{OL}, V_{OH}

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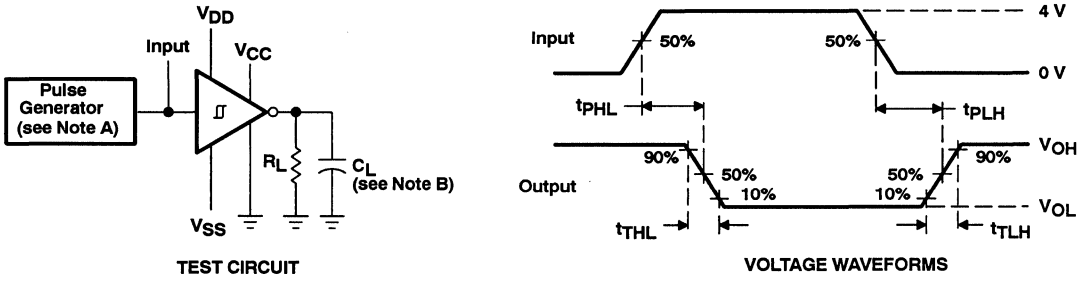
PARAMETER MEASUREMENT INFORMATION



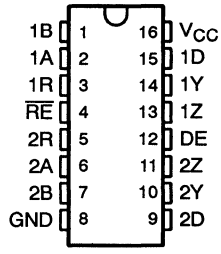
NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

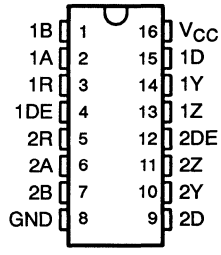
SLLS159 – D4062, MARCH 1993

- **Meets EIA Standards RS-422-A and CCITT Recommendation V.11**
- **BiCMOS Process Technology**
- **Low Supply Current Requirements 9 mA Max**
- **Low Pulse Skew**
- **Receiver Input Impedance . . . 17 kΩ Typ**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Common-Mode Input Voltage Range of −7 V to 7 V**
- **Operates From Single 5-V Supply**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Receiver 3-State Outputs Active-Low Enable for SN751167 Only**
- **Improved Replacement for the MC34050 and MC34051**

SN65C1167 . . . DB†, N, OR NS† PACKAGE
(TOP VIEW)



SN75C1177 . . . DB†, N, OR NS† PACKAGE
(TOP VIEW)



† The DB and NS packages are only available left-ended taped and reeled (order device SN_5C116_DBLE or SN_5C116_NSLE).

description

The SN75C1167 and SN75C1168 dual drivers and receivers are monolithic integrated circuits designed for balanced transmission lines and meets EIA Standards RS-422-A, CCITT recommendations V.10, V.11, X.26, and X.27.

The SN75C1167 combines dual 3-state differential line driver and 3-state differential line receivers both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN75C1168 drivers each have individual active-high enable.

The SN65C1167 and SN65C1168 are characterized from −40°C to 85°C. The SN75C1167 and SN75C1168 are characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

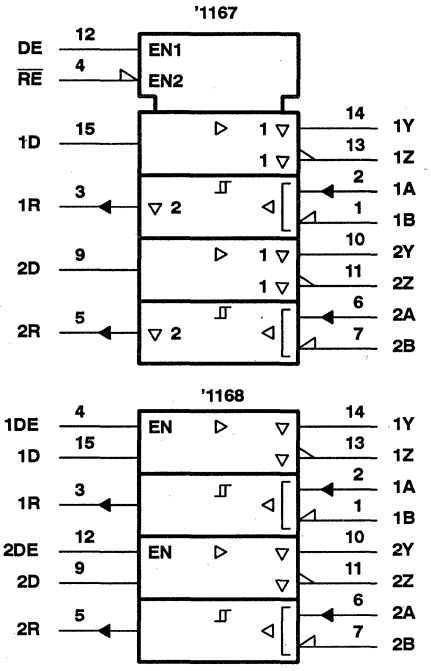
INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

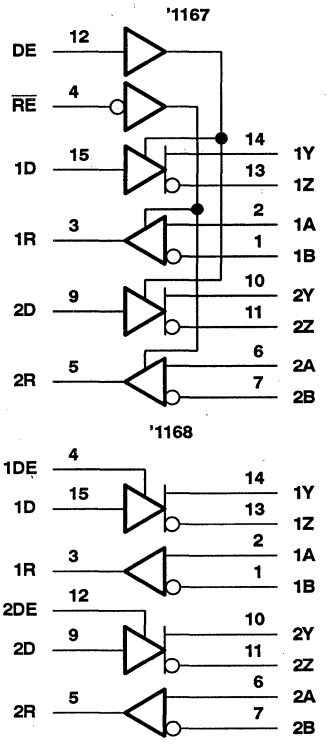
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbols†

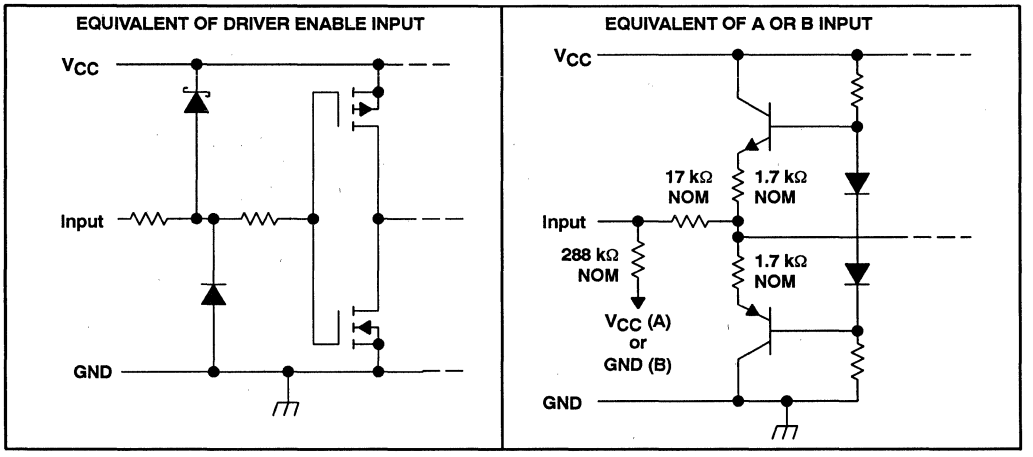


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

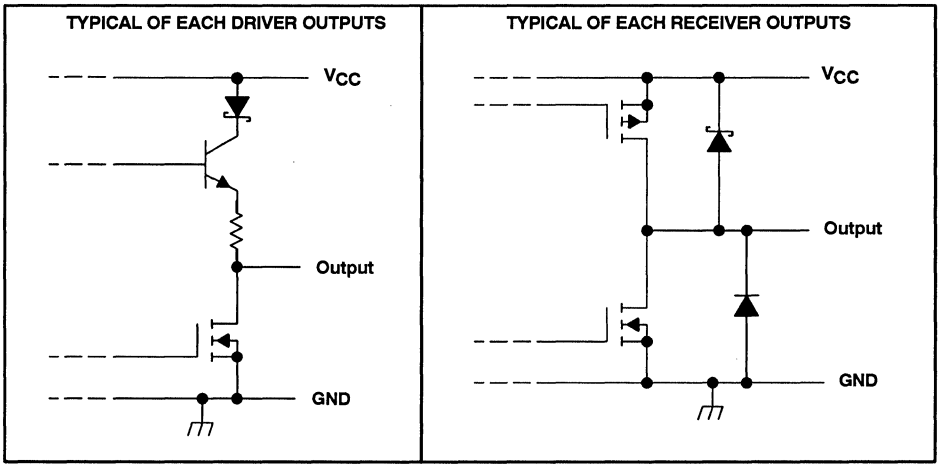
logic diagrams (positive logic)



schematics of inputs



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, A or B, Receiver ..... −11 V to 14 V
Differential input voltage range, V_{ID}, Receiver (see Note 2) ..... −14 V to 14 V
Output voltage range, V_O, Driver ..... −5 V to 7 V
Clamp current range, I_{IK} or I_{OK}, Driver ..... ±20 mA
Output current range, I_O, Driver ..... ±150 mA
Supply current, I_{CC} ..... 200 mA
GND current ..... −200 mA
Output current range, I_O, Receiver ..... ±25 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN75C1167, SN75C1168 ..... 0°C to 70°C
SN65C1167, SN65C1168 ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	781 mW	6.2 mW/°C	502 mW	409 mW
N	1250 mW	10 mW/°C	736 mW	650 mW
NS	625 mW	5 mW/°C	445 mW	325 mW

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Common-mode input voltage, V_{IC} (see Note 3)	Receiver			±7	V
Differential input voltage, V_{ID}	Receiver			±7	V
High-level input voltage, V_{IH}	Except A, B	2			V
Low-level input voltage, V_{IL}	Except A, B			0.8	V
High-level output current, I_{OH}	Receiver			−6	mA
	Driver			−20	
Low-level output current, I_{OL}	Receiver			6	mA
	Driver			20	
Operating free-air temperature, T_A	SN65C1167 and SN65C1168	−40		85	°C
	SN75C1167 and SN75C1168	0		70	

NOTE 3: Refer to EIA standards RS-422-A for exact conditions.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −20 mA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0 mA		2		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1 and Note 3		2	3.1		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage					±0.4	V
$I_{O(OFF)}$	Output current with power off (see Note 3)	V_{CC} = 0 V	V_O = 6 V			100	µA
			V_O = −0.25 V			−100	µA
I_{OZ}	High-impedance-state output current	V_O = 2.5 V				20	µA
		V_O = 5 V				−20	
I_{IH}	High-level input current	$V_I = V_{CC}$ or V_{IH}				1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}				−1	µA
I_{OS}	Short-circuit output current	$V_O = V_{CC}$ or GND, See Note 4		−30		−150	mA
I_{CC}	Supply current (total package)	No load, Enabled	$V_I = V_{CC}$ or GND		4	6	mA
			V_I = 2.4 or 0.5 V, See Note 5		5	9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	$R_1 = R_2$ = 50 Ω, R_3 = 500 Ω, $C_1 = C_2$ = C3 = 40 pF, S1 is open, See Figure 2		7	12	ns
t_{PLH}	Propagation delay time, low-to-high-level output			7	12	ns
$t_{sk(p)}$	Pulse skew			0.5	4	ns
t_r	Rise time	$R_1 = R_2$ = 50 Ω, R_3 = 500 Ω, $C_1 = C_2$ = C3 = 40 pF, S1 is open, See Figure 3		5	10	ns
t_f	Fall time			5	10	ns
t_{PZH}	Output enable time to high level	$R_1 = R_2$ = 50 Ω, R_3 = 500 Ω, $C_1 = C_2$ = C3 = 40 pF, S1 is closed, See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level			10	19	ns
t_{PHZ}	Output disable time from low level	$R_1 = R_2$ = 50 Ω, R_3 = 500 Ω, $C_1 = C_2$ = C3 = 40 pF, S1 is closed, See Figure 4		7	16	ns
t_{PLZ}	Output disable time from high level			7	16	ns
C_i	Input capacitance			6		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 3. Refer to EIA standards RS-422-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
5. Measured per input while the other inputs are at V_{CC} or GND.

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage, differential input						0.2	V
V_{T-}	Negative-going threshold voltage, differential input				−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	'1167	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −6 mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 6 mA		0.1	0.3	V
I_{OZ}	High-impedance-state output current	'1167	V_O = V_{CC} or GND			±0.5	±5	μA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = −10 V			−2.5	
I_I	Enable input current, $\overline{RE}$	'1167	V_I = V_{CC} or GND				±1	μA
r_i	Input resistance		V_{IC} = −7 V to 7 V,	Other input at 0 V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4 V or 0.5 V, See Note 5		5	9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		See Figure 5	9	17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	17	27	ns
t_{TLH}	Transition time, low-to-high-level output		V_{IC} = 0 V, See Figure 5		4	9	ns
t_{THL}	Transition time, high-to-low-level output				4	9	ns
t_{PZH}	Output enable time to high level	'1167	R_L = 1 kΩ, See Figure 6		13	22	ns
t_{PZL}	Output enable time to low level	'1167			13	22	ns
t_{PHZ}	Output disable time from high level	'1167	R_L = 1 kΩ, See Figure 6		13	22	ns
t_{PLZ}	Output disable time from low level	'1167			13	22	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: Measured per input while the other inputs are at V_{CC} or GND.

PARAMETER MEASUREMENT INFORMATION

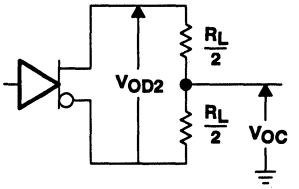


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

PARAMETER MEASUREMENT INFORMATION

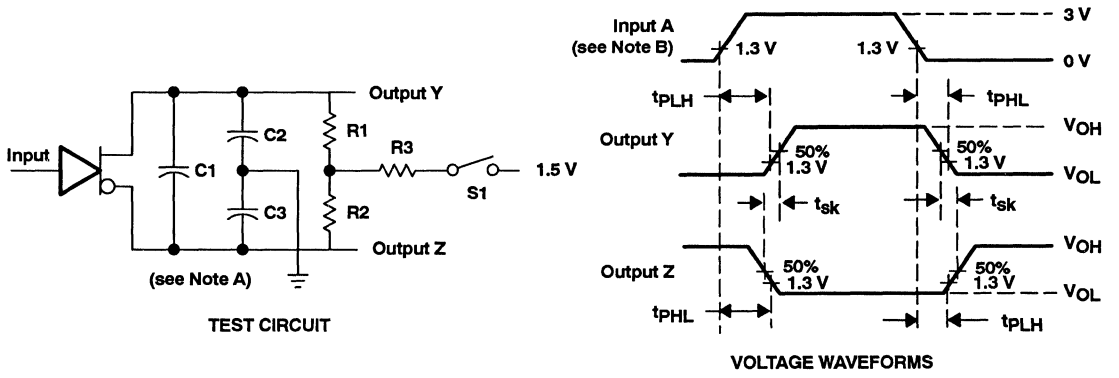


Figure 2. Driver Test Circuit and Voltage Waveforms

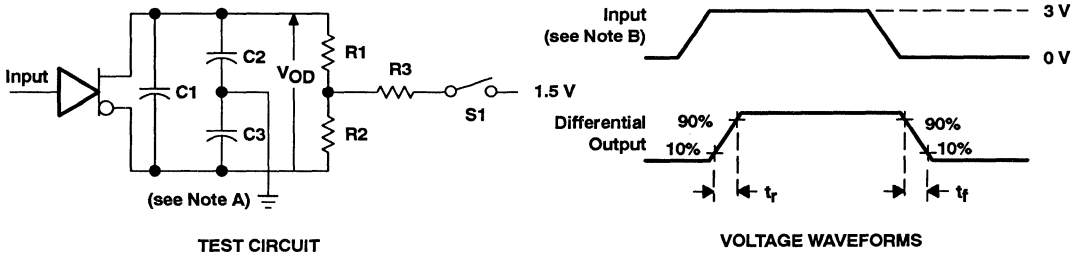


Figure 3. Driver Test Circuit and Voltage Waveforms

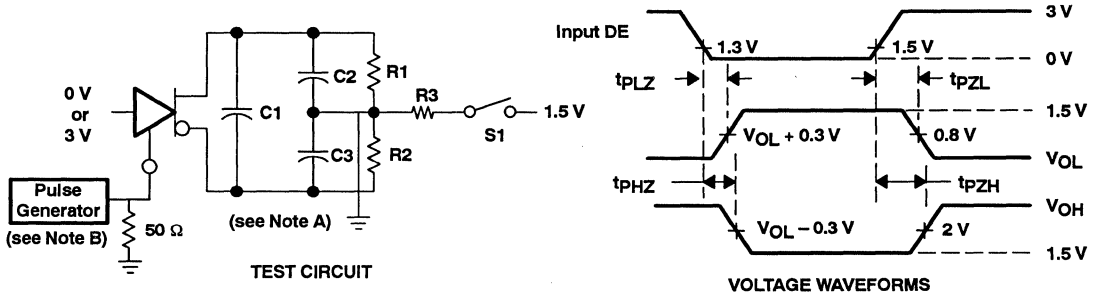


Figure 4. Driver Test Circuit and Voltage Waveforms

NOTES: A. C1 ~ C3 includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

PARAMETER MEASUREMENT INFORMATION

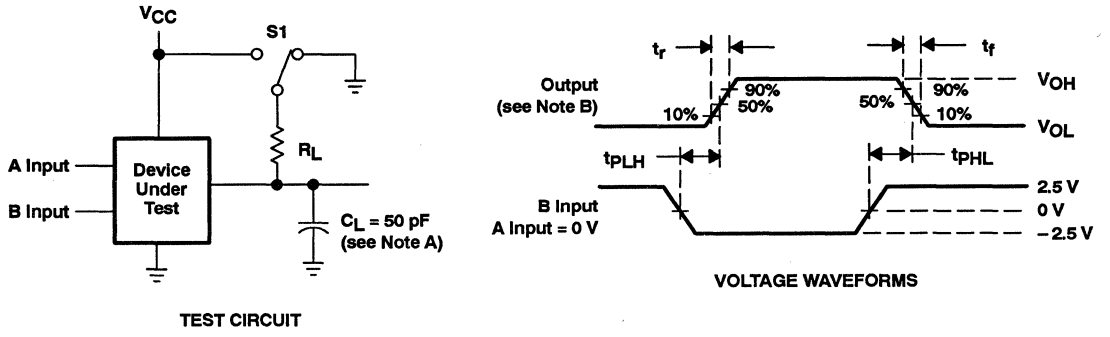


Figure 5. Receiver Test Circuit and Voltage Waveforms

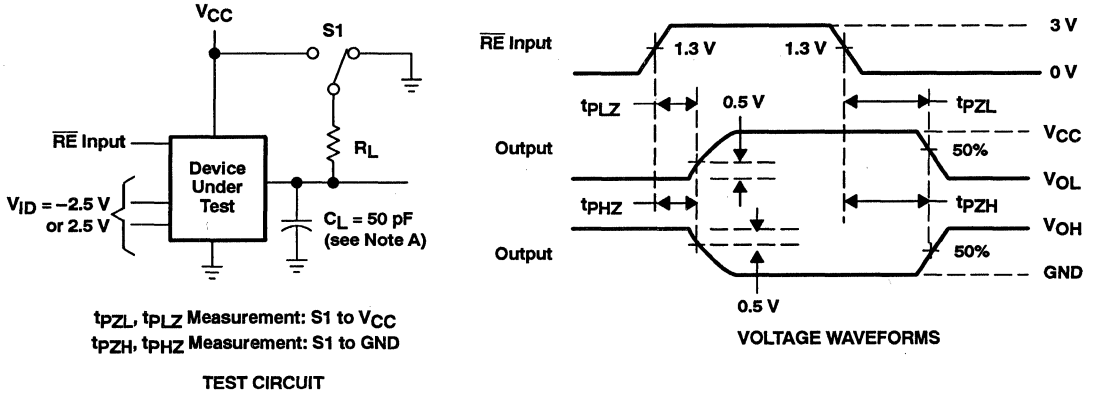


Figure 6. Receiver Test Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse a generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

SLLS059A – D3381, FEBRUARY 1990 – REVISED JANUARY 1993

- **Meets EIA Standards RS-422-A, RS485**
- **Meets CCITT Recommendations V.10, V.11, X.26, X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noise Environments**
- **Driver Common-Mode Output Voltage Range of –7 V to 12 V**
- **Driver Positive- and Negative-Current Limiting**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of –12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver High-Input-Impedance 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN751177 Only**
- **Operates From Single 5-V Supply**

description

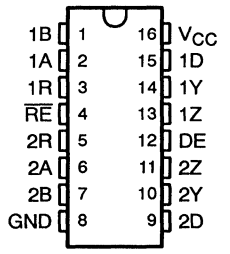
The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 Mbits per second. They are designed to improve the performance of full-duplex data communications over long bus lines and meet EIA standards RS-422-A, RS-485 and several CCITT recommendations.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on the transmission bus line.

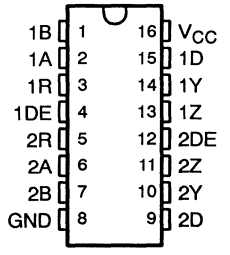
The receiver features high input impedance of 12 kΩ, an input sensitivity of ±200 mV over a common-mode input voltage range of –12 V to 12 V and typical input hysteresis of 50 mV. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs will always be high.

The SN751177 and SN751178 are characterized for operation from –20°C to 85°C.

SN751177 . . . N PACKAGE
(TOP VIEW)



SN751178 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled (order device SN751177NSLE).

Function Tables

SN751177, SN751178
EACH DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	L	L	H
X	X	Z	Z

SN751177
EACH RECEIVER

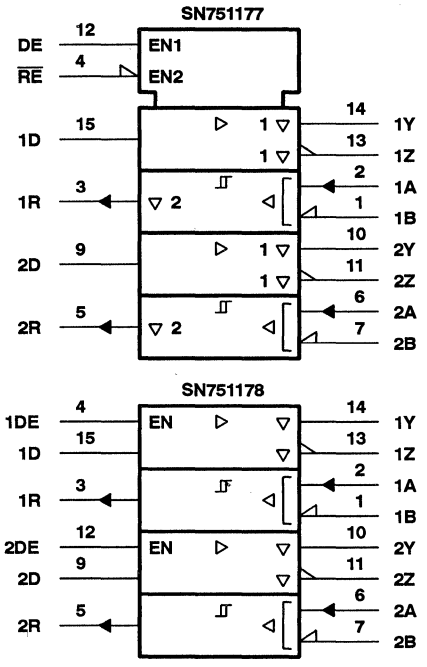
DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	L	L
$V_{ID} \leq -0.2$ V	X	X
X	H	Z
Open	L	H

SN751178
EACH RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

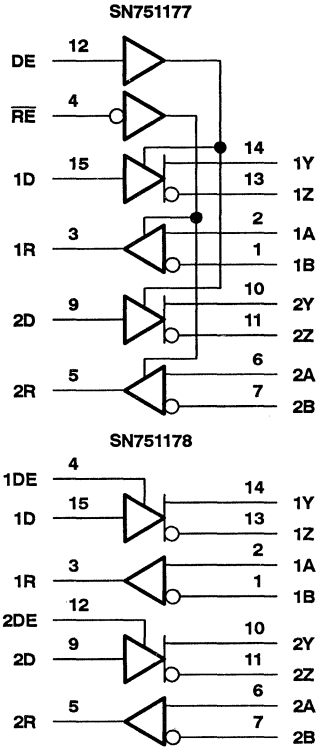
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbols†

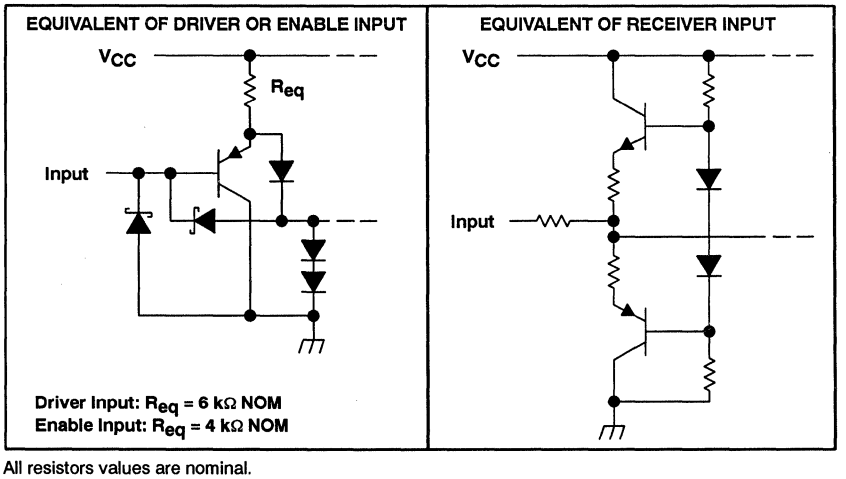


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

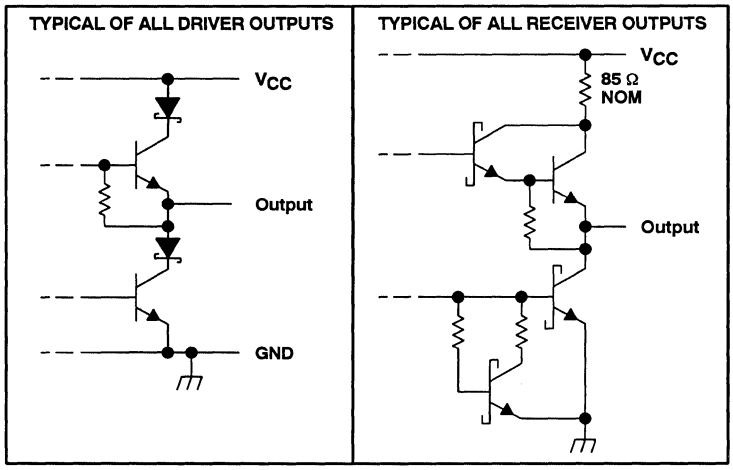


schematics of inputs



All resistors values are nominal.

schematics of outputs



All resistors values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, DE, $\overline{RE}$, and D inputs . . . . . 7 V
Input voltage range, Receiver, A or B inputs . . . . . −25 V to 25 V
Receiver differential input voltage range (see Note 2) . . . . . −25 V to 25 V
Output voltage range, Driver . . . . . −10 V to 15 V
Receiver low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, and D inputs	2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}	Driver	−7†		12	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Common-mode input voltage, V_{IC}	Receiver			±12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		−20		85	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

DRIVER SECTIONS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{OH} = -33$ mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA			1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		2			V
				1/2 V_{OD1}			
		R_L = 54 Ω, See Figure 1		1.5		5	
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage (see Note 5)	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage			−1‡		3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage (see Note 5)					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current (see Note 6)	$V_O = -7$ V				−250	mA
		$V_O = V_{CC}$				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		80	110	mA
			Outputs disabled		50	80	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

5. $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

6. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential output delay time	R_L = 54 Ω,	See Figure 3		20	25	ns
t_{tD}	Differential output transition time				27	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 4		20	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				20	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 5		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 6		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 5		90	120	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 6		30	45	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422A	RS-485
$\lvert V_{OD1} \rvert$	V_O	V_O
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{OS} \rvert$	$\lvert V_{OS} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{OS} - \overline{V}_{OS} \rvert$	$\lvert V_{OS} - \overline{V}_{OS} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTIONS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage		V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{IK}	Enable clamp voltage	SN751177	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	SN751177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input curent (see Note 7)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	SN751177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	SN751177	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current (see Note 6)				−15		−85	μA
I_{CC}	Supply current		No load,	Outputs enabled		80	110	mA
r_i	Input resistance				12			kΩ

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
NOTES: 6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
7. Refer to EIA standards RS-422-A, RS-423-A, RS-485-A for exact conditions.

switching characteristics at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		V_{ID} = −1.5 V to 1.5 V, See Figure 7		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	ns
t_{PZH}	Output enable time to high level	SN751177	See Figure 8		17	25	ns
t_{PZL}	Output enable time to low level				20	27	ns
t_{PHZ}	Output disable time from high level				25	40	ns
t_{PLZ}	Output disable time from low level				30	40	ns

PARAMETER MEASUREMENT INFORMATION

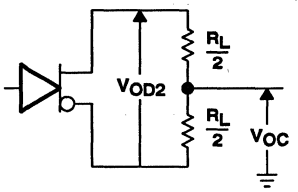


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

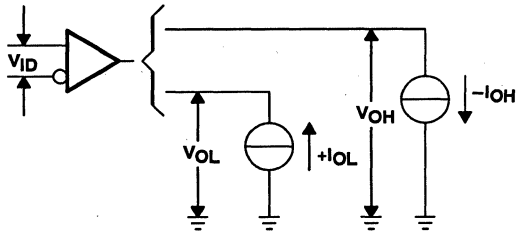
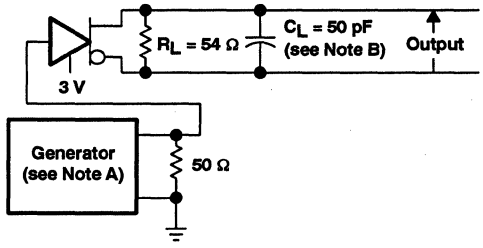
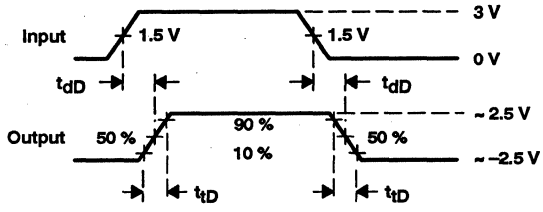


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}

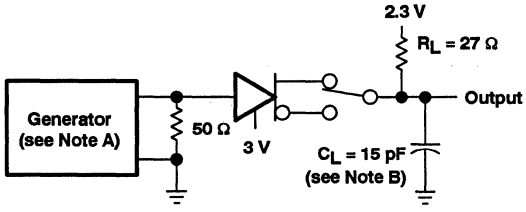


TEST CIRCUIT

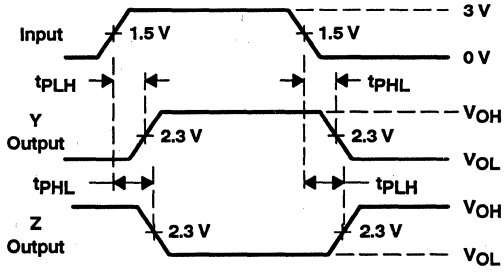


VOLTAGE WAVEFORMS

Figure 3. Driver Differential Output Delay and Transition Time Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Driver Propagation Delay Time Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

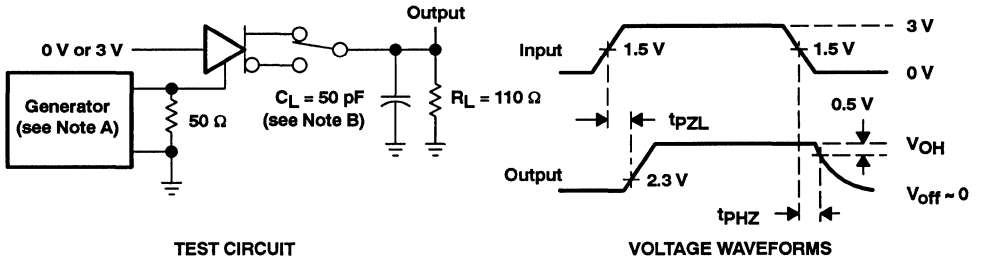


Figure 5. Driver Enable and Disable Time Test Circuit and Voltage Waveforms

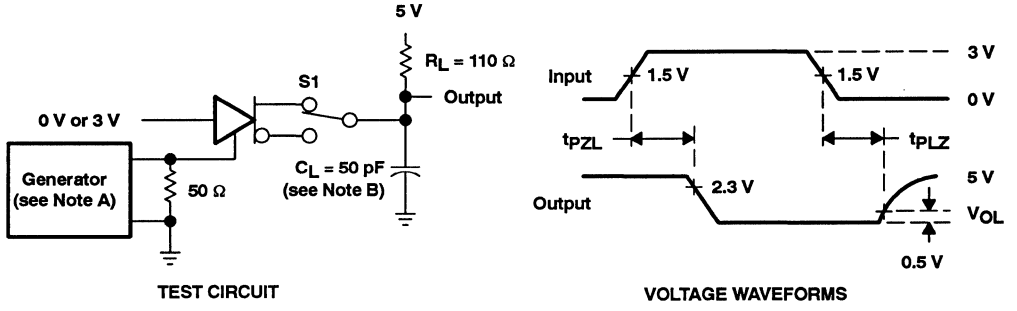


Figure 6. Driver Enable and Disable Time Test Circuit and Voltage Waveforms

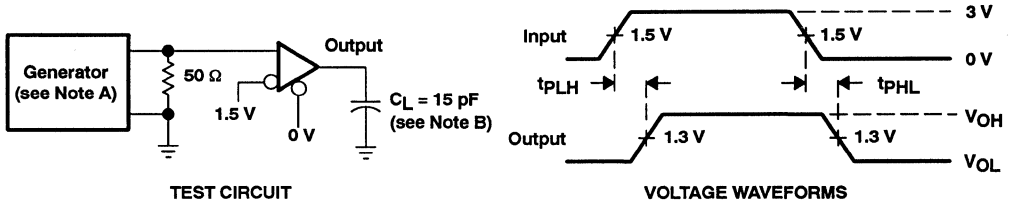
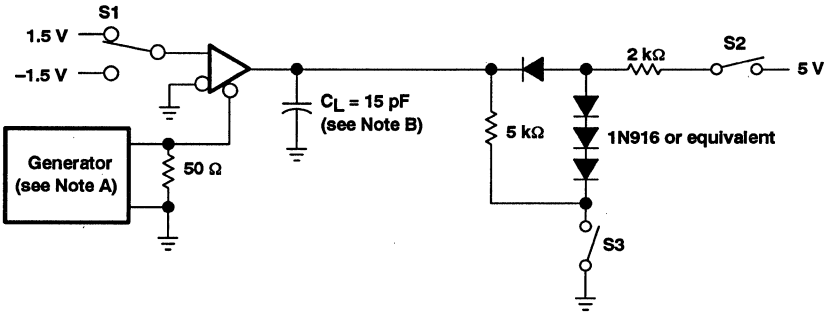


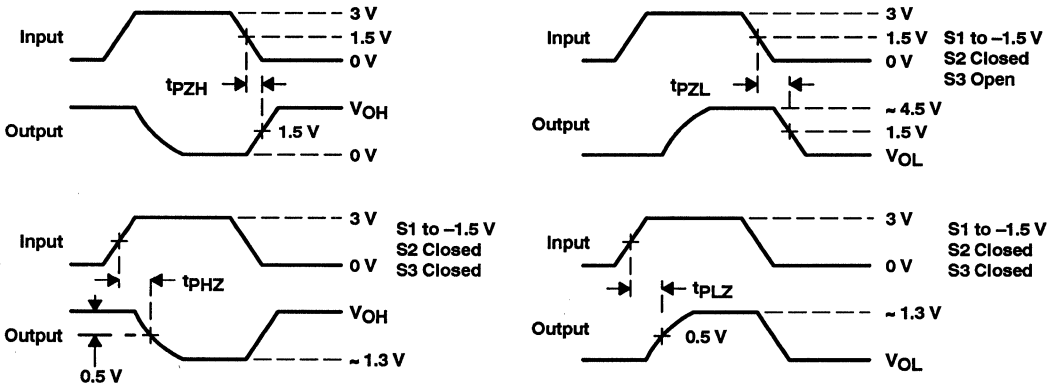
Figure 7. Receiver Propagation Delay Time Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

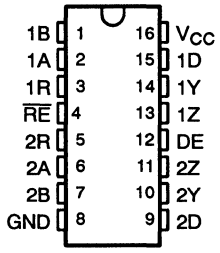
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Output Enable and Disable TIme Test Circuit and Voltage Waveforms

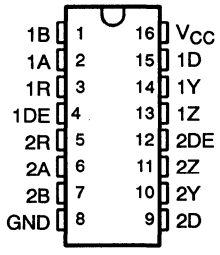
SLLS154 – D4061, MARCH 1993

- **Meet EIA Standards RS-422-A and RS485**
- **Meet CCITT Recommendations V.10, V.11, X.26, X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirement 50 mA Max**
- **Driver Positive- and Negative-Current Limiting**
- **Driver Common-Mode Output Voltage Range of −7 V to 12 V**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of −12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver High Input Impedance 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN75ALS1177 Only**
- **Operates From Single 5-V Supply**

SN75ALS1177 . . . N OR NS† PACKAGE
(TOP VIEW)



SN75ALS1178 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available in left-end taped and reeled (SN74ALS1177NSLE and SN74ALS1178SNLE).

description

The SN75ALS1177 and SN75ALS1178 dual differential drivers and receivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA standards RS-422-A, RS-485, and CCITT recommendations V.10, V.11, X.26, X.27.

The SN75ALS1177 combines dual 3-state differential line drivers and dual 3-state differential input line receivers, both of which operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN75ALS1178 drivers each have an individual active-high enable. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs will always be high.

Function Tables

SN75ALS1177, SN75ALS1178
EACH DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN75ALS1177, EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

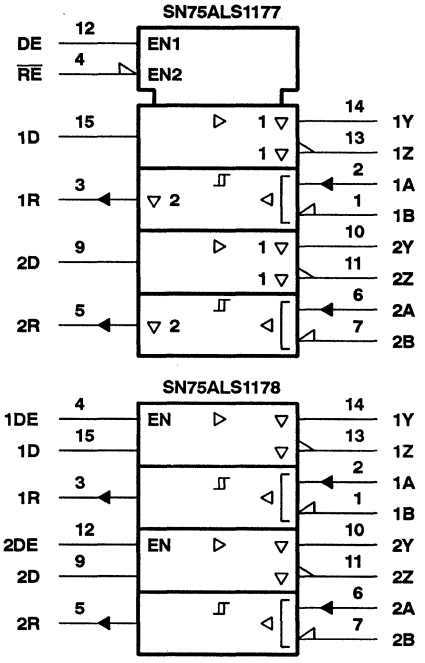
SN75ALS1178, EACH RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

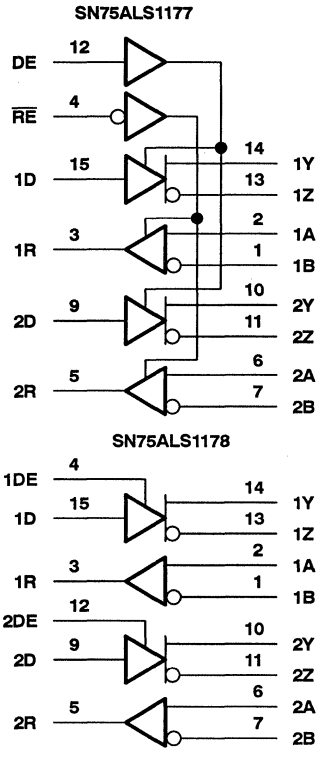
The SN75ALS1177 and SN75ALS1178 are characterized for operation from 0°C to 70°C.

logic symbols†

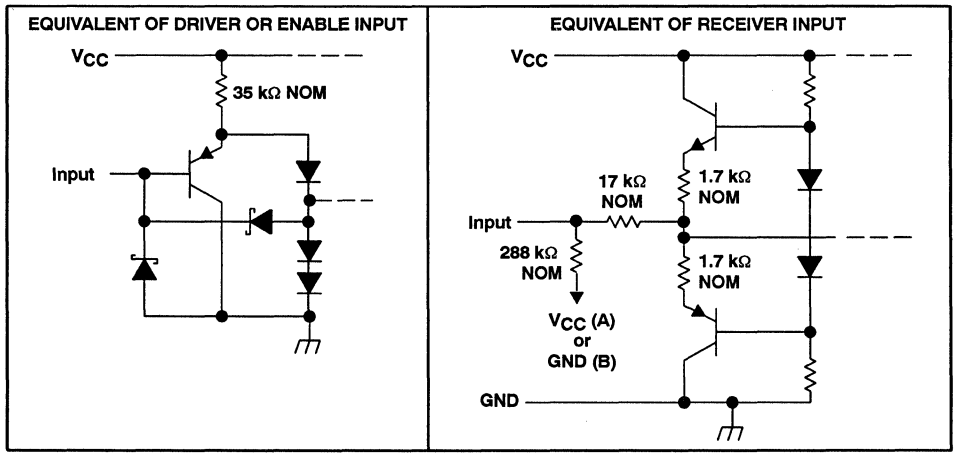


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

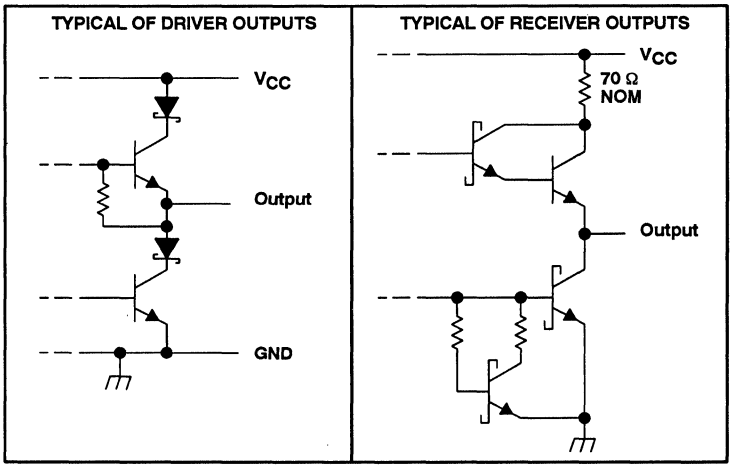


equivalent schematics



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, DE, $\overline{RE}$, and D inputs . . . . . 7 V
Output voltage range, Driver . . . . . −9 V to 14 V
Input voltage range, Receiver . . . . . −14 V to 14 V
Receiver differential input voltage range (see Note 2) . . . . . −14 V to 14 V
Receiver low-level output current . . . . . 50 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	4.0 mW/°C	445 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Differential input voltage, V_{ID}	Receiver			±12	V
Common-mode output voltage, V_{OC}	Driver	−7†		12	V
Common-mode input voltage, V_{IC}	Receiver			±12	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, D	2			V
Low-level input voltage, V_{IL}	DE, $\overline{RE}$, D			0.8	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -33$ mA			3.3		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OL} = 33$ mA			1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	$V_{CC} = 5$ V, $R_L = 100\ \Omega$	See Figure 1	1/2 V_{OD1}			V
				2			
		$R_L = 54\ \Omega$		1.5		5	
$\lvert V_{OD3}\rvert$	Differential output voltage	See Note 3		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage (see Note 4)	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage			−1‡		3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
$I_{O(OFF)}$	Output current with power off	$V_{CC} = 0$, $V_O = -7$ V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	μA
I_{IH}	High-level input current	$V_{IH} = 2.7$ V				100	μA
I_{IL}	Low-level input current	$V_{IL} = 0.4$ V				−100	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = V_{CC}$				250	
		$V_O = 12$ V				250	
		$V_O = 0$ V				150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		20	50	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, test termination measurement 2.

4. $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics at $V_{CC} = 5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high-to-low-level output	$R_L = 60\ \Omega$, See Figure 3	$C_{L1} = C_{L2} = 100$ pF,	9	15	22	ns
t_{PHL}	Propagation delay time, low-to-high-level output			9	15	22	ns
t_{sk}	Output-to-output skew			0	2	8	ns
t_{PZH}	Output enable time to high level	$C_L = 100$ pF,	See Figure 4	30	35	50	ns
t_{PZL}	Output enable time to low level	$C_L = 100$ pF,	See Figure 5	5	15	25	ns
t_{PHZ}	Output disable time from high level	$C_L = 15$ pF,	See Figure 4	7	15	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 15$ pF,	See Figure 5	7	15	30	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage		V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)					50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = 200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 5)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level input current, $\overline{RE}$	SN75ALS1177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	SN75ALS1177	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		V_O = 0 V,	See Note 6	−15		−85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled		35	50	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
NOTES: 5. Refer to EIA standards RS-422-A, RS-423-A, RS-485-A for exact conditions.
6. Not more than one output should be shorted at a time.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 15 pF,	See Figure 6	15	25	37	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns

PARAMETER MEASUREMENT INFORMATION

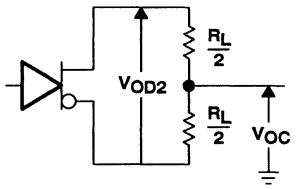


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

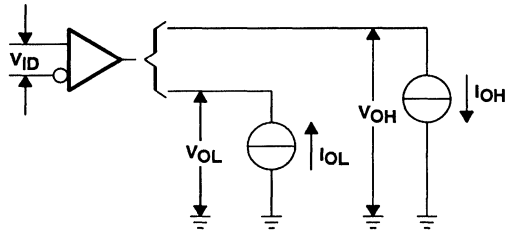
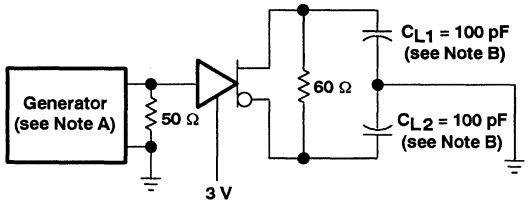
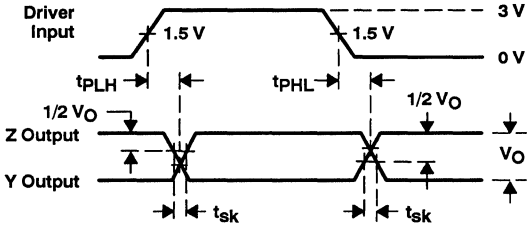


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}

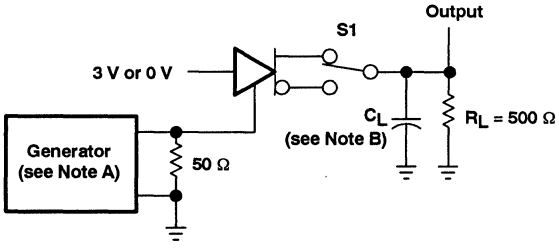


DRIVER TEST CIRCUIT

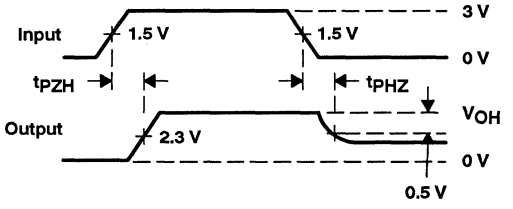


DRIVER VOLTAGE WAVEFORMS

Figure 3. Driver Propagation Delay Times



DRIVER TEST CIRCUIT



DRIVER VOLTAGE WAVEFORMS

Figure 4. Driver Enable and Disable Times

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

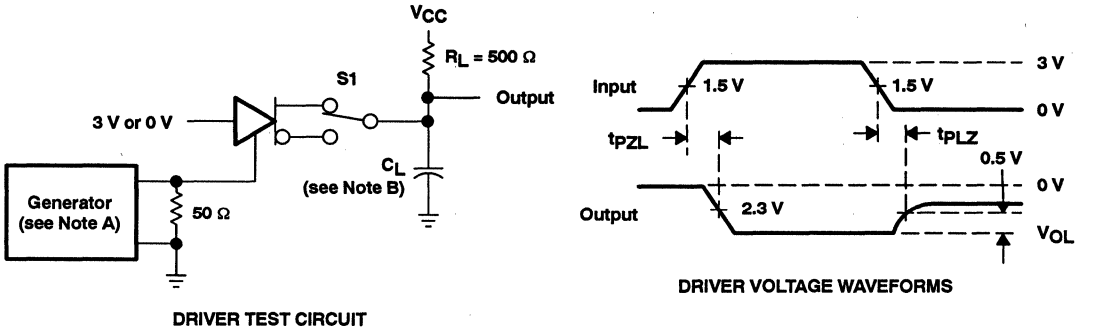


Figure 5. Driver Enable and Disable Times

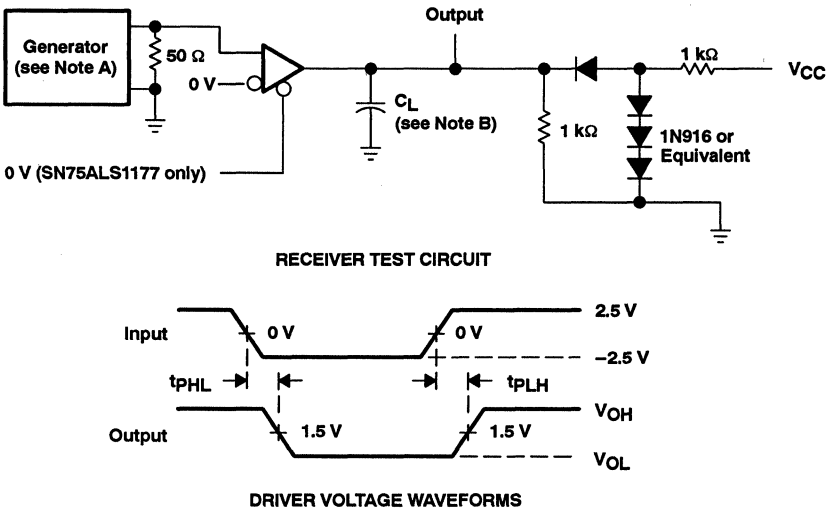
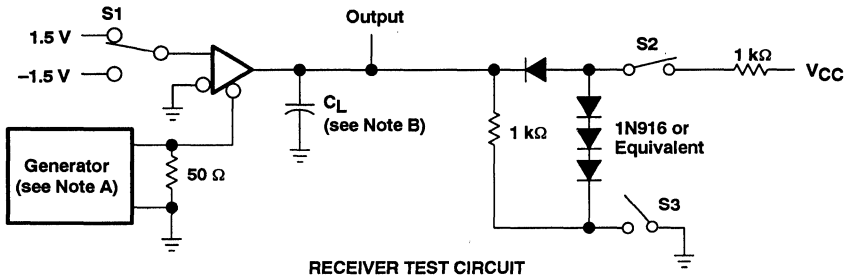


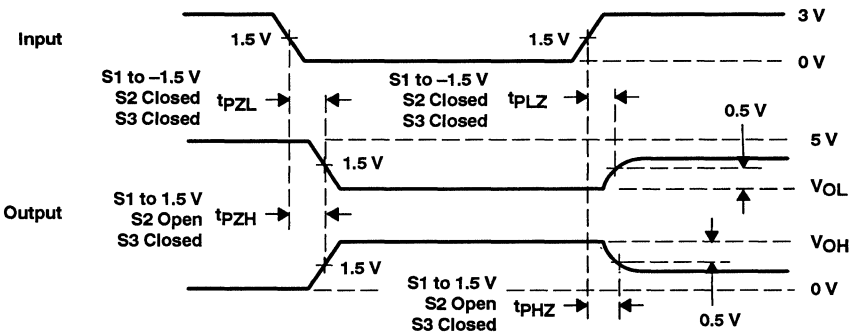
Figure 6. Receiver Propagation Delay Times

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



RECEIVER TEST CIRCUIT



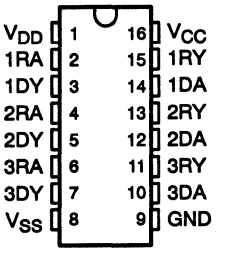
RECEIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

- **Meets Standard EIA-232-D (Revision of RS-232-C)**
- **Very Low Power Consumption . . . 5 mW Typ**
- **Wide Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable With Motorola MC145406**

D, DW, OR N PACKAGE
(TOP VIEW)



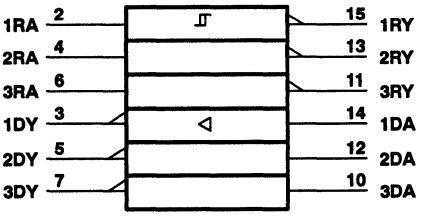
description

The SN65C1406 and SN75C1406 are low-power BI-MOS devices containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device is designed to conform to Standards ANSI/EIA-232-D-1986 (which supersedes RS-232-C). The drivers and receivers of the SN65C1406 and SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses of shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1406 and SN75C1406 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACES, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1406 and SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1406 is characterized for operation from −40°C to 85°C. The SN75C1406 is characterized for operation from 0°C to 70°C.

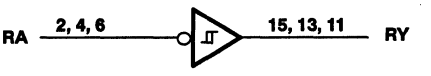
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

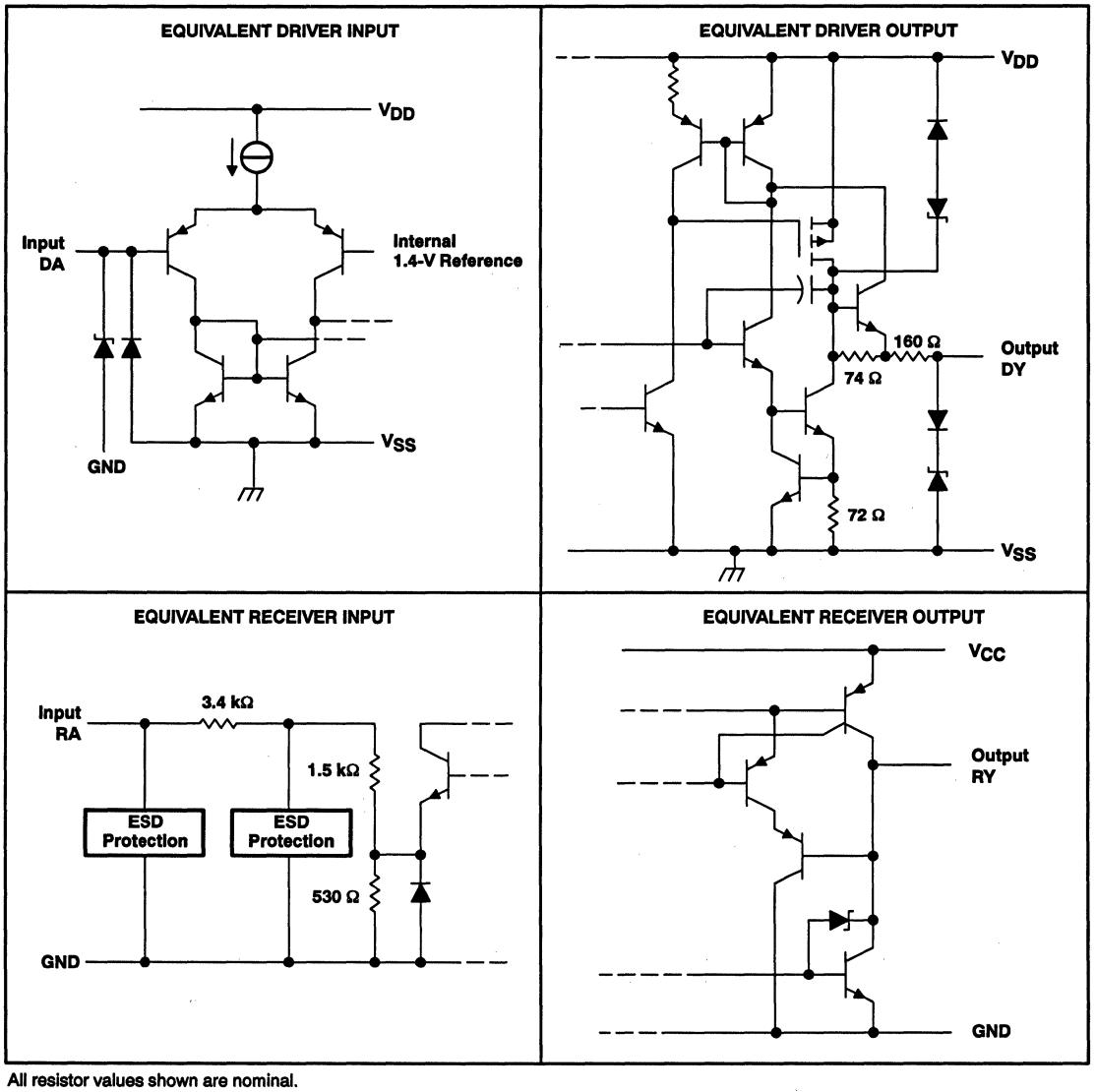
logic diagram (positive logic)

Typical of each receiver



Typical of each driver

schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} ..... −15 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range: Driver ..... V_{SS} to V_{DD}
Receiver ..... −30 V to 30 V
Output voltage range: Driver ..... (V_{SS} − 6 V) to (V_{DD} + 6 V)
Receiver ..... −0.3 V to (V_{CC} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65C1406 ..... −40°C to 85°C
SN75C1406 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	15	V
Supply voltage, V_{SS}		−4.5	−12	−15	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I	Driver	V_{SS}+2		V_{DD}	V
	Receiver			±25	
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}				−1	mA
Low-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C1406	−40		85	°C
	SN75C1406	0		70	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
			V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
			V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2				1	μA
I_{IL}	Low-level input current	V_I = 0 V, See Figure 2				−1	μA
$I_{OS(H)}$	High-level short circuit output current‡	V_I = 0.8 V, V_O = 0 or V_{SS}, See Figure 1		−7.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short circuit output current‡	V_I = 2 V, V_O = 0 or V_{DD}, See Figure 1		7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		115	250	μA
			V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	μA
			V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, V_O = −2 V to 2 V, See Note 3		300	400		Ω

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at one time.
NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Test conditions are those specified by EIA-232-D.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	μs
t_{PHL}	Propagation delay time, high-to-low level output§			2.5	3.5	μs
t_{TLH}	Transition time, low-to-high level output¶		0.53	2	3.2	μs
t_{THL}	Transition time, high-to-low level output¶		0.53	2	3.2	μs
t_{TLH}	Transition time, low-to-high level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	μs
t_{THL}	Transition time, high-to-low level output#			1	2	μs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 150 pF, See Figure 3	4	10	30	V/μs

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform.
# Measured between 3 V and −3 V points of output waveform (EIA-232-D conditions) with all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshhold voltage	See Figure 5		1.7	2	2.55	V
V_{T-}	Negative-going threshhold voltage	See Figure 5		0.65	1	1.25	V
V_{hys}	Input hysteresis (V_{T+}–V_{T-})			600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 μA, See Figure 5 and Note 4		3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V	2.8	4.4		
			V_{CC} = 5 V	3.8	4.9		
			V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5			0.17	0.4	V
I_{IH}	High-level input current	V_I = 2.5 V		3.6	4.6	8.3	mA
		V_I = 3 V		0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −2.5 V		−3.6	−5	−8.3	
		V_I = −3 V		−0.43	−0.55	−1	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V, V_O = 0, See Figure 4			−8	−15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4			13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V, V_{SS} = −5 V		320	450	mA
			V_{DD} = 12 V, V_{SS} = −12 V		320	450	

† All typical values are at T_A = 25°C.

NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 50 pF, R_L = 5 kΩ See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high-to-low level output			3	4	μs
t_{TLH}	Transition time, low-to-high level output‡			300	450	ns
t_{THL}	Transition time, high-to-low level output‡			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§	C_L = 50 pF, R_L = 5 kΩ	1		4	μs

‡ Measured between 10% and 90% points of output waveform.

§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

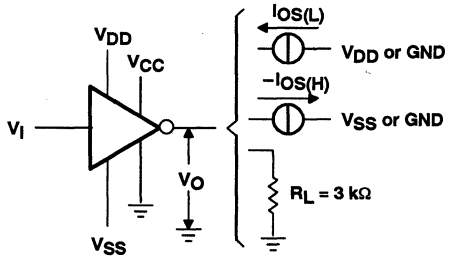


Figure 1. Driver Test Circuit V_{OH}, V_{OL}, I_{OSL}, I_{OSH}

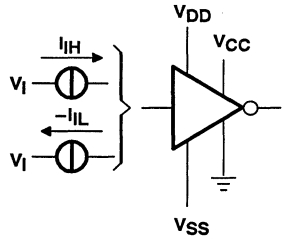
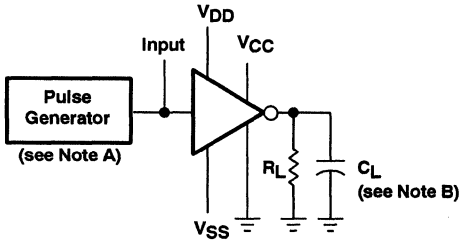
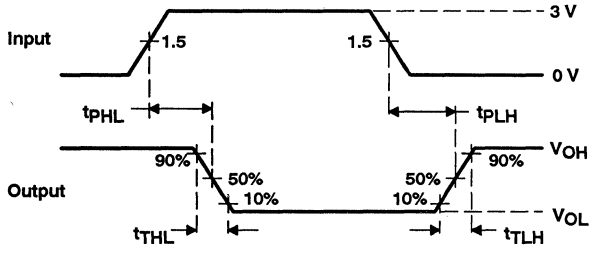


Figure 2. Driver Test Circuit, I_{IL}, I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

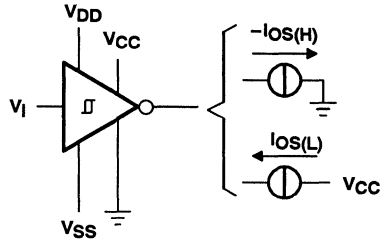


Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$

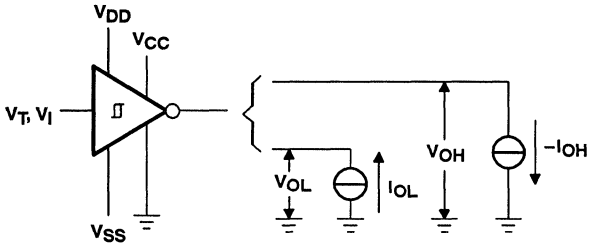
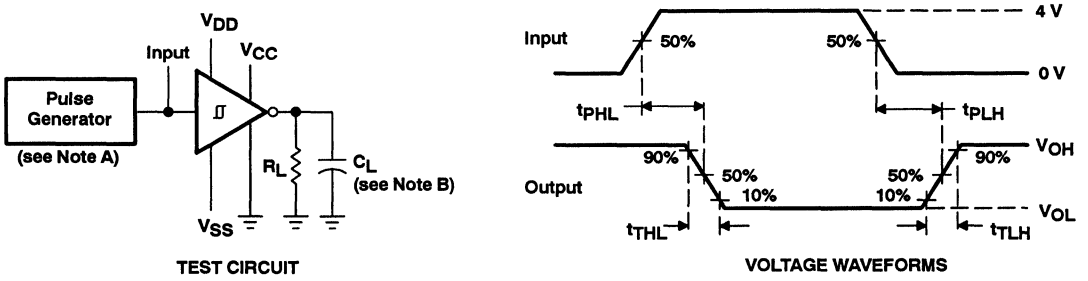


Figure 5. Receiver Test Circuit, V_T, V_{OL}, V_{OH}

PARAMETER MEASUREMENT INFORMATION



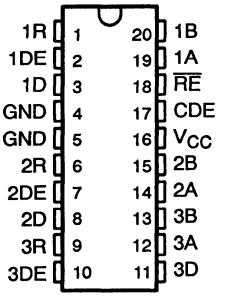
NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

SLLS117A – D3848, APRIL 1991 – REVISED FEBRUARY 1993

- **Three Bidirectional Transceivers**
- **Driver/Receiver Meets EIA Standard RS-485 and ANSI Standard X3.131-1986 (SCSI)**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges . . . –7 V to 12 V**
- **Driver Output Capacity . . . ±60 mA**
- **Driver Positive and Negative Current Limiting**
- **Thermal Shutdown Protection**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From a Single 5-V Supply**
- **Low Supply-Current Requirements 72 mA Max**
- **Glitch-Free Power-Up and Power-Down Protection**

DW OR N PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

INPUT	ENABLES		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$V_{ID} = -0.2$ V to 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high-level, L = low-level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

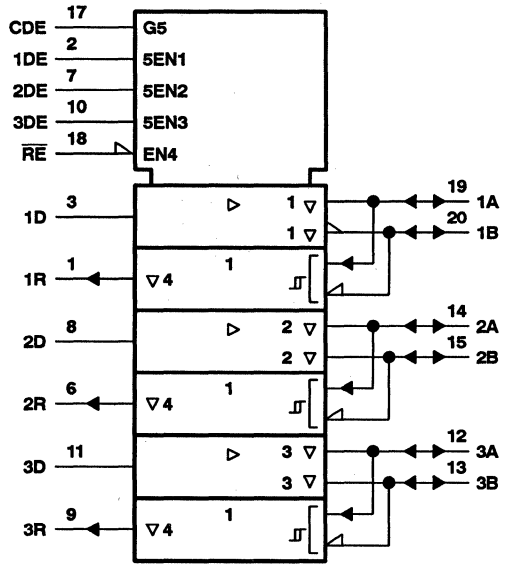
description

The SN75ALS1711 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standards RS-485 and ANSI Standard X3.131-1986 (SCSI).

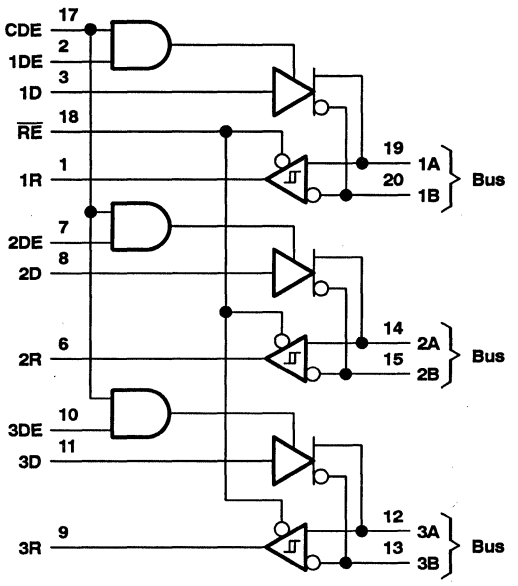
The SN75ALS1711 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS1711 is characterized for operation from 0°C to 70°C.

logic symbol†

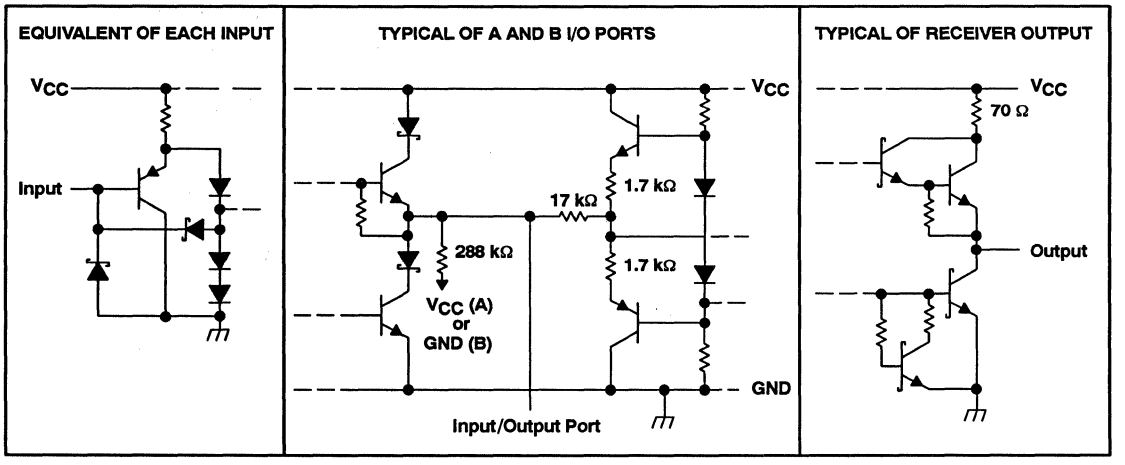


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



All values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Enable input voltage range ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I: Driver ..... −0.5 V to V_{CC} + 0.5 V
Receiver ..... −9 V to 14 V
Output voltage range, V_O: Driver ..... −9 V to 14 V
Receiver ..... −0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage at any bus terminal, V_{IC} (see Note 2)		−7†		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$, CDE	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$, CDE			0.8	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OD1}	Differential output voltage	$I_O = 0$		1.5		5	V
V_{OD2}	Differential output voltage	$R_L = 54\ \Omega$, See Figure 1		1.5		5	V
V_{OD3}	Differential output voltage	See Note 3 and Figure 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$, See Figure 1				3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡	$R_L = 54\ \Omega$, See Figure 1				±0.2	V
I_{OZ}	High-impedance state output current	Output disabled, $V_{CC} = 5.25$ V	$V_O = 12$ V			1	mA
			$V_O = 7$ V			−0.8	
I_{IH}	High-level input current, DE, EN, CDE	$V_{IH} = 2.4$ V				20	μA
I_{IL}	Low-level input current, DE, EN, CDE	$V_{IL} = 0.4$ V				−200	μA
I_{OS}	Short-circuit output current	$V_O = 12$ V				−250	mA
		$V_O = 7$ V				250	
I_{CC}	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics, $V_{CC} = 5$ V ±5%, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Differential propagation delay time, low-to-high level output	$R_L = 54\ \Omega$, $C_L = 100$ pF, See Figure 3		8	13	22	ns
t_{PHL}	Differential propagation delay time, high-to-low level output			8	15	22	
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4	S1 open, S2 closed	30	50	60	ns
t_{PHZ}	Output disable time from high level			4	16	30	
t_{PZL}	Output enable time to low level		S1 closed, S2 open	16	26	45	
t_{PLZ}	Output disable time from low level			4	8	20	

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going threshold voltage	V_O = 0.5 V,	I_O = 4 mA	−0.2‡			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				50		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = 18 mA				−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.5	V
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V,	V_O = 0.4 V to 2.4 V			±20	μA
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 12 V			1	mA
			V_I = 7 V			−0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.4 V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.4 V				−200	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current§	V_O = 0		−15		−130	mA
I_{CC}	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Not more than one output should be shorted at one time.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V ± 5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 5 and 6		13	20	37	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	20	37	
t_{PZH}	Output enable time to high level	See Figures 5 amd 7	S1 to 1.5 V, S2 open, S3 closed	3	9	20	ns
t_{PHZ}	Output disable time from high level			8	15	22	
t_{PZL}	Output enable time to low level		S1 to −1.5 V, S2 closed, S3 open	5	10	20	
t_{PZL}	Output enable time to low level			5	9	16	

PARAMETER MEASUREMENT INFORMATION

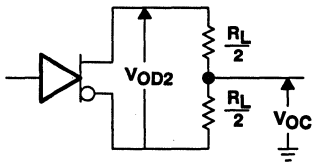


Figure 1. Driver V_{OD} and V_{OC}

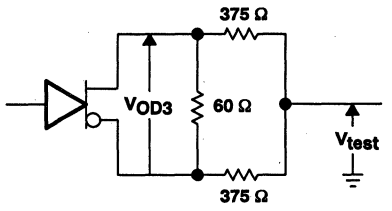
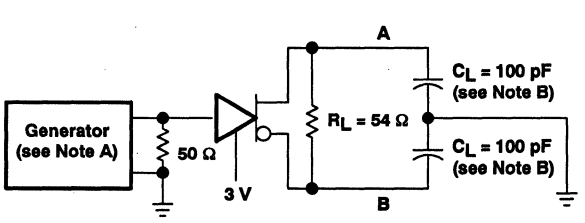


Figure 2. Driver V_{OD3}



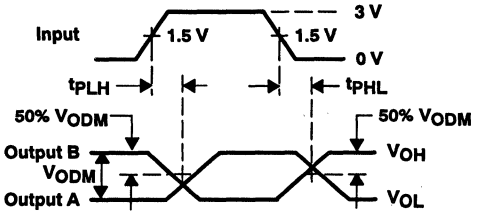
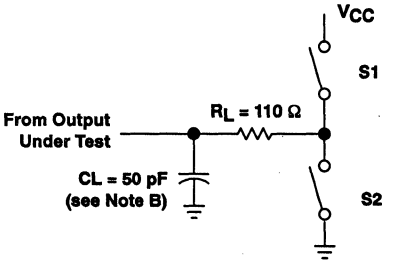


Figure 3. Driver Propagation Delay Times



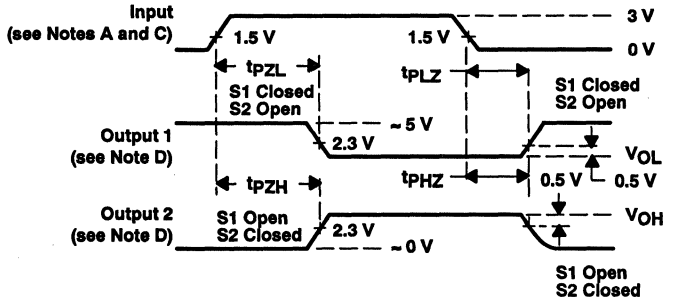


Figure 4. Driver Enable/Disable Times

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.
C. Each enable is tested separately.
D. Output 1 and output 2 are outputs with internal conditions such that the output is low or high except when disabled by the output control.

PARAMETER MEASUREMENT INFORMATION

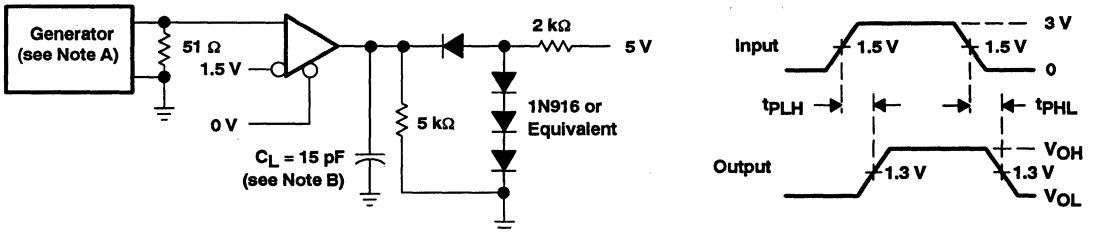


Figure 5. Receiver Propagation Delay Times

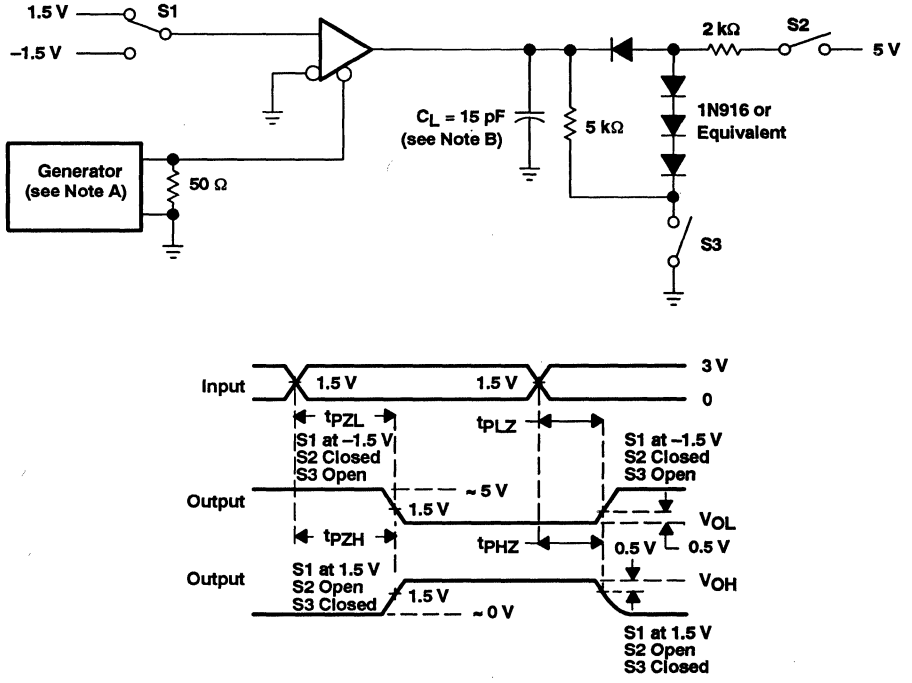


Figure 6. Receiver Enable/Disable Times

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

- **Meets IBM 360/370 Input/Output Interface Specification for 4.5 Mb/s Operation**
- **Single 5-V Supply**
- **Uncommited Emmitter-Follower Output Structure for Party-Line Operation**
- **Driver Output Short-Circuit Protection**
- **Driver Input/Receiver Output Compatible With TTL**
- **Receiver Input Resistance . . . 7.4 kΩ to 20 kΩ**
- **Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low**

description

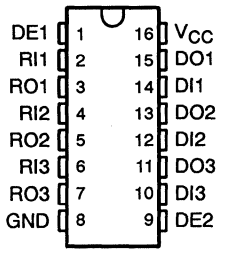
The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

An open line will affect the receiver input as would a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line, by pulling either DE1 or DE2 to a low level.

D OR N PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

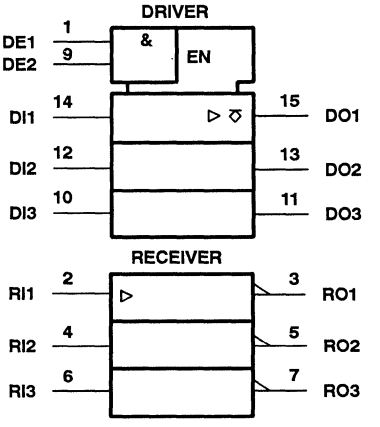
INPUTS			OUTPUT
DI	DE1	DE2	DO
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

EACH RECEIVER

INPUT RI	OUTPUT RO
L	H
H	L
Open	H

H = high level, L = low level, X = irrelevant

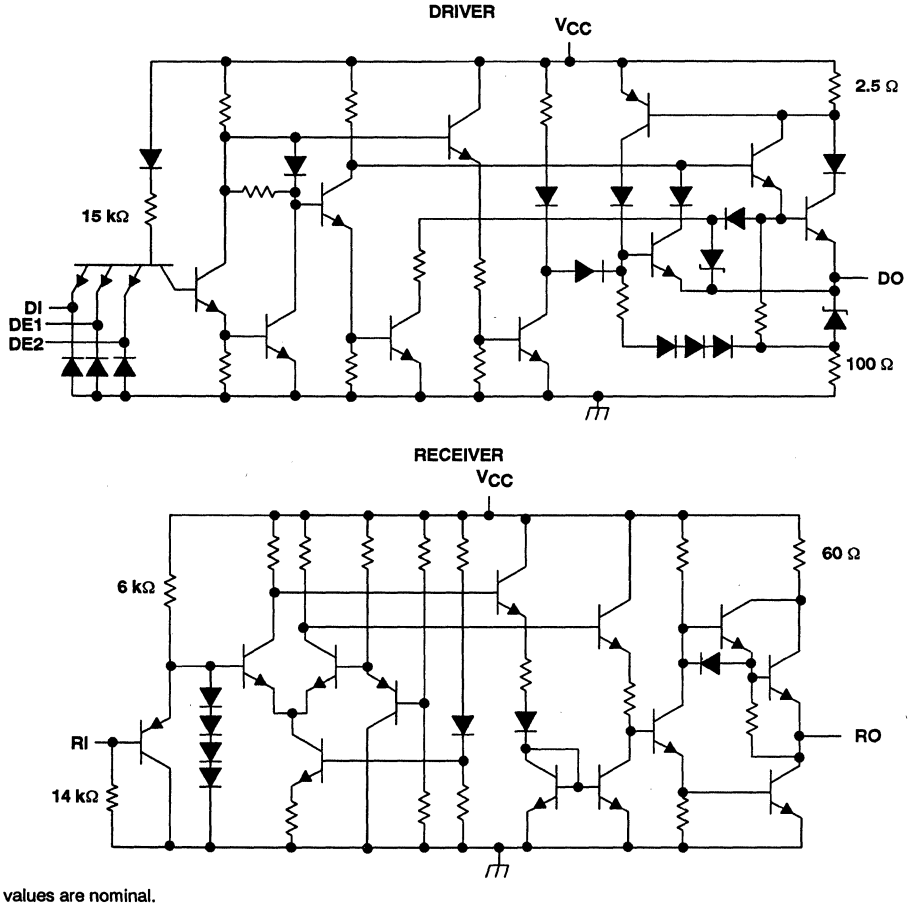
logic symbols†



† These symbols are in accordance with ANSI/IEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

equivalent schematics of driver and receiver†



† All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I: Driver ..... −0.5 V to 7 V
Receiver ..... −0.5 V to 7 V
Output voltage range, V_O: Driver ..... −0.5 V to 7 V
Enable input voltage range ..... −0.5 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mV	7.6 mW/°C	608 mW
N	1150 mV	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver, Enable	2			V
	Receiver	1.55			
Low-level input voltage, V_{IL}	Driver, Enable			0.8	V
	Receiver			1.15	
Operating free-air temperature, T_A		0		70	°C

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_{IL} = –18 mA		–1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, I_{OH} = –59.3 mA	V_{IH} = 2 V, T_A = 25°C	3.11		V
			V_{CC} = 5.25 V, I_{OH} = –78.1 mA	V_{IH} = 2 V,		4.10	
			V_{CC} = 4.75 V, R_L = 51.4 Ω	V_{IH} = 2 V,	3.05		
			V_{CC} = 5.25 V, R_L = 56.9 Ω	V_{IH} = 2 V,		4.20	
V_{ODH}	Differential high-level output voltage		R_L = 46.3 Ω or 56.9 Ω			0.50	V
V_{OL}	Low-level output voltage		V_{CC} = 5.25 V, V_{IL} = 0.8 V, V_{IH} = 4.5 V	I_{OL} = –0.24 mA		0.15	V
				R_L = 56.9 Ω		0.15	
I_{IH}	High-level input current	DI	V_{CC} = 5.25 V,	V_{IH} = 2.7 V		20	µA
		DE				60	
I_{IL}	Low-level input current	DI	V_{CC} = 5.25 V,	V_{IH} = 0.4 V		–400	µA
		DE				–1200	
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{OH} = 5 V	V_{IL} = 0		100	µA
				V_{IH} = 4.5 V		100	
I_{OS}	Short-circuit output current†		V_{CC} = 5.25 V	V_{IH} = 4.5 V		–30	mA
I_{CCH}	Supply current (total package)		V_{CC} = 5.25 V, No load	$V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0		47	mA
I_{CCL}				$V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V		80	

† No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to–high level output	R_L = 47.5 Ω,	See Figure 1	6.5	12	18.5	ns
t_{PHL}	Propagation delay time, high-to-low level output			6.5	12	18.5	ns
Δt_{pd}	Differential propagation delay time‡					10	ns
t_r	Output rise time	V_{CC} = 5 V, R_L = 47.5 Ω, See Figure 1	V_O = 0.15 V to 3.05 V, C_L = 10.2 pF,	5	10		ns
t_f	Output fall time			5	13		ns
SR	Slew rate	V_O = 1 V to 3 V average, R_L = 47.5 Ω, See Figure 1	C_L = 10.2 pF,			0.65	V/ns

‡ $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −400 μA	V_I = 1.15 V,	2.7		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 1.55 V	I_{OL} = 8 mA		0.5	V
			I_{OL} = 4 mA		0.4	
r_i	Input resistance	V_{CC} = 0,	V_I = 0.15 V to 3.9 V	7.4	20	kΩ
I_{IH}	High-level input current	V_{CC} = 4.75 V,	V_{IH} = 3.11 V		0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_{IL} = 0.15 V	−0.24	0.04	mA
I_{OS}†	Short-circuit output current	V_{CC} = 5.25 V,	V_{IL} = 0	−20	−100	mA
I_{CCH}	Supply current (total package)	V_{CC} = 5.25 V, No load	$V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0		47	mA
I_{CCL}			$V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V		80	

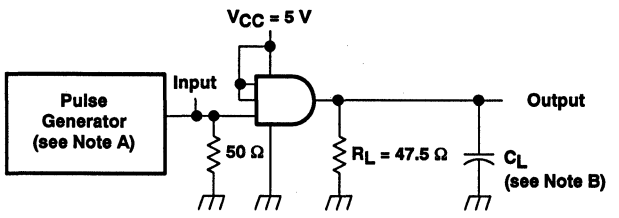
† Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

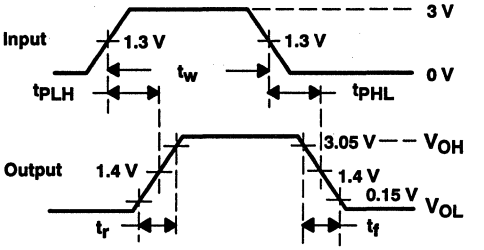
switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 2 kΩ, C_L = 15 pF, See Figure 2	7.5	12	19.5	ns
t_{PHL}	Propagation delay time, high-to-low level output		7.5	12	19.5	ns
Δt_{pd}‡	Differential propagation delay time				10	ns

‡ $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

PARAMETER MEASUREMENT INFORMATION

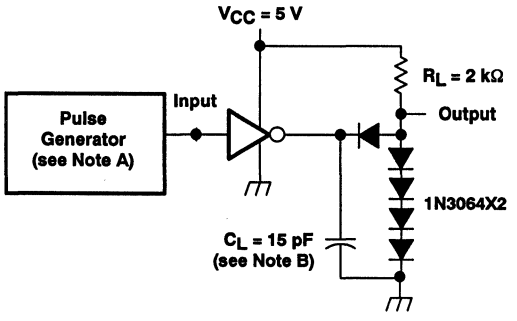


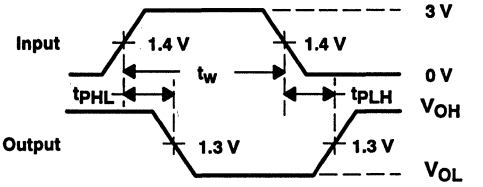


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: $Z_O \sim 50\ \Omega$, $t_w \leq 500$ ns, PRR ≤ 1 MHz, $t_f \leq 6$ ns, $t_r \leq 15$ ns.
B. C_L includes probe and jig capacitance.

Figure 1. Driver Test Circuit and Voltage Waveforms





TEST CIRCUIT **VOLTAGE WAVEFORMS**

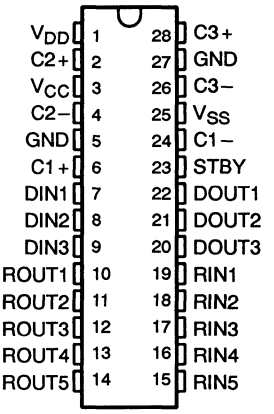
NOTES: A. The pulse generator has the following characteristics: $Z_O \sim 50\ \Omega$, $t_w \leq 500$ ns, PRR ≤ 1 MHz, $t_f \leq 10$ ns, $t_r \leq 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 2. Receiver Test Circuit and Voltge Waveforms

SLLS135B – D4072, FEBRUARY 1992 – REVISED APRIL 1993

- **Meets ANSI/EIA-232-D, 1986 Specifications (Revision of EIA Standard RS-232-C)**
- **Operates With Single 3.3-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Three Drivers and Five Receivers**
- **±30-V Input Levels (Receiver)**
- **ESD Protection on RS-232 Lines Exceeds 6 kV Per MIL-STD-883C, Method 3015**
- **Applications**
  - **EIA-232 Interface**
  - **Battery-Powered Systems**
  - **Notebook PC**
  - **Computers**
  - **Terminals**
  - **Modems**
- **Voltage Converter Operates With Low Capacitance . . . 0.47 μF Min**

DB PACKAGE
(TOP VIEW)



description

The SN75LV4735† is a low-power 3.3-V multichannel RS232 line driver/receiver. It includes three independent RS232 drivers and five independent RS232 receivers. It is designed to operate off of a single 3.3-V supply and has an internal switched-capacitor voltage converter to generate the RS232 output levels. The SN75LV4735 provides a single integrated circuit and single 3.3-V supply interface between the asynchronous communications element (ACE or UART) and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standard ANSI/EIA-232-D-1986.

The switched-capacitor voltage converter of the SN75LV4735 uses four small external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 3.3-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage.

The device also features a reduced power or standby mode that cuts the quiescent power to the integrated circuits when not transmitting data between the CPU and peripheral equipment. The STBY input is driven high for standby (reduced power) mode and driven low for normal operating mode. When in the standby mode, all driver outputs (DIN1–3) and receiver outputs (ROUT1–3) are in a high-impedance state. If the standby feature is not used in an application, STBY should be tied to GND.

The SN75LV4735 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LV4735 is characterized for operation from 0°C to 70°C.

† Patent pending design

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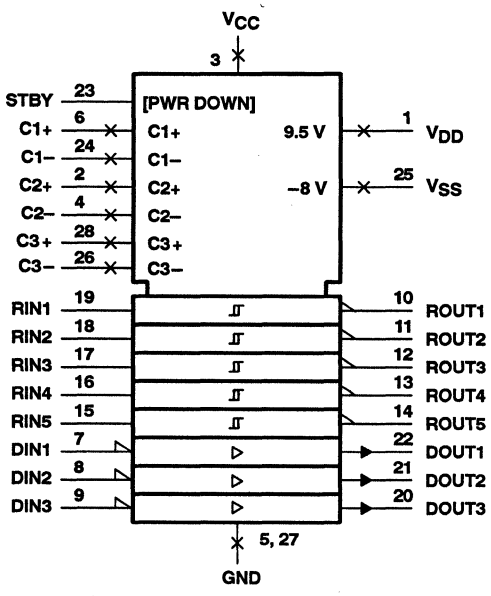
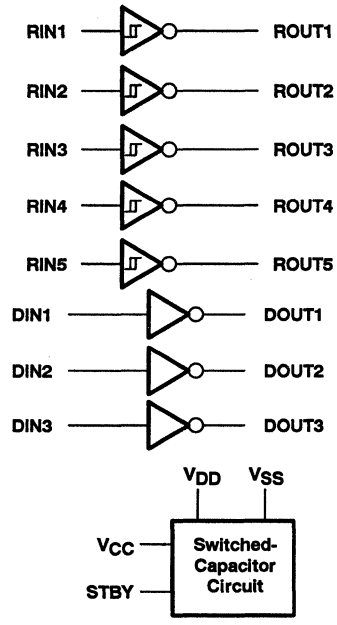
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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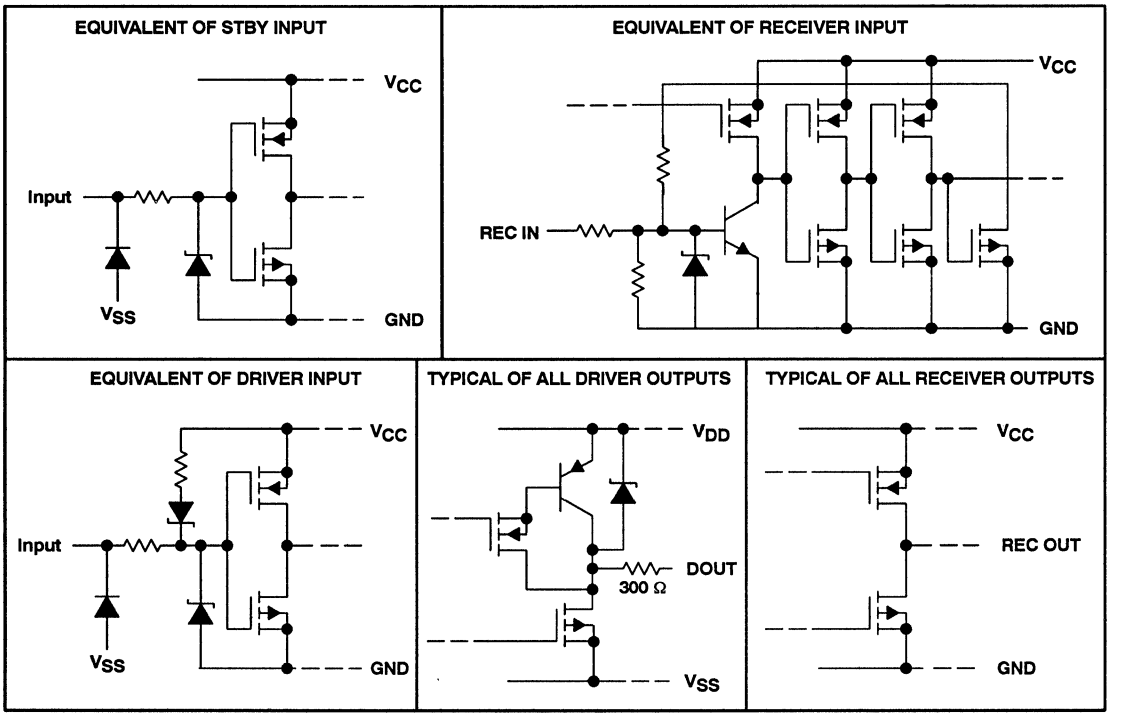
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 4 V
Positive output supply voltage, V_{DD} (see Note 1) ..... 15 V
Negative output supply voltage, V_{SS} ..... −15 V
Input voltage range, V_I: DIN1–DIN3, STBY ..... −0.3 to 7 V
RIN1–RIN5 ..... −30 V to 30 V
Output voltage range, V_O: DOUT1–DOUT3 ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
ROUT1–ROUT5 ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	665 mW	5.3 mW/°C	430 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive output supply voltage, V_{DD}		8	10		V
Negative output supply voltage, V_{SS}		−7	−8		V
Input voltage, V_I (see Note 2)	DIN1–3, STBY	0		V_{CC}	V
	RIN1–5			±30	
High-level input voltage, V_{IH}	DIN1–3, STBY	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	RIN1–5			−1	mA
Low-level output current, I_{OL}				3.2	
External capacitor		0.47	1		µF
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC} (normal operating mode)	V_{CC} = 3.3 V, No load, STBY = low-level input, All other inputs open		8.5	20	mA
I_{CC}	Supply current (standby mode)	V_{CC} = 3.3 V, No load, STBY = high-level input			10	µA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{CC} = 3.3 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ	5.5	7		V
V_{OL}	Low-level output voltage (see Note 2)	R_L = 3 kΩ	−5	−5.5		V
I_I	Input current, STBY				±1	μA
I_{IH}	High-level input current				1	μA
I_{IL}	Low-level input current				−1	μA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)	V_{CC} = 3.6 V, V_O = 0		−10	−20	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)	V_{CC} = 3.6 V, V_O = 0		10	20	mA
r_o	Output resistance	$V_{CC} = V_{DD} = V_{SS}$ = 0, V_O = −2 V to 2 V, See Note 4	300			Ω

† All typical values are at T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA-232-D.

switching characteristics, V_{CC} = 3.3 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 2	200	400	600	ns
t_{PHL}	Propagation delay time, high-to-low-level output		100	200	350	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 3		3	7	ms
t_{PZH}	Output enable time to high level (see Note 5)			1	5	ms
t_{PHZ}	Output disable time from high level (see Note 5)			1	3	μs
t_{PLZ}	Output disable time from low level (see Note 5)			0.5	3	μs
SR	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF, See Figure 2	3		30	V/μs
$SR_{(tr)}$	Transition region slew rate	R_L = 3 kΩ to GND, C_L = 2500 pF, See Figure 4		3		V/μs

NOTES: 5. Output enable occurs when STBY is driven low. Output disable occurs when STBY is driven high.
6. Measured between 3-V and −3-V points of output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage			2.2	2.6	V
V_{T-}	Negative-going threshold voltage		0.6	1		V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)		0.5	1.2	1.8	mV
V_{OH}	High-level output voltage	I_{OH} = −2 mA, See Note 7	2.4	2.6		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.2	0.4	V
I_{IH}	High-level input current	V_I = 3 V	0.43	0.55	1	mA
		V_I = 25 V	3.6	4.6	8.3	
I_{IL}	Low-level input current	V_I = −3 V	−0.43	−0.55	−1	mA
		V_I = −25 V	−3.6	−5	−8.3	
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at T_A = 25°C.

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs will remain in the high state.

switching characteristics over recommended supply voltage range, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 5	45	80	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		70	100	170	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 6		160	250	ns
t_{PZH}	Output enable time to high level (see Note 5)			4	10	µs
t_{PHZ}	Output disable time from high level (see Note 5)			300	500	ns
t_{PLZ}	Output disable time from low level (see Note 5)			140	200	ns

NOTE 5: Output enable occurs when STBY is driven low. Output disable occurs when STBY input is driven high.

APPLICATION INFORMATION

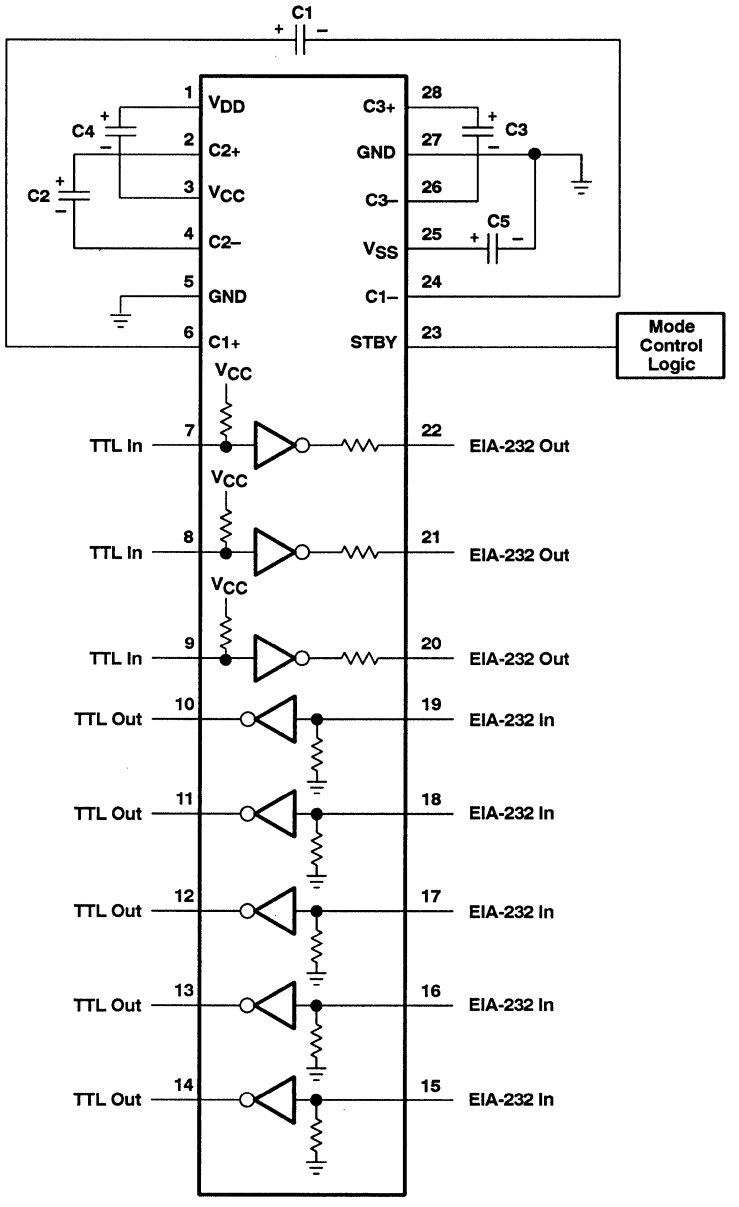
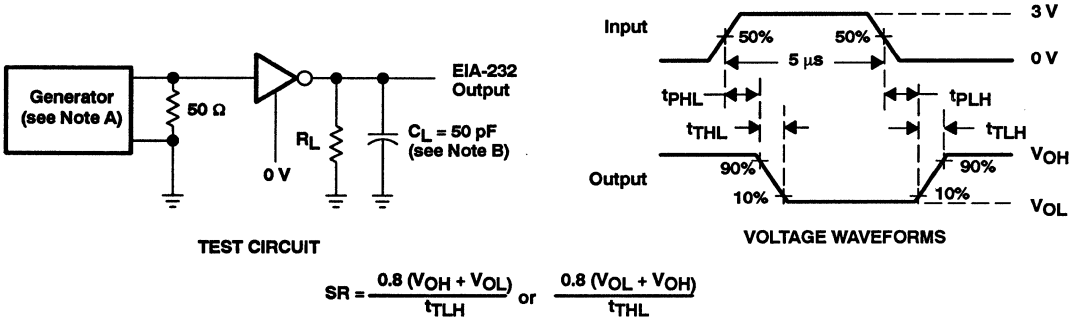


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION



$$SR = \frac{0.8\,(V_{OH} + V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\,(V_{OL} + V_{OH})}{t_{THL}}$$

Figure 2. Driver Test Circuit and Voltage Waveforms, Slew Rate at 5-μs Input

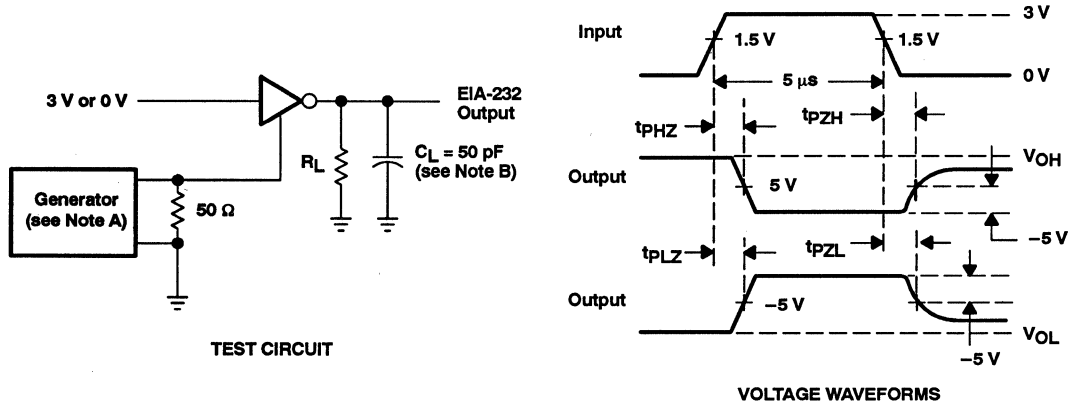
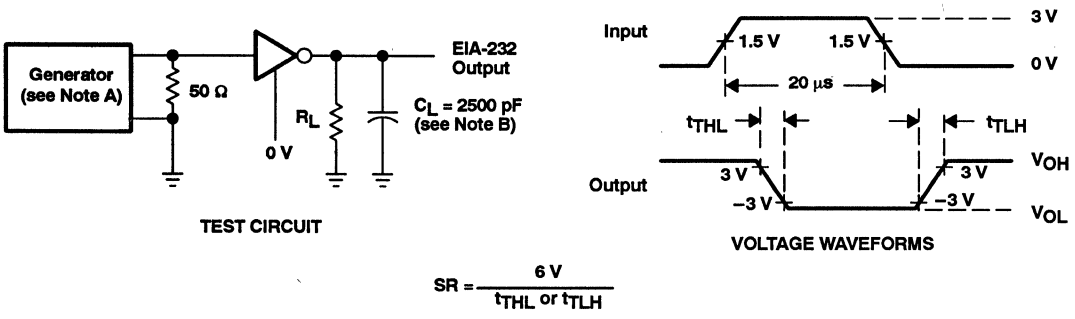


Figure 3. Driver Test Circuit and Voltage Waveforms



$$SR = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

Figure 4. Driver Test Circuit and Voltage Waveforms, Slew Rate at 20-μs Input

NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

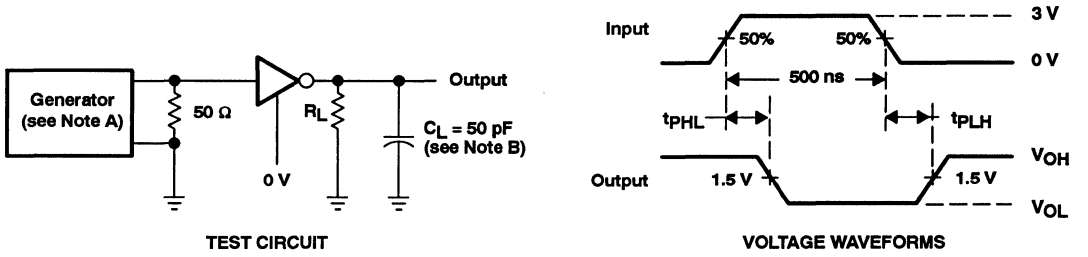


Figure 5. Receiver Test Circuit and Voltage Waveforms

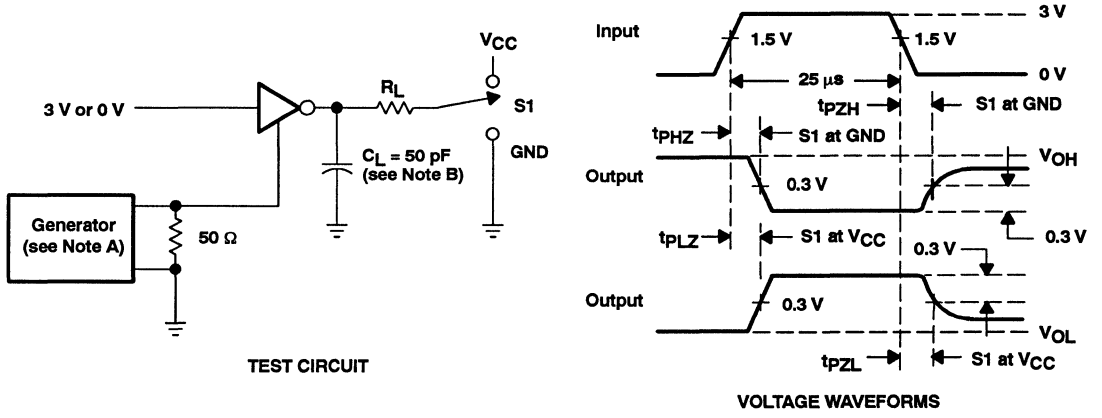


Figure 6. Receiver Test Circuit and Voltage Waveforms Enable and Disable Times

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

SLLS044B – D3408, NOVEMBER 1988 – REVISED FEBRUARY 1993

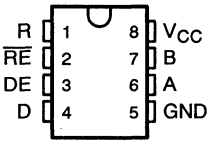
- **Bidirectional Transceiver**
- **Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation in Both Serial and Parallel Applications**
- **Low Skew . . . 6 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 120 mV Typ**
- **Fail Safe . . . High Receiver Output With Inputs Open**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Interchangeable With National DS3695**

description

The TL3695 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The TL3695 combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a directional control. The driver differential outputs and the receiver differential inputs are connected

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

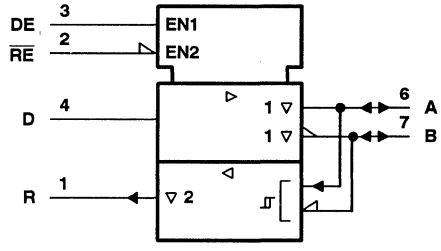
INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs Open	L	H

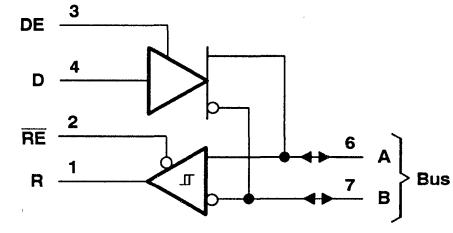
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

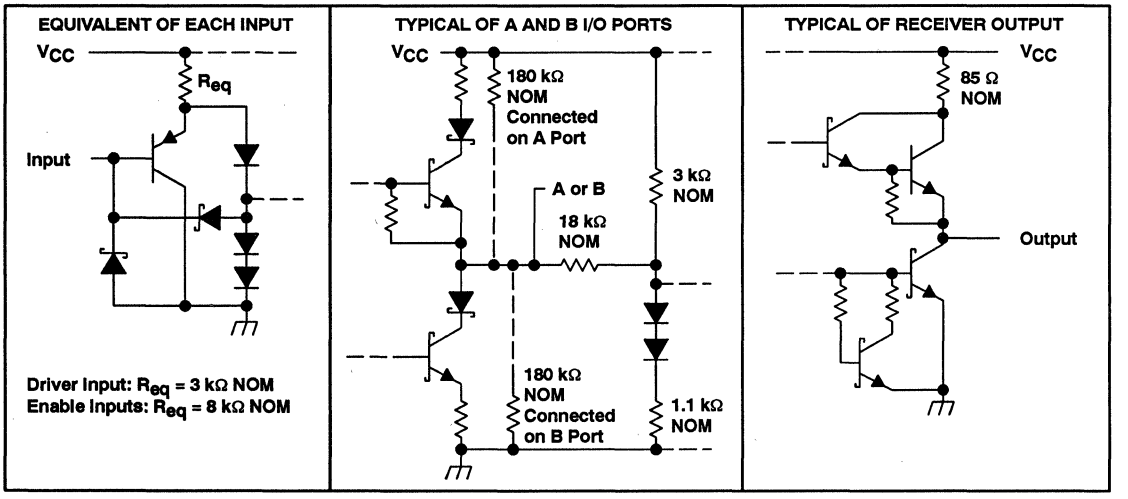


description (continued)

internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level Input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level Input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		5	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2V_{OD1} or 2¶			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V, See Figure 2		1.5		5	V
Δ $\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
Δ $\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	µA
I_{OS}	Short-circuit output current	V_O = −6 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Δ $|V_{OD}|$ and Δ $|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V whichever is greater.
NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{dD}	Differential-output delay time	$C_{L1} = C_{L2} = 100$ pF,	$R_L = 60\ \Omega$,	See Figure 3		8	22	ns
	Skew ($\lvert t_{dDH} - t_{dDL} \rvert$)					1	8	ns
t_{tD}	Differential output transition time					8	18	ns
t_{PZH}	Output enable time to high level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 4			50	ns
t_{PZL}	Output enable time to low level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 5			50	ns
t_{PHZ}	Output disable time from high level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 4		8	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 5		8	30	ns

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{T-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis (V_{T+}−V_{T-})	V_{OC} = 0			70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV or inputs open, I_{OH} = −400 μA, See Figure 6		2.4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 16 mA			0.5	V
			I_{OL} = 8 mA			0.45	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_O = 0		−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 7		14	37	ns
t_{PHL}	Propagation delay time, high-to-low-level output			14	37	ns
t_{PZH}	Output enable time to high level	See Figure 8		7	20	ns
t_{PZL}	Output enable time to low level			7	20	ns
t_{PHZ}	Output disable time from high level	See Figure 8		7	16	ns
t_{PLZ}	Output disable time from low level			8	16	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

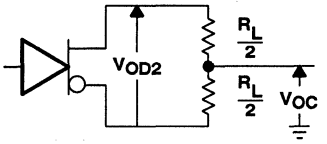


Figure 1. Driver V_{OD} and V_{OC}

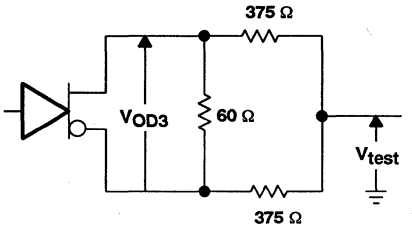
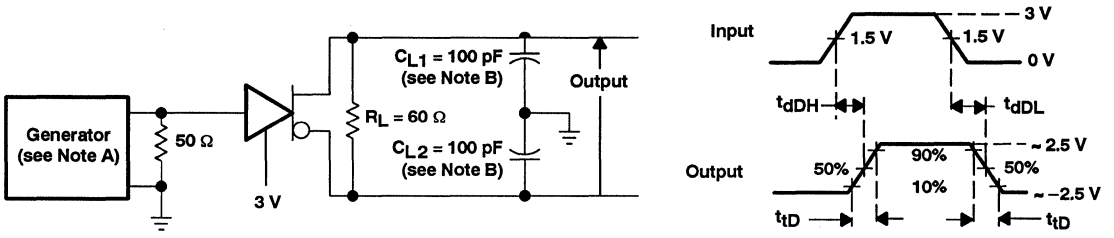
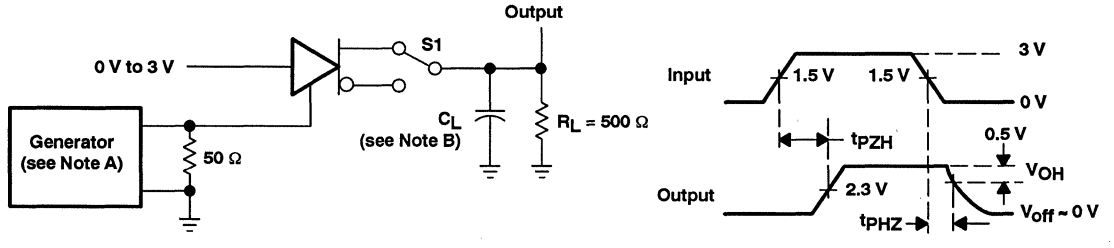


Figure 2. Driver V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

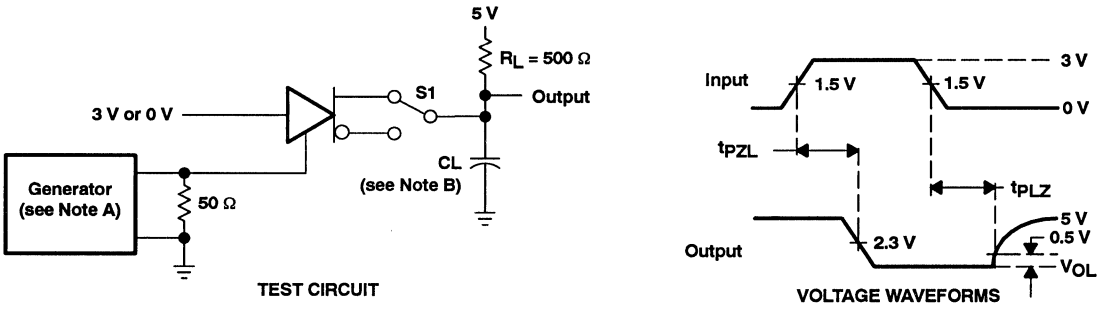
Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance (see switching characteristics – test conditions).

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω..
B. C_L includes probe and jig capacitance (see switching characteristics – test conditions).

Figure 5. Driver Test Circuit and Voltage Waveforms

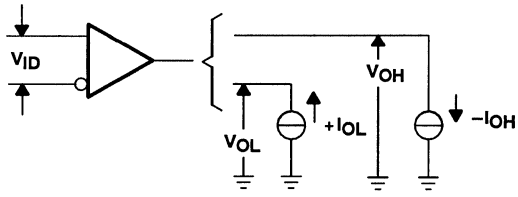
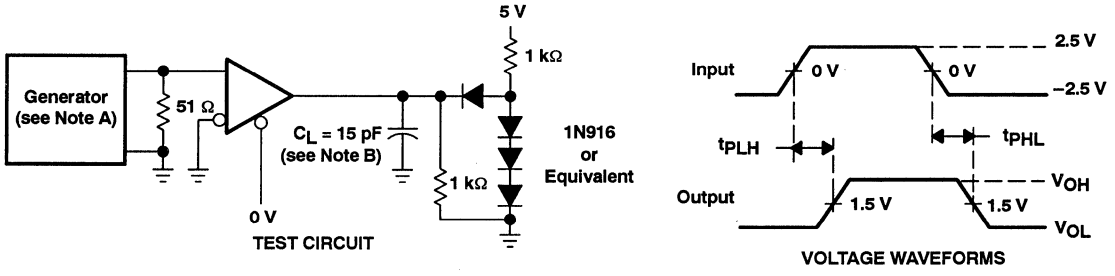


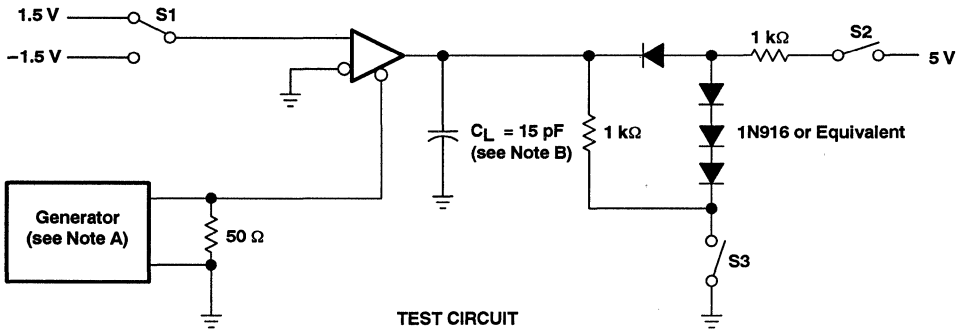
Figure 6. Receiver V_{OH} and V_{OL}



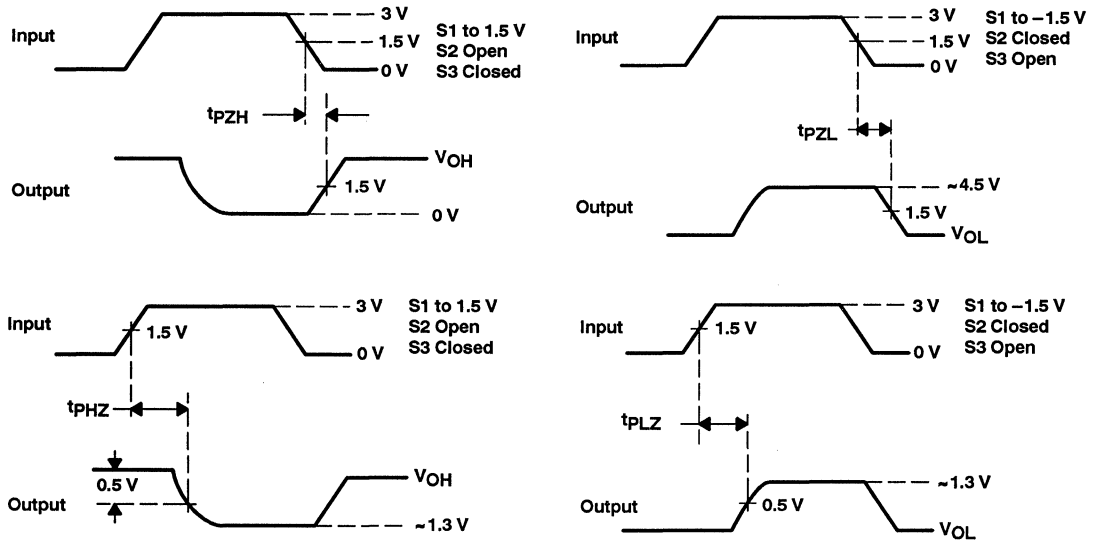
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
DRIVER HIGH-LEVEL OUTPUT CURRENT

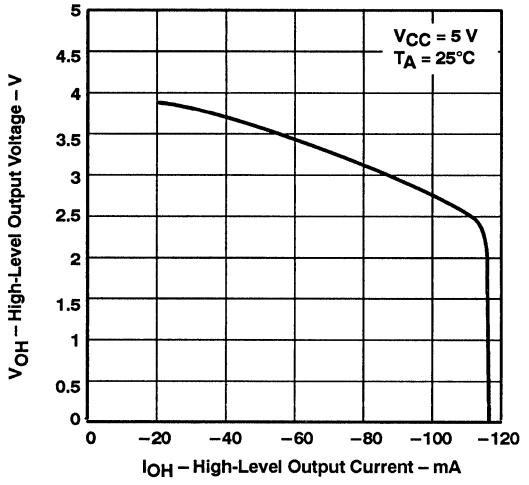


Figure 9

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
DRIVER LOW-LEVEL OUTPUT CURRENT

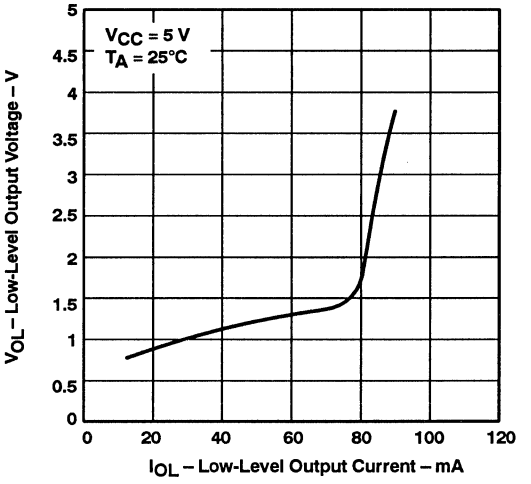


Figure 10

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

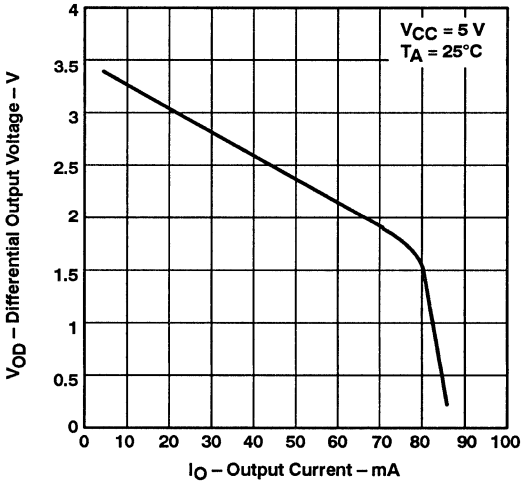


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

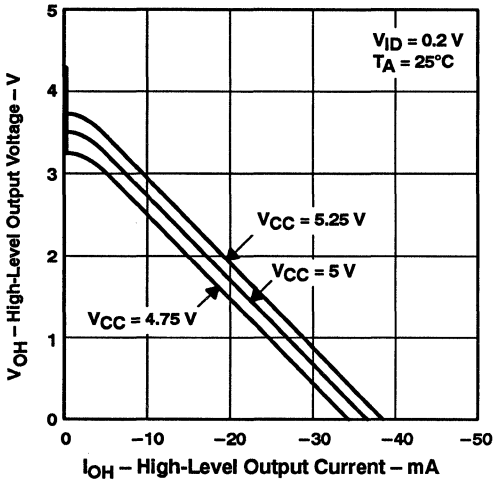


Figure 12

RECEIVER HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

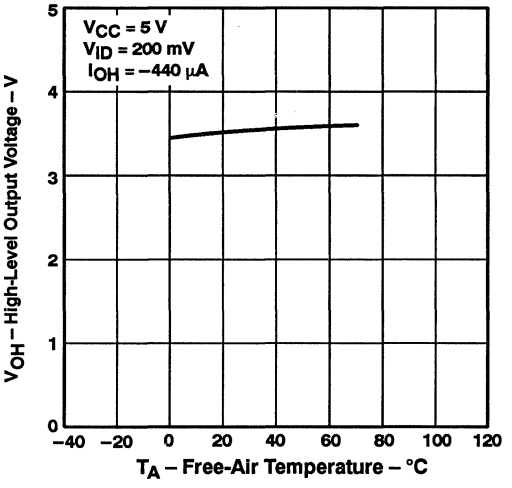


Figure 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

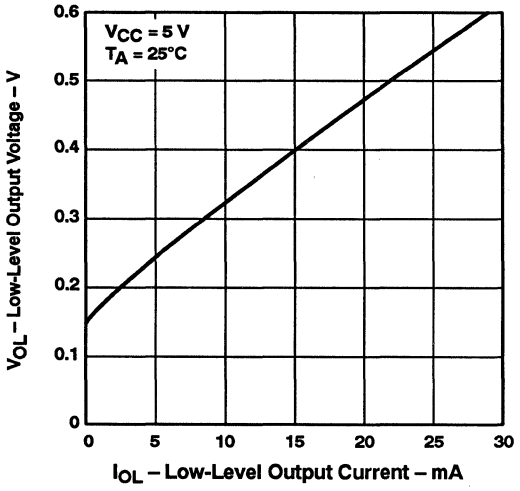


Figure 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

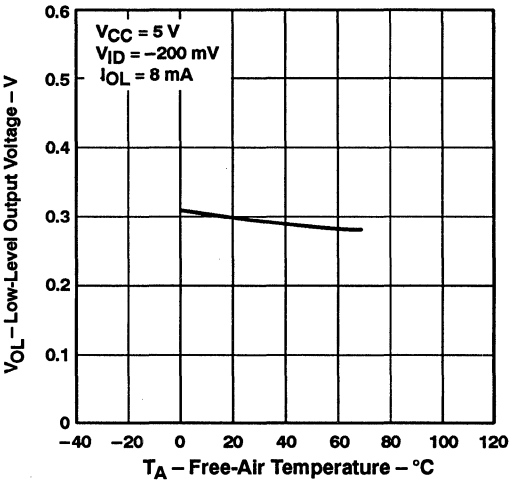


Figure 15

TYPICAL CHARACTERISTICS

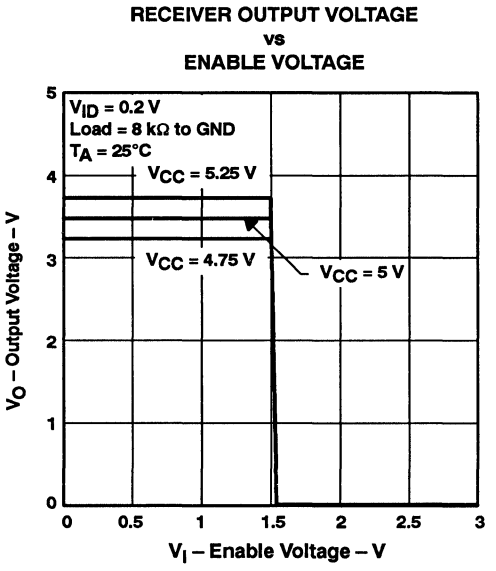


Figure 16

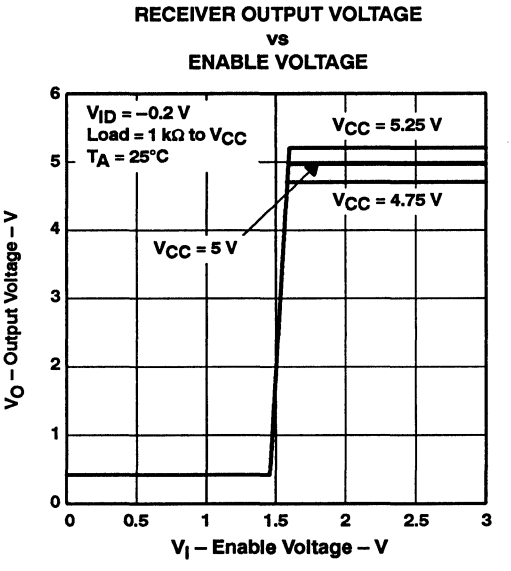
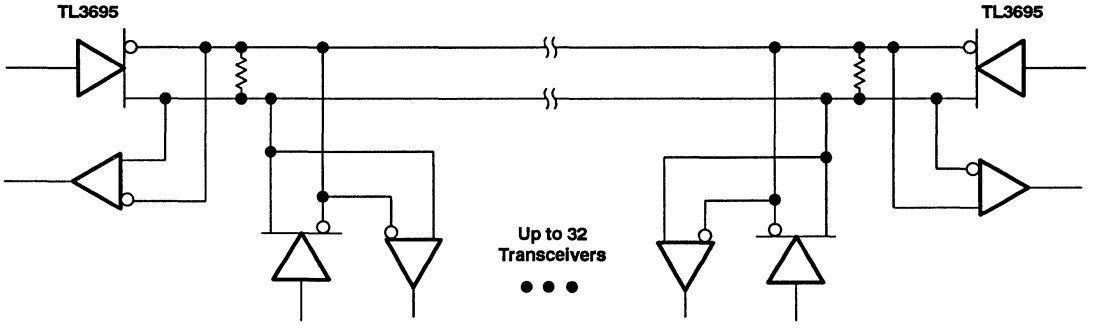


Figure 17

APPLICATION INFORMATION



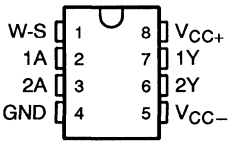
NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

SLLS110A – D2608, OCTOBER 1980 – REVISED MARCH 1993

- **Meets EIA Standards RS-423-A and RS-232-C and Federal Standard 1030**
- **Slew Rate Control**
- **Output Short-Circuit-Current Limiting**
- **Wide Supply Voltage Range**
- **8-Pin Package**
- **Designed to Be Interchangeable With Fairchild 9636A**

D OR P PACKAGE
(TOP VIEW)

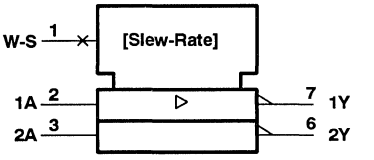


description

The uA9636AC is a dual single-ended line driver designed to meet EIA Standards RS-423-A and RS-232-C and Federal Standard 1030. The slew rates of both amplifiers are controlled by a single external resistor, R_{WS}, connected between the wave-shape-control (W-S) terminal and GND. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode protected against negative transients. This device operates from ±12 V and is supplied in an 8-pin package.

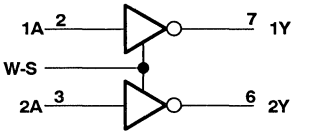
The uA9636AC is characterized for operation from 0°C to 70°C.

logic symbol†



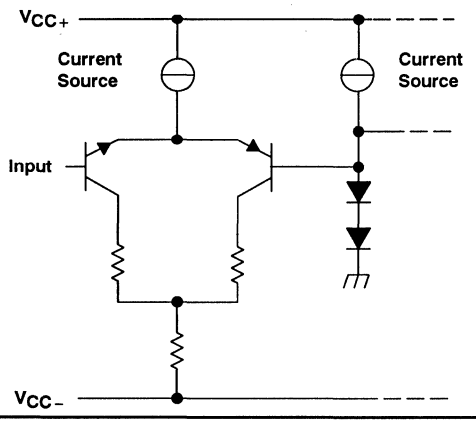
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

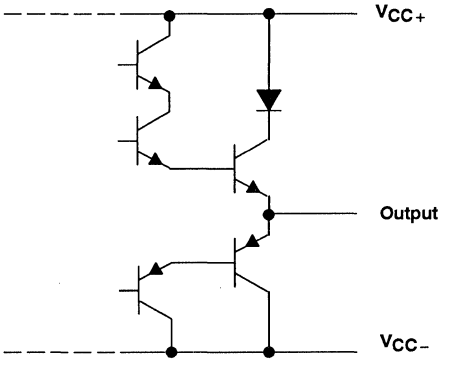


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage range, V_{CC+} (see Note 1) ..... V_{CC-} to 15 V
Negative supply voltage range, V_{CC-} ..... 0.5 V to −15 V
Output voltage ..... ±15 V
Output current ..... ±150 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Wave-shaping resistor, R_{WS}	10		1000	kΩ
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

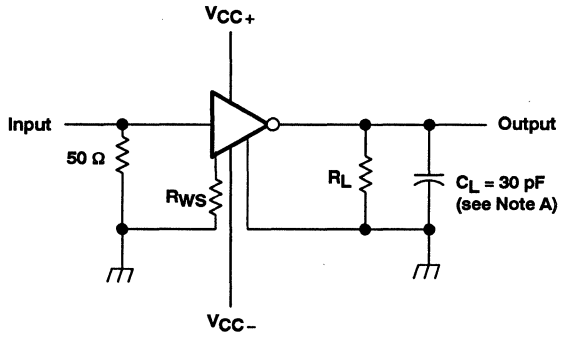
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -15$ mA			−1.1	−1.5	V
V_{OH}	High-level output voltage	$V_I = 0.8$ V	$R_L = \infty$	5	5.6	6	V
			$R_L = 3$ kΩ to GND	5	5.6	6	
			$R_L = 450$ Ω to GND	4	5.4	6	
V_{OL}	Low-level output voltage	$V_I = 2$ V	$R_L = \infty$	−6‡	−5.7	−5	V
			$R_L = 3$ kΩ to GND	−6‡	−5.6	−5	
			$R_L = 450$ Ω to GND	−6‡	−5.4	−4	
I_{IH}	High-level input current	$V_I = 2.4$ V				10	μA
		$V_I = 5.5$ V				100	
I_{IL}	Low-level input current	$V_I = 0.4$ V			−20	−80	μA
I_O	Output current (power off)	$V_{CC\pm} = 0$,	$V_O = \pm 6$ V			±100	μA
I_{OS}	Short-circuit output current§	$V_I = 2$ V		15	25	150	mA
		$V_I = 0$		−15	−40	−150	
r_o	Output resistance	$R_L = 450$ Ω			25	50	Ω
I_{CC+}	Positive supply current	$V_{CC} = \pm 12$ V, $R_{WS} = 100$ kΩ,	$V_I = 0$, Output open		13	18	mA
I_{CC-}	Negative supply current	$V_{CC} = \pm 12$ V, $R_{WS} = 100$ kΩ,	$V_I = 0$, Output open		−13	−18	mA

† All typical values are at $V_{CC} = \pm 12$ V, $T_A = 25°C$.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when −5 V is the maximum, the minimum is a more-negative voltage.
§ Not more than one output should be shorted to ground at a time.

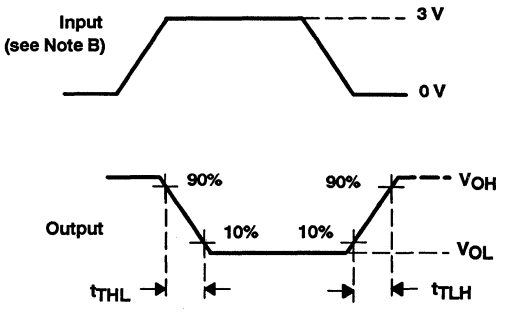
switching characteristics, $V_{CC\pm} = \pm 12$ V, $T_A = 25°C$ (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	$R_L = 450$ kΩ, $C_L = 30$ pF	$R_{WS} = 10$ kΩ	0.8	1.1	1.4	μs
			$R_{WS} = 100$ kΩ	8	11	14	
			$R_{WS} = 500$ kΩ	40	55	70	
			$R_{WS} = 1$ MΩ	80	110	140	
t_{THL}	Transition time, high-to-low-level output	$R_L = 450$ kΩ, $C_L = 30$ pF	$R_{WS} = 10$ kΩ	0.8	1.1	1.4	μs
			$R_{WS} = 100$ kΩ	8	11	14	
			$R_{WS} = 500$ kΩ	40	55	70	
			$R_{WS} = 1$ MΩ	80	110	140	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$, PRR ≤ 1 kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

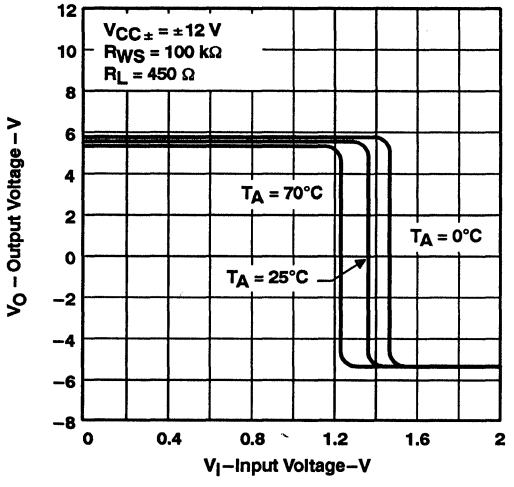


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE

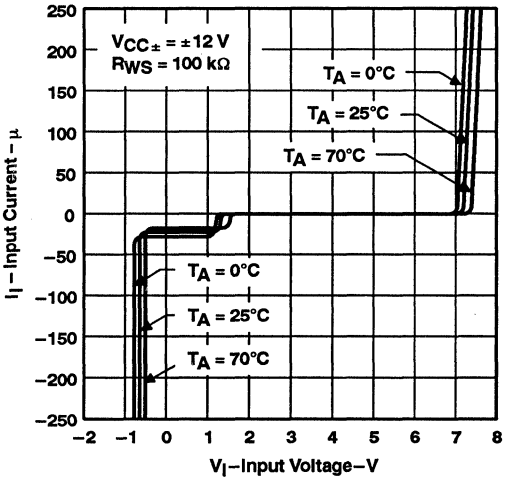


Figure 3

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE
(POWER ON)

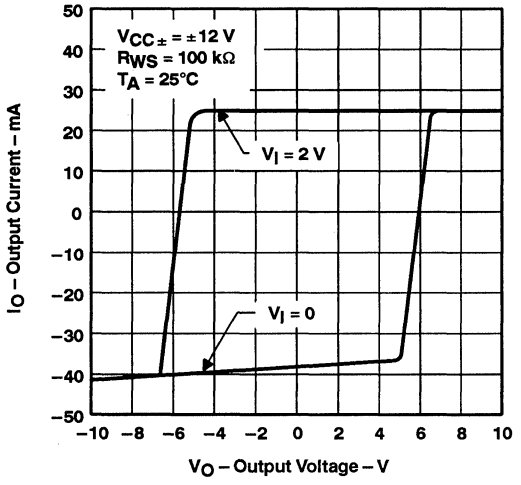


Figure 4

OUTPUT CURRENT
vs
OUTPUT VOLTAGE
(POWER OFF)

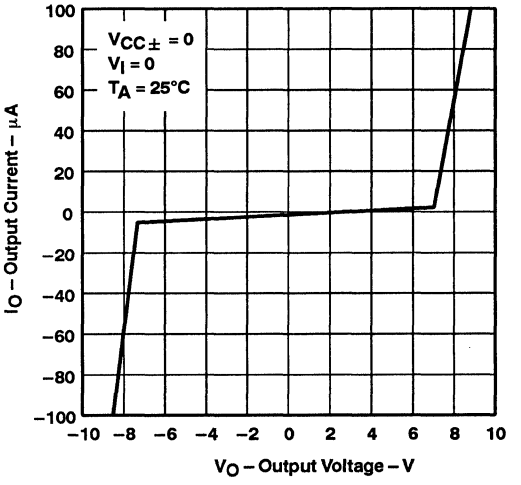


Figure 5

TRANSITION TIMES
vs
WAVE-SHAPING RESISTANCE

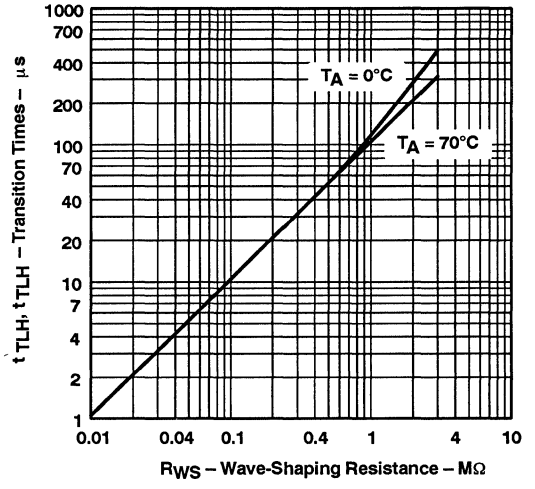


Figure 6

APPLICATION INFORMATION

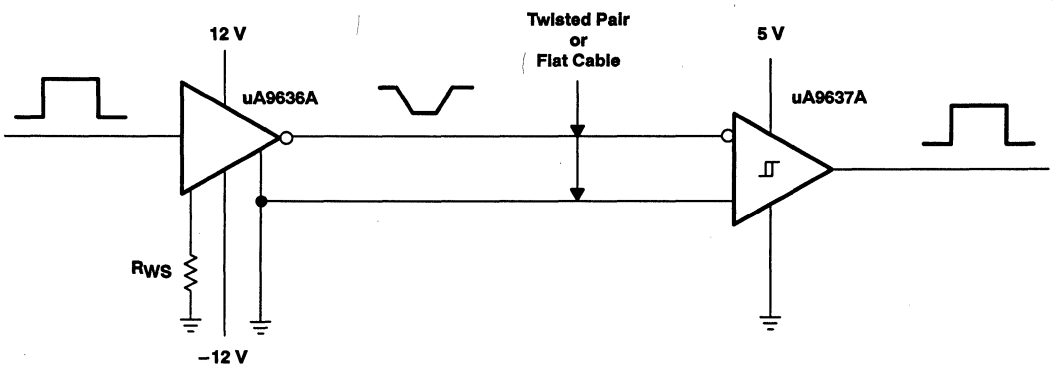
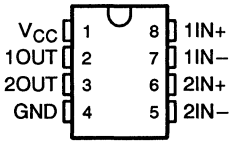


Figure 7. RS-423-A System Application

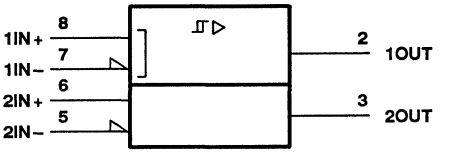
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets Federal Standards 1020 and 1030**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line and Small-Outline Packages**
- **Similar to SN75157 Except for Corner V_{CC} and Ground Pin Positions**
- **Designed to Be Interchangeable With Fairchild μA9637A**

uA9637C . . . D OR P PACKAGE
(TOP VIEW)

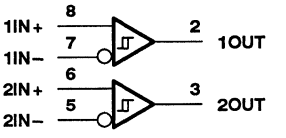


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



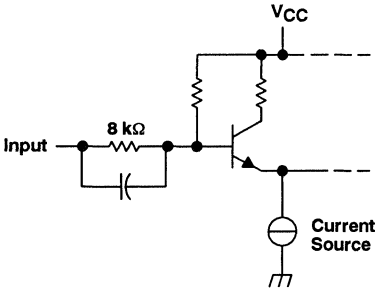
description

The uA9637AC is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. They utilize Schottky circuitry and have TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin dual-in-line package and small-outline package.

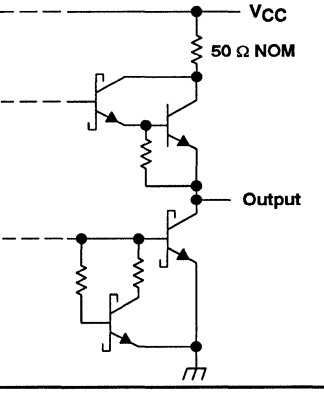
The uA9637AC is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Output voltage, V_O (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

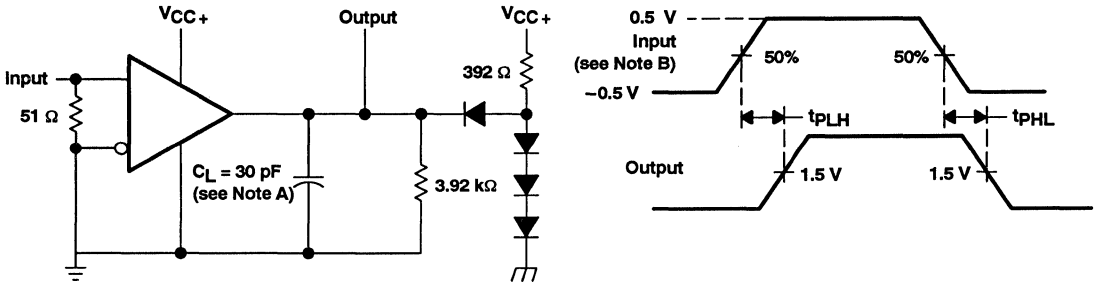
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	See Note 4				0.2	V
						0.4	
V_{T-}	Negative-going input threshold voltage	See Note 4		−0.2			V
				−0.4‡			
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 5	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

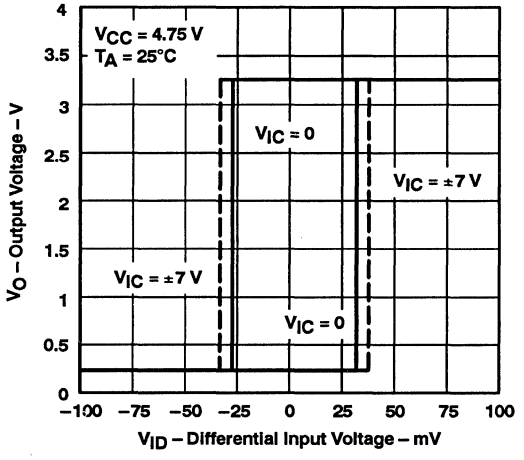


Figure 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

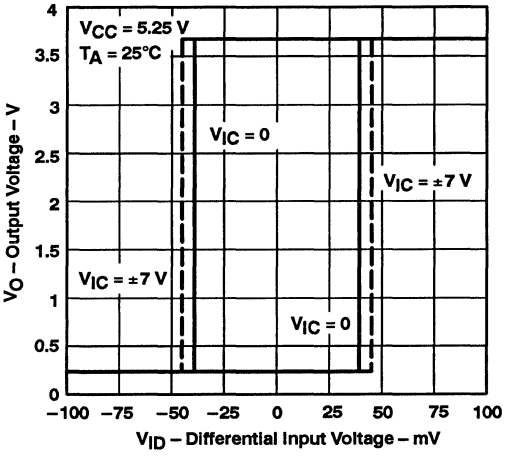


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

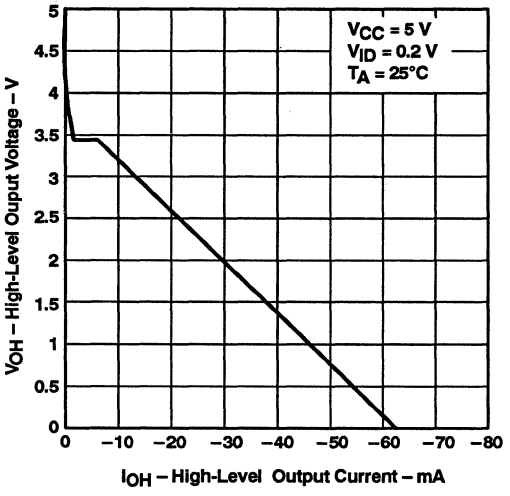


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

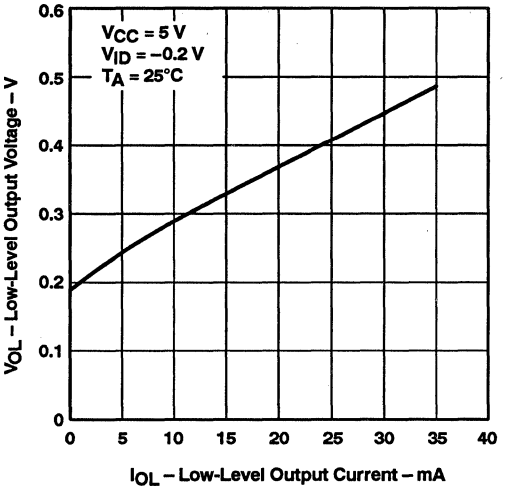


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

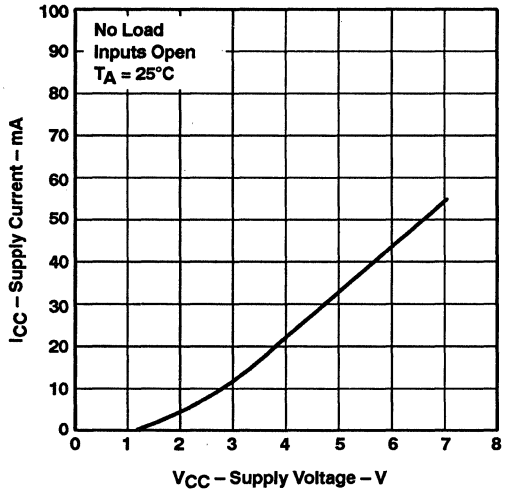


Figure 6

APPLICATION INFORMATION

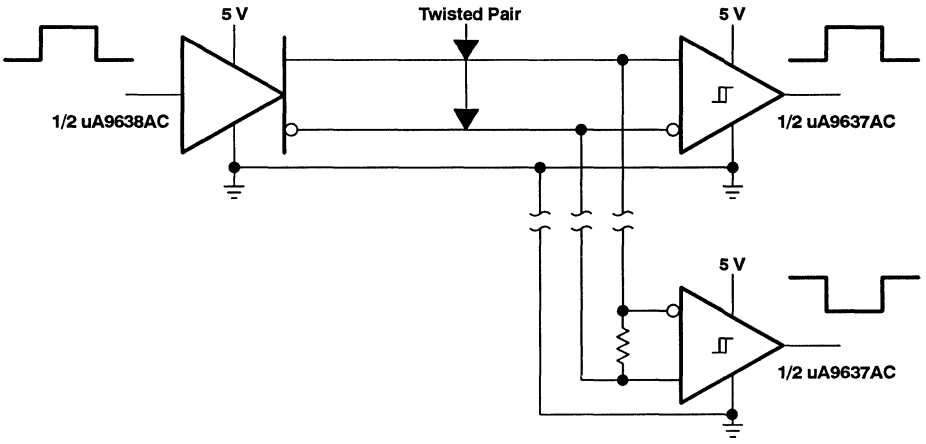


Figure 7. RS-A System Applications

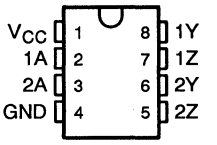
- **Meets EIA Standard RS-422-A**
- **Operates From a Single 5-V Supply**
- **TTL-and CMOS-Input Compatibility**
- **Output Short-Circuit Protection**
- **Schottky Circuitry**
- **Designed to Be Interchangeable With Fairchild 9638**

description

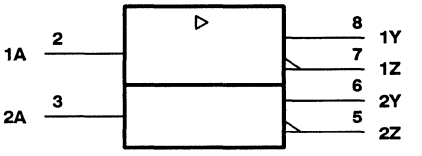
The uA9638C is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

The uA9638C is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
(TOP VIEW)

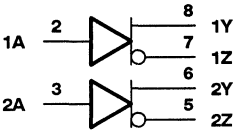


logic symbol†



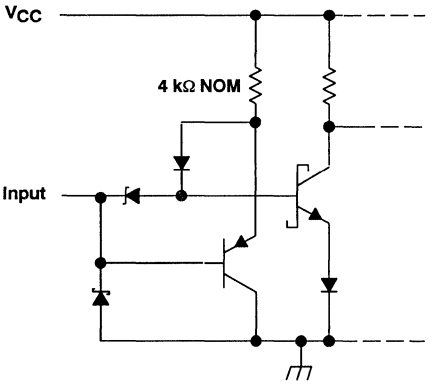
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

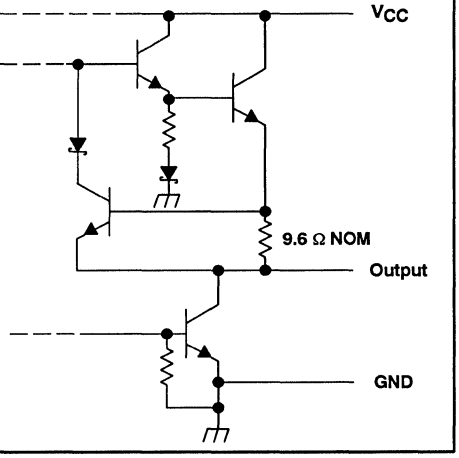


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from 10 seconds ..... 260°C

NOTE 1: Voltage values except differential output voltages are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA			−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 0.2 V, I_{OL} = 40 mA	V_{IL} = 0.8 V,			0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = 5.25 V, I_O = 0				$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, See Figure 1	R_L = 100 Ω,	2			V
$\Delta\|V_{OD}\|$	Change in magnitude of diferential output voltage‡					±0.4	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	μA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0		−50		−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, No load,	All inputs at 0 V		45	65	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		10	15	ns
t_{tD}	Differential-output transition time			10	15	ns
	Skew	See Figure 2		1		ns

PARAMETER MEASUREMENT INFORMATION

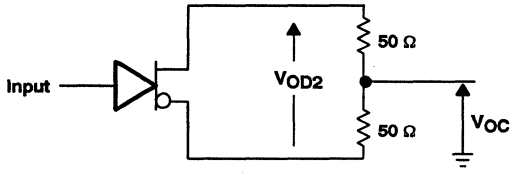
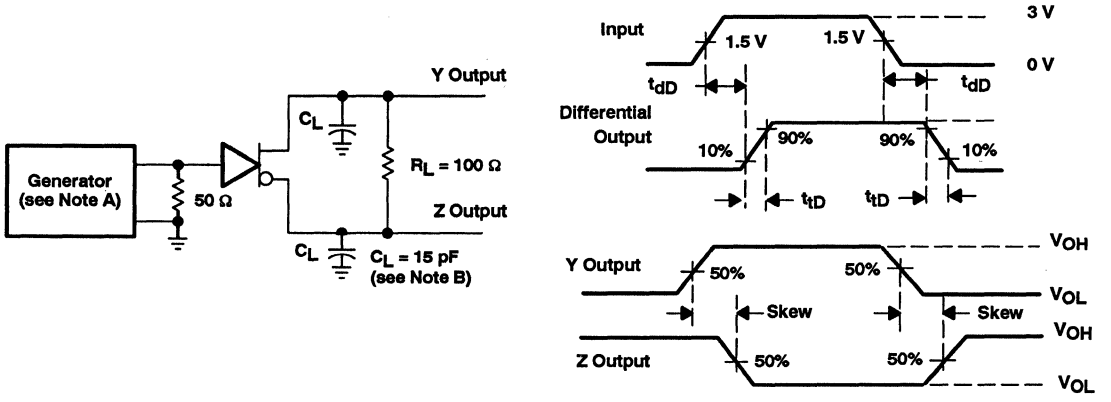


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT VOLTAGE WAVEFORMS

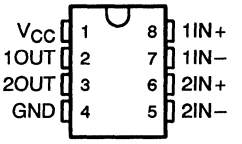
NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

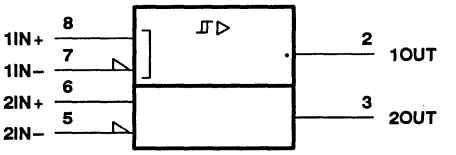
SLLS113A – D3009, OCTOBER 1986 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A and RS-423-A**
- **Meets Federal Standards 1020 and 1030**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line and Small-Outline Packages**
- **Designed to Be Interchangeable With Fairchild μA9639AC**

D OR P PACKAGE
(TOP VIEW)

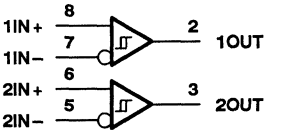


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



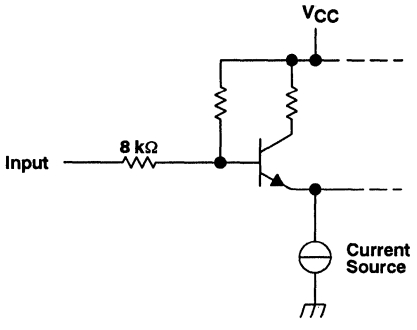
description

The uA9639C is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin dual-in-line package and small-outline package.

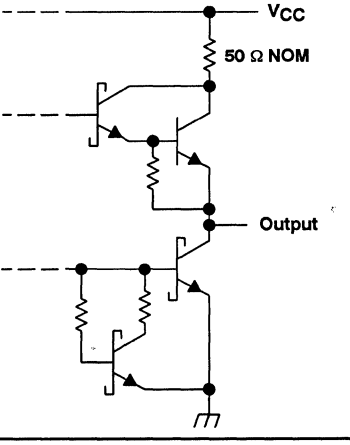
The uA9639C is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Output voltage range (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current ..... 50 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

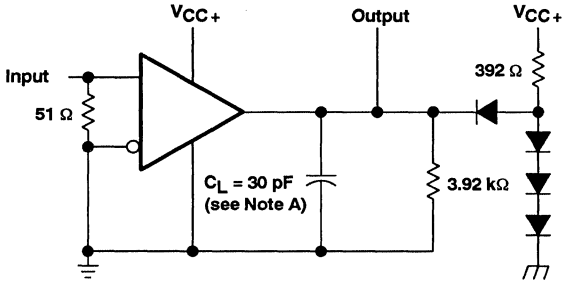
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	See Note 3				0.2	V
						0.4	
V_{T-}	Negative-going input threshold voltage	See Note 3		−0.2			V
				−0.4‡			
V_{hys}	Hysteresis ($V_{T+}-V_{T-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 5	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. The input not under test is grounded.

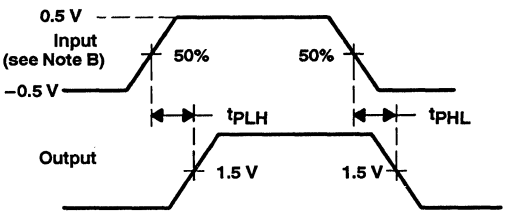
switching characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Figure 1		85	ns
t_{PHL}	Propagation delay time, high-to-low-level output			85	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

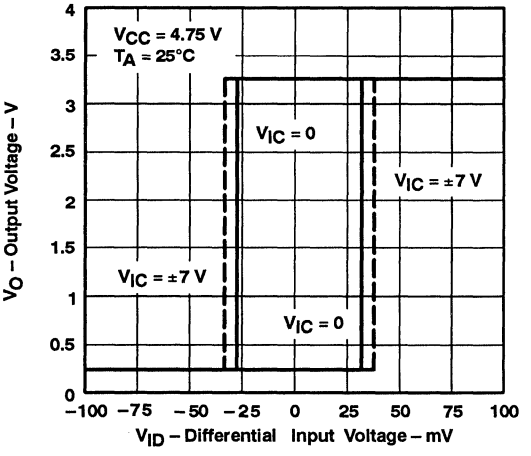


Figure 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

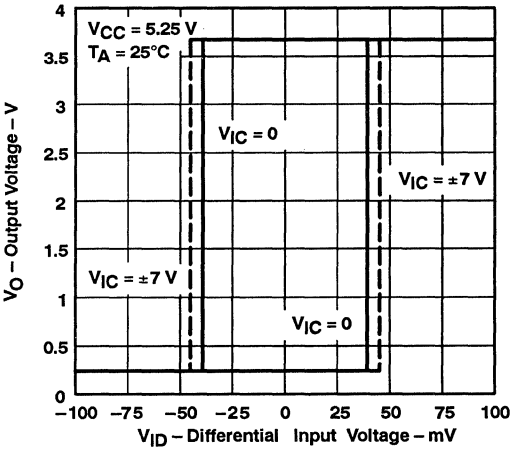


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

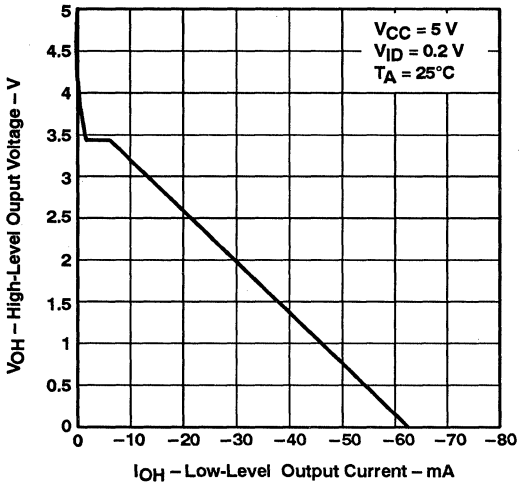


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

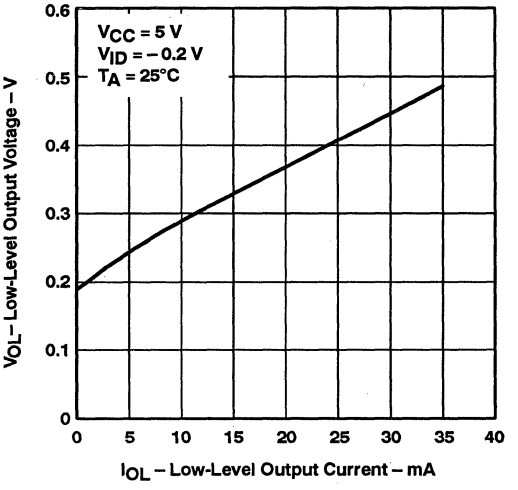


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

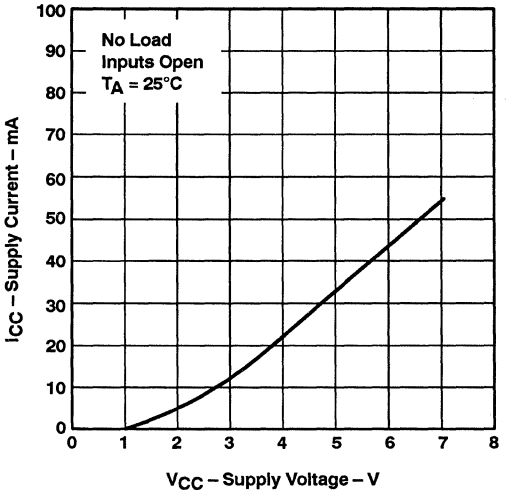


Figure 6

APPLICATION INFORMATION

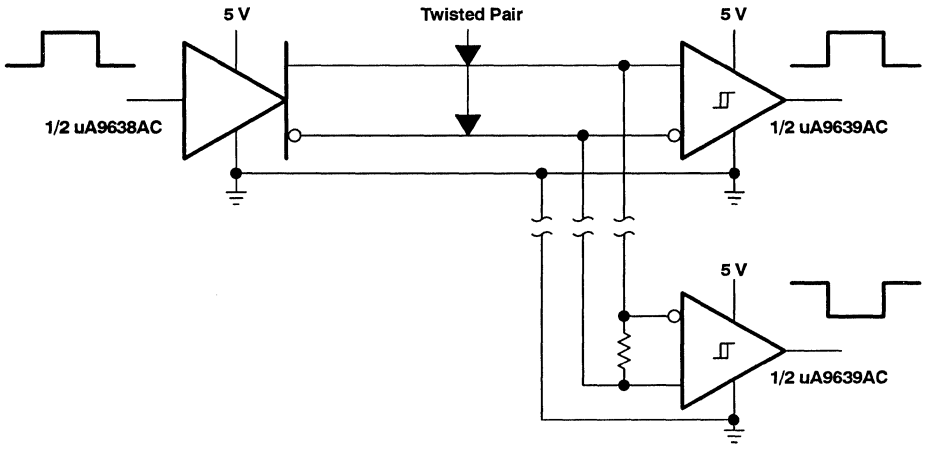


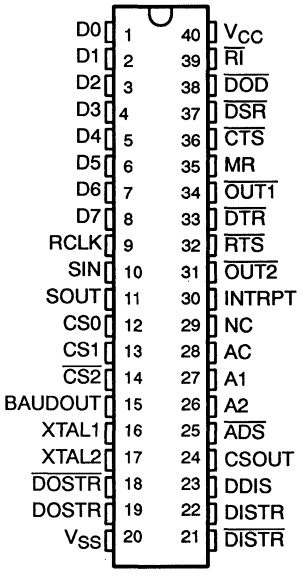
Figure 7. RS-422-A System Applications

Universal Async Receivers/Transmitters

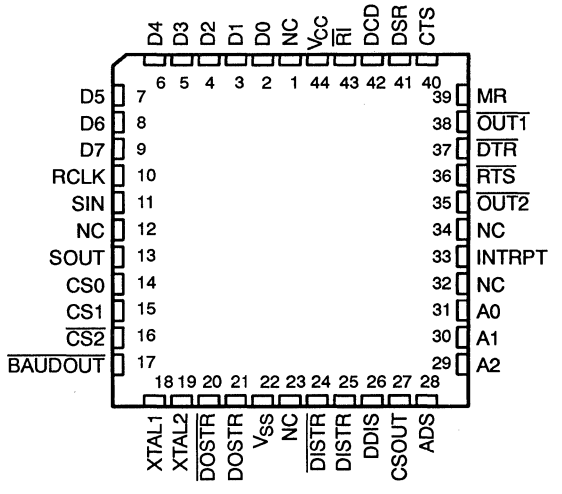
SLLS037A – D3096, MARCH 1988 – REVISED APRIL 1989

- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16 X Clock**
- **Full Double Buffering Eliminates the Need for Precise Synchronization**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (dc to 256 kb/s Per Second)**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully-Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)**
- **Easily Interfaces to Most Popular Microprocessors**
- **Faster Plug-In Replacement for National Semiconductor NS16C450**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL16C450 is a CMOS version of an asynchronous communications element (ACE). It typically functions in a microcomputer system as a serial input/output interface.

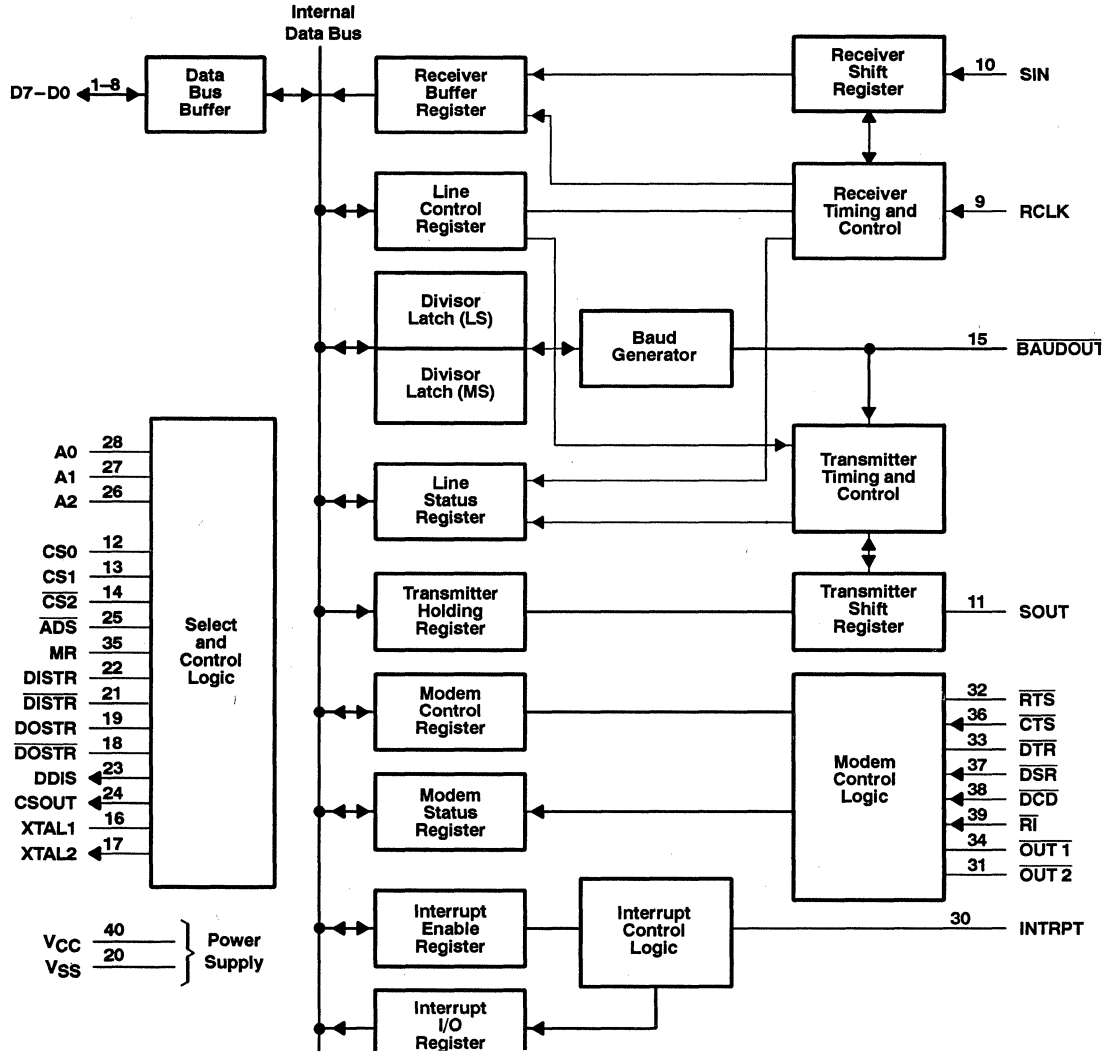
The TL16C450 performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the

description (continued)

ACE at any point in the ACE's operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C450 ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to ($2^{16}-1$) and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

block diagram



Pin numbers shown are for the N package.

Terminal Functions

PIN NAME	PIN NO.†	I/O	DESCRIPTION
A0 A1 A2	28 27 26	I	Register select. Three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDO}$ $\overline{UT}$	15	O	Baud out. 16 X clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 13 14	I	Chip select. When active (high and low, respectively), these three inputs select the ACE. Refer to the $\overline{ADS}$ signal description.
CSOUT	24	O	Chip select out. When CSOUT is high, it indicates that the ACE has been selected by the chip select inputs (CS0, CS1, and $\overline{CS2}$). CSOUT is low when the chip is deselected.
$\overline{CTS}$	36	I	Clear to send. $\overline{CTS}$ is a modem status signal whose condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 D1 D2 D3 D4 D5 D6 D7	1 2 3 4 5 6 7 8	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38	I	Data carrier detect. $\overline{DCD}$ is a modem status signal whose condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23	O	Driver disable. This output is active (high) when the CPU is not reading data. When active, this output can be used to disable an external transceiver.
DISTR $\overline{DISTR}$	22 21	I	Data input strobes. When either input is active (high or low, respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., DISTR tied low or $\overline{DISTR}$ tied high).
DOSTR $\overline{DOSTR}$	19 18	I	Data output strobes. When either input is active (high or low, respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., DOSTR tied low or $\overline{DOSTR}$ tied high).
$\overline{DSR}$	37	I	Data set ready. $\overline{DSR}$ is a modem status signal whose condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or resetting bit 0 (DTR) of the modem control register.

† Pin numbers shown are for the N package.

Terminal Functions (continued)

PIN NAME	PIN NO.†	I/O	DESCRIPTION
INTRPT	30	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTRPT output is reset (inactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{OUT1}$ $\overline{OUT2}$	34 31	O	Outputs 1 and 2. User-designated output pins that are set to their active states by setting their respective modem control register bits (OUT 1 and OUT 2) high. $\overline{OUT 1}$ and $\overline{OUT 2}$ are set to their inactive (high) states as a result of master reset or during loop mode operations or by resetting bit 2 (OUT 1) or bit 3 (OUT 2) of the MCR.
RCLK	9	I	Receiver clock. The 16 X baud rate clock for the receiver section of the ACE.
$\overline{RI}$	39	I	Ring indicator. $\overline{RI}$ is a modem status signal whose condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32	O	Request to send. When active, informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by resetting bit 1 (RTS) of the MCR.
SIN	10	I	Serial input. Serial data input from a connected communications device.
SOUT	11	O	Serial output. Composite serial data output to a connected communication device. SOUT is set to the marking (logic 1) state as a result of MR.
V_{CC}	40		5-V supply voltage
V_{SS}	20		Supply common
XTAL1 XTAL2	16 17	I/O	External clock. Connects the ACE to the main timing reference (clock or crystal).

† Pin numbers shown are for the N package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Continuous total dissipation at (or below) 70°C free-air temperature: FN package ..... 1100 mW
N package ..... 800 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±10	μA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 V to 5.25 V, Chip selected, write mode, or chip deselected			±20	μA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, DSR, DCD, CTS, and RI at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kb/s			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other pins grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175		ns
t_{w5}	Pulse duration, address strobe low	2,3	15		ns
t_{w6}	Pulse duration, write strobe	2	80		ns
t_{w7}	Pulse duration, read strobe	3	80		ns
t_{wMR}	Pulse duration, master reset		1000		ns
t_{su1}	Setup time, address	2,3	15		ns
t_{su2}	Setup time, chip select	2,3	15		ns
t_{su3}	Setup time, data	2	15		ns
t_{h1}	Hold time, address	2,3	0		ns
t_{h2}	Hold time, chip select	2,3	0		ns
t_{h3}	Hold time, write to chip select	2	20		ns
t_{h4}	Hold time, write to address	2	20		ns
t_{h5}	Hold time, data	2	15		ns
t_{h6}	Hold time, read to chip select	3	20		ns
t_{h7}	Hold time, read to address	3	20		ns
t_{d4}§	Delay time, select to write	2	15		ns
t_{d5}§	Delay time, address to write	2	15		ns
t_{d6}	Delay time, write cycle	2	80		ns
t_{d7}§	Delay time, chip select to read	3	15		ns
t_{d8}§	Delay time, address to read	3	15		ns
t_{d9}	Delay time, read cycle	3	80		ns

§ Only applies when ADS is low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	1	f = 9 MHz maximum	50		ns
t_{d3}	Delay time, select to CS output	2,3	C_L = 100 pF		70	ns
t_{d10}	Delay time, read to data	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, read to floating data	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable	3	C_L = 100 pF		60	ns

baud generator switching requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{\text{BAUDOUT}}$ low	1	f = 6.25 MHz, CLK + 1, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{\text{BAUDOUT}}$ high	1	f = 6.25 MHz, CLK + 1, C_L = 100 pF	80		ns
t_{d1}	Delay time, $\overline{\text{BAUDOUT}}$ low to high	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, $\overline{\text{BAUDOUT}}$ high to low	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	4			100	ns
t_{d13}	Delay time, stop to set interrupt	4		1	1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write THR to transmit start	5		8	24	baudout cycles
t_{d16}	Delay time, stop to interrupt	5		8	8	baudout cycles
t_{d17}	Delay time, write THR to reset interrupt	5	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	5		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	5	C_L = 100 pF		140	ns

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay time, write MCR to output	6	C_L = 100 pF		100	ns
t_{d21}	Delay time, modem input to set interrupt	6	C_L = 100 pF		170	ns
t_{d22}	Delay time, read MSR to reset interrupt	6	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

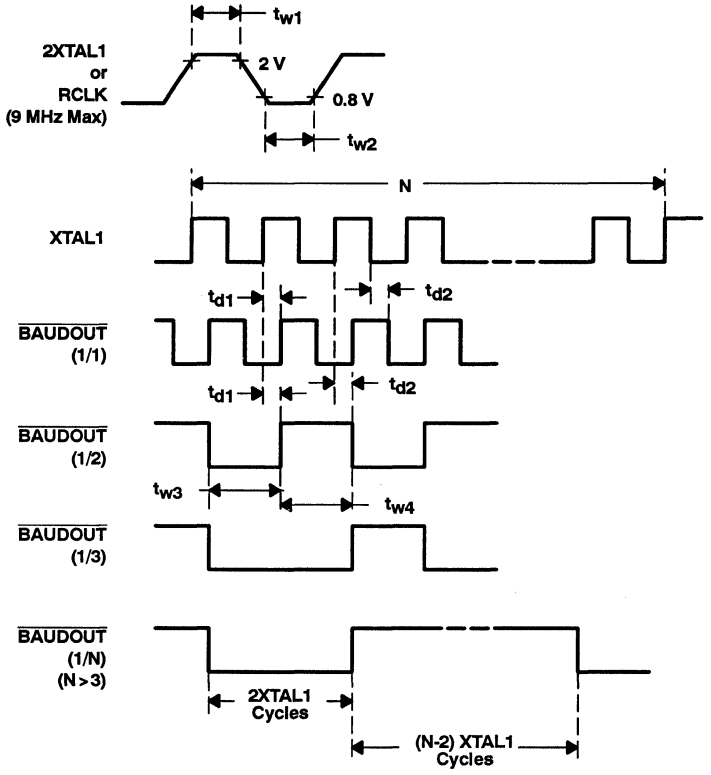
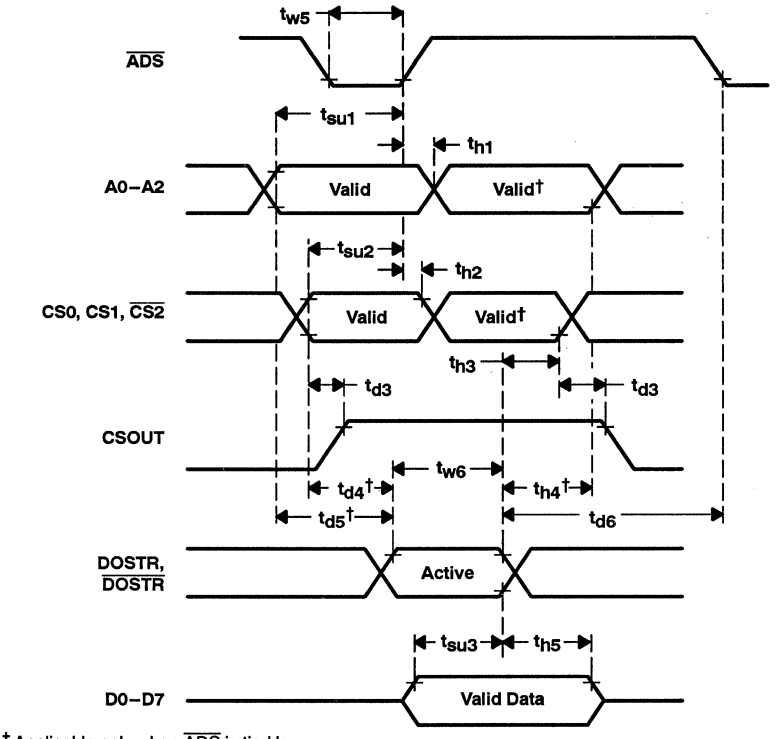


Figure 1. Baud Generator Timing

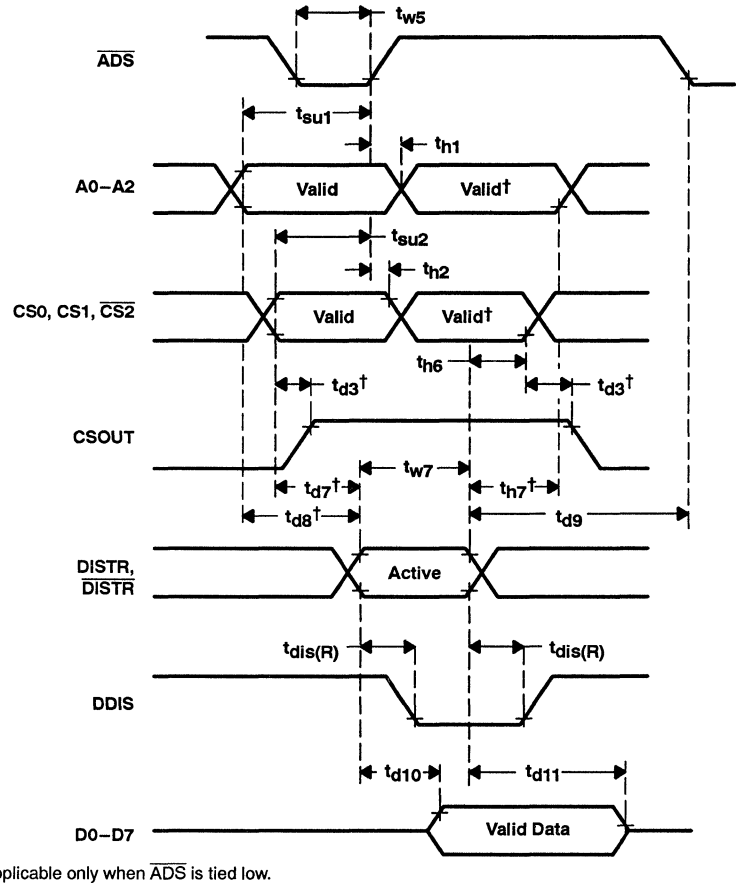
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 2. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

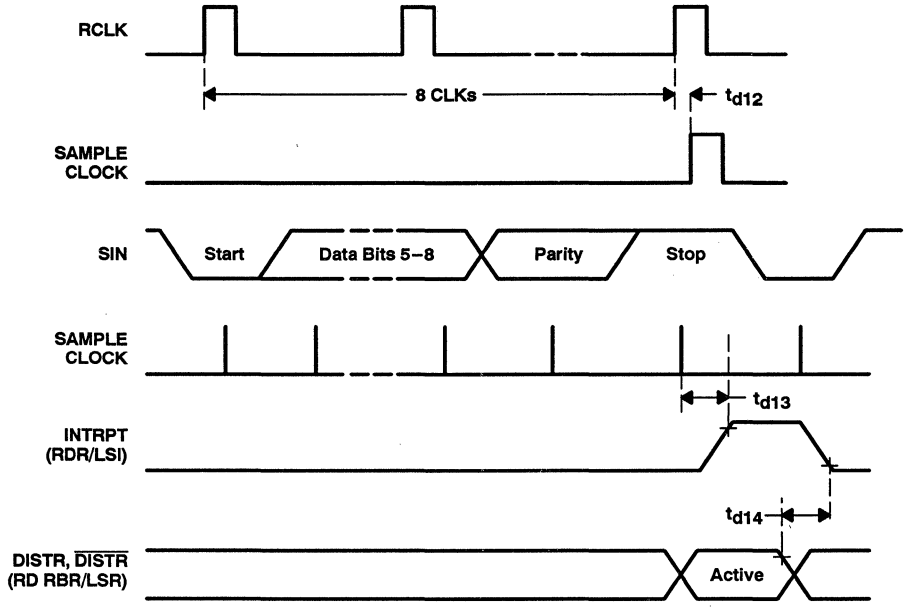


Figure 4. Receiver Timing

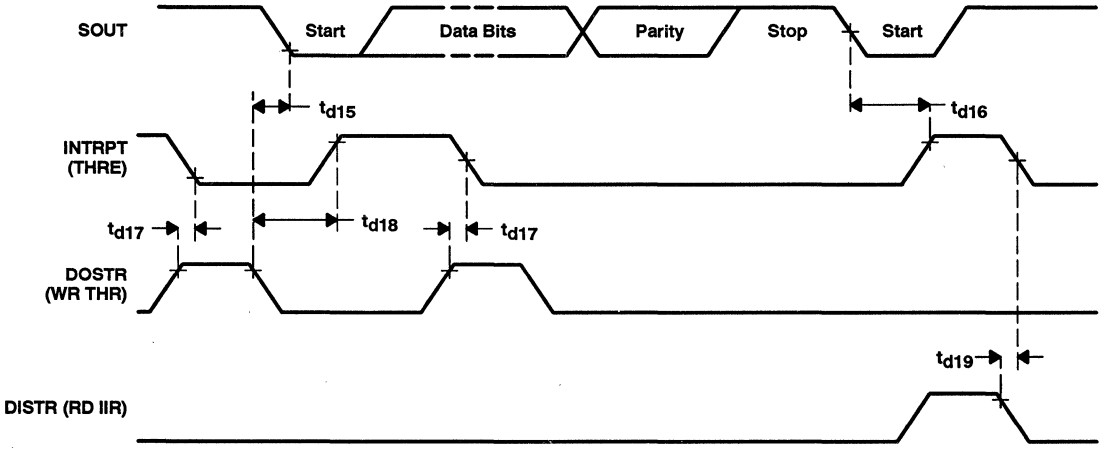


Figure 5. Transmitter Timing

PARAMETER MEASUREMENT INFORMATION

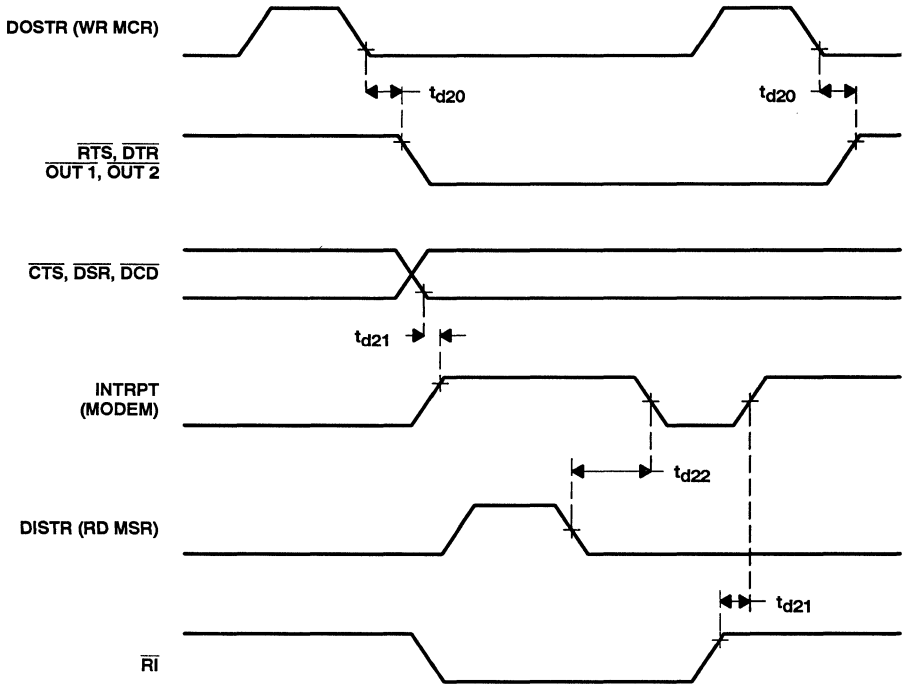


Figure 6. Modem Control Timing

APPLICATION INFORMATION

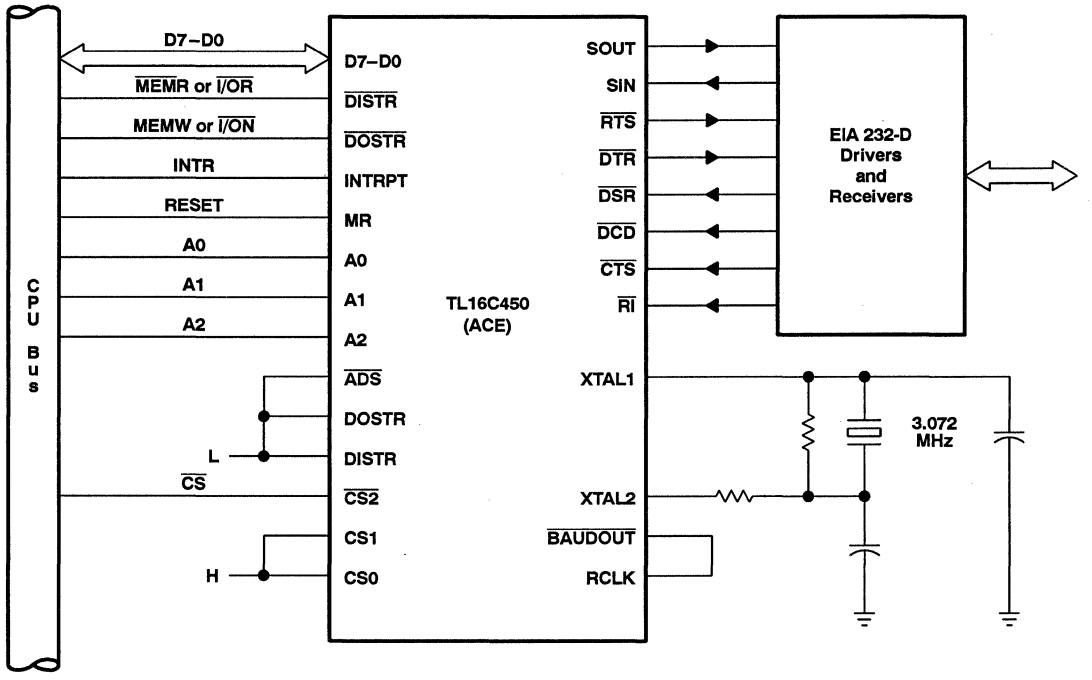


Figure 7. Basic TL16C450 Configuration

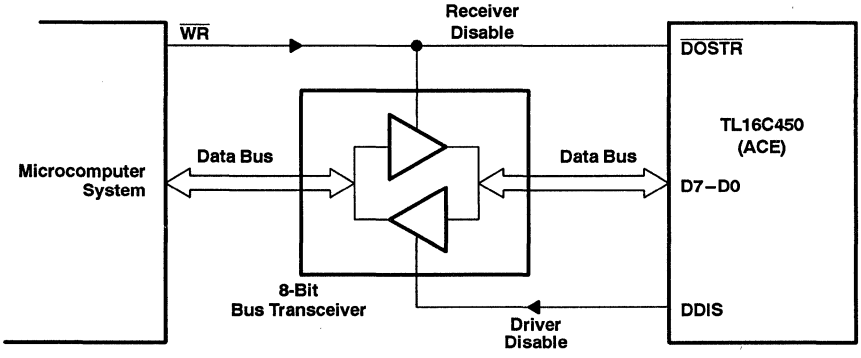


Figure 8. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION

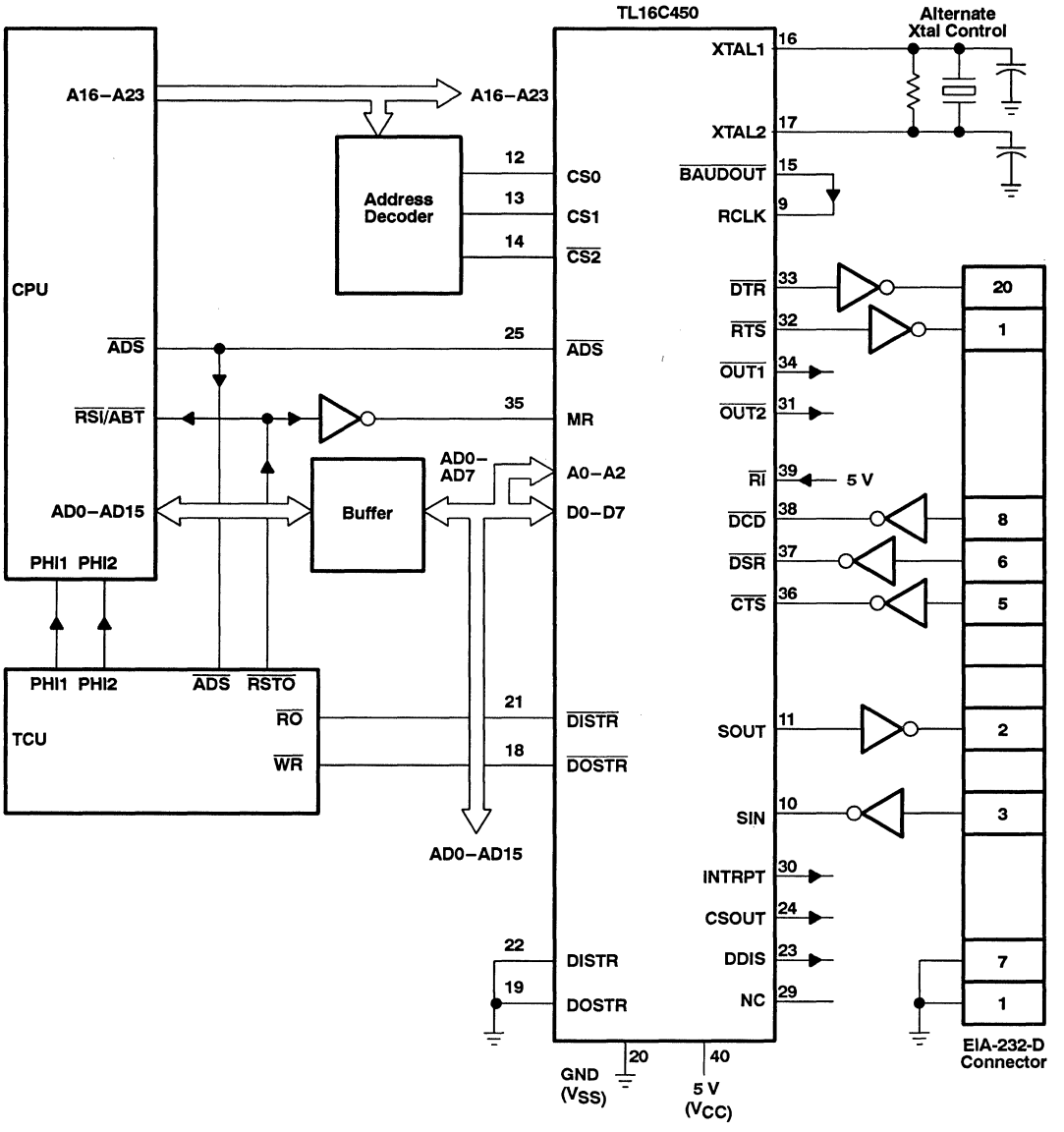


Figure 9. Typical TL16C450 Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high, bits 1 and 2 are low, and bits 3 –7 are permanently low
Line Control Register		All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	Bits 5 and 6 are high, all other bits are low
Modem Status Register	Master Reset	Bits 0–3 are low, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IIR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Register	Master Reset	No effect
Receiver Buffer Register	Master Reset	No effect
Transmitter Holding Register	Master Reset	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS										
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 0
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register IER	Interrupt Ident. Register (Read Only)	Line Control Register LCR	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBF)	"0" If Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBE)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear toSend (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register and a receiver buffer register. Timing is supplied by the 16 X receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE receiver shift register receives serial data from the serial input (SIN) pin. The receiver shift register then converts the data to a parallel form and loads it into the receiver buffer register. When a character is placed in the receiver buffer register and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the receiver buffer register.

transmitter holding register (THR)

The ACE transmitter section consists of a transmitter holding register and a transmitter shift register. Timing is supplied by the Baud Out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE transmitter holding register receives data off the internal data bus and, when the shift register is idle, moves it into the transmitter shift register. The transmitter shift register serializes the data and outputs it at the serial output (SOUT). If the transmitter holding register is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

interrupt enable register (IER)

The interrupt enable register enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

Bit 0. This bit, when set to logic 1, enables the received data available interrupt.

Bit 1. This bit, when set to logic 1, enables the transmitter holding register empty interrupt.

Bit 2. This bit, when set to logic 1, enables the receiver line status interrupt.

Bit 3. This bit, when set to logic 1, enables the modem status interrupt.

Bits 4 thru 7. Bits 4 through 7 in the interrupt enable register are not used and are always set to logic 0.

PRINCIPLES OF OPERATION

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 – Receiver line status (highest priority)
Priority 2 – Receiver data ready
Priority 3 – Transmitter holding register empty
Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

Bit 0. This bit can be used either in a hardwire prioritized or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 thru 7. Bits 3 through 7 in the interrupt identification register are not used and are always set at logic 0.

Table 4. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
1	0	0	2	Received data available	Receiver data available	Reading the receiver buffer Buffer register
0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2. This bit specifies either one, one and one-half, or two stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the data. If bit 2 is a logic 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver checks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in the following.

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

Bit 3. This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

Bit 4. Bit 4 is the even parity select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces even parity (an even number of logic is in the data and parity bits) and a logic 0 in bit 4 produces odd parity (an odd number of logic 1s).

Bit 5. This is the stick parity bit. When bits 3, 4, and 5 are logic 1s, the parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the parity bit is transmitted and checked as a logic 1.

Bit 6. This bit is the break control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the serial output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic, it only effects the serial output.

Bit 7. This bit is the divisor latch access bit (DLAB). Bit 7 must be set to a logic 1 to access the divisor latches of the baud generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

modem control register (MCR)

The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting this bit to a logic 1 forces the $\overline{DTR}$ output to its active state (low). When bit 0 is set to a logic 0, $\overline{DTR}$ goes high.

Bit 1. Bit 1 (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 2. Bit 2 (OUT 1) controls the output 1 ($\overline{OUT\ 1}$) signal, a user designated output signal, in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 3. Bit 3 (OUT 2) controls the output 2 ($\overline{OUT\ 2}$) signal, a user designated output signal, in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1. The transmitter serial output (SOUT) is set high.
2. The receiver serial input (SIN) is disconnected.
3. The output of the transmitter shift register is looped back into the receiver shift register input.
4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four modem control inputs.
6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

Bit 5 through 7. These bits are set to logic 0.

line status register (LSR)†

The line status register provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the data ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the receiver buffer register and is reset to logic 0 by reading the receiver buffer register.

Bit 1‡. Bit 1 is the overrun error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the receiver buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the line status register.

Bit 2‡. Bit 2 is the parity error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the line control register (bit 4). The PE bit is reset every time the CPU reads the contents of the line status register.

Bit 3‡. Bit 3 is the framing error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) stop bit. The FE bit is reset every time the CPU reads the contents of the line status register.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR)† (continued)

Bit4‡. Bit 4 is the break interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The B1 bit is reset every time the CPU reads the contents of the line status register.

Bit 5. Bit 5 is the transmitter holding register empty (THRE) indicator. This bit is set to a logic 1 condition when the transmitter holding register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the transmitter holding register are transferred to the transmitted shift register. This bit is reset to logic 0 concurrent with the loading of the transmitter holding register by the CPU.

Bit 6. Bit 6 is the transmitter empty (TEMT) indicator. This bit is set to a logic 1 when the transmitter holding register and the transmitter shift register are both empty. When either the transmitter holding register or the transmitter shift register contains a data character, the TEMT bit is reset to logic 0.

Bit 7. This bit is always reset to logic 0.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

modem status register (MSR)

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the modem status register. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the delta clear to send (DCTS) indicator. This bit indicates that the $\overline{\text{CTS}}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

Bit 1. Bit 1 is the delta data set ready (DDSR) indicator. This bit indicates that the $\overline{\text{DSR}}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status Interrupt is enabled, a modem status interrupt is generated.

Bit 2. Bit 2 is the trailing edge of ring indicator (TERI) detector. This bit indicates that the $\overline{\text{RI}}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the modem status Interrupt is enabled, a modem status interrupt is generated.

Bit 3. Bit 3 is the delta data carrier detect (DDCD) indicator. This bit indicates that the $\overline{\text{DCD}}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

Bit 4. Bit 4 is the complement of the clear to send ($\overline{\text{CTS}}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 1 (RTS).

Bit 5. Bit 5 is the complement of the data set ready ($\overline{\text{DSR}}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 0 (DTR).

Bit 6. Bit 6 is the complement of the ring indicator ($\overline{\text{RI}}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the complement of the data carrier detect ($\overline{\text{DCD}}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 3 (OUT 2).

PRINCIPLES OF OPERATION

scratch register (SCR)

The scratch register is an 8-bit register that is intended for programmer use as a scratchpad, in the sense that it will temporarily hold programmer data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between DC and 9 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the baud generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = XTAL1 frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called divisor latches, are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 5 and 6 illustrate the use of the baud generator with crystal frequencies of 1,8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

PRINCIPLES OF OPERATION

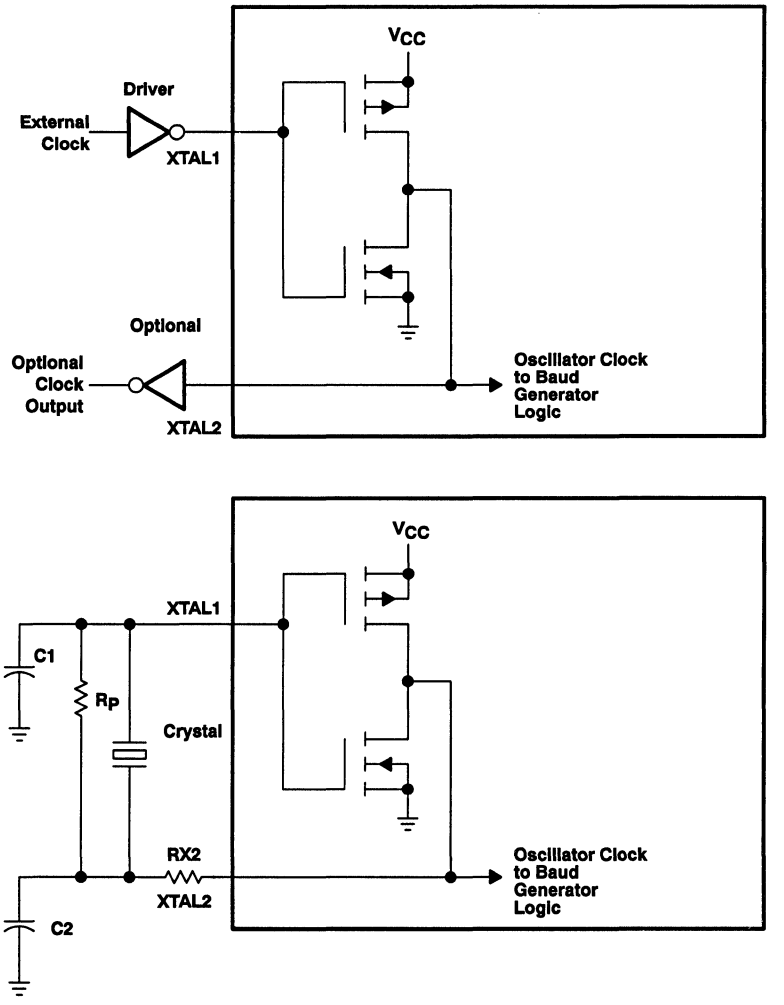
Table 5. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 6. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

PRINCIPLES OF OPERATION



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 10. Typical Clock Circuits

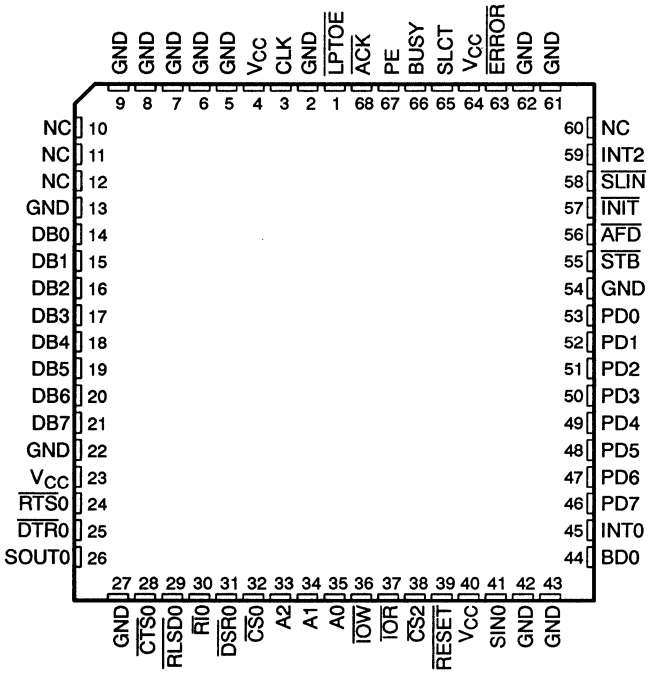
SLLS053A – D3284, MAY 1989 – REVISED JANUARY 1990

- **Integrates Most Communications Card Functions From the IBM PC/AT or Compatibles With Single- or Dual-Channel Serial Ports**
- **TL16C451 Consists of One TL16C450 Plus Centronix Printer Interface**
- **TL16C452 Consists of Two TL16C450s Plus Centronix Printer Interface**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2 Stop-Bit Generation**
  - **Programmable Baud Rate (dc to 256 kb/s Per Second)**
- **Fully Double Buffered for Reliable Asynchronous Operation**

description

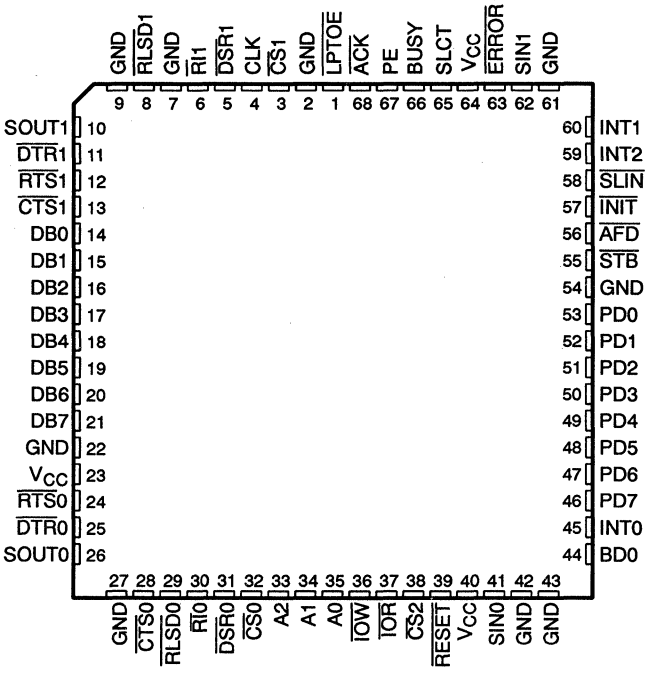
The TL16C451 and TL16C452 provide single-and dual-channel (respectively) serial interfaces along with a single Centronix parallel-port interface. The serial interfaces provide a serial-to-parallel conversion for data received from a peripheral device or modem and a parallel-to-serial conversion for data transmitted by a computer CPU. The parallel interface provides a bidirectional parallel data port that fully conforms to the requirements for a Centronix-type printer. A computer CPU can read the status of the asynchronous-communications-element (ACE) interfaces at any point in the operation. The status includes the state of the modem signals ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and RI) and any changes to these signals that have occurred since the last time they were read, the state of the transmitter and receiver including errors detected on received data, and printer status. The TL16C451 and TL16C452 provide control for modem signals ($\overline{RTS}$ and $\overline{DTR}$), interrupt enables, baud-rate programming, and parallel-port control signals.

TL16C451 . . . FN PACKAGE
(TOP VIEW)

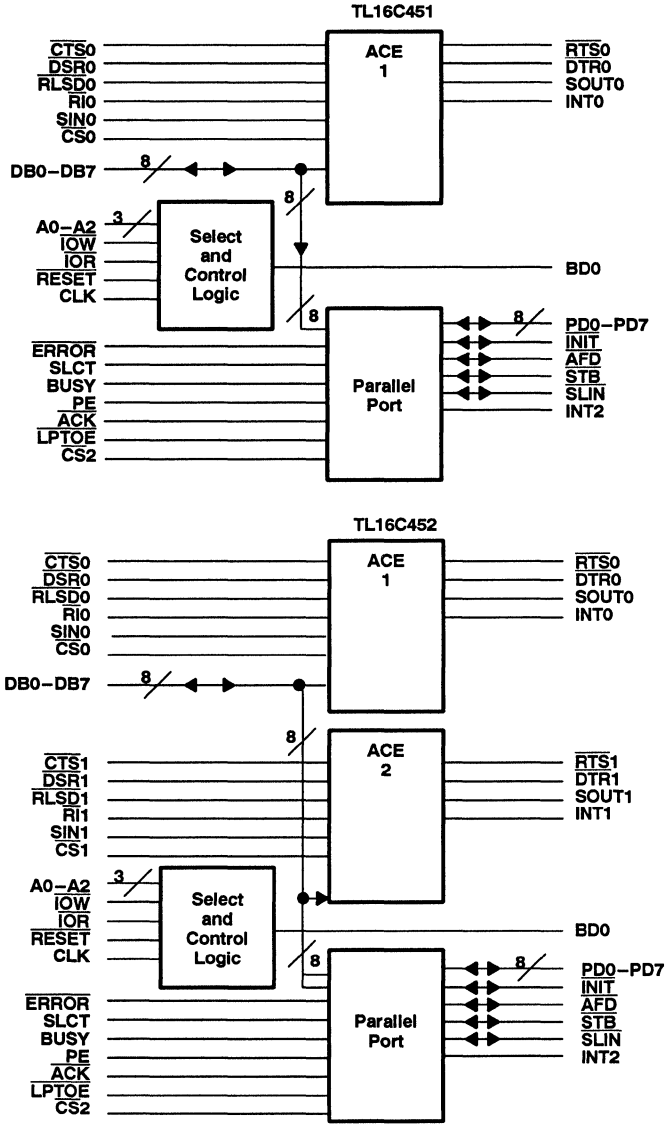


NC – No internal connection

TL16C452 . . . FN PACKAGE
(TOP VIEW)



functional block diagrams



Terminal Functions

PIN NAME†	PIN NO.	I/O	DESCRIPTION
A0 A1 A2	35 34 33	I	Register select. Three inputs used during read and write operations to select the register to read from or write to. Refer to Table 1 for register addresses, also refer to the chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$).
$\overline{ACK}$	68	I	Line printer acknowledge. This input goes low to indicate a successful data transfer has taken place. It generates a printer-port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. This open-drain line provides the line printer with a low signal when continuous-form paper is to be autofed to the printer. An internal pullup is provided.
BDO	44	O	Bus buffer output. This output is active (high) when the CPU is reading data. When active, this output can be used to disable an external transceiver.
BUSY	66	I	Line printer busy. This is an input line from the line printer that goes high when the line printer is not ready to accept data.
CLK	4	I/O	External clock. Connects the ACE to the main timing reference.
$\overline{CS0}$ $\overline{CS1}$ [V_{CC}] $\overline{CS2}$	32 3 38	I	Chip selects. Each chip select enables read and write operations to its respective channel. $\overline{CS0}$ and $\overline{CS1}$ select serial channels 0 and 1, respectively, and $\overline{CS2}$ selects the parallel port.
$\overline{CTS0}$ $\overline{CTS1}$ [GND]	28 13	I	Clear to send. $\overline{CTS}$ is an active-low modem status signal whose state can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	14 15 16 17 18 19 20 21	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the TL16C451/TL16C452 and the CPU. DBO is the least significant bit (LSB).
$\overline{DSR0}$ $\overline{DSR1}$ [GND]	31 5	I	Data set ready. $\overline{DSR}$ is an active-low modem status signal whose state can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR0}$ $\overline{DTR1}$ [NC]	25 11	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a reset or during loop mode operation or resetting bit 0 (DTR) of the modem control register.
$\overline{ERROR}$	63	I	Line printer error. This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
$\overline{INIT}$	57	I/O	Line printer initialize. This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started. An internal pullup is provided.
INT0 INT1 [NC]	45 60	O	Interrupt. INTn is an active-high 3-state output that is enabled by bit 3 of the MCR. When active, INTn informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTn output is reset (low) either when the interrupt is serviced or as a result of a reset.
INT2	59	O	Printer port interrupt. This signal is an active-high 3-state output generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the write control register.
$\overline{IOR}$	37	I	Data read strobe. When $\overline{IOR}$ input is active (low) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register.
$\overline{IOW}$	66	I	Data write strobe. When $\overline{IOW}$ input is active (low) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register.

† Names shown in brackets are for the TL16C451.

Terminal Functions (continued)

PIN NAME†	PIN NO.	I/O	DESCRIPTION
$\overline{\text{LPTOE}}$	1	I	Parallel data output enable. When low, this signal enables the write data register to the PD0–PD7 lines. A high puts the PD0–PD7 lines in the high-impedance state allowing them to be used as inputs. $\overline{\text{LPTOE}}$ is usually tied low for line printer operation.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when $\overline{\text{LPTOE}}$ is high.
PE	67	I	Line printer paper empty. This is an input line from the line printer that goes high when the printer runs out of paper.
$\overline{\text{RESET}}$	39	I	Reset. When active (low), $\overline{\text{RESET}}$ clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{\text{RI}}$0 $\overline{\text{RI}}$1 [GND]	30 6	I	Ring indicator. $\overline{\text{RI}}$ is an active-low modem status signal whose state can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{\text{RI}}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{\text{RLSD}}$0 $\overline{\text{RLSD}}$1 [GND]	29 8	I	Receive line signal detect. $\overline{\text{RLSD}}$0 is an active-low modem status signal whose state can be checked by reading bit 7 of the modem status register. Bit 3 (DRLSD) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{\text{RLSD}}$0 changes state, an interrupt is generated. This bit is low when a data carrier is detected.
$\overline{\text{RTS}}$0 $\overline{\text{RTS}}$1 [NC]	24 12	O	Request to send. When active (low), this signal informs the modem or data set that the ACE is ready to transmit data. $\overline{\text{RTS}}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a reset or during loop mode operations or by resetting bit 1 (RTS) of the modem control register.
SIN0 SIN1 [GND]	41	I	Serial input. Serial data input from a connected communications device.
SLCT	65	I	Line printer selected. This is an input line from the line printer that goes high when the line printer has been selected.
$\overline{\text{SLIN}}$	58	I/O	Line printer select. This open-drain line selects the printer when it is active (low). An internal pullup is provided.
SOUT0 SOUT1 [NC]	26 10	I	Serial output. Composite serial data output to a connected communication device. SOUT is set to the marking (logic 1) state as a result of reset.
$\overline{\text{STB}}$	55	I/O	Line printer strobe. This open-drain line provides communication synchronization between the TL16C451/TL16C452 and the line printer. When it is active (low), it provides the line printer with a signal to latch the data currently on the parallel port. An internal pullup is provided.
V_{CC}	23,40, 64		5-V supply voltage
GND	2,7,9 22,27,42, 43,54,61		Supply common

† Names shown in brackets are for the TL16C451.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Continuous total power dissipation ..... 1100 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA on DB0–DB7	2.4			V
		I_{OH} = −2 mA to 4 mA on PD0–PD7				
		I_{OH} = −0.2 mA on INIT, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$				
		I_{OH} = −0.2 mA on all other outputs				
V_{OL}	Low-level output voltage	I_{OL} = 4 mA on DB0–DB7			0.4	V
		I_{OL} = 12 mA on PD0–PD7				
		I_{OL} = 10 mA on INIT, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2)				
		I_{OL} = 2 mA on all other outputs				
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±10	µA
	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected and write mode, or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, V_{SS} = 0, SIN, $\overline{DSR}$, $\overline{RLSD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All others pins grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ are open-collector output pins that each have an internal pullup to V_{CC}. This will generate a maximum of 2 mA of internal I_{OL} per pin. In addition to this internal current, each pin will sink at least 10 mA while maintaining the V_{OL} specification of 0.4 V Max.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175		ns
t_{w1}	Pulse duration, clock high	1	50		ns
t_{w2}	Pulse duration, clock low	1	50		ns
t_{w5}	Pulse duration, write strobe	2	80		ns
t_{w6}	Pulse duration, read strobe	3	80		ns
t_{wRST}	Pulse duration, reset		1000		ns
t_{su1}	Setup time, address	2,3	15		ns
t_{su2}	Setup time, chip select	2,3	15		ns
t_{su3}	Setup time, data	2	15		ns
t_{h1}	Hold time, address	2,3	20		ns
t_{h2}	Hold time, chip select	2,3	20		ns
t_{h3}	Hold time, data	2	15		ns
t_{d3}	Delay time, write cycle	2	80		ns
t_{d4}	Delay time, read cycle	3	80		ns

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, read to data	3	C_L = 100 pF		60	ns
t_{d6}	Delay time, read to floating data	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable	3	C_L = 100 pF		60	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d7}	Delay time, RCLK to sample	4			100	ns
t_{d8}	Delay time, stop to set interrupt	4		1	1	RCLK cycles
t_{d9}	Delay time, read RBR/LSR to reset interrupt	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d10}	Delay time, initial write THR to transmit start	5		8	24	baudout cycles
t_{d11}	Delay time, stop to interrupt	5		8	8	baudout cycles
t_{d12}	Delay time, write THR to reset interrupt	5	C_L = 100 pF		140	ns
t_{d13}	Delay time, initial write to interrupt (THRE)	5		16	32	baudout cycles
t_{d14}	Delay time, read IIR to reset interrupt (THRE)	5	C_L = 100 pF		140	ns

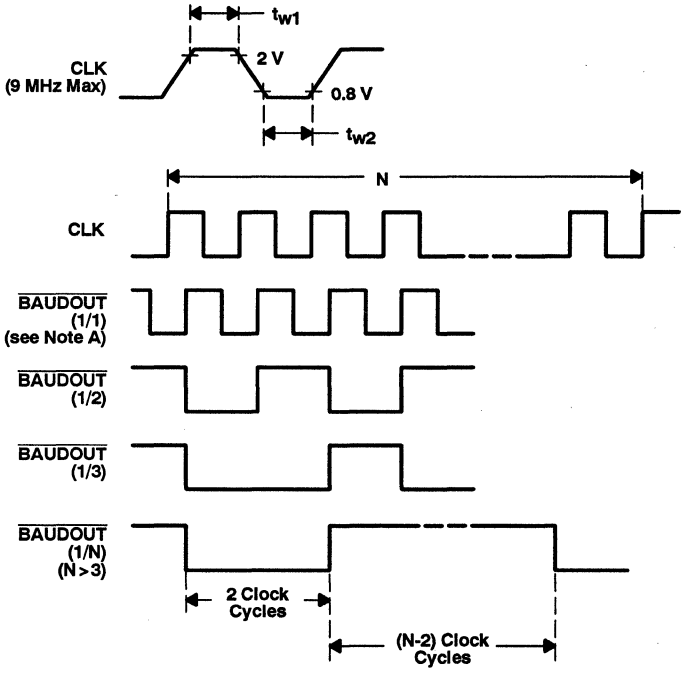
modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, write MCR to output	6	C_L = 100 pF		100	ns
t_{d16}	Delay time, modem input to set interrupt	6	C_L = 100 pF		170	ns
t_{d17}	Delay time, read MSR to reset interrupt	6	C_L = 100 pF		140	ns

parallel port switching characteristics over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d18}	Delay time, write parallel port control to output	7	C_L = 100 pF		60	ns
t_{d19}	Delay time, write parallel port data to output	7	C_L = 100 pF		60	ns
t_{d20}	Delay time, output enable to data	7	C_L = 100 pF		60	ns
t_{d21}	Delay time, $\overline{ACK}$ to INT2	7	C_L = 100 pF		100	ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{BAUDOUT}$ is an internally generated signal used in the receiver and transmitter circuits to synchronize data.

Figure 1. Baud Generator Timing

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PARAMETER MEASUREMENT INFORMATION

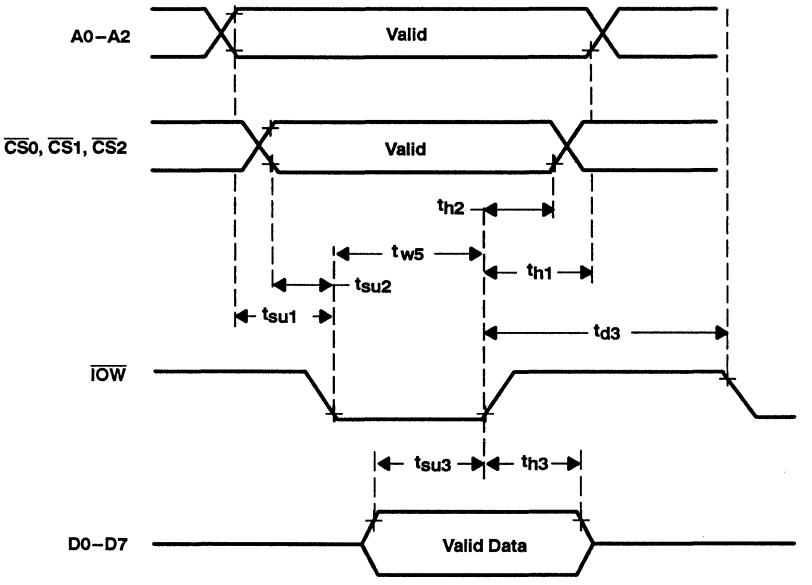

Figure 2. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

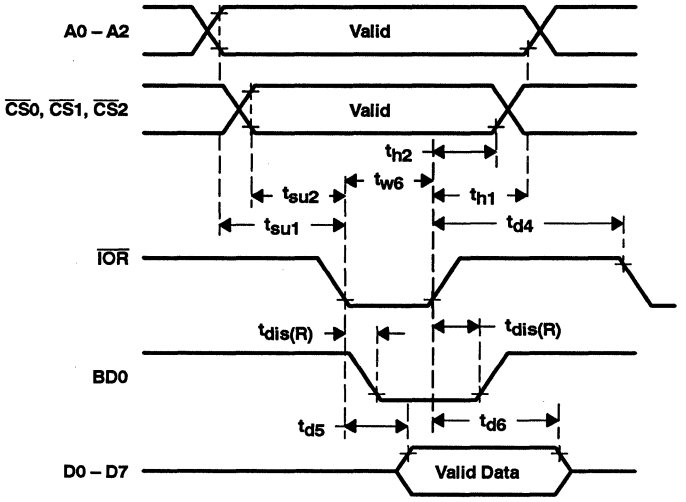

Figure 3. Read Cycle Timing

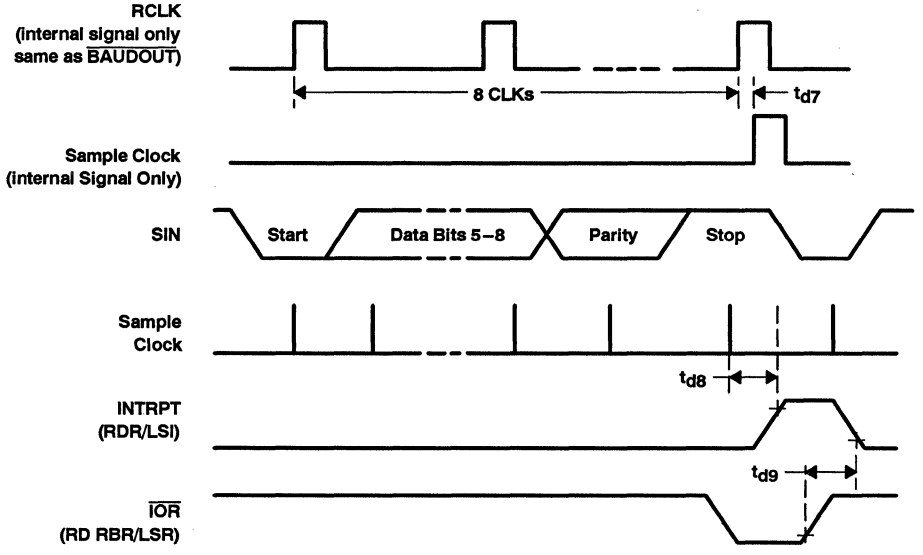

Figure 4. Receiver Timing

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PARAMETER MEASUREMENT INFORMATION

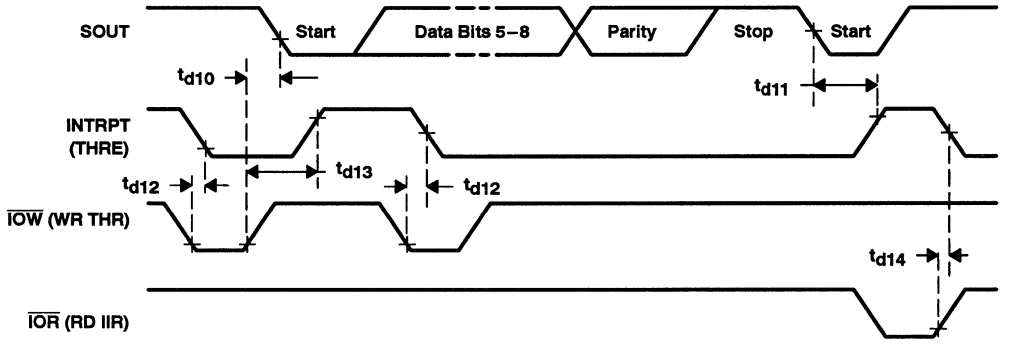

Figure 5. Transmitter Timing

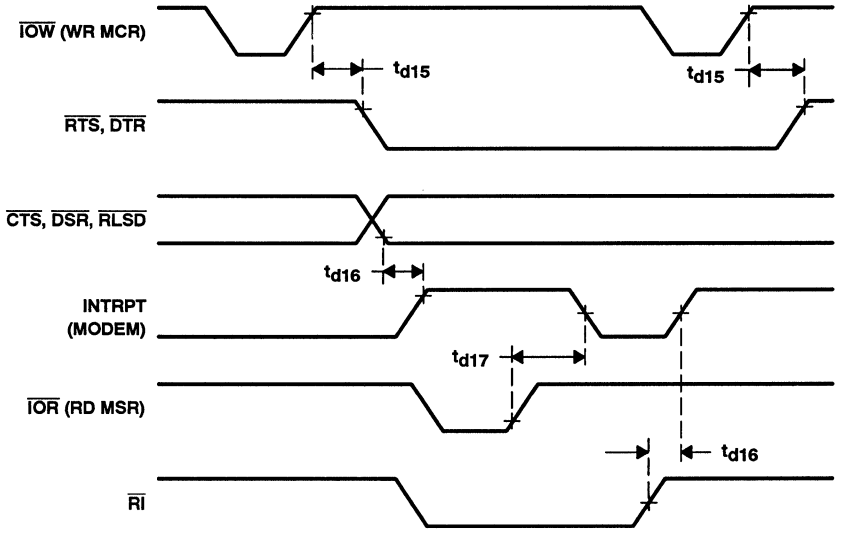

Figure 6. Modem Control Timing

PARAMETER MEASUREMENT INFORMATION

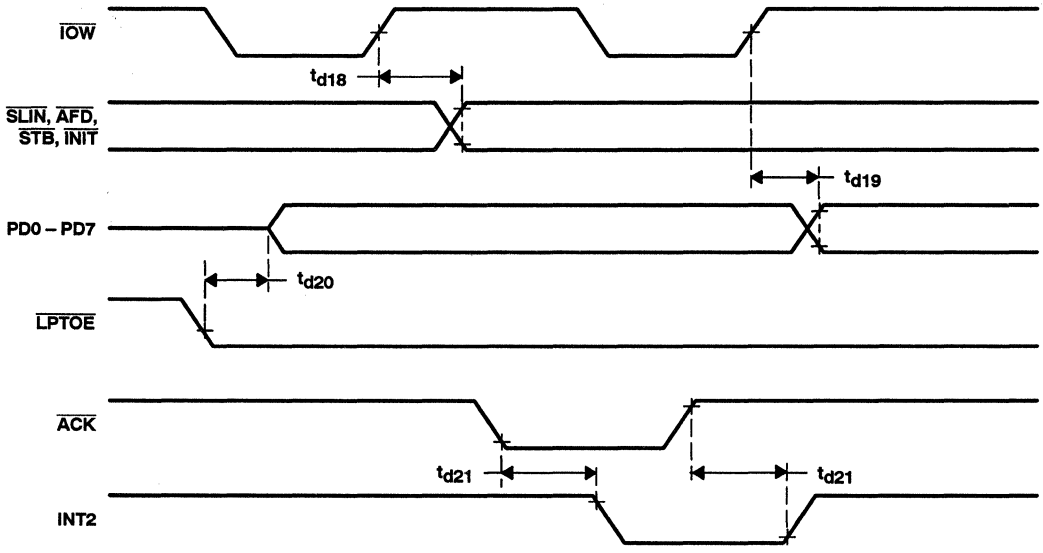

Figure 7. Parallel Port Timing

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APPLICATION INFORMATION

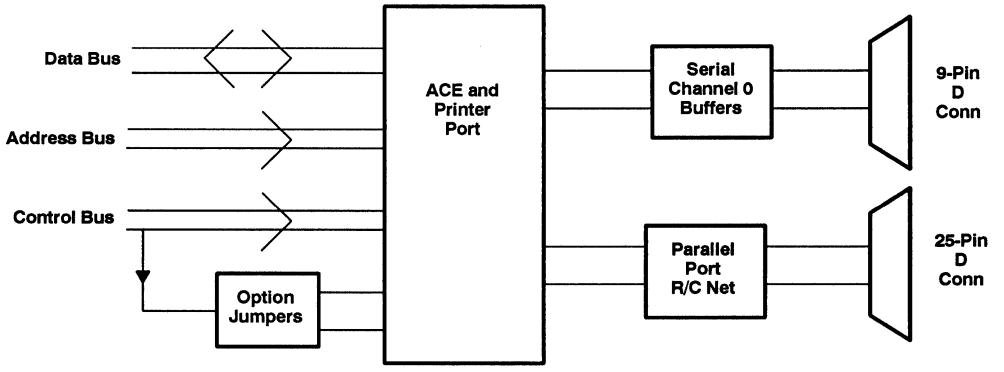


Figure 8. TL16C451

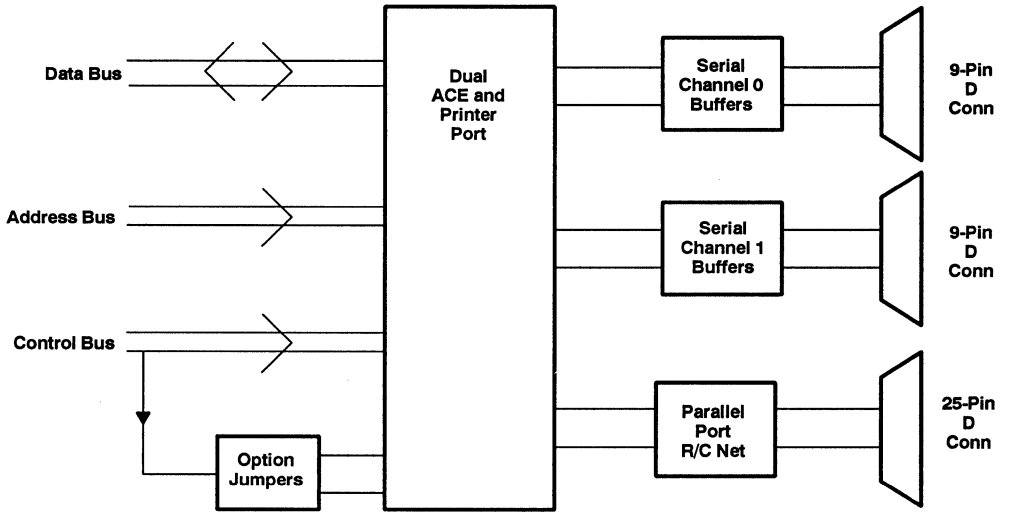


Figure 9. TL16C452

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	$\overline{\text{Reset}}$	All bits low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Reset	Bit 0 is high, bits 1 and 2 are low, and bits 3–7 are permanently low
Line Control Register	$\overline{\text{Reset}}$	All bits low
Modem Control Register	$\overline{\text{Reset}}$	All bits low
Line Status Register	$\overline{\text{Reset}}$	Bits 5 and 6 are high, all other bits are low
Modem Status Register	$\overline{\text{Reset}}$	Bits 0–3 are low, bits 4–7 are input signals
SOUT	$\overline{\text{Reset}}$	High
INTRPT (receiver error flag)	Read LSR/$\overline{\text{Reset}}$	Low
INTRPT (received data available)	Read RBR/$\overline{\text{Reset}}$	Low
INTRPT (transmitter holding register empty)	Read IIR/Write THR/$\overline{\text{Reset}}$	Low
INTRPT (modem status changes)	Read MSR/$\overline{\text{Reset}}$	Low
$\overline{\text{OUT 2}}$ (interrupt enable)	$\overline{\text{Reset}}$	High
$\overline{\text{RTS}}$	$\overline{\text{Reset}}$	High
$\overline{\text{DTR}}$	$\overline{\text{Reset}}$	High
$\overline{\text{OUT 1}}$	$\overline{\text{Reset}}$	High
Scratch Register	$\overline{\text{Reset}}$	No effect
Divisor Latch (LSB and MSB) Registers	$\overline{\text{Reset}}$	No effect
Receiver Buffer Registers	$\overline{\text{Reset}}$	No effect
Transmitter Holding Registers	$\overline{\text{Reset}}$	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS										
	O DLAB = 0	O DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	O DLAB = 1	1 DLAB = 0
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERBF)	"0" If Interrupt Pending	Word Length Select Bit 0 (WLSO)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBE)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 (Interrupt Enable)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmit-ter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmit-ter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Receive Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register and a receiver buffer register. Timing is supplied by the 16 X receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE receiver shift register receives serial data from the serial input (SIN) pin. The receiver shift register then converts the data to a parallel form and loads it into the receiver buffer register. When a character is placed in the receiver buffer register and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the receiver buffer register.

transmitter holding register (THR)

The ACE transmitter section consists of a transmitter holding register and a transmitter shift register. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE transmitter holding register receives data off the internal data bus and, when the shift register is idle, moves it into the transmitter shift register. The transmitter shift register serializes the data and outputs it at the serial output (SOUT). If the transmitter holding register is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

interrupt enable register (IER)

The interrupt enable register enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

Bit 0. This bit, when set to logic 1, enables the received data available interrupt.

Bit 1. This bit, when set to logic 1, enables the transmitter holding register empty interrupt.

Bit 2. This bit, when set to logic 1, enables the receiver line status interrupt.

Bit 3. This bit, when set to logic 1, enables the modem status interrupt.

Bits 4 thru 7. Bits 4 through 7 in the interrupt enable register are not used and are always set to logic 0.

PRINCIPLES OF OPERATION

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 – Receiver line status (highest priority)
Priority 2 – Receiver data ready
Priority 3 – Transmitter holding register empty
Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

Bit 0. This bit can be used either in a hardwire prioritized or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 thru 7. Bits 3 through 7 in the interrupt idendtification register are not used and are always set at logic 0.

Table 4 . Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
1	0	0	2	Received data available	Receiver data available	Reading the receiver buffer register
0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt Identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

PRINCIPLES OF OPERATION

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2. This bit specifies either one, one and one-half, or two stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the data. If bit 2 is a logic 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The number of stop bits generated, in relation to word length and bit 2, is as follows:

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

Bit 3. This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

Bit 4. Bit 4 is the even parity select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces even parity (an even number of logic is in the data and parity bits) and a logic 0 in bit 4 produces odd parity (an odd number of logic 1s).

Bit 5. This is the stick parity bit. When bits 3, 4, and 5 are logic 1s, the parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the parity bit is transmitted and checked as a logic 1.

Bit 6. This bit is the break control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the serial output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic, it only effects the serial output.

Bit 7. This bit is the divisor latch access bit (DLAB). Bit 7 must be set to a logic 1 to access the divisor latches of the baud generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

modem control register (MCR)

The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting this bit to a logic 1 forces the $\overline{DTR}$ output to its active state (low). When bit 0 is set to a logic 0, $\overline{DTR}$ goes high.

Bit 1. Bit 1 (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 2. Bit 2 (OUT 1) is a reserved location used only in the loopback mode.

Bit 3. Bit 3 (OUT 2) controls the output enable for the interrupt signal. When set to a logic 1, the interrupt is enabled. When bit 3 is set to a logic 0, the interrupt is disabled.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1. The transmitter serial output (SOUT) is set high.
2. The receiver serial input (SIN) is disconnected.
3. The output of the transmitter shift register is looped back into the receiver shift register input.
4. The four modem status inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected.
5. The modem control register bits (DTR, RTS, OUT1, and OUT2) are connected to the modem status register bits (DSR, CTS, RI, and RLSD), respectively.
6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

Bit 5 through 7. These bits are set to logic 0.

line status register (LSR)†

The line status register provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the data ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the receiver buffer register and is reset to logic 0 by reading the receiver buffer register.

Bit 1‡. Bit 1 is the overrun error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the receiver buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the line status register.

Bit 2‡. Bit 2 is the parity error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the line control register (bit 4). The PE bit is reset every time the CPU reads the contents of the line status register.

Bit 3‡. Bit 3 is the framing error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the line status register.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR)† (continued)

Bit 4‡. Bit 4 is the break interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is reset every time the CPU reads the contents of the line status register.

Bit 5. Bit 5 is the transmitter holding register empty (THRE) indicator. This bit is set to a logic 1 condition when the transmitter holding register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the transmitter holding register are transferred to the transmitted shift register. This bit is reset to logic 0 concurrent with the loading of the transmitter holding register by the CPU.

Bit 6. Bit 6 is the transmitter empty (TEMT) indicator, This bit is set to a logic 1 when the transmitter holding register and the transmitter shift register are both empty. When either the transmitter holding register or the transmitter shift register contains a data character, the TEMT bit is reset to logic 0.

Bit 7. This bit is always reset to logic 0.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

modem status register (MSR)

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the modem status register. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the delta clear to send (DCTS) indicator. This bit indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status Interrupt is enabled, a modem status interrupt is generated.

Bit 1. Bit 1 is the delta data set ready (DDSR) indicator. This bit indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status Interrupt is enabled, a modem status interrupt is generated.

Bit 2. Bit 2 is the trailing edge of ring indicator (TERI) detector. This bit indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the modem status Interrupt is enabled, a modem status interrupt is generated.

Bit 3. Bit 3 is the delta receive line signal detect (DRLSD) indicator. This bit indicates that the $\overline{RLSD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

Bit 4. Bit 4 is the complement of the clear to send ($\overline{CTS}$) input, If Bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 1 (RTS).

Bit 5. Bit 5 is the complement of the data set ready ($\overline{DSR}$) input. If Bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 0 (DTR).

Bit 6. Bit 6 is the complement of the ring indicator ($\overline{RI}$) input. If Bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the complement of the receive line signal detect ($\overline{RLSD}$) input. If Bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 3 (OUT 2).

PRINCIPLES OF OPERATION

scratch register (SCR)

The scratch register is an 8-bit register that is intended for programmer use as a scratchpad, in the sense that it will temporarily hold programmer data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the baud generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = CLK frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called divisor latches, are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

interrupt control logic

The interrupt control logic is shown in Figure 10.

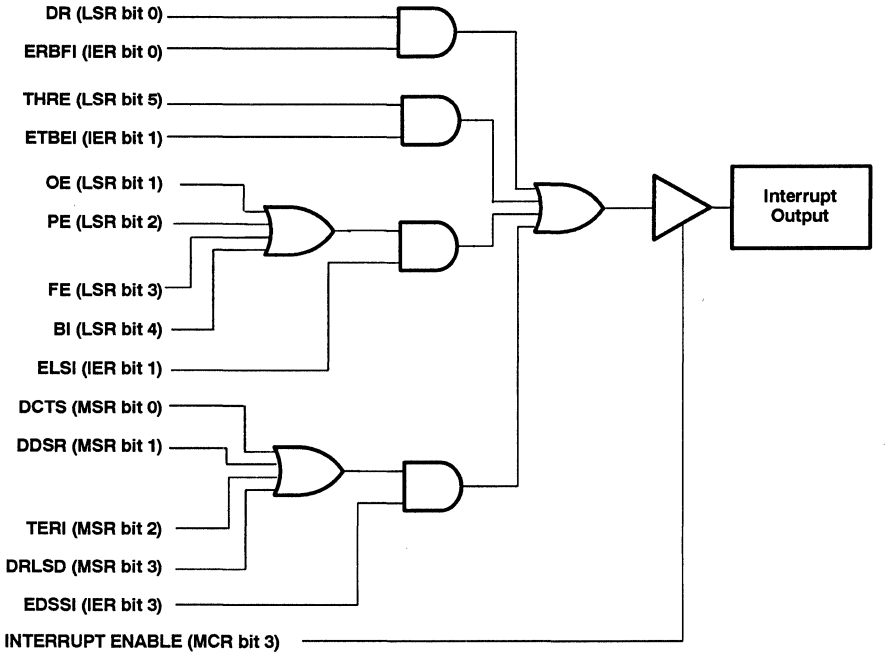


Figure 10. Interrupt Control Logic

PRINCIPLES OF OPERATION

parallel port registers

The parallel port registers interface either device to a Centronix-style printer. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Tables 5 and 6 show the registers associated with this parallel port. The read or write function of the register is controlled by the state or the read ($\overline{IOR}$) and write ($\overline{IOW}$) pin as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are printer busy ($\overline{BUSY}$), acknowledge ($\overline{ACK}$) which is a handshake function, paper empty (PE), printer selected (SLCT), and error ($\overline{ERROR}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines, which are interrupt enable (IRQ ENB), select In (SLIN), initialize the printer ($\overline{INIT}$), autofeed the paper (AFD), and strobe (STB), which informs the printer of the presence of a valid byte on the parallel bus. These signals are set to 0 when a reset occurs. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial/parallel adaptor.

Table 5. Parallel Port Registers

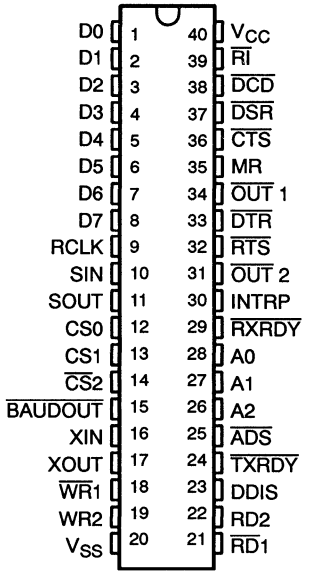
REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	AFD	STB

Table 6. Parallel Port Register Select

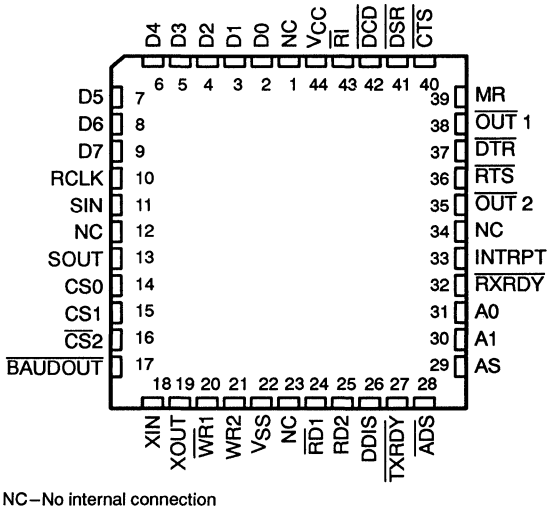
CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read Data
L	H	L	L	H	Read Status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write Data
H	L	L	L	H	Invalid
H	L	L	H	L	Write Control
H	L	L	H	H	Invalid

- Capable of Running With All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- In the FIFO Mode, Transmitter and Receiver Are Each Buffered With 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU
- In the TL16C450 Mode, Holding and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generates an Internal 16 X Clock
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data Stream
- Independent Receiver Clock Input
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Fully Programmable Serial Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (dc to 256 Kilobits Per Second)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)
- Faster Plug-In Replacement for National Semiconductor NS16550A

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL16C550A is a functional upgrade of the TL16C450 asynchronous communications element (ACE). Functionally identical to the TL16C450 on power up (character mode†), the TL16C550A can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

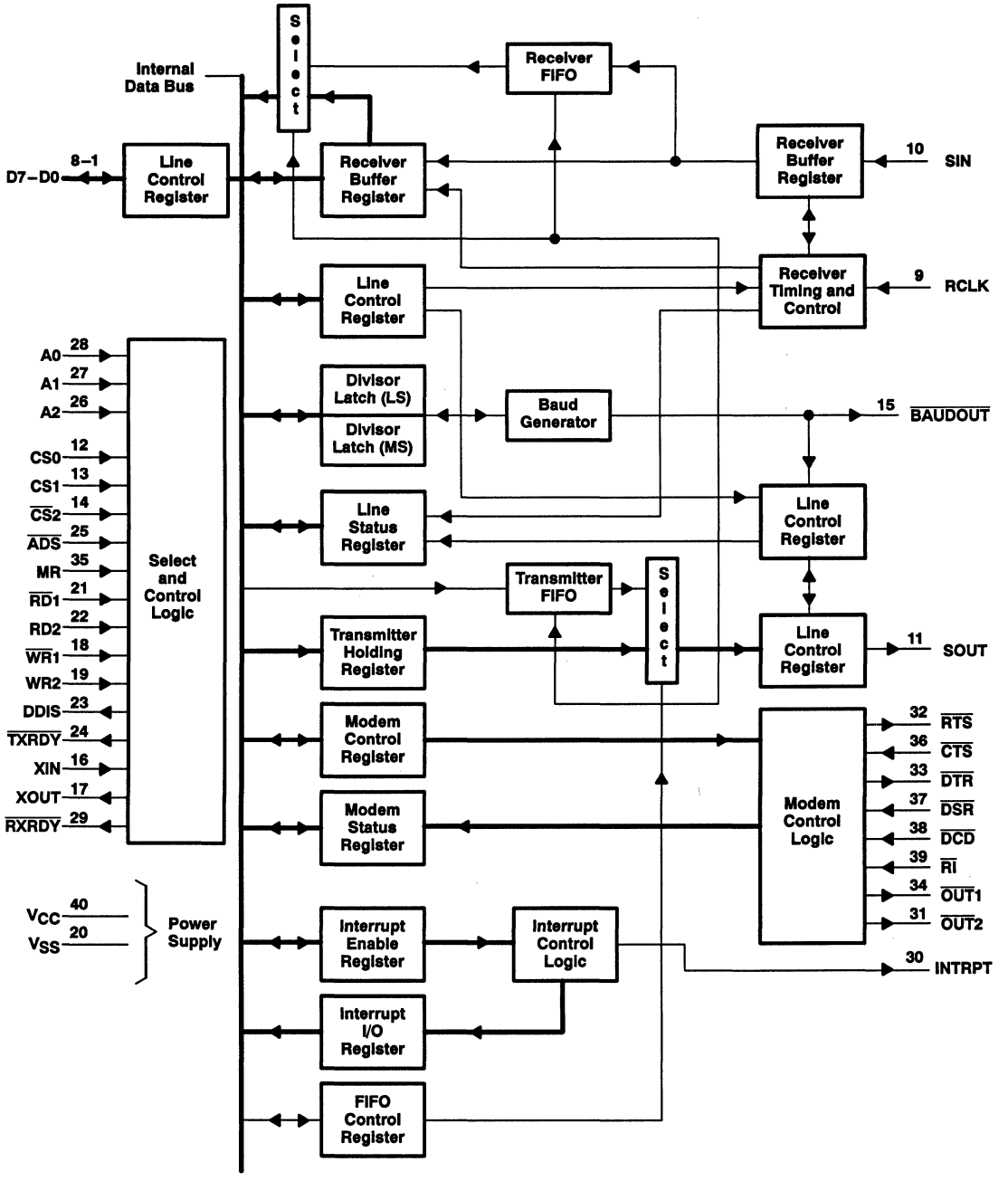
In this mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits or error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 pin functions (pins 24 and 29 on the N package and pins 27 and 32 on the FN package) have been changed to allow signalling of DMA transfers.

The TL16C550A performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550A ACE includes a programmable, on-board, baud-rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to $(2^{16}-1)$ and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

† The TL16C550A can also be reset to the TL16C450 mode under software control.

block diagram



Pin numbers shown are for the N package.

Terminal Functions

PIN NAME	PIN NO.†	I/O	DESCRIPTION
A0 A1 A2	28 [31] 27 [30] 26 [29]	I	Register select. Three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25 [28]	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15 [17]	O	Baud out. 16 X clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 [14] 13 [15] 14 [16]	I	Chip select. When active (high, high, and low, respectively), these three inputs select the ACE. If any of these inputs are inactive, the ACE remains inactive. Refer to the $\overline{ADS}$ (address strobe) signal description.
$\overline{CTS}$	36 [40]	I	Clear to send. $\overline{CTS}$ is a modem status signal whose condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 D1 D2 D3 D4 D5 D6 D7	1 [2] 2 [3] 3 [4] 4 [5] 5 [6] 6 [7] 7 [8] 8 [9]	I/O	Data bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38 [42]	I	Data carrier detect. $\overline{DCD}$ is a modem status signal whose condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23 [26]	O	Driver disable. This output is active (high) when the CPU is not reading data. When active, this output can be used to disable an external transceiver.
$\overline{DSR}$	37 [41]	I	Data set ready. $\overline{DSR}$ is a modem status signal whose condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33 [37]	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or resetting bit 0 (DTR) of the modem control register.
INTRPT	30 [33]	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has a interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available or timeout (FIFO mode only), the transmitter holding register is empty, and an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35 [39]	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2.
$\overline{OUT1}$ $\overline{OUT2}$	34 [38] 31 [35]	O	Outputs 1 and 2. User-designated output pins that are set to their active states by setting their respective modem control register bits (OUT 1 and OUT 2) high. $\overline{OUT}$ 1 and $\overline{OUT}$ 2 are set to their inactive (high) states as a result of master reset or during loop mode operations or by resetting bit 2 (OUT 1) or bit 3 (OUT 2) of the MCR.
RCLK	9 [10]	I	Receiver clock. The 16 X baud rate clock for the receiver section of the ACE.
$\overline{RD1}$ RD2	21 [24] 22 [25]	I	Read inputs. When either input is active (high or low, respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{RD1}$ tied high).

† Pin numbers shown in brackets are for the FN package.

Terminal Functions (continued)

PIN NAME	PIN NO.†	I/O	DESCRIPTION
$\overline{RI}$	39 [43]	I	Ring indicator. $\overline{RI}$ is a modem status signal whose condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32 [36]	O	Request to send. When active, informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a master reset or during loop-mode operations or by resetting bit 1 (RTS) of the MCR.
$\overline{RXRDY}$	29 [32]	O	Receiver ready output. Receiver DMA signalling is available with this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating in the TL16V450 mode, only DMA Mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA Mode 0 (FCRO = 0 or FCRO = 1, FCR3 = 0), if there is at least 1 character in the receiver FIFO or receiver holding register, $\overline{RXRDY}$ will be active (low). When RXRDY has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ will go inactive (high). In DMA Mode 1 (FCRO = 1, FCR3 = 1), when the trigger level or the timeout has been reached, $\overline{RXRDY}$ will go active (low); when it has been active but there are no more characters in the FIFO or holding register, it will go inactive (high).
SIN	10 [11]	I	Serial input. Serial data input from a connected communications device.
SOUT	11 [13]	O	Serial output. Composite serial data output to a connected communication device. SOUT is set to the marking (logic 1) state as a result of master reset.
$\overline{TXRDY}$	24 [27]	O	Transmitter ready output. Transmitter DMA signalling is available with this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40 [44]		5-V supply voltage
V_{SS}	20 [22]		Supply common
$\overline{WR1}$ WR2	18 [20] 19 [21]	I	Write inputs. When either input is active (high or low, respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{WR1}$ tied high).
XIN XOUT	16 [18] 17 [19]	I/O	External clock. Connects the ACE to the main timing reference (clock or crystal).

† Pin numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{lkg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other pins floating			±10	μA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	μA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second			10	mA
C_{XIN}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other pins grounded, f = 1 MHz, T_A = 25°C		15	20	pF
C_{XOUT}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XOUT.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)	RC		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)	WC		175		ns
t_{w5}	Pulse duration, address strobe low	t_{ADS}	2, 3	15		ns
t_{w6}	Pulse duration, write strobe	t_{WR}	2	80		ns
t_{w7}	Pulse duration, read strobe	tRD	3	80		ns
t_{w8}	Pulse duration, master reset	t_{MR}		1		ns
t_{su1}	Setup time, address	t_{AS}	2, 3	15		ns
t_{su2}	Setup time, chip select	t_{CS}	2, 3	15		ns
t_{su3}	Setup time, data	t_{DS}	2	15		ns
t_{h1}	Hold time, address	t_{AH}	2, 3	0		ns
t_{h2}	Hold time, chip select	t_{CH}	2, 3	0		ns
t_{h3}	Hold time, write to chip select	t_{WCS}	2	20		ns
t_{h4}	Hold time, write to address	t_{WA}	2	20		ns
t_{h5}	Hold time, data	t_{DH}	2	15		ns
t_{h6}	Hold time, read to chip select	t_{RCS}	3	20		ns
t_{h7}	Hold time, read to address	t_{RA}	3	20		ns
t_{d4}§	Delay time, select to write	t_{CSW}	2	15		ns
t_{d5}§	Delay time, address to write	t_{AW}	2	15		ns
t_{d6}§	Delay time, write cycle	t_{WC}	2	80		ns
t_{d7}§	Delay time, chip select to read	t_{CSR}	3	15		ns
t_{d8}§	Delay time, address to read	t_{AR}	3	15		ns
t_{d9}	Delay time, read cycle	tRC	3	80		ns

§ Only applies when ADS is low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	t_{XH}	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	t_{XL}	1	f = 9 MHz maximum	50		ns
t_{d10}	Delay time, read to data	t_{RVD}	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, read to floating data	t_{HZ}	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Read to driver disable	t_{RDD}	3	C_L = 100 pF		60	ns

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{\text{BAUDOOUT}}$ low	t_{LW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{\text{BAUDOOUT}}$ low	t_{HW}	1	f = 9 MHz, CLK ÷ 2, C_L = 100 pF	100		ns
t_{d1}	Delay time, $\overline{\text{BAUDOUT}}$ low to high	t_{BLD}	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, $\overline{\text{BAUDOUT}}$ high to low	t_{BHD}	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	t_{SCD}	4			100	ns
t_{d13}	Delay time, stop to set interrupt or read RBR to LSI interrupt	t_{SINT}	4,5,6,7,8			1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	t_{RINT}	4,5,6,7,8	C_L = 100 pF		150	ns

NOTES: 2. Charge and discharge time is determined by V_{OL}, V_{OH}, and external loading.
3. In FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	9		8	24	baudout cycles
t_{d16}	Delay time, stop to interrupt	t_{STI}	9		8	8	baudout cycles
t_{d17}	Delay time, write THR to reset interrupt	t_{HR}	9	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrup (THRE)	t_{SI}	9		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	t_{IR}	9	C_L = 100 pF		140	ns
t_{d20}	Delay time, write to TXRDY inactive	t_{WXI}	10,11	C_L = 100 pF		195	ns
t_{d21}	Delay time, start to TXRDY active	t_{SXA}	10,11	C_L = 100 pF		8	baudout cycles

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d22}	Delay time, write MCR to output	t_{MDO}	12	C_L = 100 pF		100	ns
t_{d23}	Delay time, modem interrupt to set interrupt	t_{SIM}	12	C_L = 100 pF		170	ns
t_{d24}	Delay time, read MSR to reset interrupt	t_{RIM}	12	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

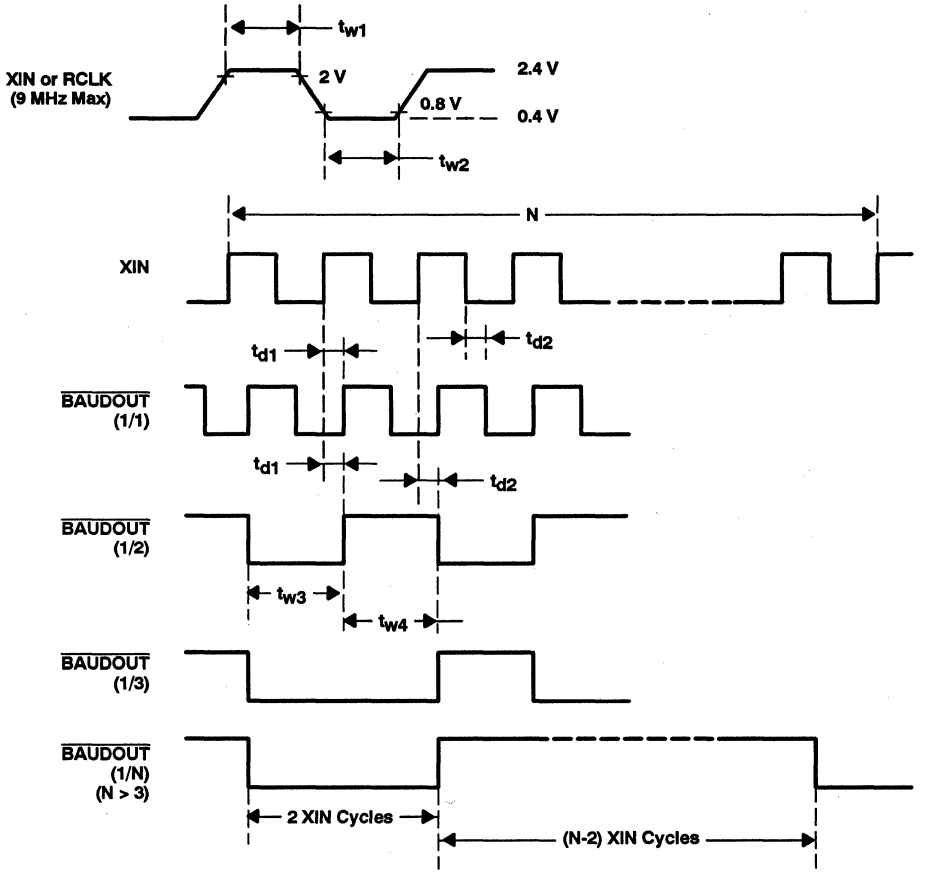
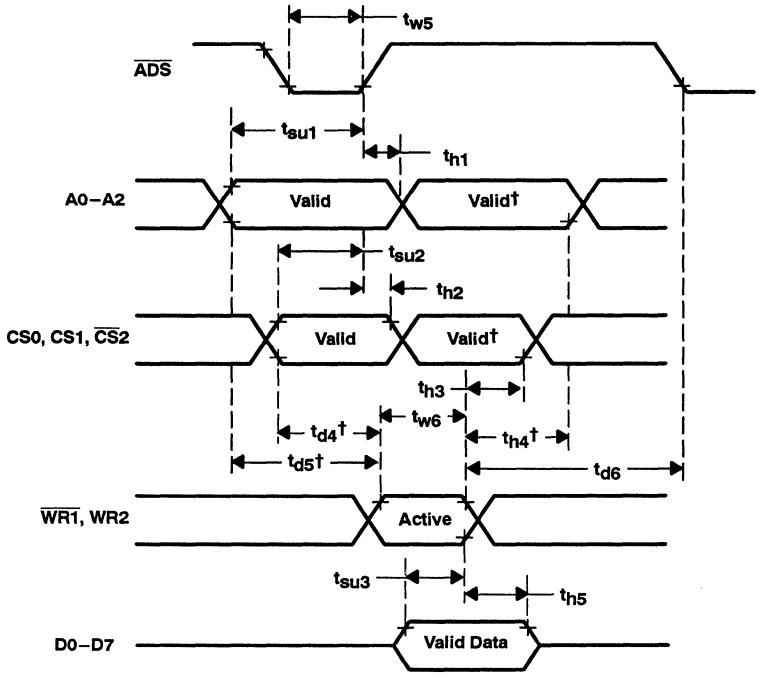


Figure 1. Baud Generator Timing

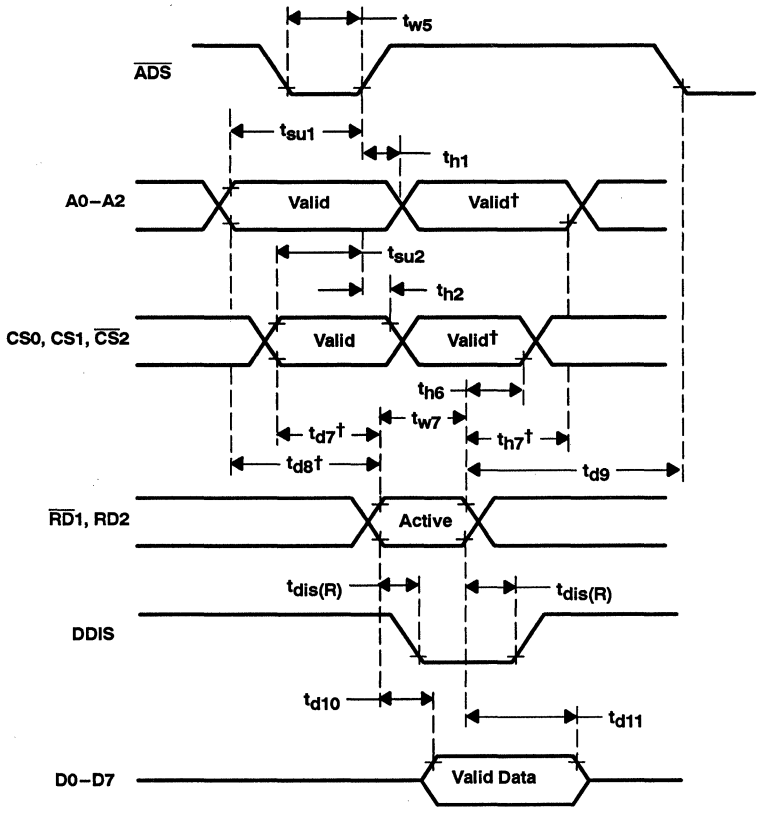
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 2. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Applicable only when ADS is tied low.

Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

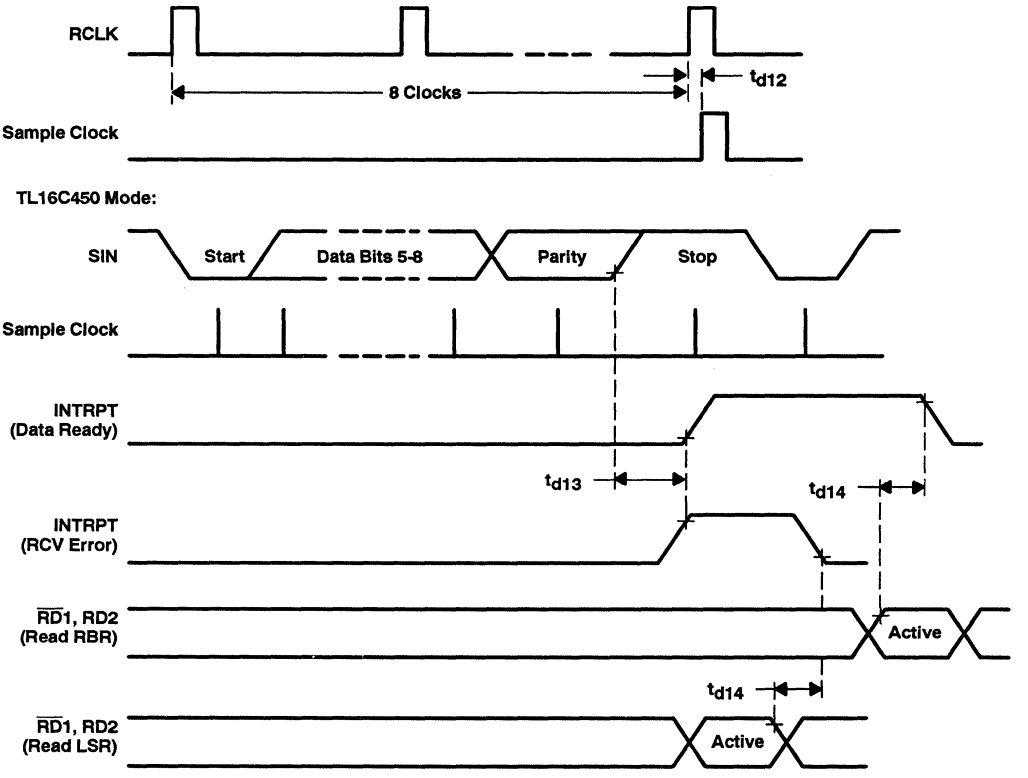


Figure 4. Receiver Timing

PARAMETER MEASUREMENT INFORMATION

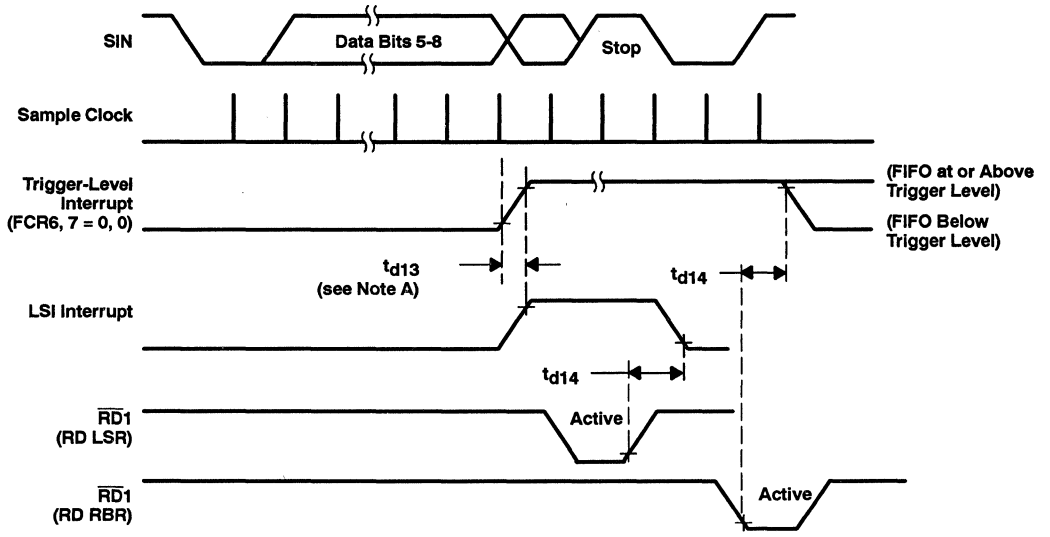


Figure 5. Receiver FIFO First Byte (Sets DR Bit)

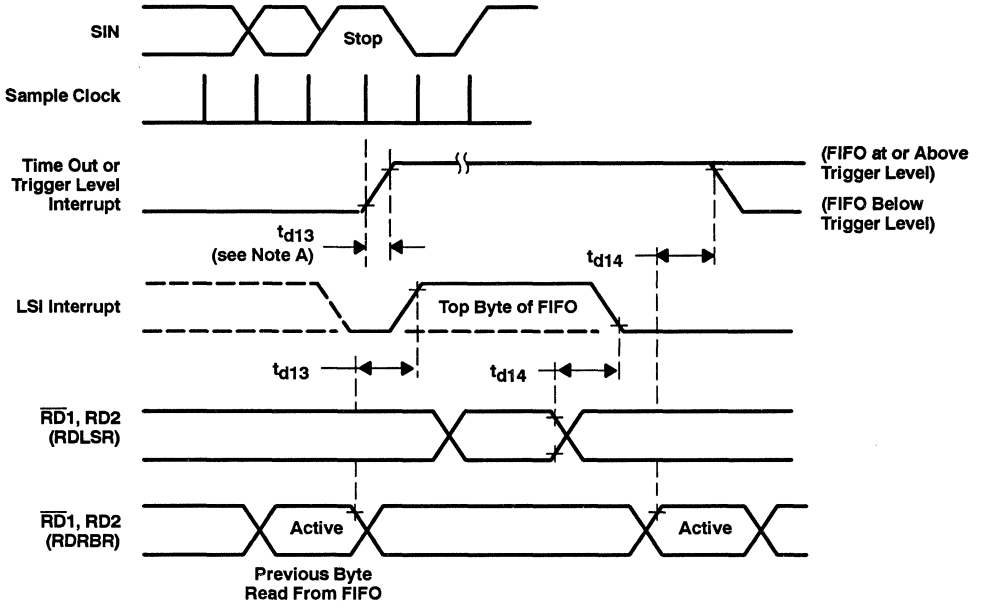


Figure 6. Receiver FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set)

NOTE A: For a timeout interrupt, t_{d13} = 8 RCLKs.

PARAMETER MEASUREMENT INFORMATION

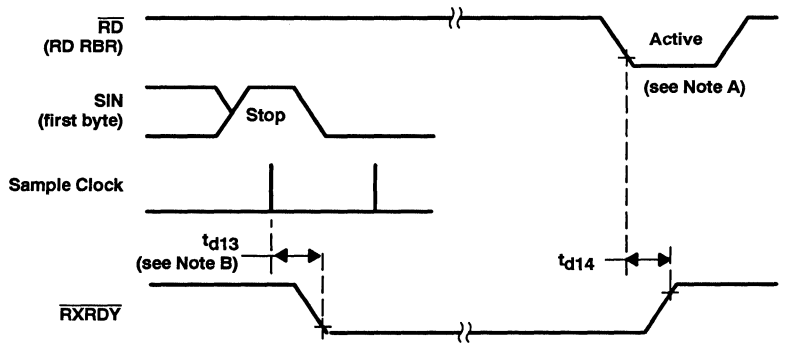


Figure 7. Receiver Ready ($\overline{RXRDY}$), FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)

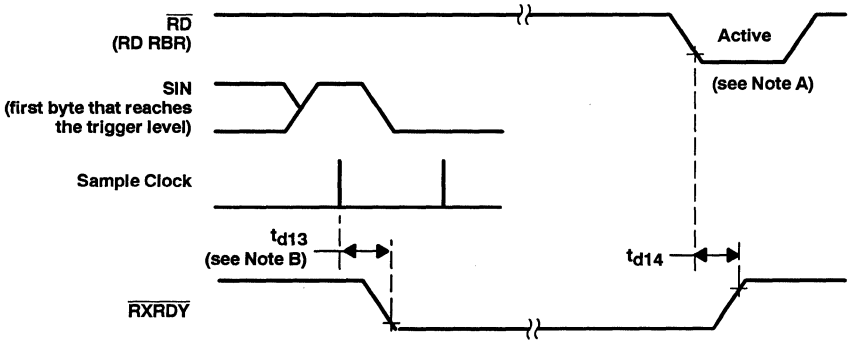


Figure 8. Receiver Ready ($\overline{RXRDY}$), FCR = 1 or FCR3 = 1 (mode 1)

NOTES: A. This is the reading of the last byte in the FIFO.
B. For a timeout interrupt, t_{d13} = 8 RCLKs.

PARAMETER MEASUREMENT INFORMATION

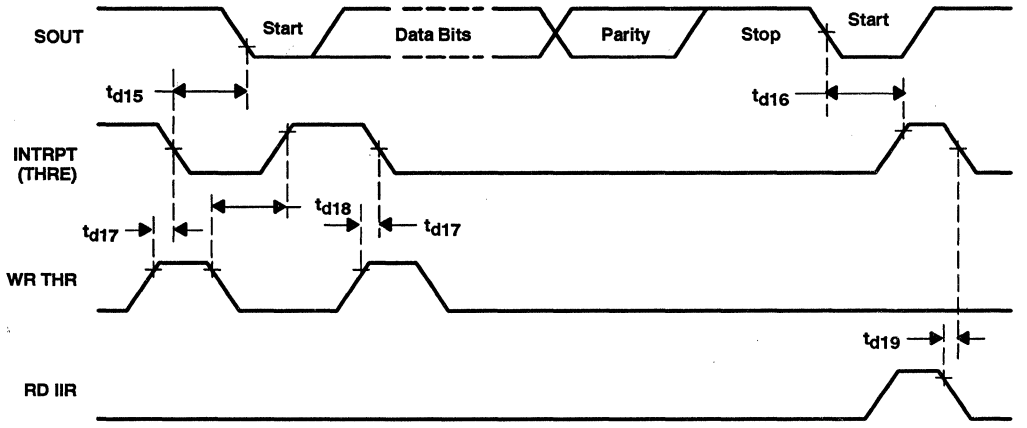


Figure 9. Transmitter Timing

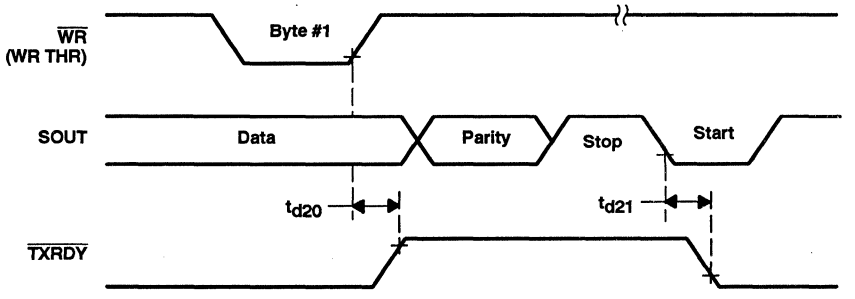


Figure 10. Transmitter Ready ($\overline{\text{TXRDY}}$), FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (mode 0)

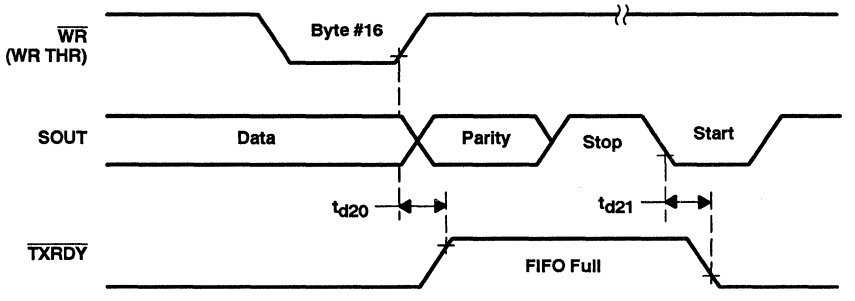


Figure 11. Transmitter Ready ($\overline{\text{TXRDY}}$), FCR0 = 1 and FCR3 = 1 (mode 1)

PARAMETER MEASUREMENT INFORMATION

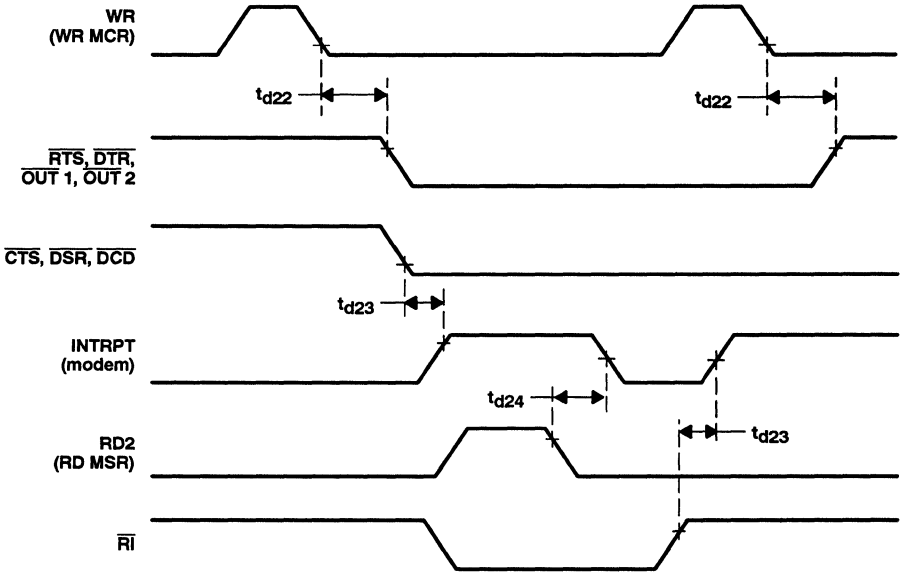


Figure 12. Modem Control Timing

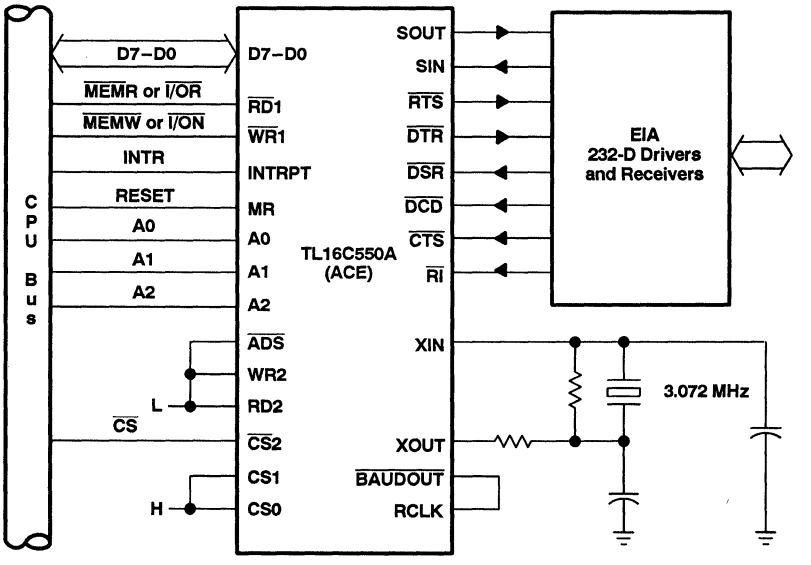


Figure 13. Basic TL16C550A Configuration

APPLICATION INFORMATION

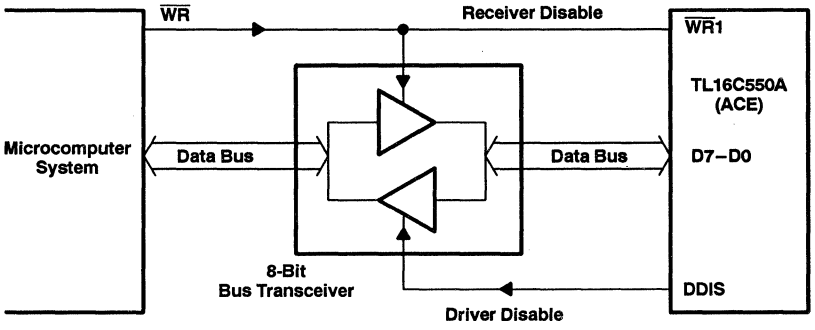


Figure 14. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION

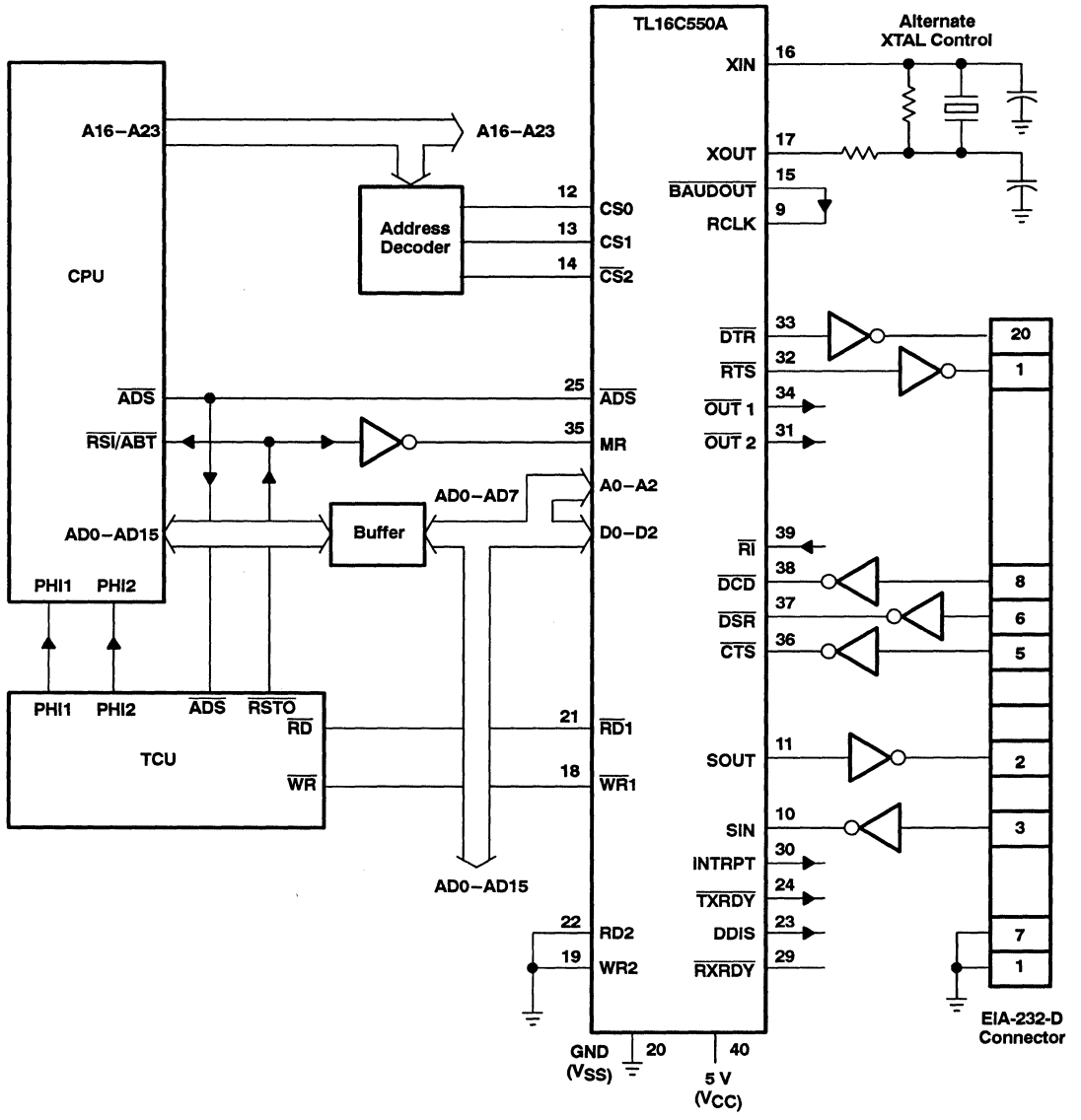


Figure 15. Typical TL16C550A Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	L	FIFO control (write)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. Ace Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high, bits 1–3 are low, and bits 4–7 are permanently low
FIFO Control Register	Master Reset	All bits low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low (5–7 permanent)
Line Status Register	Master Reset	Bits 5 and 6 are high, all other bits are low
Modem Status Register	Master Reset	Bits 0–3 are low, bits 4–7 are input signals
SOUT	Master Reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
Scratch Register	Master Reset	No effect
Divisor Latch (LSB and MSB) Registers	Master Reset	No effect
Receiver Buffer Registers	Master Reset	No effect
Transmitter Holding Registers	Master Reset	No effect
RCVR FIFO	MR/FCR1-FCR0/ ΔFCR0	All bits low
XMIT FIFO	MR/FCR2-FCR0/ ΔFCR0	All bits low

PRINCIPLES OF OPERATION

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0†	Data Bit 0	Enable Received Data Available Interrupt (ERB)	"0" if interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Transmitter FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 4)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 4)	Receiver Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 4)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 4)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
NOTE 4: These bits are always 0 in the TL16C450 mode.

PRINCIPLES OF OPERATION

receiver buffer register (RBR)

The ACEs receiver section consists of a receiver shift register (RSR) and a receiver buffer register (RBR). The RBR is actually a 16-byte FIFO. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACEs line control register.

The ACEs RSR receives serial data from the serial input (SIN) pin. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the receiver buffer register and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the receiver buffer register. in the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

transmitter holding register (THR)

The ACEs transmitter section consists of a transmitter holding register (THR) and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is suppled by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE's line control register.

The ACE THR receives data off the internal data bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the serial output (SOUT). In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

interrupt enable register (IER)

The Interrupt enable register enables each of the five types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table3 and are described below.

Bit 0. This bit, when set to logic 1, enables the received data available interrupt.

Bit 1. This bit, when set to logic 1, enables the transmitter holding register empty interrupt.

Bit 2. This bit, when set to logic 1, enables the receiver line status interrupt.

Bit 3.This bit, when set to logic 1, enables the modem status interrupt.

Bits 4 thru 7. Bits 4 through 7 in the interrupt enable register are not used and are always set to logic 0.

FIFO control register

The FIFO control register (FCR) is a write-only register at the same location as the IIR, which is a read-only register. The FCR is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

Bit 0. FCR0, when set to logic 1, enables the transmit and receive FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed. Changing this bit clears the FIFOs.

Bit 1. FCR1, when set to logic 1, clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.

Bit 2. FCR2, when set to logic 1, clears all bytes in the transmit FIFO and resets its counter to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.

Bit 3. If FCR0 is a 1, setting FCR3 to a 1 causes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from mode 0 to mode 1.

PRINCIPLES OF OPERATION

Bits 4 and 5. FCR4 and FCR5 are reserved for future use.

Bits 6 and 7. FCR6 and FCR7 are used to set the trigger level for the receiver FIFO interrupt.

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1–Receiver line status (highest priority)
Priority 2–Receiver data ready or receiver character timeout
Priority 3–Transmitter holding register empty
Priority 4–Modem status (lowest priority)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Detail on each bit are as follows:

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending, as indicated in Table 4.

Bit 3. This bit is always 0 in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt is pending.

Bits 4 thru 5. These two bits are not used and are always set at logic 0.

Bits 6 and 7. These two bits are always 0 in the TL16C450 mode. They are set when bit 0 of the FIFO control register is equal to 1.

PRINCIPLES OF OPERATION

Table 4. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	–
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrrupt	Reading the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode.	Reading the receiver buffer register
1	1	0	0	2	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time	Reading the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

PRINCIPLES OF OPERATION

Bit 2. This bit specifies either one, one and one-half, or two stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the data. If bit 2 is a logic 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receive clocks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in the following.

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

Bit 3. This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.

Bit 4. Bit 4 is the even parity select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces even parity (an even number of logic 1's in the data and parity bits) and a logic 0 in bit 4 produces odd parity (an odd number of logic 1's).

Bit 5. This is the stick parity bit. When bits 3, 4, and 5 are logic 1s, the parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1's and bit 4 is a logic 0, the parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0, stick parity is disabled.

Bit 6. This bit is the break control bit. Bit 6 is set to a logic 1 to force a break condition, i.e., a condition where the serial output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic; it only effects the serial output.

Bit 7. This bit is the divisor latch access bit (DLAB). Bit 7 must be set to a logic 1 to access the divisor latches of the baud generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

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modem control register (MCR)

The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the data terminal ready ($\overline{DTR}$) output. Setting this bit to a logic 1 forces the $\overline{DTR}$ output to its low state. When bit 0 is set to a logic 0, $\overline{DTR}$ goes high.

Bit 1. Bit 1 (RTS) controls the request to send ($\overline{RTS}$) output in a manner identical to Bit 0's control over the $\overline{DTR}$ output.

Bit 2. Bit 2 (OUT 1) controls the output 1 ($\overline{OUT}$ 1) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.

Bit 3. Bit 3 (OUT 2) controls the uutput 2 ($\overline{OUT}$ 2) signal, a user-designated output signal, in a manner identical to bit 0's control over the $\overline{DTR}$ output.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

1. The transmitter serial output (SOUT) is set high.
2. The receiver serial input (SIN) is disconnected.
3. The output of the transmitter shift register is looped back into the receiver shift register input.
4. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected.
5. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT}$ 1, and $\overline{OUT}$ 2) are internally connected to the four modem control inputs.
6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

Bit 5 through 7. These bits are permanently set to logic 0.

line status register (LSR)†

The line status register provides information to the CPU concerning the status of data transfers. The contents of this register are described below and summarized in Table 3.

Bit 0. Bit 0 is the data ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the receiver buffer register or the FIFO and is reset to logic 0 by reading all of the data in the receiver buffer register or the FIFO.

Bit 1‡. Bit 1 is the overrun error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the receiver buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the line status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten but is not transferred to the FIFO.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

Bit 2‡. Bit 2 is the parity error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the line control register (bit 4). The PE bit is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3‡. Bit 3 is the framing error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) stop bit. The FE bit is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE will try to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.

Bit 4‡. Bit 4 is the break interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and Stop bits. The B1 bit is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only on 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Bit 5. Bit 5 is the transmitter holding register empty (THRE) indicator. This bit is set to logic 1 when the transmitter holding register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the transmitter holding register are transferred to the transmitted shift register. This bit is reset to logic 0 concurrent with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

Bit 6. Bit 6 is the transmitter empty (TEMT) indicator. This bit is set to a logic 1 when the transmitter holding register and the transmitter shift register are both empty. When either the transmitter holding register or the transmitter shift register contains a data character, the TEMT bit is reset to logic 0. In the FIFO mode, this bit is set to a 1 when the transmitter FIFO and shift register are both empty.

Bit 7. In the TL16C550A, this bit is always reset to logic 0. In the TL16C450 mode, this bit is always a 0. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

modem status register (MSR)

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state, the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the modem status register. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 is the change in clear to send (DCTS) indicator. This bit indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU . When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

‡ Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

Bit 1. Bit 1 is the change in data set ready (DDSR) indicator. This bit indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

Bit 2. Bit 2 is the trailing edge of ring indicator (TERI) detector. This bit indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

Bit 3. Bit 3 is the change in data carrier detect (DDCD) indicator. This bit indicates that the $\overline{DCD}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

Bit 4. Bit 4 is the compliment of the clear to send ($\overline{CTS}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 1 (RTS).

Bit 5. Bit 5 is the compliment of the data set ready ($\overline{DSR}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control register bit 1 (DTR).

Bit 6. Bit 6 is the compliment of the ring indicator ($\overline{RI}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the compliment of the data carrier detect ($\overline{DCD}$) input. If bit 4 (loop) of the modem control register is set to a logic 1, this bit is equivalent to the modem control registers bit 3 (OUT 2).

scratch register (SCR)

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the baud generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = XIN frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called divisor latches, are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 5 and 6, which follow, illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

PRINCIPLES OF OPERATION

FIFO interrupt-mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupts will occur as follows:

1. The receive data available interrupt will be issued to the microprocessor when the FIFO has reached its programmed trigger level. It will be cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts will occur as follows:

1. FIFO timeout interrupt will occur if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed, the second one is included in this time delay).
   c. The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago. This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.
4. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts will occur as follows:

1. The transmitter holding register interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmit FIFO empty indications will be delayed 1 character time minus the last stop bit time when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt; transmit FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO polled-mode operation

With FCR0 = 1, resetting IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

PRINCIPLES OF OPERATION

FIFO polled-mode operation (continued)

In this mode, the user program will check receiver and transmitter status via the LSR. As stated previously:

1. LSR0 will be set as long as there is one byte in the receiver FIFO.
2. LSR1 through LSR4 will specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2 = 0.
3. LSR5 will indicate when the transmit FIFO is empty.
4. LSR6 will indicate that both the transmit FIFO and shift registers are empty.
5. LSR7 will indicate whether there are any errors in the receiver FIFO.

There is no trigger level reached or timeout conditions indicated in the FIFO polled mode. However, the receiver and transmit FIFO,s are still fully capable of holding characters.

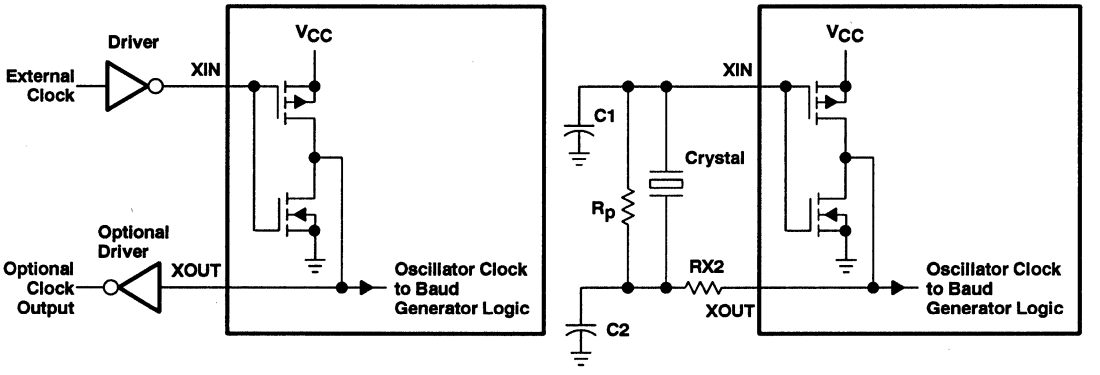
Table 5. Baud Rates Using A 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

PRINCIPLES OF OPERATION

Table 6. Baud Rates Using A 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	



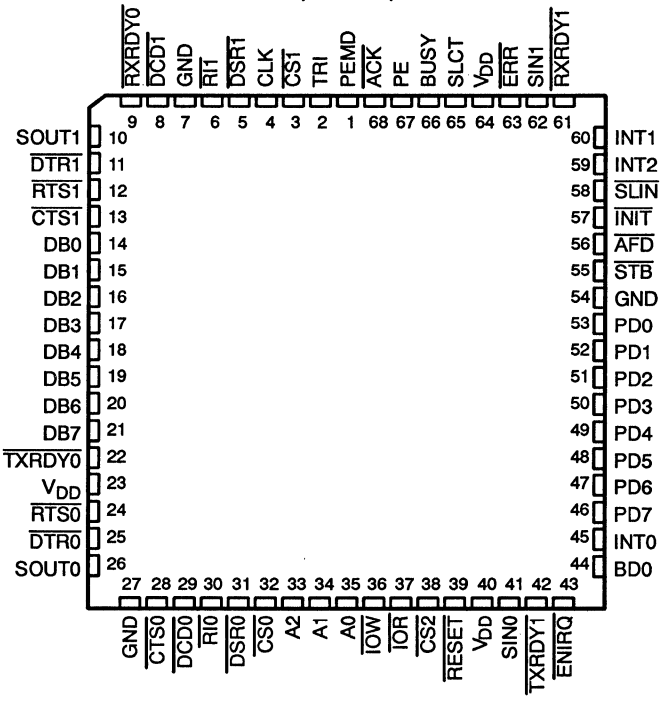
TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	Rp	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 16. Typical Clock Circuits

- **IBM PC/AT Compatible**
- **Two TL16C550 ACEs**
- **Enhanced Bidirectional Line Printer Port**
- **16-Byte FIFOs Reduce CPU Interrupts**
- **Independent Control of Transmit, Receive, Line Status, and Data Set Interrupts on Each Channel**
- **Individual Modem Control Signals for Each Channel**
- **Programmable Serial Interface Characteristics for Each Channel:**
  5-, 6-, 7-, or 8-bit Characters
  Even-, Odd-, or No-Parity Bit Generation and Detection
  1-, 1 1/2-, or 2-Stop Bit Generation
- **3-State TTL Drive for the Data and Control Bus on Each Channel**
- **Hardware and Software Compatible With TL16C452**

FN PACKAGE
(TOP VIEW)



description

The TL16C552 is an enhanced dual-channel version of the popular TL16C550 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions.

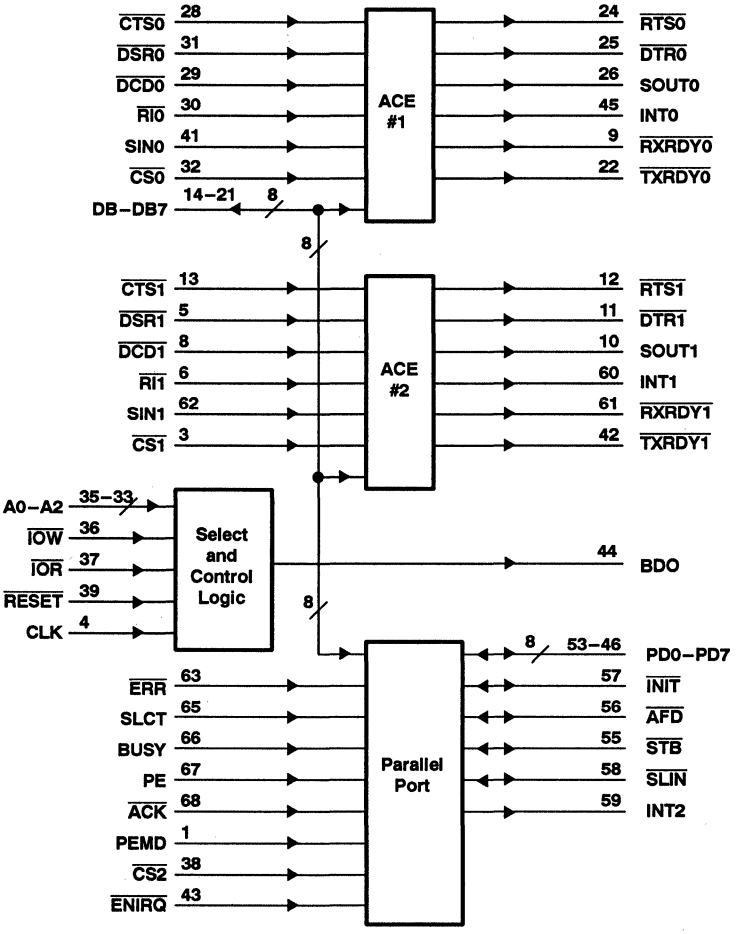
description (continued)

In addition to its dual communications interface capabilities, the TL16C552 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics-type printer. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16} - 1)$.

The TL16C552 is housed in a 68-pin plastic leaded chip carrier.

functional block diagram



TEXAS INSTRUMENTS
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Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{ACK}$	68	I	Line printer acknowledge. This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line printer autofeed. This open-drain line provides the line printer with an active-low signal when continuous form paper is to be autofed to the printer. This pin has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	I	Address lines A0–A2. The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels and Table 11 for the decode of the parallel line printer port.
BDO	44	O	Bus buffer output. This active-high output is asserted when either serial channel or the parallel port is read. This output can be used to control the system bus driver (74LS245).
BUSY	66	I	Line printer busy. This is an input line from the line printer that goes high when the line printer is not ready to accept data.
CLK	4	I	Clock input. The external clock input to the baud rate divisor of each ACE.
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	32, 3, 38	I	Chip selects. Each input acts as an enable for the write and read signals for the serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enables the signals to the line printer port.
$\overline{CTS0}$, $\overline{CTS1}$	28, 13	I	Clear to send inputs. The logical state of each $\overline{CTS}$ pin is reflected in the CTS bit of the (MSR) modem status register (CTS is bit 4 of the MSR, written MSR (4)) of each ACE. A change of state in either $\overline{CTS}$ pin since the previous reading of the associated MSR causes the setting of DCTS (MSR(0)) of each modem status register.
DB0-DB7	14-21	I/O	Data bits DB0–DB7. The data bus provides eight three-state I/O lines for the transfer of data, control, and status information between the TL16C552 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{DCD0}$, $\overline{DCD1}$	29, 8	I	Data carrier detect. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the modem status registers. MSR(3) (DDCD) of the modem status register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver.
$\overline{DSR0}$, $\overline{DSR1}$	31, 5	I	Data set ready inputs. The logical state of the DSR pins is reflected in MSR(5) of its associated modem status register. DDSR (MSR(1)) indicates whether the associated DSR pin has changed state since the previous reading of the MSR.
$\overline{DTR0}$, $\overline{DTR1}$	25, 11	O	Data terminal ready lines. Each DTR pin can be set (low) by writing a logic 1 to MCR(0), modem control register bit 0 of its associated ACE. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR(0)) or whenever a reset occurs. When active (low), the DTR pin indicates that its ACE is ready to receive data.
$\overline{ENIRQ}$	43	I	Parallel port interrupt source mode selection. When low, the AT mode of interrupts is enabled. In this mode, the INT2 output is internally connected to the $\overline{ACK}$ input. If the $\overline{ENIRQ}$ input is tied high, the INT2 output is internally tied to the $\overline{PRINT}$ signal in the line printer status register. INT2 is latched high on rising edge of $\overline{ACK}$.
$\overline{ERR}$	63	I	Line printer error. This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
GND	7, 27, 54		Ground (0 V). All pins must be tied to ground for proper operation.
$\overline{INIT}$	57	I/O	Line printer intialize. This open-drain line provides the line printer with an active-low signal that allows the line printer initialization routine to be started. This pin has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
$\overline{IOR}$	37	I	Input/output read strobe. This is an active-low input that enables the selected channel to output data to the data bus (DB0–DB7). The data output depends upon the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the line printer port.
$\overline{IOW}$	36	I	Input/output write strobe. This is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends upon the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.

Terminal Functions (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
INT0, INT1	45, 60	O	Serial channel interrupts. Each 3-state serial channel interrupt output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt enable register of its associated channel: receiver error flag, received data available, transmitter holding register empty, and modem status. The interrupt is reset low upon appropriate service. Upon reset, the interrupt output will be in the high-impedance state.
INT2	59	O	Printer port interrupt. This signal is an active-high, three-state output, generated by the positive transition of $\overline{ACK}$. It is enabled by bit 4 of the write control register. Upon a reset, the interrupt output will be in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). These eight lines provide a byte-wide input or output port to the system.
PE	67	I	Line printer paper empty. This is an input line from the line printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer enhancement mode. When low, this signal enables the write data register to the PD0–PD7 lines. A high on this signal allows direction control of the PD0–7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	I	Reset. When low, the reset input forces the TL16C552 into an idle mode in which all serial data activities are suspended. The modem control register (MCR) along with its associated outputs are cleared. The line status register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. This input has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	O	Request to send outputs. An $\overline{RTS}$ pin is set low by writing a logic 1 to MCR(1) bit 1 of its UARTs modem control register. Both $\overline{RTS}$ pins are reset high by $\overline{RESET}$. A low on the $\overline{RTS}$ pin indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{RTS}$ is used to control the direction of the line.
$\overline{RXRDY0}$, $\overline{RXRDY1}$	9, 61	O	Receiver ready. Receiver DMA signaling is also available through this pin. One of two types of DMA signaling can be selected via FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the RCVR FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDY}$ will be active (low) when in the FIFO mode (FCR0=1, FCR3=0) or when in the TL16C450 mode (FCR0=0) and the RCVR FIFO or RCVR holding register contain at least one character. When there are no more characters in the FIFO or holding register, the $\overline{RXRDY}$ pin will go inactive (high). Mode 1. $\overline{RXRDY}$ will go active (low) in the FIFO mode (FCR0=1) when FCR3=1 and the timeout or trigger levels have been reached. It will go inactive (high) when the FIFO or holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	I	Ring indicator inputs. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each ACE. The modem status register output TERI (MSR(2)) indicates whether the $\overline{RI}$ input has changed from high to low since the previous reading of the MSR.
SIN0, SIN1	41, 62	I	Serial data inputs. The serial data inputs move information from the communication line or modem to the TL16C552 receiver circuits. A mark (1) is high and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
SLCT	65	I	Line printer selected. This is an input line from the line printer that goes high when the line printer has been selected.
$\overline{SLIN}$	58	I/O	Line printer select. This open-drain selects the printer when it is active (low). This pin has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
SOUT0, SOUT1	26, 10	O	Serial data outputs. These lines are the serial data outputs from the ACEs transmitter circuitry. A mark is a logic 1 (high) and a space is a logic 0 (low). Each SOUT is held in the mark condition when the transmitter is disabled, $\overline{RESET}$ is true (low), the transmitter register is empty, or when in the loop mode.
$\overline{STB}$	55	I/O	Line printer strobe. This open-drain line provides communication between the TL16C552 and the line printer. When it is active (low), it provides the line priner with a signal to latch the data currently on the parallel port. This pin has an internal pullup resistor to V_{DD} of approximately 10 kΩ.

Terminal Functions (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
TRI	2	I	3-state control. This pin is used to control the 3-state control of all I/O and output pins. When this pin is asserted, all I/O and outputs become high impedance, allowing board level testers to drive the outputs without overdriving internal buffers. This pin is level sensitive. This pin is pulled down with an internal resistor that is approximately 5 kΩ and is a CMOS input.
$\overline{\text{TXRDY0}}$, $\overline{\text{TXRDY1}}$	22, 42	O	Transmitter ready. Two types of DMA signaling are available. Either can be selected via FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiply transfers that are made continuously until the XMIT FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR0=1, FCR3=0) or in the TL16C450 mode (FCR0=0) and there are no characters in the XMIT holding register or XMIT FIFO, $\overline{\text{TXRDY}}$ will be active (low). Once $\overline{\text{TXRDY}}$ is activated (low), it will go inactive after the first character is loaded into the holding register of XMIT FIFO. Mode 1. $\overline{\text{TXRDY}}$ will go active (low) if in the FIFO mode (FCR0=1) when FCR3=1 and there are no characters in the XMIT FIFO. When the XMIT FIFO is completely full, $\overline{\text{TXRDY}}$ will go inactive (high).
V_{DD}	23, 40, 64		Power supply. The power supply requirement is 5 V ±5%.

detailed description

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations are shown in the table below for the registers.

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line-control register (bit 7) to select the register to be written or read (see Table 1).

Table 1. Serial Channel Internal Registers

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver buffer register (read only)
L	L	L	L	THR	Transmitter holding register (write only)
L	L	L	H	IER	Interrupt enable register
X	L	H	L	IIR	Interrupt identification register (read only)
X	L	H	L	FCR	FIFO control register (write only)
X	L	H	H	LCR	Line control register
X	H	L	L	MCR	Modem control register
X	H	L	H	LSR	Line status register
X	H	H	L	MSR	Modem status register
X	H	H	H	SCR	Scratch register
H	L	L	L	DLL	Divisor latch (LSB)
H	L	L	H	DLM	Divisor latch (MSB)

X = irrelevant, L = low level, H = high level
NOTE: The serial channel is accessed when either $\overline{\text{CS0}}$ or $\overline{\text{CS1}}$ is low.

detailed description (continued)

Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR (7) refers to line control register bit 7.

The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered so that read and write operations may be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

line-control register

The format of the data character is controlled by the line-control register. The LCR may be read. Its contents are described below and shown in Figure 1.

LCR(0) and LCR(1) word length select bit 1:

The number of bits in each serial character is programmed as shown in Figure 1.

LCR(2) stop bit select bit 2:

LCR(2) specifies the number of stop bits in each transmitted character as shown in Figure 1. The receiver always checks for one stop bit.

LCR(3) parity enable bit 3:

When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) even parity select bit 4:

When enabled, a logic one selects even parity.

LCR(5) stick parity bit 5:

When parity is enabled (LCR(3)=1), LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR(4). This forces parity to a known state and allows the receiver to check the parity bit in a known state.

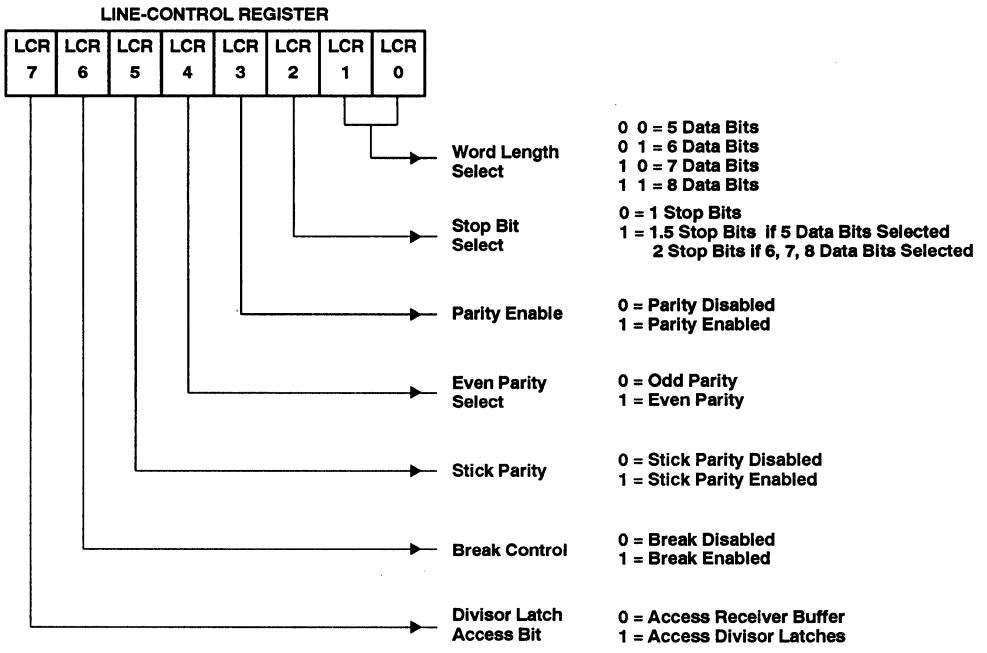


Figure 1. Line Control Register Contents

line-control register (continued)

LCR(6) break control bit 6:

When LCR(6) is set to a logic 1, the serial output (SOUT1/SOUT0) is forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. If the following sequence is used, no invalid characters will be transmitted because of the break:

Step 1 Load a zero byte in response to the transmitter holding register empty (THRE) status indication.

Step 2 Set the break in response to the next THRE status indication.

Step 3 Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT=1). Then clear the break when the normal transmission has to be restored.

LCR(7) divisor latch access bit (DLAB) bit 7:

Bit 7 must be set high (logic 1) to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR(7) must be input low (logic 0) to access the receiver buffer register, the transmitter holding register or the interrupt enable register.

line status register

The line status register (LSR) is a single register that provides status indications. The line status register shown in Table 2 is described below:

LSR(0) data ready (DR) bit 0:

Data ready is set high when an incoming character has been received and transferred into the receiver buffer register or the FIFO. LSR(0) is reset low by a CPU read of the data in the receiver buffer register or the FIFO.

LSR(1) overrun error (OE) bit 1:

Overrun error indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the line status register. An overrun error will occur in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO but it is overwritten.

LSR(2) parity error (PE) bit 2:

Parity error indicates that the received data character does not have the correct parity as selected by LCR(3) and LCR(4). The PE bit is set high upon detection of a parity error and is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR(2) reflects the error when the character is at the top of the FIFO.

LSR(3) framing error (FE) bit 3:

Framing error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR(3) reflects the error when the character is at the top of the FIFO.

Table 2. Line Status Register Bits

LSR BITS	1	0
LSR(0) data ready (DR)	Ready	Not ready
LSR(1) overrun error (OE)	Error	No error
LSR(2) parity error (PE)	Error	No error
LSR(3) framing error (FE)	Error	No error
LSR(4) break interrupt (BI)	Break	No break
LSR(5) transmitter holding register empty (THRE)	Empty	Not empty
LSR(6) transmitter empty (TEMT)	Empty	Not empty
LSR(7) RCVR FIFO error	Error in FIFO	No error in FIFO

LSR(4) break interrupt (BI) bit 4:

Break interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the line status register. In the FIFO mode, this is associated with a particular character in the FIFO. LSR(2) reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR(1) – LSR(4) are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the interrupt enable register.

line status register (continued)

LSR(5) transmitter holding register empty (THRE) bit 5:

THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the transmitter holding register into the transmitter shift register. LSR(5) is reset low by the loading of the transmitter holding register by the CPU. LSR(5) is not reset by a CPU read of the LSR. In the FIFO mode when the XMIT FIFO is empty, this bit is set. It is cleared when one byte is written to the XMIT FIFO. When the THRE interrupt is enabled by IER(1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) transmitter empty (TEMT) bit 6:

TEMT is set high when the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set to one.

LSR(7) RCVR FIFO error bit 7:

The LSR(7) bit is always 0 in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break interrupt indication. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE: The line status register may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

FIFO-control register

This write-only register is at the same location as the IIR. It is used to enable and clear the FIFOs, set the trigger level of the RCVR FIFO, and select the type of DMA signaling.

FCR(0) enables both the XMIT and RCVR FIFOs. All bytes in both FIFOs can be cleared by resetting FCR(0). Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR(0) = 1.

FCR(1) = 1 clears all bytes in the RCVR FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR(2) = 1 clears all bytes in the XMIT FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR(3) = 1 will change the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ pins from mode 0 to mode 1 if FCR(0) = 1.

FCR(4) – FCR(5): These two bits are reserved for future use.

FCR(6) – FCR(7): These two bits are used for setting the trigger level for the RCVR FIFO interrupt as follows:

BIT		RCVR FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

modem-control register

The modem-control register (MCR) controls the interface with the modem or data set as described in Figure 2. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

MCR(0): When MCR(0) is set high, the $\overline{DTR}$ output is forced low. When MCR(0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the $\overline{RTS}$ output is forced low. When MCR(1) is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver to obtain the proper polarity input at the modem or data set.

MCR(2): When MCR(2) is set high, $\overline{OUT1}$ is forced low.

MCR(3): When MCR(3) is set high, the $\overline{OUT2}$ output is forced low.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, serial output (SOUT) is set to the marking (logic 1) state, and the receiver data input serial input (SIN) is disconnected. The output of the transmitter shift register is looped back into the receiver shift register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem-control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OIUT1}$, and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem-control output pins are forced to their inactive state (high) on the TL16C552. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational. However, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external pins represented by those four bits.

MCR(5) – MCR(7) are permanently set to logic 0.

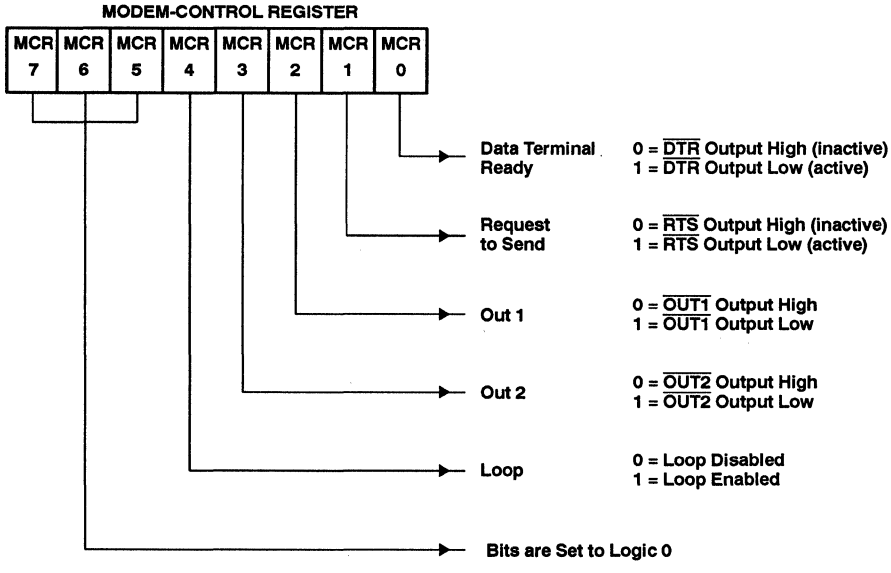


Figure 2. Modem-Control Register Contents

modem-status register

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state and reset low when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$. MSR(4) – MSR(7) are status indications of these lines. A status bit = 1 indicates the input is a low. A status bit = 0 indicates the input is high. If the modem-status interrupt in the interrupt enable register is enabled (IER(3)), an interrupt is generated whenever MSR(0) – MSR(3) is set to a one. The MSR is a priority 4 interrupt. The contents of the modem-status register are described in Table 3.

MSR(0) delta clear to send (DCTS) bit 0:

DCTS displays that the $\overline{CTS}$ input to the serial channel has changed state since it was last read by the CPU.

MSR(1) delta data set ready (DDSR) bit 1:

DDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) trailing edge of ring indicator (TERI) bit 2:

TERI indicates that the $\overline{RI}$ input to the serial channel has changed state from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.

MSR(3) delta data carrier detect (DDCD) bit 3:

DDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) clear to send (CTS) bit 4:

CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in the loop mode ((MCR(4)=1), MSR(4) reflects the value of RTS in the MCR.

MSR(5) data set ready (DSR) bit 5:

DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode (MCR(4)=1), MSR(5) reflects the value of DTR in the MCR.

Table 3. Modem-Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR(0)	DCTS	Delta clear to send
MSR(1)	DDSR	Delta data set ready
MSR(2)	TERI	Trailing edge of ring indicator
MSR(3)	DDCD	Delta data-carrier detect
MSR(4)	$\overline{CTS}$	Clear to send
MSR(5)	$\overline{DSR}$	Data set ready
MSR(6)	$\overline{RI}$	Ring indicator
MSR(7)	$\overline{DCD}$	Data-carrier detect

modem-status register (continued)

MSR(6) ring indicator (RI) bit 6:

RI is the complement of the $\overline{RI}$ input. If the channel is in the loop mode (MCR(4)=1), MSR(6) reflects the value of $\overline{OUT1}$ in the MCR.

MSR(7) data carrier detect (DCD) bit 7:

Data carrier detect indicates the status of the data carrier detect ($\overline{DCD}$) input. If the channel is in the loop mode (MCR(4)=1), MSR(7) reflects the value of OUT2 in the MCR.

Reading the MSR register clears the delta modem status indications but has no effect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read instead of being set again. In the loop-back mode, when modem status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input pins are ignored. However, a modem-status interrupt may still be generated by writing to MCR3–MCR0. Applications software should not write to the modem-status register.

divisor latches

The ACE serial channel contains a programmable baud-rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the baud generator is 16X the data rate (divisor # = clock ÷ (baud rate x 16)) referred to in this document as RCLK. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512K bps are available. Tables 5, 6, and 7 illustrate the divisors needed to obtain standard rates using these three frequencies.

scratchpad register

The scratchpad register is an 8-bit read/write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

interrupt identification register

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver line status (priority 1)
2. Received data ready (priority 2) or character timeout
3. Transmitter holding register empty (priority 3)
4. Modem status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt identification register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 4.

Table 4. Interupt Identification Register

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character timeout indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	MSR read

interrupt identification register (continued)

IIR(0) can be used to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 4.

IIR(3): This bit is always logic 0 when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.

IIR(4) – IIR(5): These two bits are always set to logic 0.

IIR(6) – IIR(7): FCR(0)=1 sets these two bits.

interrupt enable register

The interrupt enable register (IER) is used to independently enable the four serial channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by resetting IER(0) – IER(3) of the interrupt enable register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the interrupt identification register and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are described in Table 9 and below.

IER(0). When set to one, IER(0) enables the received data available interrupt and the timeout interrupts in the FIFO mode.

IER(1). When set to one, IER(1) enables the transmitter holding register empty interrupt.

IER(2). When set to one IER(2) enables the receiver line status interrupt.

IER(3). When set to one, IER(3) enables the modem status interrupt.

IER(4) – IER(7). These four bits of the IER are logic 0.

receiver

Serial asynchronous data is input into the SIN pin. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The line-control register determines the number of data bits in a character [LCR(0), LCR(1)]. If parity is used LCR(3) and the polarity of parity LCR(4) are needed. Status for the receiver is provided in the line status register. When a full character is received, including parity and stop bits, the data received indication in LSR(0) is set high. The CPU reads the receiver buffer register, which resets LSR(0). If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). If there is a parity error, the parity error is set in LSR(2). If a stop bit is not detected, a framing error indication is set in LSR(3).

If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

1. Intializes the transmitter and receiver clock counters.
2. Clears the line status register (LSR), except for transmitter shift register empty (TEMT) and transmit holding register empty (THRE), which are set. The modem control register (MCR) is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The line control register (LCR), divisor latches, receiver buffer register, and transmitter buffer register are not affected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in the idle mode until programmed.

A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the ACE is given in Table 8.

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

FIFO-interrupt-mode operation

The following RCVR status occurs when the RCVR FIFO and receiver interrupts are enabled:

1. LSR(0) is set when a character is transferred from the shift register to the RCVR FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver line status interrupt has higher priority than the received data available interrupt IIR = 04.
3. Receive data available interrupt will be issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it will be cleared.
4. IIR = 04 (receive data available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following RCVR FIFO character timeout status occurs when RCVR FIFO and receiver interrupts are enabled.

1. If the following conditions exist, a FIFO character timeout interrupt occurs.

   Minimum of one character in FIFO

   Last received serial character was longer than 4 continuous previous character times ago (if two stop bits are programmed, the second one is included in the time delay).

   The last CPU read of the FIFO was more than 4 continuous character times earlier. At 300 baud and 12-bit characters, the FIFO timeout interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. (The delay is proportional to the baud rate.)
3. The timeout timer is reset after the CPU reads the RCVR FIFO or after a new character is received, when there has been no timeout interrupt.
4. A timeout interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

XMIT interrupts occur as follows when the transmitter and XMIT FIFO interrupts are enabled (FCRO = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02) occurs. The interrupt is cleared as soon as the transmitter holding register is written to or the IIR is read. One to sixteen characters may be written to the transmit FIFO when servicing this interrupt.
2. The XMIT FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following occurs:

   THRE = 1 and there has not been a minimum of two bytes at the same time in XMIT FIFO, since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be immediate, however, assuming it is enabled.

RCVR FIFO trigger level and character timeout interrupts have the same priority as the received data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Resetting IER0, IER1, IER2, IER3, or all to zero, with FCR0 = 1, puts the ACE into the FIFO polled mode. RCVR and XMITER are controlled separately. Therefore, either or both can be in the polled mode.

In the FIFO polled mode, there is no timeout condition indicated or trigger level reached. However, the RCVR and XMIT FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

Table 5. Baud Rates (1.8432-MHz clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 6. Baud Rates (3.072-MHz clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

Table 7. Baud Rates (8.192-MHz clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	1000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

Table 8. $\overline{\text{RESET}}$

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt enable register	Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt identification register	Reset	Bit 0 is high, bits 1, 2, 3, 6, and 7 low Bits 4–5 are permanently low
Line control register	Reset	All bits low
Modem control register	Reset	All bits low
FIFO control register	Reset	All bits low
Line status register	Reset	All bits low, except bits 5 and 6 are high
Modem status register	Reset	Bits 0–3 low, bits 4–7 input signal
SOUT	Reset	High
Interrupt (RCVR errs)	Read LSR/Reset	Low
Interrupt (RCVR data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

Table 9. Serial Channel Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBFI) Enable received data available interrupt
2	FCR (write only)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit (2)‡	Interrupt ID Bit (1)	Interrupt ID Bit (0)	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in RCVR FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(DDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(DDSR) Delta data set ready	(DCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

parallel port registers

The TL16C552's parallel port can be used to interface the device to a Centronics-style printer. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) pin as shown. The read data register allows the microprocessor to read the information on the parallel bus.

The read status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy $\overline{BSY}$, acknowledge ($\overline{ACK}$) which is a handshake function, paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$) and printer interrupt ($\overline{PRINT}$). The read control register allows the state of the control lines to be read. The write control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM serial parallel adaptor.

Table 10. Parallel Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read Control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 11. Parallel Port Register Select

CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

line printer port

The line printer port contains the functionality of the port included in the TL16C452, but offers a hardware programmable extended mode controlled by the printer enhancement mode (PEMD) pin. This enhancement is the addition of a direction control bit, and an interrupt status bit.

register 0 line printer data register

The line printer (LPD) port is either output only or bidirectional, depending on the state of the extended mode pin and data direction control bits.

Compatibility mode (PEMD pin = 0)

Reads to the LPD register return the last data that was written to the port. Write operations immediately output data to the PD0–PD7 pins.

Extended mode (PEMD pin = 1)

Read operations return either the data last written to the LPT data register if the direction bit is set to write (low), or the data that is present on PD0–PD7 if the direction is set to read (high). Writes to the LPD register latch data into the output register, but only drive the LPT port when the direction bit is set to write (low).

The table below summarizes the possible combinations of extended mode and the direction-control bit. In either case, the bits of the LPD register are defined as follows:

PEMD	DIR	PD0–PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2 mode – output
H	1	PS/2 mode – input

register 1 read line printer status register

The line printer status (LPS) register is a read-only register that contains interrupt and printer status of the LPT connector pins. In the table below (in the default column), are the values of each bit after reset in the case of the printer being disconnected from the port. The bits are described as follows:

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

Bits 0 and 1 – Reserved. Read as ones.

Bit 2 – Printer interrupt ($\overline{\text{PRINT}}$, active low) status bit. When set (low) indicates that the printer has acknowledged the previous transfer with an ACK handshake (bit if 4 of the control register is set to 1). The bit is set to zero on the active to inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set to a one after a read of the status port.

Bit 3 – Error ($\overline{\text{ERR}}$, active low) status bit corresponds to $\overline{\text{ERR}}$ input.

Bit 4 – Select (SLCT) status bit corresponds to SLCT input.

Bit 5 – Paper empty (PE) status bit corresponds to PE input.

Bit 6 – Acknowledge ($\overline{\text{ACK}}$, active low) status bit corresponds to $\overline{\text{ACK}}$ input.

Bit 7 – Busy ($\overline{\text{BSY}}$, active low) status bit corresponds to BUSY input (active high).

register 2 line-printer-control register

The line-printer-control (LPC) register is read/write port that is used to control the PD0–PD7 direction and drive the printer-control lines. Write operations set or reset these bits, while read operations return the state of the last write operation to this register. The bits in this register are defined as follows:

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved (0)
7	Reserved (0)

Bit 0 – Printer strobe (STB) control bit; when 1, the $\overline{\text{STB}}$ signal is asserted on the LPT interface; when 0, the signal is negated.

Bit 1 – Auto feed (AFD) control bit; when 1, the $\overline{\text{AFD}}$ signal will be asserted on the LPT interface; when 0, the signal is negated.

Bit 2 – Initialize printer ($\overline{\text{INIT}}$) control bit; when 1, the $\overline{\text{INIT}}$ signal is negated; when 0, the $\overline{\text{INIT}}$ signal is asserted on the LPT interface.

register 2 line-printer-control register (continued)

Bit 3 – Select input (SLIN) control bit; when 1, the SLCT signal is asserted on the LPT interface; when 0, the signal is negated.

Bit 4 – Interrupt request enable (INT2 EN) control bit; when 1, enables interrupts from the LPT port whenever the $\overline{ACK}$ signal is released; when 0, disables interrupts and places INT2 signal in 3-state.

Bit 5 – Direction (DIR) control bit (only used when PEMD is high); when 1, the output buffers in the LPD port are disabled allowing data driven from external sources to be read from the LPD port. When DIR is low, the LPD port is in output mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation ..... 500 mW
Operating free-air temperature range ..... −10°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to ground (V_{SS}).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$	2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			8	MHz
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA for DB0–DB7, I_{OH} = −2 mA for PD0–PD7, I_{OH} = −0.4 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OH} = −0.4 mA for all other outputs	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA for DB0–DB7, I_{OL} = 12 mA for PD0–PD7, I_{OL} = 10 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OL} = 2 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V, All other pins are floating		±10	μA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	μA
I_{OZ}	Off-state output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected, or V_O = 5.25 V with chip and write mode selected		±20	μA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, SIN0, SIN1, $\overline{DSR0}$, $\overline{DSR1}$, $\overline{DCD0}$, $\overline{DCD1}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{RI0}$ and $\overline{RI1}$ at 2 V, Other inputs at 0.8 V, Baud rate generator f_{clock} = 8 MHz, Baud rate = 56 kb/s		50	mA

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK high (external clock, 8 MHz max) (see Figure 3)	55		ns
t_{w2}	Pulse duration, CLK low (external clock, 8 MHz max) (see Figure 3)	55		ns
t_{w3}	Pulse duration, master reset (see Figure 18)	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 6)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	80		ns
t_{su1}	Setup time, chip select valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{h2}	Hold time, chip select valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 4)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	80		ns

NOTES: 2. These four pins contain an internal pullup resistor to V_{DD} of approximately 10 kΩ.
3. The internal address strobe is always active.
4. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (IIR and LSR).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 7)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ low	80		ns
t_{su4}	Setup time, chip select valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su6}	Setup time, D0–D7 valid before $\overline{IOW}$ high	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h4}	Hold time, chip select valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h5}	Hold time, D0–D7 valid after $\overline{IOW}$ high	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ high to $\overline{IOW}$ or $\overline{IOR}$ low	80		ns

NOTE 3: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 6)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ high to BD0 high or from $\overline{IOR}$ low to BD0 low	C_L = 100 pF, See Note 5		60	ns
t_{en}	Enable time from $\overline{IOR}$ low to D0–D7 valid	C_L = 100 pF, See Note 5		60	ns
t_{dis}	Disable time from $\overline{IOR}$ high to D0–D7 released	C_L = 100 pF, See Note 5	0	60	ns

NOTE 5: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 8, 9, and 10)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE low to SOUT low at start		8	24	RCLK cycles
t_{d6}	Delay time, SOUT low at start to interrupt THRE high	See Note 6	8	8	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) high to interrupt THRE high	See Note 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT low at start to $\overline{TXRDY}$ low	C_L = 100 pF		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) low to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd4}	Propagation delay time from $\overline{IOR}$ (RD IIR) high to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd5}	Propagation delay time from $\overline{IOW}$ (WR THR) high to $\overline{TXRDY}$ high	C_L = 100 pF		195	ns

NOTE 6: If the transmitter interrupt delay is active, this delay will be lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 11, 12, 13, 14 and 15)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT high	See Note 7		1	RCLK cycle
t_{pd6}	Propagation delay time from RCLK high to sample CLK high			100	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) high to reset interrupt low	C_L = 100 pF		150	ns
t_{pd8}	Propagation delay time from $\overline{IOR}$ (RD RBR) low to $\overline{RXRDY}$ high			150	ns

NOTE 7: The receiver data available indication, the overrun error indication, the trigger level interrupts and the active $\overline{RXRDY}$ indication will be delayed three RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) will be delayed three RCLK cycles. These indicators will be updated immediately for any further bytes received after RDRBR goes active. There are eight RCLK cycle delays for trigger change level interrupts.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 16)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd9}	Propagation delay time from $\overline{IOW}$ (WR MCR) high to $\overline{RTS}$ ($\overline{DTR}$) low/high	C_L = 100 pF		100	ns
t_{pd10}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) low/high to interrupt high	C_L = 100 pF		170	ns
t_{pd11}	Propagation delay time from $\overline{IOR}$ (RD MSR) high to interrupt low	C_L = 100 pF		140	ns
t_{pd12}	Propagation delay time from $\overline{RI}$ high to interrupt high	C_L = 100 pF		170	ns

parallel port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 17)

		MIN	MAX	UNIT
t_{s07}	Setup time, data valid before $\overline{STB}$ low	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ high	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ low	1	500	µs
t_{d10}	Delay time, BUSY high to $\overline{ACK}$ low	Defined by printer		
t_{d11}	Delay time, BUSY low to $\overline{ACK}$ low	Defined by printer		
t_{w6}	Pulse duration, $\overline{ACK}$ low	Defined by printer		
t_{w7}	Pulse duration, BUSY high	Defined by printer		
t_{d12}	Delay time, BUSY high after $\overline{STB}$ high	Defined by printer		

PARAMETER MEASUREMENT INFORMATION

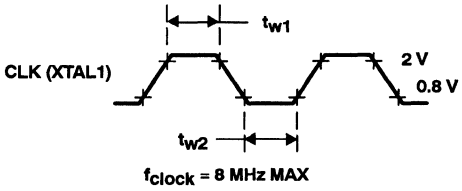
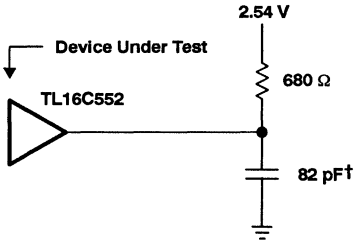


Figure 3. Clock Input (CLK) Voltage Waveform



†Includes scope and jig capacitance

Figure 4. Output Load Circuit

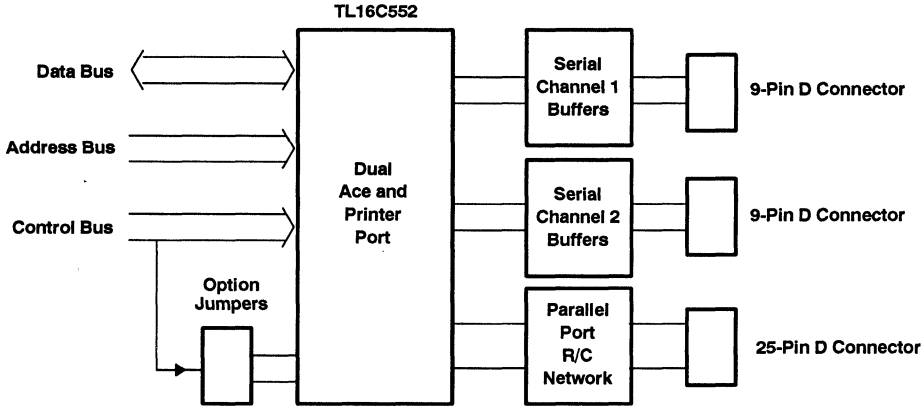


Figure 5. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

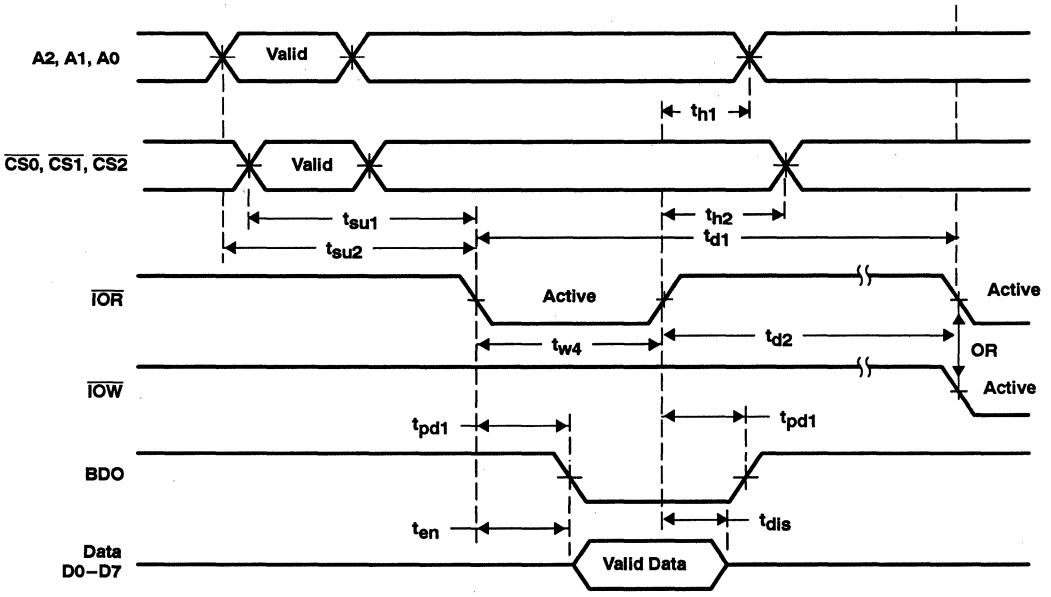


Figure 6. Read Cycle Timing Waveforms

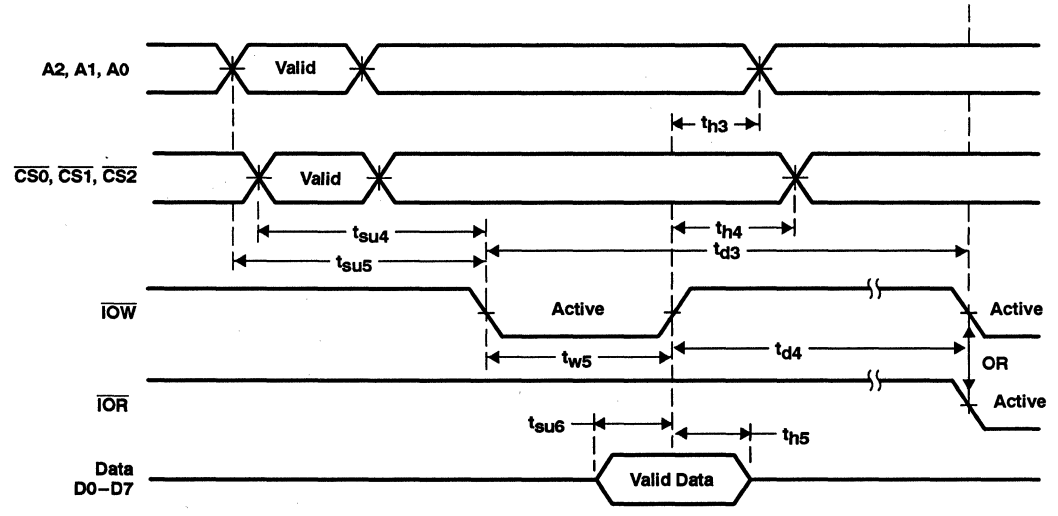


Figure 7. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

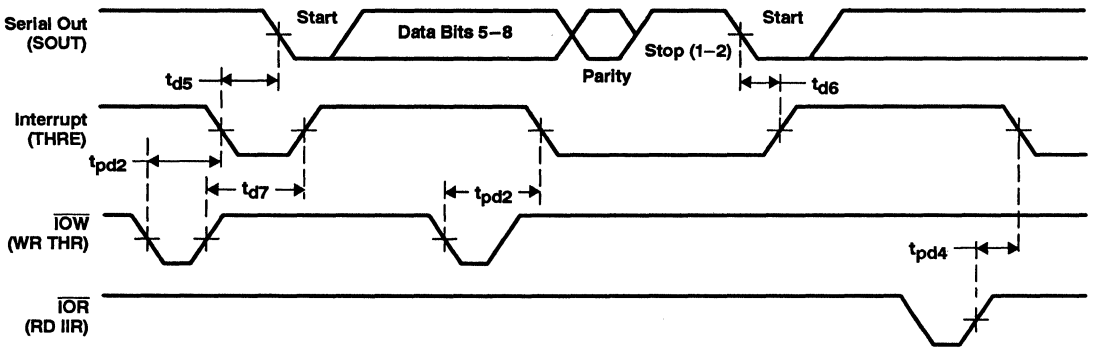


Figure 8. Transmitter Timing Waveforms

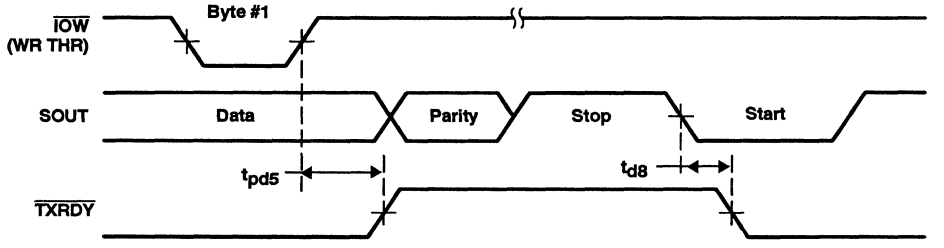


Figure 9. Transmitter Ready Mode 0 Timing Waveforms

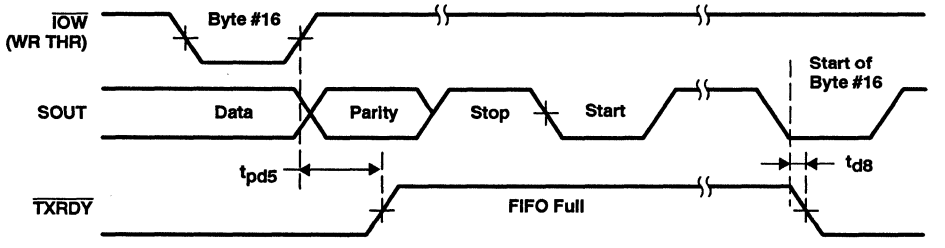


Figure 10. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

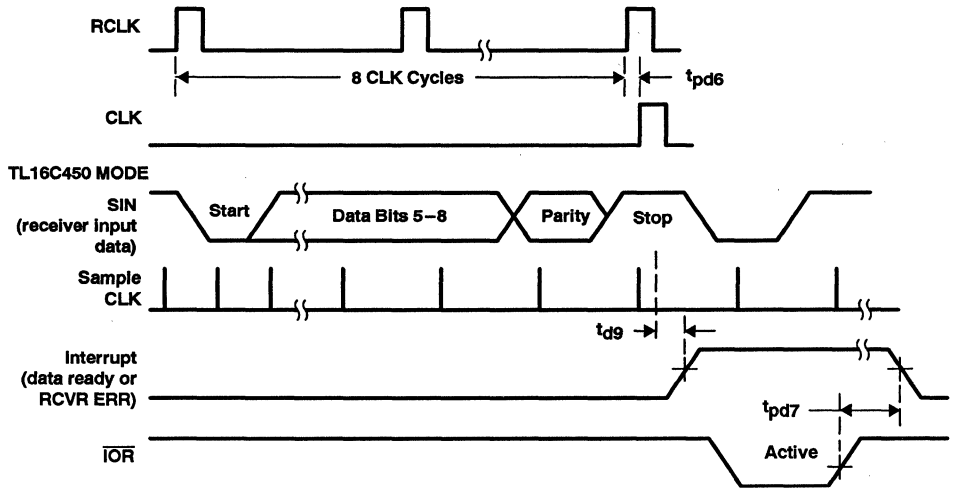


Figure 11. Receiver Timing

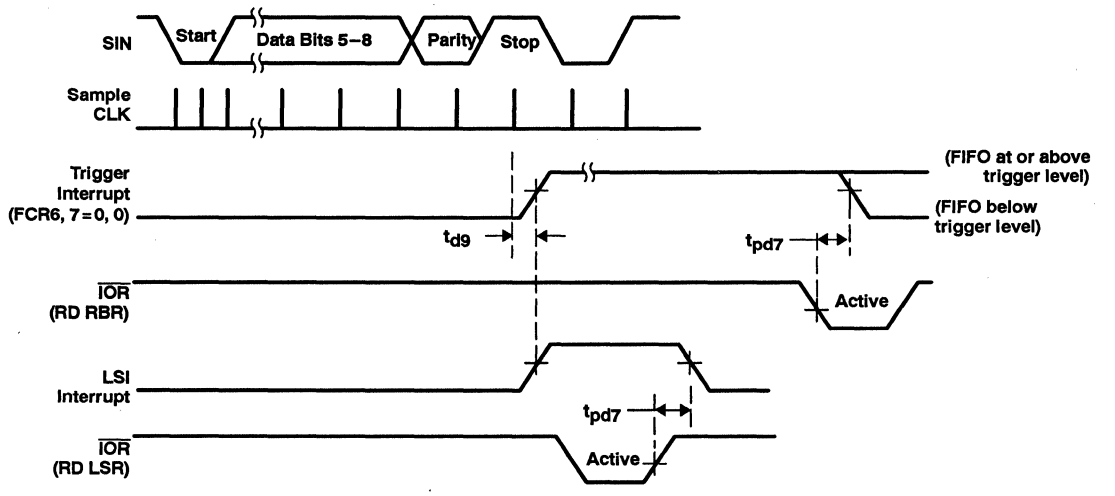


Figure 12. Receiver FIFO First Byte (Sets RDR)

PARAMETER MEASUREMENT INFORMATION

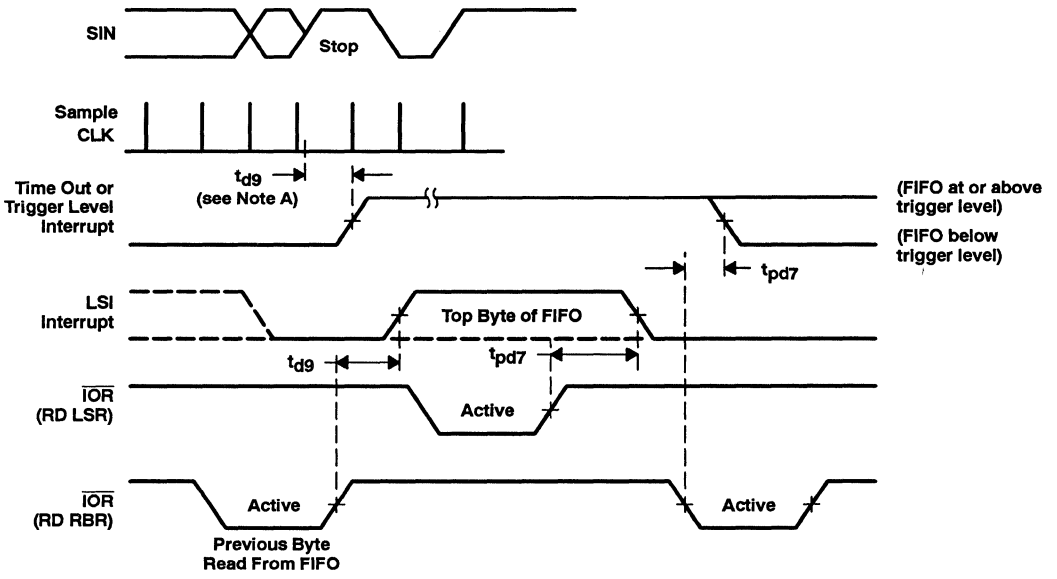


Figure 13. Receiver FIFO After First Byte (After RDR Set)

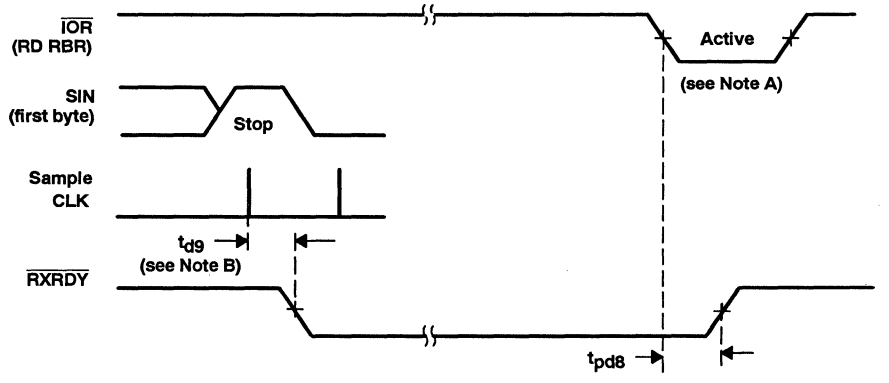
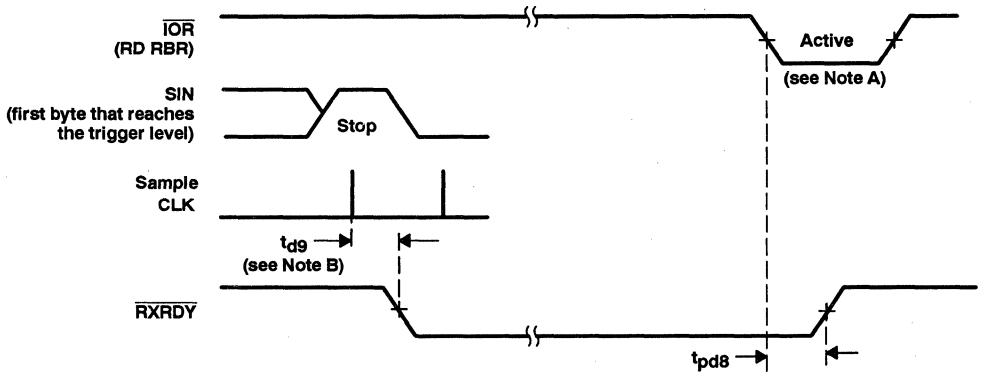


Figure 14. Receiver Ready-Mode 0

NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0=1, then t_{d9} = 3 RCLK cycles. For a timeout interrupt, t_{d9} = 8 RCLK cycles.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0=1, then t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK

Figure 15. Receiver Ready-Mode 1

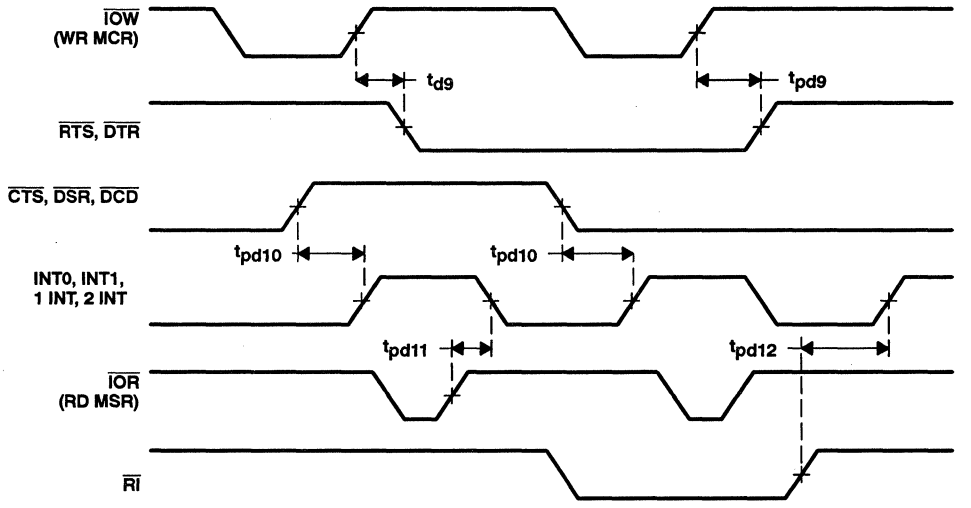


Figure 16. Modem Timing

PARAMETER MEASUREMENT INFORMATION

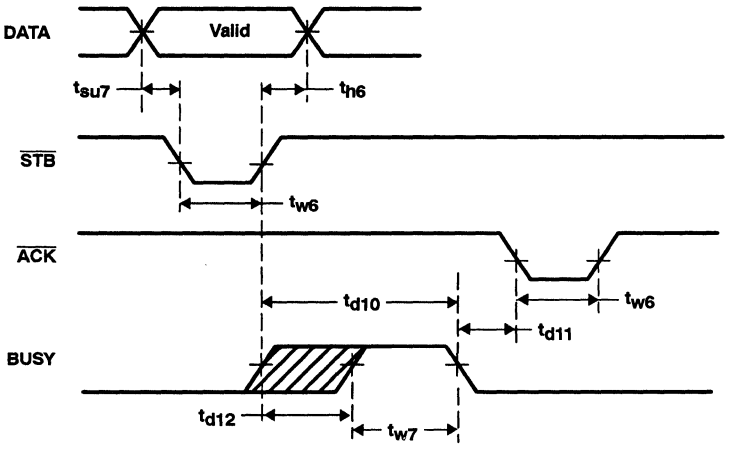


Figure 17. Parallel Port Timing

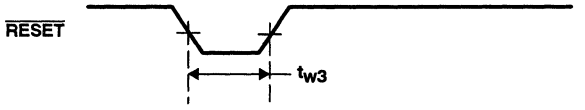


Figure 18. $\overline{RESET}$ Voltage Waveform

4 Explanation of Logic Symbols

Explanation of Logic Symbols

by F.A. Mann

Contents

List of Tables

List of Illustrations

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
IEEE Standards Office
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

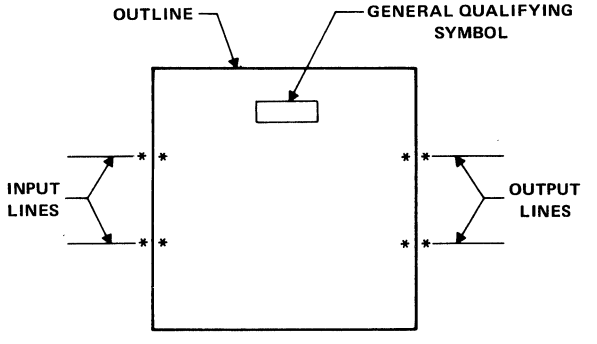
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply ANSI/IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this data book and is somewhat briefer than the explanation that appears in several of TI's data books on digital logic. However, it includes a new section (6.0) that explains several symbols for actual devices in detail. This has proven to be a powerful learning aid.

2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 9.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

3 Qualifying Symbols

3.1 General Qualifying Symbols

Table 1 shows general qualifying symbols defined by ANSI/IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

X/Y is the general qualifying symbol for identifying coders, code converters, and level converters. X and Y may be used in their own right to stand for some code or either or both may be replaced by some other indication of the code or level such as BCD or TTL. As might be expected, interface circuits make frequent use of this set of qualifying symbols.

Table 1. General Qualifying Symbols

SYMBOL	DESCRIPTION
&	AND gate or function
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.
=1	Exclusive OR. One and only one input must be active to activate the output.
1	A simple 1-input gate or element
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).
⊓	Schmitt trigger; element with hysteresis
X/Y	Coder, code converter, level converter
	The following are examples of subsets of this general class of qualifying symbol used in this book.
	BCD/7-SEG — BCD to 7-segment display driver
	TTL/MOS — TTL to MOS level converter
	CMOS/PLASMA DISP — Plasma-display driver with CMOS-compatible inputs
	MOS/LED — Light-emitting-diode driver with MOS-compatible inputs
	CMOS/VAC FLUOR DISP — Vacuum-fluorescent display driver with CMOS-compatible inputs
	CMOS/EL DISP — Electroluminescent display driver with CMOS-compatible inputs
	TTL/GAS DISCH DISPLAY — Gas-discharge display driver with TTL-compatible inputs
SRGm	Shift register. m = number of bits.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2 and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangle polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 2. Qualifying Symbols for Inputs and Outputs


Logic negation at input. External 0 produces internal 1.


Logic negation at output. Internal 1 produces external 0.


Active-low input. Equivalent to in positive logic

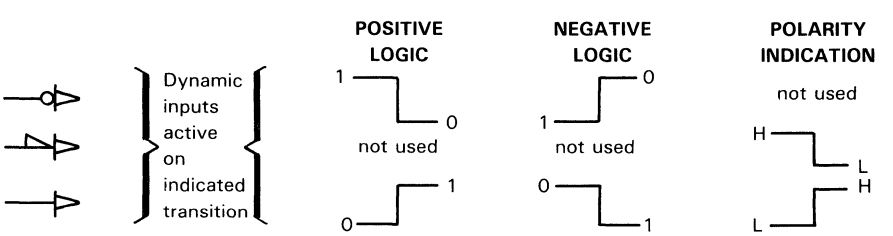

Active-low output. Equivalent to in positive logic


Active-low input in the case of right-to-left signal flow


Active-low output in the case of right-to-left signal flow


Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.


Bidirectional signal flow




Nonlogic connection. A label inside the symbol will usually define the nature of this pin.


Input for analog signals (on a digital symbol) (see Figure 11)


Input for digital signals (on an analog symbol) (see Figure 11)

3.3 Symbols Inside the Outline

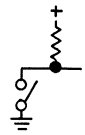
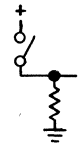
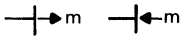
Table 3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the element and has no effect on inputs. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 6.11. Binary-weighted inputs are arranged in order and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. This number is the sum of the weights ($1, 2, 4 \ldots 2^n$) of those input standing at their 1 states. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Table 3. Symbols Inside the Outline

	Bithreshold input (input with hysteresis)
	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.
	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.
	3-state output
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector, open-emitter outputs, and three-state outputs at external high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2. Produces a number equal to the sum of the weights of the active inputs
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., differential inputs.

3.4 Combinations of Outlines and Internal Connections

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

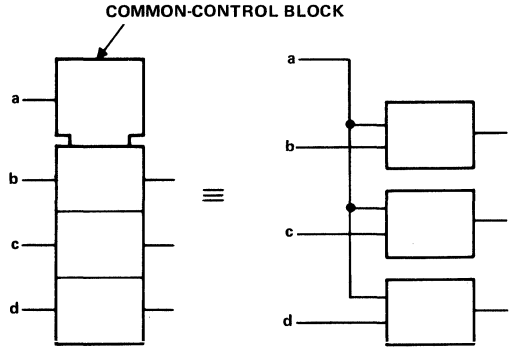


Figure 2. Common-Control Block

The outlines of elements may be embedded within one another or abutted to form complex elements, in which case the following rules apply. There is no logic connection between elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection when the line common to two outlines is perpendicular to the direction of signal flow. If no indications are shown on either side of the common line, it is assumed that there is only one logic connection. If more than one internal connection exists between adjacent elements, the number of connections will be clarified by the use of one or more of the internal connection symbols from Table 4 and/or appropriate qualifying symbols or dependency notation.

Table 4. Symbols for Internal Connections

	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Dynamic internal connection. Transition from 1 to 0 on left produces transitory 1 state on right.

Table 4 shows symbols that are used to represent internal connection with specific characteristics. The first is a simple noninverting connection, the second is inverting, the third is dynamic. As with this symbol and an external input line, the transition from 0 to 1 on the left produces a momentary 1-state on the right. The fourth symbol is similar except that the active transition on the left is from 1 to 0.

Only logic states, not levels, exist inside symbols. The negation symbol ( ) is used internally even when direct polarity indication ( ) is used externally.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN75163B symbol (see 6.5) illustrates this principle.

4 Dependency Notation

Some readers will find it more to their liking to skip this section and proceed to the explanation of the symbols for a few actual devices in 6.0. Reference will be made there to various parts of this section as it is needed. If this procedure is followed, it is recommended that 5.0 be read after 6.0 and then all of 4.0 be reread.

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined but only the eight used in this book are explained. They are listed below in the order in which they are presented and are summarized in Table 5 following 4.10.2.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	EN, Enable
4.10	M, Mode

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 3 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

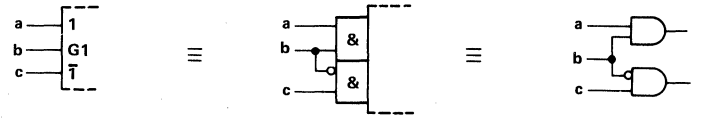


Figure 3. G Dependency Between Inputs

In Figure 4, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 5 shows input **a** to be ANDed with a dynamic input **b**.

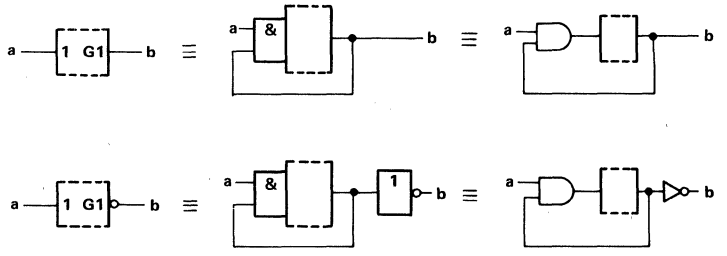


Figure 4. G Dependency Between Outputs and Inputs

Figure 5. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1. Labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2. Labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 3).

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other (Figure 6).

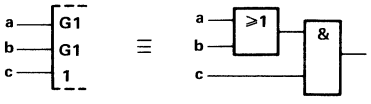


Figure 6. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 12).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 12).

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 7).

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

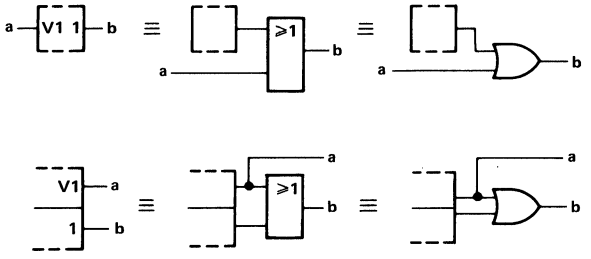
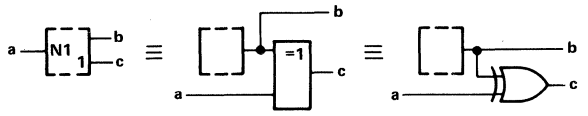


Figure 7. V (OR) Dependency

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 8). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.



If a = 0, then c = b
If a = 1, then c = $\overline{b}$

Figure 8. N (Negate) (Exclusive-OR) Dependency

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 9).

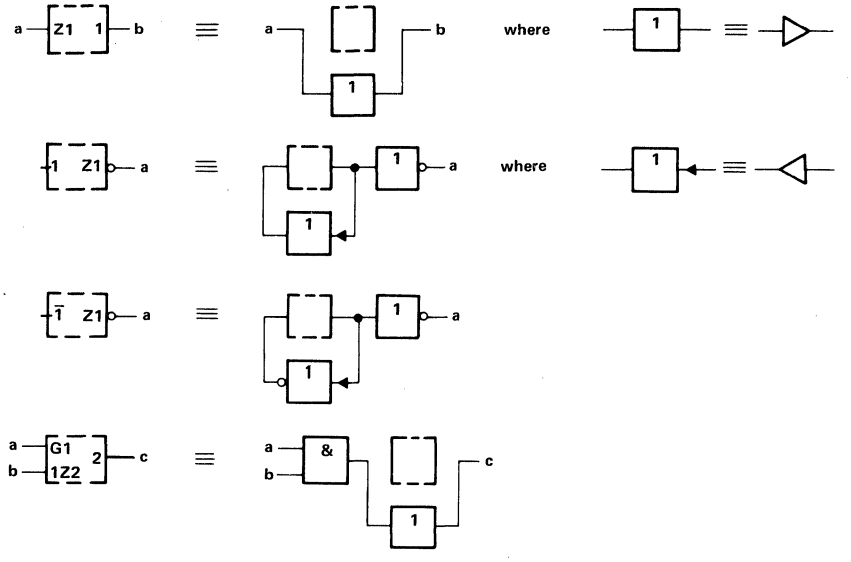


Figure 9. Z (Interconnection) Dependency

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 10).

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

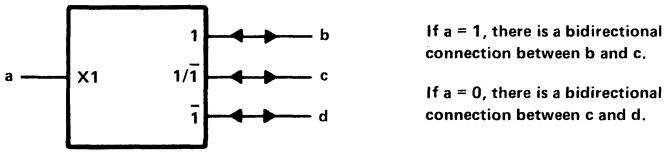


Figure 10. X (Transmission) Dependency

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 10 and 11 would be omitted.

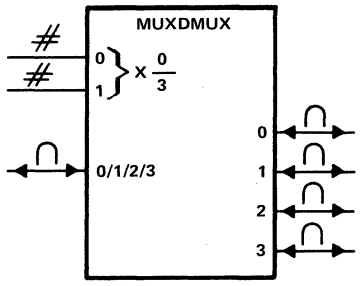


Figure 11. Analog Data Selector (Multiplexer/Demultiplexer)

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the second example of Figure 12.

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

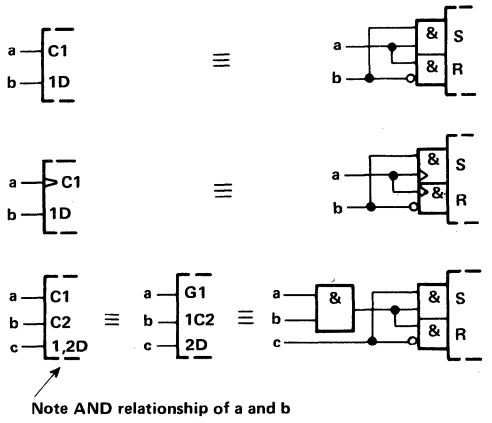
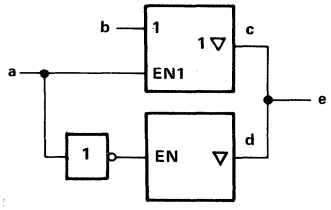


Figure 12. C (Control) Dependency

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 13).



If a = 0, input b and output c are disabled and e = d
If a = 1, output d is disabled and e = c

Figure 13. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their high-impedance state, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

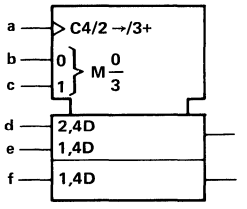
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi, e.g., $(1/2)\overline{CT}=0 \equiv 1\overline{CT}=0/2\overline{CT}=0$ where 1 and 2 refer to M1 and M2.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 14 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d, e,** and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 14. M (Mode) Dependency Affecting Inputs

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 15 shows a symbol for a device whose output can behave like either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state and, in that case, the three-state symbol applies and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect and the open-element symbol applies.

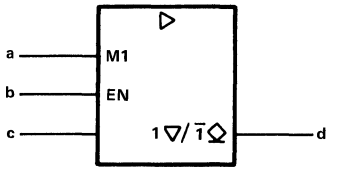


Figure 15. Type of Output Determined by Mode

Table 5. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇ outputs turned off ▽ outputs at external high impedance Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-NOR)	N	Complements state	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number.

5 Bistable Elements

The dynamic input symbol and dependency notation provide the tools to identify different types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 16).

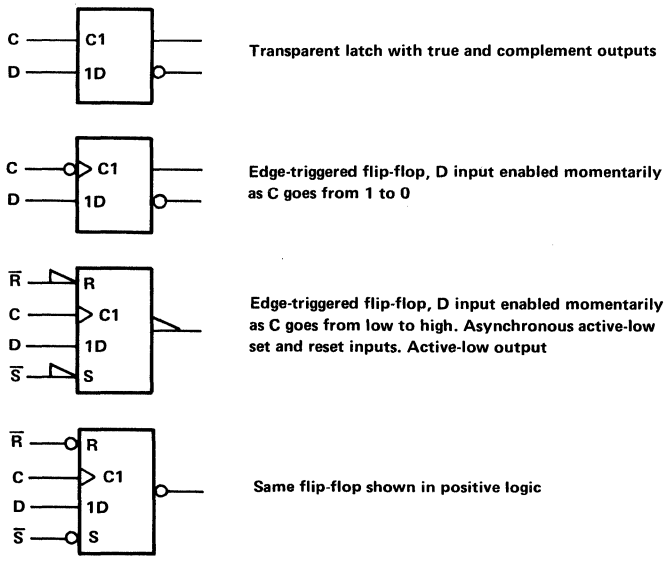


Figure 16. Latches and Flip-Flops

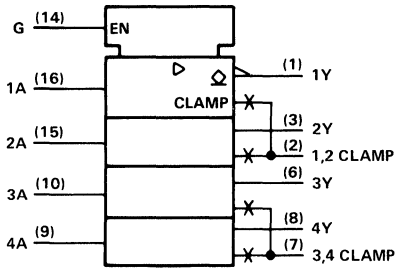
Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C.

Notice that synchronous inputs can be readily recognized by their dependency labels (a number preceding the functional label, 1D in these examples) compared to the asynchronous inputs (S and R), which are not dependent on the C inputs. Of course if the set and reset inputs were dependent on the C inputs, their labels would be similarly modified (e.g., 1S, 1R).

6 Examples of Actual Device Symbols

The symbols explained in this section include some of the most complex in this book. These were chosen, not to discourage the reader, but to illustrate the amount of information that can be conveyed. It is likely that if one reads these explanations and follows them reasonably well, most of the other symbols will seem simple indeed. The explanations are intended to be independent of each other so they may seem somewhat repetitious. However each illustrates new principles. They are arranged more or less in the order of complexity.

6.1 SN75437A Quadruple Peripheral Driver

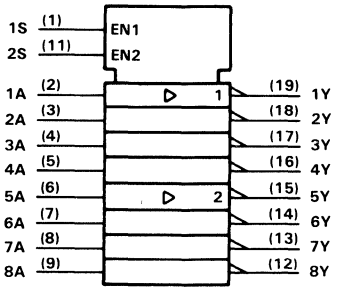


There are four identical sections. The symbology is complete for the first element; the absence of any symbology for the other elements indicates they are identical. The top two elements share a common output clamp, pin 2. This is shown to be a nonlogic connection by the superimposed X on the line. The function for this type of connection is indicated briefly and not necessarily exactly by a small amount of text within the symbol. The bottom two elements likewise share a common clamp.

Each element is shown to be an inverter with amplification (indicated by ▷). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The latter applies in this case. The output is shown by ◇ to be open collector.

All the outputs share a common EN input, pin 14. See Figure 2 for an explanation of the common control block. When EN = 0 (pin 14 is low), the outputs, being open-collector types, are turned off and would be pulled high by an external pullup resistor.

6.2 SN75128 8-Channel Line Receiver

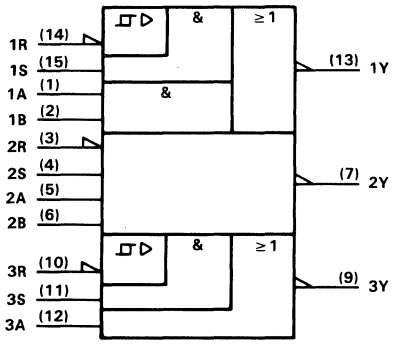


There are eight identical sections. The symbology is complete for the first element; the absence of any symbology for the next three elements indicates they are identical. Likewise the symbology is complete for the fifth element; the absence of any symbology for the next three elements indicates they are identical to the fifth.

Each element is shown to be an inverter with amplification (indicated by ▷). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The former applies in this case. Since neither the symbol for open-collector (◇) or 3-state (▽) outputs is shown, the outputs are of the totem-pole type.

The top four outputs are shown to be affected by affecting input number 1, which is EN1, meaning they will be enabled if EN1 = 1 (pin 1 is high). See 4.9 for an explanation of EN dependency. If pin 1 is low, EN1 = 0 and the affected outputs will go to their inactive (high) levels. Similarly, the lower four outputs are controlled by pin 11.

6.3 SN75122 Triple Line Receivers

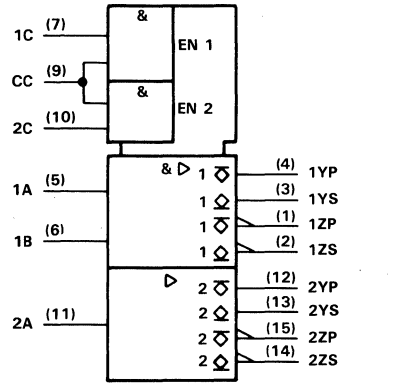


There are two identical sections. The symbology is complete for the first section; the absence of any symbology for the next section indicates it is identical. Likewise the symbology is complete for the third section, which is similar, but not identical, to the first and second.

The top section may be considered to be an OR element (≥1) with two embedded ANDs (&), one of which has an active-low amplified input (▷) with hysteresis (⊓), pin 14. This is ANDed with pin 15 and the result is ORed with the AND of pins 1 and 2. The output of the OR, pin 13, is active-low.

The third section is identical to the first except that pin 12 has no input ANDed with it. Since neither the symbol for open-collector (◇) or 3-state (▽) outputs is shown, the outputs are of the totem-pole type.

6.4 SN75113 Differential Line Drivers with Split 3-State Outputs

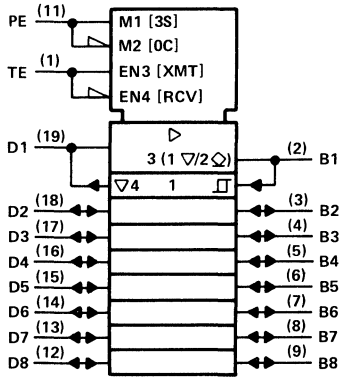


There are two similar elements in the array. The first is a 2-input AND element (indicated by &); the second has only a single input. Both elements are shown to have special amplification (indicated by ▷). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The latter applies in this case.

Each element has four outputs. Pins 4 and 3 are a pair consisting of one open-emitter output (▽) and one open-collector output (◇). Relative to the AND function, both are active high. Pins 1 and 2 are a similar pair but relative to the AND function, both are active low. All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated symbol or label inside the element. Here there is no such contrary indication. All four outputs are shown to be affected by affecting input number 1, which is EN1, meaning they will all be enabled if EN1 = 1. See 4.9 for an explanation of EN dependency. If EN1 = 0, all the affected outputs will be turned off. EN1 is the output of an AND gate (indicated by &) whose active-high inputs are pins 7 and 9. Both pins 7 and 9 must be high to enable the outputs of the top element. Assuming they are enabled and that pins 5 and 6 are both high, the internal state of all four outputs will be a 1. Pins 4 and 3 will both be high, pins 1 and 2 will both be low. The part is designed so that pins 3 and 4 may be connected together creating an active-high 3-state output. Likewise pins 1 and 2 may be connected together to create an active-low 3-state output.

All that has been said about the first element regarding its outputs and their enable inputs also applies to the second element. Pins 9 and 10 are the enable inputs in this case.

6.5 SN75163B Octal General-Purpose Interface Bus Transceiver



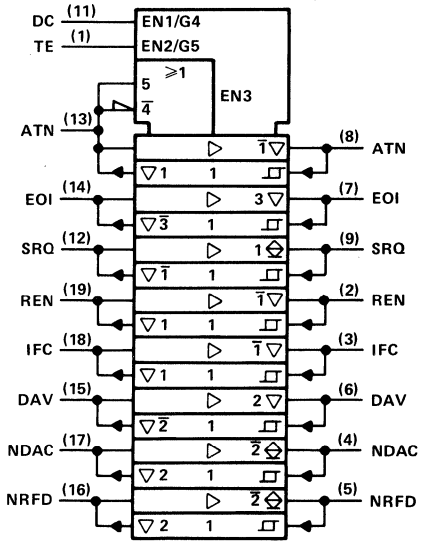
There are eight I/O ports on each side, pins 2 through 9 and 12 through 19. There are eight identical channels. The symbology is complete for the first channel; the absence of any symbology for the other channels indicates they are identical. The eight bidirectional channels each have amplification from left to right, that is, the outputs on the right have increased drive capability (indicated by ▷), and the inputs on the right all have hysteresis (indicated by ⊓).

The outputs on the left are shown to be 3-state outputs by the ▽. They are also shown to be affected by affecting input number 4, which is EN4, meaning they will be enabled if EN4 = 1 (pin 1 is low). See 4.9 for an explanation of EN dependency. If EN4 = 0 (pin 1 is high), the affected outputs will go to their high-impedance (off) states.

The labeling at pin 2, which applies to all the outputs on the right, is unusual because the outputs themselves have an unusual feature. The label includes both the symbol for a 3-state output (▽) and for an open-collector output (◇), separated by a slash indicating that these are alternatives.

The symbol for the 3-state output is shown to be affected by affecting input number 1, which is M1, meaning the ▽ label is valid when M1 = 1 (pin 11 is high), but is to be ignored when M1 = 0 (pin 11 is low). See 4.10 for an explanation of M (mode) dependency. Likewise the symbol for the open-collector output is shown to be affected by affecting input number 2, which is M2, meaning the ◇ label is valid when M2 = 1 (pin 11 is low), but is to be ignored when M2 = 0 (pin 11 is high). These labels are enclosed in parentheses (used as in algebra); the numeral 3 indicates that in either case the output is affected by EN3. Thus the right-hand outputs will be off if pin 1 is low. It can now be seen that pin 1 is the direction control and pin 11 is used to determine whether the outputs are of the 3-state or open-collector variety.

6.6 SN75161B Octal IEEE Std 488 Interface Bus Transceiver



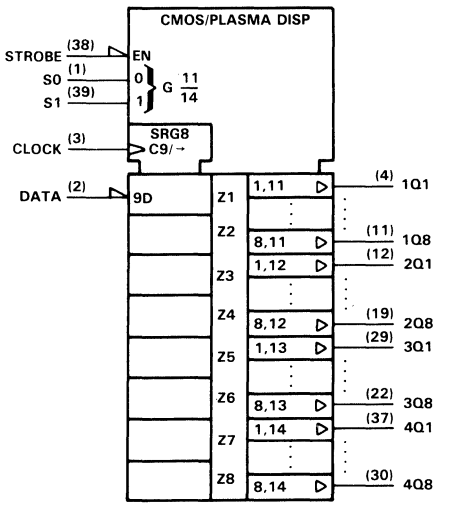
There are eight I/O ports on each side, pins 2 through 9 and 12 through 19. Pin 13 is not only an I/O port; the line running into the common-control block (see Figure 2) indicates that it also has control functions. Pins 1 and 11 are also controls. The eight bidirectional channels each have amplification from left to right, that is, the outputs on the right have increased drive capability (indicated by ▷), and the inputs on the right all have hysteresis (indicated by ⊓). All of the outputs are shown to be of the 3-state type by the ▽ symbol except for the outputs at pins 9, 4, and 5, which are shown to have passive pullups by the ⟐ symbol.

Starting with a typical I/O port, pin 18, the output portion is identified by an arrow indicating right-to-left signal flow and the three-state output symbol (▽). This output is shown to be affected by affecting input number 1, which is EN1, meaning it will be enabled as an output if EN1 = 1 (pin 11 is high). See 4.9 for an explanation of EN dependency. If pin 11 is low, EN1 = 0 and the output at pin 18 will be in its high-impedance (off) state. This also applies to the 3-state outputs at pins 13 and 19 and to the passive-pullup output at pin 9. On the other hand, the outputs at pins 8, 2, 3, and 12 all are affected by the complement of EN1. This is indicated by the bar over the 1 at each of those outputs. They are enabled only when pin 11 is low. Thus one function of pin 11 is to serve as direction control for the first, third, fourth, and fifth channels.

Similarly it can be seen that pin 1 serves as direction control for the sixth, seventh, and eighth channels. If pin 1 is high, transmission will be from left to right in the sixth channel, right to left in the seventh and eighth. These transmissions are reversed if pin 1 is low.

The direction control for the second channel, EN3, is more complex. EN3 is the output of an OR (≥ 1) function. One of the inputs to this OR is the active-high signal on pin 13. This signal is shown to be affected at the input to the OR gate by affecting input number 5, which is G5, meaning that pin 13 is ANDed with pin 1 before entering the OR gate. See 4.2 for an explanation of G (AND) dependency. The other input to the OR is the active-low signal on pin 13. This signal is ANDed with the complement of pin 11 before entering the OR gate. This is indicated by the G4 at pin 1 and the 4 with a bar over it at pin 13. Thus for EN3 to stand at the 1 state, which would enable transmission from pin 14 to pin 7, both pins 13 and 1 must be high or both pins 13 and 11 must be low.

6.7 SN75500E AC Plasma Display Driver with CMOS-Compatible Inputs



The heart of this device and its symbol is an 8-bit shift register. It has a single D input, pin 2, which is shown to be affected by affecting input number 9, which is C9, meaning it will be enabled if C9 = 1. See 4.8 for an explanation of C dependency and 5.0 for a discussion of bistable elements. Since the C input is dynamic, the storage elements are edge-triggered flip-flops. While C9 = 1, which in this case will occur on the transition of pin 3 from low to high, the state of the D input will be stored. Pin 2 is shown to be active low so to store a 1, pin 2 must be low.

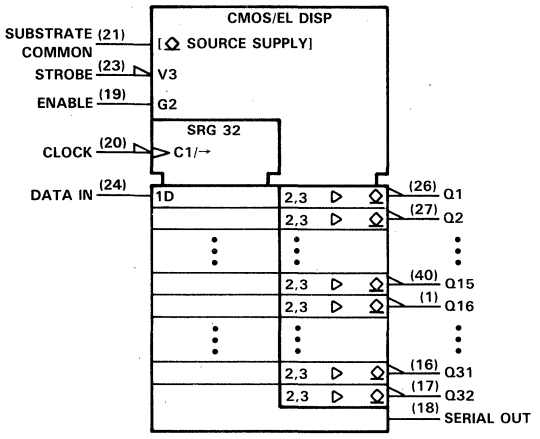
In addition to controlling the D input, pin 3 is shown by /→ to have an additional function. As pin 3 goes from low to high, data stored in the shift register is shifted one position. The right-pointing arrow means that the data is shifted away from the control block (down).

On the right side of the symbol an abbreviation technique has been used that is practical only when the internal labels and the pin numbers are both consecutive. Thus it should be clear that the input of the element whose output is pin 5 is affected by affecting input number 2, just as the input of the element whose output is pin 4 is affected by affecting input number 1. Affecting inputs 1 through 8 are Z inputs (Z1 through Z8), which means their signals are tranferred directly to the output elements. See 4.6 for an explanation of Z dependency.

The inputs of the 32 implicitly shown output elements are also shown to be affected by affecting inputs numbers 11, 12, 13, and 14 in four blocks of eight each. These inputs will be found in the common control block preceded by a letter G and a brace. The brace is called the binary grouping symbol. It is equivalent to a decoder with outputs in this case driving four G inputs (G11, G12, G13, and G14). The weights of the inputs to the coder are shown to be 2^0 and 2^1 for pins 1 and 39, respectively. The decoder has four outputs corresponding to the four possible sums of the weights of the activated decoder inputs. If pins 1 and 39 are both low, the sum of the weights = 0 and G11 = 1. If pin 1 is low while pin 39 is high, the sum = 2 and G13 = 1 and so forth. G indicates AND dependency, see 4.2. Only one of the four affecting G inputs at a time can take on the 1 state. The block of eight output elements affected by that G input are enabled; the 0 state is imposed on the other 24 output elements and externally those output pins are low.

Because of their high-current, high-voltage characteristics, the outputs are labeled with the amplification symbol ▷. All the outputs share a common EN input, pin 38. See Figure 2 for an explanation of the common control block. When EN = 0 (pin 38 is high), the outputs take on their internal 0 states. Being active high, that means they are forced low.

6.8 SN75551 Electroluminescent Row Driver with CMOS-Compatible Inputs



The heart of this device and its symbol is a 32-bit shift register. It has a single D input, pin 24, which is shown to be affected by affecting input number 1, which is C1, meaning it will be enabled if C1 = 1. See 4.8 for an explanation of C dependency and 5.0 for a discussion of bistable elements. Since the C input is dynamic, the storage elements are edge-triggered flip-flops. While C1 = 1, which in this case will occur on the transition of pin 20 from high to low, the state of the D input will be stored. Pin 24 is shown to be active high so to store a 1, pin 24 must be high.

In addition to controlling the D input, pin 20 is shown by /→ to have an additional function. As pin 20 goes from high to low, data stored in the shift register is shifted one position. The right-pointing arrow means that the data is shifted away from the control block (down). The internal inputs of the output buffers are all shown to be affected by affecting inputs 2 and 3. Affecting input 2 is G2, meaning that pin 19 is ANDed with each of the internal register outputs, which are the buffer inputs. If pin 19 is high, the affected buffer inputs are enabled. If pin 19 is low, the 0 state is imposed on the affected buffer inputs. See 4.2 for an explanation of G (AND) dependency. Affecting input 3 is V3, meaning that pin 23 (active low) is ORed with each of the internal register outputs. If pin 23 is high, V3 = 0 and the affected buffer inputs are enabled. If pin 23 is low, V3 = 1 and the 1 state is imposed on the affected buffer inputs. See 4.4 for an explanation of V (OR) dependency. The effect of V3 is taken into account after that of G2 because of the order in which the labels appear. This means that the imposition of the 1 state on the internal buffer inputs by pin 23 would take precedence over the imposition of the 0 state by pin 19 in case both inputs were active. Pin 18 is shown to be an output directly from the thirty-second stage of the shift register. Pins 19 and 23 do not affect this output.

An abbreviation technique has been used for the shift register elements and associated the output lines. This technique is practical only when the pin numbers and pin names are both consecutive.

The symbol ◇ designates an n-p-n open-collector or similar output. In this device, the outputs are actually open-drain n-channel field-effect transistors. Instead of being grounded, the sources of these transistors are all connected to pin 21. This pin is used as an input to control the output voltage.

5 Applications

Contents
Section 5.

1. Introduction

1.1. Data Transmission

It may seem strange that TI's 'Data transmission' products are included within the Linear seminar. Data Transmission as part of TI's Linear Products portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are

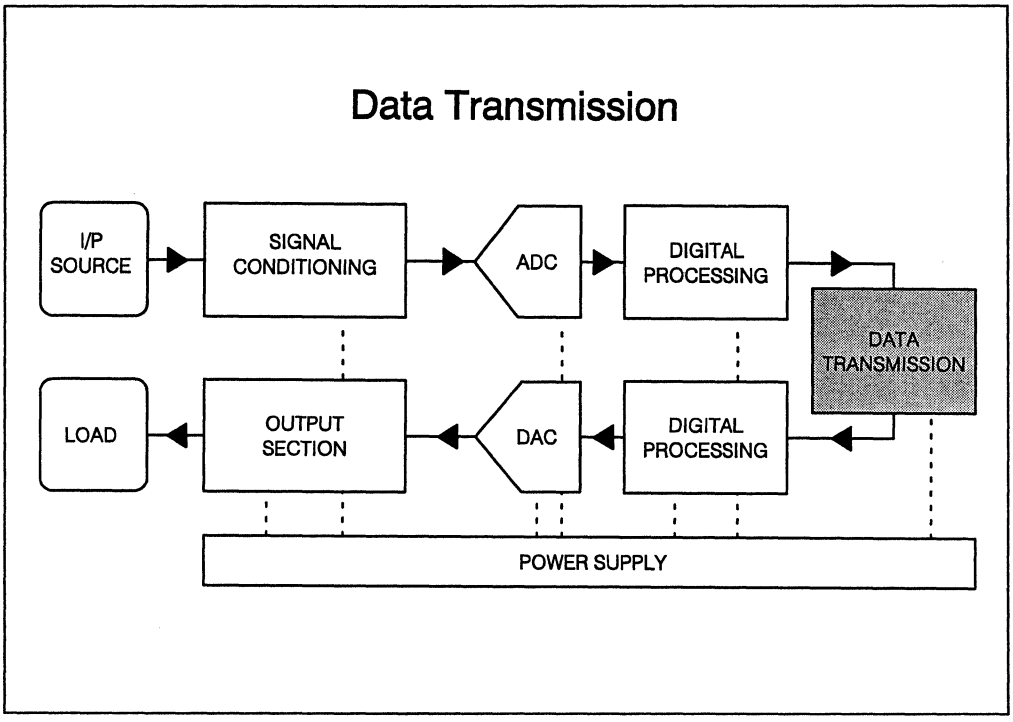


Figure 5.1 - Data Transmission

primarily of an analog more than a digital nature. Likewise the design of data transmission ICs requires experienced analog engineers to implement functions such as slew rate limiting, receiver filtering and common-mode protection.

In this year's seminar we will concentrate on two very popular transmission standards, RS-232 or as it is now known EIA/TIA-232-E, and the multi-point, half duplex RS-485 standard. The last section covers the physical layer of the increasingly popular Small Computer Systems Interface Standard (SCSI).

1.1.1. The Need for Transmission Standards

Data transmission standards evolved for two main reasons: From the need to transmit data reliably over long distances, and to provide a standard interface to facilitate communication between equipment from different suppliers. Although TTL/Logic signal levels and products can be used, they generally lack the power handling capabilities, robustness and noise margins required for reliable transmission. Indeed for backplane equipment, TTL is no longer specified for the newer high speed standards, such as Futurebus+ which uses BTL transceivers. In general the standards concerned with transmitting data over long distances incorporate wider voltage swings, increased robustness and higher power outputs than can be delivered using conventional 'Logic' products. Similarly the sub-micron technologies used in the fabrication of today's logic devices cannot provide the power handling and robustness necessary for successful long distance transmission.

1.1.2. Specialist Technologies

This leads to the need for specialist ICs, and technologies, to meet the exacting requirements of these transmission standards. The traditional technological answer has been to utilise the inherent robustness afforded by bipolar technologies, however the additional need for low power consumption and high levels of integration no longer makes this attractive. SC manufacturers are now having to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS™ technology combining the robustness of bipolar together with the power consumption and integration afforded by CMOS. Other manufacturers are using pure CMOS and integrating shottky diodes to the same end. The result is very specialised and reliable products that are able to withstand the harsh environment unique to data transmission products.

Texas Instruments has been a leading supplier of data transmission products for many years, and is continually innovating new fields. Although the following sections are limited to the more common interface standards, TI is actively involved in many new emerging standards and markets, for example Futurebus+, a backplane standard with virtually no ceiling on data rate, the high speed serial data link evolving from the P1394 committee and multiplex wiring systems such as ABUS, CAN and VAN. The reader is advised to contact a TI representative for information on these product areas.

With the considerable expertise in design, product definition and range of technologies Texas Instruments is the ideal choice for supplying your data transmission product requirements.

1.1.3. About This Section

This Section is split into four distinct sections each of which provides a practical rather than theoretical approach to in an attempt to give the reader an insight into three popular data transmission standards, EIA/TIA-232, RS-485 and the SCSI standard. The Section is split as follows:

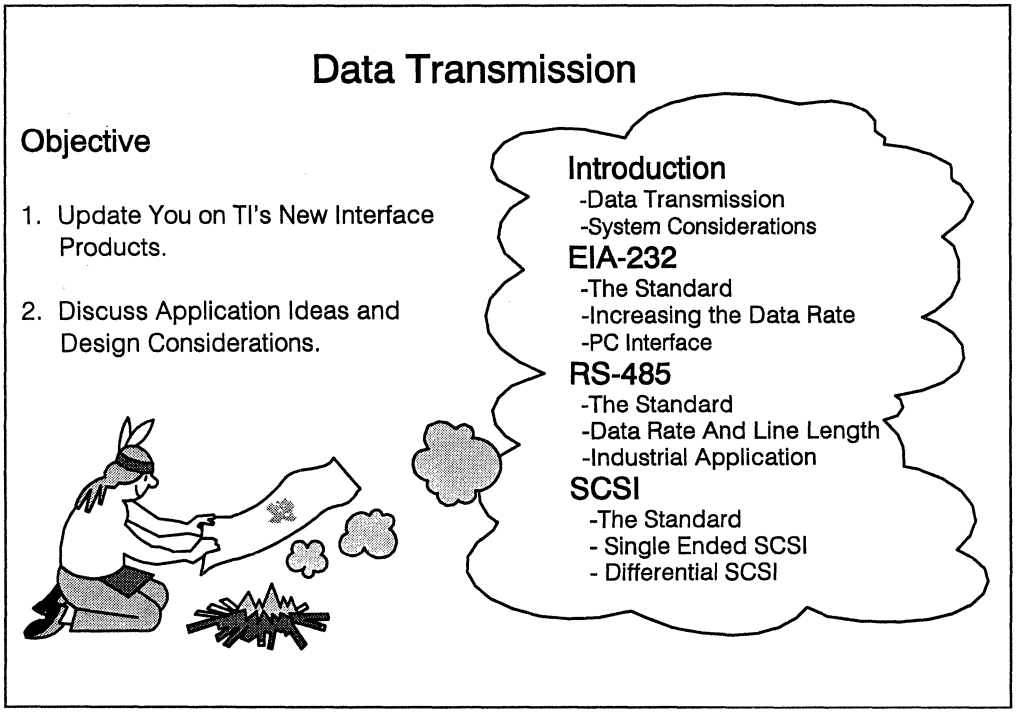


Figure 5.2 - Data Transmission Agenda

1. Introduction: An overview of the various factors that affect any data transmission system. Under discussion is the line length versus data rate trade-off, noise sources, correct line termination and network topology in addition to explaining the use of eye patterns as a tool to measure transmission quality.
2. EIA-232: A discussion of the standard with particular attention paid to the changes made in the 'E' revision. Also covered is the use of '232' at higher data rates, up to 116 kbps (kilo bits per second) and an application focus on the popular DB9 PC interface. Particular attention is paid to TI's new products throughout the section. The generic '232' standard will be referred to in this book as EIA-232, where a parameter is unique to a specific revision the EIA-232 reference will be used.
3. RS-485: An overview of the RS-485 specification followed by a design example. We use an industrial control application to understand the factors that need to be taken into account when

designing an RS-485 system. Highlighted throughout the section will be TI's new products compliant with this standard.

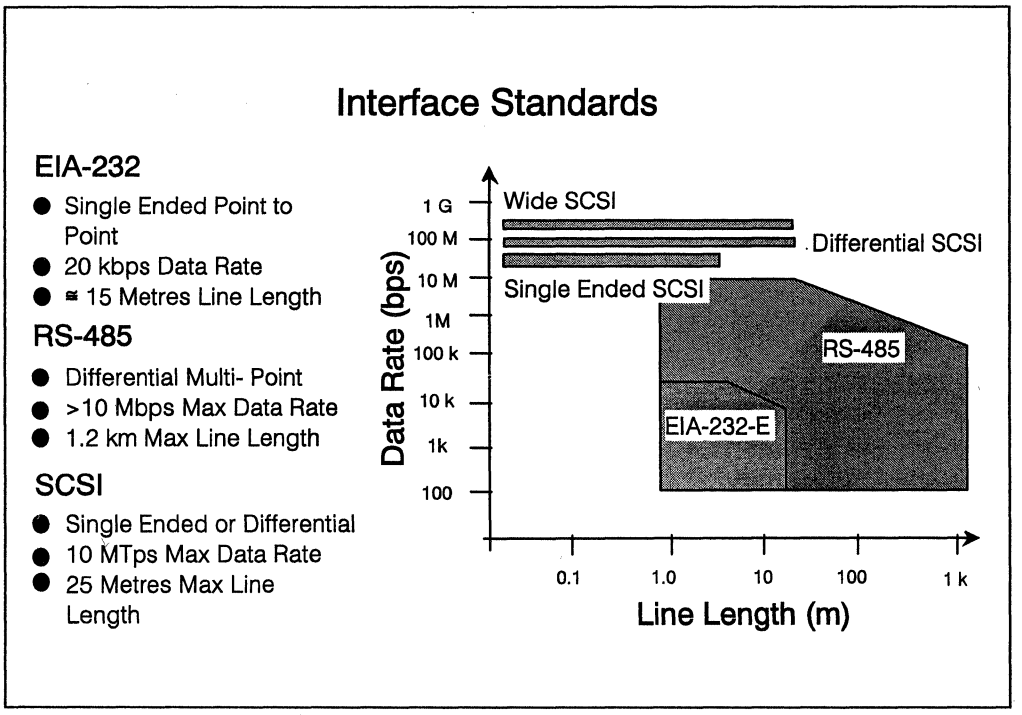


Figure 5.3 - Interface Standards

4. SCSI: We will consider the physical layer of this standard that concern both single ended and differential transmission. For single ended transmission we will look specifically at optimising the line termination to achieve maximum transmission rate over the 6 metre distance as specified in the standard. The differential SCSI system increases the line length to 25 metres and uses the RS-485 standard to achieve this. We will look at TI's new nine channel RS-485 transceiver which minimises the problems caused by the 18 line wide bus as defined by the standard.

1.2.Overview of the Interface Standards

Referring to Figure 5.3 we can see the relationship of each transmission standard when comparing data rate and line length.

1.2.1. EIA/TIA-232

EIA-232 or 'Recommended Standard' 232 is defined in the ANSI (American National Standard Institution) specification as "The Interface Between Data Terminal Equipment and Data Circuit-

Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial transmission scheme and outlines the set of rules for exchanging data between computer equipment, originally this being a Computer Terminal (DTE) and a modem (DCE). The standard has evolved over the years with the latest 'E' revision released in July 1991. The standard is now known as EIA/TIA-232-E, with EIA standing for the Electronic Industries Association and TIA for the Telecommunications Industry Association.

As with previous revisions of the standard the maximum data rate is defined as 20 k bits per second (kbps) although there are now a number of software applications that now push this data rate up to 116 kbps, well outside the standard. The 'C' revision defined the maximum line length as 15 metres however this failed to comprehend the type of cable used and consequently the load capacitance on the line driver. Both the 'D' and 'E' revisions addressed this by more correctly defining the line length in terms of load capacitance. The maximum load capacitance is specified as 2500 pF that translates using standard cables to between 15 and 20 metres. Line length and data rate are limited as the standard employs single ended communication which is prone to external factors. For longer line lengths and higher data rates a differential balanced line communication link is essential.

1.2.2. RS-485

RS-485 was primarily an upgrade to the EIA RS-422-A standard utilising the same signal levels but facilitating half duplex multi-point communication. The standard is less complex than the EIA-232 standard as it only specifies the physical layer of the transmission scheme. Hardware such as the connector is left to the user to define. The standard specifies a balanced transmission line whose maximum line length is undefined but is nominally 1.2 km for 24 AWG cable based on 6 dB signal attenuation. The maximum data rate is also undefined but is specified by the relationship of signal rise time to bit time which is influenced both by the line driver and the line length and the line loading. In the majority of applications it is the line length that is the limiting factor on data rate due to signal dispersion. This is discussed in later sections.

1.2.3. Small Computer Systems Interface (SCSI)

SCSI is an industry-standard interface, defined by the ANSI, for the interchange of data between computer and computer peripherals. Standard SCSI is a byte wide parallel interface for high speed data transfer over relatively short distances. The SCSI bus is bi-directional and is terminated at both ends of the cable to reduce reflections. For the single ended interface the standard specifies a maximum line length of 6 metres. The maximum data rate is not specified but at present 5 Million Transfers per second (MTps) is achievable using active termination. This can be increased up to 10 MTps using innovative termination as we will discuss later. For longer line length applications, up to 25 metres, the SCSI standard defines the interface using the RS-485 standard as the physical layer. This pushes the data rate to 10 MTps over the full 25 metres which equates to 80 Mbps. A further development of SCSI is 'Wide' SCSI which increases the data bus to 16 bits wide. Using the 10 MTps differential interface this increases the bit rate to 160 Mbps.

1.2.4. Summary of EIA Interface Standards

Parameter		EIA-232	RS-423-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20 k	100 k	10 M	10 M
Maximum Common-Mode Voltage (V)		±25	±6	6 to –0.25	12 to –7
Driver Output	Unloaded	±5	±3.6	±2	±1.5
Levels (V)	Loaded	±15	±6	±5	±5
Driver Load (Ω)		3 k to 7 k	450 (Min)	100 (Min)	60 (Min)
Driver Slew Rate		30 V/µs (Max.)	External Control	NA	NA
Driver Output Short Circuit Current Limit (mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to –7 or 12 V
Driver Output Resistance -	Power on	NA	NA	NA	12 k
High Z state (Ω)	Power off	300	60 k	60 k	12 k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3 V	±200 mV	±200 mV	±200 mV

1.3.System Influences

Noise, distortion and attenuation are always present in data transmission systems and strictly limit performance. We will consider each one of these in turn although there is some overlap i.e. noise can cause distortion.

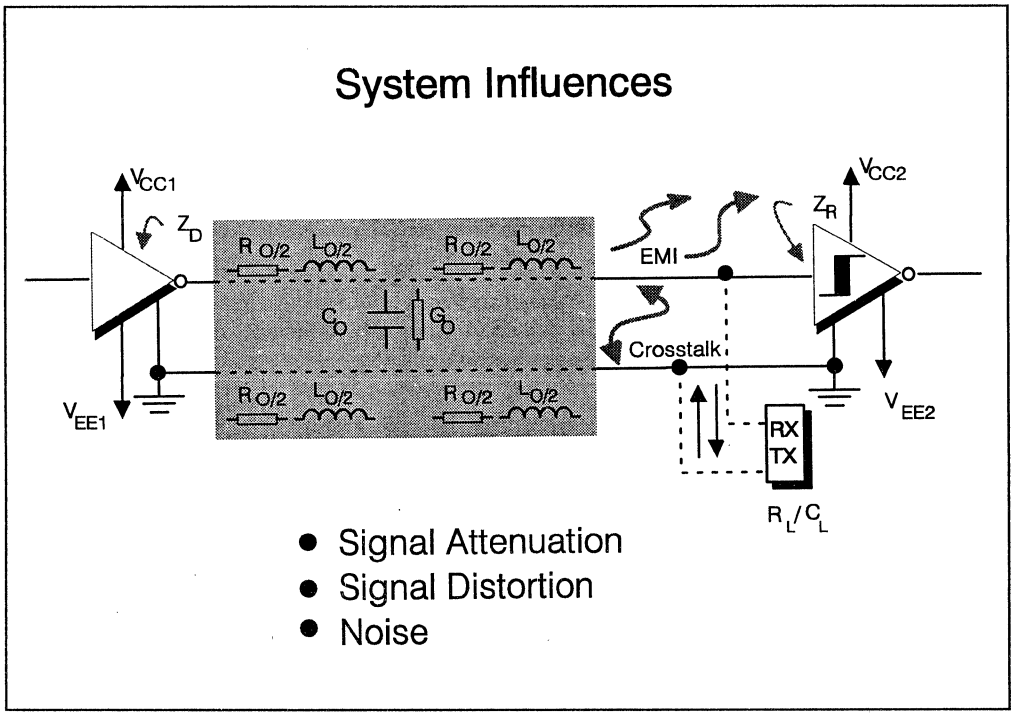


Figure 5.4 - System Influences

1.3.1. Signal Attenuation

Any data transmission over wire experiences losses and distortion due to distributed constants present along the cable: distributed series inductance, distributed shunt capacitance, distributed series resistance and distributed shunt conductance. Attenuation of the signal in a cable is affected by each of the these components. The series resistance, **R**, is frequency dependent and is a result of the DC resistance of the cable and the skin effect. Skin effect is a term which refers to the tendency of electrons to travel to the surface of a conductor at higher frequencies, thereby reducing the overall cross sectional area and increasing the resistance. The series inductance, **L**, represents the opposition to change in current levels caused by the collapsing and expanding magnetic fields created due to fluctuating current levels. The shunt capacitance, **C** ,is created by the two conductors in close proximity and separated by a dielectric. As the signal frequency increases the capacitive reactance

decreases, consequently reducing the opposition to current flow. The final component, shunt transconductance or G, is a function of the dielectric loss of the insulation around each conductor which allows some leakage current to pass between conductors. In modern dielectrics this is often assumed to be negligible.

The overall effect of these distributed constants is called the characteristic impedance of the line, Z_o, and is expressed as:

$$Z_o = \sqrt{\frac{R + j2\pi fL}{G + j2\pi fC}}$$

Where:
L is in henries/unit length
R is in ohms/unit length
C is in farads/unit length
G is on siemens/unit length

The current/voltage relationship of an incident wave travelling down a transmission line in the direction of the load will be determined by this equation. Equally a reflected wave travelling from the direction of the load will also be dependent on this relationship. We will revisit this equation when we discuss transmission line termination in section 1.5. The signal velocity along the transmission line and the attenuation depends upon the propagation constant γ of the line. The propagation constant, when separated into its real and imaginary parts, is symbolised by $\alpha + j\beta$ where α is known as the attenuation constant and β as the phase constant. α determines the rate of attenuation and has units of nepers per unit length, and β determines the phase velocity, where:

Phase velocity,

$$Vp = \frac{\omega}{\beta}$$

Where ω is the angular velocity.

Additionally, the propagation constant,

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

In practice the attenuation of a particular cable can be determined from manufacturers data where usually a curve of bit rate or frequency is plotted against dB, usually quoted per 100 ft or 30 metres. The attenuation constant, β, can be converted to dBs by multiplying by 8.686.

The maximum attenuation allowable will be dependent on the system configuration but a figure of 6 dBV maximum is a good guide. Actual curves are discussed later in the RS-485 section.

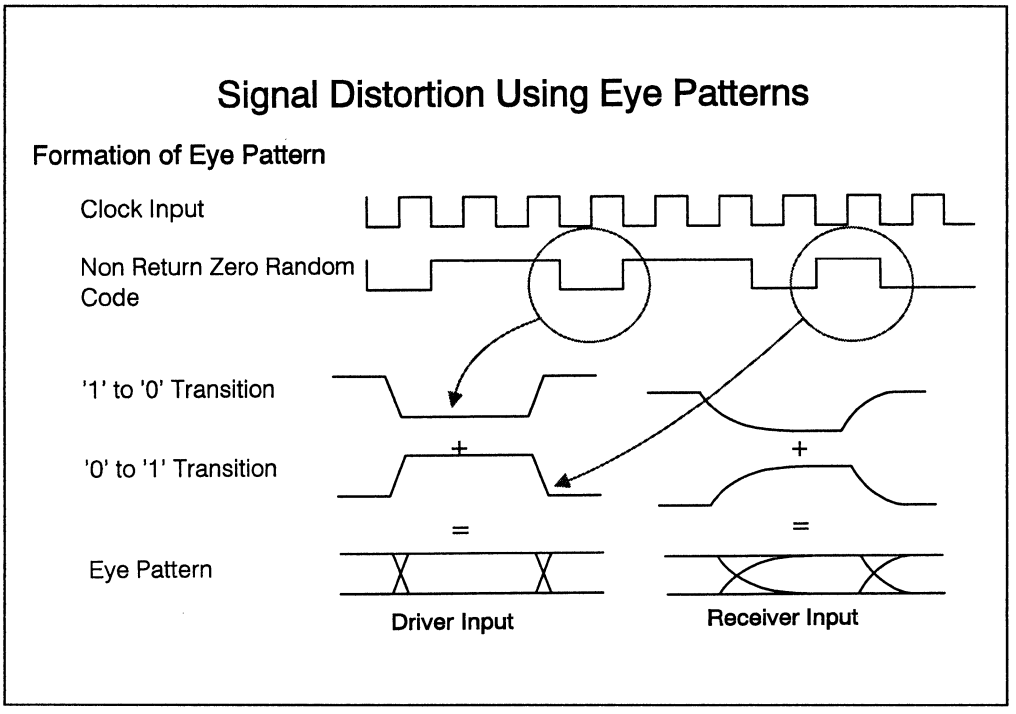


Figure 5.5 - Signal Distortion Using Eye Patterns

1.3.2. Signal Distortion

One of the primary causes of signal distortion is the effect known as frequency dispersion. As discussed in 1.3.1. phase velocity and attenuation are both frequency dependent and whose effect is to distort and delay the signal pulse. The high frequency components contained in the leading and lagging edges of a pulse experience minimum delay but experience maximum attenuation. The pulse top and low frequency components are subjected to increased delays. The result is that various parts of the pulse arrive at the receiving end at different times and at differing levels causing distortion of the original signal. It follows the longer the line length the more the bit rate must be reduced. In many transmission systems it is this factor alone which determines the maximum signalling rate.

Once again cable manufacturers sometimes specify a bit rate versus line length curve but a better way to check signal distortion of your system is by the use of eye patterns or eye diagrams. Indeed cable manufacturers generate their bit rate/distance curves using eye pattern measurements. Eye patterns allow you to visibly see and measure signal distortion as a function of data rate. See later sections on how to implement Eye Patterns.

1.3.3. Noise

Noise is generated from a variety of sources and can strongly influence how you implement your data transmission system. All extraneous signals appearing at the receiving end of the transmission circuit that are not due to the input signal are considered as noise. The two most likely sources of noise that will affecting data transmission systems in the context of this Section are common-mode voltages and cross talk. We will discuss both these types of noise and how the relate to the type of transmission system in section 1.6.

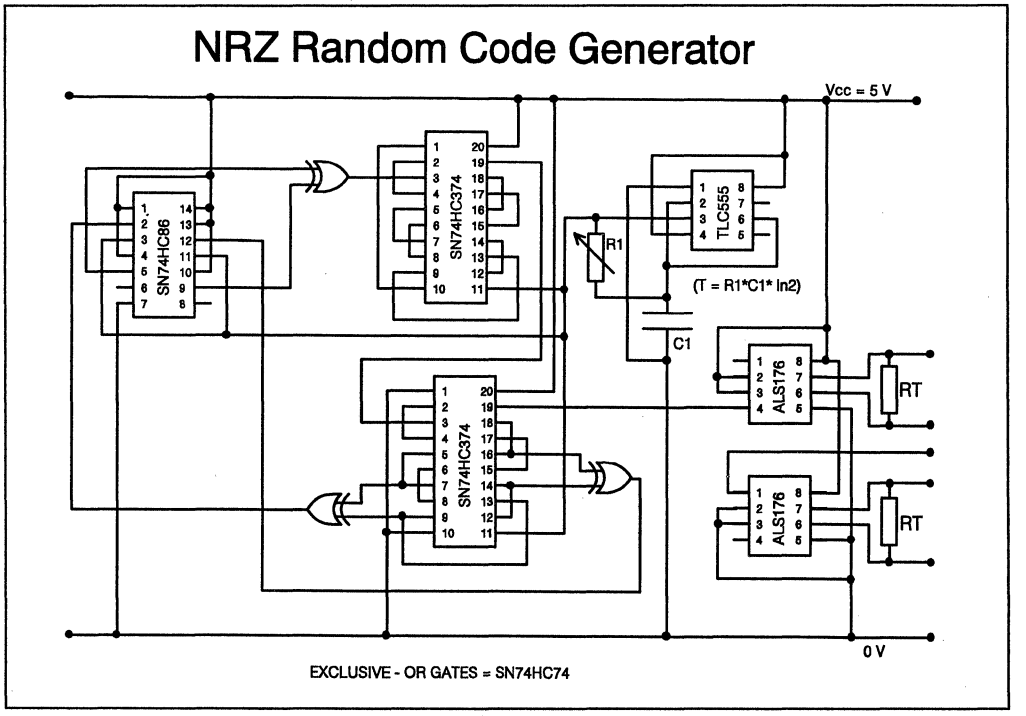


Figure 5.5.1 - NRZ Random Code Generator

1.4.Eye patterns

To determine the effects of signal distortion, noise etc. on Intersymbol interference (ISI) in a data transmission system the eye pattern is used. ISI is the effect of neighbouring pulses in a pulse train spilling over into adjacent pulses and forces a reduction in the allowable permitted pulse rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope with the term 'Eye' coming from the appearance of the trace on the CRT.

1.4.1. Setting up the eye pattern

The eye pattern is obtained by applying a random non return zero (NRZ) code down the transmission line under test. This represents all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the 'scope triggered using the synchronisation clock to the NRZ code generator on a separate trace. See Figure 5.5 Over any one unit interval the random code generator should produce a combination of signals. The resulting signals can then be viewed on the oscilloscope over one unit interval, each unit interval should resemble an eye, similar to Figure 5.6. For differential transmission both signals at the end of the transmission line should be applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

Figure 5.5.1 shows a circuit to generate the NRZ code. In this case we have used it to test the RS-485 SN75176 type transceiver.

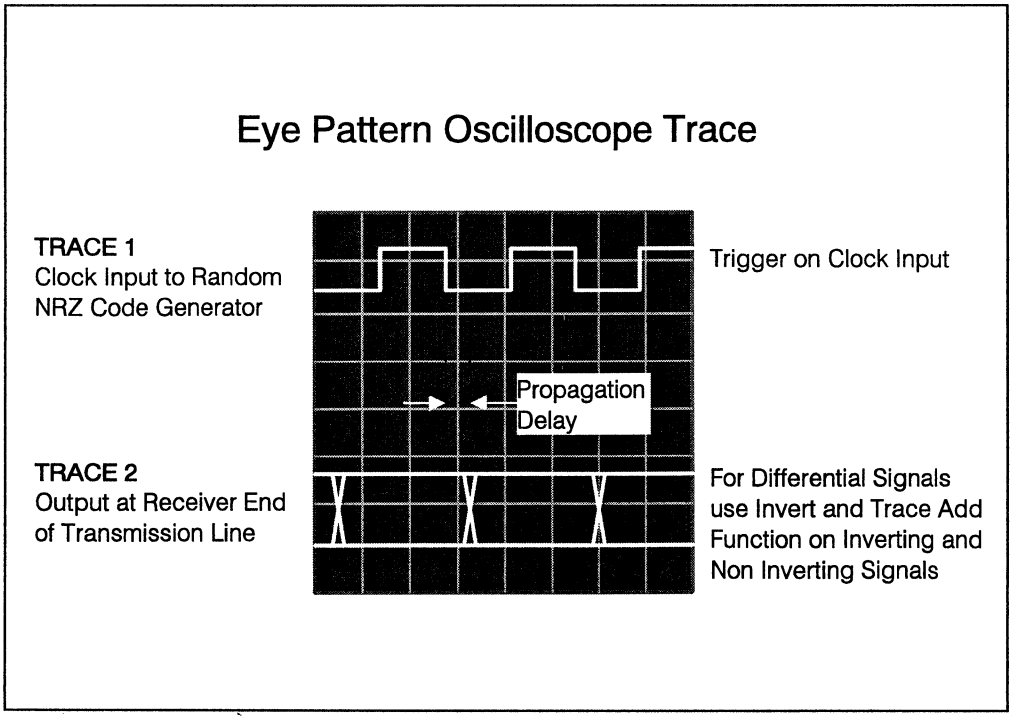


Figure 5.6 - Eye Pattern Oscilloscope Trace

1.4.2. Taking Measurements from Eye Patterns

Before considering actual measurements the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The 'openness' of the eye is an

indication of the 'quality' of the transmitted signal and is an indication of the noise and distortion tolerance of the system.

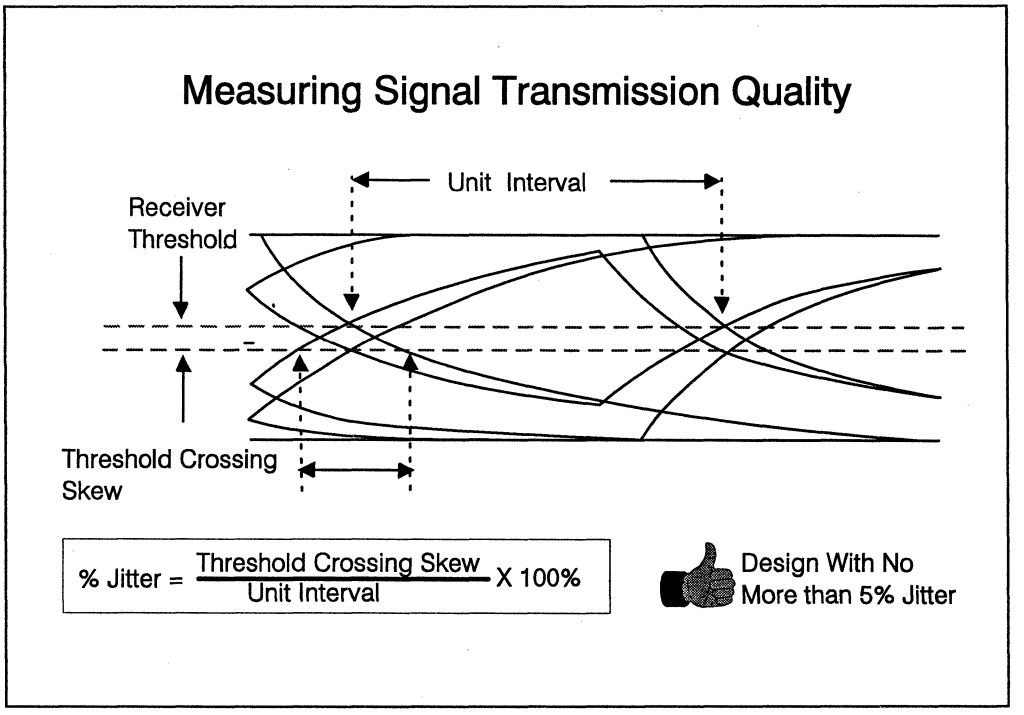


Figure 5.7 - Measuring Signal Transmission Quality

For actual measurements the decision points of the transceiver should be superimposed upon the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum jitter tolerance of the system. A good guide, and one that is used by cable manufacturers to determine data rate versus line length curves, is to design with no more than 5% jitter. Where % jitter is defined as the ratio of Threshold crossing Skew to unit interval as shown in Figure 5.7. Jitter is caused by a number of factors including , signal frequency, noise and cross talk. (Noise frequency can modulate the transmitted signal, for example 50 Hz hum or from other low frequency sources). It should also be noted at this point the effect of threshold misalignment which can cause severe problems with the received signal, reducing the detected pulse width considerably.

1.5.Line Termination

The behaviour of the transmitted signal and the integrity of the data at the receiving end depends upon the data rate and line length of the cable. There are two behavioural models; of a transmission cable:

i. **Lumped parameter model (Short wire) .**

ii. **Distributed parameter model (Transmission line)**

As discussed in section 1.3.1 the distributed parameter model models the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections and as a result the transmission line is said to have a characteristic impedance, Z_0. Z_0 is independent of distance along the line and represents the voltage and current relationship for an incident wave at any point as it travels along the line.

1.5.1. Transmission Line Test

Classifying as a Lumped or Distributed Parameter Model

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings.

Consider a signal propagating down a simple data link comprising two wires. When the signal starts to change at the transmitter output the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the transmitter terminals.

If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system.

A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated; If the rise time , t_T, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from transmitter to receiver and back to transmitter, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given in Figure 5.8 where a safety margin is built in to the propagation delay/rise time relationship.

1.5.2. Transmission Line Considerations & Effects

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. This extra load decreases the line impedance and reduces the speed of the signal along the line.

In the case of the lumped parameter model the line represents a pure fixed load to the transmitter device. For example, the capacitance of the line will be modelled as a fixed value which effectively

limits the output voltage slew rate of the transmitter (assuming it can supply a finite amount of current to the line).

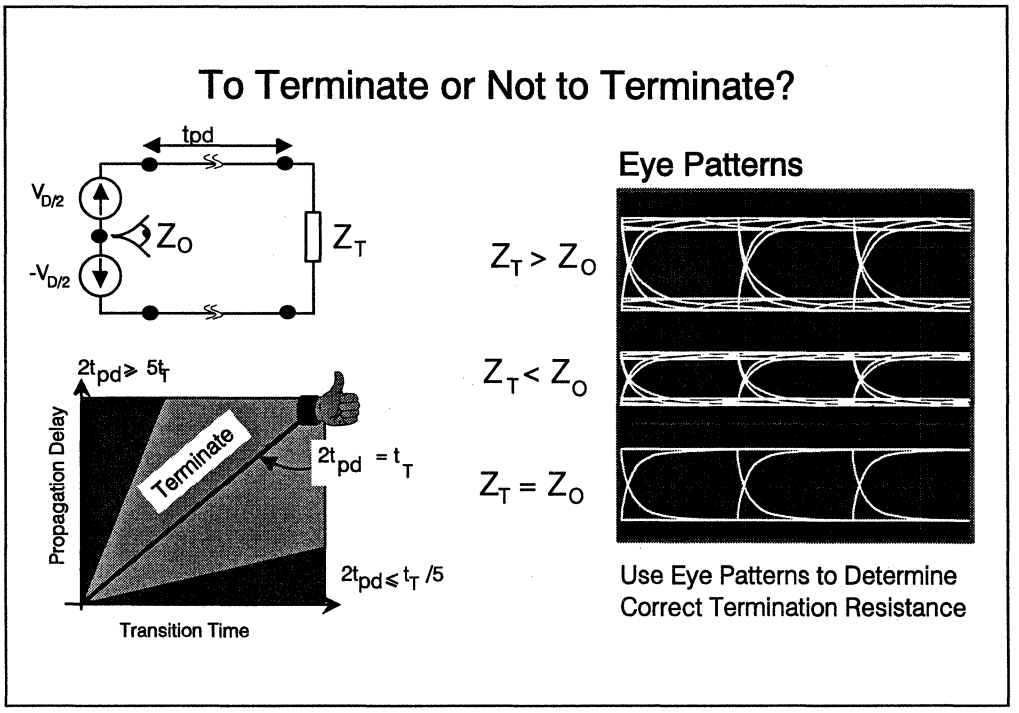


Figure 5.8 - To Terminate or Not to Terminate?

1.5.3. Transmission Line Reflections

Consider a driver circuit driving the line. When the driver output voltage changes state, the driver appears to see the effective characteristic impedance of the line, Z_O. This will cause the voltage at the output of the driver circuit to reduce as a result of the potential divider action formed by Z_O and the driver circuit output impedance, Z_D.

At any point along the line the ideal source impedance will appear as Z_O and the ideal load impedance will also appear as Z_O. This gives the impression that the line is being driven by a voltage source of twice the magnitude of the line voltage.

When the signal reaches the receiving end of the line it sees a terminating impedance equal to the impedance (Z_O) of the line that it is already travelling on. It interprets this as a continuation of the line. The voltage on the line will not alter and the current flowing along the line will flow through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency, with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

If the termination impedance is dis-similar to the characteristic impedance of the line itself, the voltage at the termination point will alter. The voltage at the termination point is dependent on the relative size of the termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage will increase causing a positive voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage will decrease leading to a negative reflection. The same effect will occur at the driver output terminals due to impedance mismatches between driver and line.

Reflections at each end of the line will eventually settle and leave a constant dc voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False receiver triggering can occur and repeated signal reflections will cause signal wave distortion.

1.5.4. Using Eye Patterns to Determine Z_0

Referring back to eye patterns, these can also be used to find the characteristic impedance of a transmission line. Figure 5.8 shows three sets of eye patterns, $Z_T > Z_O$, $Z_T < Z_O$, and $Z_T = Z_O$, where Z_T is 200 Ω, 50 Ω, and 100 Ω, respectively. Where $Z_T > Z_O$ the signal is larger with multiple traces, while with $Z_T < Z_O$ the signal is similar but much reduced in amplitude and could cause signal to noise ratio problems at the receiver. With $Z_T = Z_O$, the signal is very clear with a near perfect eye pattern. In practice it is possible to use a variable resistance and the eye pattern to determine the correct termination impedance for zero reflections.

1.6.Noise Influences

There are two main classification of transmission scheme, single ended or differential. Each are affected by noise influences in differing ways - the next two section describe each transmission scheme paying particular attention to the affects of noise. Figure 5.9 details both types of transmission scheme.

1.6.1. Single Ended Line Considerations

Single ended data transmission systems consist of a signal line on which data is sent down, and a ground line through which the current returns. A direct result of this is that the ground line forms part of the transmission line, which can be of benefit in some circumstances but not in others.

One of the major benefits, and most obvious, is that a single ended system is the lowest cost solution in terms of cabling costs. In general terms it requires only half the cable of a differential system. It is also relatively simple to install and operate.

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, any transient voltage or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation ultimately leading to false receiver triggering. For example, a shift in the ground potential at the

receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing susceptibility to noise.

Cross talk is also a major concern especially at high frequencies. Cross talk is generated from both capacitive and inductive coupling. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line

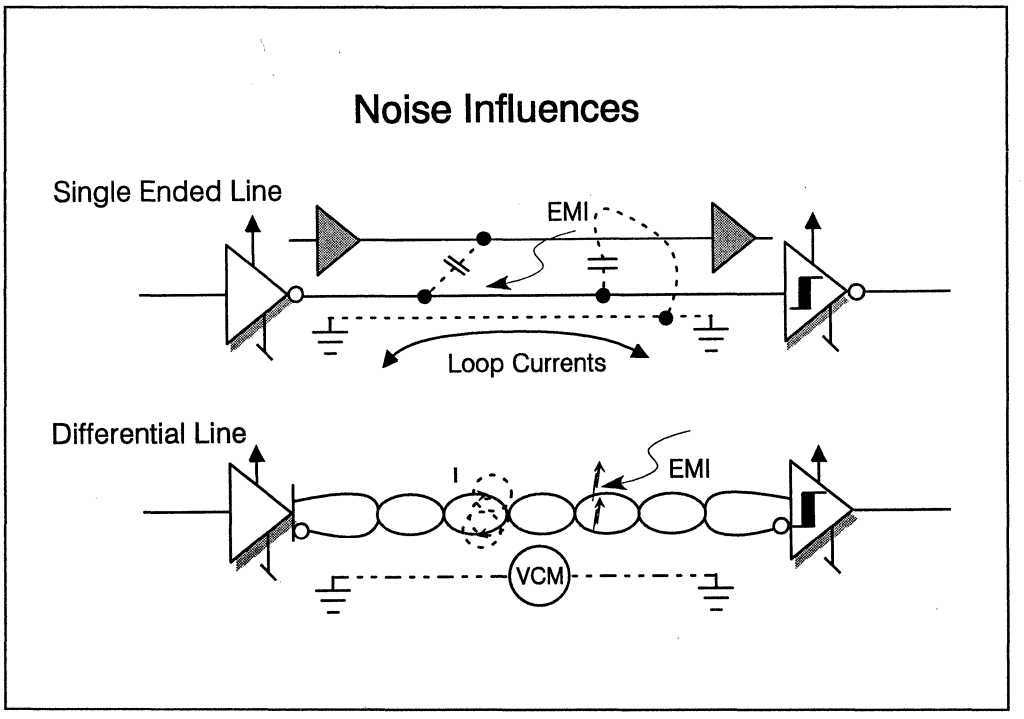


Figure 5.9 - Noise Influences

determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow.

These problems will normally limit the distance and speed of reliable operation for a single ended link.

Cross talk can be reduced by;

i. **Limiting the slew-rate of signals so that they do not cause cross talk to be induced onto other lines**

ii. **Limiting the line length.**

iii. **Shielding the signal conductor.**

While the common-mode noise could be reduced by:-

i. **Isolating the signal ground from power conductors (e.g. keep signal grounds separated as far as possible from power grounds).**

ii. **Ground wires should be as low as impedance as possible.**

iii. **Using star ground system configurations.**

Some of these techniques are used in systems such as EIA-232 e.g. Maximum slew rate of EIA-232 is defined as 30 V/μs while Futurebus+, an emerging high speed backplane standard, uses trapezoidal waveforms to limit cross talk

1.6.2. Differential Line Considerations

A differential communication system involves the use of two signal carrying wires between transmitter and receiver, such that the signal current flows in opposite directions in each wire. The net effect of this is the receiver is only concerned with the ***difference*** in voltage between the two wires. The absolute value of the dc common mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common mode voltage range in which they can operate.

The use of a differential communications interface allows transmission at higher data rates over longer distances to be accomplished. This is because the effects of external noise sources and cross talk are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost but provides superior performance when data is transmitted at high rates over long distances.

The RS-485 and RS-422-A standards both use differential type transmission.

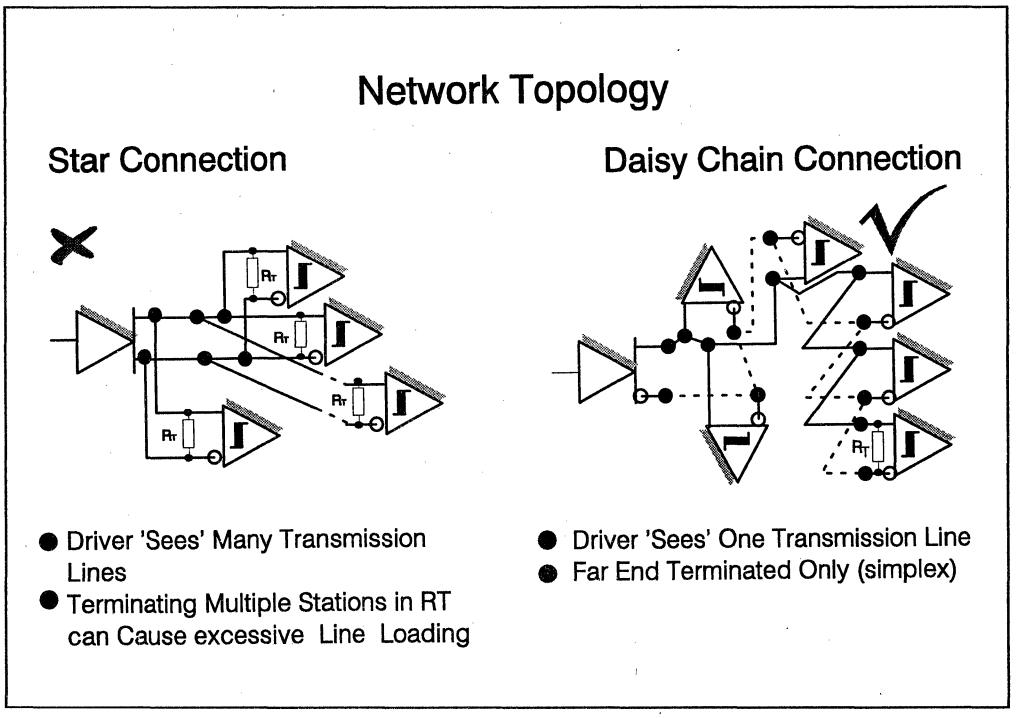


Figure 5.10 - Network Topology

1.7.Network Topology

In addition to considering signal attenuation, the effects of noise, signal distortion and correct line termination, we must also consider the way in which stations are connected to the line. Furthermore the position of the line termination resistor and device positioning must be considered. There are two basic methods of connection, see Figure 5.10;

i. **The star connection**

ii. **The daisy chain connection**

Considering the star connection, the transition edge from the driver will be loaded by a group of separate transmission lines, rather than one. Each transmission line boundary will cause a change in impedance resulting in reflections.

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended and is accounted for in each standard. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.

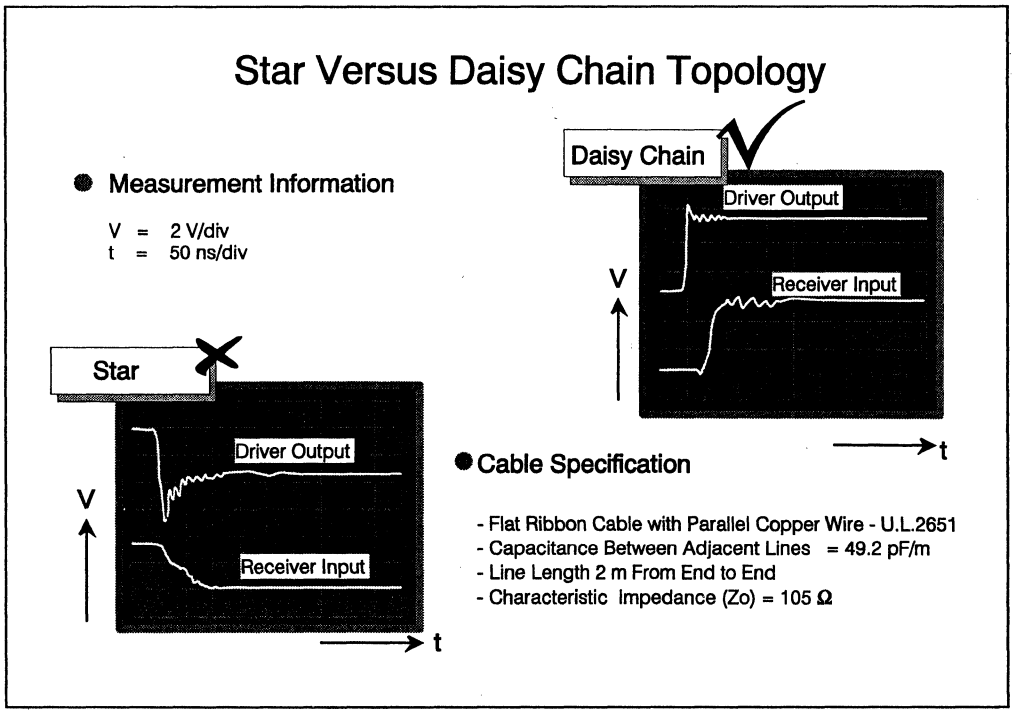


Figure 5.11 - Star Versus Daisy Chain Topology

The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and hence the driver will see one continuous transmission line with only one termination resistor. Each tap-off will in effect be a stub, but in this case they will not be all grouped together and will be kept very short to reduce their effect.

The Figure 5.11 shown further confirms the need to keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.

In both instances exactly the same application scenario was used as was the same cable specification. The cable used was a flat ribbon cable with parallel copper wire conforming to U.L. specification 2651. Connections were made as shown in the previous figure and the total cable length from source to destination was 2 m.

1.7.1. How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the round trip propagation delay, t_{pd} ,is more than 5 times the transition times of the driver, t_T. The converse is true

if the line is not to operate as a transmission line but as a lumped parameter model. This forms the basis of the stub length calculation given below.

The rule of thumb states that the transition time of the pulse sent down the line should take ten times the time taken for the pulse to propagate to the end of the stub. As a result, any reflections will be incorporated into the transition edge.

From this basis, the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, **U**, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used. The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These facts can be brought together to give the length of the stub, L_S , as;

$$L_S = \frac{t_{tD}}{10}$$

Using the SN75ALS180 and its transition time of 13 ns, a cable with a characteristic impedance of 78Ω and line capacitance of 65pF,:

Using: $Z_O = \sqrt{\frac{L_O}{C_O}}$, as an approximation of the equation shown in section 1.3.1. (In practical situations $j\omega L >> R$ and $j\omega C >> G$, therefore **R** and **G** can be assumed to be negligible although the **R** component must be considered for long line lengths.)

And: $V_P = \frac{1}{\sqrt{L_O x C_O}}$ as an approximation of the phase velocity equation in 1.3.1,

Substitution gives: $V_P = \frac{1}{Z_O x C_O}$

Using the values given earlier: $V_P = \frac{1}{78x65x10^{-12}} = 198x10^6 ms^{-1}$

Now, using our rule of thumb described earlier: $t_{pd} = \frac{t_{tD}}{10}$ and $L_S = t_{pd} x V_P$

Gives $t_{pd} = \frac{13x10^{-9}}{10}$ and therefore $L_S = 1.3x10^{-9} x198x10^6 = 257mm = 10inches$

This means the length of each stub should be no more than 257 mm. Under this length the stub can be considered as a lumped load and will not cause any unwanted reflections. The main effect of each stub in this case will be a slight increase in the capacitance loading of the line.

2. Interface Circuits for EIA-232

2.1. General Information

This section on EIA/TIA-232, or RS-232 as it has been known in the past, will discuss the electrical aspects of the standard, i.e. the physical layer. Initially we will discuss the latest developments of the 'E' revision upgrade and then cover TI's latest products conforming to this standard. However the reader should note the products under discussion in this section are application specific to the 9-pin DB9 Personal Computer DTE serial interface which is effectively a sub-set of the full EIA-232 standard. As a semiconductor manufacturer we find the majority of EIA-232 applications are moving to this interface. Due to the nature of the signals i.e. 5 receive and 3 transmit lines the older established EIA-232 products no longer provide an optimum solution. This interface is now driving the need for single chip EIA-232 solutions. Additional features such as single supply operation, increased ESD protection, power down modes have moved from the desirable features to the essential features of today's interface. In the later half of this section we will discuss the DB9 interface and TI's products designed specifically for this application.

Looking at the DB9 interface one step back into the digital system, there is in most cases a UART or ACE (asynchronous communication element). The ACE provides the parallel to serial conversion and the necessary start/stop bits, parity bit generation and checking for error free data transmission. TI manufactures a number of ACEs, the most advanced being the TL16C552. This integrates two serial ports with FIFO buffers together with a PC parallel port. Although not specifically covered in this section a selection guide on ACEs is included towards the rear of this section.

2.1.1. Reliability Data

System designers have long been aware the mean-time-between-failure (MTBF) for most systems is limited by the reliability of the line interface circuitry. This is mainly due to the shear power dissipation of such line circuits. The older devices such as the SN75188 quad driver ran at quite high temperatures with obvious degradation on reliability. For today's products the use of low power bipolar and more recently BiCMOS technologies significantly reduces operating temperatures while maintaining the robustness associated with bipolar designs providing for a more reliable interface. This is show by reliability data collected on TI's products.

Life test data collected on a range of EIA-232 devices yielded a failure rate of 1.65 FITS (failures per 10^9 device hours). This was at an ambient temperature of 55°C (to an upper confidence level of 60% and assumes an activation energy of 0.96 eV).

2.2.EIA/TIA-232-E Industry Standard for Data Transmission

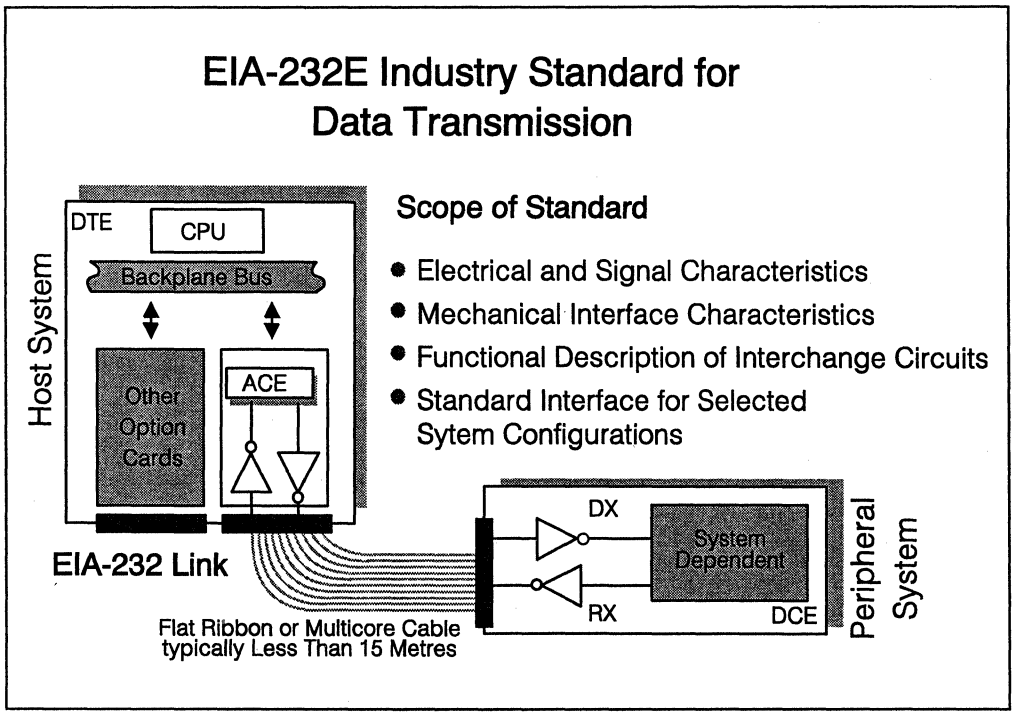


Figure 5.12 - EIA-232-E Industry Standard for Data Transmission

The Electronic Industries Association (EIA) introduced the RS-232 standard in 1962 in an attempt to standardise the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). The DTE comprises the data source, data sink or both. The DCE provides the functions to establish, maintain and terminate a connection, and to code/decode the signals between the DTE and the data channel. Although emphasis was then placed on interfacing between a modem unit and data terminal equipment, other applications were quick to adopt the EIA-232 standard. The growing use of the PC (personal computer) quickly ensured that EIA-232 became the industry standard for all low-cost serial interfaces between the DTE and peripheral. The mouse, plotter, printer, scanner, digitiser, and tracker-ball, in addition to the external modem unit, are all examples

of peripherals that connect to an EIA-232 port. Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

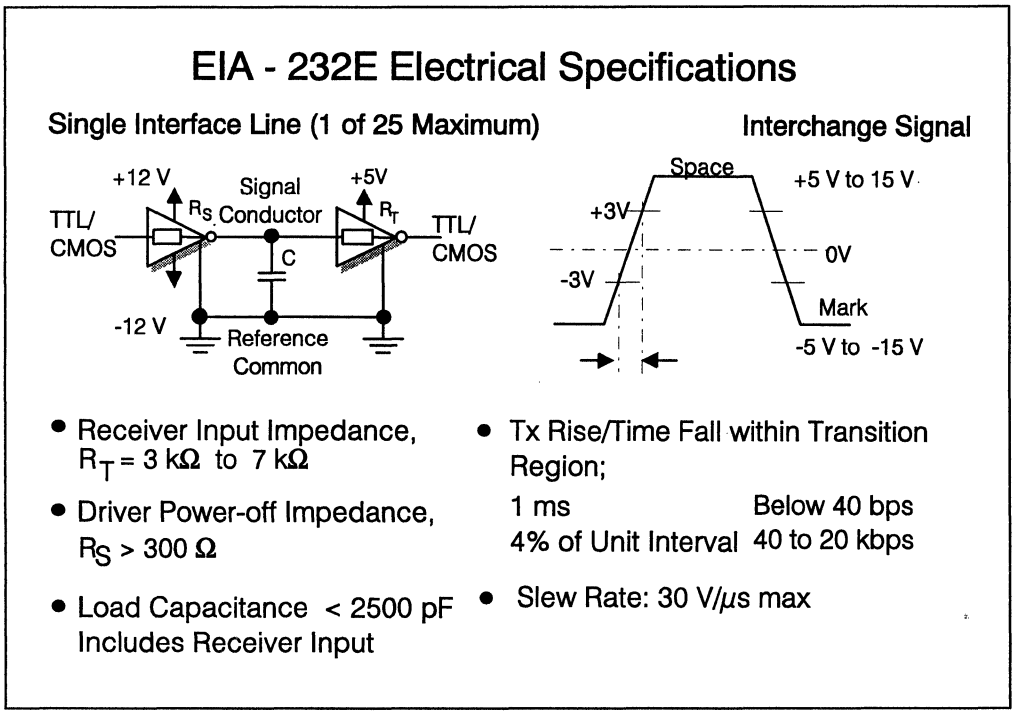


Figure 5.13 - EIA-232-E Electrical Specifications

The EIA RS-232-C standard, revised in 1969, was superseded by EIA-232-D (1986), and recently has been once again superseded by EIA/TIA-232-E which brings it in-line with CCITT V24, V.28 and ISO IS2110. (TIA refers to the Telecommunication Industry Association). The latest revision includes an update on the rise time to unit interval ratio and reverses the changes made by the 'D' revision, see Figure 5.14. Although an older standard, with problems like high-noise susceptibility, low data rates and very limited transmission length, EIA-232 fulfils a vital need as a low cost communication system. Consequently new products are being developed at a faster rate than ever.

2.3.EIA-232 Specification

The standard sets out to ensure:

i. Compatible voltage and signal levels

ii. Common pin wiring configurations

iii. A minimum amount of control information between the DTE and DCE.

It accomplishes this by incorporating the following areas in the standard:

Electrical and Signal Characteristics

Electrical and signal characteristics of the transmitted data in terms of signal voltage levels, impedance's, and rates of change.

Mechanical Interface Characteristics

Mechanical interface characteristics defined as a 25-way "D" connector, with dimensions and pin assignments specified in the standard. Although the standard only specifies a 25-pin D-type connector, most laptop and desktop PCs, today use a 9-pin "DB9S" connector shown in Figure 5.17. The reader should note the DCE equipment connector is male for the connector housing and female for the connection pins. Like wise the DTE connector is a female housing with male connection pins.

Handshake Information

A functional description of the interchange circuit enables a fully interlocked handshake exchange of data between equipment's at opposite ends of the communication channel. However, V24 defines many more signal functions than RS-232, but those that are common are compatible. Twenty two of the twenty five connector pins have designated functions, although few, if any, practical implementations use all of them. The most commonly used signals are also shown in Figure 5.17.

It is worth noting that for applications which use the 25-pin D-type connector there is often a problem in communication due to different handshaking signals employed by each system.

2.3.1. EIA-232-E Electrical Specifications

All EIA-232 circuits carry bipolar voltage signals with the voltage at the connector pins not to exceed ±25 V. Any pin must be able to withstand short circuit to any other pin without sustaining permanent damage. Each line should have a minimum load of 3 kΩ and maximum load of 7 kΩ which is usually part of the receiver circuit. A logic '0' is represent by a driven voltage of between +5 V and +15 V and a logic '1' of between -5 V and -15 V. At the receiving end a voltage of between +3 V and +15 V represents a '0' and a voltage of between -3 V and -15 V represents a '1'. Voltages between ±3 V are undefined and lie in the transition region. This effectively gives a 2 volt minimum noise margin at the receiver.

The maximum cable length was originally defined in RS-232C as 15 metres, however this has been revised in EIA-232-D and EIA/TIA-232-E and is now more correctly specified as a maximum capacitive load of 2500 pF. This equates to around 15 to 20 metres line length depending on cable capacitance.

As mentioned in an earlier section, EIA-232 specifies a maximum slew rate of the signal at the output of the driver to be 30 V/µs. This limitation is concerned with the problem of cross talk between conductors in a multiconductor cable. The faster the transition edge the greater the cross talk. This restriction together with the fact of the driver and receiver using a common signal ground and the associated noise introduced by the ground current severely limits the maximum data throughput.

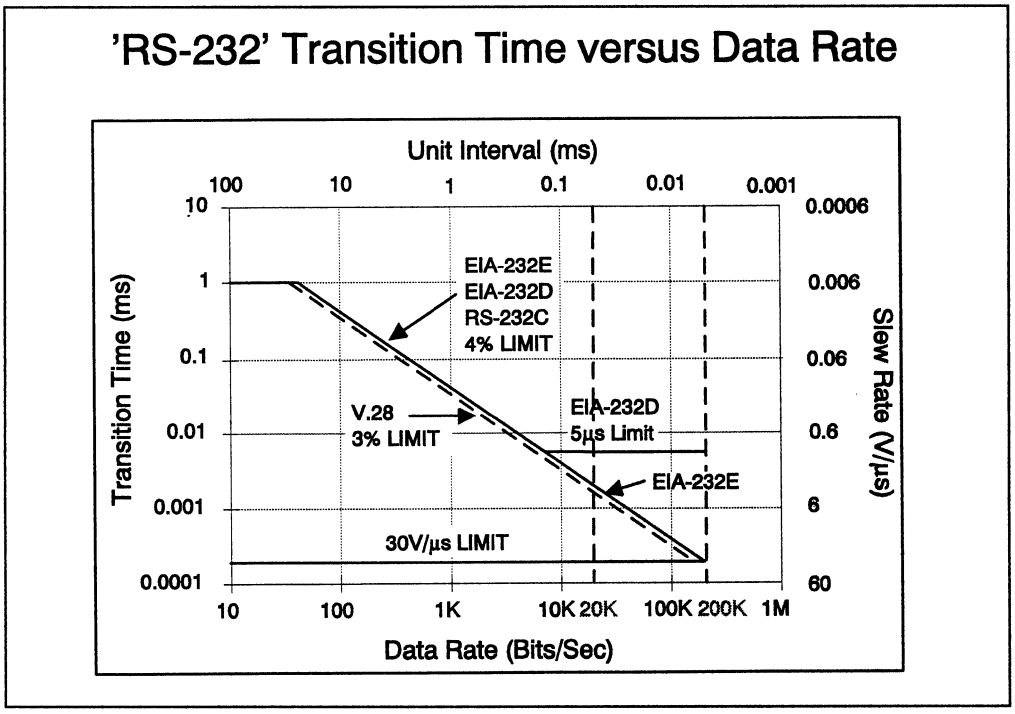


Figure 5.14 - 'RS-232' Transition Time versus Data Rate

For this reason the EIA-232 standard specifies a maximum data rate of 20 kbps. The standard also specifies the relationship between unit interval and rise time through the transition region (+3 V to -3 V) or t_T. This is the main difference between the 'E' and the 'D' revision. This is shown more clearly in Figure 5.14. EIA-232-D up to 8 kbps specified the relationship between transition time and unit interval or bit time t_b to be 4% maximum. Above 8 kbps this was relaxed to 5 µs maximum independent of the data rate. Both the 'C' and the 'E' revision specify the ratio of t_T/t_b to be 4% all the way up to 20 kbps. One can extrapolate this further, using the 4% figure and with the maximum slew rate of 30 V/µs, the maximum achievable data rate is 200 kbps however practically this is limited to around 120 kbps. A number of software programs operate at transfer rates of 116 kbps. Furthermore over longer line lengths the maximum drive current or short circuit current of the line driver becomes the dominant feature on data rate as against the 30 V/µs slew rate. As the line length increases the load capacitance also increases requiring more current to maintain the same transition time. The curves shown in Figure 5.15 indicate the drive current required to maintain the 4% relationship at different data rates. In today's low power systems, this level of output current is not sustainable at above say 20 kbps. In practice the line length is usually limited to around 4 metres for the higher data rates. Most drivers can handle the higher transmission rates over this line length without seriously compromising supply current.

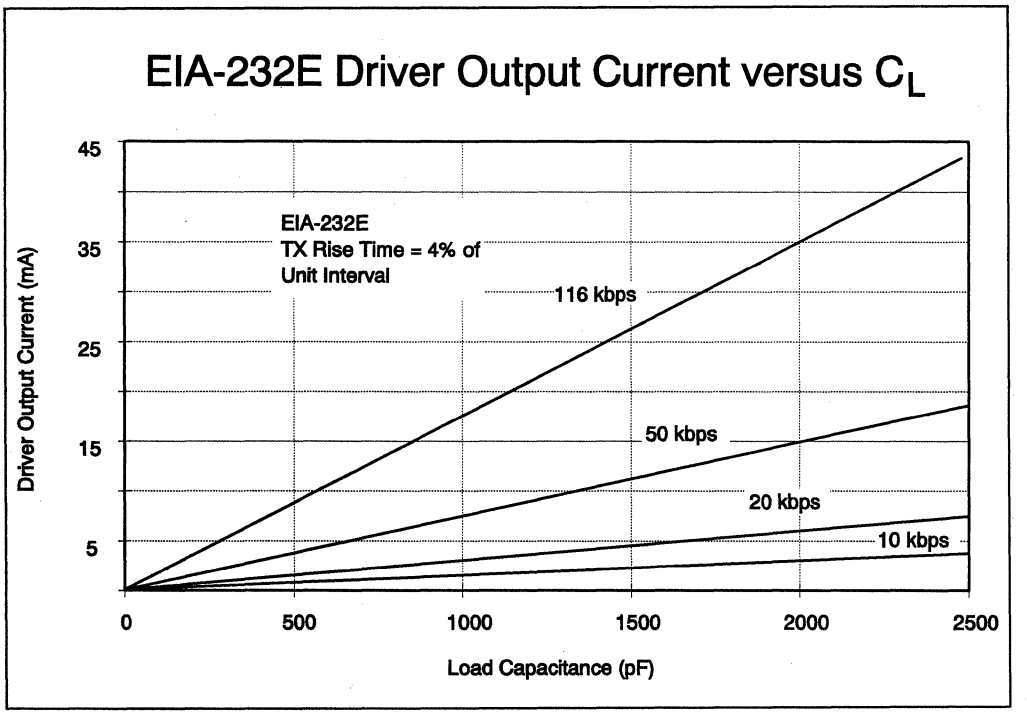


Figure 5.15 - EIA-232-EDriver Output Current versus C_L

The curves shown in Figure 5.15 were generated using the following equation which is an approximate equation relating transition time t_T, line capacitance C_l, receiver input impedance R_i, driver short circuit current I_o, and the initial and final line voltage (-3 V and +3 V) of the transition region, V_i and V_f respectively,

$$t_T = R_i \times C_l \times \ln\left[\frac{|R_i \times I_o| + |V_f|}{|R_i \times I_o| - |V_i|}\right]$$

Turning this equation around with respect to C_l, and cancelling R_i, V_i and V_f we get:

$$C_l = \frac{1}{3} \times \frac{t_T}{\ln\left[\frac{I_o + 1}{I_o - 1}\right]} \text{ nF}$$

The voltage levels, V_f and V_i, used in this equation are the extremes of the transition region. Assuming a typical driver short circuit current of 20 mA and a receiver input resistance of 5 kΩ, the typical time taken to pass through the transition region would be :-

$$t_T = 300 \times C_l \qquad \text{seconds.}$$

This equation can be manipulated further to gain a relationship of unit interval with line length in terms of load capacitance and short circuit driver current. The equation in Figure 5.16 assumes conformance to the 4% rule.

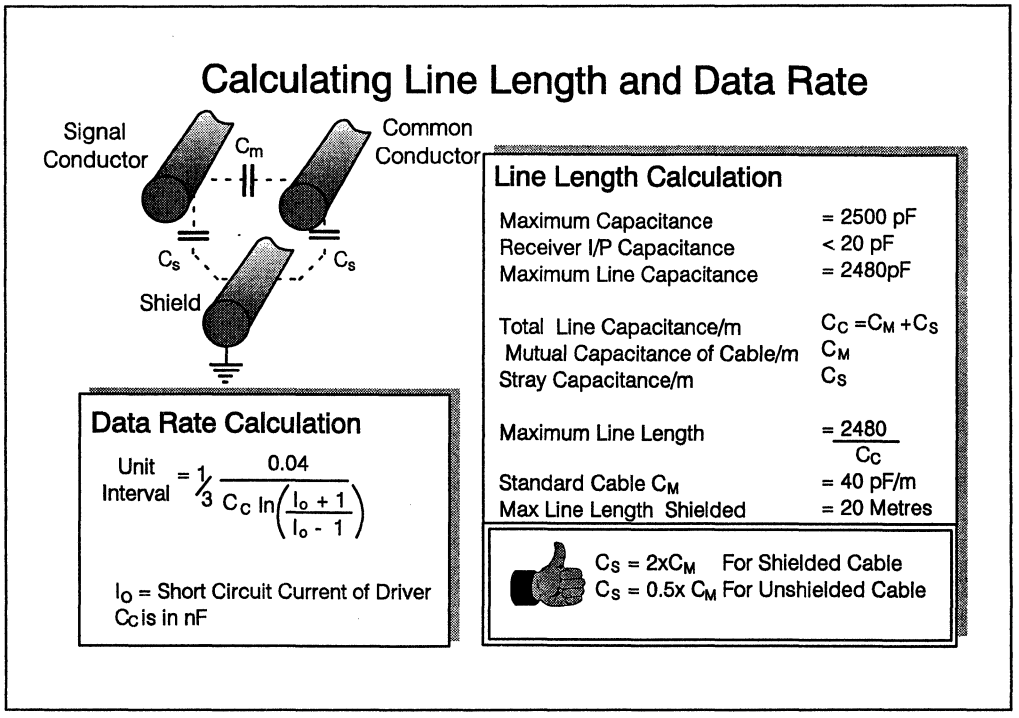


Figure 5.16 - Calculating Line Length and Data Rate

2.3.2. Calculating maximum line length

So far we have discussed line length in terms of load capacitance. For practical purposes we must now consider turning this value for load capacitance into true line length. The standard states a maximum line capacitance of 2500 pF. The input capacitance of a receiver is say 20 pF which leaves 2480 pF as the maximum line capacitance.

We must now consider the type of cable to be used. Standard EIA-232 cable as supplied by a number of manufacturers has a mutual capacitance of approximately 40 pF per metre. In addition to this we must add the stray capacitance. Stray capacitance varies considerably on whether the line is shielded.

For non shielded cable the stray capacitance is approximately half the mutual capacitance, for shielded cable it is double the mutual capacitance. As can be seen from Figure 5.16, for shielded cable the maximum line length is 20 metres, with unshielded cable it is over 40 metres.

2.3.3. The DB9S Connector

As mentioned earlier today's notebook and laptop PCs, with their quest for reduced size, no longer use the standard 25-way D-type connector detailed in the standard but have substituted it for a 9-way D-type. This is commonly known as the DB9S connector. Like the 25-way, the DCE equipment connector is a male outer casing with female connection pins, and the DTE is a female outer casing with male connecting pins.

As the interface is now made up of only nine pins the handshaking lines have been reduced accordingly but still are sufficient for most applications. Figure 5.17 shows the pins assignments for the interconnect cable into the DTE connector. An explanation of the function of each signal is given below:

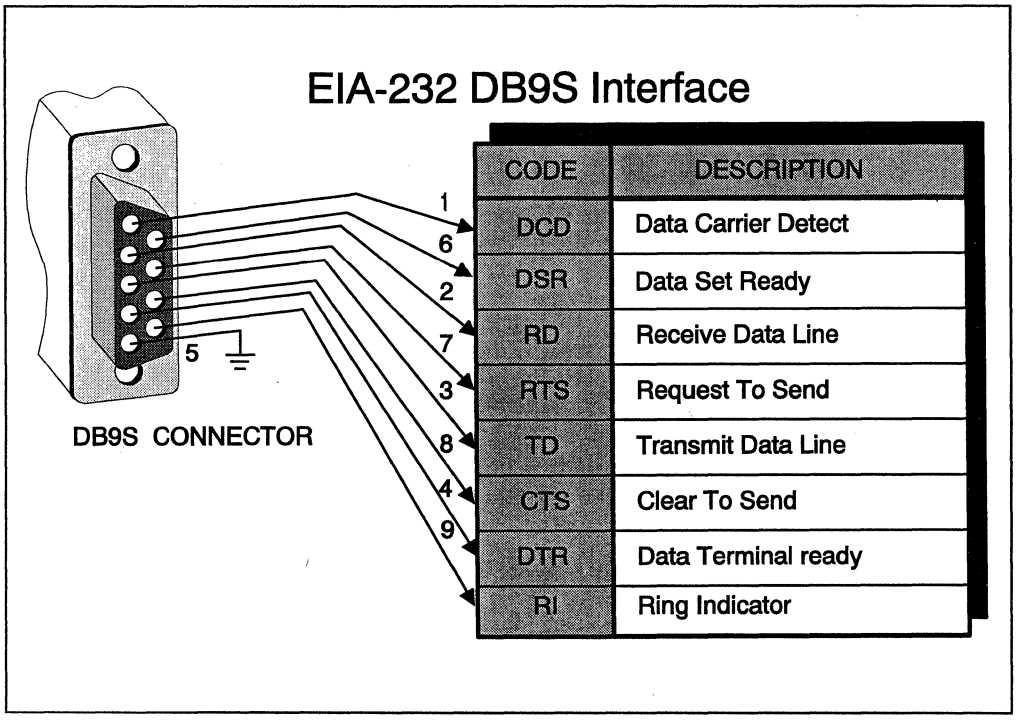


Figure 5.17 - EIA-232 DB9S Interface

Data Carrier Detect (DCD) - Received Line Signal Detector

The ON condition on this signal line as sent by the DCE informs the DTE that it is receiving a carrier signal which meets its suitability criteria from the remote DCE. In modems, this circuit is held on as long as it is receiving a signal that can be recognised as a carrier. On half duplex channels, DCD is held off when RTS is in the on condition.

Data Set Ready (DSR)

This is a signal turned on by the DCE to indicate to the DTE that it is connected to the line.

Receive Data Line (RD)

The signals on the RD line are in serial form . When the DCD signal is in the off condition the RD line must be held in the Mark state.

Request to Send (RTS)

This signal is turned on by the DTE to indicate it is now ready to transmit data. The DCE must then prepare to receive data. In half duplex operation, it also inhibits the receive mode. After some delay the DCE will turn the CTS line on to inform the DTE it is ready to receive data. Once communication is over and no more data is transmitted by the DTE, RTS is then turned from on to off by the DTE. After a brief time delay to ensure all data has been received that was transmitted, the DCE turns CTS off.

Transmit Data Line (TD)

The signals on this circuit are transmitted serially from DTE to DCE. When no data is being transmitted the signal line is held in the Mark state. For data to be transmitted, DSR, DTR, RTS and CTS must all be in the on state.

Clear to Send (CTS)

This signal is turned on by the DCE to indicate to the DTE that it is ready to receive data. CTS is turned on in response to simultaneous on condition of the RTS, DSR and DTR signals.

Data terminal Ready (DTR)

This in conjunction with DSR indicate equipment readiness. DTR is turned on by the DTE to indicate to the DCE it is ready to receive or transmit data. DTE must be in the on condition before the DCE can turn on DSR. When DTR is turned off by the DTE, the DCE is removed from the communication channel following the completion of transmission.

Ring Indicator (RI)

The ring indicator is turned on by the DCE while ringing is being received and is a term left over from the use of the standard in telephone line modem applications. Primarily used in auto-answer systems.

Signal Ground (pin 5)

This is the ground which provides the common ground reference for all the interchange circuits and is separate from the protective ground. The protective ground is electrically bonded to the equipment frame and is usually directly connected to the external ground. Any static discharges are then routed directly to ground without affecting the signal lines.

While all these pins are assigned, once again not all equipment uses every pin. Consider the mouse which can use as few as 4 lines, Signal ground, RI, TD and RD. Most equipment does however utilise a minimum of RTS, DTR, TD, RD, CTS and DSR.

Also of note is the usage of the DTE interface. The majority of equipment uses this interface and makes use of the null modem as a means of communication between DTEs. The null modem makes use of feeding back the RTS signal to the CTS line on each interface, Figure 5.17.1 details the connections for implementing a full null modem for the DB9S connector.

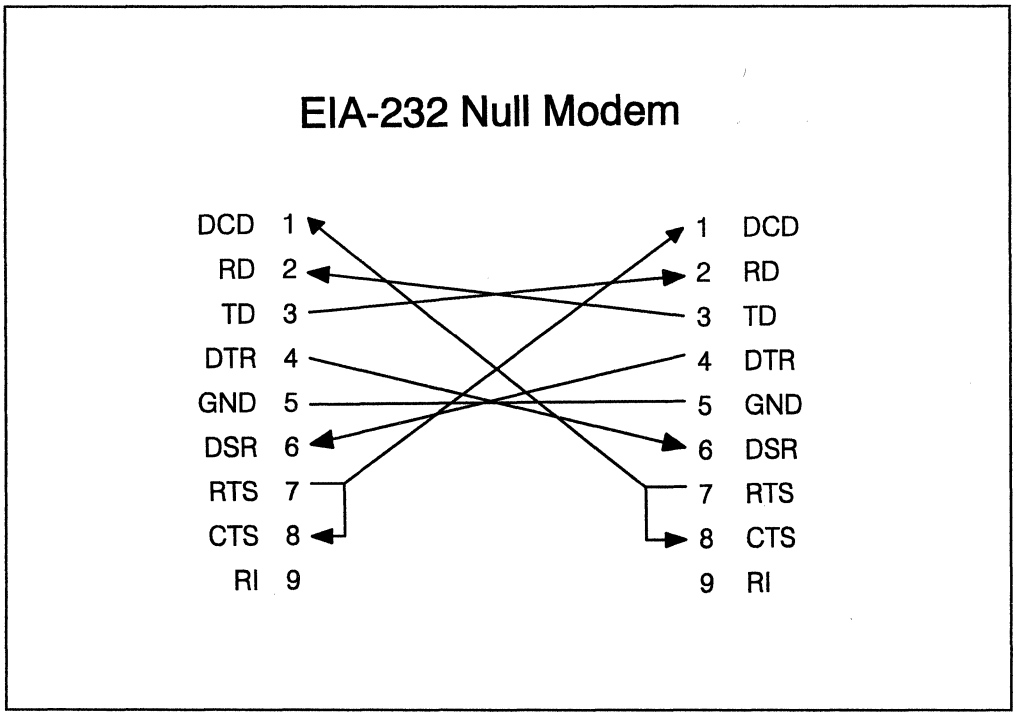


Figure 5.17.1 - EIA-232 Null Modem

2.4.SN75C185: Optimised PC Interface

If we study the DB9S DTE interface further we see there are 3 transmit lines and 5 receive lines. This is an awkward combination for the standard EIA-232 IC configurations in use today. Consider the ubiquitous SN75188 and SN75189 quad drivers and receivers. To implement this interface would require 3 ICs, one '188 and two '189s. Equal combinations of drivers such as the triple driver/receiver of the SN75C1406 still requires two chips to implement the interface.

For this reason TI has developed the SN75C185. By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly optimised solution can be

provided – the SN75C185 is just that. The SN75C185 integrates three drivers and five receivers and includes the necessary capacitors for driver slew-rate limit (30 V/μs) and receiver filter implementation, all in a single 20-pin package

The designer's dilemma is eased further by the use of a flow-through pin out architecture, see Figure 5.18. By aligning one side of the SN75C185 with the pins of the DB9S connector and the other to industry standard ACEs or UARTs, printed circuit board (PCB) layout can be greatly simplified.

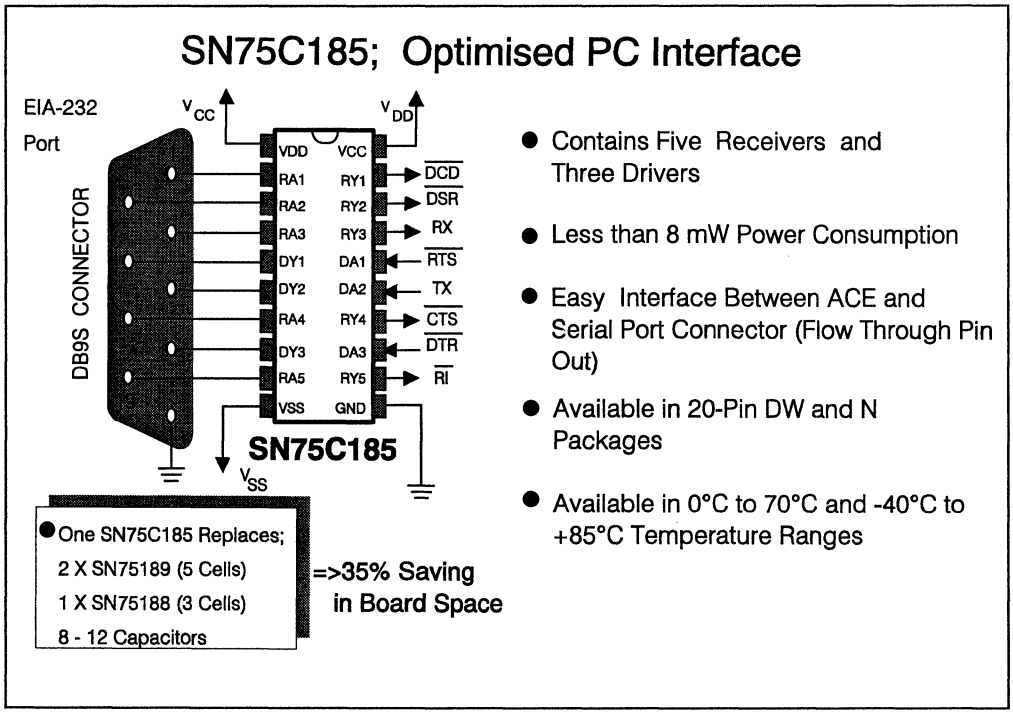


Figure 5.18 - SN75C185; Optimised PC Interface

2.4.1. Low Power as Well

In common with all of Texas Instruments BiMOS products, these devices combine the benefits of Bipolar's drive capability and robustness along with the low-power consumption of CMOS. This power saving, when compared to the alternatives is calculated in the following pages and is illustrated graphically in Figure 5.19.

Available in either a single 20-pin, wide-bodied SO pack or DIP pack, the SN75C185 offers designers greater than 25% saving in board space, compared to alternate solutions.

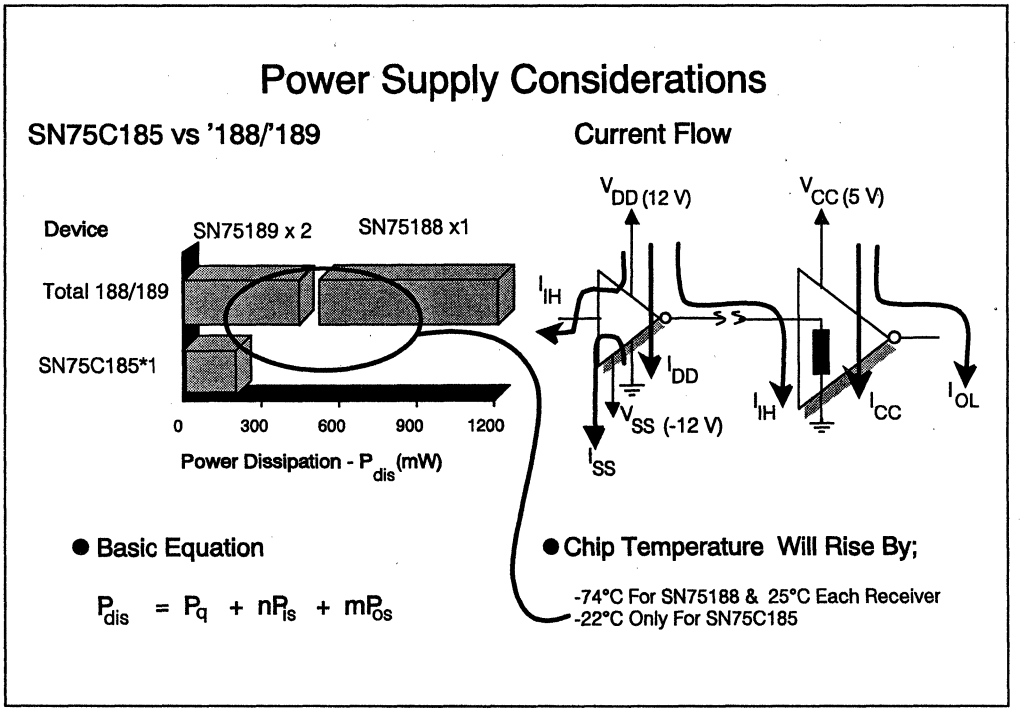


Figure 5.19 - Power Supply Considerations

2.4.2. SN75C185; Power Considerations

System power consumption is often considered very late in the design cycle. Of even more concern is that the power consumption of the interface circuitry, being the least attractive circuit to design, is often totally overlooked. The consequences of this can be catastrophic especially when using devices in confined spaces. These areas will normally have very poor air circulation, causing the ambient temperature of the whole system to increase.

These types of problems are particularly difficult to diagnose as failure can often be intermittent as devices pass into and out of thermal shutdown.

For these reasons, low quiescent-power devices are becoming a necessity for modern applications. As digital technologies advance, their power consumption decreases, making the interface circuits the limiting factor as far as system power consumption is concerned.

2.4.3. Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of EIA-232 require one quad-driver package and two quad-receiver packages; in the driver chip, one device is redundant while in

the receiver chips, three devices are redundant. These devices would, however, still be taking their quiescent current and hence wasting power. In order to provide the interface signals, three integrated circuits were required while only two-thirds of the capability was being used. The calculations below demonstrate this difference.

When comparing the 'C185 solution to that provided by the SN75188 and SN75189 devices, the power saving is enormous.

Both implementations require three supply voltages; a 5 V and ±12 V supplies. The power dissipated, P_{dis}, within each device is the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{os}, (when it is driving the line).

Hence,

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

Where n is the number of active input stages and m is the number of active output stages.

SN75188/SN75189 Combination

Using an SN75188 for the driver, the quiescent power consumption would be 576 mW. In addition to this the power dissipated in the input stage, P_{isd}:-

$$P_{isd} = V_{CC} * I_{IL}$$

$$= 12 * 1.6 \text{ mW}$$

$$= 19.2 \text{ mW}.$$

This is multiplied by four to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems that could be introduced by leaving the input floating.

The power dissipated in the output stage, P_{osd}, is:

$$P_{osd} = (V_{CC} - V_{OH}) * \frac{V_{OH}}{R_L}$$

$$= (12 - 9) * \frac{9}{3} \text{ mW}$$

$$= 9 \text{ mW}.$$

This figure will be multiplied by three to take into account the active three drivers driving the interface line. These sum up to give a total power dissipation of

$$P_{dis} = 576 + 4 \times 19.2 + 3 \times 9 \text{ mW}$$

$$= 680 \text{ mW}.$$

The junction temperature of a DIP device would have risen by 74°C.

Using the SN75189 receivers, a quiescent power of 130 mW would be dissipated by each package. This would be multiplied by two to take into account both chips.

The power dissipated in the output stage has a similar equation to that of the driver.

$$P_{osr} = V_{OL} * I_{OL}$$
$$= 0.45 \times 10 \text{ mW}$$
$$= 4.5 \text{ mW}$$

This power dissipated is multiplied by five to take into account the five receivers being used. The input stage can also dissipate some power, but this power is not supplied by this part of the interface system. The power dissipated within the IC will however cause the junction temperature to rise.

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$
$$= \frac{9^2}{3} \text{ mW}$$
$$= 27 \text{ mW}$$

This power dissipation is then multiplied by five. The remaining receivers will require tying to a state where they will not be susceptible to noise. Tying them to the 5 V supply increases the power dissipation by a further 8.3 mW per receiver.

Assuming three receivers in one SN75189 are being used and two receivers in the other, the power dissipated for the first receiver is:

$$P_{dis} = 130 + 4 \times 27 + 3 \times 4.5 \text{ mW}$$
$$= 233 \text{ mW}.$$

The power dissipated in the second receiver is:-

$$P_{dis} = 130 + 4 \times 27 + 2 \times 4.5 \text{ mW}$$
$$= 210 \text{ mW}.$$

This raises the temperature of the first and second receiver by 25°C and 23°C, respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, equalling **1.12 W.**

Using the SN75C185

The power dissipation of the SN75C185 can be calculated in a similar manner. The quiescent-power consumption of the SN75C185 is equal to:-

$$P_q = V_{DD} * I_{DD} + V_{SS} * I_{SS} + V_{CC} \times I_{CC}$$
$$= 12 * 200 + -12 \times -200 + 5 \times 750 \quad \mu W$$
$$= 8.55 \text{ mW}$$

The power dissipated in the input stage of the driver is:-

$$P_{isd} = V_{DD} \times I_{IL}$$
$$= 12 \times 1 \ \mu W$$

$= 12\ \mu W.$

This is multiplied by three to take into account all of the drivers.

The power dissipated in the output stage of the driver, P_{osd}, is:

$$P_{osd} = (V_{DD} - V_{OH}) \times \frac{V_{OH}}{R_L}$$

$$= (12 - 10) \times \frac{10}{3} \text{ mW}$$

$= 6.67$ mW.

This is multiplied by three to take into account the three drivers driving the interface line, giving a power dissipation of 20 mW.

The power dissipated in the output stage of the receiver has a similar equation to that of the driver, so:

$$Posr = V_{OL} \times I_{OL}$$

$= 0.4 \times 3.2$ mW

$= 1.28$ mW

This value is multiplied by five giving a total of 6.4 mW of power dissipated in the receiver's output stages. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the chip will however cause the junction temperature to rise.

The power dissipated in the input stage, P_{isr}, equals:

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$

$$= \frac{10^2}{3} \text{ mW}$$

$= 33.3$ mW

This power dissipation will also require multiplying by five. Giving a total input power dissipation of 167 mW.

Summing all the power contributors the total power dissipation is given by;

$$P_{dis} = P_q + 3P_{isd} + 3P_{osd} + 5P_{isr} + 5P_{osr}$$

$= 8.55 + 3 \times 12 \times 10\text{-}3 + 3 \times 6.67 + 5 \times 33.3 + 5 \times 1.28$ mW

$= 201$ mW.

The total power dissipated by the SN75C185 is **201 mW**

This is represents a tremendous power saving, especially when considering that the line is still being driven. The temperature rise within the SN75C185 would only be 22°C, enabling it to operate more reliably and with higher ambient temperatures.

2.4.4. On Chip Slew Rate Limiting

The EIA-232-E standard specifies a maximum slew rate through the transition region of **30 V/μs**. Relating this to capacitance and current only 100 μA of output current into 30 pF load capacitance is needed to exceed the slew-rate limit. All devices are capable of supplying more than 5 mA. Therefore if the slew rate limit is not to be exceeded, the switching speed of the driver's output stage needs to be reduced. An established solution is to place loading capacitors on the output of the driver. The value of the loading capacitor required will depend upon the line length, but it is generally in the order of 330 pF. The effect of this capacitor is to cause the output transistors to saturate, causing it to short circuit current limit, thus preventing fast switching edges.

There are some major problems with this established process; one being the variance in current at which the output short-circuit current limit operates, especially when taking temperature changes into consideration. Again the value of capacitance placed on the line will depend upon the driver's output short-circuit capability as well as line length. For example a device capable of sourcing 10 mA will need a total capacitance of 330 pF placed on its output to meet the 30 V/μs slew rate limit, while placing this value across a device capable of sourcing 4 mA will have its slew rate limited to less than 12 V/μs.

Another problem encountered is the increase in power dissipation through the output stage. The output voltage of the driver will normally be close to one supply rail, so when it tries to switch to the other, the active transistor will have almost all of the supply voltages across it. The extra external capacitor will clamp the driver's voltage close to the supply voltage causing the output transistor to source large amounts of current. The combination of a large source current and large voltage cause it to dissipate large amounts of power. Operating at these prolonged bursts of high current will ultimately increase the chip temperature which in turn can affect the long-term life of the device. Bipolar technologies are normally much better able to withstand such effects

A better solution, and that employed by the drivers in the SN75C185, is to place the slew-rate limiting within the chip itself. Using similar techniques to those employed for slew-rate-limited operational amplifiers, the slew rate of line drivers can also be limited. Using the Miller capacitance multiplying effect, the slew rate of the driver can be slowed down. The on-chip capacitors are normally in the order of 5 pF, while the currents driving the on-chip capacitor are the order of micro amperes, thus reducing power consumption within the device. The biasing current to the output transistors is unaffected by this technique and will be more than sufficient to drive the 3 kΩ load as offered by the receiver.

2.4.5. Internal Noise Filtering

The standard states a maximum line cable capacitance of 2500 pF, which corresponds to an approximate line length of 20 metres. As the interface line gets longer, it becomes more susceptible to noise pick-up from the surrounding environment. This pick-up is due in part to the inductive nature of the line. As the signal switches, a rapidly changing magnetic field induces noise currents

into the line, thereby corrupting signal data. The level and cause of this noise will dictate the nature of solutions or precautions that should be taken.

For operation at high data rates, the use of a differential line might be the best solution. If however, a low cost and simple single-ended solution is required then standard EIA-232 devices can be modified to give noise protection. This is achieved by slowing down the response of the receiver's input stage, making them too slow to respond to fast switching noise pulses. Even small levels of input noise can falsely trigger the receiver. The maximum data rate specified in the standard is 20 kbps, corresponding to a minimum pulse period of 100 μs. Therefore in normal applications, most devices are far faster than the specification requires.

To slow down older bipolar receivers such as SN75189s, a capacitor, C_C, needed to be placed on each of its response control pins. This means an additional four capacitors per device, which can be awkward and costly. The effect of this response control capacitor is to set up a low-pass filter on the receiver's input. In order to provide large pulse rejection, the capacitor needs to be quite large. Furthermore, the filter response is asymmetric, affording protection against positive noise voltage spikes only, negative spikes are unaffected, and will tend to attenuate rather than reject short noise pulses.

Receivers in the SN75C185 integrate on-chip filtering which reject fast transient noise pulses. The on-chip filters are more precise than filters implemented using external passives. Consequently the receiver response is unaffected. These filters are totally symmetrical, offering protection against both positive and negative noise pulses and with the ability to reject rather than attenuate short noise pulses. To approach the level of filtering offered by the 'C185 receivers the standard '188 type receivers require much larger capacitors and even then fall well short of filtering requirements.

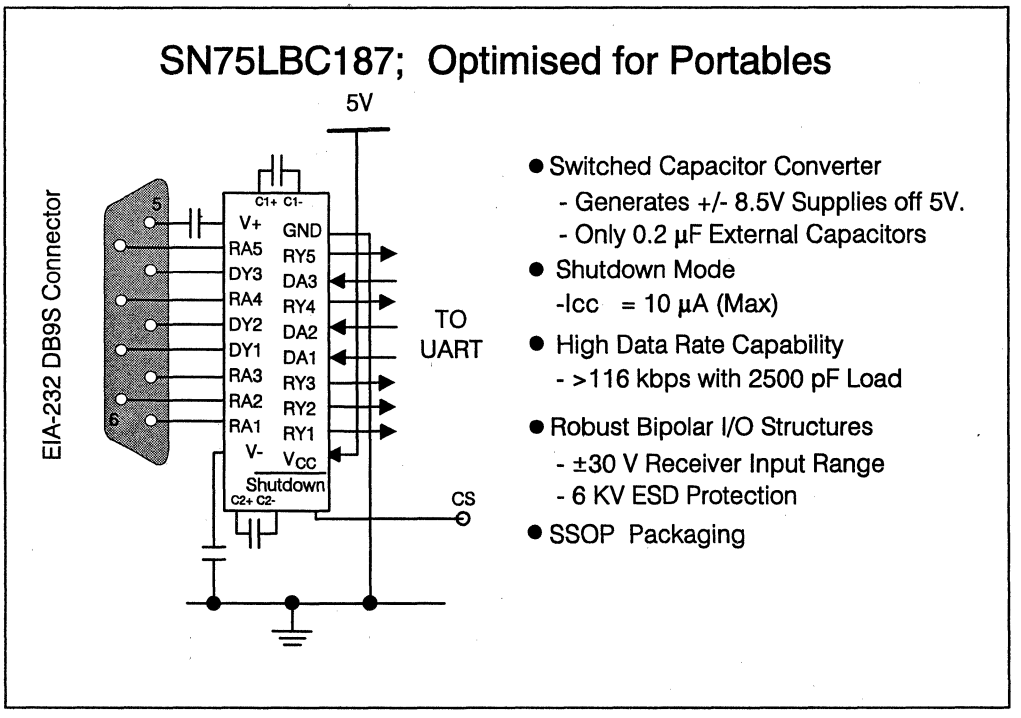


Figure 5.20 - SN75LBC187; Optimised for portables

2.5.SN75LBC187; Optimised for Portables

The SN75C185 is the ideal choice for computer applications where the bipolar supplies required by EIA-232 are available within a computer system. Most desk top computers generate ±12 volt supplies for powering the internal disk drive. However for portable equipment, e.g. laptops, notebooks, hand held measuring equipment, the EIA-232 interface may be the sole user of a negative supply. The cost of implementing a switch mode supply, using inductive switching regulators, to generate the negative supply can make this option unattractive. Switch mode supplies also have the draw back of increasing the EMI emissions, a factor becoming an increasingly important design constraint. Integrating a switch mode power supply on silicon would reduce the emissions, and has been the dream of semiconductor manufacturers, but thus far no one has yet managed to integrate the inductor.

An alternative way, and the basis of modern technology charge pumps, is to make switching regulators using capacitors. In essence they operate by applying charge to a capacitor via an input voltage and then adding, subtracting or inverting the voltage on the positive or negative voltage terminals. This charge is transferred into a holding reservoir capacitor that is then used to supply the

output voltages. Furthermore such a scheme can be integrated into silicon. Using a network of capacitors both voltage doublers and invertors can be made.

The SN75LBC187 integrates the charge pump on the same IC as the EIA-232 drivers and receivers. It is fabricated in TI's proprietary LinBiCMOS technology and contains three independent drivers and 5 independent receivers together with the switched-capacitor voltage converter. The SN75LBC187 provides a single 5 V supply interface between the asynchronous communications element (ACE or UART) and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standards EIA/TIA-232-E-1986 and EIA/TIA-562 and CCITT recommendation V.28.

The switched-capacitor voltage converter of the SN75LBC187 uses four small (0.2 μF) external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 5 V logic supply input. Like the SN75C185 the drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without sustaining damage. Furthermore the 'LBC187 is guaranteed to withstand up to 6KV ESD on any of its pins making it TI's most rugged EIA-232 product.

The device also features a reduced power or shutdown mode that virtually eliminates the quiescent power supply when the IC is not active.

The primary application for the 'LBC187 is for battery operated, portable equipment where power consumption is a key factor. A separate consideration, and one that usually goes hand in hand with these factors, is that of shear physical size. With the 'LBC187, TI has used the latest SSOP packaging to reduce board area to an absolute minimum. The new SSOP package reduces board space to 43% of the standard 28-pin SOIC package Couple this with the small 0.2 μF and you have the ideal single supply solution for space restricted applications.

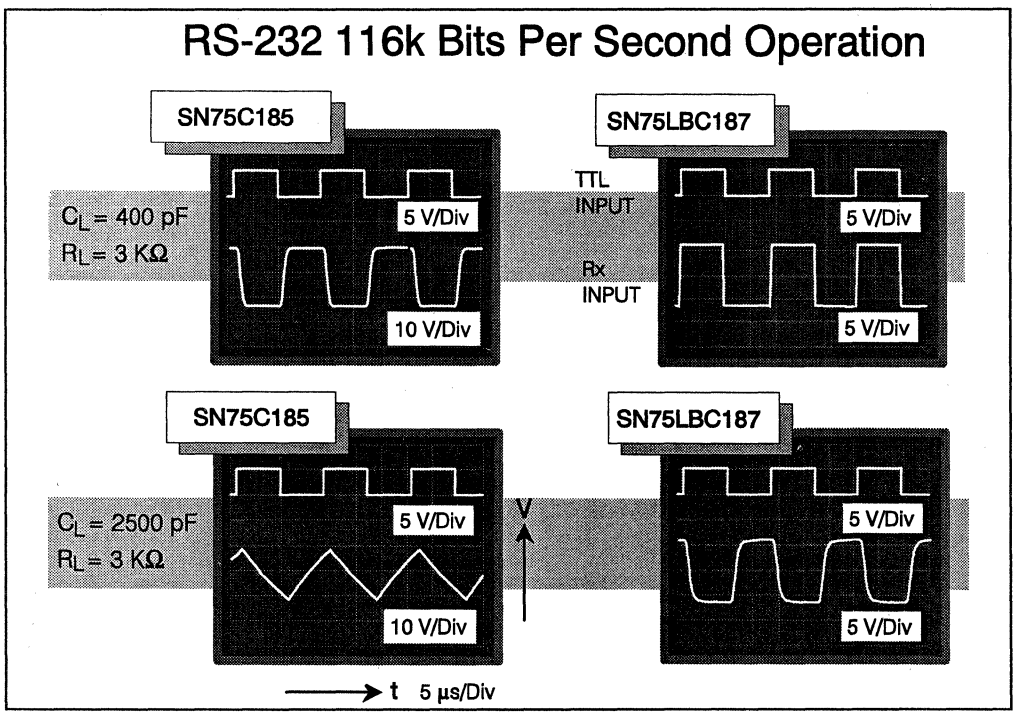


Figure 5.21 - RS-232 116k Bits Per Second Operation

2.5.1. SN75LBC187; 116 kbps operation

As discussed in section 2.3.1 the limitation on data rate is one of short circuit output current and the actual load capacitance. With the 'LBC187 the driver short circuit current, I_{OS}, is higher than say the SN75C185 and is therefore able to drive longer line lengths at higher data rates. Figure 5.21 illustrates this. The 400 pF load in the top half of the figure represents a cable approximately 3 metres long. As the 'scope traces show, the 'C185 produces a perfectly acceptable output trace at 116 kbps. Similarly with the 'LBC187 trace.

If the line length is now upped to 20 metres or 2500 pF load, we can see how the short circuit current limit now limits the slew rate. With the 'LBC187 the trace is still acceptable and will provide reliable data transmission. With the 'C185, the data will still be transmitted but the probability of error is now increased. Most software programs that operate 116 kbps, e.g. Laplink™ (Laplink is a trademark of Travelling Software Inc.) provide the interconnect cable as part of the system. In most cases this cable is less than 3 metres in line length so either the 'C185 or 'LBC187 would be able to transmit data reliably. It is interesting to note that both devices would meet EIA-232-D if the rise time to unit interval relationship was extrapolated, however both would fail EIA-232-E. Of course conformance to EIA-232 is not relevant above 20 kbps.

2.5.2. Conformance to EIA-562

A new standard has recently been introduced in an attempt to provide a low power standard for 5 volt systems and also to increase the data rate over EIA-232. Known as EIA-562, the standard increase the maximum data rate from 20 kbps to 64 kbps and facilitates lower driver voltages. The downside is the reduced noise margin at the receiver. The specification also details the rise time and ripple conditions of the driver. The SN75LBC187 is fully conformant to this standard.

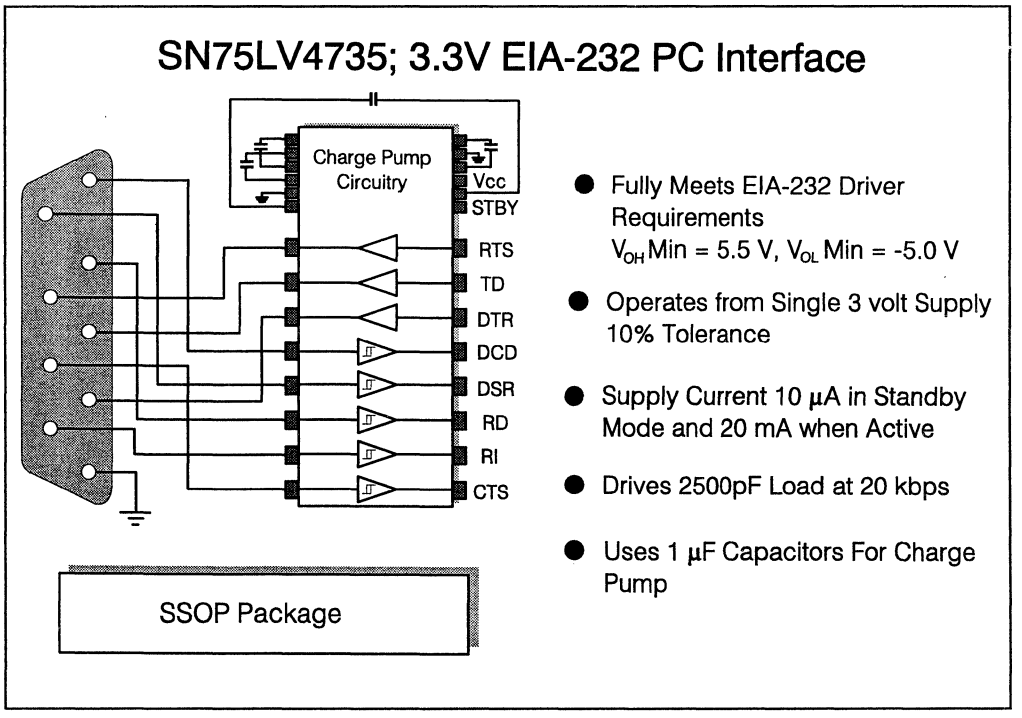


Figure 5.22 - SN75LV4735; 3.3V EIA-232-E PC Interface

2.6.SN75LV4735; 3 Volt EIA-232 PC Interface

Continuing the move to lower power systems the obvious choice is to reduce the supply voltage of the system. Assuming supply current remains constant power dissipation is instantly reduced. The driving force behind this reduction is once again the notebook type PC equipment. To facilitate the move to 3 Volts, TI has introduced the SN75LV4735. From 3 volts the device is still capable of producing the required V_{OH} and V_{OL} for conformance with EIA-232.

Once again the device is designed specifically for the DB9S PC DTE interface containing 3 drivers and 5 receivers for a single package solution.

The device is packaged in the TSSOP package with a board area of only 22 mm^2 and a maximum package height of 1 mm.

2.7.ACEs (UARTs) From Texas Instruments

Most EIA-232 systems use dedicated communication controllers. Termed ACEs (Asynchronous Communication Elements) or UARTs (Universal Asynchronous Receiver Transmitter), these devices are responsible for controlling the exchange of information over the EIA-232 interface.

The ACE

The ACE is a dedicated asynchronous communications controller designed to off load most of the communication activities from the CPU, thus freeing the CPU for other activities. It has the ability to add or delete start and stop bits and provide odd/even parity code generation and detection. Industry standard devices such as the **TL16C450** family contain many extra features as listed below:

- **Programmable bps-rate generator**
- **Adds and deletes standard asynchronous communication bit**
- **Fully programmable serial interface characteristics**
- **Data communication diagnostic capability**
- **Modem-control functions**
- **Simple interface to microprocessors**
- **Maximum data rate of 256 k bits per second**

All devices are designed using Texas instruments EPIC™ CMOS process and operate from a single 5 V supply. The **TL16C450** is the most common choice for standard PC applications as well as many other asynchronous serial applications. The TL16C450, housed in a 40-pin package, contains all the necessary facilities for implementing a single asynchronous serial port. The CPU within the system can read and report on the status of the ACE at any point in the ACEs operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered, parity, overrun etc.

The TL16C450 ACE includes a programmable, on-board, bps-rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2^{16} -1) and producing a 16 x clock for dividing the internal transmitter logic. Provisions are included to use this 16 x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimise the computing required to handle the communications link. The **TL16C451** is similar to TL16C450 with the single serial port, but also contains a Centronix parallel printer port. The IBM PC AT/XT sets the standard for this parallel printer interface that all "compatible" manufactures have to follow. TTL-level signals are presented on a 25-pin D-type socket. Apart from the choice of connector, this parallel printer port is directly compatible with the "Centronix" standard printer interface. The **TL16C452** has two serial ports plus a parallel Centronix printer port. Using this ACE together with two SN75C185s provides a simple three chip complete solution for the two EIA-232 ports plus a printer port that is common on basic PC configurations.

EPIC is a trademark of Texas Instruments Incorporated

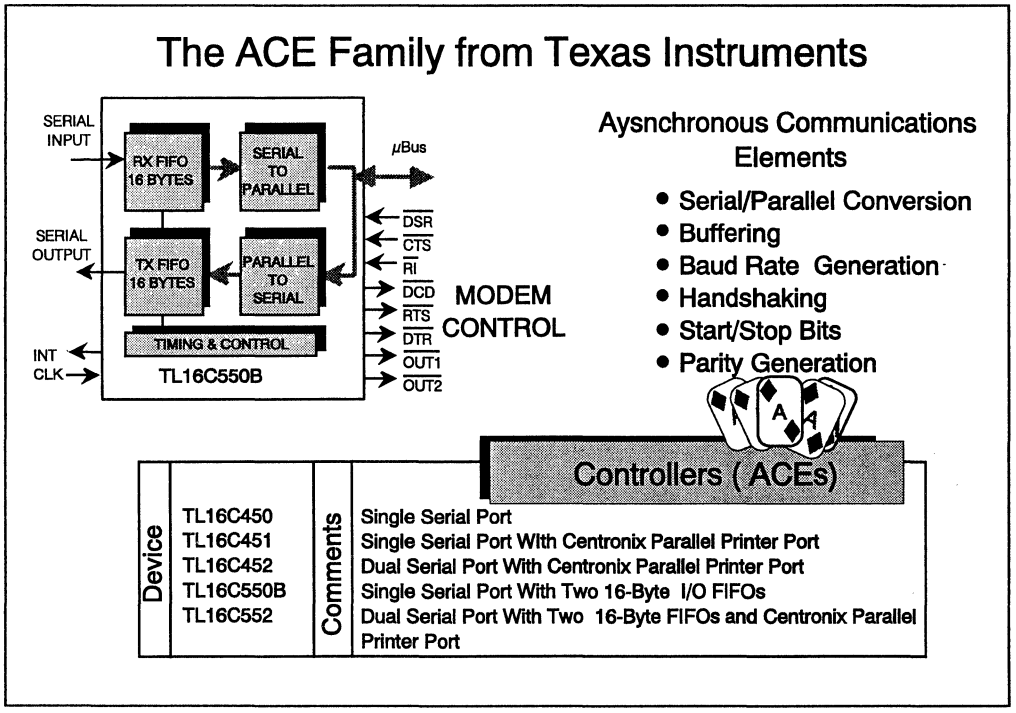


Figure 5.22.1 - The ACE Family from Texas Instruments

2.7.1. The FIFO (First-In-First Out)

The CPU can send data at much faster rates than a normal ACE can handle. This is particularly true for today's multitasking applications that demand high performance microprocessors. This can be expensive in CPU overheads as the CPU will be tied to the speed of the serial interface, i.e., data will be transferred over the interface through the ACE and onto the CPU bus. This is true also when the data is exchanged from the CPU to interface via the ACE.

Devices like the **TL16C550B** and **TL16C552** alleviate this problem by including buffer registers and FIFOs in series with the ACE's transmitter and receiver. These are quick access registers that hold data until the CPU can be freed. The CPU can then execute a block read or write.

The ACE is, in effect, isolated from the slow communications channel.

The TL16C550B is similar to the TL16C450, but two 16-byte FIFOs are included to buffer the transceiver and receiver data stream, further reducing the number of interrupts from the microprocessor.

2.7.2. Forward-Looking Performance With Backward Compatibility

By allowing two modes of operation, the TL16C550B allows users to maintain software compatibility with earlier industry standard ACEs such as the TL16C450. In addition to the TL16C450 mode, the TL16C550B can operate in the FIFO mode. In FIFO mode, two 16-byte FIFOs (First-In-First-Out) are enabled to relieve the CPU of excessive software overheads. The independent receive and transmit FIFOs act as buffers, vastly reducing the number of interrupts required. Furthermore two dedicated pins serve as handshaking lines to a DMA (Direct Memory Access) controller, thus allowing the FIFOs to load and unload data without direct intervention from the CPU.

The flagship of the range is the TL16C552, which is similar to the TL16C452 in structure but with the added advantage of input/output FIFOs as in the TL16C550B

This device serves two serial input/output interfaces simultaneously in either microcomputer or microprocessor-based systems. In addition to its dual asynchronous serial communication capabilities, the TL16C552 provides a fully bi-directional parallel data port that fully supports the parallel Centronix-type printer. The parallel port and the two serial ports provide IBM PC/AT compatible computers with a single low-power device to serve the three-port system. Like the TL16C550B, the TL16C552 contains 16-byte receive and transmit FIFOs that act as buffers to reduce the number of interrupts on the CPU. Also in common with the TL16C550B, the device contains two pins for each ACE that serve as handshaking lines for DMA control. The TL16C552 is housed in a 68-pin plastic-leaded chip carrier, PLCC.

Integration of FIFO and DMA signalling circuitry onto a single chip makes the TL16C550B and TL16C552 one of the most efficient solutions for higher performance multitasking systems.

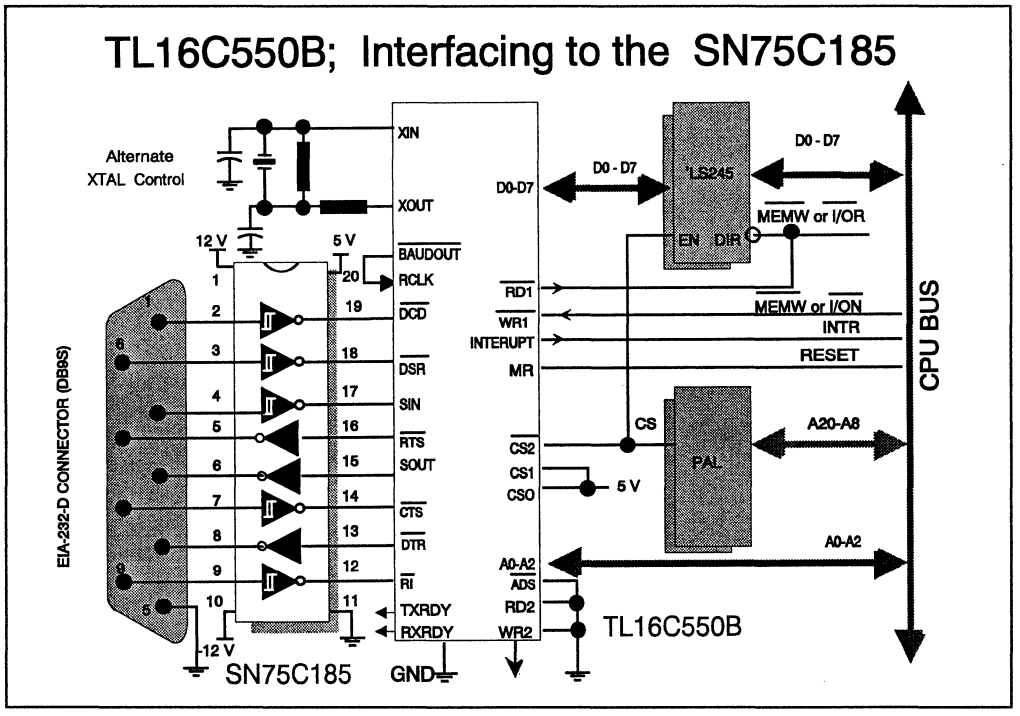


Figure 5.22.2 - TL16C550B; Interfacing to the SN75C185

2.7.3. Interfacing Between the TL16C550B and the SN75C185

The circuit shown demonstrates the simplicity, in hardware terms, in implementing an asynchronous serial interface with the SN75C185 driver/receiver and the communications controller TL16C550B.

When interfacing between the TL16C550B ACE and the Intel CPU bus, minimal glue logic is required. Namely an 'LS245 Octal bus transceiver is used to provide drive current to an 'off-card' CPU, and programmable array logic (PAL) to decode address lines and generate a chip select signal. While an exhaustive description of this interface is beyond the scope of this section, a discussion of key interface lines can be useful.

Xin/Xout:
External clock. Connects the ACE to the main timing reference (clock or crystal).

$\overline{\text{baudout}}$,RCLK:

The transmitter reference clock is available externally via the $\overline{\text{baudout}}$ pin. In this application bpsout is fed into the receiver clock to provide a timing reference for the receiver circuitry. Clock

rate is established by the reference oscillator clock frequency (xin) and divided by a driver specified by the bps generator divisor latches.

$\overline{\text{TXRDY}}$:

Transmitter Ready Output. This pin is used during DMA signalling.

$\overline{\text{RXRDY}}$:

Receiver Ready Output. This pin is also used during DMA signalling.

D0 to D7:
Databus. Eight 3-state data lines provide the bi-directional path for data, control, and status information between the ACE and CPU bus.

$\overline{\text{RD1}}$, RD2:

Read inputs. When either input is active (high or low respectively) during ACE selection, the CPU is allowed to read status information from the selected ACE register. Since only one of these inputs is required for the transfer of data during the read operation, RD2 is tied to its inactive state, i.e., low.

$\overline{\text{DCD}}$, $\overline{\text{DSR}}$, SIN, $\overline{\text{RTS}}$, SOUT, $\overline{\text{CTS}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$:

These signals are the EIA-232 compatible modem control lines. Devices such as the SN75C185 are employed to convert the TTL/CMOS level signals from the ACE to EIA-232 compatible bipolar voltages of between ±5 V to ±15 V. The signal can then be transmitted over distances of up to 15 m.

The advantages of the SN75C185 can be clearly seen by the simplicity of the interface connections. For example, driving/receiving combinations precisely match the interface requirement, plus the pin-out is aligned directly to the DB9S connector.

$\overline{\text{WR1}}$, WR2:

Write inputs. A logic applied to $\overline{\text{WRI}}$, during ACE selection allows the CPU to write either control words or data into a selected ACE registers. WR2 is tied in active, i.e.: logic low.

INTERRUPT:
When active (high) the interrupt pin informs the CPU that the ACE has an interrupt to be serviced. This interrupt could occur for one of four reasons;

- **Receiver error**
- **Received data available or time-out (FIFO mode only)**
- **Transmitter holding register empty**
- **Enable modem status interrupt**

The interrupt is reset (deactivated) either when the interrupt has been serviced or by a master reset (MR).

MR:
Master reset. When active (high), MR clears most ACE registers and sets the states of various outputs (i.e. interrupt).

CS0, CS1, $\overline{CS2}$:

Chip Select. An active low on the $\overline{CS2}$ pin selects the ACE. CS0 and CS1 must be tied active (high) to ensure proper functioning of the $\overline{CS2}$ chip select. A logic high on $\overline{CS2}$ will de-select the ACE.

A0 to A2:
Register Select. These three inputs are used during read or write operations to select the appropriate ACE registers. For example, providing the correct write/read operation had taken place at logic 0 at A2, A1, and A0 would cause the receiver buffer (read) or the transmitter buffer to write.

$\overline{ADS}$:

Address strobe. An active low on $\overline{ADS}$, the register select signals (A0 TO A2) and chip-select signal ($\overline{CS2}$) drive the internal logic directly.

2.8.EIA-232 Products Summary

In this section we have discussed devices which are concerned primarily with the DB9S connector. TI also has a wide range of other EIA-232 ICs which offer differing combinations of drivers and receivers which can offer the optimum solution for your system. The reader is advised to consult the current edition of Interface Circuits Data Book (Reference SLYD006) which contains a complete selection guide of EIA-232 products.

2.9.EIA-232 Selection Guide

Data Transmission Circuits

Function	Per Package	Type	Features
	2	SN75150	Industry Standard
		UA9636AC	Industry Standard
Line Driver	4	LT1030	Robust bipolar design, with 3-state driver outputs
		SN55188	–55°C to 125°C temperature range
		SN75188	Industry standard
		SN65C188	–40°C to 85°C temperature range
		SN75C188	Low-power BiMOS
		SN65C198	–40°C to 85°C temperature range
		SN75C198	Low-power BiMOS with sleep-mode

Line Receiver	4	SN75154	Industry standard
		SN55189	-55°C to 125°C temperature range
		SN75189	Industry standard
		SN55189A	-55°C to 125°C temperature range
		SN75189A	-55°C to 125°C temperature range
		SN65C189	-40°C to 85°C temperature range
		SN65C189A	-40°C to 85°C temperature range
		SN75C189	Low-power BiMOS
		SN75C189A	Low-power BiMOS

Continued Over.....

Data Transmission Circuits (Continued)

Function	Per Package	Type	Features
Line Driver / Receiver	1/1	SN75155	On-chip 5-v regulator
	2/2	MAX232	On-chip charge pump
	2/2	LT1080	On-chip charge pump and 3-state outputs
	2/2	LT1080	On-chip charge pump
	3/3	LT1039	Robust bipolar design, with 3-state outputs
	3/3	SN65C1406	–40°C to 85°C temperature range
	3/3	SN75C1406	Low-power BiMOS
	4/4	SN75186	Robust bipolar design, with loopback
	4/4	SN65C1154	–40°C to 85°C temperature range
	4/4	SN75C1154	Low-power BiMOS
	3/5	SN65C185	–40°C to 85°C temperature range
	3/5	SN75C185	Optimised for DB9S (9-pin) connector
	3/5	SN75LV4735	3 volt operation
	3/5	SN75LBC187	Optimised for Laptop Applications¥

Control Circuits

Function	Type	Features
ACE+	TL16C450	Single ACE
	TL16C451	Single ACE with parallel port
	TL16C452	Dual ACE with parallel port
	TL16C550B	Single ACE with FIFO§
	TL16C552	Dual ACE with parallel port and FIFO

Notes

+ ACE: Asynchronous Communications Element.

§ FIFO: First In First Out.

¥ Product currently under development, contact TI representative for further details.

3. Interface Circuits for RS-485

3.1. The Need for Balanced Transmission Line Standards

This section focuses on industry's most widely used balanced transmission line standard, the EIA RS-485. After reviewing key aspects of the standard, the reader will be introduced to the practicalities of implementing a differential transmission scheme based on a factory automation example. Finally, new additions to Texas Instruments EIA product range will be discussed along with their application, where appropriate.

Data transmission between computer system components and peripherals over long distances and under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-485 is a balanced (differential) digital transmission line interface developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations. The advantages are;

- **Data rate - to 10 Mbps and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

3.1.1. Application Areas

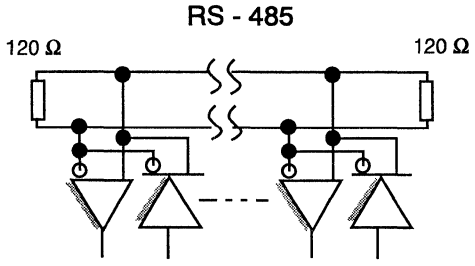
RS-485 is an upgraded version of RS-422-A extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bi-directional multi-point party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the physical layer specification of their standard. Examples include the ANSI (American Nationals Standards Institute) Small Computer Systems Interface (SCSI) which we will discuss in section 4, the Profibus standard, the DIN Measurement Bus.

3.1.2. EIA RS-485

The balanced transmission line standard EIA RS-485 was developed in 1983 to interface a host computer's data, timing or control lines to its peripherals. The standard specifies the physical layer only. Protocols, timing, serial or parallel data, connector choice are all left to be defined by the user

RS-485 Specification Highlights



- Up to 32 Unit Loads (typ)
- Half Duplex communication
- Protocol Not Included in Spec.

KEY PARAMETERS	SPEC. LIMITS
Maximum Common Mode Voltage	-7 V to + 12 V
Receiver Input Resistance	12 kΩ
Driver Load	60 Ω
Driver Output Short Circuit Limit	150mA to GND
	250 mA to -7 V or 12 V

Figure 5.23 - RS-485 Specification Highlights

RS-485 was originally defined as an upgrade and more flexible version of RS-422-A. Where RS-422 facilitates simplex communication only, RS-485 allows for multiple drivers and receivers on a single line facilitating half-duplex communication. Like RS-422 the maximum line length is not specified but, based on 24 AWG cable, is nominally around 1.2 km. Maximum data rate is unlimited and is set by the ratio of rise time to bit time, similar to EIA-232. In many cases it is the line length of the cable which limits the data rate more than the drivers due to transmission line effects, see section 1.

The differences between the RS-485 standard and the RS-422 standard lie primarily in the features that allow reliable multi-point communications.

3.1.3. RS-485 Driver features

i. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

ii. The driver output, off-state, leakage current should be 100 µA or less with any line voltage from -7 V to +12 V.

iii. The driver should be capable of providing a differential output voltage of 1.5 V to 5 V with common-mode line voltages from -7 V to 12 V.

iv. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

3.1.4. RS-485 Receiver features

i. High receiver input resistance, 12 kΩ minimum.

ii. A receiver input common-mode range of -7 V to 12 V.

iii. Differential input sensitivity of ±200 mV over a common-mode range of -7 V to 12 V.

3.2.Process Control Design Example

To fully understand the considerations of designing an RS-485 system it is advantageous to take a specific design example. In this case we will consider a factory automation system with a host controller and several out-stations. Each out-station is capable of transmitting as well as receiving data.

The general system specification is shown in Figure 5.24 and comprises:

i. Furthest out-station is 500 m from the host controller.

ii. We require up to 31 out-stations on the line. With the host controller this totals 32 stations in total.

iii. System data rate will be 500 kilobits per second.

iv. Only one cable will be used for data transmission operating in half duplex mode.

With this system specification the main design consideration are:

i. Line Loading including termination.

ii. Cable choice

iii. Signal Attenuation and distortion

iv. Fault Protection including fail safe operation

Consider each one of these points:

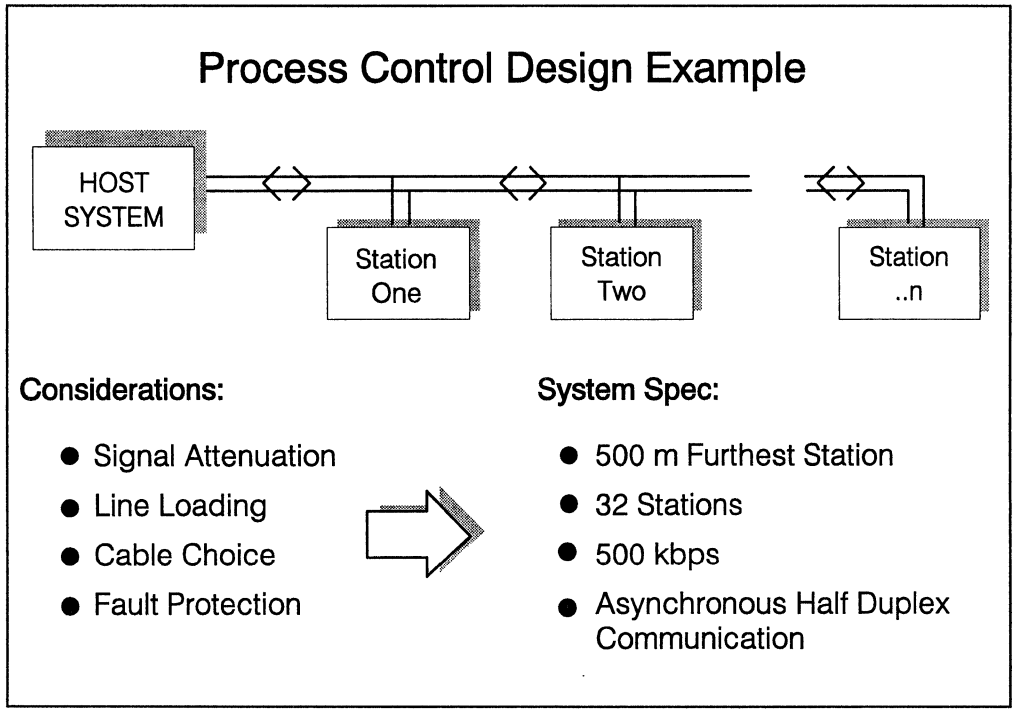


Figure 5.24 - Process Control Design Example

3.3.Line Loading

The RS-485 standard takes into account the need for line termination and the subsequent loading on the transmission line. The decision on whether to terminate or not will be system dependent and will be affected by the choice of line driver and the maximum line length.

Line Termination

As we discussed in section 1 the test for whether a transmission line is to be considered as a distributed parameter model or a lumped parameter model is dependent upon the relationship of signal rise time, t_T, at the receiving end and the propagation time of the signal down the cable. The threshold between the two types of transmission line is given by the following equation:

$$2t_{pd} = t_T$$

If we build a margin of error into this equation a better test is to determine the relationship of twice the rise time to 5 times the propagation delay:

If the relationship $2t_{pd} \geq 5t_T$ is true then the transmission line must be treated as a distributed parameter model and terminated accordingly. If the converse i.e. $2t_{pd} \geq \frac{t_T}{5}$ is true. the transmission line can be treated as a lumped parameter model and termination is not necessary.

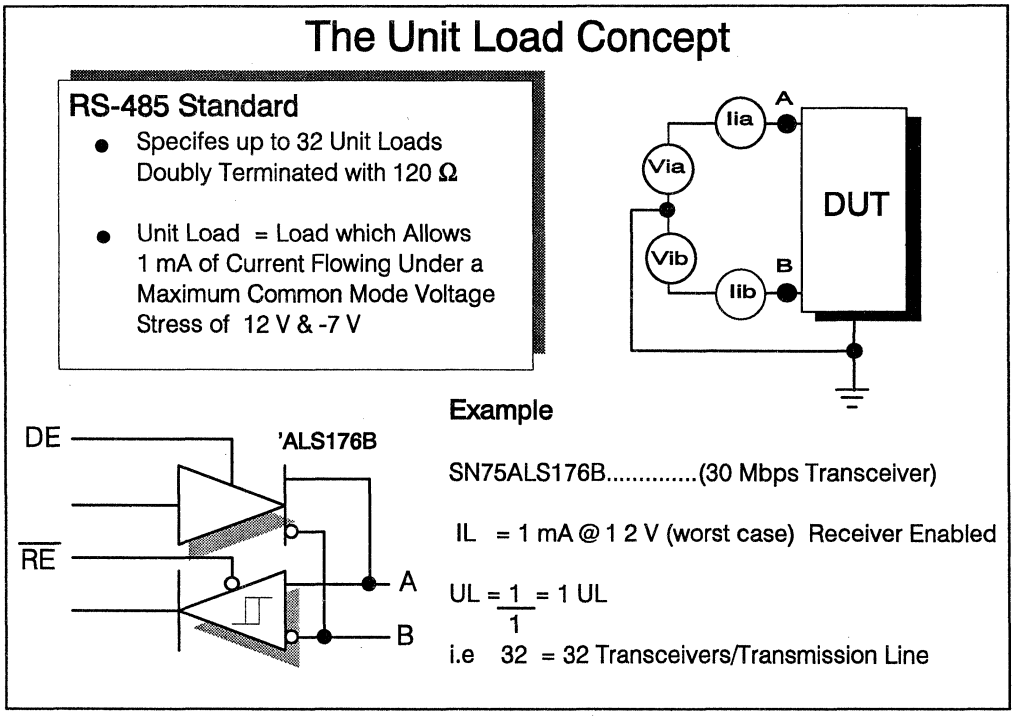


Figure 5.25 - The Unit Load Concept

To determine t_T tests must be carried out on the transmission cable. For the purposes of this example we chose a low cost non shielded, twisted pair cable - 500 m of a Belden type 8205 cable as supplied by RS Components Ltd of the UK, reference number 360-964. On the driving and receiving ends we connected a SN75ALS176 single channel transceiver. The rise time at the receiver end measured :

$t_T = 0.9$ µs to the 10% and 90% points.

Assuming a propagation delay down the line of 5 ns/m, the time tpd = 500 x 5 = 2500 ns or 2.5 µs.

so in this case:

$5\ t_T = 4.5$ µs and $2t_{pd} = 5$ µs, so 2 tpd > 5 t_T and therefore the transmission line should be considered as having a distributed parameter model and consequently must be terminated in its

characteristic impedance. In this case as we are using half duplex transmission the line must be terminated at the furthest ends.

To determine the characteristic impedance of the cable we used the technique described in section 1.5.4. Z_O in this case measured at 100 Ω.

The Unit Load Concept

The maximum number of drivers and receivers that can be placed on a single RS-485 communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

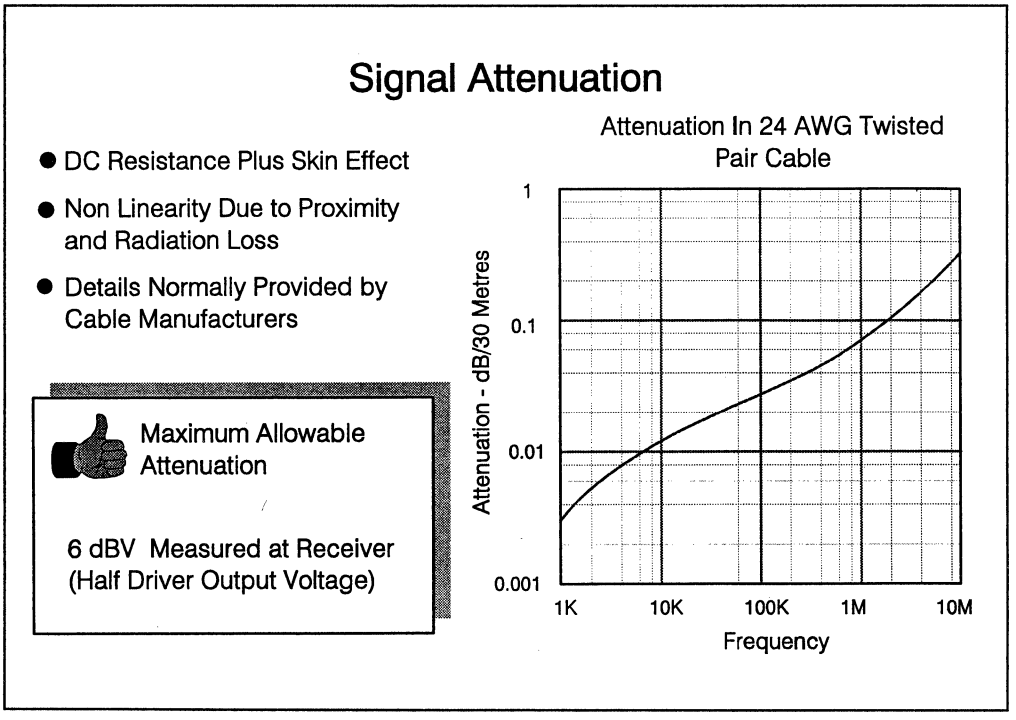


Figure 5.26 - Signal Attenuation

One U.L (at worst case) is defined as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V. The loads may consist of drivers and/or receivers but does not include the termination resistors, which may present additional loads as low as 50Ω total for doubly terminated lines.

The example in Figure 5.25 shows a unit load calculation for the SN75ALS176B. Since this device is internally connected as a transceiver, i.e. driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation

reference is made to the receiver input resistance, 12 kΩ, giving a transceiver current of 1 mA. This can be taken to represent 1 U.L. which will allow up to 32 devices to be connected to the line.

Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designer's risk.

3.3.1. Signal Attenuation

Section 1.3 discusses attenuation in more detail but a sufficient rule of thumb is where the attenuation of the line reduces the driven signal by no more than 6 dBV. Attenuation figures are usually supplied by cable manufacturers. The curve in Figure 5.26 shows the attenuation curve versus frequency for 24 AWG cable. For 500 metres of cable and using the 6 dBV figure, the maximum attenuation we can tolerate is 0.35 dBV/30 metres. In this case the 500 kbps data rate attenuation is well within this limit. The attenuation of the fundamental frequency and higher frequency components of the signal up to 10 Mbps will still be detectable at the receiver. This effect coupled with the the variation of signal velocity with frequency (termed dispersion) results in distortion of the pulse at the receiving end of the line.

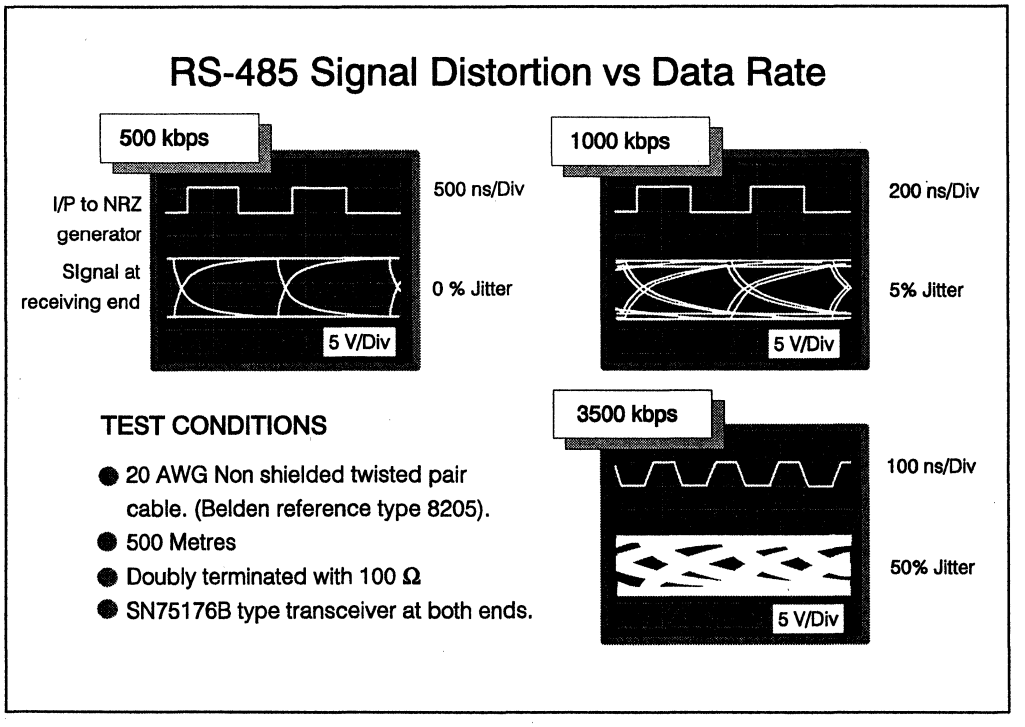


Figure 5.27 - RS-485 Signal Distortion vs Data Rate

3.3.2. Signal Distortion Vs Data Rate

The simplest way to determine the effects of random noise, jitter, attenuation, dispersion, on the inter symbol interference is by the use of eye patterns. For information on how to set up eye patterns, refer to section 1.4 of this Section. Figure 5.27 shows the distortion of the signal at the receiving end of 500 metres of 20 AWG twisted pair cable at different data rates. Using the system constraint of 500 kbps, we see the distortion is limited to the rounding of the signal pulse. If the data rate is increased further, the effects of jitter then become noticeable. In this case at 1 Mbps we begin to observe 5% jitter. At 3.5 Mbps we start to loose the signal completely and the quality of transmission is severely degraded. The maximum allowable jitter in a system should be limited to 5%. The causes of jitter are discussed in more detail in section 1.4.2.

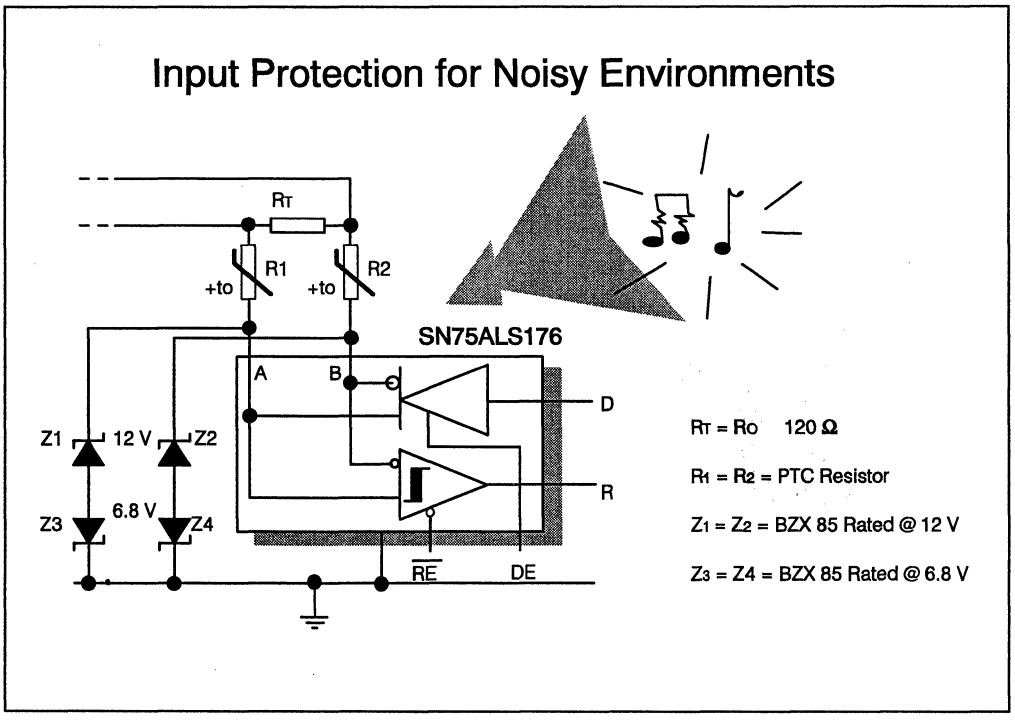


Figure 5.28 - Input Protection for Noisy Environments

3.3.3. Fault Protection and Fail Safe Operation

Fault Protection

Factory control applications generally require protection against excessive noise voltages. The noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 can be insufficient. Protection can be accomplished in a number of ways,

the most effective being through galvanic isolation which we will discuss later. Galvanic isolation provides system level protection but does not necessarily limit the voltages indcued on the transmission lines with respect to the RS-485 driver/receiver grounds. This can be accomplished by the use of protection diodes.

Figure 5.28 shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z_1 and Z_2 are chosen to protect the input from positive spikes greater than 12 V whilst Z_3 and Z_4 protect the device from negative going spikes greater than -6.8 V.

Fail Safe Operation

The feature of fail safe protection is also a requirement in many RS-485 applications, however its usefulness needs to be considered and understood at an application level.

The Need For Fail Safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle and occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or logic low state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called **fail safe**. An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

There are several ways implement a fail safe, including a hard-wired fail safe using line bias resistors or protocols. Protocols, although complicated to implement, are the preferred method. However since most system designers, hardware designers in this case, prefer to implement such functions in hardware a hard-wired fail safe is often implemented.

A hard wired fail safe should provide a defined voltage across the receiver's input regardless of whether the line is shorted to either supply rail or is left open circuited. The fail safe should also be incorporated into the line termination if present when at the extremes of the line.

Internal Fail safe

Manufacturers have gone part way to facilitating fail safe design by including some form of open line fail safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved of little use. The extra circuitry is quite often just a large pull-up resistor on the non-inverting receiver input, and a large pull-down resistor on the inverting

input of the receiver. These resistors are normally in the range of 100 kΩ, and so when used in conjunction with line termination resistors to form a potential divider, only a few millivolts are generated. As a result this voltage (receiver threshold voltage) is insufficient to switch the receiver. To use these internal resistors effectively means no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

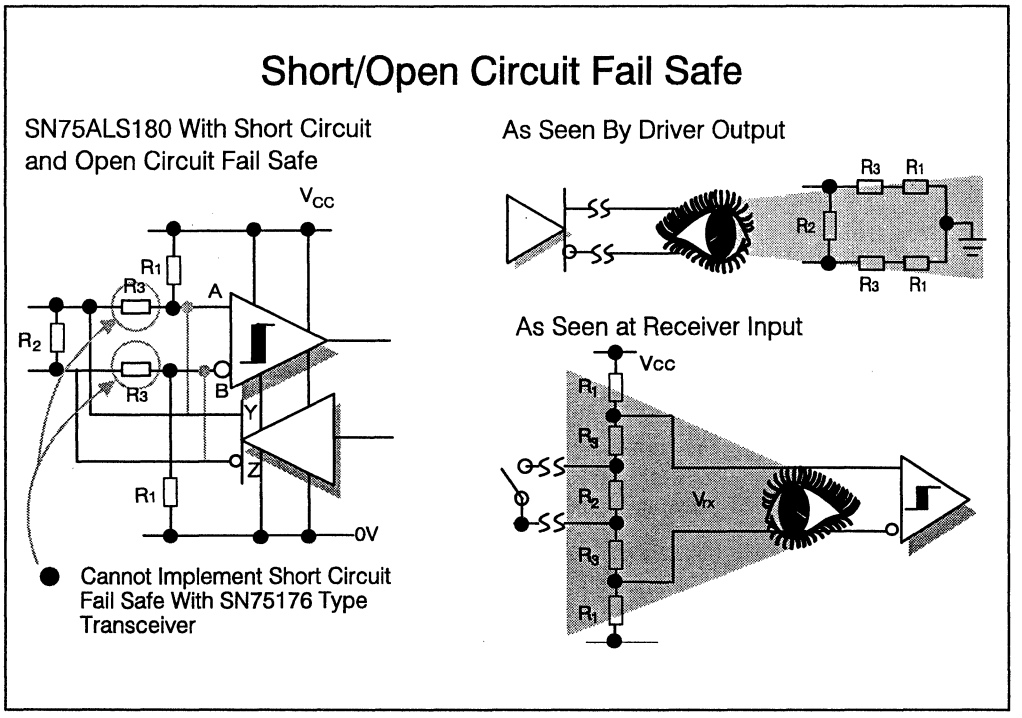


Figure 5.29 - Short/Open Circuit Fail Safe

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an ac. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedance's. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Placing external pull-up and pull-down resistors R_1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic

impedance, Z_O, produces a potential divider between $2R_1$ and Z_O. The voltage formed across the line, V_{OC}, equals

$$V_{oc} = V_{cc} \times \frac{Z_o}{2R_1 + Z_o}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{OC} to be greater than 200 mV. From this the relationship of R_1 to Z_O can be derived:-

$$R_1 = Z_o \times \frac{1}{2} \times \frac{V_{cc} - V_{oc}}{V_{oc}}$$

With V_{CC} = 5V, V_{OC} = 200 mV and Z_O = 100 Ω, yields R_1 = 1.2 kΩ.

Biasing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers, like the SN75ALS176, it is not possible to provide shorted line fail safe configurations, since the driver and receiver share the same IC. pins. Hence for devices like the SN75ALS176 this open line configuration is the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the input to the receiver can provide shorted line fail safe protection.

The extra resistors, R_3 in Figure 5.29, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R_3 would cause extra attenuation of the output signal. The 'ALS180 will have its driver outputs fed directly to the line, bypassing resistors R_3.

Calculating the Resistor Values

If the line became shorted then R_2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{cc} \times R_3/(R_1 + R_3) \qquad \textbf{(a).}$$

For RS-485 applications the standard specifies V_{rx} to be greater than 200 mV. So

$V_{rx} = V_{th} = 200\ mV.$

Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R_1 and R_3.

When the line goes into a high impedance state the receiver will see the two R_3 in series with R_2 plus the two R_1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{cc} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \qquad \textbf{(b).}$$

Relating this new V_{rx} to the minimum specified in the standard, V_{th}, gives:

$$R_1 = \tfrac{1}{2} R_2 \times [\{(V_{cc} - \alpha V_{th})(V_{cc} - V_{th})\}/\{(\alpha - 1) V_{th} V_{cc}\}]$$

$$R_3 = R_2 \times (V_{cc} - V_{th})/V_{th}$$

Where α is the ratio of V_{oc}/V_{rx}

The transmission line will see an effective line termination resistance of R_2 in parallel with twice the sum of R_1 and R_3. This should match the transmission line's characteristic impedance, Z_o, therefore

$$Z_o = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \qquad \textbf{(c)}$$

Combining equations **(a)**, **(b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = \tfrac{1}{2} Z_o \times \frac{(V_{cc} - V_{th})^2}{(\alpha - 1) V_{th} V_{cc}}$$

$$R_2 = Z_o \times \frac{V_{cc} - V_{th}}{V_{cc} - \alpha V_{th}}$$

$$R_3 = \tfrac{1}{2} Z_o \times \frac{V_{cc} - V_{th}}{(\alpha - 1) V_{cc}}$$

In this application assuming the supply voltage is 4.5 V and V_{th} = 200 mV with an a value α of 1.5 and driving a line with characteristic impedance of 120 Ω yields the following values:-

R_1 = 2.2k Ω

R_2 = 120 Ω

R_3 = 110 Ω

The values of R_1, R_2, and R_3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R_1 and R_3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers are the same, all R_1 resistors are the same, and that all R_3 resistors are the same Since all of R_1 and all of R_3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R_3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 12 kΩ.

3.3.4. Galvanic Isolation

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application, which is shown in Figure 5.30.

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

For example consider the case in a process control system where the interface node, shown in Figure 5.30, connects between a data logger and host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a process control type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit.

capability. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability.

Transceiver protection circuitry is formed by Z_1, Z_2, Z_3 and Z_4 along with current limiters PTC_1 and PTC_2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows;

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O [1 + V_{TH}/V_{CC}]$$

The bus driver used is the **SN75LBC176**, chosen for its low power consumption and high data rate Using a cable with a characteristic impedance of Z_O = 120 Ω and a desired V_{TH} of 200 mV, requires $R_1 = R_2$ to be around 1.6 kΩ in value. The terminating resistor, R_T would be in the order of 124 Ω.

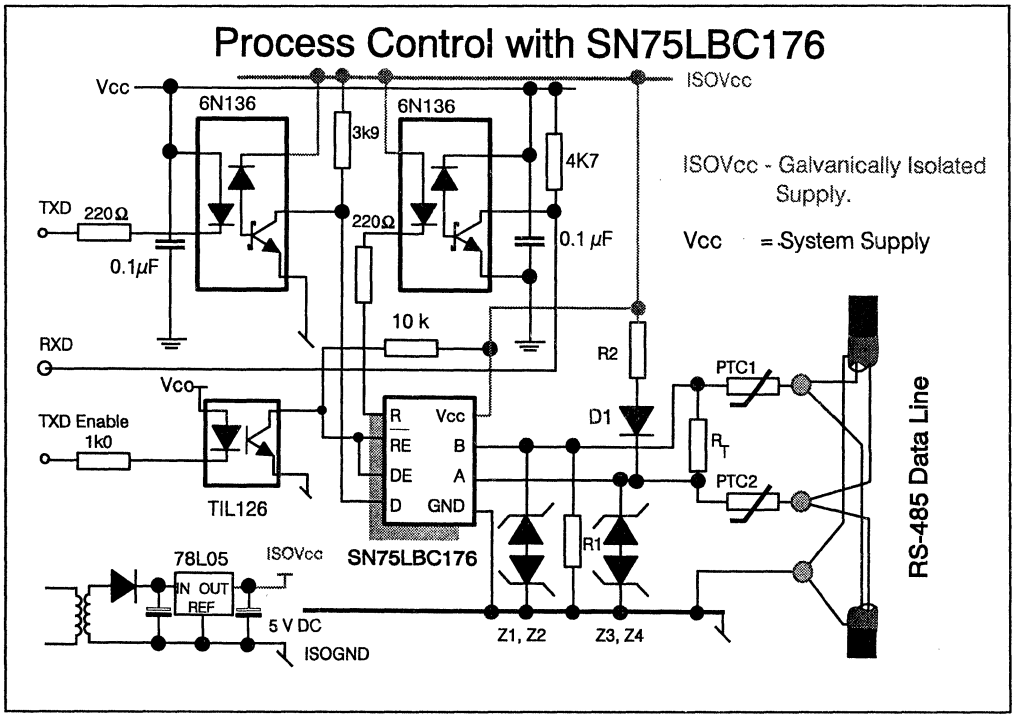


Figure 5.30 Process Control SN75LBC176

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions. The values of $R_1 = R_2$ are best kept as low as

possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.

Galvanic isolation is afforded by means of three optocouplers/opto isolators. The 6N136 is chosen for its high data rate capability, t_p = 75 ns (max), and its high voltage isolation.

The 6N136 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The 6N136 consists of a GaAsP light emitting diode and integrated light detector, composed of a photo diode, a high gain amplifier and a Shottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of 13 mA (eight 1.6 mA TTL loads). A TTL input is provided for applications that require output transistor gating.

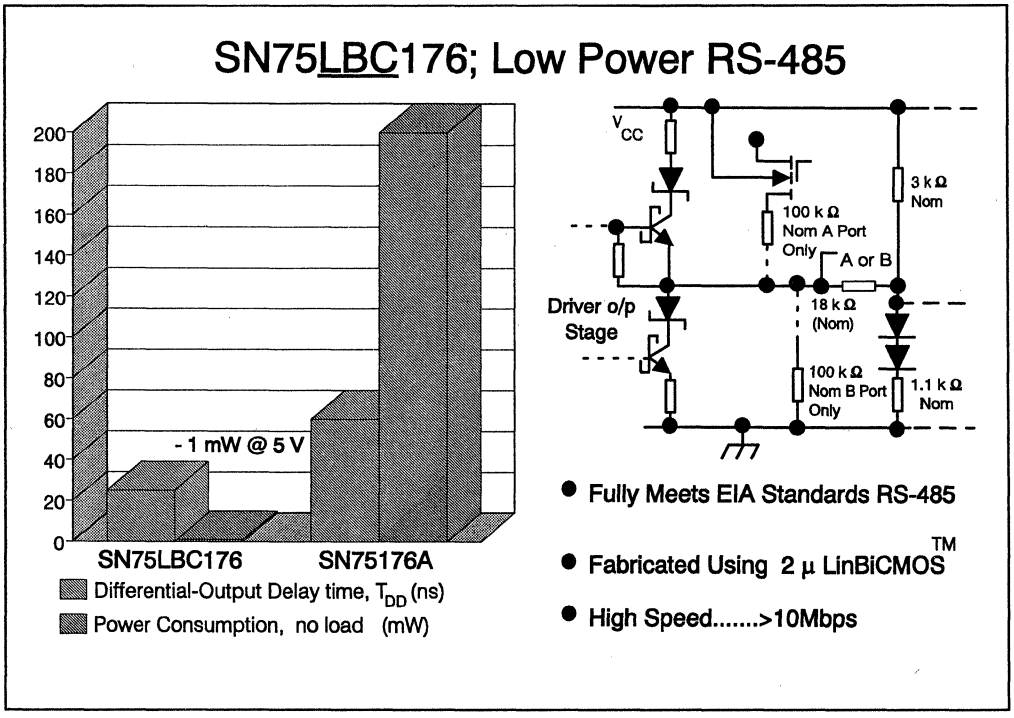


Figure 5.31 - SN7LBC176; Ultra Low Power

Housed in a single 8-pin dual-in-line plastic package the 6N136 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000 Vµs.

A 0.1 µF capacitor has been connected between V_{CC} and ground to improve switching performance.

3.4.SN75LBC176; Ultra Low Power

The key feature of the SN75LBC176 is the very low power consumption, 1 mW. Compare this to the consumption of the older generation SN75176A, where the quiescent power is as high as 200 mW. Normally low power consumption signifies a reduction in ac performance. In the case of the 'LBC176 the ac performance is improved over the SN75176A. Data rates of greater than 10 Mbps are achievable while still being conformant to RS-485. The low power consumption has further benefits than simply reducing supply current:

3.4.1. Improve MTBF

Although not representing the most glamorous end of the semiconductor design spectrum, reliable line interface circuits are crucial if the overall system mean time between failure (MTBF) is to be minimised. System designers have long been aware that often the weak link in ensuing system reliability has been line interface circuits. This vulnerability is due in part to the circuits close proximity to the outside world via the edge connector. Consequently interface circuits are particularly susceptible to failure from high external voltages caused by noise, ESD or incorrect insertion of cables. For this reason the technology of choice for many Texas Instruments emerging interface products is LinBiCMOS.

LinBiCMOS, the Technology of Choice

LinBiCMOS is based on TI's highly successful LinCMOS process. LinCMOS is a 3 µm pure CMOS technology with 16 V capability, making it ideal for the design of low power analog products such as op-amps and analog-to-digital converters (many examples of which are discussed elsewhere in this book). By shrinking the geometry to 2 µm and adding a high performance 30 V bipolar structure, a new analog merged bipolar/CMOS technology has been produced.

Probably LinBiCMOS's greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost , as many "nice to have" features can make a process too expensive to address a wide range of opportunities.

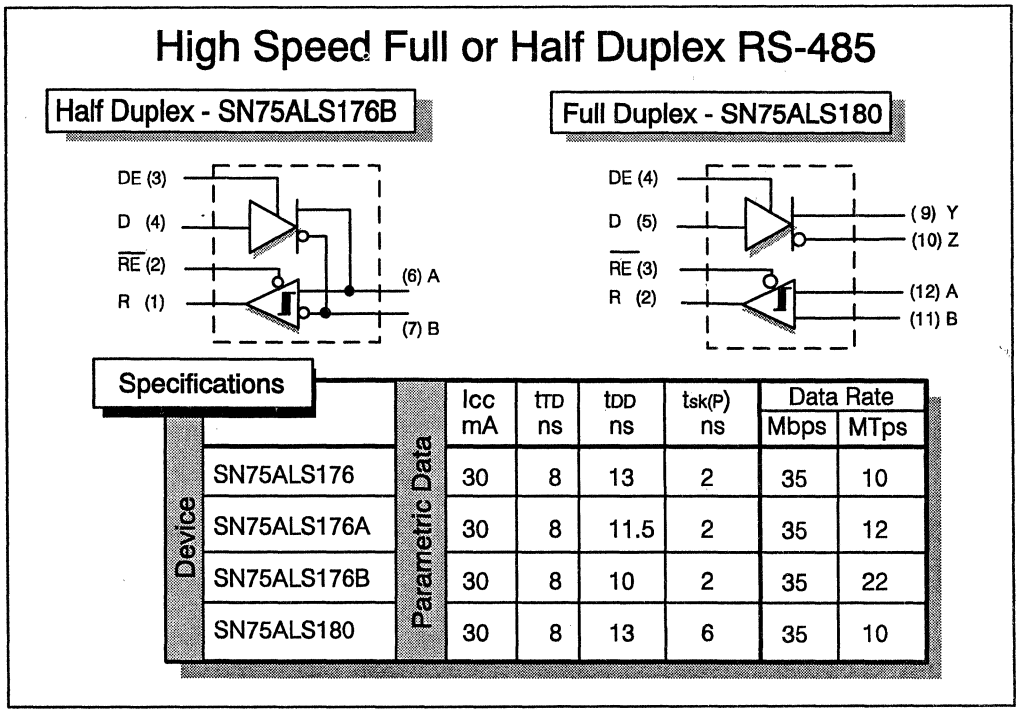
By making LinBiCMOS modular, only the process modules needed to address a particular application need be used, making it very cost effective. Modules available for LinBiCMOS

include high speed NPNs (with an f_T of 3GHz compared with 500MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and shottky diodes for clamping.

The Applications

With its high voltage capability and excellent switching speed LinBiCMOS is ideal to address standards such as EIA-232 and RS-485. For example the RS-485 standard, demands that driver outputs can be shorted to +12V and -7V without damage. This is particularly difficult to implement as RS-485 devices are designed to operate from a single 5 V supply, meaning that parts of the chip must be designed to operate well outside its supply rails. Further more the "party line" nature of the standard requires devices that must be able to withstand contention (multiple drivers accessing the bus simultaneous) without failure. For this reason short circuit protection and thermal shutdown are built into the chip.

The standard SN75LBC176 is charaterised for commercial temperature range applications. For more extreme conditions the SN65LBC176 extends the operating range to -40°C to +85°C.



Device	Parametric Data: Icc mA	tTD ns	tDD ns	tsk(P) ns	Data Rate: Mbps	Data Rate: MTps
SN75ALS176	30	8	13	2	35	10
SN75ALS176A	30	8	11.5	2	35	12
SN75ALS176B	30	8	10	2	35	22
SN75ALS180	30	8	13	6	35	10

Figure 5.32 - High Speed Full or Half Duplex RS-485

3.4.2. Full Duplex and High Speed RS-485

In the process control example we discussed earlier, the key requirement has been for reliable data transmission over 500 metres of cable. The data rate under consideration was limited to 500 kbps however in many systems the data rate requirements are in excess of 10 Mbps. Cable length must be reduced accordingly as transmissions at this rate are only possible over short line lengths, <50 metres. We have discussed the SN75LBC176, however for speeds above 10 Mbps we must look towards a technology which is more well suited for high speed applications.

Advanced Low Power Shottky technology provides the key to the quest for speed. The SN75ALS176 utilises the true benefits of ALS pushing the data rate to over 35 Mbps. For synchronous systems where skew limits are critical, the SN75ALS176B facilitates 22 MTps (Million Transfers per second). This is the highest speed RS-485 transceiver on the market today.

The SN75ALS176, like the SN75176, DS3695, TL3695, is of a transceiver configuration. As shown in figure. 4.32, the transmit and receive pins are accessible through pins 6 and 7 only. With this configuration communication is limited to half duplex only. For quasi-full duplex operation, using

two separate RS-485 lines, one must use a device like the SN75ALS180. this device allows separate lines to be connected to both the receiver and driver. The 'ALS180 has similar performance to the 'ALS176 facilitating up to 35 Mbps.

3.4.3. RS-485 Selection Guide

In this section we have concentrated on the single transceiver type function. TI does however support a wide range of parts compliant with the RS-485 standard in various configurations and multiples. The below selection guide is provided for convenience. The reader is advised to consult the Interface Circuits Data Book (Reference SLYD006) for the latest technical specifications.

RS-485 Data Transmission Circuits

Device	Devices	Device	Key
Line Drivers	4	SN75172	Industry Standard
		SN75174	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
Line Receivers	4	SN75173	Industry Standard
		SN75175	Industry Standard
		SN75ALS173	High Speed
		SN75ALS175	High Speed
Line Transceivers (Drivers / Receivers)	1	SN75176A	Reduced Slew-rate
		SN75176B	Industry Standard
		SN75177B	Industry Standard Repeater
		SN75178B	Industry Standard Repeater
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra- Low Power
	1/1	SN75179B	Industry Standard
		SN75ALS180	Full Duplex Communication
		SN75ALS181	Full Duplex Communication
	2/2	SN751177	High Speed
		SN751178	High Speed
		SN75ALS1177	High Speed
		SN75ALS1178	High Speed
	3	SN75ALS170	High Speed
		SN75ALS171	High Speed
		SN75ALS1711	High Speed
	9	SN75LBC976	Low Power

Notes

¥ Product currently under development, contact TI representative for further details.

4. Interface Circuits for SCSI

4.1.SCSI Overview

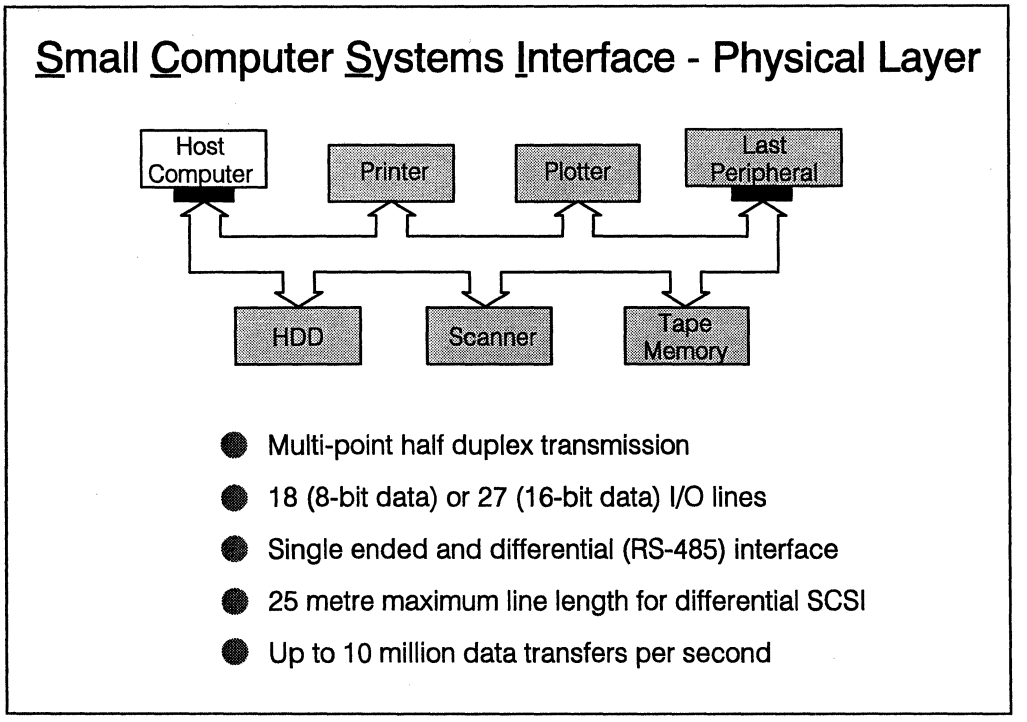


Figure 5.33

SCSI is the acronym for Small Computer Systems Interface and details the ANSI specification for a peripheral bus and command set. The specification defines a high performance peripheral interface that distributes data independently of its host, helping to free up the host for more user oriented

commands. The objective of the interface is to provide high speed data transfer between computer peripherals independently of the host. Already there are a large number of disk drives, notebook PCs, and CD ROM drives incorporating a SCSI port.

Basic SCSI is an eight bit parallel I/O bus, with parity, and nine control/handshaking lines, making . 18 lines in total. More recently, to increase the data throughput, the data bus has been increased to 16 bits with two parity bits while maintaining the nine control lines, making for 27 lines in total. This is referred to as wide SCSI.

4.1.1. SCSI Physical Layer

There are two electrical specifications referred to in the SCSI standard, single ended and differential:

It is beyond the scope of this seminar hand book to discuss the complete SCSI standard, we shall concern ourselves with the physical layer only. For more information on the standard the reader is encouraged to refer to the numerous publications on SCSI.

Single Ended Interface

The single-ended driver and receiver configuration utilises TTL logic levels and is primarily intended for applications with a cabinet, the maximum line length being limited to 6 metres and the data rate is normally limited to 5 Million Transfers per second (MTps), although innovative termination techniques enable the maximum trasnfer rate to approach 10 MTps.

Differential Interface

The differential driver and receiver configuration uses the EIA RS-485 standard and is primarily concerned with transmitting data between cabinets. Maximum line length is 25 metres with the maximum data rate currently 10 MTps.

4.2.Single Ended SCSI

4.2.1. Termination of Single Ended Bus

Termination of the single ended SCSI bus is becoming increasingly important as designers strive for faster system speeds. If error-free data rates of 10 Mbps over the 6 metre bus are to be achieved then signal integrity must be preserved. Termination will reduce unfavourable transmission line effects such as reflections and distortion which can degrade system performance as signal speeds increase. Proper termination of a bi-directional bus such as SCSI requires terminators at each end of the cable.

4.2.2. Signal Transitions

The potential for high data rates depends upon quick and clean transitions between low and high signal levels. The range of SCSI signals is shown below in fig 4.33.1. A low to high transition, or de-assertion, of a signal is initiated by an open collector driver switching off and causing an instantaneous voltage step to travel down the line.

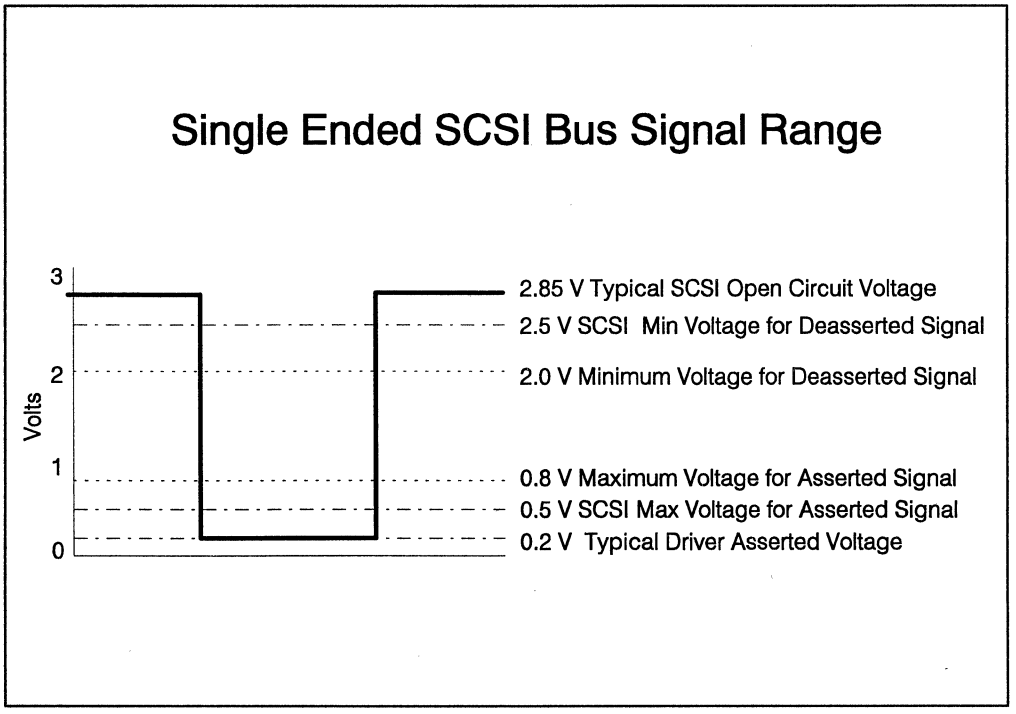


Figure 5.33.1 - SCSI Bus Signal Range

The size of the first step on de-assertion depends upon the amount of current in the line, I_L, the characteristic line impedance seen by the signal, Z_O, and the driver output-low voltage (V_{OL}), and can be calculated as follows ;

$$V_S = V_{OL} + Z_O I_L$$

To achieve the maximum data rate the first step needs to exceed the receiver threshold voltage in a single transition. Although the 110 Ω impedance of a typical SCSI ribbon cable suggests that this will require only limited line current capability, the impedance seen by a signal is always less than the specified cable value. Extra capacitance due to peripheral connections to the bus, transmission line effects, and the position of the signal source, can all combine to reduce the effective impedance by 50% or more.

To make up for this lack of 'real' impedance, it is the terminators job to source as much current as possible during de-assertion. This role is restricted by the SCSI specification, however, which limits each terminator to supplying a maximum of 24 mA to prevent the line current from exceeding the 48 mA current sink limit of the open collector drivers.

The role of the SCSI terminator is not confined to low-to-high signal transitions. Once a signal has been de-asserted the terminator is required to bias the bus lines to the correct open circuit voltage level and thereby provide maximum noise margins.

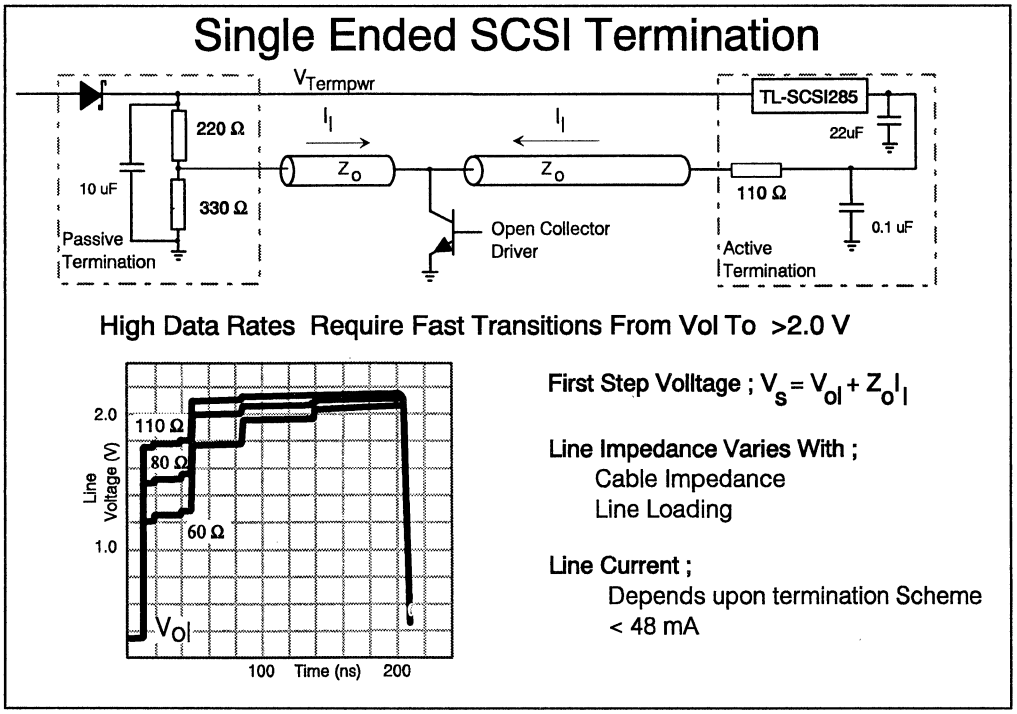


Figure 5.34 - Single Ended SCSI Termination

4.2.3. Passive and Active SCSI Termination

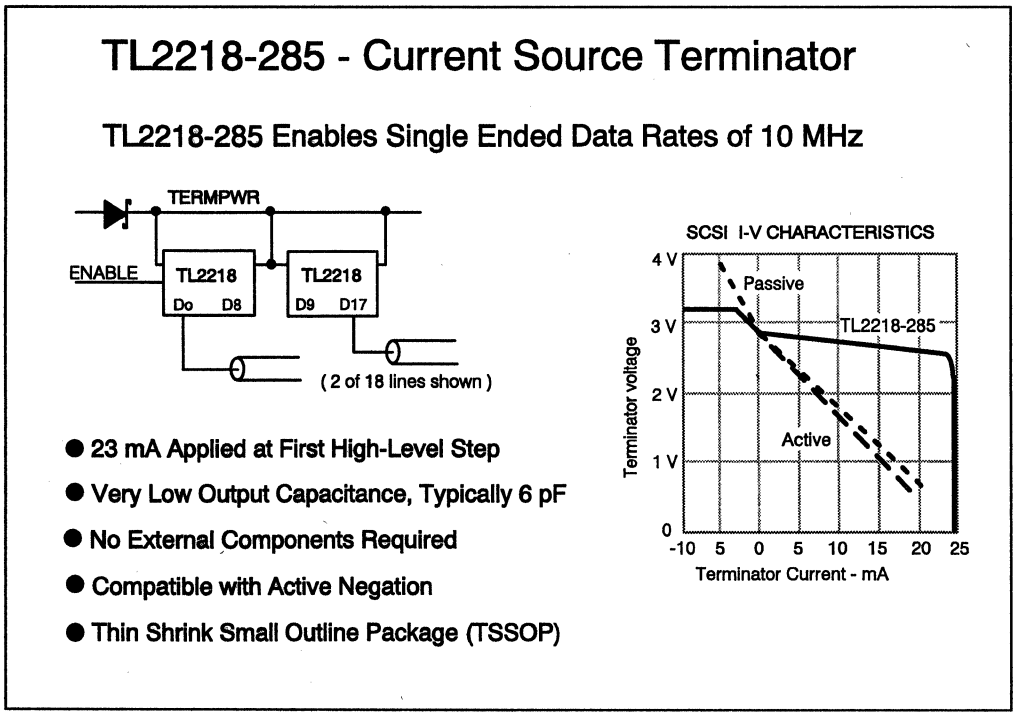
SCSI termination has traditionally been carried out using passive termination networks. As illustrated in Figure 5.34 these consist of 2 resistors per signal line ; a 220 Ω pull up resistor connected to the termination power source (Termpwr), and a 330 Ω pull down resistor connected to ground. The Shottky diode is needed by all termination schemes to protect the power source from reverse currents.

This type of termination typically results in a maximum line current of around 17 mA. Assuming the terminator is on a heavily loaded bus, signified by an impedance of approximately 75 Ω, then the above equation gives a first step value of 1.76 V - well short of the desired 2.0 V level.

In addition to this limited current capability and the power consumption penalty imposed by the resistor dividers, passive terminators also suffer from an unregulated line bias voltage. As a result the

line voltage will fluctuate with variations in the load current and Termpwr, leading to smaller noise margins, lower line currents, and reduced data rates.

The most common alternative to passive termination replaces the resistive network with a voltage regulator in series with a single 110 Ω resistor per line (fig 4.34). This method, known as Active, Boulay, or Alternative 2 termination, was developed to overcome two of the main shortcomings of passive termination.



4.35 TL2218-285 Current Source Termination

The 110 Ω resistors increase the typical line current available on de-assertion to 21 mA, which, from a transmission line viewpoint, is equivalent to a 35% increase in line impedance. The line current and the high-level noise margins are also more stable since Termpwr is no longer used to set the bias voltage directly. Instead it is used to form the input to the voltage regulator, which then provides a regulated bias voltage.

The TL-SCSI285 and TL2217-285 low dropout regulators from Texas Instruments are specifically designed for active SCSI termination. With an overall accuracy of 2 % and a maximum dropout voltage of 0.6V the TL-SCSI285 is the highest performance dropout regulator available for SCSI active termination.

4.2.4. Current Source Termination Using the TL2218

Although active termination brings a number of advantages to SCSI termination these can be further improved upon. The TL2218-285 from Texas Instruments is a completely new type of SCSI terminator which does just that.

During de-assertion the TL2218-285 operates as a 23.5 mA current source which is able to maintain this current level until the signal reaches the correct SCSI open circuit voltage. At this point the TL2218-285 becomes a voltage source of 2.85 V.

The additional current supplied by the TL2218-285 reduces the low-to-high transition time by ensuring that each voltage step is consistently the largest possible. The effect of this can be seen in Figure 5.36, which shows the signal wave forms obtained after using a TL2218-285, a commercially available active terminator, and a passive termination network to terminate a 50 Ω cable (the equivalent of a heavily loaded bus). Even at 10 MHz the first step voltage of the TL2218-285 terminated system still exceeds the desired 2.0 V level.

Another feature of the TL2218-285 is the inclusion of a disable function which allows the terminator output to be shut down. This is particularly useful for a peripheral which finds itself somewhere other than the physical end of the bus, and needs some way of easily 'removing' its terminator. If disabled the TL2218-285 consumes just 500 µA of current, and maintains an output capacitance of 6 pF. Allowing for the 15 - 16 pF typical output capacitance of a peripherals transceivers, this will give a total node capacitance well within the 25 pF SCSI limit. An active terminator, on the other hand, will normally maintain a disabled output capacitance of 10 pF, often leaving the system to operate outside of the SCSI specification.

Use of the TL2218-285 also removes two possible causes of system failure or driver damage associated with active termination.. Firstly the 2% output tolerance of the TL2218-285 ensures it does not supply more current than allowed by the driver protecting SCSI limit. The tolerances of the voltage regulator and the 110 Ω resistors used in active termination, however, can result in the terminator supplying in excess of the maximum 24 mA.

The other potentially damaging situation arises when active negation drivers are being used. These devices sense bus voltages and source sufficient additional current to ensure that first step voltages reaches the minimum SCSI level. Despite this attractive feature their relatively high cost has limited their use to ultra fast changing control lines such as ACK and REQ.
To be compatible with active negation drivers it is clear that any terminator connected to the bus must be able to sink current. Again this is a problem with active termination but not with either the TL2218-285 or a passive terminator. The voltage regulator of an active terminator will shutdown when any driver voltage exceeds 2.85 V. This allows the line voltage to rise and any driver which then pulls low may sink more than their 48 mA limit.

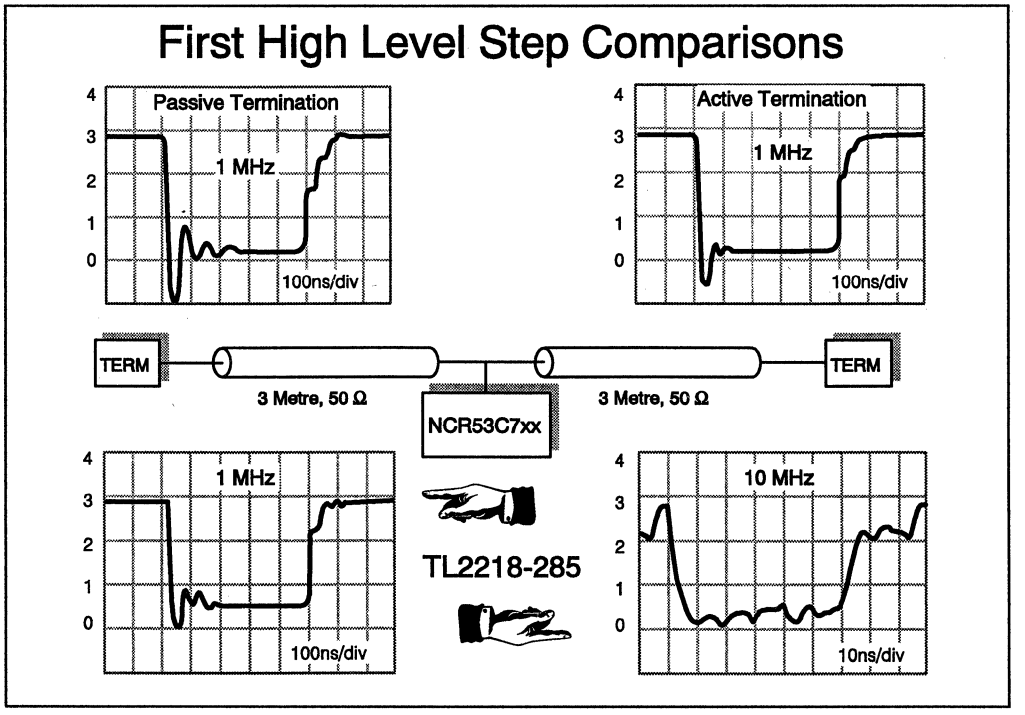


Figure 5.36 - First High Level Step Comparisons

4.2.5. Power Considerations

As well as enabling increased data rates, termination will also increase the power consumption of a SCSI system. As SCSI has found increased usage in portable or battery powered systems this has become more important. Exactly how much depends upon the method of termination, but not quite as obviously as might at first be thought.

During data on periods, the power dissipation of each of the SCSI termination methods is very similar. For an 8 bit bus with all the data lines asserted the power dissipation in each case will be around 1 W.

During data off periods the position is significantly changed. The resistor dividers of a passive terminator will still draw around 750 mW of power. Both the TL2218-285 and active terminators, however, require a total quiescent current of less than 10 mA, providing a 30x saving in power consumption.

For a single TL2218-285 it is possible to calculate a worst case dynamic power dissipation of 493 mW. This assumes that all nine lines in the package are asserted simultaneously and experience a 50% duty cycle. In some systems it may be desirable to avoid any single device dissipating this much power. This can be achieved by partitioning the SCSI bus lines in an appropriate manner. One

such method is to split the data lines between the two devices (for an 8 bit system) and also assign the REQ and ACK lines to separate packages.

Battery powered systems will also benefit from the extended Termpwr range of the TL2218-285. Compared to competing solutions which require a minimum Termpwr of 4 volts, the 3.5 V to 5.5 V range of the TL2218-285 greatly increases the potential for prolonged operation.

4.3.Differential SCSI

4.3.1. SN75LBC976DL; Two Chip Differential SCSI

Much debate has taken place on differential versus single ended SCSI for data rates above 5 million transfers per second (MTps). It is clear however, that for data rates approaching 10 MTps and at line lengths in excess of 6 metres, differential SCSI is essential.

As we discussed earlier, the standard 8-bit interface is made up of 8 data lines, one parity bit, and 9 control lines, making 18 channels in total. The only differential transceivers capable of transmitting at 10 MTps data rate have utilised the LS and ALS technologies. Using these technologies and considering the 18 transceivers per interface the power consumption is quite considerable, 2.4 W with all drivers disabled. Turn the drivers on and the power consumption rises to nearly 4 W.

From a designers viewpoint, 2.4 watts is a considerable amount of heat to remove from a system. This is evident in the case of compact hard disk drives where shear equipment size is the limiting element. A further factor is board area, using one discrete transceiver per channel, i.e. 18 8-pin SO packages, is unacceptable for many applications.

From a semiconductor designers viewpoint integrating a number of transceivers is of course possible however the limiting factor once again is power dissipation. The SN75LBC976 is designed to overcome both the problems of power dissipation and integration. The device incorporates on a single IC, nine RS-485 configurable transceivers each capable of transmitting at 10 MTps. This is made possible using LinBiCMOS technology. With all drivers disabled the quiescent power consumption of the 'LBC976 is a mere 1.5 mW, with all drivers enabled the quiescent consumption rises to 45 mW, a considerable saving over LS and ALS parts. The package size has also been reduced to a minimum using the 0.635 mm pitch 56 pin SSOP package which reduces board area significantly compared with alternate packages such as PLCC. The reader should note that irrespective of the device power, there is still the relatively high line current. The SSOP package has been thermally enhanced to handle this level of power dissipation. We will cover this point later as we look at the thermal characteristics of the package.

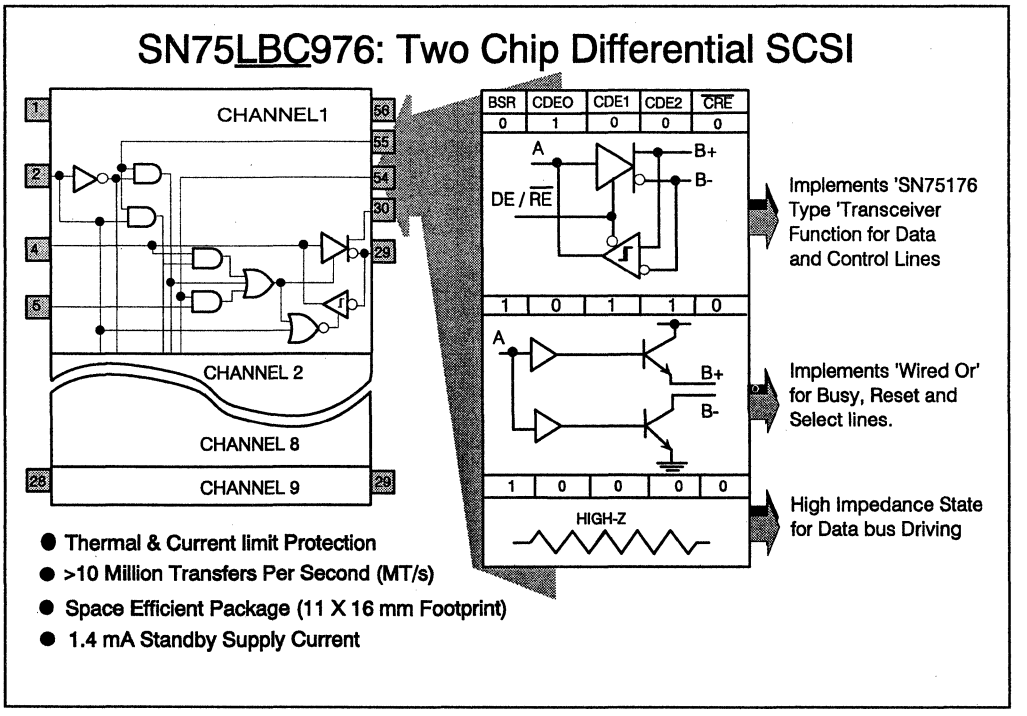


Figure 5.37 - SN75LBC976: Two Chip Differential SCSI

The SN75LBC976 is fully configurable to facilitate connection to any type of SCSI system arrangement. The 9 channels can be arranged into seven possible channel functions using the BSR, CDE0, CDE1, CDE2, CRE control pins.

The 7 channel configurations are:

1. Transparent, permanently enabled Receiver.
2. Transparent, permanently enabled Driver.
3. Bi-directional transceiver with direction control.
4. Driver with enable control.
5. Open ended driver for Wired OR control lines.
6. Driver with ORed data and enable lines.
7. Permanent high impedance state.

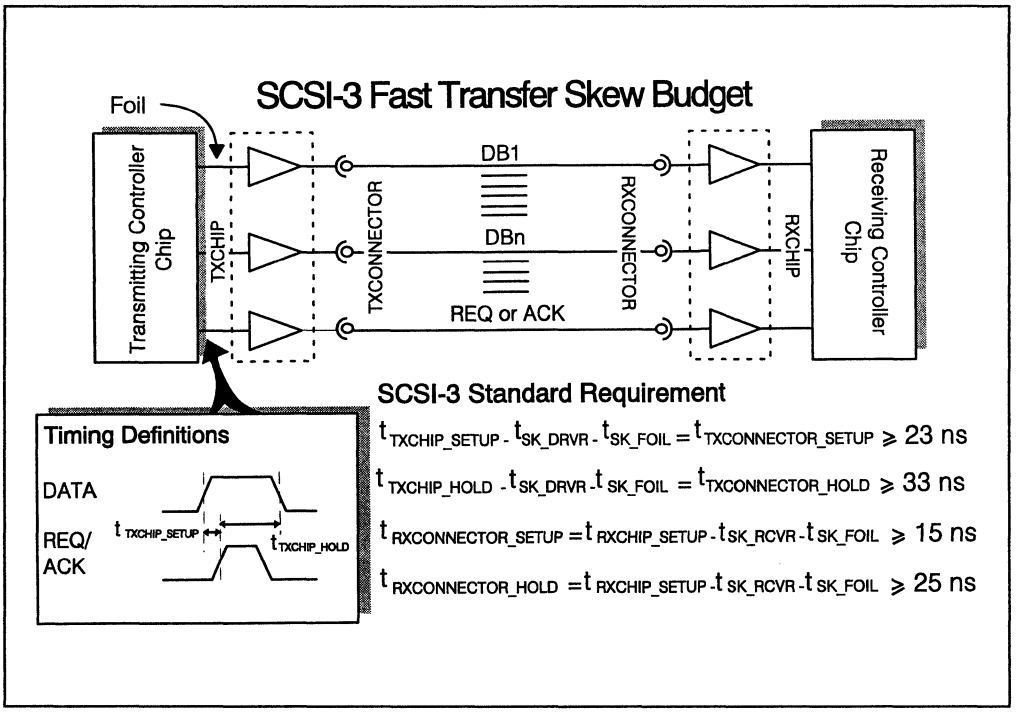


Figure 5.38 - SCSI-3 Fast Transfer Skew Budget

4.3.2. SCSI and IPI Skew Considerations

SCSI as we have discussed is a parallel data bus. This is also the case with IPI. IPI, an acronym for Intelligent Peripheral Interface, is similar to SCSI in that it is a high speed peripheral bus with the same high speed differential interface requirements. By the parallel nature of the interface, both standards transfer data over the cable more than one bit at a time. SCSI and IPI allow 8-bit (one Byte) or a 16-bit (one word) data width and transfers as often as once every 100 ns or 10 million transfers per second.

Since the logical state of any one bit can change every 100 ns, this defines a period during which the logical state should be valid across the bus. This is the unit Interval (UI). The voltage transitions which define the start and end of the UI can propagate along the bus at different velocities due to the physical differences along each electrical path. So the original UI at the start will be different at the destination.

Time variation of the defining voltage transitions is typically called skew. The limit for skew, designated $t_{sk(lim)}$, is the fastest minus the slowest propagation delays along any part of the bus. This, in effect, will reduce the UI by $t_{sk(lim)}$ establishing a minimum unit interval, UI_{min}, that can be transmitted with a particular data bus.

The proposed SCSI-3 standard for fast transfers (10 MTps), defines UI_{min} in terms of set-up and hold times at the SCSI connector for inter-operability with any other SCSI device. At the time this document is being written the requirements are as shown in Figure 5.38.

The budget behind the connector is left to the designer and depends upon the SCSI controller, transceivers, and layout being used. The table shows some skew budget examples with various controller chips that would comply with the requirements at the SCSI connector. The column under 'Rec' (for recommended) is data for the worst case number for SCSI controllers surveyed by the SCSI SPI Working Group and budgets 8 ns for the external driver and 9 ns for the external receiver. This is the origin of the $t_{sk(lim)}$ specifications in the SN75LBC976 data sheet.

Parameter	Rec	Vendor A	Vendor B	Vendor C	Units
min Tx_controller_setup =	32	30	35	35	ns
min Tx_controller_hold =	42	42	45	45	ns
min Rx_controller_setup =	5	0	5	0	ns
min Rx_controller_hold =	15	20	15	10	ns
t_{sk_etch} =	1	1	1	1	ns
max t_{sk_dvr} =	8	6	11	11	ns
max t_{sk_rvc} =	9	4	9	14	ns

Transceiver Skew Budgets for Various SCSI Controllers

The time it takes one transceiver of the 'LBC976 to change logic states is called the propagation delay time. For a driver this is designated as t_{dD} and for a receiver t_{pd} and does not differentiate whether the logical transition is from high-to-low or low-to-high level. The $t_{sk(lim)}$ parameter for the transceiver is nothing more than the maximum difference of the propagation delay times between any two drivers or any two receivers on any two devices. Compliance to the $t_{sk(lim)}$ specifications of the data sheet and the recommendation of the SCSI standard is assured by measuring the propagation delay time of each channel of each 'LBC976 and accepting only those devices within the $t_{sk(lim)}$ band. To keep the production costs of the 'LBC976 reasonable, this testing is done at 25°C and at 70°C ambient temperatures at a V_{CC} of 5 volts.

Admittedly, the die temperatures and supply voltage are all the same (or nearly the same) during TI's production testing and not necessarily the same would be seen in actual use. However the sensitivity of the propagation delay times to these factors is the same and repeatable from device to device. In other words, as long as the operating environment of all of the channels of the SCSI interface is similar, the change in propagation delay times from the data sheet conditions will be the same. This will maintain the $t_{sk(lim)}$ even though the actual propagation delay times may change.

It is nearly impossible to predict the instantaneous die temperatures of these devices in actual use. Due to the non-deterministic nature of the state of any one channel and the averaging affect of nine channels and of the package thermal time constant, the die temperature must be considered using the mean power dissipation. It is also reasonable to assume the mean power dissipation of separate

devices on the same printed circuit board to be close to each other and the temperature of the air around them will not have a large (<5°C) gradient between the two. Even if there was an air temperature gradient of 45°C, there would be only about a 2 ns difference in the driver propagation delay times and, from recent data, little or no difference in the receiver propagation delay times. If such a temperature gradient actually existed across a board, it' is likely that skew budgets are not going to be the problem with the equipment!

In summary:

1. The designer should determine the transceiver skew requirements based upon his controller and board design.
2. The current specification and testing of $t_{sk(lim)}$ of the 'LBC976 is, the best compromise for a cost effective solution.
3. We have application information from our experience gained through numerous users with no inter-operability problems detected at the time of writing.

4.3.3. SN75LBC976 Channel Power Dissipation Considerations

Channel Power Dissipation

To understand the SN75LBC976 power dissipation when connected to a SCSI bus and the subsequent heat sinking requirements, we must develop a realistic model for the power consumption under working conditions. We must consider the power dissipation within the silicon. There are three primary sources, the dc quiescent power, the ac or switching power, and the dc or resistive losses in the output drivers.

The current necessary to bias the circuits of a single enabled 'LBC976 differential driver is typically 0.53 mA and a maximum of 1.1 mA. A single enabled receiver circuit requires 3.22 mA typically and 5.00 mA maximum. The typical values have been measured on 94 SN75LBC976DLs from three different wafer lots. The maximums have been verified over temperature on the same samples.

It follows the driver quiescent power consumption, P_{DCC} is:

$$P_{DCC} = I_{CC} \times V_{CC}$$
$$= 0.53 \text{ mA} \times 5.00 \text{ V} = 2.65 \text{ mW/Channel average}$$
$$= 1.11 \text{ mA} \times 5.25 \text{ V} = 5.83 \text{ mW/Channel maximum}$$

And the receiver quiescent power, P_{RCC} is:

$$P_{RCC} = I_{CC} \times V_{CC}$$
$$= 3.22 \text{ mA} \times 5.00 \text{ V} = 16.10 \text{ mW/Channel average}$$
$$= 5.00 \text{ mA} \times 5.25 \text{ V} = 26.25 \text{ mW/Channel maximum}$$

The average I_{CC} of a representative sampling of the SN75LBC976 has been measured to be 9.77 mA for nine unloaded drivers switching at 5 MHz (10 Mbps), a 50% duty cycle, and at a V_{CC} of 5 V. Nine receivers at the same frequency and duty cycle and unloaded outputs consumed 36.0 mA average. Since both measurements include P_{DCC} or P_{RCC}, they are subtracted below:

Driver switching losses, P_{DAC}, at 5 MHz:

$$P_{DAC} + P_{DCC(average)} = (I_{CC(average)}/9) \times V_{CC}$$

$$P_{DAC} = (I_{CC(average)}/9) \times V_{CC} - P_{DCC(average)}$$

$$= (97.7/9) \times 5.0 - 2.65$$

$$= 51.6 \text{ mW/Channel}$$

Receiver switching losses, P_{RAC}, at 5 MHz:

$$P_{RAC} + P_{RCC(average)} = (I_{CC(average)}/9) \times V_{CC}$$

$$P_{RAC} = (I_{CC\ (average)}/9) \times V_{CC} - P_{RCC(average)}$$

$$= (36.0 \text{ mA}/9) \times 5.0 \text{ V} - 16.10$$

$$= 3.9 \text{ mW/Channel}$$

The output stage losses vary with the magnitude of the output voltages or the output transistor saturation voltages and with the load conditions. The following is based upon the solution of the equivalent circuit of a differential SCSI bus and no further proof is included in this analysis.

For the differential driver, the worst case condition is with a driver asserting the line with SCSI bus termination and a differential output voltage of about 2 V. Under these conditions there would be 144 mW dissipated in the output transistors when asserted and 71 mW when negated. The average output voltage of the SN75LBC976 driver is 2 V. As such, the average power dissipated in the output transistors is also a worst case condition.

Driver output dc losses, P_{DOH} is given by:

$$P_{DOH} = 144.0 \text{ mW/Channel}$$

The same circuit but with the line negated:

$$P_{DOL} = 71.0 \text{ mW/Channel}$$

The receiver output stage is rated for sinking 8.0 mA at a maximum low-level output voltage of 0.8 V.

Receiver output dc losses, P_{RO}, is given by:

$$P_{RO} = 8.0 \text{ mA} \times 0.8 \text{ V} = 6.4 \text{ mW/Channel maximum}$$

Since $P_{DCC} + P_{DAC} = P_{DO} >> P_{RCC} + P_{RAC} + P_{RO}$, the worst case power dissipation in a data channel occurs when the driver is enabled and transmitting data. This case will be used to analyse the device power dissipation.

Device Power Dissipation

Assuming the probability that any one bit on the bus is asserted is equal to the probability of being negated, the state of the output is non-deterministic, and the thermal time constant of the device is long with respect to the data transfer period, the mean die temperature will be determined by the mean power dissipation. In the driver output this is the mean of the asserted and negated values:

Mean device output dc losses:

$$P_{DO(DEV)} = (P_{DOH} + P_{DOL})/2 \times 9 \text{ Channels}$$
$$= (144 \text{ mW/Ch} + 71 \text{ mW/Ch})/2 \times 9 \text{ Channels}$$
$$= 967.5 \text{ mW}$$

From the assumptions above and the probability that the driver output will change state on the next cycle is equal to the probability that it will not, the mean power dissipated due to driver switching is one-half P_{DAC} which was measured with the switching loss occurring every cycle.

Mean device switching losses:

$$P_{DAC(DEV)} = P_{DAC}/2 \times 9 \text{ Channels}$$
$$= (51.6 \text{ mW/Ch})/2 \times 9 \text{ Channels}$$
$$= 232.2 \text{ mW}$$

Total Device quiescent power:

$$P_{DCC(DEV)} = P_{DCC(average)} \times 9 \text{ Channels}$$
$$= 2.65 \text{ mW/Ch} \times 9 \text{ Channels}$$
$$= 23.85 \text{ mW}$$

The total mean power dissipated in 9 enabled drivers transmitting over a SCSI bus for several package thermal time constants is then

$$P_{D(DEV)} = P_{DO(DEV)} + P_{DAC(DEV)} + P_{DCC(DEV)}$$
$$= 967.5 \text{ mW} + 232.2 \text{ mW} + 23.85 \text{ mW}$$
$$= 1223.6 \text{ mW}$$

4.3.4. Junction Temperature and Layout Considerations

Measurements of the thermally enhanced 56-pin SSOP package and lead frame used on the SN75LBC976DL were performed on a 130 mm by 98 mm six layer printed circuit board with the ground and heat sinking pins soldered to a common solder pad and connected to a second layer ground plane through one via interconnect, see Figure 5.39. The ground plane was 0.254 mm below the surface of the board and was a 1 oz copper layer. The results of two tests resulted in θ_{JA}s of 52.9 and 46.6°C/W with zero air flow.

The mean junction temperature rise above ambient when all drivers are enabled and transmitting data over the SCSI bus for several package thermal time constants can then be calculated.

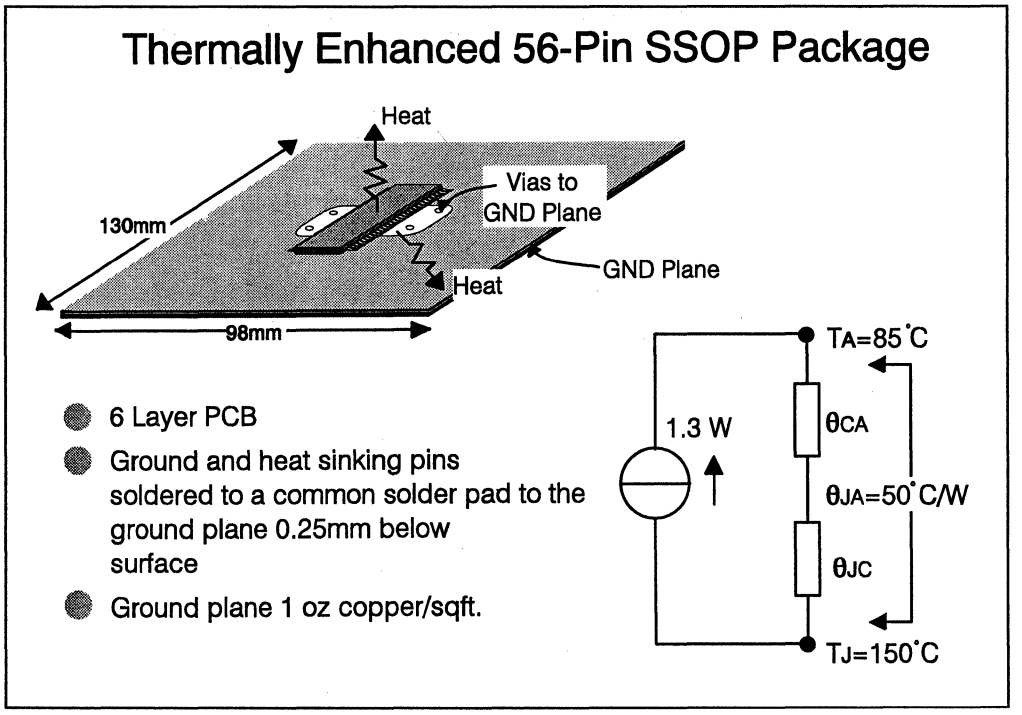


Figure 5.39 - Thermally Enhanced 56-pin SSOP Package

Junction temperature rise above ambient:

$$T_J - T_A = \theta_{JA} \times P_{D(DEV)}$$
$$= (52.9°C/W + 46.6°C/W)/2 \times 1233.6°mW \times 1\ W/1000\ mW$$
$$= 60.8°C$$

Most designs require two junction temperature conditions to be met. The junction operating temperature should not exceed 150°C under worst case operating conditions and the average operating junction temperature should be no more than 110°C.

Since the worst case condition of all nine channels transmitting data was used for analysis, the maximum ambient air temperature, T_A, with no air flow should be:

$$T_{A(maximum)} = 150°C - 60.8°C$$
$$= 89.2°C$$

When evaluating the average operating junction temperature the effects of transmit/receive duty cycle communication port activity must be taken into account.

4.4.Driving the 'Wired-Or' SCSI Lines with the SN75LBC976

The control lines of the SCSI bus have three 'Wired-Or' lines, these are BSY (busy), RST (reset), and SEL (select). These lines are wired-or in that the line drivers connected to these lines drive in one direction (assertion) only and are tri-stated (high impedance) when negated. This allows numerous drivers to be active at the same time without affecting the logic state of the line and requires that all drivers be released or off before the logical state can change. When tri-stated the bus termination network passively negates the signal.

The technique used for wired-or operation with differential transceivers is to input the signal into the driver enable pin and connect the driver input to a fixed logic level input. When the input signal to the driver enable is active (high), the driver becomes enabled and the outputs drive the SCSI bus to the state of the driver input. When the input signal at the driver enable pin goes low, the driver turns off and allows the bus termination to negate the signal on the bus after all other drivers on the bus are also shut off.

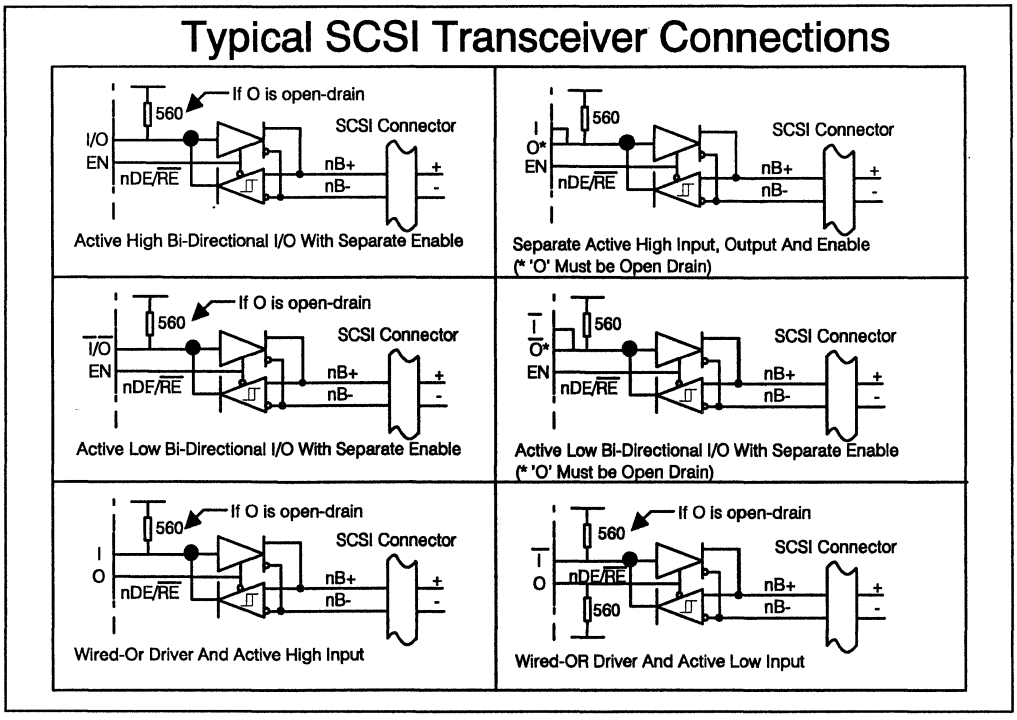


Figure 5.40 - Typical SCSI Transceiver Connections

Many communications controllers used for differential SCSI have separate inputs and outputs for these signals. When used with the SN75176 type RS-485 transceiver, these controller I/Os can be directly connected to separate driver enable inputs or receiver outputs. The SN75LBC976 device does not have a separate driver input and receiver input, these are tied together internally to save pins.

Controllers with separate I/Os can still be used with the 'LBC976 using the connections shown in Figure 5.40. The controller output will go high and enable the driver and disable the receiver. Upon disabling the receiver, the external pull-up or pull-down resistor will drive pin A of the 'LBC976 to the proper level for bus assertion and the driver will assert the SCSI signal line. When the controller output goes low, the driver disables and allows the termination to negate the bus signal. After a short delay, the receiver outputs are enabled and will reflect the logical state of the bus signal.

5. Summary and Further Information

5.1. EIA Standards

For copies of the EIA standards please contact the Electronic Industries Association. For details and a copy of the Catalog of EIA & Jedec Standards & Engineering Publications contact the EIA Standard Sales office at the following address and telephone number:

EIA Standard Sales Office
2001 Pennsylvania Avenue, N.W.
Washington, D.C. 20006
United States
Telephone Number + 1 (202) 457-4966

5.2. References

The following books were invaluable in producing the Section on data transmission:

1. **Digital, Analog, and Data Communication** - William Sinnema & Tom McGovern - Prentice-Hall International - ISBN 0-835-91313-9.

2. **Data Transmission** - D. Tugal and O. Tugal - McGraw Hill - 1980

5.3. Texas Instruments - Completing the Picture

The range of products discussed throughout this section demonstrate the commitment made by Texas Instruments to the field of peripheral interfacing. Use of leadership technologies has enabled the production of high performance, reliable line drive/receive functions and highly integrated controllers.

Obviously in a seminar this short it is impossible to cover all TI's data transmission products. The reader is encouraged to contact a TI representative to obtain the latest data books on transmission ICs. As a minimum the designer should posses a copy of the Interface Circuits Data Book.

Finally, although we have discussed the older standards such as EIA-232 and RS-485 TI is continuing to work and participate in the various standard definition committees to ensure new and emerging standards gain the full support of TI's semiconductor experience. Testimony to this fact has been the SN75LBC976 RS-485 transceiver, the specifications for which were closely aligned with the outcome of the work done by the SCSI-3 standards group.

Over the next 12 months TI will be releasing products in support of Futurebus+, and is actively supporting the P1394 high speed serial bus Working Group among others.

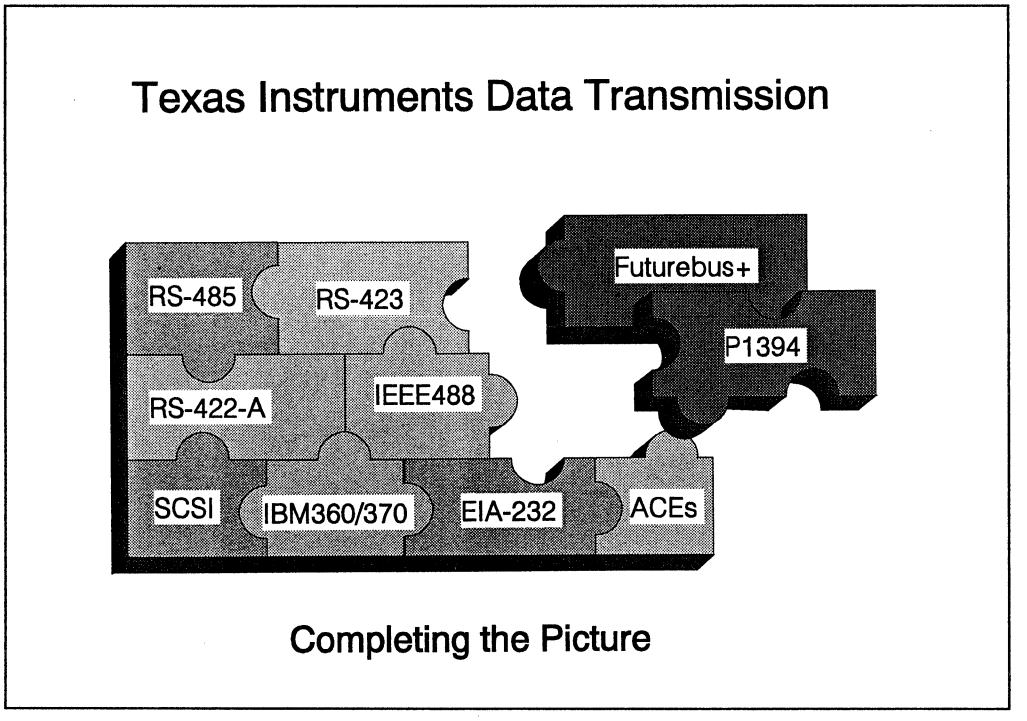


Figure 5.41 - Texas Instruments Data Transmission - Completing the Picture

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example: **SN** **75189** **N** **-00**

Prefix

MUST CONTAIN TWO, THREE, OR FOUR LETTERS

SN ..... TI Special Functions or Interface Products
TL ..... TI Linear Products

STANDARD SECOND-SOURCE PREFIXES

AM ..... Advanced Micro Devices
DP or DS ..... National
LT ..... Linear Technology
MAX ..... Maxim Integrated Products
MC ..... Motorola
N8T ..... Signetics
uA ..... Fairchild/National

Unique Circuit Description

MUST CONTAIN THREE TO EIGHT CHARACTERS
(From Individual Data Sheets)

Examples: 232 75160B
3695 75C1154
75115 75ALS180

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FK, FN, J, JD, JG, N, NT, NS, P, PS, W
(From Pin-Connection Diagrams on Individual Data Sheet)

Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

-00 No special instructions
-10 Solder-dipped leads (N, NT packages only)

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (D, DB, DL, DW, J, JD, JG, N, NT, P)
– Slide Magazines
– A-Channel Plastic Tubing
– Sectioned cardboard box
– Individual Cardboard Box

Chip Carriers (FK, FN, FT)
– Anti-Static Plastic Tubing
Flat (W)
– Wells Carrier

Dual-In-Line Surface Mount (DR, DBLE, DLR, DWR, NSLE, PSLE)
– Taped and Reeled

Military Data Transmission Nomenclature

Example: SNJ 55 109A J

Prefix

SN = Standard
SNJ = Class B Processing

Second-Source Prefix

AM = AMD
MC = Motorola

Operating Temperature Range

55 = Military
–55°C to 125°C
95 = Nonstandard

Unique Circuit Description

Possibly with A or B in Last Positiion

Package Designation

FK = LCC
J = C-DIP
JG = 8-Pin C-DIP
W = Flatpack

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

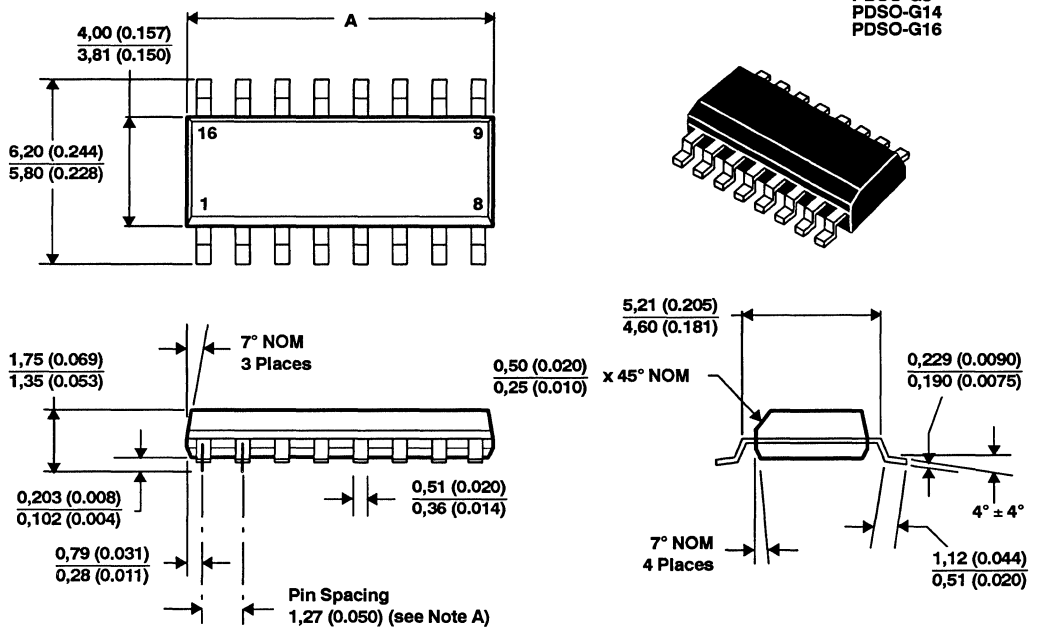
D008, D014, and D016
plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)

Designation per JEDEC Std 30:

PDSO-G8
PDSO-G14
PDSO-G16



DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

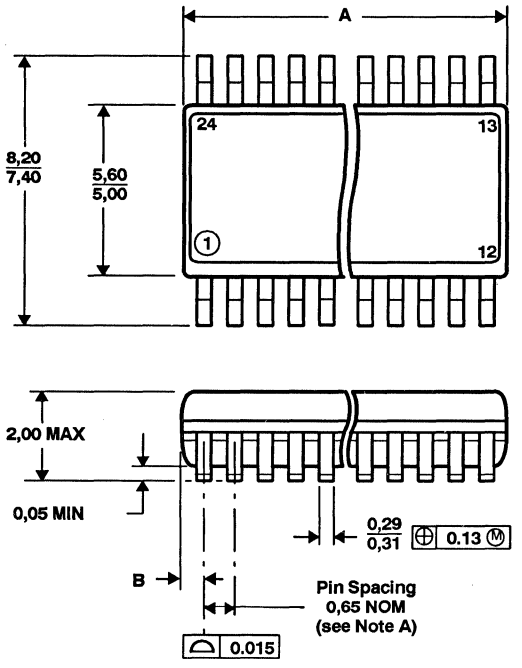
DB008, DB014, DB016, DB020, DB024, DB028, DB030
plastic shrink small-outline packages

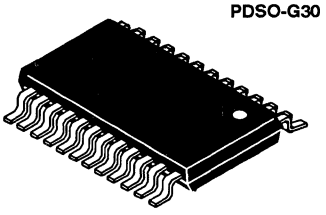
These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DB008, DB014, DB016, DB020, DB024, DB028, DB030
(24-pin package used for illustration)

Designation per JEDEC Std 30:

PDSO-G8
PDSO-G14
PDSO-G16
PDSO-G20
PDSO-G24
PDSO-G28
PDSO-G30





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold or flash end protrusion shall not exceed 0,15 mm.
D. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
E. Lead tips to be planar within ±0,05 mm exclusive of solder.

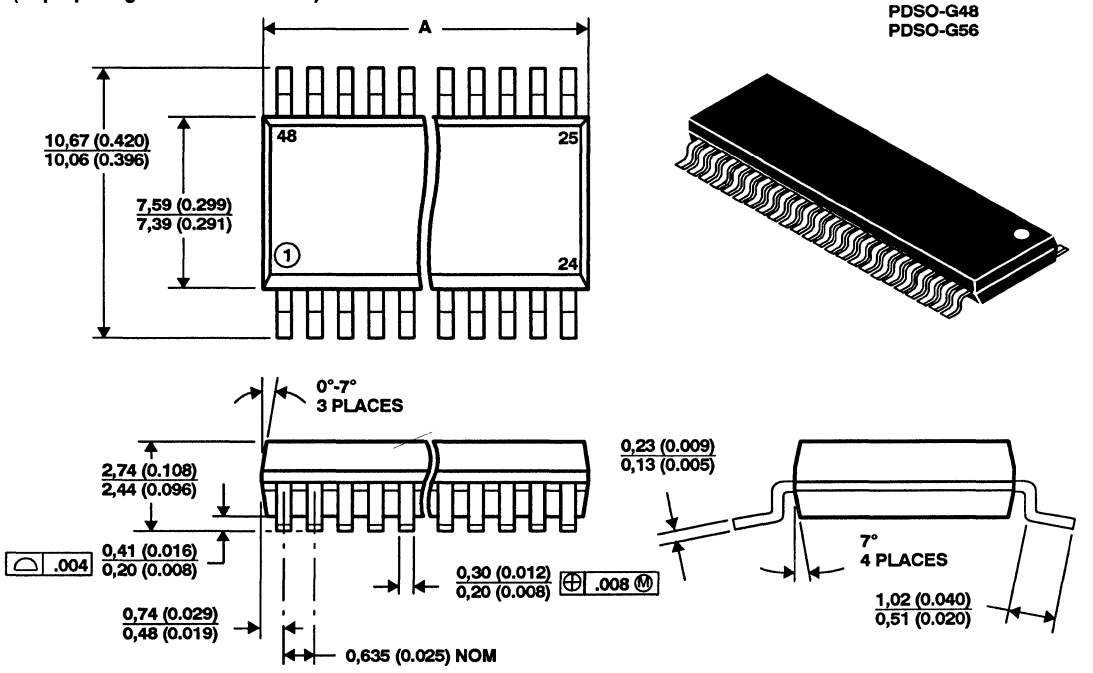
PINS / DIM	8	14	16	20	24	28	30
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50
B MAX	0,68	1,30	0,98	0,83	0,68	1,03	0,70

DL028, DL048, and DL056
plastic shrink small-outline packages

Each of these shrink small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DL028, DL048, and DL056
(48-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G28
PDSO-G48
PDSO-G56



DIM \ PINS	28	48	56
A MIN	9,46 (0.370)	15,75 (0.620)	18,29 (0.720)
A MAX	9,65 (0.380)	16,00 (0.630)	18,54 (0.730)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

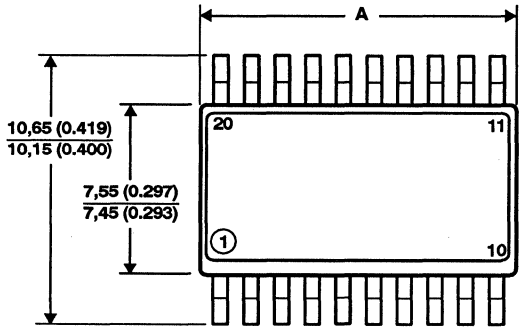
NOTES: A. Body dimensions do not include mold flash or protrusion.
B. End protrusion shall not exceed 0,15 (0.006).
C. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
D. Lead tips to be planar within ±0,05 (0.002).

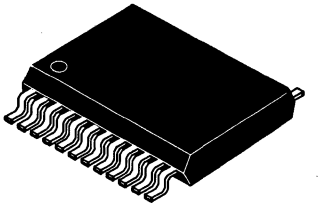
DW016, DW020, DW024, and DW028 plastic small-outline packages

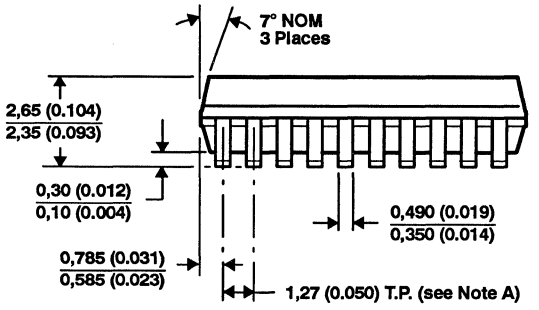
Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

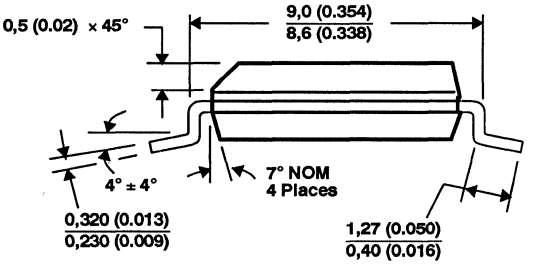
DW016, DW020, DW024, and DW028
(20-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G16
PDSO-G20
PDSO-G24
PDSO-G28









DIM \ PINS	16	20	24	28
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed, 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

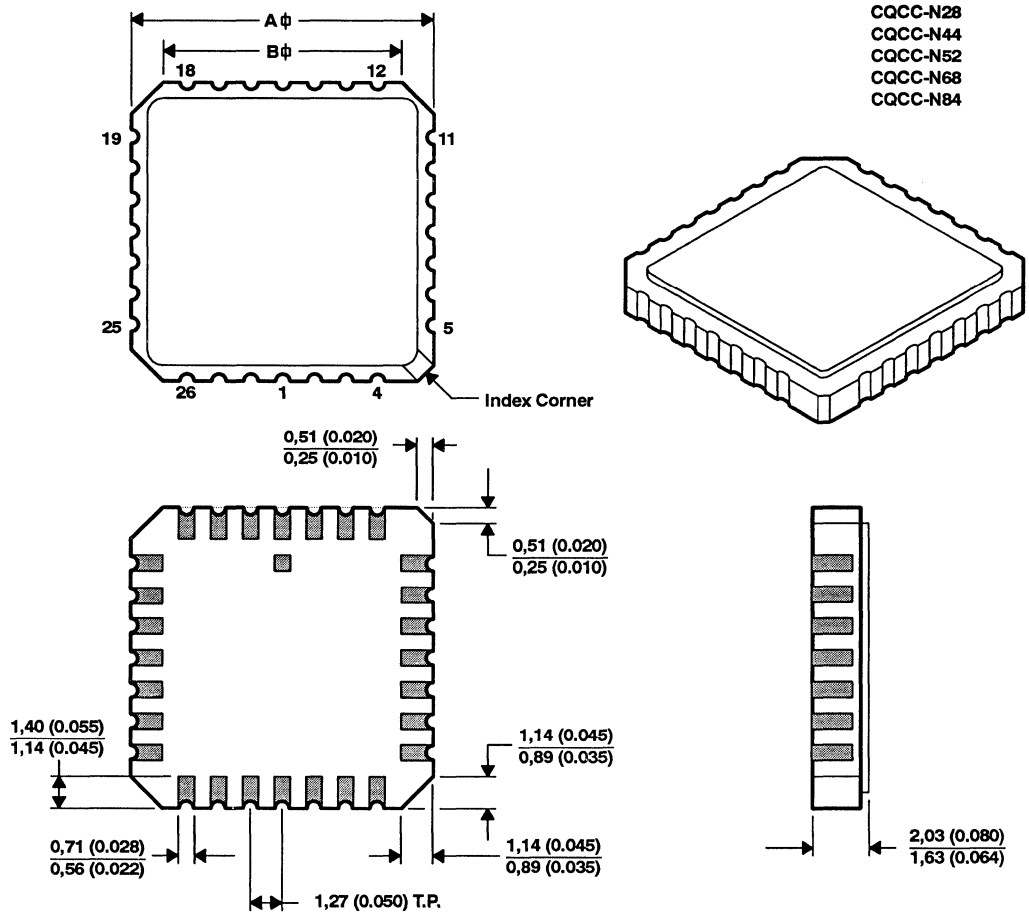
FK020, FK028, FK044, FK052, FK068, and FK084
ceramic chip carrier

Each of these hermetically-sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. These packages are intended for surface mounting on solder leads on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

FK020, FK028, FK044, FK052, FK068, AND FK084
(28-pin package used for illustration)

Designation per JEDEC Std 30:
CQCC-N20
CQCC-N28
CQCC-N44
CQCC-N52
CQCC-N68
CQCC-N84



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier (continued)

JEDEC OUTLINE DESIGNATION†	NUMBER OF TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS-004-CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS-004-CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS-004-CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS-004-CE	52	18,78 (0.740)	19,32 (0.760)	12,58 (0.495)	14,22 (0.560)
MS-004-CF	68	23,83 (0.938)	24,43 (0.962)	21,60 (0.850)	21,80 (0.858)
MS-004-CG	84	28,99 (1,141)	29,59 (1.164)	26,60 (1.047)	27,00 (1.063)

† All dimensions and notes for the specified JEDEC outline apply.

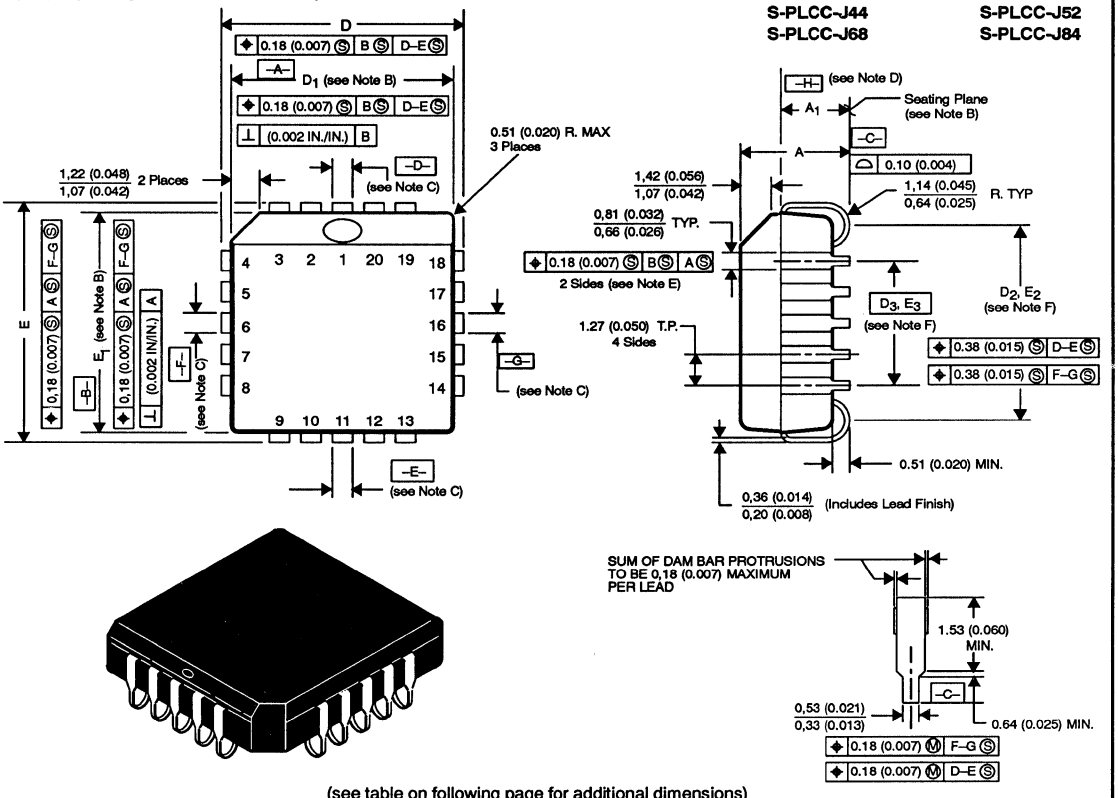
FN020, FN028, FN044, FN052, FN068, and FN084
plastic J-leaded chip carrier

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN052, FN068, and FN084
(20-pin package used for illustration)

Designation per JEDEC Std 30:

S-PLCC-J20	**S-PLCC-J28**
S-PLCC-J44	**S-PLCC-J52**
S-PLCC-J68	**S-PLCC-J84**



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M-1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

C. Datums [D – E] and [F – G] for center leads are determined at datum [– H –].

D. Datum [– H –] is located at top of leads where they exit plastic body.

E. Location of datums [– A –] and [– B –] to be determined at datum [– H –].

F. Determined at seating plane [– C –].

FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier (continued)

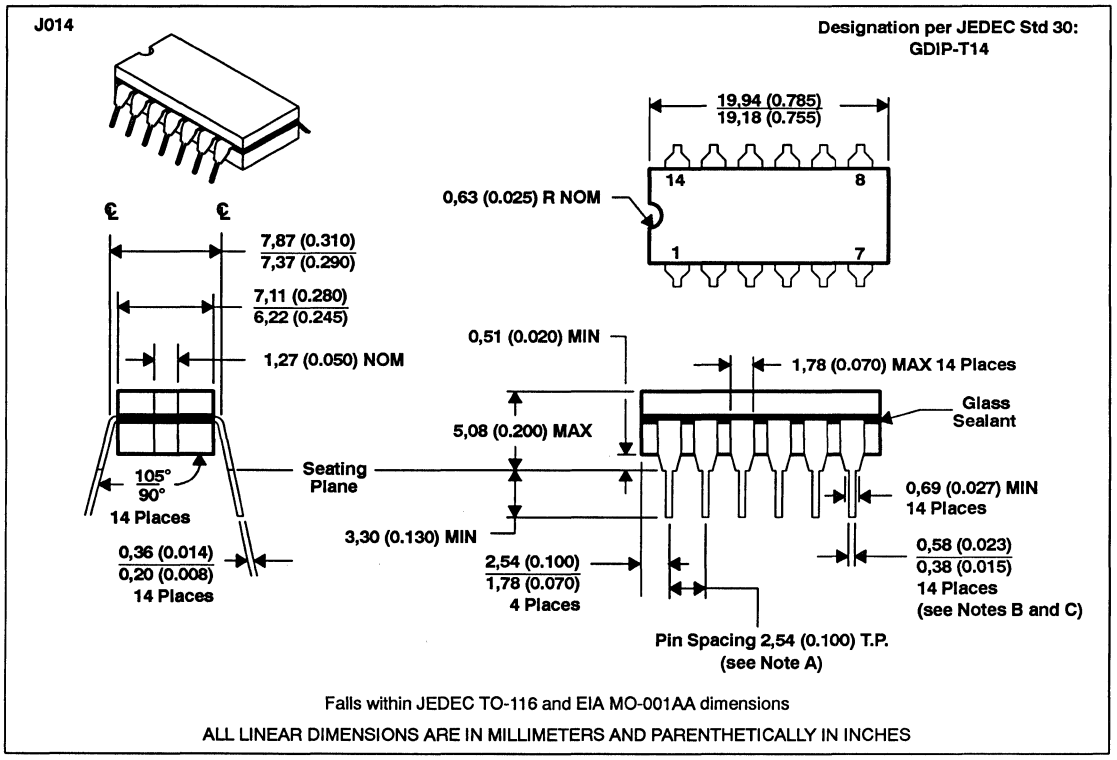
JEDEC OUTLINE	NO.OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2		D_3, E_3
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	BASIC
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 90.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.141)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES A: All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M-1982.

F: Determined at seating plane $\boxed{-C-}$.

J014
ceramic dual-in-line package

This hermetically-sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



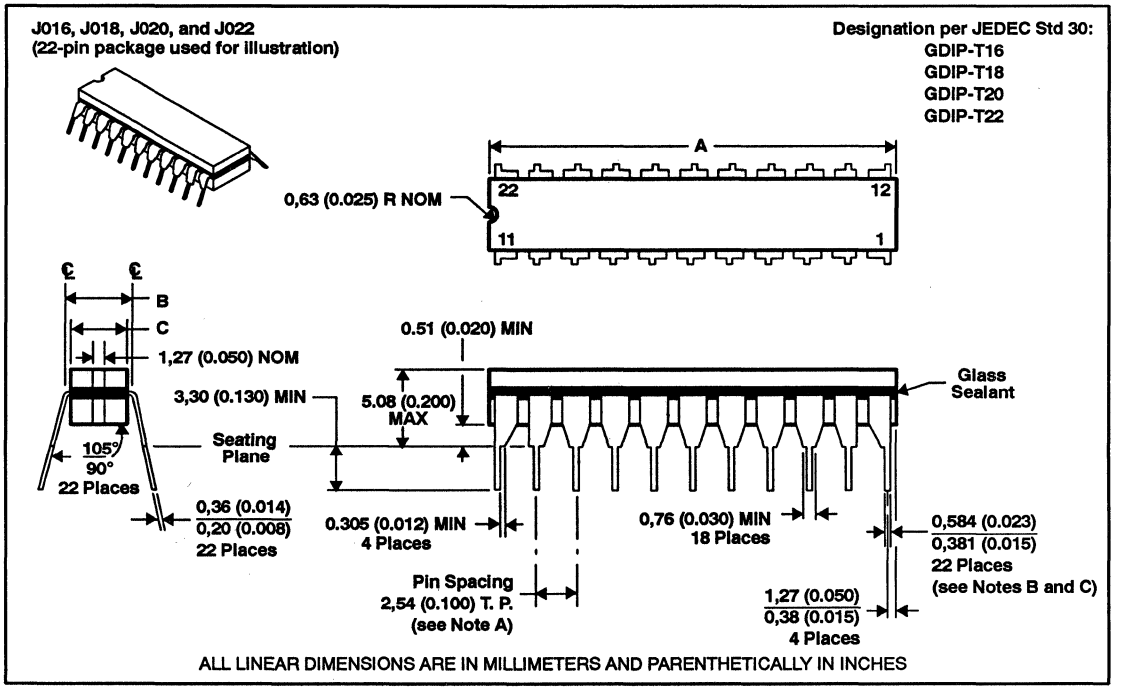
Falls within JEDEC TO-116 and EIA MO-001AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

J016, J018, J020, and J022 ceramic dual-in-line

These hermetically-sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. These packages are intended for insertion in mounting-hole rows of 7,62 (0.300) centers for the J016, J018, J020, and 10,16 (0.400) centers for the J022, respectively. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (bright-dipped) leads require no additional cleaning or processing when used in solder assembly.

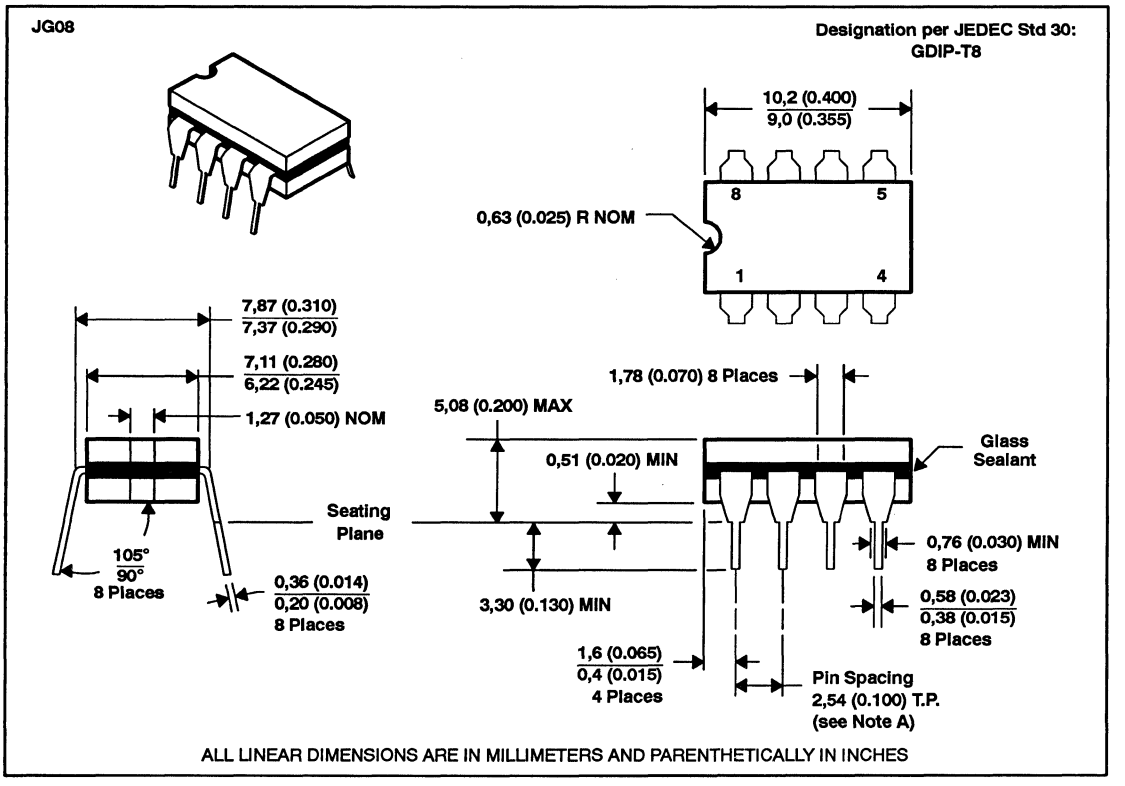


PINS \ DIM	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
16	19,18 (0.755)	19,94 (0.785)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
18		23,1 (0.910)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
20	23,62 (0.930)	24,76 (0.975)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
22		28,0 (1.100)	9,91 (0.390)	10,41 (0.410)		9,65 (0.388)

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JG008
ceramic dual-in-line package

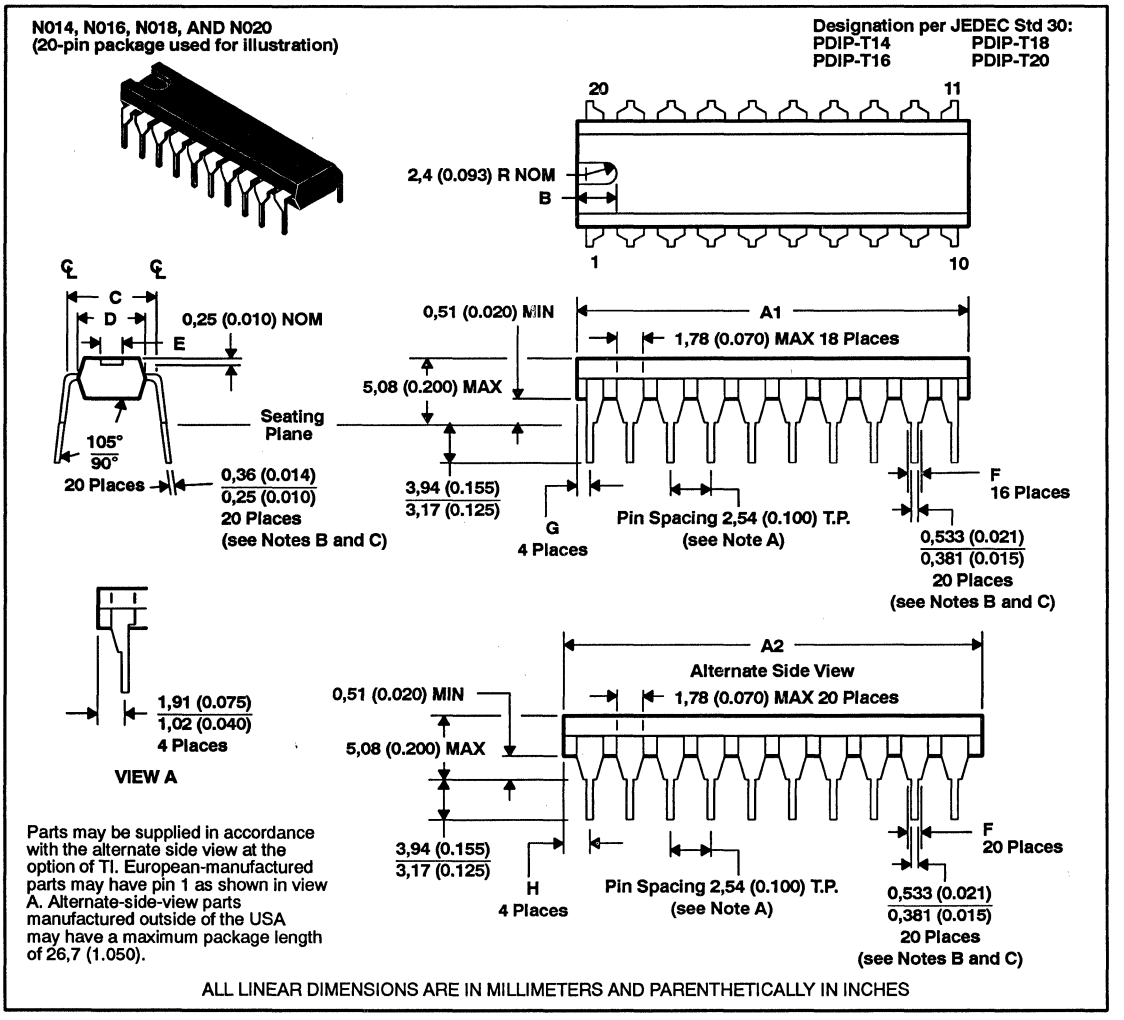
This hermetically-sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N014, N016, N018, and N020
300-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

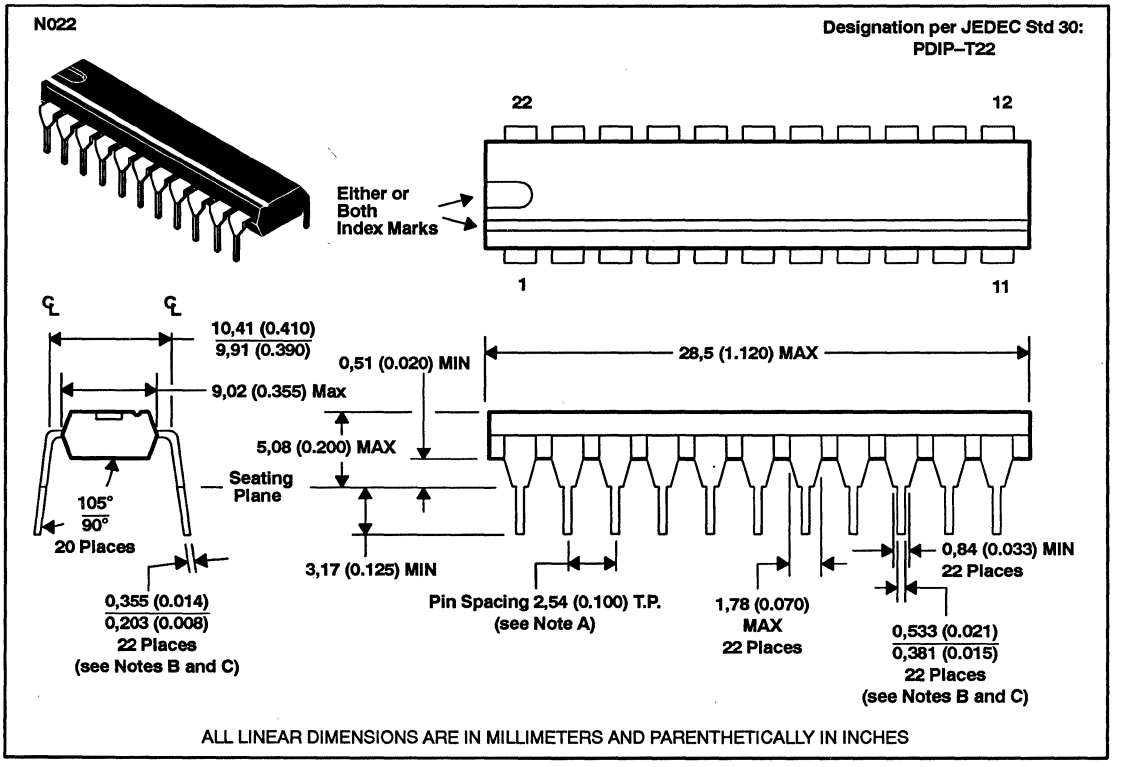
N014, N016, N018, and N020
300-mil plastic dual-in-line package (continued)

DIM \ PIN		14	16	18	20
A1	MIN	18,0 (0.710)			23,22 (0.914)
	MAX	19,8 (0.780)	19,8 (0.780)	23,4 (0.920)	24,77 (0.975)
A2	MIN	18,0 (0.710)			23,62 (0.930)
	MAX	19,8 (0.780)			25,4 (1.000)
B	NOM	2,8 (0.110)	2,8 (0.110)	4,06 (0.160)	2,80 (0.110)
C	MIN	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)
	MAX	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)
D	MIN	6,10 (0.240)	6,10 (0.240)		6,60 (0.240)
	MAX	6,60 (0.260)	6,60 (0.260)	6,99 (0.275)	7,11 (0.280)
E	NOM	2,0 (0.080)	2,0 (0.080)	2,03 (0.080)	2,0 (0.080)
F	MIN	0,84 (0.033)	0,84 (0.033)	0,89 (0.035)	0,84 (0.033)
G	MIN	See Note D	0,38 (0.015)	See Note D	1,68 (0.066)
	MAX	See Note D	1,65 (0.065)	See Note D	0,22 (0.009)
H	MIN	2,54 (0.100)	1,02 (0.040)	0,23 (0.009)	0,38 (0.015)
	MAX	1,52 (0.060)	2,41 (0.095)	1,91 (0.075)	1,27 (0.050)

NOTE D: The 14-pin and 18-pin plastic dual-in-line package is only offered with the external pins shaped in their entirety, and do not have alternate side view dimensions.

N022
400-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

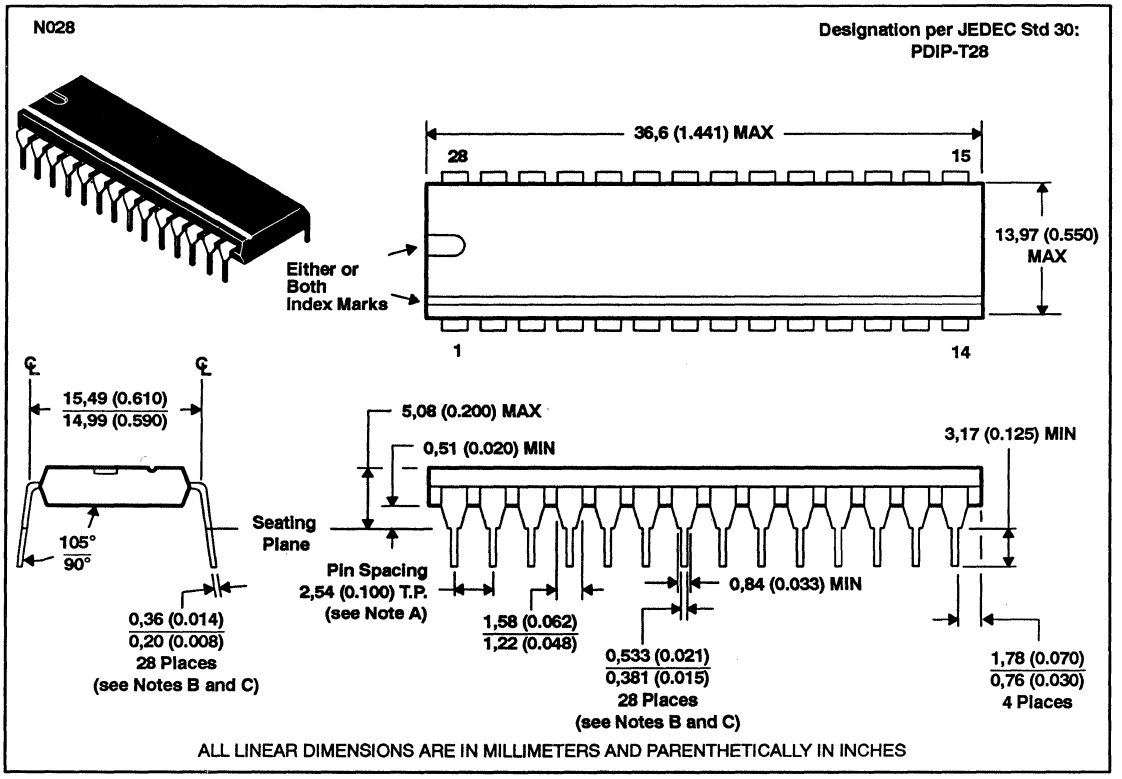


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028
600-mil plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



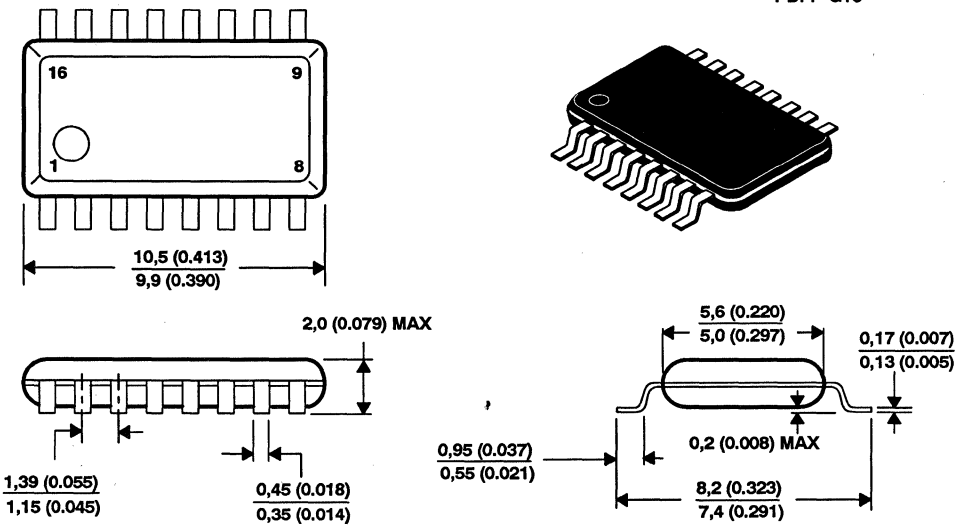
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NS016
plastic package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

NS016

Designation per JEDEC Std 30:
PDFP-G16

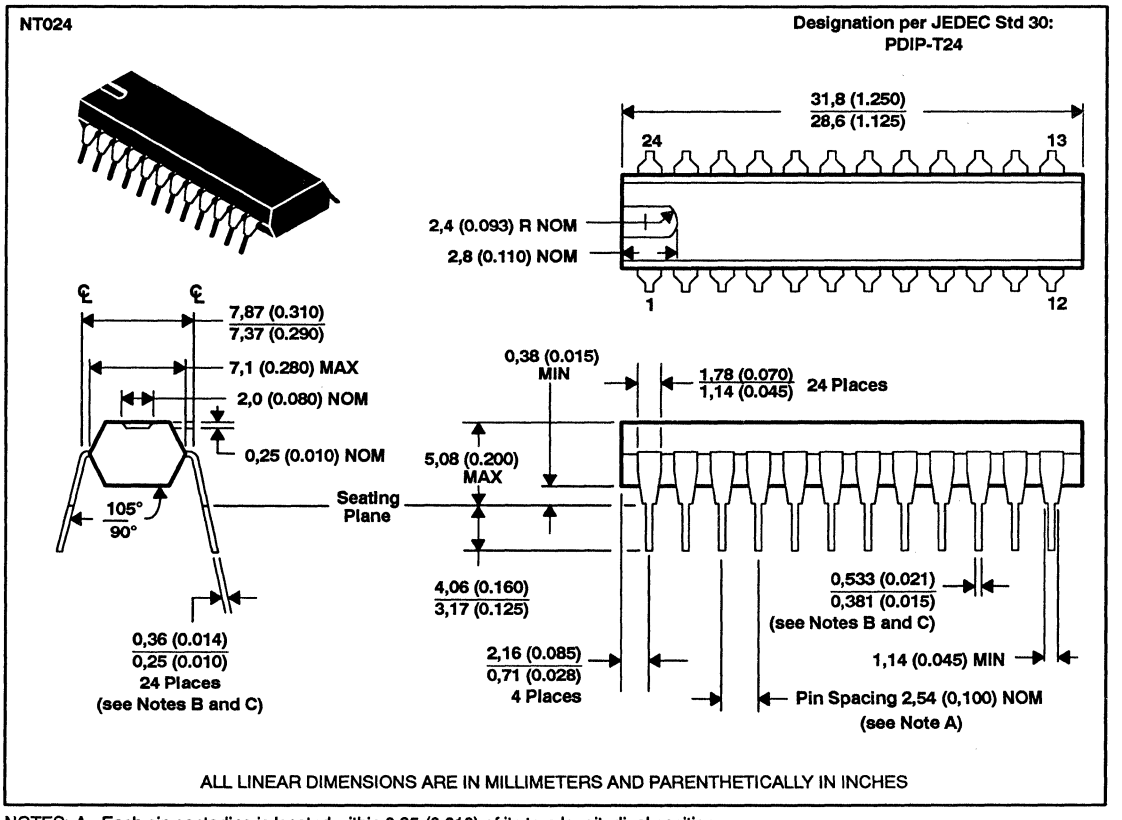


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NT024
300-mil plastic dual-in-line packages

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin package, the letter N is used by itself since the 24-pin package may be available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



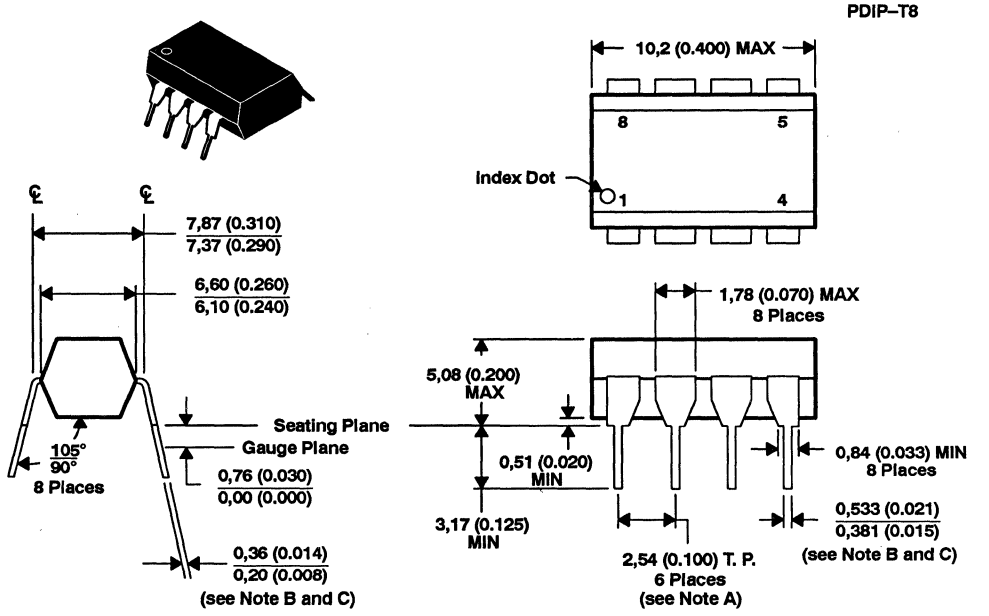
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P008
plastic dual-in-line package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound.The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated lead require no additional cleaning or processing when used in soldered assembly.

P008

Designation per JEDEC Std 30:
PDIP–T8



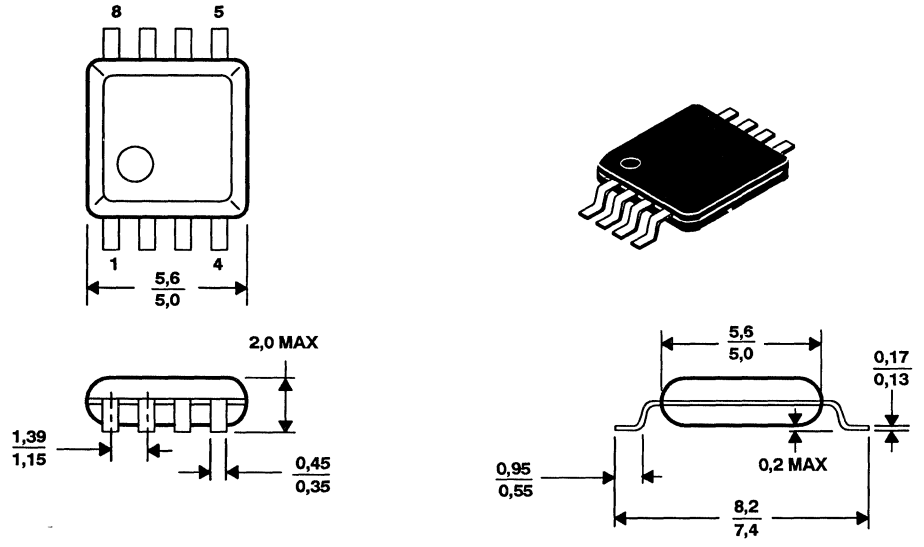
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

PS
plastic dual-in-line package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

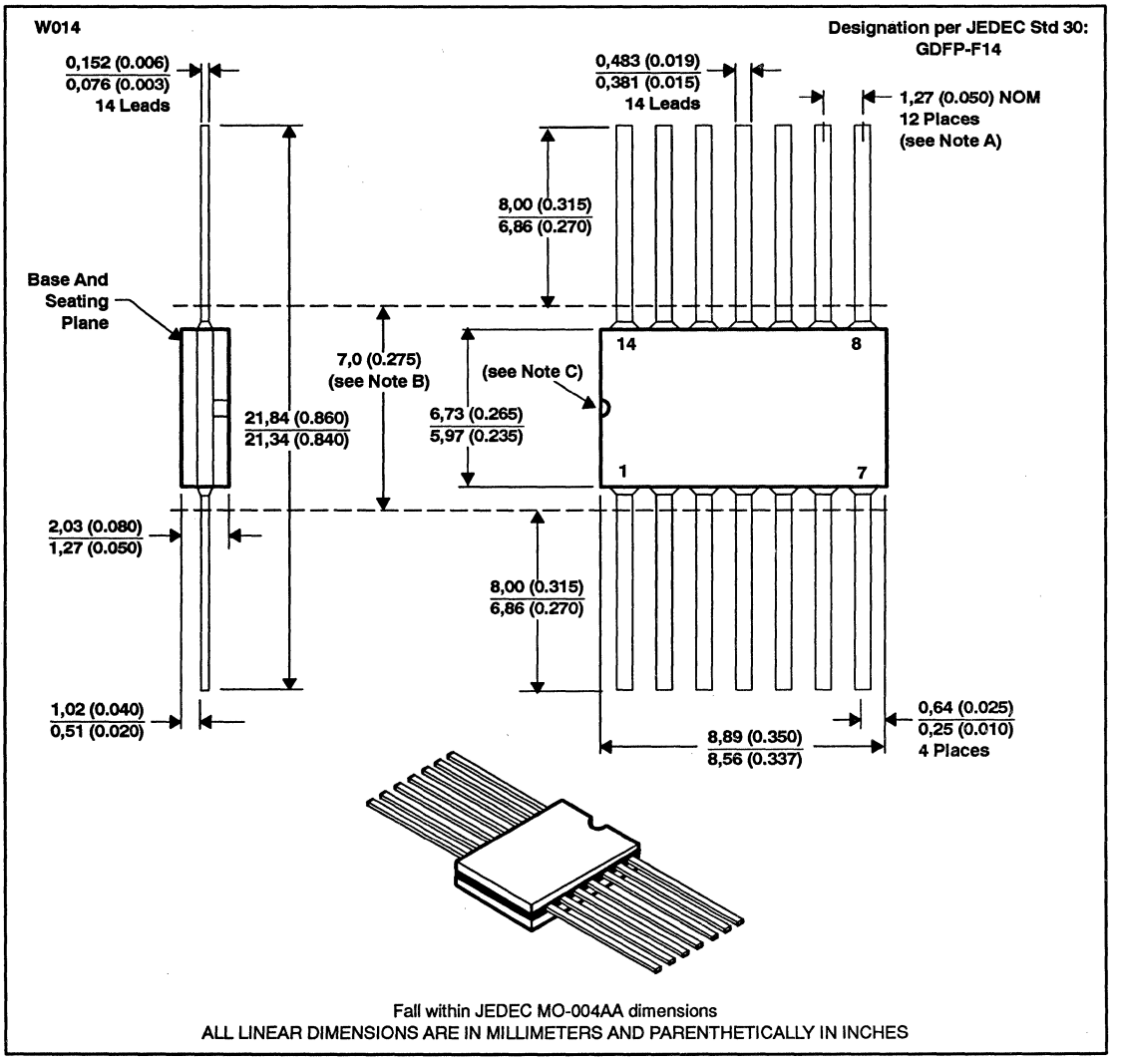
PS008



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

W014
ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

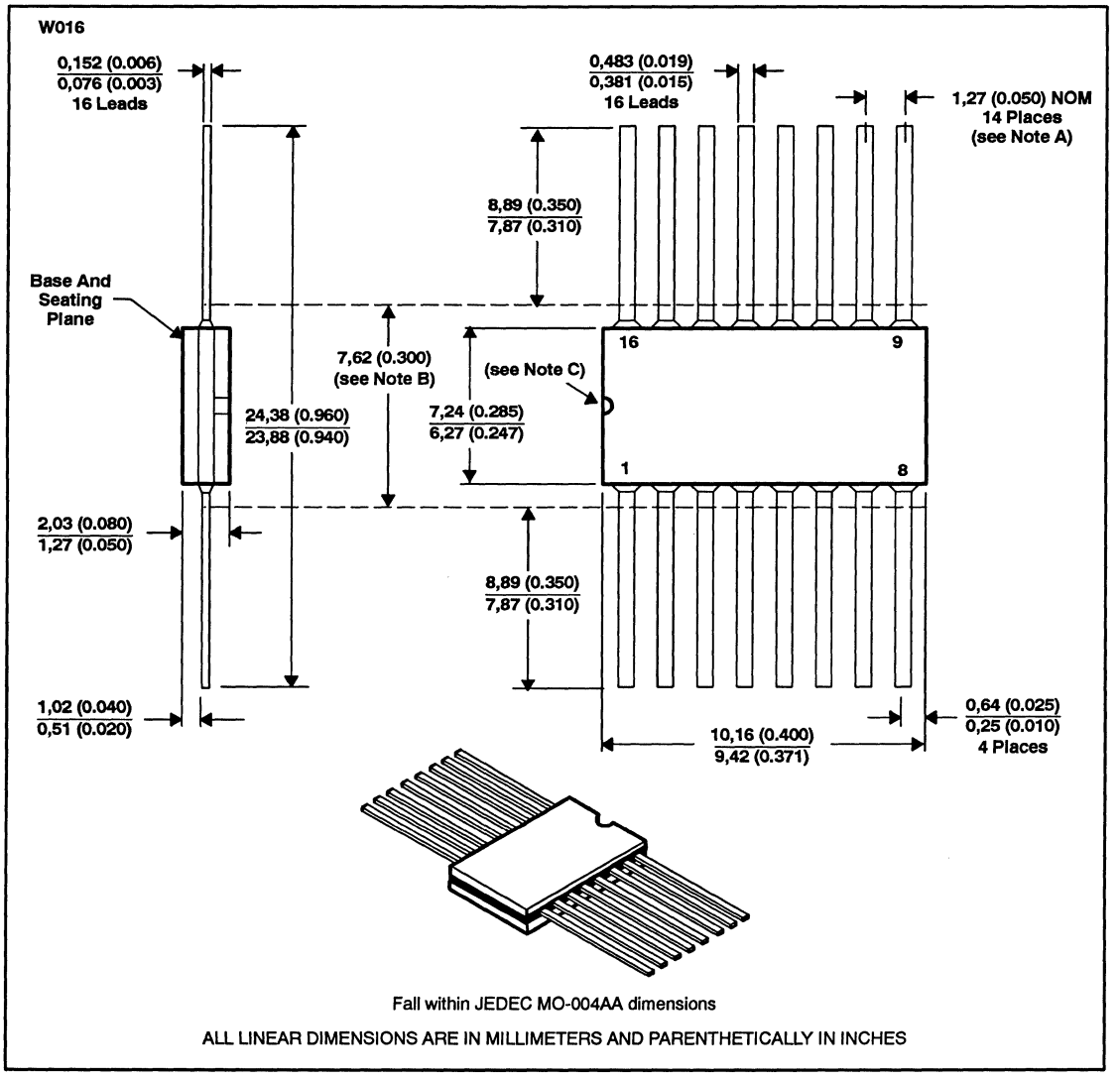


Fall within JEDEC MO-004AA dimensions
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

W016
ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



Fall within JEDEC MO-004AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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