Data Book

MOS Memory
Commercial and Military Specifications

1993

TEXAS INSTRUMENTS

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INTRODUCTION

The 1993 *MOS Memory Data Book* from Texas Instruments includes complete detailed specifications on the expanding MOS Memory product line including Dynamic Random Access Memories (DRAMs), Single-In-Line Memory Modules (SIMMs), Erasable Programmable Read-Only Memories (EPROMs), One-Time Programmable Read-Only Memories (OTP PROMs), Electrically Erasable Programmable Read-Only Memories (Flash Memories), Video RAMs (VRAMs), Field Memories (FMEMs), and Memory Cards. Also included are military specifications for DRAMs, EPROMs, and VRAMs.

The data book is divided into 13 chapters. Below you will find a brief description of each chapter.

Chapter 1. General Information — Includes an alphanumeric index for quickly finding device numbers and a part number guide with ordering information.

Chapter 2. Selection Guide — An easy-to-use reference guide that includes specific device information. Page numbers are also shown for easy access to the detailed specifications.

Chapter 3. Glossary/Timing Conventions/Data Sheet Structure — Defines terms and standards used throughout the data book.

Chapter 4–9. Product specifications for over 100 devices can be found in these sections.

Chapter 10. Logic Symbols — Includes an explanation and examples of the IEEE standard.

Chapter 11. Quality and Reliability — Details selected processes and the philosophies of Texas Instruments that are used to ensure high quality standards.

Chapter 12. Electrostatic Discharge Guidelines — Because all MOS Memory devices are ESD-sensitive, handling guidelines are included.

Chapter 13. Mechanical Data — Detailed package drawings and specifications are shown in this section.

For ordering information or further assistance, please contact your nearest Texas Instruments Sales Office or Distributor as listed in the back of this book.

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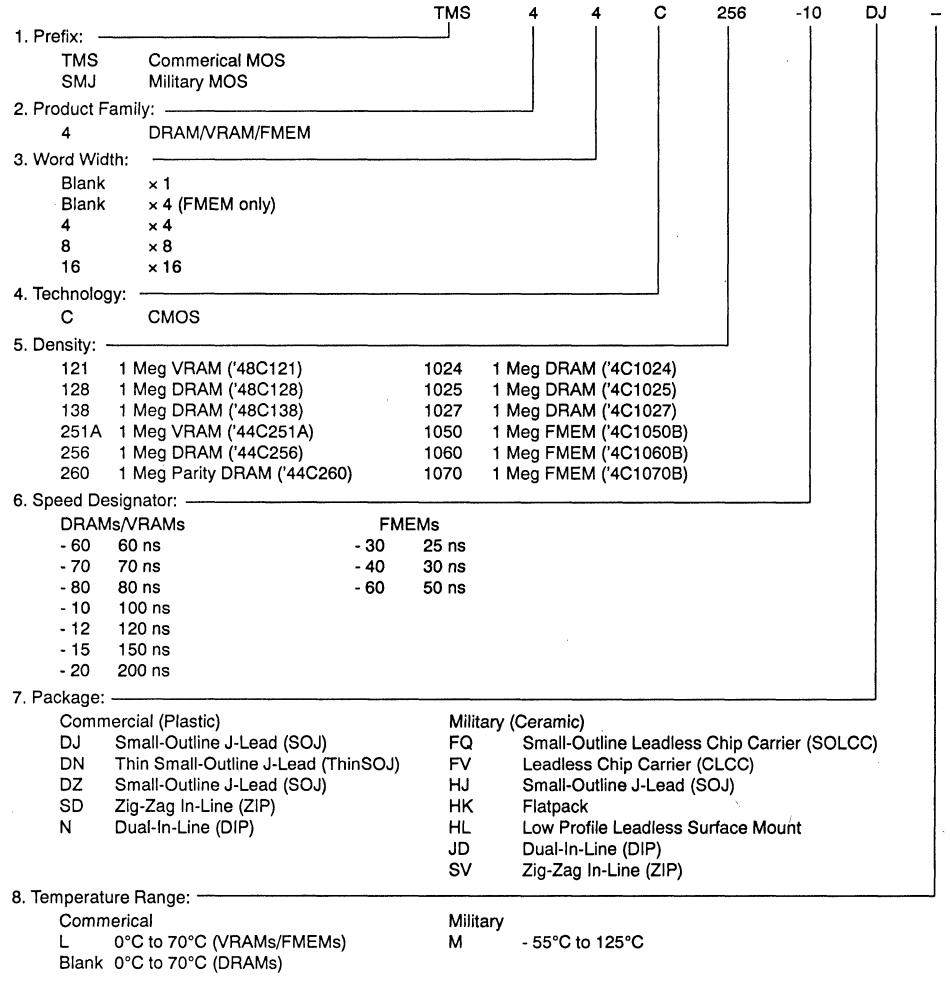
DRAM/VRAM/FMEM Ordering Information

Factory orders for 1 Meg DRAMs, VRAMs, and FMEMs described in this book should include an eight-part type number as explained in the following example:



DRAM Ordering Information

Factory orders for the 4 Meg and 16 Meg DRAMs described in this book should include an eight-part type number as explained in the following example:

TMS 4 4 1 00 -80 DM –

1. Prefix:
   - TMS Commercial MOS
   - SMJ Military MOS
2. Product Family:
   - 4 DRAM
3. Density — Refresh:
   - 2 2 Meg 1K Refresh
   - 4 4 Meg 1K Refresh
   - 5 4 Meg 512 Cycle Refresh
   - 6 4 Meg 1K Refresh 3.3 V
   - 7 4 Meg 512 Cycle Refresh 3.3 V
   - 16 16 Meg 4K Refresh 5 V
   - 17 16 Meg 2K Refresh 5 V
   - 18 16 Meg 1K Refresh 5 V
   - 26 16 Meg 4K Refresh 3.3 V
   - 27 16 Meg 2K Refresh 3.3 V
   - 28 16 Meg 1K Refresh 3.3 V
4. Organization — I/O:
   - 10 × 1 Std
   - 26 × 2 Quad-CAS
   - 40 × 4 Std
   - 41 × 4 WPB
   - 46 × 4 Quad-CAS
   - 80 × 8 Std
   - 81 × 8 WPB
   - 90 × 9 Std
   - 91 × 9 WPB
   - 16 × 16 Std
   - 17 × 16 WPB
   - 18 × 18 Std
   - 19 × 18 WPB
5. Functional Mode/Options:
   - 0 Enhanced Page Mode
   - 0 Enhanced Page Mode 2 $\overline{CAS}$ (×16 and ×18 Devices)
   - 0 Enhanced Page Mode 4 $\overline{CAS}$ (Quad-CAS Devices)
   - 1 Nibble Mode
   - 2 Static Column Decode Mode (SCD)
   - 2 SCD 2 $\overline{CAS}$ (×16 and ×18 Devices)
   - 3 Serial Mode
   - 5 Enhanced Page Mode 2 $\overline{WE}$ (×16 and ×18 Devices)
   - 6 Burst Mode
   - 7 SCD With Burst Mode
   - 8 SCD 2 $\overline{WE}$ (×16 and ×18 Devices)
6. Speed Designator:
   - -60 60 ns
   - -70 70 ns
   - -80 80 ns
   - -10 100 ns
   - -12 120 ns
   - -15 150 ns
7. Package:

   Commercial (Plastic)
   - DGA 300-mil Thin Small Outline (TSOP) (26-lead)
   - DGB 300-mil Reverse Lead Thin Small Outline (TSOP) (26-lead)
   - DGC 400-mil Thin Small Outline (TSOP) (28-lead)
   - DGD 400-mil Reverse Lead Thin Small Outline (TSOP) (28-lead)
   - DGE 400-mil Thin Small Outline (TSOP) (44-lead)
   - DGF 400-mil Reverse Lead Thin Small Outline (TSOP) (44-lead)
   - DC 400-mil Thin Small Outline (TSOP) (50/44-lead) 0.8 mm pitch
   - DE 400-mil Thin Small Outline (TSOP) (32-lead) 1.27 mm pitch
   - DJ 300-mil Small Outline J-Lead (SOJ) (26/24-lead)
   - DM 350-mil Small Outline J-Lead (SOJ)
   - DN Thin Small Outline J-Lead (SOJ)
   - DZ 400-mil Small Outline J-Lead (SOJ)
   - RE 400-mil Small Outline J-Lead (SOJ) (50-mil pitch)
   - SD Zig-Zag In-Line (ZIP)
   - RVA Vertical Package (VPAK)

   Military (Ceramic)
   - HM Small-Outline Leadless Chip Carrier (SOLCC)
   - HJ Small-Outline J-Lead (SOJ)
   - HR Flatpack
   - JD Side-Brazed Dual-In-Line
8. Temperature Range:

   Commercial
   - Blank 0°C to 70°C

   Military
   - M – 55°C to 125°C

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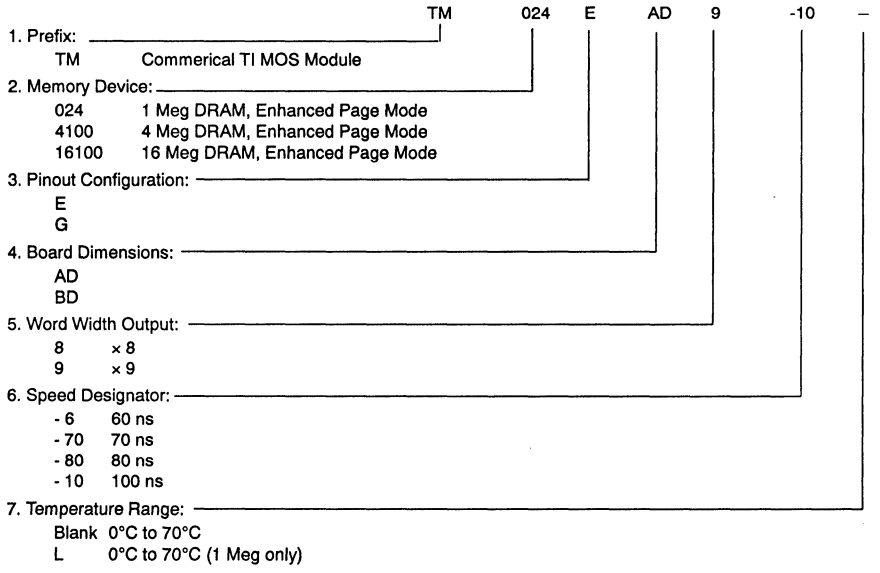
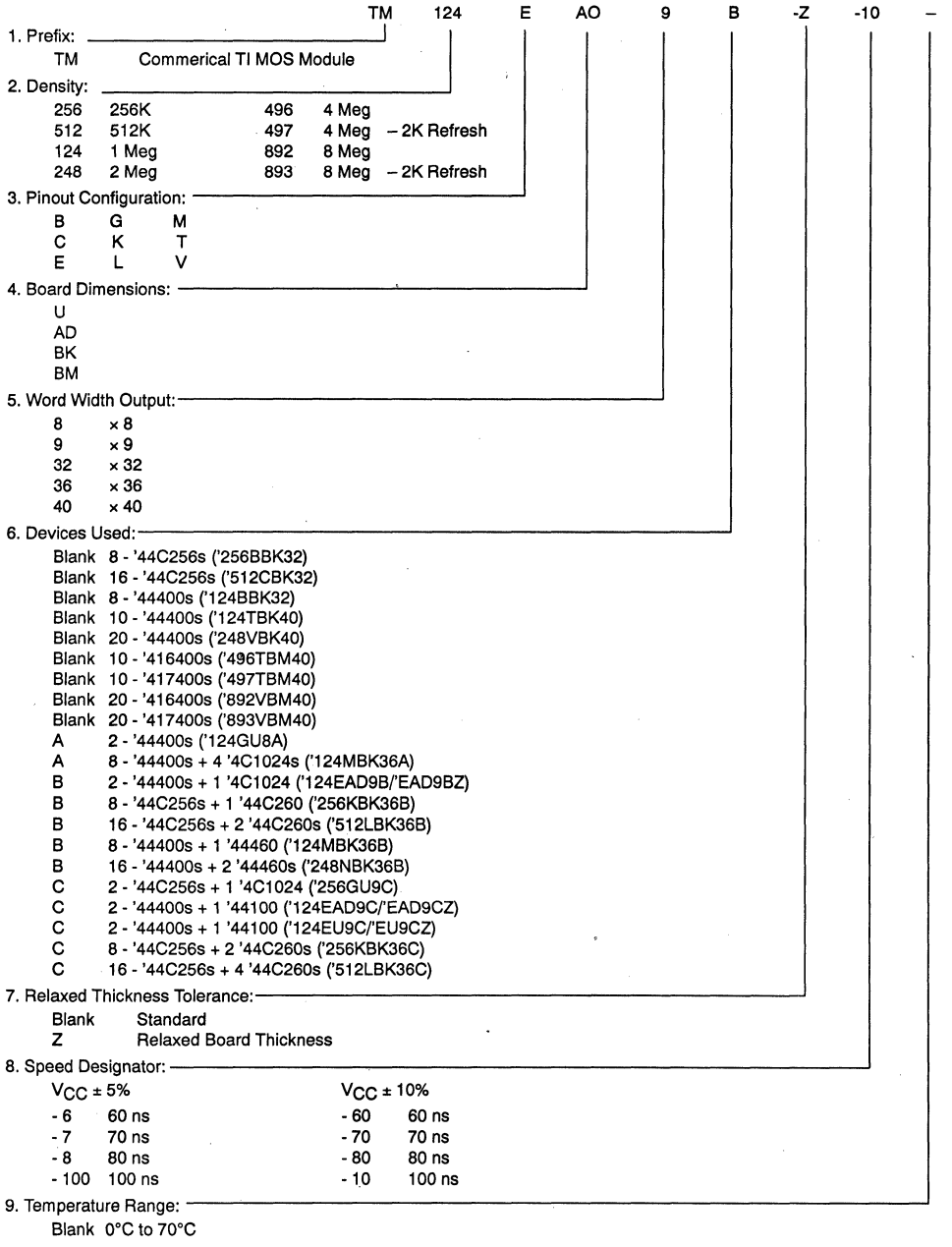
Standard DRAM Module Ordering Information

Factory orders for the standard DRAM Modules described in this book should include a seven-part type number as explained in the following example:



Differentiated DRAM Module Ordering Information

Factory orders for the mixed DRAM Modules described in this book should include an eight-part type number as explained in the following example:



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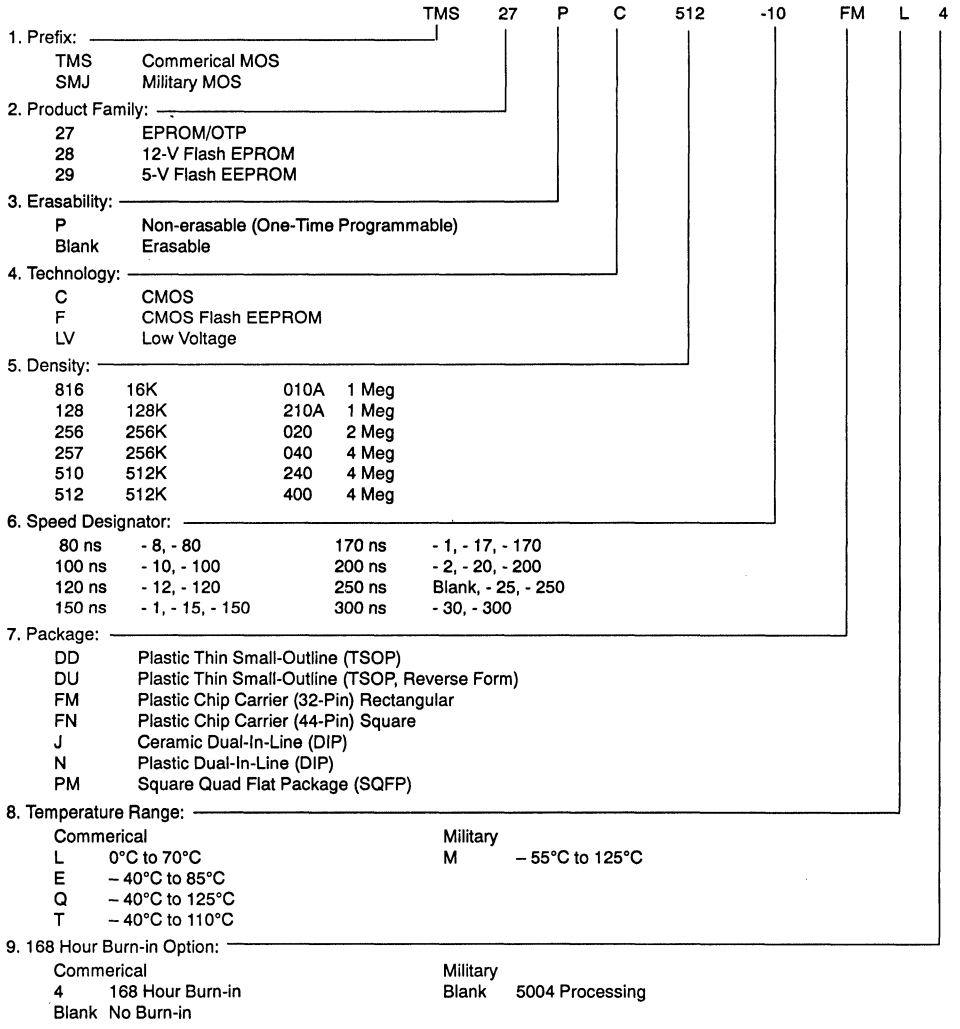
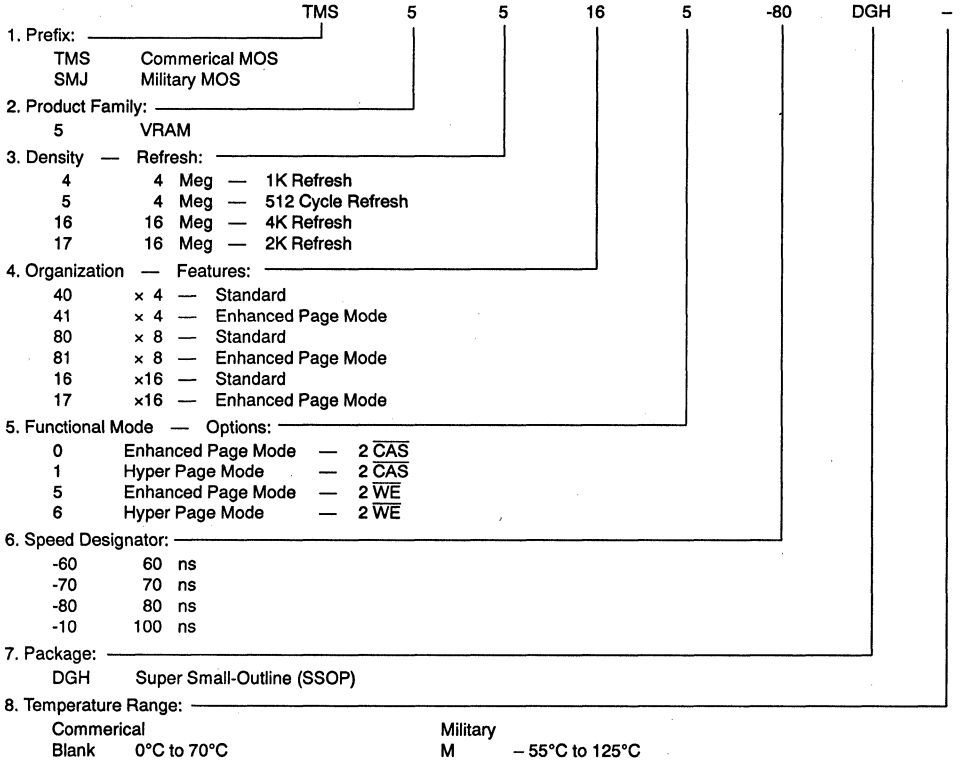
Nonvolatile Ordering Information

Factory orders for EPROMs, OTPs, and Flash Memories described in this book should include a nine-part type number as explained in the following example:



VRAM Ordering Information

Factory orders for 4 Meg VRAMs described in this book should include an eight-part type number as explained in the following example:



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Memory Card Ordering Information†

Factory orders for memory cards (excluding CMS401–CMS410 and CMS209–CMS216 OTP PROM memory cards) described in this book should include a nine-part type number as explained in the following example:

CMS 68 F 1 MB – – – N -250

1. Prefix:
   - CMS — Card Module Standard
   - CMP — Prototype Card Module
2. Number of Pins:
   - 60
   - 68
   - 88
3. Memory Type:
   - D — DRAM
   - F — Flash EPROM
   - P — OTP PROM
   - S — SRAM
4. Total Density:
   - 256 — 256K Byte
   - 512 — 512K Byte
   - 1 MB — 1 M Byte
   - 2 MB — 2 M Byte
   - 4 MB — 4 M Byte
   - 8 MB — 8 M Byte
5. Width:
   - Blank — User Selectable (x 8/x 16)
   - 8 — x 8
   - 9 — x 9
   - 16 — x16
   - 18 — x18
   - 32 — x32
   - 36 — x36
6. Power:
   - Blank — Standard
   - L — Low Power
   - S — Super-Low Power
7. Differentiator:
   - A, B, C, etc. — Alpha characters will be used when necessary to differentiate between similar card types.
8. Attribute Memory:
   - Blank — Attribute Memory
   - N — No Attribute Memory
9. Speed:
   - -70 — 70 ns
   - -80 — 80 ns
   - -200 — 200 ns
   - -250 — 250 ns

† This is the new memory card part numbering system. This system excludes existing DRAM memory cards CMS401–CMS410 and OTP PROM memory cards CMS209–CMS216.

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DRAM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
1024K	1024K × 1	SMJ4C1024-80 SMJ4C1024-10 SMJ4C1024-12 SMJ4C1024-15	80 100 120 150	5 ± 10%	413 385 330 303	17	18, 20, 26	FQ, HJ, HK, HL, JD, SV	Military CMOS Enhanced Page Mode	9-27
	256K × 4	SMJ44C256-80 SMJ44C256-10 SMJ44C256-12 SMJ44C256-15	80 100 120 150	5 ± 10%	440 385 330 303	17	20, 26	FQ, HJ, HK, HL, JD, SV	Military CMOS Enhanced Page Mode	9-5
4096K	4096K × 1	TMS44100-60 TMS44100-70 TMS44100-80	60 70 80	5 ± 10%	523 468 413	11	20, 26	DGA DGB, DJ, SD	CMOS Enhanced Page Mode	4-5
		TMS44100P-60 TMS44100P-70 TMS44100P-80	60 70 80	5 ± 10%	523 468 413	11	20, 26	DGA DGB, DJ, SD	CMOS Enhanced Page Mode Low Power	4-5
		SMJ44100-80 SMJ44100-10 SMJ44100-12	80 100 120	5 ± 10%	468 440 385	22	18, 20, 26	HM, HR, JD	Military CMOS Enhanced Page Mode	9-47
		TMS46100-70‡ TMS46100-80‡ TMS46100-10‡	70 80 100	3.3 ± 10%	216 180 144	3.6	20, 26	DGA, DGB, DJ, SD	CMOS Enhanced Page Mode Low Voltage	4-49
		TMS46100P-70‡ TMS46100P-80‡ TMS46100P-10‡	70 80 100	3.3 ± 10%	216 180 144	3.6	20, 26	DGA, DGB, DJ, SD	CMOS Enhanced Page Mode Low Voltage Extended Refresh	4-49
	1024K × 4	TMS46400-70‡ TMS46400-80‡ TMS46400-10‡	70 80 100	3.3 ± 10%	252 216 180	7.2	20, 26	DGA, DGB, DJ, SD	CMOS Enhanced Page Mode Low Voltage	4-71
		TMS46400P-70‡ TMS46400P-80‡ TMS46400P-10‡	70 80 100	3.3 ± 10%	252 216 180	7.2	20, 26	DGA, DGB, DJ, SD	CMOS Enhanced Page Mode Low Voltage Extended Refresh	4-71

† DGA Plastic Small-Outline-Package (SOP)
DGB Plastic Small-Outline Reverse Form Package (SOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DN Plastic Thin Small-Outline J-Lead (ThinSOJ)
FQ Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
HJ Leaded Ceramic Chip Carrier (Military)
HK Flatpack (Military)
HL Small-Outline Leadless Ceramic Chip Carrier (Military)
HM Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JD Ceramic Sidebrazed Dual In-Line Package (Military) (DIP)
N Plastic Dual In-Line Package (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)
SV Ceramic Zig-Zag-In-Line Package (Military)

‡ Advance Information for product under development by TI

DRAM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
4096K	512K × 8	TMS44800-60 TMS44800-70 TMS44800-80 TMS44800-10	60 70 80 100	5 ± 10%	660 605 550 495	11	28	DZ, DGC	CMOS Enhanced Page Mode	4-93
		TMS44800P-60 TMS44800P-70 TMS44800P-80 TMS44800P-10	60 70 80 100	5 ± 10%	660 605 550 495	11	28	DZ, DGC	CMOS Enhanced Page Mode Low Power	4-93
	256K × 16	TMS44165-70‡ TMS44165-80‡ TMS44165-10‡	70 80 100	5 ± 10%	660 578 523	11	40, 44	DZ, DGE	CMOS Enhanced Page Mode	4-115
		TMS44165P-70‡ TMS44165P-80‡ TMS44165P-10‡	70 80 100	5 ± 10%	660 578 523	11	40, 44	DZ, DGE	CMOS Enhanced Page Mode Low Power	4-115
		TMS45160-70 TMS45160-80 TMS45160-10	70 80 100	5 ± 10%	880 770 660	11	40, 44	DZ, DGE	CMOS Enhanced Page Mode	4-137
		TMS45160P-70 TMS45160P-80 TMS45160P-10	70 80 100	5 ± 10%	880 770 660	11	40, 44	DZ, DGE	CMOS Enhanced Page Mode Low Power	4-137
		TMS45165-70‡ TMS45165-80‡ TMS45165-10‡	70 80 100	5 ± 10%	880 770 660	11	40, 44	DZ, DGE	CMOS Enhanced Page Mode	4-159
		TMS45165P-70‡ TMS45165P-80‡ TMS45165P-10‡	70 80 100	5 ± 10%	880 770 660	11	40, 44	DZ, DGE	CMOS Enhanced Page Mode Low Power	4-159
	1024K × 4	TMS44400-60 TMS44400-70 TMS44400-80	60 70 80	5 ± 10%	550 495 440	11	20, 26, 20, 26, 20	DJ, DGA, DGB, SD	CMOS Enhanced Page Mode	4-27
		TMS44400P-60 TMS44400P-70 TMS44400P-80	60 70 80	5 ± 10%	550 495 440	11	20, 26, 20, 26, 20	DJ, DGA, DGB, SD	CMOS Enhanced Page Mode Low Power	4-27
		SMJ44400-80 SMJ44400-10 SMJ44400-12	80 100 120	5 ± 10%	468 440 358	22	20, 20, 20, 20	JD, HM, HR	Military CMOS Enhanced Page Mode	9-67
16 384K	16 384K × 1 and 16 384K × 4	Product Preview: TMS416100, TMS416400, and TMS417400	60 70 80	5 ± 10%	440 385 330	–	24, 26	DJ, DGA, DGB	CMOS Enhanced Page Mode	4-249

† DGA Plastic Small-Outline-Package (SOP)
DGB Plastic Small-Outline Reverse Form Package (SOP)
DGC Plastic Thin Small-Outline Package
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
HM Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JD Ceramic Sidebrazed Dual In-Line Package (Military) (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)

‡ Advance Information for product under development by TI

DRAM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	ACTIVE (mW)	STANDBY (mW)	PINS	PACKAGE†	NOTES	PAGE
16 384K	16 384K × 1	TMS416100-60	60	5 ± 10%	495	11	24, 28	DGC, DGD, DZ	CMOS Enhanced Page Mode	4-385
		TMS416100-70	70		440					
		TMS416100-80	80		385					
		SMJ416100-60	60	5 ± 10%	495	11	24, 28	FNC, HKB	Military Enhanced Page Mode	9-87
		SMJ416100-70	70		440					
		SMJ416100-80	80		385					
		SMJ416100-10	100		330					
		SMJ417100-60	60	5 ± 10%	605	11	24, 28	FNC, HKB	Military Enhanced Page Mode	9-125
		SMJ417100-70	70		550					
		SMJ417100-80	80		495					
		SMJ417100-10	100		440					
	4096K × 4	TMS416400-60	60	5 ± 10%	495	11	24, 28	DGC, DGD, DZ	CMOS Enhanced Page Mode	4-203
		TMS416400-70	70		440					
		TMS416400-80	80		385					
		SMJ416400-60	60	5 ± 10%	495	11	24, 28	FNC, HKB	Military Enhanced Page Mode	9-105
		SMJ416400-70	70		440					
		SMJ416400-80	80		385					
		SMJ416400-10	100		330					
		TMS417400-60	60	5 ± 10%	495	11	24, 28	DGC, DGD, DZ	CMOS Enhanced Page Mode	4-227
		TMS417400-70	70		440					
		TMS417400-80	80		385					
		SMJ417400-60	60	5 ± 10%	605	11	24, 28	FNC, HKB	Military Enhanced Page Mode	9-143
		SMJ417400-70	70		550					
		SMJ417400-80	80		495					
		SMJ417400-10	100		440					
		TMS426400-60§	60	3.3 ± 10%	252	3.6	24, 26	DGA, DGB, DJ	CMOS Enhanced Page Mode Low Voltage	4-409
		TMS426400-70§	70		216					
		TMS426400-80§	80		180					
		TMS426400-10§	100		144					
		TMS426400P-60§	60	3.3 ± 10%	252	3.6	24, 26	DGA, DGB, DJ	CMOS Enhanced Page Mode Low Voltage Low Power	4-409
		TMS426400P-70§	70		216					
		TMS426400P-80§	80		180					
		TMS426400P-10§	100		144					
		TMS427400-60§	60	3.3 ± 10%	252	3.6	24, 26	DGA, DGB, DJ	CMOS Enhanced Page Mode Low Voltage	4-433
		TMS427400-70§	70		216					
		TMS427400-80§	80		180					
		TMS427400-10§	100		144					

† DGA Plastic Small-Outline-Package (SOP)
DGB Plastic Small-Outline Reverse Form Package (SOP)
DGC Plastic Thin Small–Outline Package (TSOP)
DGD Plastic Thin Small-Outline Reverse Form Package (TSOP)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
FNC Small-Outline Leadless Chip Carrier (Military) (SOLCC)
HKB Flatpack (Military)
HJ Ceramic Small-Outline Leadless J-Lead (Military) (SOLCC)
HM Small-Outline Leadless Ceramic Chip Carrier (Military) (SOLCC)
HR Flatpack (Military)
JD Ceramic Sidebrazed Dual In-Line Package (Military) (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)

‡ Advance Information for product under development by TI

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DRAM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
16 384K	4096K × 4	TMS427400P-60§ TMS427400P-70§ TMS427400P-80§ TMS427400P-10§	60 70 80 100	3.3 ± 10%	252 216 180 144	3.6	24, 26	DGA, DGB, DJ	CMOS Enhanced Page Mode Low Voltage Low Power	4-433
		TMS416800-60‡ TMS416800-70‡ TMS416800-80‡	60 70 80	5 ± 10%	495 440 385	11	28, 32	DE, DZ	CMOS Enhanced Page Mode	4-341
		TMS416800P-60‡ TMS416800P-70‡ TMS416800P-80‡	60 70 80	5 ± 10%	495 440 385	11	28, 32	DE, DZ	CMOS Enhanced Page Mode Low Power	4-341
	2048K × 8	TMS417800-60‡ TMS417800-70‡ TMS417800-80‡	60 70 80	5 ± 10%	688 633 578	11	28, 32	DE, DZ	CMOS Enhanced Page Mode	4-363
		TMS417800P-60‡ TMS417800P-70‡ TMS417800P-80‡	60 70 80	5 ± 10%	688 633 578	11	28, 32	DE, DZ	CMOS Enhanced Page Mode Low Power	4-363
		TMS426800-70‡ TMS426800-80‡	70 80	3.3 ± 10%	288 252	3.6	28, 32	DE, DZ	CMOS Enhanced Page Mode Low Voltage	4-457
		TMS426800P-70‡ TMS426800P-80‡	70 80	3.3 ± 10%	288 252	3.6	28, 32	DE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-457
		TMS427800-70‡ TMS427800-80‡	70 80	3.3 ± 10%	414 378	3.6	28, 32	DE, DZ	CMOS Enhanced Page Mode Low Voltage	4-479
		TMS427800P-70‡ TMS417800P-80‡	70 80	3.3 ± 10%	414 378	3.6	28, 32	DE, DZ	CMOS Enhanced Page Mode Low Voltage Low Power	4-479
	1024K × 16	TMS416160-60‡ TMS416160-70‡ TMS416160-80‡	60 70 80	5 ± 10%	495 440 385	11	42, 44, 50	DC, RE	CMOS Enhanced Page Mode	4-253
		TMS416160P-60‡ TMS416160P-70‡ TMS416160P-80‡	60 70 80	5 ± 10%	495 440 385	11	42, 44, 50	DC, RE	CMOS Enhanced Page Mode Low Power	4-253

† DGA Plastic Small-Outline-Package (SOP)
DGB Plastic Small-Outline Reverse Form Package (SOP)
DC Plastic Surface Mount Thin Small-Outline Package (TSOP)
DE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
DZ Plastic Small-Outline J-Lead (SOJ)
RE Plastic Surface Mount Small-Outline J-Lead Package (SOJ)

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DRAM (concluded)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
16 384K	1024K × 16	TMS418160-60‡ TMS418160-70‡ TMS418160-80‡	60 70 80	5 ± 10%	990 880 770	11	42, 44, 50	DC, RE	CMOS Enhanced Page Mode	4-297
		TMS418160P-60‡ TMS418160P-70‡ TMS418160P-80‡	60 70 80	5 ± 10%	990 880 770	11	42, 44, 50	DC, RE	CMOS Enhanced Page Mode Low Power	4-297
		TMS426160-70‡ TMS426160-80‡	70 80	3.3 ± 10%	288 252	3.6	42, 44, 50	DC, RE	CMOS Enhanced Page Mode Low Voltage	4-275
		TMS426160P-70‡ TMS426160P-80‡	70 80	3.3 ± 10%	288 252	3.6	42, 44, 50	DC, RE	CMOS Enhanced Page Mode Low Voltage Low Power	4-275
		TMS428160-70‡ TMS428160-80‡	70 80	3.3 ± 10%	TBD	3.6	42, 44, 50	DC, RE	CMOS Enhanced Page Mode Low Voltage	4-319
		TMS428160P-70‡ TMS428160P-80‡	70 80	3.3 ± 10%	TBD	3.6	42, 44, 50	DC, RE	CMOS Enhanced Page Mode Low Voltage Low Power	4-319
		TMS426100-60‡ TMS426100-70‡ TMS426100-80‡ TMS426100-10‡	60 70 80 100	3.3 ± 10%	252 216 180 144	3.6	24, 26	DGA, DGB, DJ	CMOS Enhanced Page Mode Low Voltage	4-385
	16K × 1	TMS426100P-60‡ TMS426100P-70‡ TMS426100P-80‡ TMS426100P-10‡	60 70 80 100	3.3 ± 10%	252 216 180 144	3.6	24, 26	DGA, DGB, DJ	CMOS Enhanced Page Mode Low Voltage Low Power	4-385
16 385K	1M Byte × 2	SDRAM-6§ SDRAM-8§ SDRAM-10§	N/A	3.3 ± 10%	TBD	TBD	44	DGE	Synchronous DRAM	4-501

† Advance Information for product under development by TI

† DC Plastic Surface Mount Thin Small-Outline Package (TSOP)
DGA Plastic Small-Outline-Package (SOP)
DGB Plastic Small-Outline Reverse Form Package (SOP)
DGE Plastic Surface Mount Thin Small-Outline Package (TSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
RE Plastic Surface Mount Small-Outline J-Lead Package (SOJ)

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DRAM Module

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE	PAGE
					ACTIVE (mW)	STANDBY (mW)			
9216K	1024K × 9	TM124EU9B-6	60	5 ± 5%	1496	32	30	Single-Sided Socketable	5-5
		TM124EU9B-70	70	5 ± 10%	1403	33			
		TM124EU9B-80	80	5 ± 10%	1238	33			
		TM124EU9B-10	100	5 ± 10%	1073	33			
		TM124EU9C-6	60	5 ± 5%	1496	32	30	Single-Sided Socketable	5-5
		TM124EU9C-70	70	5 ± 10%	1403	33			
		TM124EU9C-80	80	5 ± 10%	1238	33			
		TM124EU9C-10	100	5 ± 10%	1073	33			
32 768K	4096K × 9	TM497EAD9B-60†	60	5 ± 10%	1843	17	30	Single-Sided Socketable	5-13
		TM497EAD9B-70†	70		1678				
		TM497EAD9B-80†	80		1513				
		TM497EAD9B-10†	100		1348				
	4096K × 8	TM497GAD8A-60†	60	5 ± 10%	1320	22	30	Single-Sided Socketable	5-83
		TM497GAD8A-70†	70		1210				
		TM497GAD8A-80†	80		1100				
		TM497GAD8A-10†	100		990				
		TM4100GAD8-60	60	5 ± 10%	3990	88	30	Single-Sided Socketable	5-75
		TM4100GAD8-70	70		3740				
		TM4100GAD8-80	80		3300				
	1024K × 32	TM124BBK32-60	60	5 ± 10%	4620	88	72	Single-Sided, Socketable	5-29
		TM124BBK32-70	70		3960				
		TM124BBK32-80	80		3520				
		TM124BBK32S-60	60	5 ± 10%	4620	88	72	Single-Sided Socketable Solder-Tabbed	5-29
		TM124BBK32S-70	70		3960				
		TM124BBK32S-80	80		3520				
36 864K	4096K × 9	TM4100EAD9-60	60	5 ± 10%	5198	99	30	Single-Sided Socketable	5-67
		TM4100EAD9-70	70		4455				
		TM4100EAD9-80	80		3960				
	1024K × 36	TM124MBK36-6	60	5 ± 5%	6405	126	72	Double-Sided Socketable	5-39
		TM124MBK36-70	70	5 ± 10%	5720	132			
		TM124MBK36-80	80	5 ± 10%	5170	132			
		TM124MBK36Q-6	60	5 ± 5%	6405	126	72	Double-Sided Socketable Solder-Tabbed	5-39
		TM124MBK36Q-70	70	5 ± 10%	5720	132			
		TM124MBK36Q-80	80	5 ± 10%	5170	132			
		TM124MBK36B-60†	60	5 ± 10%	5198	99	72	Single-Sided Socketable Gold-Tabbed	5-47
		TM124MBK36B-70†	70		4455				
		TM124MBK36B-80†	80		3960				
		TM124MBK36R-60†	60	5 ± 10%	5198	99	72	Single-Sided Socketable Solder-Tabbed	5-47
		TM124MBK36R-70†	70		4455				
		TM124MBK36R-80†	80		3960				
		TM124MBK36C-60	60	5 ± 10%	5775	110	72	Single-Sided Socketable Gold-Tabbed	5-57
		TM124MBK36C-70	70		4950				
		TM124MBK36C-80	80		4400				
		TM124MBK36S-60	60	5 ± 10%	5775	110	72	Single-Sided Socketable Solder-Tabbed	5-57
		TM124MBK36S-70	70		4950				
		TM124MBK36S-80	80		4400				
40 960K	1024K × 40	TM124TBK40-60†	60	5 ± 10%	5225	220	72	Single-Sided Socketable	5-137
		TM124TBK40-70†	70		4675				
		TM124TBK40-80†	80		4125				

† Advance Information for product under development by TI

DRAM Module

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE	PAGE
					ACTIVE (mW)	STANDBY (mW)			
65 536K	2048K × 32	TM248CBK32-60 TM248CBK32-70 TM248CBK32-80	60 70 80	5 ± 10%	4708 4048 3608	176	72	Double-Sided Socketable Gold-Tabbed	5-29
		TM248CBK32S-60 TM248CBK32S-70 TM248CBK32S-80	60 70 80	5 ± 10%	4708 4048 3608	176	72	Double-Sided Socketable Solder-Tabbed	5-29
73 728K	2048K × 36	TM248NBK36B-60† TM248NBK36B-70† TM248NBK36B-80†	60 70 80	5 ± 10%	5297 4554 4059	198	72	Double-Sided Socketable Gold-Tabbed	5-47
		TM248NBK36R-60† TM248NBK36R-70† TM248NBK36R-80†	60 70 80	5 ± 10%	5297 4554 4059	198	72	Double-Sided Socketable Solder-Tabbed	5-47
		TM248NBK36C-60 TM248NBK36C-70 TM248NBK36C-80	60 70 80	5 ± 10%	5885 5060 4510	220	72	Double-Sided Socketable Gold-Tabbed	5-57
		TM248NBK36S-60 TM248NBK36S-70 TM248NBK36S-80	60 70 80	5 ± 10%	5885 5060 4510	220	72	Double-Sided Socketable Solder-Tabbed	5-57
81 920K	2048K × 40	TM248VBK40-60† TM248VBK40-70† TM248VBK40-80†	60 70 80	5 ± 10%	5335 4785 4235	220	72	Double-Sided Socketable	5-137
131 072K	4096K × 32	TM497BBK32-60† TM497BBK32-70† TM497BBK32-80†	60 70 80	5 ± 10%	5280 4840 4400	88	72	Double-Sided Socketable	5-105
	16 384K × 8	TM16100GBD8-60† TM16100GBD8-70† TM16100GBD8-80† TM16100GBD8-10†	60 70 80 100	5 ± 10%	3960 3520 3080 2640	88	30	Double-Sided Socketable	5-91
147 456K	16 384K × 9	TM16100EBD9-60† TM16100EBD9-70† TM16100EBD9-80† TM16100EBD9-10†	60 70 80 100	5 ± 10%	4455 3960 3465 2970	99	30	Double-Sided Socketable	5-99
	4096K × 36	TM497MBK36A-60† TM497MBK36A-70† TM497MBK36A-80†	60 70 80	5 ± 10%	8140 6820 6160	132	72	Double-Sided Socketable	5-21
		TM497MBK36Q-60† TM497MBK36Q-70† TM497MBK36Q-80†	60 70 80	5 ± 10%	8140 6820 6160	132	72	Double-Sided Socketable Solder-Tabbed	5-21
163 840K	4096K × 40	TM496TBM40-60† TM496TBM40-70† TM496TBM40-80†	60 70 80	5 ± 10%	4950 4400 3850	110	72	Double-Sided Socketable Gold-Tabbed	5-125
		TM496TBM40S-60† TM496TBM40S-70† TM496TBM40S-80†	60 70 80	5 ± 10%	4950 4400 3850	110	72	Double-Sided Socketable Solder-Tabbed	5-125
		TM497TBM40-60† TM497TBM40-70† TM497TBM40-80†	60 70 80	5 ± 10%	6600 6050 5500	110	72	Double-Sided Socketable Gold-Tabbed	5-115
		TM497TBM40S-60† TM497TBM40S-70† TM497TBM40S-80†	60 70 80	5 ± 10%	6600 6050 5500	110	72	Double-Sided Socketable Solder-Tabbed	5-115

† Advance Information for product under development by TI

DRAM Module (concluded)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE	PAGE
					ACTIVE (mW)	STANDBY (mW)			
262 144K	8192K × 32	TM893CBK32-60†	60	5 ± 10%	5368	176	72	Double-Sided Socketable	5-105
		TM893CBK32-70†	70		4928				
		TM893CBK32-80†	80		4488				
327 680K	8192K × 40	TM892VBM40-60†	60	5 ± 10%	5060	220	72	Double-Sided Socketable Gold-Tabbed	5-125
		TM892VBM40-70†	70		4510				
		TM892VBM40-80†	80		3960				
		TM892VBM40S-60†	60	5 ± 10%	6710	220	72	Double-Sided Socketable Solder-Tabbed	5-125
		TM892VBM40S-70†	70		6160				
		TM892VBM40S-80†	80		5610				
		TM893VBM40-60†	60	5 ± 10%	5060	220	72	Double-Sided Socketable Gold-Tabbed	5-115
		TM893VBM40-70†	70		4510				
		TM893VBM40-80†	80		3960				
		TM893VBM40S-60†	60	5 ± 10%	5060	220	72	Double-Sided Socketable Solder-Tabbed	5-115
		TM893VBM40S-70†	70		4510				
		TM893VBM40S-80†	80		3960				

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EPROM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
128K	16K × 8	TMS27C128-12	120	5 ± 10%	165	1.4	28	J	CMOS	6-2
		TMS27C128-15	150							
		TMS27C128-20	200							
		TMS27C128-25	250							
		SMJ27C128-12	120	5 ± 5%	131	1.6	28	J	Military CMOS	9-81
		SMJ27C128-15	150	5 ± 10%	220	1.7				
		SMJ27C128-17	170	5 ± 10%	220	1.7				
		SMJ27C128-20	200	5 ± 10%	220	1.7				
		SMJ27C128-25	250	5 ± 10%	220	1.7				
		SMJ27C128-30	300	5 ± 10%	220	1.7				
256K	32K × 8	TMS27C256-10	100	5 ± 10%	165	1.4	28	J	CMOS	6-3
		TMS27C256-12	120							
		TMS27C256-15	150							
		TMS27C256-17	170							
		TMS27C256-20	200							
		TMS27C256-25	250							
		SMJ27C256-15	150	5 ± 10%	220	1.7	28	J	Military CMOS	9-253
		SMJ27C256-17	170							
		SMJ27C256-20	200							
		SMJ27C256-25	250							
		SMJ27C256-30	300							
512K	64K × 8	TMS27C510-12	120	5 ± 10%	165	1.4	32	J	CMOS	6-15
		TMS27C510-15	150							
		TMS27C510-17	170							
		TMS27C510-20	200							
		TMS27C510-25	250							
		TMS27C512-10	100	5 ± 10%	165	1.4	28	J	CMOS	6-27
		TMS27C512-12	120							
		TMS27C512-15	150							
		TMS27C512-20	200							
		TMS27C512-25	250							
		SMJ27C512-20	200	5 ± 10%	263	1.8	28	J	Military CMOS	9-263
		SMJ27C512-25	250							
		SMJ27C512-30	300							
1024K	128K × 8	TMS27C010A-10	100	5 ± 10%	165	0.55	32	J	CMOS	6-39
		TMS27C010A-12	120							
		TMS27C010A-15	150							
		TMS27C010A-20	200							
		TMS27LV010A-20‡	200	3.3 ± 10%	54	.09	32	J	CMOS Low Voltage	6-203
		TMS27LV010A-25‡	250							
		TMS27LV010A-30‡	300							
	64K × 16	TMS27C210A-10	100	5 ± 10%	165	0.55	40	J	CMOS	6-51
		TMS27C210A-12	120							
		TMS27C210A-15	150							
		TMS27C210A-20	200							
		TMS27C210A-25	250							
2048K	256K × 8	TMS27C020-12	120	5 ± 10%	165	0.55	32	FM, J	CMOS	6-61
		TMS27C020-15	150							
		TMS27C020-20	200							
		TMS27C020-25	250							

† FM Plastic Leaded Chip Carrier
J Ceramic Dual In-Line Package (DIP)

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EPROM (concluded)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
4096K	512K × 8	TMS27C040-10 TMS27C040-12 TMS27C040-15	100 120 150	5 ± 10%	275	0.55	32	J	CMOS	6-71
		SMJ27C040-10 SMJ27C040-12 SMJ27C040-15	100 120 150	5 ± 10%	330	0.55	32	J	Military CMOS	9-275
	256K × 16	TMS27C240-10 TMS27C240-12 TMS27C240-15	100 120 150	5 ± 10%	275	0.55	40	J	CMOS	6-81
		TMS27C400-10‡ TMS27C400-12‡ TMS27C400-15‡	100 120 150	5 ± 10%	275	0.55	40	J	CMOS	6-91

† J Ceramic Dual In-Line Package (DIP)
‡ Advance Information for product under development by TI

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Flash EEPROM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
16K	2K × 8	TMS29F816-06	N/A	5 ± 10%	110	N/A	18	FM	CMOS 5-V Flash Serial JTAG Bus	6-101
		SMJ29F816-06‡	N/A	5 ± 10%	110	N/A	18	FM	CMOS 5-V Flash Serial JTAG Bus	9-285
512K	64K × 8	TMS28F512-10‡ TMS28F512-12‡ TMS28F512-15‡ TMS28F512-17‡	100 120 150 170	5 ± 10%	165	.55	32	DD, DU, FM, N	CMOS Flash EEPROM	6-145
1024K	128K × 8	TMS28F010-10‡ TMS28F010-12‡ TMS28F010-15‡ TMS28F010-17‡	100 120 150 170	5 ± 10%	165	.55	32	DD, DU, FM, N	CMOS Flash EEPROM	6-145
	64K × 16	TMS28F210-10§ TMS28F210-12§ TMS28F210-15§ TMS28F210-17§	100 120 150 170	5 ± 10%	275	.55	40, 44	FN, J	CMOS Flash EEPROM	6-165
4096K	512K × 8	TMS28F040-80‡	80	5 ± 10%	165	0.55	32, 40	DD, DU, N	CMOS Flash EEPROM	6-185

† DD Plastic Thin Small-Outline Package
DU Plastic Thin Small-Outline Reverse Form Package
FM Plastic Leaded Chip Carrier
FN Plastic Leaded Chip Carrier
J Ceramic Dual In-Line Package (DIP)
N Plastic Dual In-Line Package (DIP)

‡ Advance Information for product under development by TI

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One-Time Programmable (OTP) PROM

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
128K	16K × 8	TMS27PC128-15 TMS27PC128-20 TMS27PC128-25	150 200 250	5 ± 10%	165	1.4	28, 32	FM, N	CMOS	6-2
256K	32K × 8	TMS27PC256-10 TMS27PC256-15 TMS27PC256-17 TMS27PC256-20 TMS27PC256-25	100 150 170 200 250	5 ± 10%	165	1.4	28, 32	FM, N	CMOS	6-3
512K	64K × 8	TMS27PC510-15 TMS27PC510-17 TMS27PC510-20 TMS27PC510-25	150 170 200 250	5 ± 10%	165	1.4	32	FM, N	CMOS	6-15
		TMS27PC512-10 TMS27PC512-12 TMS27PC512-15 TMS27PC512-20 TMS27PC512-25	100 120 150 200 250	5 ± 10%	165	1.4	28, 32	DD, DU, FM, N	CMOS	6-27
1024K	128K × 8	TMS27PC010A-12 TMS27PC010A-15 TMS27PC010A-20	120 150 200	5 ± 10%	165	0.55	32	DD, DU, FM, N	CMOS	6-39
		TMS27LV010A-20‡ TMS27LV010A-25‡ TMS27LV010A-30‡	200 250 300	3.3 ± 10%	54	0.09	32	FM	CMOS Low Voltage	6-203
	64K × 16	TMS27PC210A-12 TMS27PC210A-15 TMS27PC210A-20 TMS27PC210A-25	120 150 200 250	5 ± 10%	165	0.55	44	FN	CMOS	6-51
2048K	256K × 8	TMS27PC020-12 TMS27PC020-15 TMS27PC020-20 TMS27PC020-25	120 150 200 250	5 ± 10%	165	0.55	32	FM	CMOS	6-61
4096K	512K × 8	TMS27PC040-10 TMS27PC040-12 TMS27PC040-15	100 120 150	5 ± 10%	275	0.55	32	FM	CMOS	6-71
	256K × 16	TMS27PC240-10 TMS27PC240-12 TMS27PC240-15	100 120 150	5 ± 10%	275	0.55	44	FN	CMOS	6-81
		TMS27PC400-10‡ TMS27PC400-12‡ TMS27PC400-15‡	100 120 150	5 ± 10%	275	0.55	44	N	CMOS	6-91

† DD Plastic Thin Small-Outline Package
DU Plastic Thin Small-Outline Reverse Form Package
FM Plastic Leaded Chip Carrier
FN Plastic Leaded Chip Carrier
N Plastic Dual In-Line Package (DIP)
‡ Advance Information for product under development by TI

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Video RAMs/Field Memories

DENSITY	ORGANIZATION (WORDS x BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	PACKAGE†	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)				
1024K	256K x 4	SMJ44C250-10 SMJ44C250-12	100 120	5 ± 10%	635 550	90 83	28	HJ, JD	Military CMOS Multiport Video RAM	9-161
		SMJ44C251-10 SMJ44C251-12	100 120	5 ± 10%	550 495	83	28	HJ, JD	Military CMOS Multiport Video RAM	9-199
		TMS4C1050B-30 TMS4C1050B-40 TMS4C1050B-60	30 40 60	5 ± 10%	275 248 193	55	16, 20, 26	DJ, N, SD	CMOS Field Memory	7-109
		TMS4C1060B-30 TMS4C1060B-40 TMS4C1060B-60	30 40 60	5 ± 10%	275 248 193	55	16, 20, 26	DJ, N, SD	CMOS Field Memory	7-121
		TMS4C1070B-30‡ TMS4C1070B-40‡ TMS4C1070B-60‡	30 40 60	5 ± 10%	275 248 193	55	18	N	CMOS Field Memory	7-133
4096K	256K x 16	TMS55160-70 TMS55160-80	70 80	5 ± 10%	908 880	28	64	DGH	CMOS Multiport Video RAM	7-3
		TMS55165-70 TMS55165-80	70 80	5 ± 10%	908 880	28	64	DGH	CMOS Multiport Video RAM	7-57

† DGH Plastic Super Small-Outline Package (SSOP)
DJ Plastic Small-Outline J-Lead (SOJ)
HJ Ceramic Small-Outline J-Lead (Military) (SOJ)
JD Ceramic Sidebrazed Dual In-Line Package (Military) (DIP)
N Plastic Dual In-Line (DIP)
SD Plastic Zig-Zag In-Line Package (ZIP)
‡ Advance Information for product under development by TI

Memory Card

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)			
256K	256K × 8 or 128K × 16	CMS68F256-250†	250	5 ± 5%	420	131	68	PCMCIA Standard Flash EEPROM Memory Card	8-45
	256K × 8 or 128K × 16	CMS68P256-200	200	5 ± 5%	1050	52.5	68	PCMCIA Standard OTP PROM Memory Card Includes Attribute Memory	8-35
	256K × 8 or 128K × 16	CMS68P256N-200	200	5 ± 5%	1050	52.5	68	PCMCIA Standard OTP PROM Memory Card	8-35
512K	512K × 8 or 256K × 16	CMS68F512-250†	250	5 ± 5%	420	131	68	PCMCIA Standard Flash EEPROM Memory Card	8-45
	512K × 8 or 256K × 16	CMS68P512-200‡	200	5 ± 5%	1050	52.5	68	PCMCIA Standard OTP PROM Memory Card Includes Attribute Memory	8-35
	512K × 8 or 256K × 16	CMS68P512N-200	200	5 ± 5%	1050	52.5	68	PCMCIA Standard OTP PROM Memory Card	8-35
	64K × 8	CMS213-200 CMS213-250	200 250	5 ± 5%	263	21	60	OTP PROM Memory Card	8-65
1024K	1024K × 8 or 512K × 16	CMS68F1MB-250†	250	5 ± 5%	420	131	68	PCMCIA Standard Flash EEPROM Memory Card	8-45
	1024K × 8 or 512K × 16	CMS68P1MB-200	200	5 ± 5%	1050	52.5	68	PCMCIA Standard OTP PROM Memory Card Includes Attribute Memory	8-35
	1024K × 8 or 512K × 16	CMS68P1MBN-200	200	5 ± 5%	1050	52.5	68	PCMCIA Standard OTP PROM Memory Card	8-35
	64K × 16	CMS209-200 CMS209-250	200 250	5 ± 5%	525	42	60	OTP PROM Memory Card	8-65
	128K × 8	CMS214-200 CMS214-250	200 250	5 ± 5%	263	42	60	OTP PROM Memory Card	8-65

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Memory Card (concluded)

DENSITY	ORGANIZATION (WORDS × BITS)	DEVICE NUMBER	MAX ACCESS TIME (ns)	POWER SUPPLY (V)	MAX POWER DISSIPATION		PINS	NOTES	PAGE
					ACTIVE (mW)	STANDBY (mW)			
2048K	2048K × 8 or 1024K × 16	CMS68F2MB-250‡	250	5 ± 5%	420	131	68	PCMCIA Standard Flash EEPROM Memory Card	8-45
	1024K × 18	CMS407-7 CMS407-8	70 80	5 ± 5%	3098 2783	68	60	DRAM Memory Card	8-3
	1024K × 16	CMS408-7 CMS408-8	70 80	5 ± 5%	2153 1943	47	60	DRAM Memory Card	8-3
	128K × 16	CMS210-200 CMS210-250	200 250	5 ± 5%	525	84	60	OTP PROM Memory Card	8-65
	256K × 8	CMS216-200 CMS216-250	200 250	5 ± 5%	263	84	60	OTP PROM Memory Card	8-65
4096K	2048K × 18	CMS405-7 CMS405-8	70 80	5 ± 5%	3161 2846	131	60	DRAM Memory Card	8-3
	2048K × 16	CMS406-7 CMS406-8	70 80	5 ± 5%	2195 1985	89	60	DRAM Memory Card	8-3
8192K	1024K × 36	CMS88D4MB36-7† CMS88D4MB36-8†	70 80	5 ± 5%	4988 4463	58	88	DRAM Memory Card	8-27
	4096K × 18	CMS409-7 CMS409-8	70 80	5 ± 5%	8768 7823	194	60	DRAM Memory Card	8-17
	4096K × 16	CMS410-7 CMS410-8	70 80	5 ± 5%	7823 6983	173	60	DRAM Memory Card	8-17
	2048K × 36	CMS88D8MB36-7† CMS88D8MB36-8†	70 80	5 ± 5%	5045 4520	110	88	DRAM Memory Card	8-27

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GENERAL CONCEPTS AND TYPES OF MEMORIES

Address – Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down – see Chip Enable Input.

Bit – Contraction of *Binary digit* i.e., a 1 or a 0. In electrical terms, the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte – A word of 8 bits (see Word).

C of C – Certification of Conformance.

CDIP – Ceramic Dual In-Line Package.

CERPAC – CERamic flat PACk (hermetic).

CMOS – A complementary MOS technology that uses transistors with electron (N-channel) and hole (P-channel) conduction.

Chip Enable Input – A control input to an integrated circuit that, when active, permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and, when inactive, causes the integrated circuit to be in a reduced-power standby mode.

Chip Select Input – Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous – Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous – Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe ($\overline{\text{CAS}}$) – A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

Data – Any information stored or retrieved from a memory device.

Die – Unpackaged semiconductor.

DIP – Dual In-line Package.

DESC – Defense Electronics Supply Center.

Dynamic (Read/Write) Memory (DRAM) – A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:

1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Erasable Programmable Read-Only Memory (EEPROM) – A nonvolatile memory that can be field-programmed like an OTP PROM or EPROM but that can be electrically erased by a combination of electrical signals at its inputs.

EPIC – Enhanced Performance Implanted CMOS.

Erasable and Programmable Read-Only Memory (EPROM) – A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase – Typically associated with EPROMs and EEPROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

ESD – Electrostatic Discharge.

Field Memory (FMEM) – A serial-access memory that performs high-speed, asynchronous read/write operations. (Used mainly for fields of digital TV/VTR that require higher speed operation, lower power consumption, and larger capacity.)

Field-Programmable Read-Only Memory – See One-Time Programmable Read-Only Memory.

FIFO – First-In, First-Out.

Fit – Originally stood for Failures-In-Time. Currently means a failure rate of one failure in one billion hours.

Fixed Memory – A common term for ROMs, EPROMs, EEPROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EEPROMs is nonvolatile since their data may be easily changed.

Flash EEPROM –

FRAM – First-in first-out pseudo-static RAM or Field RAM.

Fully Static RAM – In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need of clocks. There is no precharge required for static periphery.

GENERIC DATA – Group A, B, C, & D Quality Conformance Data.

JAN – Joint Army Navy. Specifically, a JM38510 qualified device.

JANB – Class B screened JAN device.

JANS – Class S screened JAN device.

JEDEC – Joint Electronic Device Engineering Council.

JTAG – Joint Testability Action Group.

K – When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65\,536$ bits.

Mask-Programmed Read-Only Memory – A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory – A medium capable of storing information that can be retrieved.

Memory Card – A pocket-size memory storage system.

Memory Cell – The smallest subdivision of a memory into which a unit of data has been or can be entered in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) – The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

MIL-M-38510 – A military controlling specification pertaining mainly to JAN qualified devices (microcircuits).

MIL-STD-883 – A military controlling specification containing detailed descriptions of the screening processes pertaining to Class B and Class S devices (microcircuits).

NMOS – A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS.)

Nonvolatile Memory – A memory in which the data content is maintained whether the power supply is connected or not.

OTP – One-Time Programmable.

One-Time Programmable (OTP) Read-Only Memory – A read-only memory that, after being manufactured, can have the data content of each memory cell altered once. Also referred to as OTP.

Output Enable – A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select.)

PCMCIA – Personal Computer Memory Card International Association

PDIP – Plastic Dual-In-line Package.

PLCC – Plastic Leaded Chip Carrier.

PMOS – A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS.)

Parallel Access – A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down – A mode of a memory during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program – Typically associated with EPROM and OTP memories, the procedure whereby logical 0s (or 1s) are stored into various desired locations in a previously erased device.

Program Enable – An input signal that, when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) – See One-Time Programmable (OTP) Read-Only Memory.

Printed Wiring Board (PWB) – A substrate of epoxy glass, clad material, or other material upon which a pattern of conductive traces is formed to interconnect the components that will be mounted upon it.

Read – A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) – A memory in which the contents are not intended to be altered during normal operation. NOTE: Unless otherwise qualified, the term "read-only memory" implies that the contents are determined by its structure and are unalterable.

Read/Write Memory – A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe ($\overline{\text{RAS}}$) – A clock used in dynamic RAMs to control the input of the row addresses. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

SCD – Source Control Drawings.

Scaled-MOS (SMOS) – MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

SDRAM – Synchronous Dynamic Random Access Memory.

Semi-Static (Quasi-Static, Pseudo-Static) RAM – In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access – A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially from a single output.

SIP – Single In-line Package.

Small Outline Integrated Circuit (SOIC) – A package in which an integrated circuit chip can be mounted to form a surface-mounted component. It is made of a plastic material that can withstand high temperatures and has leads formed in a gull-wing shape along its two longer sides for connection to a PWB footprint.

SMD – Standard Military Drawing.

SOLCC – Small Outline Leadless ceramic Chip Carrier.

SOJ – Small Outline J-lead package.

SOP – Small Outline Package.

SQFP – Small Quad Flat Pack.

Static RAM (SRAM) – A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

ThinSOJ – (TSOJ) Thin Small-Outline J-Lead package.

ThinSOP – (TSOP) Thin Small-Outline package.

Very-Large-Scale Integration (VLSI) – The description of an IC technology that is much more complex than large-scale integration (LSI) and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Video RAM (VRAM) – A dual-port dynamic random-access memory with a on-chip serial data register.

Volatile Memory – A memory in which the data content is lost when the power supply is disconnected.

Word – A series of one or more bits that occupy a given address location and then can be stored and retrieved in parallel.

Write – A memory operation whereby data is written into a desired address location.

Write Enable – A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

ZIP – Zig-zag In-line Package.

OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}

The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}

The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance state) output current (of a three-state output,) I_{OZ}

The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{BB}, I_{CC}, I_{DD}, I_{PP}

The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

*Current out of a terminal is given as a negative value.

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground V_{SS}.

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the un-classified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$t_{AB\text{-}CD}$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high

L = low or transition to low

V = a valid steady-state level

X = unknown, changing, or "don't care" level

Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for $\overline{RAS}$.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older from t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high
$t_{h(CLCA)}$	t_{CL-CAX}	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	t_{RL-CAX}	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	t_{RL-RAX}	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(AC)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(RL)}$	t_{RLRH}	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)
$t_{su(CA)}$	t_{CAV-CL}	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	t_{RAV-RL}	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	t_{CHCH}	$\overline{CAS}$ rise time
$t_{f(C)}$	t_{CLCL}	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

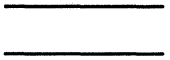
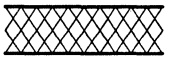
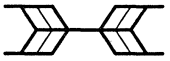
The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address

This supersedes the older form t_{PVX}.

TIMING DIAGRAMS CONVENTIONS

Timing Diagram Symbol	Meaning: Input Forcing Functions	Meaning: Output Response Functions
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated intervals
	Low-to-high changes permitted	Will be changing from low to high sometime during designated intervals
	Don't care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

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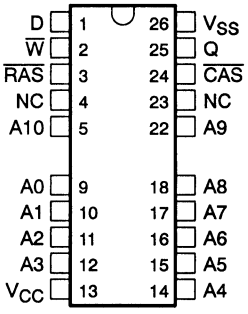
- **Organization . . . 4 194 304 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

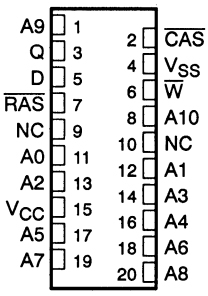
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44100/P-60	60 ns	15 ns	30 ns	110 ns
TMS44100/P-70	70 ns	18 ns	35 ns	130 ns
TMS44100/P-80	80 ns	20 ns	40 ns	150 ns

- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **1024-Cycle Refresh in 16 ms (Max)**
  - **128 ms for Low Power, Self-Refresh Version (TMS44100P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 300-Mil 20/26-Lead Surface Mount (SOJ) Package, 20-Pin Zig-Zag In-line (Zip) Package, 20/26-Lead Thin Small Outline (TSOP) Package, and Reverse Thin Small Outline Package**
- **Operating Free-Air Temperature Range 0°C to 70°C**

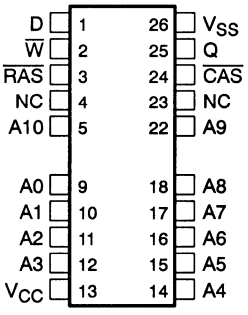
DJ PACKAGE† (TOP VIEW)



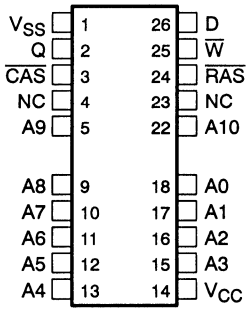
SD PACKAGE† (TOP VIEW)



DGA PACKAGE† (TOP VIEW)



DGB PACKAGE† (TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44100 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

The TMS44100P series are high-speed, low power, self-refresh 4 194 304-bit dynamic random-access memories organized as 4 194 304-words of one bit each.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power consumption is as low as 385 mW operating and 6 mW standby.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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(continued)

The TMS44100 and TMS44100P are offered in a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), a 20-pin zig-zag in-line package (SD suffix), a 20/26-lead plastic small outline package (DGA suffix), and a 20/26-lead plastic small outline package reverse form (DGB suffix). All packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A10)

Twenty two address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins

with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the 1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS44100P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 ms while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

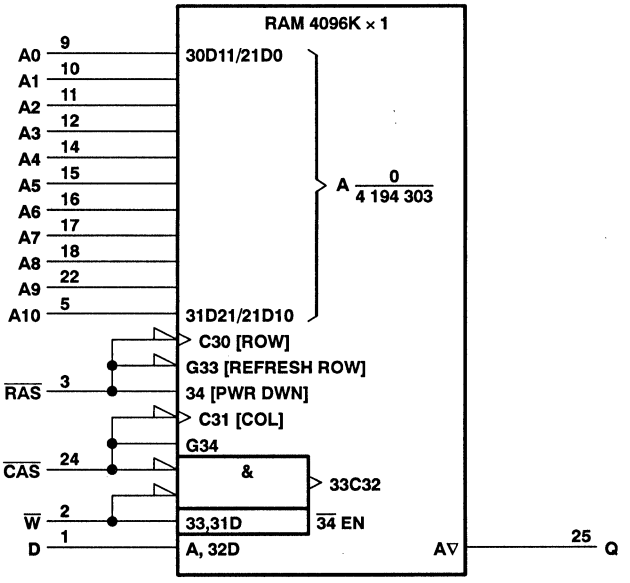
test mode

An industry standard Design For Test (DFT) mode is incorporated in the TMS44100. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

self refresh (TMS44100P)

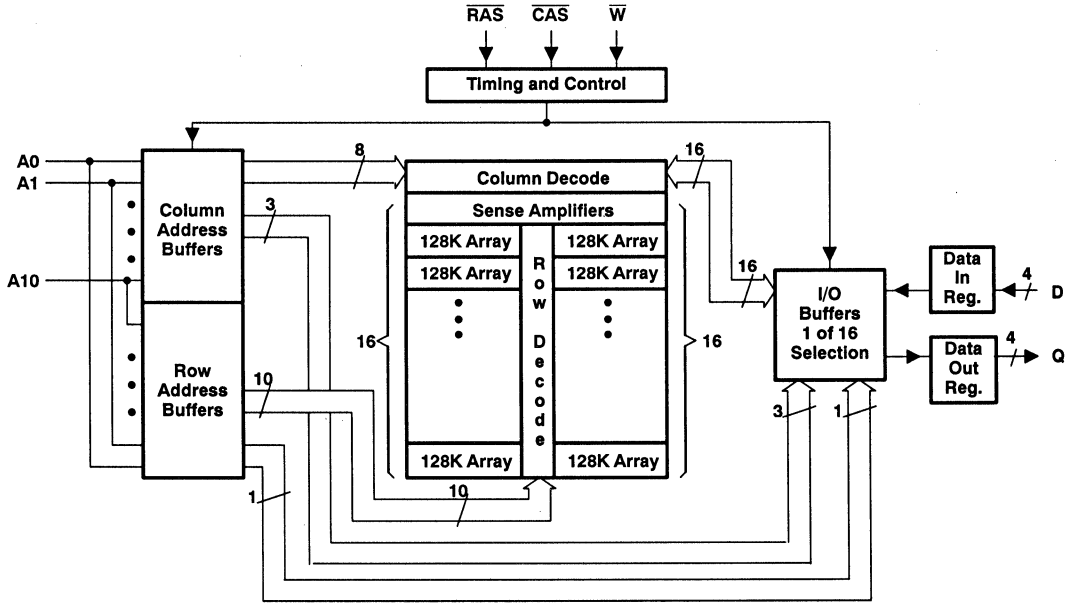
The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS44100-60 TMS44100P-60		TMS44100-70 TMS44100P-70		TMS44100-80 TMS44100P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V			105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'44100		1		1		1	mA
			'44100P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			105		90		80	mA
I_{CC4}†	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling			90		80		70	mA
I_{CC6}†‡	Self-refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, measured after t_{RASS} min			500		500		500	µA
I_{CC7}†	Standby current	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = Enabled			5		5		5	mA
I_{CC10}‡	Battery backup operating current (equivalent refresh time is 256 ms) CBR only	t_{RC} = 125 ms, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA

† Measured with outputs open.
‡ For TMS44100P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44100-60 TMS44100P-60		TMS44100-70 TMS44100P-70		TMS44100-80 TMS44100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44100-60 TMS44100P-60		TMS44100-70 TMS44100P-70		TMS44100-80 TMS44100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle time	130		153		175		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns

Continued next page.

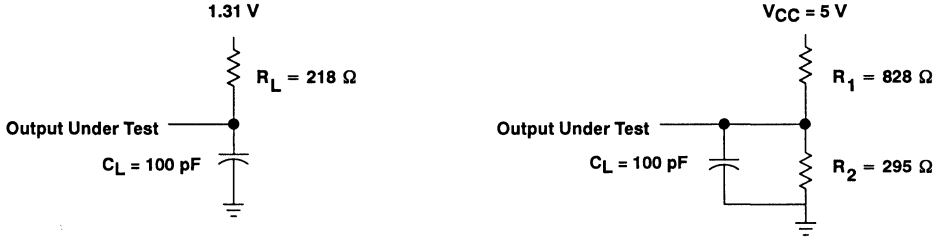
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

			TMS44100-60 TMS44100P-60		TMS44100-70 TMS44100P-70		TMS44100-80 TMS44100P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)		60		70		80		ns
t_{CPS}	$\overline{CAS}$ precharge before self-refresh		0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self-refresh		110		130		150		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low		100		100		100		ms
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)		–50		–50		–50		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	'44100		16		16		16	ms
		'44100P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

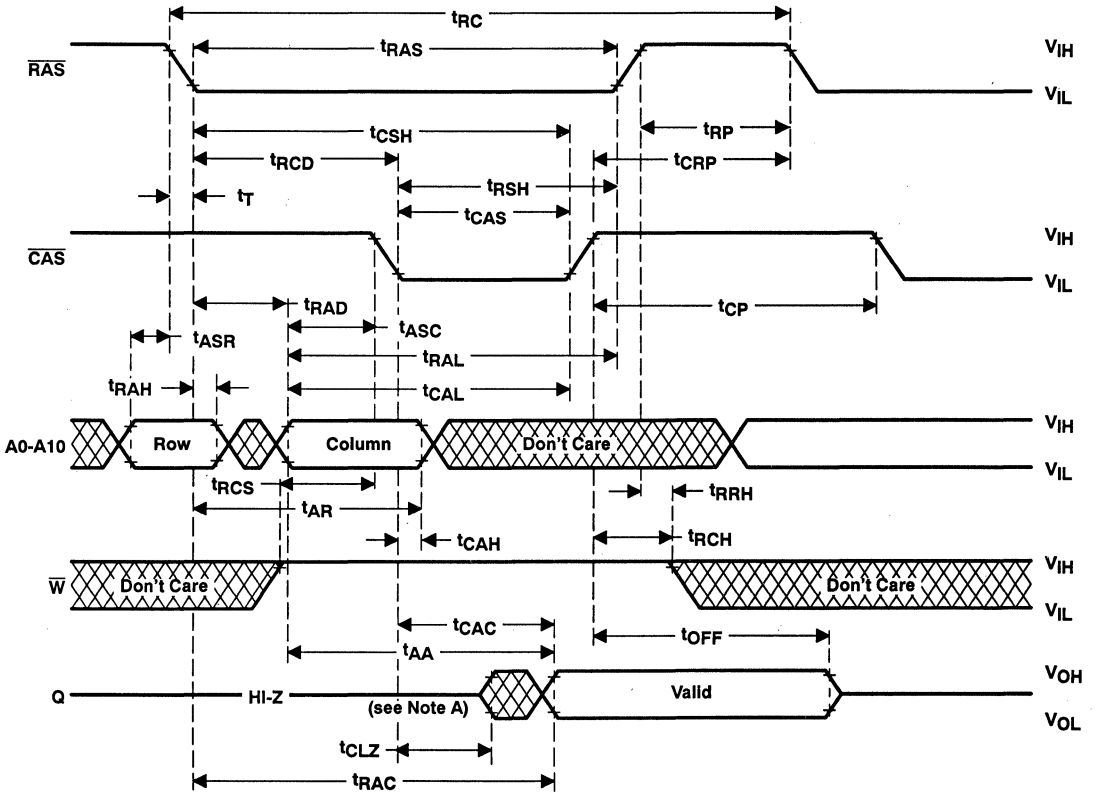
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

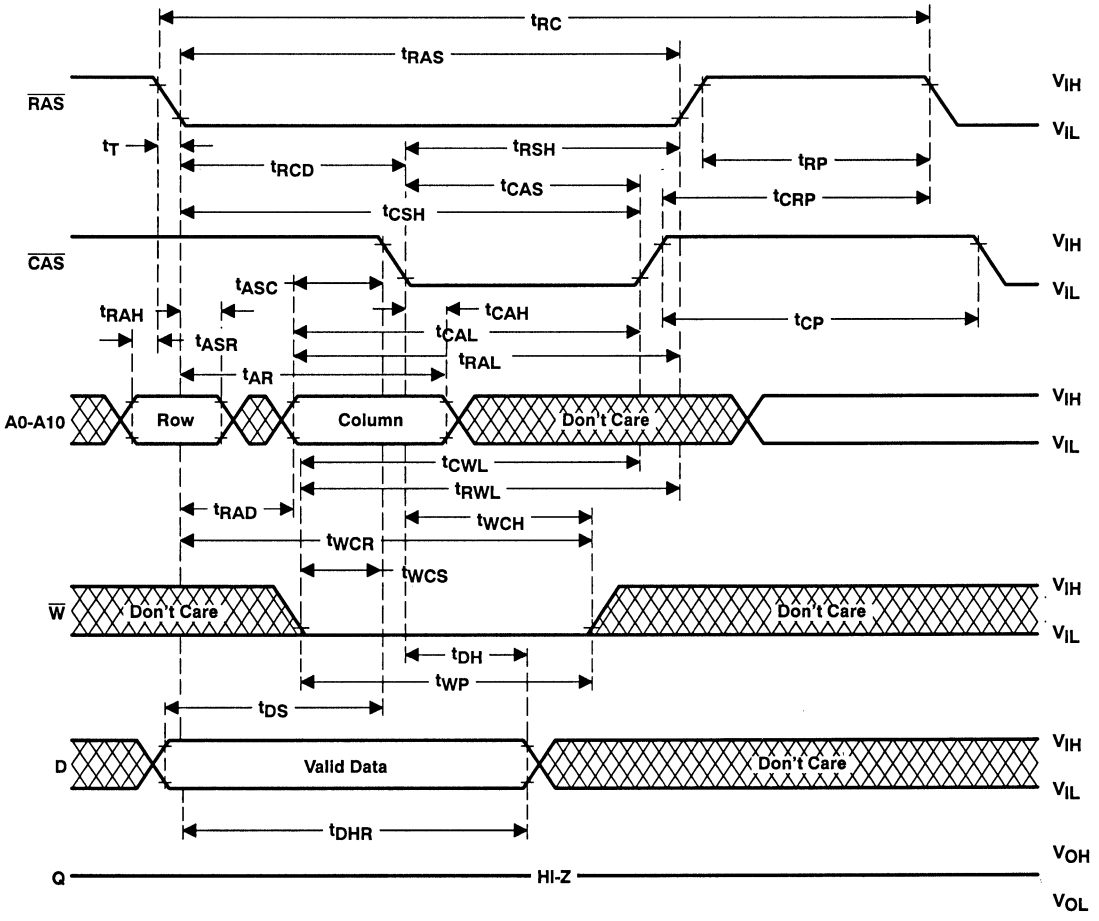


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

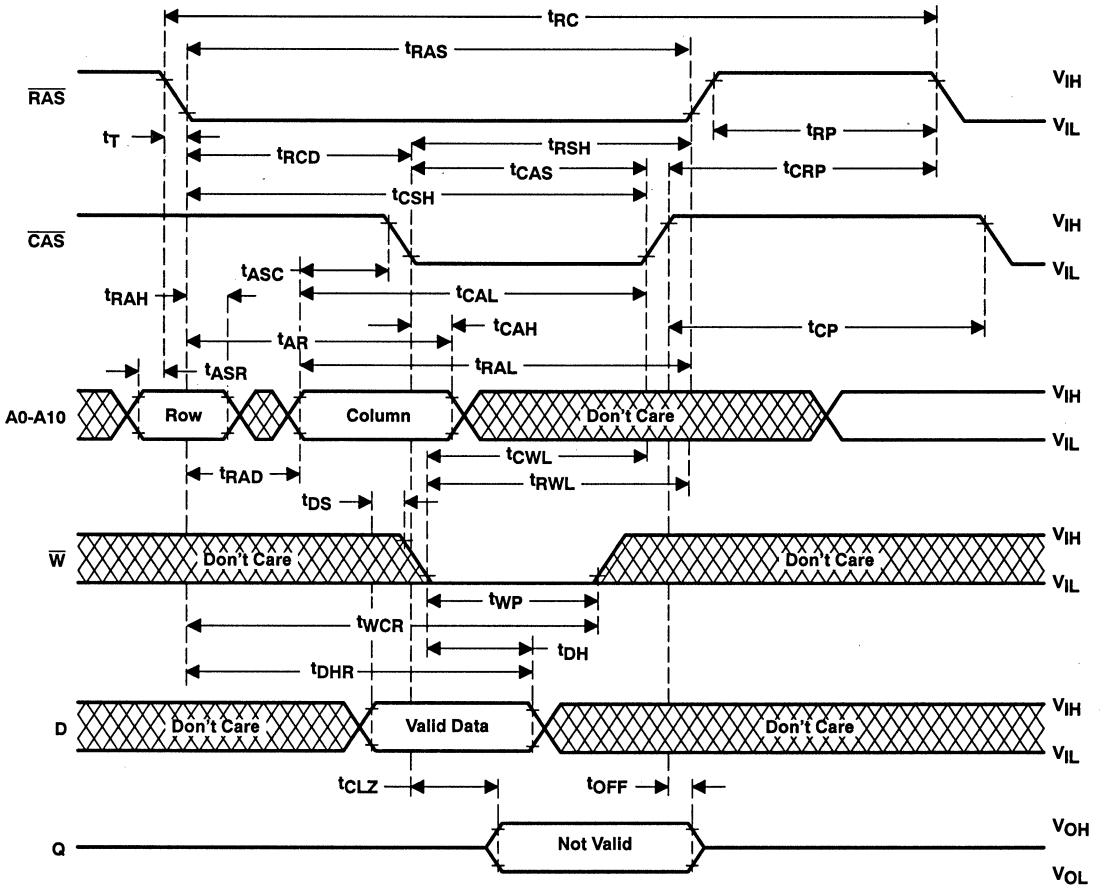


Figure 4. Write Cycle Timing

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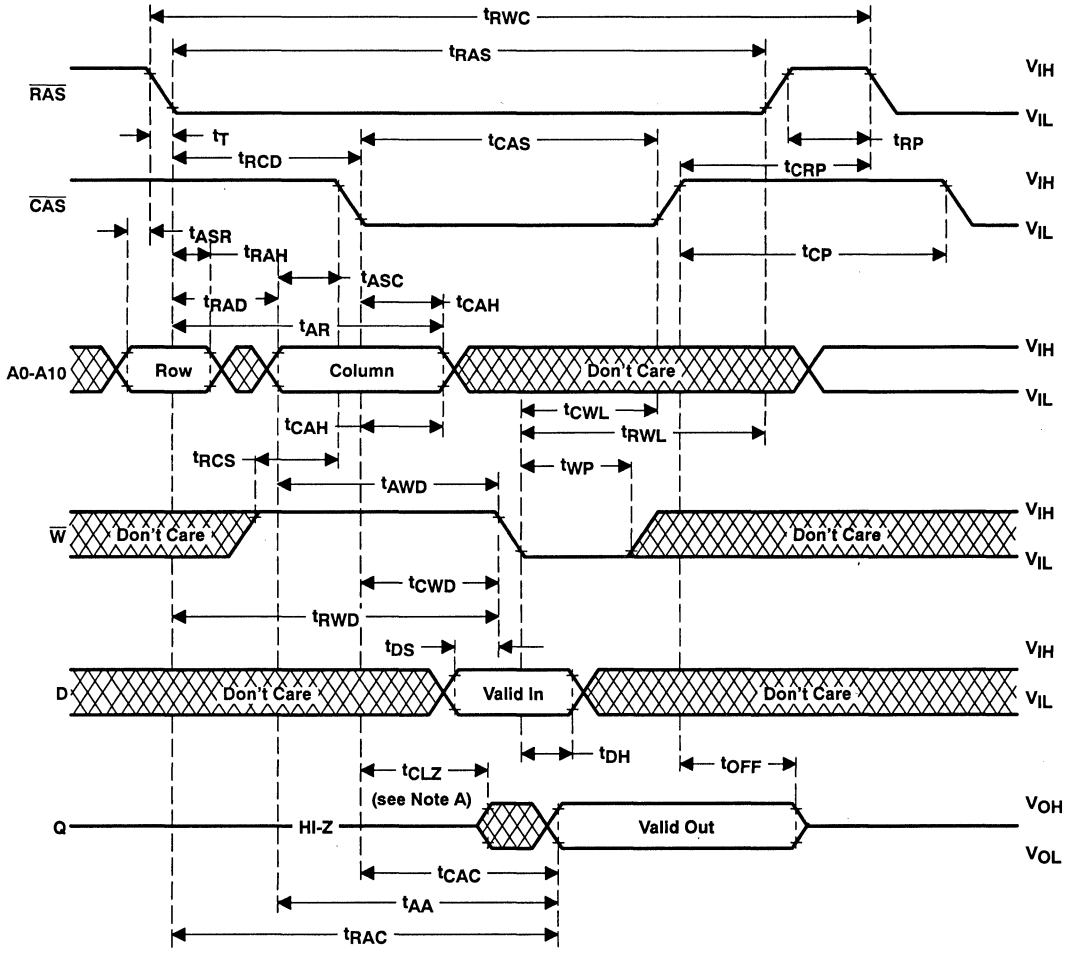
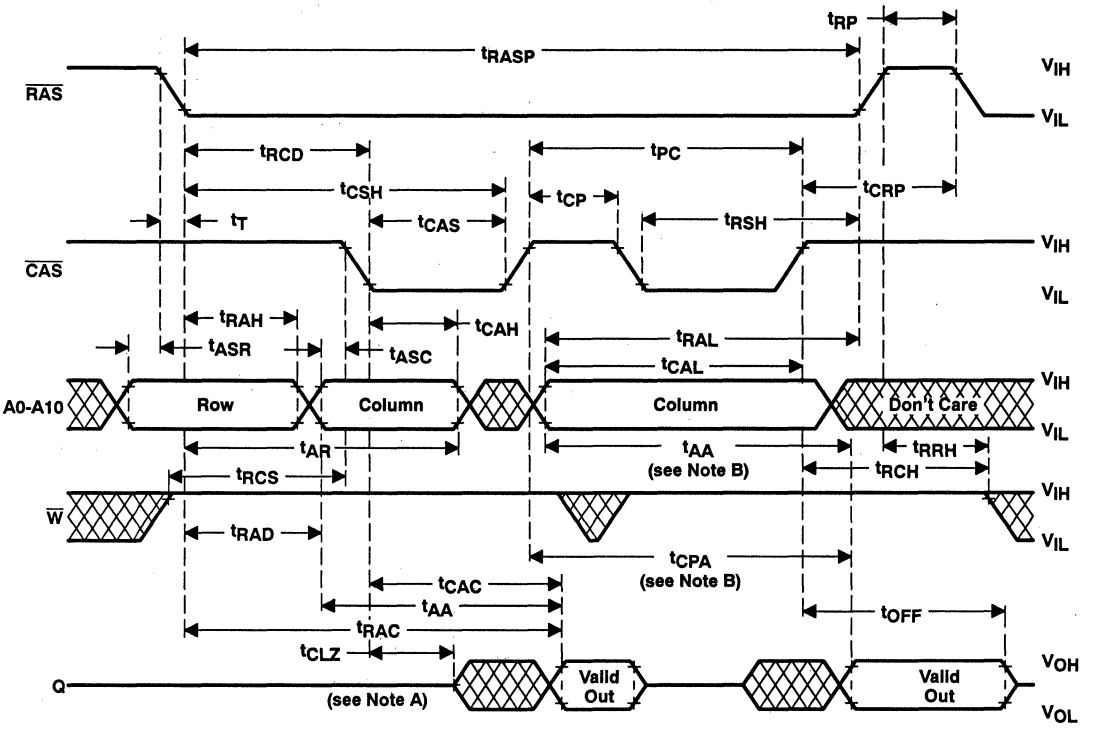
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

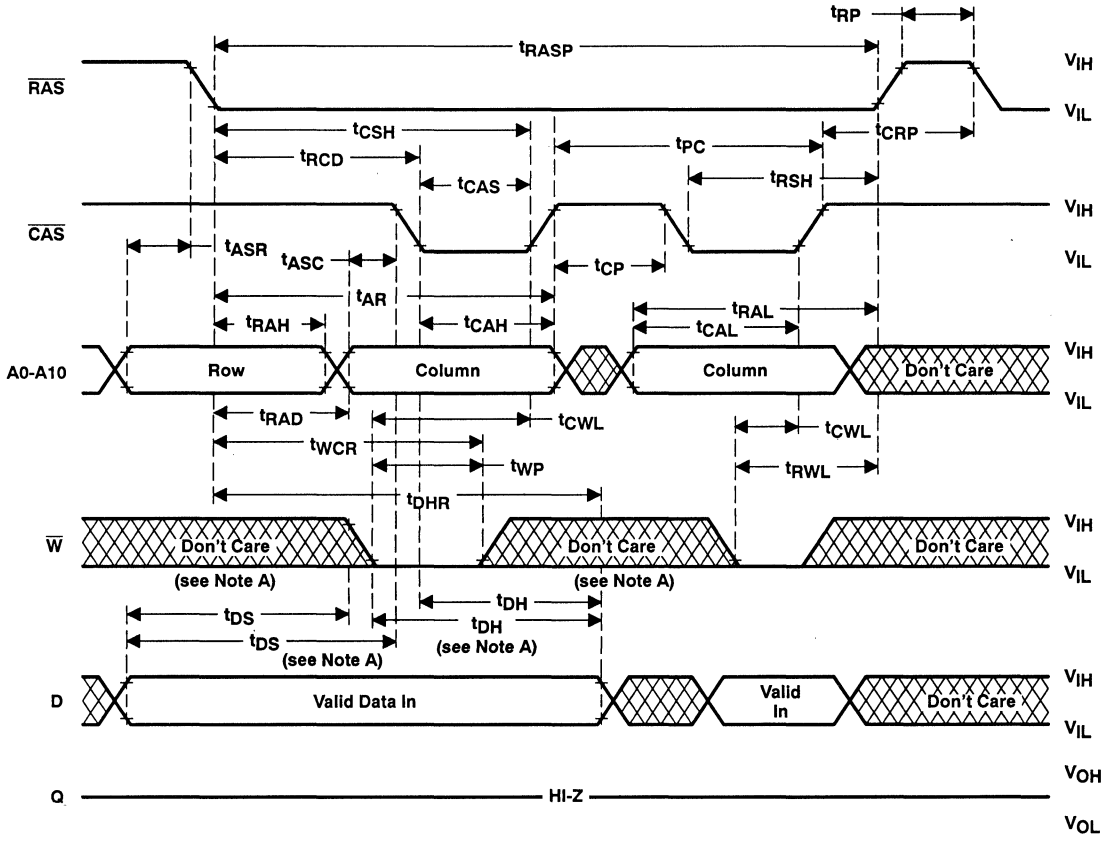
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

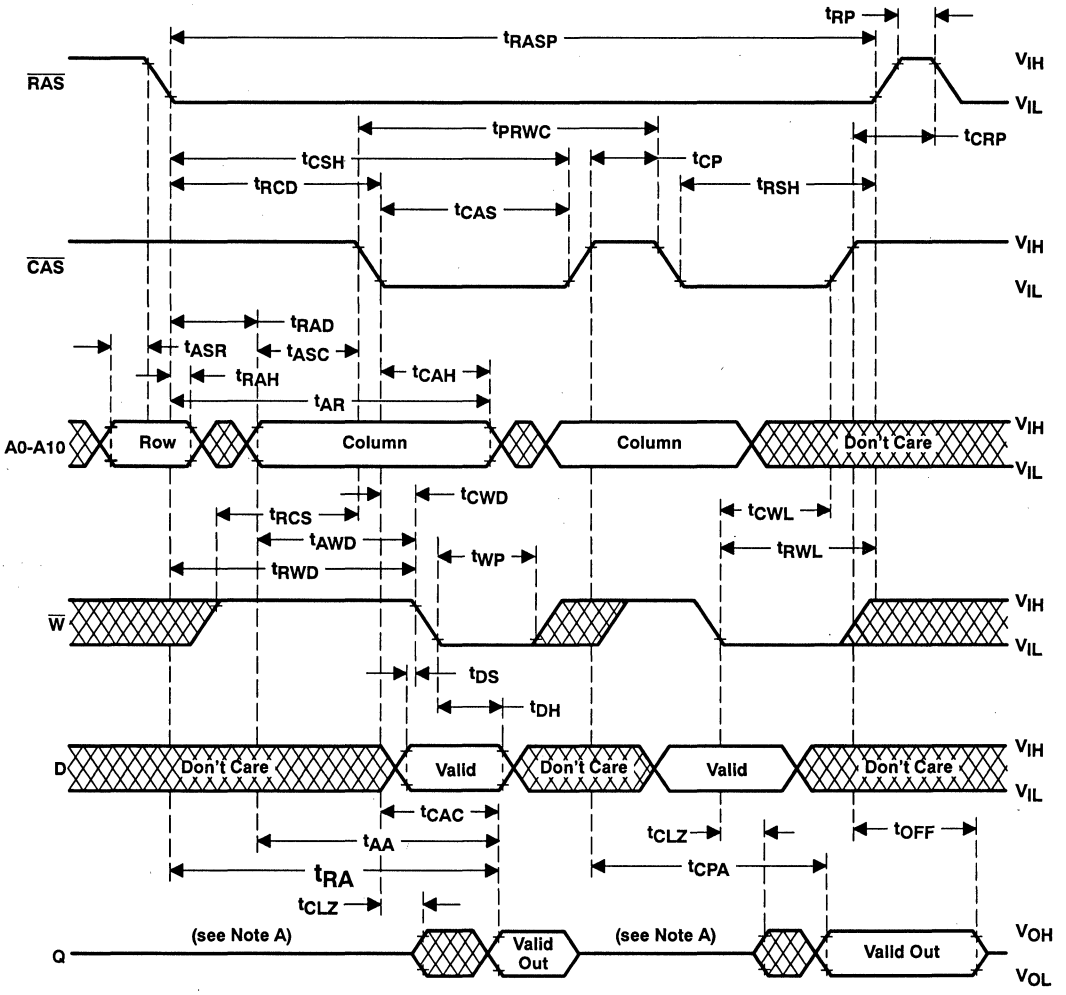
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

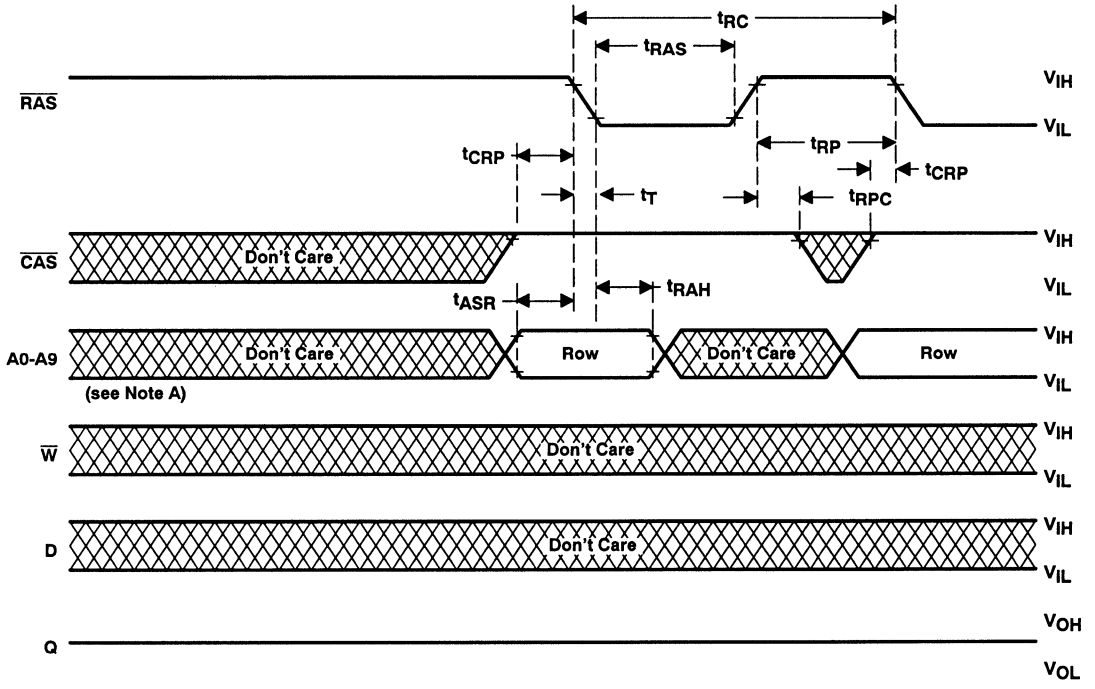
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

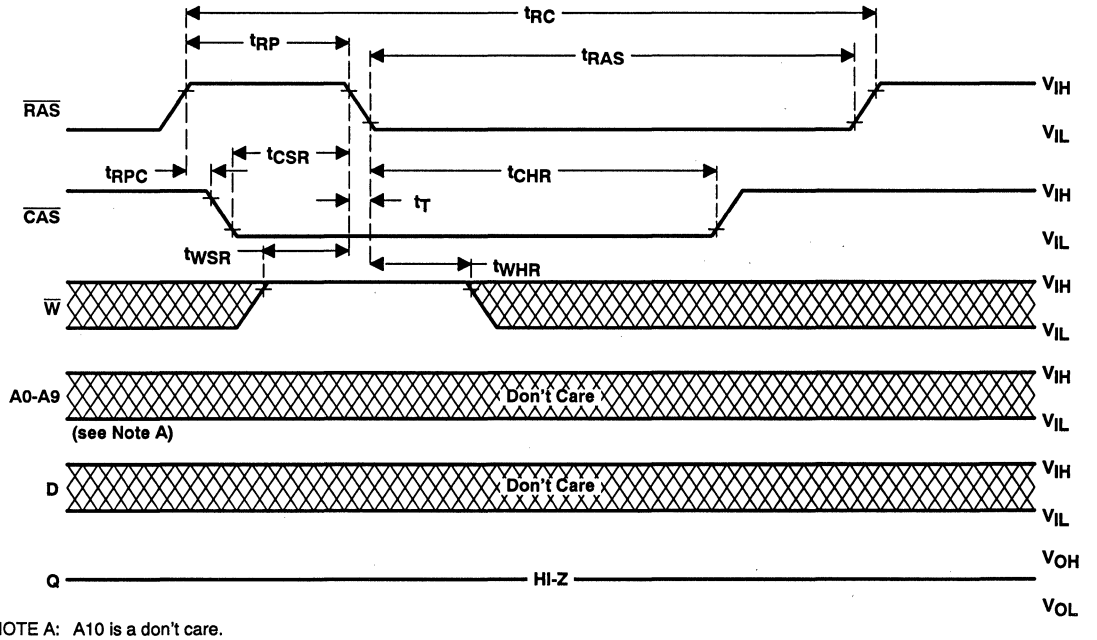
PARAMETER MEASUREMENT INFORMATION



NOTE A: A10 is a don't care.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: A10 is a don't care.

Figure 10. Automatic ($\overline{CAS}$-before-$\overline{RAS}$) Refresh Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

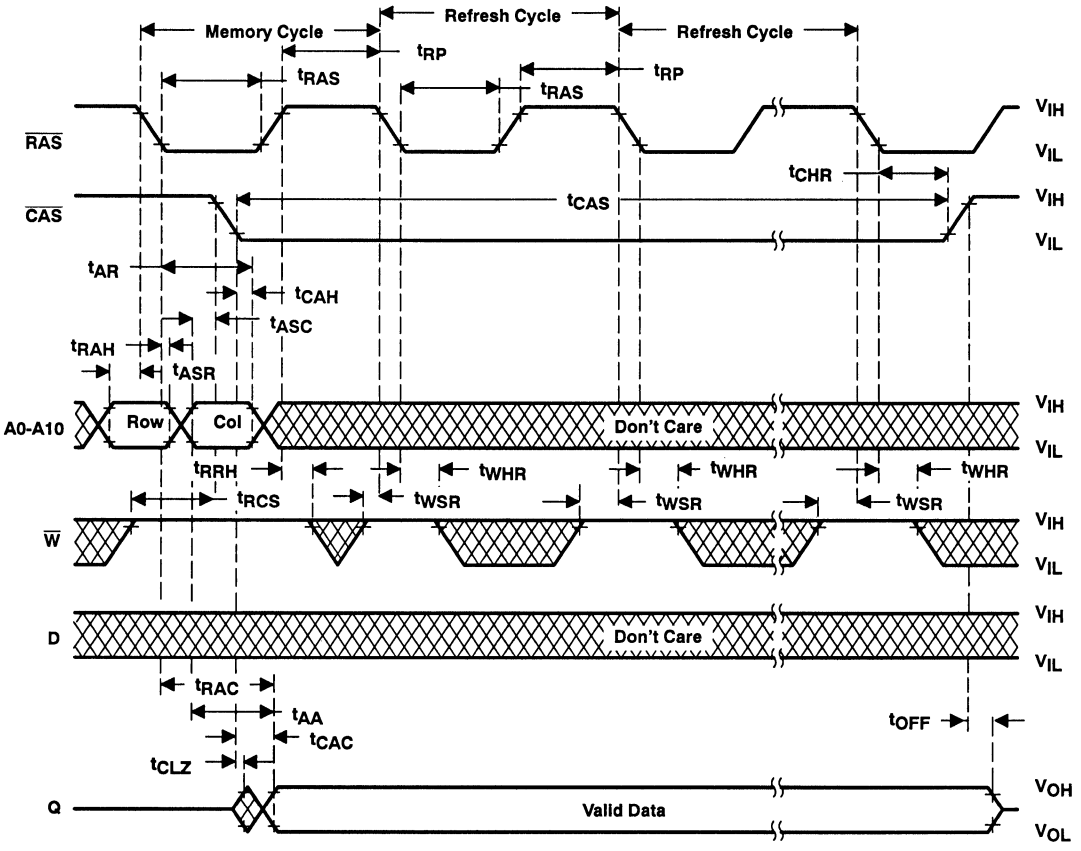


Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION

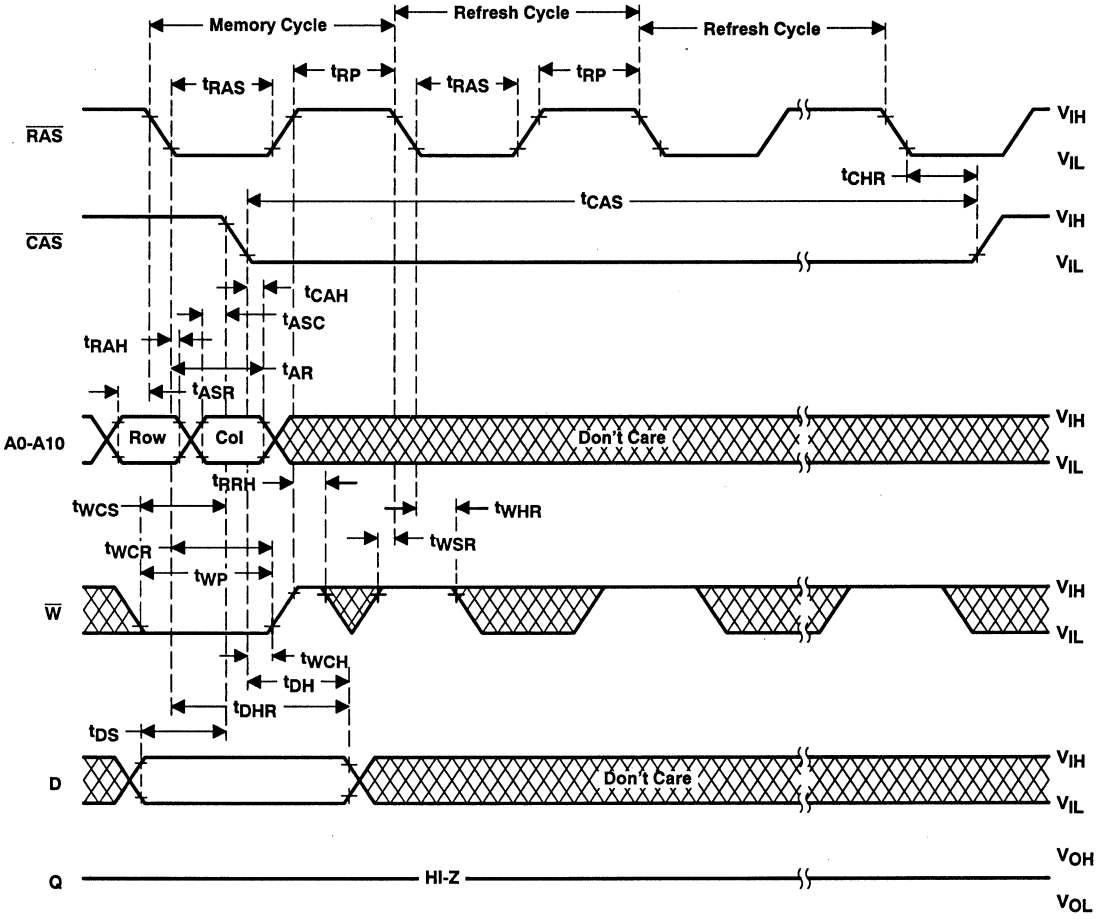


Figure 12. Hidden Refresh Cycle (Write)

PARAMETER MEASUREMENT INFORMATION

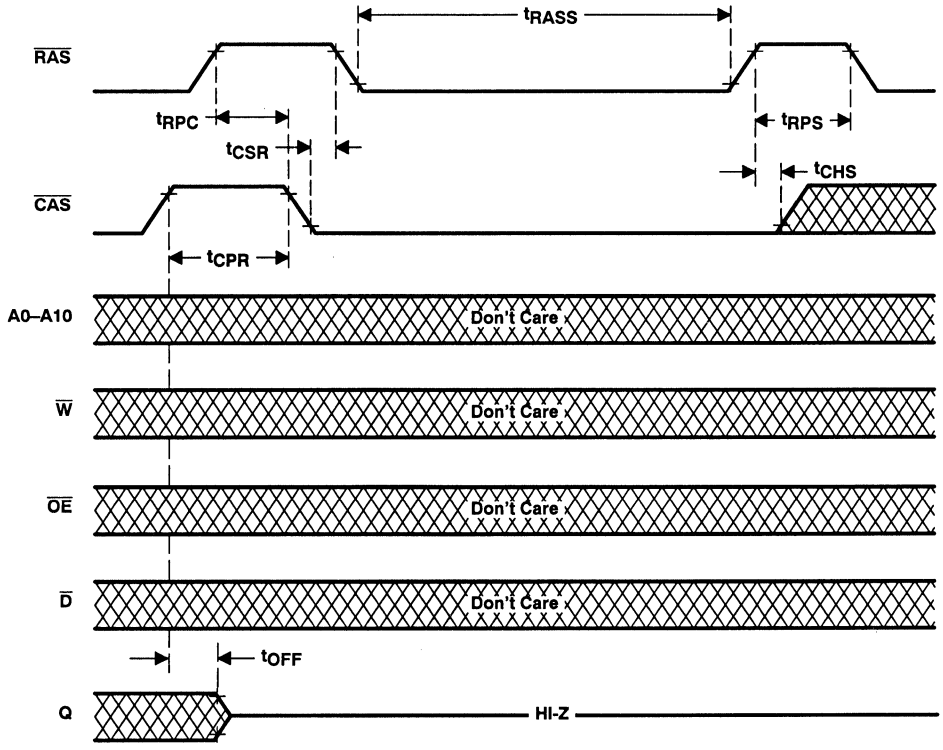


Figure 13. Self Refresh Timing

PARAMETER MEASUREMENT INFORMATION

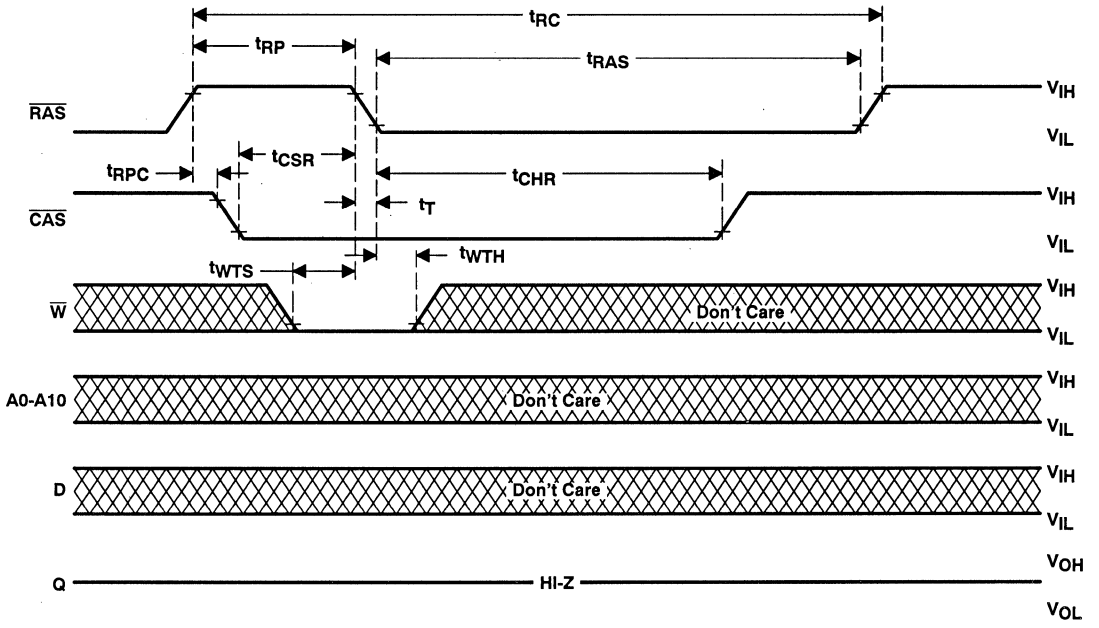
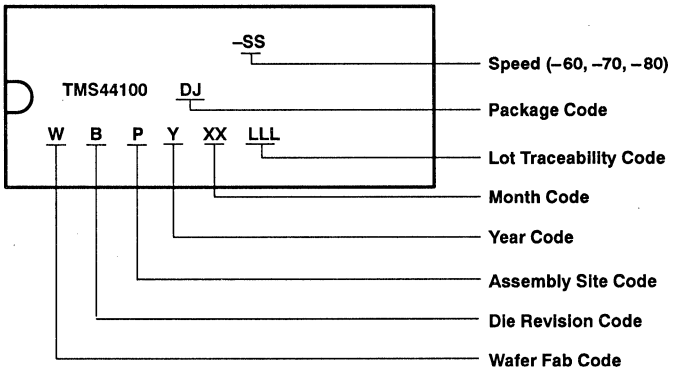


Figure 14. Test Mode Entry Cycle

device symbolization



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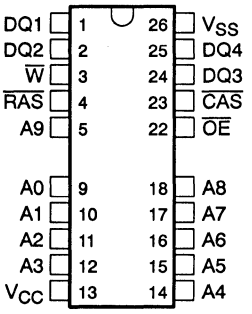
- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

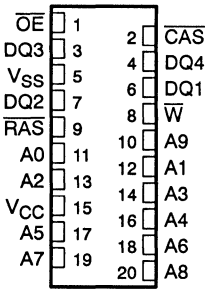
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44400/P-60	60 ns	15 ns	30 ns	110 ns
TMS44400/P-70	70 ns	18 ns	35 ns	130 ns
TMS44400/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period**
  - **1024-Cycle Refresh In 16 ms (Max)**
  - **128 ms for Low Power, Self-Refresh Version (TMS44400P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 300-Mil 20/26-Lead Surface Mount (SOJ) Package, 20-Pin Zig-Zag In-Line (ZIP) Package, 20/26-Lead Thin Small Outline (TSOP) Package, and Reverse Thin Small Outline Package**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**

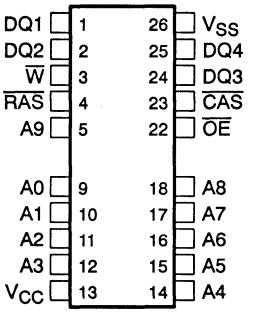
DJ PACKAGE† (TOP VIEW)



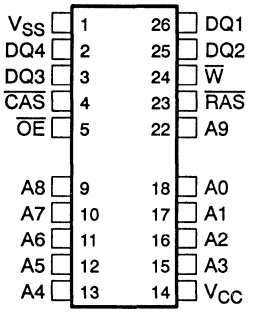
SD PACKAGE† (TOP VIEW)



DGA PACKAGE† (TOP VIEW)



DGB PACKAGE† (TOP VIEW)



†The packages shown are for pinout reference only.

description

The TMS44400 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

The TMS44400P series are high speed, low power, self-refresh 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
NC	No Internal Connection
V_{CC}	5-V Supply
V_{SS}	Ground

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power consumption is as low as 385 mW operating and 6 mW standby.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The TMS44400/P is offered in a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), a 20-pin zig-zag in-line package (SD suffix), a 20/26-lead plastic small outline package (DGA suffix), and a 20/26-lead plastic small outline package reverse form (DGB suffix). All packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44400/P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available in the TMS44400/P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \leq V_{CC} - 0.2$ V).

power-up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

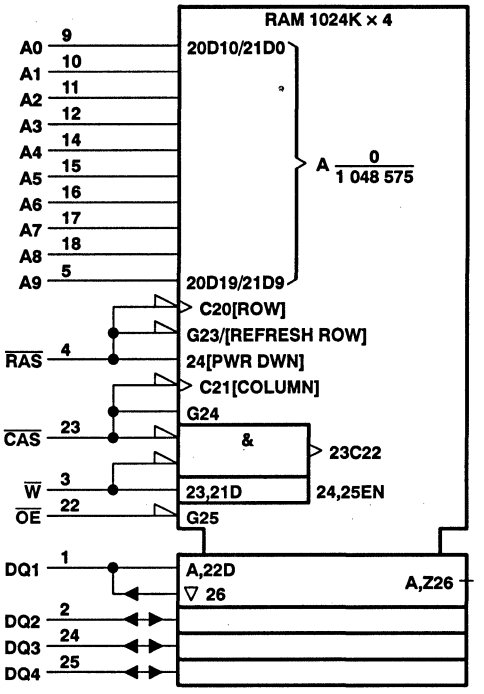
test mode

A Design For Test (DFT) mode is incorporated in the TMS44400. A $\overline{CAS}$-before-$\overline{RAS}$ with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different, a DQ pin will go low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1 meg × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode. On all devices marked with revision C, data may be written to and read from all four DQs. During a read cycle, two internal bits are compared for each DQ pin separately. If the two bits agree, the DQ pin will go high; if the two pins disagree, the DQ pin will go low.

self refresh (TMS44400/P)

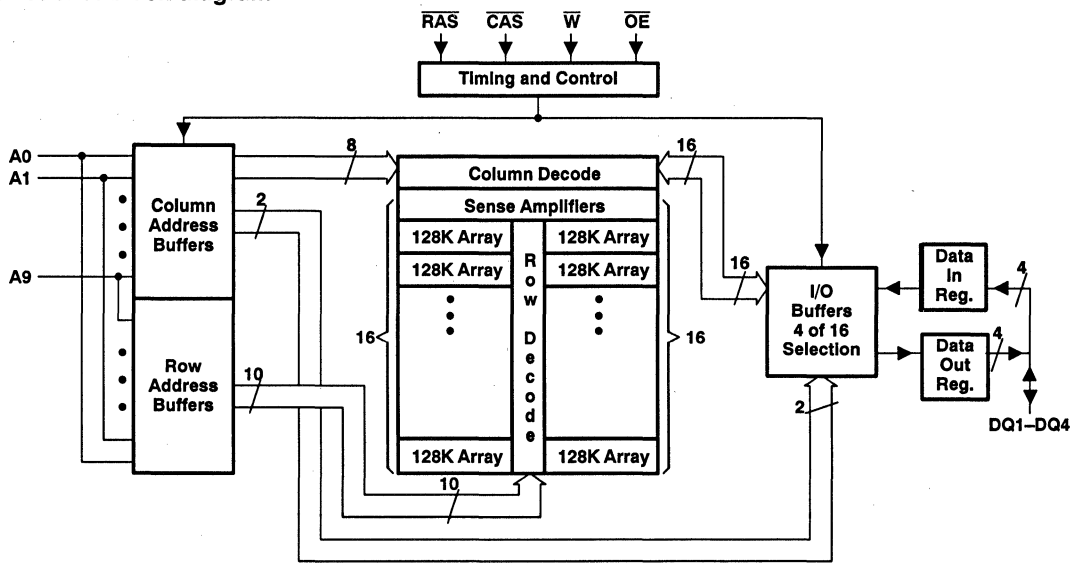
The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ packages.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS44400-60 TMS44400P-60		TMS44400-70 TMS44400P-70		TMS44400-80 TMS44400P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V			105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.05 V (CMOS)	'44400		1		1		1	mA
			'44400P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			105		90		80	mA
I_{CC4}†	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V $\overline{RAS}$ low, $\overline{CAS}$ cycling			90		80		70	mA
I_{CC6}†	Self-refresh current	$\overline{CAS}$, $\overline{RAS}$ < 0.2 V, measured after t_{RASS} min.			500		500		500	µA
I_{CC7}†	Standby current	$\overline{RAS}$ = VIH, $\overline{CAS}$ = VIL, Data out = Enabled			5		5		5	mA
I_{CC10}	Battery backup operating current (equivalent refresh time is 128 ms) CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA

† Measured with outputs open.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS44400-60 TMS44400P-60		TMS44400-70 TMS44400P-70		TMS44400-80 TMS44400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS44400-60 TMS44400P-60		TMS44400-70 TMS44400P-70		TMS44400-80 TMS44400P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$r efresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		ns

Continued next page.

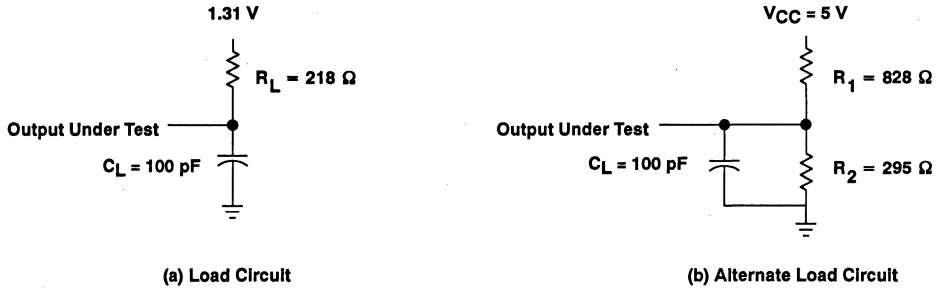
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

			TMS44400-60 TMS44400P-60		TMS44400-70 TMS44400P-70		TMS44400-80 TMS44400P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)		40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time		15		18		20		ns
t_{OED}	$\overline{OE}$ to data delay		15		18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)		85		98		110		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{CPS}	$\overline{CAS}$ precharge before self-refresh		0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self-refresh		110		130		150		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low		100		100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)		−50		−50		−50		ns
t_{REF}	Refresh time interval	'44400		16		16		16	ms
		'44400P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ns

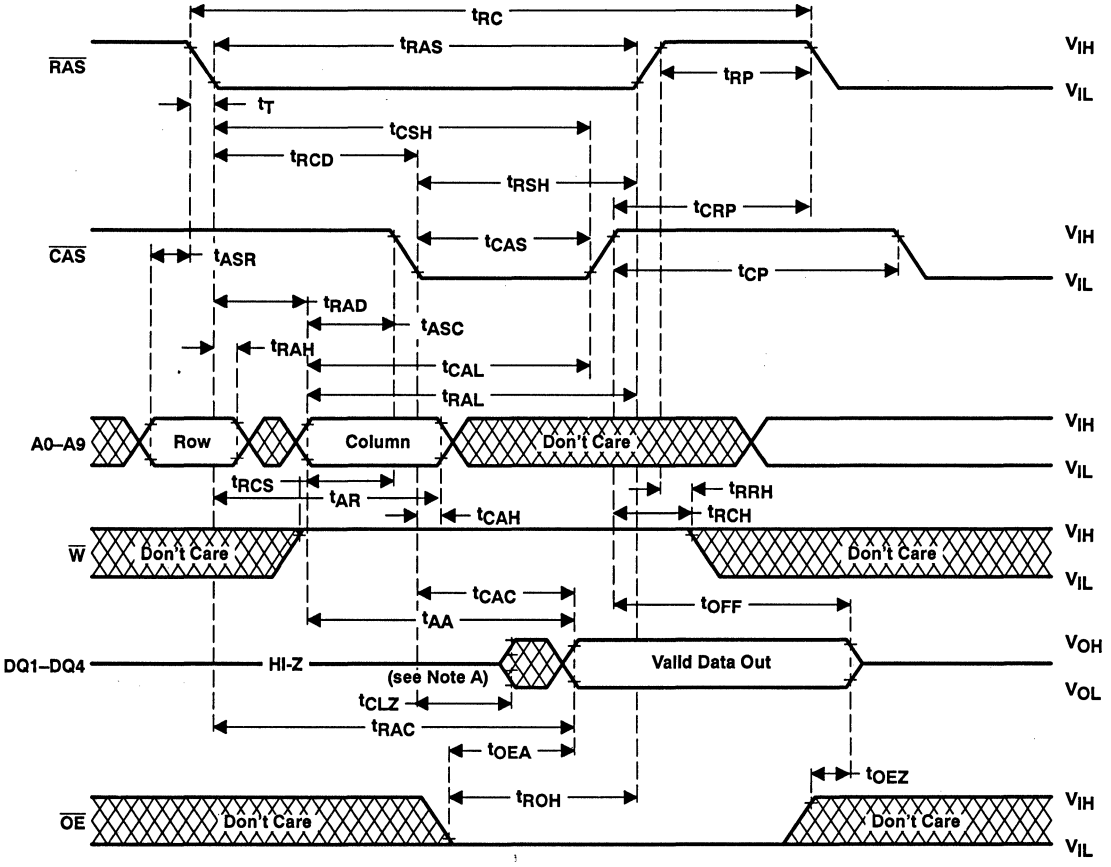
NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

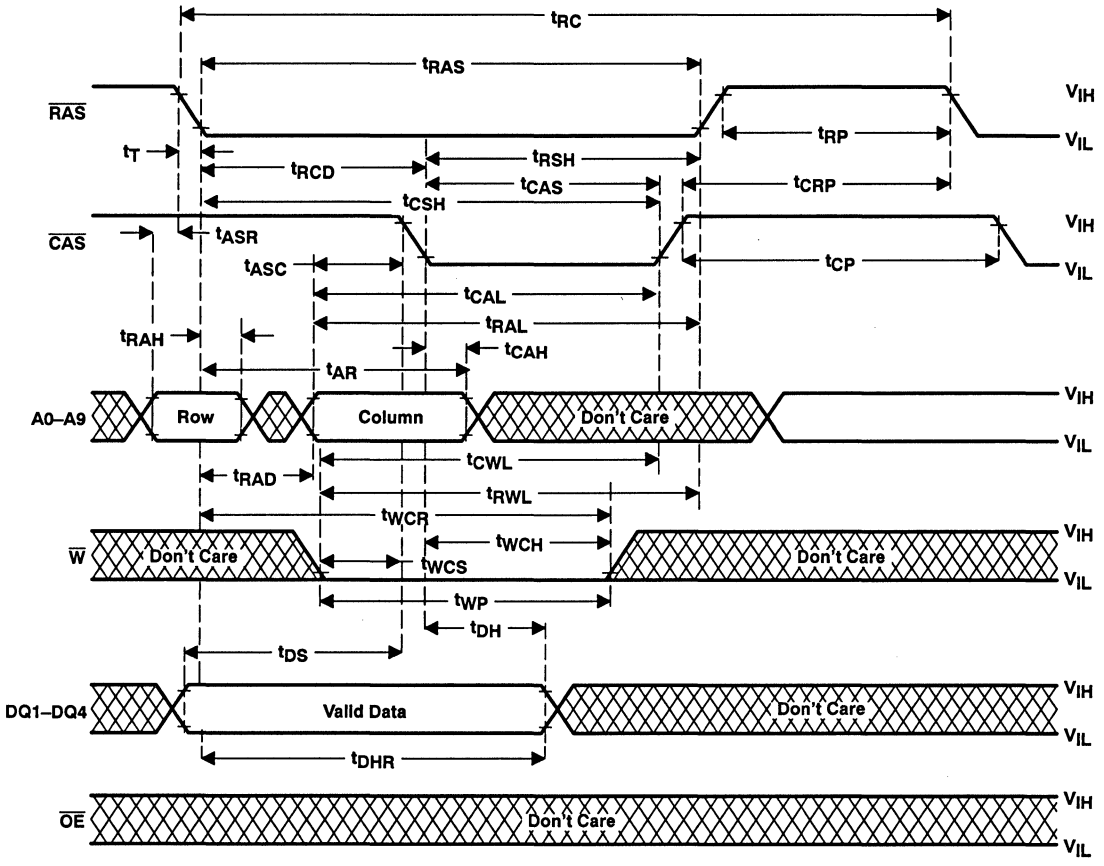


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

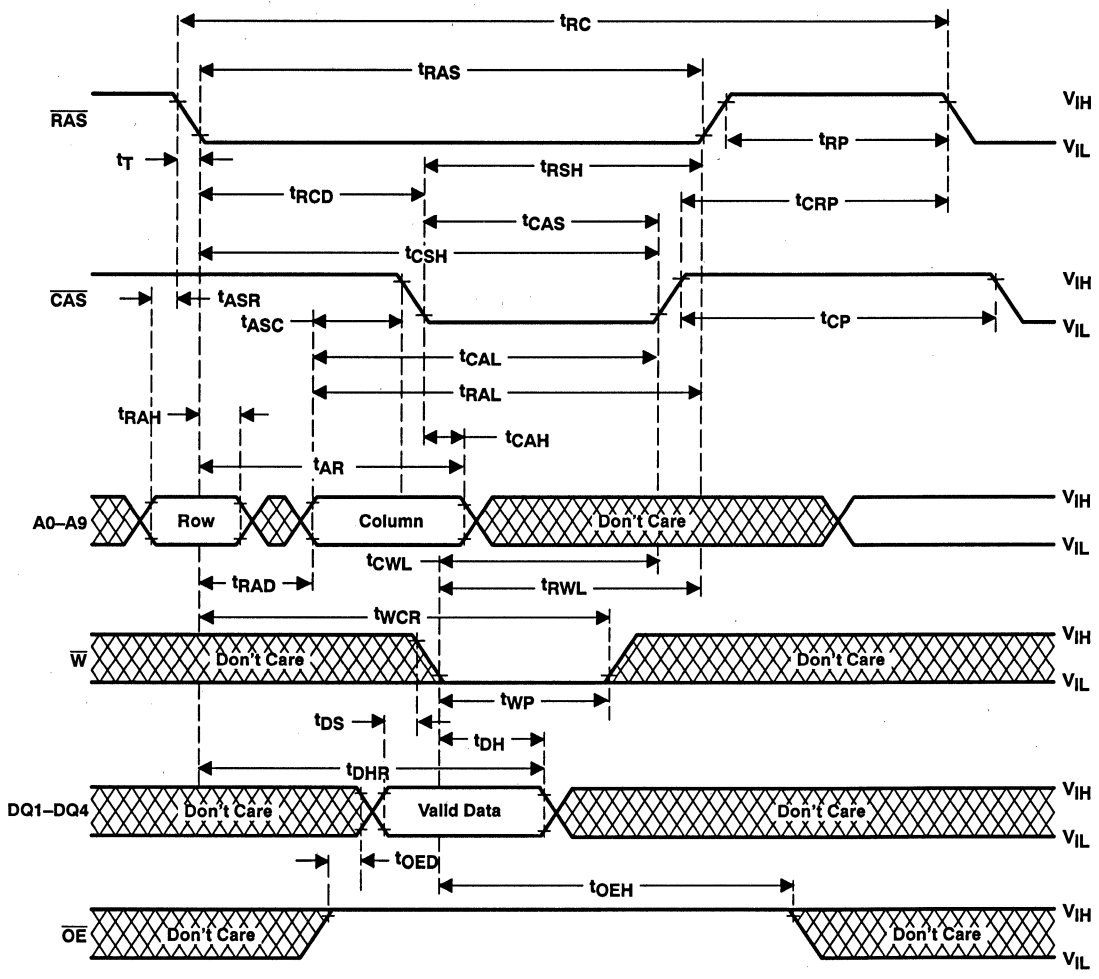


Figure 4. Write Cycle Timing

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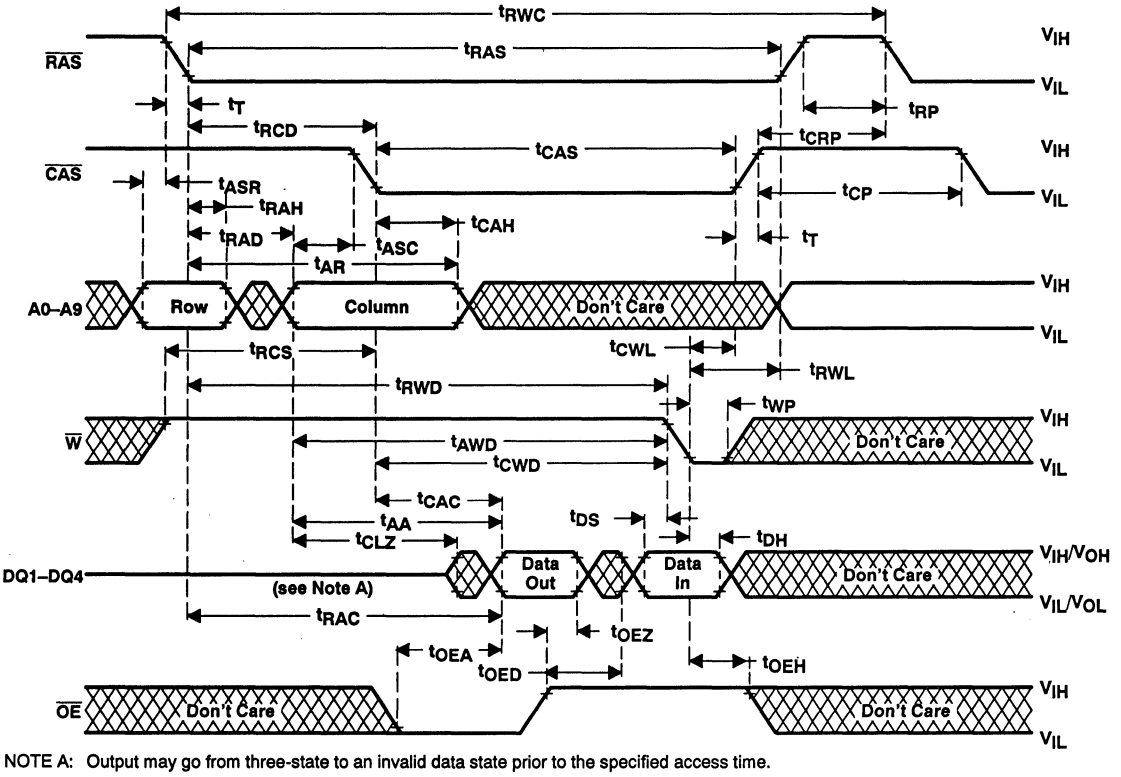
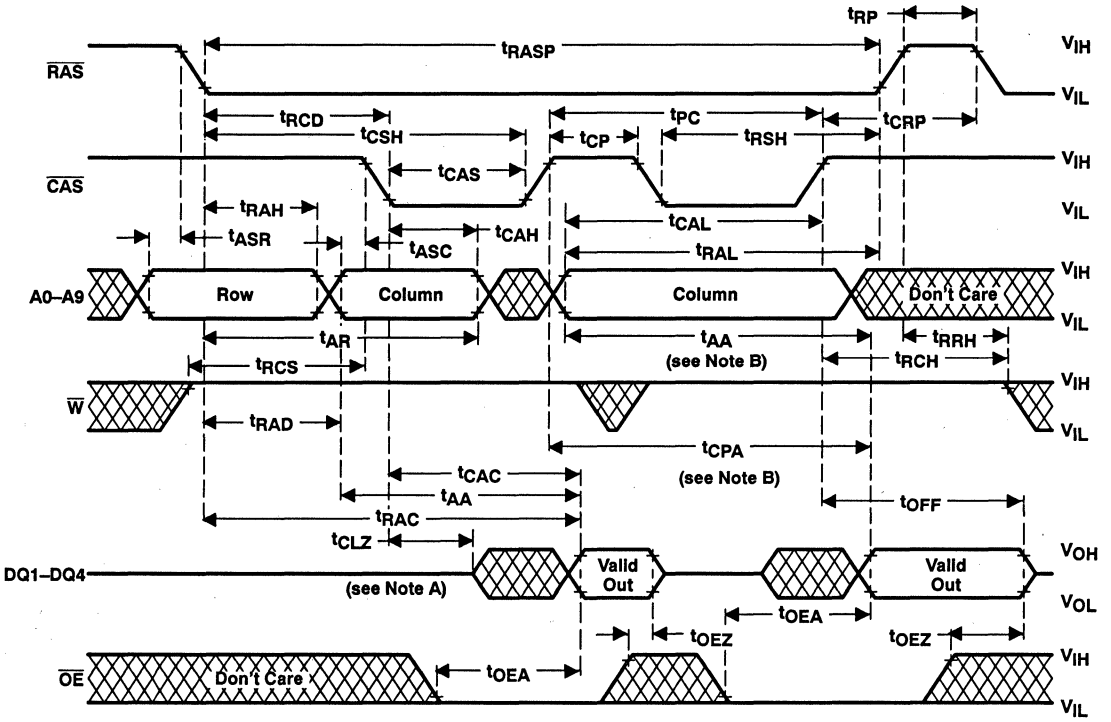
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 5. Read-write Cycle Timing

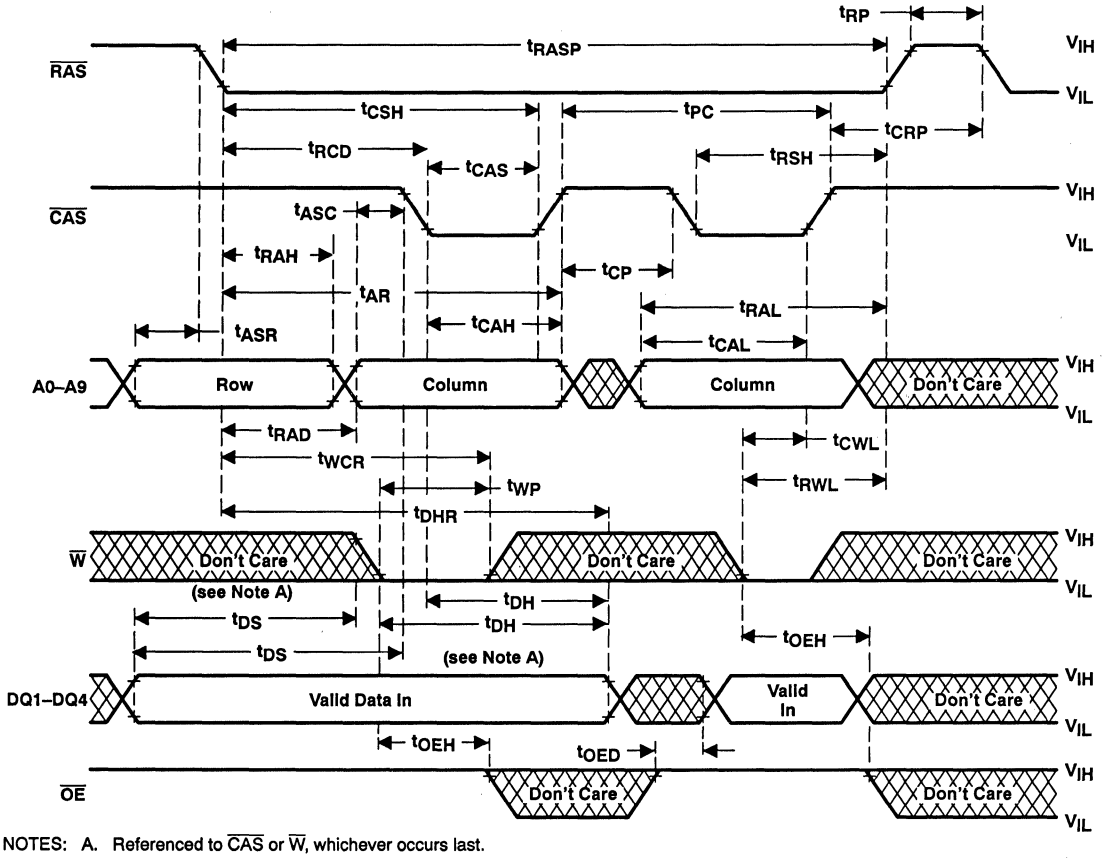
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

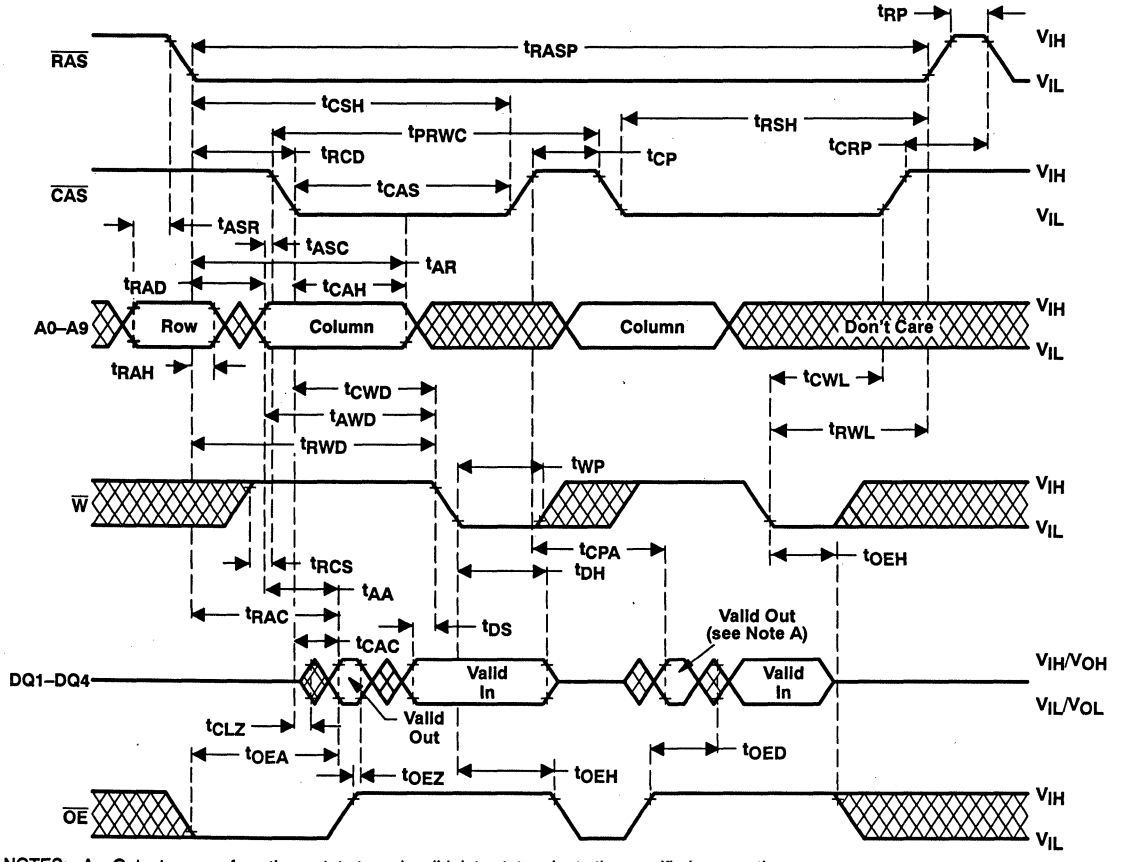
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-mode Read-write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

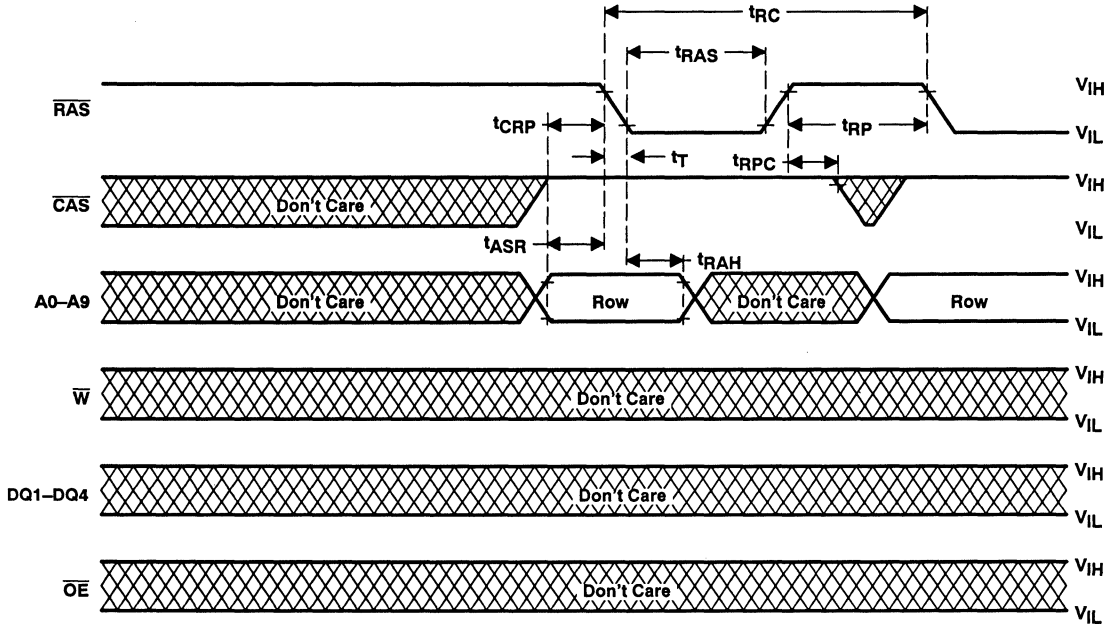


Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

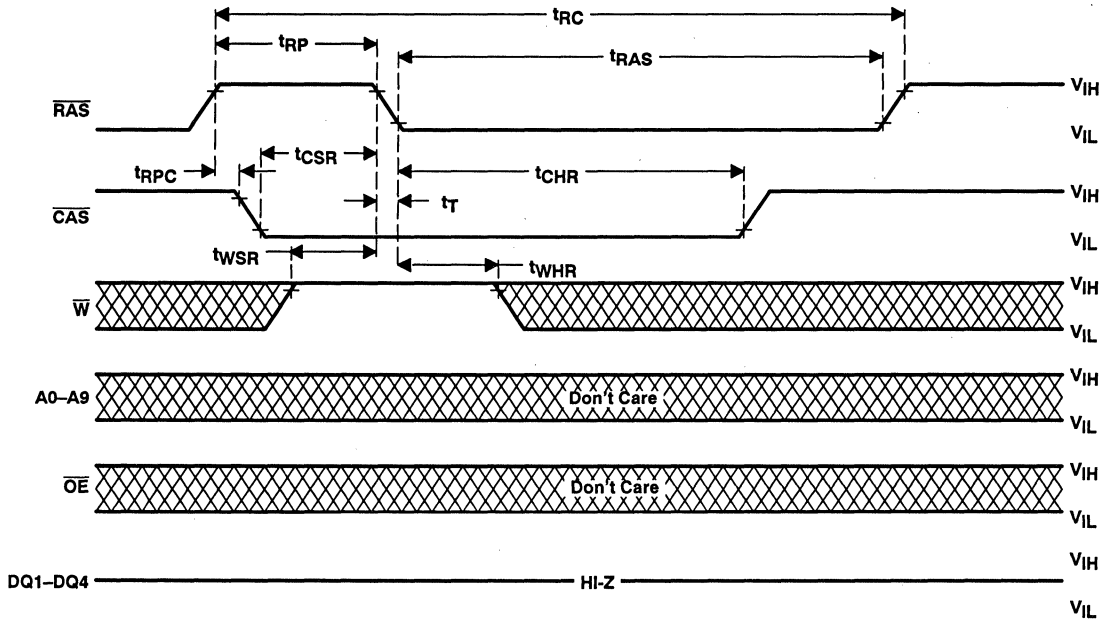


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

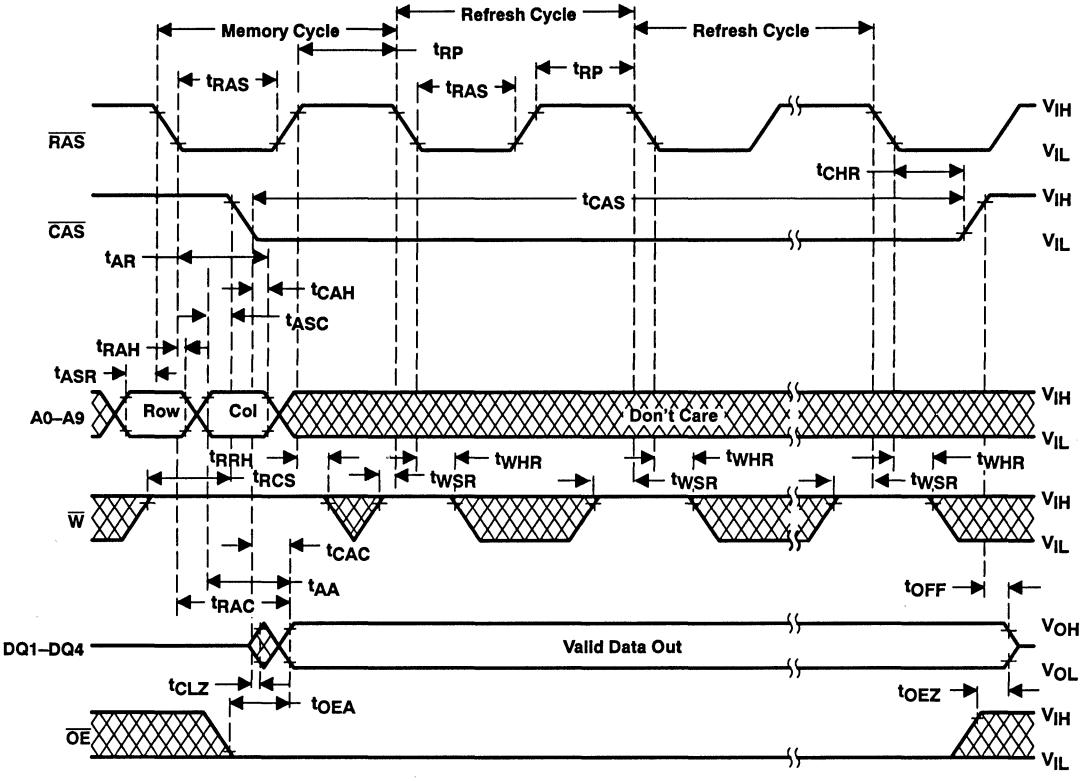


Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION

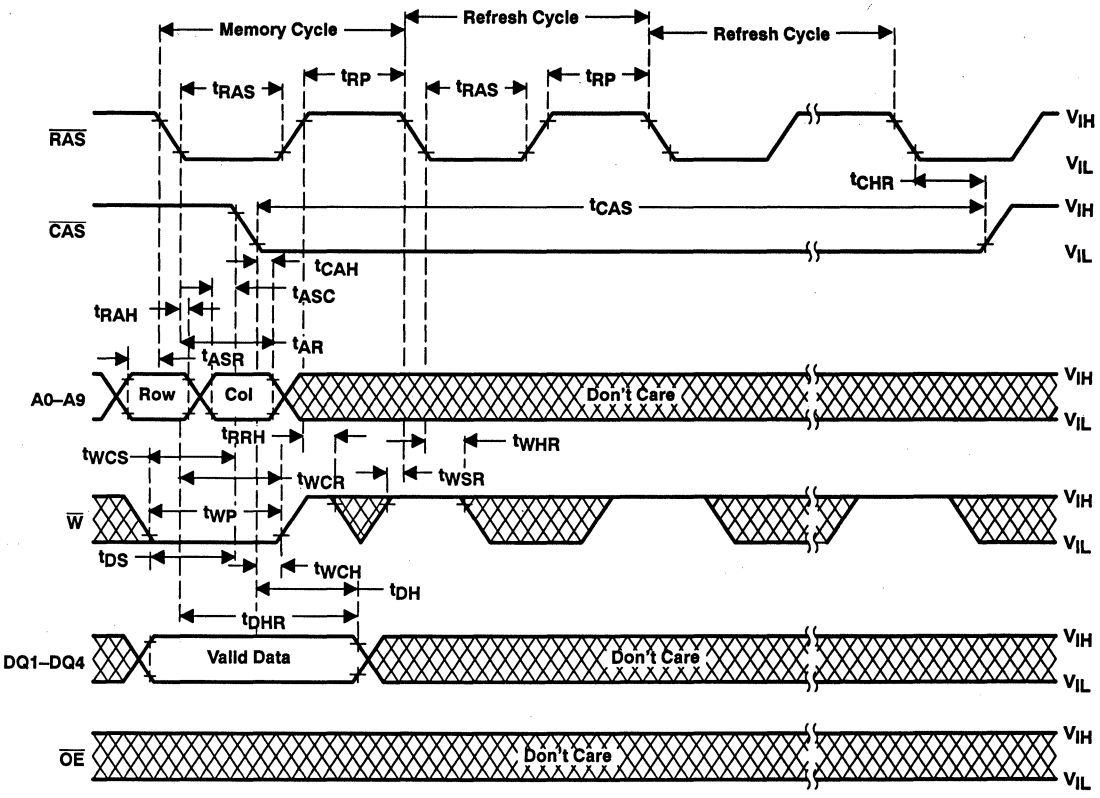


Figure 12. Hidden Refresh Cycle (Write)

PARAMETER MEASUREMENT INFORMATION

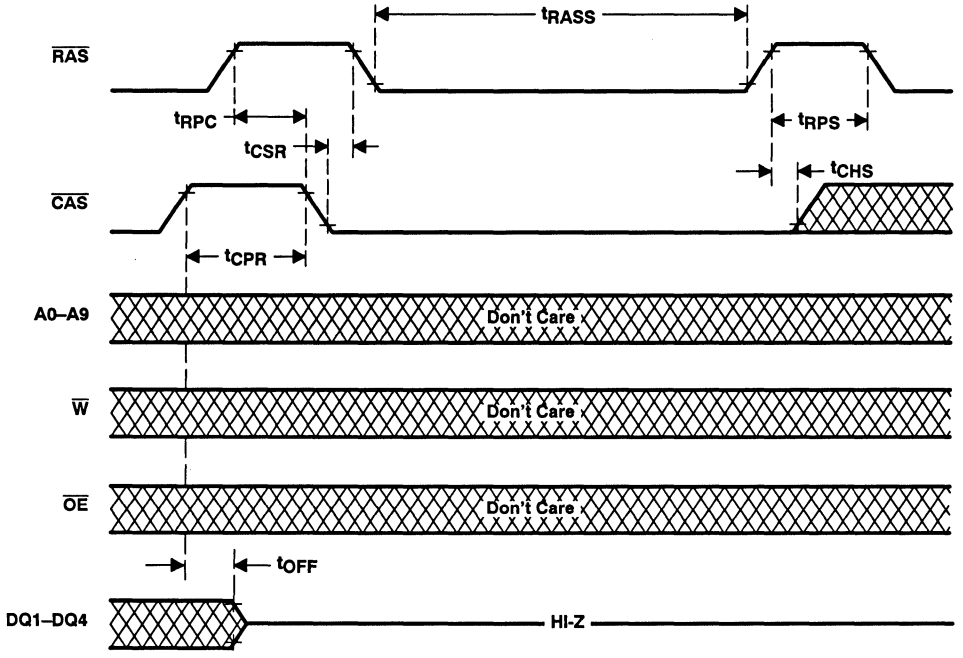


Figure 13. Self Refresh Timing

PARAMETER MEASUREMENT INFORMATION

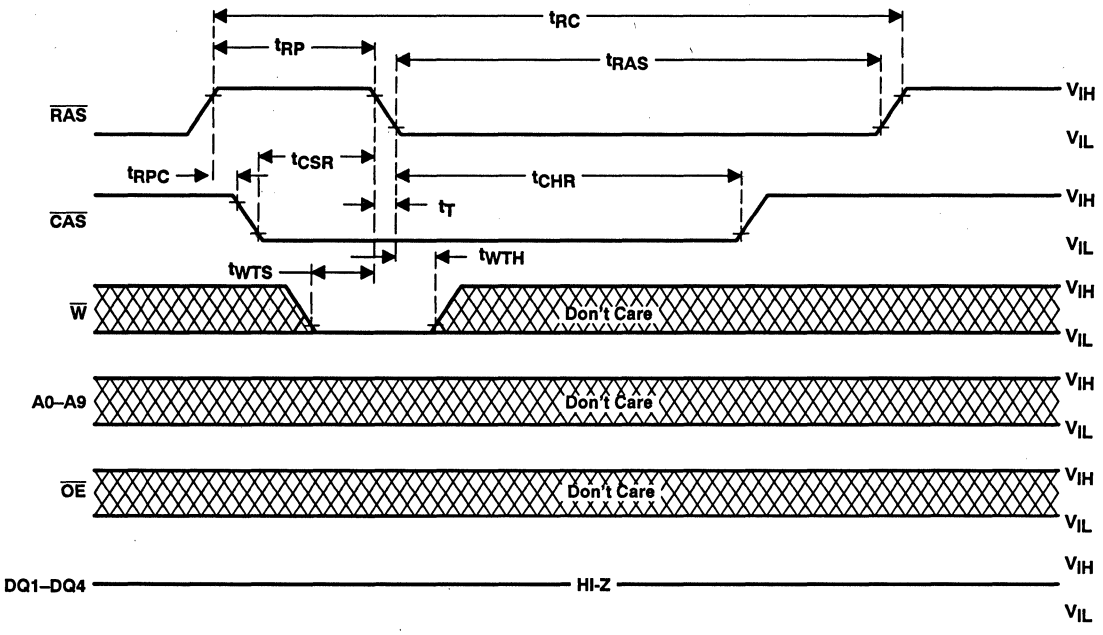
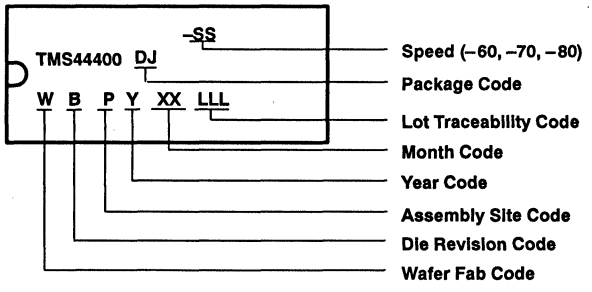


Figure 14. Test Mode Entry Cycle

device symbolization

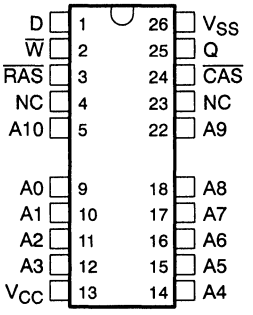


- **Organization . . . 4 194 304 × 1**
- **Single 3.3-V Power Supply (±0.3-V Tolerance)**
- **Low Power Dissipation (TMS46100P)**
  - **200 μA CMOS Standby**
  - **200 μA Self-Refresh**
  - **300 μA Extended Refresh Battery Backup**
- **Performance Ranges:**

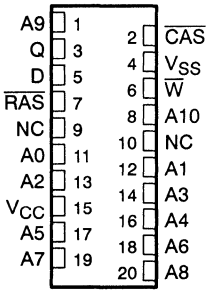
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS46100/P-70	70 ns	18 ns	35 ns	130 ns
TMS46100/P-80	80 ns	20 ns	40 ns	150 ns
TMS46100/P-10	100 ns	25 ns	50 ns	180 ns

- **Enhanced Page Mode Opration for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **1024-Cycle Refresh in 16 ms**
  - **128 ms (Max) for Extended-Refresh Version (TMS46100P)**
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 300-Mil 20/26-Lead Surface Mount (SOJ) Packages, 20-Pin Zig-Zag In-line (ZIP) Package, 20/26-Lead Thin Small Outline Package, and Reverse Thin Small Outline Package**
- **Operating Free-Air Temperature Range 0°C to 70°C**

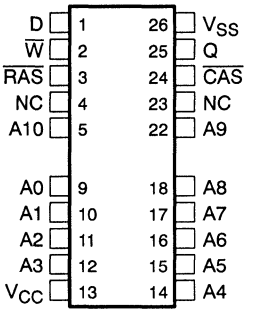
DJ PACKAGE† (TOP VIEW)



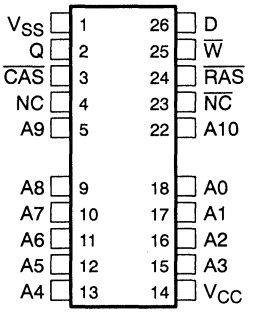
SD PACKAGE† (TOP VIEW)



DGA PACKAGE† (TOP VIEW)



DGB PACKAGE† (TOP VIEW)



†The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS46100 series are high-speed, low-voltage 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each.

The TMS46100P series are high-speed, self-refresh with extended-refresh, low-voltage, 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each.

Both series employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low voltage at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 180 mW operating, 0.72 mW standby, and 1.1 mW battery backup for an 80-ns device.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS46100 and TMS46100P are offered in a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), a 20-pin zig-zag in-line package (SD suffix), a 20/26-lead plastic small outline package (DGA suffix), and a 20/26-lead plastic small outline package, reverse form (DGB suffix). All packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS46100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A10)

Twenty two address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS46100P) to retain data. This can be achieved by strobing each of the 1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS46100P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs, while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

power-up

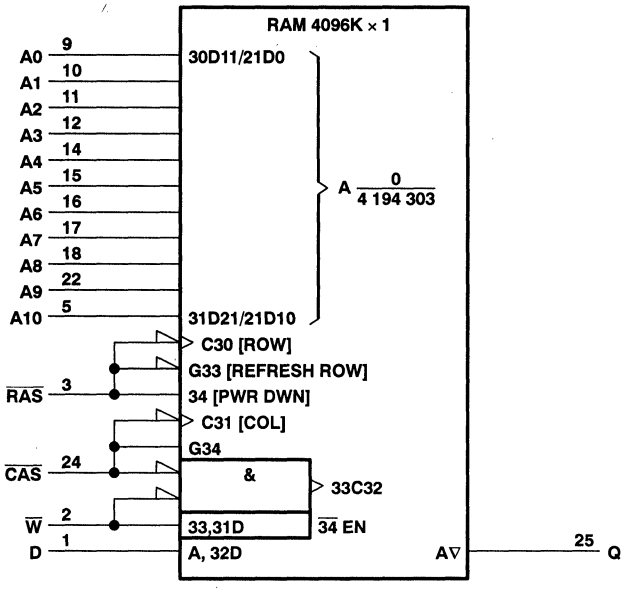
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

An industry standard Design For Test (DFT) mode is incorporated in the TMS46100 and TMS46100P. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

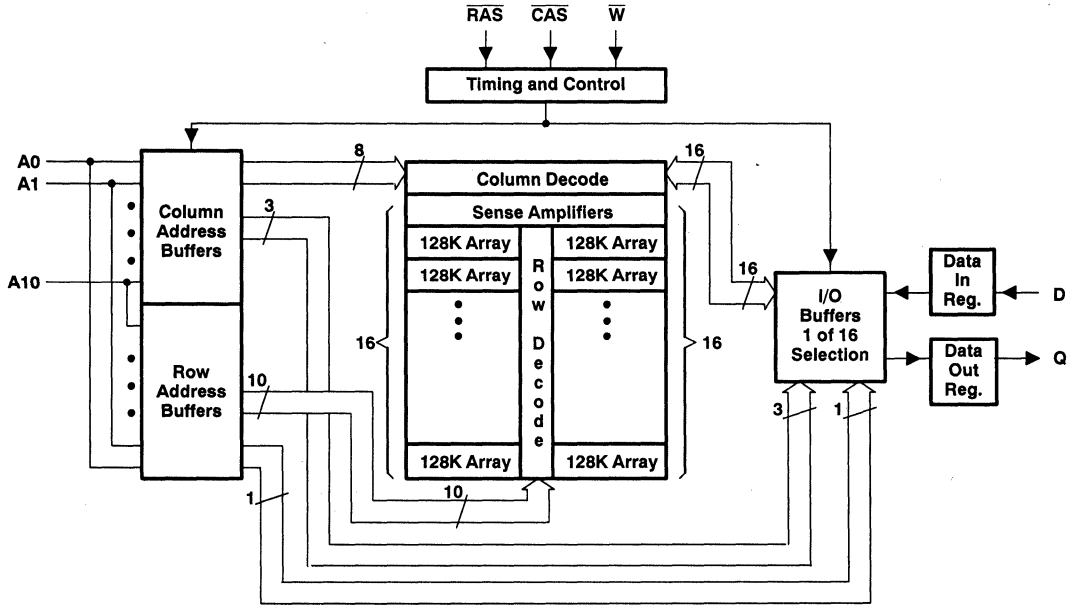
ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package (DJ suffix).

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 0.5 V to 4.6 V
Voltage range on V_{CC} ..... – 0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

ADVANCE INFORMATION

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS46100-70 TMS46100P-70		TMS46100-80 TMS46100P-80		TMS46100-10 TMS46100P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC} 0–0.2		V_{CC} 0–0.2		V_{CC} 0–0.2		V
V_{OL}	Option	I_{OL} = 100 µA			0.2		0.2		0.2	
I_I	Input current (leakage)	V_I = 0 to 3.9 V, V_{CC} = 3.6 V, All other pins =0 to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 3.6 V			60		50		40	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.0 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'46100		500		500		500	µA
			'46100P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 3.6 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			60		50		40	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 3.6 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling			50		45		40	mA
I_{CC6}†	Self-refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA
I_{CC10}†	Battery backup (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			300		300		300	µA

† For TMS46100P only.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS46100-70 TMS46100P-70		TMS46100-80 TMS46100P-80		TMS46100-10 TMS46100P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS46100-70 TMS46100P-70		TMS46100-80 TMS46100P-80		TMS46100-10 TMS46100P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	130		150		180		ns
t_{RWC}	Read-write cycle time	153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	10 000	80	10 000	100	10 000	ns
t_{RASS}	Self-refresh, $\overline{RAS}$ low time	100		100		100		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{RPS}	Self-refresh, RAS high (precharge)	130		150		180		ns
t_{WP}	Write pulse duration	15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 13)	55		60		75		ns
t_{DH}	Data hold time (see Note 10)	15		15		20		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see Note 13)	55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 13)	55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns

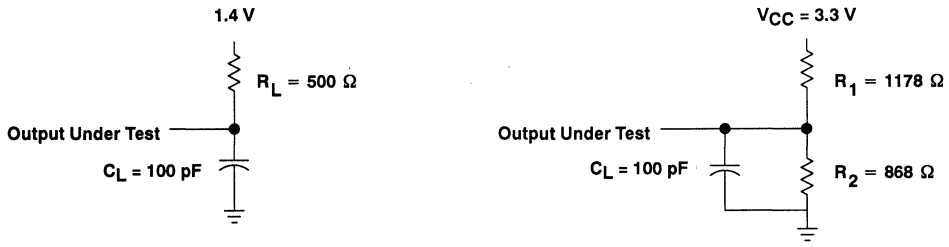
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

			TMS46100-60 TMS46100P-60		TMS46100-70 TMS46100P-70		TMS46100-80 TMS46100P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		ns
t_{CHS}	Self-refresh, $\overline{CAS}$ low hold time after $\overline{RAS}$ high		−50		−50		−50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)		15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)		20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)		70		80		100		ns
t_{TAA}	Access time from address (test mode)		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		75		85		105		ns
t_{REF}	Refresh time interval	'46100		16		16		16	ms
		'46100P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

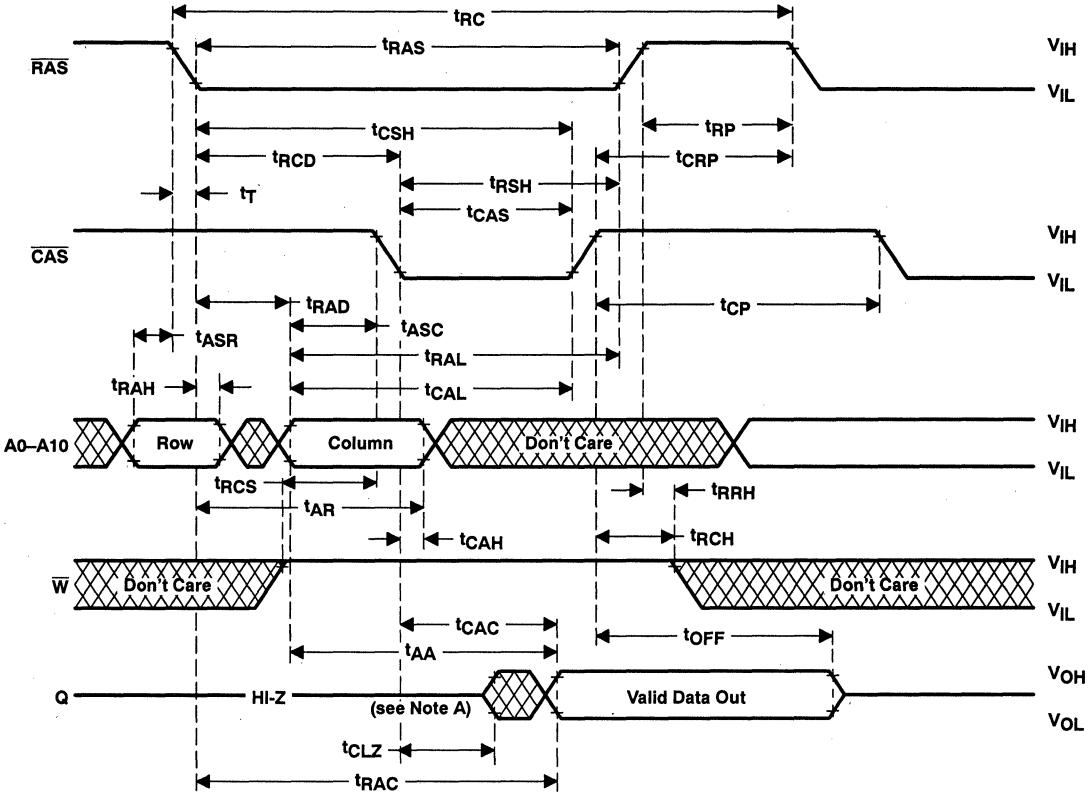


(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

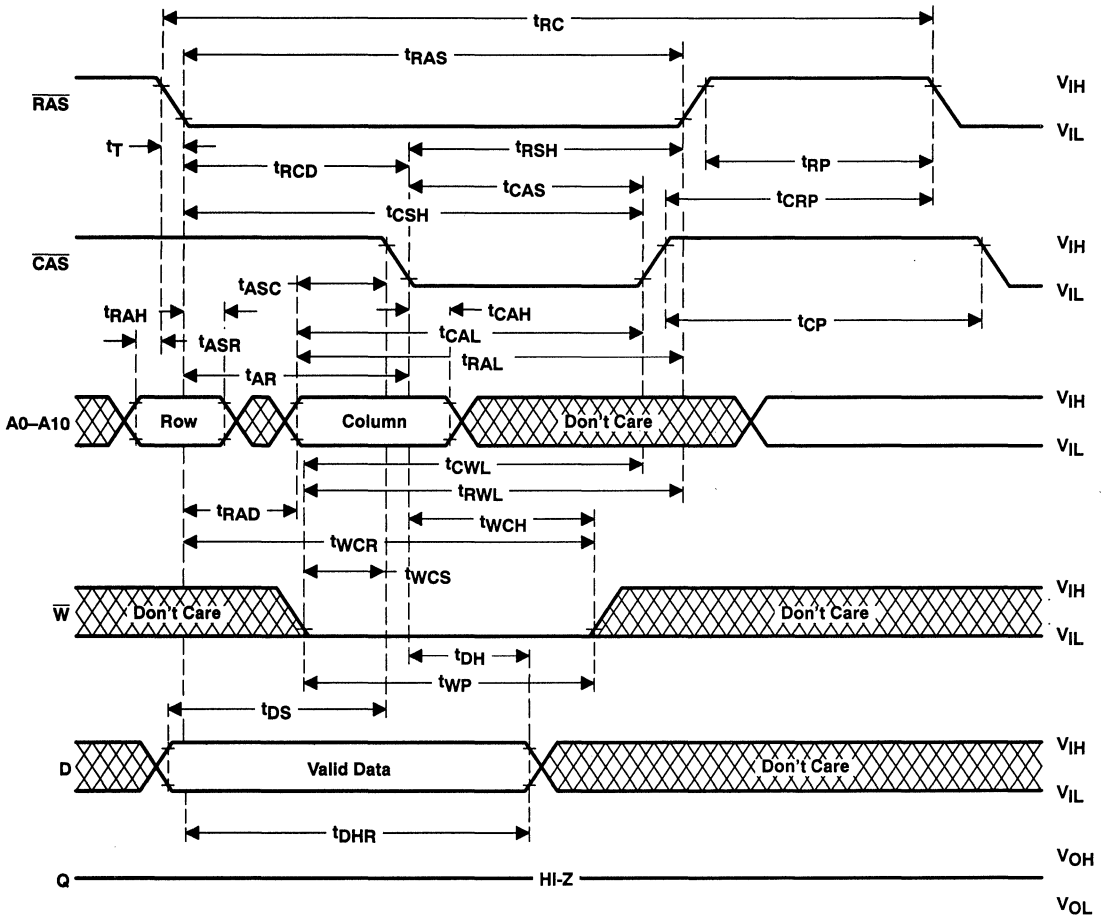


Figure 3. Early Write Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

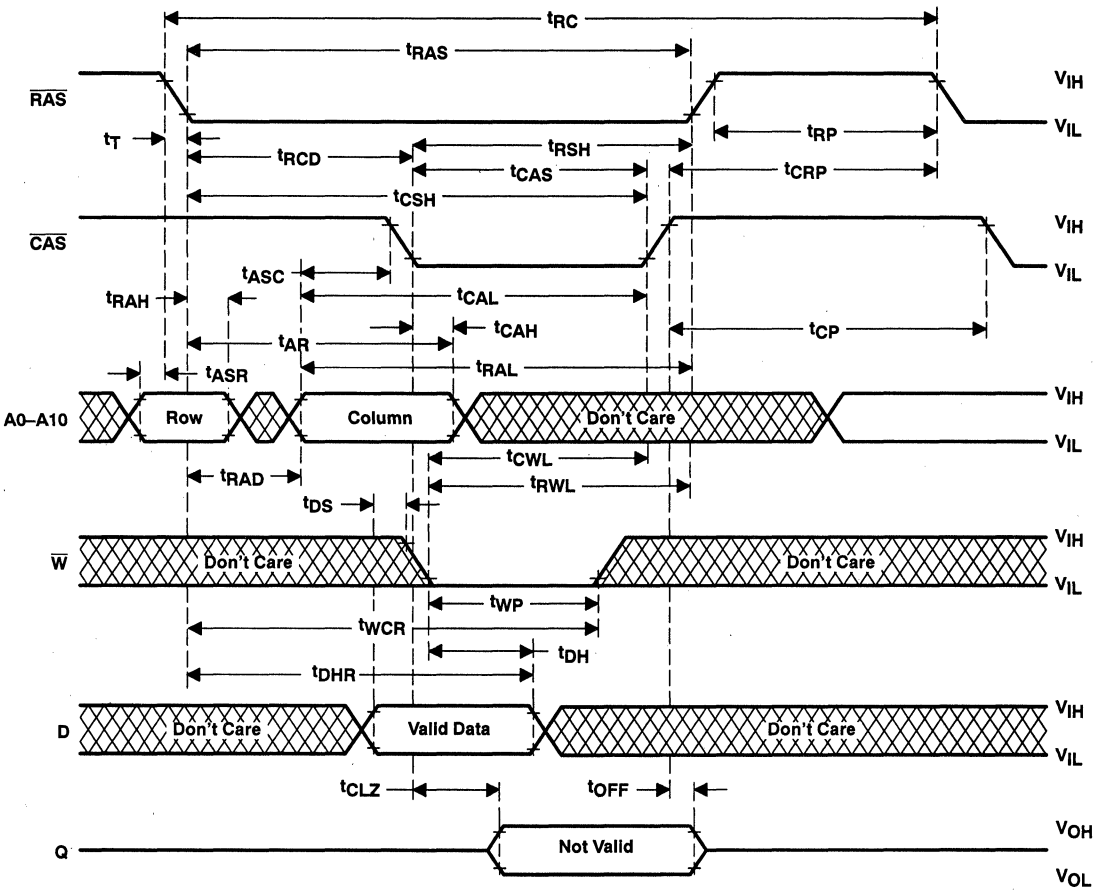
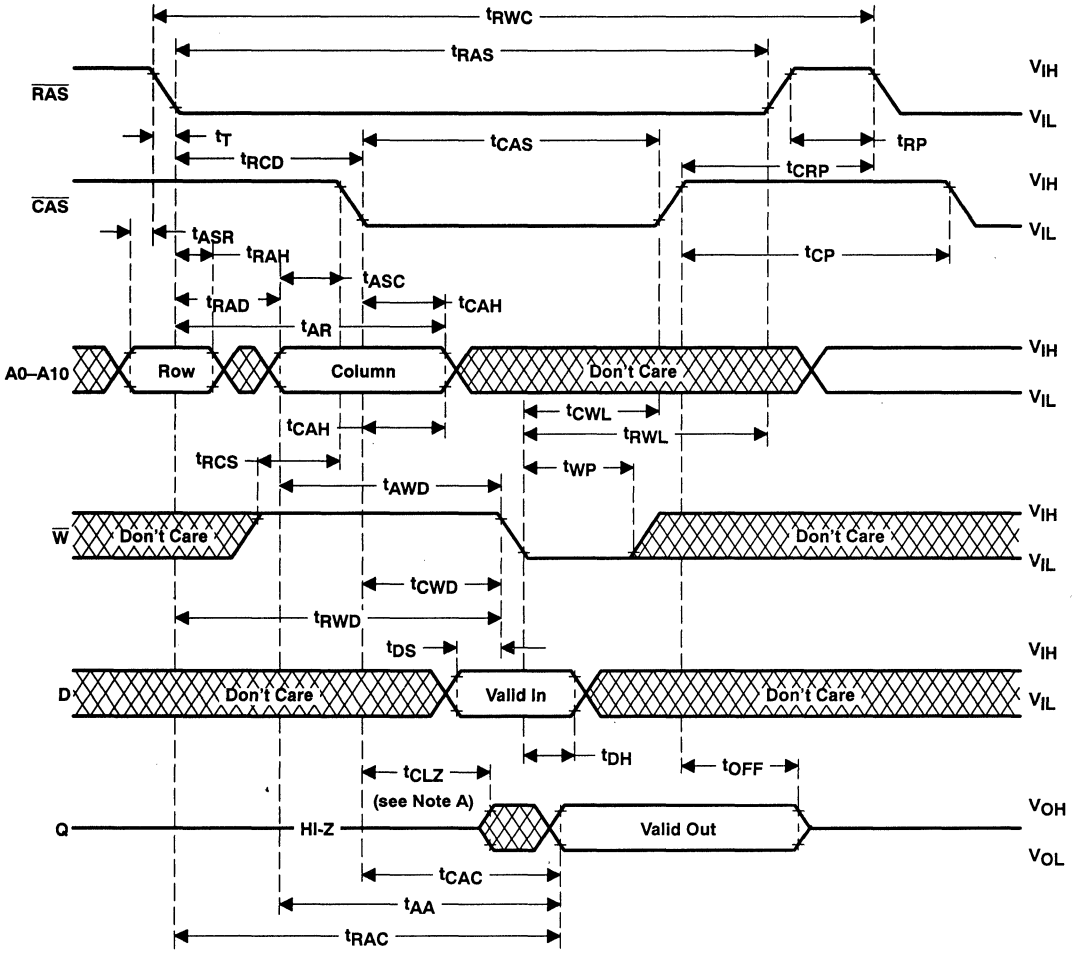


Figure 4. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

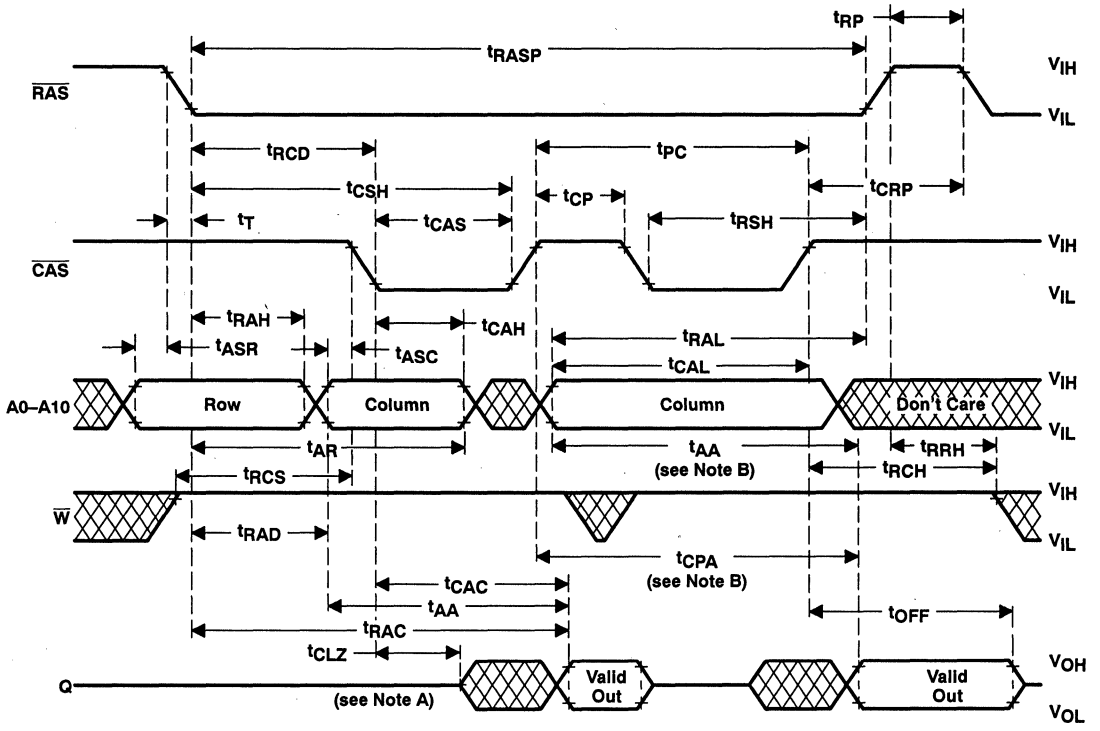


NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

ADVANCE INFORMATION

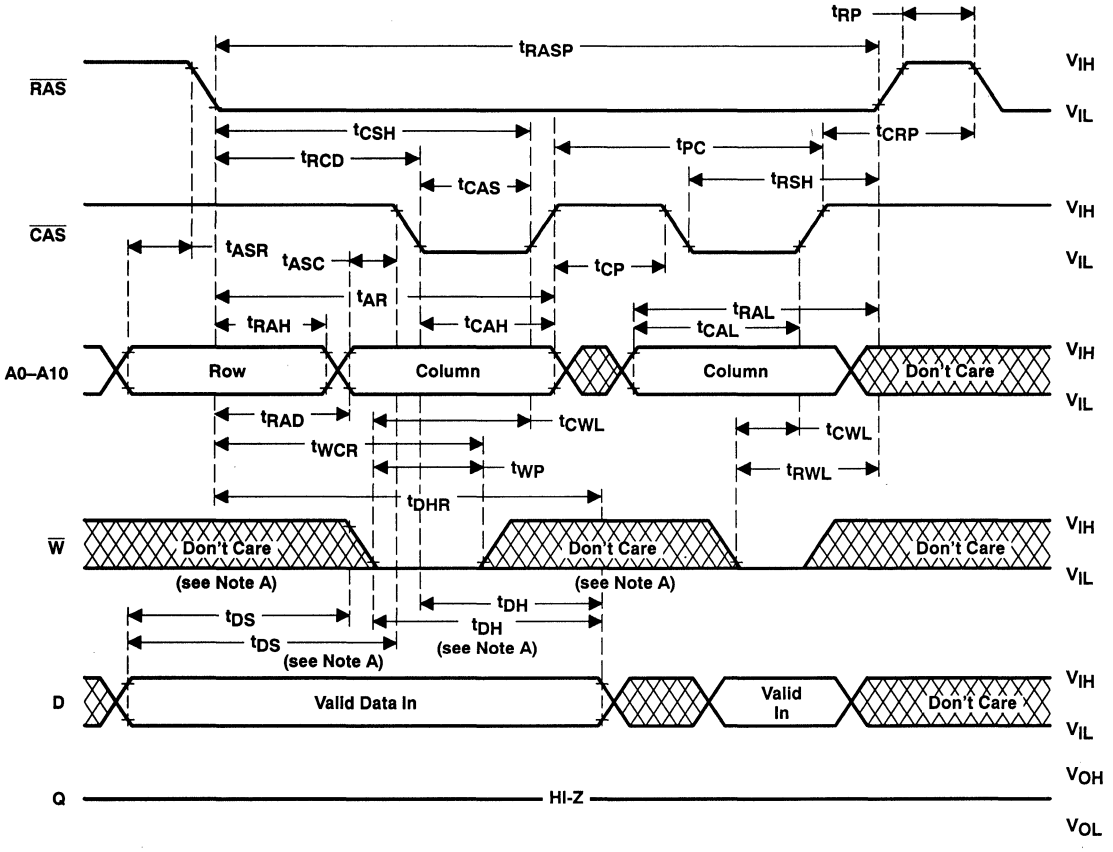
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

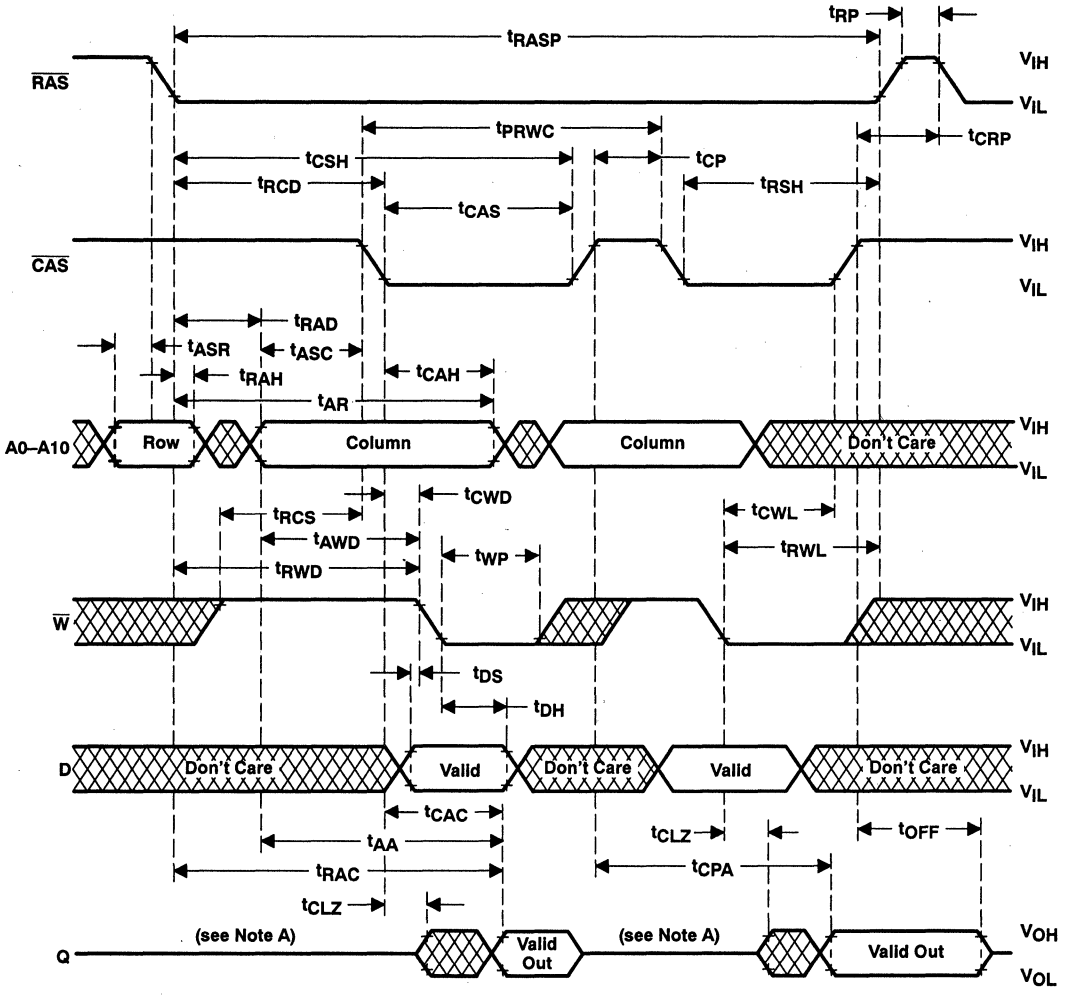


NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

ADVANCE INFORMATION

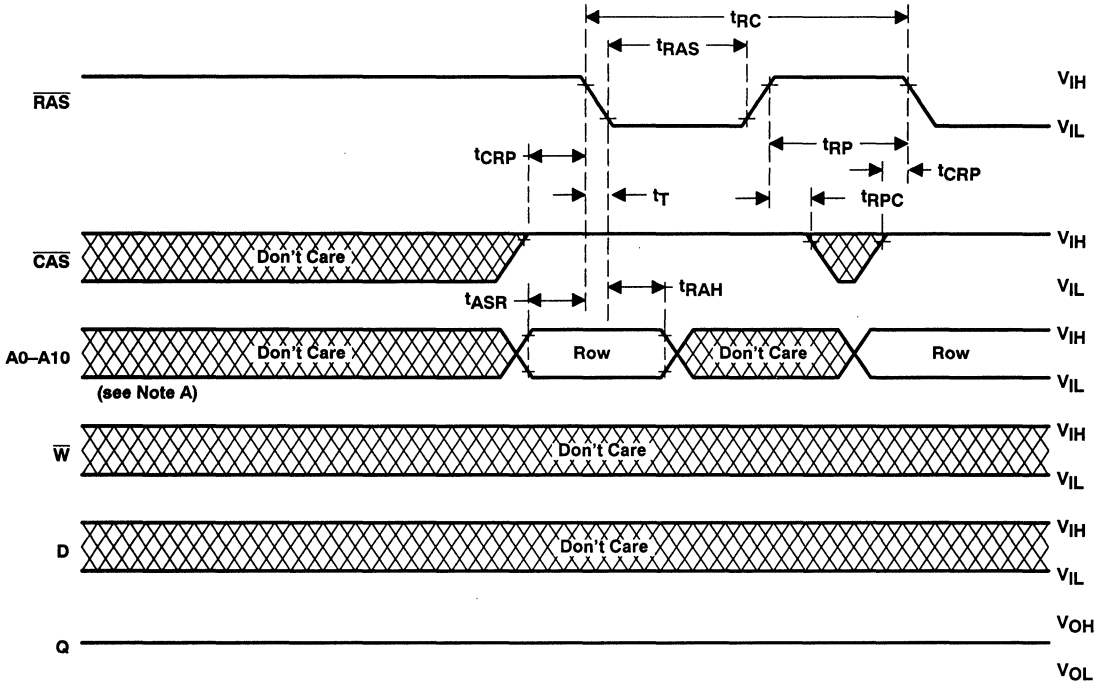
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

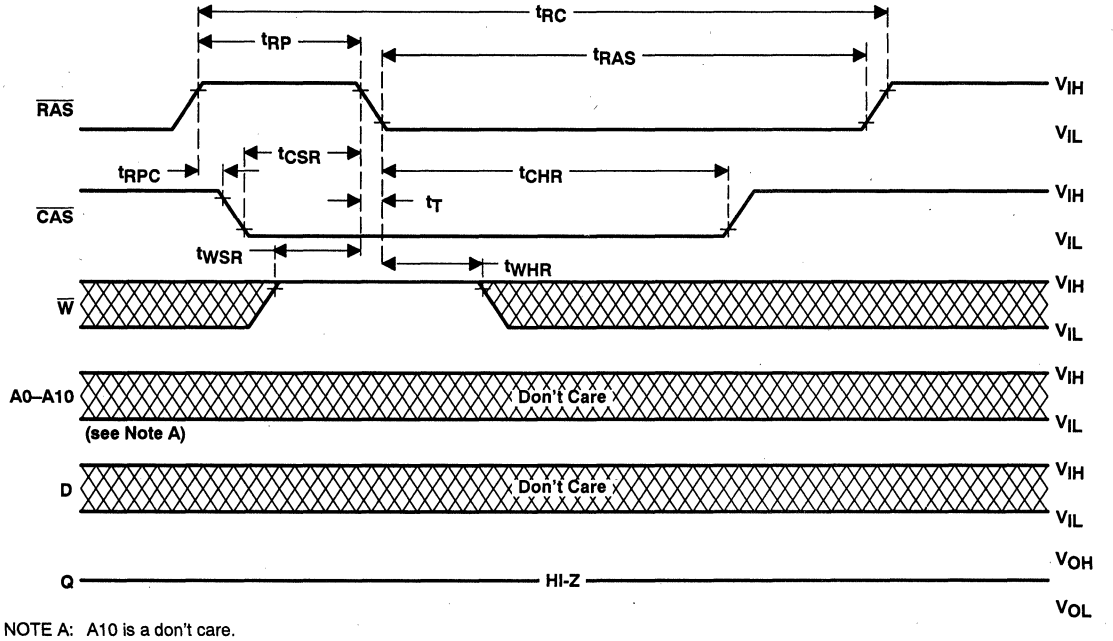


NOTE A: A10 is a don't care.

Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: A10 is a don't care.

Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

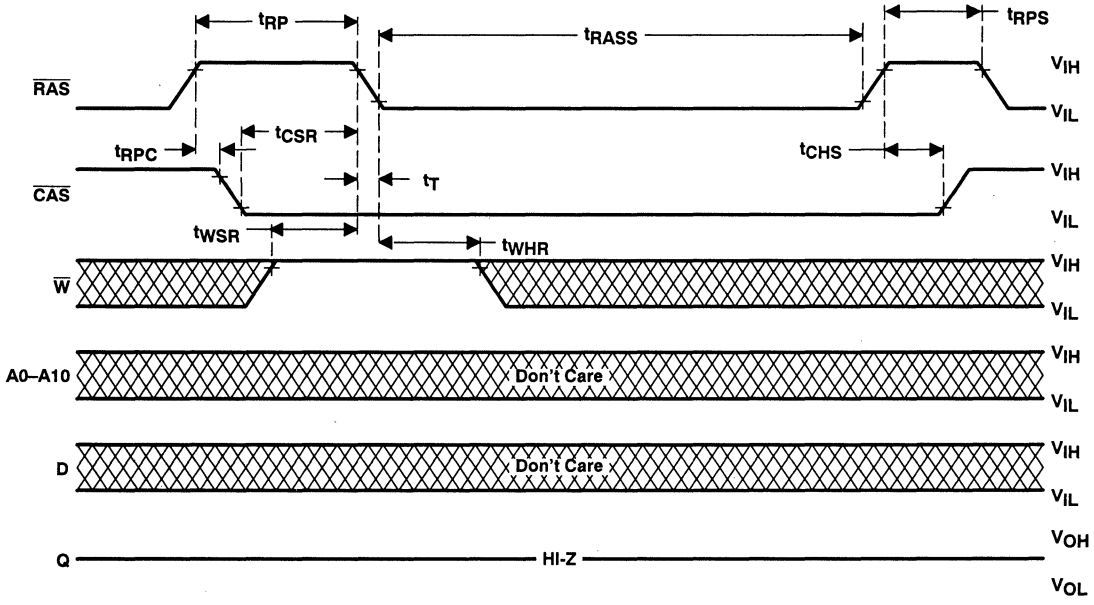


Figure 11. Self Refresh Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

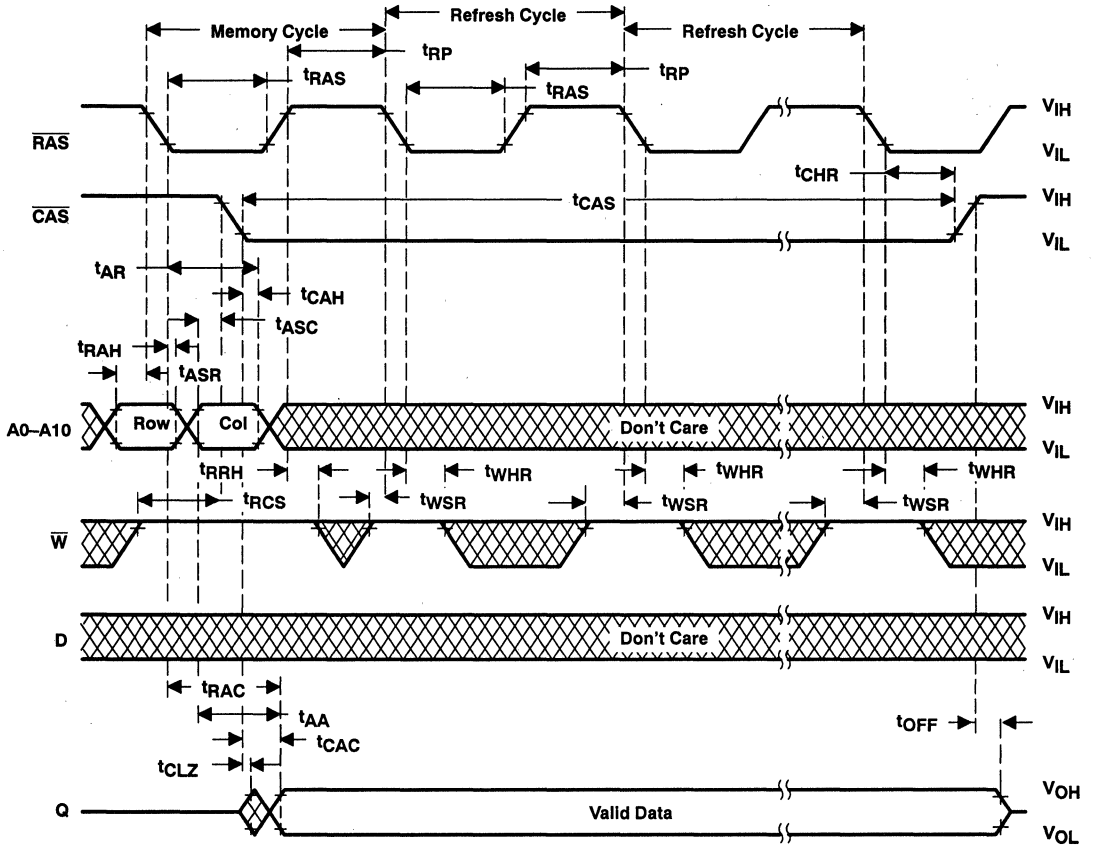


Figure 12. Hidden Refresh Cycle (Read)

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

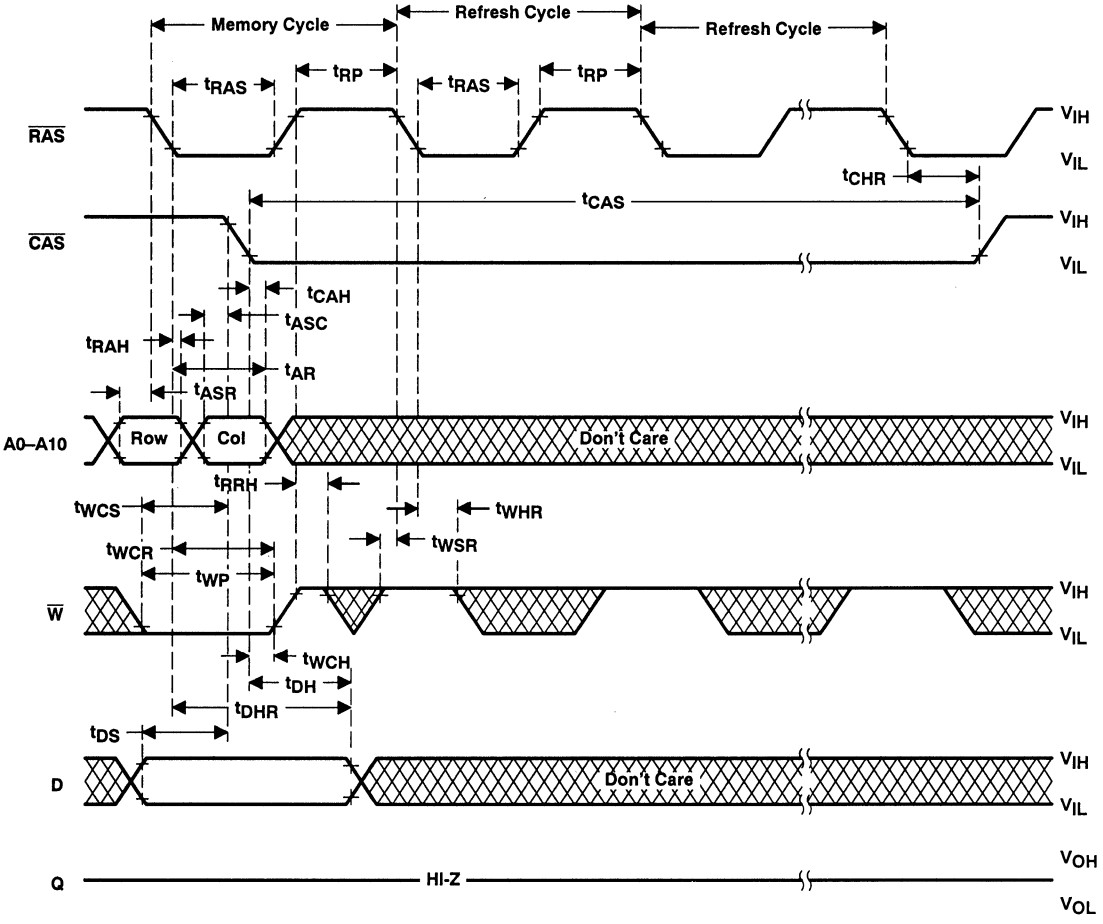


Figure 13. Hidden Refresh Cycle (Write) Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

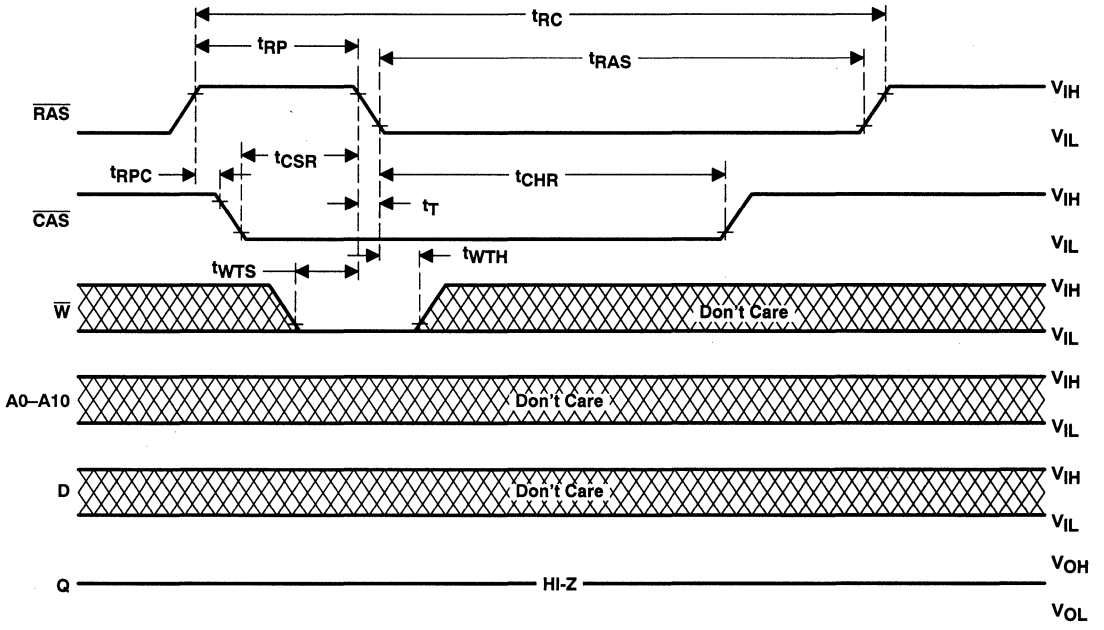
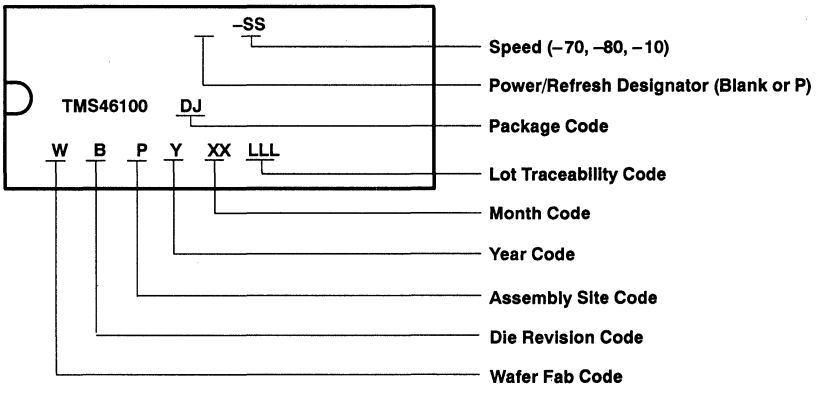


Figure 14. Test Mode Entry Cycle

device symbolization



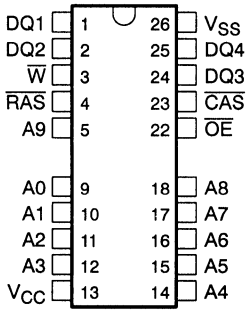
ADVANCE INFORMATION

- **Organization . . . 1 048 576 × 4**
- **Single 3.3-V Power Supply (±0.3-V Tolerance)**
- **Low Power Dissipation (TMS46400P)**
  - **200 μA CMOS Standby**
  - **200 μA Self-Refresh**
  - **300 μA Extended Refresh Battery Backup**
- **Performance Ranges:**

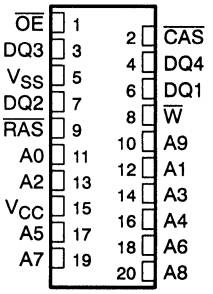
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS46400/P-70	70 ns	18 ns	35 ns	130 ns
TMS46400/P-80	80 ns	20 ns	40 ns	150 ns
TMS46400/P-10	100 ns	25 ns	50 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **1024-Cycle Refresh in 16 ms**
  - **128 ms for Extended-Refresh Version (TMS46400P)**
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 300-Mil 20/26-Lead Surface Mount (SOJ) Package, 20-Pin Zig-Zag In-line (ZIP) Package, 20/26-Lead Thin Small Outline Package, and Reverse Thin Small Outline Package**
- **Operating Free-Air Temperature Range 0°C to 70°C**

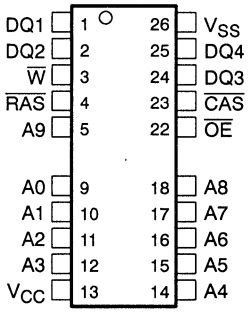
DJ PACKAGE† (TOP VIEW)



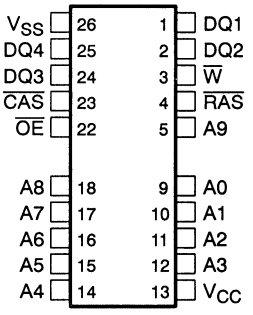
SD PACKAGE† (TOP VIEW)



DGA PACKAGE† (TOP VIEW)



DGB PACKAGE† (TOP VIEW)



†The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS46400 series are high-speed, low-voltage 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of one bit each.

The TMS46400P series are high-speed, self-refresh and extended-refresh, low-voltage 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each.

Both series employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 180 mW operating, 0.72 mW standby, and 1.1 mW battery backup for an 80-ns device.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS46400 and TMS46400P are offered in a 300-mil 20/26-lead plastic surface mount SOJ package (DJ suffix), a 20-pin zig-zag in-line package (SD suffix), a 20/26-lead plastic small outline package (DGA suffix), and a 20/26-lead plastic small outline package, reverse form (DGB suffix). All packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS46400 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 through A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. They will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS46400P) to retain data. This can be achieved by strobing each of the 1024 rows (A0-A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS46400P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs, while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

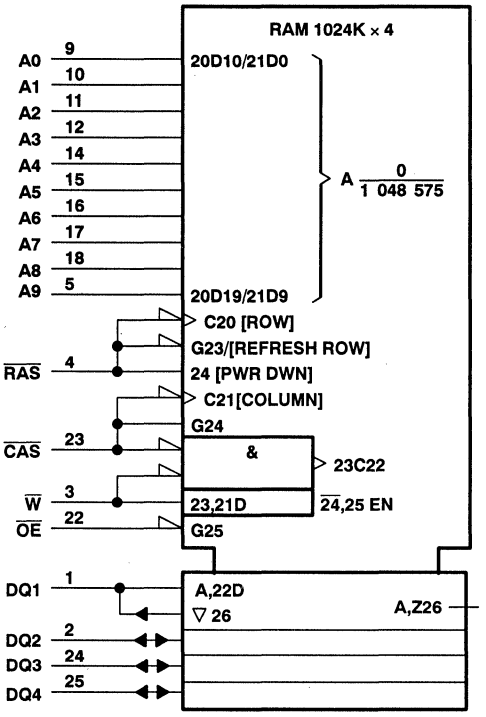
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

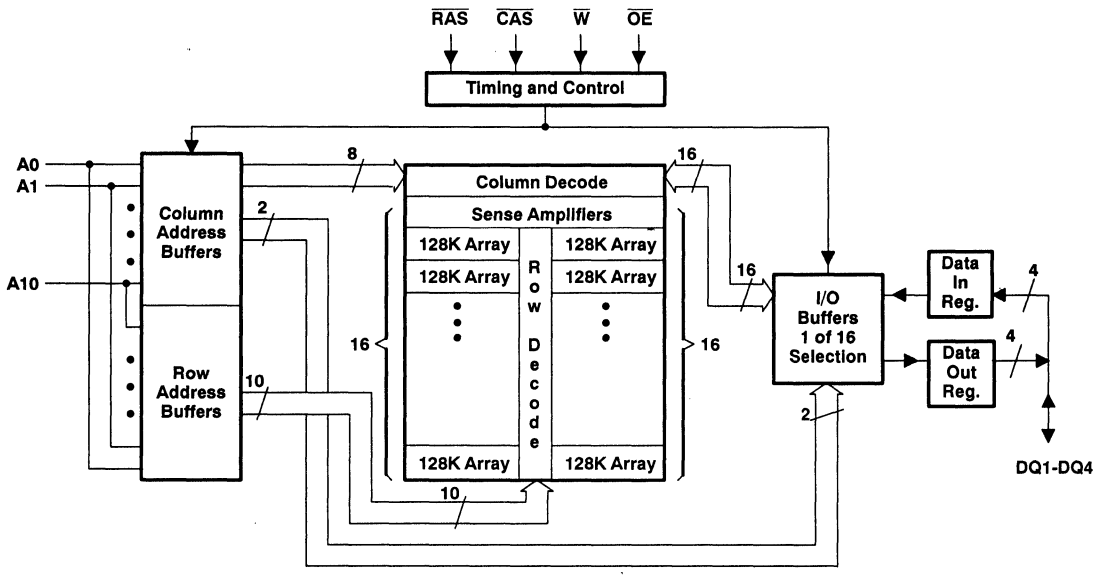
A Design For Test (DFT) mode is incorporated in the TMS46400 and TMS46400P. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different, a DQ pin will go low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1-megabit × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package (DJ suffix).

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 0.5 V to 4.6 V
Voltage range on V_{CC} ..... – 0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS46400-70 TMS46400P-70		TMS46400-80 TMS46400P-80		TMS46400-10 TMS46400P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		V
V_{OL}	Option	I_{OL} = 100 µA			0.2		0.2		0.2	
I_I	Input current (leakage)	V_I = 0 to 3.9 V, V_{CC} = 3.6 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 3.6 V			70		60		50	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'46400		500		500		500	µA
			'46400P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 3.6 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 3.6 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}†	Self-refresh current	$\overline{CAS}$< 0.2 V, $\overline{RAS}$< 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA
I_{CC10}†	Battery backup (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			300		300		300	µA

† For TMS46400P only.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS46400-70 TMS46400P-70		TMS46400-80 TMS46400P-80		TMS46400-10 TMS46400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS46400-70 TMS46400P-70		TMS46400-80 TMS46400P-80		TMS46400-10 TMS46400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	130		150		180		ns
t_{RWC}	Read-write cycle time	181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	10 000	80	10 000	100	10 000	ns
t_{RASS}	Self-refresh, $\overline{RAS}$ low time		100		100		100	µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{RPS}	$\overline{RAS}$ precharge after self-refresh	130		150		180		ns
t_{WP}	Write pulse duration	15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	18		20		25		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	18		20		25		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	55		60		75		ns
t_{DH}	Data hold time (see Note 11)	15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	55		60		75		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		20		20		ns

Continued next page.

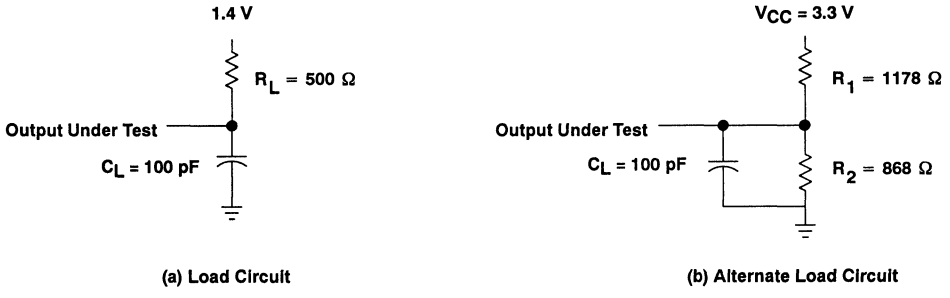
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

			TMS46400-70 TMS46400P-70		TMS46400-80 TMS46400P-80		TMS46400-10 TMS46400P-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		ns
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)		−50		−50		−50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)		15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)		20	52	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)		98		110		135		ns
t_{TAA}	Access time from address (test mode)		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		75		85		105		ns
t_{REF}	Refresh time interval	'46400		16		16		16	ms
		'46400P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit

(b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

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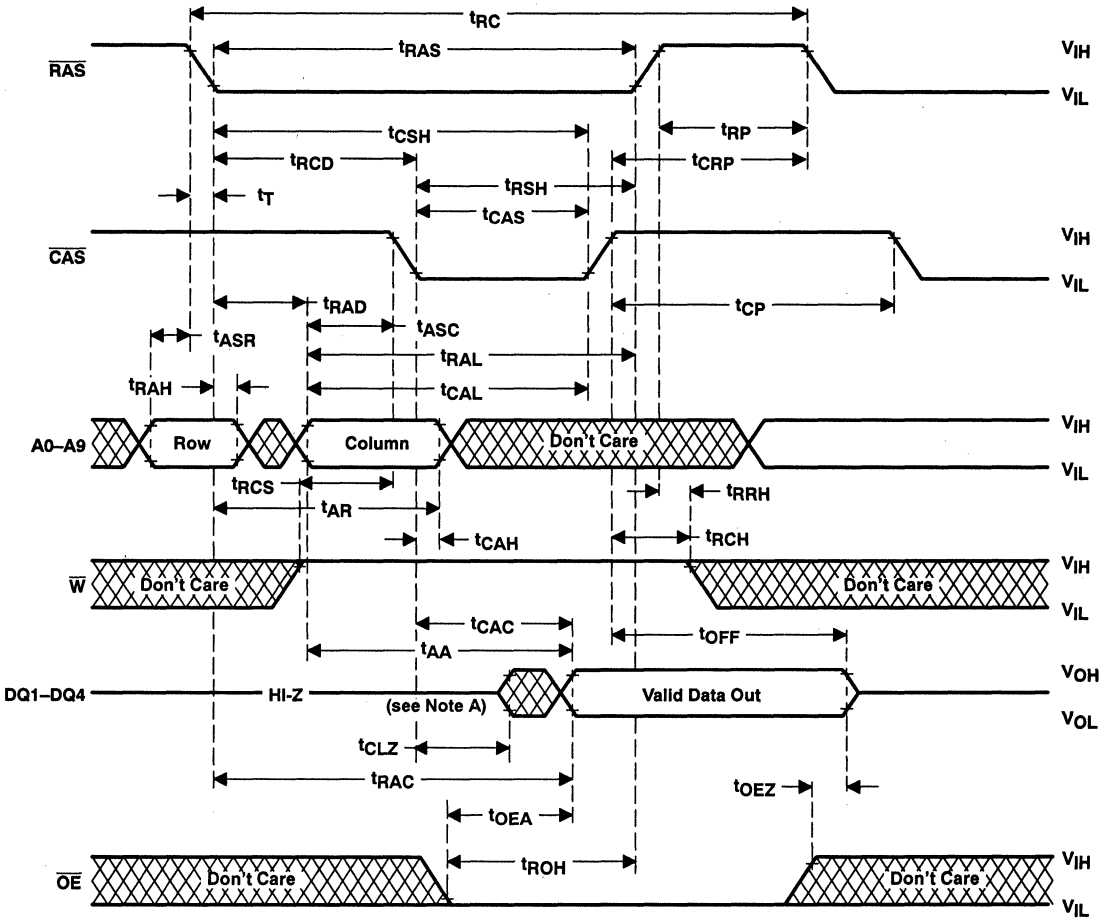

NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

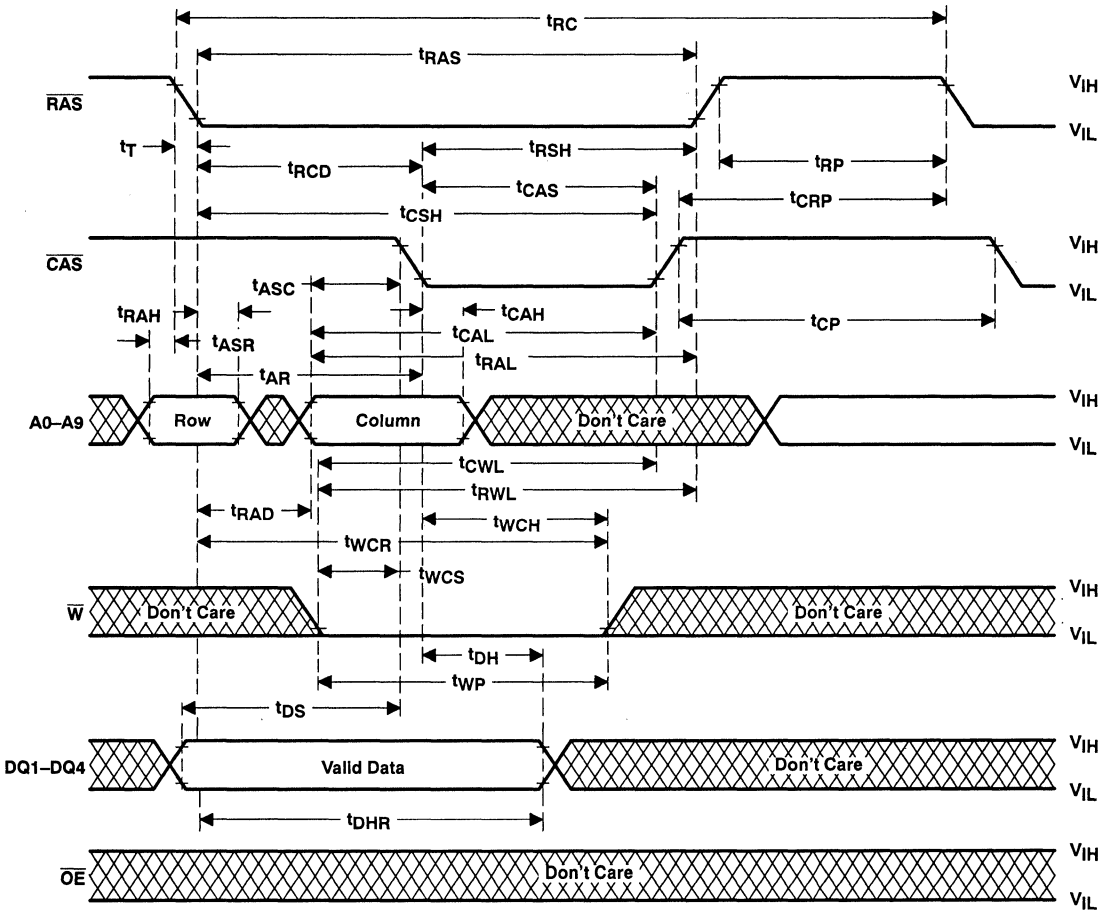

Figure 3. Early Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

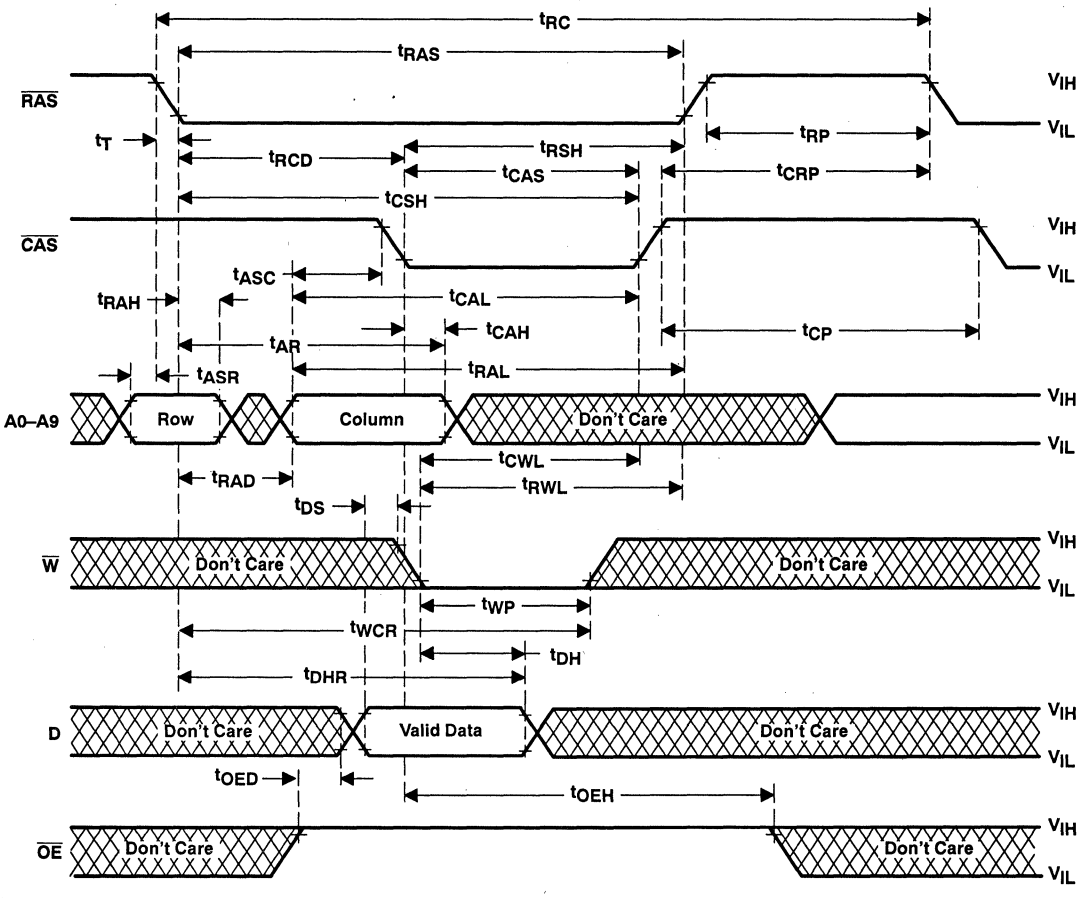
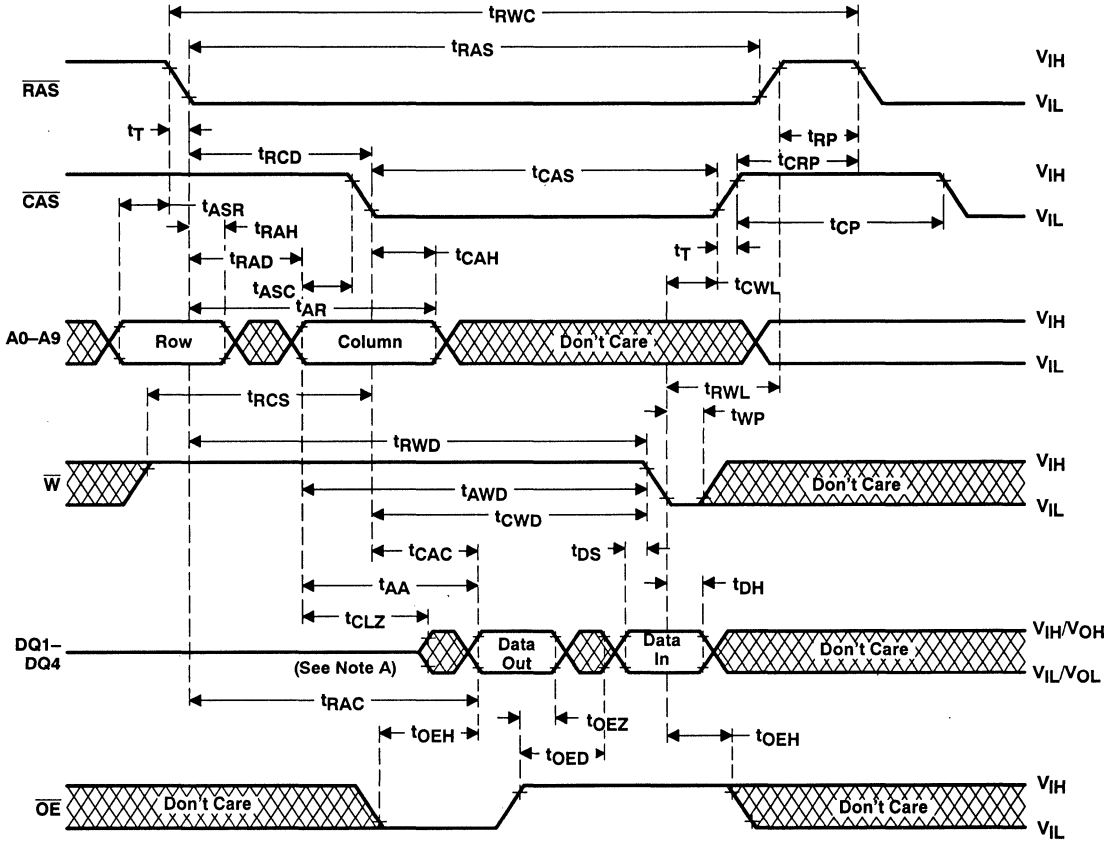


Figure 4. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

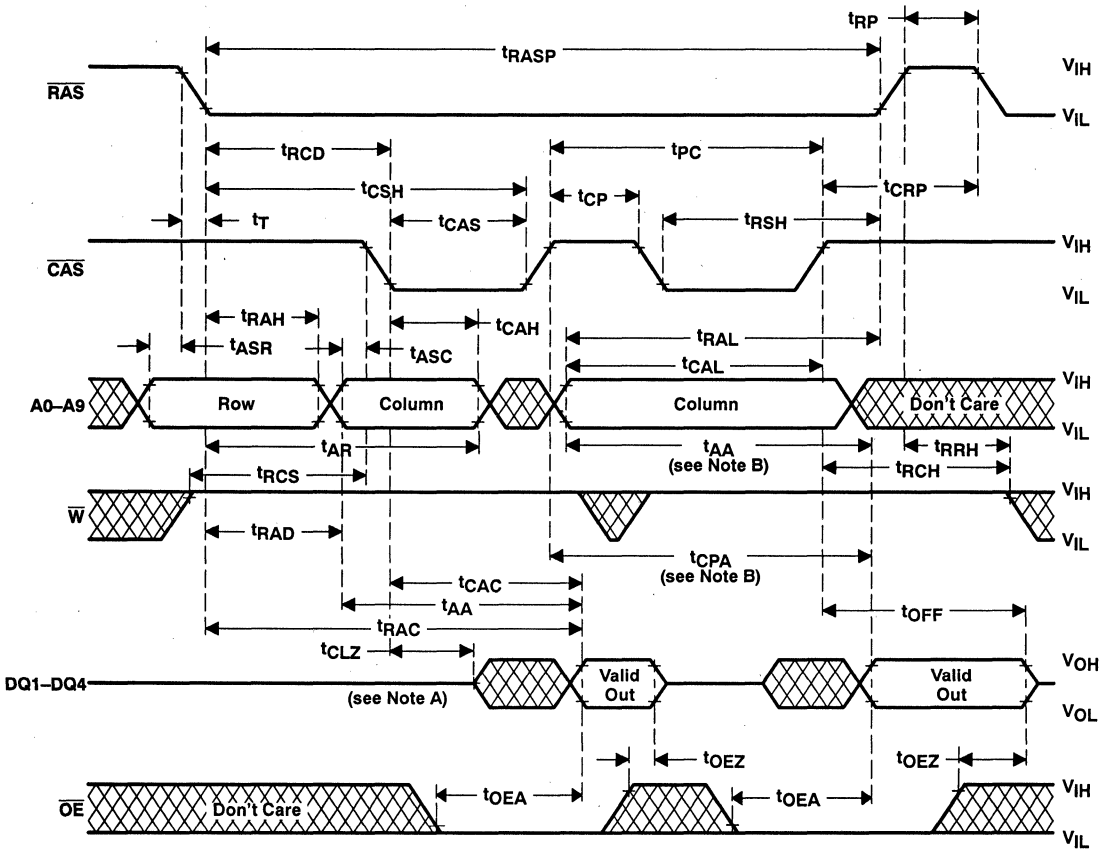


NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

ADVANCE INFORMATION

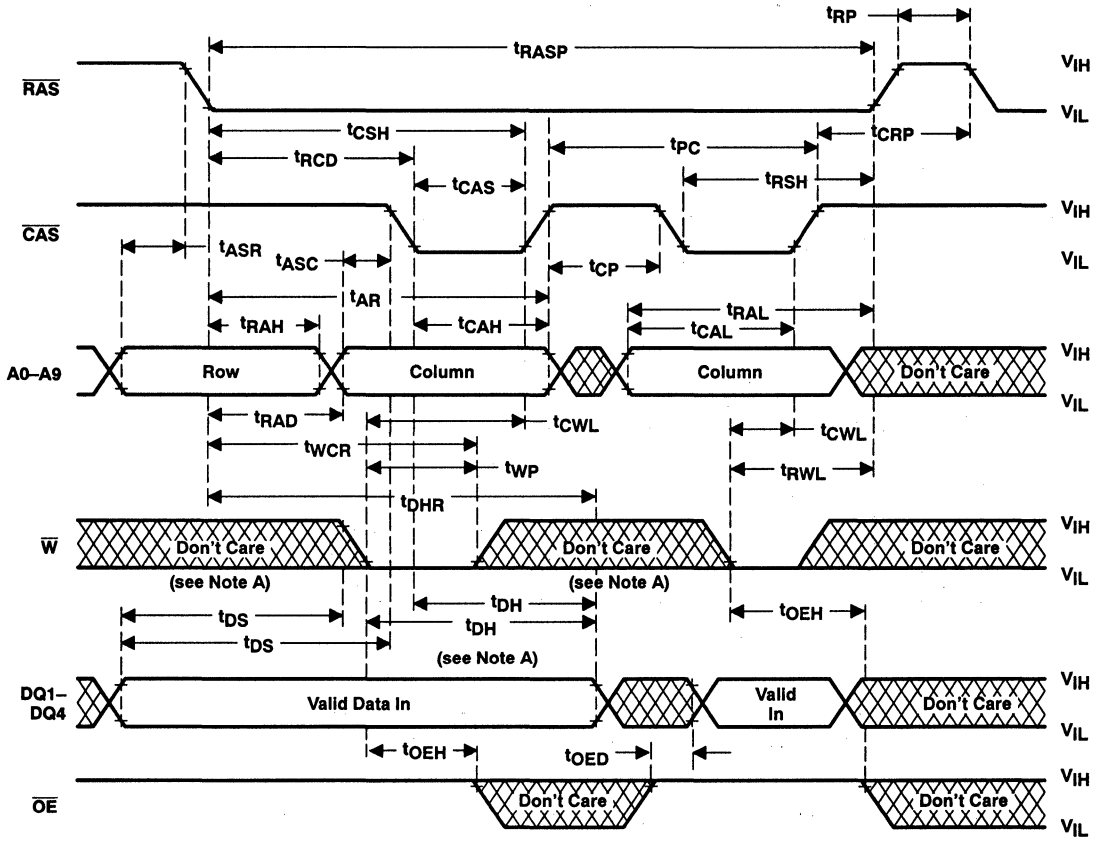
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

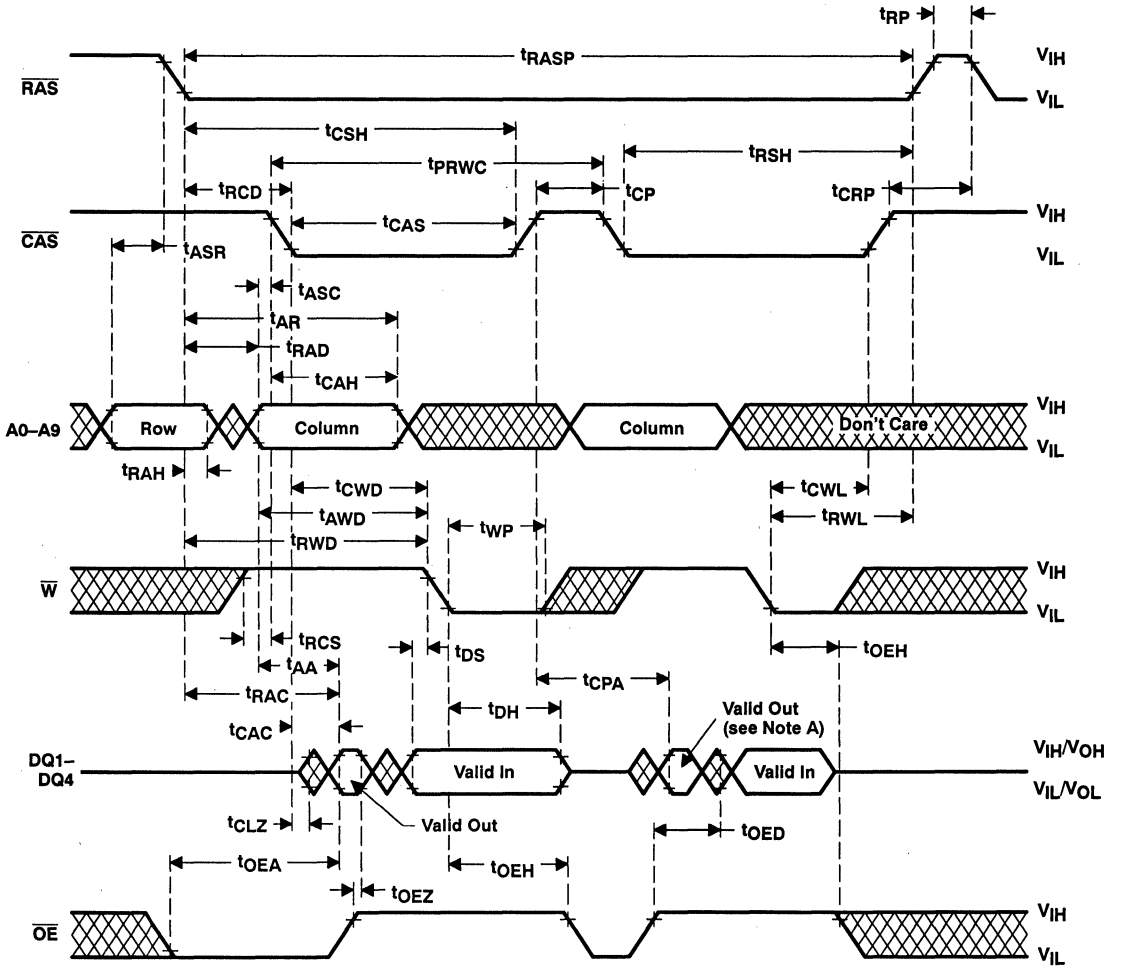


NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

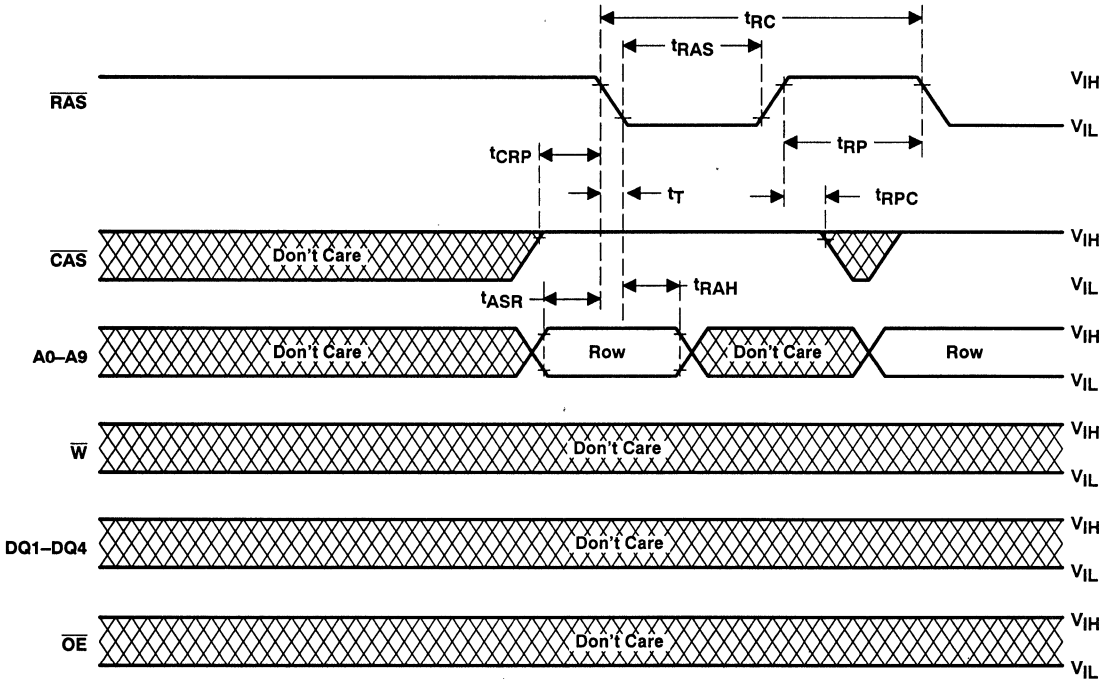


Figure 9. $\overline{RAS}$-Only Refresh Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

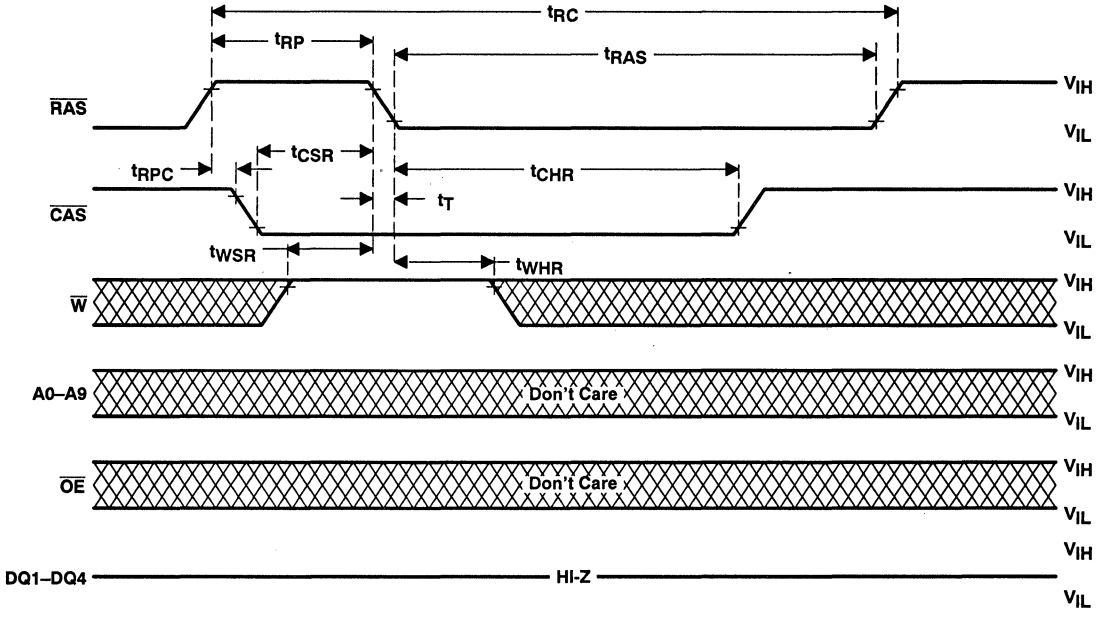


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

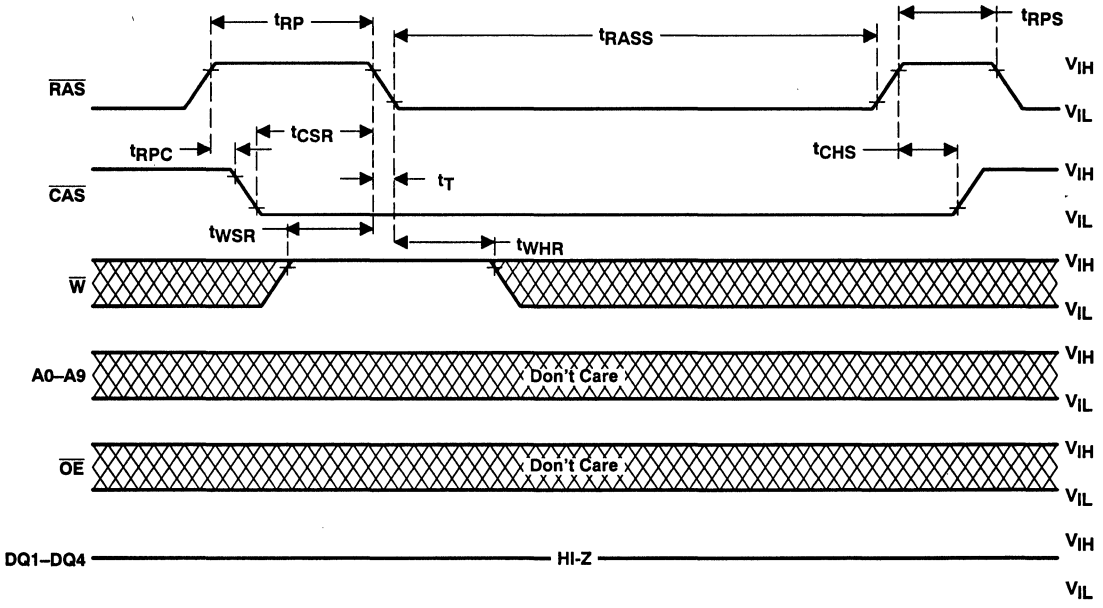


Figure 11. Self Refresh Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

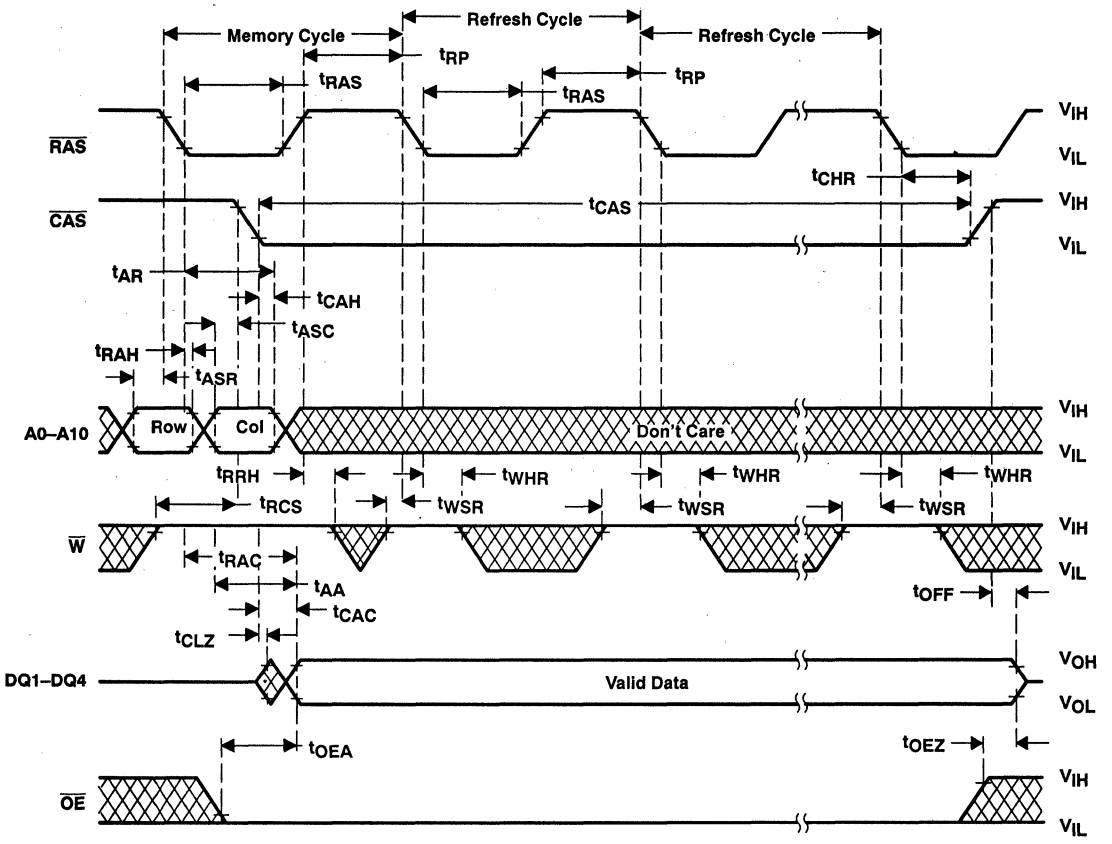


Figure 12. Hidden Refresh Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

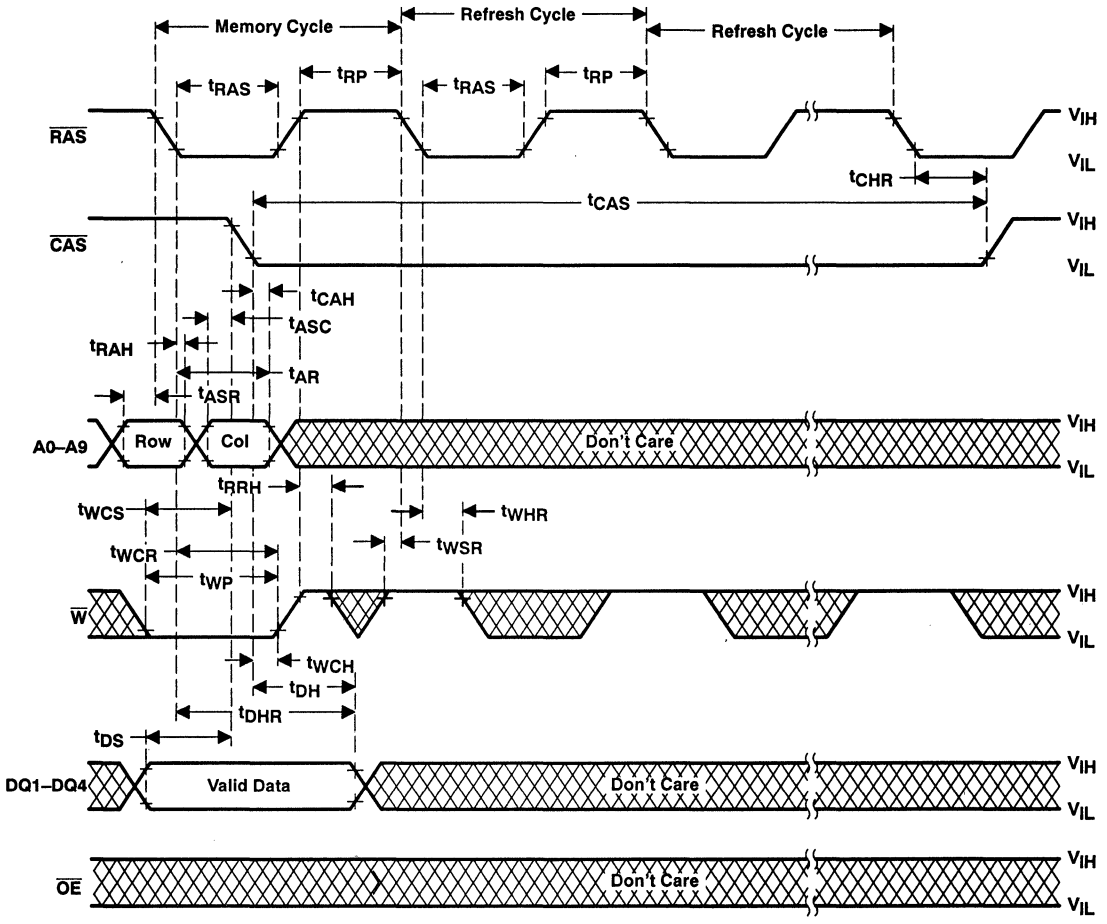


Figure 13. Hidden Refresh Cycle (Write) Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

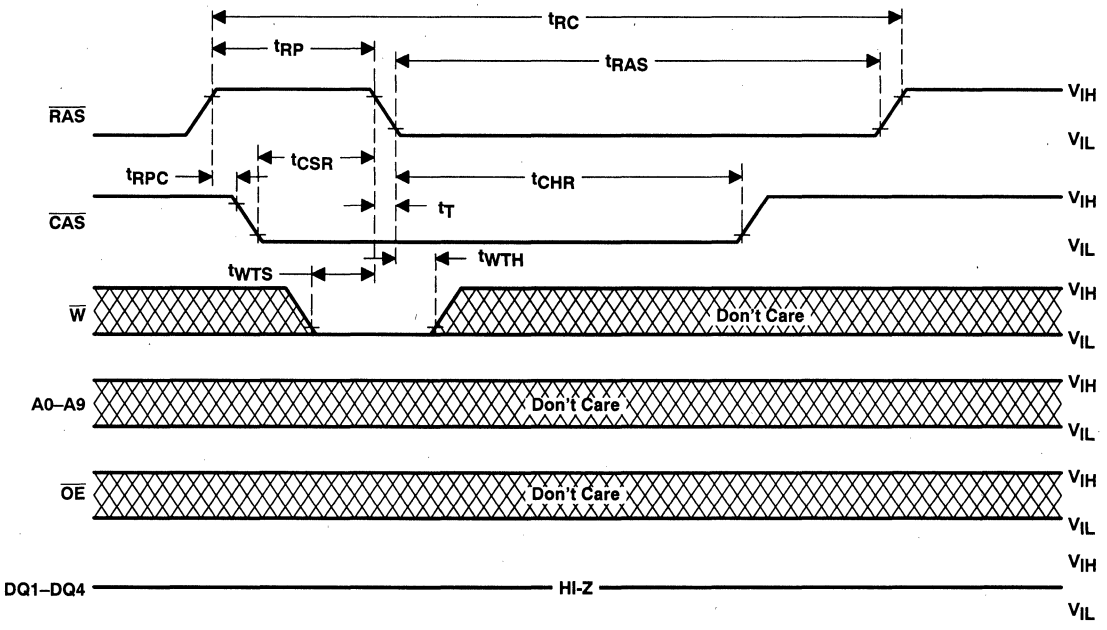
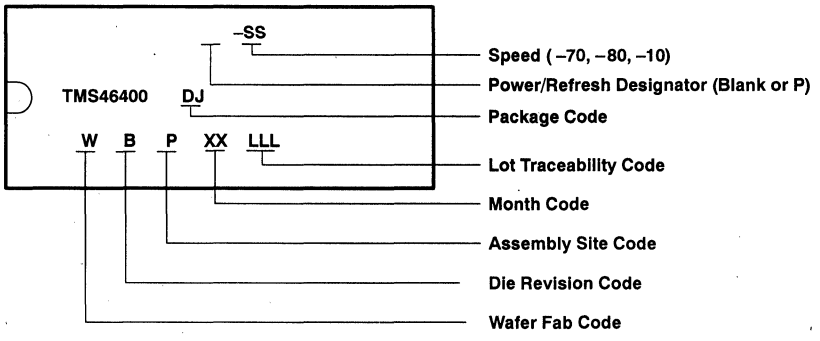


Figure 14. Test Mode Entry Cycle

device symbolization



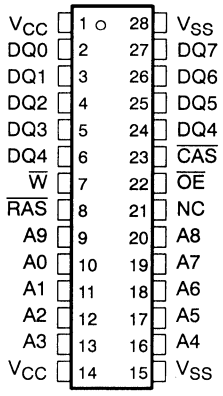
This data sheet is applicable to all TMS44800/Ps symbolized with Revision "B" and subsequent revisions as described on page 22.

- **Organization . . . 524 288 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'44800/P-60	60 ns	15 ns	30 ns	110 ns
'44800/P-70	70 ns	20 ns	35 ns	130 ns
'44800/P-80	80 ns	20 ns	40 ns	150 ns
'44800/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  1024-Cycle Refresh in 16 ms (Max)
  128 ms for Low Power With Self-Refresh Version (TMS44800P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 28-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 28-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low-Power With Self-Refresh Version**

DZ AND DGC PACKAGES†
(TOP VIEW)



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44800 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 524 288 words of eight bits each.

The TMS44800P series are high-speed, low-power with self-refresh, 4 194 304-bit dynamic random-access memories, organized as 524 288 words of eight bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 495 mW operating and 11 mW standby on 100-ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS44800 and TMS44800P series are offered in a 400-mil 28-lead plastic surface mount SOJ package (DZ suffix) and a 28-lead plastic surface mount TSOP package (DGC suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44800 and TMS44800P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Nineteen address bits are required to decode 1 of 524 288 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ0–DQ7)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. They will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS44800P) to retain data. This can be achieved by strobing each of the1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS44800P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

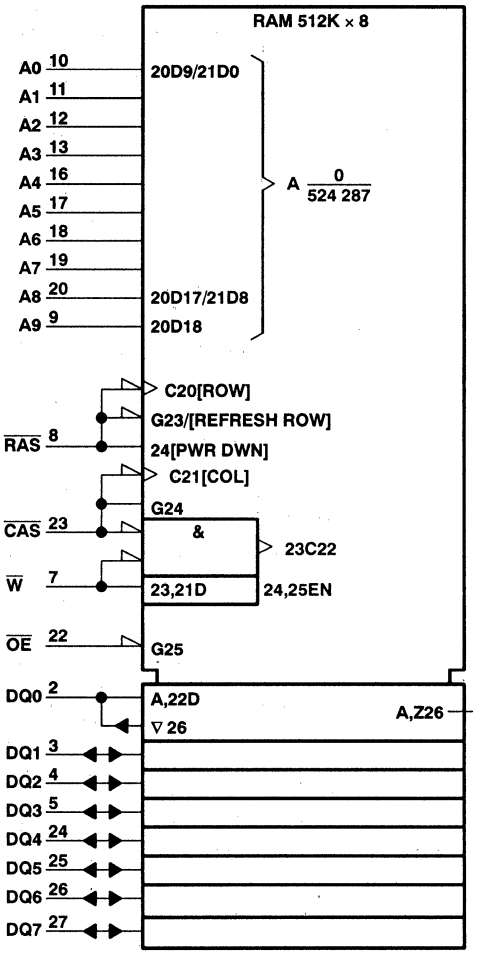
self refresh (TMS44800P)

The self refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

power up

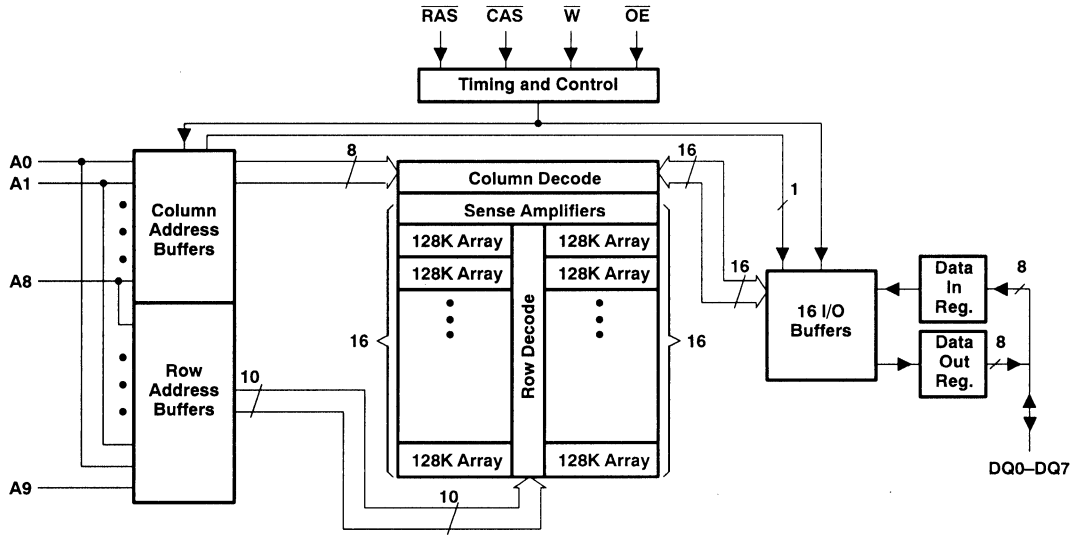
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Supply voltage range on V_{CC} . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'44800-60 '44800P-60		'44800-70 '44800P-70		'44800-80 '44800P-80		'44800-10 '44800P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			120		110		100		90	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'44800		1		1		1		1	mA
			'44800P		200		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			120		110		100		90	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			120		110		100		90	mA
I_{CC5}‡	Battery backup operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			300		300		300		300	µA
I_{CC6}†‡	Self refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			200		200		200		200	µA

† Measured with outputs open.
‡ For TMS44800P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'44800-60 '44800P-60		'44800-70 '44800P-70		'44800-80 '44800P-80		'44800-10 '44800P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		20		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		20		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	20	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	20	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'44800-60 '44800P-60		'44800-70 '44800P-70		'44800-80 '44800P-80		'44800-10 '44800P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-modify-write cycle time	155		185		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		90		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	20	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		20		20		25		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		20		20		25		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'44800-60 '44800P-60		'44800-70 '44800P-70		'44800-80 '44800P-80		'44800-10 '44800P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	30		35		35		45		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	30		35		35		45		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	10		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	30		35		35		45		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-modify-write operation only)	55		65		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	40		50		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		20		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		20		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	50	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	85		100		110		135		ns

NOTES: 11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or T_{RCH} must be satisfied for a read cycle.
14. The maximum value is specified only to assure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'44800-60 '44800P-60		'44800-70 '44800P-70		'44800-80 '44800P-80		'44800-10 '44800P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		0		ns
t_{RAS}	$\overline{RAS}$ precharge after self refresh	110		130		150		180		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high	−50		−50		−50		−50		ns
t_{REF}	Refresh time interval (TMS44800 only)		16		16		16		16	ms
t_{REF}	Refresh time interval, Low power (TMS44800P only)		128		128		128		128	ms
t_T	Transition time	2	50	2	50	2	50	2	50	ns

PARAMETER MEASUREMENT INFORMATION

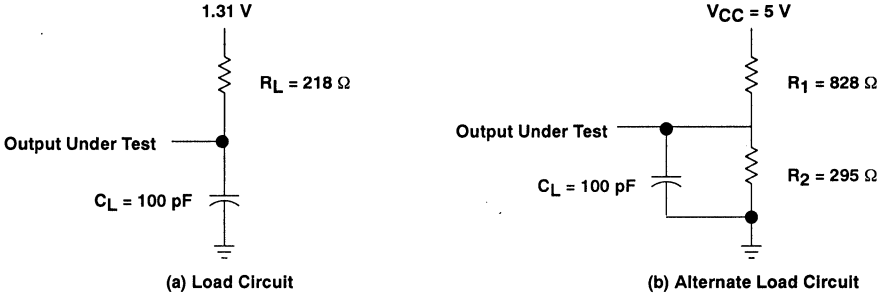
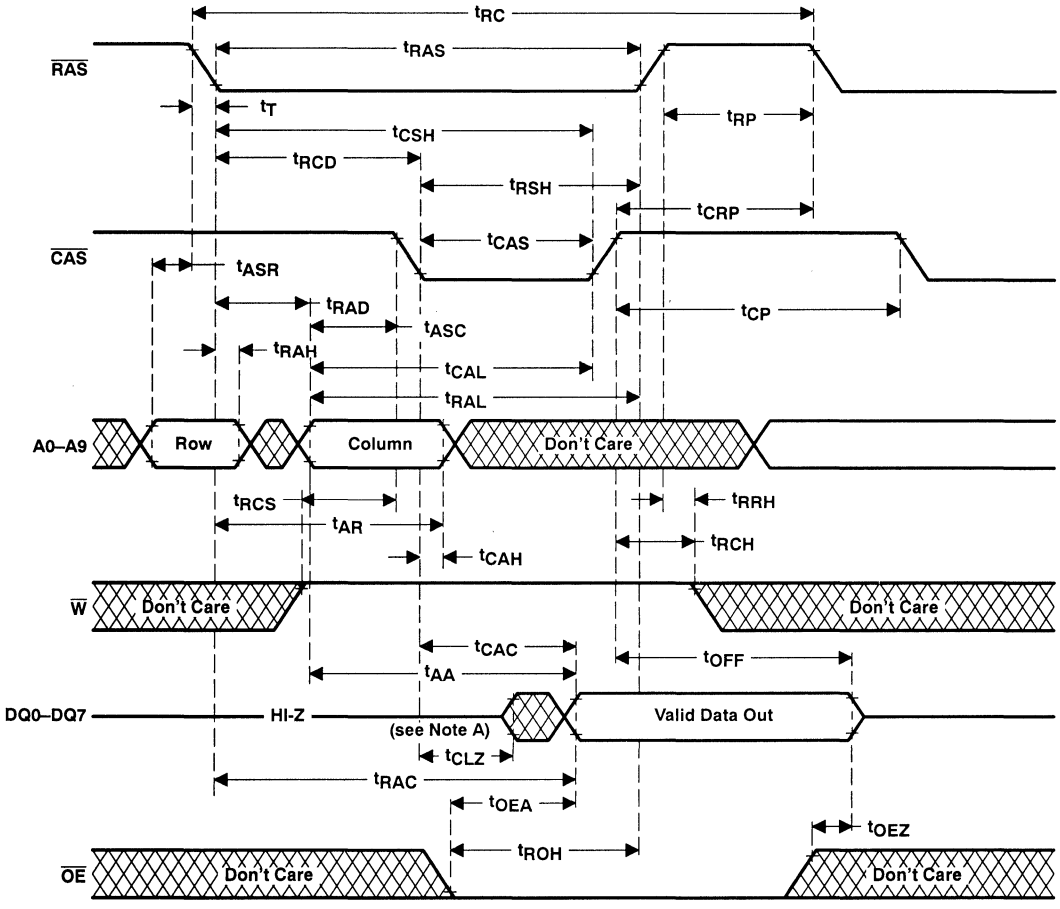


Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

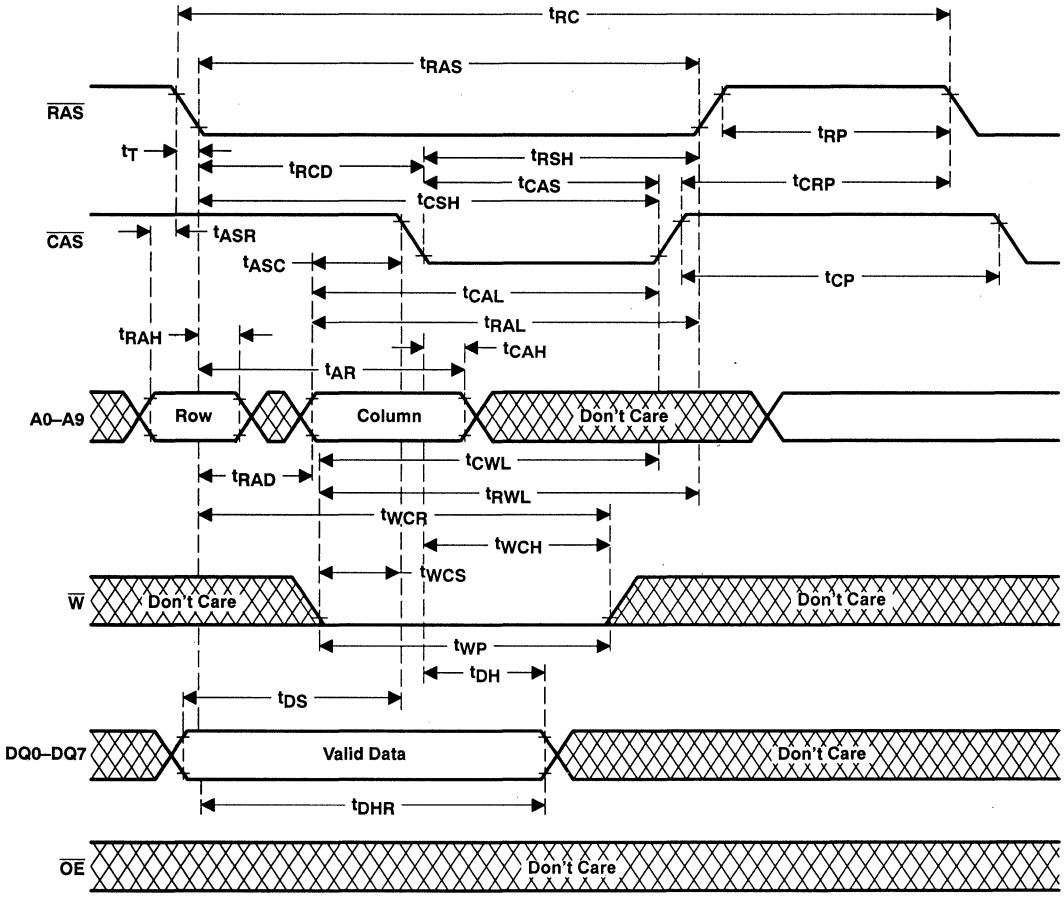
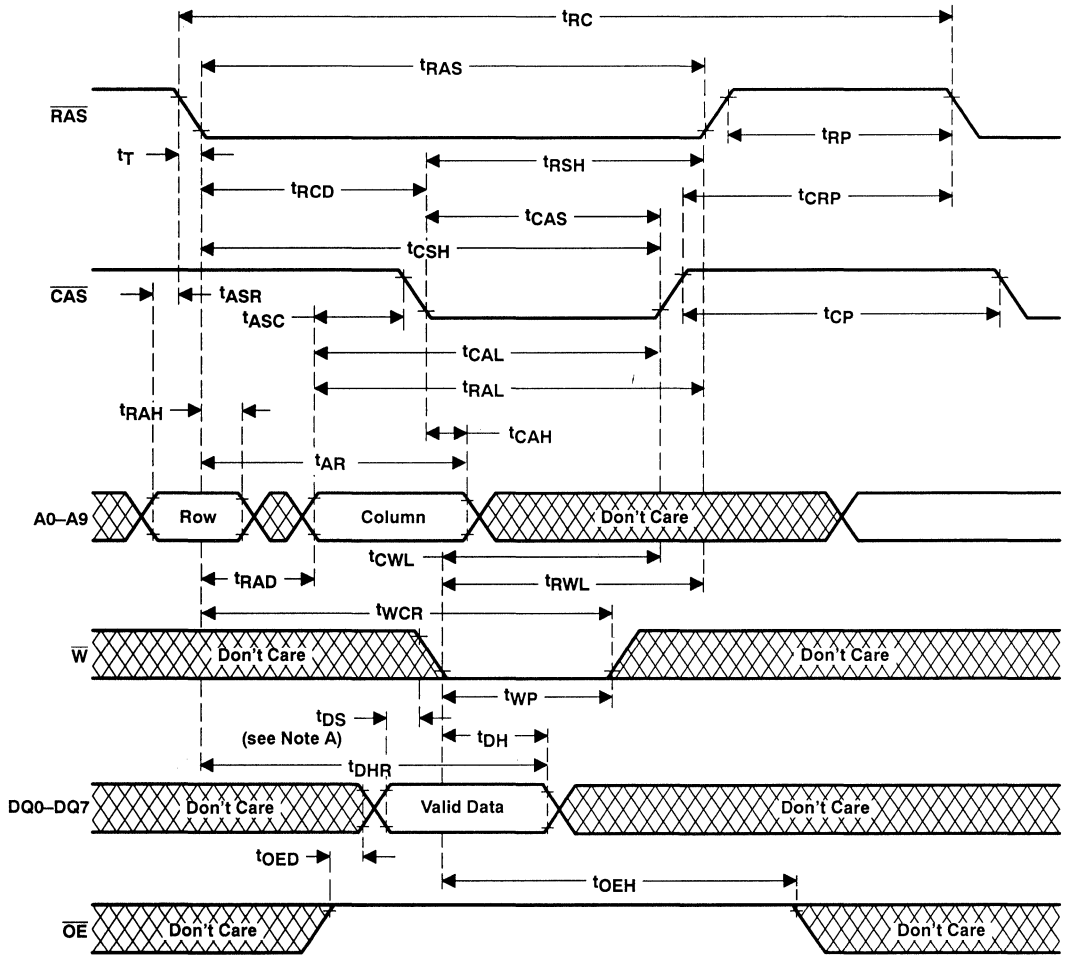


Figure 3. Early Write Cycle Timing

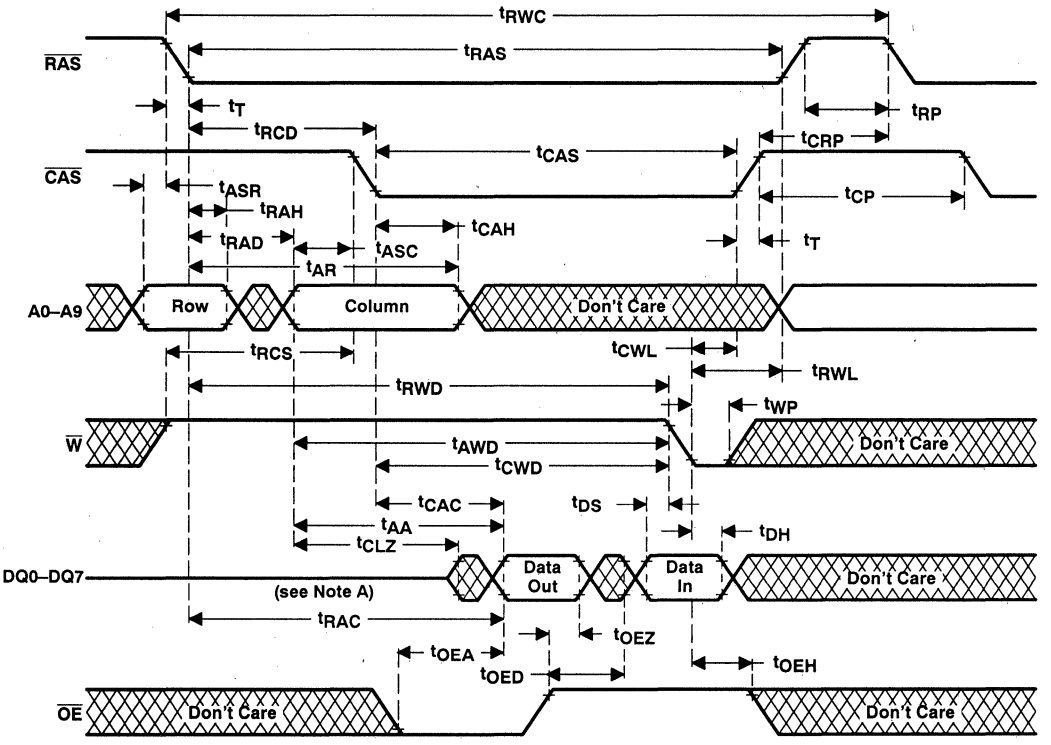
PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 4. Write Cycle Timing

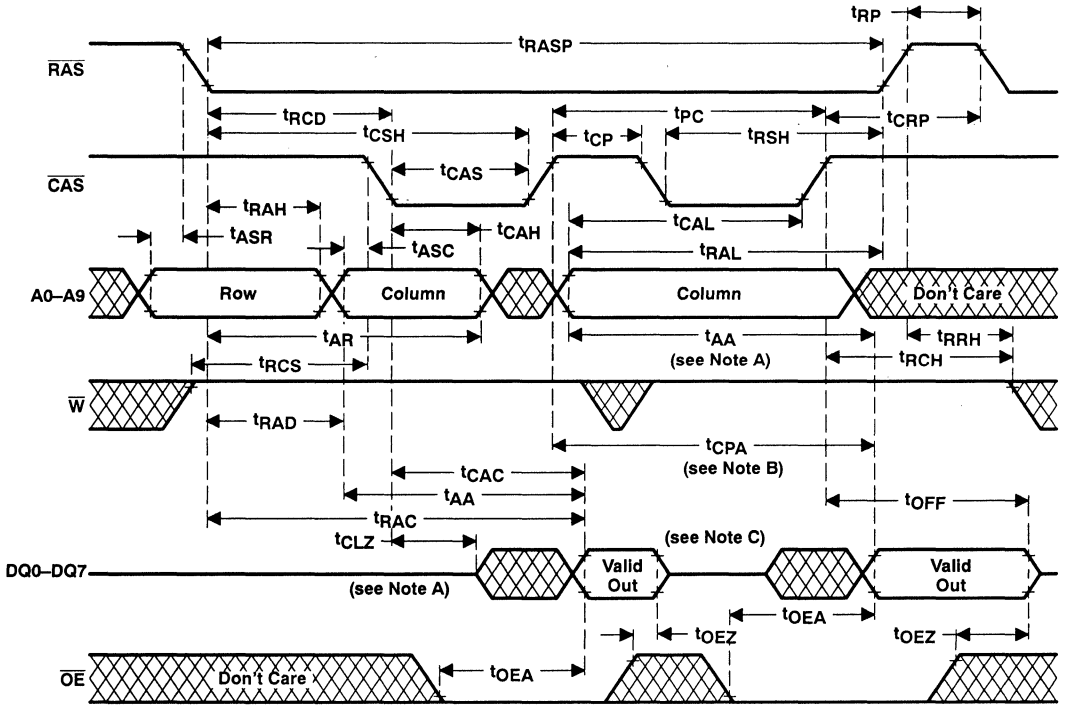
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

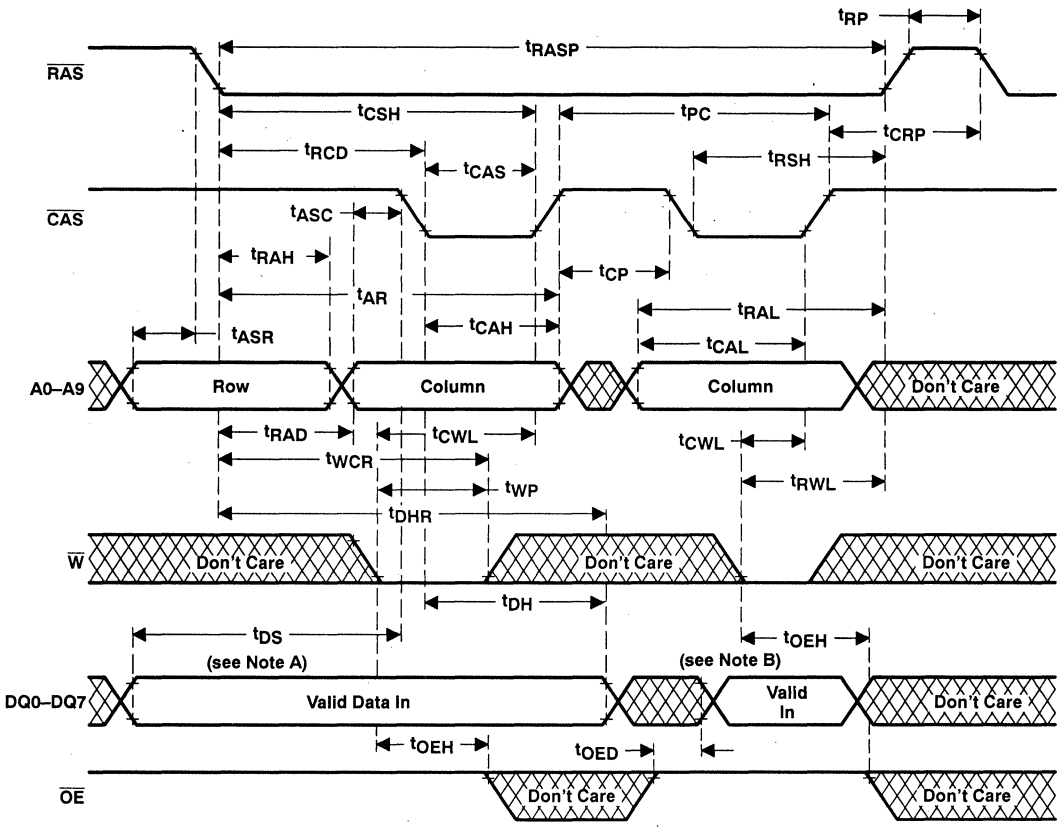
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

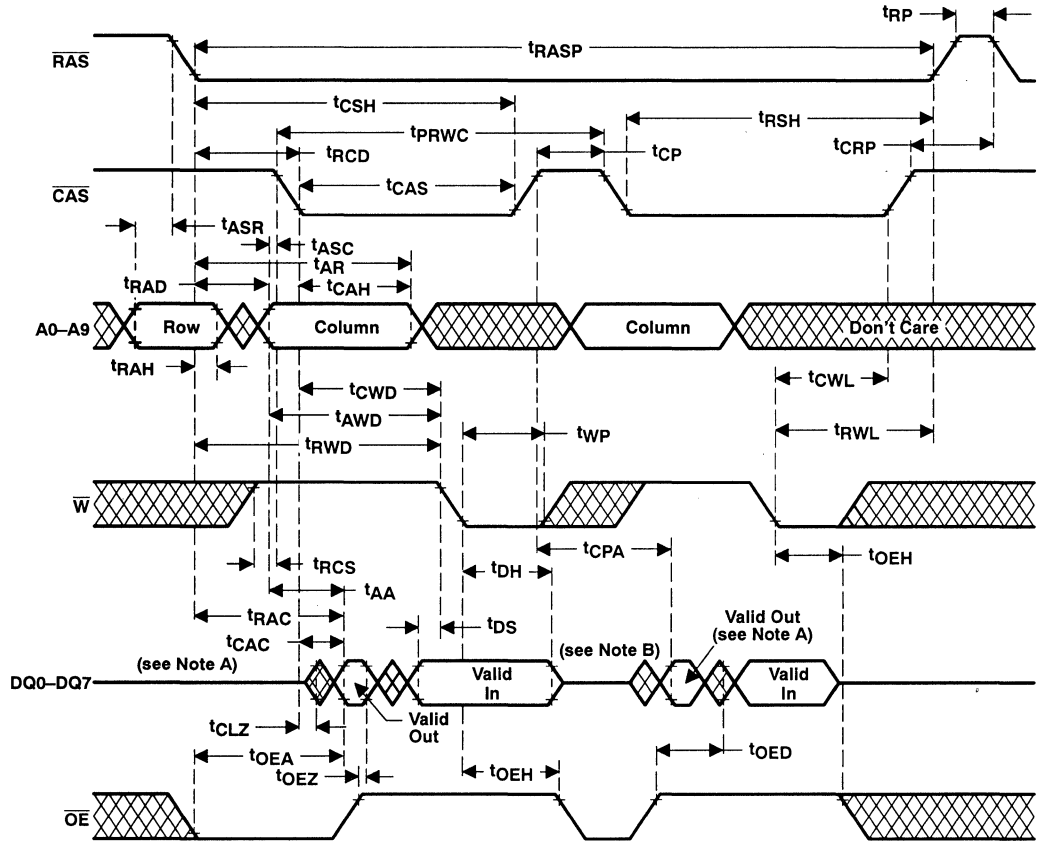
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

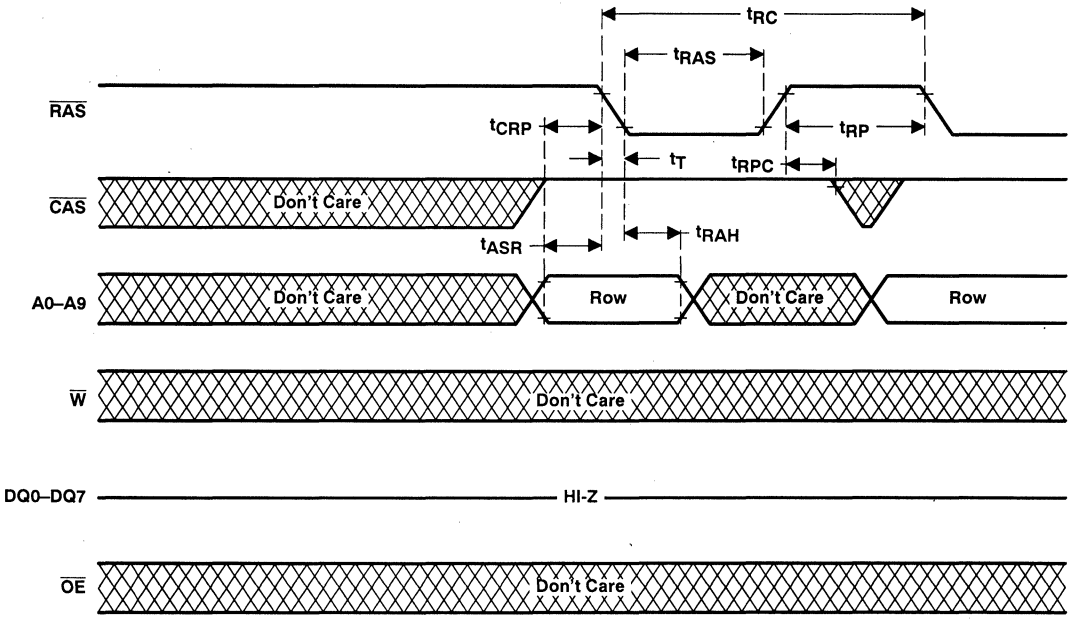


Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

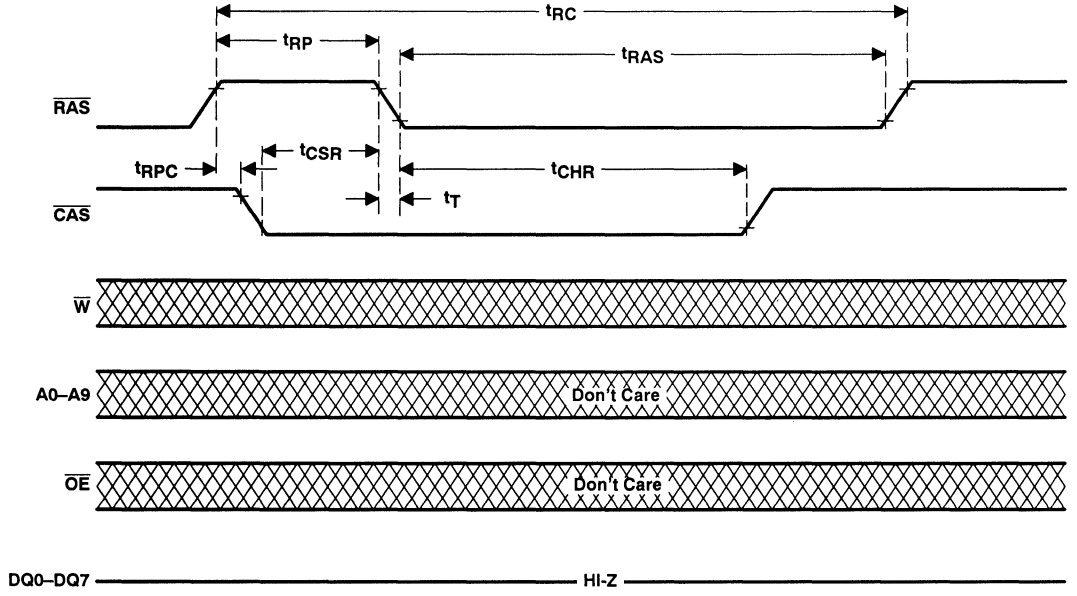


Figure 10. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

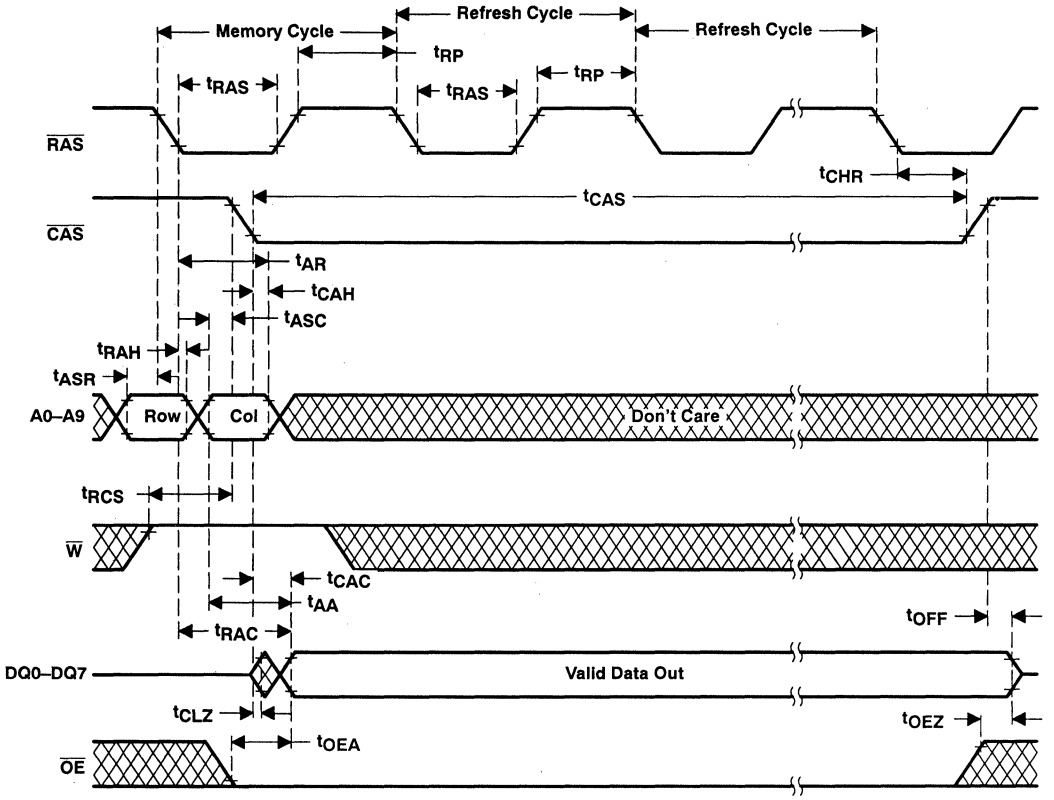


Figure 11. Hidden Refresh Cycle

PARAMETER MEASUREMENT INFORMATION

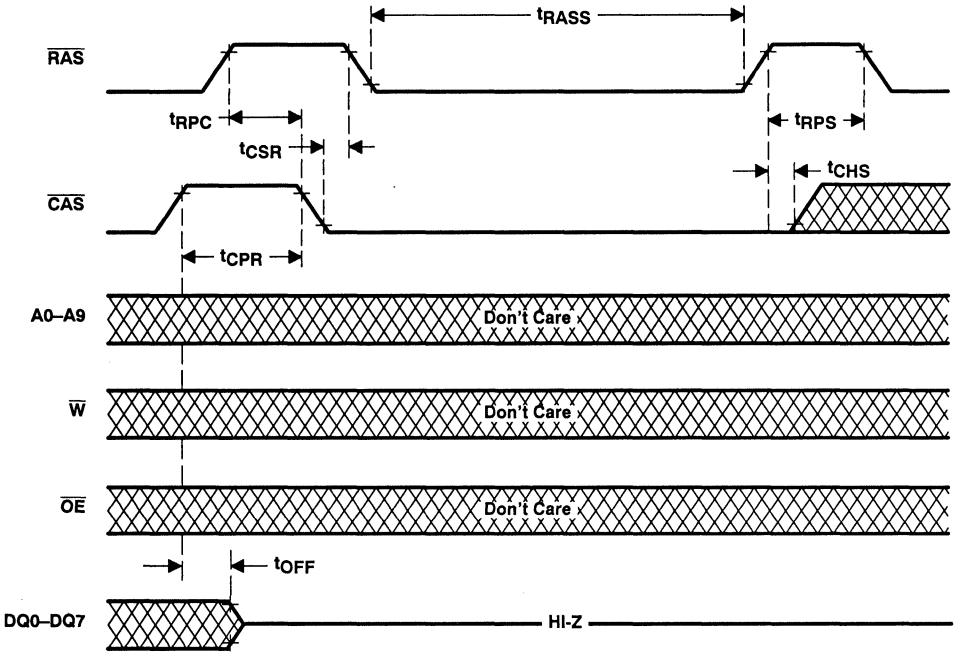
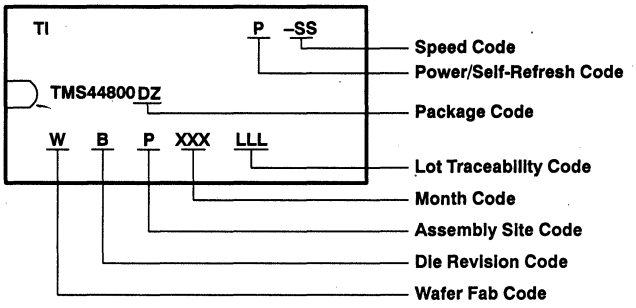


Figure 12. Self Refresh Timing

device symbolization



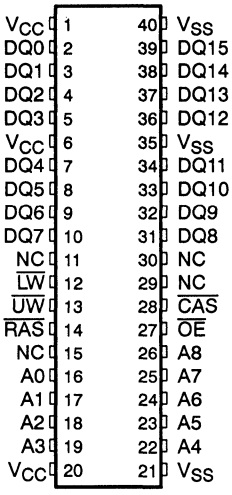
This data sheet is applicable to all TMS44165/Ps symbolized with Revision "B" and subsequent revisions as described on page 22.

- **Organization . . . 262 144 × 16**
- **Single 5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

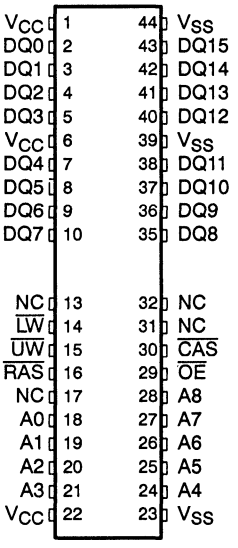
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'44165/P-70	70 ns	20 ns	35 ns	130 ns
'44165/P-80	80 ns	20 ns	40 ns	150 ns
'44165/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period**
  1024-Cycle Refresh in 16 ms (Max)
  128 ms for Low Power With Self-Refresh Version (TMS44165P)
- **High-Impedance Unlatched Output**
- **Lower Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 40-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 40/44-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Self-Refresh With Low-Power**
- **Upper and Lower Byte Control During Write Operations**

DZ PACKAGE† (TOP VIEW)



DGE PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{LW}$	Lower Write Enable
$\overline{UW}$	Upper Write Enable
$\overline{RAS}$	Row-Address Strobe
NC	No Internal Connection
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS44165 series are high-speed, 4 194 304-bit dynamic random access memories organized as 262 144 words of sixteen bits each.

The TMS44165P series are high-speed, low-power with self-refresh, 4 194 304-bit dynamic random-access memories organized as 262 144 words by sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

EPIC is a trademark of Texas Instruments Incorporated.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 522 mW operating and 11 mW standby on 100 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44165 and TMS44165P are each offered in a 40-lead plastic surface mount SOJ (DZ suffix) package, and a 40/44-lead plastic surface mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44165 and TMS44165P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of the last $\overline{CAS}$).

address (A0–A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the TMS44165 and TMS44165P, $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{UW}$, $\overline{LW}$)

The read or write mode is selected through the upper or lower write-enable ($\overline{UW}$, $\overline{LW}$) input. $\overline{LW}$ controls DQ0–DQ7, and $\overline{UW}$ controls DQ8–DQ15. A logic high on the $\overline{UW}$ and $\overline{LW}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{UW}$ or $\overline{LW}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

NOTE: Either $\overline{UW}$ or $\overline{LW}$ can be brought low in a given write cycle and only eight data bits will be written into. The user may bring both $\overline{UW}$ and $\overline{LW}$ low at the same time and all 16 data bits will be written into.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$, $\overline{UW}$, or $\overline{LW}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{UW}$ or $\overline{LW}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{UW}$ or $\overline{LW}$ with setup

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and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines. The $\overline{LW}$ pin controls DQ0–DQ7. The $\overline{UW}$ pin controls DQ8–DQ15.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every eight milliseconds (64 ms for TMS44165P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR)

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS44165P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self-refresh (TMS44165P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

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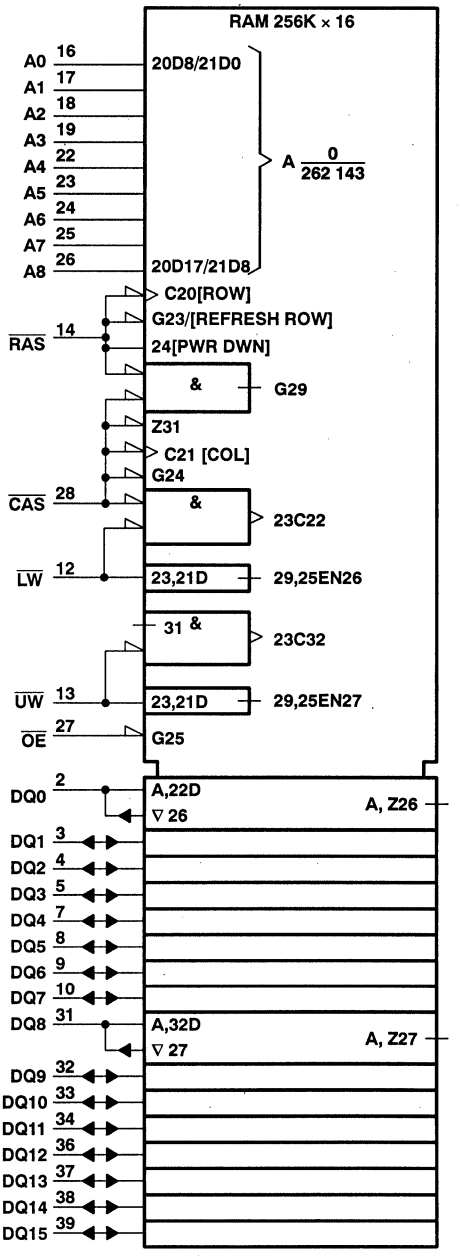
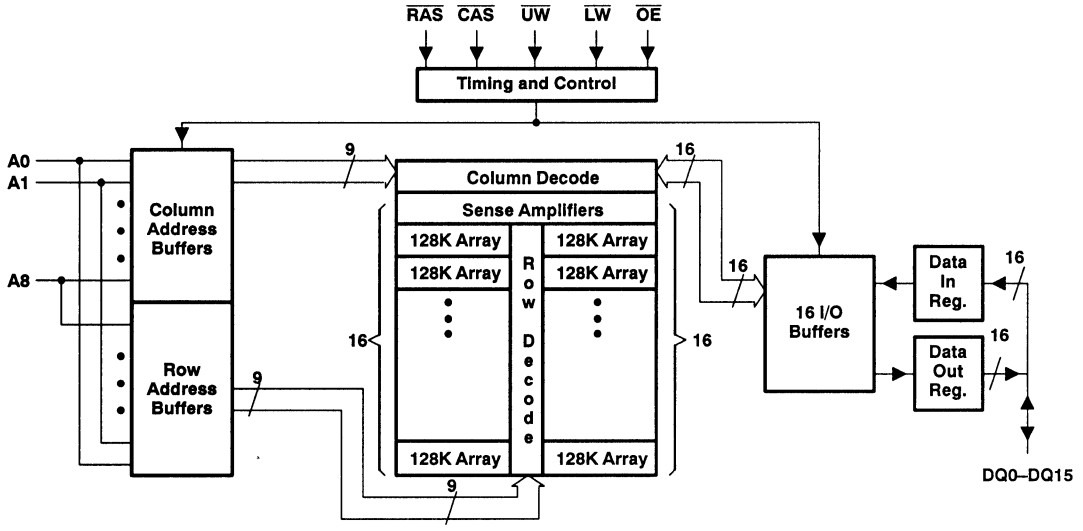
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'44165-70 '44165P-70 MIN	'44165-70 '44165P-70 MAX	'44165-80 '44165P-80 MIN	'44165-80 '44165P-80 MAX	'44165-10 '44165P-10 MIN	'44165-10 '44165P-10 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			120		105		95	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'44165		1		1		1	mA
			'44165P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, ($\overline{RAS}$-only), $\overline{RAS}$ cycling, $\overline{CAS}$ high (CBR only) $\overline{RAS}$ low after $\overline{CAS}$ low			120		105		95	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			120		105		95	mA
I_{CC5}‡	Battery backup operating current (equivalent refresh time is 64 ms) (CBR only)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{UW}$, $\overline{LW}$ and $\overline{OE}$=V_{IH}, Address and Data stable			300		300		300	µA
I_{CC6}†‡	Self refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			200		200		200	µA

† Measured with outputs open.
‡ For TMS44165P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'44165-70 '44165P-70		'44165-80 '44165P-80		'44165-10 '44165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		20		20		25	ns
t_{AA}	Access time from column address		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{CLZ}	$\overline{CAS}$ low to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	20	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	20	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		'44165-70 '44165P-70		'44165-80 '44165P-80		'44165-10 '44165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 8)	130		150		180		ns
t_{WC}	Write cycle time	130		150		180		ns
t_{RWC}	Read-modify-write cycle time	185		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	45		50		55		ns
t_{PRWC}	Page-mode read-modify-write cycle time	90		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Write pulse duration	15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{xW}$ low (see Note 12)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{xW}$-low setup time before $\overline{CAS}$ high	20		20		25		ns
t_{RWL}	$\overline{xW}$-low setup time before $\overline{RAS}$ high	20		20		25		ns
t_{WCS}	$\overline{xW}$-low setup time before $\overline{CAS}$ low (see Note 13)	0		0		0		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 15)	35		35		45		ns
t_{DH}	Data hold time after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 15)	35		35		45		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 16)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 16)	0		0		0		ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
8. All cycle times assume t_T = 5 ns.
9. $t_{PC} > t_{CP}$ min + t_{CAS} min + 2t_T.
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
12. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
13. Early write operation only.
14. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
15. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7) (concluded)

	PARAMETER	'44165-70 '44165P-70		'44165-80 '44165P-80		'44165-10 '44165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low (see Note 13)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 15)	35		35		45		ns
t_{AWD}	Delay time, column address to $\overline{xW}$ low (see Note 17)	65		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 14)	15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 14)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{xW}$ low (see Note 17)	50		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	20		20		25		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	20		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 18)	15	35	15	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)	20	50	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 14)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{xW}$ low (see Note 17)	100		110		135		ns
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		180		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{REF}	Refresh time interval (TMS44165)		16		16		16	ms
t_{REF}	Refresh time interval, low power (TMS44165P only)		128		128		128	ms
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high	−50		−50		−50		ns
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
13. Early write operation only.
14. $\overline{CAS}$-before-$\overline{RAS}$ refresh only
15. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
17. Read-modify-write operation only.
18. Maximum value specified only to assure access time.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

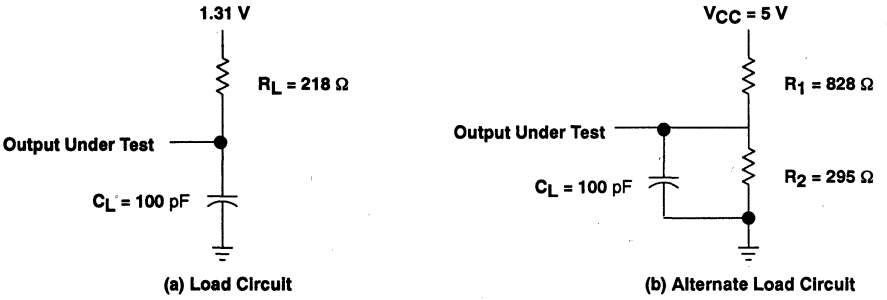
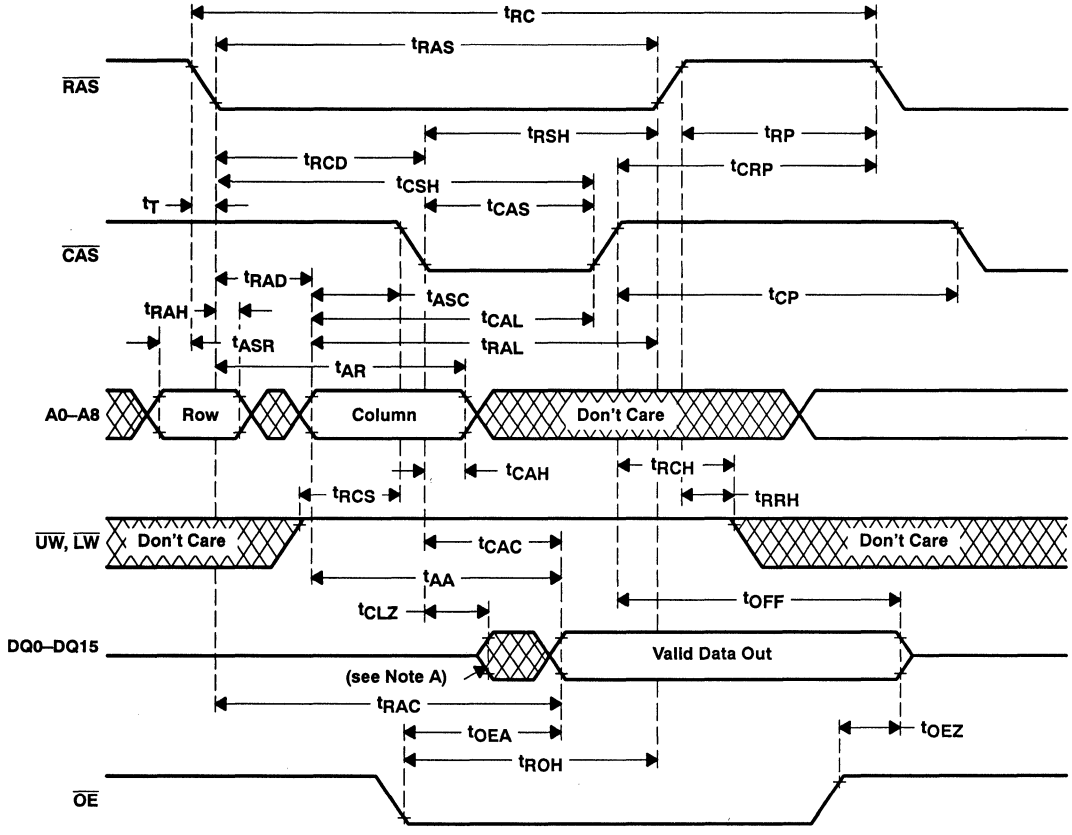


Figure 1. Load Circuits for Timing Parameters

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

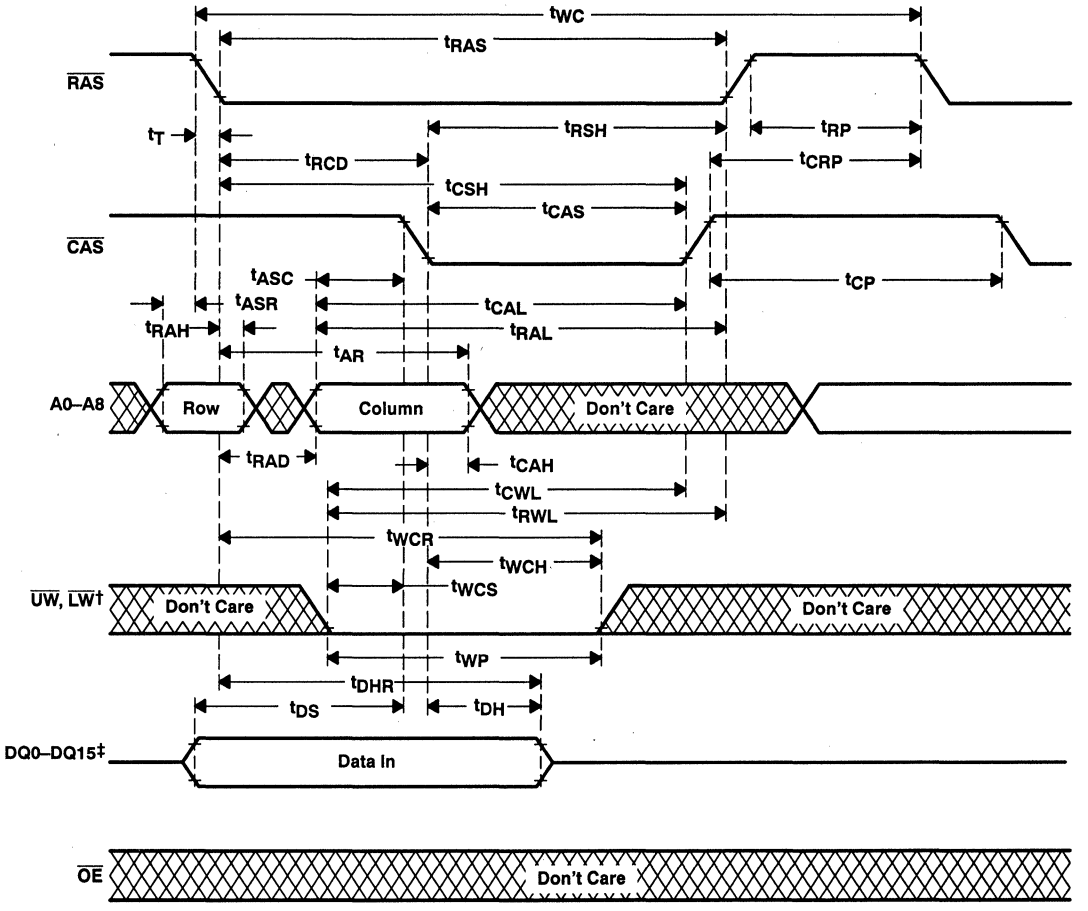


NOTE A: Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

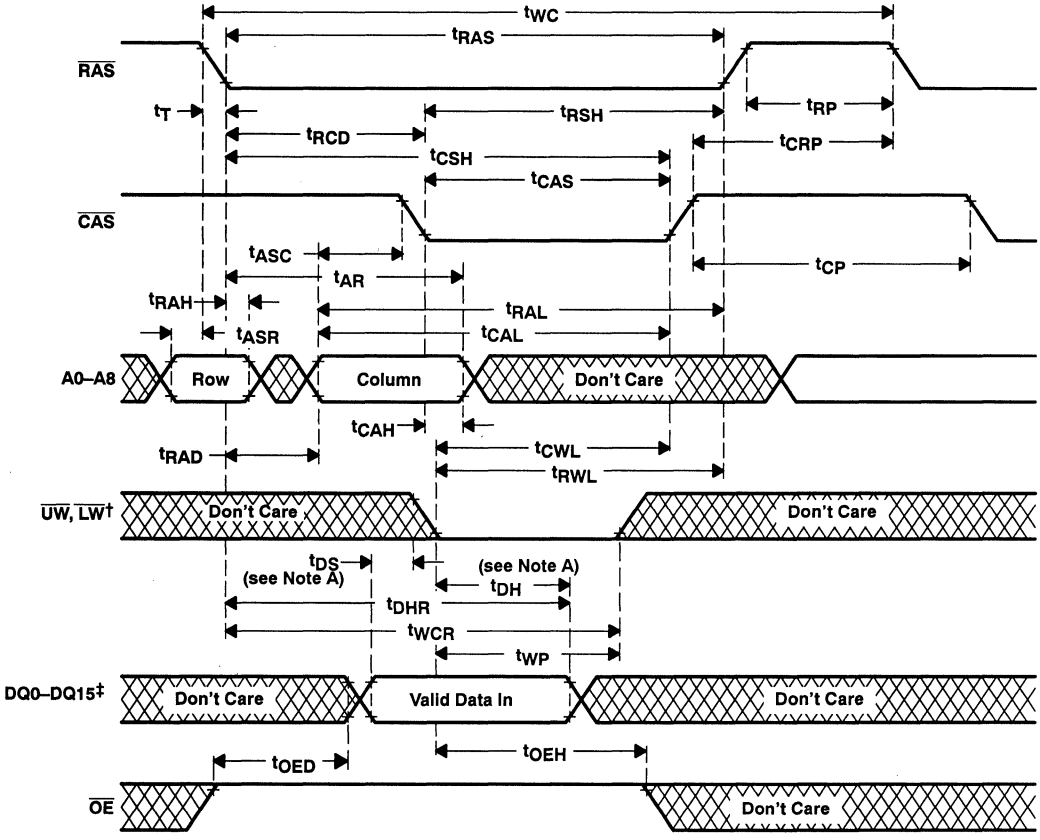


† Either $\overline{UW}$ or $\overline{LW}$ may be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ may be brought low at the same time and all 16 DQ locations will be written into.

‡ All DQ pins remain in the HI-Z state for an early write cycle.

Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

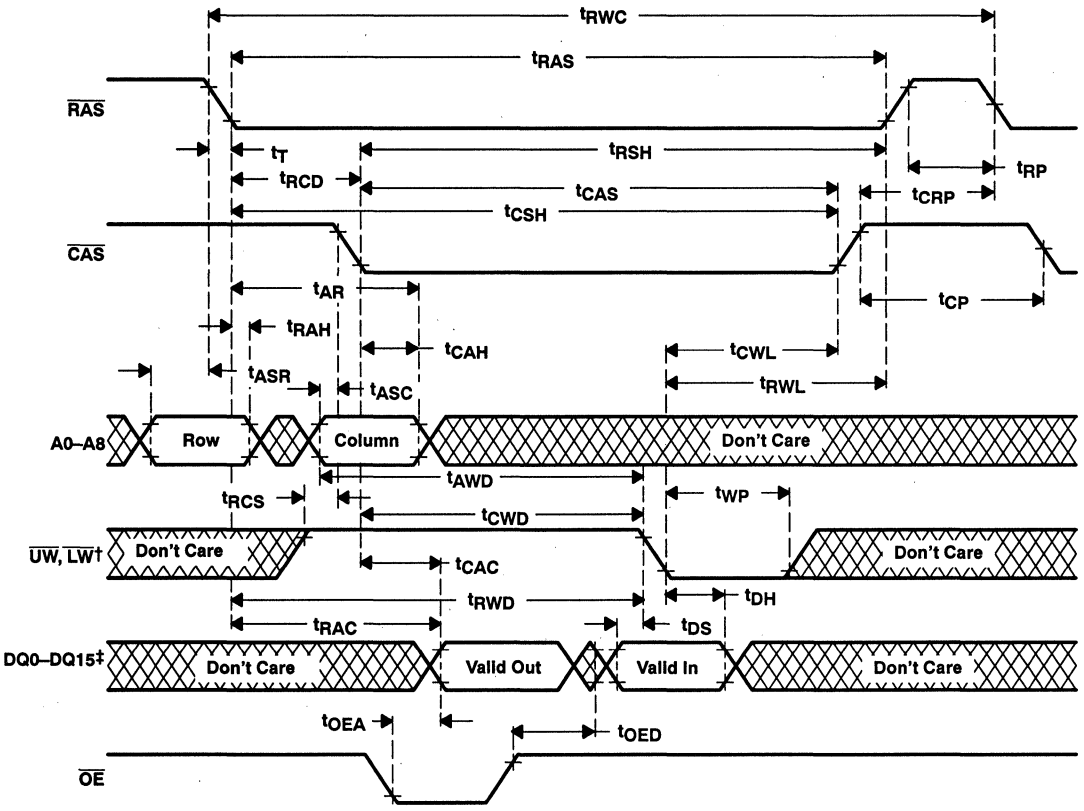


† Either $\overline{UW}$ or $\overline{LW}$ may be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ may be brought low at the same time and all 16 DQ locations will be written into.
‡ All DQ pins remain in the HI-Z state while $\overline{OE}$ is high.
NOTE A: Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.

Figure 4. Write Cycle Timing

ADVANCE INFORMATION

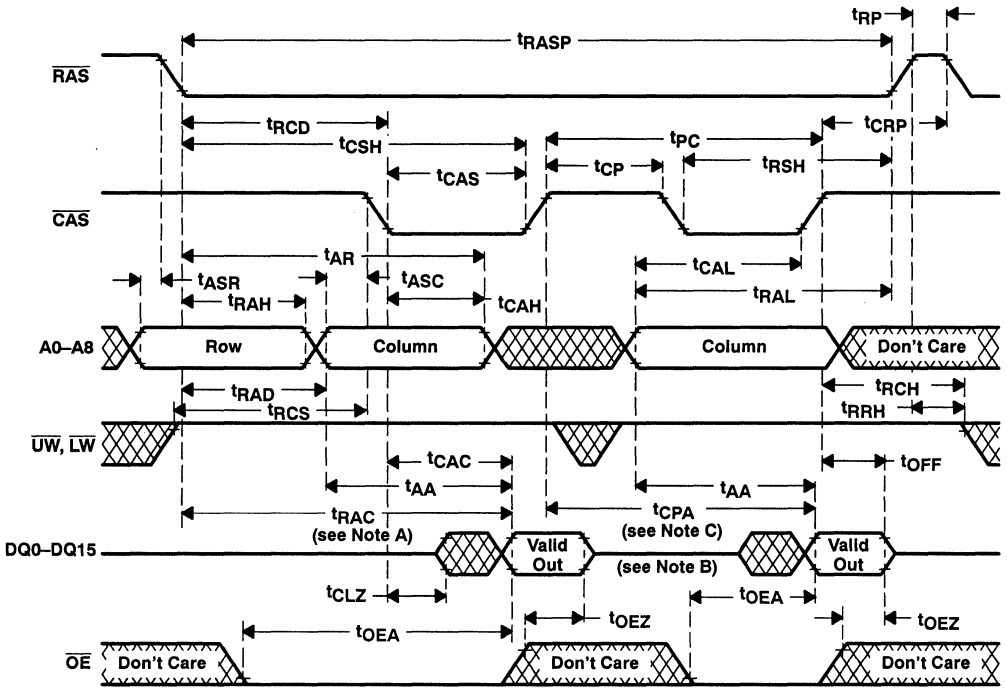
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ may be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ may be brought low at the same time and all 16 DQ locations will be written into.
‡ All DQ pins remain in the HI-Z state for an early write cycle.

Figure 5. Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

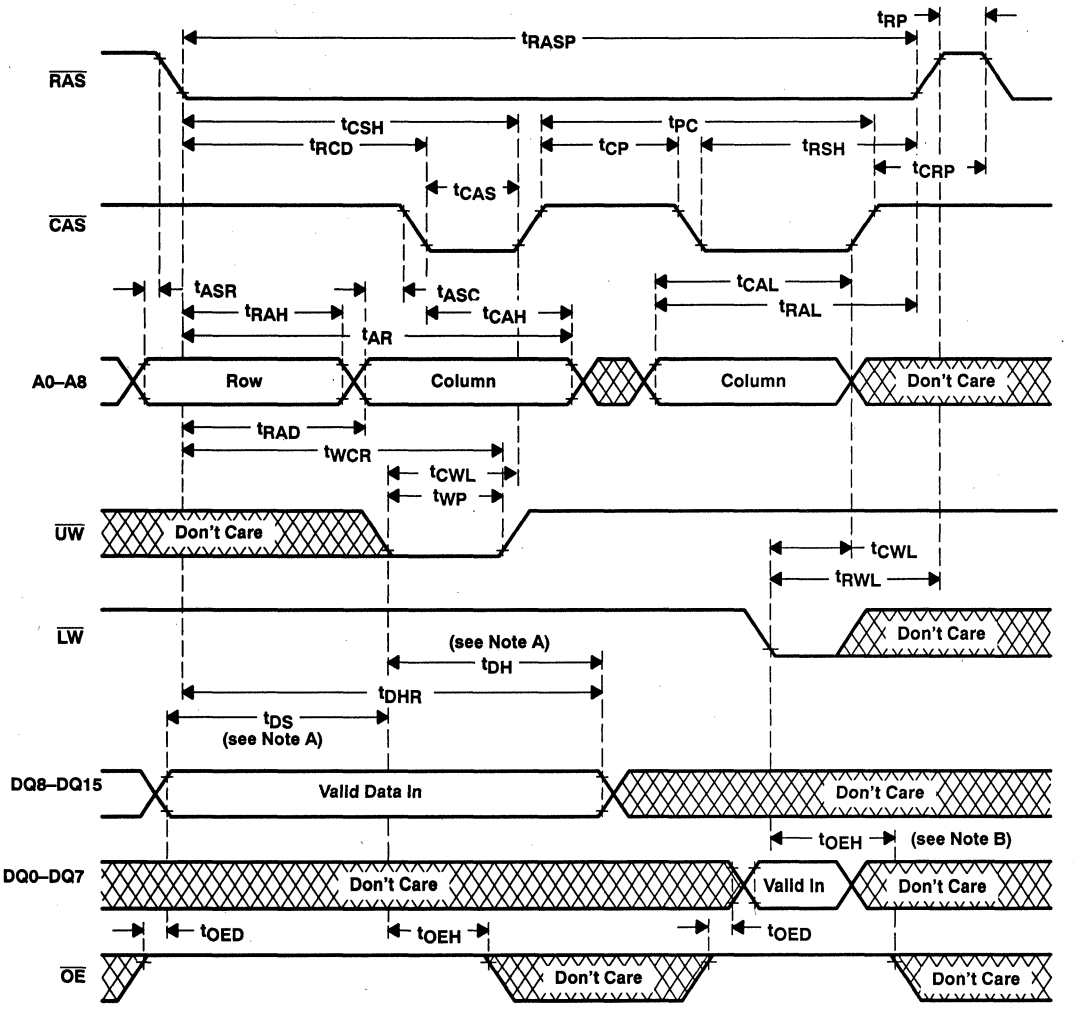


NOTES: A. Output may go from high impedance to an invalid data state prior to the specified access time.
B. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

ADVANCE INFORMATION

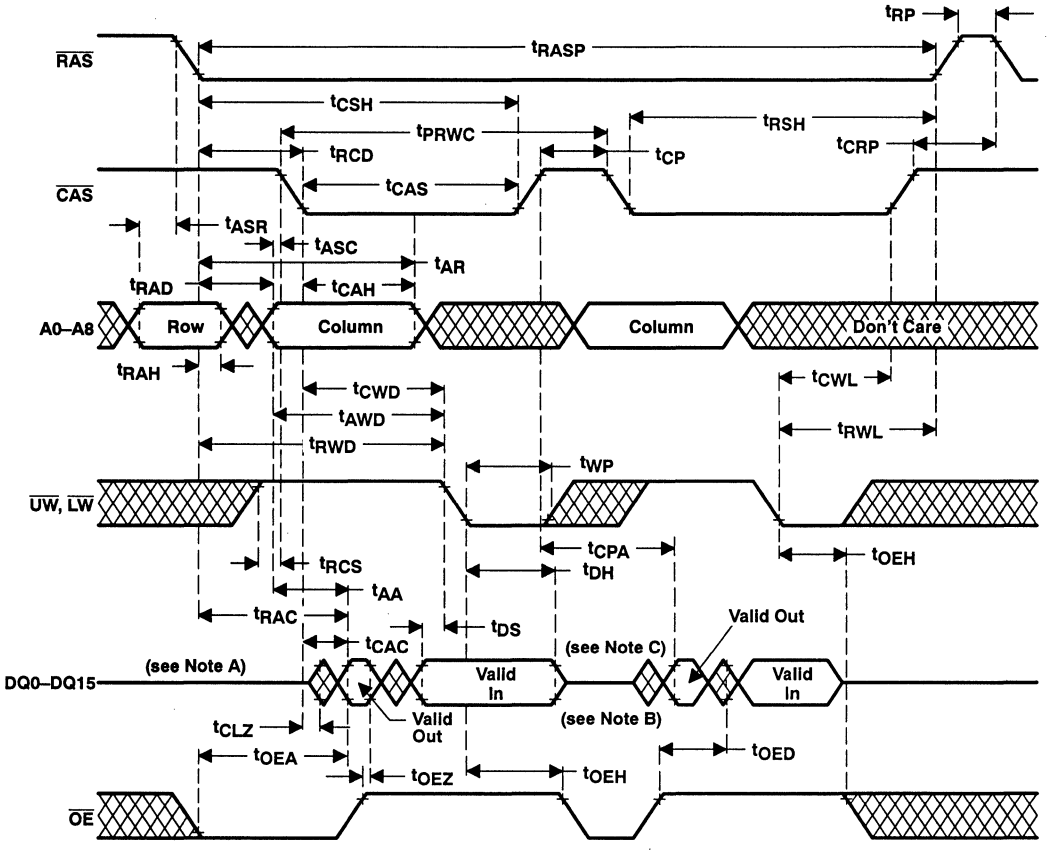
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from high impedance to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

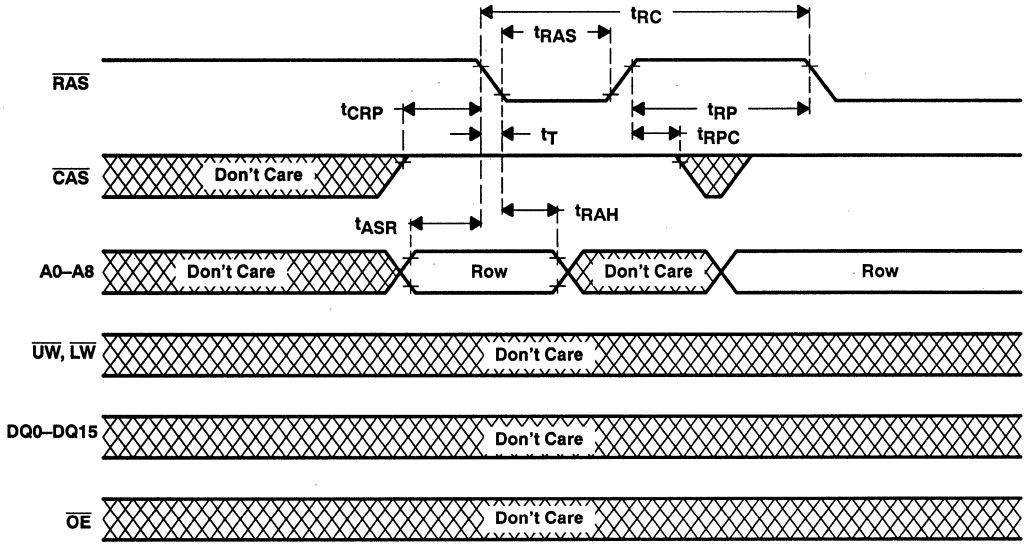


Figure 9. RAS-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

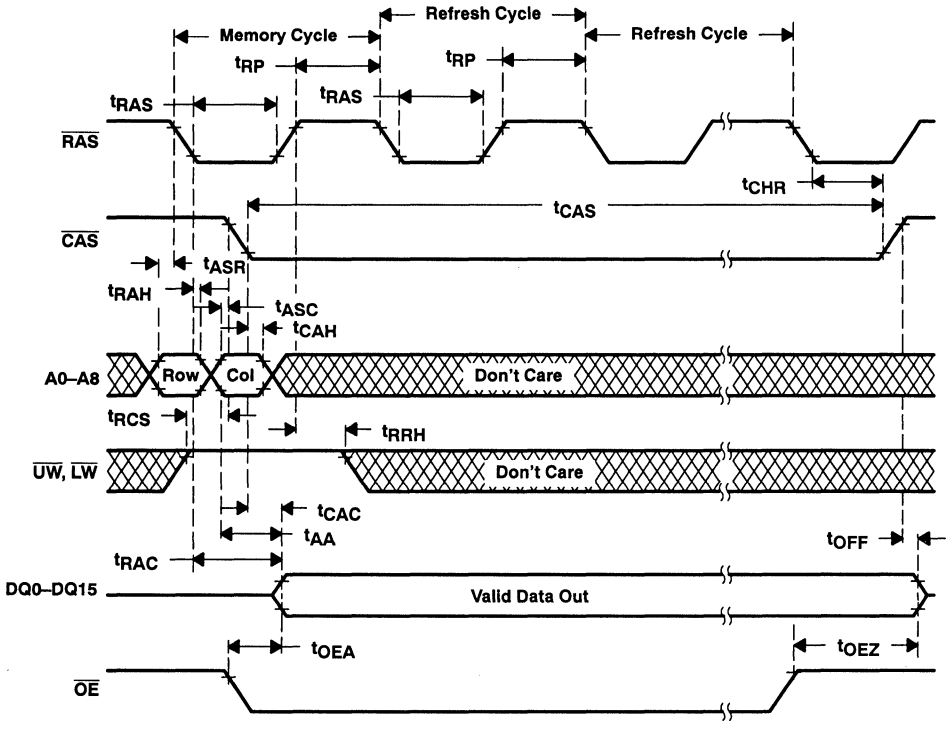
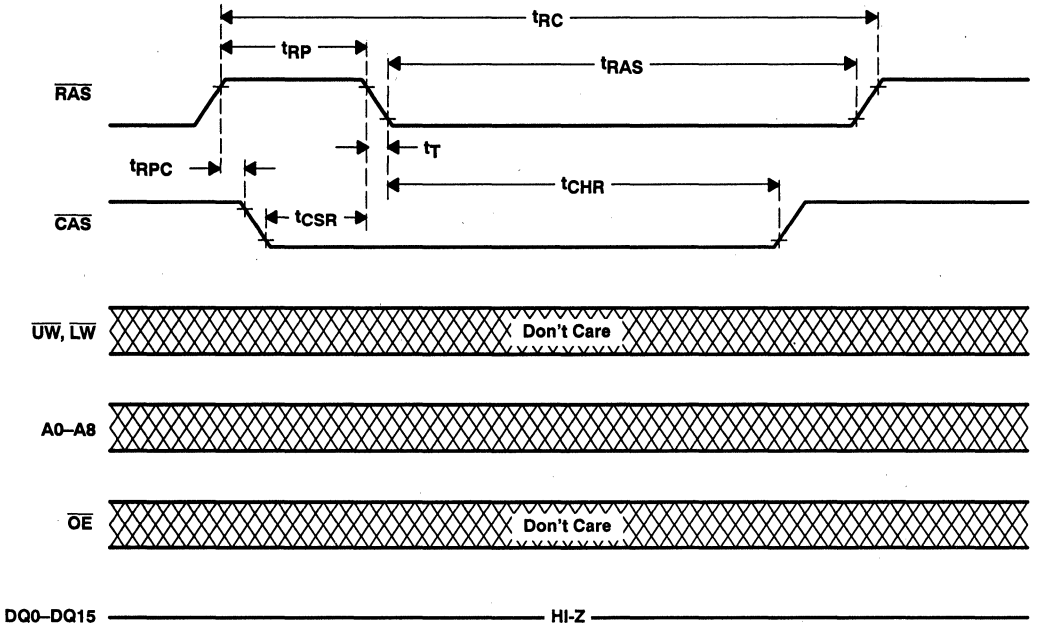


Figure 10. Hidden Refresh Cycle

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: 512 CBR cycles must be used for CBR counter test.

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

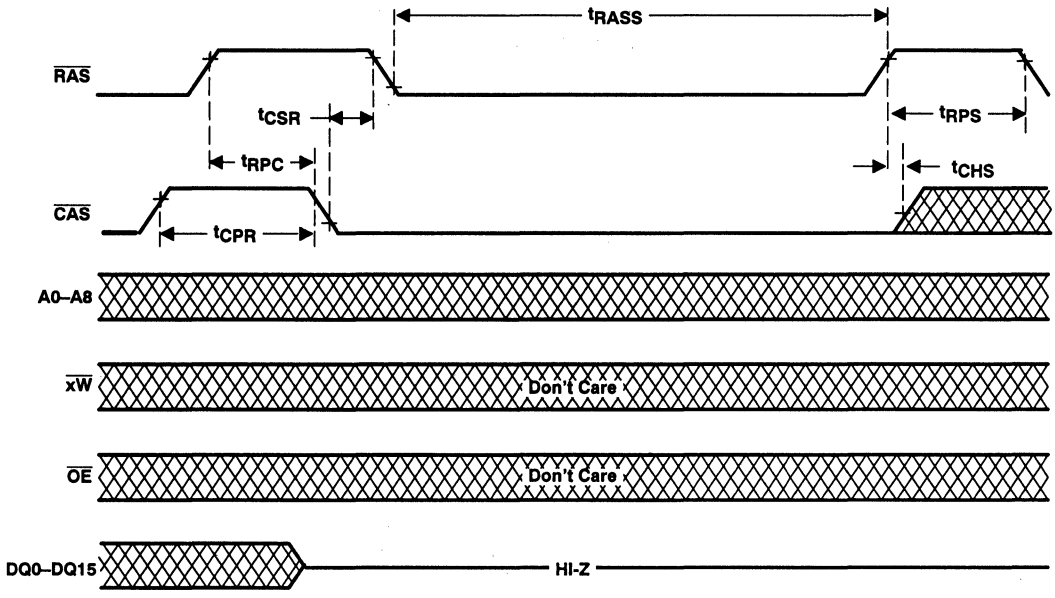
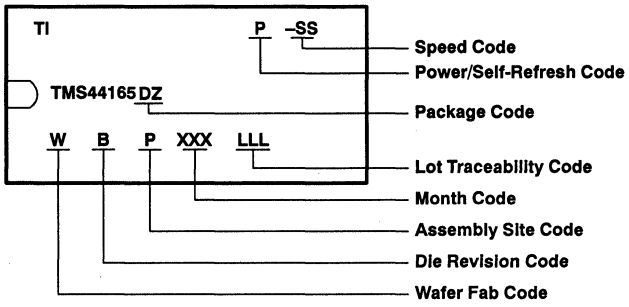


Figure 12. Self Refresh Timing

device symbolization



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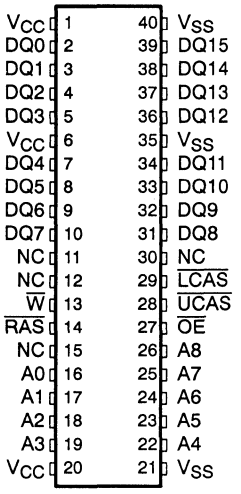
This data sheet is applicable to all TMS45160/Ps symbolized with Revision"B" and subsequent revisions as described on page 22

- **Organization . . . 262 144 × 16**
- **Single 5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

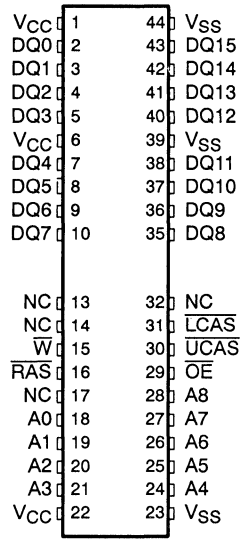
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45160/P-70	70 ns	20 ns	35 ns	130 ns
'45160/P-80	80 ns	20 ns	40 ns	150 ns
'45160/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  512-Cycle Refresh in 8 ms (Max)
  64 ms Max for Low-Power With Self-Refresh Version (TMS45160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 40-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 40/44-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low-Power With Self-Refresh Version**
- **Upper and Lower Byte Control During Read and Write Operations**

DZ PACKAGE† (TOP VIEW)



DGE PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A8	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS45160 series are high-speed, 4 194 304-bit dynamic random-access memories organized as 262 144 words of sixteen bits each.

The TMS45160P series are high-speed, low-power with self-refresh, 4 194 304-bit dynamic random-access memories organized as 262 144 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 660 mW operating and 11 mW standby on 100 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS45160 and TMS45160P are each offered in a 40-lead plastic surface mount SOJ (DZ suffix) package, and a 40/44-lead plastic surface mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ pin going low enables its corresponding DQ pins with data coming from the column address to be latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{xCAS}$ to its corresponding DQx pins.

In order to latch in a new column address, all $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early write cycles, the data is latched on the first falling $\overline{xCAS}$ edge. Only the DQs that have the corresponding $\overline{xCAS}$ low will be written into. Each $\overline{xCAS}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, both $\overline{xCAS}$ pins need to come high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by $\overline{RAS}$. Then, nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into low-impedance state. They will remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every eight milliseconds (64 ms for TMS45160P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{xCAS}$-before-$\overline{RAS}$ refresh

$\overline{xCAS}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS45160P. Data integrity is maintained using $\overline{xCAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

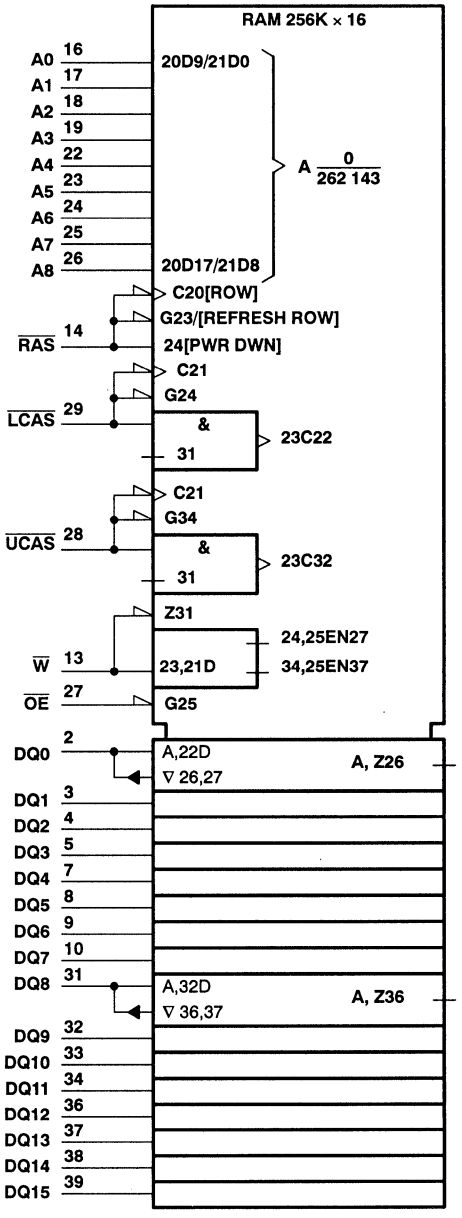
self refresh (TMS45160P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}.

power up

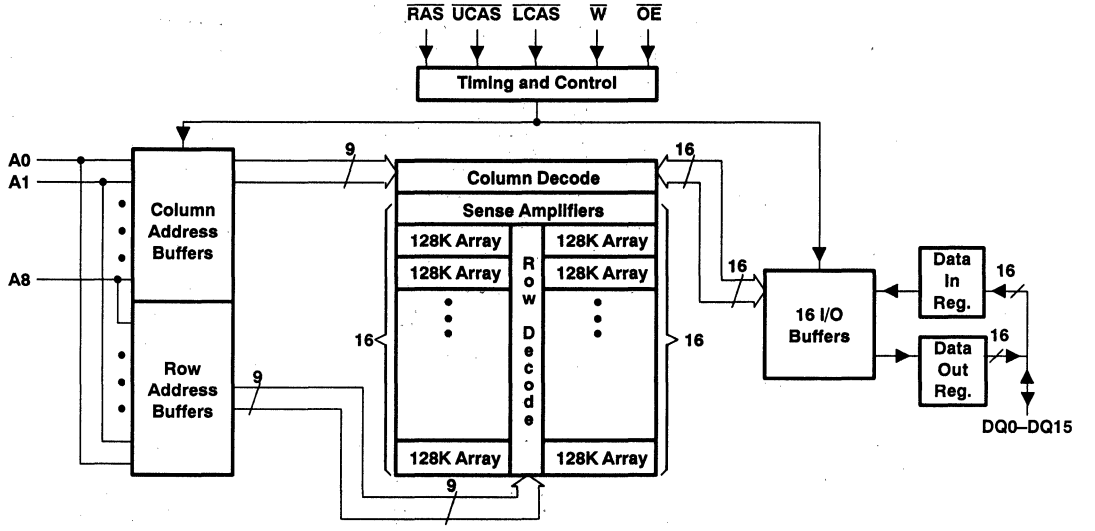
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS45160-70 TMS45160P-70		TMS45160-80 TMS45160P-80		TMS45160-10 TMS45160P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†§	Read or write cycle current	V_{CC} = 5.5 V, Minimum cycle			160		140		120	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'45160		1		1		1	mA
			'45160P		200		200		200	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only or CBR)	V_{CC} = 5.5 V, Minimum cycle, ($\overline{RAS}$-only), $\overline{RAS}$ cycling, $\overline{CAS}$ high (CBR only), $\overline{RAS}$ low after $\overline{CAS}$ low			160		140		120	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			160		140		120	mA
I_{CC5}¶	Battery back-up operating current (equivalent refesh time is 64 ms). CBR only.	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			300		300		300	µA
I_{CC6}†¶	Self refresh	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA

† Measured with outputs open.
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}.
¶ For TMS45160P only.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz# (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

Capacitance measurements are made on a sample basis only.
NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS45160-70 TMS45160P-70		TMS45160-80 TMS45160P-80		TMS45160-10 TMS45160P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		20		20		25	ns
t_{AA}	Access time from column address		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	20	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	20	0	20	0	25	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		TMS45160-70 TMS45160P-70		TMS45160-80 TMS45160P-80		TMS45160-10 TMS45160P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	130		150		180		ns
t_{WC}	Write cycle time	130		150		180		ns
t_{RWC}	Read-write/read-modify-write cycle time	185		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	45		50		55		ns
t_{PRWC}	Page-mode read-modify-write cycle time	90		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	20	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Write pulse duration	15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{xCAS}$ high	20		20		25		ns

Continued next page.

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{xCAS}$ low time (t_{CAS}).
10. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

		TMS45160-70 TMS45160P-70		TMS45160-80 TMS45160P-80		TMS45160-10 TMS45160P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	20		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before x$\overline{CAS}$ low (see Note 12)	0		0		0		ns
t_{CAH}	Column-address hold time after x$\overline{CAS}$ low (see Note 10)	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{DH}	Data hold time after x$\overline{CAS}$ low (see Note 10)	15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Read hold time after x$\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Write hold time after x$\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{CLCH}	Hold time, x$\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 15)	65		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	15		20		20		ns
t_{CRP}	Delay time, x$\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, x$\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		ns
t_{CWD}	Delay time, x$\overline{CAS}$ low to $\overline{W}$ low (see Note 15)	50		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	20		20		25		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	20		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 16)	15	35	15	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to x$\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ low (see Note 16)	20	50	20	60	25	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to x$\overline{CAS}$ low (see Note 11)	0		0		0		ns

Continued next page.

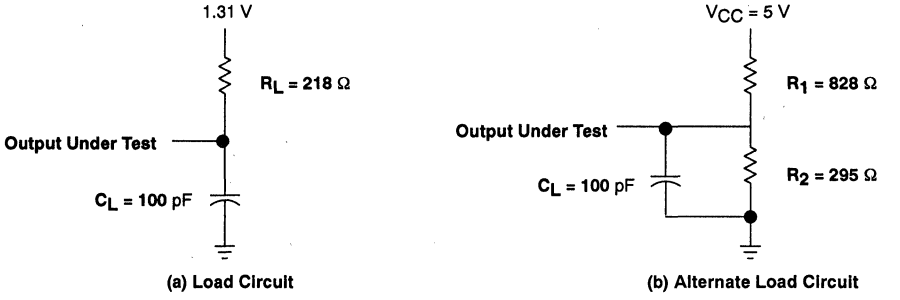
NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Later of x$\overline{CAS}$ or $\overline{W}$ in write operations.
11. x$\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Read-modify-write operation only.
16. Maximum value specified only to assure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

		TMS45160-70 TMS45160P-7		TMS45160-80 TMS45160P-80		TMS44160-10 TMS45160P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high	20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	100		110		135		ns
t_{CPR}	$\overline{xCAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		180		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{REF}	Refresh time interval (TMS45160 only)		8		8		8	ms
t_{REF}	Refresh time interval, low power (TMS45160P only)		64		64		64	ms
t_{CHS}	$\overline{xCAS}$ low hold time after $\overline{RAS}$ high	– 50		– 50		– 50		ns
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
15. Read-modify-write operation only.

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

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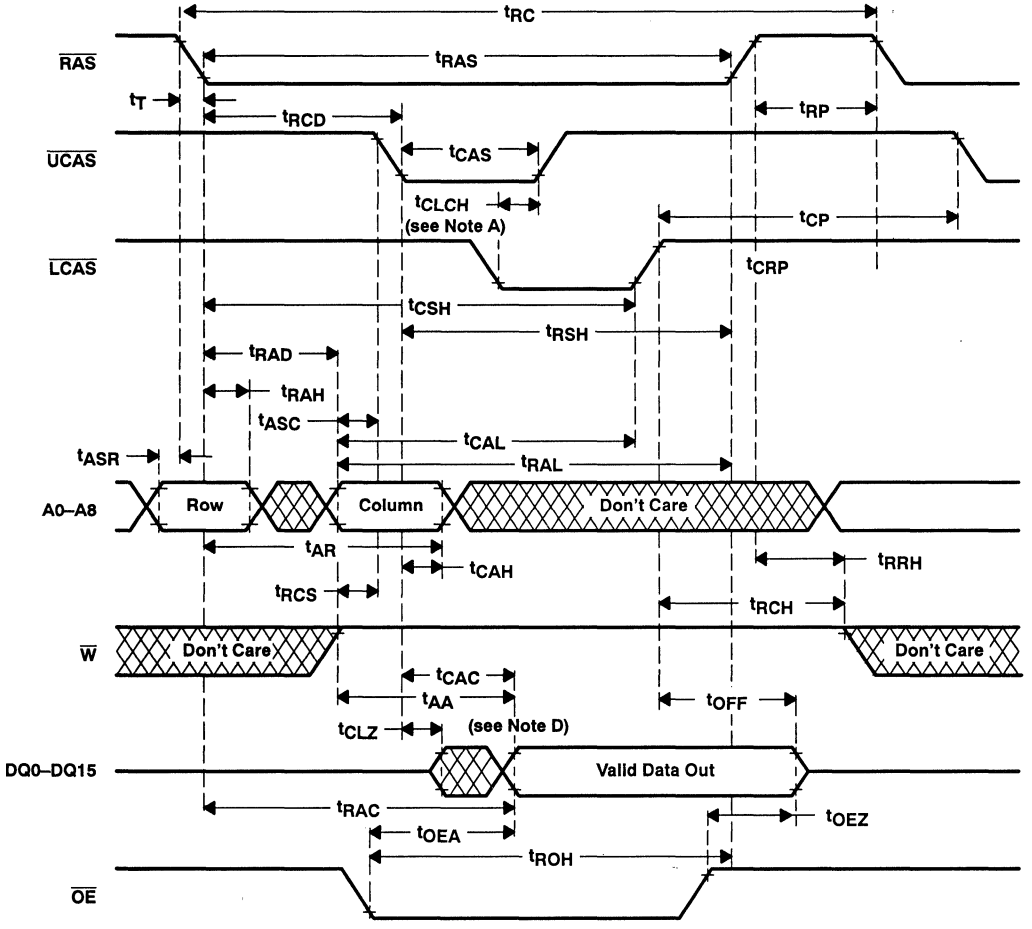
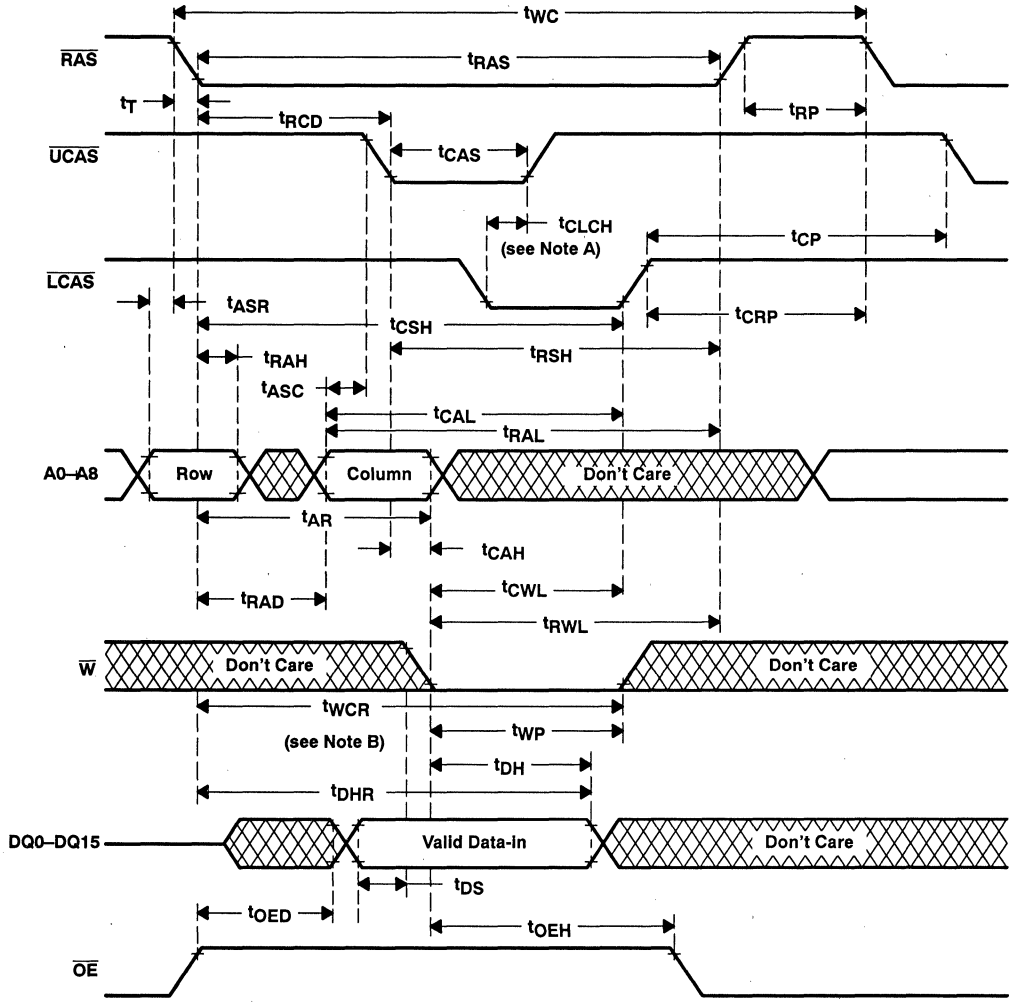
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle

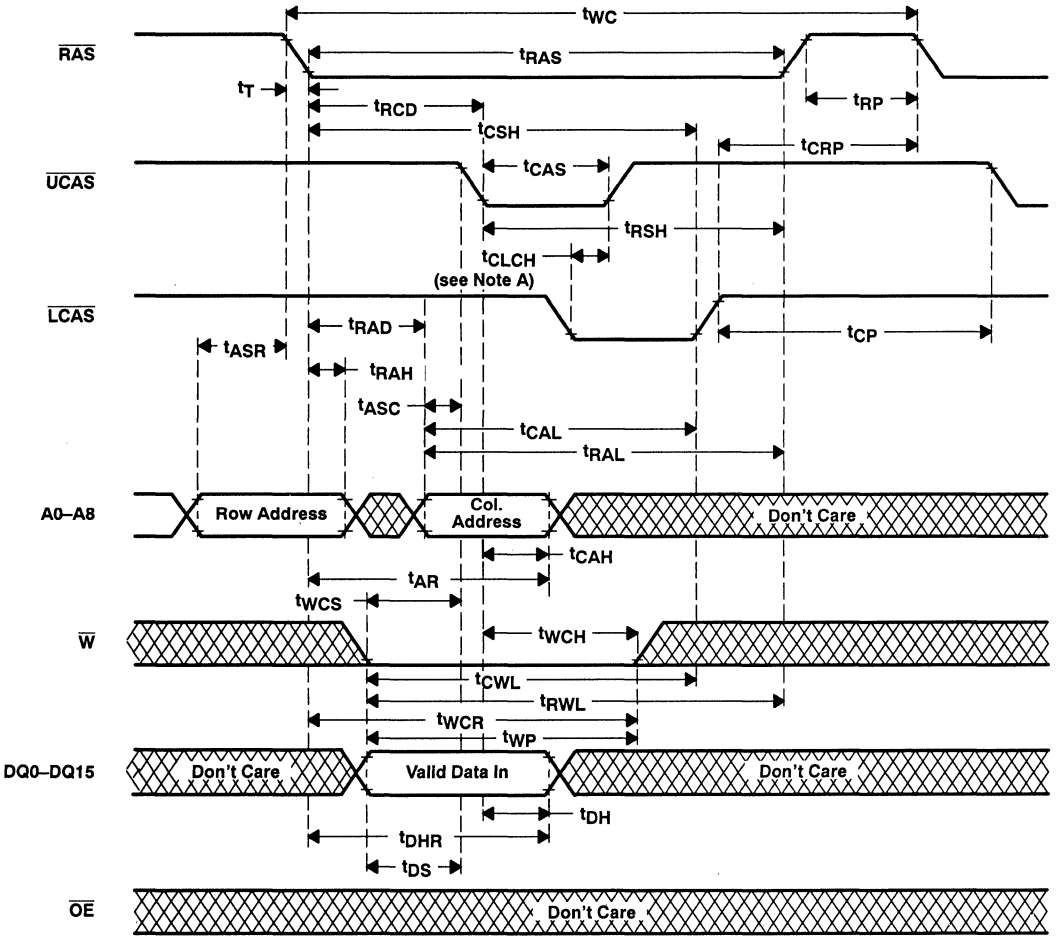
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Later of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ in write operations
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Write Cycle

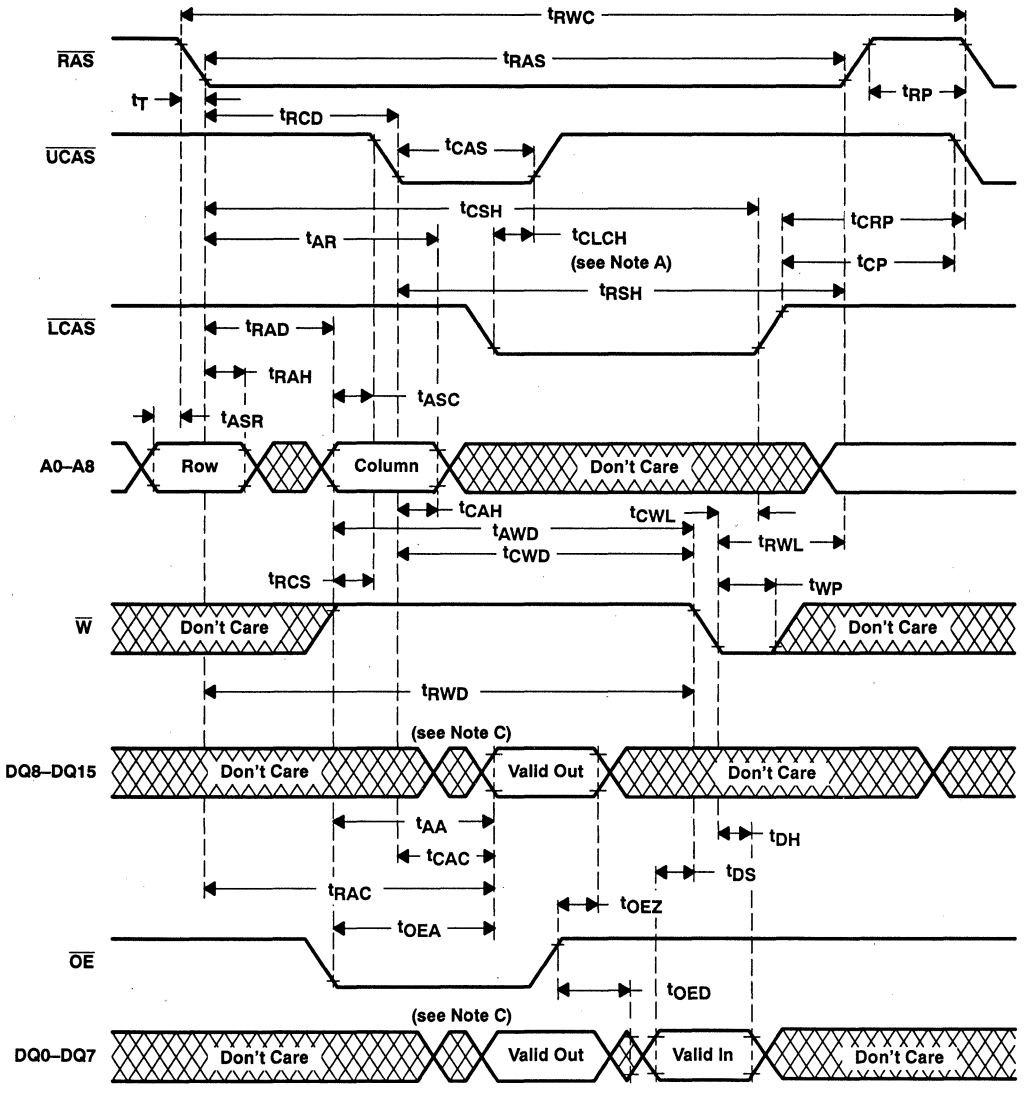
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early Write Cycle Timing

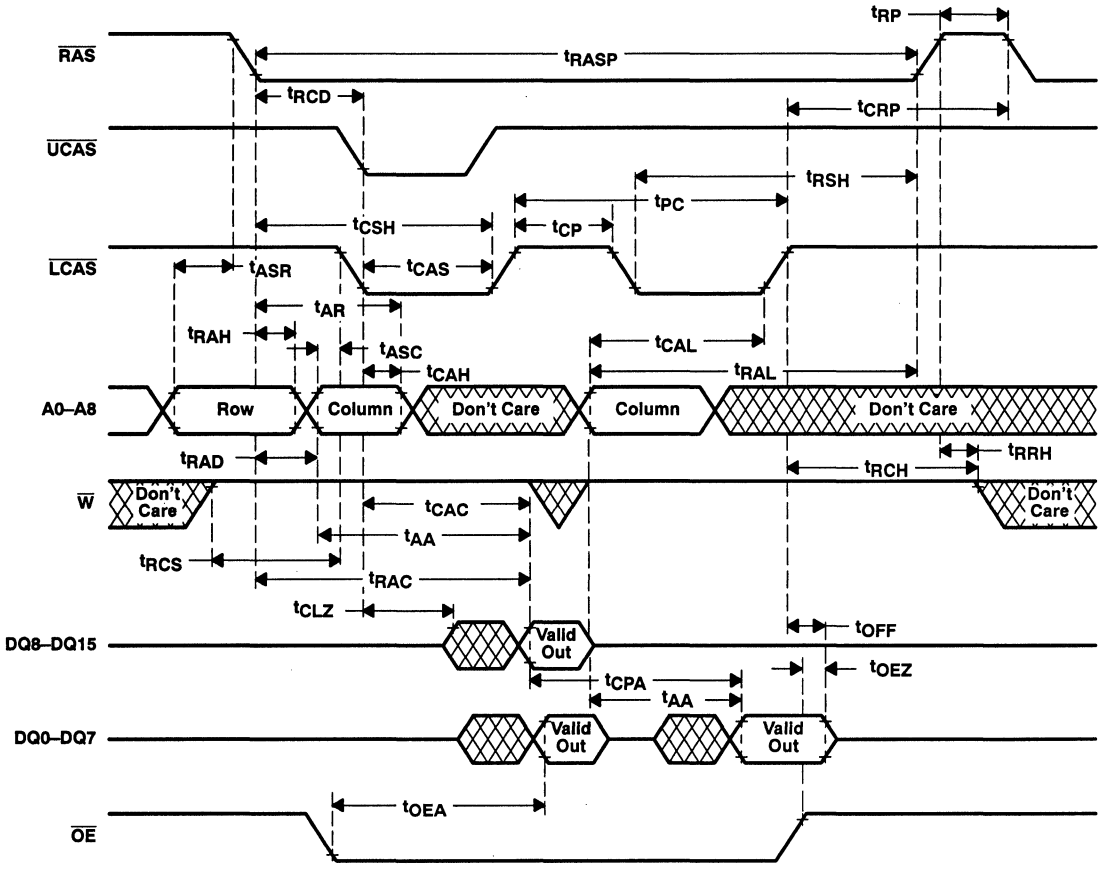
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle

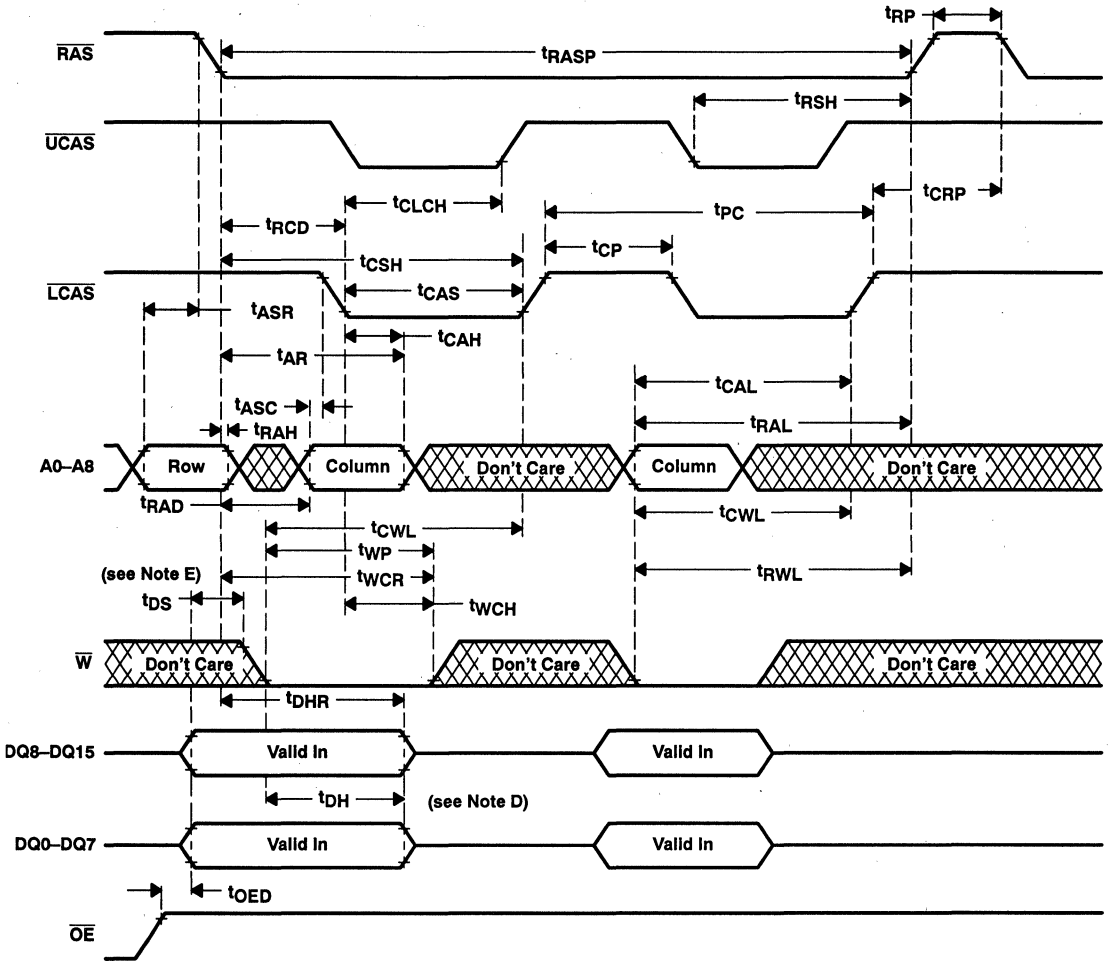
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

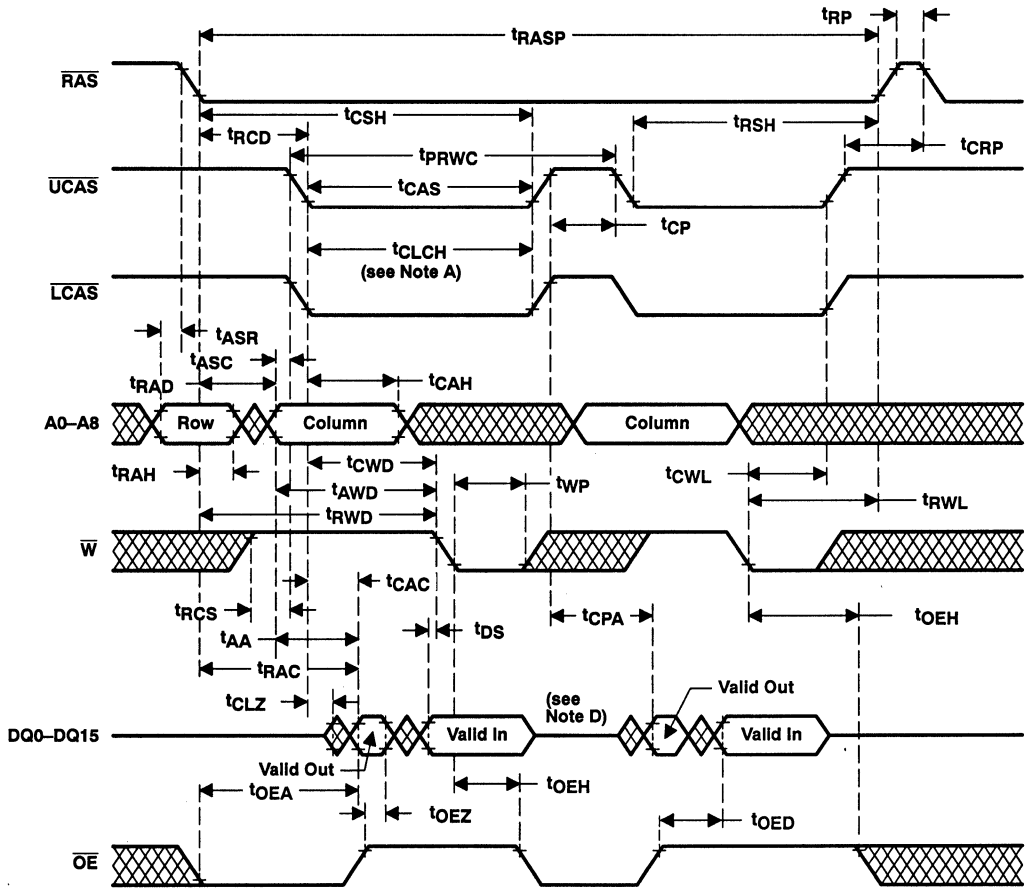
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
D. Referenced to $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

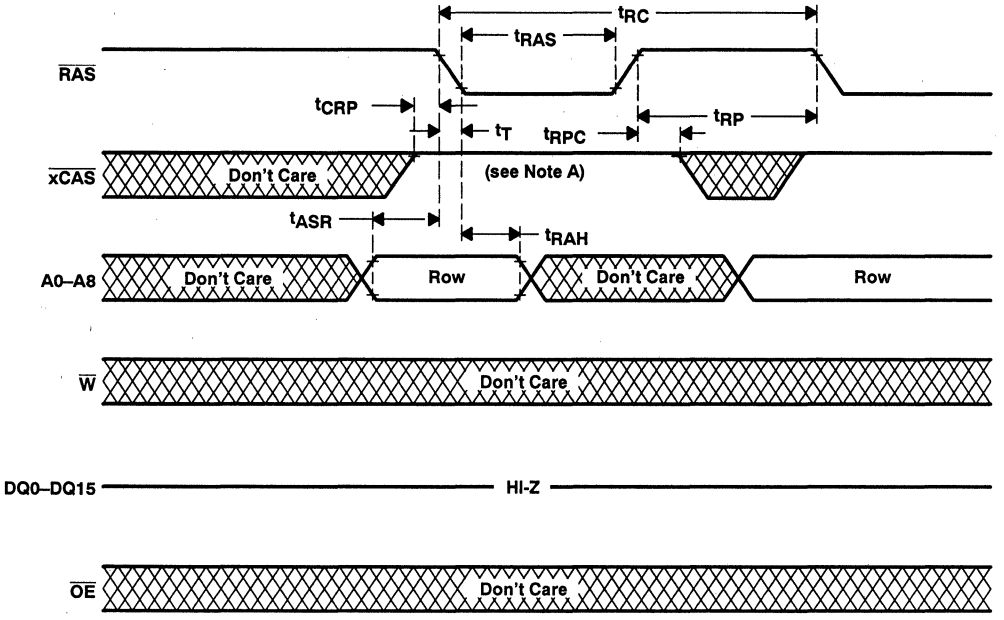
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

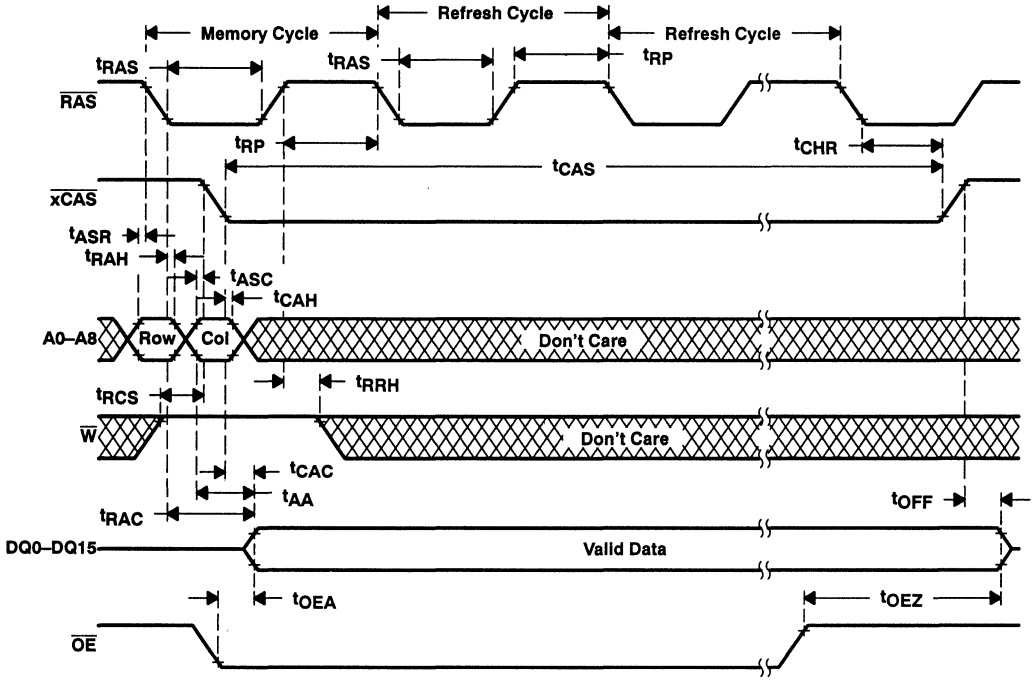
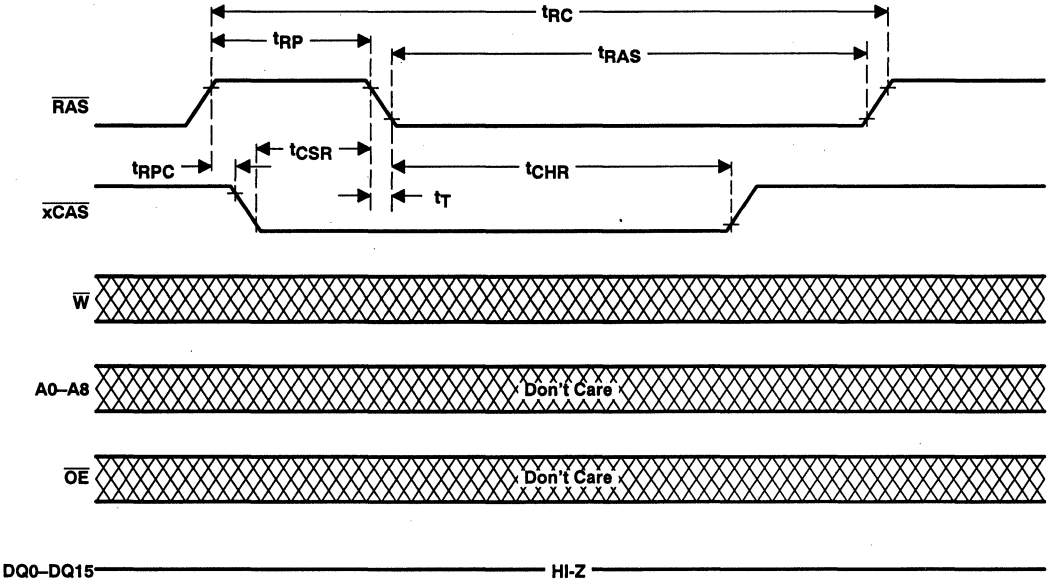


Figure 10. Hidden Refresh Cycle

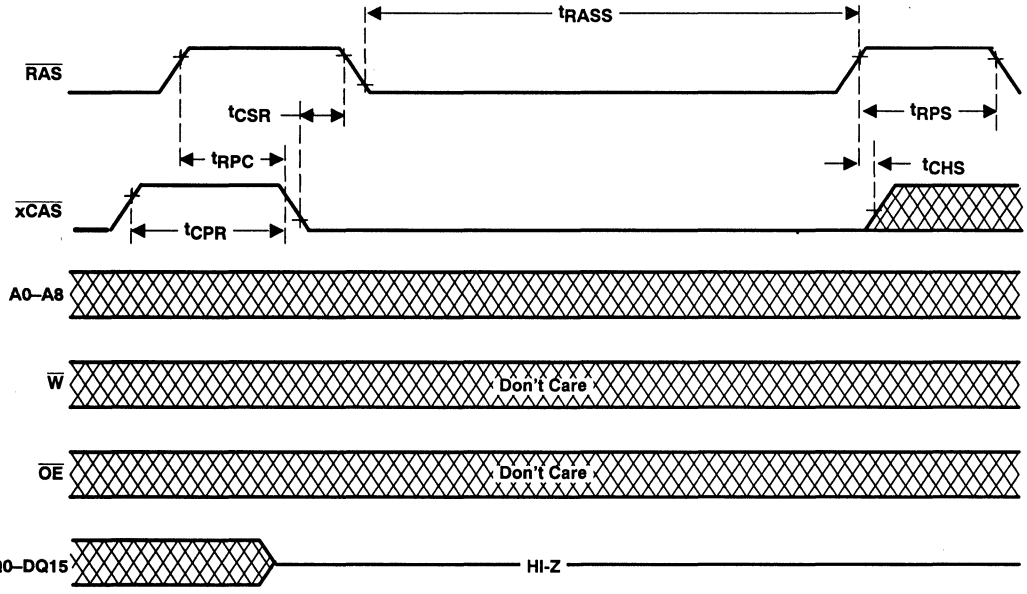
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Any $\overline{\text{xCAS}}$ may be used.
B. 512 CBR cycles must be used for CBR counter test.

Figure 11. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh Cycle Timing

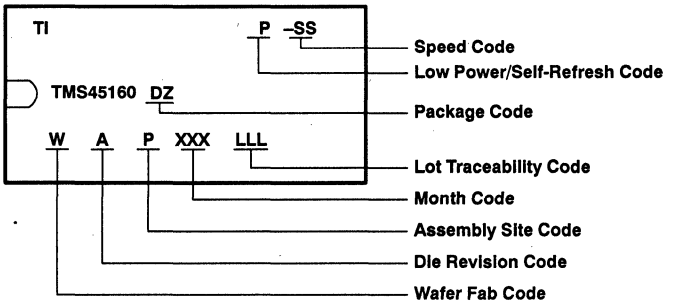
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{xCAS}$ may be used.

Figure 12. Self Refresh Timing

device symbolization



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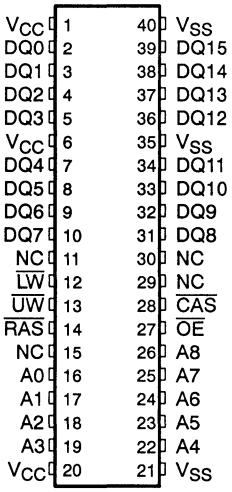
This data sheet is applicable to all TMS45165/Ps symbolized with Revision "B" and subsequent revisions as described on page 23.

- **Organization . . . 262 144 × 16**
- **Single 5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

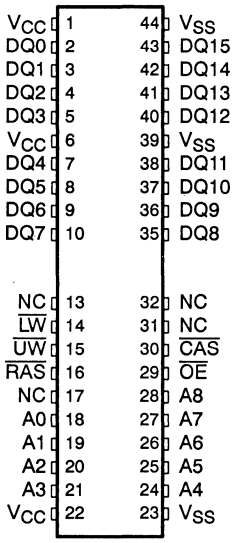
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45165/P-70	70 ns	20 ns	35 ns	130 ns
'45165/P-80	80 ns	20 ns	40 ns	150 ns
'45165/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  512-Cycle Refresh in 8 ms (Max)
  64 ms for Low Power With Self-Refresh Version (TMS45165P)
- **3-State Unlatched Output**
- **Lower Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 40-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 40/44-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range – 0°C to 70°C**
- **Low-Power With Self-Refresh**
- **Upper and Lower Byte Control During Write Operations**

DZ PACKAGE
(TOP VIEW)



DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{LW}$	Lower Write Enable
$\overline{UW}$	Upper Write Enable
$\overline{RAS}$	Row-Address Strobe
NC	No Internal Connection
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS45165 series are high-speed, 4 194 304-bit dynamic random access memories organized as 262 144 words of sixteen bits each.

The TMS45165P series are high-speed, low-power with self-refresh, 4 194 304-bit dynamic random-access memories organized as 262 144 words by sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost. These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 660 mW operating and 11 mW standby on 100 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS45165 and TMS45165P are each offered in a 40-lead plastic surface mount SOJ (DZ suffix) package, and a 40/44-lead plastic surface mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS45165 and TMS45165P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of the last $\overline{CAS}$).

address (A0–A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the TMS45165 and TMS45165P $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{UW}$, $\overline{LW}$)

The read or write mode is selected through the upper or lower write-enable ($\overline{UW}$, $\overline{LW}$) input. $\overline{LW}$ controls DQ0–DQ7, and $\overline{UW}$ controls DQ8–DQ15. A logic high on the $\overline{UW}$ and $\overline{LW}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{UW}$ or $\overline{LW}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

NOTE: Either $\overline{UW}$ or $\overline{LW}$ can be brought low in a given write cycle and only eight data bits will be written into. The user may bring both $\overline{UW}$ and $\overline{LW}$ low at the same time and all 16 data bits will be written into.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$, $\overline{UW}$, or $\overline{LW}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{UW}$ or $\overline{LW}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{UW}$ or $\overline{LW}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines. The $\overline{LW}$ pin controls DQ0–DQ7. The $\overline{UW}$ pin controls DQ8–DQ15.

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data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every eight milliseconds (64 ms for TMS45165P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR)

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS45165P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

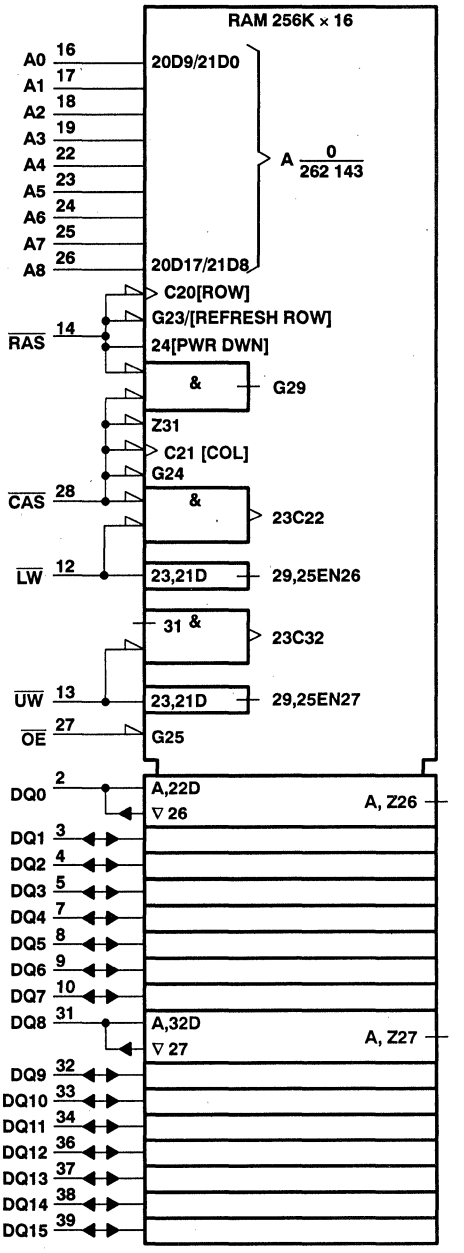
self-refresh (TMS45165P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

power up

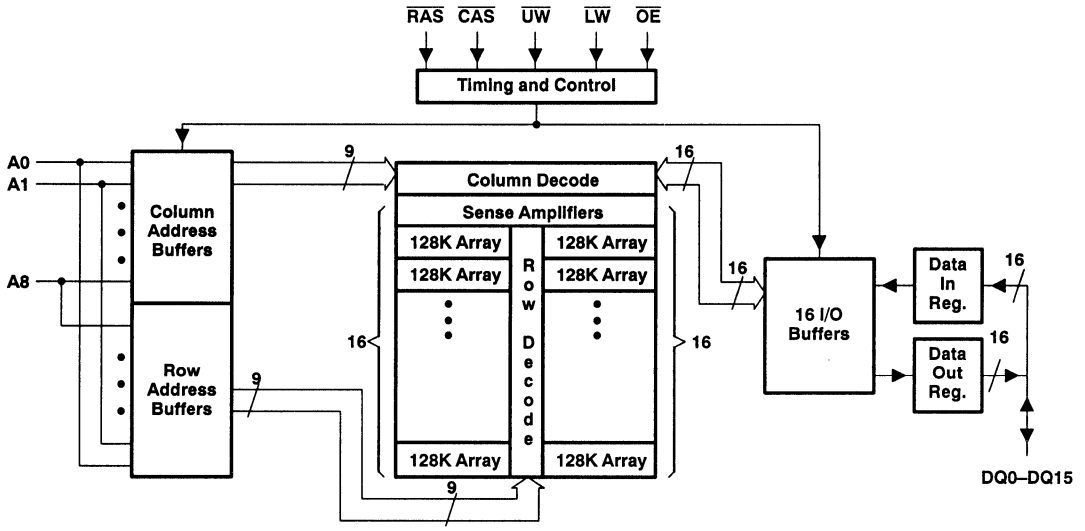
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Supply voltage range on V_{CC} . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

ADVANCE INFORMATION

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'45165-70 '45165P-70 MIN	'45165-70 '45165P-70 MAX	'45165-80 '45165P-80 MIN	'45165-80 '45165P-80 MAX	'45165-10 '45165P-10 MIN	'45165-10 '45165P-10 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			160		140		120	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'45165		1		1		1	mA
			'45165P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, ($\overline{RAS}$-only), $\overline{RAS}$ cycling, $\overline{CAS}$ high (CBR only) $\overline{RAS}$ low after $\overline{CAS}$ low			160		140		120	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			160		140		120	mA
I_{CC5}‡	Battery backup operating current (equivalent refresh time is 64 ms) (CBR only)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{UW}$, $\overline{LW}$ and $\overline{OE}$=V_{IH}, Address and Data stable			300		300		300	µA
I_{CC6}†‡	Self refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			200		200		200	µA

† Measured with outputs open.
‡ For TMS45165P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'45165-70 '46165P-70		'45165-80 '46165P-80		'45165-10 '46165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		20		20		25	ns
t_{AA}	Access time from column address		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{CLZ}	$\overline{CAS}$ low to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	20	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	20	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 8)	130		150		180		ns
t_{WC}	Write cycle time	130		150		180		ns
t_{RWC}	Read-modify-write cycle time	185		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	45		50		55		ns
t_{PRWC}	Page-mode read-modify-write cycle time	90		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Write pulse duration	15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{xW}$ low (see Note 12)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{xW}$-low setup time before $\overline{CAS}$ high	20		20		25		ns
t_{RWL}	$\overline{xW}$-low setup time before $\overline{RAS}$ high	20		20		25		ns
t_{WCS}	$\overline{xW}$-low setup time before $\overline{CAS}$ low (see Note 13)	0		0		0		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 15)	35		35		45		ns
t_{DH}	Data hold time after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 15)	35		35		45		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 16)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 16)	0		0		0		ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
8. All cycle times assume t_T = 5 ns.
9. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
12. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
13. Early write operation only.
14. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
15. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7) (concluded)

	PARAMETER	'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low (see Note 13)	15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 15)	35		35		45		ns
t_{AWD}	Delay time, column address to $\overline{xW}$ low (see Note 17)	65		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 14)	15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 14)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{xW}$ low (see Note 17)	50		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	20		20		25		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	20		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 18)	15	35	15	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)	20	50	20	60	25	75	ns
t_{RPC}	Delay time, RAS high to CAS low (see Note 14)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{xW}$ low (see Note 17)	100		110		135		ns
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		180		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{REF}	Refresh time interval (TMS45165 only)		8		8		8	ms
t_{REF}	Refresh time interval, low power (TMS45165P only)		64		64		64	ms
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high	−50		−50		−50		ns
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
13. Early write operation only.
14. $\overline{CAS}$-before-$\overline{RAS}$ refresh only
15. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
17. Read-modify-write operation only.
18. Maximum value specified only to assure access time.

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PARAMETER MEASUREMENT INFORMATION

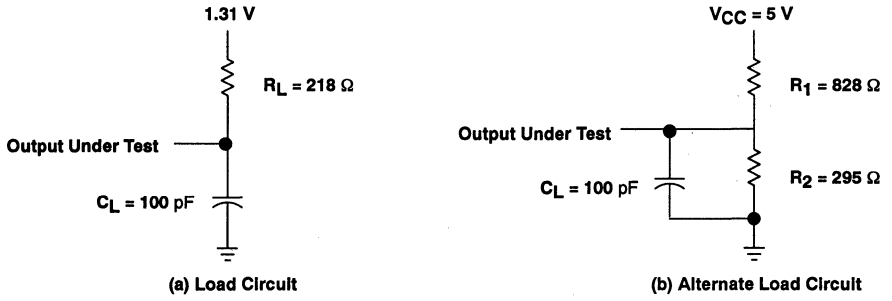

Figure 1. Load Circuits for Timing Parameters

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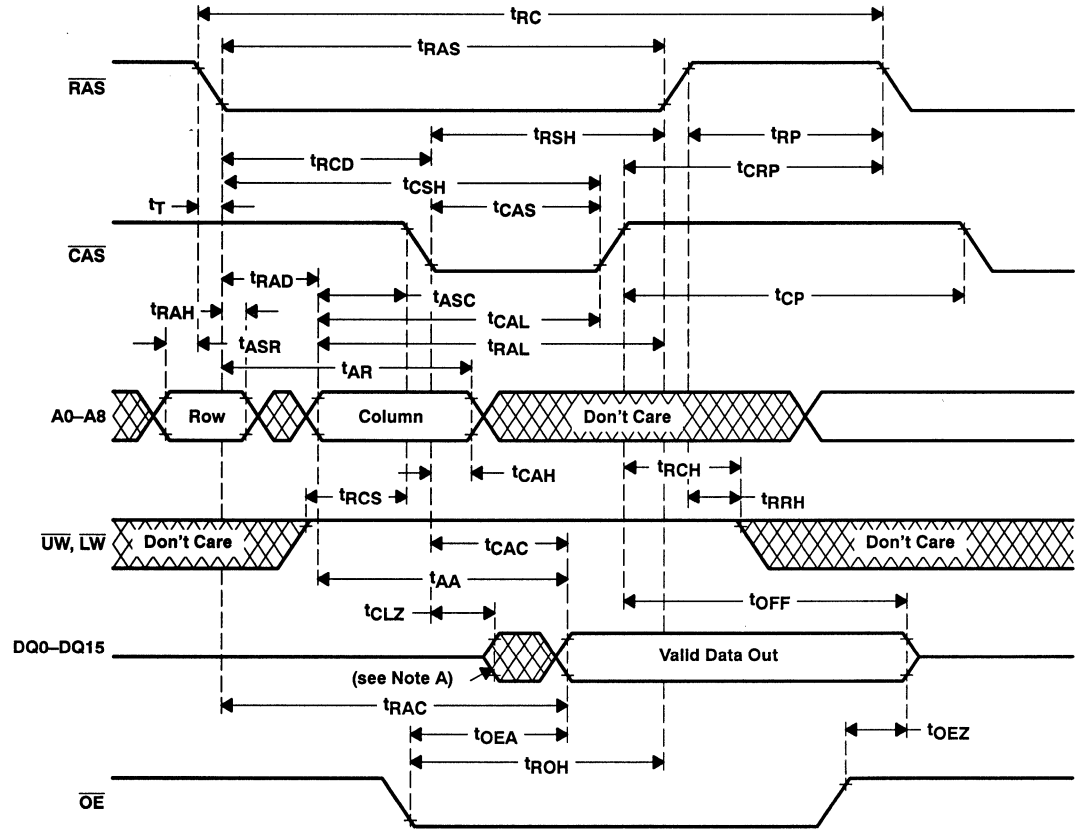
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

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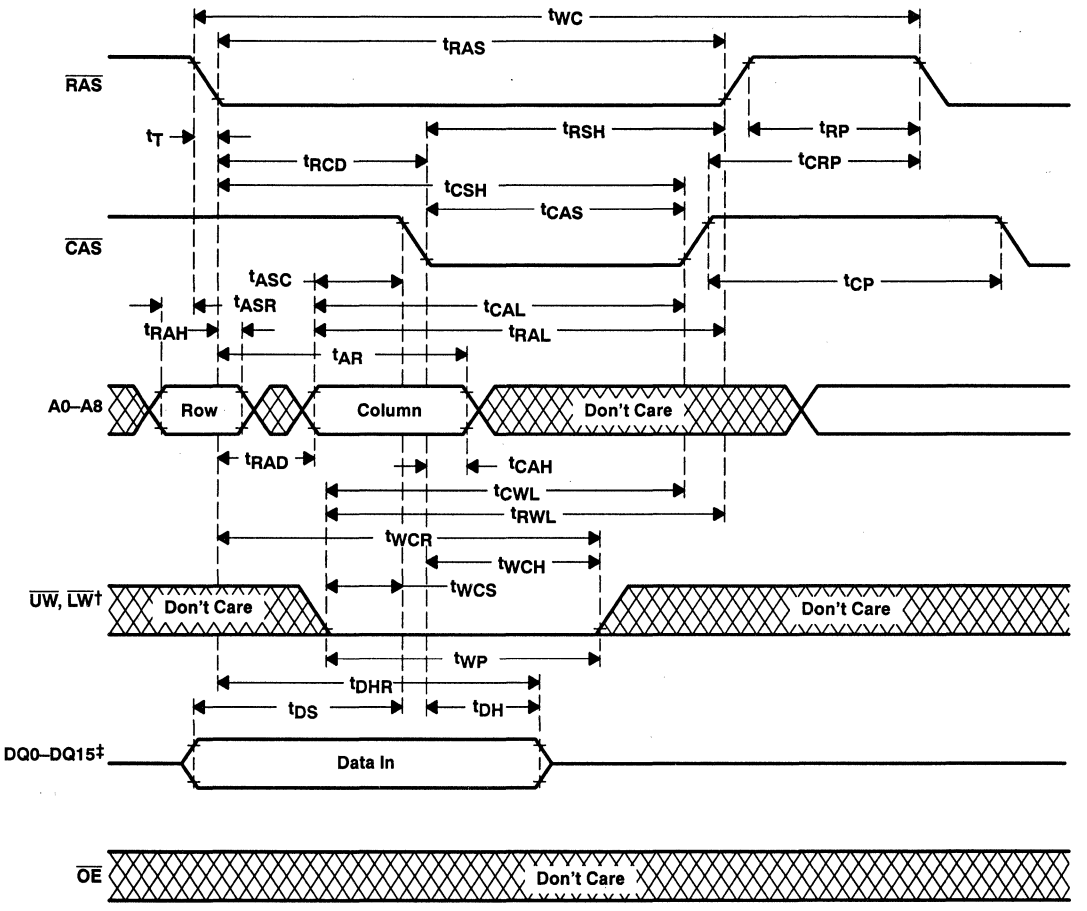
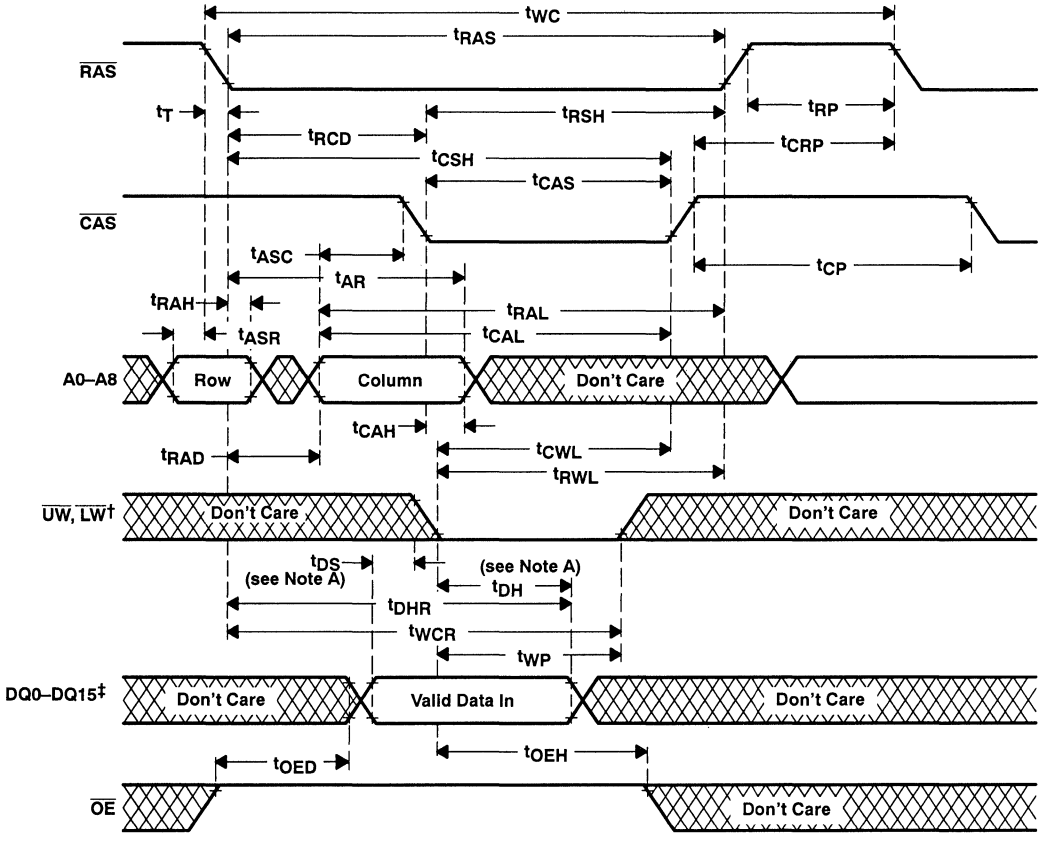
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ may be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ may be brought low at the same time and all 16 DQ locations will be written into.
‡ All DQ pins remain in the HI-Z state for an early write cycle.

Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

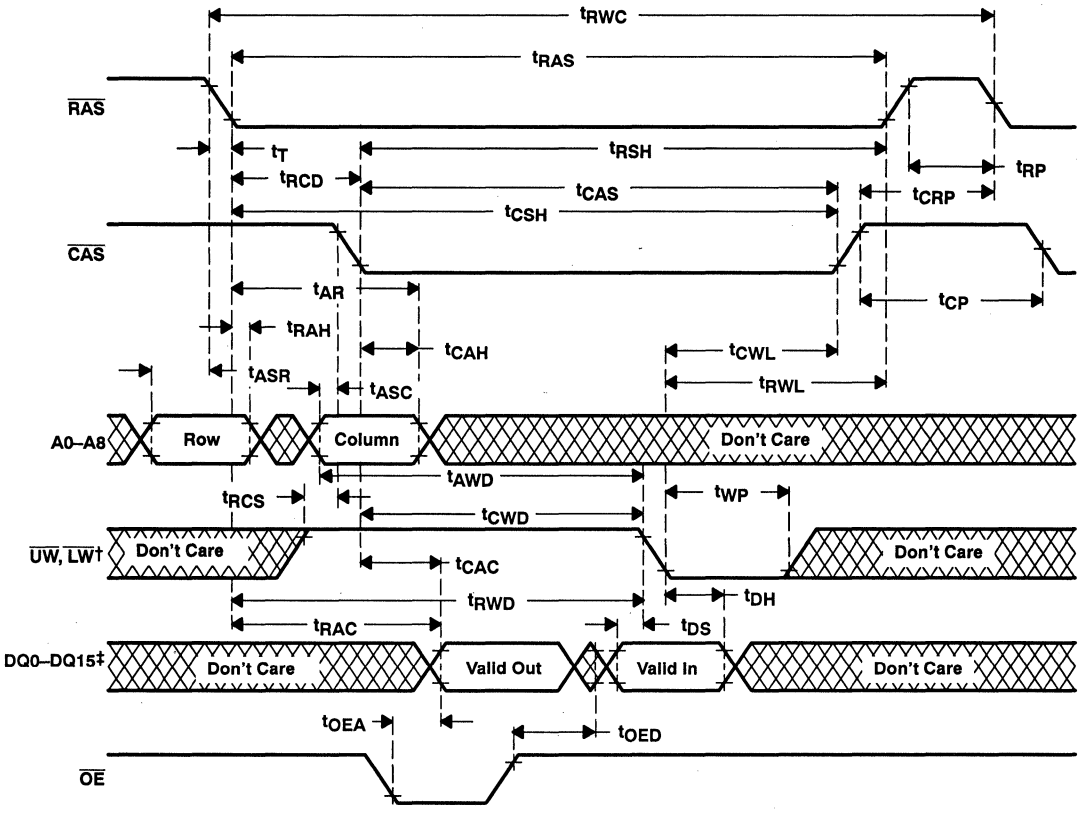


† Either $\overline{UW}$ or $\overline{LW}$ may be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ may be brought low at the same time and all 16 DQ locations will be written into.
‡ All DQ pins remain in the HI-Z state while $\overline{OE}$ is high.
NOTE A: Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.

Figure 4. Write Cycle Timing

ADVANCE INFORMATION

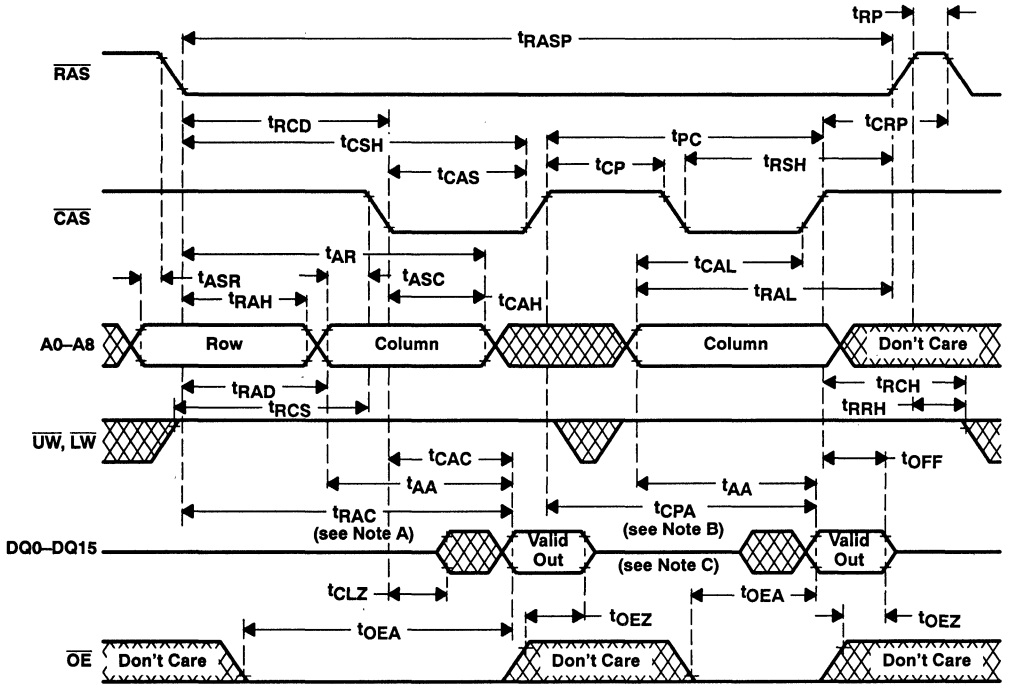
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ may be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ may be brought low at the same time and all 16 DQ locations will be written into.
‡ All DQ pins remain in the HI-Z state for an early write cycle.

Figure 5. Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

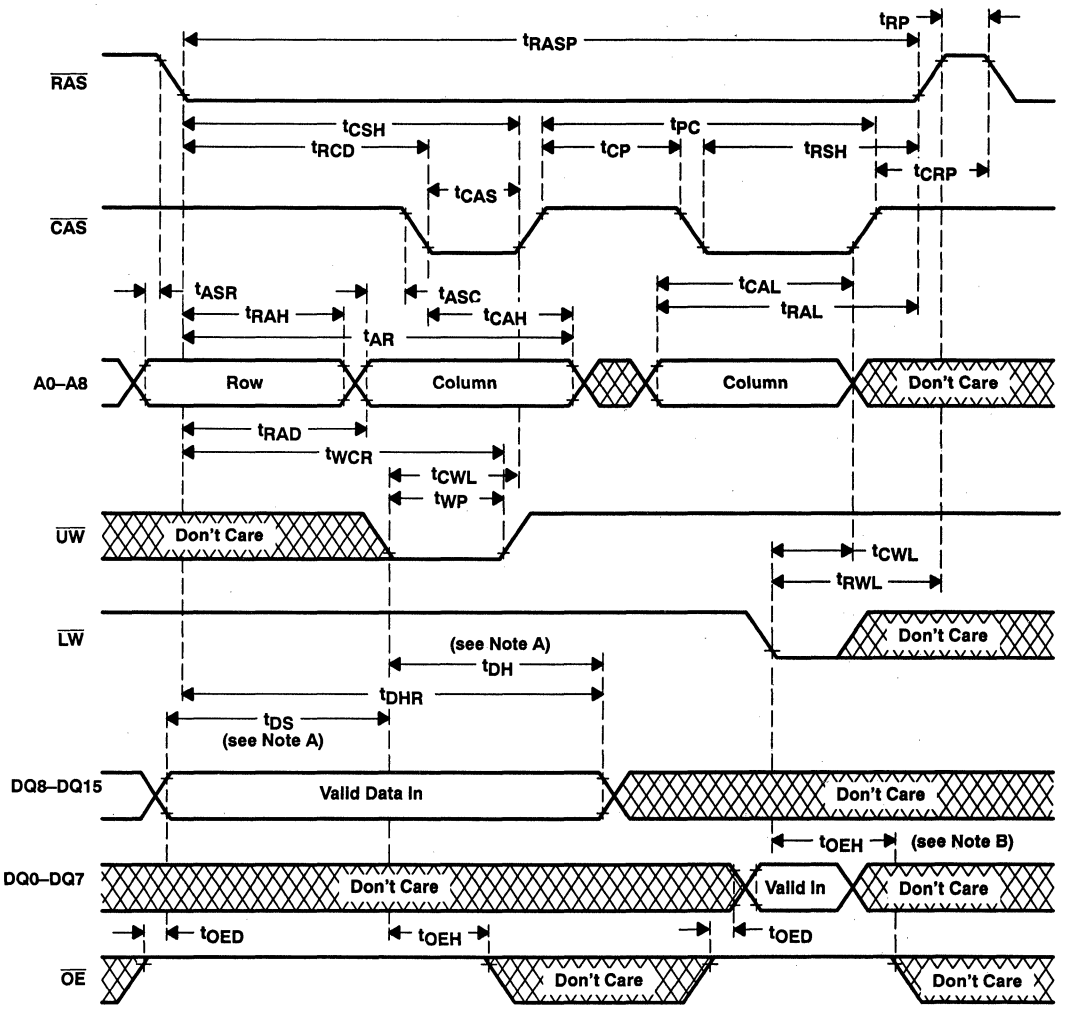


NOTES: A. Output may go from high impedance to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

ADVANCE INFORMATION

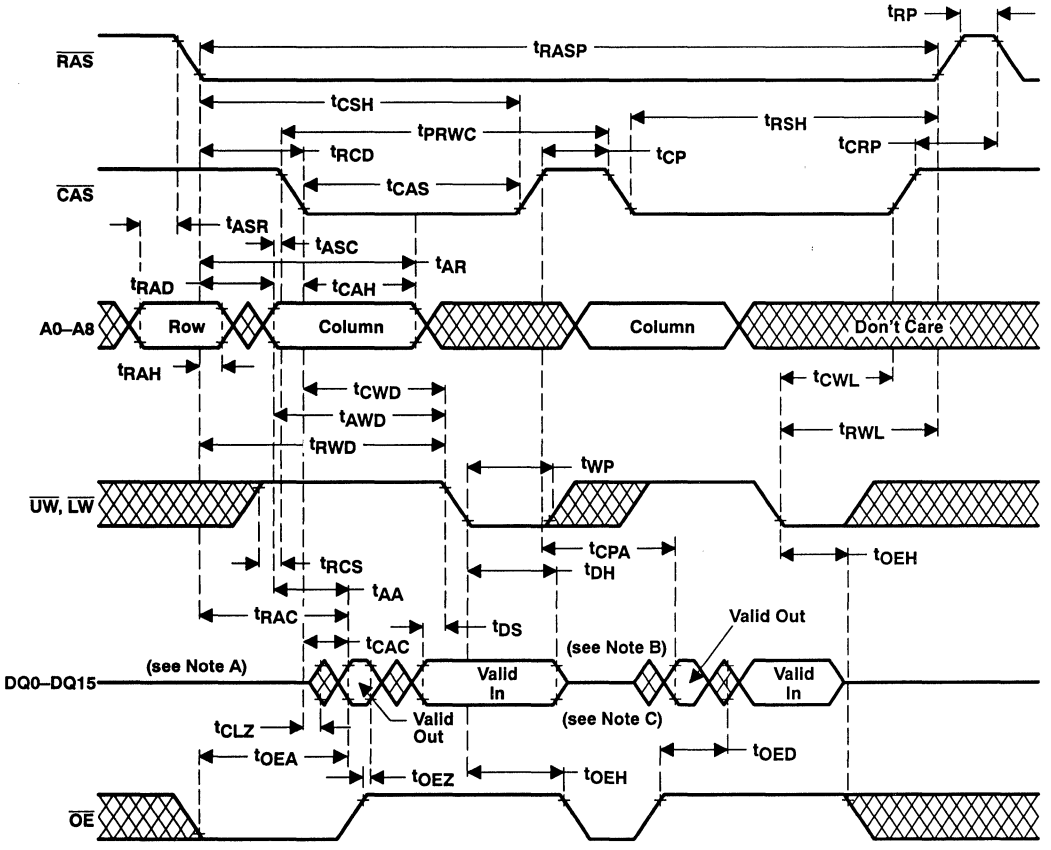
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from high impedance to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
C. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

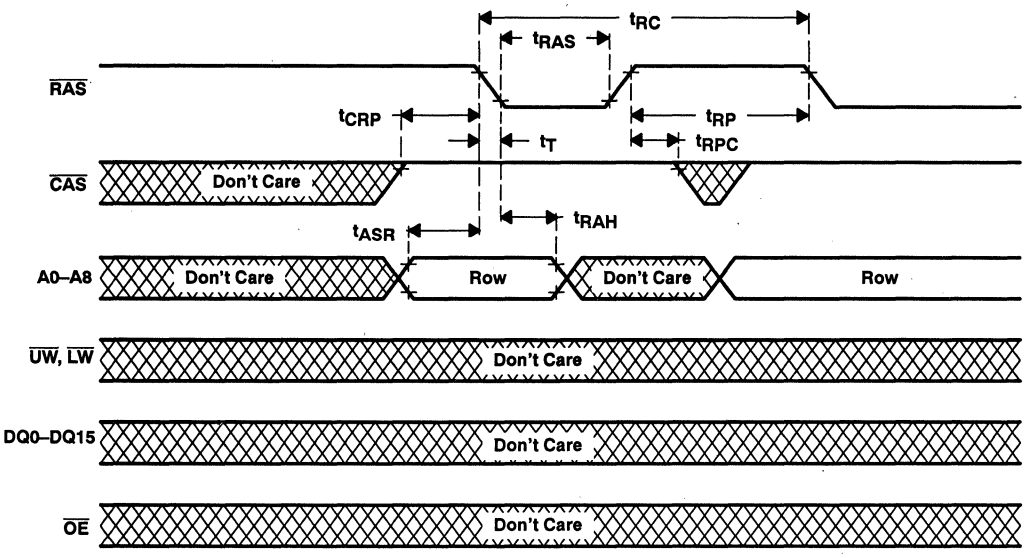


Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

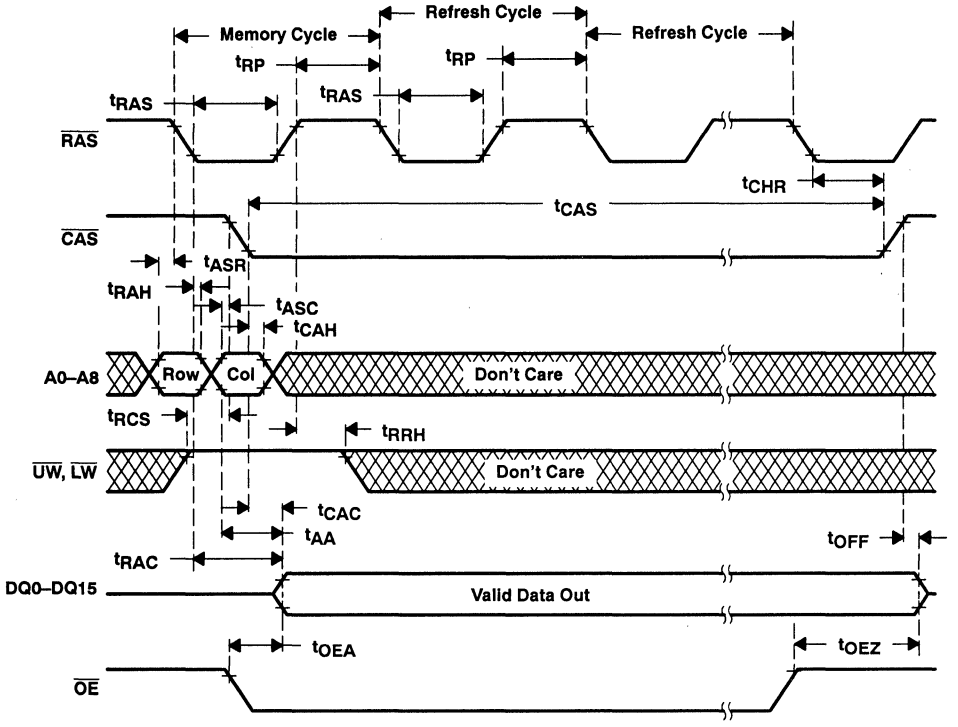
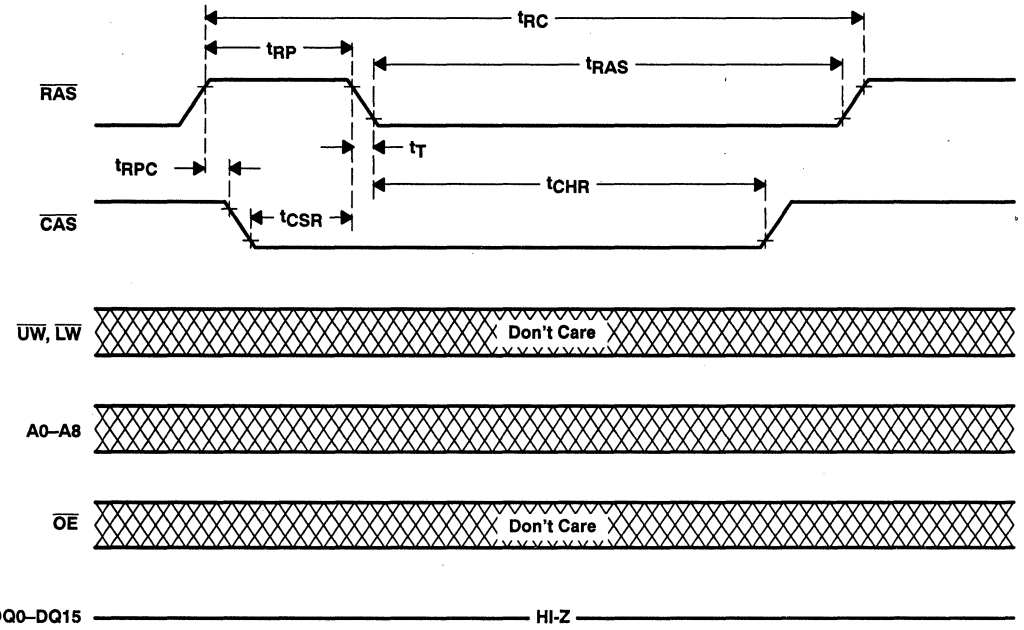


Figure 10. Hidden Refresh Cycle

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: 512 CBR cycles must be used for CBR counter test.

Figure 11. Automatic (CAS-Before-RAS) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

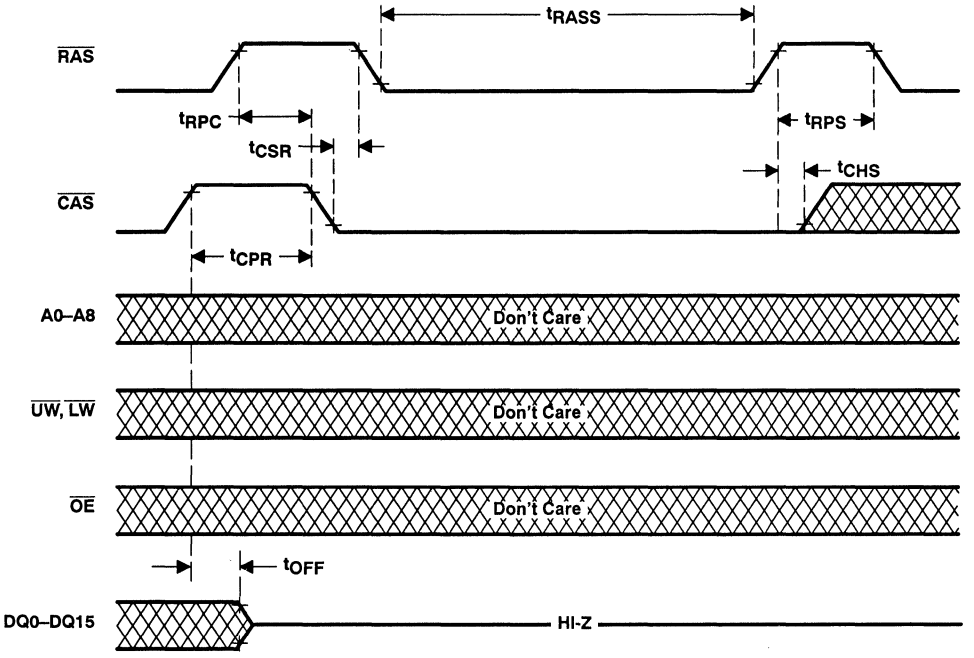
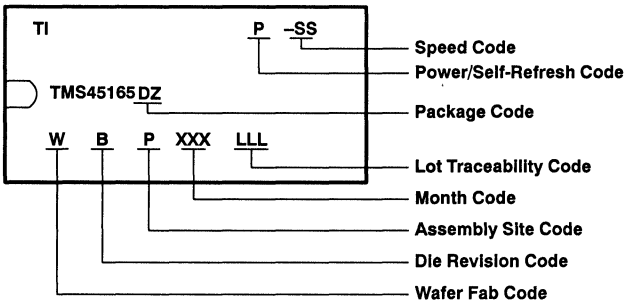


Figure 12. Self Refresh Timing

device symbolization



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This data sheet is applicable to all TMS416100s symbolized with Revision "A" and subsequent revisions as described on page 22.

- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS416100-60	60 ns	15 ns	30 ns	110 ns
TMS416100-70	70 ns	18 ns	35 ns	130 ns
TMS416100-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycle Refresh in 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

description

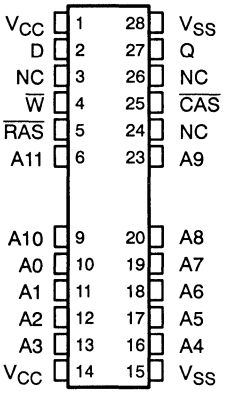
The TMS416100 series are high-speed, 16 777 216-bit dynamic random-access memories, organized as 16 777 216 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

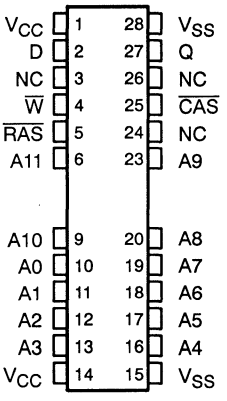
All inputs, outputs, and clocks are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416100 is offered in 400-mil 24/28-pin surface mount SOJ (DZ suffix) and 400-mil 24/28-pin surface mount thin SOP (DGC and DGD suffixes) packages. This device is characterized for operation from 0°C to 70°C.

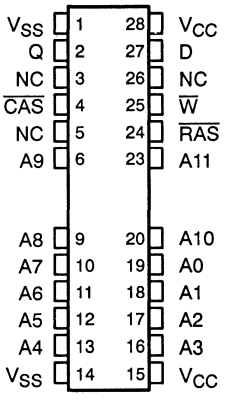
DZ PACKAGE†
(TOP VIEW)



DGC PACKAGE†
(TOP VIEW)



DGD PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
Q	Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

The column address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS416100 to operate at a higher data bandwidth than conventional page-mode parts since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if tAA max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. Twelve column-address bits are set on inputs A0–A11 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the fallling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

refresh

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

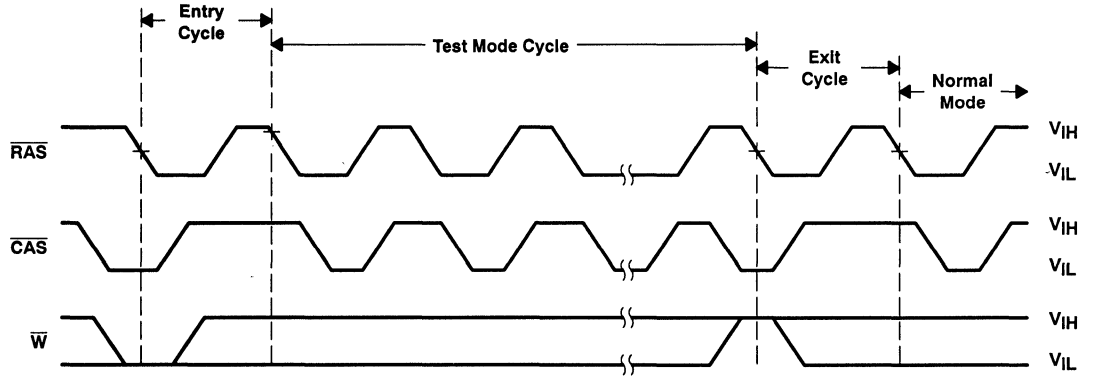
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits the test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

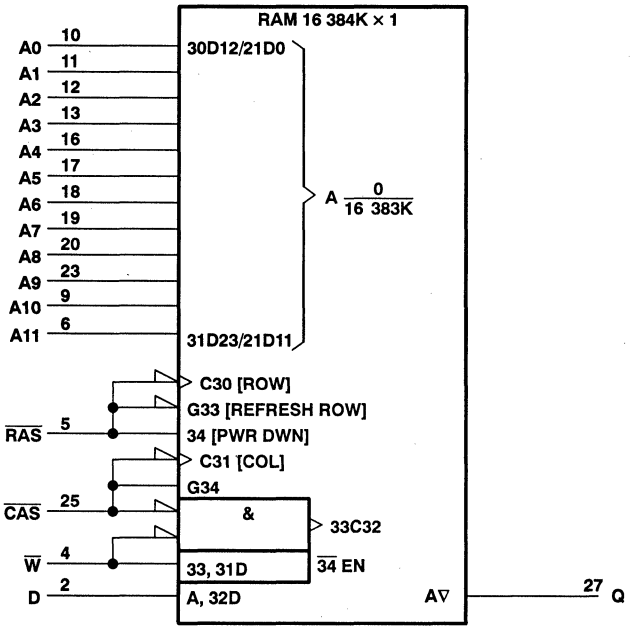
Test mode causes the part to be internally reconfigured into a 1024K × 16 bit device with 16-bit parallel read and write data path. Column addresses CA0, CA1, CA10, and CA11 are not used. During a read cycle all 16 bits of the internal data bus are compared. If all bits are the same data state, the output pin will go high. If one or more bits disagree, the output pin will go low. Test time in test mode can thus be reduced by a factor of 16, compared to normal memory mode.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

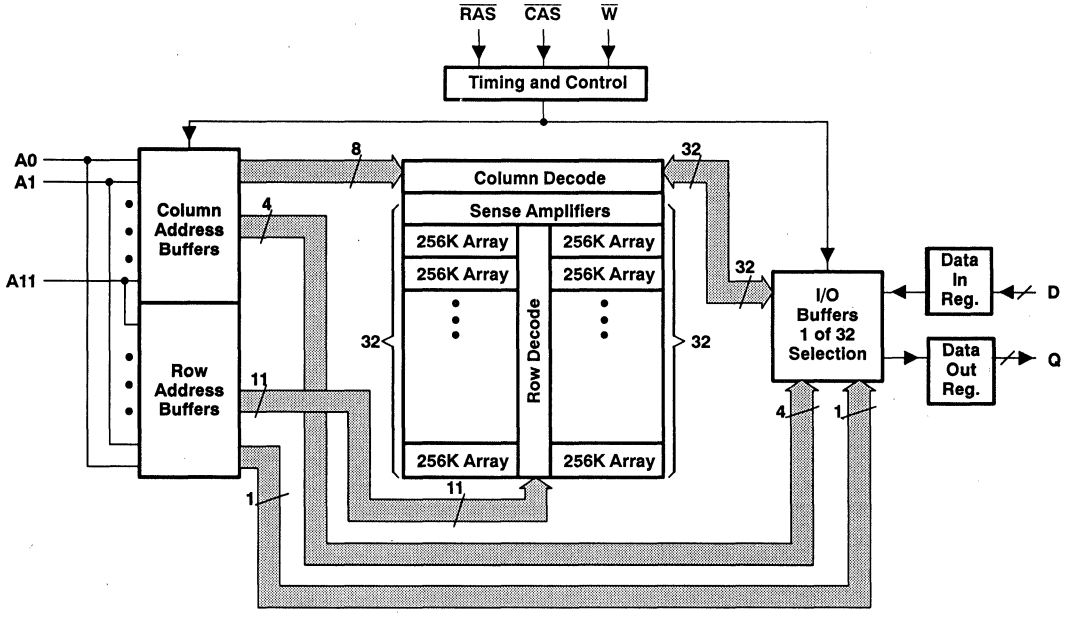
Figure 1. Test Mode Cycle†

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 24/28 pin SOJ package (DZ suffix) and the 24/28-pin thin SOP package (DGC suffix).

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note1) ..... – 1 V to 7 V
Voltage range, V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS416100-60		TMS416100-70		TMS416100-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Notes 3 and 5)	Minimum cycle, V_{CC} = 5.5 V		90		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} –0.2 V (CMOS)		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 and 5)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70	mA
I_{CC4}	Average page current (see Notes 4 and 5)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50	mA
I_{CC7}	Standby current output enable (see Note 5)‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.
5. Measured with no load connected.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(D)}$	Input capacitance, data inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 6: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416100-60		TMS416100-70		TMS416100-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS416100-60		TMS416100-70		TMS416100-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 8)	110		130		150		ns
t_{RWC}	Read-write cycle time	130		153		175		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 12)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns

Continued next page.

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		TMS416100-60		TMS416100-70		TMS416100-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		ns
t_{CPRH}	$\overline{RAS}$ hold time form $\overline{CAS}$ precharge	35		40		45		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	35		40		45		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

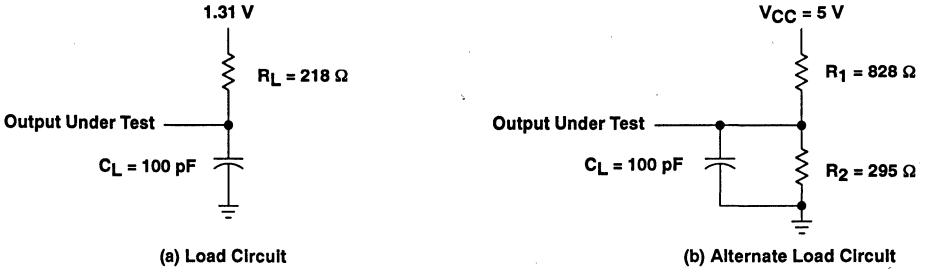

Figure 2. Load Circuits for Timing Parameters

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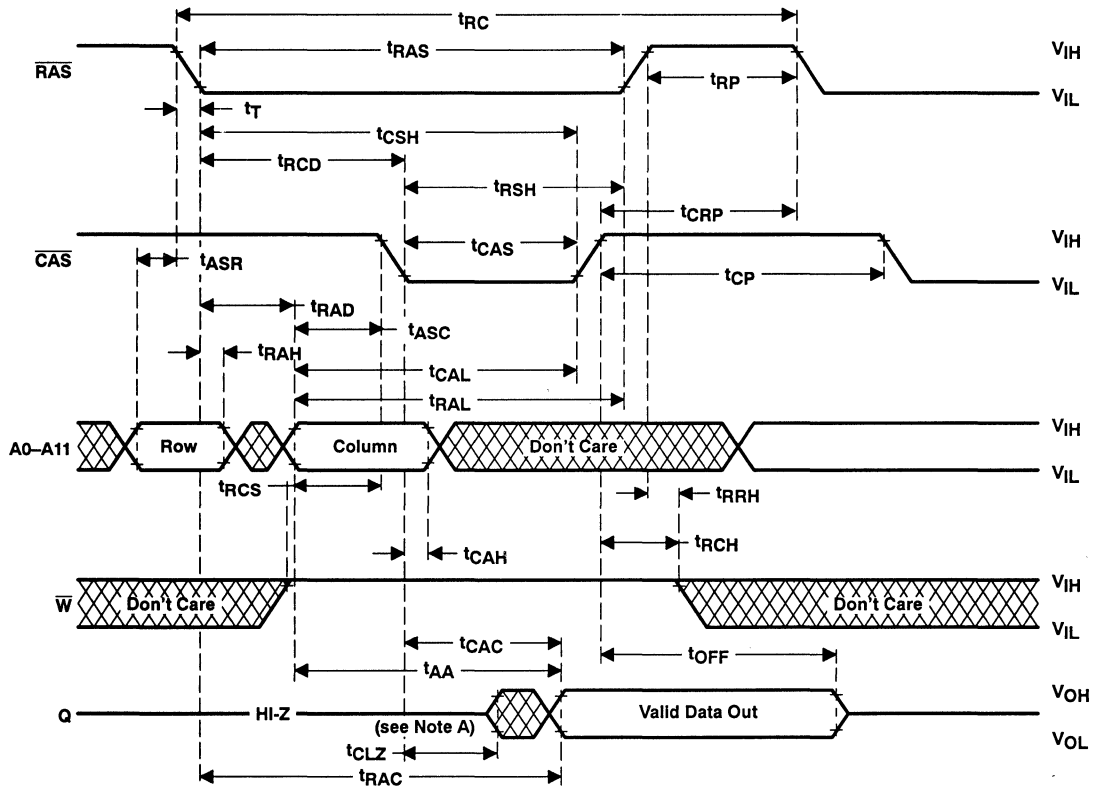
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

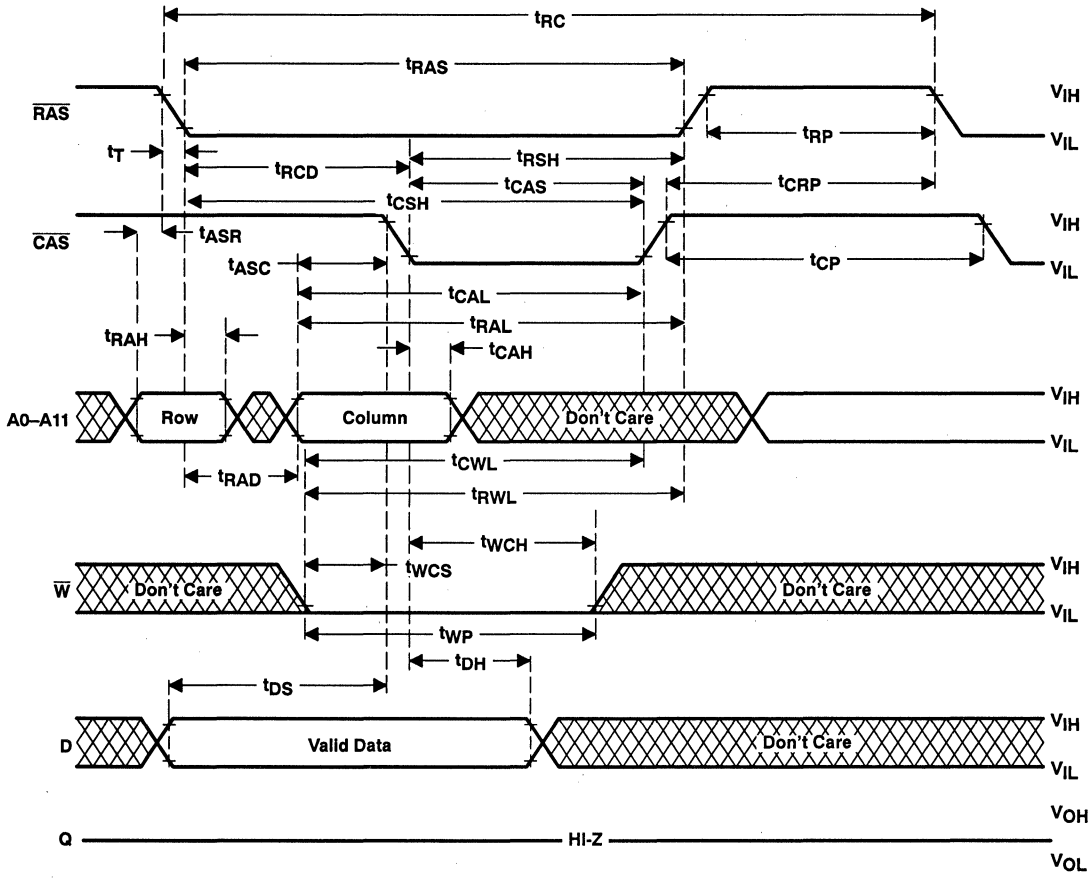


Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

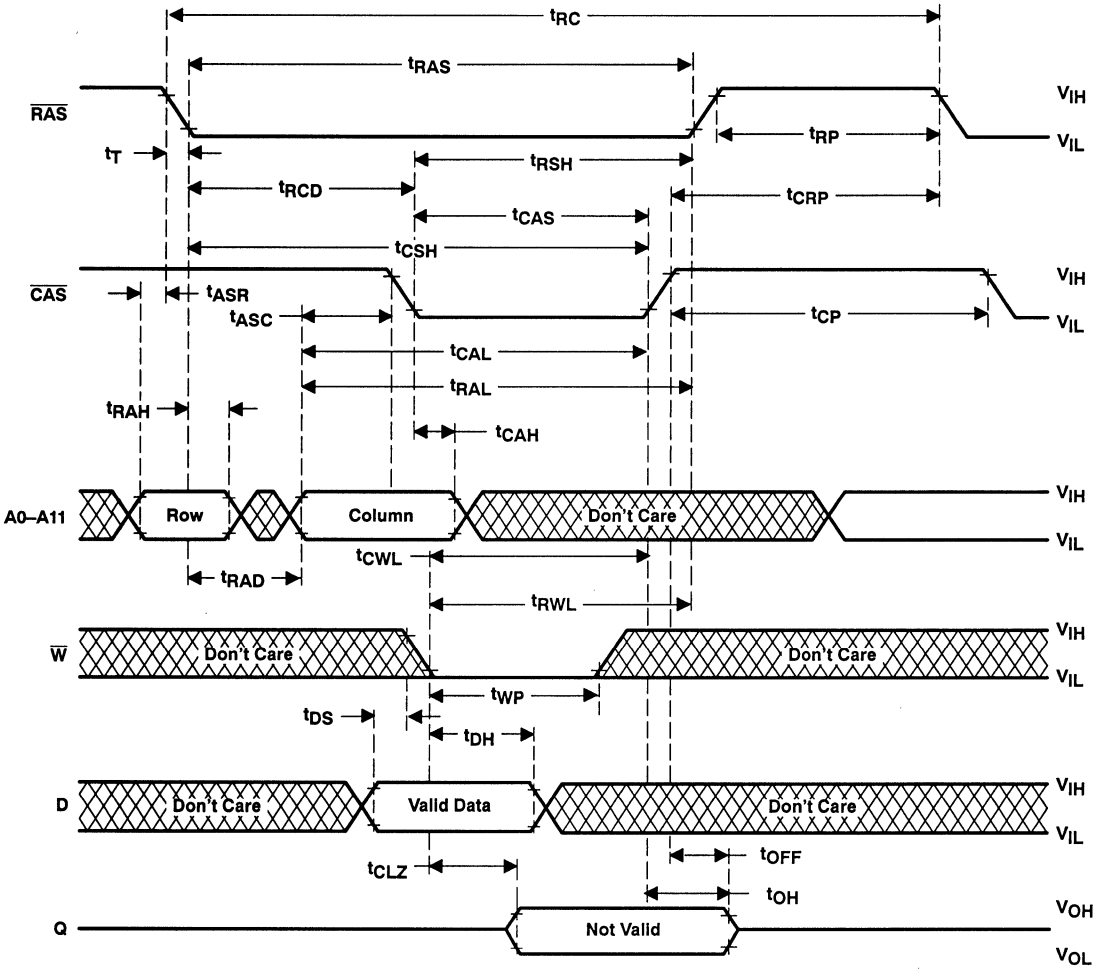
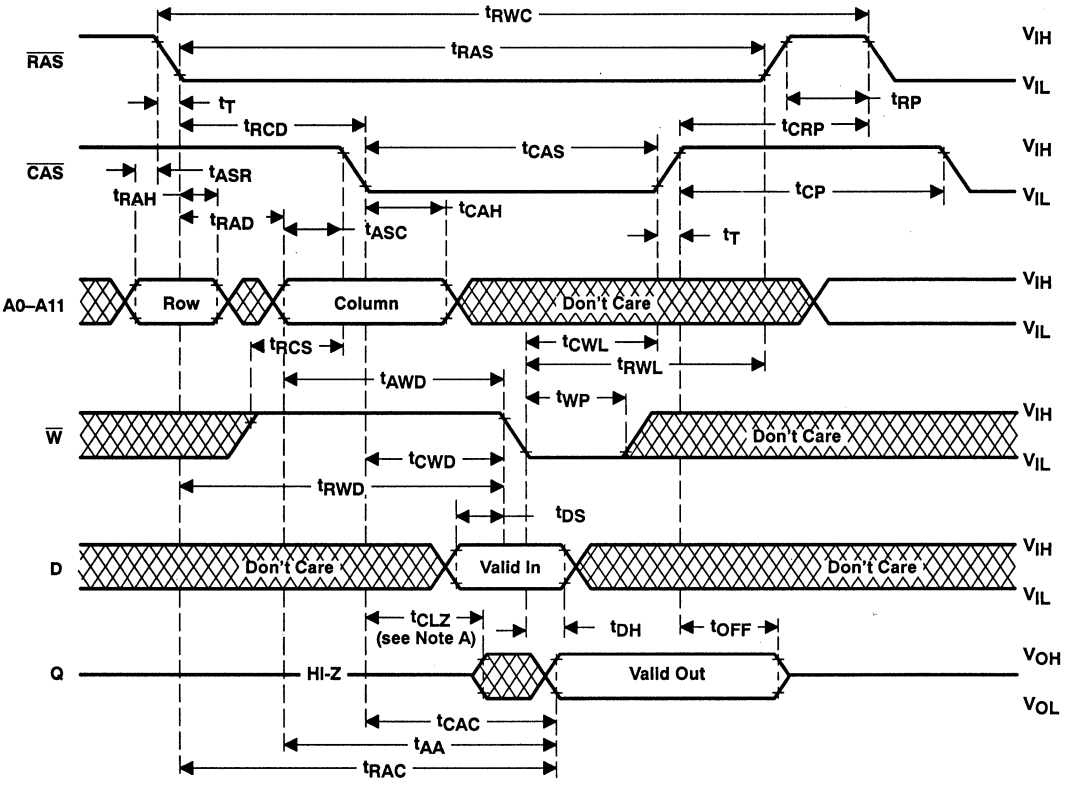


Figure 5. Write Cycle Timing

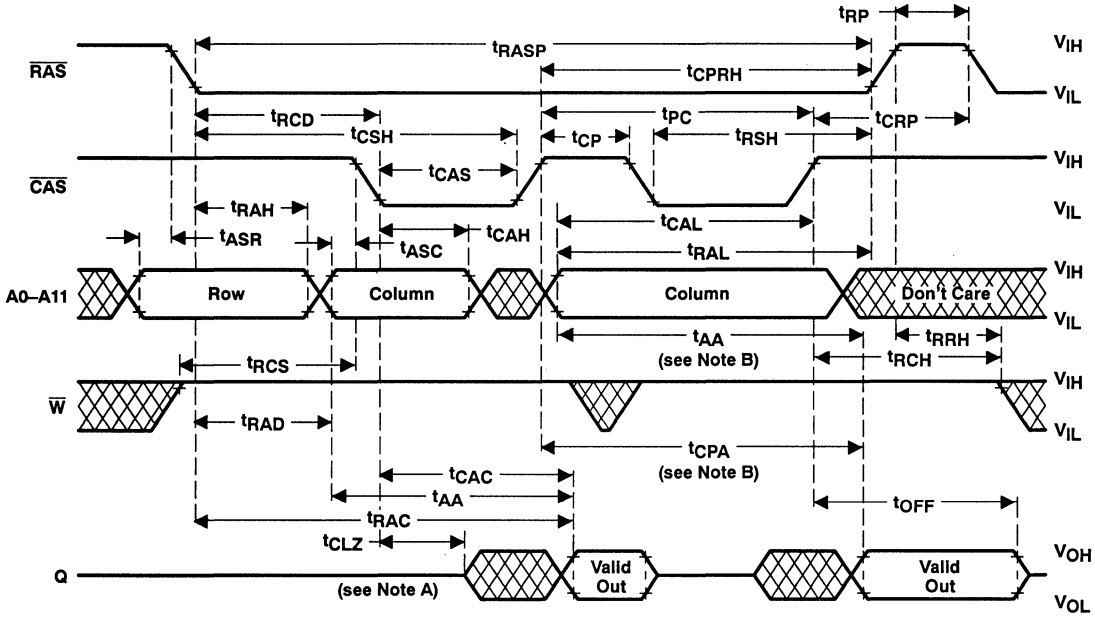
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

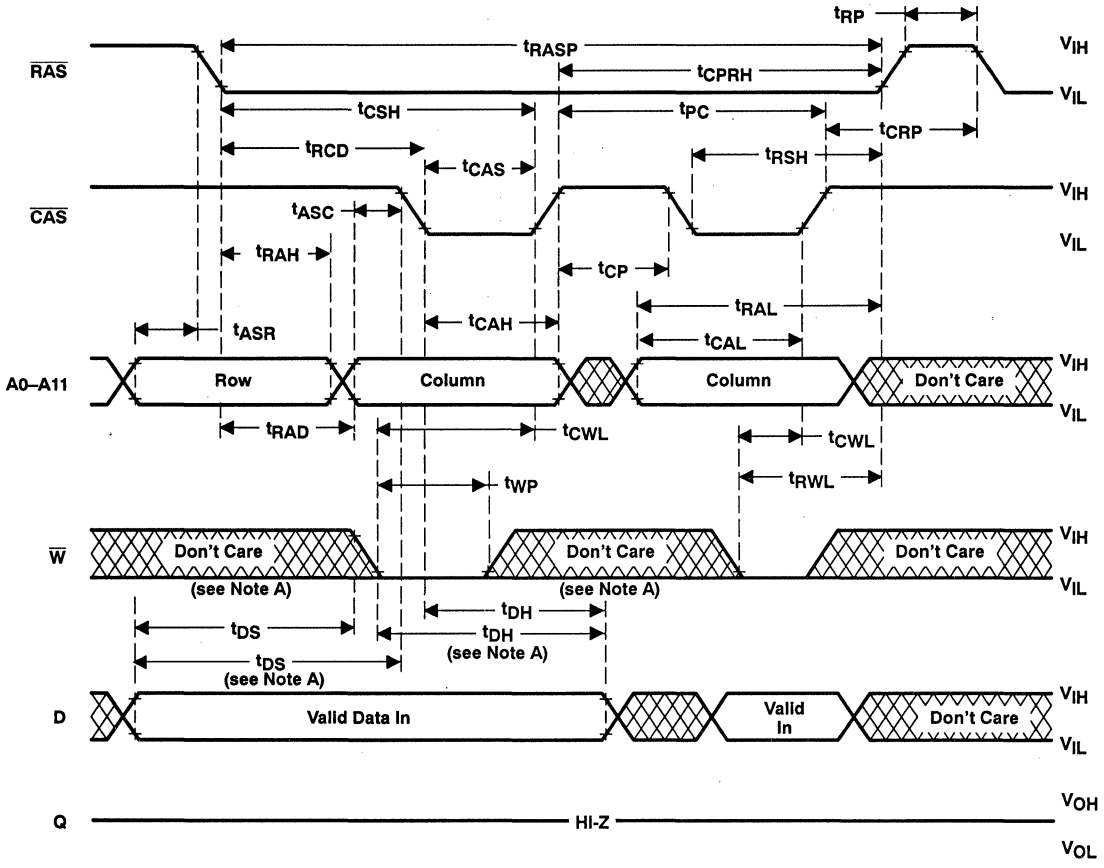
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

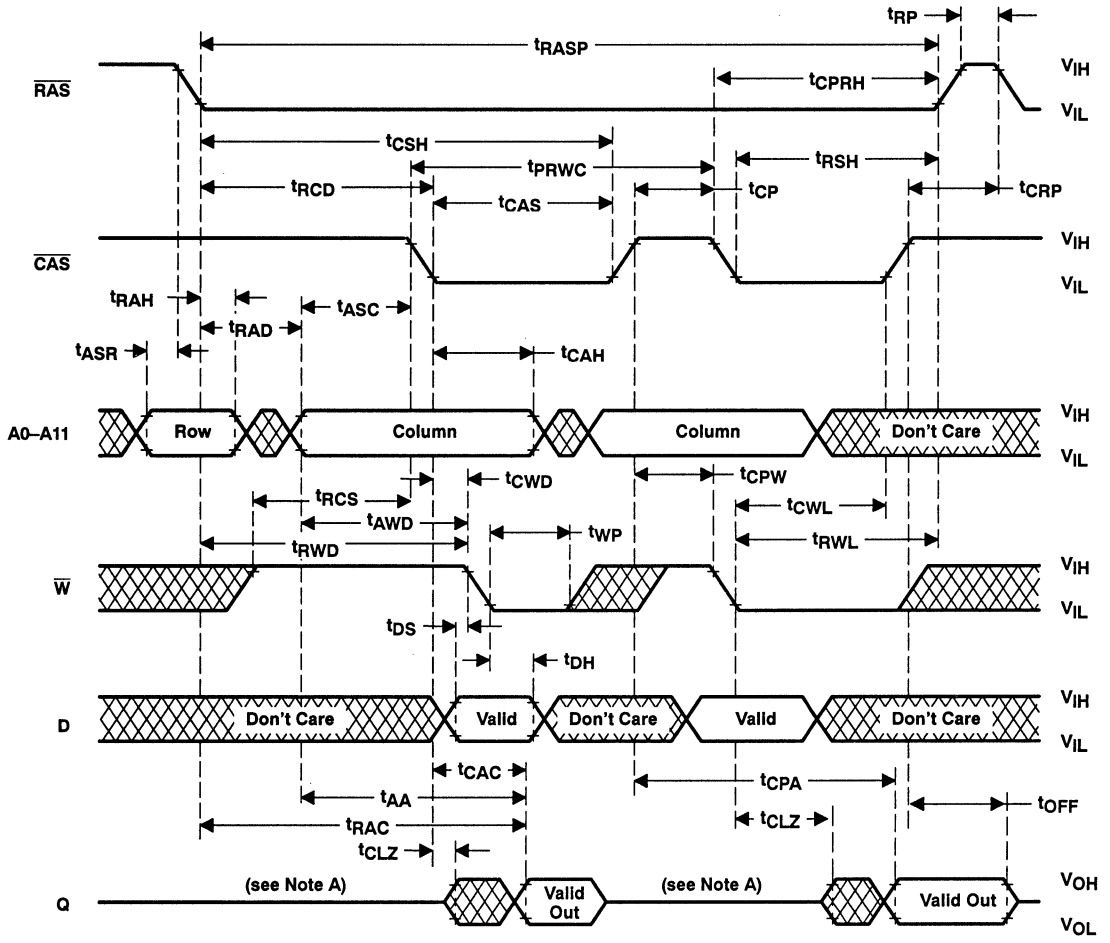
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

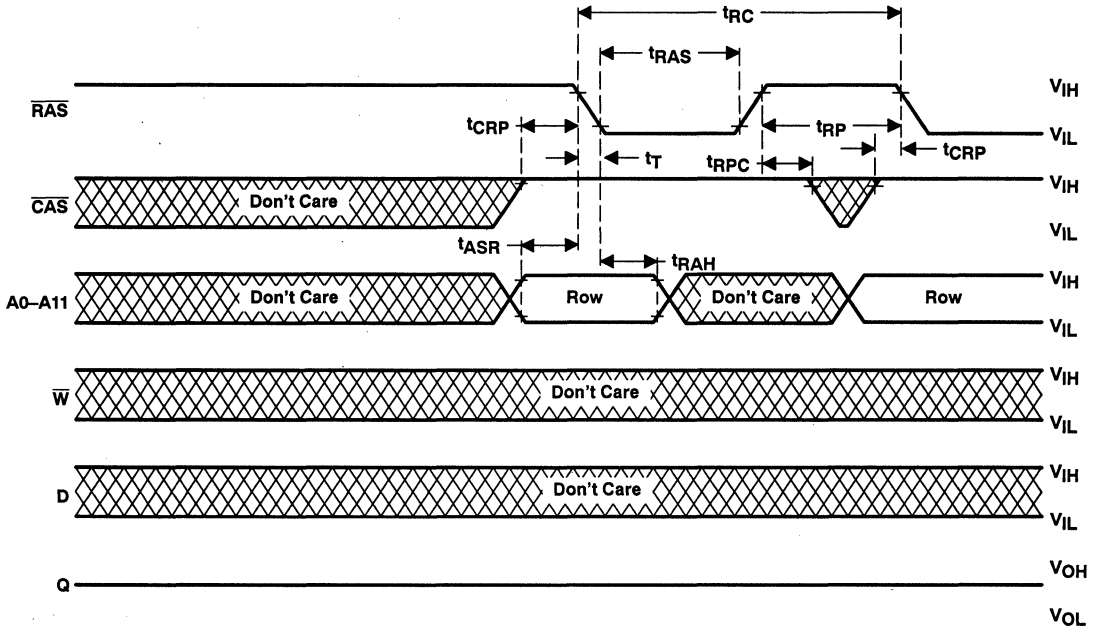


Figure 10. $\overline{RAS}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

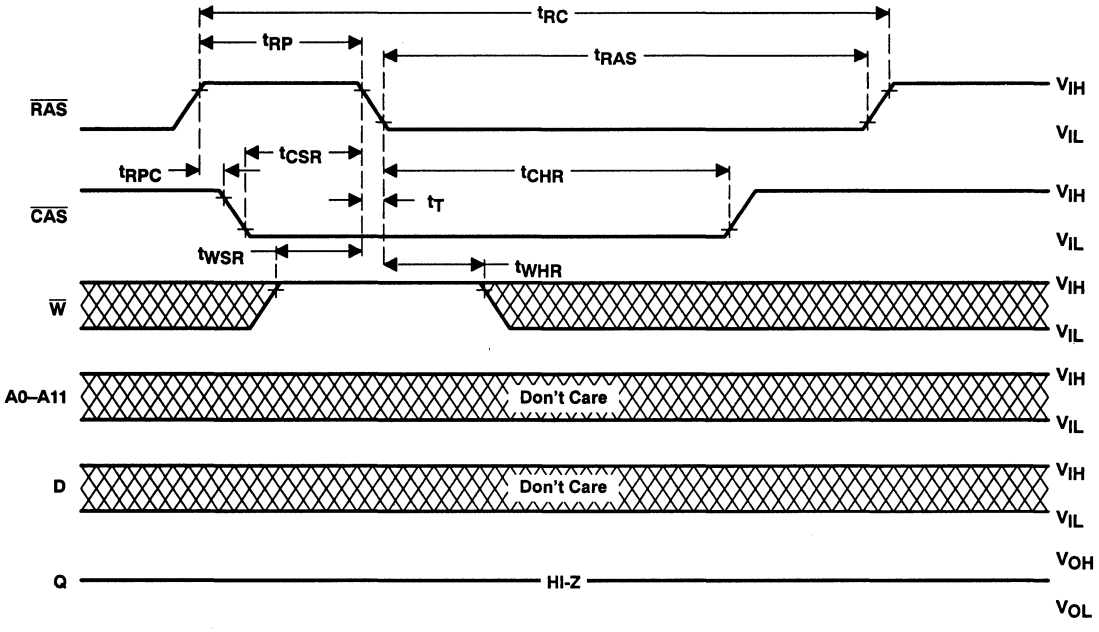

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

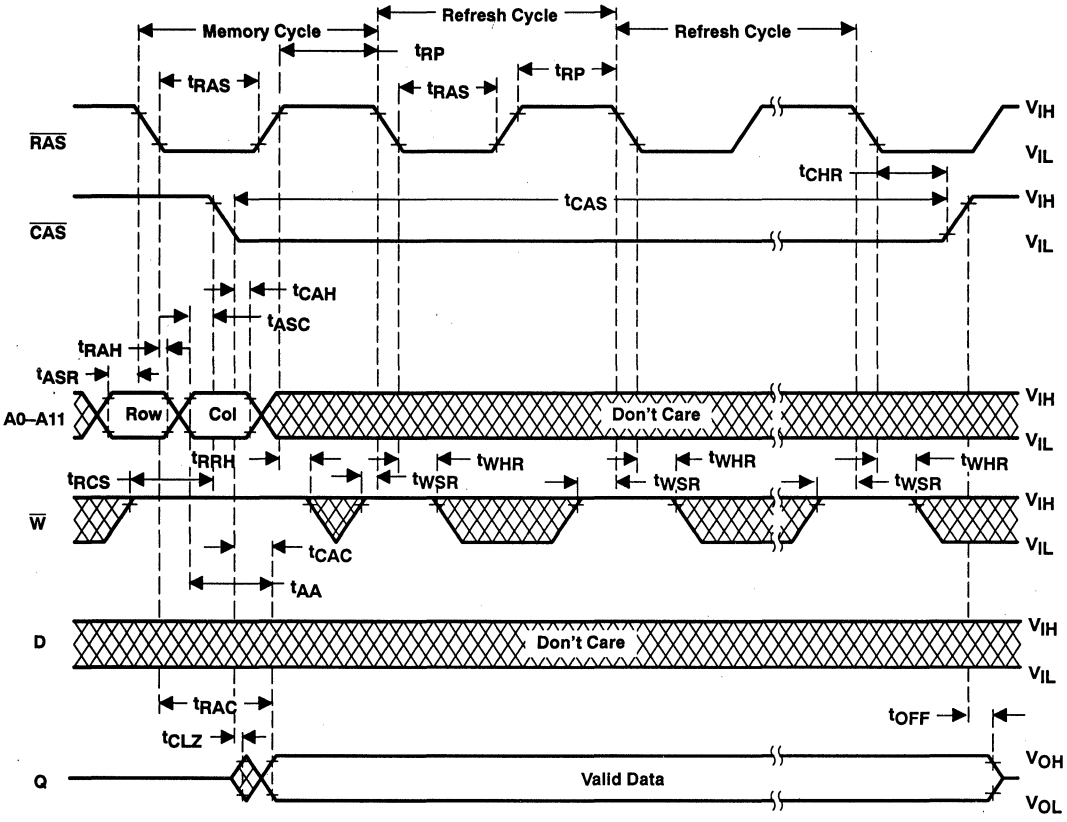

Figure 12. Hidden Refresh Cycle (Read) Timing

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PARAMETER MEASUREMENT INFORMATION

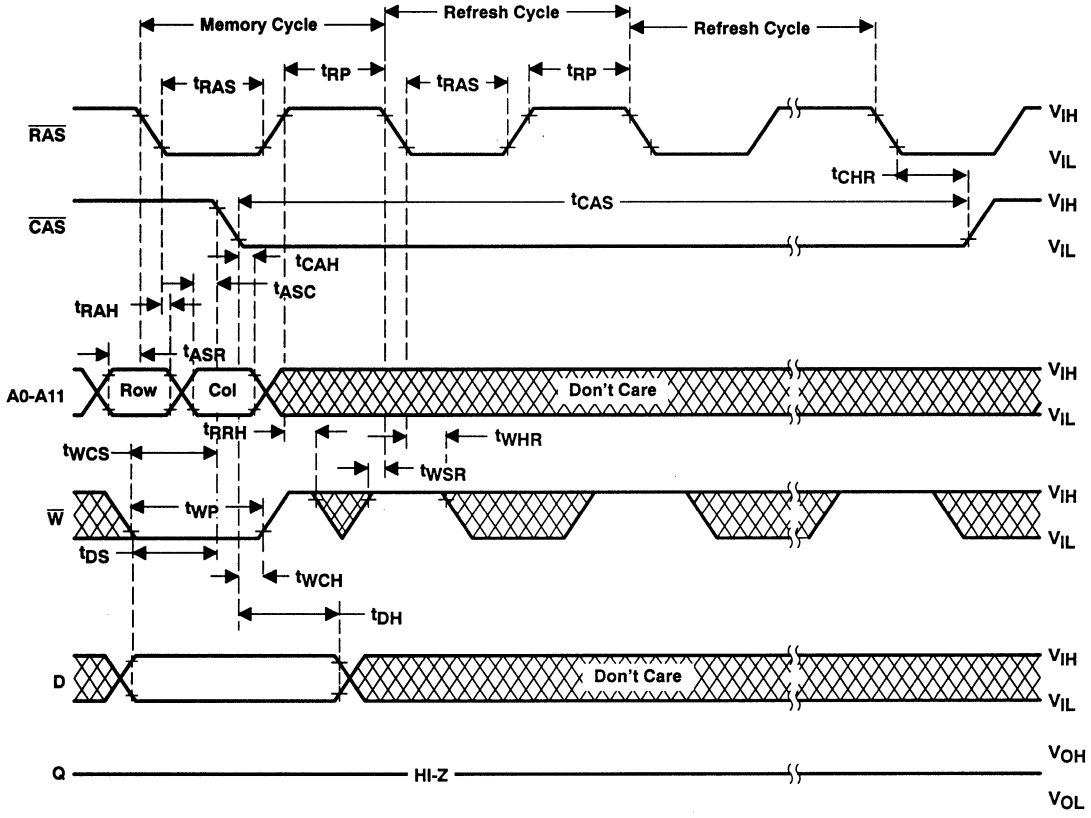


Figure 13. Hidden Refresh Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

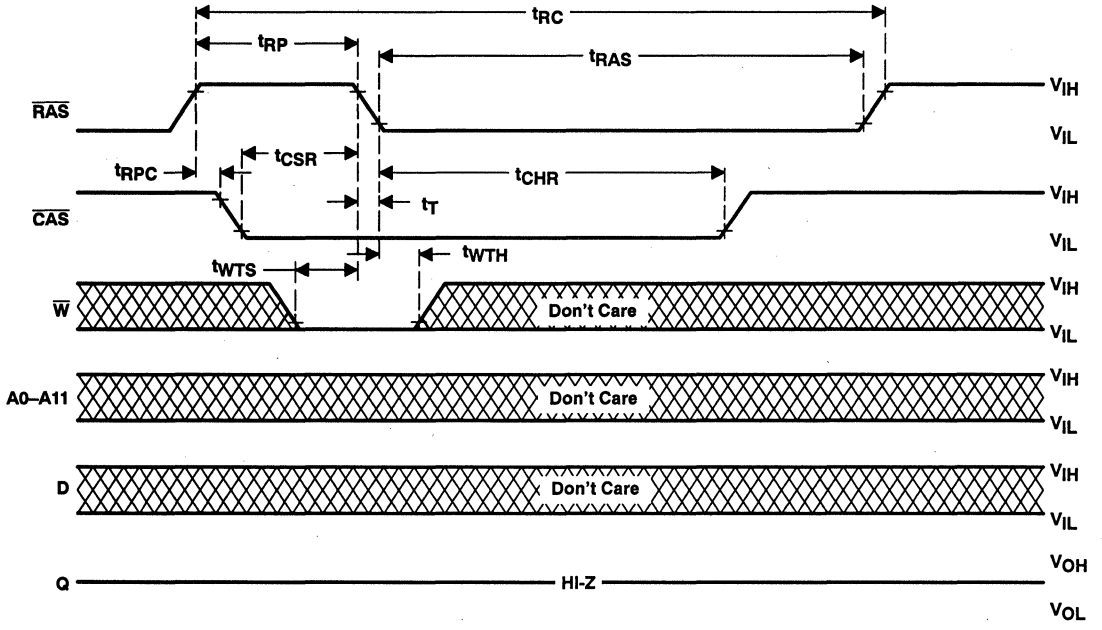


Figure 14. Test Mode Entry Cycle

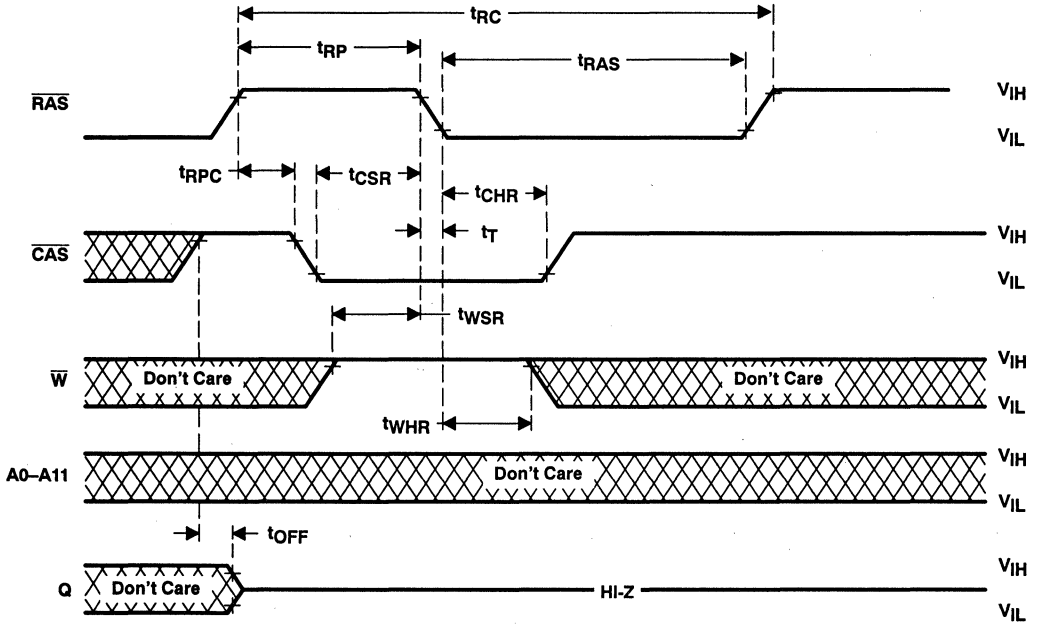
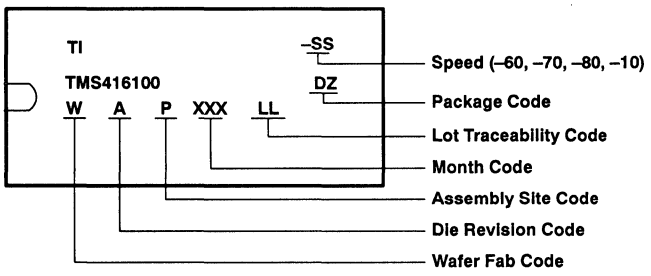


Figure 15. Test Mode Exit Cycle ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)

device symbolization



This data sheet is applicable to all TMS416400s symbolized with Revision "A" and subsequent revisions as described on page 25.

- **Organization . . . 4 194 304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
TMS416400-60	60 ns	15 ns	30 ns	110 ns
TMS416400-70	70 ns	18 ns	35 ns	130 ns
TMS416400-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycles Refresh in 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

description

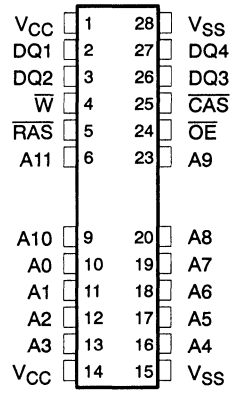
The TMS416400 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 4 194 304-bit words by four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

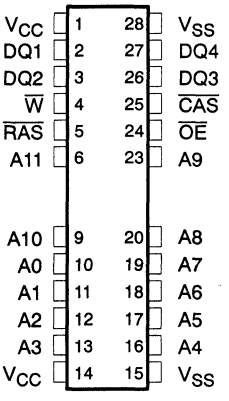
All inputs, outputs, and clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416400 is offered in 400-mil 24/28-pin surface mount SOJ (DZ suffix) and 400-mil 28/24-pin surface mount thin SOP (DGC and DGD suffixes) packages. This device is characterized for operation from 0°C to 70°C.

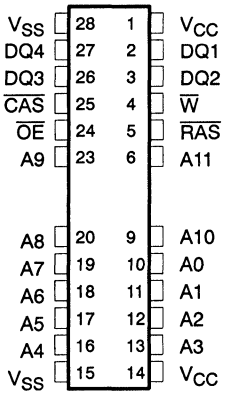
DZ PACKAGE† (TOP VIEW)



DGC PACKAGE† (TOP VIEW)



DGD PACKAGE† (TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS416400 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAS} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the Row Address Strobe $\overline{RAS}$. Ten column-address bits are set on A0 through A9. CA10 and CA11 are not used. Row address A11 is required during a normal access and during $\overline{RAS}$ only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain for the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixty-four milliseconds to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

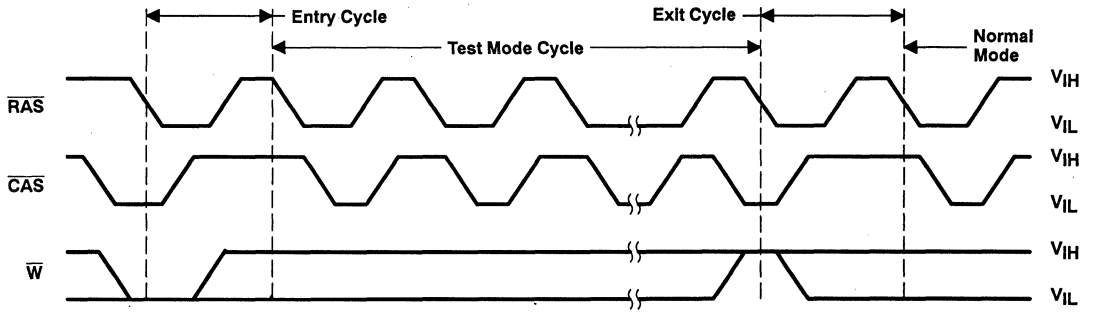
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

The part is configured as 1024K × 4 × 4 bit device in test mode, where each DQ pin has a separate 4-bit parallel read and write data bus where CA0 and CA1 are ignored. During a read cycle, the 4 internal bits are compared for each DQ pin separately. If the 4 bits agree, the DQ pin will go high, if not, the DQ pin will go low. All 4 bits are written to the state of their respective DQ pin during a parallel write. Thus, each DQ pin is independent of the other and any data pattern desired may be written on each DQ pin. Test time is thus reduced by a factor of 4 for this series.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

Figure 1. Test Mode Cycle†

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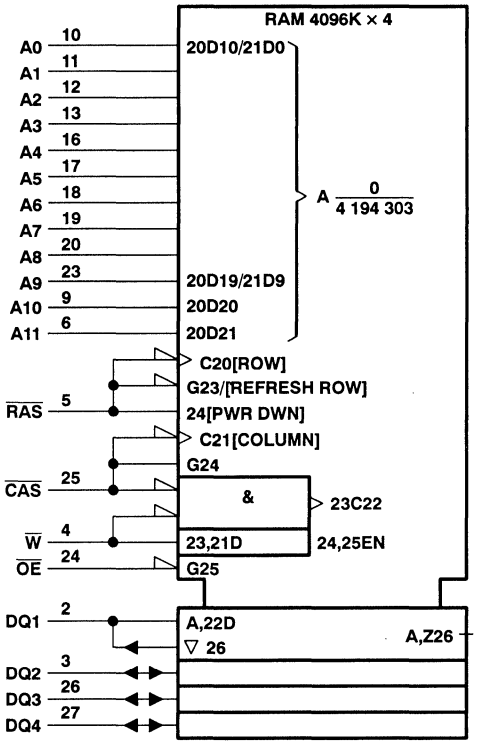
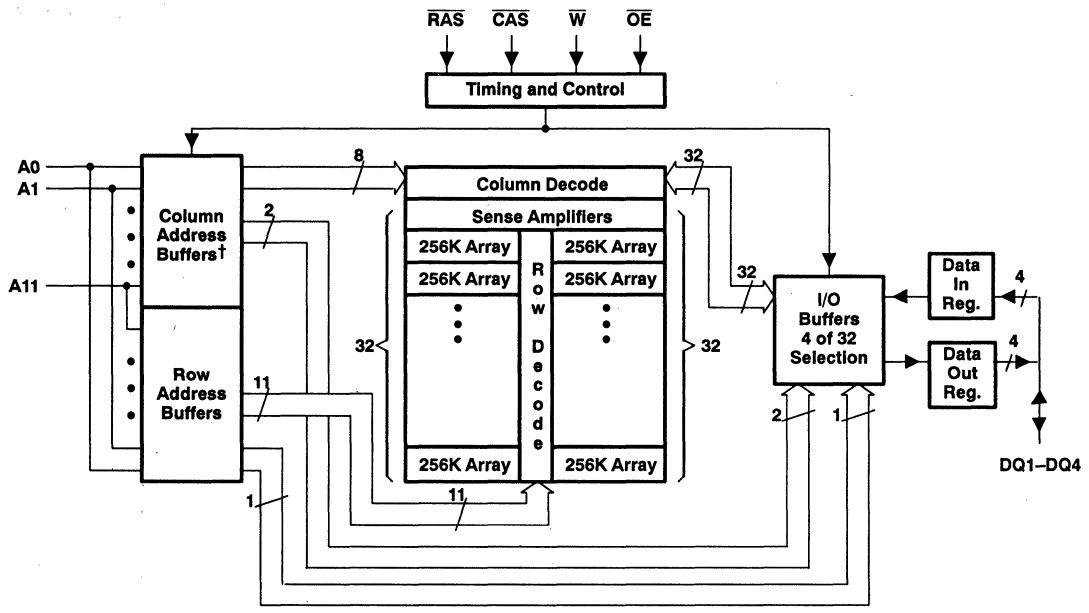
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the DZ package.

functional block diagram



† Column Address 10 and Column Address 11 are not used.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Then algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS416400-60		TMS416400-70		TMS416400-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Notes 3 and 5)	Minimum cycle, V_{CC} = 5.5 V		90		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.05 V (CMOS)		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 and 5)‡	$\overline{RAS}$ cycling $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70	mA
I_{CC4}	Average page current (see Notes 4 and 5)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50	mA
I_{CC7}	Standby current output enable‡ (see Note 5)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.
5. Measured with no load connected.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 6: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416400-60		TMS416400-70		TMS416400-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		ns
t_{OHO}	Output disable time start of $\overline{OE}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS416400-60		TMS416400-70		TMS416400-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 8)	110		130		150		ns
t_{RWC}	Read-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 12)	0		0		0		ns
t_{RCS}	Read setup before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test-mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns

Continued next page.

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS416400-60		TMS416400-70		TMS416400-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$(test mode)	65		75		85		ns
t_{REF}	Refresh time interval		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

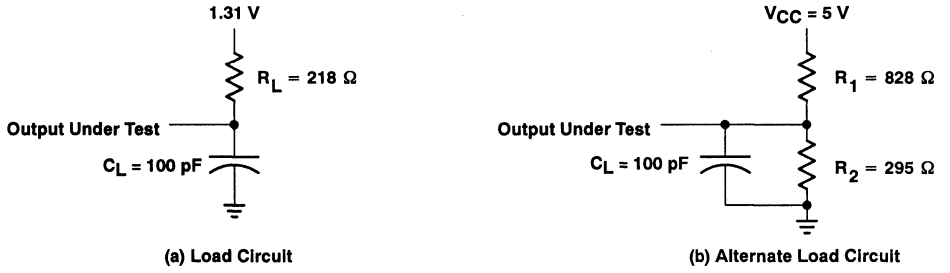
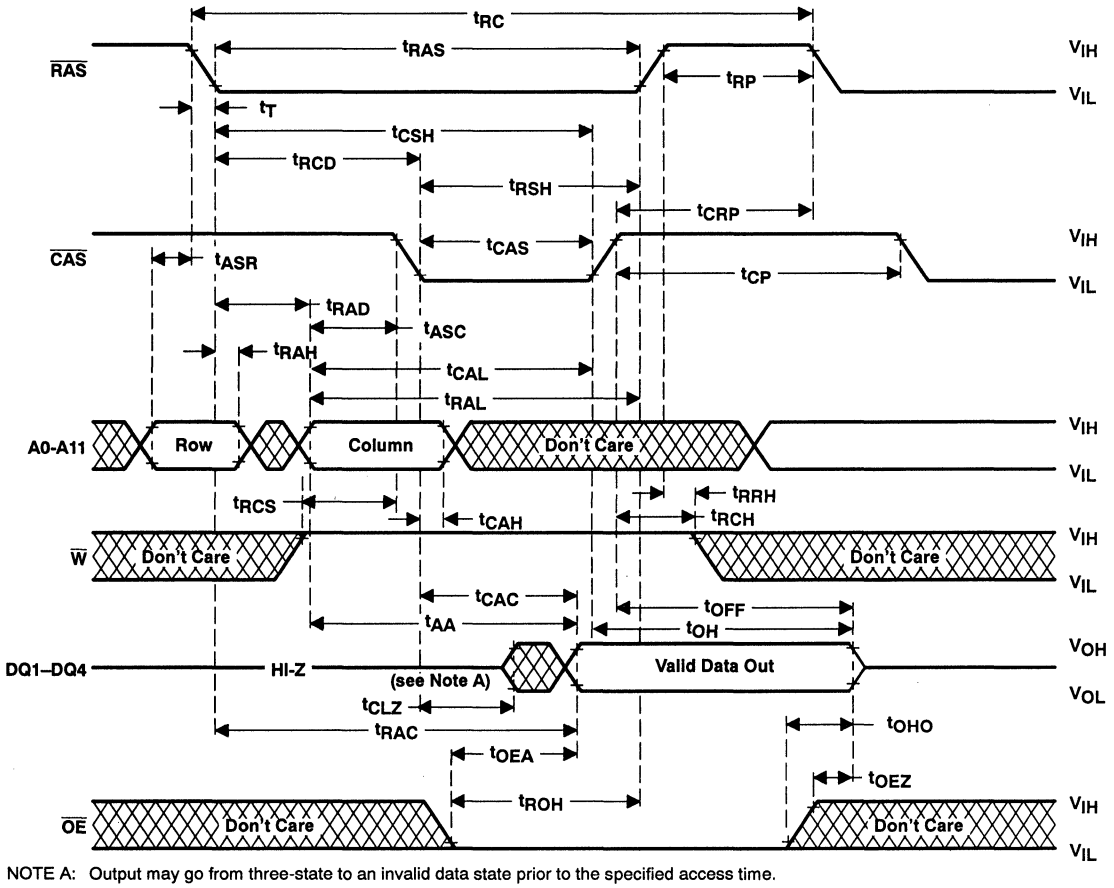


Figure 2. Load Circuits for Timing Parameters



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

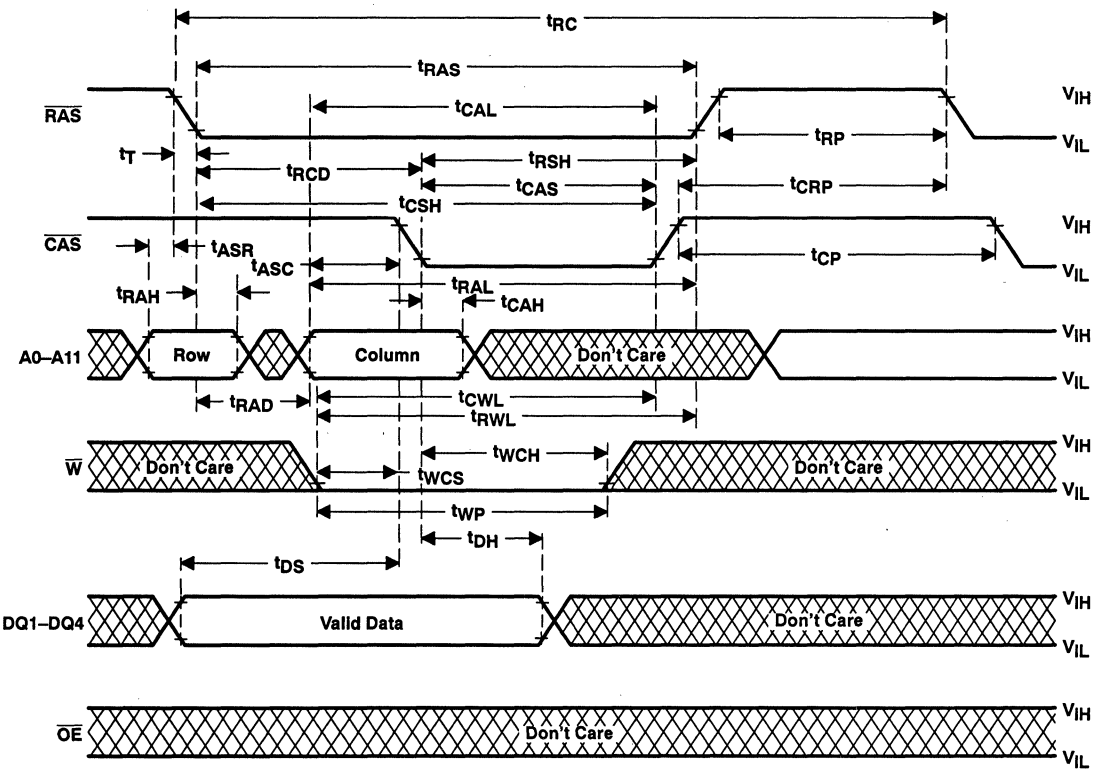


Figure 4. Early Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

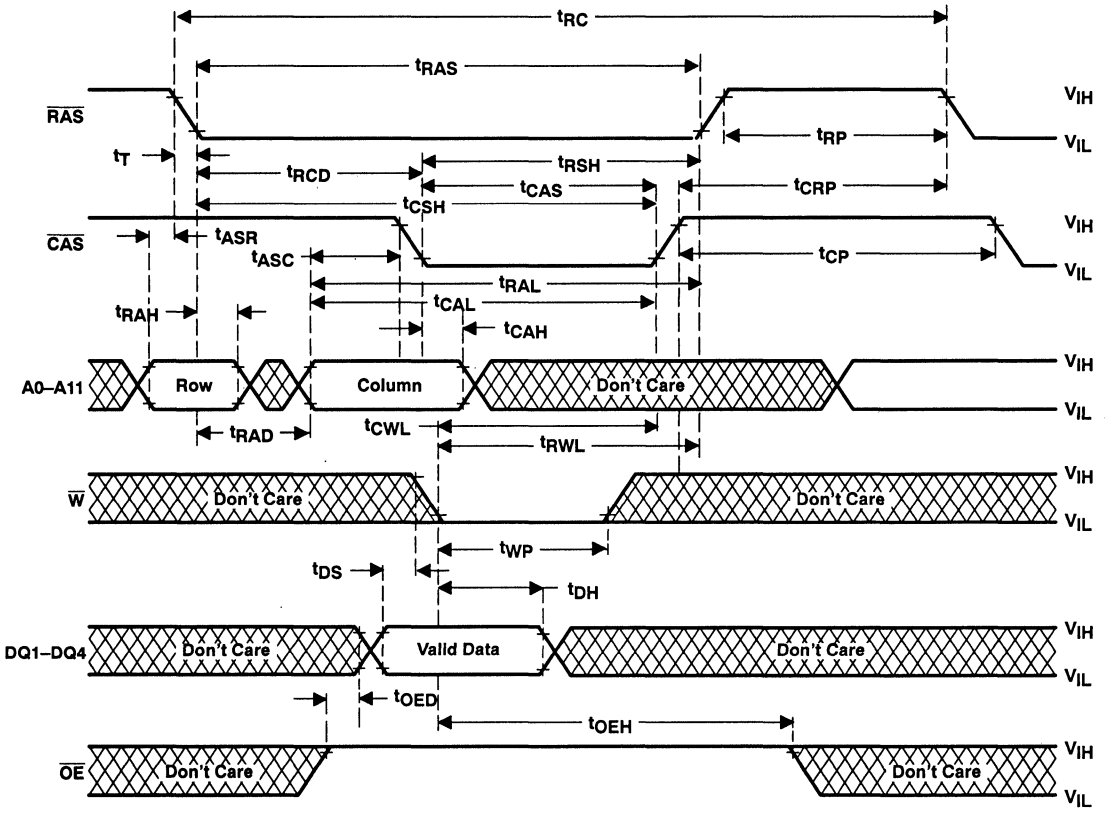
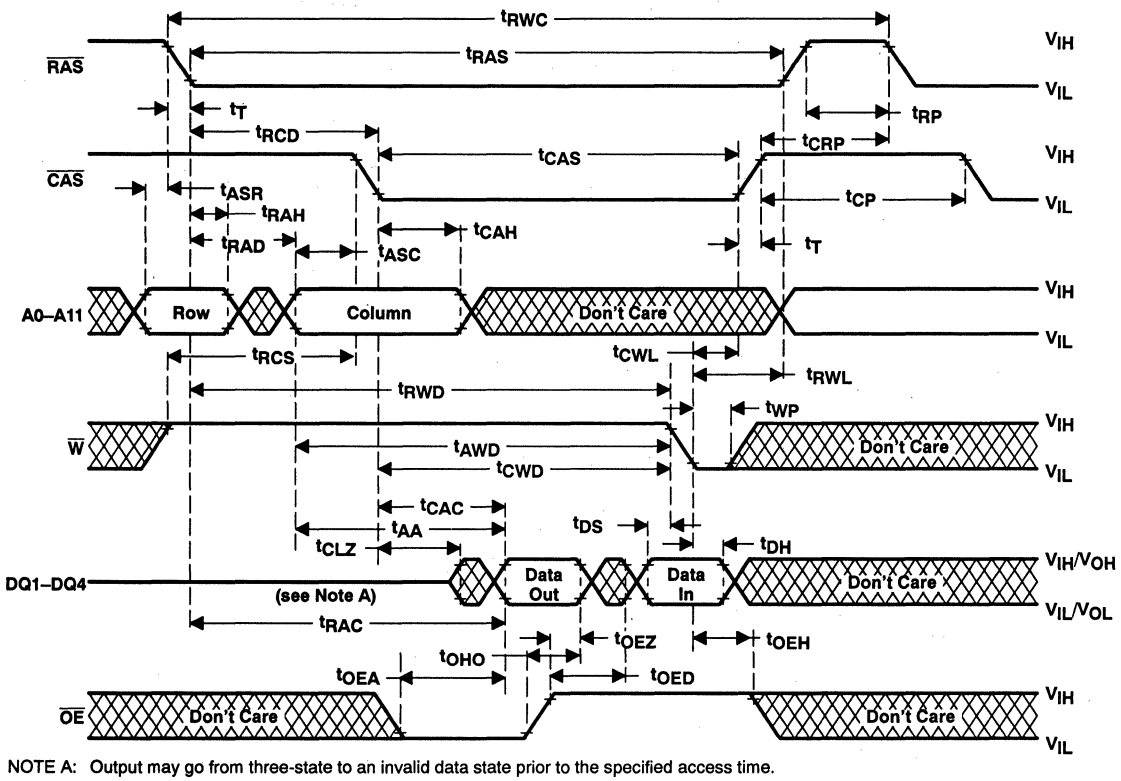


Figure 5. Write Cycle Timing

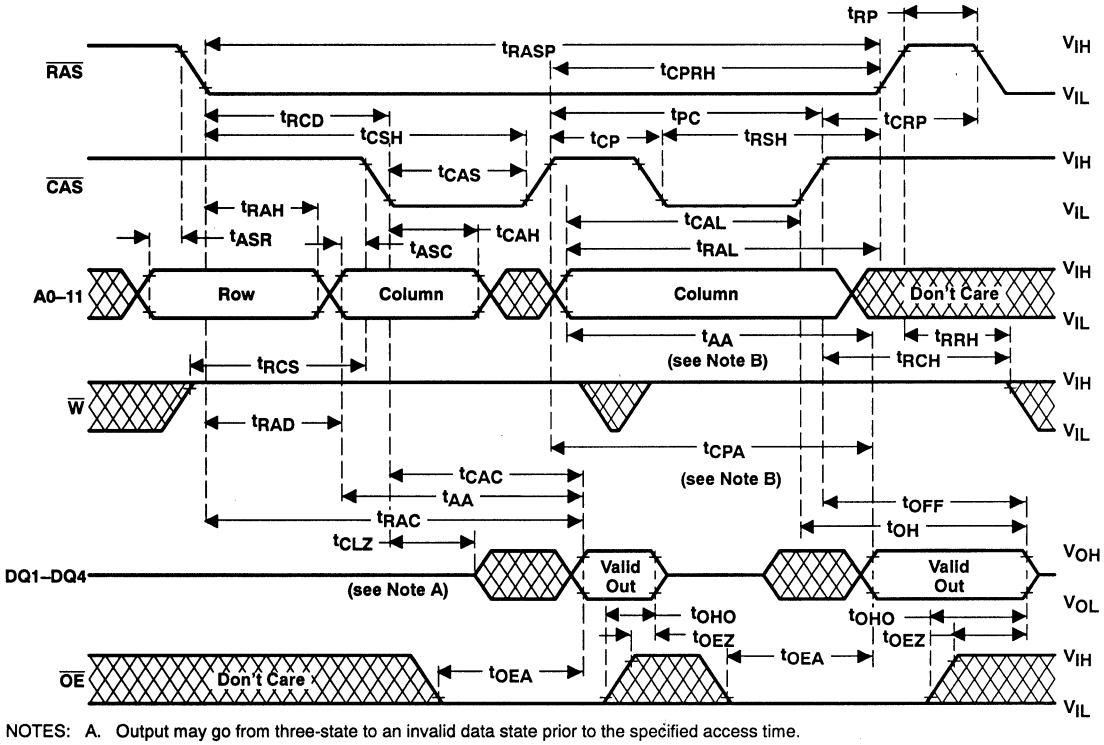
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

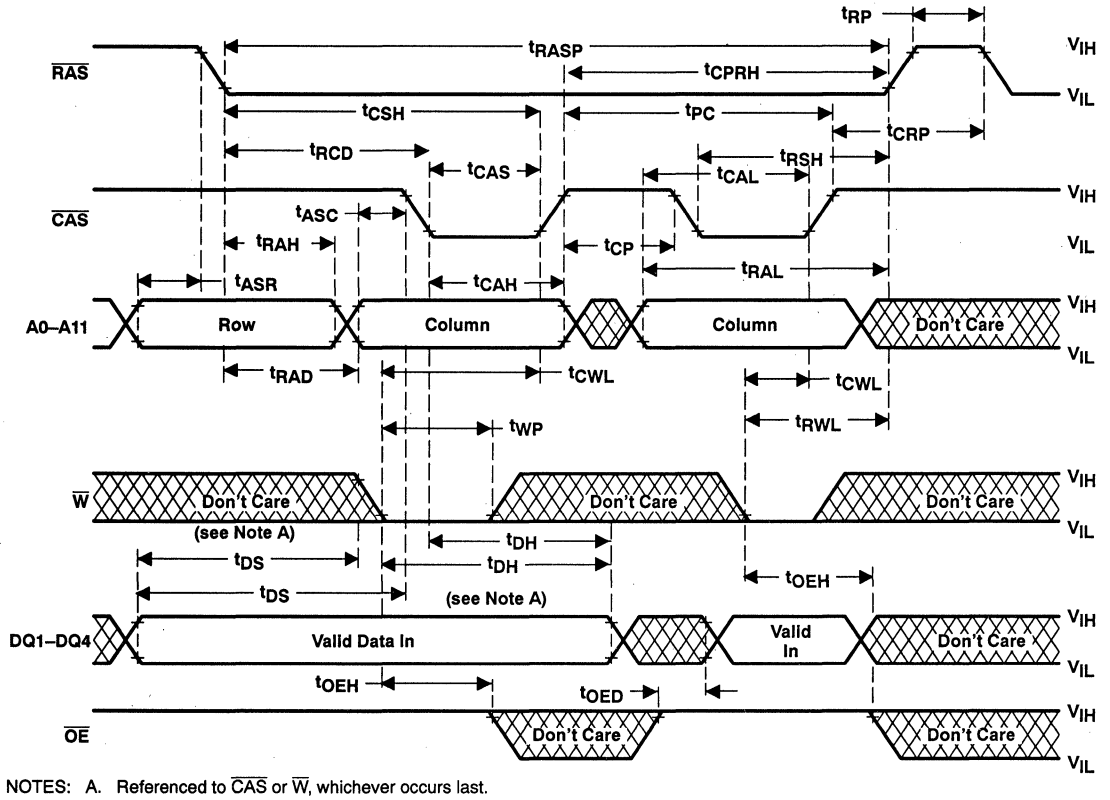
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

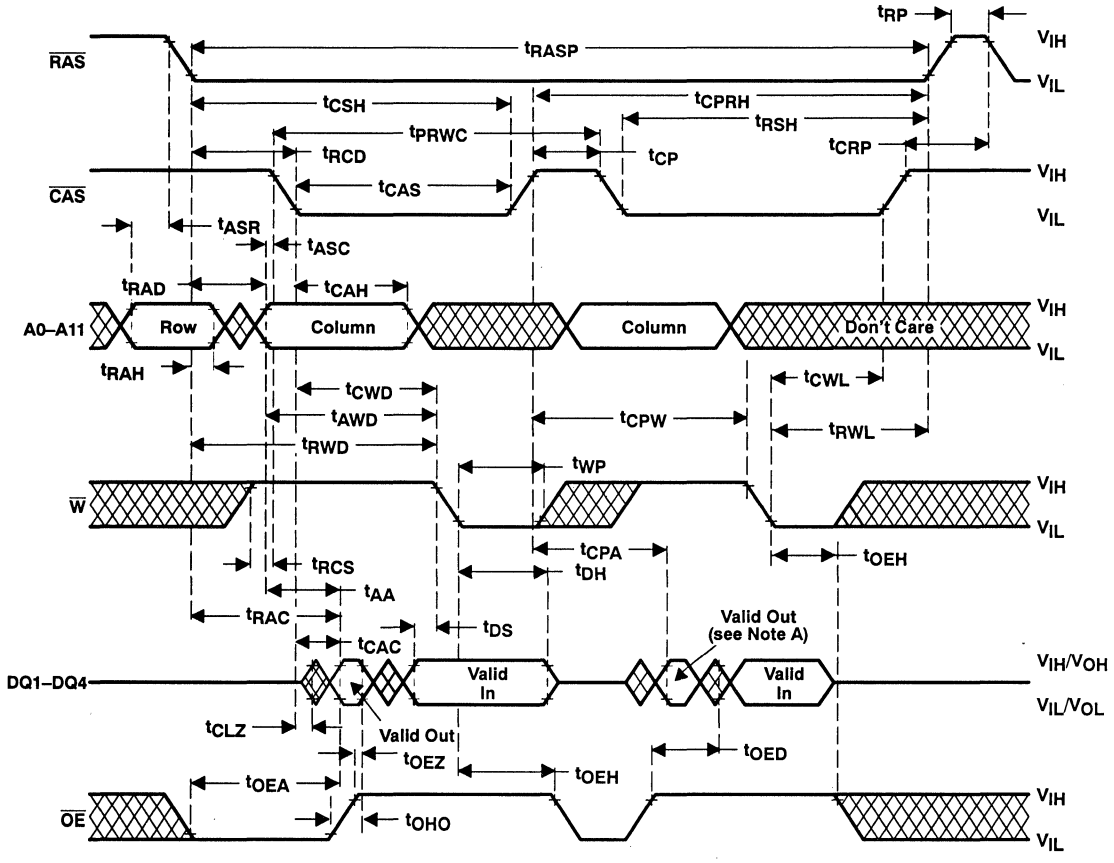
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

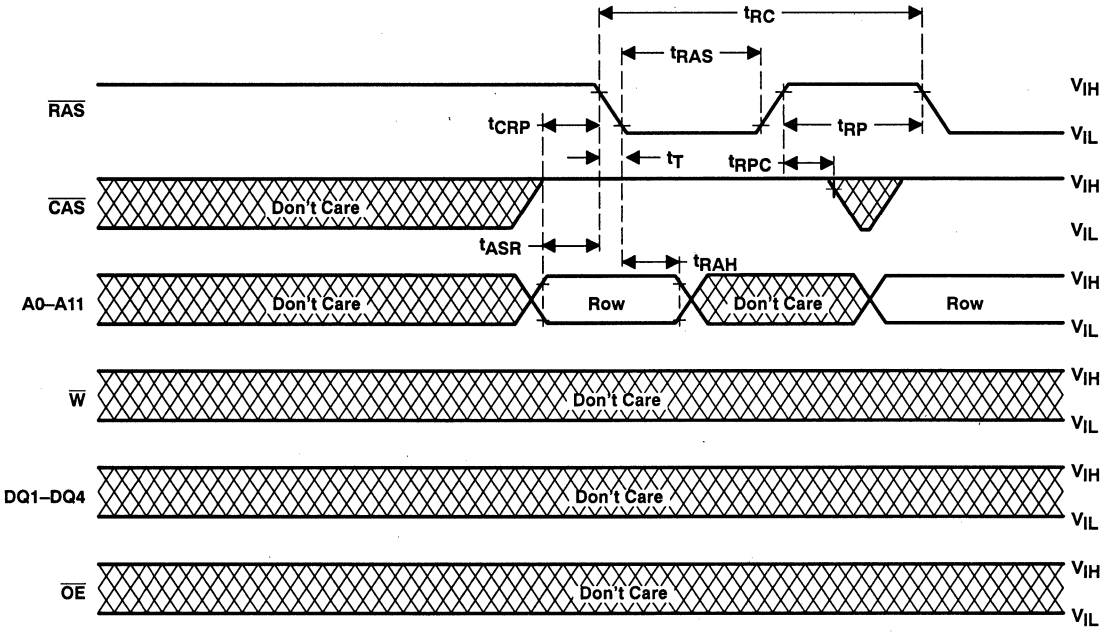


Figure 10. $\overline{\text{RAS}}$-Only Refresh Timing

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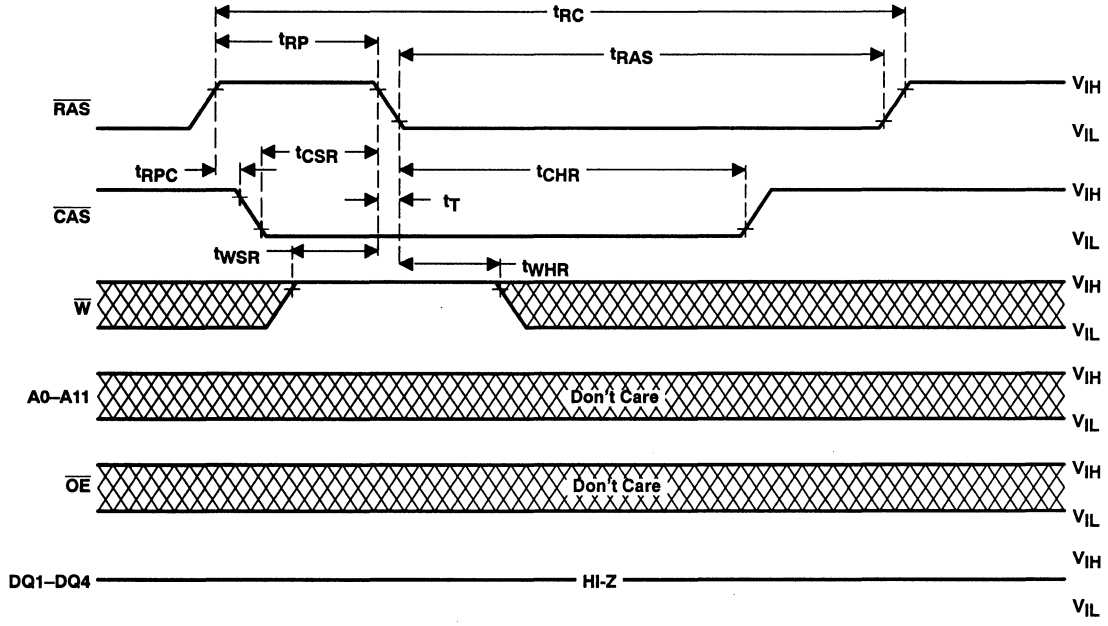

Figure 11. Automatic ($\overline{CAS}$-before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

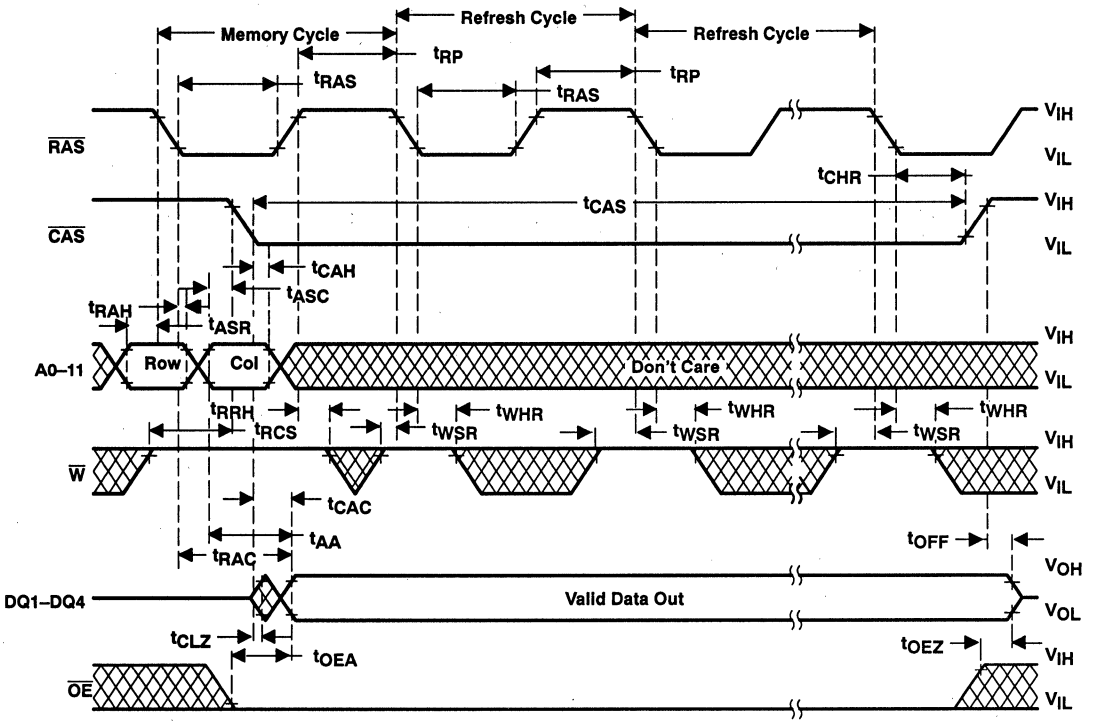

Figure 12. Hidden Refresh Cycle (Read)

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PARAMETER MEASUREMENT INFORMATION

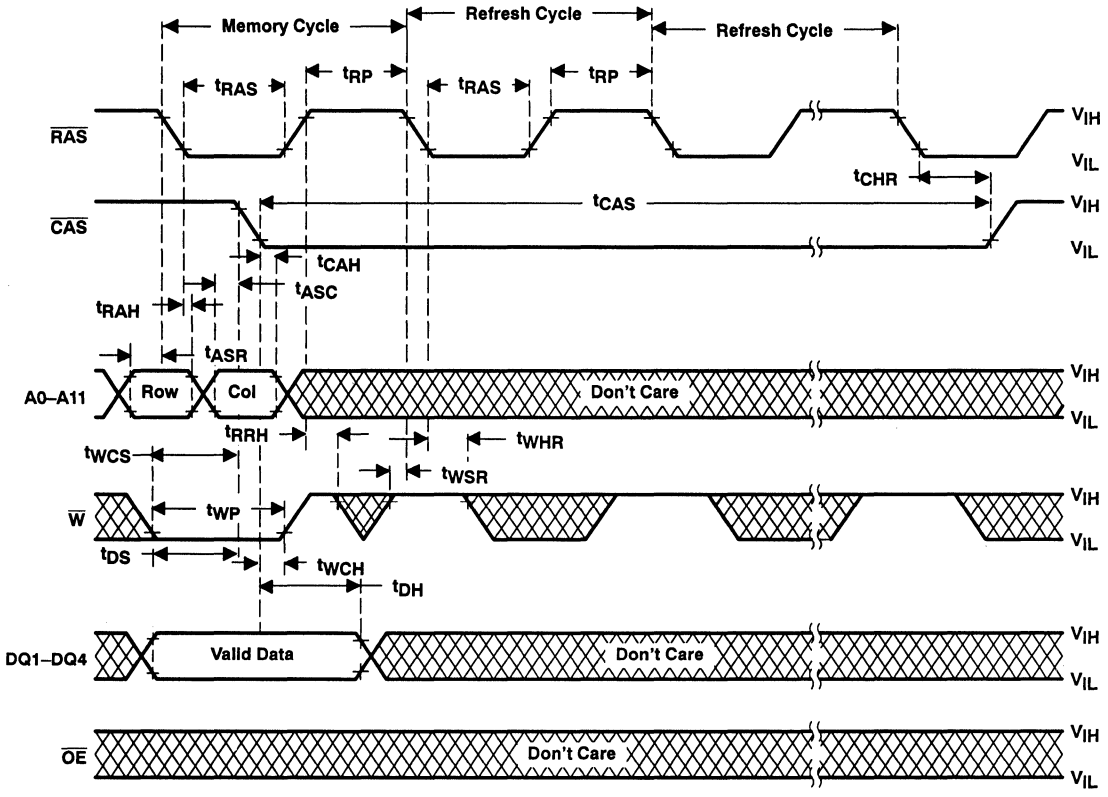

Figure 13. Hidden Refresh Cycle (Write)

PARAMETER MEASUREMENT INFORMATION

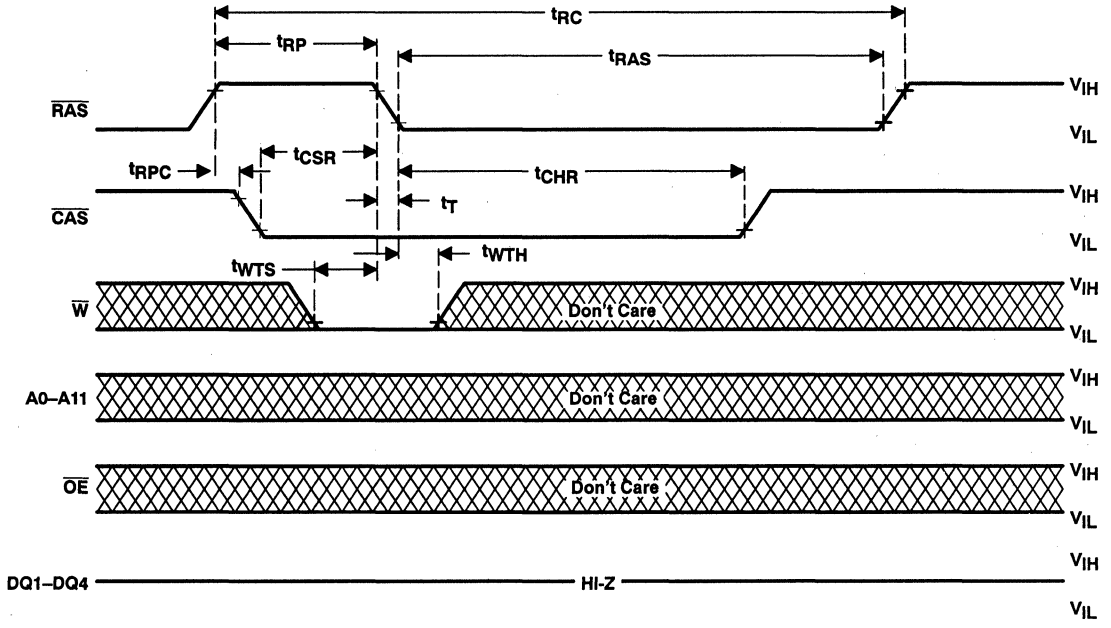

Figure 14. Test Mode Entry Cycle

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PARAMETER MEASUREMENT INFORMATION

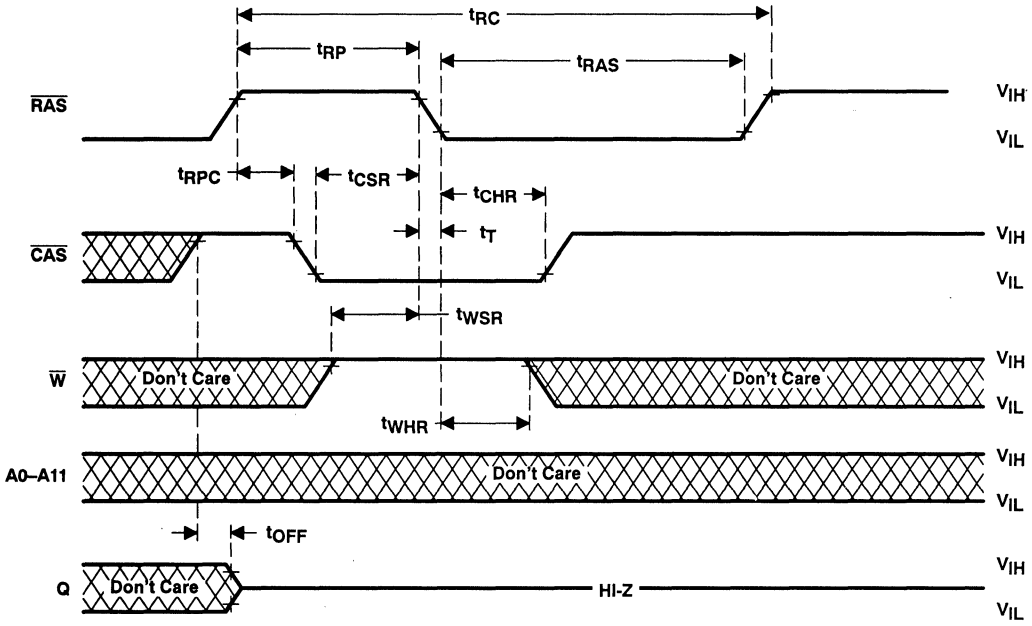
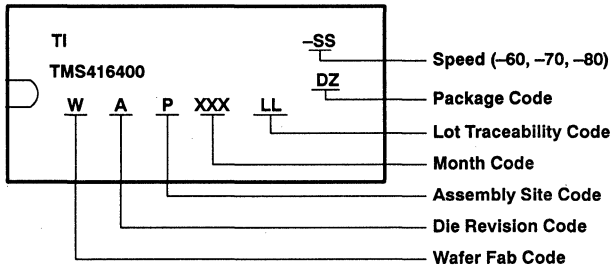


Figure 15. Test Mode Exit Cycle ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)

device symbolization



This data sheet is applicable to all TMS417400s symbolized with Revision "A" and subsequent revisions as described on page 23.

- **Organization . . . 4 194 304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
TMS416400-60	60 ns	15 ns	30 ns	110 ns
TMS416400-70	70 ns	18 ns	35 ns	130 ns
TMS416400-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 2048 Cycles Refresh in 32 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

description

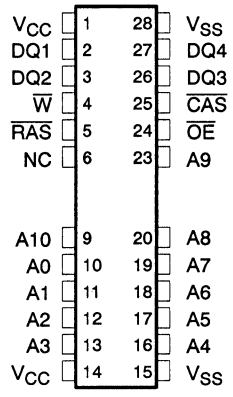
The TMS417400 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 4 194 304-bit words by four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

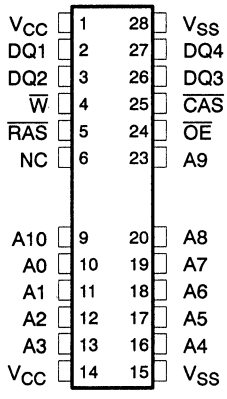
All inputs, outputs, and clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS417400 is offered in 400-mil 28/24-pin surface mount SOJ (DZ suffix) and 400-mil 28/24-pin surface mount thin SOP (DGC and DGD suffixes) packages. This device is characterized for operation from 0°C to 70°C.

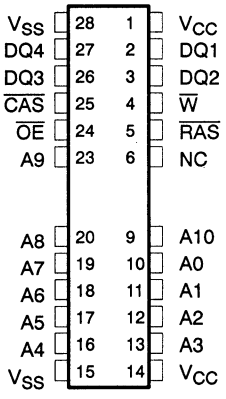
DZ PACKAGE†
(TOP VIEW)



DGC PACKAGE†
(TOP VIEW)



DGD PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS417400 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAS} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A10)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Twelve row-address bits are set on inputs A0 through A10 and latched onto the chip by the Row Address Strobe $\overline{RAS}$. Eleven column-address bits are set on A0 through A10. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain for the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every thirty-two milliseconds to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

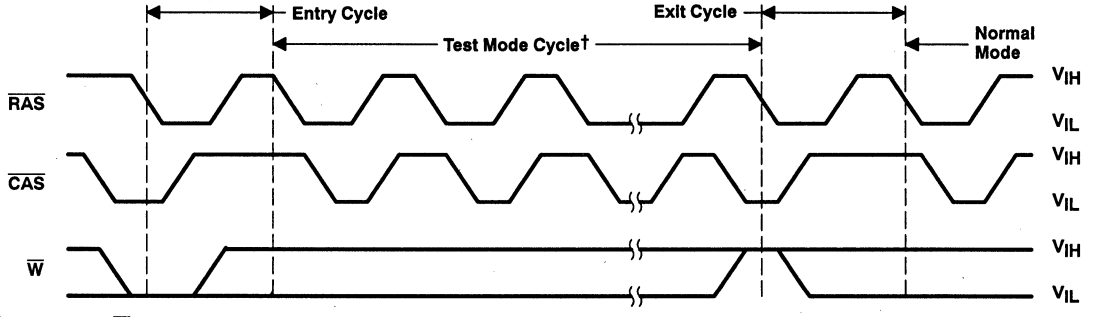
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

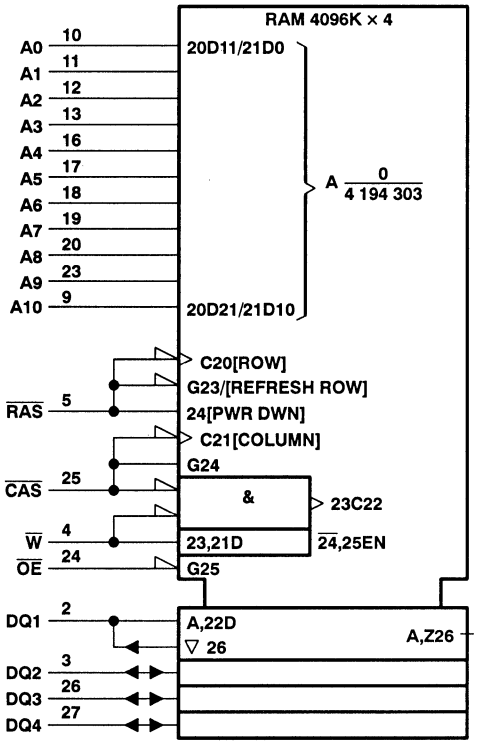
The part is configured as 1024K × 4 × 4 bit device in test mode, where each DQ pin has a separate 4-bit parallel read and write data bus where CA0 and CA1 are ignored. During a read cycle, the 4 internal bits are compared for each DQ pin separately. If the 4 bits agree, the DQ pin will go high, if not, the DQ pin will go low. All 4 bits are written to the state of their respective DQ pin during a parallel write. Thus, each DQ pin is independent of the other and any data pattern desired may be written on each DQ pin. Test time is thus reduced by a factor of 4 for this series.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

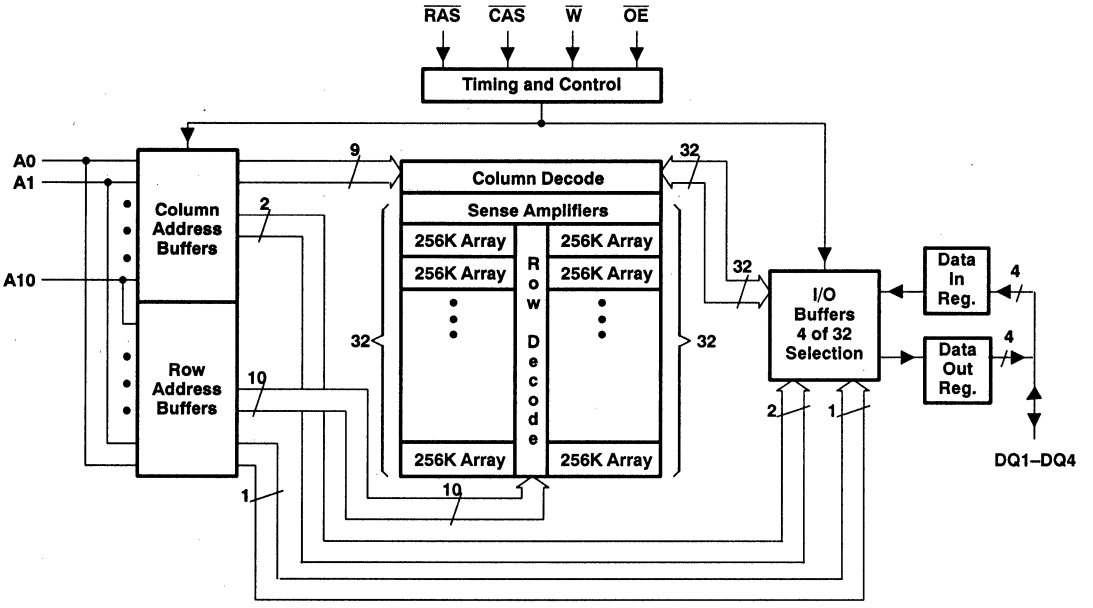
Figure 1. Test Mode Cycle

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



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absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Then algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS417400-60		TMS417400-70		TMS417400-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Notes 3 and 5)	Minimum cycle, V_{CC} = 5.5 V		120		110		100	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = $\overline{VCC}$ – 0.2 V (CMOS)		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 and 5)‡	$\overline{RAS}$ cycling $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		120		110		100	mA
I_{CC4}	Average page current (see Notes 4 and 5)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50	mA
I_{CC7}	Standby current output enable (see Note 5)‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.
5. I_{CC} MAX is specified with no load connected.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 6: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS417400-60		TMS417400-70		TMS417400-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		ns
t_{OHO}	Output disable time start of $\overline{OE}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS417400-60		TMS417400-70		TMS417400-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 8)	110		130		150		ns
t_{RWC}	Read-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 12)	0		0		0		ns
t_{RCS}	Read setup before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test-mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		ns

Continued next page.

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS417400-60		TMS417400-70		TMS417400-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$(test mode)	65		75		85		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

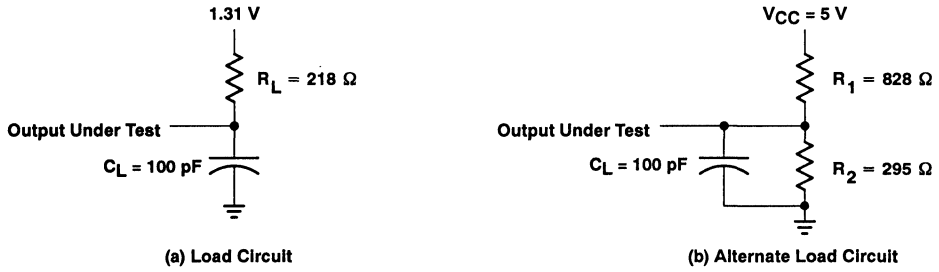
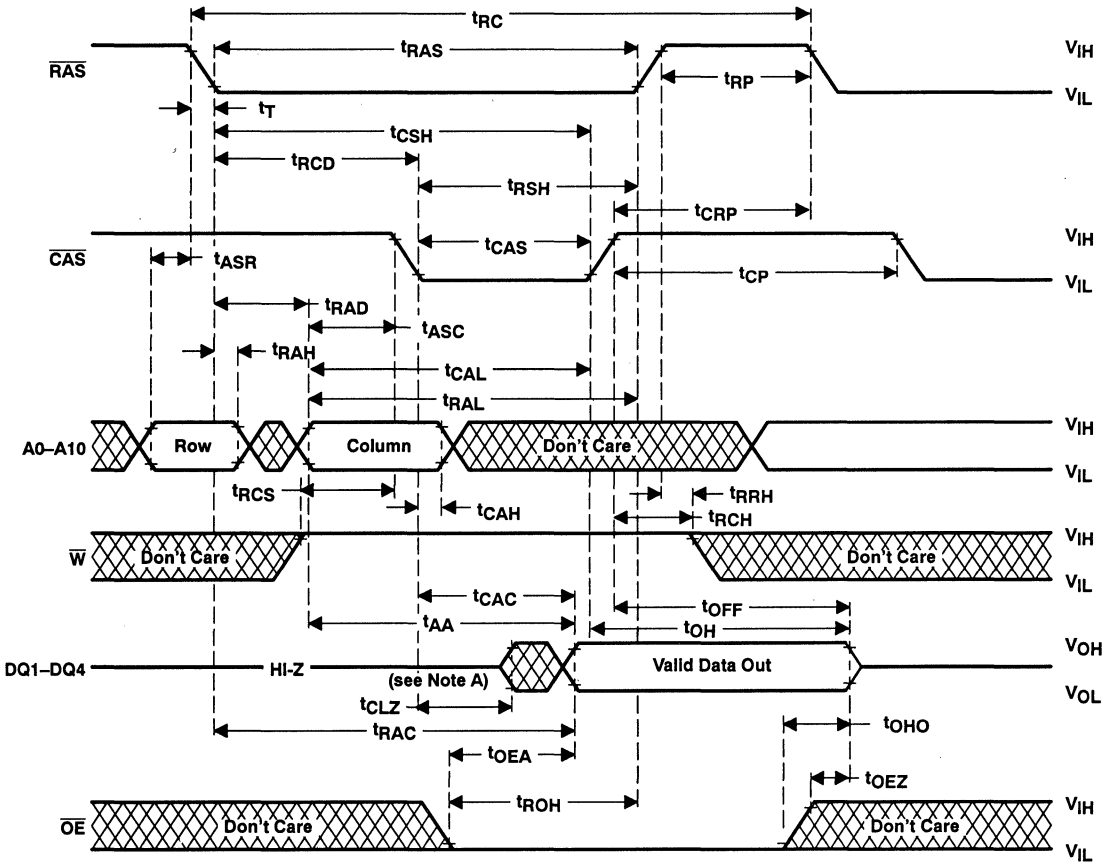


Figure 2. Load Circuits for Timing Parameters



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

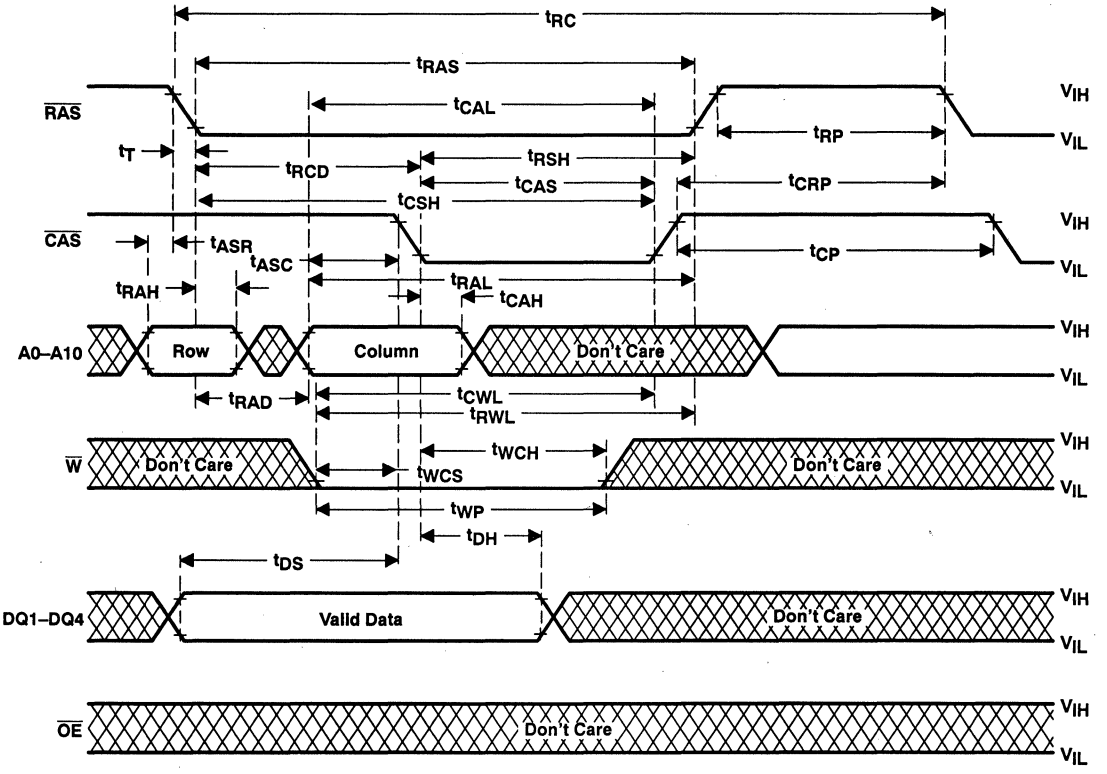


Figure 4. Early Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

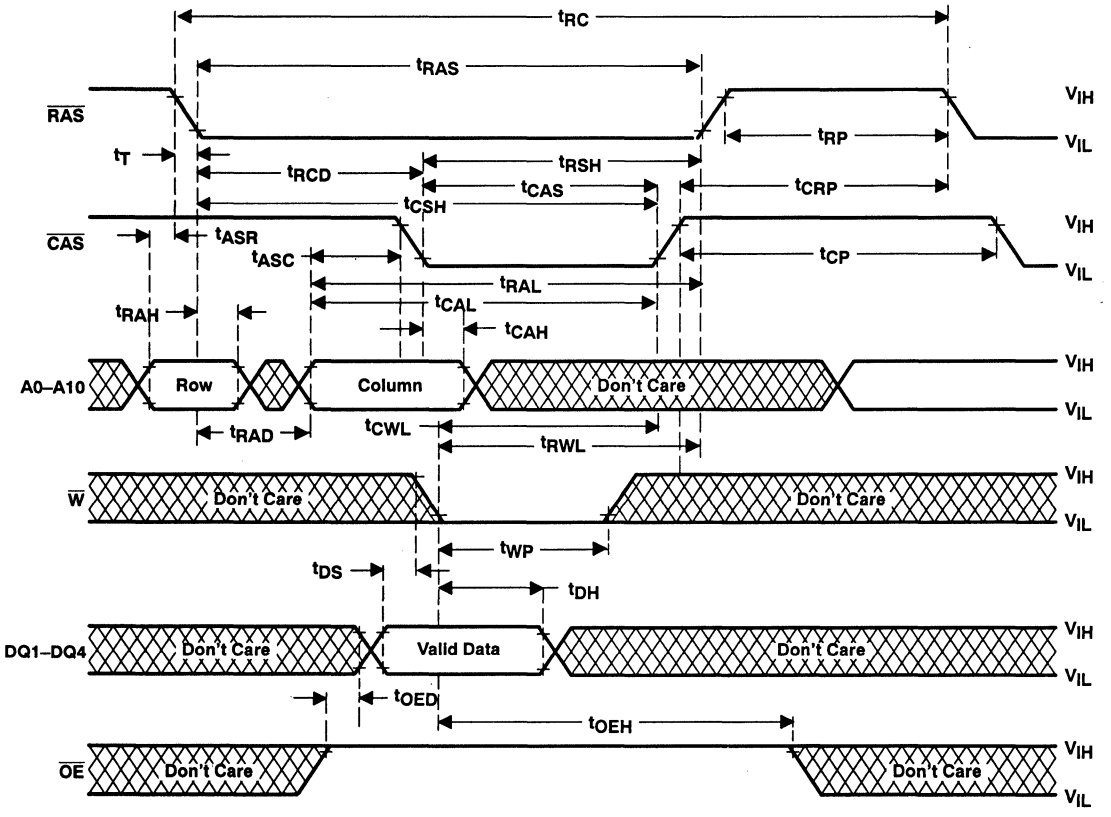
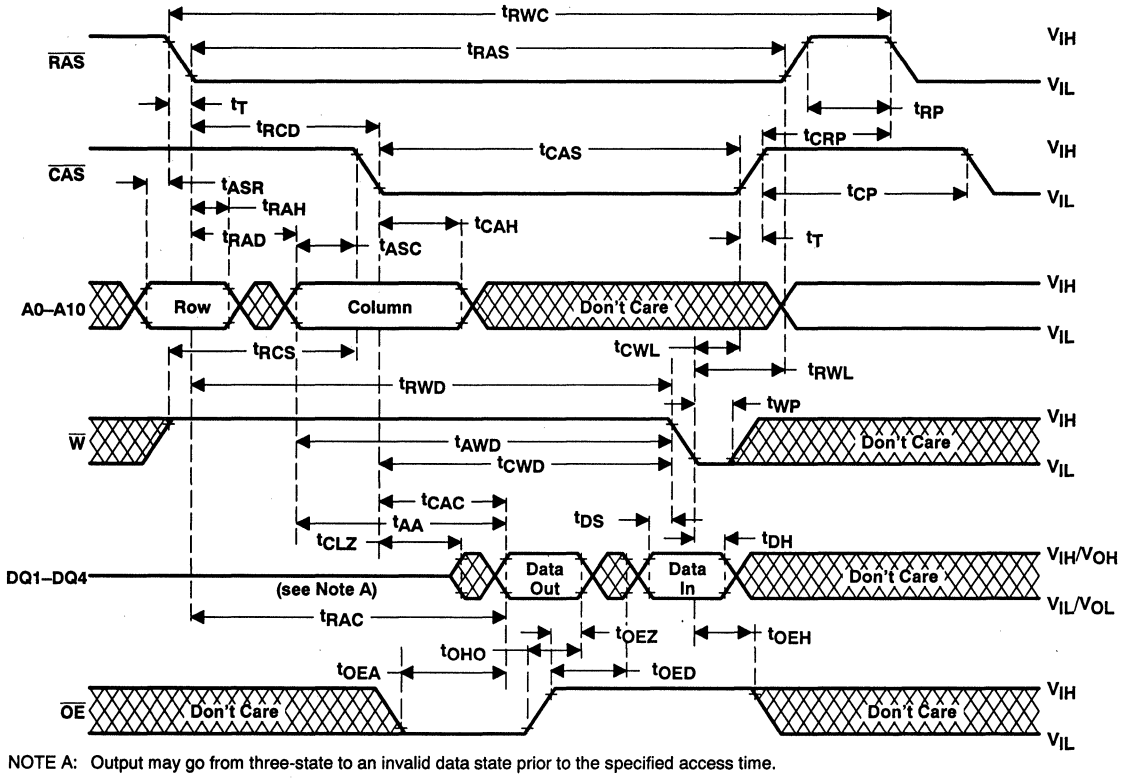


Figure 5. Write Cycle Timing

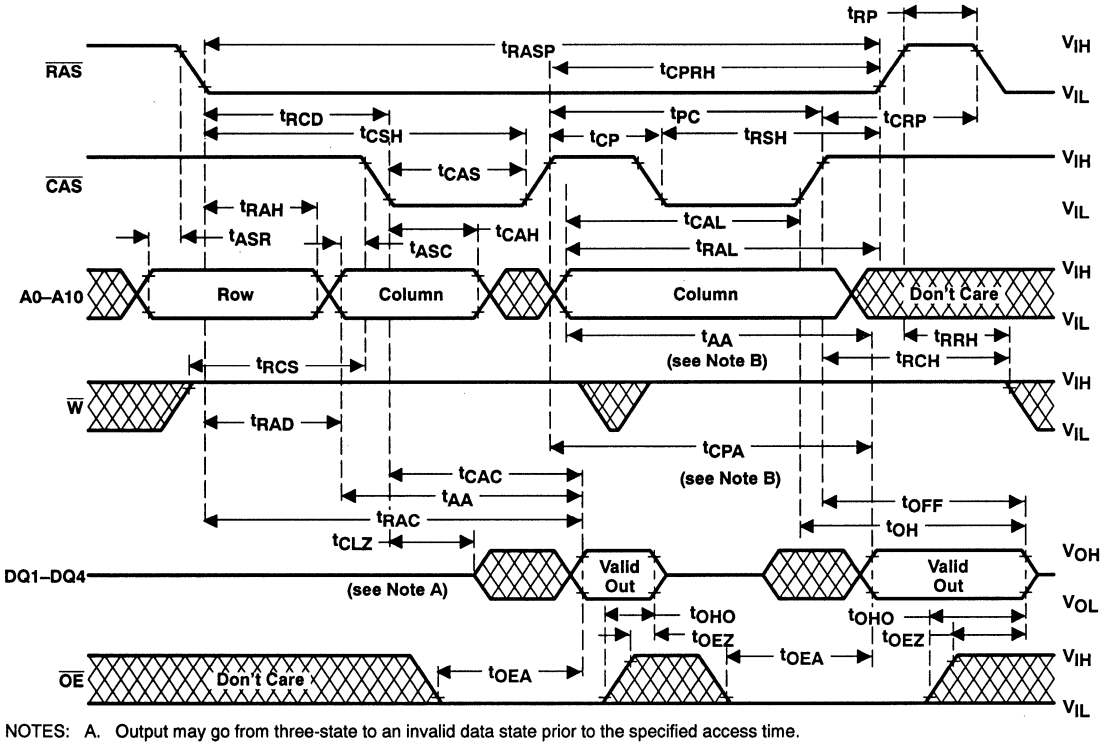
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

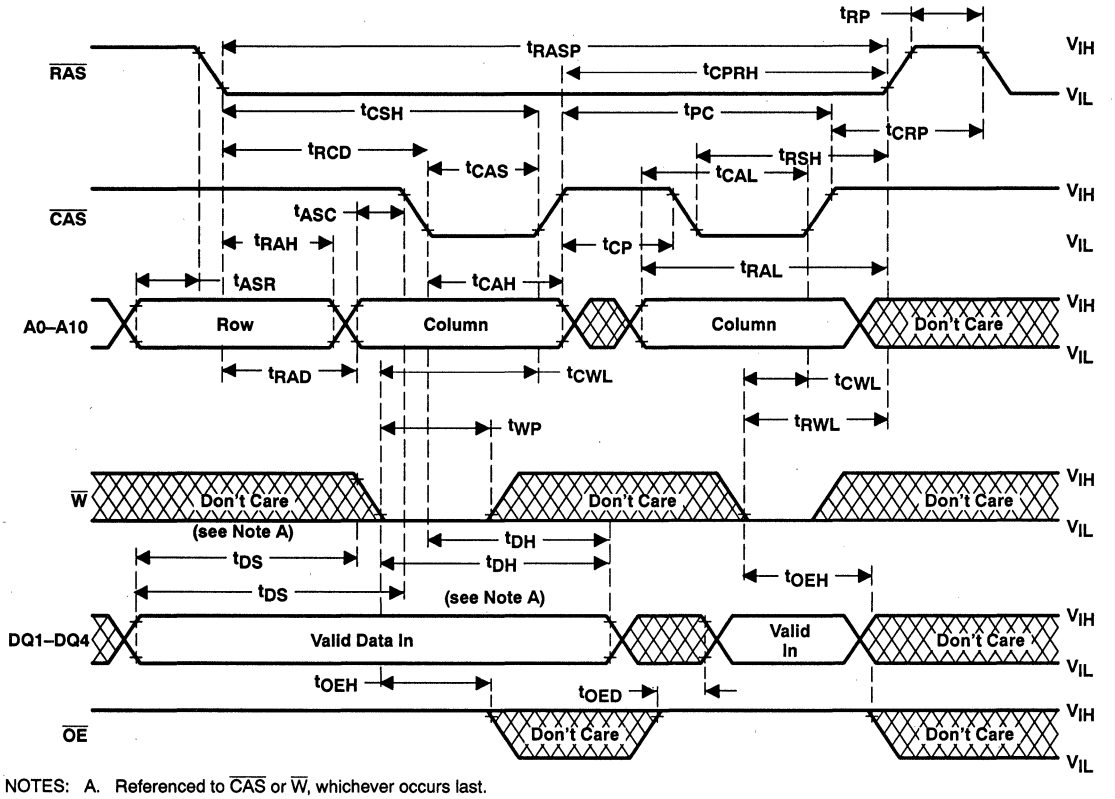
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

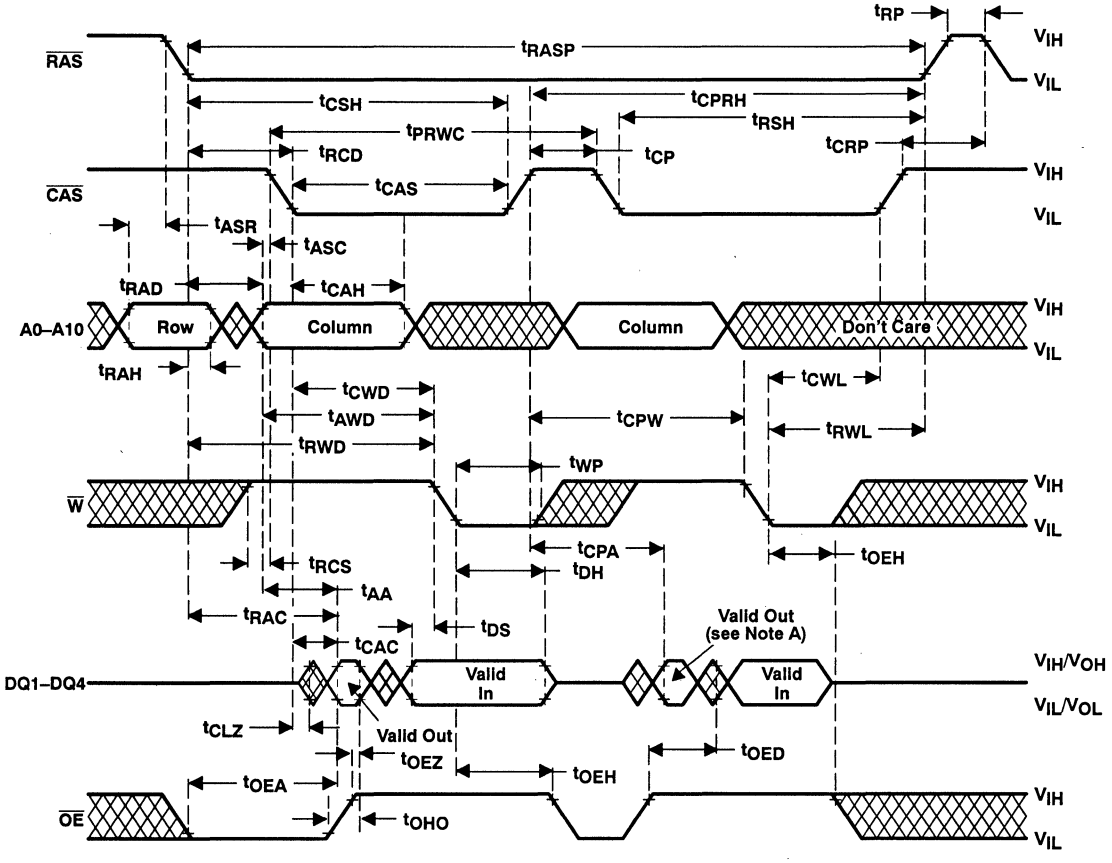
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

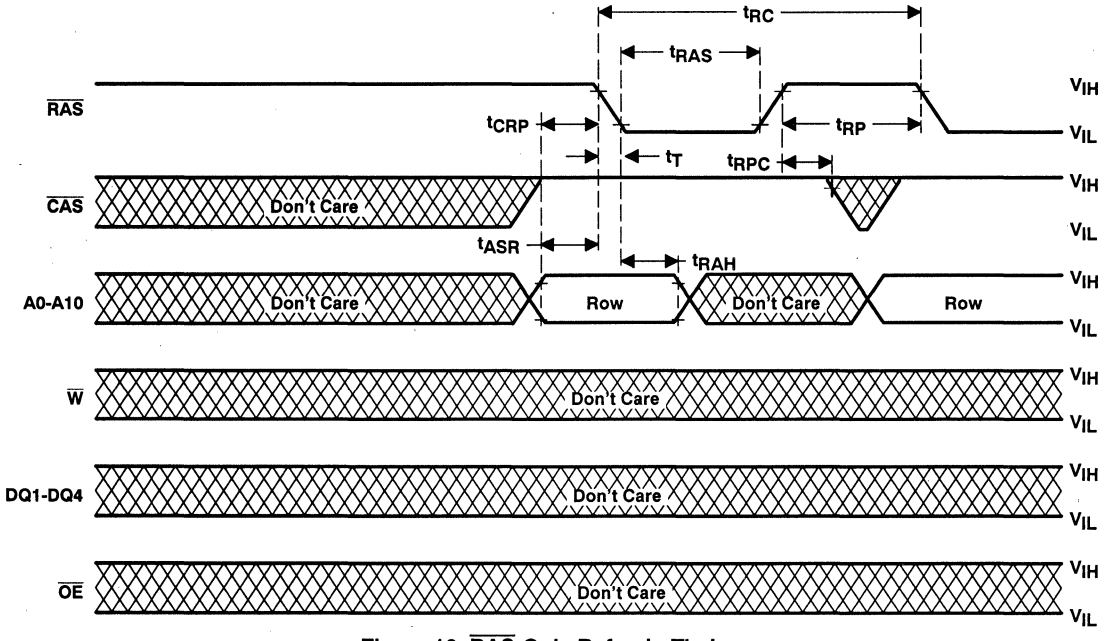


Figure 10. $\overline{RAS}$-Only Refresh Timing

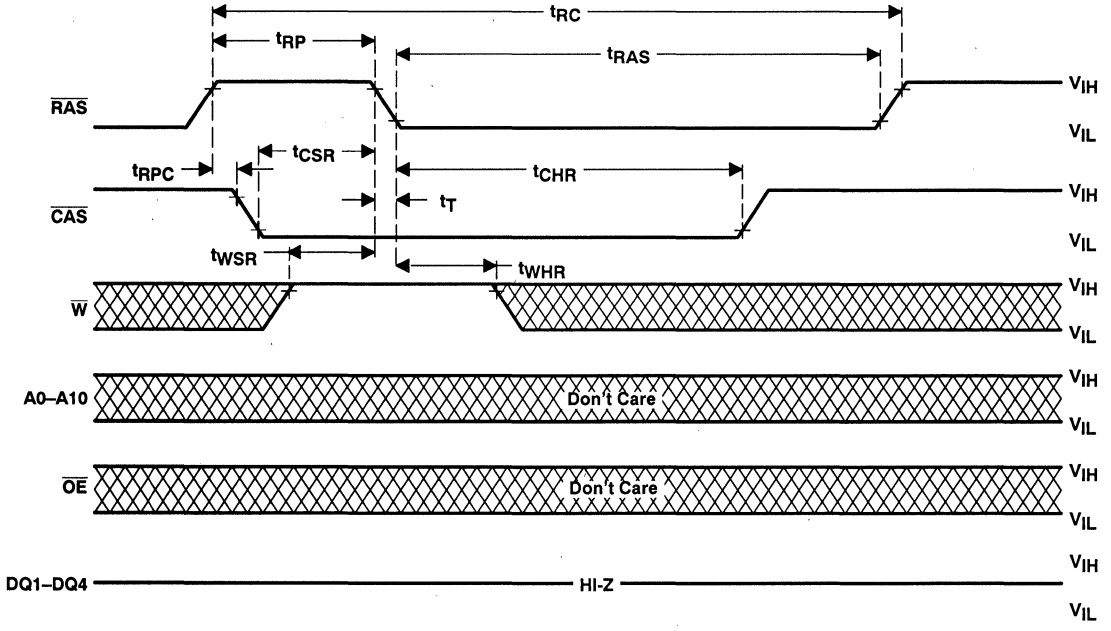


Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

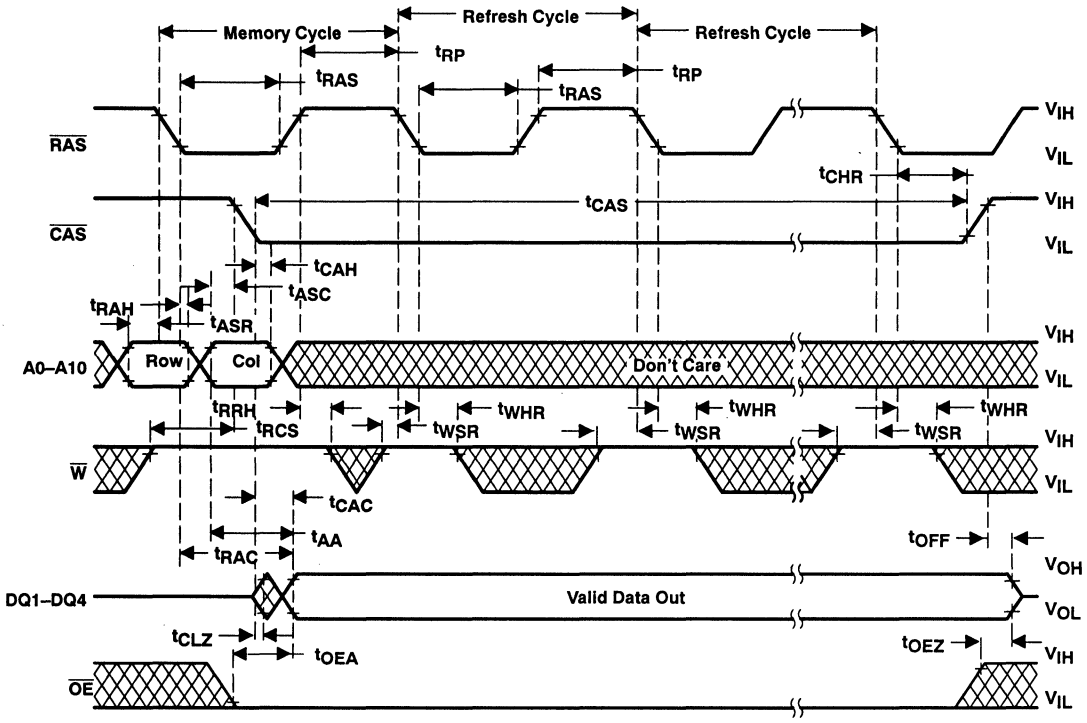

Figure 12. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION

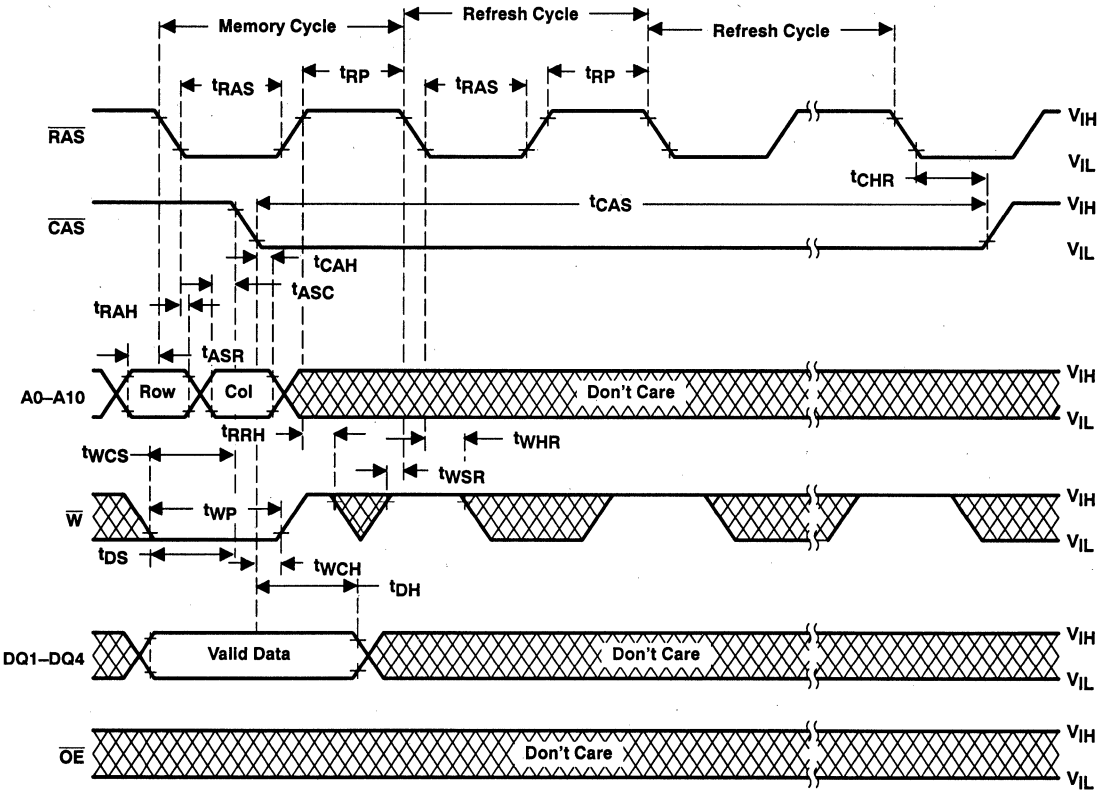

Figure 13. Hidden Refresh Cycle (Write)

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PARAMETER MEASUREMENT INFORMATION

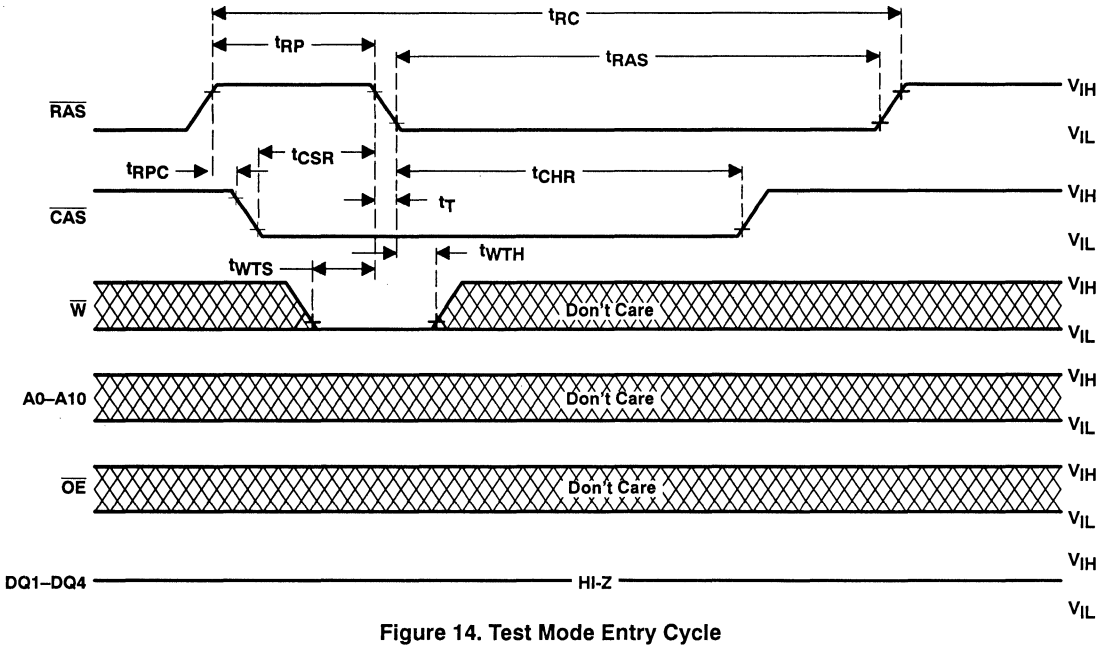


Figure 14. Test Mode Entry Cycle

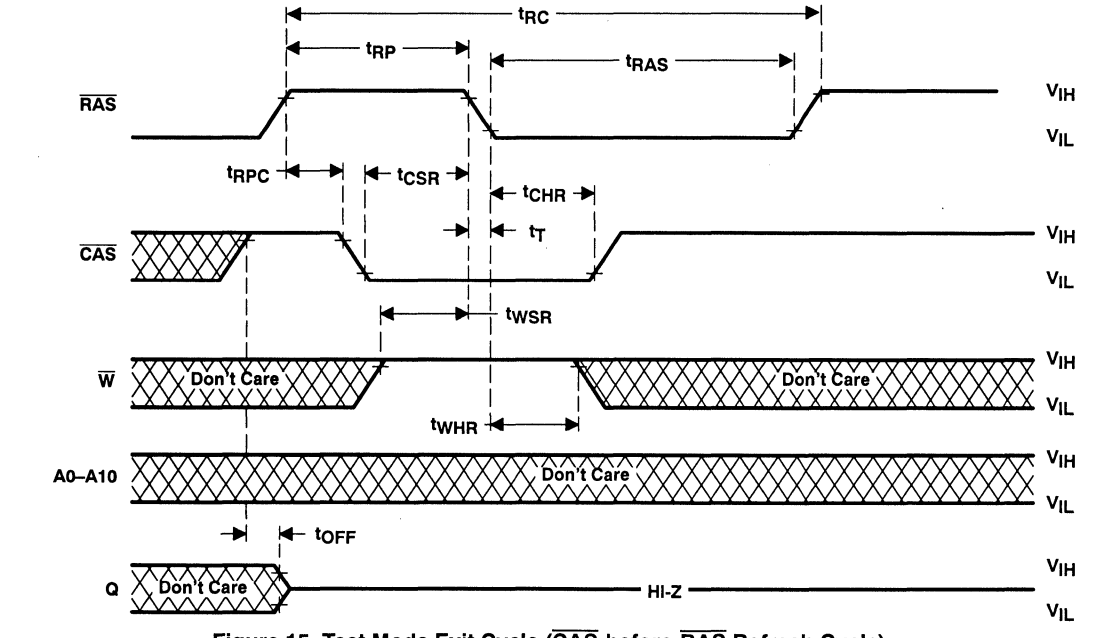
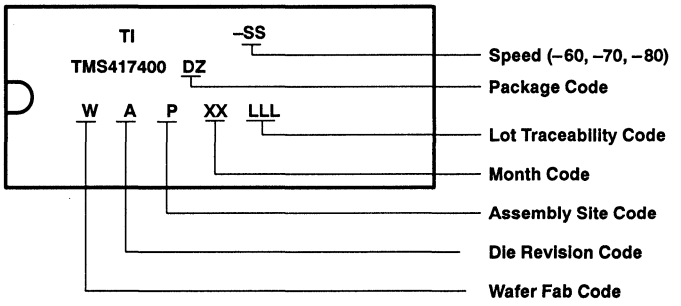


Figure 15. Test Mode Exit Cycle ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle)

device symbolization



This Product Preview is Applicable to All TMS416100/P, TMS416400/P, and TMS417400/P Devices Symbolized With Revision "B" and Subsequent Revisions as Described on Page 4.

- **Organization:**
  16 777 216 × 1 TMS416100, TMS416100P
  4 194 304 × 4 TMS416400 , TMS416400P
  4 194 304 × 4 TMS417400, TMS417400P
- **High Reliability Plastic 300-Mil 24/26-Lead Surface Mount (SOJ) Package, 24/26-Lead Thin Small Outline Package, and Reverse Thin Small Outline Package**
- **Low Power Dissipation**
  - **500 μA CMOS Standby Current (TMS416100P, TMS416400P, TMS417400P)**
  - **500 μA Self-Refresh Current (TMS416100P, TMS416400P, TMS417400P)**
  - **500 μA Extended Refresh Battery Backup Current (TMS416100P, TMS416400P, TMS417400P)**
- **3-State Unlatched Output**
- **All Inputs, Outputs, and Clocks Are TTL Compatible**
- **Enhanced Page Mode Operation for Faster Memory Access**
- **Long Refresh Period**
  - **4096-Cycle Refresh in 64 ms (TMS416100, TMS416400)**
  - **2048-Cycle Refresh in 32 ms (TMS417400)**
  - **256 ms for Extended Refresh Version (TMS416100P, TMS416400P, TMS417400P)**
- **Single 5 V Power Supply (10% Tolerance)**
- **$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh**
- **Operating Free-Air Temperature Range 0°C to 70°C**

- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)	I_{CC1} OPERATING CURRENT (MIN)	I_{CC3} REFRESH CURRENT (MIN)
TMS416100/P-60	60 ns	15 ns	30 ns	110 ns	80 mA	80 mA
TMS416100/P-70	70 ns	18 ns	35 ns	130 ns	70 mA	70 mA
TMS416100/P-80	80 ns	20 ns	40 ns	150 ns	60 mA	60 mA
TMS416400/P-60	60 ns	15 ns	30 ns	110 ns	80 mA	80 mA
TMS416400/P-70	70 ns	18 ns	35 ns	130 ns	70 mA	70 mA
TMS416400/P-80	80 ns	20 ns	40 ns	150 ns	60 mA	60 mA
TMS417400/P-60	60 ns	15 ns	30 ns	110 ns	110 mA	110 mA
TMS417400/P-70	70 ns	18 ns	35 ns	130 ns	100 mA	100 mA
TMS417400/P-80	80 ns	20 ns	40 ns	150 ns	90 mA	90 mA

description

The TMS416100, TMS416400, TMS417400 series are high-speed, 16 777 216-bit dynamic random-access memories, organized as either 16 777 216 words of one bit each (TMS416100) or 4 194 304 words of four bits each (TMS416400, TMS417400).

The TMS416100P, TMS416400P, and TMS417400P series are high-speed, self-refresh and extended-refresh, 16 777 216-bit DRAMS, organized as either 16 777 216 words of one bit each (TMS416100P) or 4 194 304 words of four bits each (TMS416400P, TMS417400P).

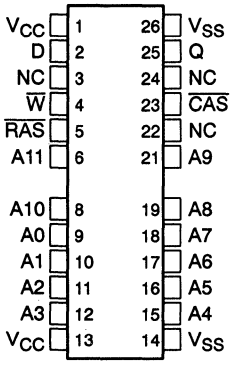
The TMS416100/P, TMS416400/P, and TMS417400/P are offered in a 300-mil 24/26-lead plastic surface mount SOJ package (DJ suffix), a 24/26-lead plastic small outline package (DGA suffix), and a 24/26-lead plastic small outline package, reverse form (DGB suffix). All packages are characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

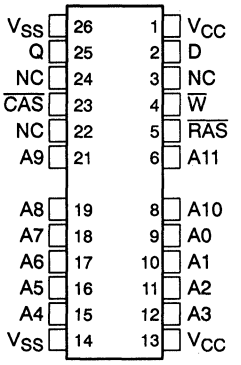
PRODUCT PREVIEW

TMS416100

DJ, DGA PACKAGE† (TOP VIEW)



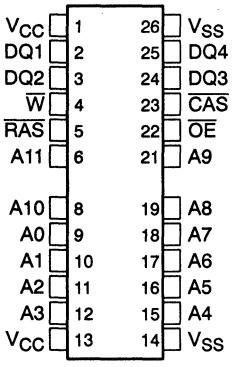
DGB PACKAGE† (TOP VIEW)



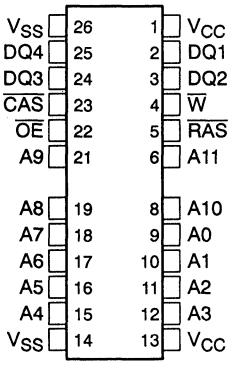
PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

TMS416400

DJ, DGA PACKAGE† (TOP VIEW)



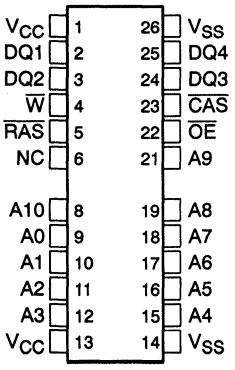
DGB PACKAGE† (TOP VIEW)



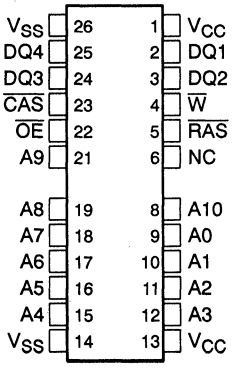
PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

TMS417400

DJ, DGA PACKAGE† (TOP VIEW)



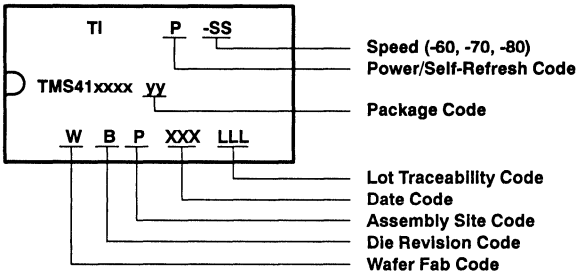
DGB PACKAGE† (TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

† The packages shown are for pinout reference only.

device symbolization



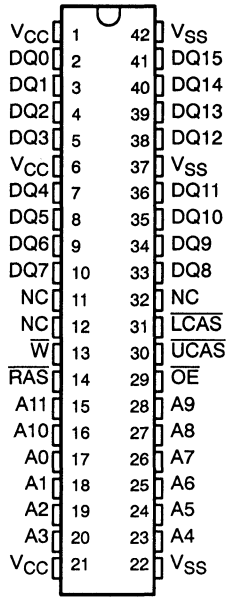
PRODUCT PREVIEW

- **Organization . . . 1 048 576 × 16**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

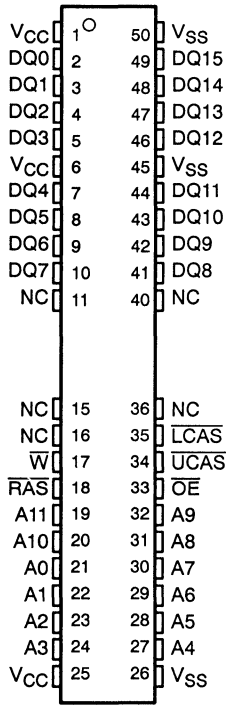
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'416160/P-60	60 ns	15 ns	30 ns	110 ns
'416160/P-70	70 ns	18 ns	35 ns	130 ns
'416160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  4096-Cycle Refresh in 64 ms (Max)
  512 ms Max for Low-Power, Self-Refresh Version (TMS416160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Self-Refresh with Low Power**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 44/50-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

RE PACKAGE†
(TOP VIEW)



DC PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS416160 series are high-speed, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

The TMS416160P series are high-speed, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 385 mW operating and 11 mW standby on 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS416160 and TMS416160P are each offered in a 42-lead plastic surface mount SOJ (RE suffix) package, and a 44/50-lead plastic surface mount TSOP (DC suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ pin going low enables its corresponding DQ pin with data coming from the column address to be latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early write cycles, the data is latched on the first falling $\overline{xCAS}$ edge. Only the DQs that have the corresponding $\overline{xCAS}$ low will be written into. Each $\overline{xCAS}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{xCAS}$ pins need to come high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 256 columns specified by column addresses A0 through A7 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, because data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A11)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Twelve row-address bits are set up on pins A0 through A11 and latched onto the chip by $\overline{RAS}$. Then, eight column–address bits are set up on pins A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every sixty-four milliseconds (512 ms for TMS416160P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{xCAS}$-before-$\overline{RAS}$ refresh

$\overline{xCAS}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS416160P. Data integrity is maintained using $\overline{xCAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

PRODUCT PREVIEW

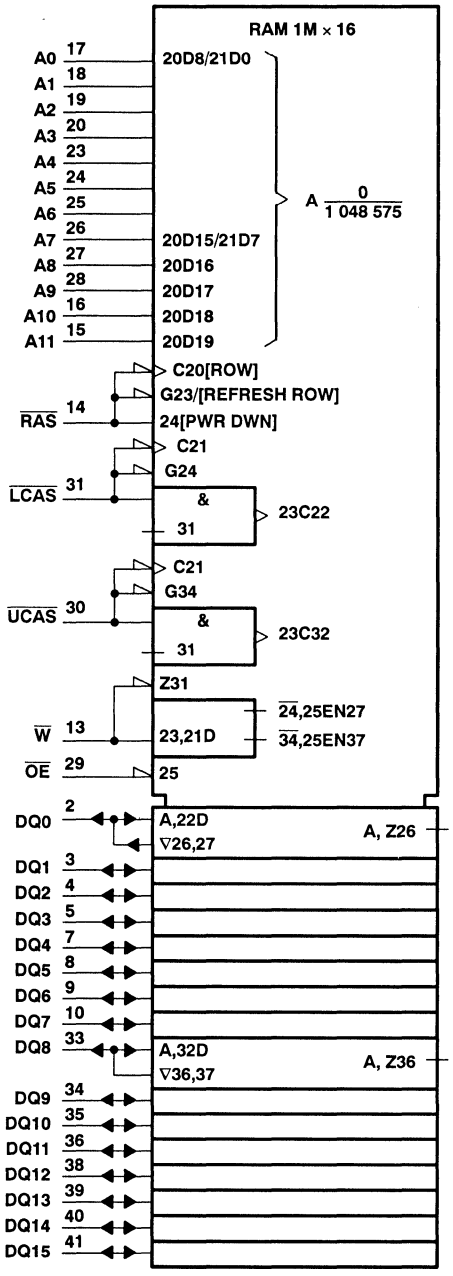
self refresh (TMS416160P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power up to the full V_{CC} level.

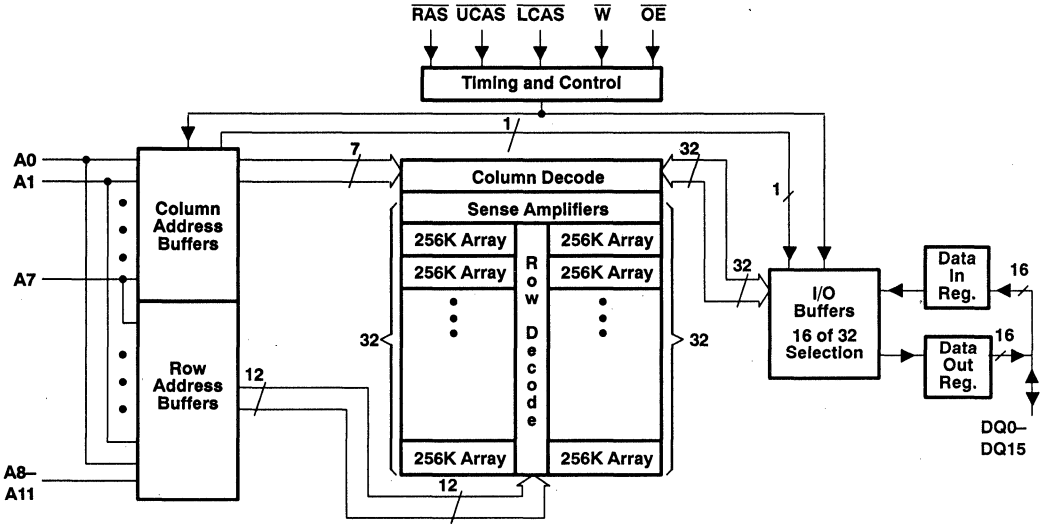
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the RE package.

PRODUCT PREVIEW

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . –1 V to 7 V
Supply voltage range on V_{CC} . . . . . –1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†‡	Read or write cycle current	V_{CC} = 5.5 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'416160		1		1		1	mA
			'416160P		500		500		500	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			90		80		70	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			90		80		70	mA
I_{CC6}¶	Self refresh	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			500		500		500	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}¶	Battery back-up operating current (equivalent refresh time is 512 ms). CBR only.	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA

† Measured with outputs open.
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}.
¶ For TMS416160P only.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

PRODUCT PREVIEW

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		15		18		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low Z	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	18	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	110		130		150		ns
t_{WC}	Write cycle time	110		130		150		ns
t_{RWC}	Read-write/read-modify-write cycle time	155		181		205		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high (precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{xCAS}$ high	15		18		20		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{xCAS}$ low time (t_{CAS}).
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{CAH}	Column-address hold time after $\overline{xCAS}$ low	10		15		15		ns
t_{DH}	Data hold time after $\overline{xCAS}$ low (see Note 10)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{xCAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{xCAS}$ low (see Note 12)	15		15		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (see Note 11)	20		20		20		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (see Note 14)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	15		18		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 15)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{xCAS}$ precharge	60		68		75		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{xCAS}$ precharge	35		40		45		ns
t_{CPR}	$\overline{xCAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	110		130		150		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.
11. $\overline{xCAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to assure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

		'416160-60 '416160P-60		'416160-70 '416160P-70		'416160-80 '416160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{CHS}	$\overline{xCAS}$ low hold time after $\overline{RAS}$ high (self refresh)	−50		−50		−50		ns
t_{REF}	Refresh time interval (TMS416160)		64		64		64	ms
t_{REF}	Refresh time interval, low power (TMS416160P only)		512		512		512	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.

PARAMETER MEASUREMENT INFORMATION

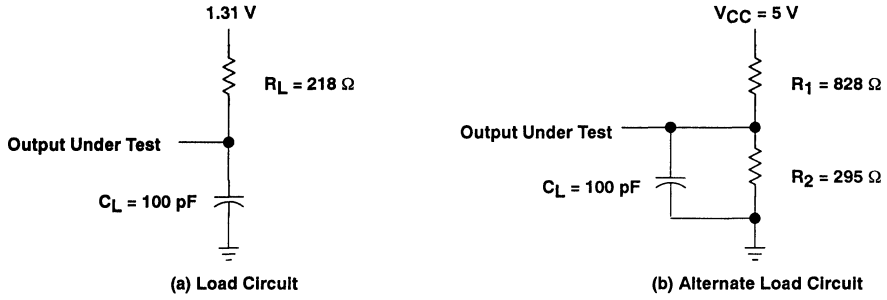

Figure 1. Load Circuits for Timing Parameters

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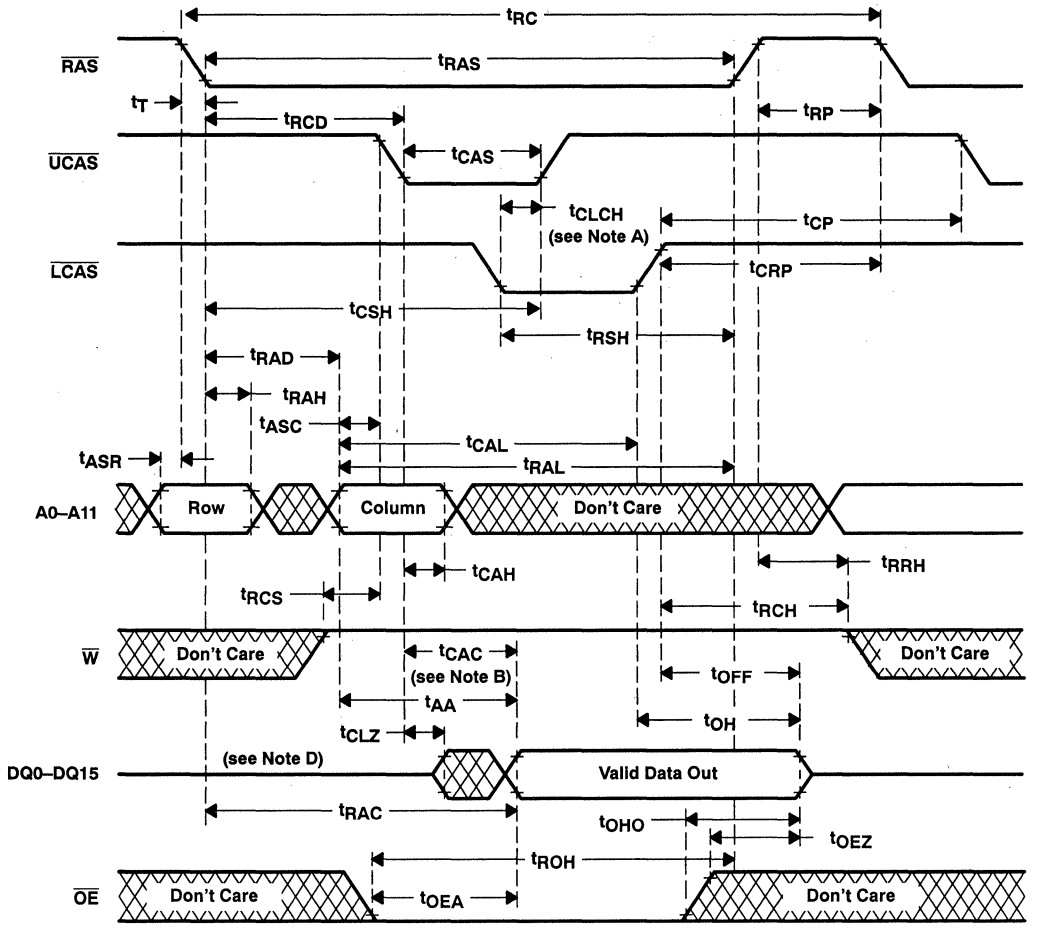
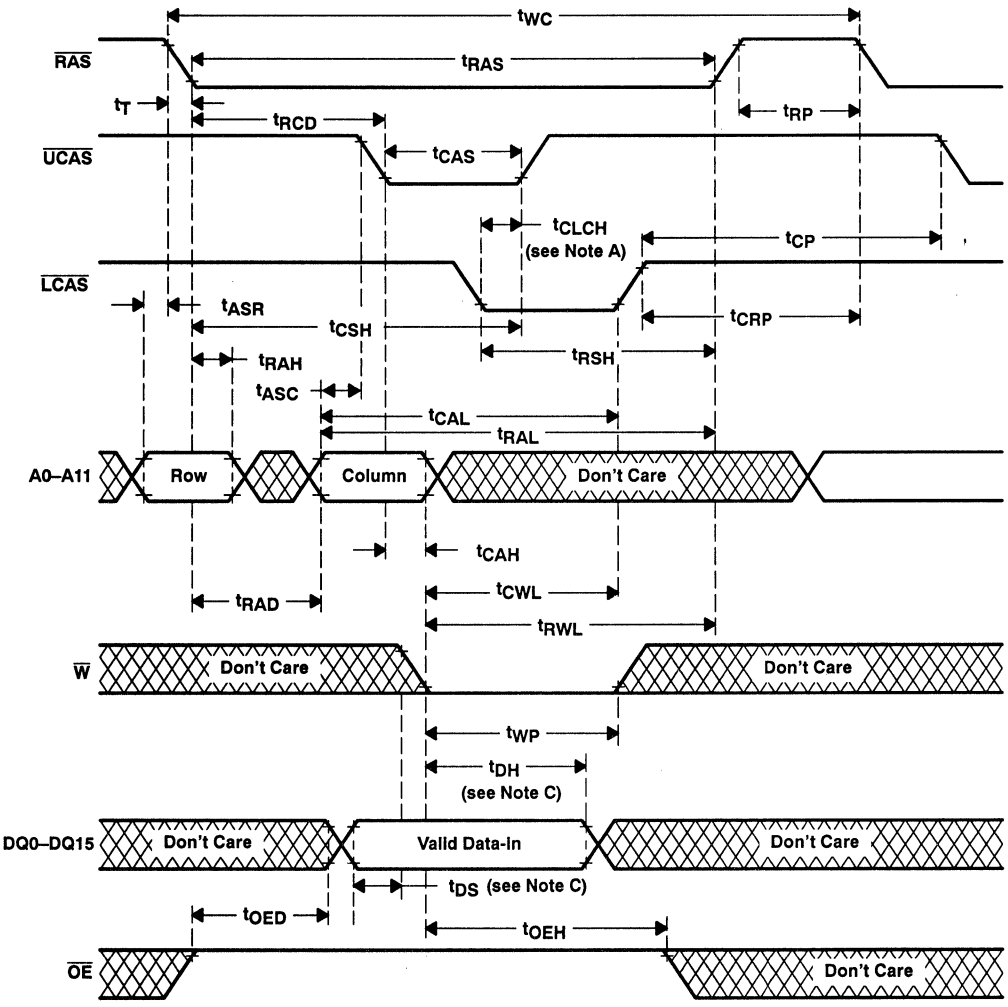
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

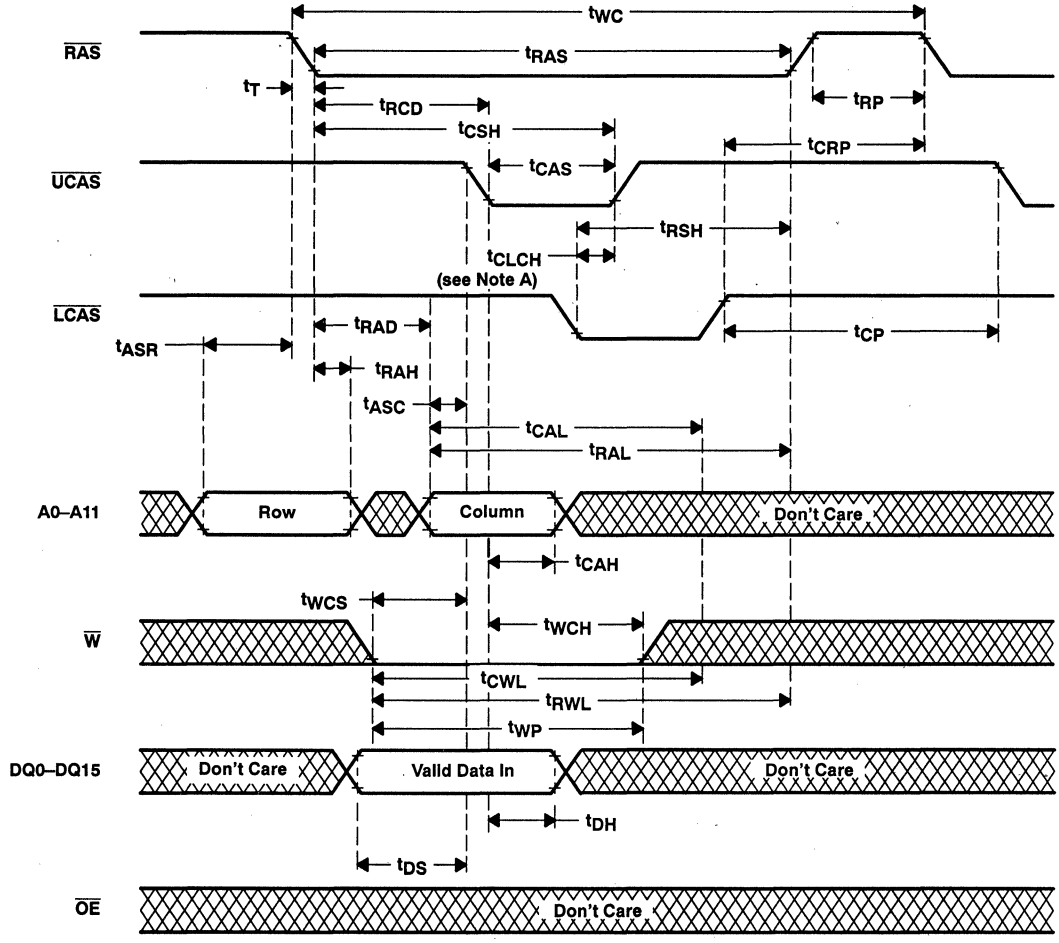


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 3. Write Cycle Timing

PRODUCT PREVIEW

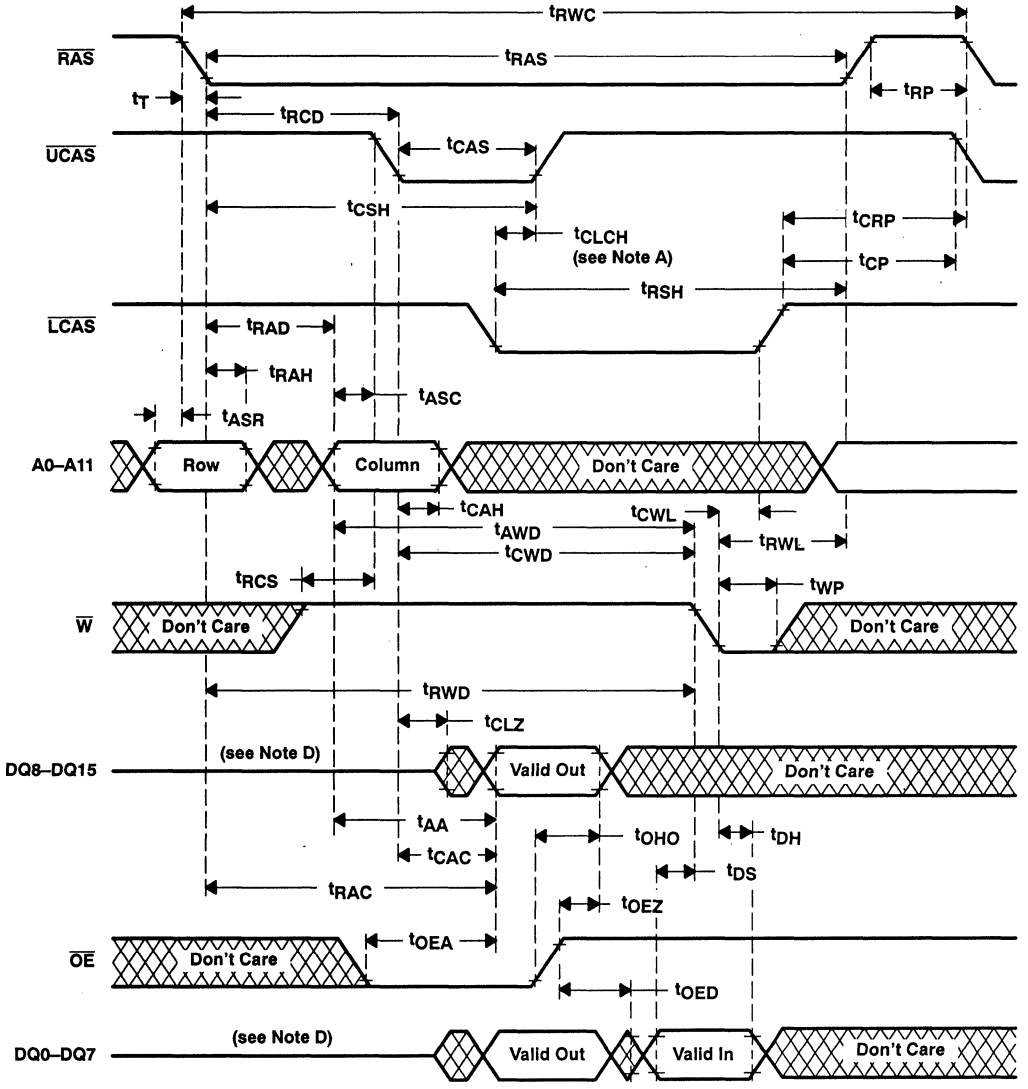
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

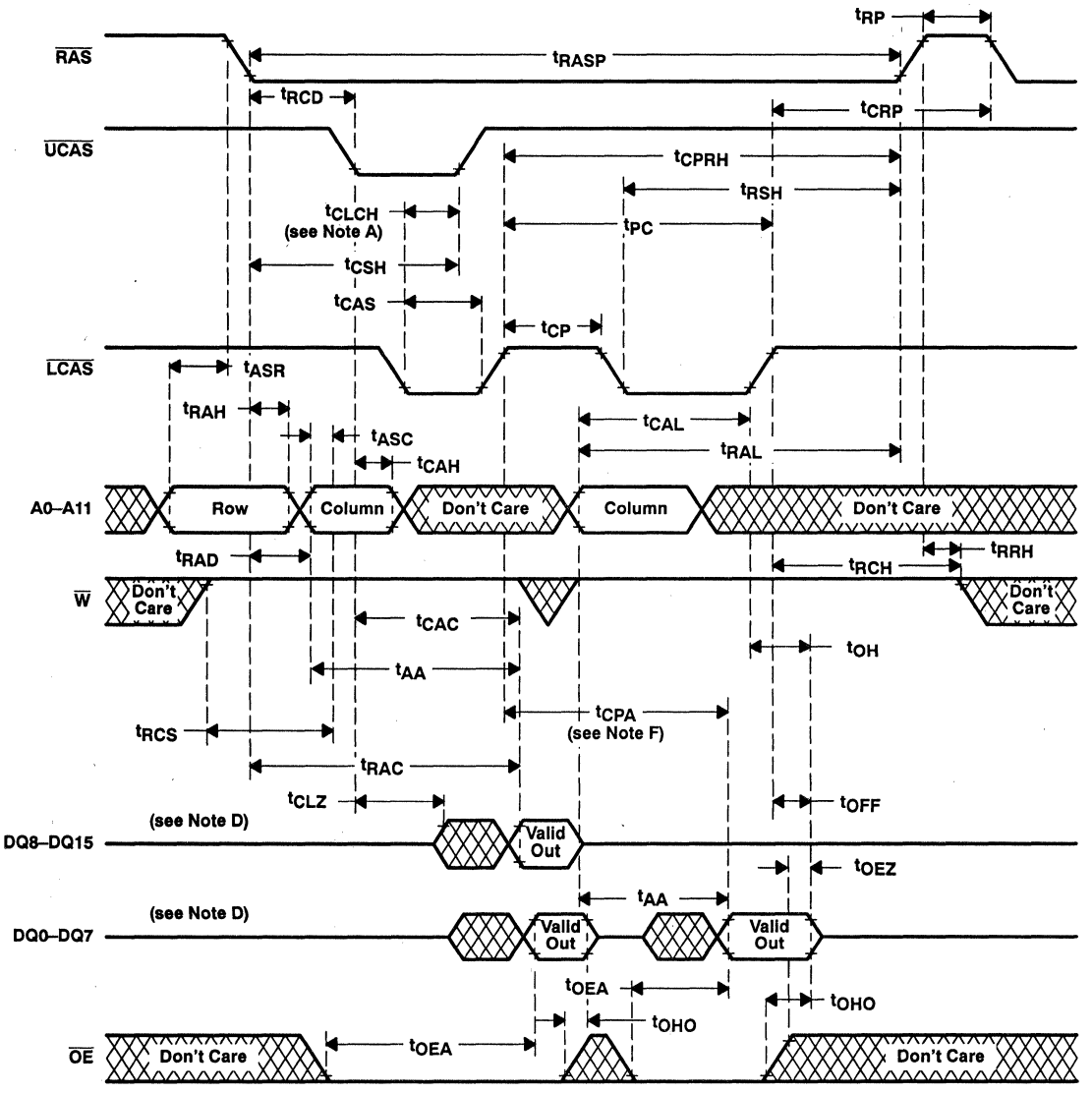


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. t_{CAC} in measured from $\overline{xCAS}$ to its corresponding DQx.
D. Output might go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

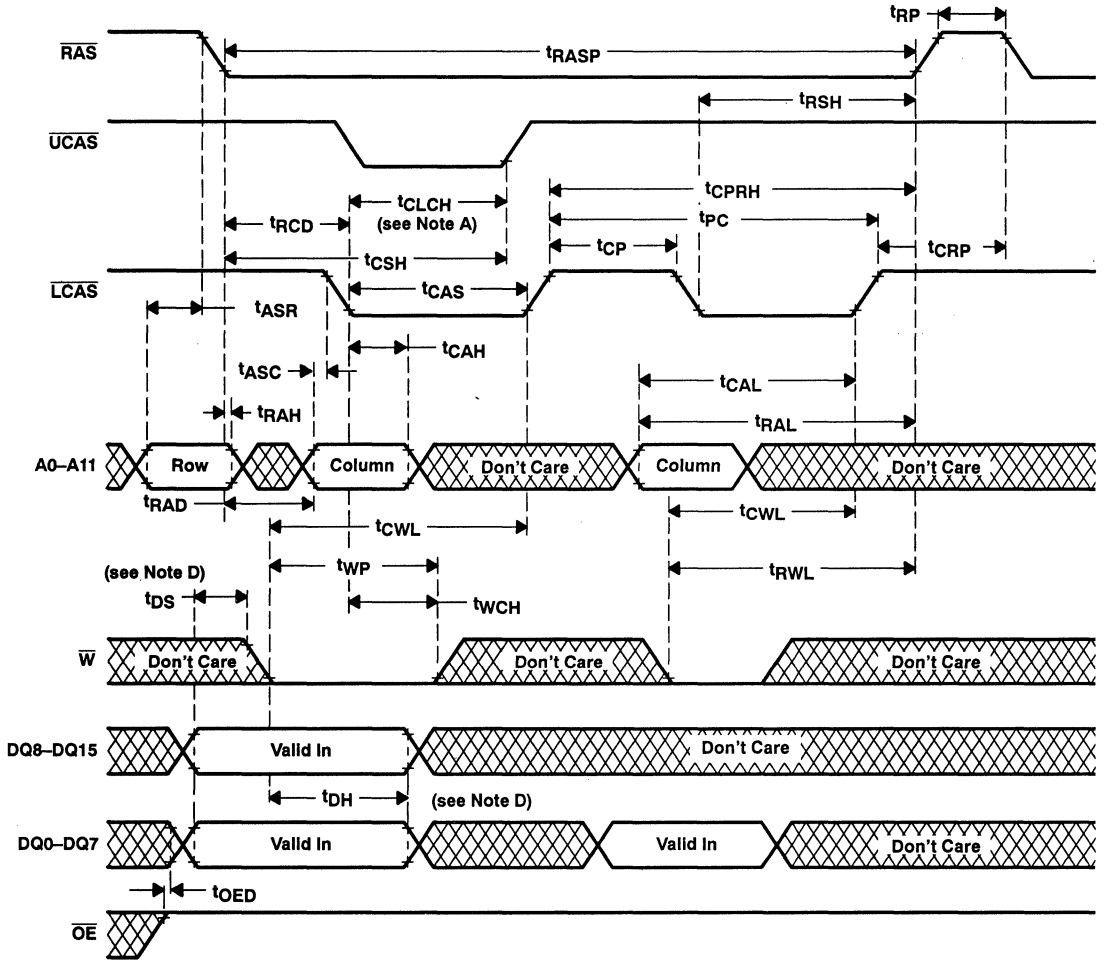
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

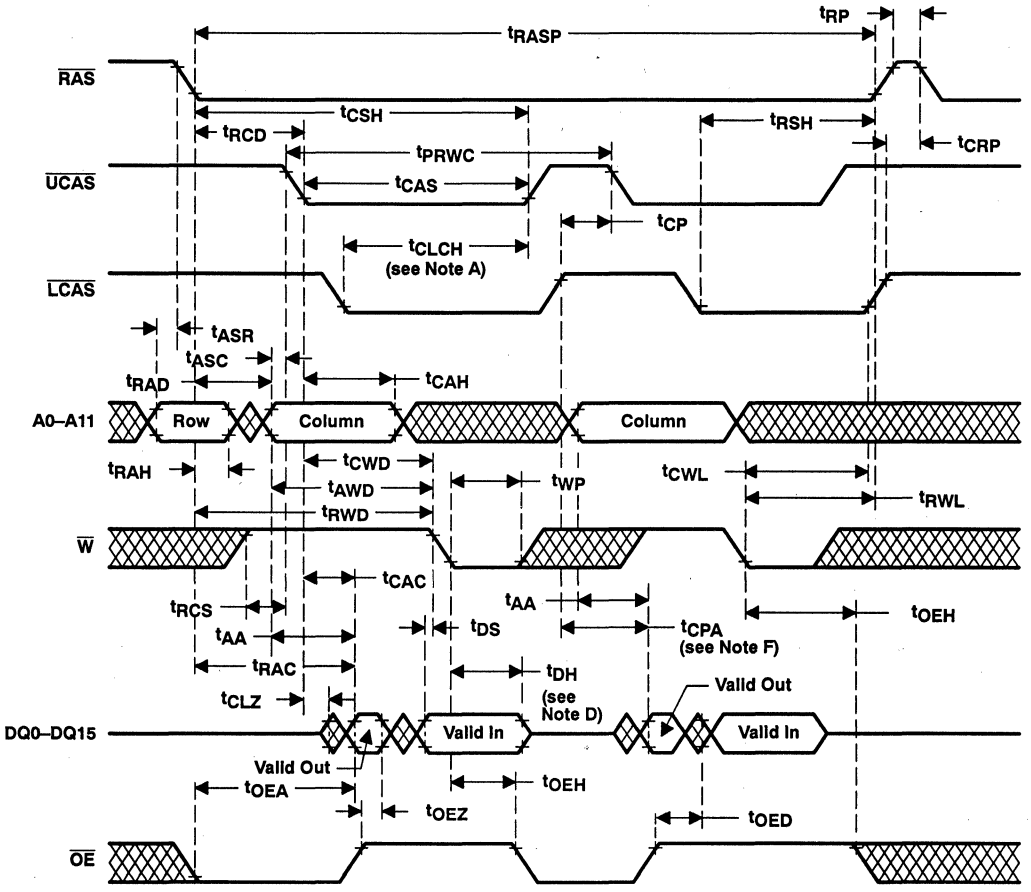


NOTES: A. In order to hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. xCAS order is arbitrary.
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
D. Referenced to the first xCAS or W, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

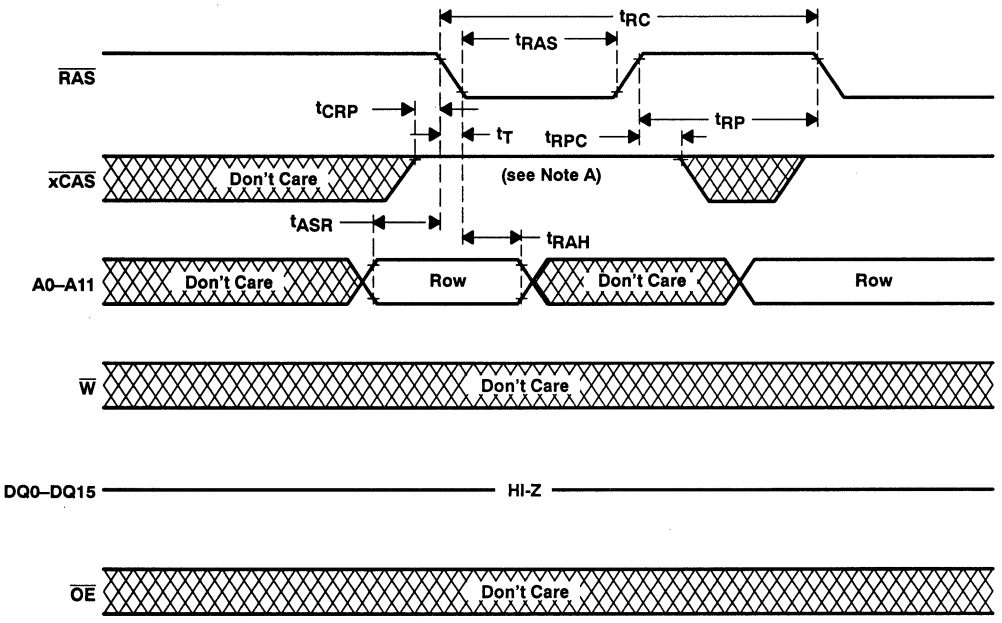
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

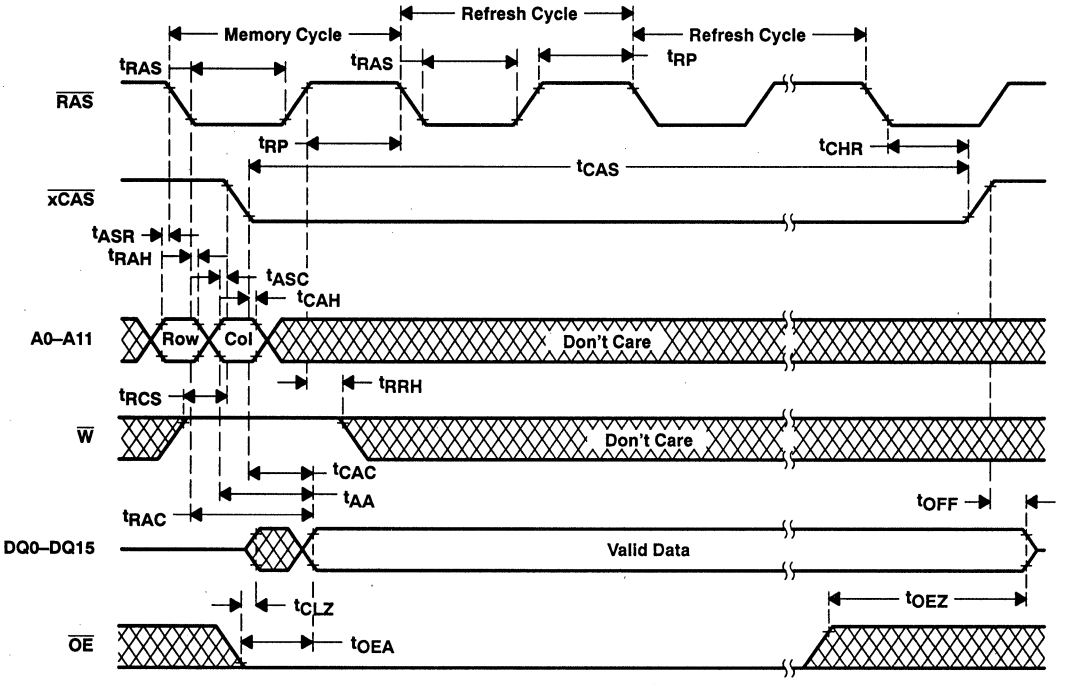


Figure 10. Hidden Refresh Cycle Timing

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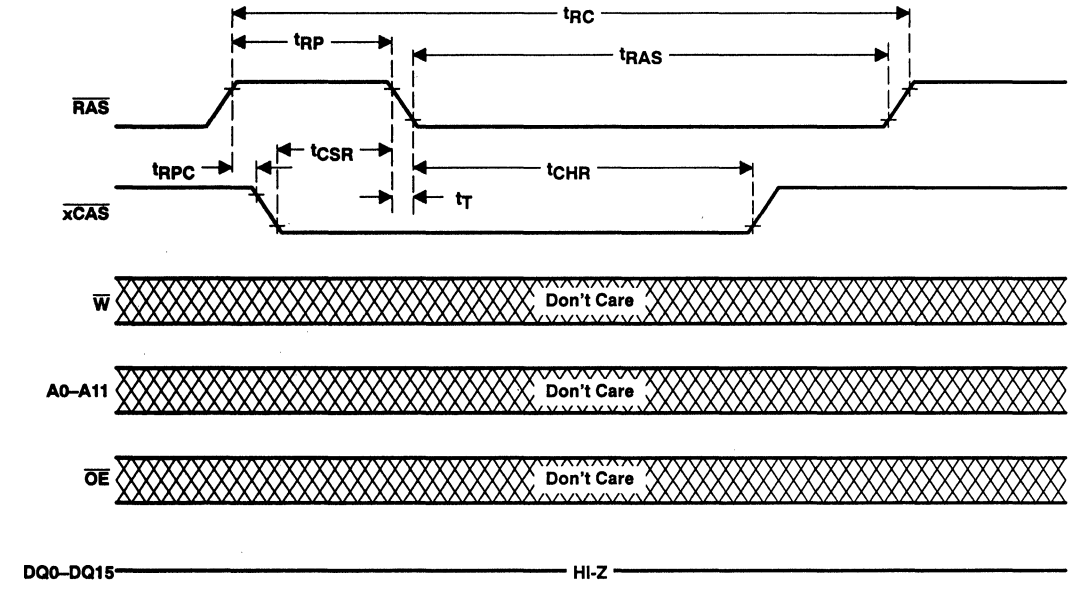
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Any $\overline{xCAS}$ may be used.

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

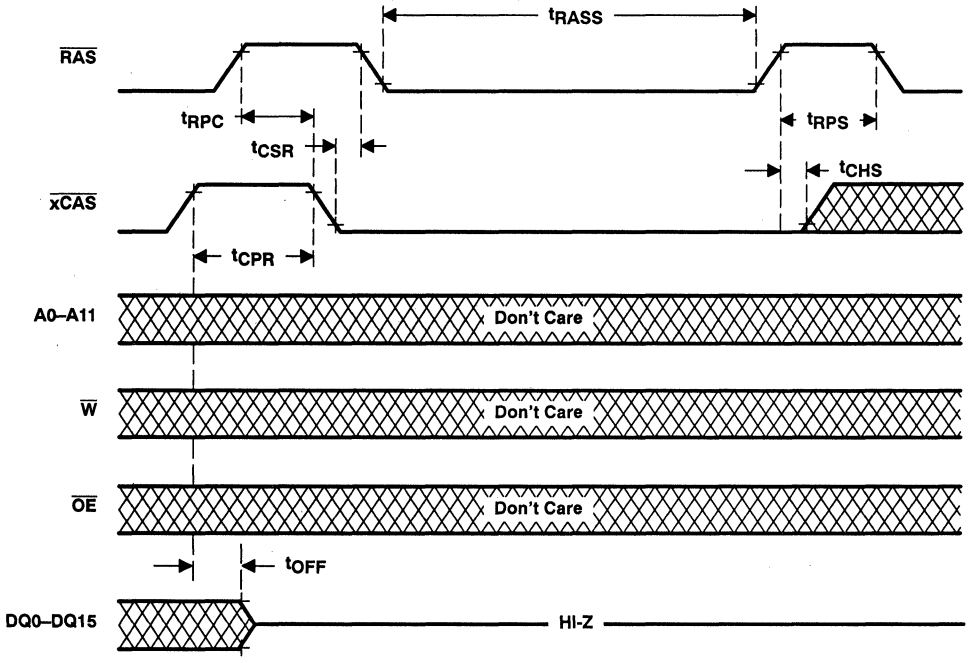
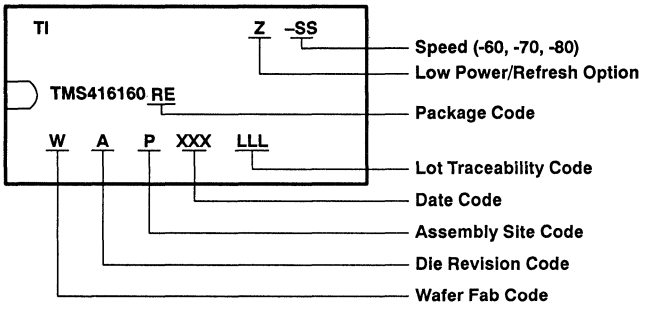


Figure 12. Self Refresh Timing

device symbolization

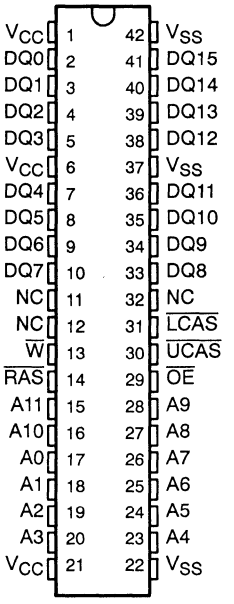


- **Organization . . . 1 048 576 × 16**
- **Single 3.3-V Supply (± 0.3 V Tolerance)**
- **Performance Ranges:**

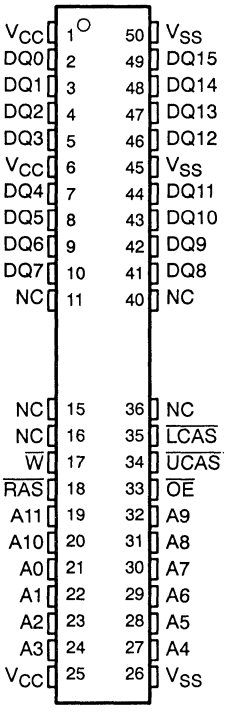
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'426160/P-70	70 ns	18 ns	35 ns	130 ns
'426160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  4096-Cycle Refresh in 64 ms (Max)
  512 ms Max for Low-Power, Self-Refresh Version (TMS426160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
  - **100 μA CMOS Standby**
  - **100 μA Extended Refresh Battery Backup**
- **Self-Refresh with Low Power**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 44/50-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

RE PACKAGE† (TOP VIEW)



DC PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

description

The TMS426160 series are high-speed, low voltage, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

The TMS426160P series are high-speed, low voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns and 80 ns. Maximum power dissipation is as low as 0.36 mW standby and battery backup on 80-ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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PRODUCT PREVIEW

The TMS426160 and TMS426160P are each offered in a 42-lead plastic surface mount SOJ (RE suffix) package, and a 44/50-lead plastic surface mount TSOP (DC suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ pin going low enables its corresponding DQ pin with data coming from the column address to be latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge. The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early write cycles, the data is latched on the first falling $\overline{xCAS}$ edge. Only the DQs that have the corresponding $\overline{xCAS}$ low will be written into. Each $\overline{xCAS}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{xCAS}$ pins need to come high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 256 columns specified by column addresses A0 through A7 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, because data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as *enhanced page mode.* Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A11)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Twelve row-address bits are set up on pins A0 through A11 and latched onto the chip by $\overline{RAS}$. Then, eight column–address bits are set up on pins A0 through A7 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

PRODUCT PREVIEW

write enable ($\overline{W}$)

The read or write mode is selected through the $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every sixty-four milliseconds (512 ms for TMS426160P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{xCAS}$-before-$\overline{RAS}$ refresh

$\overline{xCAS}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS426160P. Data integrity is maintained using $\overline{xCAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

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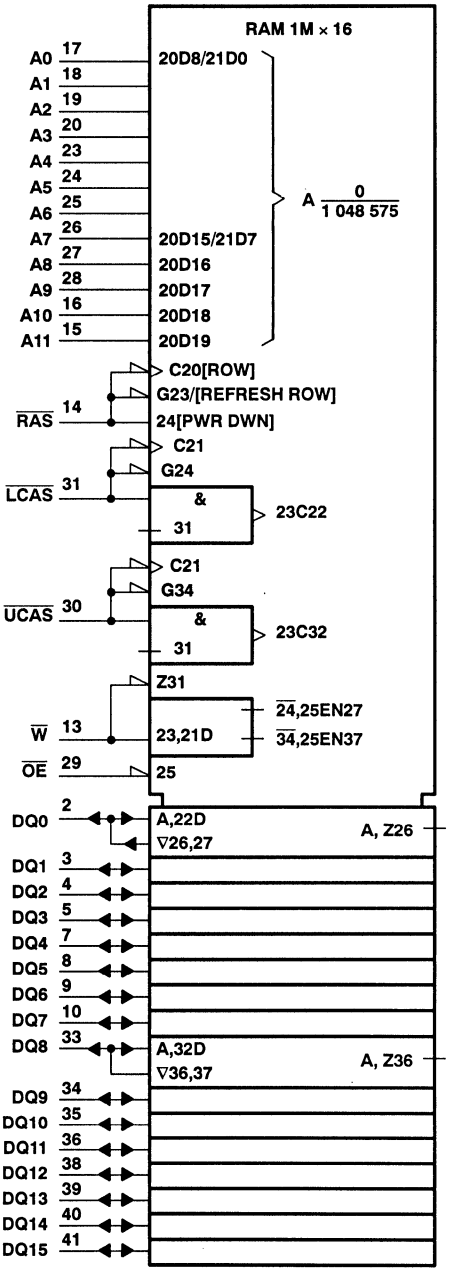
self refresh (TMS426160P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the RE package.

PRODUCT PREVIEW

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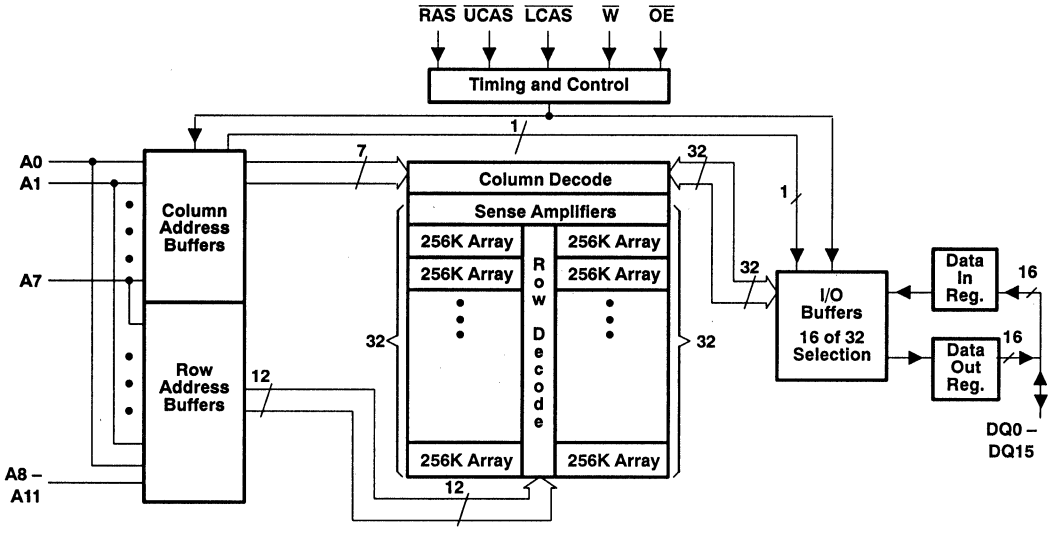
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Supply voltage range on V_{CC} . . . . . – 0.5 V to 4.6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'426160-70 '426160P-70 MIN	'426160-70 '426160P-70 MAX	'426160-80 '426160P-80 MIN	'426160-80 '426160P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC}–0.2		V_{CC}–0.2		V
V_{OL}	Option	I_{OL} = 100 µA			0.2		0.2	V
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 to 3.9 V, All other pins = 0 V to V_{CC}			± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 to V_{CC}, $\overline{xCAS}$ high			± 10		± 10	µA
I_{CC1}†‡	Read or write cycle current	V_{CC} = 3.6 V, Minimum cycle			80		70	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'426160		300		300	µA
			'426160P		100		100	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			80		70	mA
I_{CC4}†§	Average page current	V_{CC} = 3.6 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			80		70	mA
I_{CC6}¶	Self refresh	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			100		100	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled			5		5	mA
I_{CC10}¶	Battery back-up operating current (equivalent refresh time is 512 ms). CBR only.	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100	µA

† Measured with outputs open.
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}.
¶ For TMS426160P only.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'426160-70 '426160P-70		'426160-80 '426160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		18		20	ns
t_{AA}	Access time from column address		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20	ns
t_{CPA}	Access time from column precharge		40		45	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low Z	0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	18	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'426160-70 '426160P-70		'426160-80 '426160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{RWC}	Read-write/read-modify-write cycle time	181		205		ns
t_{PRWC}	Page-mode read-modify-write cycle time	96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high (precharge)	10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		ns
t_{WP}	Write pulse duration	15		15		ns
t_{ASC}	Column-address setup time before $\overline{xCAS}$ low	0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		ns
t_{RCS}	Read setup time before $\overline{xCAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{xCAS}$ high	18		20		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{xCAS}$ low time (t_{CAS}).
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

		'426160-70 '426160P-70		'426160-80 '426160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	18		20		ns
t_{WCS}	$\overline{W}$-low setup time before x$\overline{CAS}$ low	0		0		ns
t_{CAH}	Column-address hold time after x$\overline{CAS}$ low	15		15		ns
t_{DH}	Data hold time after x$\overline{CAS}$ low (see Note 10)	15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		ns
t_{RCH}	Read hold time after x$\overline{CAS}$ high (see Note 13)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		ns
t_{WCH}	Write hold time after x$\overline{CAS}$ low (see Note 12)	15		15		ns
t_{CLCH}	Hold time, x$\overline{CAS}$ low to x$\overline{CAS}$ high	5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ high (see Note 11)	20		20		ns
t_{CRP}	Delay time, x$\overline{CAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ high	70		80		ns
t_{CSR}	Delay time, x$\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		ns
t_{CWD}	Delay time, x$\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	18		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	18		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		ns
t_{CAL}	Delay time, column address to x$\overline{CAS}$ high	35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ low (see Note 15)	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to x$\overline{CAS}$ low	0		0		ns
t_{RSH}	Delay time, x$\overline{CAS}$ low to $\overline{RAS}$ high	18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from x$\overline{CAS}$ precharge	68		75		ns
t_{CPRH}	$\overline{RAS}$ hold time from x$\overline{CAS}$ precharge	40		45		ns
t_{CPR}	x$\overline{CAS}$ precharge before self refresh	0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Reference to the first x$\overline{CAS}$ or $\overline{W}$, whichever occurs last.
11. x$\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to assure access time.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

		'426160-70 '426160P-70		'426160-80 '426160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		µs
t_{CHS}	$\overline{xCAS}$ low hold time after $\overline{RAS}$ high (self refresh)	−50		−50		ns
t_{REF}	Refresh time interval (TMS426160)		64		64	ms
t_{REF}	Refresh time interval, low power (TMS426160P only)		512		512	ms
t_T	Transition time	3	30	3	30	ns

NOTE 5: Timing measurements are referenced to V_{IL} max and V_{IH} min.

PARAMETER MEASUREMENT INFORMATION

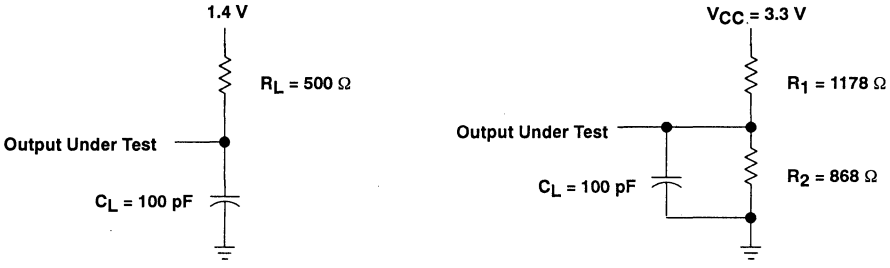

Figure 1. Load Circuits for Timing Parameters

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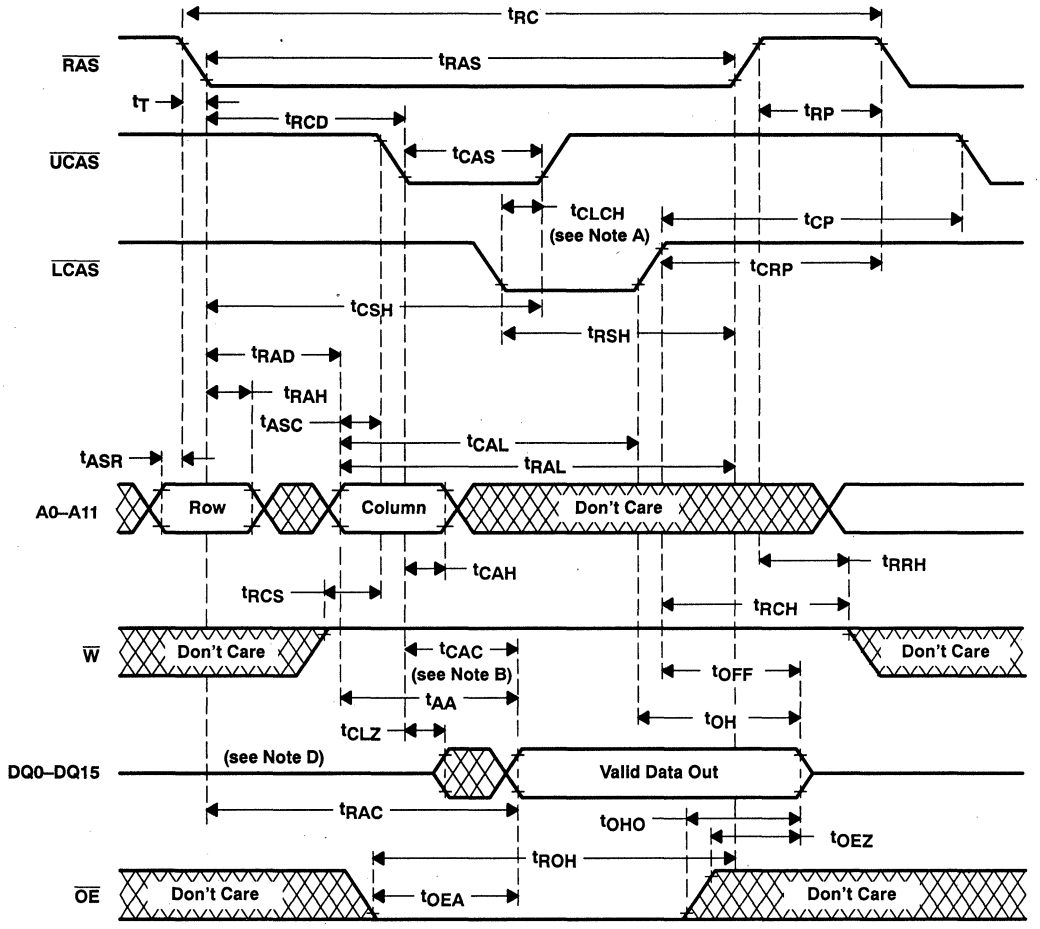
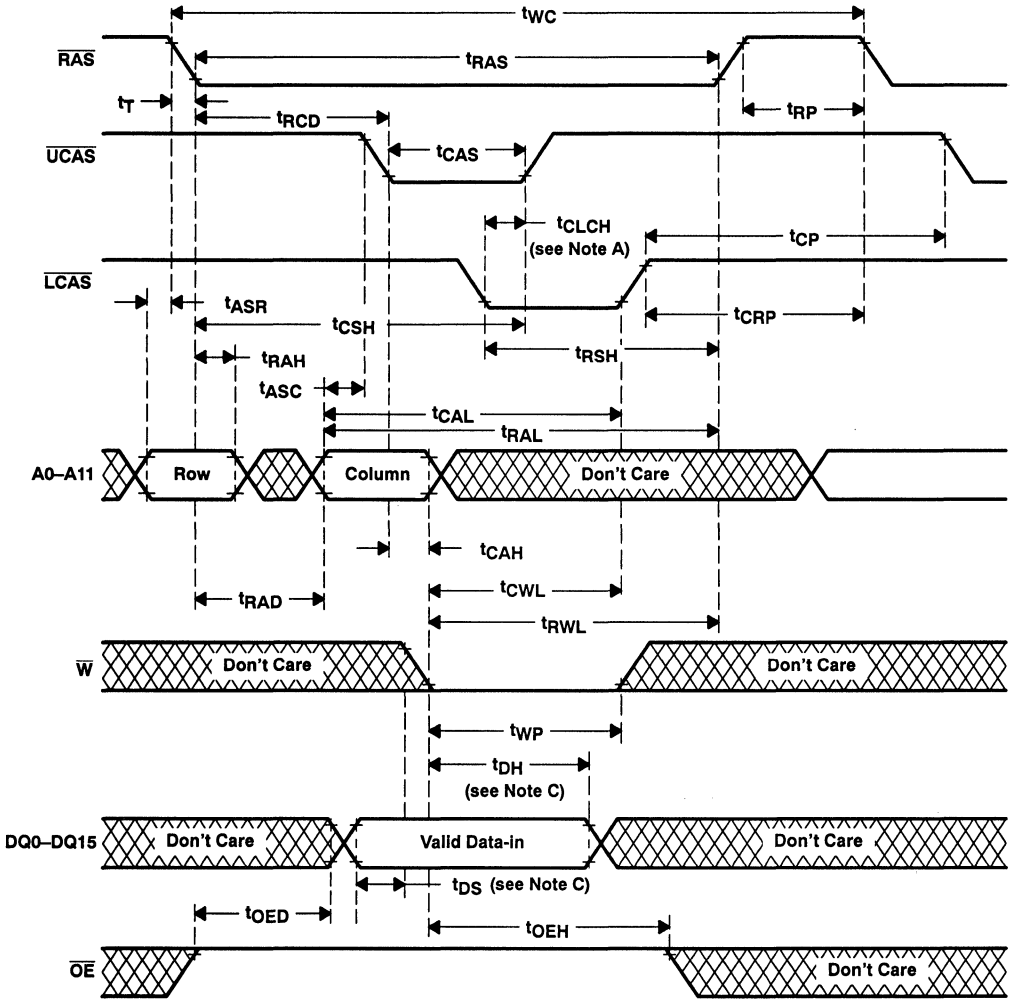
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 3. Write Cycle Timing

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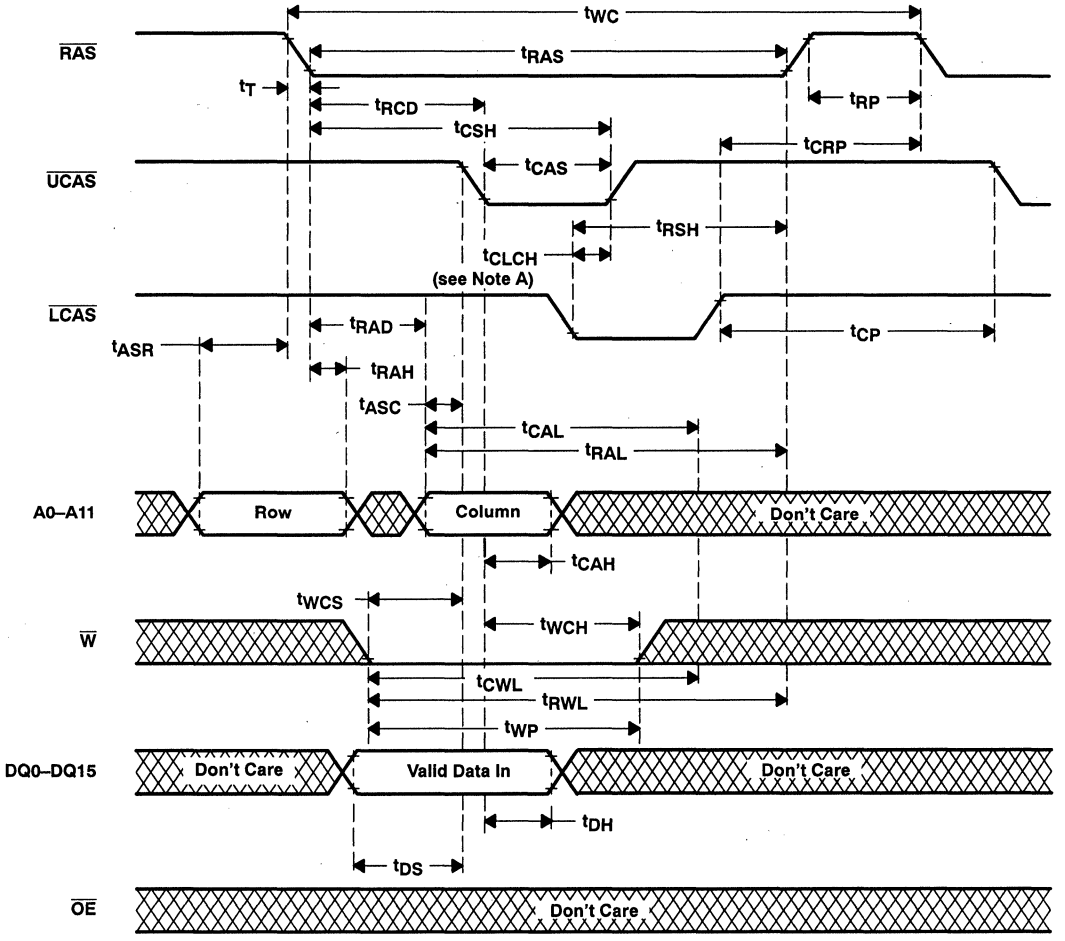
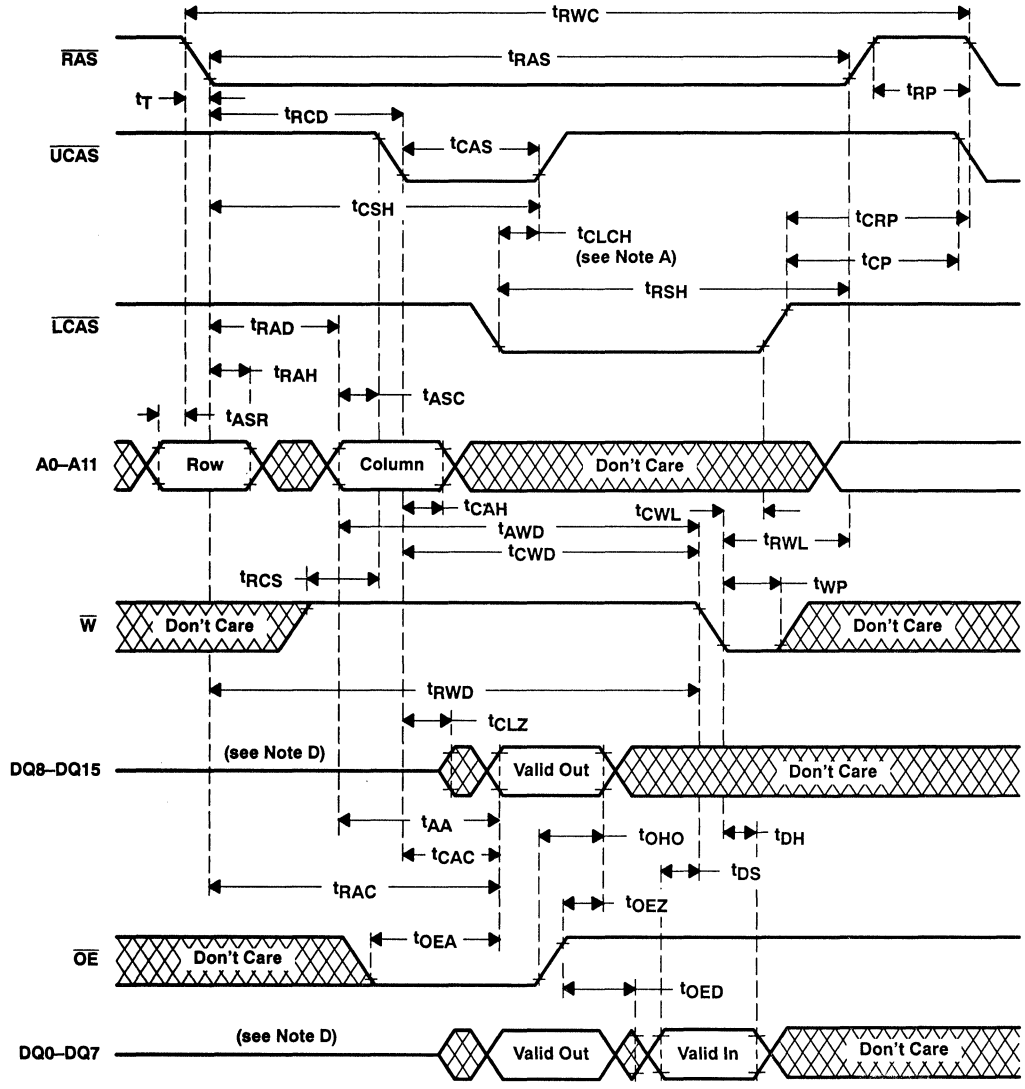
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. t_{CAC} in measured from $\overline{xCAS}$ to its corresponding DQx.
D. Output might go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

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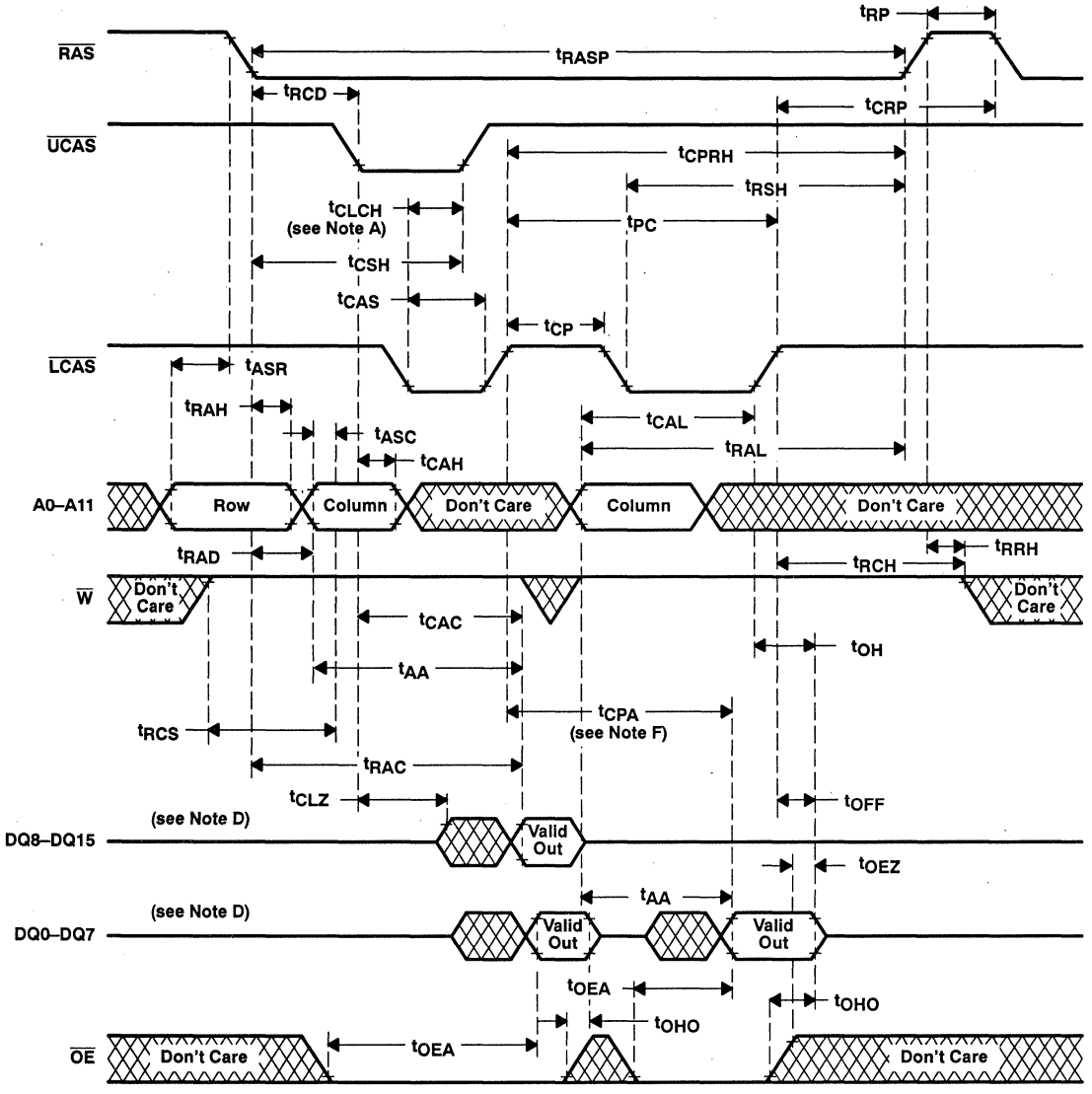
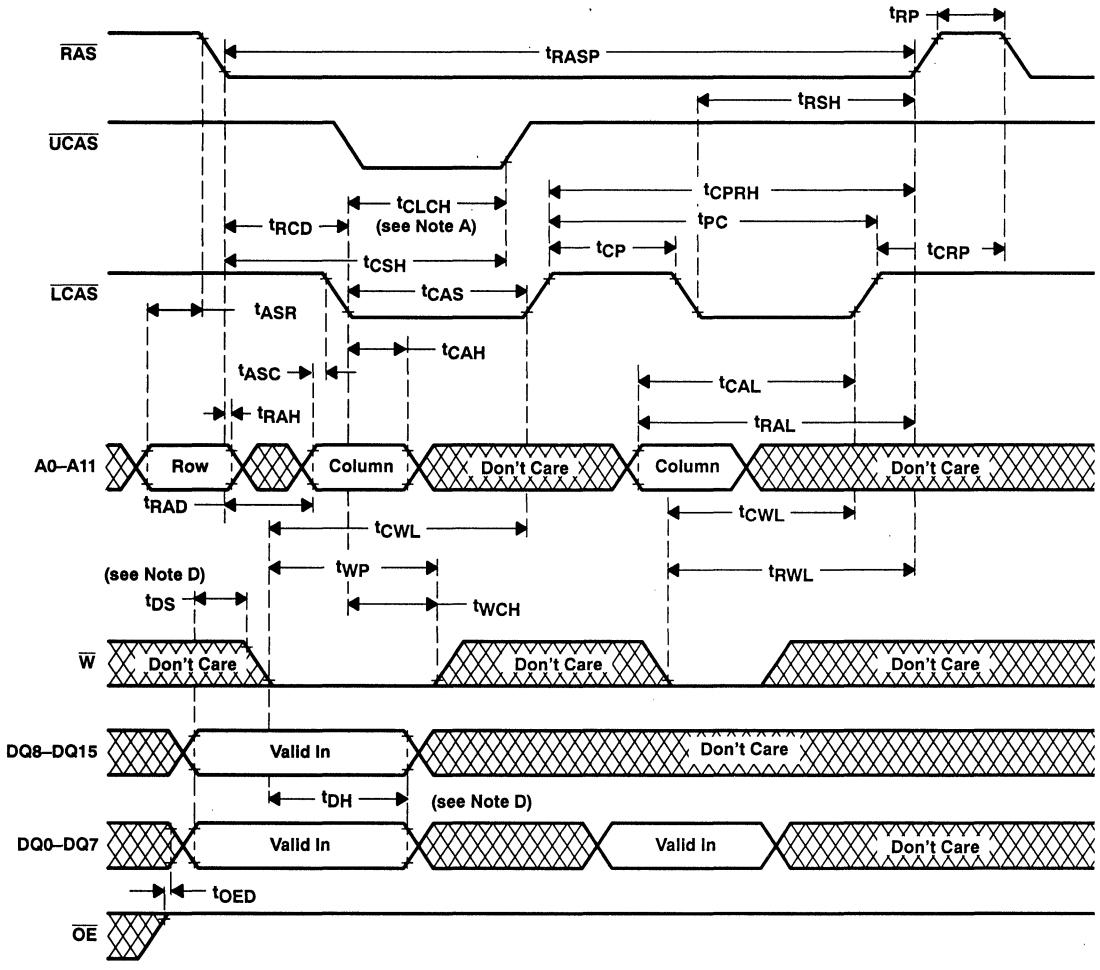
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
D. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

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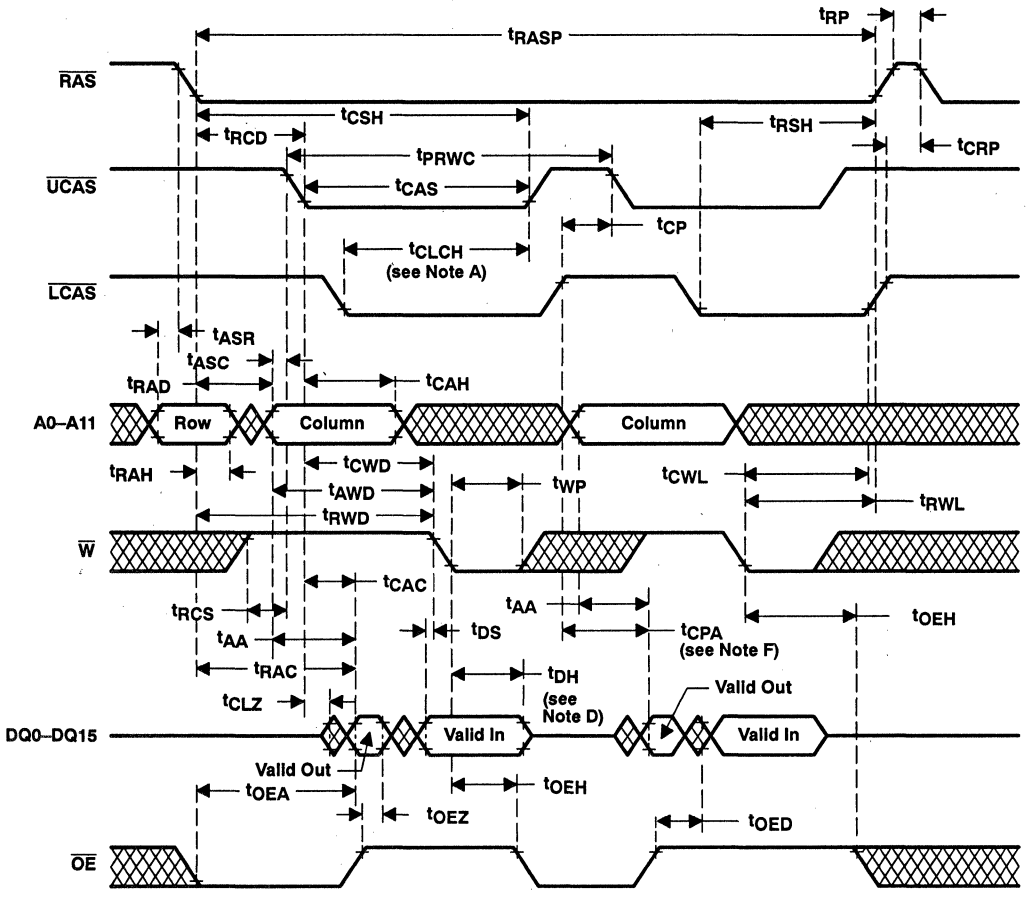
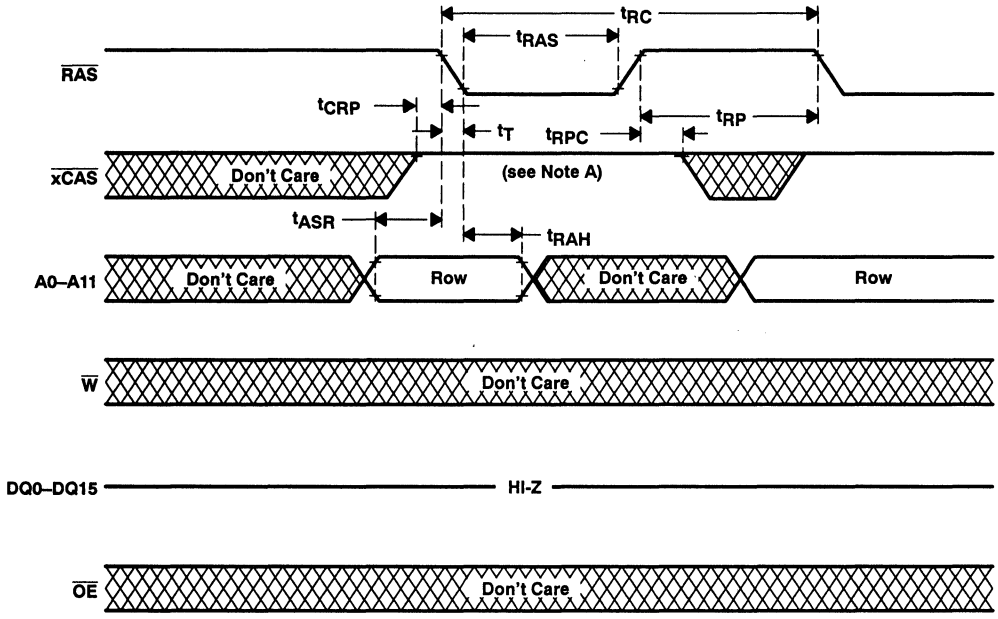
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

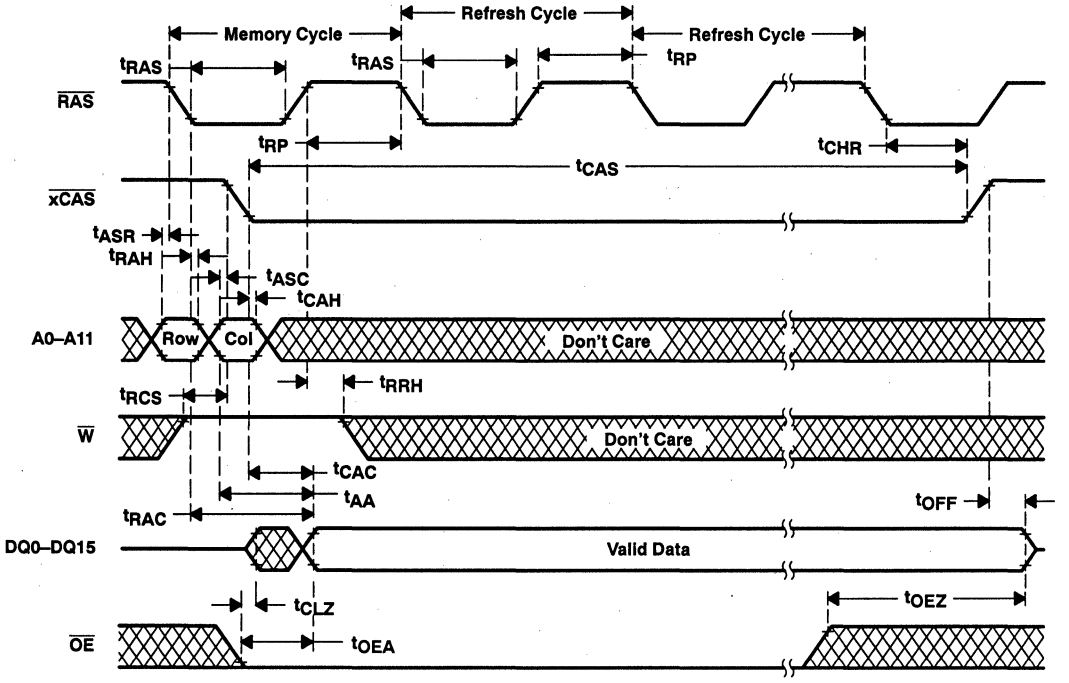

Figure 10. Hidden Refresh Cycle Timing

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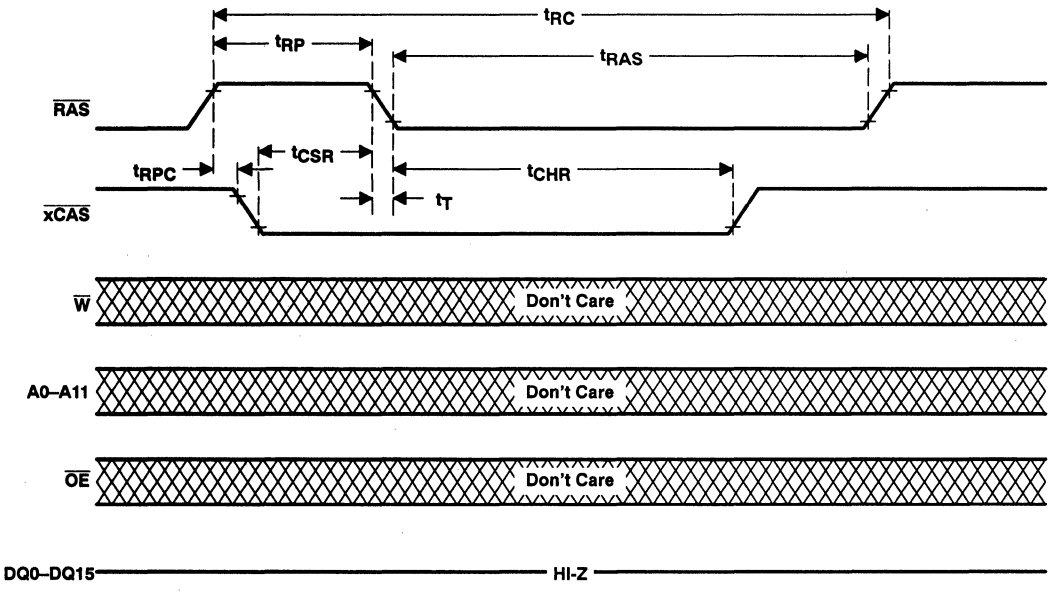
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Any $\overline{xCAS}$ may be used.

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

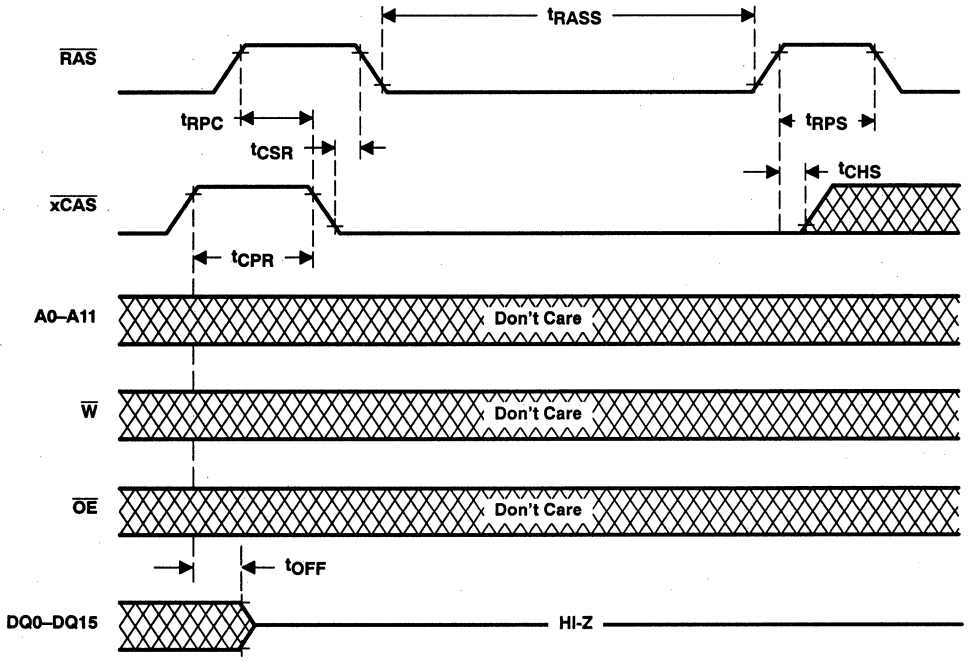
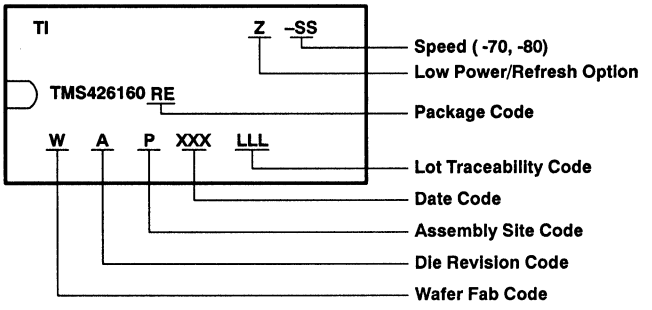


Figure 12. Self Refresh Timing

device symbolization



PRODUCT PREVIEW

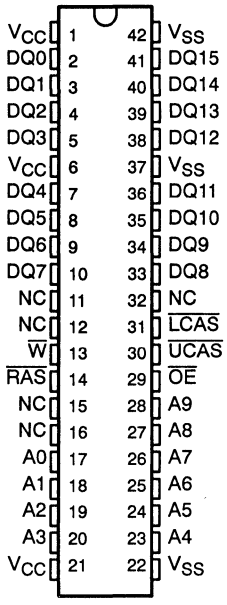
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

- **Organization . . . 1 048 576 × 16**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

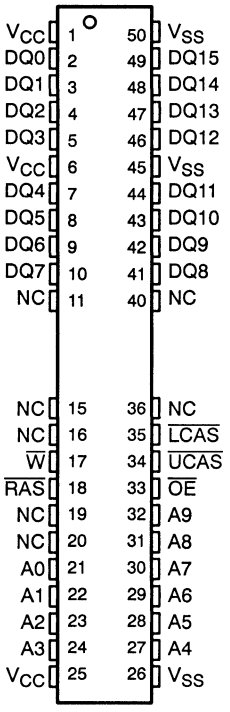
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'418160/P-60	60 ns	15 ns	30 ns	110 ns
'418160/P-70	70 ns	18 ns	35 ns	130 ns
'418160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  1024-Cycle Refresh in 16 ms (Max)
  128 ms Max for Low-Power, Self-Refresh Version (TMS418160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Self-Refresh With Low Power**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 44/50-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

RE PACKAGE† (TOP VIEW)



DC PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only

PIN NOMENCLATURE	
A0–A9	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS418160 series are high-speed, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

The TMS418160P series are high-speed, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 11 mW standby on 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS418160 and TMS418160P are each offered in a 42-lead plastic surface mount SOJ (RE suffix) package, and a 44/50-lead plastic surface mount TSOP (DC suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ pin going low enables its corresponding DQ pin with data coming from the column address to be latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early write cycles, the data is latched on the first falling $\overline{xCAS}$ edge. Only the DQs that have the corresponding $\overline{xCAS}$ low will be written into. Each $\overline{xCAS}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{xCAS}$ pins need to come high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, because data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on pins A0 through A9 and latched onto the chip by $\overline{RAS}$. Then, ten column–address bits are set up on pins A0 through A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every sixteen milliseconds (128 ms for TMS418160P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{xCAS}$-before-$\overline{RAS}$ refresh

$\overline{xCAS}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS418160P. Data integrity is maintained using $\overline{xCAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

PRODUCT PREVIEW

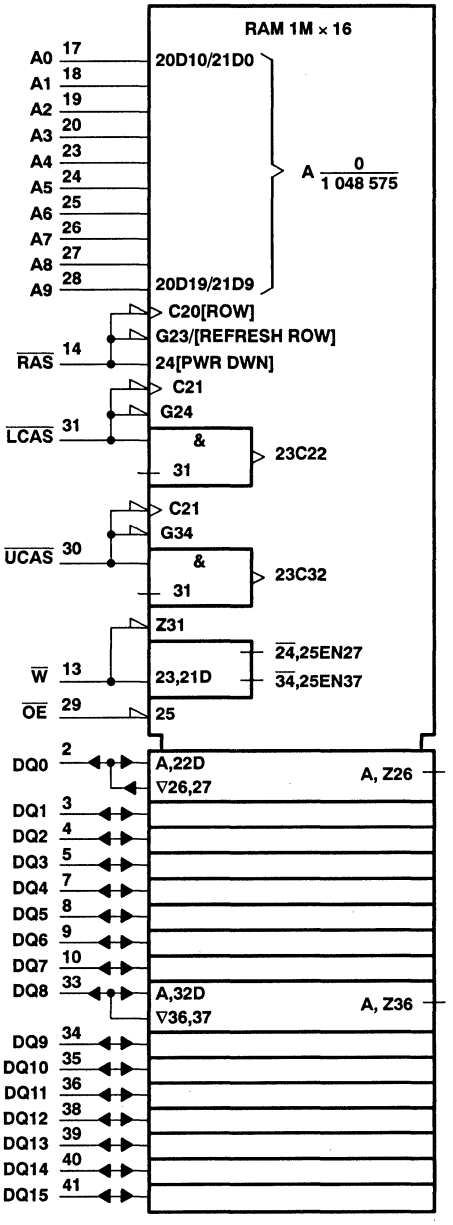
self refresh (TMS418160P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power-up to the full V_{CC} level.

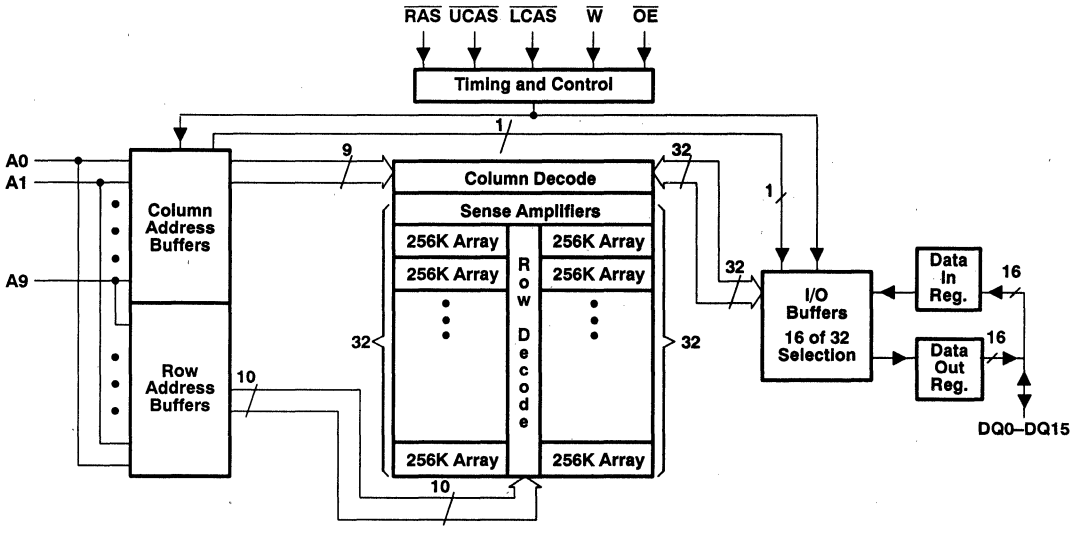
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the RE package.

PRODUCT PREVIEW

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Supply voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{xCAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†‡	Read or write cycle current	V_{CC} = 5.5 V, Minimum cycle			TBD		TBD		TBD	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'418160		1		1		1	mA
			'418160P		500		500		500	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			TBD		TBD		TBD	mA
I_{CC4}†§	Average page current	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			TBD		TBD		TBD	mA
I_{CC6}¶	Self refresh	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			500		500		500	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}¶	Battery back-up operating current (equivalent refresh time is 128 ms). CBR only.	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA

† Measured with outputs open.
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}.
¶ For TMS418160P only.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

	PARAMETER	MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		15		18		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low Z	0		0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	15	0	18	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	110		130		150		ns
t_{WC}	Write cycle time	110		130		150		ns
t_{RWC}	Read-write/read-modify-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high (precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{xCAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{xCAS}$ high	15		18		20		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{xCAS}$ low time (t_{CAS}).
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before x$\overline{CAS}$ low (see Note 12)	0		0		0		ns
t_{CAH}	Column-address hold time after x$\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time after x$\overline{CAS}$ low (see Note 10)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after x$\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		ns
t_{WCH}	Write hold time after x$\overline{CAS}$ low (see Note 12)	15		15		15		ns
t_{CLCH}	Hold time, x$\overline{CAS}$ low to x$\overline{CAS}$ high	5		5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ high (see Note 11)	20		20		20		ns
t_{CRP}	Delay time, x$\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, x$\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		ns
t_{CWD}	Delay time, x$\overline{CAS}$ low to $\overline{W}$ low (see Note 14)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	15		18		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to x$\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to x$\overline{CAS}$ low (see Note 15)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to x$\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, x$\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from x$\overline{CAS}$ precharge	60		68		75		ns
t_{CPRH}	$\overline{RAS}$ hold time from x$\overline{CAS}$ precharge	35		40		45		ns
t_{CPR}	x$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	110		130		150		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Reference to the first x$\overline{CAS}$ or $\overline{W}$, whichever occurs last.
11. x$\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to assure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

		'418160-60 '418160P-60		'418160-70 '418160P-70		'418160-80 '418160P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{CHS}	$\overline{xCAS}$ low hold time after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns
t_{REF}	Refresh time interval (TMS418160 only)		16		16		16	ms
t_{REF}	Refresh time interval, low power (TMS418160P only)		128		128		128	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.

PARAMETER MEASUREMENT INFORMATION

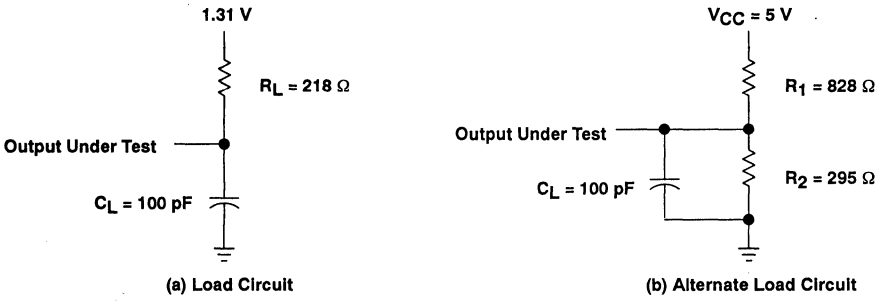
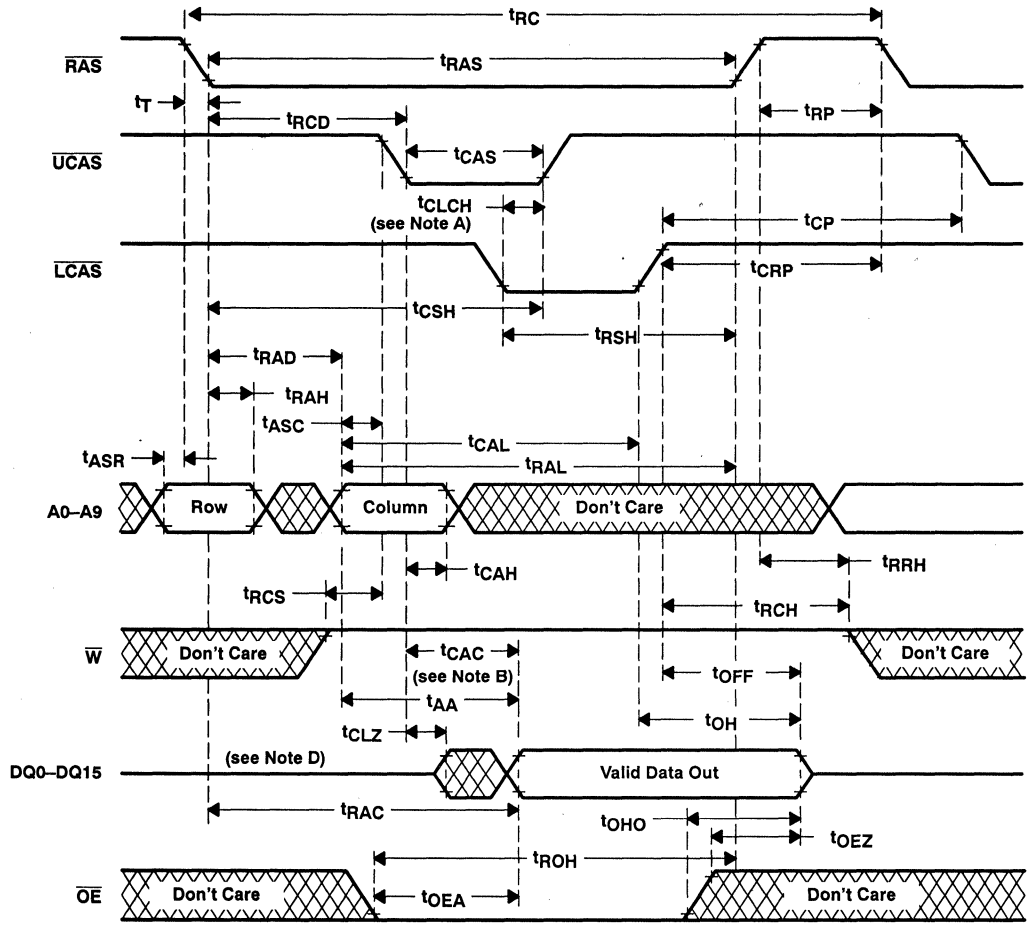


Figure 1. Load Circuits for Timing Parameters

PRODUCT PREVIEW

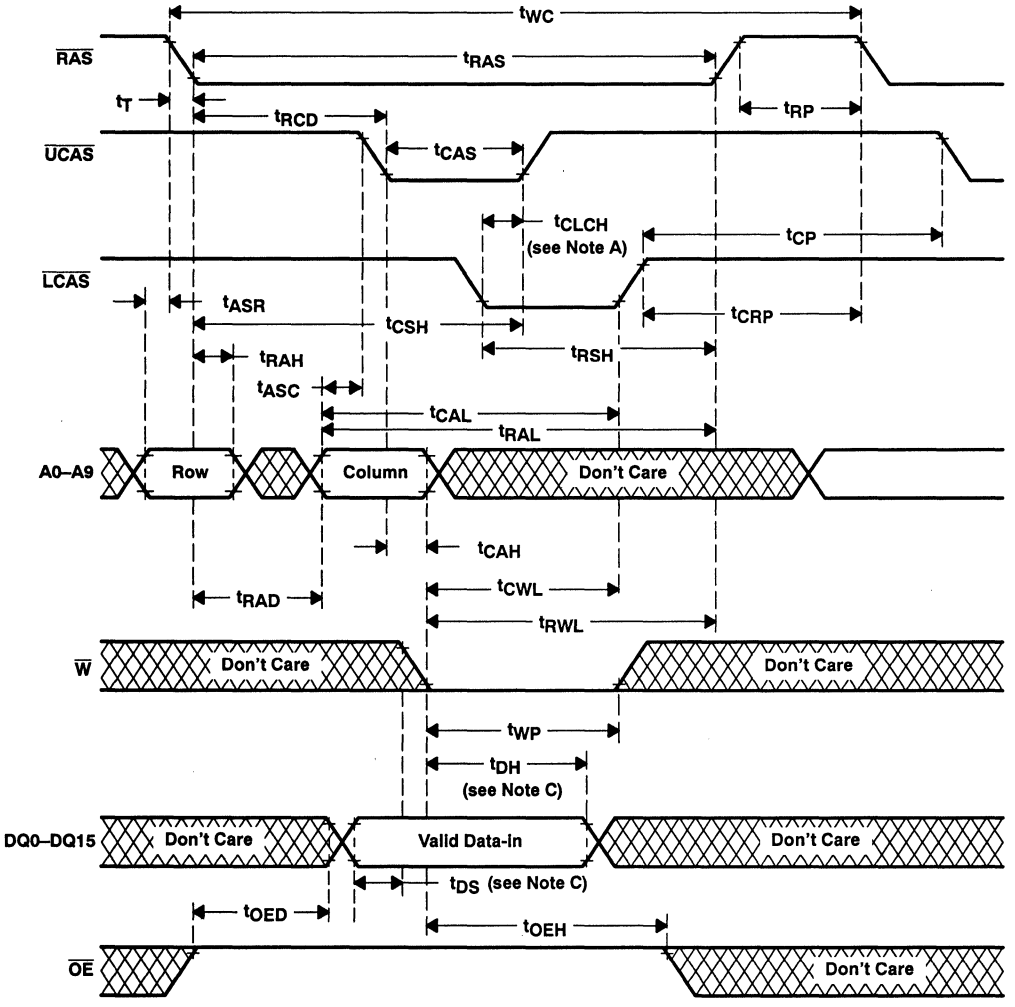
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

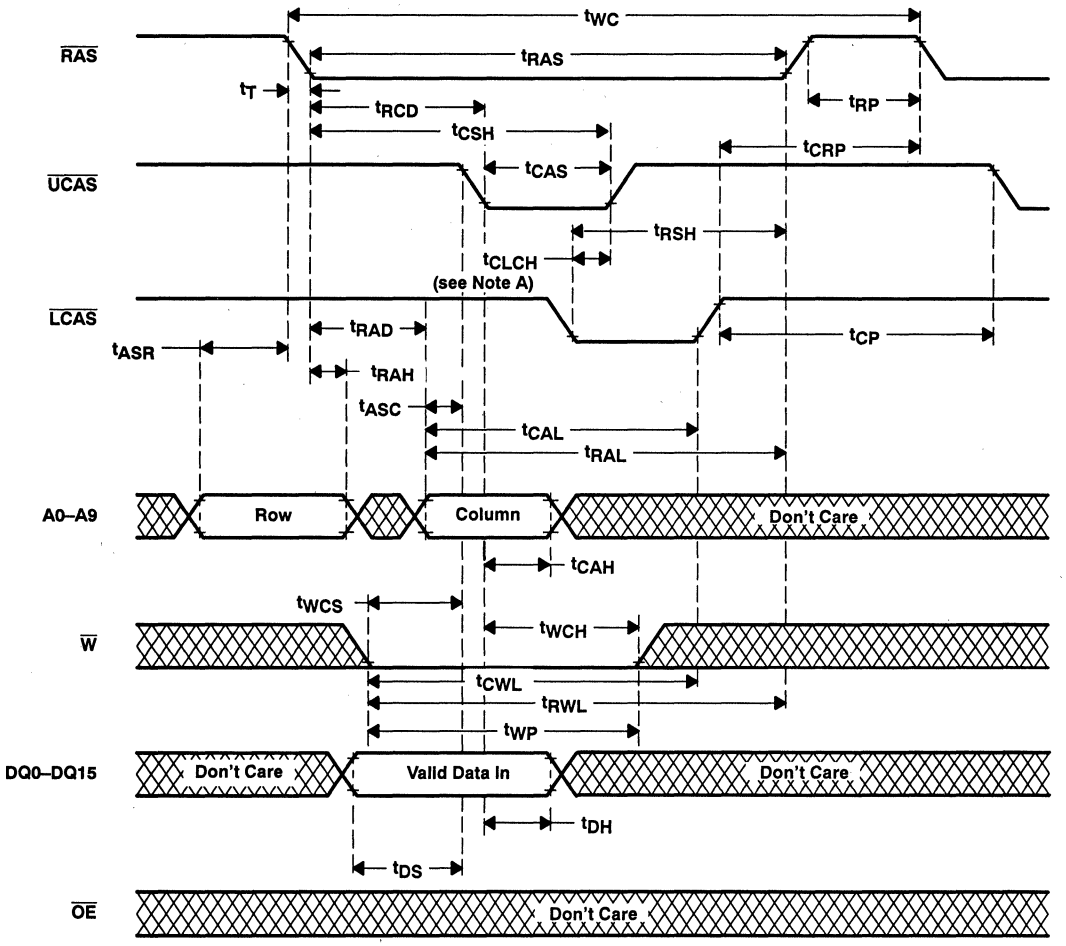


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 3. Write Cycle Timing

PRODUCT PREVIEW

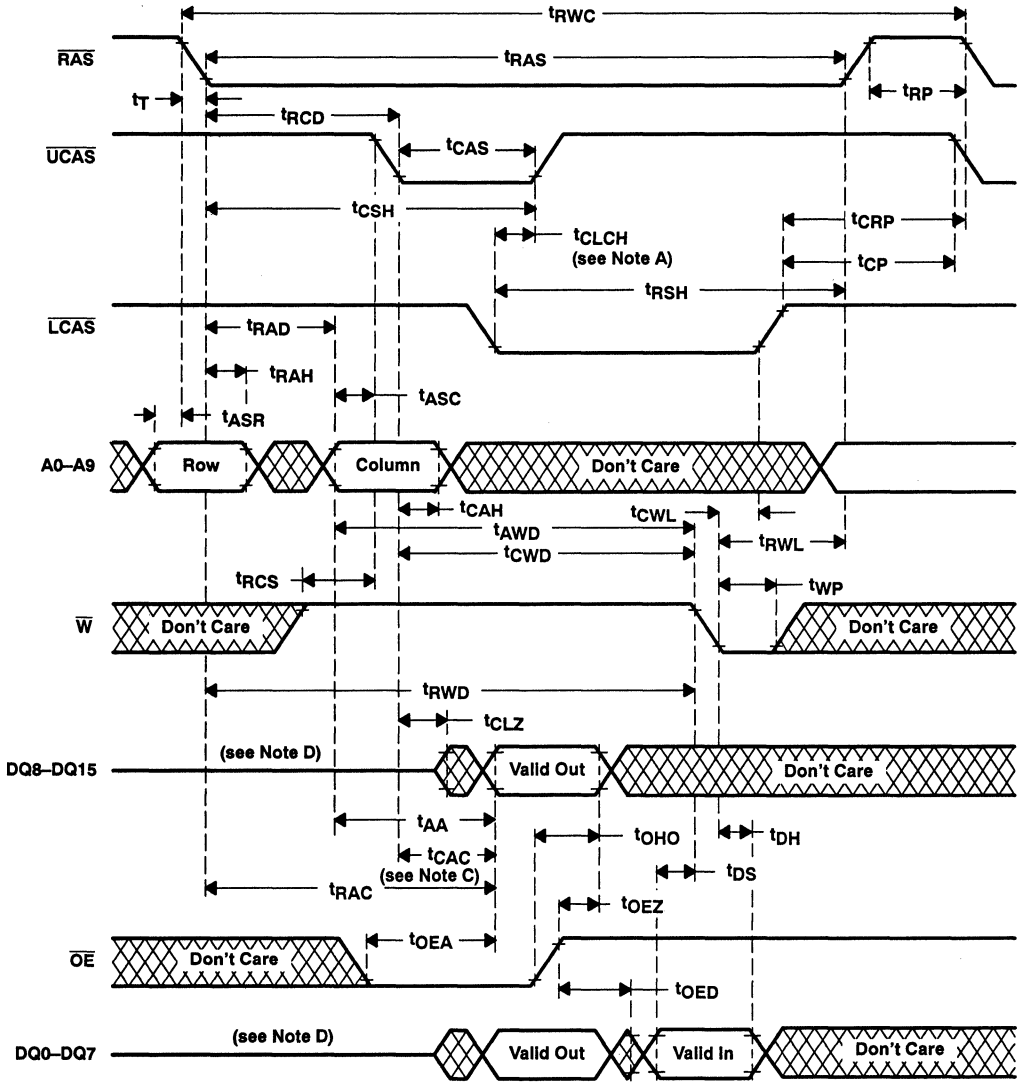
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

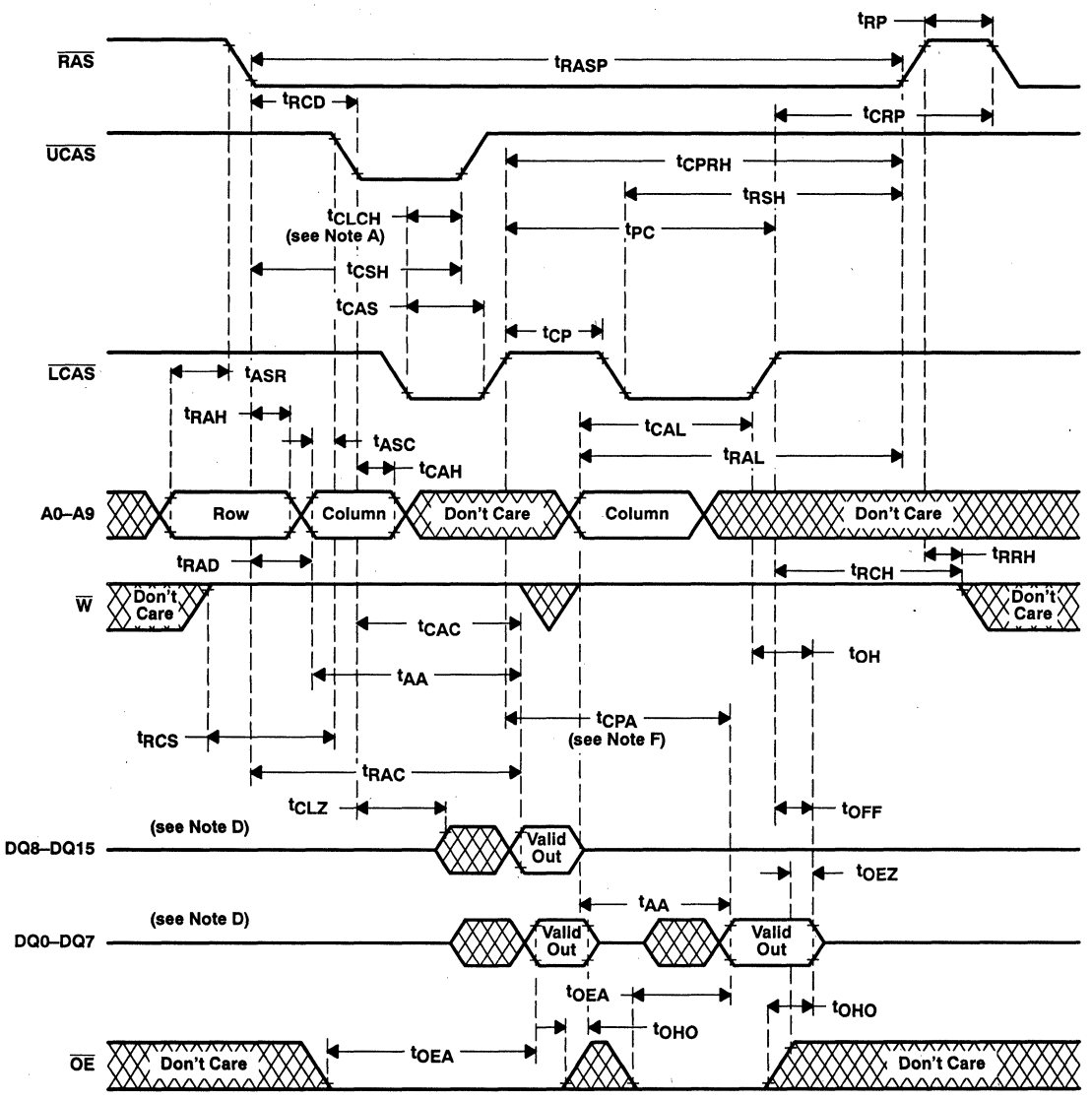


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. t_{CAC} in measured from $\overline{xCAS}$ to its corresponding DQx.
D. Output might go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

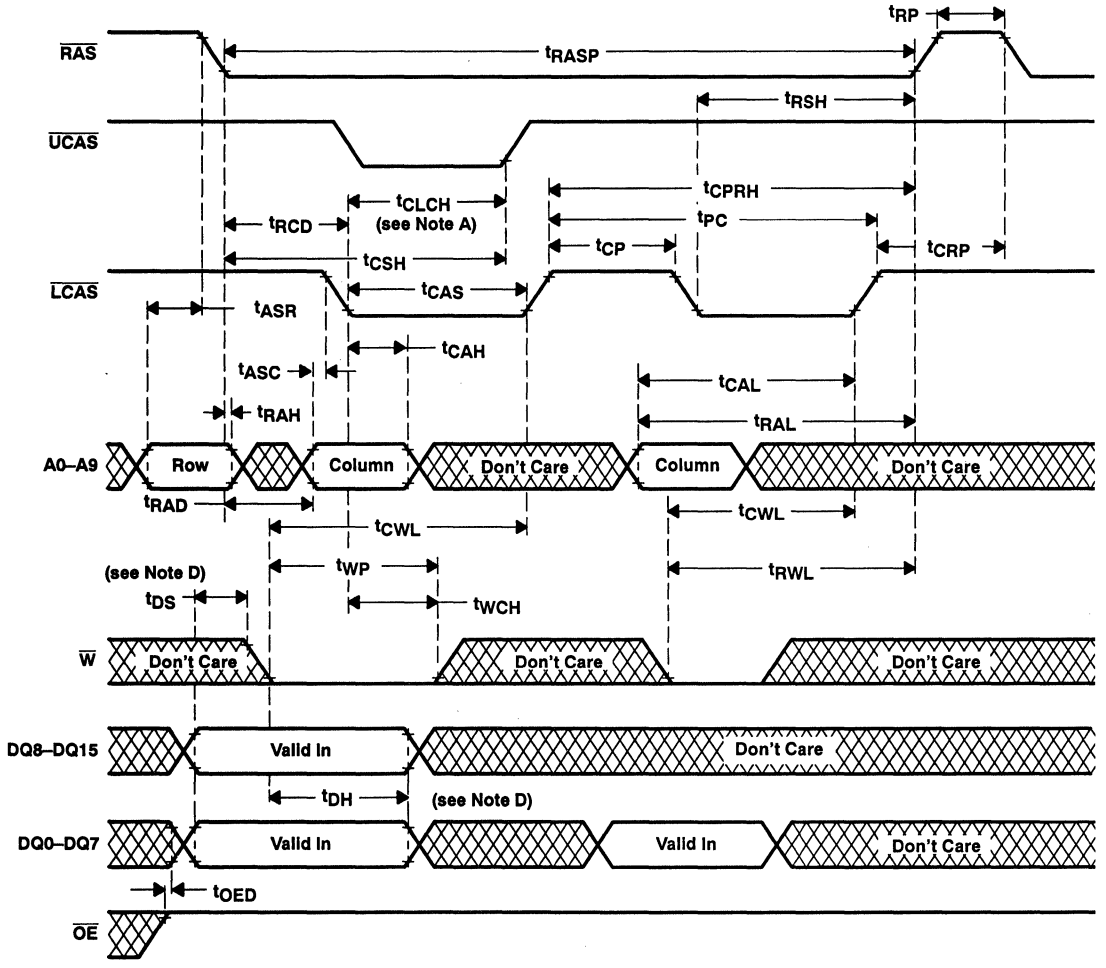
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

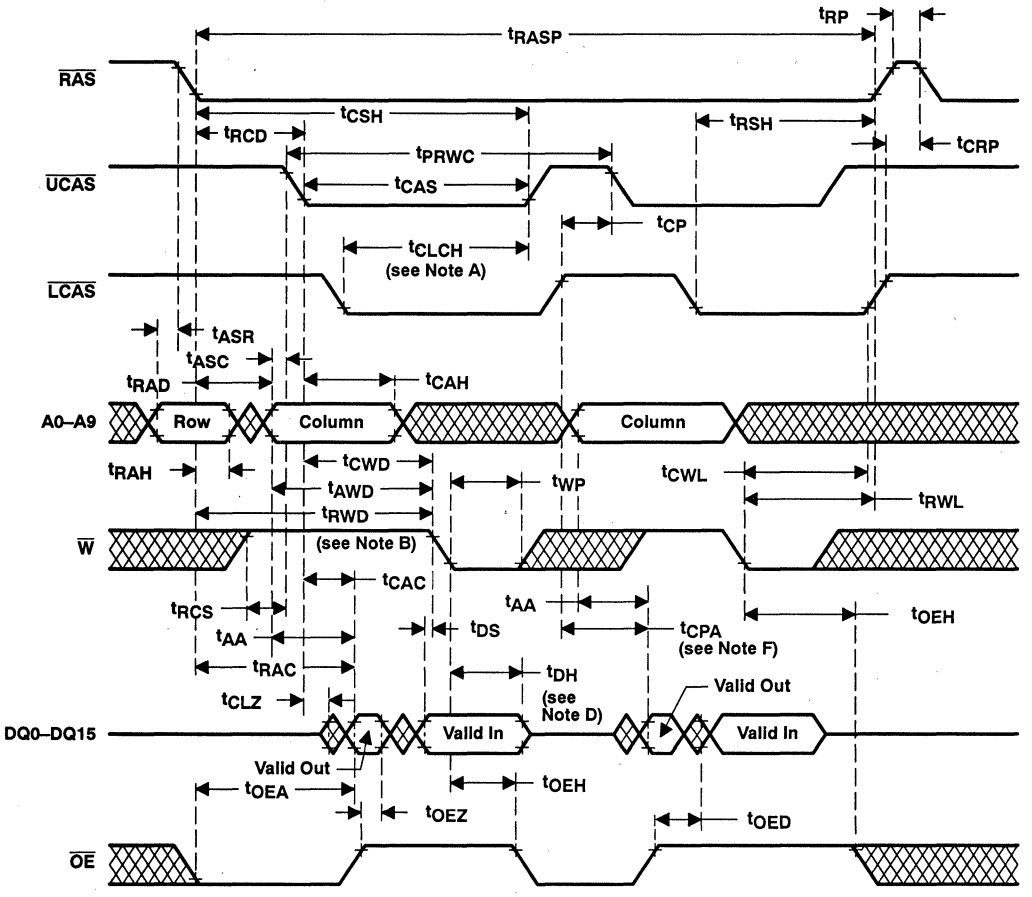


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
D. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

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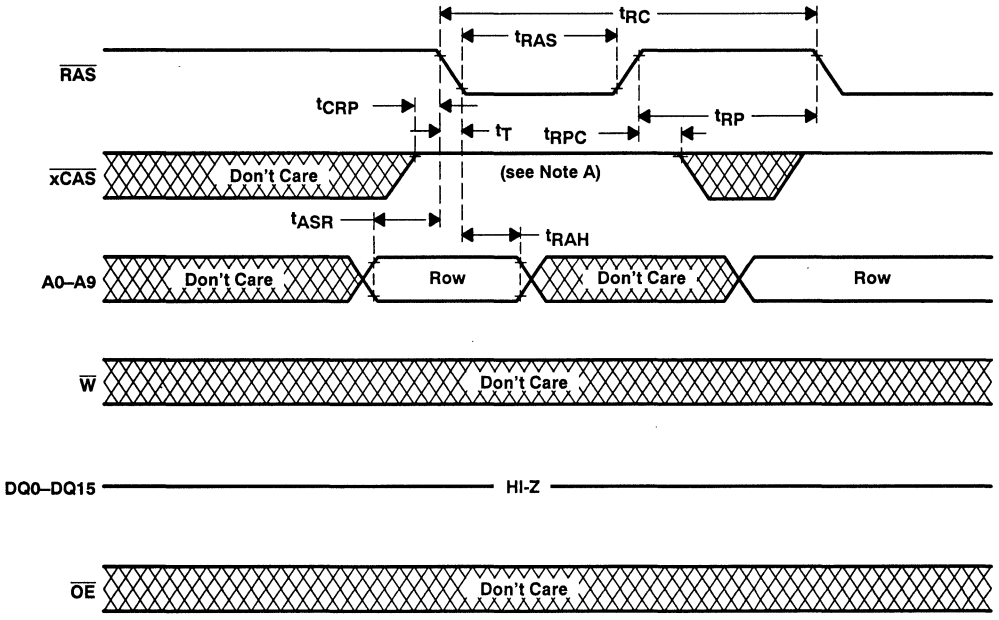
PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

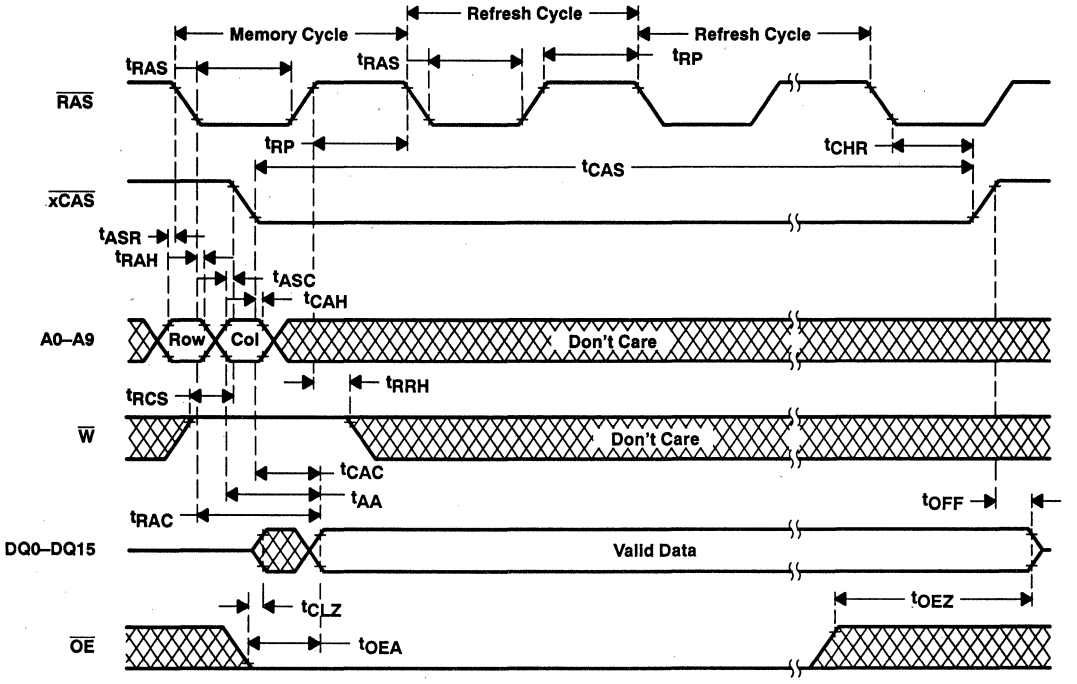


Figure 10. Hidden Refresh Cycle Timing

PRODUCT PREVIEW

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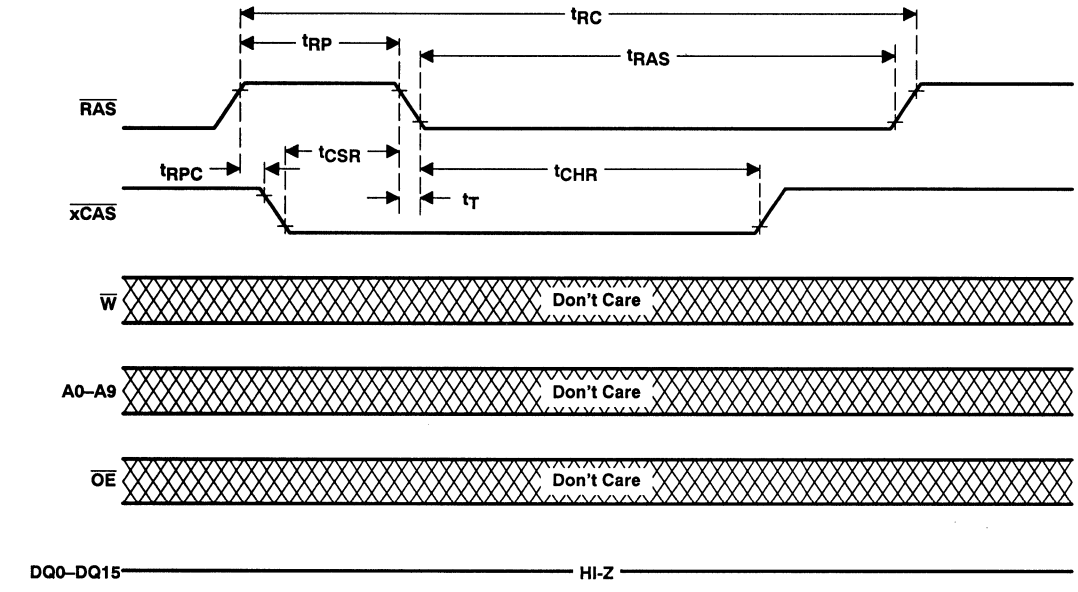
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Any xCAS may be used.

Figure 11. Automatic (CAS-Before-RAS) Refresh Cycle Timing

PRODUCT PREVIEW

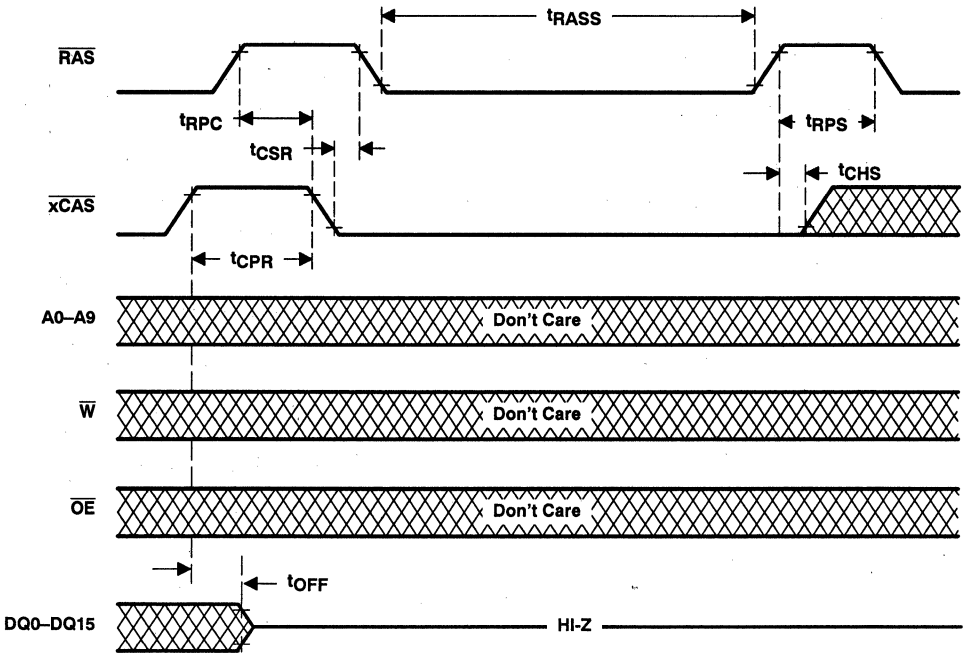
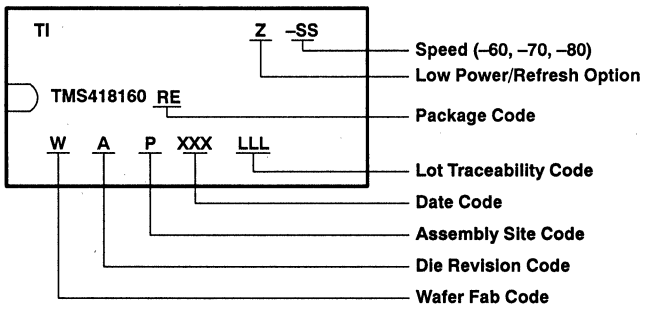


Figure 12. Self Refresh Timing

device symbolization

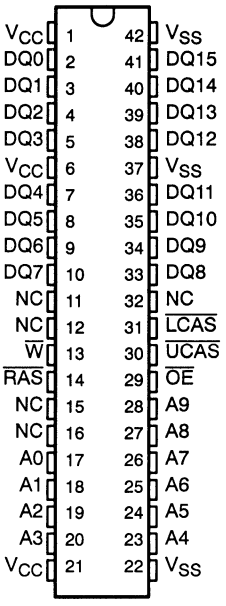


- **Organization . . . 1 048 576 × 16**
- **Single 3.3-V Supply (±0.3V Tolerance)**
- **Performance Ranges:**

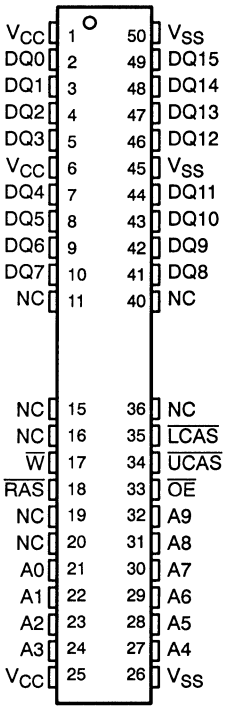
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'428160/P-70	70 ns	18 ns	35 ns	130 ns
'428160/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  1024-Cycle Refresh in 16 ms (Max)
  128 ms Max for Low-Power, Self-Refresh Version (TMS428160P)
- **3-State Unlatched Output**
- **Low Power Dissipation**
  - **100 μA CMOS Standby**
  - **100 μA Extended Refresh Battery Backup**
- **Self-Refresh With Low Power**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 44/50-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

RE PACKAGE† (TOP VIEW)



DC PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only

PIN NOMENCLATURE	
A0–A9	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{LCAS}$	Lower Column-Address Strobe
$\overline{UCAS}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS428160 series are high-speed, low voltage, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

The TMS428160P series are high-speed, low voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns and 80 ns. Maximum power dissipation is as low as 0.36 mW standby and battery backup on 80-ns devices.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS428160 and TMS428160P are each offered in a 42-lead plastic surface mount SOJ (RE suffix) package, and a 44/50-lead plastic surface mount TSOP (DC suffix). These packages are characterized for operation from 0°C to 70°C.

operation

dual $\overline{CAS}$

Two $\overline{CAS}$ pins ($\overline{LCAS}$–$\overline{UCAS}$) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with $\overline{LCAS}$ corresponding to DQ0–DQ7 and $\overline{UCAS}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{xCAS}$ falling edge. Each $\overline{xCAS}$ pin going low enables its corresponding DQ pin with data coming from the column address to be latched on the first falling $\overline{xCAS}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{xCAS}$ edge.The delay time from $\overline{xCAS}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{CAS}$ to its corresponding DQx pin.

In order to latch in a new column address, all $\overline{xCAS}$ pins must be brought high. The column precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first falling $\overline{xCAS}$ edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

For early write cycles, the data is latched on the first falling $\overline{xCAS}$ edge. Only the DQs that have the corresponding $\overline{xCAS}$ low will be written into. Each $\overline{xCAS}$ will have to meet t_{CAS} minimum in order to ensure writing into the storage cell. In order to latch a new address and new data, all $\overline{xCAS}$ pins need to come high and meet t_{CP}.

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{xCAS}$ page-mode cycle time used. With minimum $\overline{xCAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{xCAS}$ is high. The falling edge of the first $\overline{xCAS}$ latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, because data retrieval begins as soon as column address is valid rather than when $\overline{xCAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{xCAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{xCAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{xCAS}$ goes high, minimum access time for the next cycle is determined by t_{CPA} (access time from rising edge of the last $\overline{xCAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on pins A0 through A9 and latched onto the chip by $\overline{RAS}$. Then, ten column–address bits are set up on pins A0 through A9 and latched onto the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{xCAS}$ and the data is strobed in by the first occurring $\overline{xCAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{xCAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{xCAS}$ to be brought low for the output buffers to go into low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{xCAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every sixteen milliseconds (128 ms for TMS428160P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding all $\overline{xCAS}$ at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{xCAS}$-before-$\overline{RAS}$ refresh

$\overline{xCAS}$-before-$\overline{RAS}$ refresh is utilized by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{xCAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS428160P. Data integrity is maintained using $\overline{xCAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels (V_{IL} < 0.2 V, V_{IH} > V_{CC} – 0.2 V).

PRODUCT PREVIEW

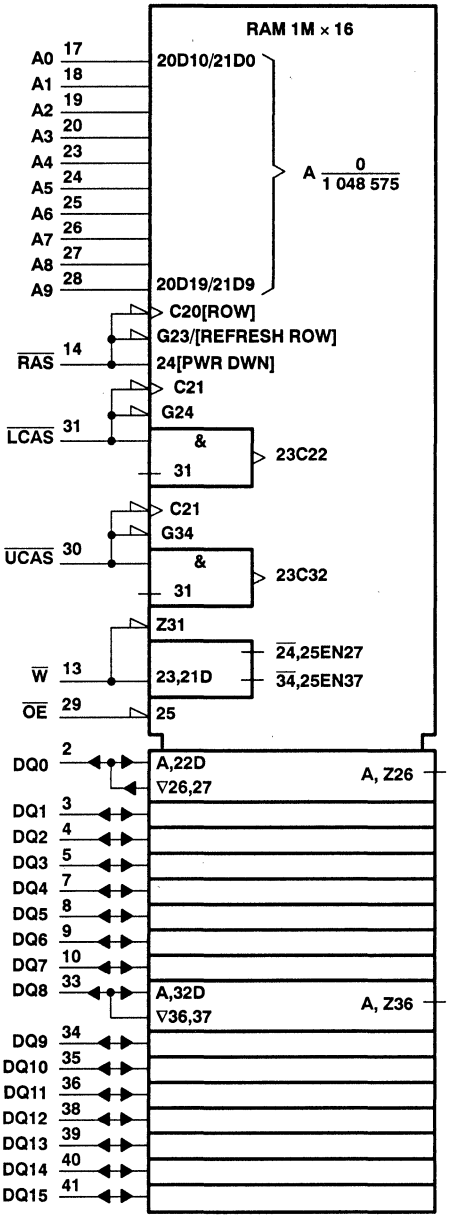
self refresh (TMS428160P)

The self-refresh mode is entered by dropping $\overline{\text{xCAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{xCAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power-up to the full V_{CC} level.

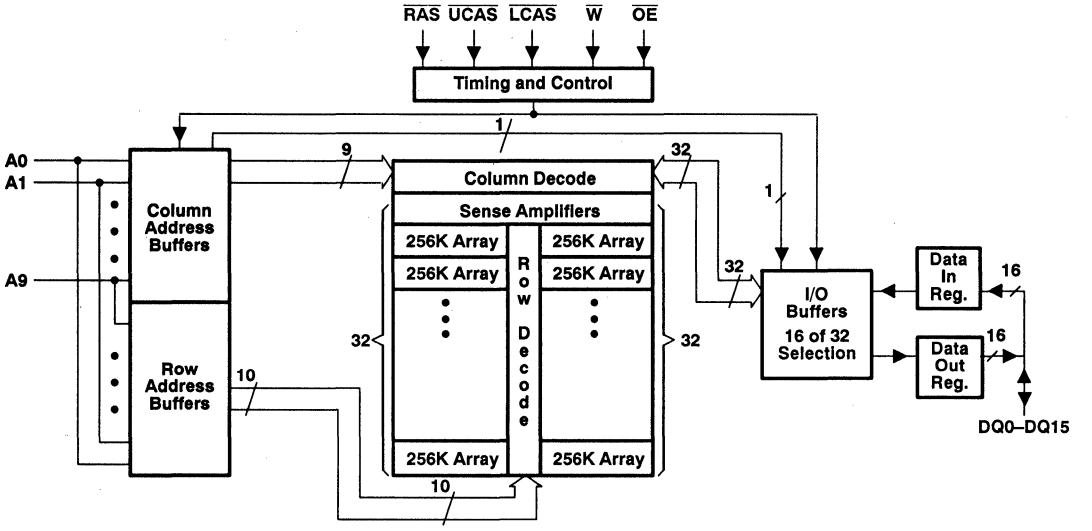
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the RE package.

PRODUCT PREVIEW

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 0.5 V to 4.6 V
Supply voltage range on V_{CC} ..... – 0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'428160-70 '428160P-70 MIN	'428160-70 '428160P-70 MAX	'428160-80 '428160P-80 MIN	'428160-80 '428160P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC} – 0.2		V_{CC} – 0.2		V
V_{OL}	Option	I_{OL} = 100 µA			0.2		0.2	V
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 to 3.9 V, All other pins = 0 V to V_{CC}			± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 to V_{CC}, $\overline{xCAS}$ high			± 10		± 10	µA
I_{CC1}†‡	Read or write cycle current	V_{CC} = 3.6 V, Minimum cycle			TBD		TBD	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high	'428160		300		300	µA
			'428160P		100		100	µA
I_{CC3}‡	Average refresh current ($\overline{RAS}$-only or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only) $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)			TBD		TBD	mA
I_{CC4}†§	Average page current	V_{CC} = 3.6 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			TBD		TBD	mA
I_{CC6}¶	Self refresh	$\overline{xCAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			100		100	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{xCAS}$ = V_{IL}, Data out = enabled			5		5	mA
I_{CC10}¶	Battery back-up operating current (equivalent refresh time is 128 ms). CBR only.	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100	µA

† Measured with outputs open.
‡ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
§ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}.
¶ For TMS428160P only.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 3: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'428160-70 '428160P-70		'428160-80 '428160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{xCAS}$ low		18		20	ns
t_{AA}	Access time from column address		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20	ns
t_{CPA}	Access time from column precharge		40		45	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ low to output in low Z	0		0		ns
t_{OH}	Output data hold time (from $\overline{xCAS}$)	3		3		ns
t_{OHO}	Output data hold time (from $\overline{OE}$)	3		3		ns
t_{OFF}	Output disable time after $\overline{xCAS}$ high (see Note 4)	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 4)	0	18	0	20	ns

NOTE 4: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'428160-70 '428160P-70		'428160-80 '428160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time (see Note 6)	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{RWC}	Read-write/read-modify-write cycle time	181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 8)	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ low (see Note 9)	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{xCAS}$ high (precharge)	10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		ns
t_{WP}	Write pulse duration	15		15		ns
t_{ASC}	Column-address setup time before $\overline{xCAS}$ low	0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		ns
t_{DS}	Data setup time before $\overline{W}$ low (see Note 10)	0		0		ns
t_{RCS}	Read setup time before $\overline{xCAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{xCAS}$ high	18		20		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_T = 5 ns.
7. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
8. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
9. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{xCAS}$ low time (t_{CAS}).
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

		'428160-70 '428160P-70		'428160-80 '428160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{xCAS}$ low (see Note 12)	0		0		ns
t_{CAH}	Column-address hold time after $\overline{xCAS}$ low	15		15		ns
t_{DH}	Data hold time after $\overline{xCAS}$ low (see Note 10)	15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		ns
t_{RCH}	Read hold time after $\overline{xCAS}$ high (see Note 13)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		ns
t_{WCH}	Write hold time after $\overline{xCAS}$ low (see Note 12)	15		15		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (see Note 14)	63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high (see Note 11)	20		20		ns
t_{CRP}	Delay time, $\overline{xCAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ high	70		80		ns
t_{CSR}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		ns
t_{CWD}	Delay time, $\overline{xCAS}$ low to $\overline{W}$ low (see Note 14)	46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	18		20		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	18		20		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ high	35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{xCAS}$ low (see Note 15)	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{xCAS}$ low	0		0		ns
t_{RSH}	Delay time, $\overline{xCAS}$ low to $\overline{RAS}$ high	18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 14)	98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{xCAS}$ precharge	68		75		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{xCAS}$ precharge	40		45		ns
t_{CPR}	$\overline{xCAS}$ precharge before self refresh	0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		ns

NOTES: 5. Timing measurements are referenced to V_{IL} max and V_{IH} min.
10. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.
11. $\overline{xCAS}$-before-$\overline{RAS}$ refresh only.
12. Early write operation only.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. Read-modify-write operation only.
15. Maximum value specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

		'428160-70 '428160P-70		'428160-80 '428160P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		µs
t_{CHS}	$\overline{xCAS}$ low hold time after $\overline{RAS}$ high (self refresh)	−50		−50		ns
t_{REF}	Refresh time interval (TMS428160 only)		16		16	ms
t_{REF}	Refresh time interval, low power (TMS428160P only)		128		128	ms
t_T	Transition time	3	30	3	30	ns

NOTE 5: Timing measurements are referenced to V_{IL} max and V_{IH} min.

PARAMETER MEASUREMENT INFORMATION

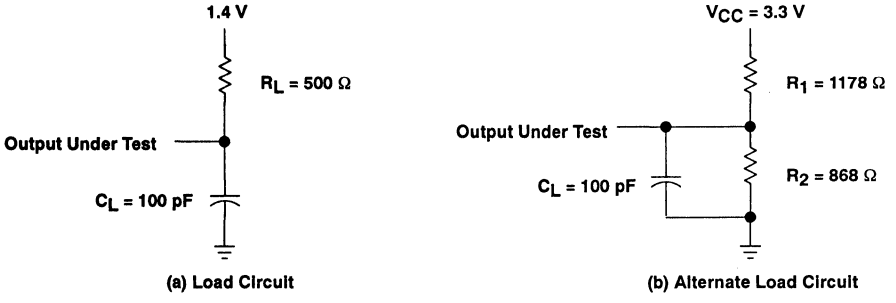
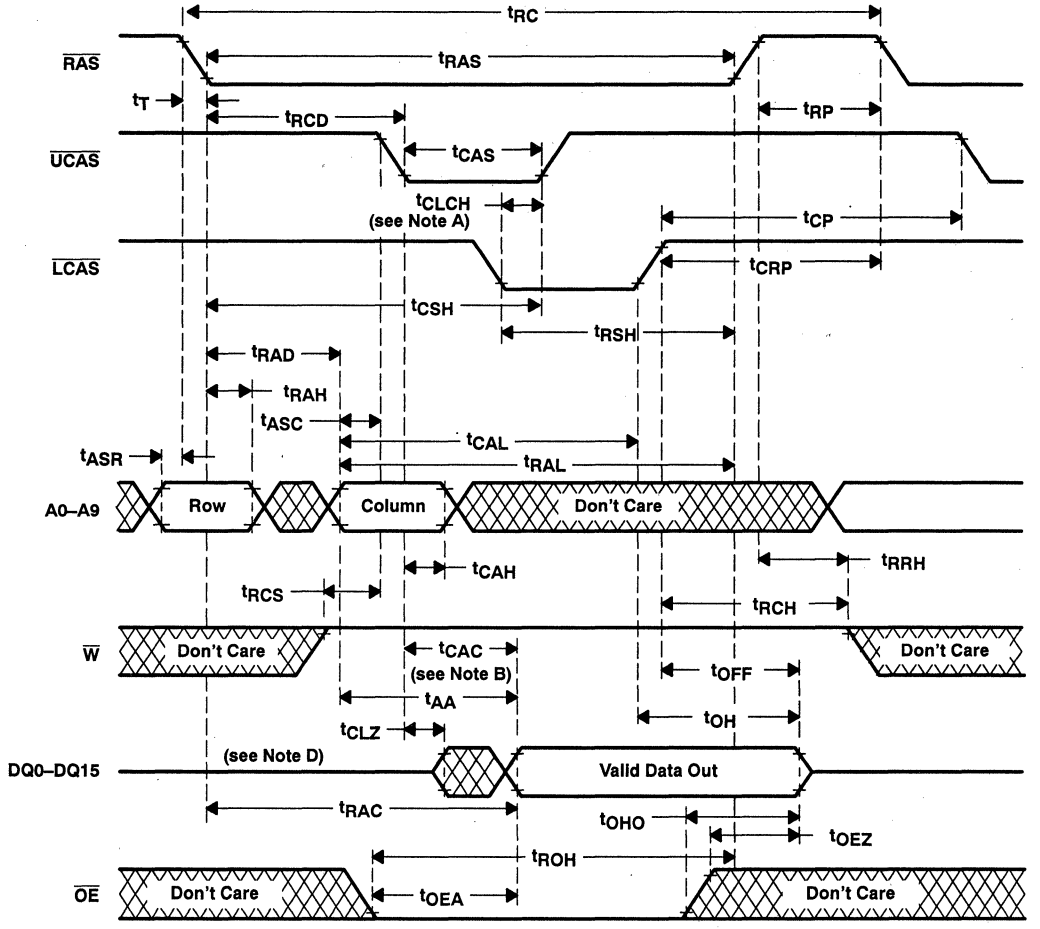


Figure 1. Load Circuits for Timing Parameters

PRODUCT PREVIEW

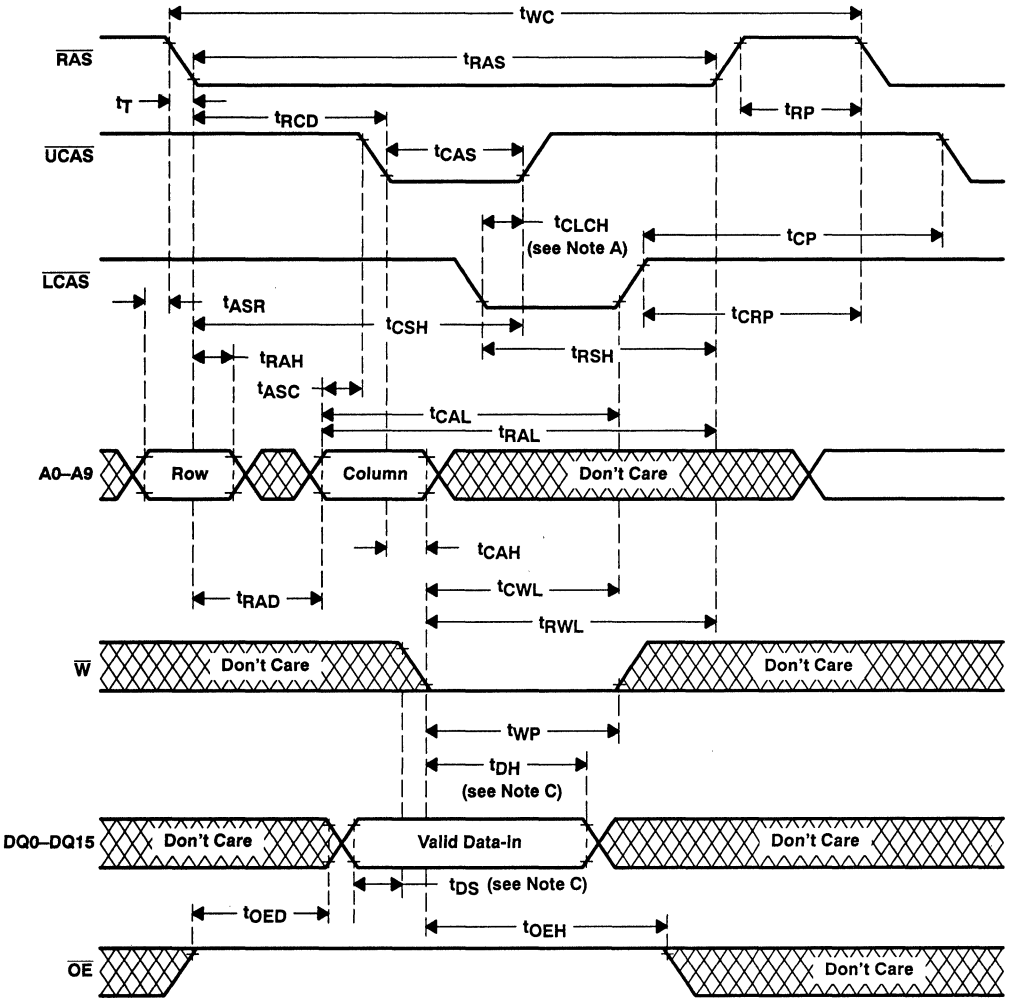
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

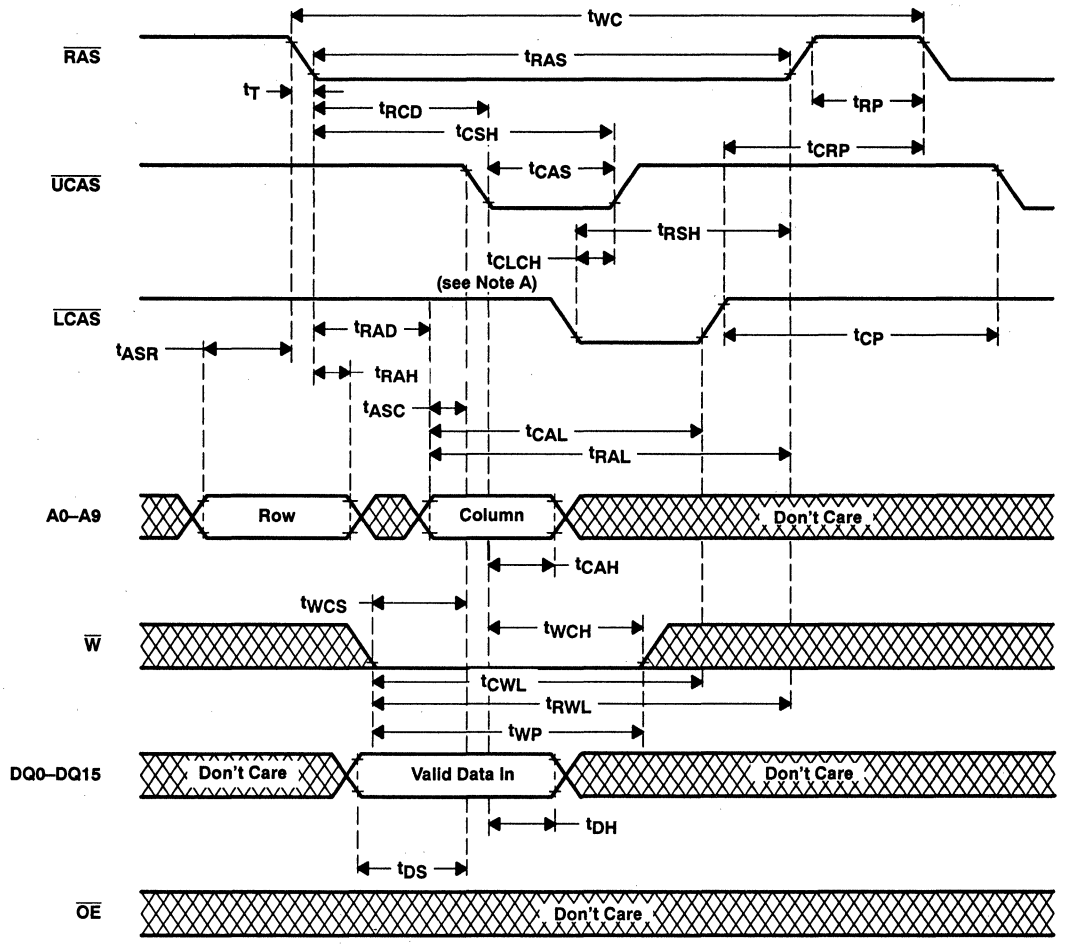


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. Reference to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 3. Write Cycle Timing

PRODUCT PREVIEW

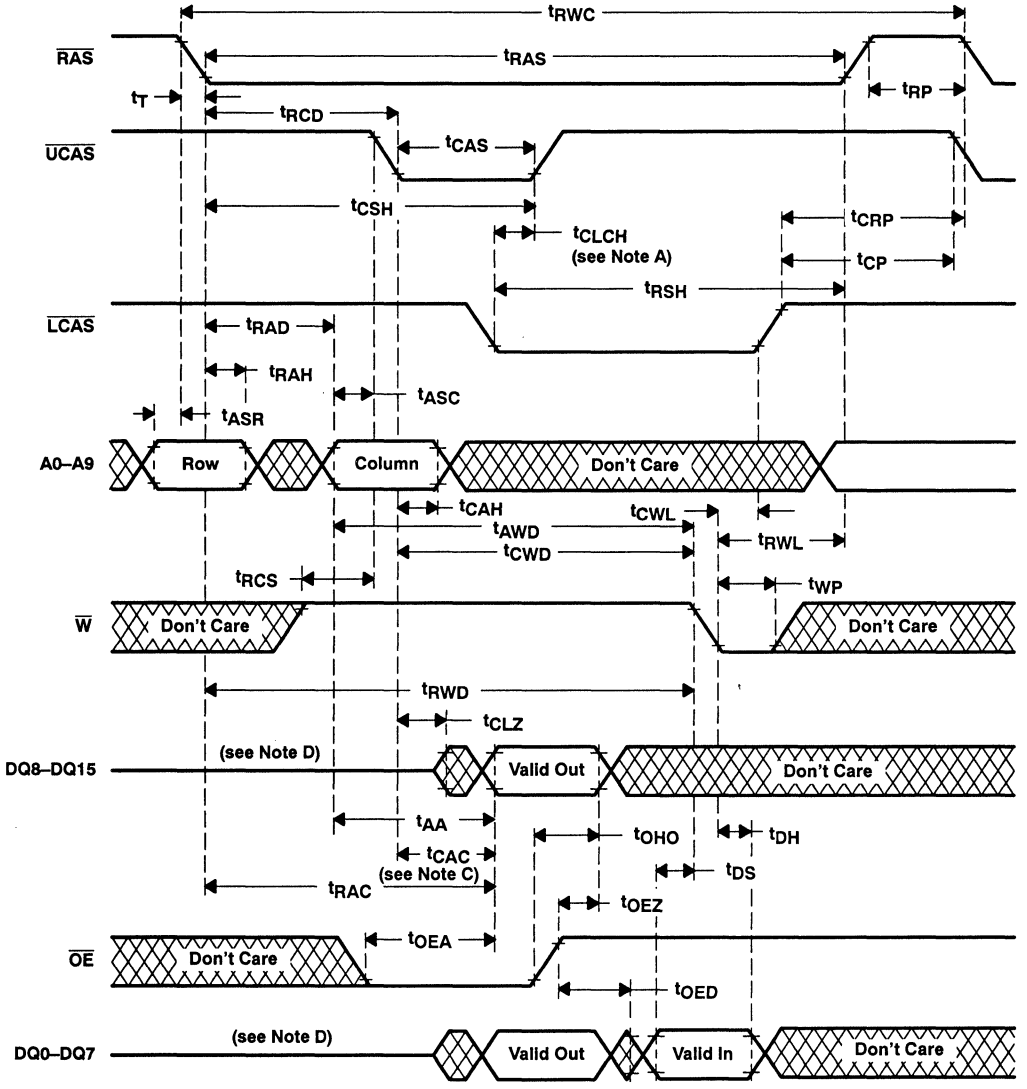
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.

Figure 4. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

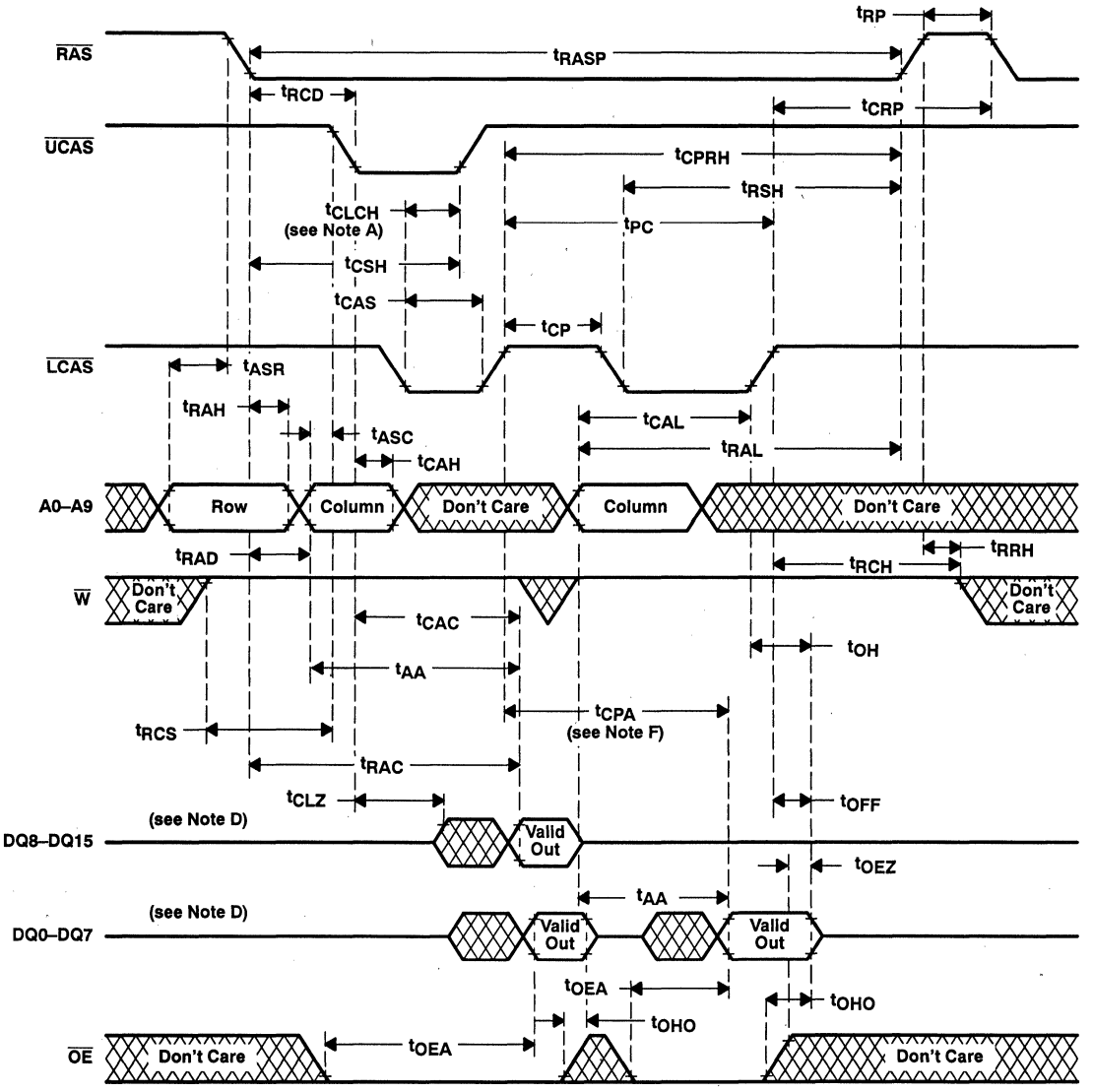


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. t_{CAC} in measured from $\overline{xCAS}$ to its corresponding DQx.
D. Output might go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

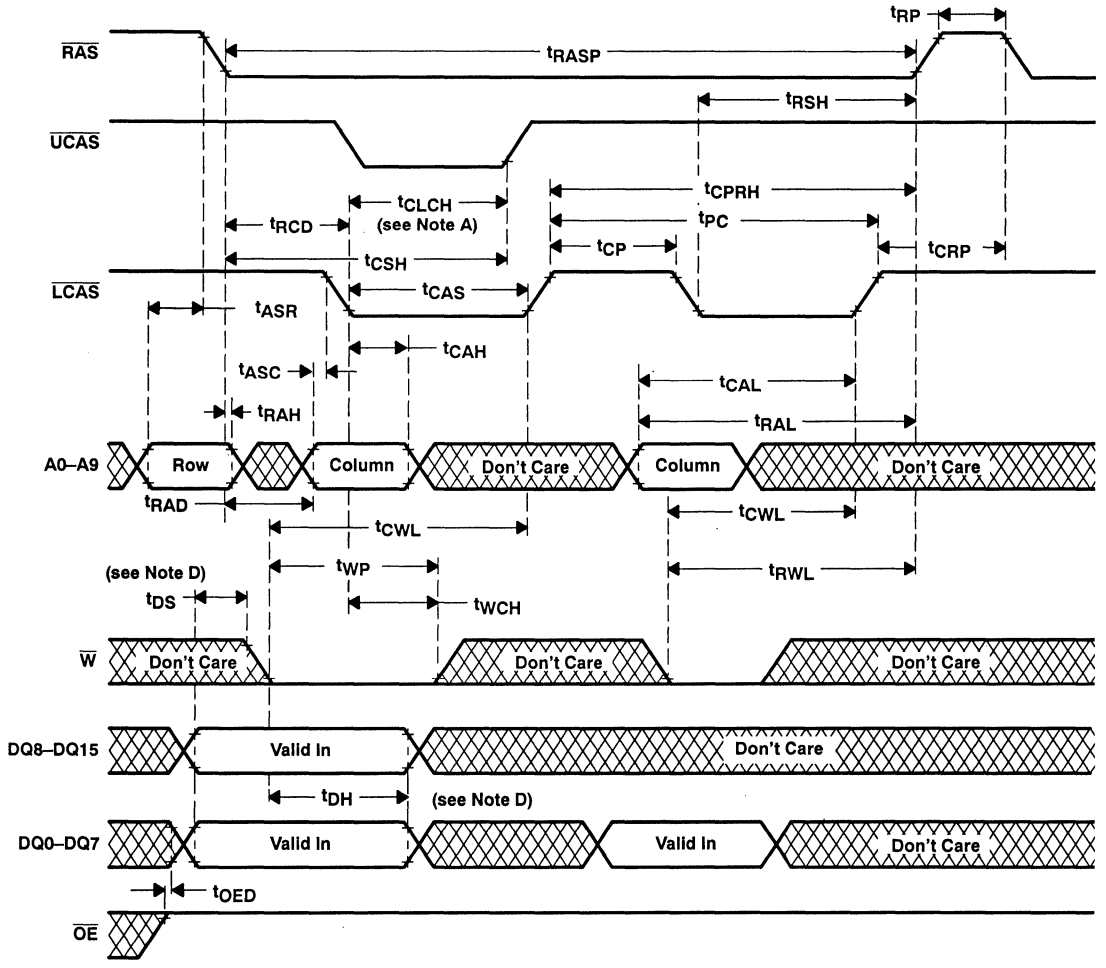
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

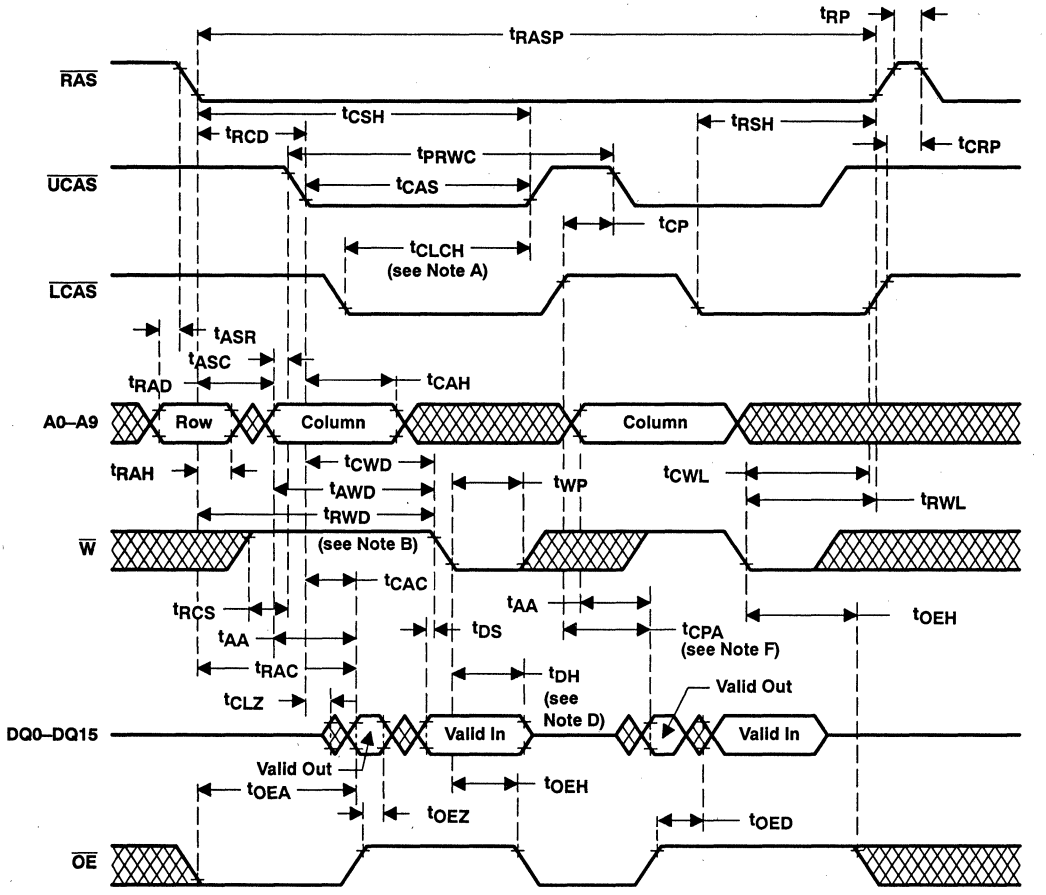


NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{xCAS}$ order is arbitrary.
C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
D. Referenced to the first $\overline{xCAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

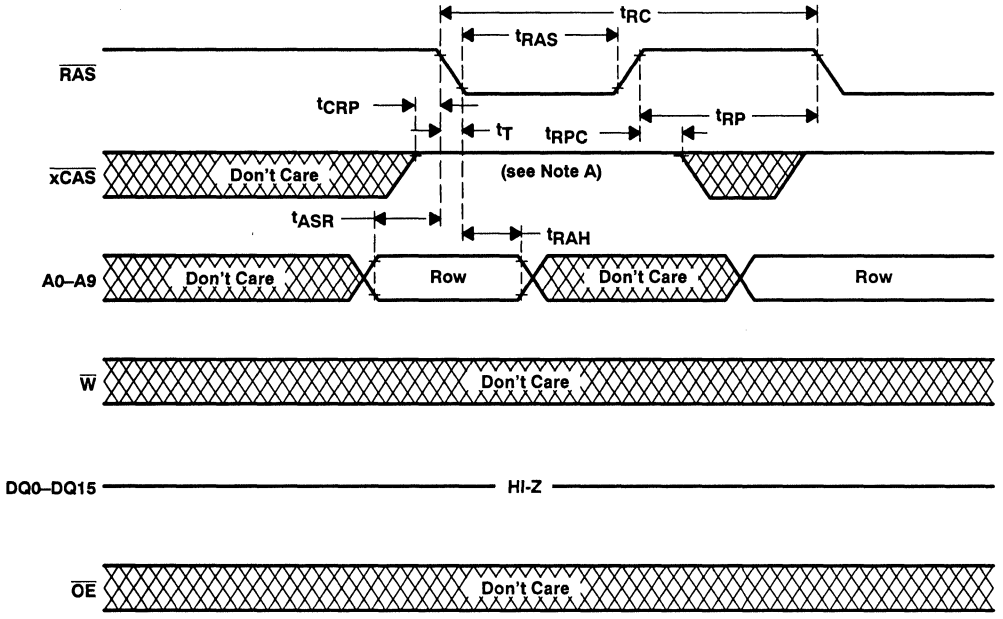
PARAMETER MEASUREMENT INFORMATION



NOTES: A. In order to hold the address latched by the first $\overline{xCAS}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{xCAS}$ to its corresponding DQx.
C. $\overline{xCAS}$ order is arbitrary.
D. Output may go from high-impedance to an invalid data state prior to the specified access time.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
F. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: All $\overline{xCAS}$ must be high.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

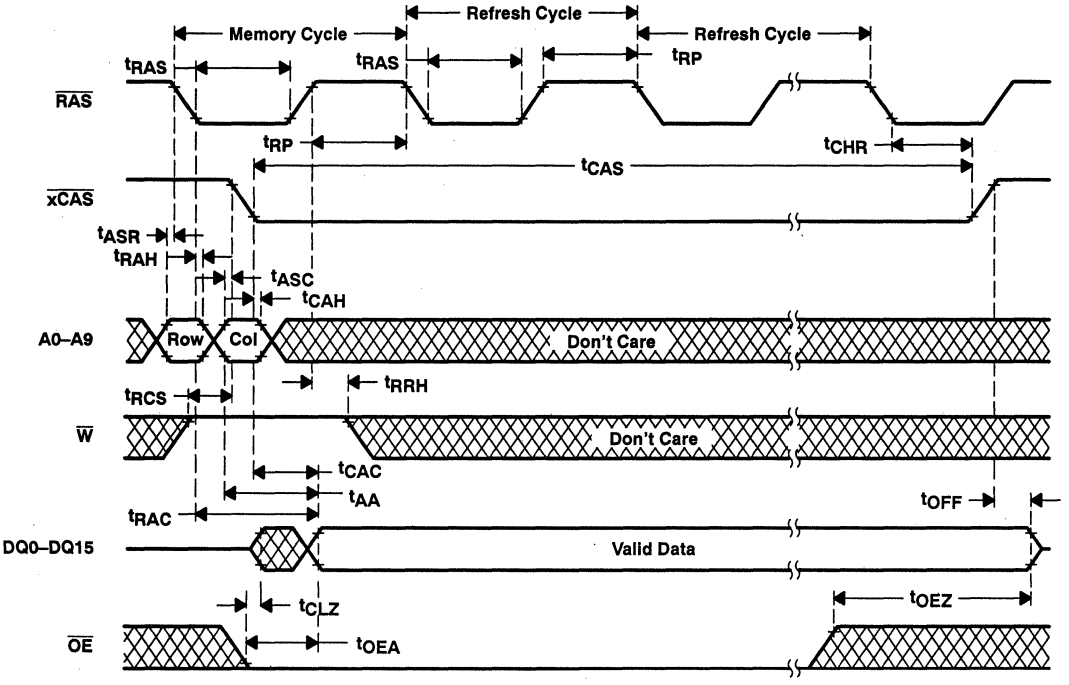
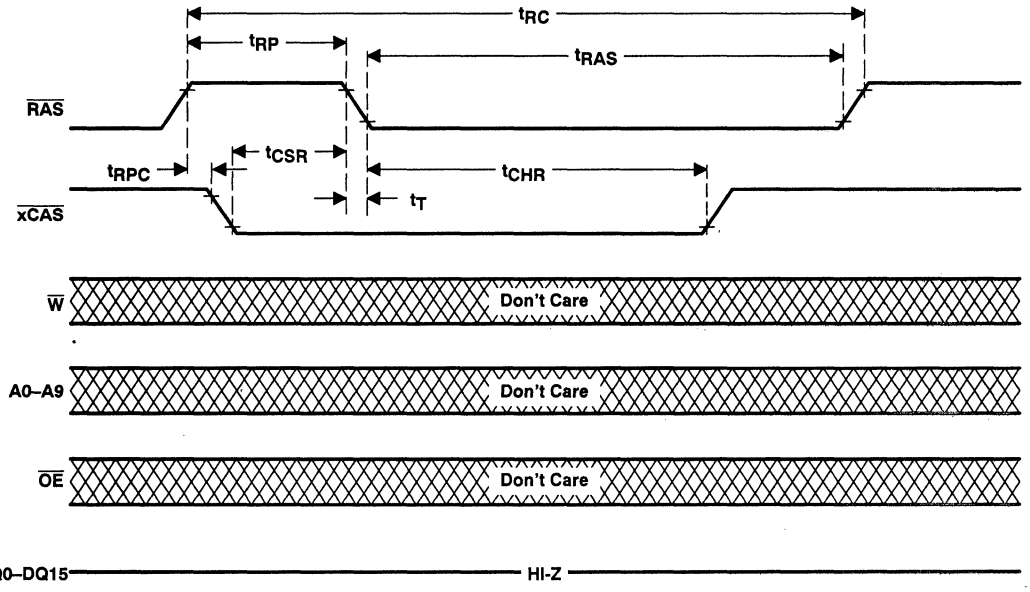


Figure 10. Hidden Refresh Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Any xCAS may be used.

Figure 11. Automatic (CAS-Before-RAS) Refresh Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

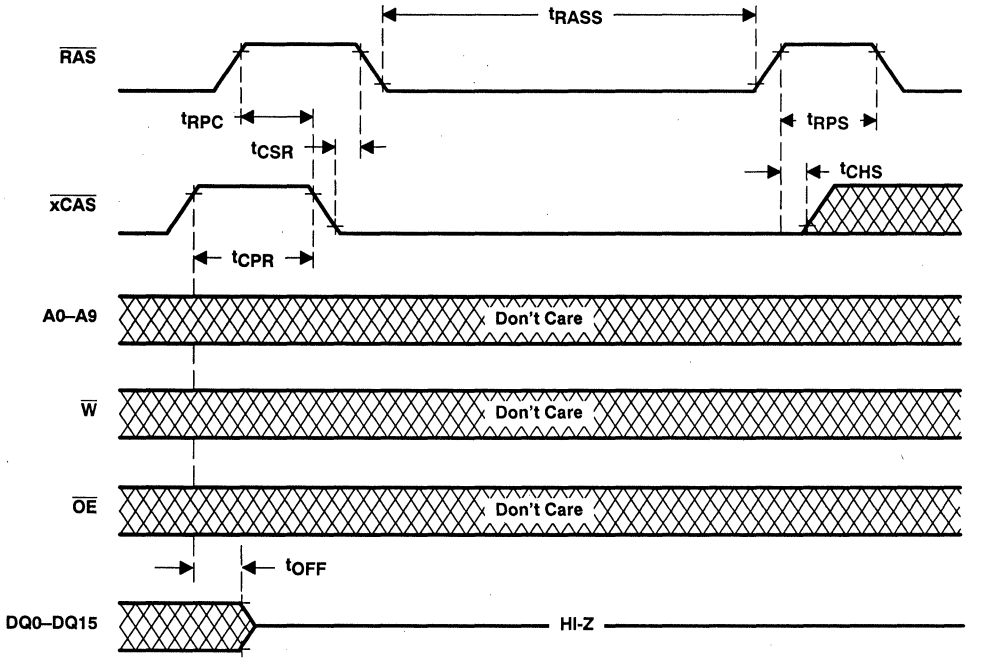
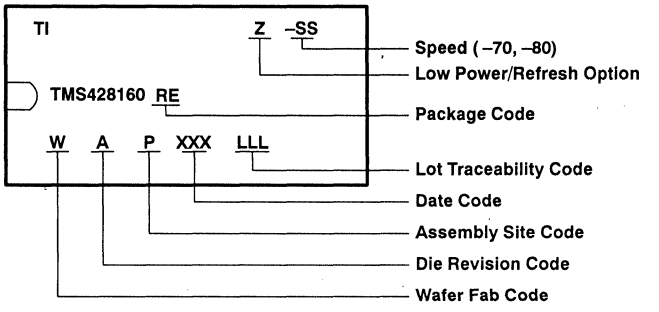


Figure 12. Self Refresh Timing

device symbolization



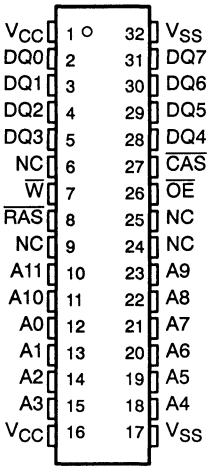
PRODUCT PREVIEW

- **Organization . . . 2 097 152 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

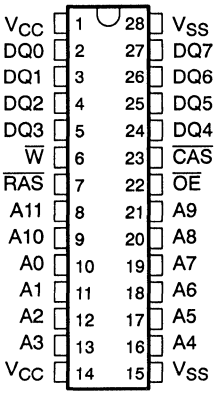
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'416800/P-60	60 ns	15 ns	30 ns	110 ns
'416800/P-70	70 ns	18 ns	35 ns	130 ns
'416800/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **4096-Cycle Refresh in 64 ms (Max)**
  - **512 ms for Low Power, Self-Refresh Version (TMS416800P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Self-Refresh With Low-Power**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 28-Pin, J-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 32-Pin, Plastic Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

DE PACKAGE†
(TOP VIEW)



DZ PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write-Enable
V_{CC}	5-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS416800 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

The TMS416800P series are high-speed, low-power, self-refresh, 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 385 mW operating and 11 mW standby for 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416800 and TMS416800P series are offered in a 400-mil 28-lead plastic surface mount SOJ package (DZ suffix) and a 32-lead plastic surface mount TSOP package (DE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS416800 and TMS416800P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A11)

Twenty-one address bits are required to decode 1 of 2 097 152 storage cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ0–DQ7)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 64 milliseconds (512 ms for TMS416800P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS416800P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh (TMS416800P)

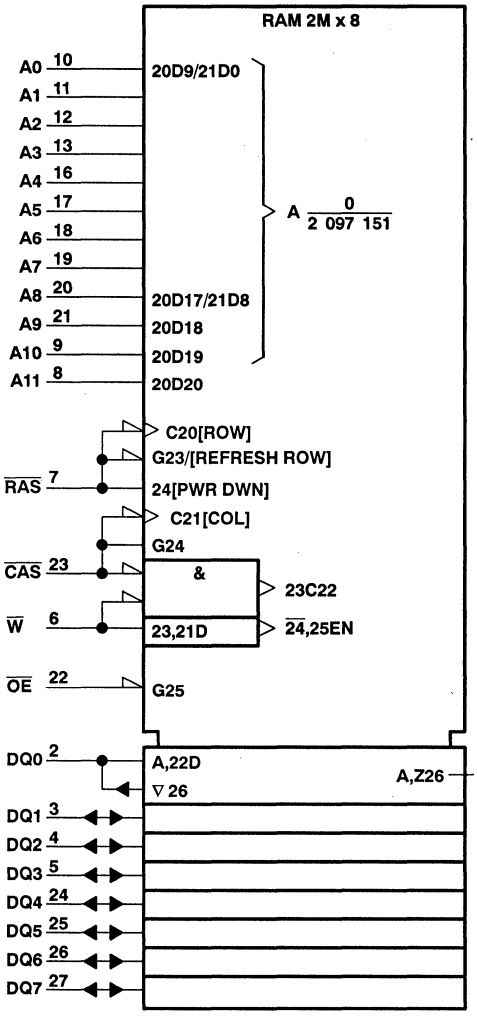
The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

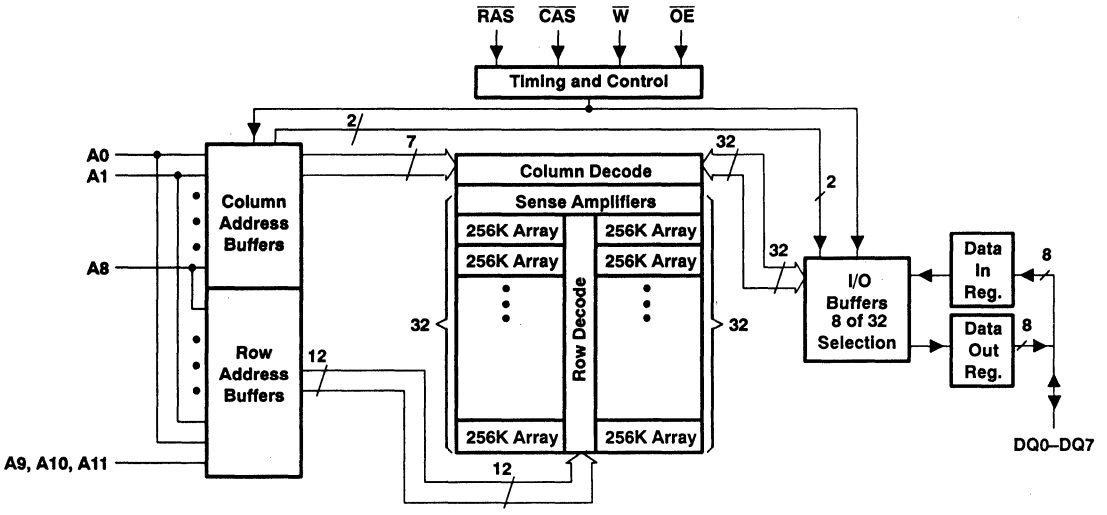
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS416800-60 TMS416800P-60		TMS416800-70 TMS416800P-70		TMS416800-80 TMS416800P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			90		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		$V_{IH} = V_{CC} - 0.2$ V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'416800		1		1		1	mA
			'416800P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			90		80		70	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			90		80		70	mA
I_{CC10}‡	Battery backup operating current (equivalent refresh time is 512 ms) CBR only	t_{RC} = 125 µs, $t_{RAS} \le 1$ µs, $V_{CC} - 0.2\ V \le V_{IH} \le 6.5$ V, $0\ V \le V_{IL} \le 0.2$ V, $\overline{W}$ and $\overline{OE} = V_{IH}$, Address and Data stable			500		500		500	µA
I_{CC6}‡	Self refresh current	$\overline{CAS} \le 0.2$ V, $\overline{RAS} < 0.2$ V, Measured after t_{RASS} minimum			500		500		500	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$ Data out = Enabled			5		5		5	mA

† Measured with outputs open.
‡ For TMS416800P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$.
4. Measured with a maximum of one address change while $\overline{CAS} = V_{IH}$.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416800-60 TMS416800P-60		TMS416800-70 TMS416800P-70		TMS416800-80 TMS416800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns
t_{OHO}	Output disable time, start of $\overline{OE}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS416800-60 TMS416800P-60		TMS416800-70 TMS416800P-70		TMS416800-80 TMS416800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-modify-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high ($\overline{CAS}$ precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high ($\overline{RAS}$ precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		TMS416800-60 TMS416800P-60		TMS416800-70 TMS416800P-70		TMS416800-80 TMS416800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-modify-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	35		40		45		ns

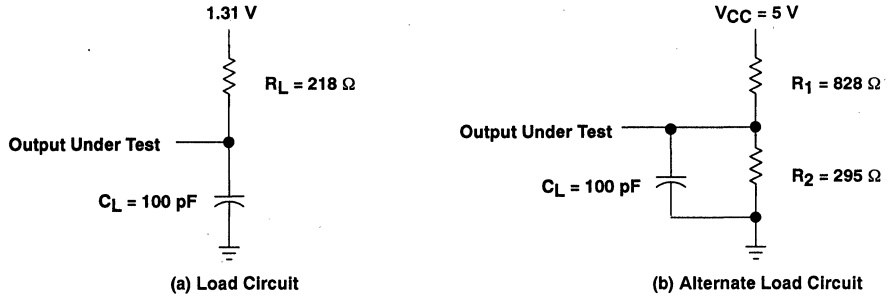
NOTES: 11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or T_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		TMS416800-60 TMS416800P-60		TMS416800-70 TMS416800P-70		TMS416800-80 TMS416800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	110		130		150		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	– 50		– 50		– 50		ns
t_{REF}	Refresh time interval (TMS416800 only)		64		64		64	ms
t_{REF}	Refresh time interval Low power (TMS416800P only)		512		512		512	ms
t_T	Transition time	3	30	3	30	3	30	ns

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

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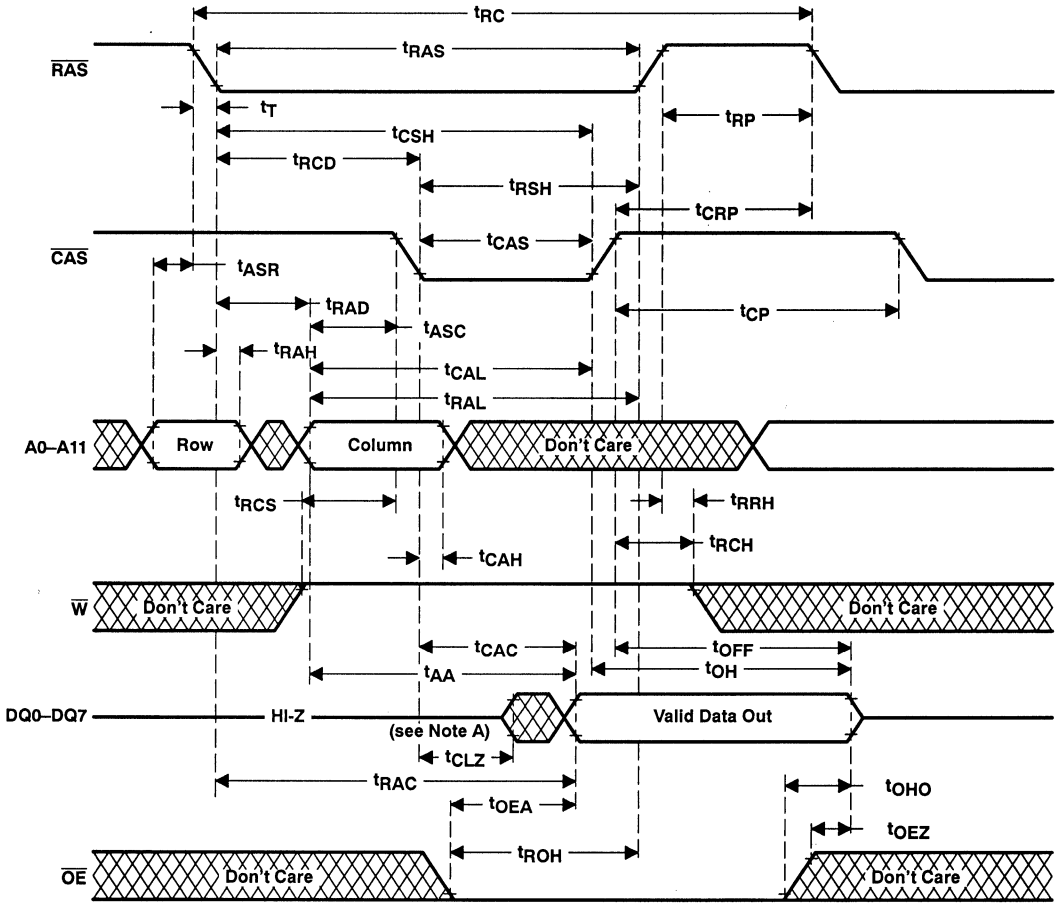
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

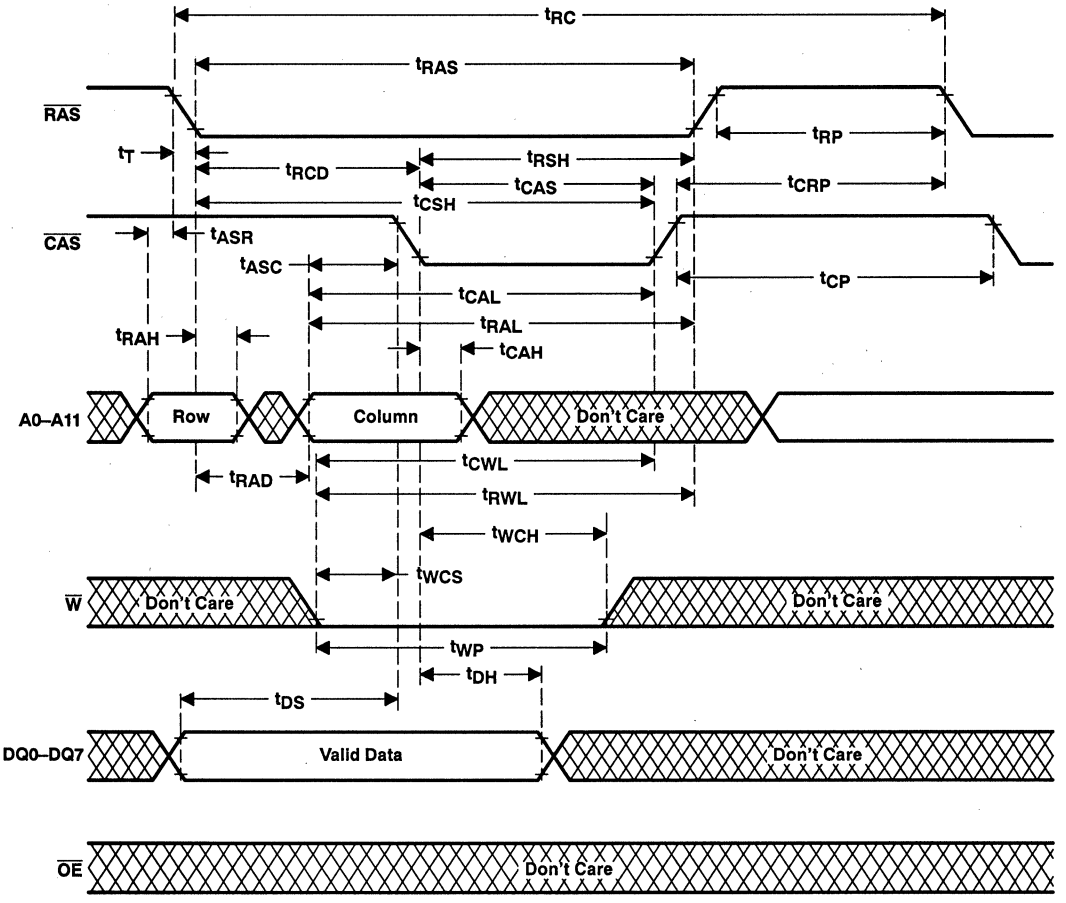
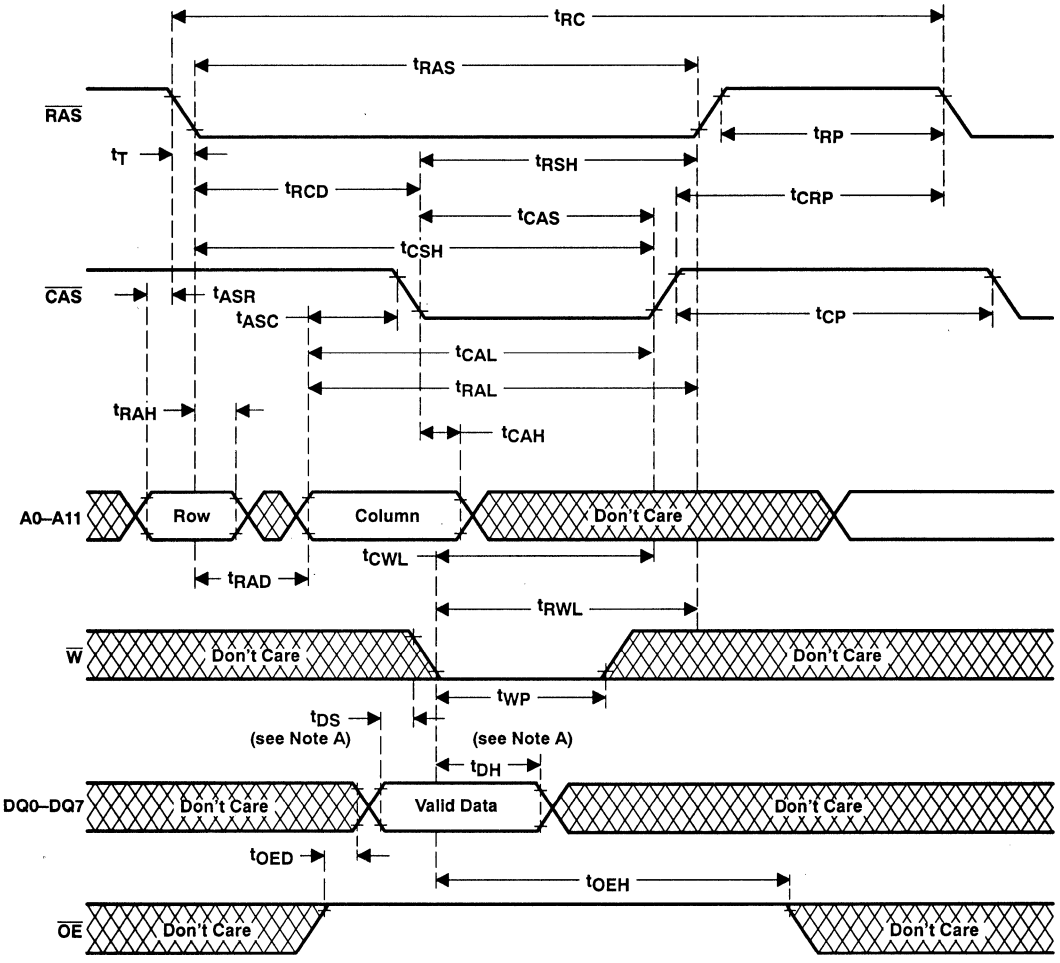


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 4. Write Cycle Timing

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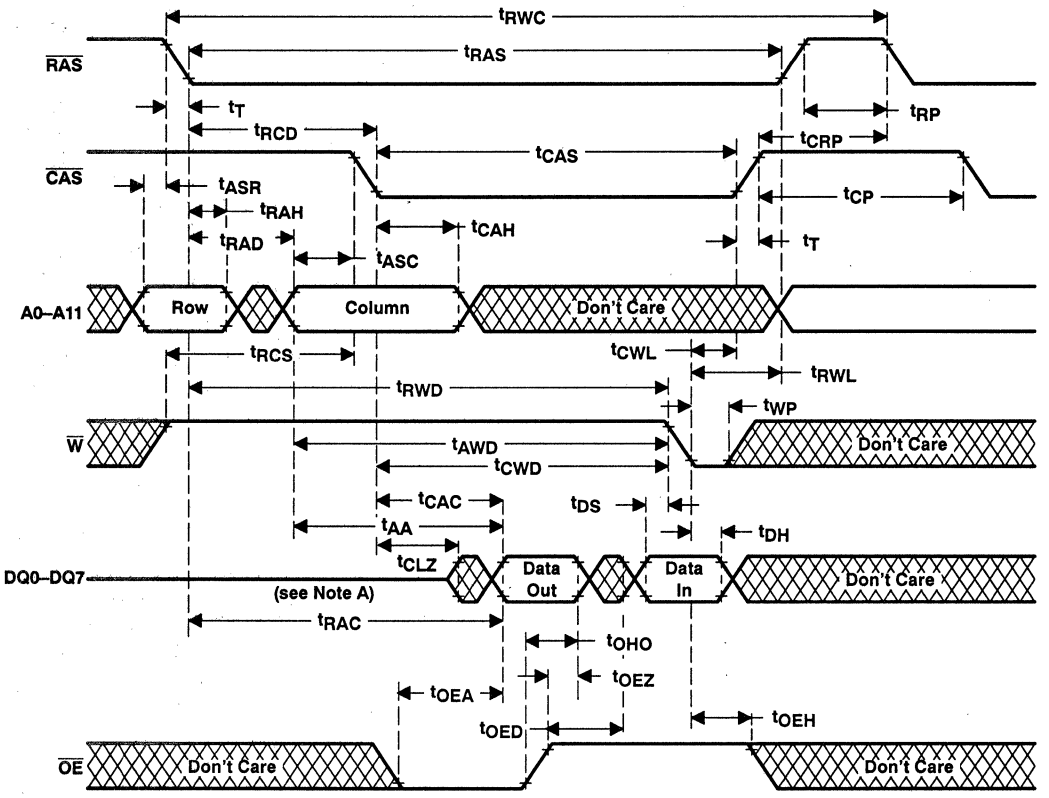
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

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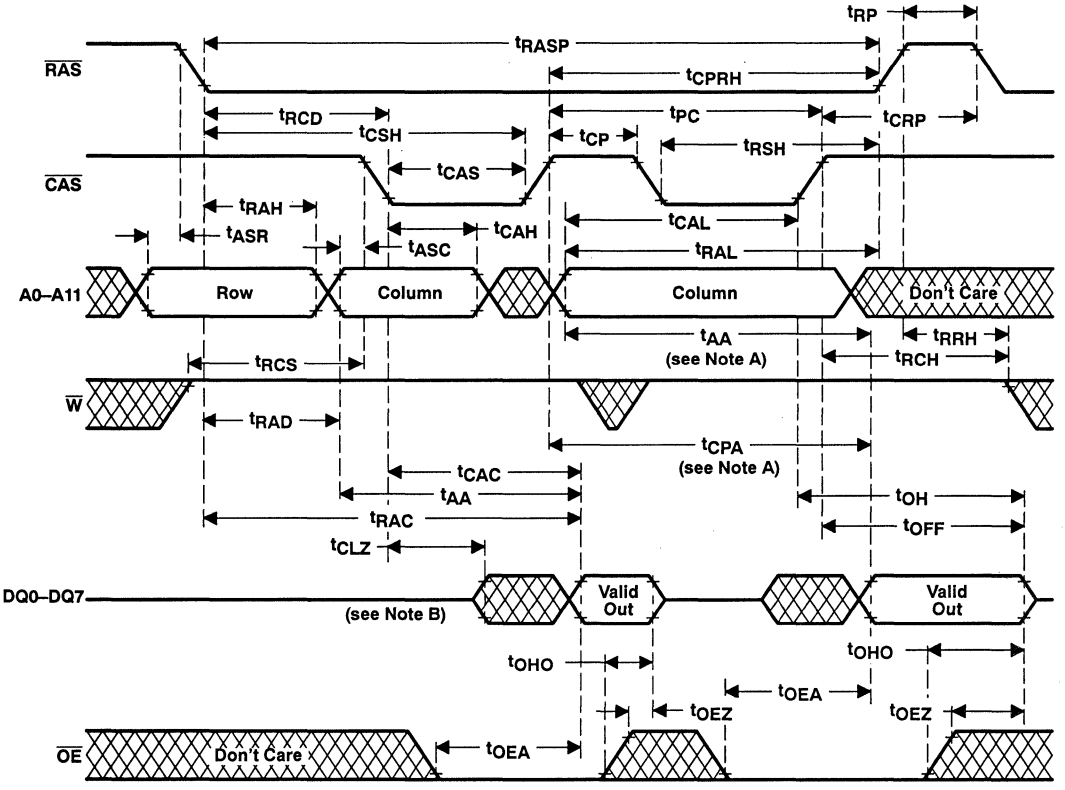
PARAMETER MEASUREMENT INFORMATION

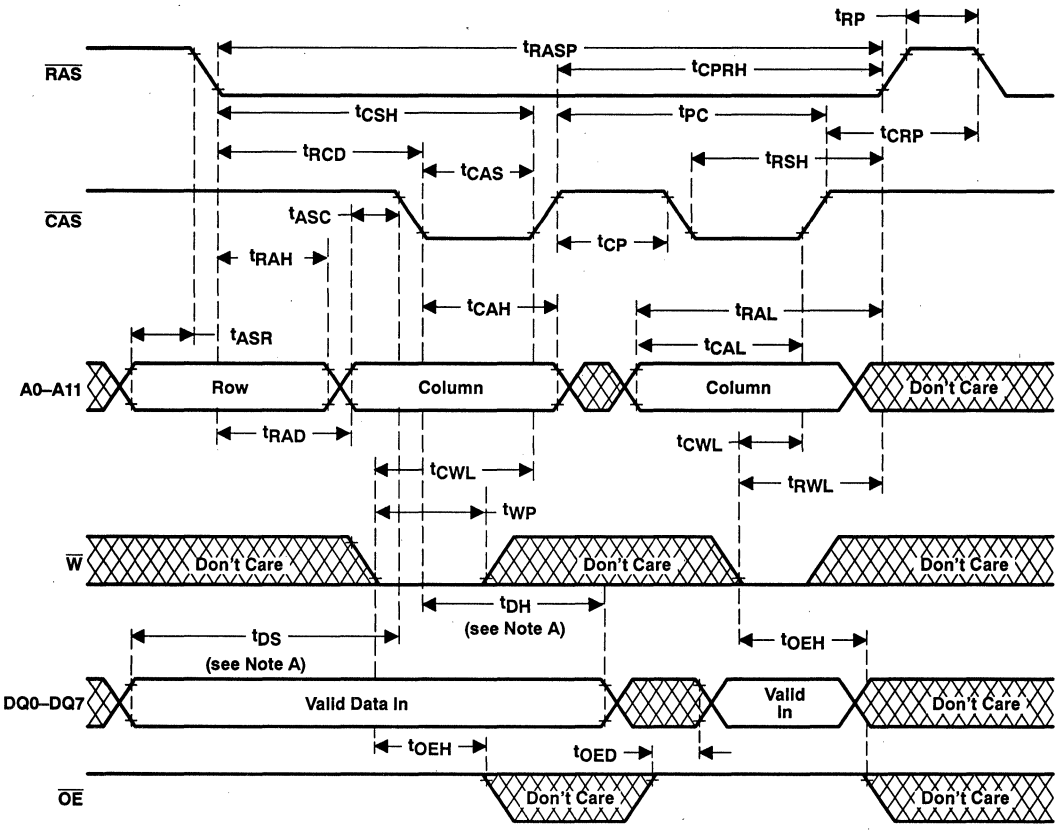


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
C. A write cycle or read-modify-write cycle can be intermixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PRODUCT PREVIEW

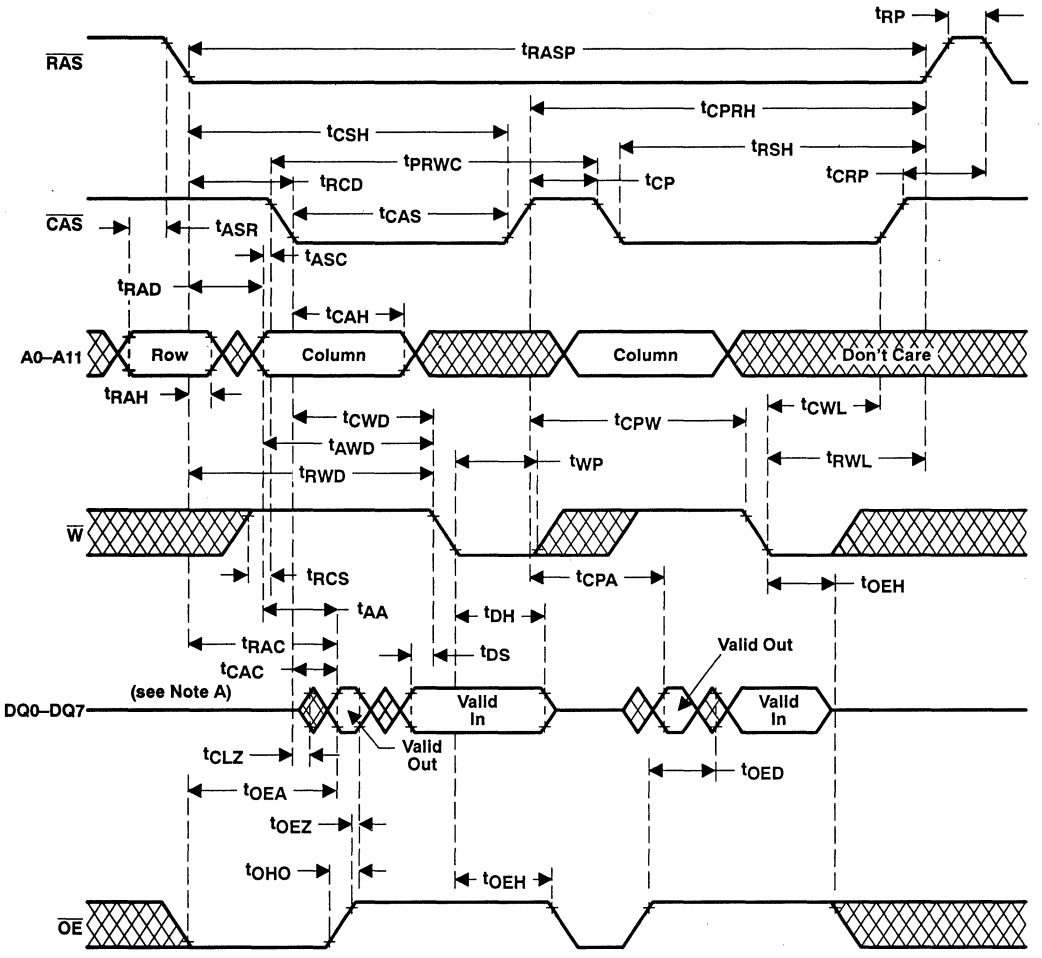
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
B. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

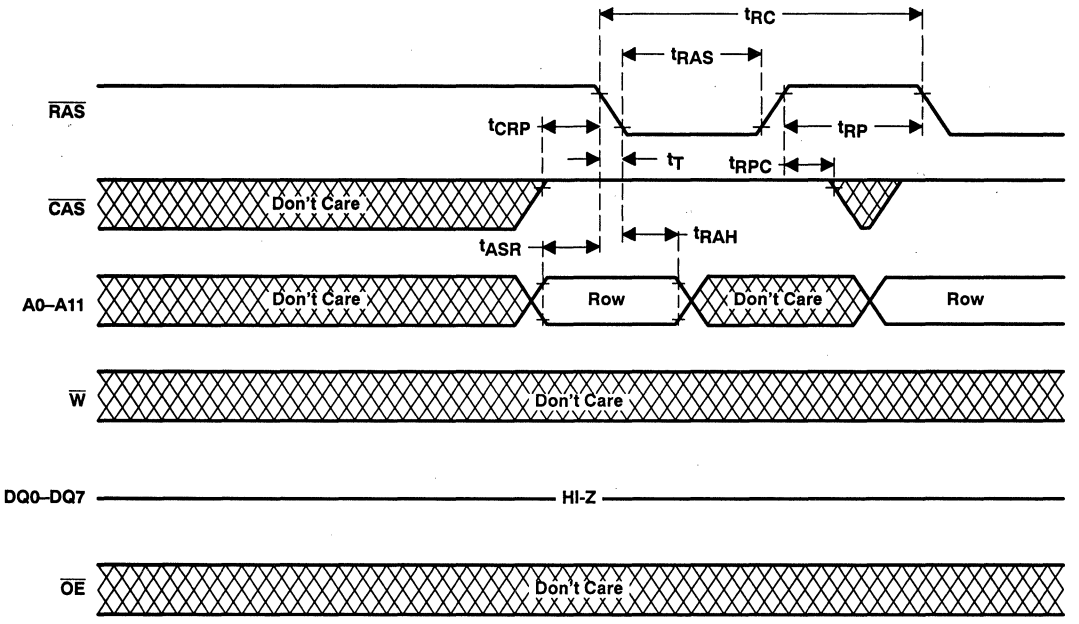


Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

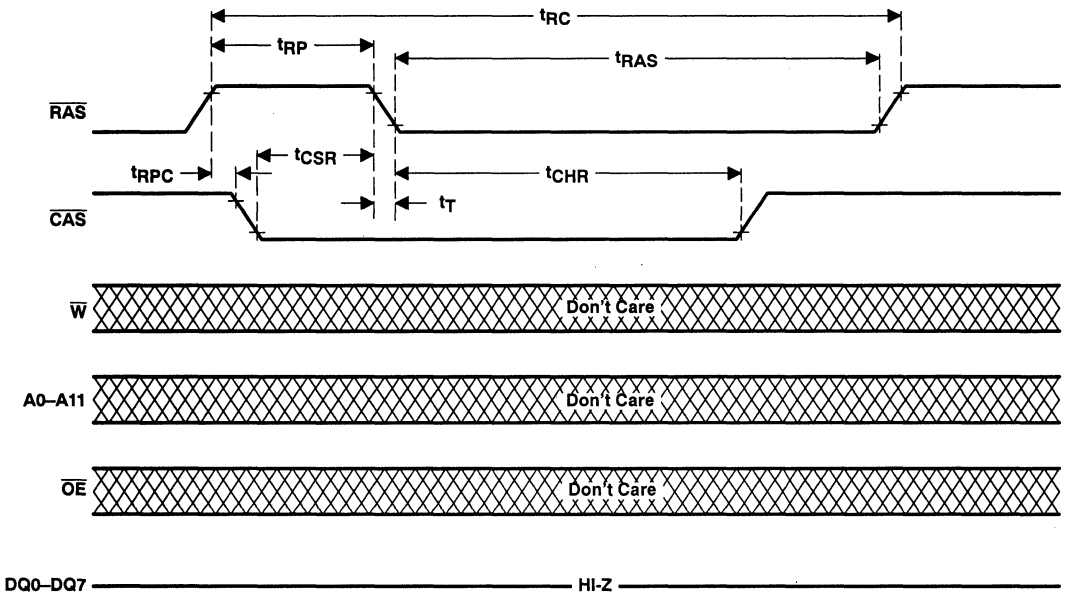
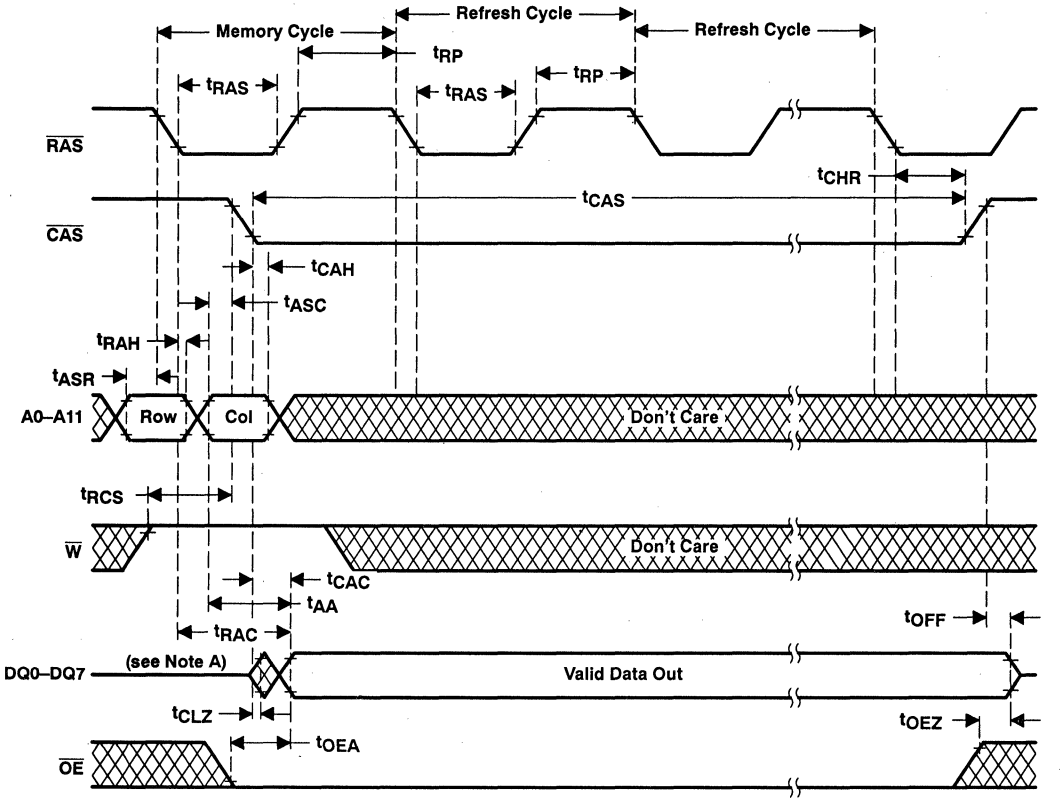


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PRODUCT PREVIEW

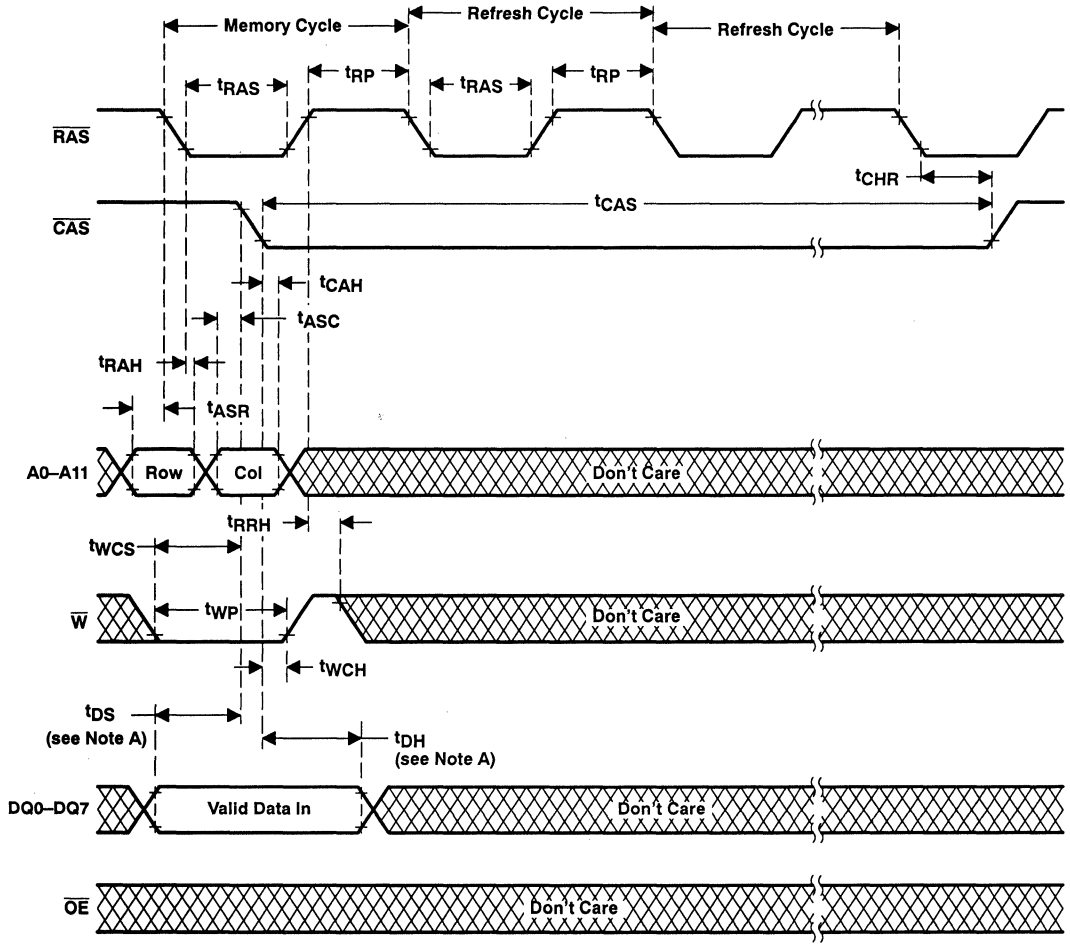
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 12. Hidden Refresh Cycle (Write)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

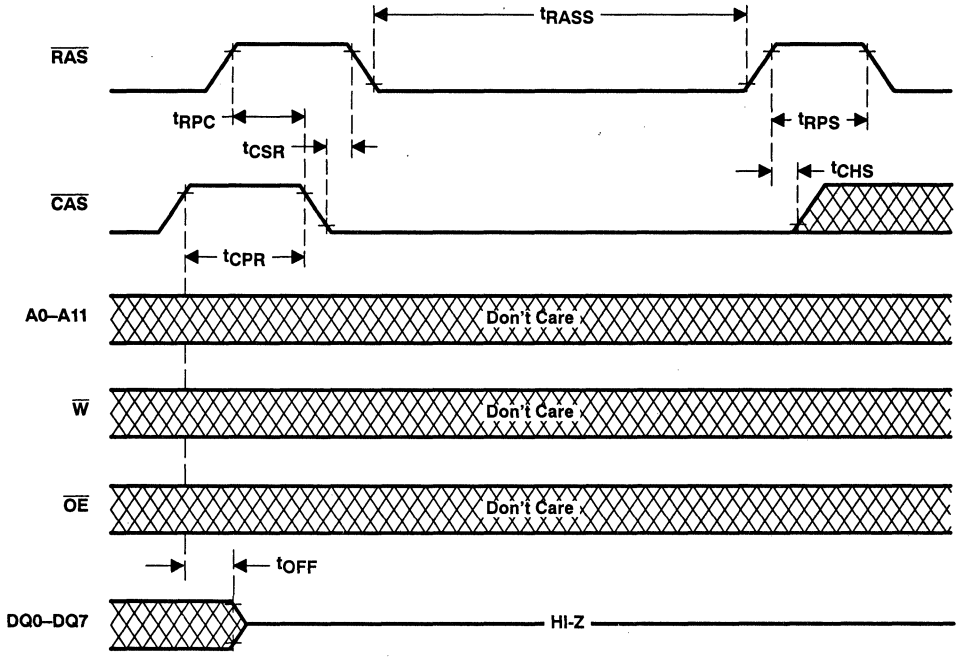
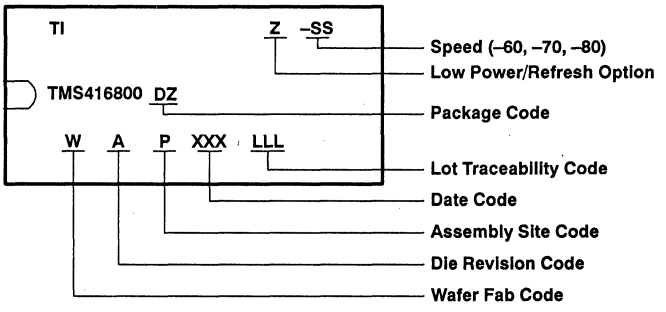


Figure 13. Self Refresh Timing

device symbolization



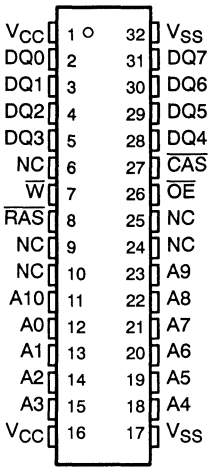
PRODUCT PREVIEW

- **Organization . . . 2 097 152 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

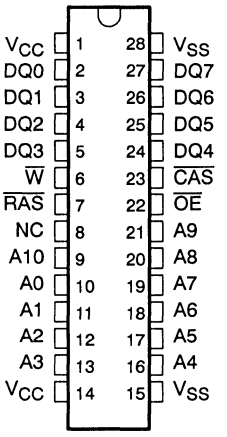
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'417800/P-60	60 ns	15 ns	30 ns	110 ns
'417800/P-70	70 ns	18 ns	35 ns	130 ns
'417800/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **2048-Cycle Refresh in 32 ms (Max)**
  - **256 ms for Low Power, Self-Refresh Version (TMS417800P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Self-Refresh With Low-Power**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 28-Pin, J-Lead 400-Mil-Wide Surface Mount Package (SOJ), and 32-Pin, Plastic Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

DE PACKAGE† (TOP VIEW)



DZ PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write-Enable
V_{CC}	5-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS417800 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

The TMS417800P series are high-speed, low-power, self-refresh, 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 578 mW operating and 11 mW standby for 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS417800 and TMS417800P series are offered in a 400-mil 28-lead plastic surface mount SOJ package (DZ suffix) and a 32-lead plastic surface mount TSOP package (DE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS417800 and TMS417800P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-one address bits are required to decode 1 of 2 097 152 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ0–DQ7)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every thirty-two milliseconds (256 ms for TMS417800P) to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 μA refresh current is available on the TMS417800P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

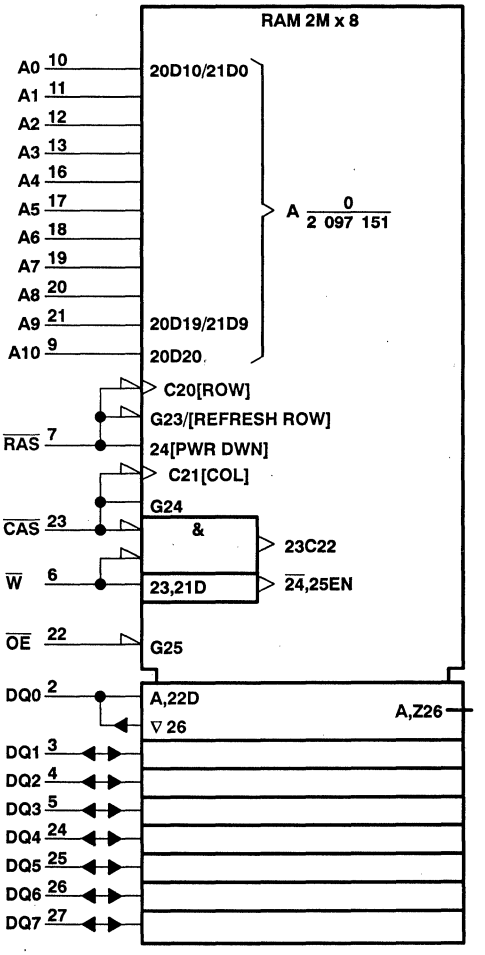
self refresh (TMS417800P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

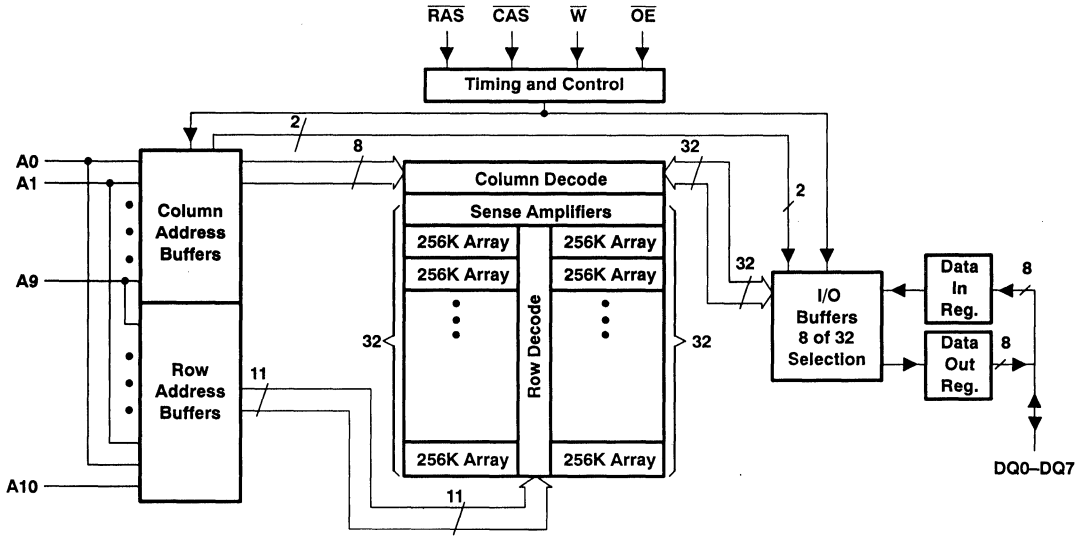
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . –1 V to 7 V
Supply voltage range on V_{CC} . . . . . –1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			125		115		105	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'417800		1		1		1	mA
			'417800P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			125		115		105	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			125		115		105	mA
I_{CC10}‡	Battery backup operating current (equivalent refresh time is 256 ms) CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA
I_{CC6}‡	Self refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			500		500		500	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Data out = Enabled			5		5		5	mA

† Measured with outputs open.
‡ For TMS417800P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

PRODUCT PREVIEW

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz † (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns
t_{OHO}	Output disable time, start of $\overline{OE}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-modify-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high ($\overline{CAS}$ precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high ($\overline{RAS}$ precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-modify-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	35		40		45		ns

NOTES: 11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or T_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	110		130		150		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	−50		−50		−50		ns
t_{REF}	Refresh time interval (TMS417800)		32		32		32	ms
t_{REF}	Refresh time interval Low power (TMS417800P only)		256		256		256	ms
t_T	Transition time	3	30	3	30	3	30	ns

PARAMETER MEASUREMENT INFORMATION

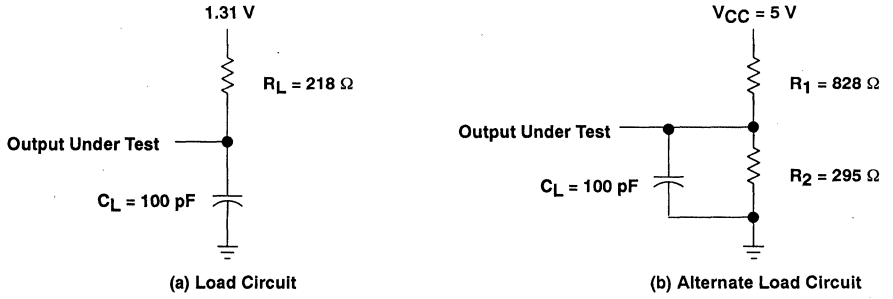

Figure 1. Load Circuits for Timing Parameters

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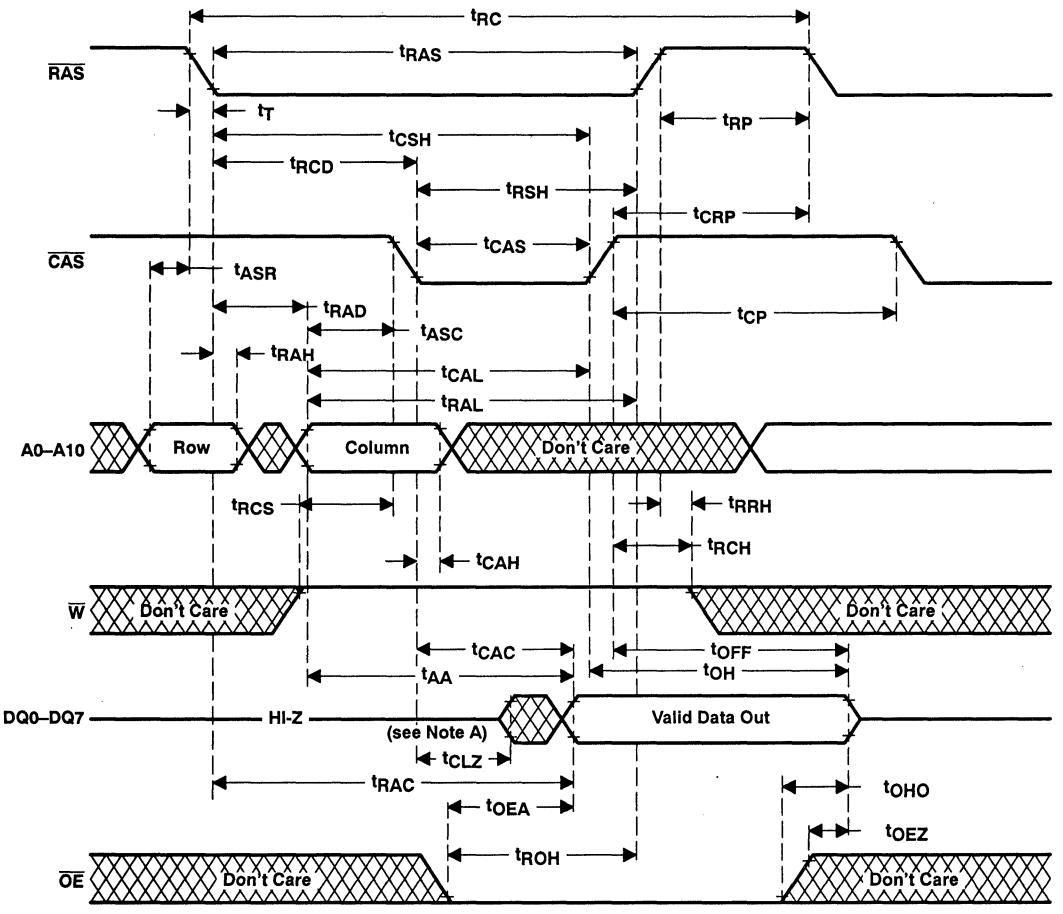
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

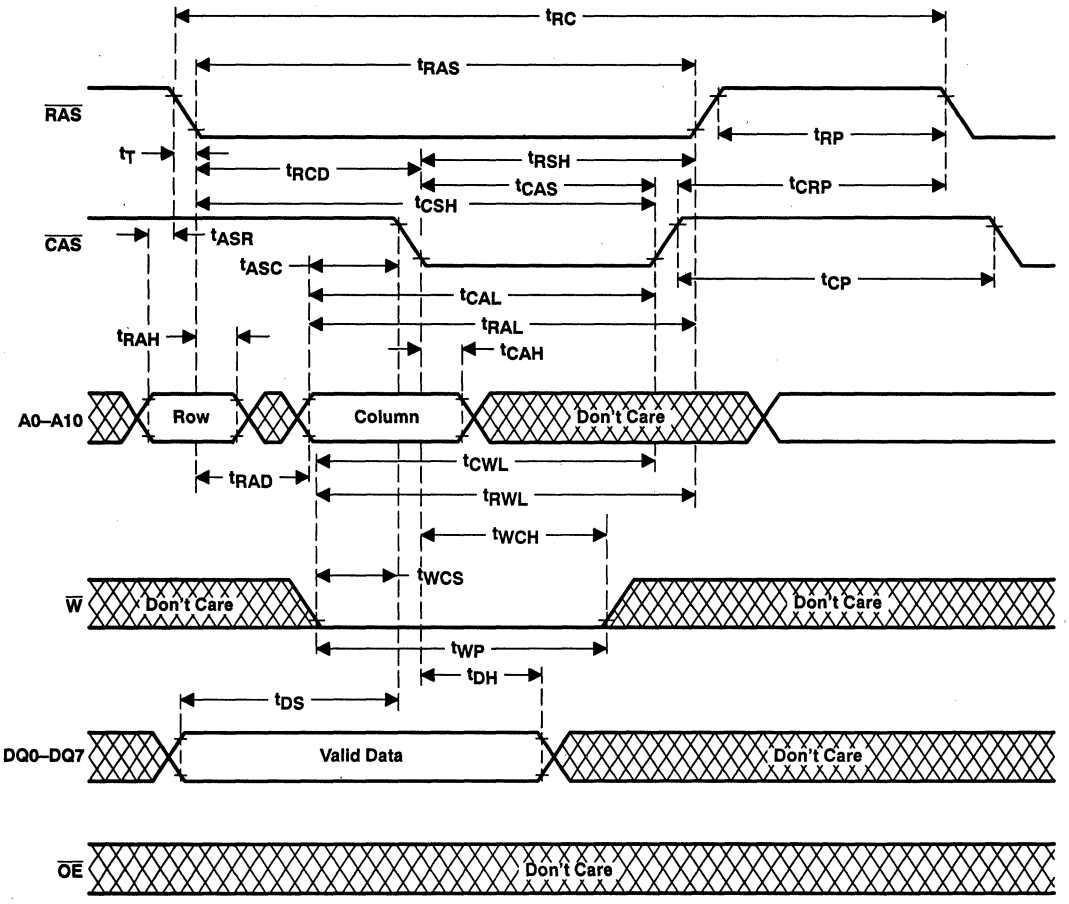
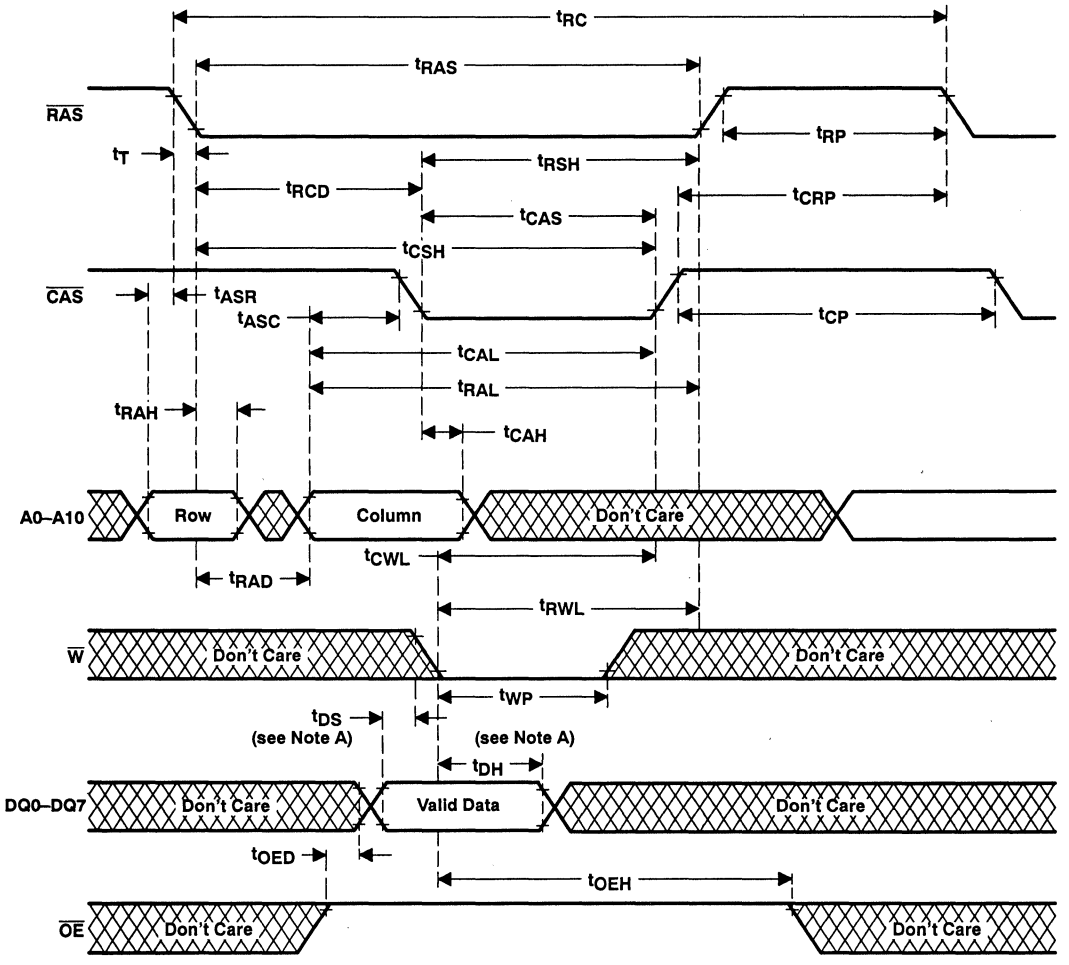


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

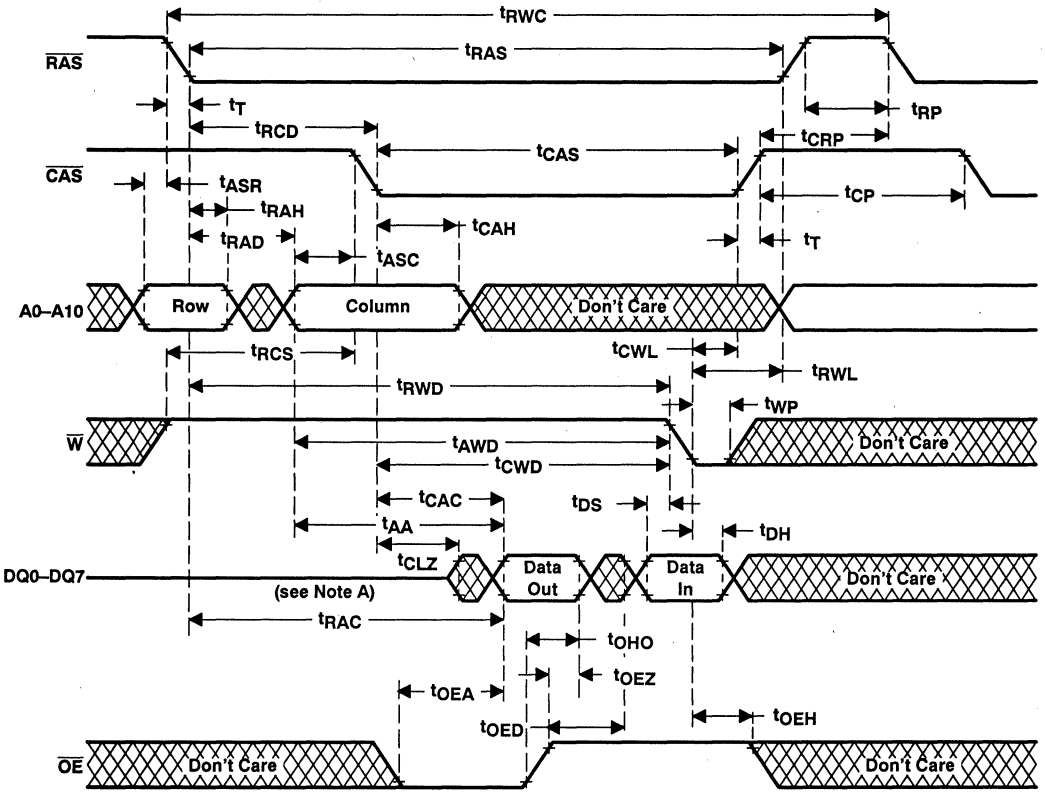


NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 4. Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

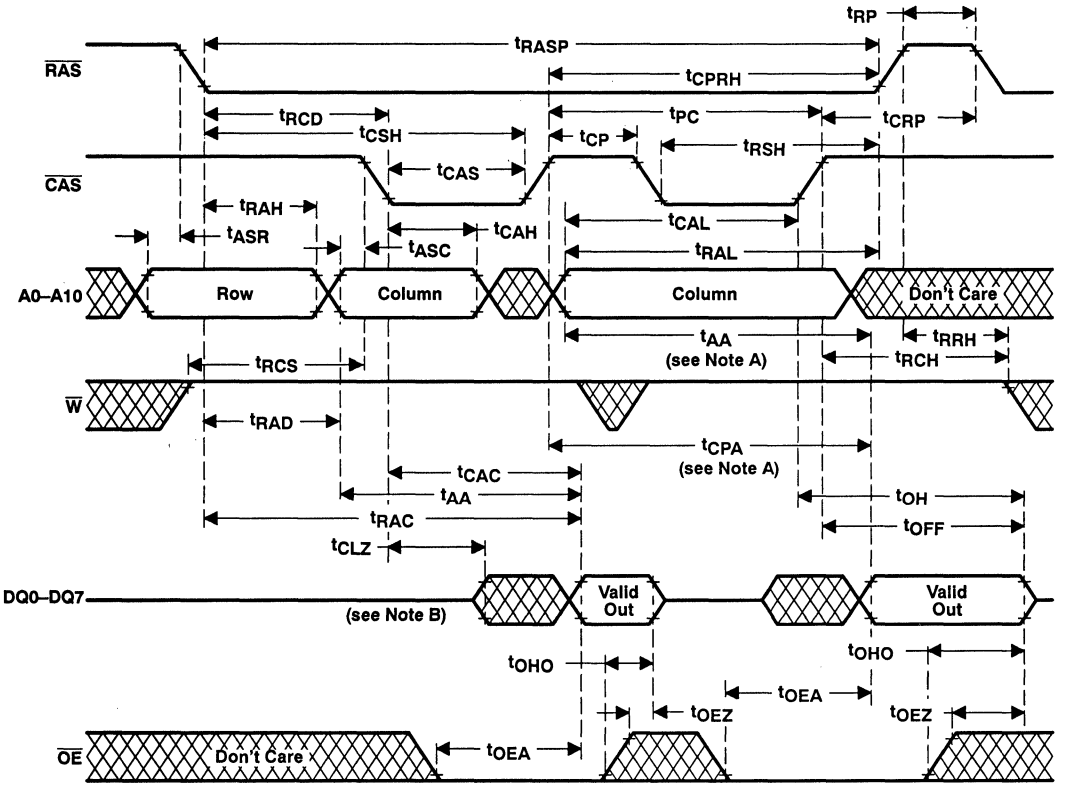


NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

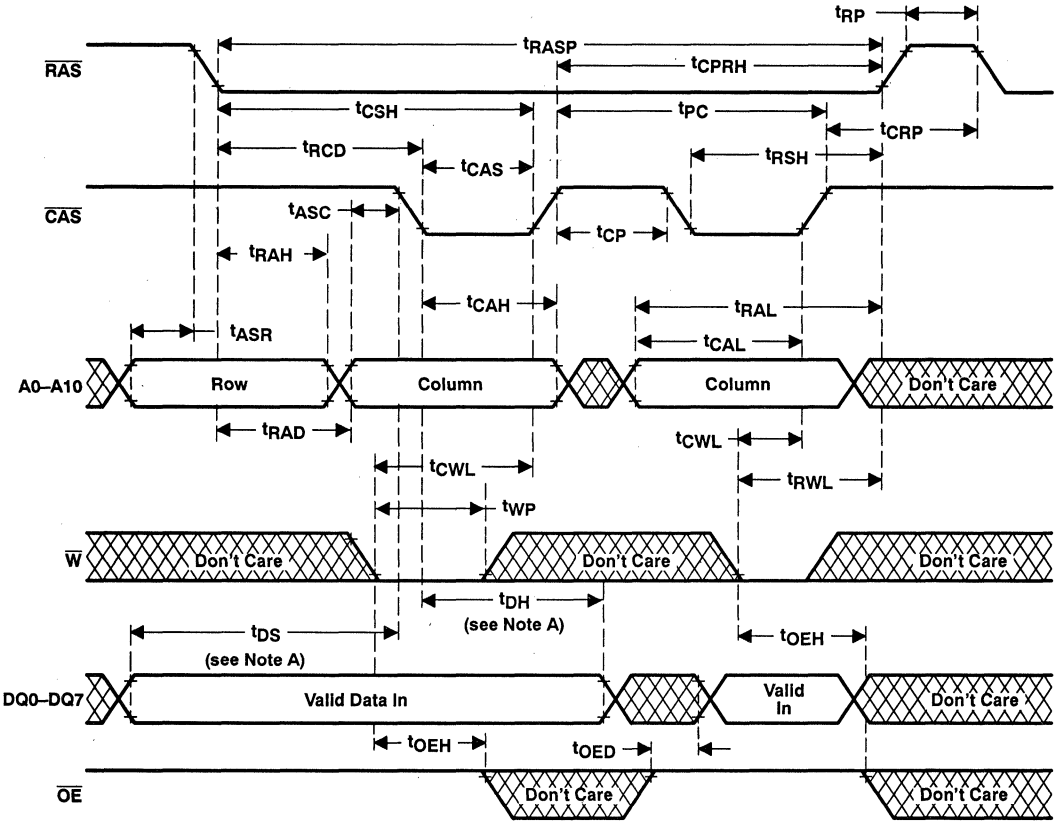


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
C. A write cycle or read-modify-write cycle can be intermixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

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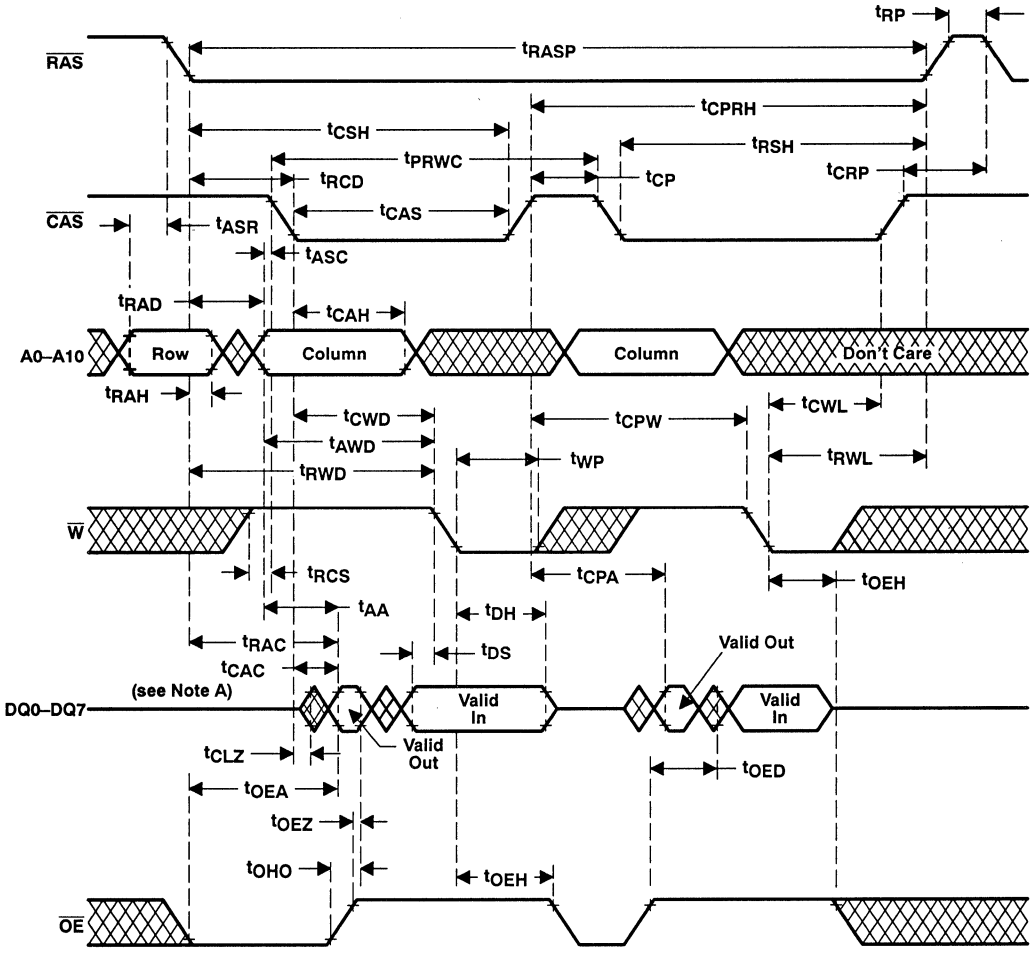
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

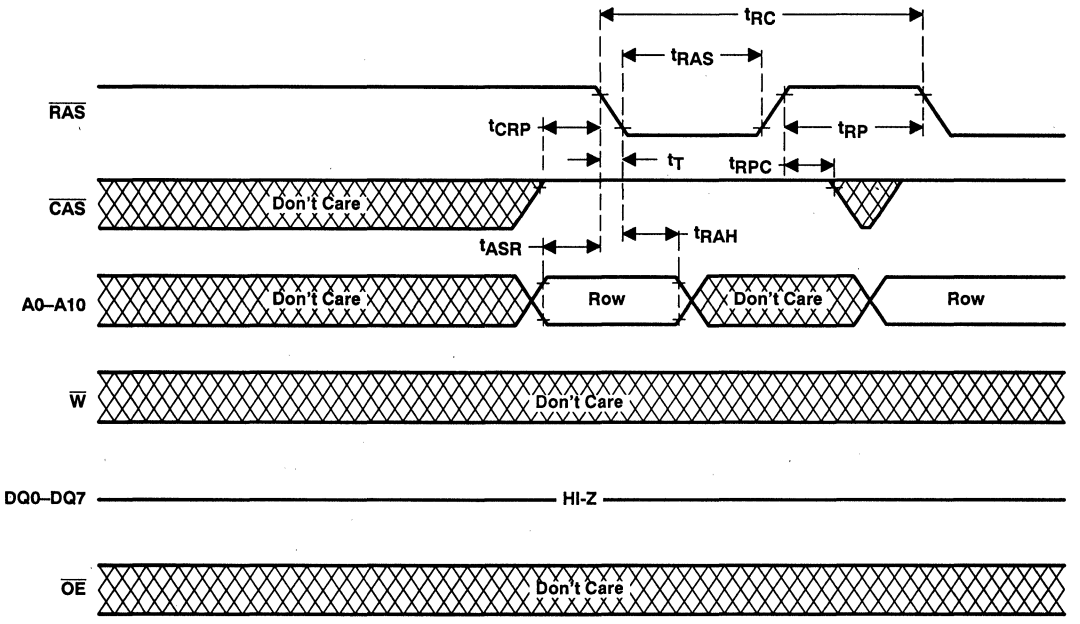


Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

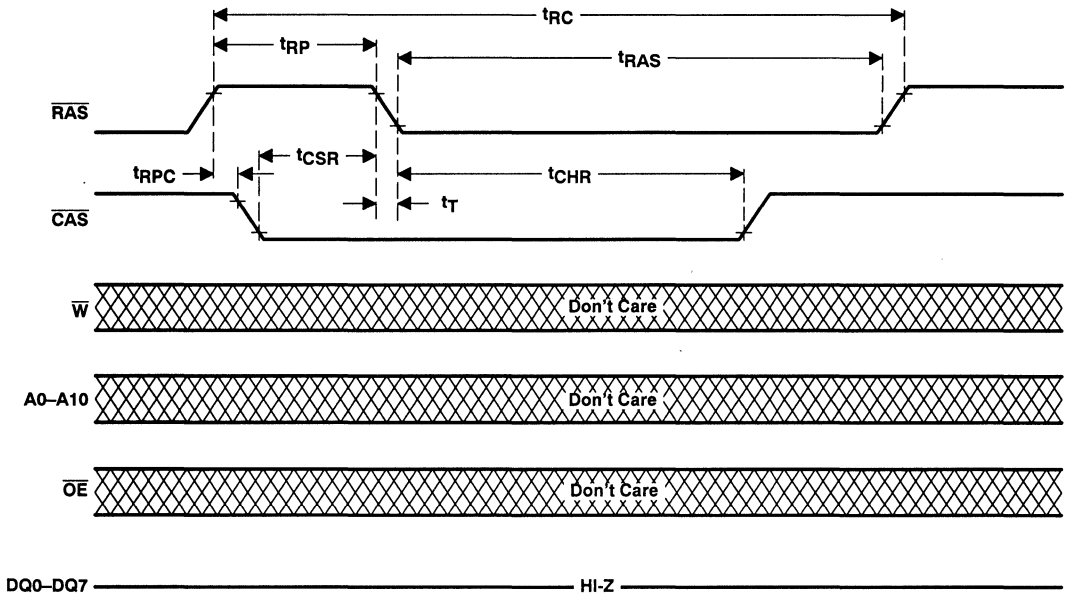
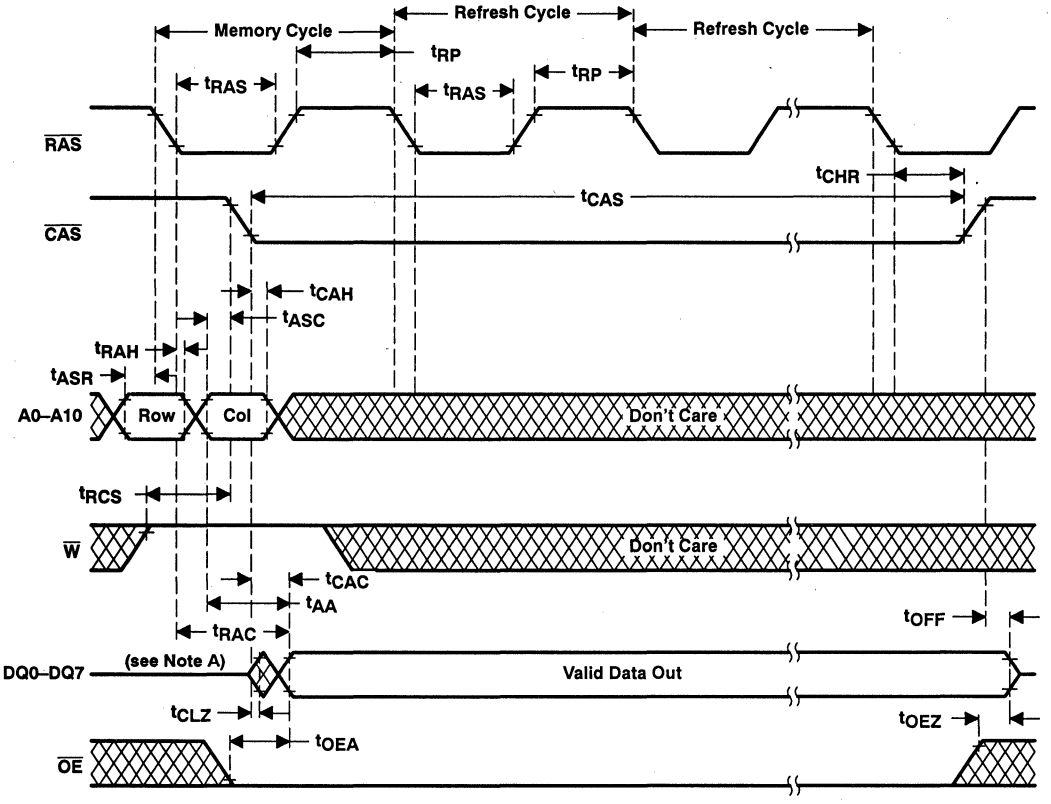


Figure 10. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 11. Hidden Refresh Cycle (Read)

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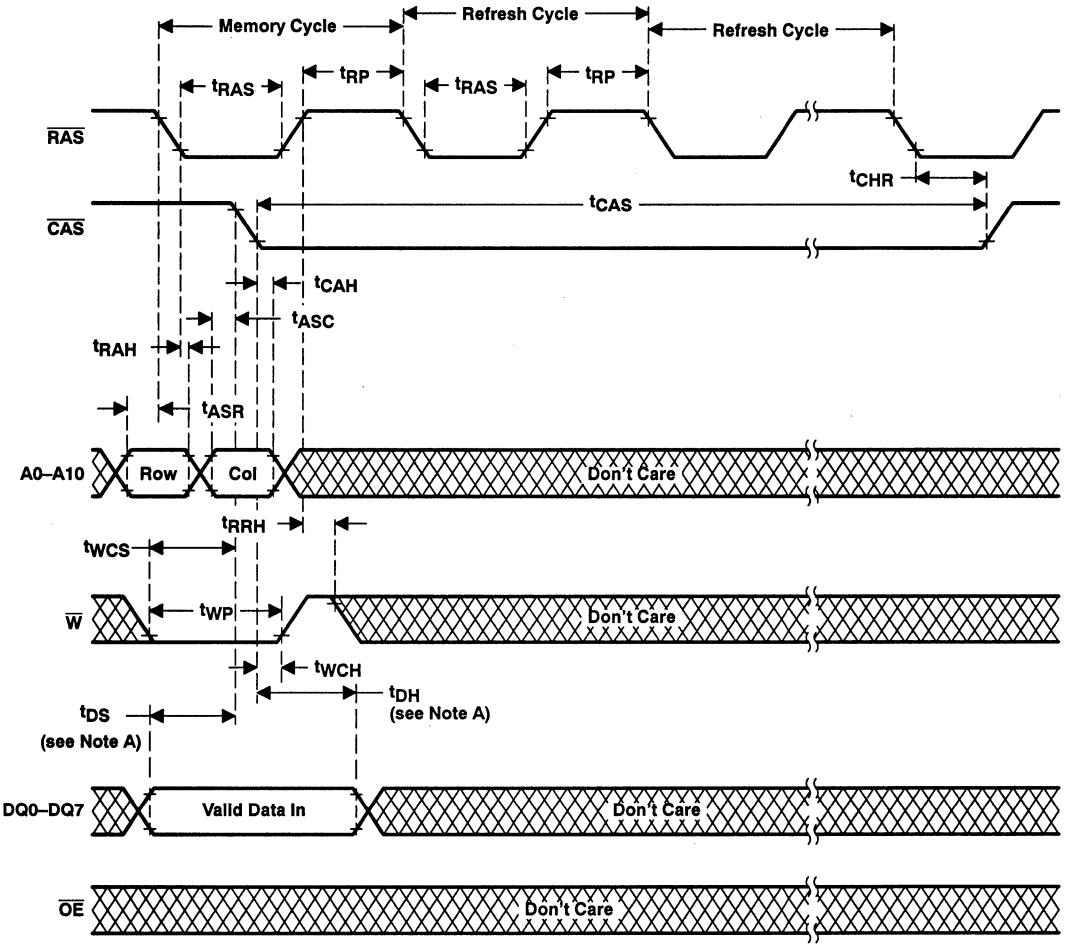
PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 12. Hidden Refresh Cycle (Write)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

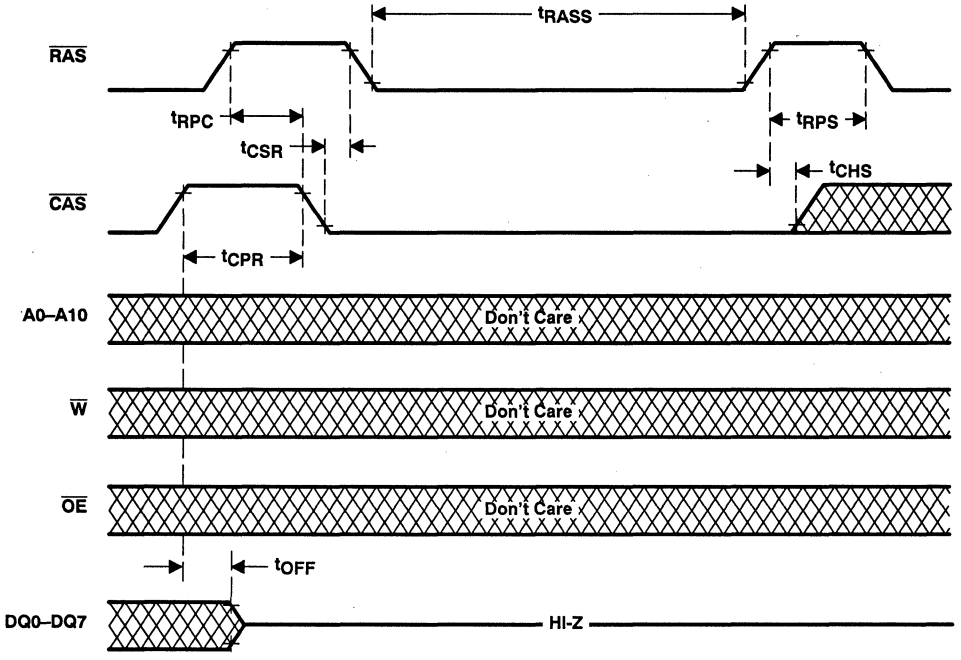
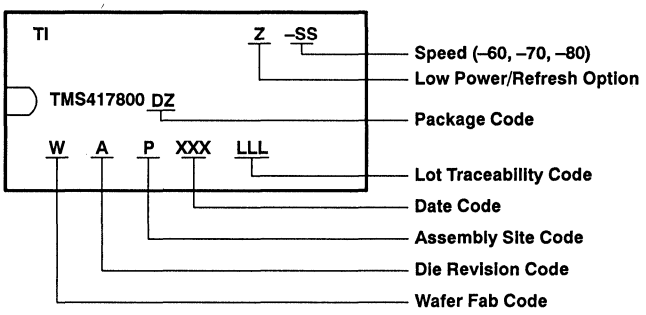


Figure 13. Self Refresh Timing

device symbolization



PRODUCT PREVIEW

TEXAS INSTRUMENTS
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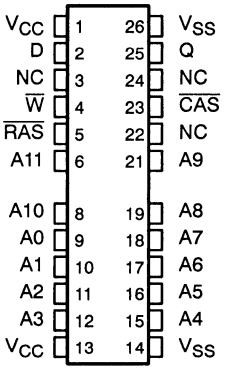
- **Organization . . . 16 777 216 × 1**
- **Single 3.3-V Power Supply (±0.3-V Tolerance)**
- **Low Power Dissipation (TMS426100P Only)**
  - **100 μA CMOS Standby**
  - **100 μA Self Refresh**
  - **100 μA Extended Refresh Battery Backup**
- **Performance Ranges:**

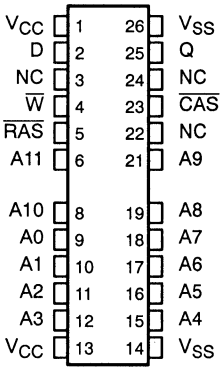
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'426100/P-60	60 ns	15 ns	30 ns	110 ns
'426100/P-70	70 ns	18 ns	35 ns	130 ns
'426100/P-80	80 ns	20 ns	40 ns	150 ns
'426100/P-10	100 ns	25 ns	50 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **4096 Cycle Refresh in 64 ms (Max)**
  - **512 ms Max for Low-Power, Self Refresh Version (TMS426100P)**
- **3-State Unlatched Output**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

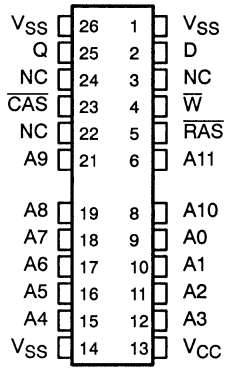
DJ PACKAGE†
(TOP VIEW)



DGA PACKAGE†
(TOP VIEW)



DGB PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

description

The TMS426100 series are high-speed, low-voltage 16 777 216-bit dynamic random-access memories, organized as 16 777 216 words by one bit each.

The TMS426100P series are high-speed, low-voltage low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 16 777 216 words by one bit each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low voltage at low cost.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

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EPIC is a trademark of Texas Instruments Incorporated.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns. Maximum power dissipation is as low as 180 mW operating, 0.36 mW standby, and battery backup for an 80-ns device.

All inputs and outputs, and clocks are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS426100, TMS426100P is offered in a 300-mil 24/26-lead plastic surface mount SOJ package (DJ suffix), a 24/26-lead plastic small outline package (DGA suffix), and a 24/26-lead plastic small outline package, reverse form (DGB suffix). All packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that may be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

The column address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS426100 family to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set up on inputs A0–A11 and latched during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the fallling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

refresh

A refresh operation must be performed at least once every 64 ms (512 ms for TMS426100P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS426100P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs, while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self-refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

power up

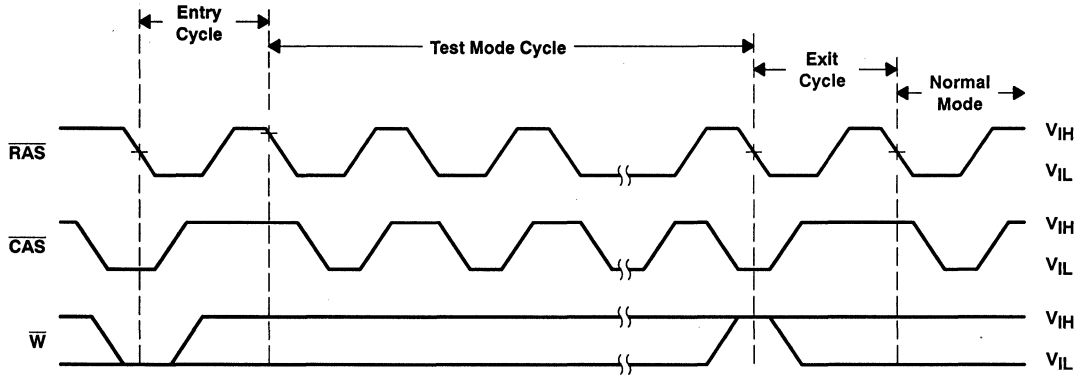
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

PRODUCT PREVIEW

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits the test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

Test mode causes the part to be internally reconfigured into a 1M × 16 bit device with 16-bit parallel read and write data path. Column addressess CA0, CA1, CA10, and CA11 are not used. During a read cycle all 16 bits of the internal data bus are compared. If all bits are the same data state, the output pin will go high. If one or more bits disagree, the output pin will go low. Test time in test mode can thus be reduced by a factor of 16, compared to normal memory mode.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

Figure 1. Test Mode Cycle†

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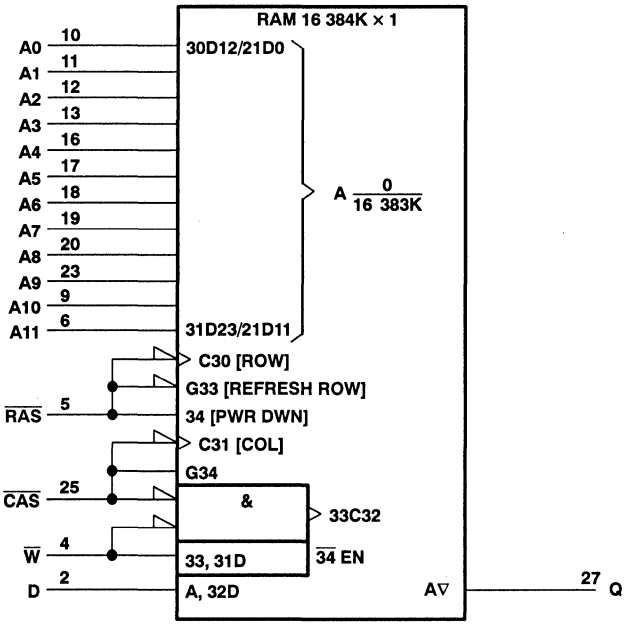
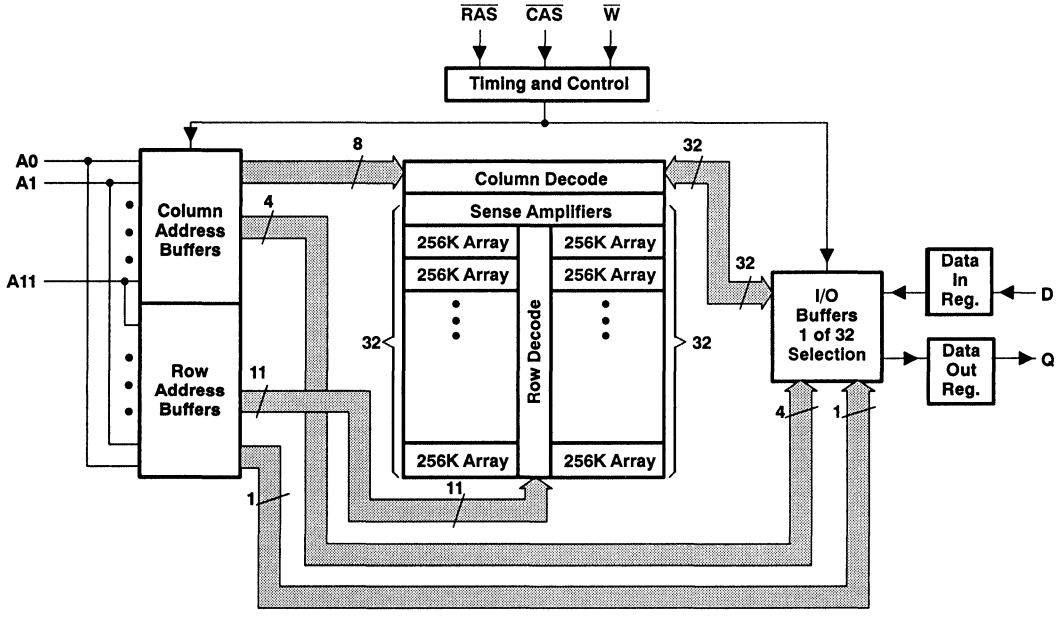
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 20/26 pin SOJ package (DJ suffix).

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin, V_{SS} (see Note1) ..... – 0.5 V to 4.6 V
Supply voltage range, V_{CC} ..... – 0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'426100-60 '426100P-60		'426100-70 '426100P-70		'426100-80 '426100P-80		'426100-10 '426100P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = + 2 mA			0.4		0.4		0.4		0.4	V
V_{OH}	Option	I_{OH} = –100 µA		V_{CC} – 0.2		V_{CC} – 0.2		V_{CC} – 0.2		V_{CC} – 0.2		V
V_{OL}	Option	I_{OL} = +100 µA			0.2		0.2		0.2		0.2	
I_I	Input current (leakage)†	V_I = 0 to 3.9 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)†	V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 3.6 V			70		60		50		40	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			1		1		1		1	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH}= V_{CC} –0.2 V (CMOS)	'426100		300		300		300		300	µA
			'426100P		100		100		100		100	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50		40	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40		35	mA
I_{CC6}‡	Self-refresh	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			100		100		100		100	µA
I_{CC7}	Standby current output enable‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5		5	mA
I_{CC10}‡	Battery backup (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100		100		100	µA

† Minimum cycle, V_{CC} = 3.6
‡ For TMS426100P only

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{I(D)}$	Input capacitance, data input			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS426100-60 TMS426100P-60		TMS426100-70 TMS426100P-70		TMS426100-80 TMS426100P-80		TMS426100-10 TMS426100P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	25	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS426100-60 TMS426100P-60		TMS426100-70 TMS426100P-70		TMS426100-80 TMS426100P-80		TMS426100-10 TMS426100P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{RASS}	Self-refresh, $\overline{RAS}$ low time		100		100		100		100	µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RPS}	$\overline{RAS}$ precharge after self-refresh	110		130		150		180		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'426100-60 '426100P-60		'426100-70 '426100P-70		'426100-80 '426100P-80		'426100-10 '426100P-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low		10		15		15		15		ns
t_{DH}	Data hold time (see Note 10)		10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low		10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)		0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)		5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)		15		15		15		15		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)		10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)		30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high		60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)		10		10		10		10		ns
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (Self-refresh)		−50		−50		−50		−50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)		15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)		15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high		30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)		20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)		60		70		80		100		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge		35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge		35		40		45		50		ns
t_{TAA}	Access time from address (test mode)		35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		105		ns
t_{REF}	Refresh time interval	'426100		64		64		64		64	ms
		'426100P		512		512		512		512	ms
t_T	Transition time		3	30	3	30	3	30	3	30	ns

NOTES: 10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to insure access time.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

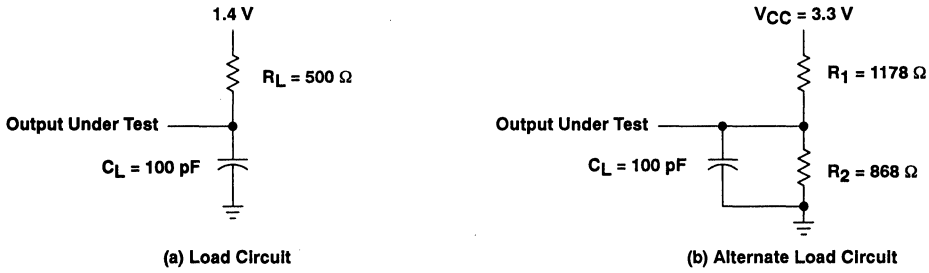
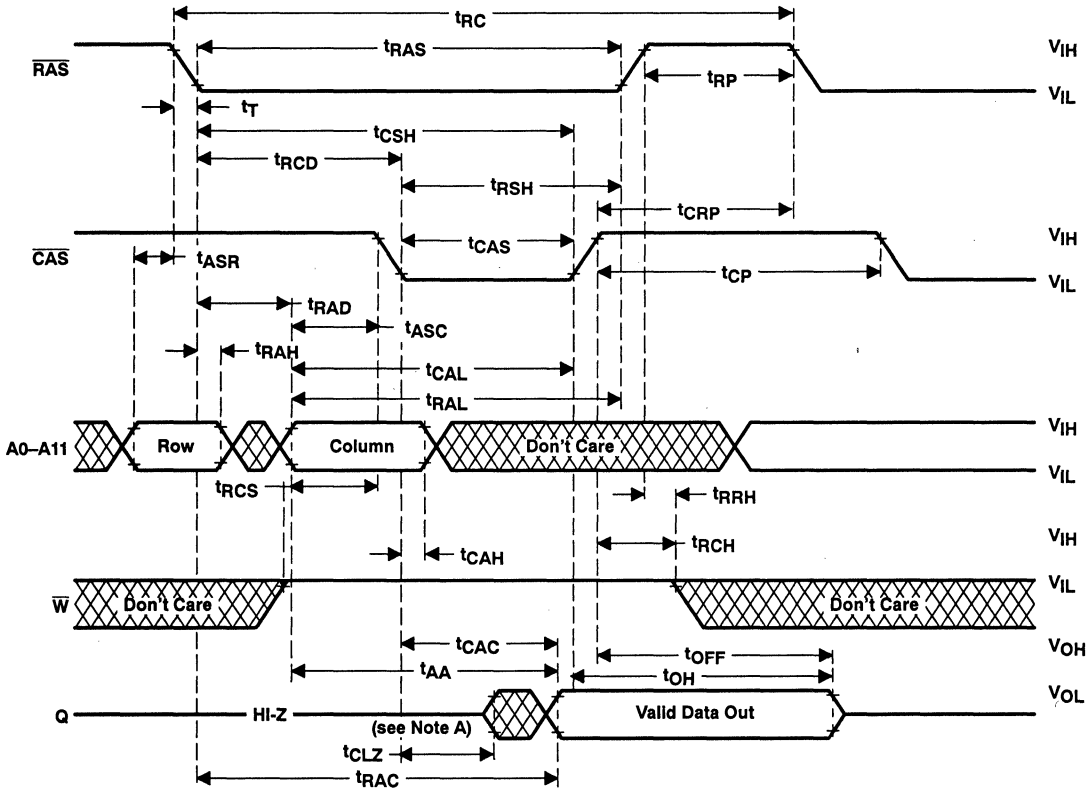


Figure 2. Load Circuits for Timing Parameters



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

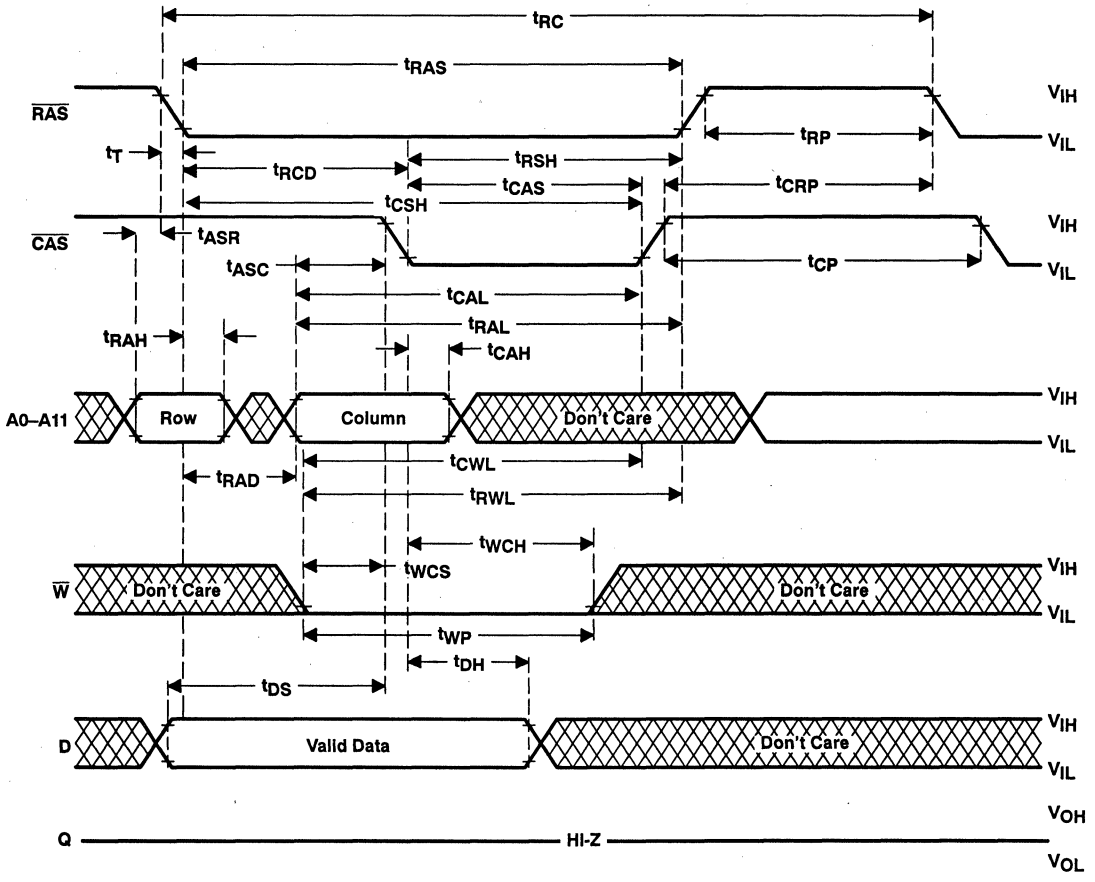

Figure 4. Early Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

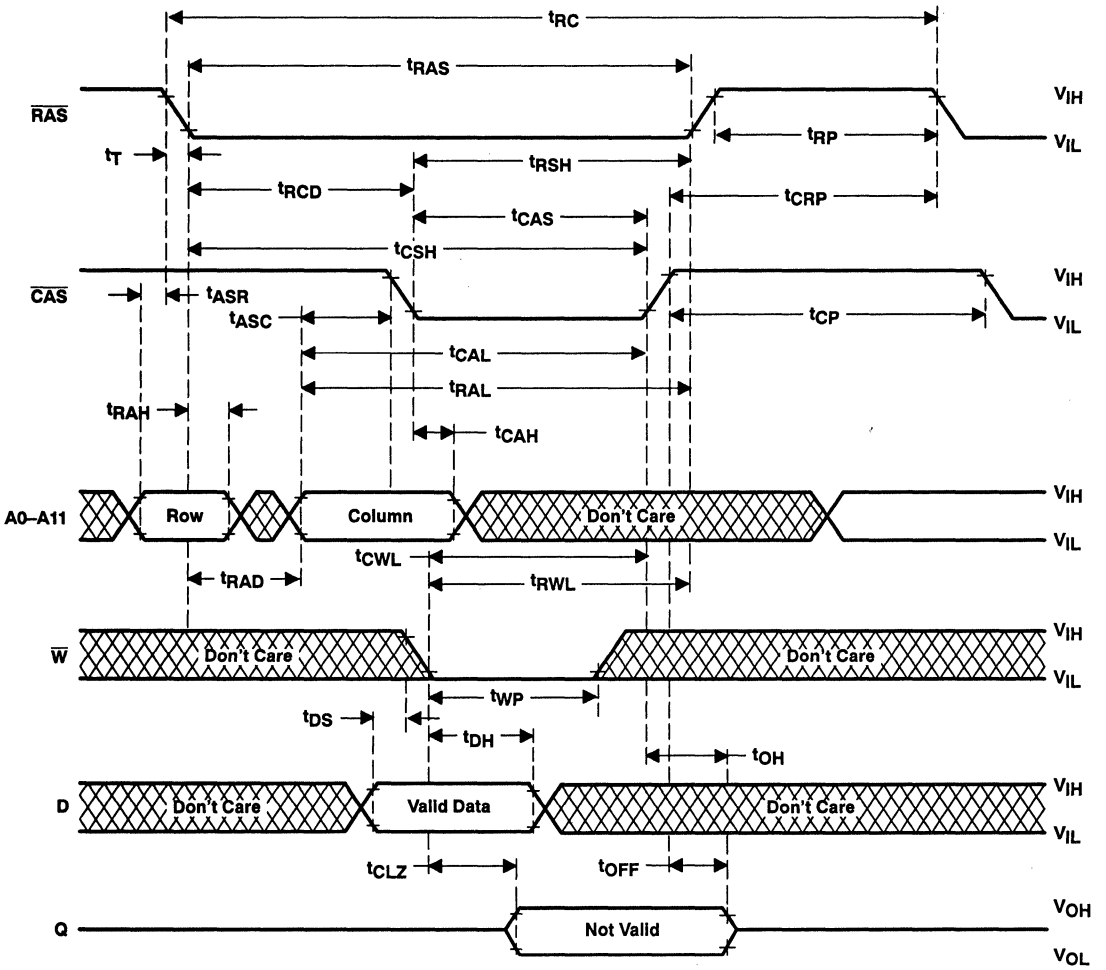
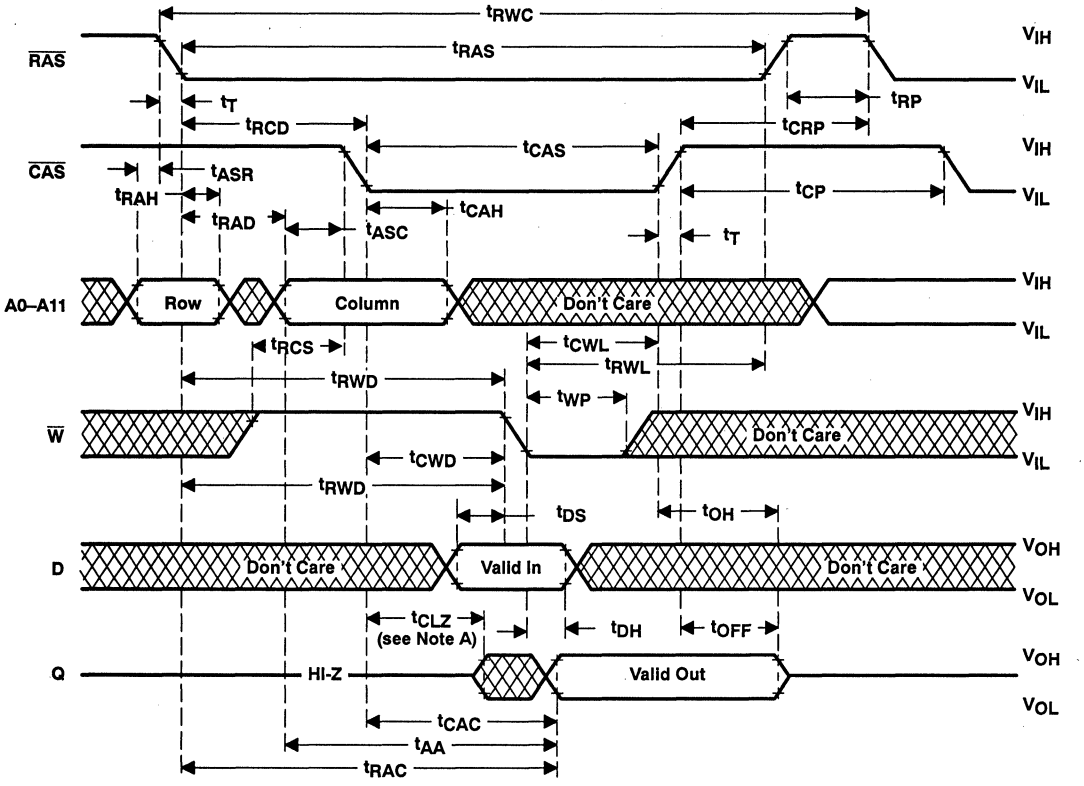


Figure 5. Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

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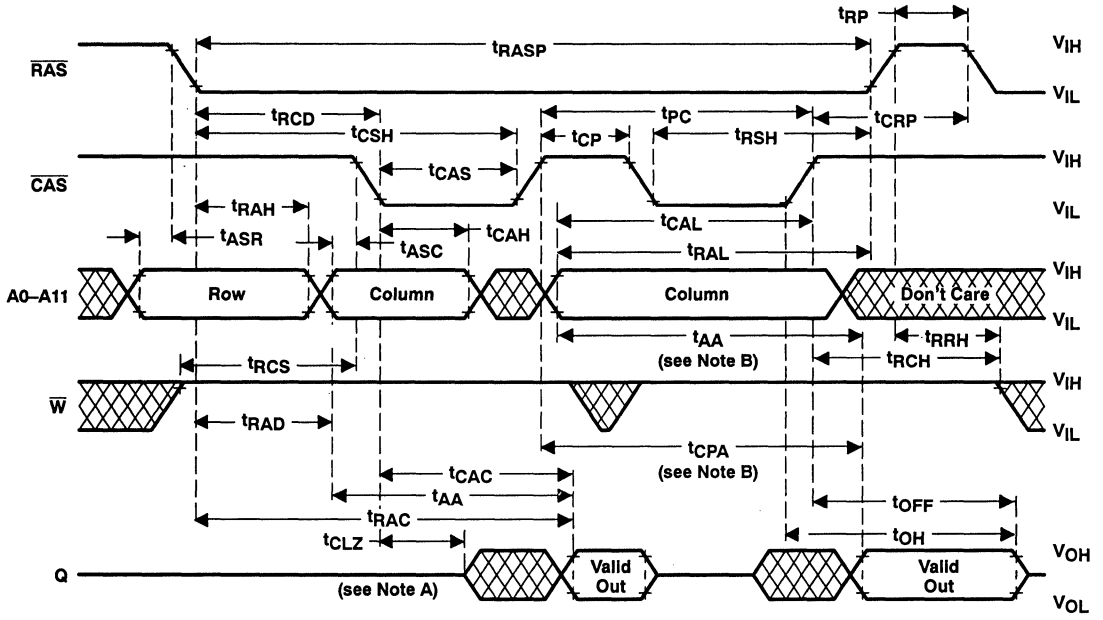
PARAMETER MEASUREMENT INFORMATION

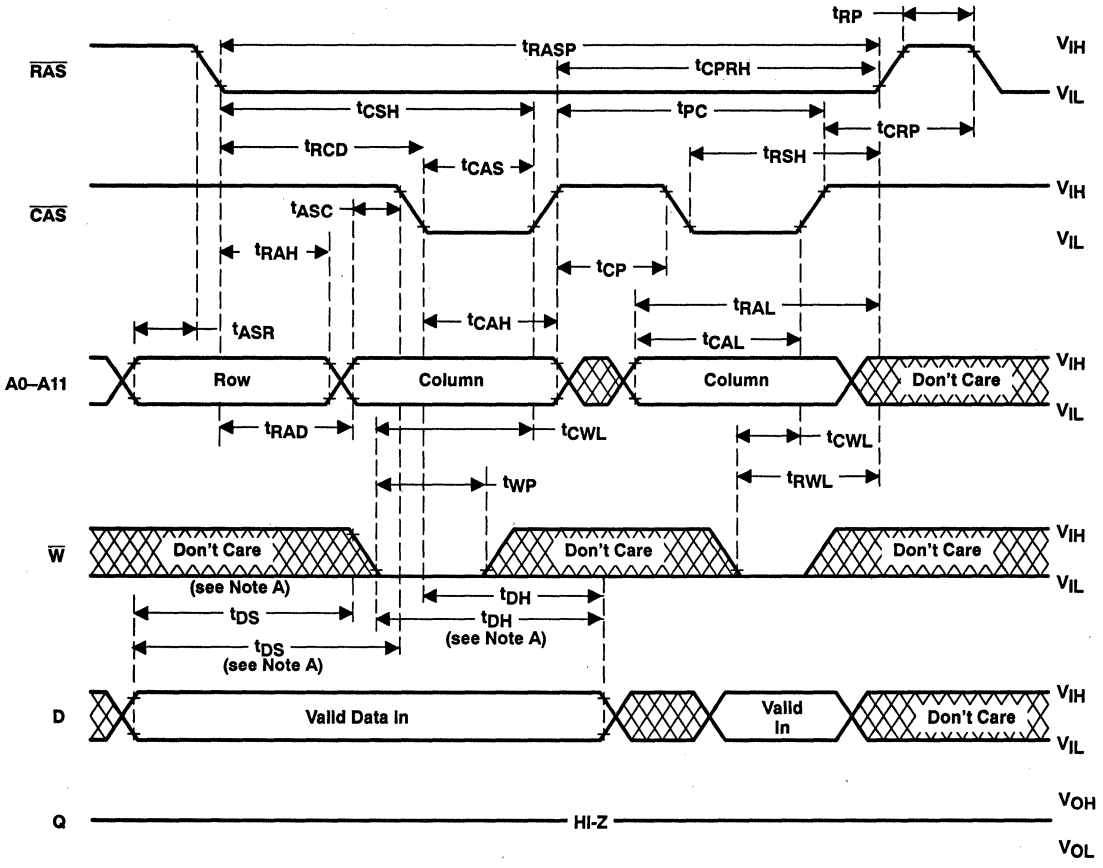


NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

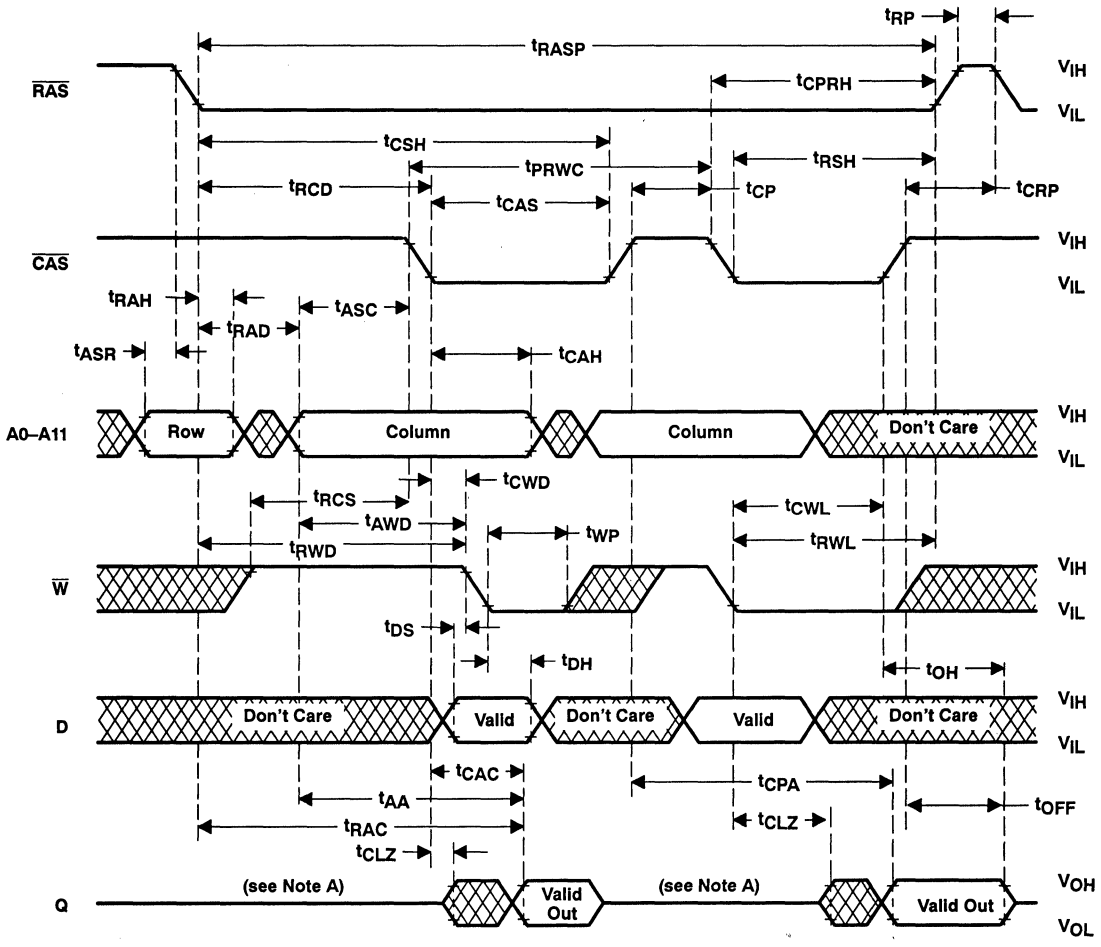


NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

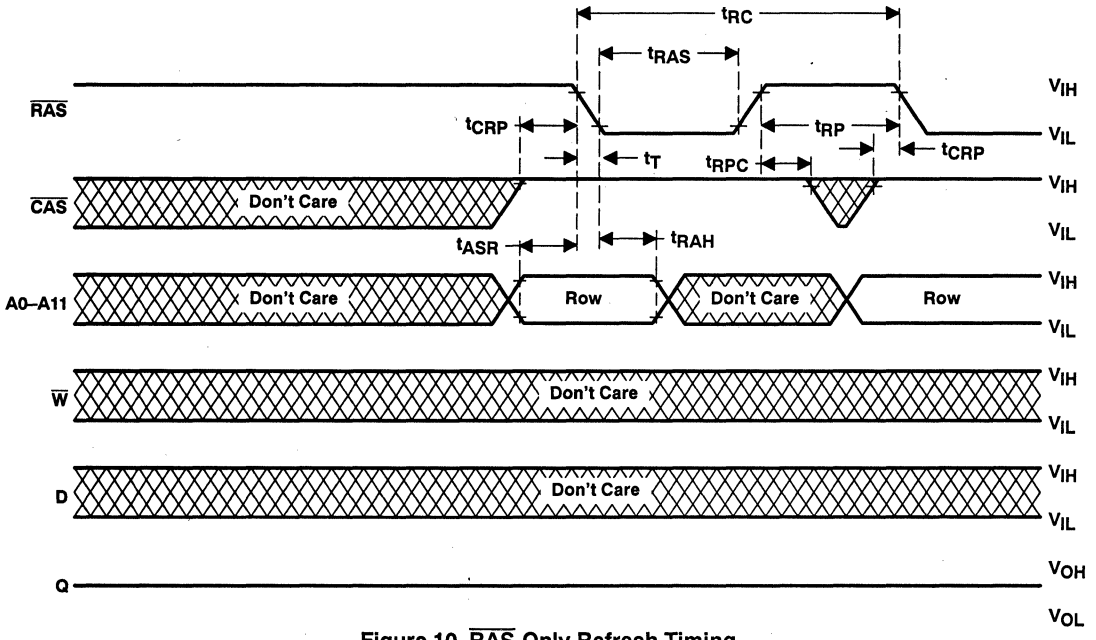

Figure 10. $\overline{RAS}$-Only Refresh Timing

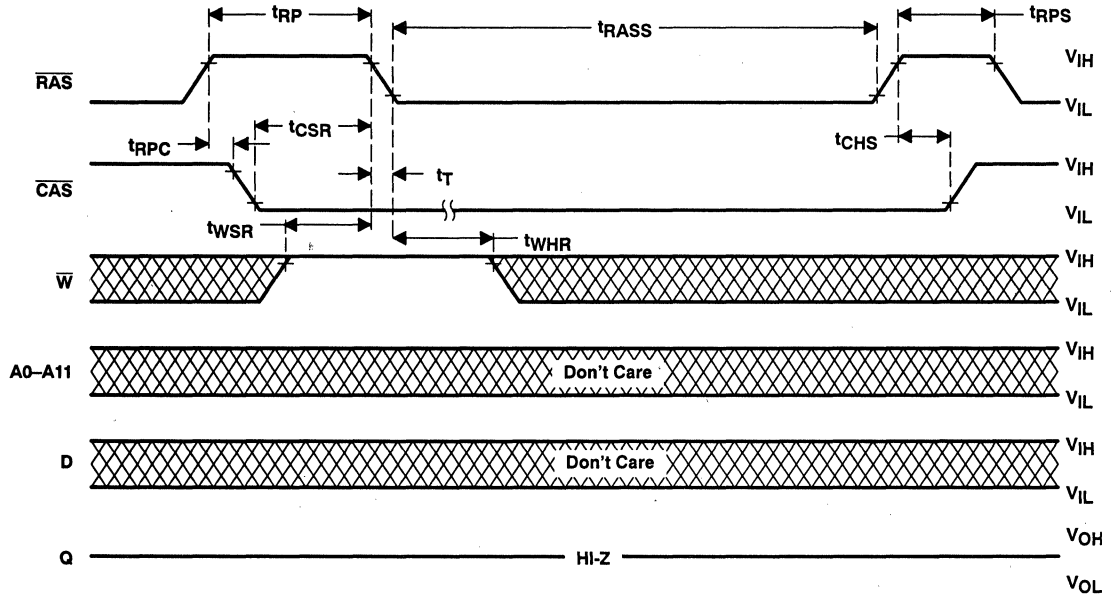

Figure 11. Self Refresh Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

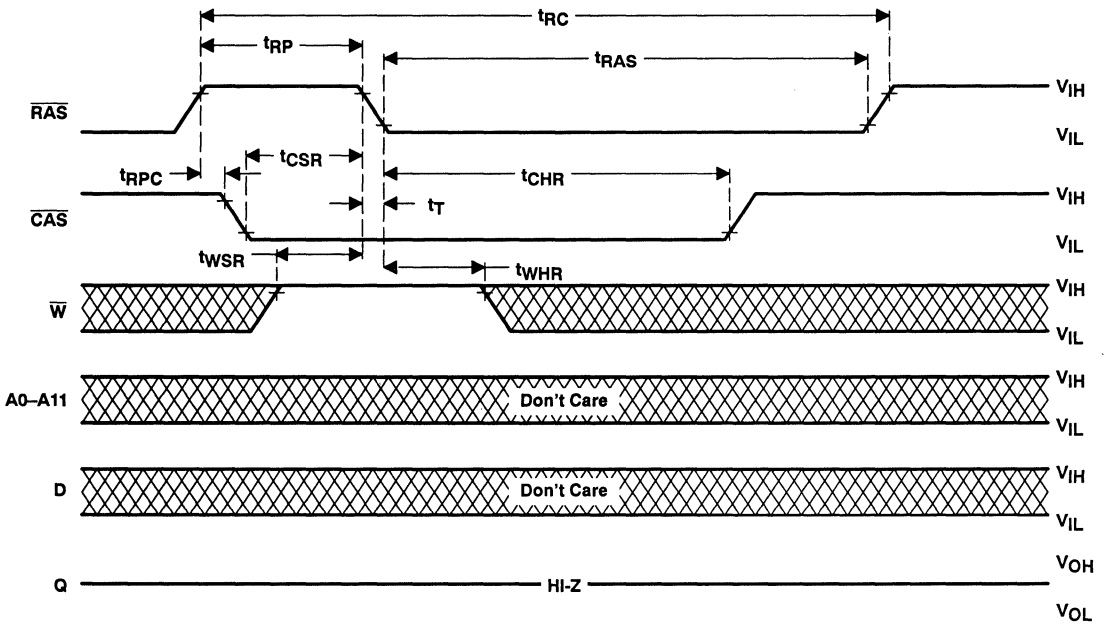

Figure 12. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

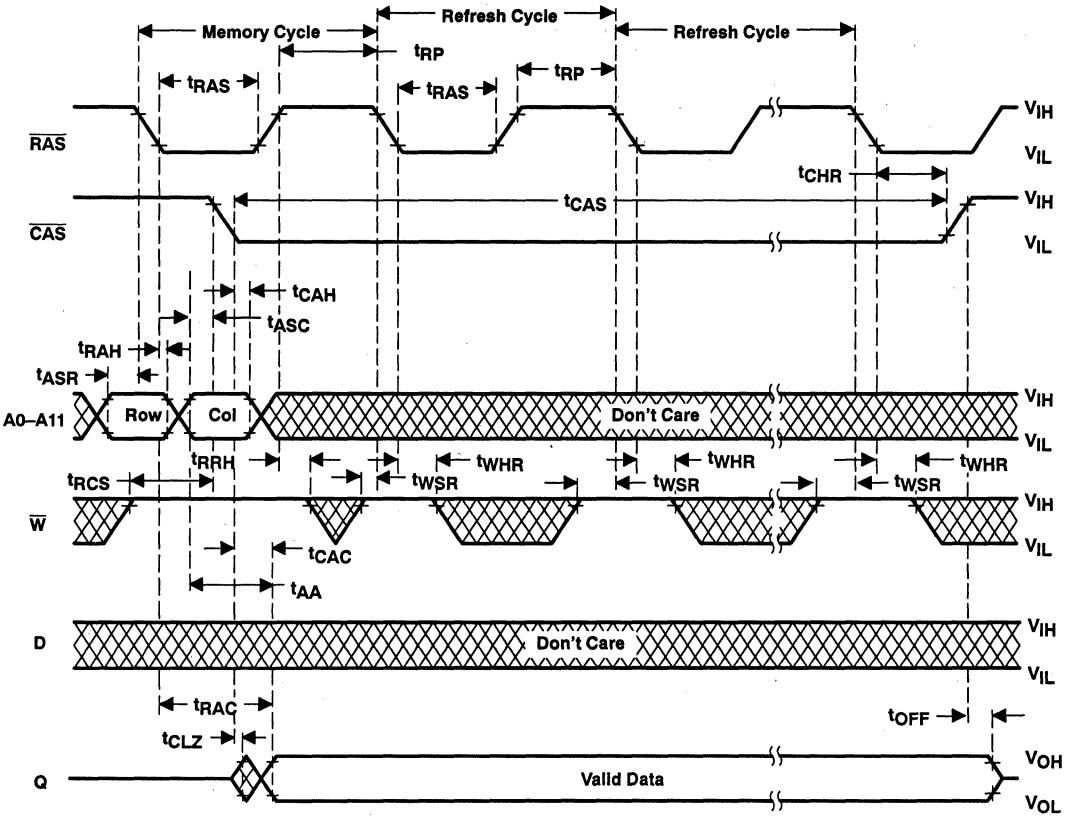

Figure 13. Hidden Refresh Cycle (Read)

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PARAMETER MEASUREMENT INFORMATION

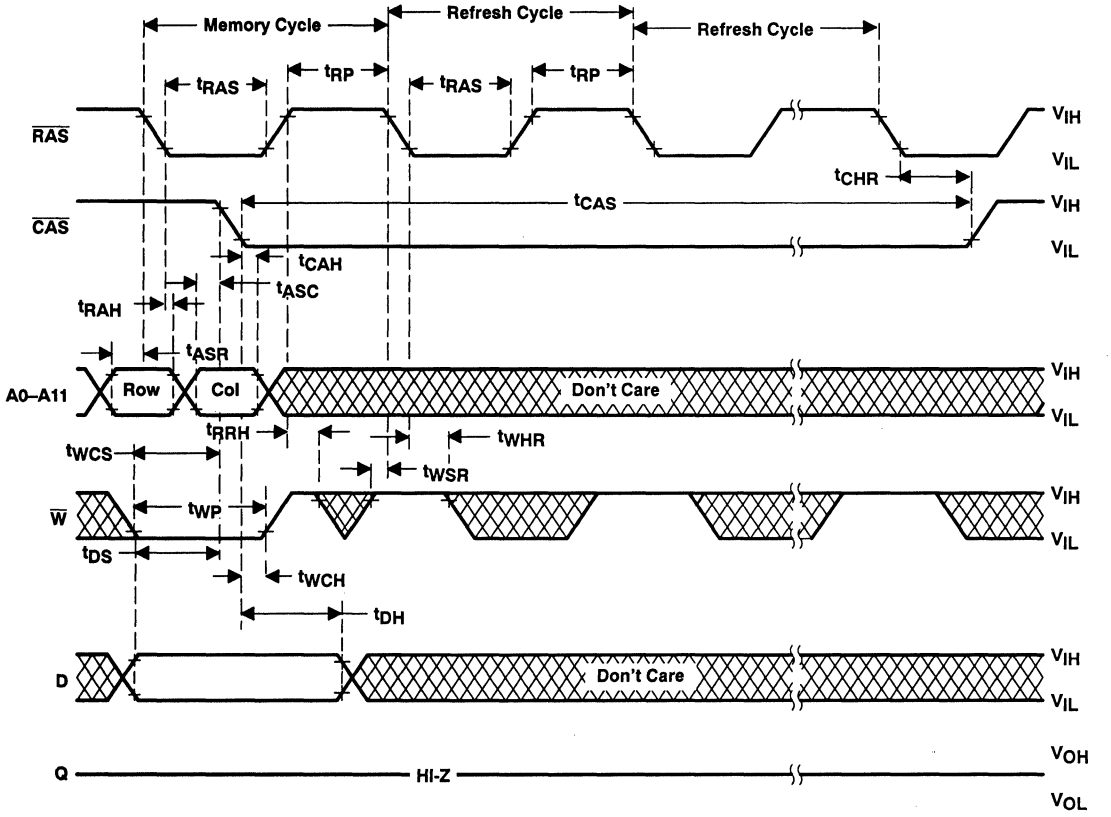

Figure 14. Hidden Refresh Cycle (Write)

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PARAMETER MEASUREMENT INFORMATION

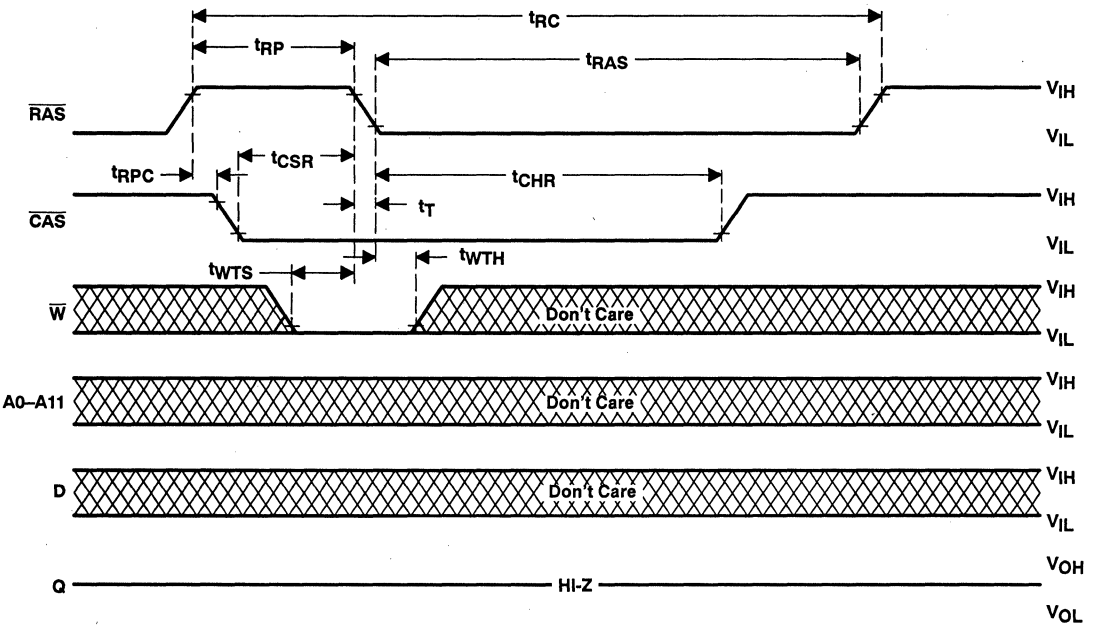


Figure 15. Test Mode Entry Cycle

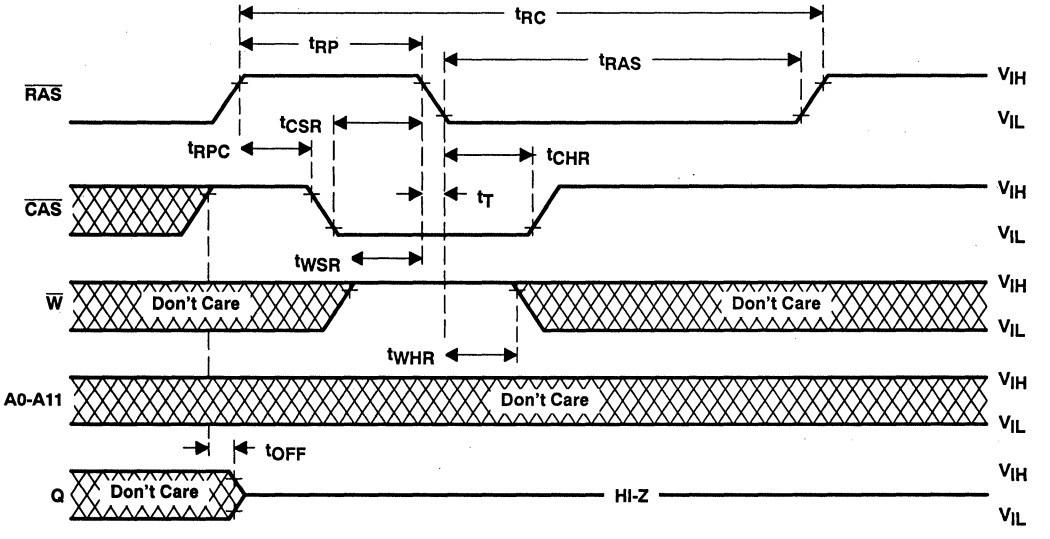
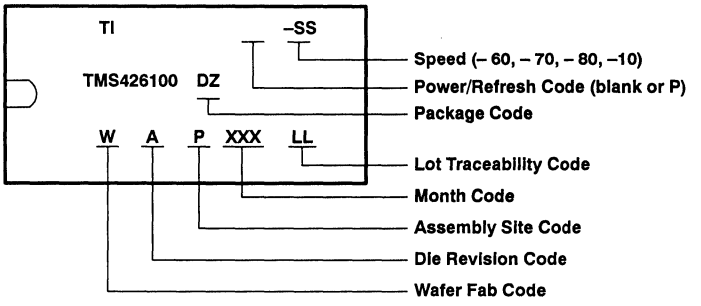


Figure 16. Test Mode Exit Cycle ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)

PRODUCT PREVIEW

device symbolization



PRODUCT PREVIEW

TEXAS INSTRUMENTS
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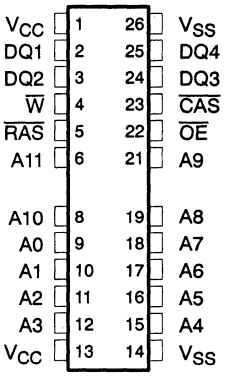
- **Organization . . . 4 194 304 × 4**
- **Single 3.3-V Power Supply (± 0.3 V Tolerance)**
- **Low Power Dissipation (TMS426400P)**
  - **100 μA CMOS Standby**
  - **100 μA Self-Refresh**
  - **100 μA Extended Refresh Battery Backup**
- **Performance Ranges:**

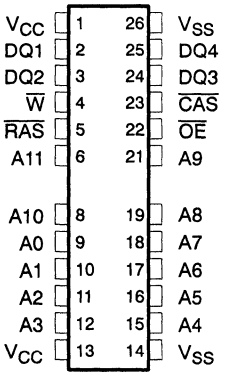
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'426400/P-60	60 ns	15 ns	30 ns	110 ns
'426400/P-70	70 ns	18 ns	35 ns	130 ns
'426400/P-80	80 ns	20 ns	40 ns	150 ns
'426400/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period**
  - **4096 Cycle Refresh in 64 ms**
  - **512 ms Max for Low-Power, Self-Refresh Version (TMS426400P)**
- **3-State Unlatched Output**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

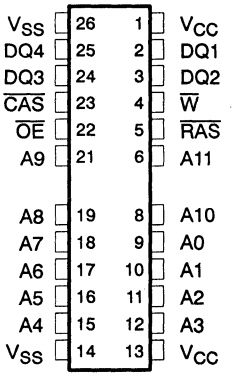
DJ PACKAGE† (TOP VIEW)



DGA PACKAGE† (TOP VIEW)



DGB PACKAGE† (TOP VIEW)



† Packages shown are for pinout reference only.

PRODUCT PREVIEW

description

The TMS426400 series are high-speed, low-voltage 16 777 216-bit dynamic random-access memories, organized as 4 194 304-bit words by four bits each. The TMS426400P series are high-speed, low-voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 4 194 304-bit words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low voltage at a low cost.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 180 mW operating, 0.36 mW standby and battery backup for an 80-ns device.

All inputs, outputs, and clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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The TMS426400 family is offered in a 300-mil 24/26-lead plastic surface mount SOJ package (DJ suffix), a 24/26-lead plastic small outline package (DGA suffix), and a 24/26-lead plastic small outline package, reverse form (DGB suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The column address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS426400 family to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAS} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the row address strobe, $\overline{RAS}$. Ten column-address bits are set on A0 through A9. Column addresses A10 and A11 are not used. Row address A11 is required during a normal access and during $\overline{RAS}$-only refresh, as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable input, $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain for the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 64 ms (512 ms for TMS426400P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS426400P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self-refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

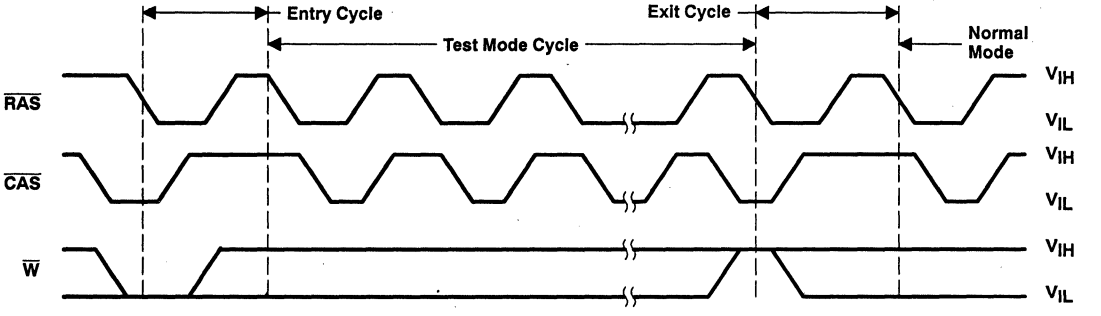
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

The part is configured as 1024K × 4 × 4 bit device in test mode, where each DQ pin has a separate 4-bit parallel read and write data bus where column addresses A0 and A1 are ignored. During a read cycle, the four internal bits are compared for each DQ pin separately. If the four bits agree, the DQ pin will go high; if not, the DQ pin will go low. All four bits are written to the state of their respective DQ pin during a parallel write. Thus, each DQ pin is independent of the others, and any data pattern desired may be written on each DQ pin. Test time is thus reduced by a factor of 4 for this series.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

Figure 1. Test Mode Cycle†

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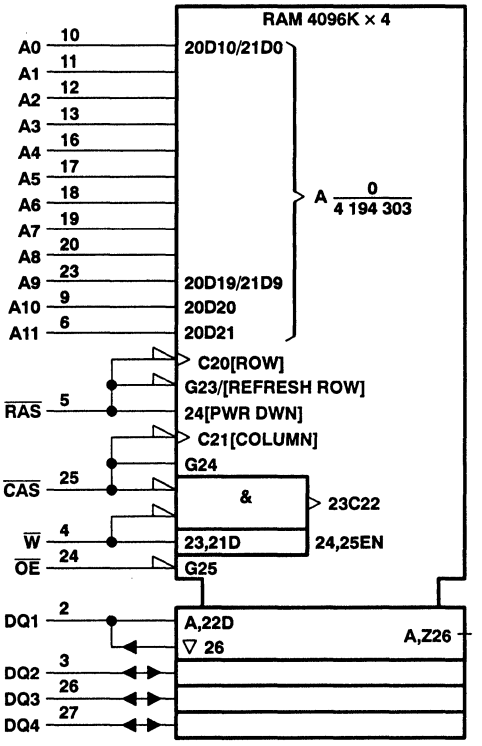
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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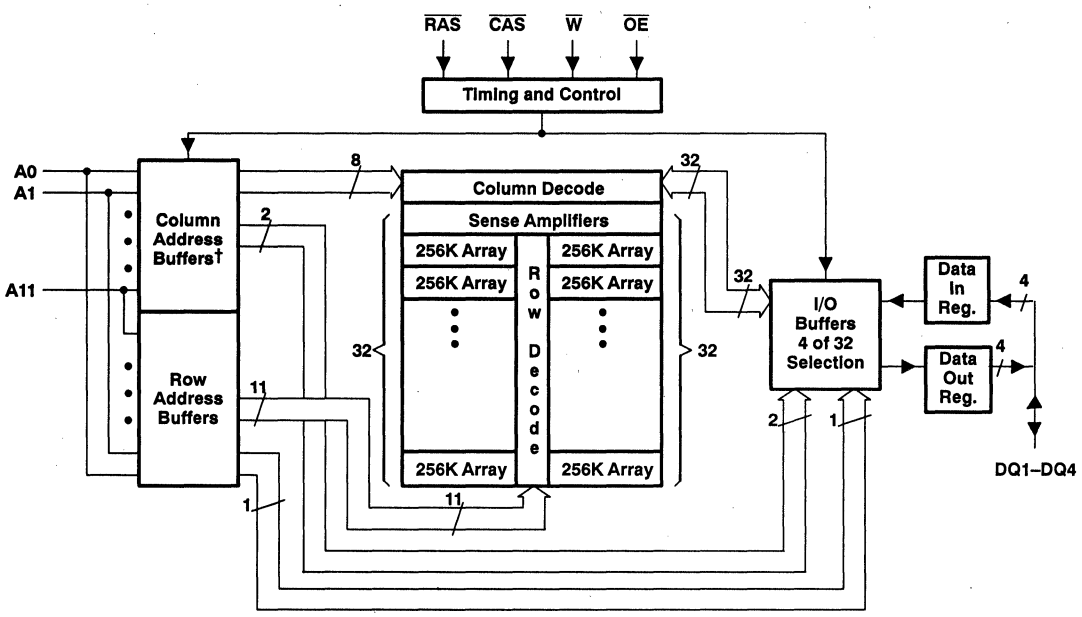
functional block diagram



† Column Address 10 and Column Address 11 are not used.

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absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... – 0.5 V to 4.6 V
Voltage range on V_{CC} ..... – 0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS426400-60 TMS426400P-60		TMS426400-70 TMS426400P-70		TMS426400-80 TMS426400P-80		TMS426400-10 TMS426400P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC} – 0.2		V_{CC} – 0.2		V_{CC} – 0.2		V_{CC} – 0.2		V
V_{OL}	Option	I_{OL} = + 100 µA			0.2		0.2		0.2		0.2	
I_I	Input current (leakage)‡	V_I = 0 to 3.9 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Notes 3 & 5)	Minimum cycle, V_{CC} = 3.6 V			70		60		50		40	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.0 V (LVTTL)			1		1		1		1	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'426400		300		300		300		300	µA
			'426400P		100		100		100		100	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 & 5)†	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50		40	mA
I_{CC4}	Average page current (see Notes 4 & 5)†	$\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40		35	mA
I_{CC6}‡	Self-refresh	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			100		100		100		100	µA
I_{CC7}	Standby current output enable (see Note 5)†	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5		5	mA
I_{CC10}‡	Battery backup (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100		100		100	µA

† Minimum cycle, V_{CC} = 3.6 V.
‡ For TMS426400P only.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.
5. I_{CC} max is specified with no load connected.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 6: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS426400-60 TMS426400P-60		TMS426400-70 TMS426400P-70		TMS426400-80 TMS426400P-80		TMS426400-10 TMS426400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OHO}	Output disable time start of $\overline{OE}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	0	25	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS426400-60 TMS426400P-60		TMS426400-70 TMS426400P-70		TMS426400-80 TMS426400P-80		TMS426400-10 TMS426400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 8)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{RASS}	Self-refresh, $\overline{RAS}$ low time		100		100		100		100	µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RPS}	$\overline{RAS}$ precharge after self-refresh	110		130		150		180		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 12)	0		0		0		0		ns
t_{RCS}	Read setup before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test-mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		5		ns

Continued next page.

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS426400-60 TMS426400P-60		TMS426400-70 TMS426400P-70		TMS426400-80 TMS426400P-80		TMS426400-10 TMS426400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	−50		−50		−50		−50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		135		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		85		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval (TMS426400)		64		64		64		64	ms
t_{REF}	Refresh time internal (TMS426400P)		512		512		512		512	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

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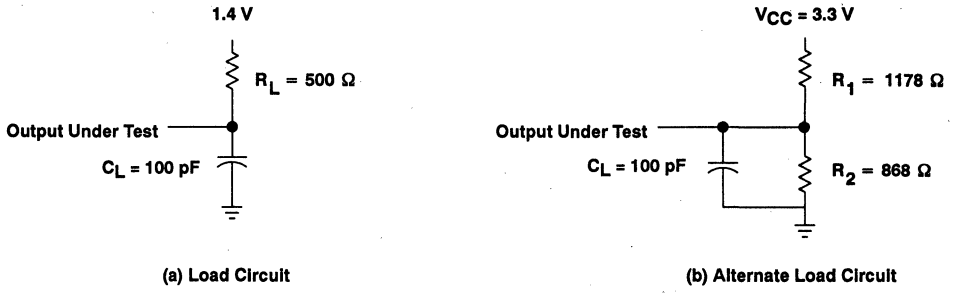
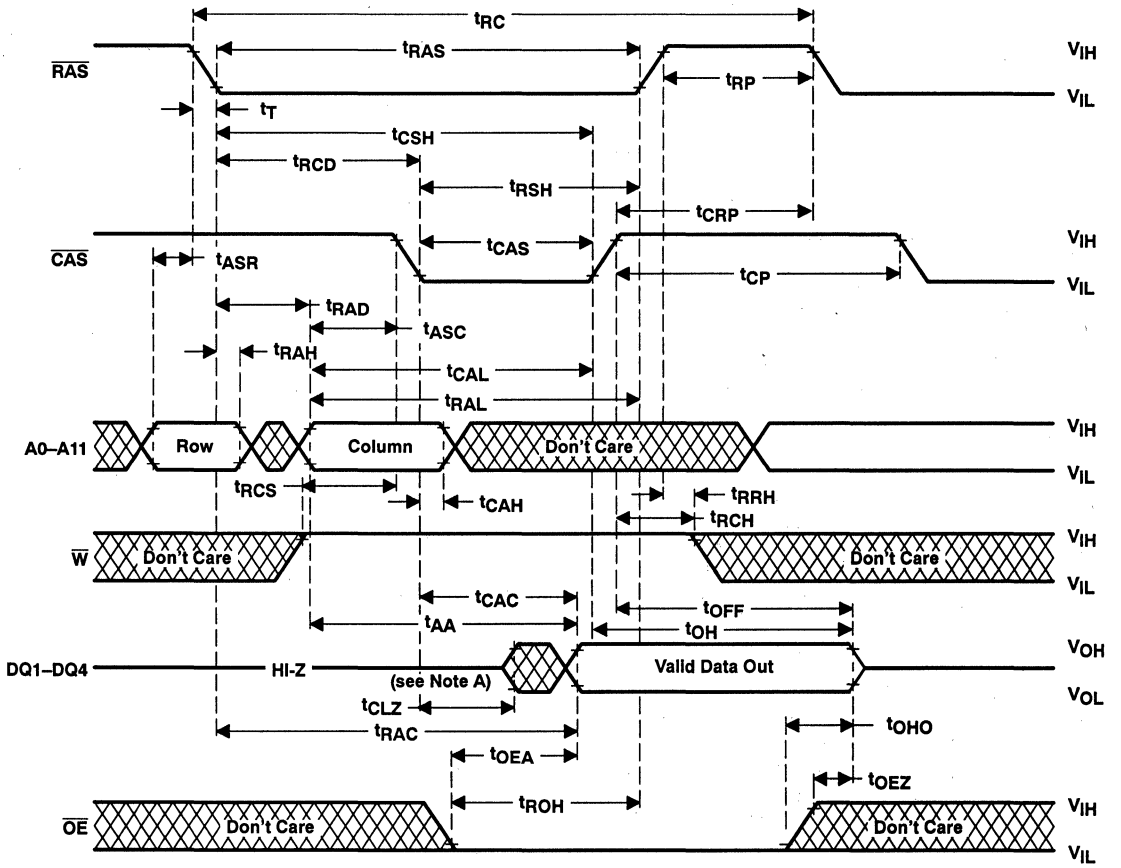
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 2. Load Circuits for Timing Parameters



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

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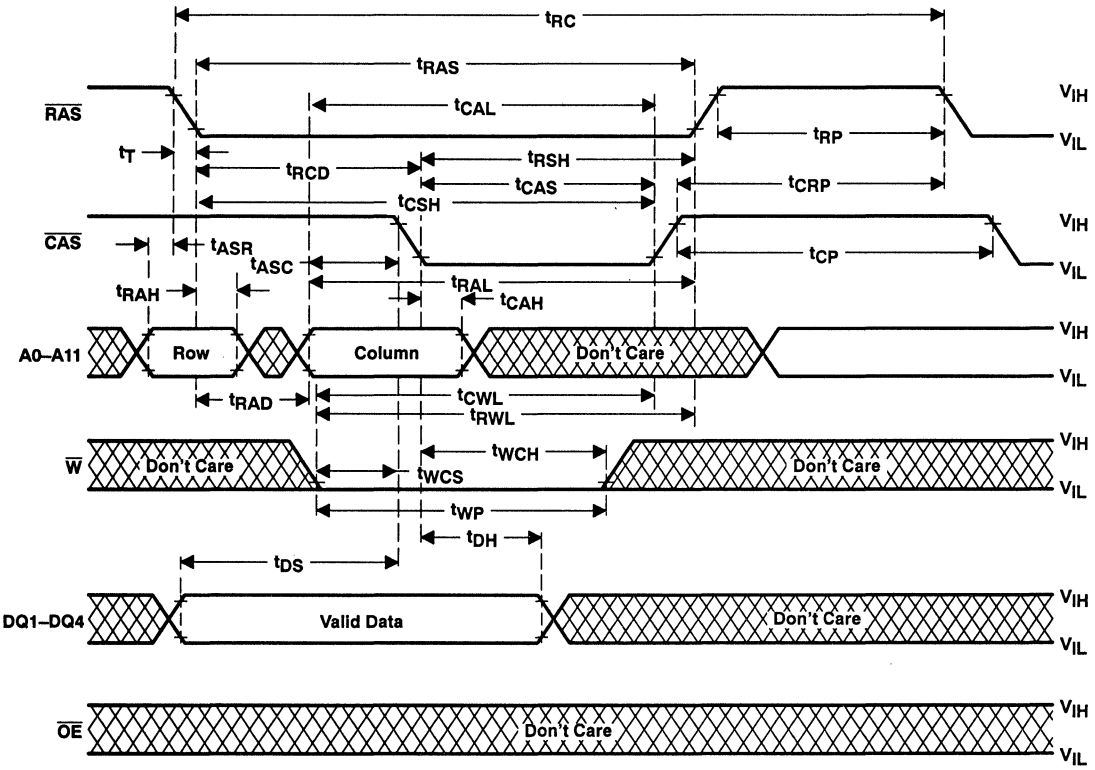

Figure 4. Early Write Cycle Timing

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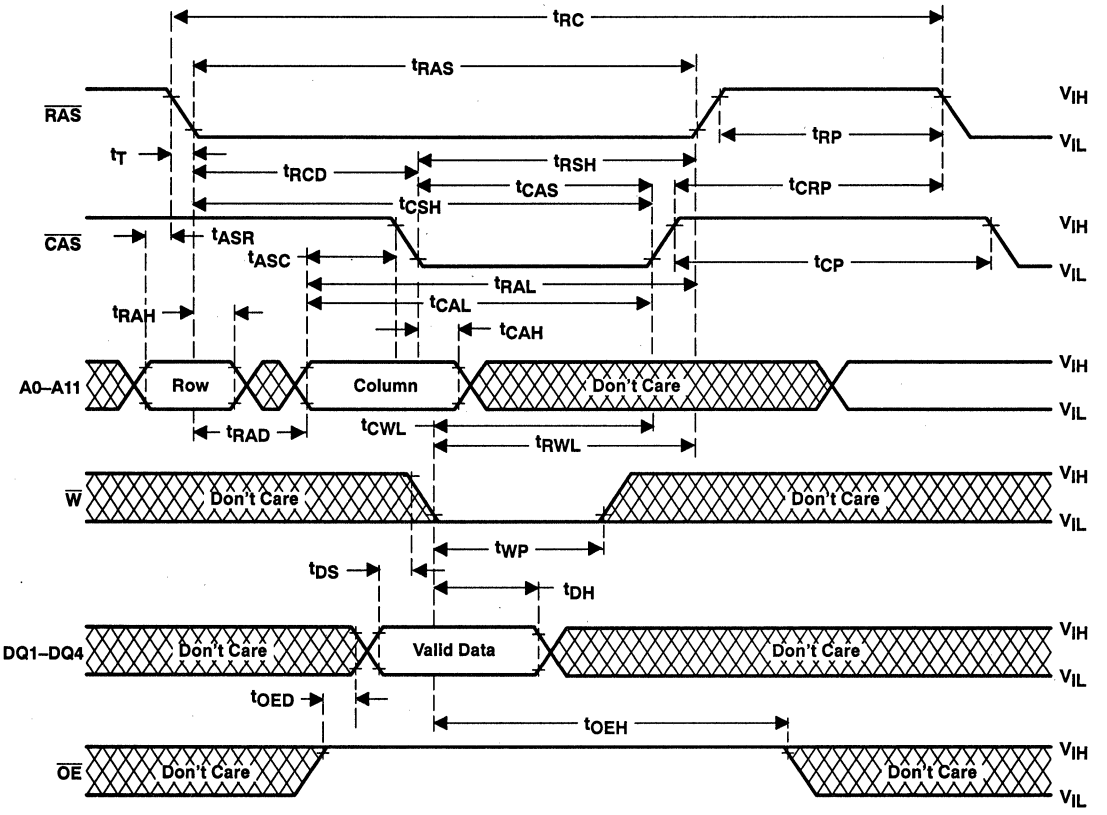
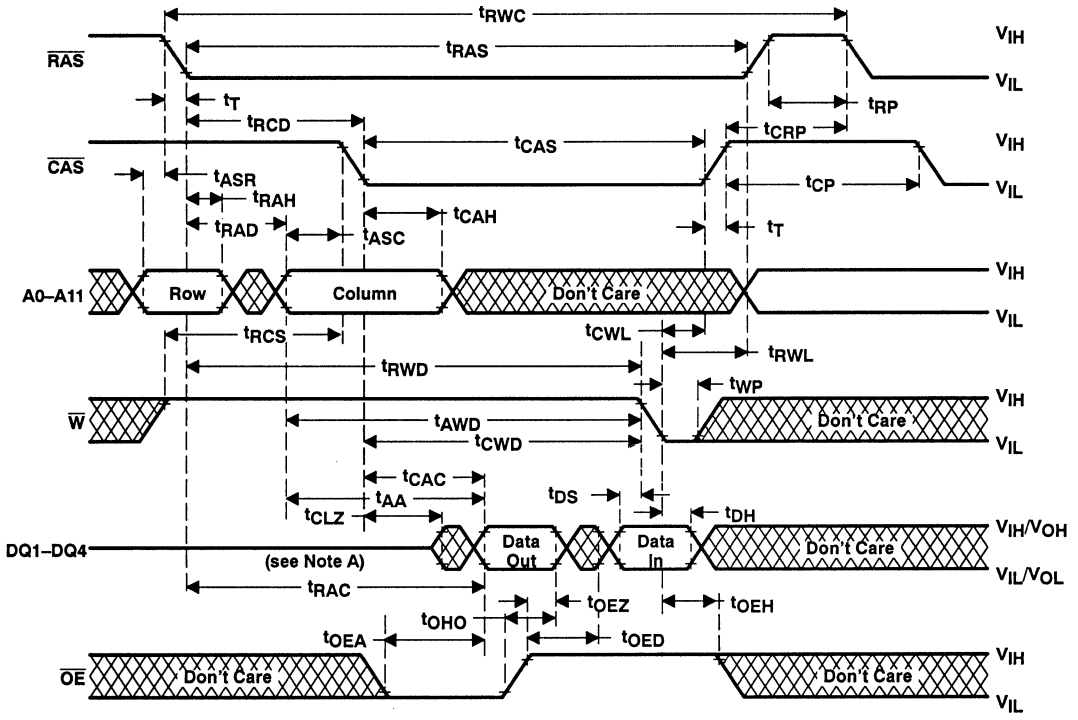


Figure 5. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

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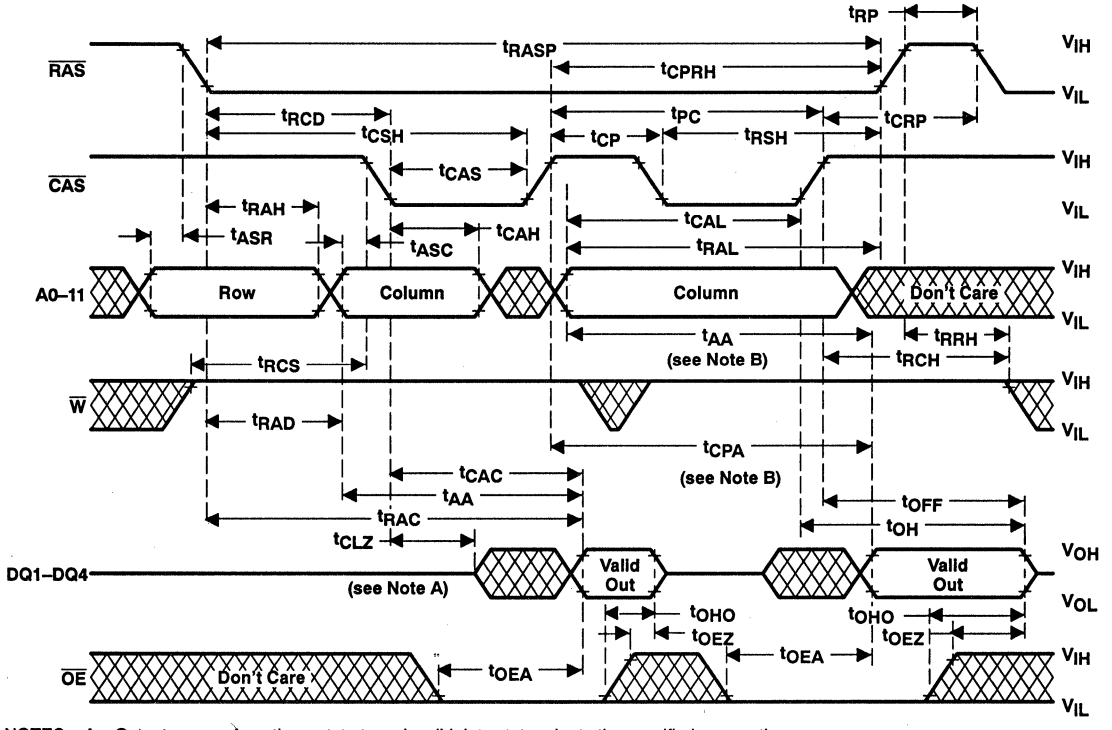
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

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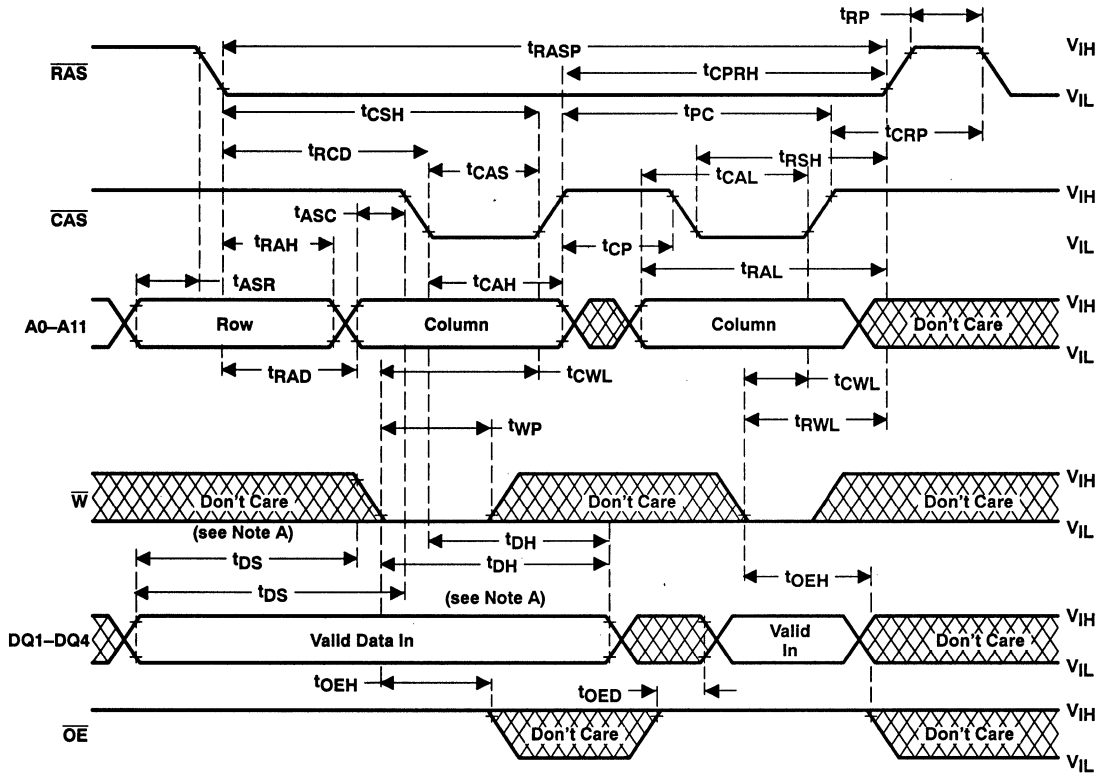
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

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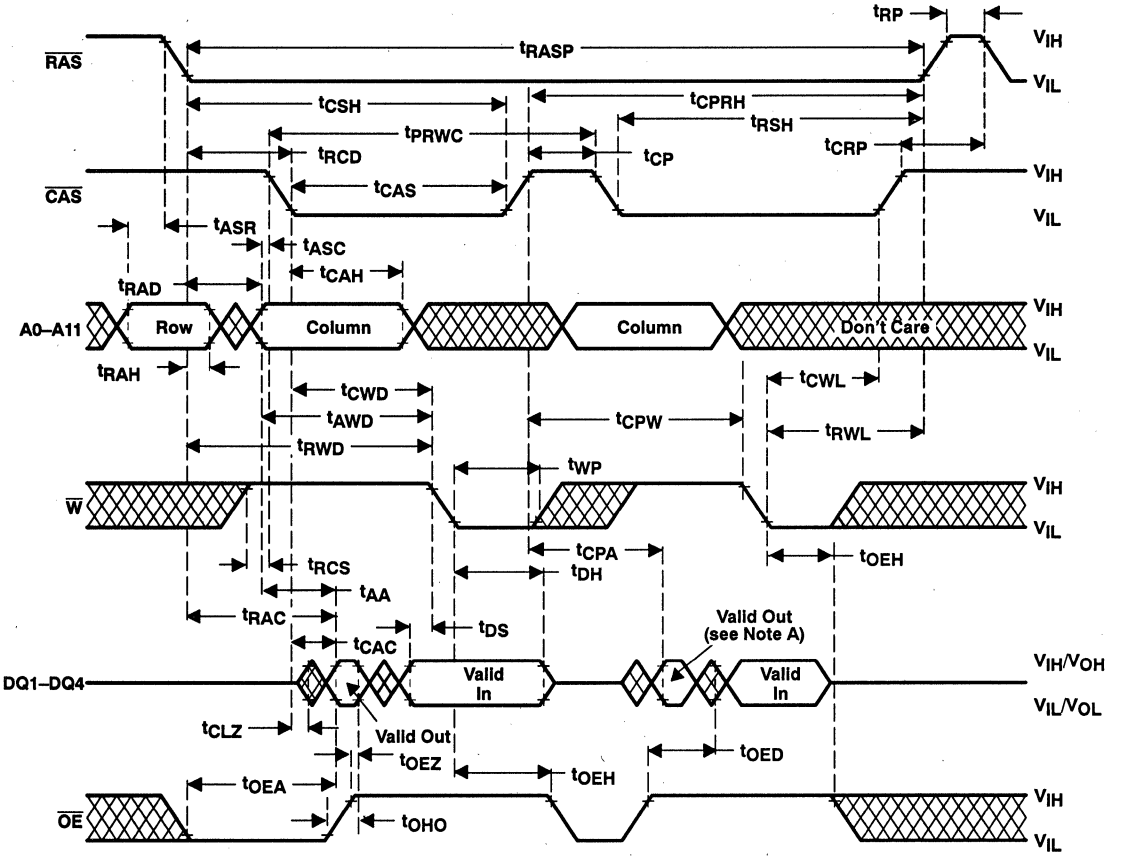
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

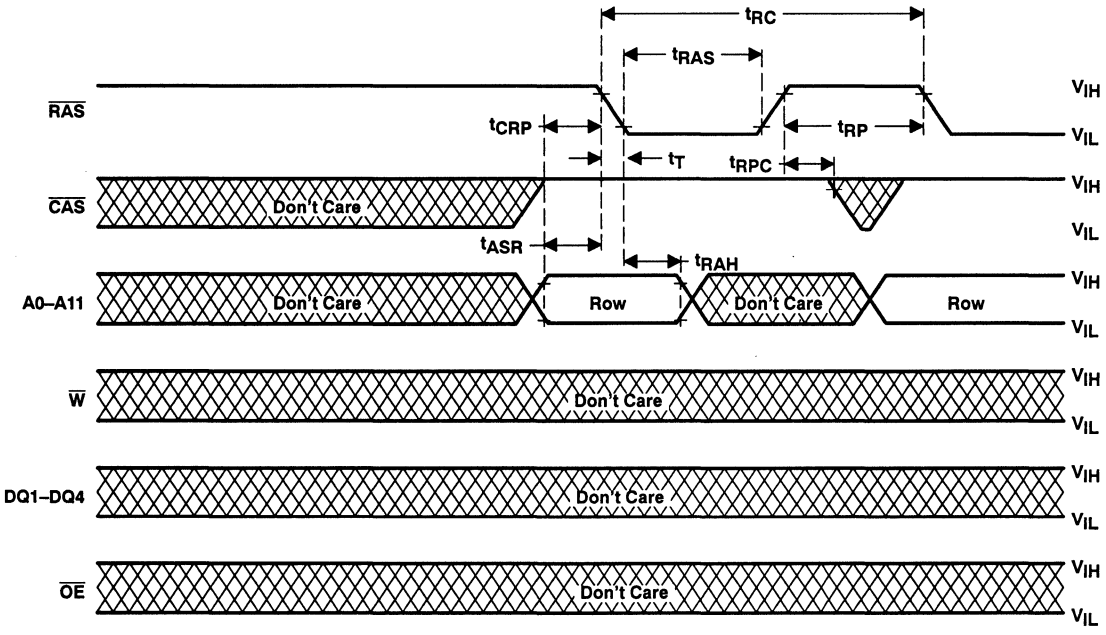

Figure 10. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

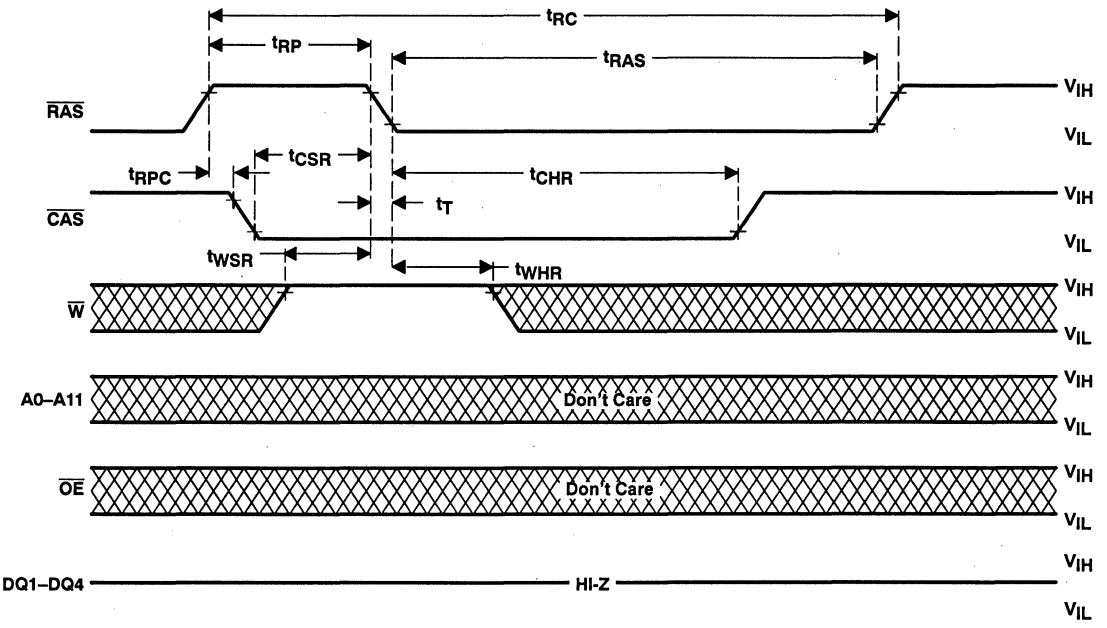

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

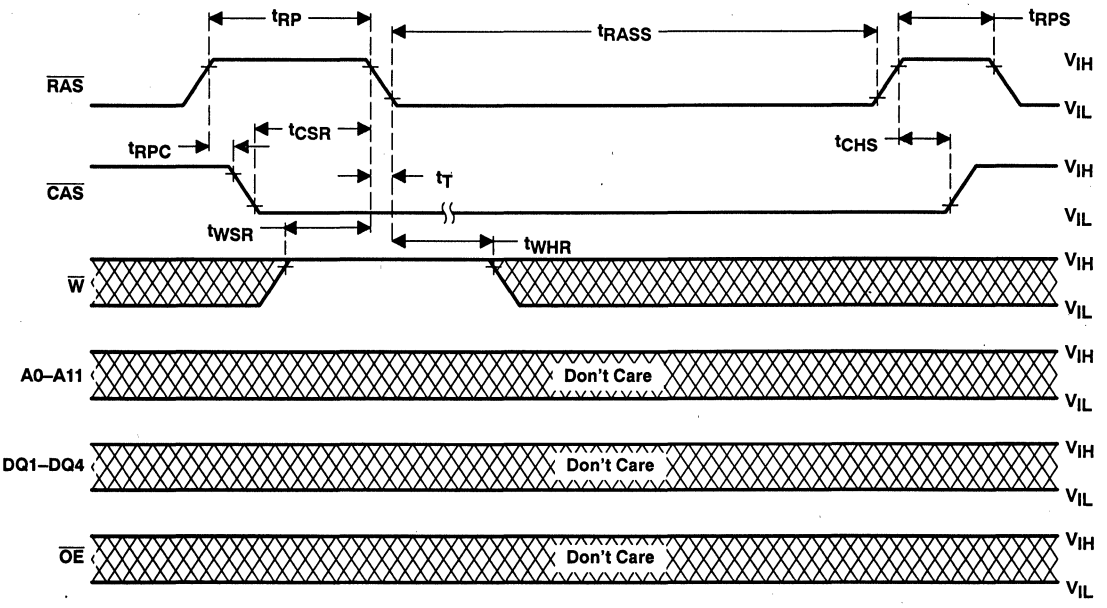

Figure 12. Self Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

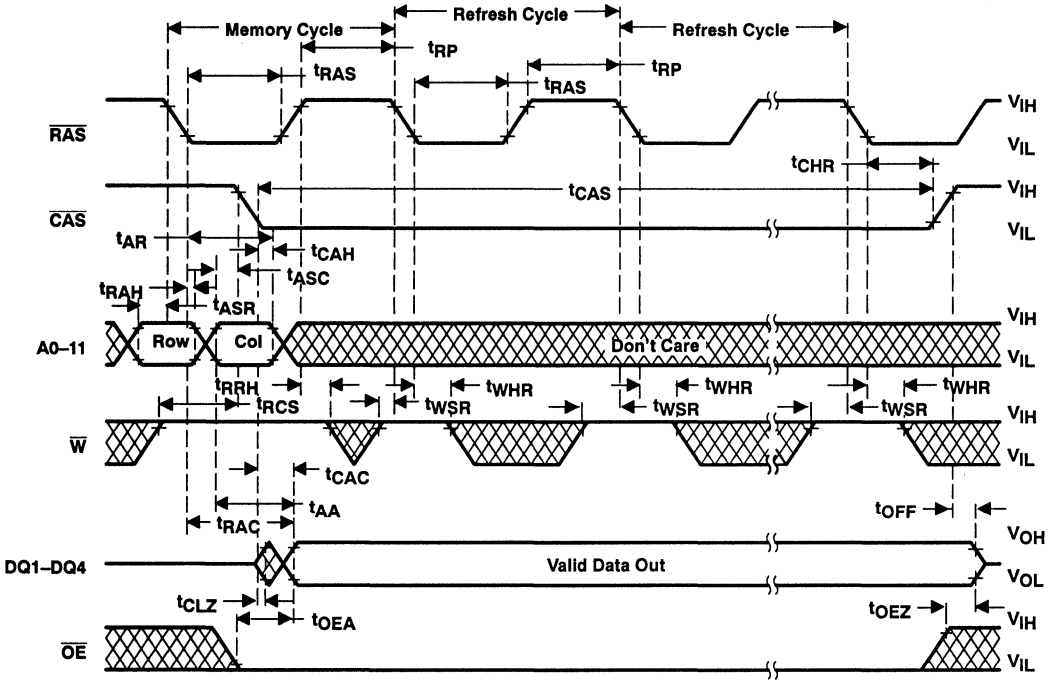

Figure 13. Hidden Refresh Cycle (Read)

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PARAMETER MEASUREMENT INFORMATION

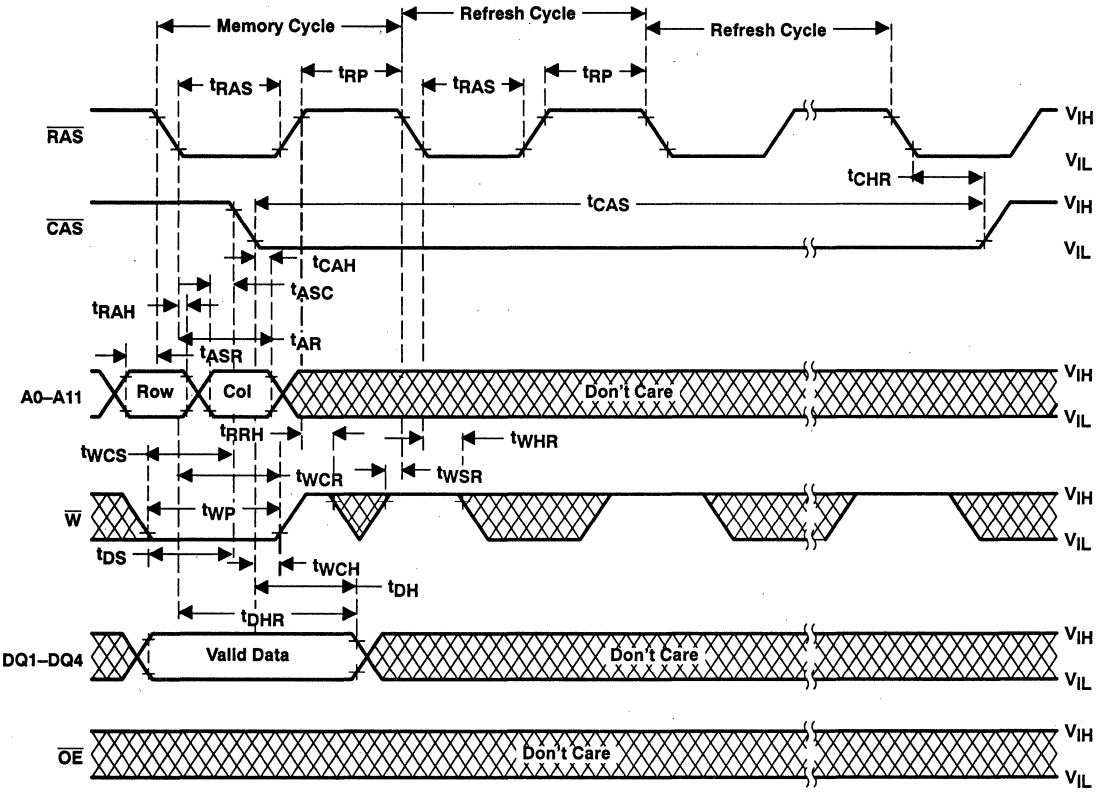

Figure 14. Hidden Refresh Cycle (Write)

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PARAMETER MEASUREMENT INFORMATION

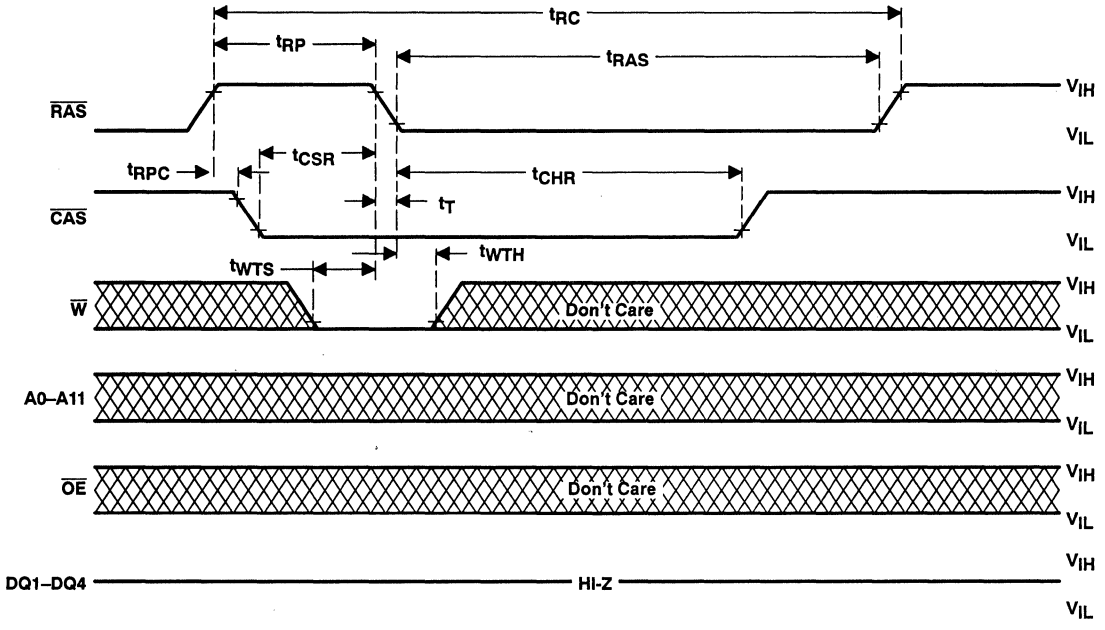

Figure 15. Test Mode Entry Cycle

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PARAMETER MEASUREMENT INFORMATION

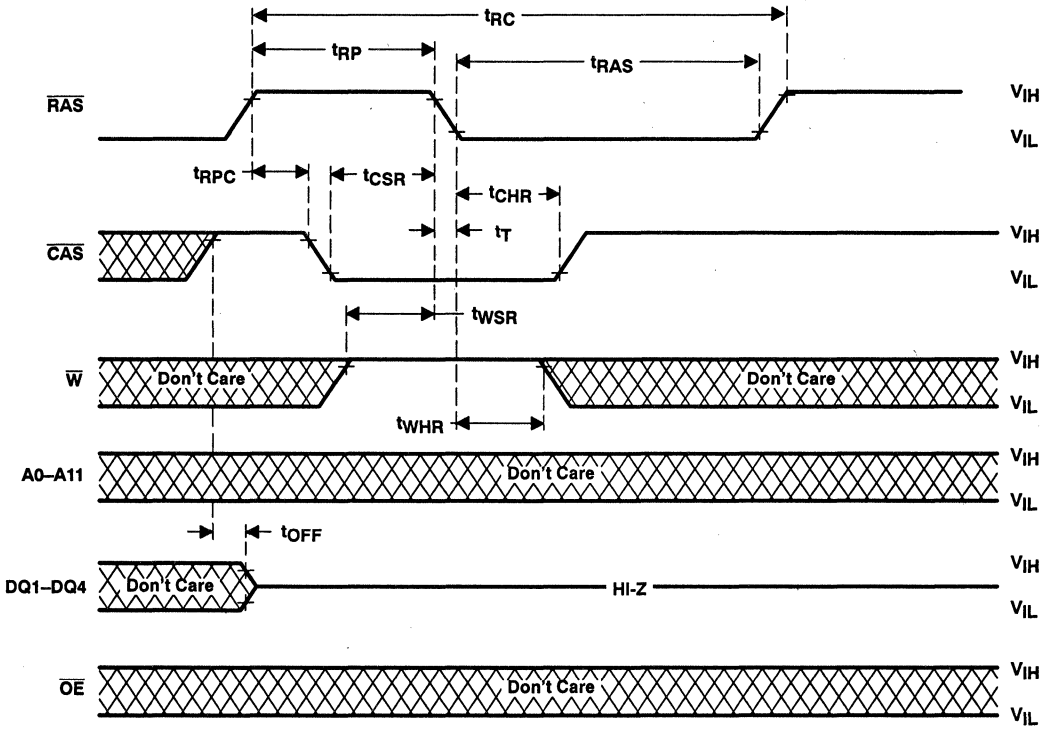
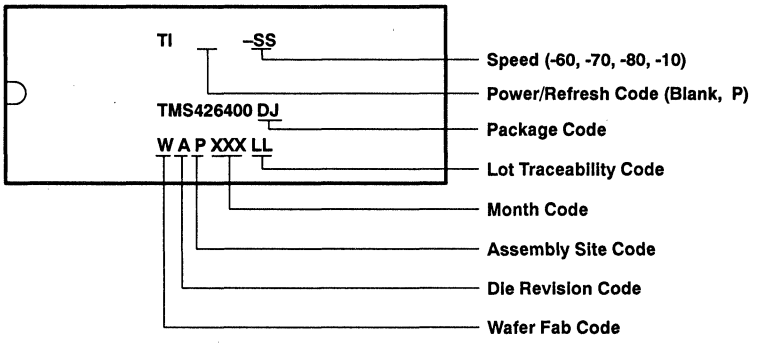


Figure 16. Test Mode Exit Cycle ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)

device symbolization



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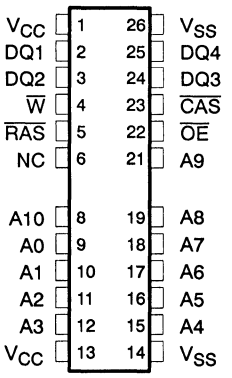
- **Organization . . . 4 194 304 × 4**
- **Single 3.3-V Power Supply (± 0.3 V Tolerance)**
- **Low Power Dissipation (TMS427400P)**
  - **100 μA CMOS Standby**
  - **100 μA Self-Refresh**
  - **100 μA Extended Refresh Battery Backup**
- **Performance Ranges:**

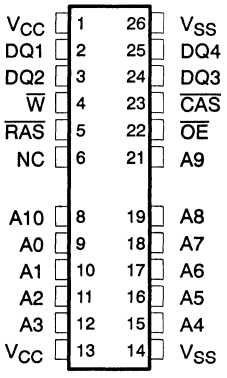
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
'427400/P-60	60 ns	15 ns	30 ns	110 ns
'427400/P-70	70 ns	18 ns	35 ns	130 ns
'427400/P-80	80 ns	20 ns	40 ns	150 ns
'427400/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period**
  - **2048 Cycle Refresh in 32 ms**
  - **256 ms Max for Low-Power, Self-Refresh Version (TMS427400P)**
- **3-State Unlatched Output**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range 0°C to 70°C**

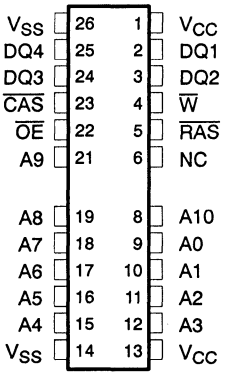
DJ PACKAGE† (TOP VIEW)



DGA PACKAGE† (TOP VIEW)



DGB PACKAGE† (TOP VIEW)



† Packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

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description

The TMS427400 series are high-speed, low-voltage 16 777 216-bit dynamic random-access memories, organized as 4 194 304-bit words by four bits each. The TMS427400P series are high-speed, low-voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 4 194 304-bit words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low voltage at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 288 mW operating, 0.36 mW standby and battery backup for an 80-ns device.

All inputs, outputs, and clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The TMS427400 family is offered in a 300-mil 24/26-lead plastic surface mount SOJ package (DJ suffix), a 24/26-lead plastic small outline package (DGA suffix), and a 24/26-lead plastic small outline package, reverse form (DGB suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The column address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the TMS427400 family to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAS} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set on inputs A0 through A10 and latched onto the chip by the row address strobe, $\overline{RAS}$. Eleven column-address bits are set on A0 through A10. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable input, $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain for the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 32 ms (256 ms for TMS427400P) to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS427400P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self-refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This will ensure the DRAM is fully refreshed.

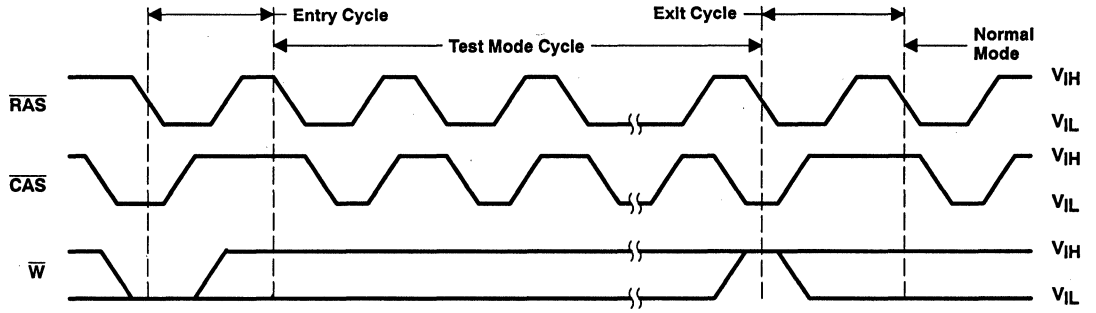
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

The test mode is initiated with a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle while simultaneously holding the $\overline{W}$ input low (WCBR). The initiate cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in test mode, any desired data sequence can be performed on the device. The device exits test mode if a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle with $\overline{W}$ input held high, or a $\overline{RAS}$-only refresh (ROR) cycle is performed.

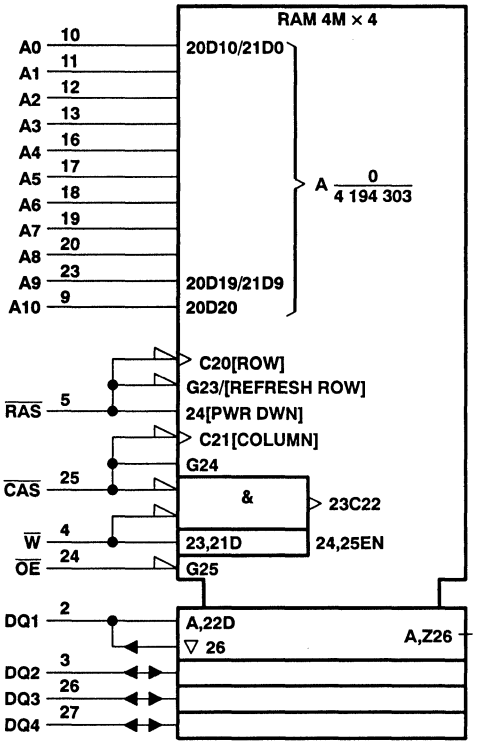
The part is configured as 1M × 4 × 4 bit device in test mode, where each DQ pin has a separate 4-bit parallel read and write data bus where column addresses A0 and A1 are ignored. During a read cycle, the four internal bits are compared for each DQ pin separately. If the four bits agree, the DQ pin will go high; if not, the DQ pin will go low. All four bits are written to the state of their respective DQ pin during a parallel write. Thus, each DQ pin is independent of the others, and any data pattern desired may be written on each DQ pin. Test time is thus reduced by a factor of 4 for this series.



† The states of $\overline{W}$, Data-in, and Address are defined by the type of cycle used during test mode.

Figure 1. Test Mode Cycle†

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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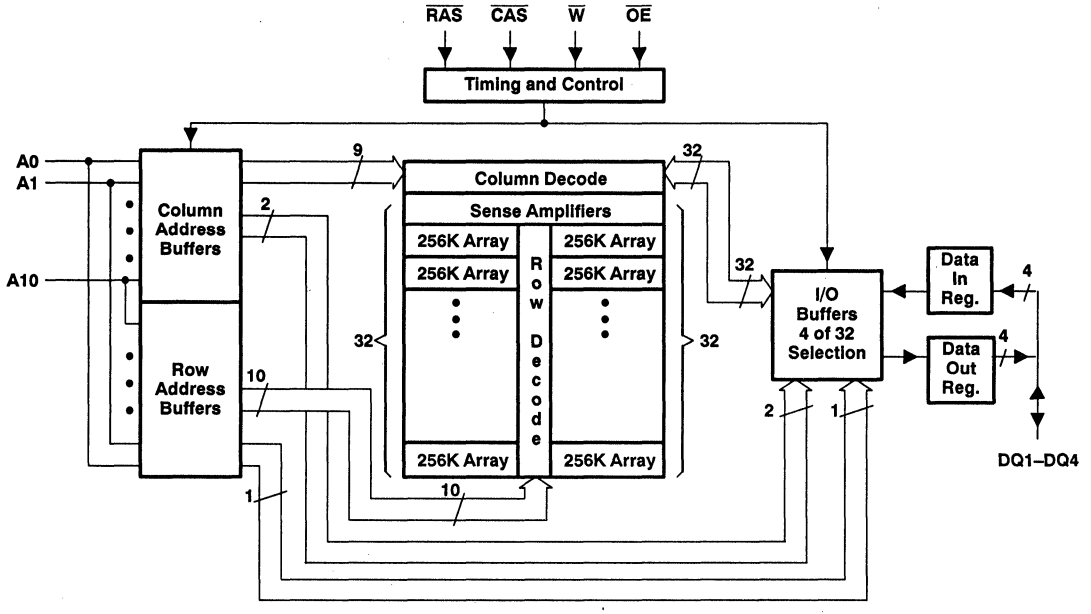
functional block diagram



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absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... −0.5 V to 4.6 V
Voltage range on V_{CC} ..... −0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	−0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS427400-60 TMS427400P-60		TMS427400-70 TMS427400P-70		TMS427400-80 TMS427400P-80		TMS427400-10 TMS427400P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC} – 0.2		V_{CC} – 0.2		V_{CC} – 0.2		V_{CC} – 0.2		V
V_{OL}	Option	I_{OL} = + 100 µA			0.2		0.2		0.2		0.2	
I_I	Input current (leakage)‡	V_I = 0 to 3.9 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Notes 3 & 5)	Minimum cycle, V_{CC} = 3.6 V			100		90		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.0 V (LVTTL)			1		1		1		1	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'427400		300		300		300		300	µA
			'427400P		100		100		100		100	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Notes 3 & 5)†	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			100		90		80		70	mA
I_{CC4}	Average page current (see Notes 4 & 5)†	$\overline{RAS}$ low, $\overline{CAS}$ cycling			60		50		40		35	mA
I_{CC6}‡	Self-refresh	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			100		100		100		100	µA
I_{CC7}	Standby current output enable (see Note 5)†	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5		5	mA
I_{CC10}‡	Battery backup (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100		100		100	µA

† Minimum cycle, V_{CC} = 3.6 V.
‡ For TMS427400P only.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.
5. I_{CC} max is specified with no load connected.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 6: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS427400-60 TMS427400P-60		TMS427400-70 TMS427400P-70		TMS427400-80 TMS427400P-80		TMS427400-10 TMS427400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OHO}	Output disable time start of $\overline{OE}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 7)	0	15	0	18	0	20	0	25	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TMS427400-60 TMS427400P-60		TMS427400-70 TMS427400P-70		TMS427400-80 TMS427400P-80		TMS427400-10 TMS427400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 8)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 9)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{RASS}	Self-refresh, $\overline{RAS}$ low time		100		100		100		100	µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{RPS}	$\overline{RAS}$ precharge after self-refresh	110		130		150		180		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 12)	0		0		0		0		ns
t_{RCS}	Read setup before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTS}	$\overline{W}$-low setup time (test-mode only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	5		5		5		5		ns

Continued next page.

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

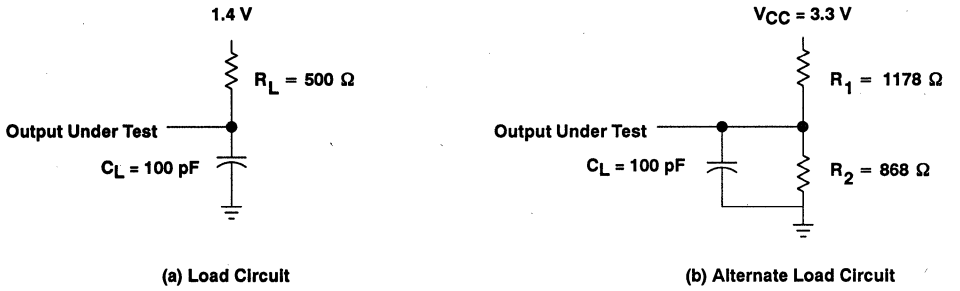
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TMS427400-60 TMS427400P-60		TMS427400-70 TMS427400P-70		TMS427400-80 TMS427400P-80		TMS427400-10 TMS427400P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	−50		−50		−50		−50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		135		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		85		ns
t_{TAA}	Access time from address (test mode)	35		40		45		50		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		55		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		105		ns
t_{REF}	Refresh time interval (TMS427400)		32		32		32		32	ms
t_{REF}	Refresh time internal (TMS427400P)		256		256		256		256	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

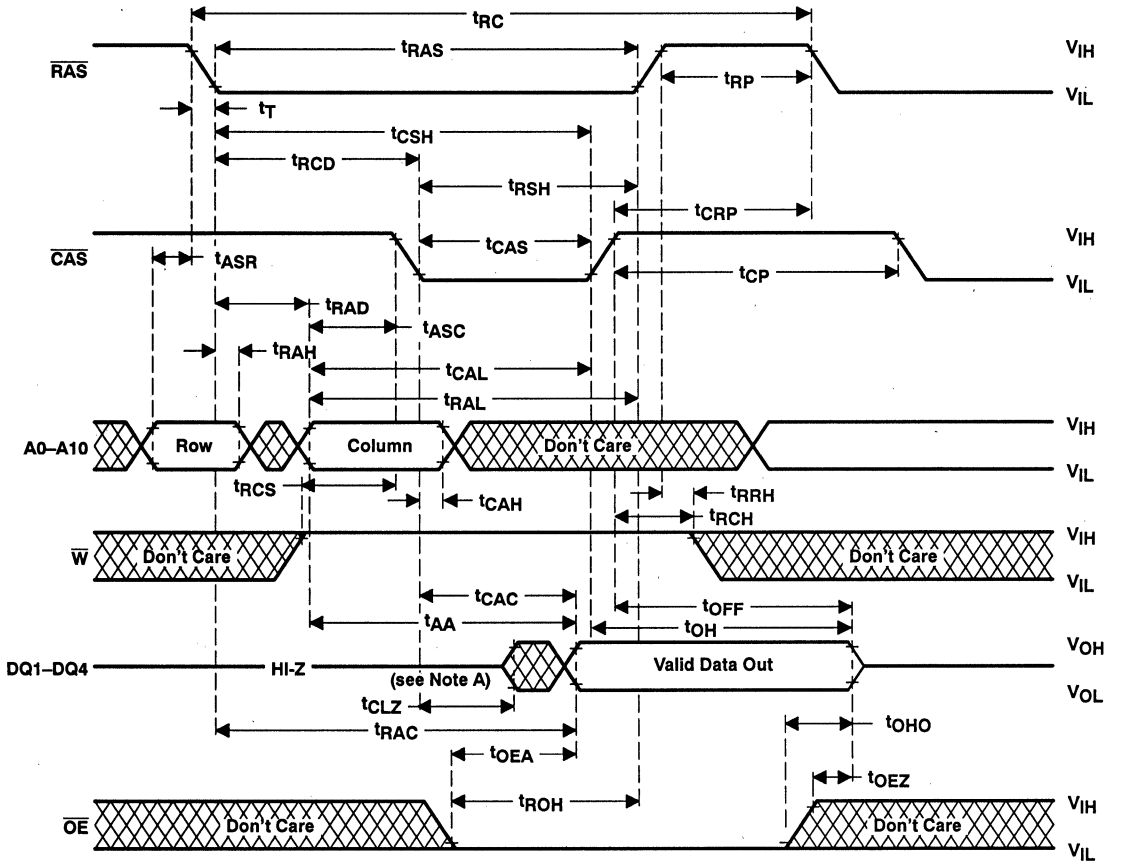
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 2. Load Circuits for Timing Parameters



NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 3. Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

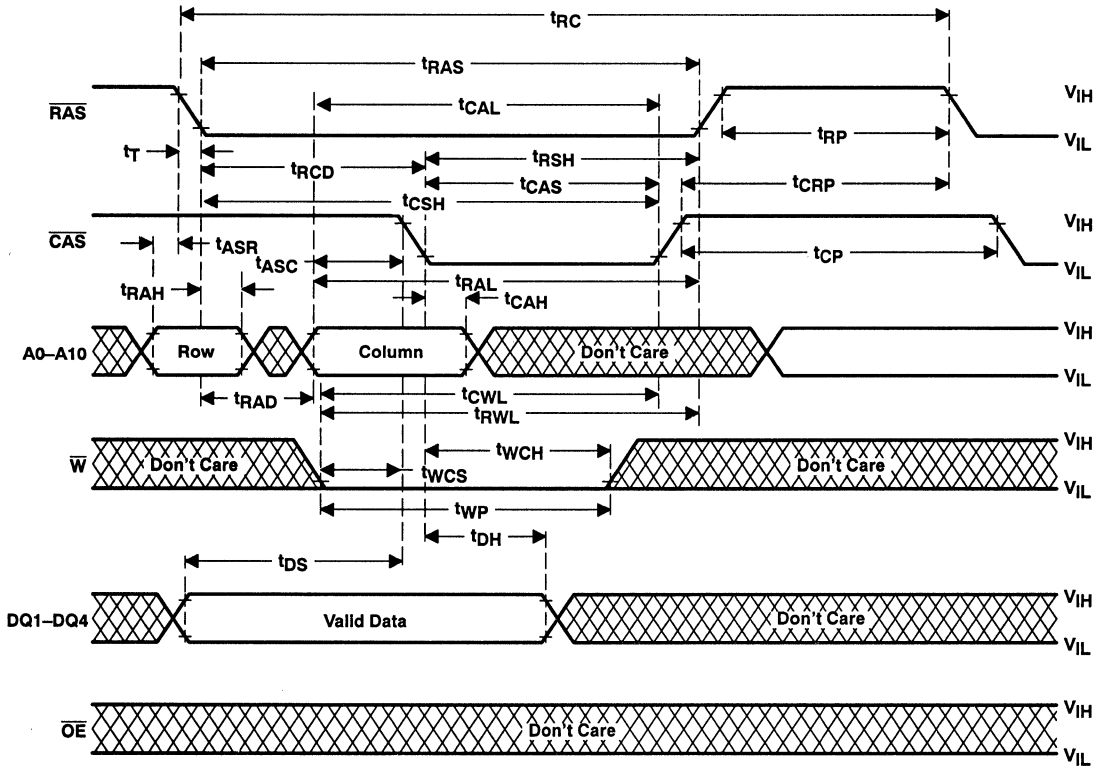


Figure 4. Early Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

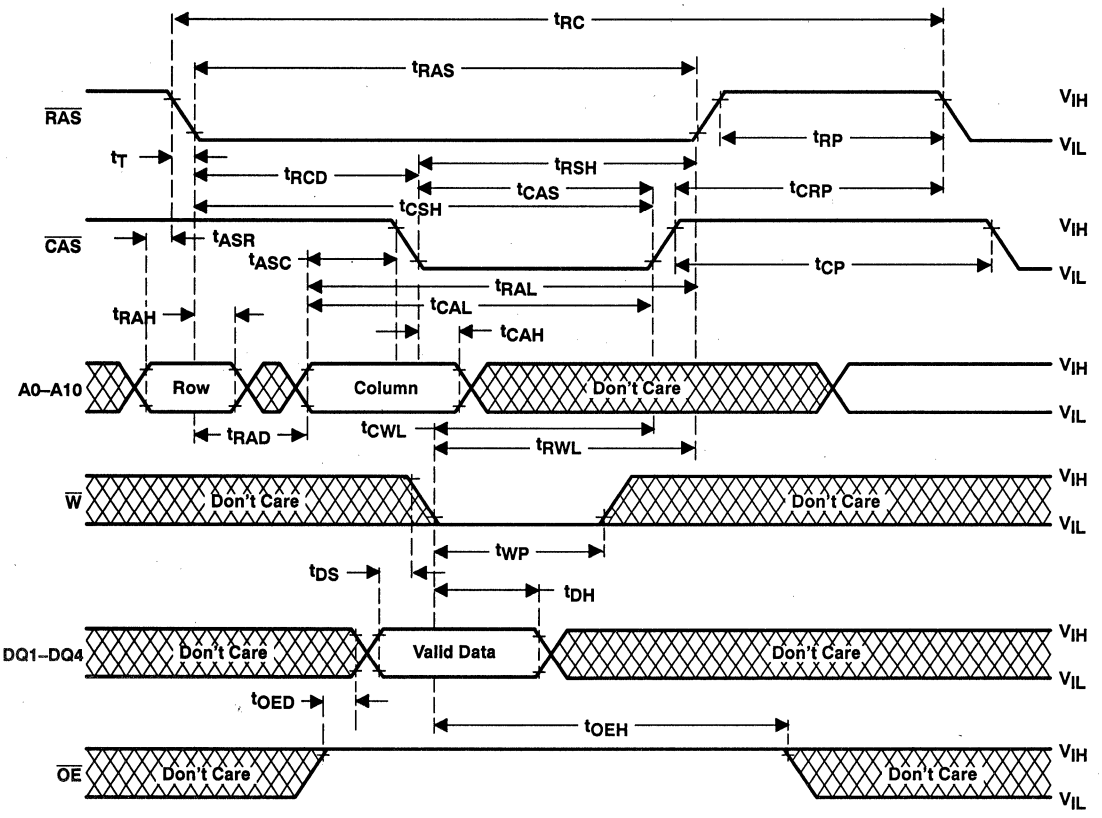


Figure 5. Write Cycle Timing

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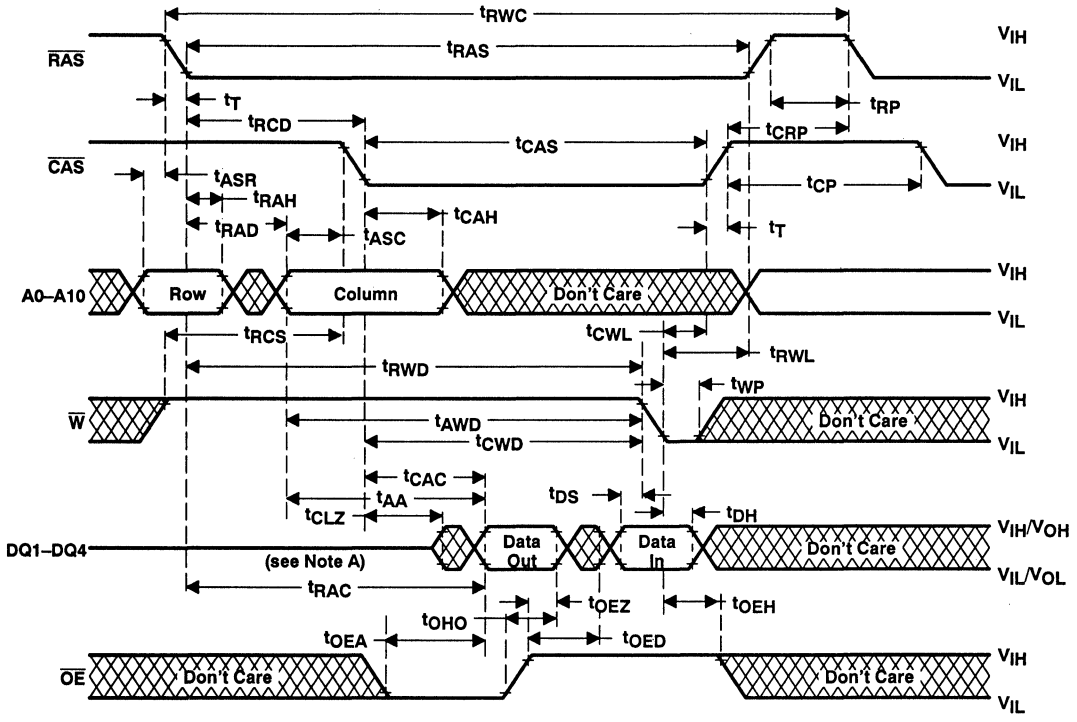
PARAMETER MEASUREMENT INFORMATION

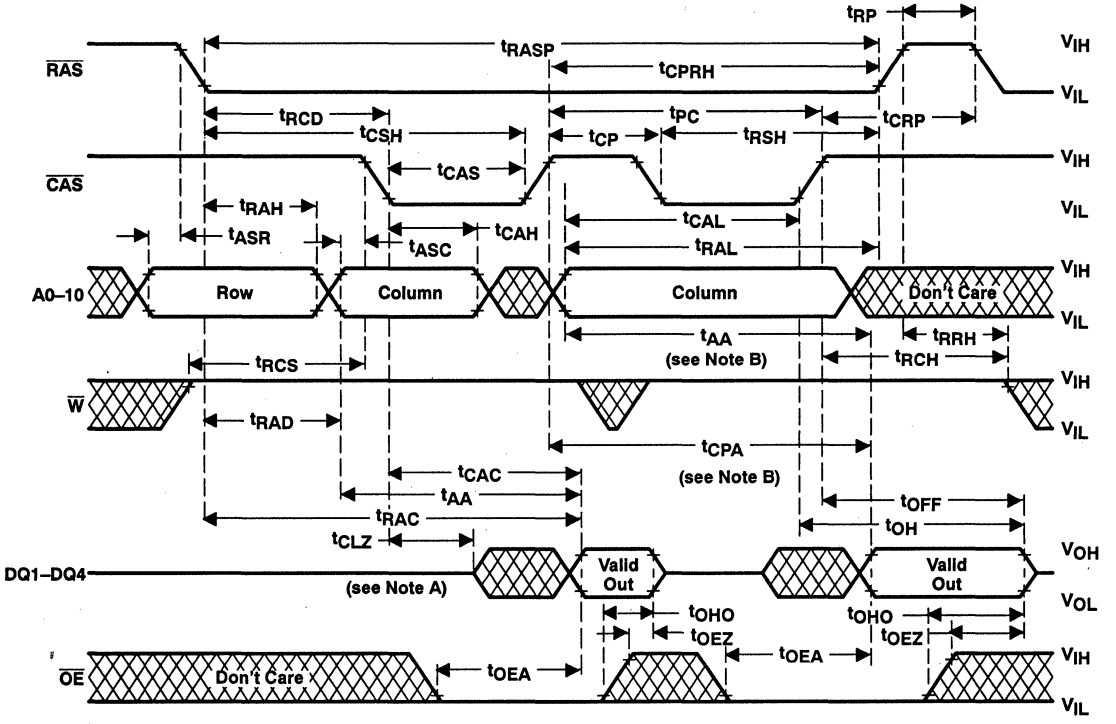


NOTE A: Output may go from three-state to an invalid data state prior to the specified access time.

Figure 6. Read-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

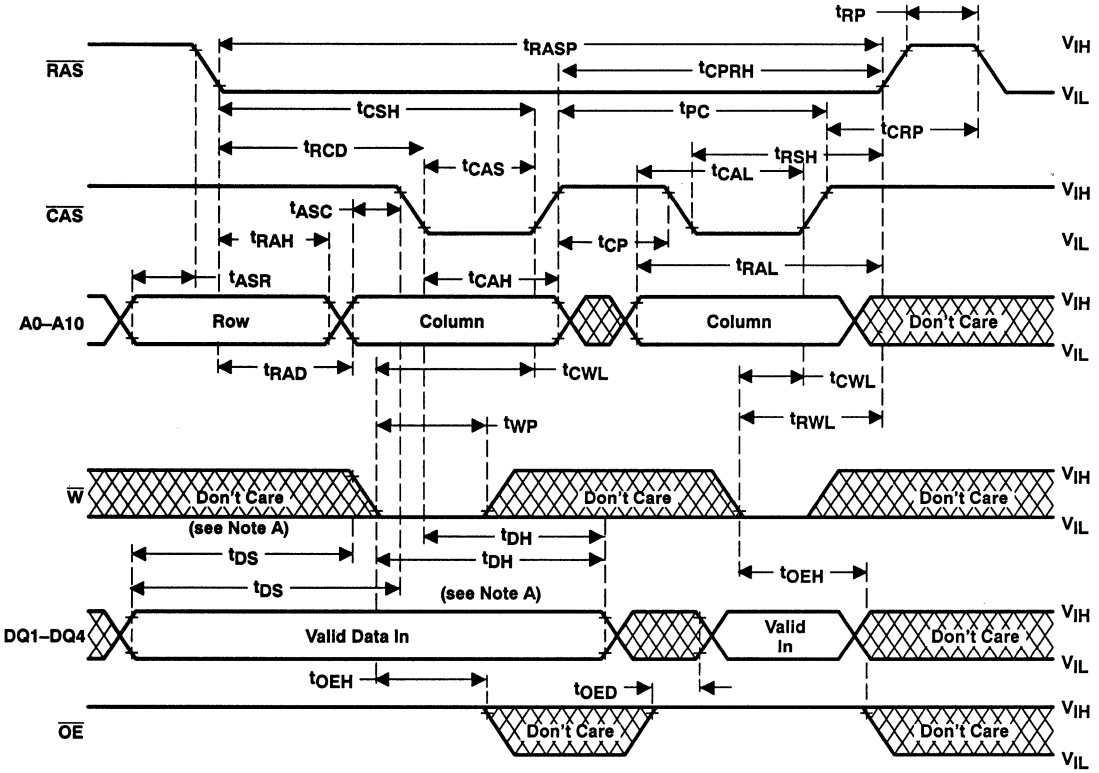


NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 7. Enhanced Page-Mode Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

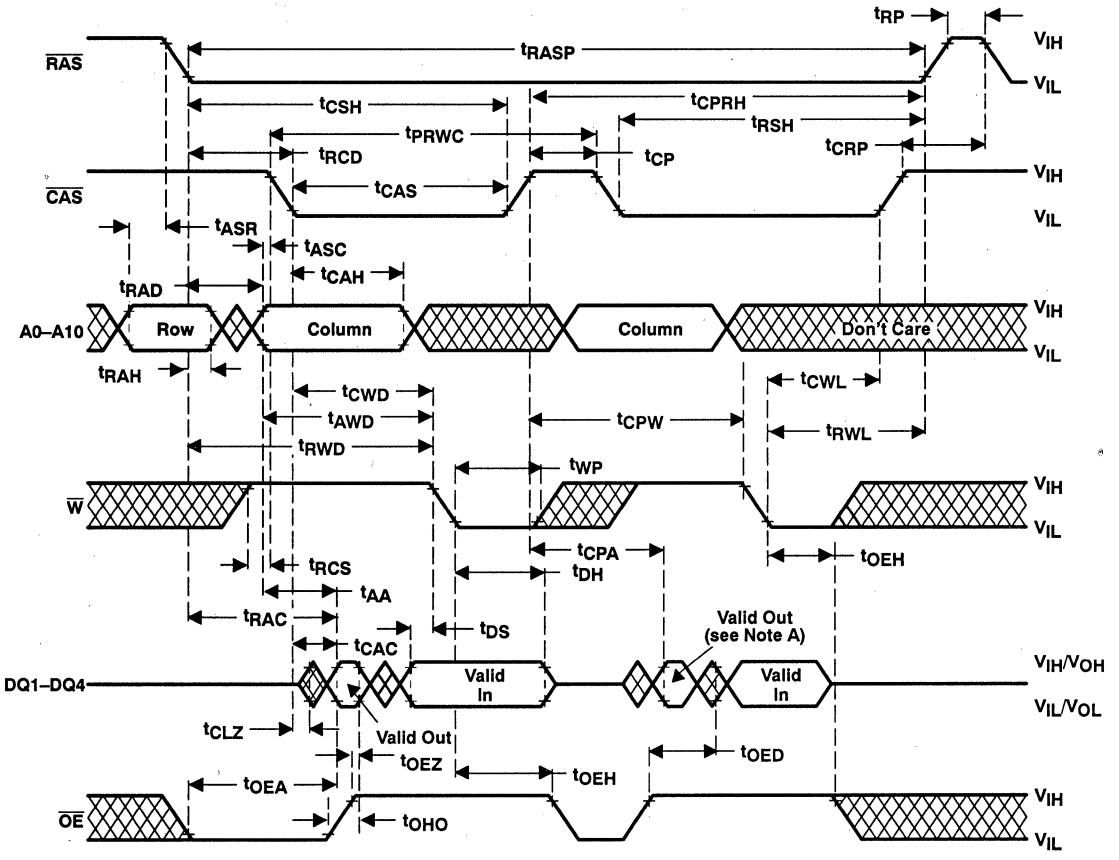


NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from three-state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

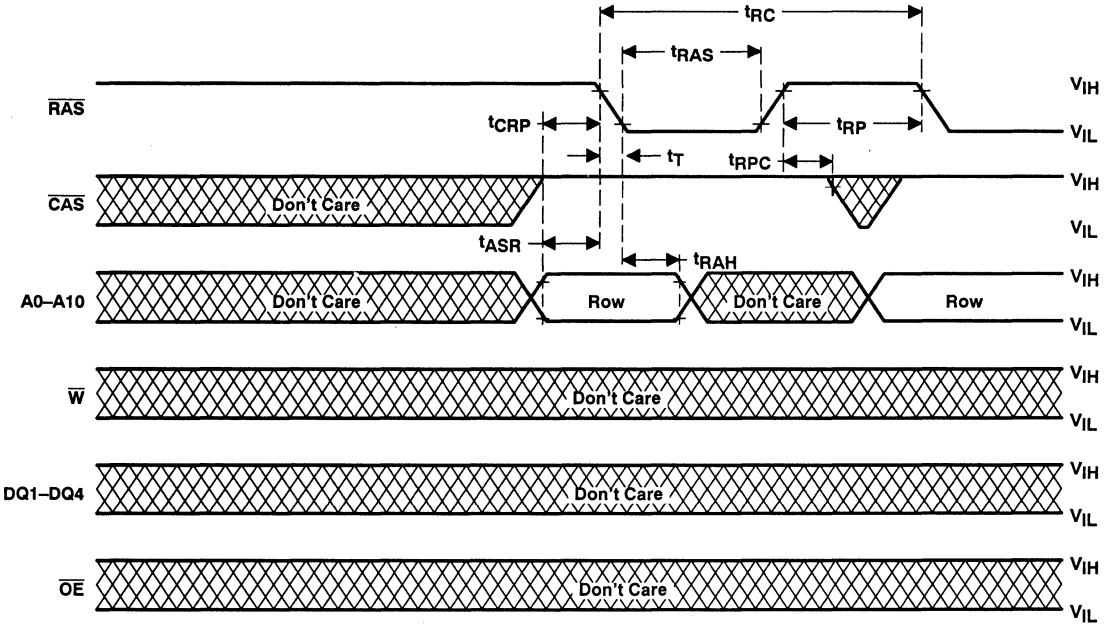


Figure 10. $\overline{RAS}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

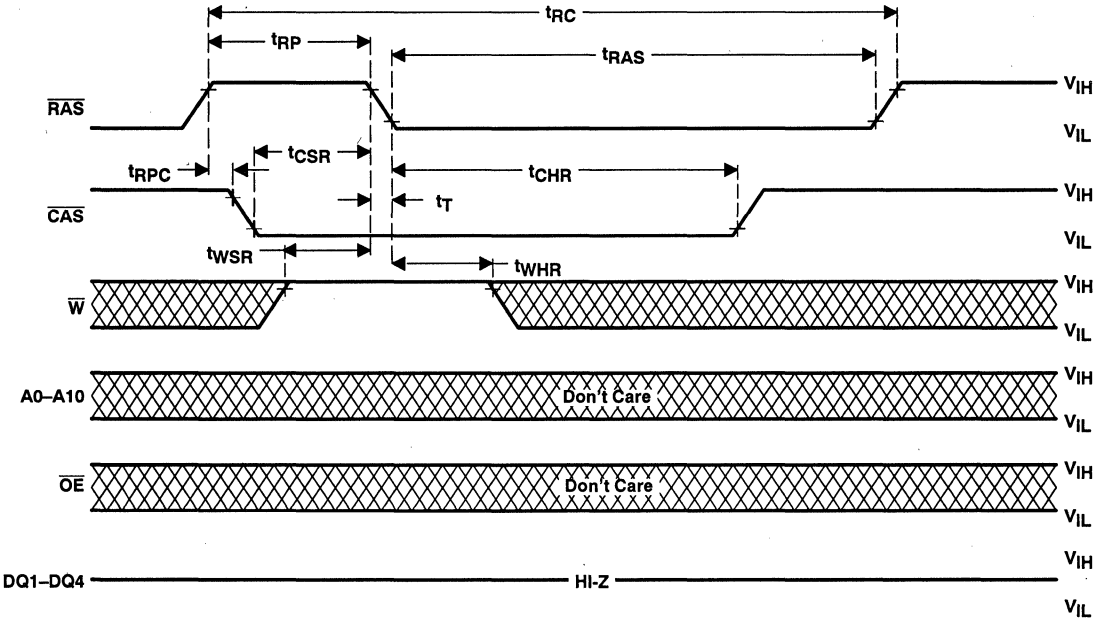

Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

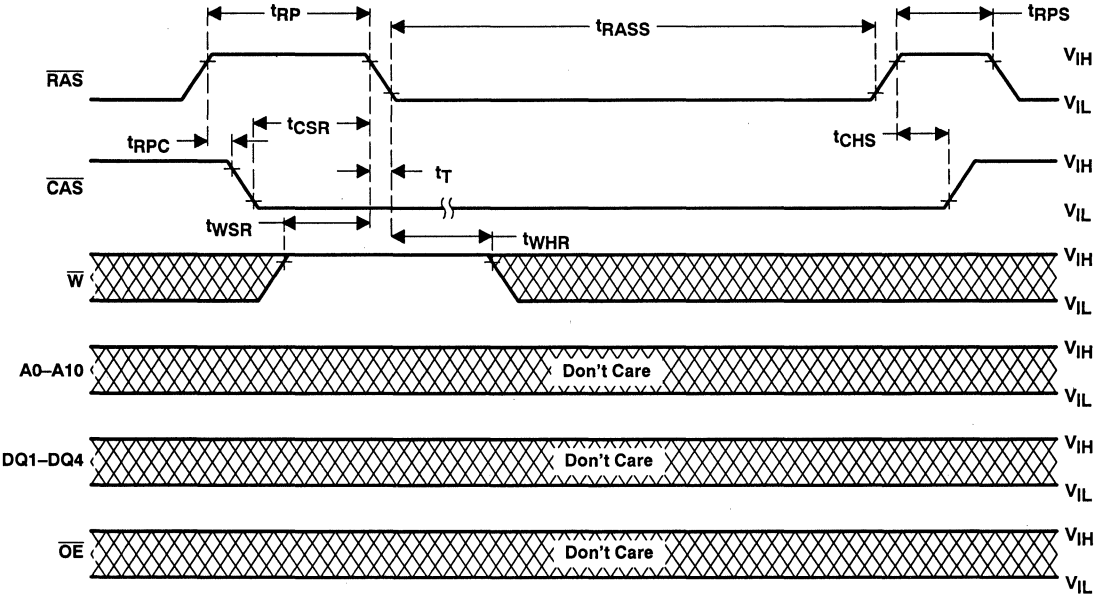

Figure 12. Self Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

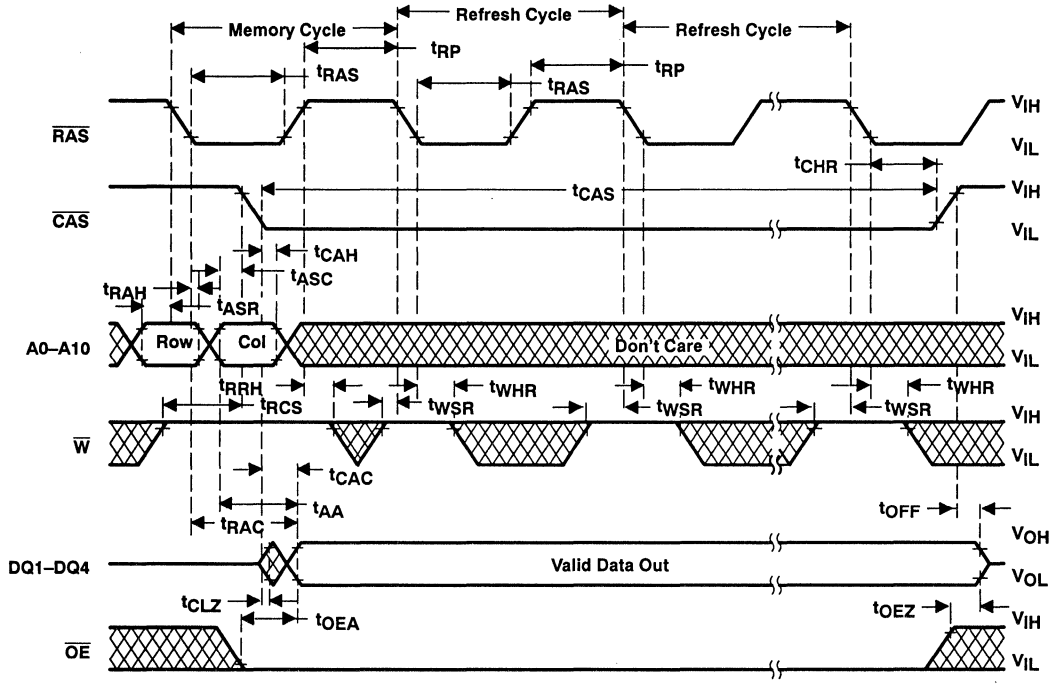

Figure 13. Hidden Refresh Cycle (Read)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

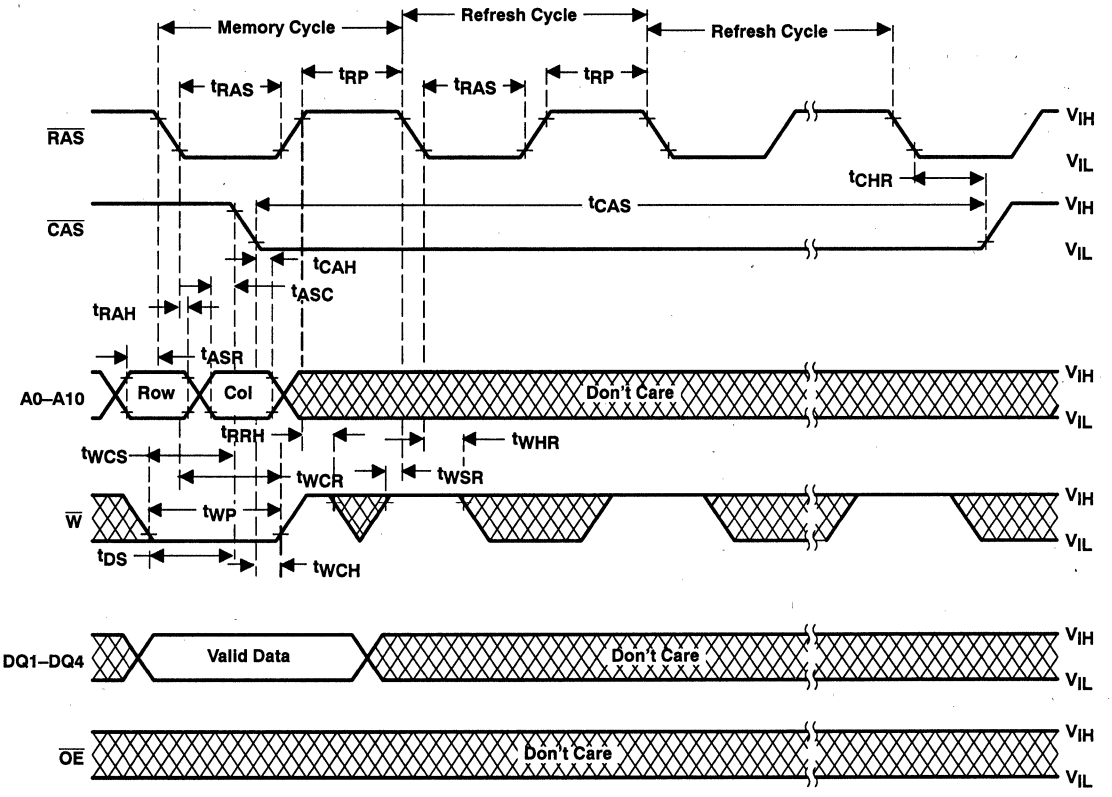

Figure 14. Hidden Refresh Cycle (Write)

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PARAMETER MEASUREMENT INFORMATION

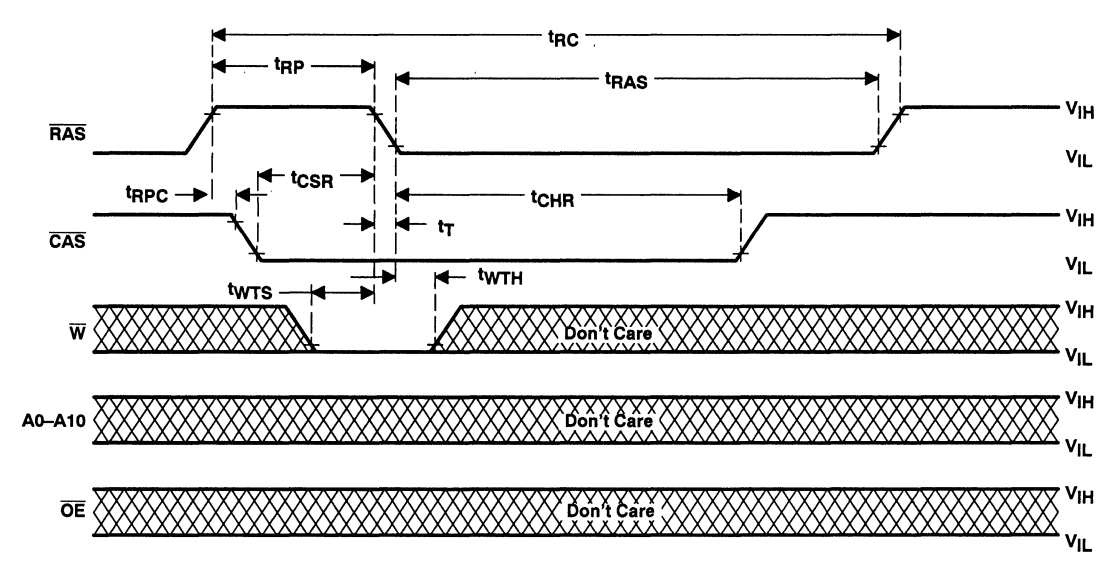
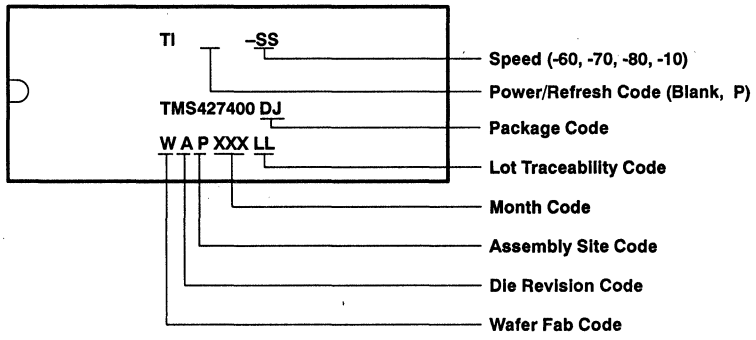


Figure 15. Test Mode Entry Cycle

PRODUCT PREVIEW

device symbolization



PRODUCT PREVIEW

TEXAS INSTRUMENTS
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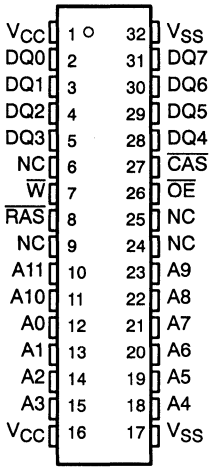
- **Organization . . . 2 097 152 × 8**
- **Single 3.3-V Power Supply (±0.3 V Tolerance)**
- **Performance Ranges:**

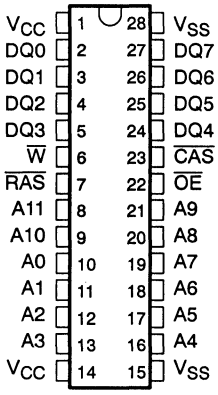
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'426800/P-70	70 ns	18 ns	35 ns	130 ns
'426800/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **4096-Cycle Refresh in 64 ms (Max)**
  - **512 ms for Low Power, Self-Refresh Version (TMS426800P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
  - **100 μA CMOS Standby**
  - **100 μA Extended Refresh Battery Backup**
- **Self-Refresh With Low-Power**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 28-Pin, J-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 32-Pin, Plastic Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

DE PACKAGE† (TOP VIEW)



DZ PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write-Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS426800 series are high-speed, low voltage 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

The TMS426800P series are high-speed, low voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns and 80 ns. Maximum power dissipation is as low as 252 mW operating, and 0.36 mW standby and battery backup for 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS426800 and TMS426800P series are offered in a 400-mil 28-lead plastic surface mount SOJ package (DZ suffix) and a 32-lead plastic surface mount TSOP package (DE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS426800 and TMS426800P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode.* Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A11)

Twenty-one address bits are required to decode 1 of 2 097 152 storage cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ0–DQ7)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 64 milliseconds (512 ms for TMS426800P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS426800P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs, while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh (TMS426800P)

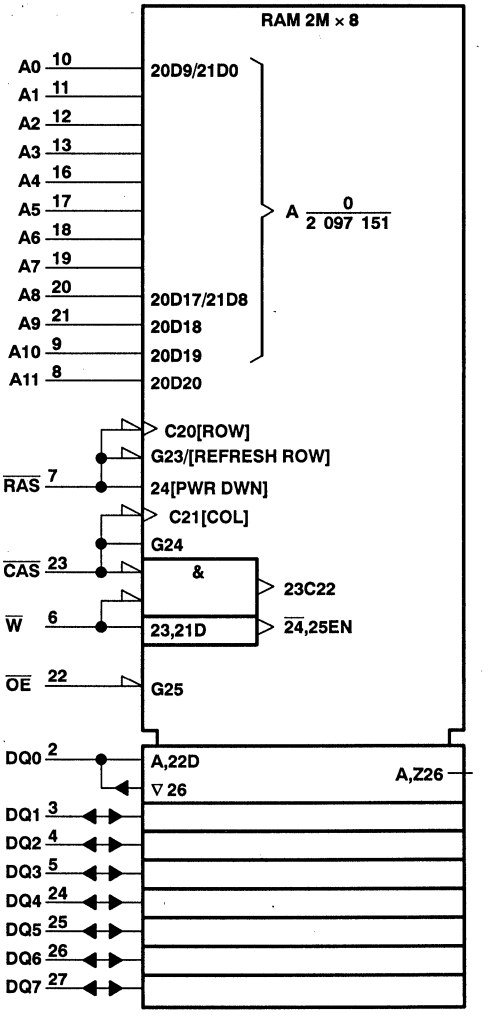
The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

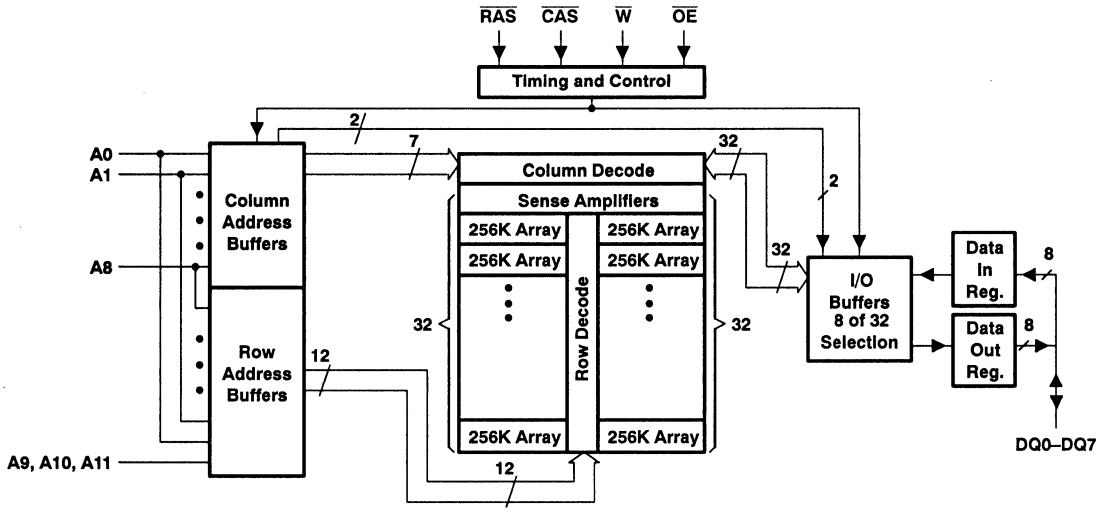
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Supply voltage range on V_{CC} . . . . . – 0.5 V to 4.6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}+ 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS426800-70 TMS426800P-70 MIN	TMS426800-70 TMS426800P-70 MAX	TMS426800-80 TMS426800P-80 MIN	TMS426800-80 TMS426800P-80 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC} –0.2		V_{CC} –0.2		V
V_{OL}	Option	I_{OL} = +100 µA			0.2		0.2	V
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 to 3.9 V, All other pins = 0 to V_{CC}			± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 3.6 V, Minimum cycle			80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'426800		300		300	µA
			'426800P		100		100	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			80		70	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 3.6 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			80		70	mA
I_{CC6}‡	Self refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			100		100	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Data out = Enabled			5		5	mA
I_{CC10}‡	Battery backup operating current (equivalent refresh time is 512 ms) CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100	µA

† Measured with outputs open.
‡ For TMS426800P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS426800-70 TMS426800P-70		TMS426800-80 TMS426800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20	ns
t_{CPA}	Access time from column precharge		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		ns
t_{OHO}	Output disable time, start of $\overline{OE}$ high	3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	18	0	20	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	TMS426800-70 TMS426800P-70		TMS426800-80 TMS426800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	130		150		ns
t_{RWC}	Read-modify-write cycle time	181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high ($\overline{CAS}$ precharge)	10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high ($\overline{RAS}$ precharge)	50		60		ns
t_{WP}	Write pulse duration	15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

	PARAMETER	TMS426800-70 TMS426800P-70		TMS426800-80 TMS426800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		ns
t_{DH}	Data hold time (see Note 11)	15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-modify-write operation only)	63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	18		20		ns
t_{OED}	$\overline{OE}$ to data delay	18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	68		75		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	40		45		ns

NOTES: 11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		TMS426800-70 TMS426800P-70		TMS426800-80 TMS426800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	– 50		– 50		ns
t_{REF}	Refresh time interval (TMS426800 only)		64		64	ms
t_{REF}	Refresh time interval Low power (TMS426800P only)		512		512	ms
t_T	Transition time	3	30	3	30	ns

PARAMETER MEASUREMENT INFORMATION

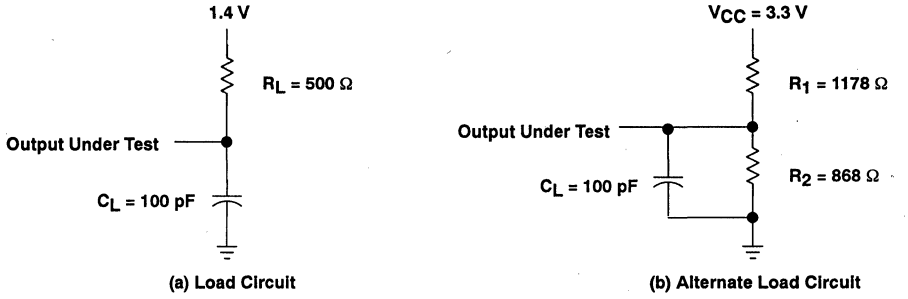
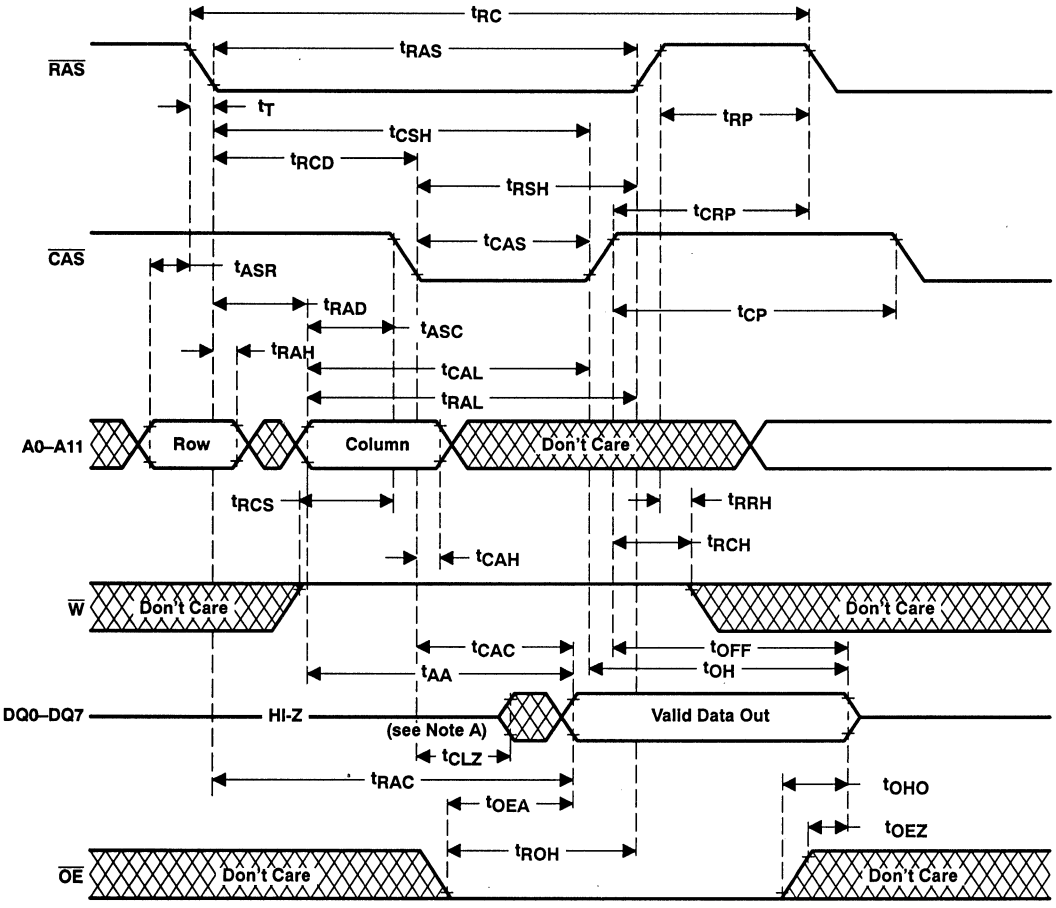


Figure 1. Load Circuits for Timing Parameters

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

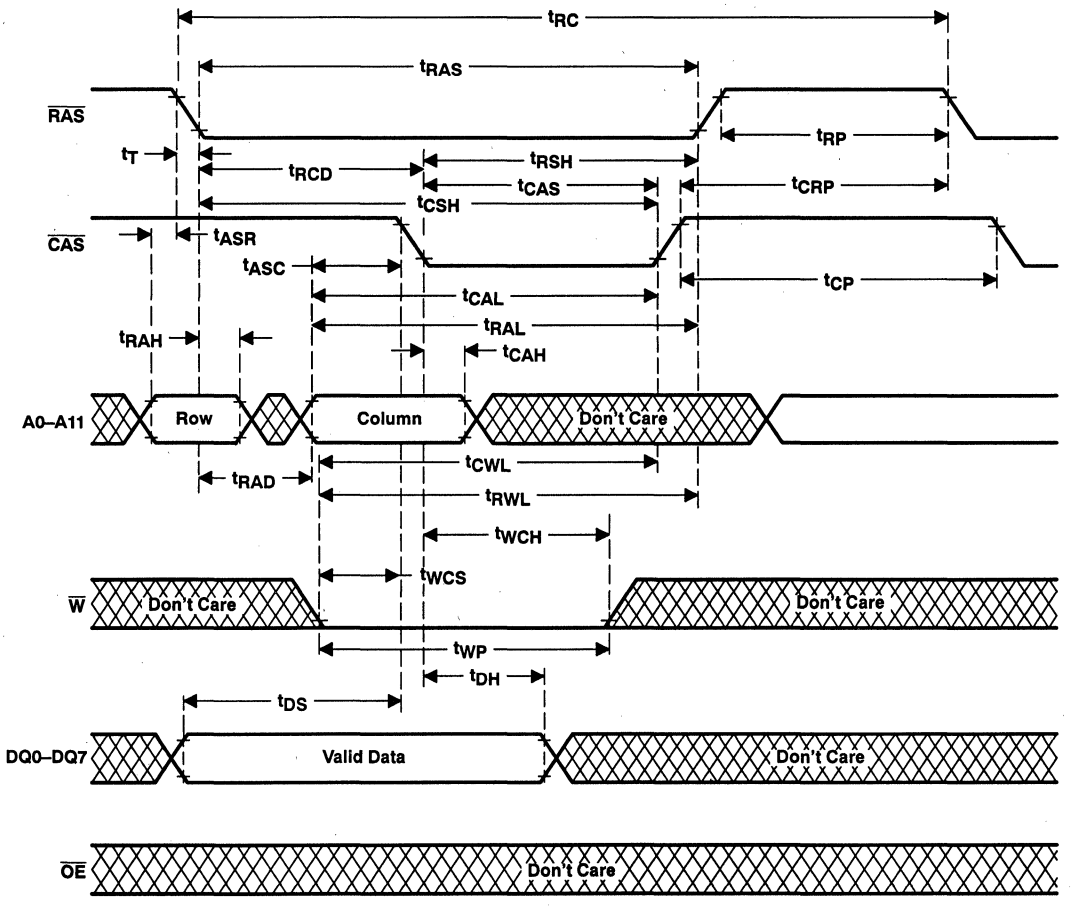
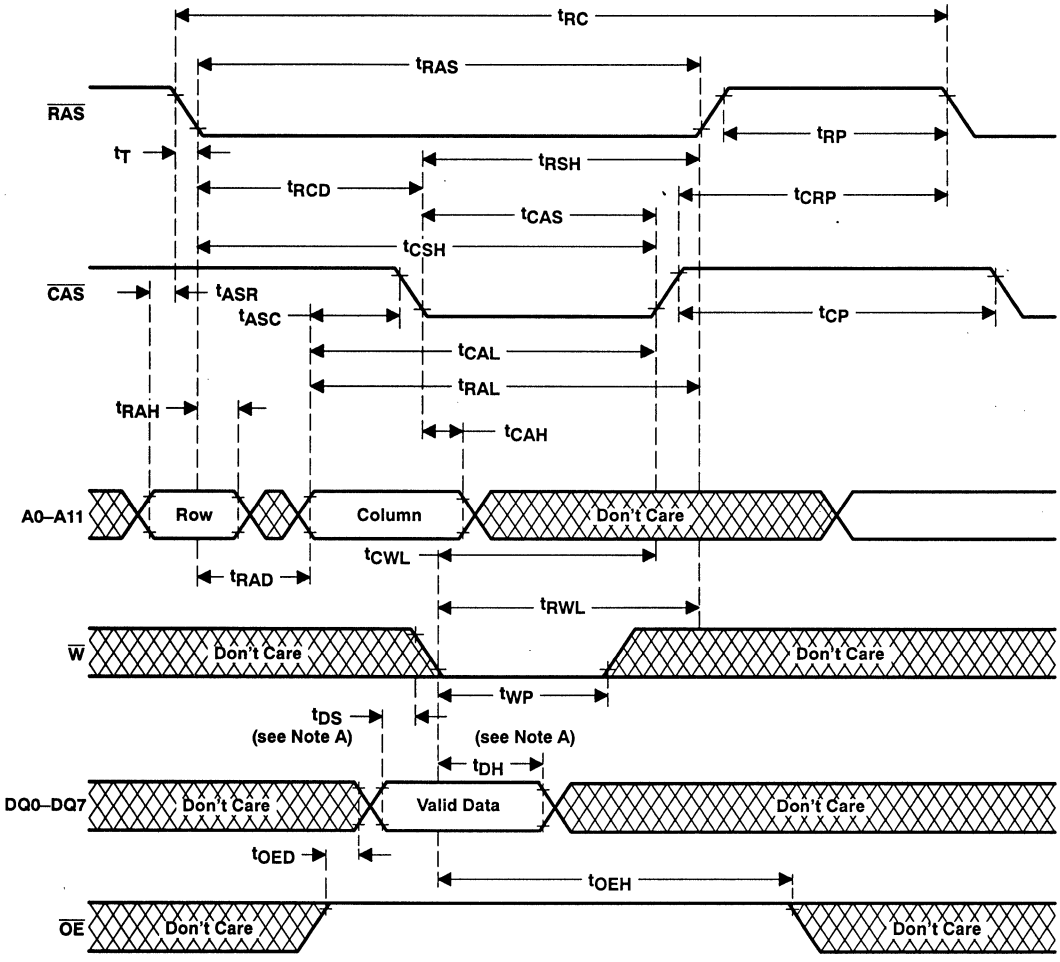


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 4. Write Cycle Timing

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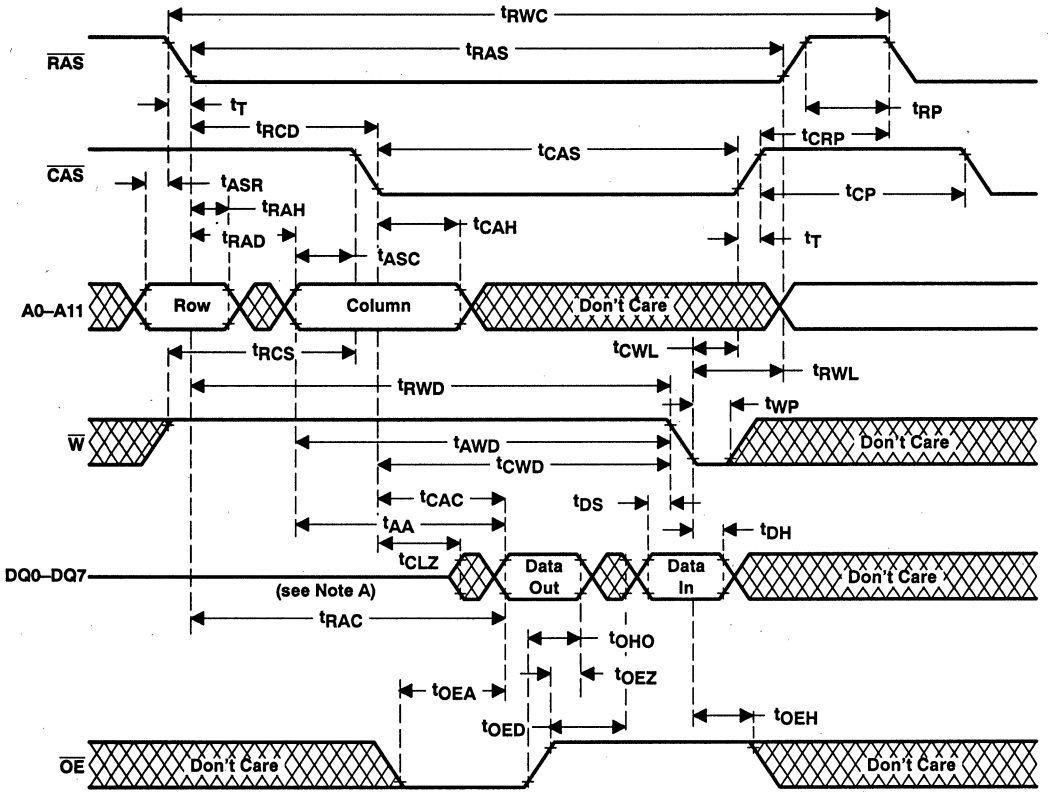
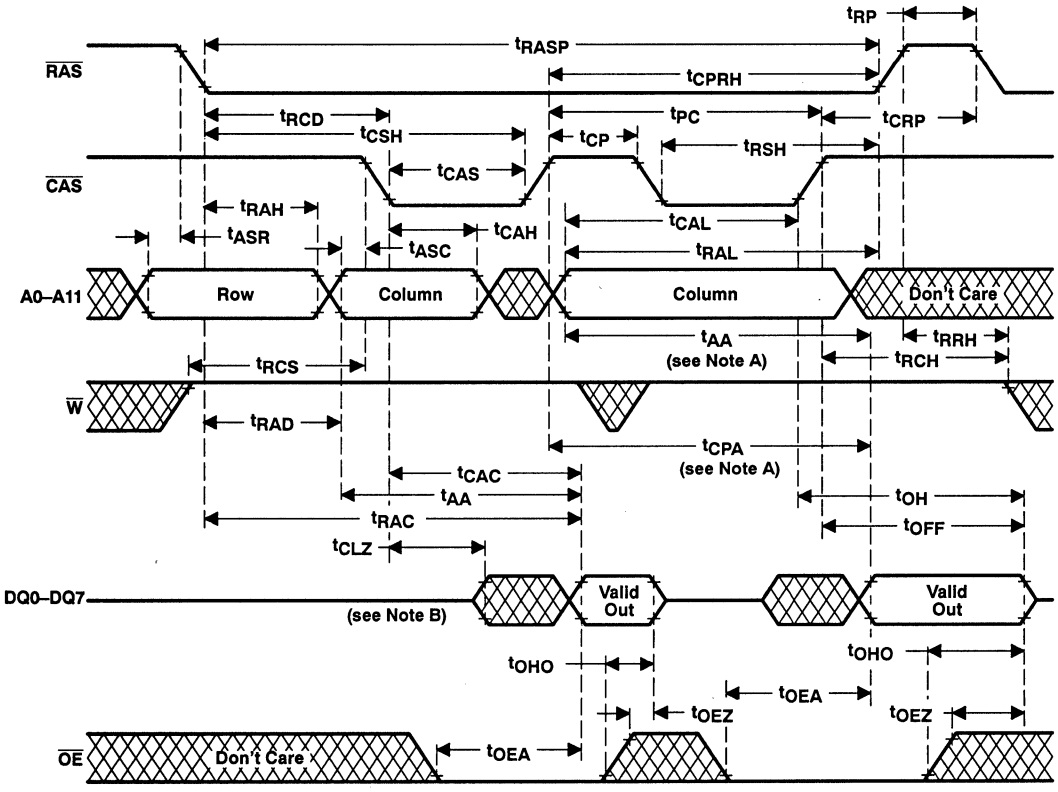
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

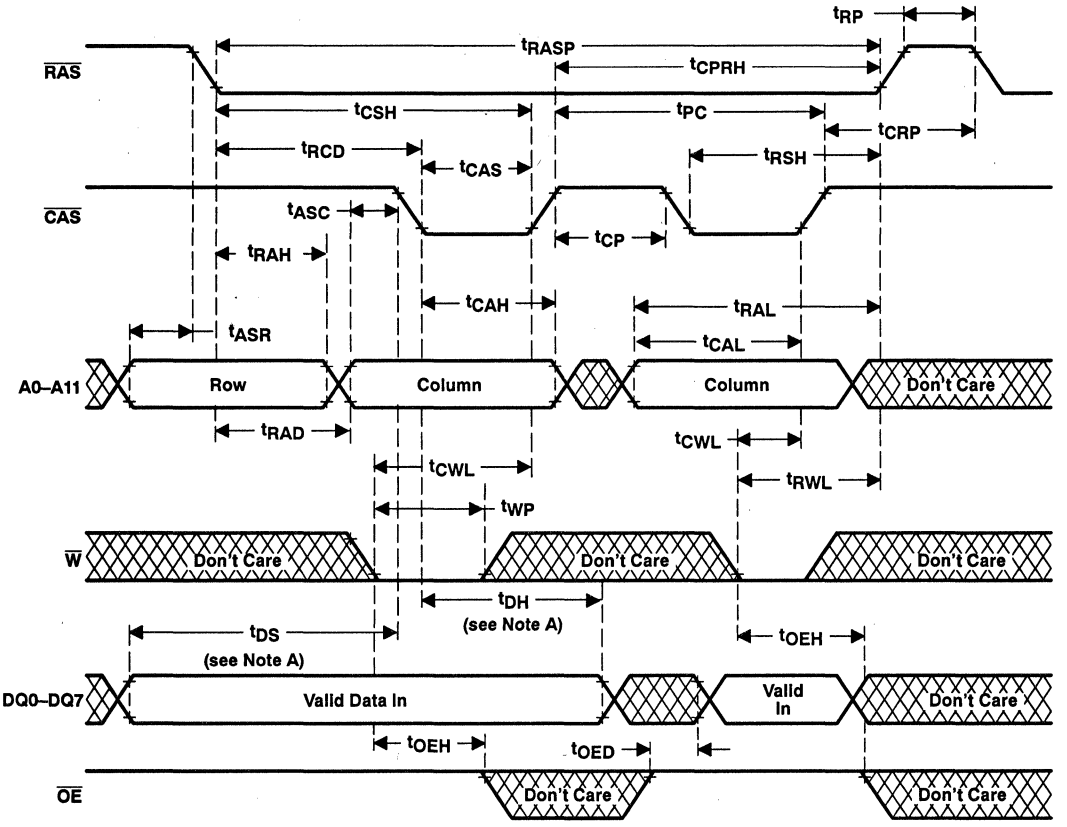


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
C. A write cycle or read-modify-write cycle can be intermixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
B. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

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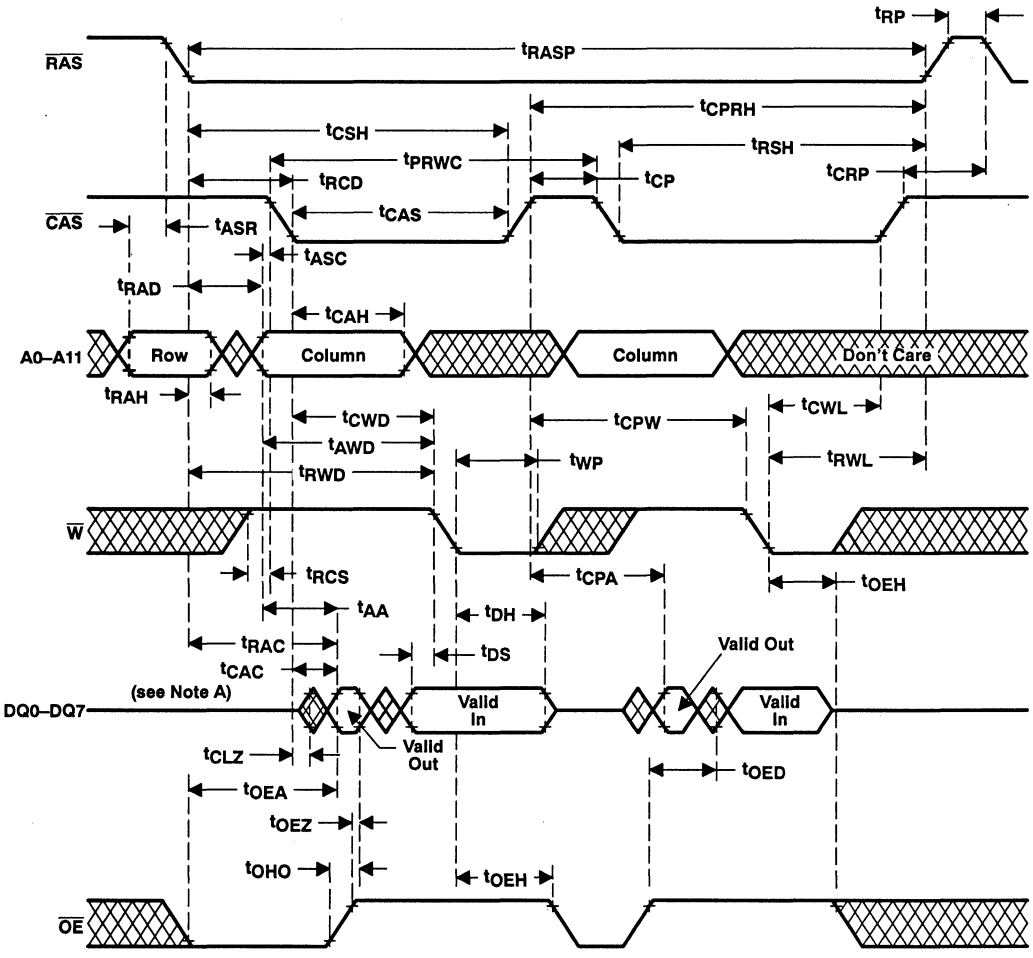
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

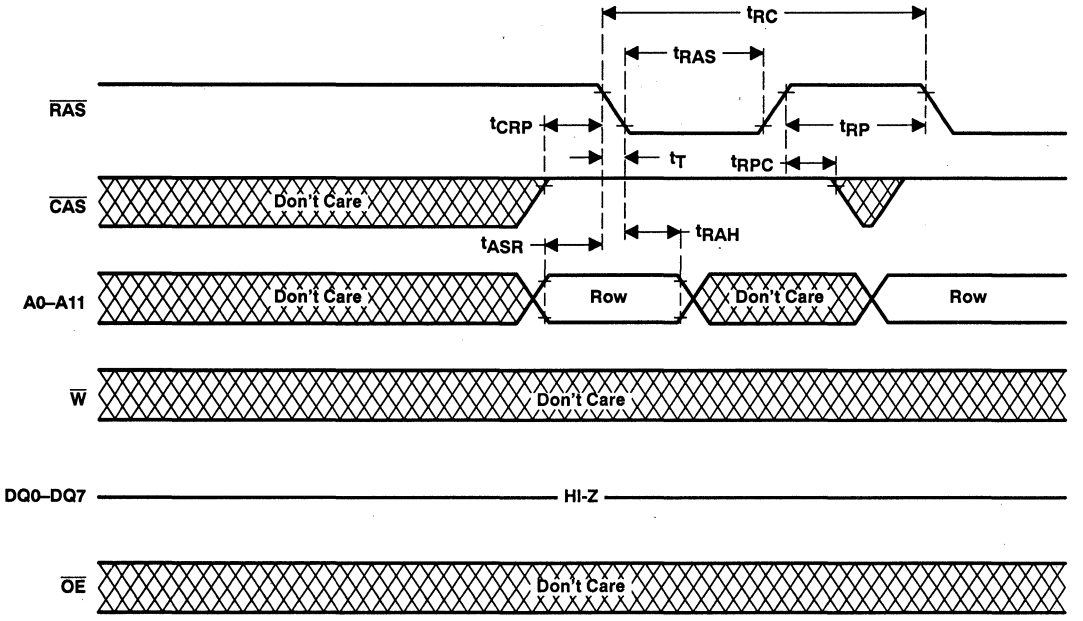


Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

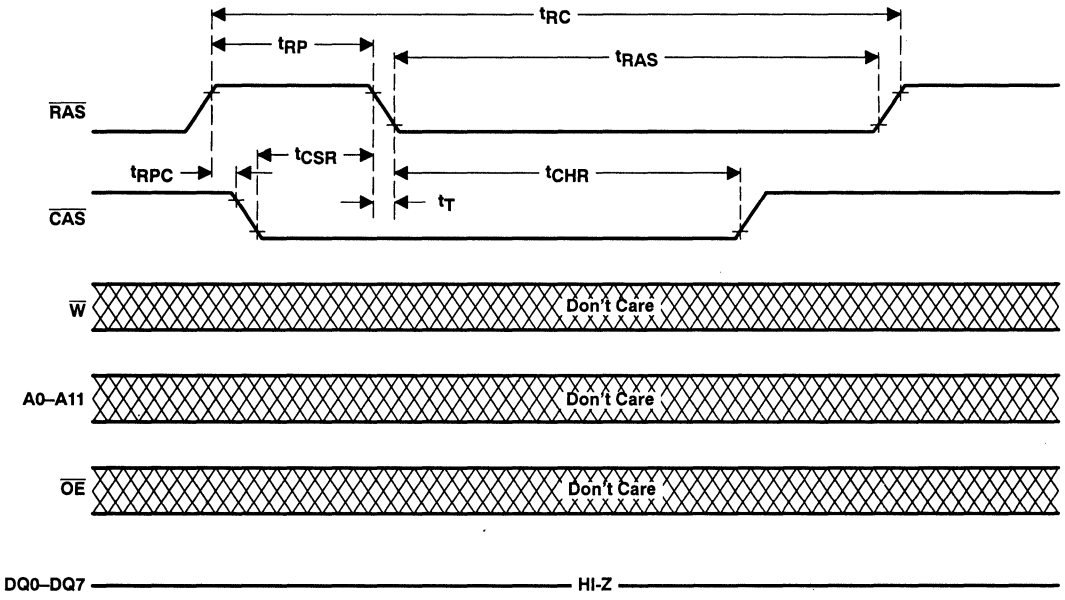
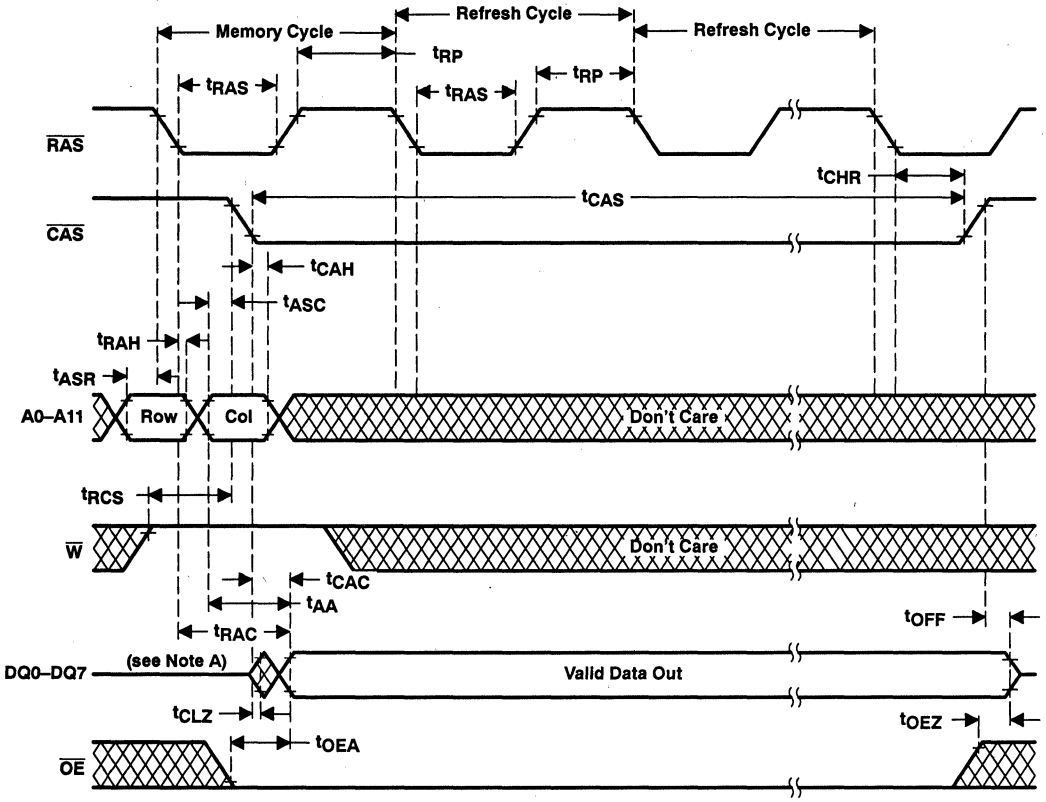


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PRODUCT PREVIEW

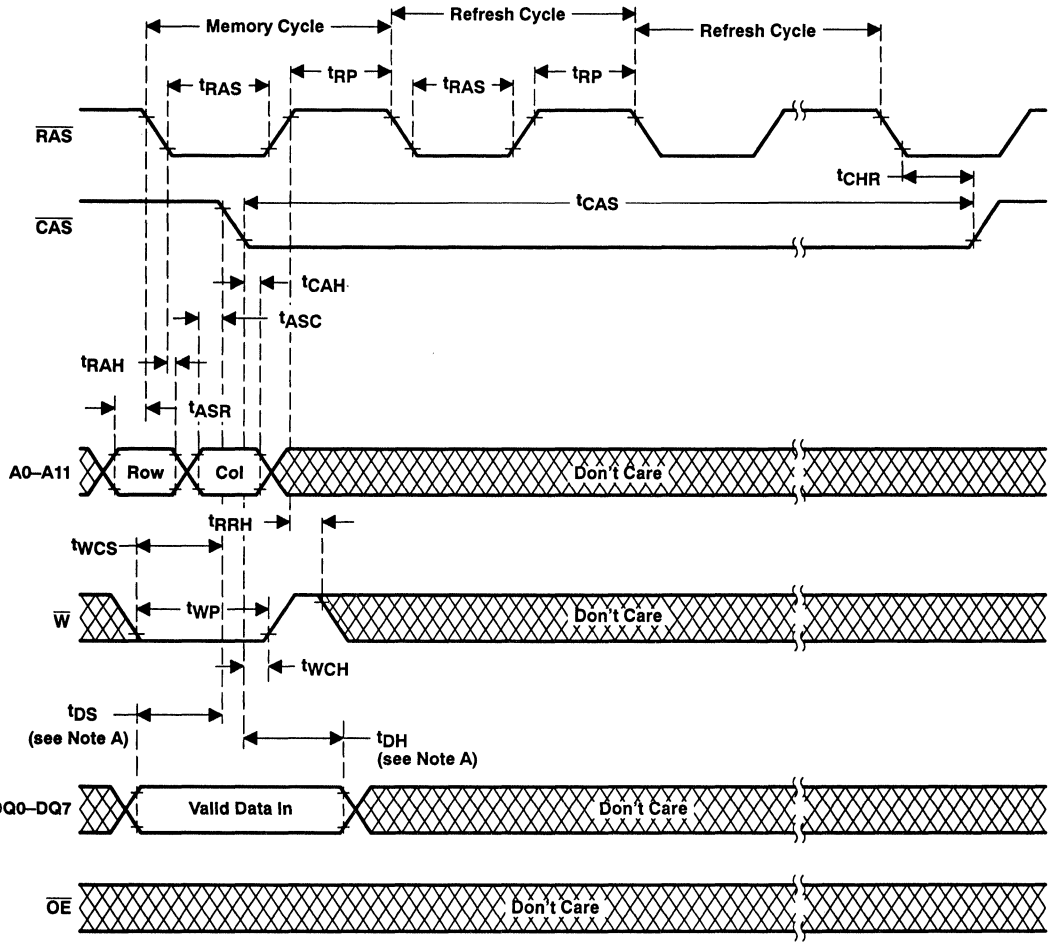
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 12. Hidden Refresh Cycle (Write)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

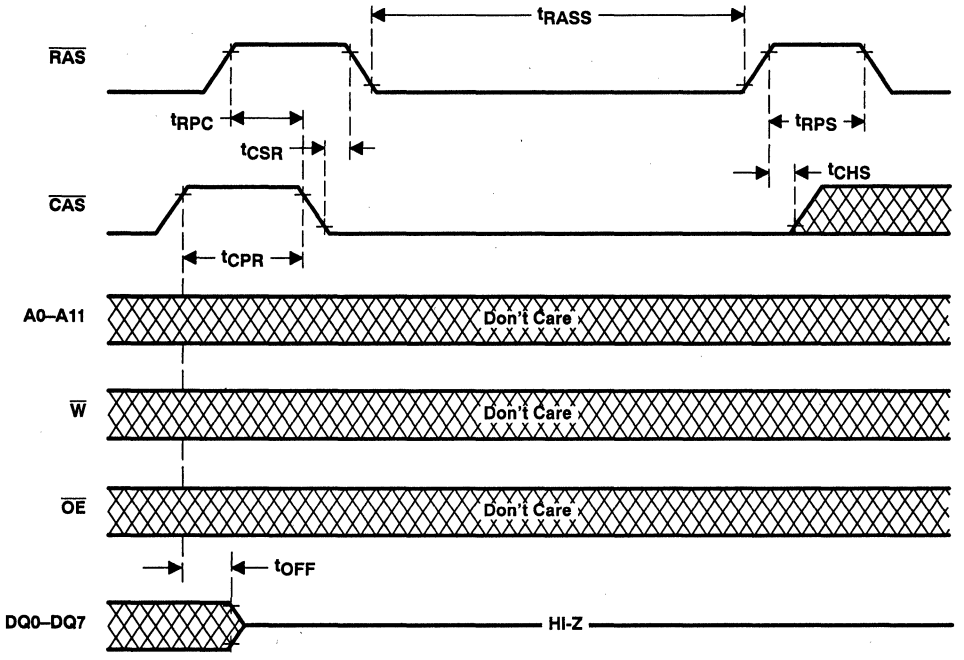
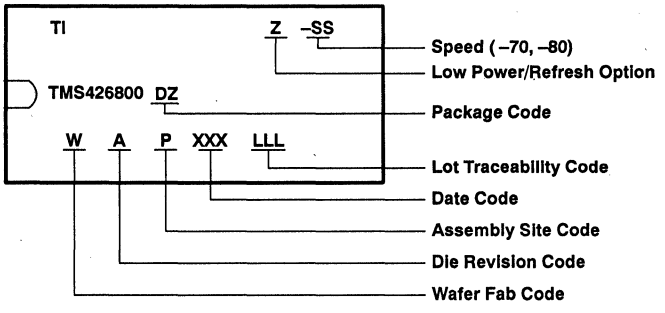


Figure 13. Self Refresh Timing

device symbolization



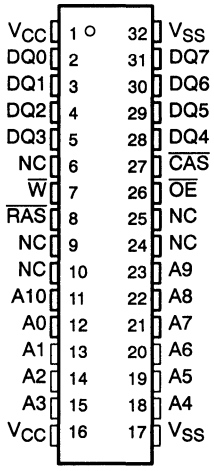
PRODUCT PREVIEW

- **Organization . . . 2 097 152 × 8**
- **Single 3.3-V Power Supply (±0.3 V Tolerance)**
- **Performance Ranges:**

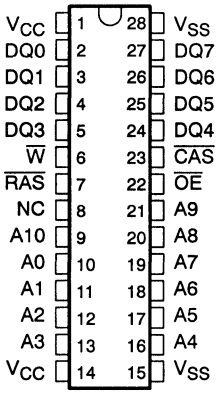
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'427800/P-70	70 ns	18 ns	35 ns	130 ns
'427800/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **2048-Cycle Refresh in 32 ms (Max)**
  - **256 ms for Low Power, Self-Refresh Version (TMS427800P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
  - **100 µA CMOS Standby**
  - **100 µA Extended Refresh Battery Backup**
- **Self-Refresh With Low-Power**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 28-Pin, J-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 32-Pin, Plastic Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

DE PACKAGE† (TOP VIEW)



DZ PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write-Enable
V_{CC}	3.3-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS427800 series are high-speed, low voltage 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

The TMS427800P series are high-speed, low voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 70 ns and 80 ns. Maximum power dissipation is as low as 378 mW operating, and 0.36 mW standby and battery backup for 80-ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS427800 and TMS427800P series are offered in a 400-mil 28-lead plastic surface mount SOJ package (DZ suffix) and a 32-lead plastic surface mount TSOP package (DE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS427800 and TMS427800P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-one address bits are required to decode 1 of 2 097 152 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ0–DQ7)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 32 milliseconds (256 ms for TMS427800P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 100 μA refresh current is available on the TMS427800P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 μs, while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh (TMS427800P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 μs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

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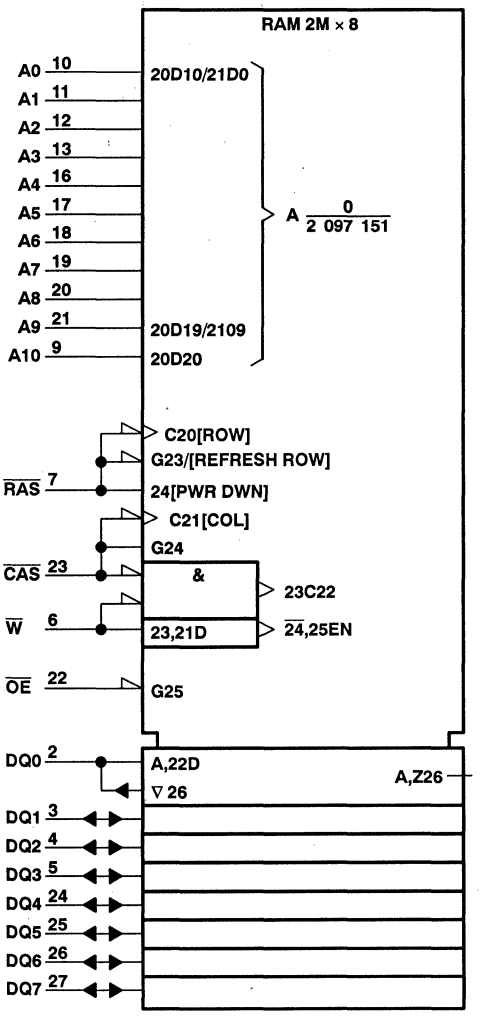
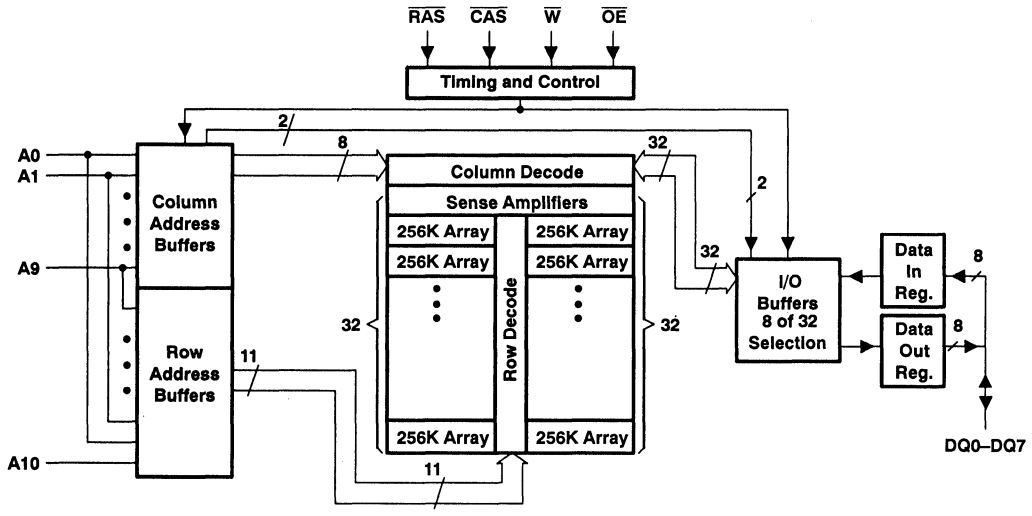
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –0.5 V to 4.6 V
Supply voltage range on V_{CC} ..... –0.5 V to 4.6 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}+ 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	–0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS427800-70 TMS427800P-70		TMS427800-80 TMS427800P-80		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
V_{OH}	Option	I_{OH} = – 100 µA		V_{CC} –0.2		V_{CC} –0.2		V
V_{OL}	Option	I_{OL} = +100 µA			0.2		0.2	V
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 to 3.9 V, All other pins = 0 to V_{CC}			± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 3.6 V, Minimum cycle			115		105	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2 V (LVTTL)			1		1	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427800		300		300	µA
			'427800P		100		100	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			115		105	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 3.6 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			115		105	mA
I_{CC6}‡	Self refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			100		100	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Data out = Enabled			5		5	mA
I_{CC10}‡	Battery backup operating current (equivalent refresh time is 256 ms) CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			100		100	µA

† Measured with outputs open.
‡ For TMS427800P only.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 3.3 V ± 0.3 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS427800-70 TMS427800P-70		TMS427800-80 TMS427800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		18		20	ns
t_{CPA}	Access time from column precharge		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		ns
t_{OHO}	Output disable time, start of $\overline{OE}$ high	3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	18	0	20	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS427800-70 TMS427800P-70		TMS427800-80 TMS427800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	130		150		ns
t_{RWC}	Read-modify-write cycle time	181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high ($\overline{CAS}$ precharge)	10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high ($\overline{RAS}$ precharge)	50		60		ns
t_{WP}	Write pulse duration	15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		TMS427800-70 TMS427800P-70		TMS427800-80 TMS427800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		ns
t_{DH}	Data hold time (see Note 11)	15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-modify-write operation only)	63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	18		20		ns
t_{OED}	$\overline{OE}$ to data delay	18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	68		75		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	40		45		ns

NOTES: 11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to assure access time.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		TMS427800-70 TMS427800P-70		TMS427800-80 TMS427800P-80		UNIT
		MIN	MAX	MIN	MAX	
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	– 50		– 50		ns
t_{REF}	Refresh time interval (TMS427800)		32		32	ms
t_{REF}	Refresh time interval Low power (TMS427800P only)		256		256	ms
t_T	Transition time	3	30	3	30	ns

PARAMETER MEASUREMENT INFORMATION

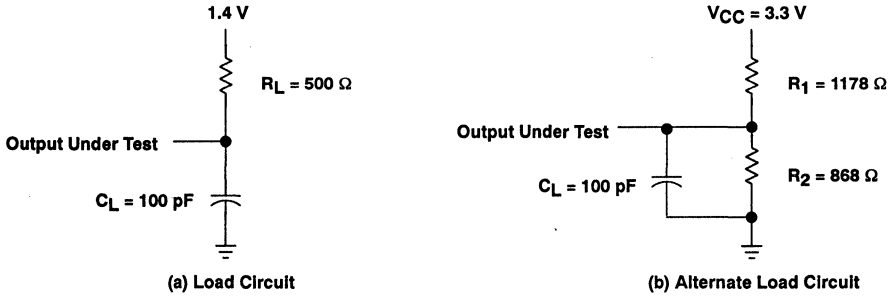

Figure 1. Load Circuits for Timing Parameters

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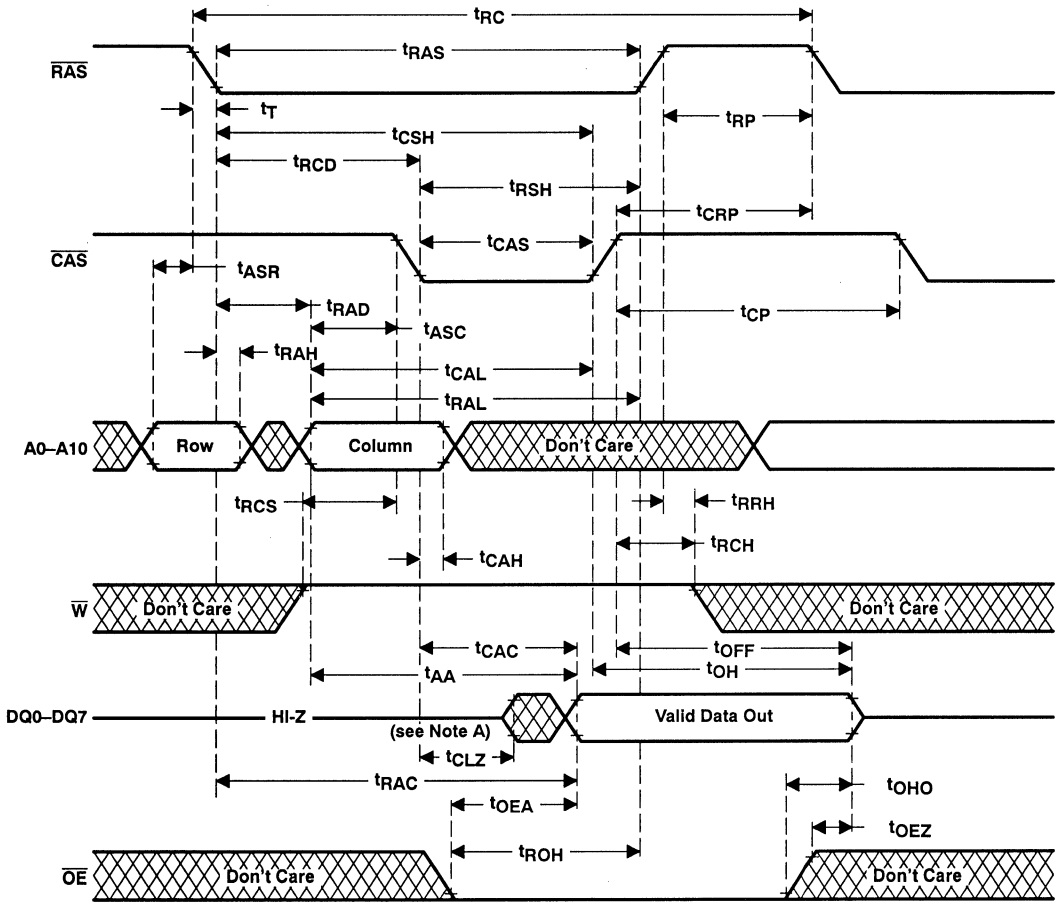
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

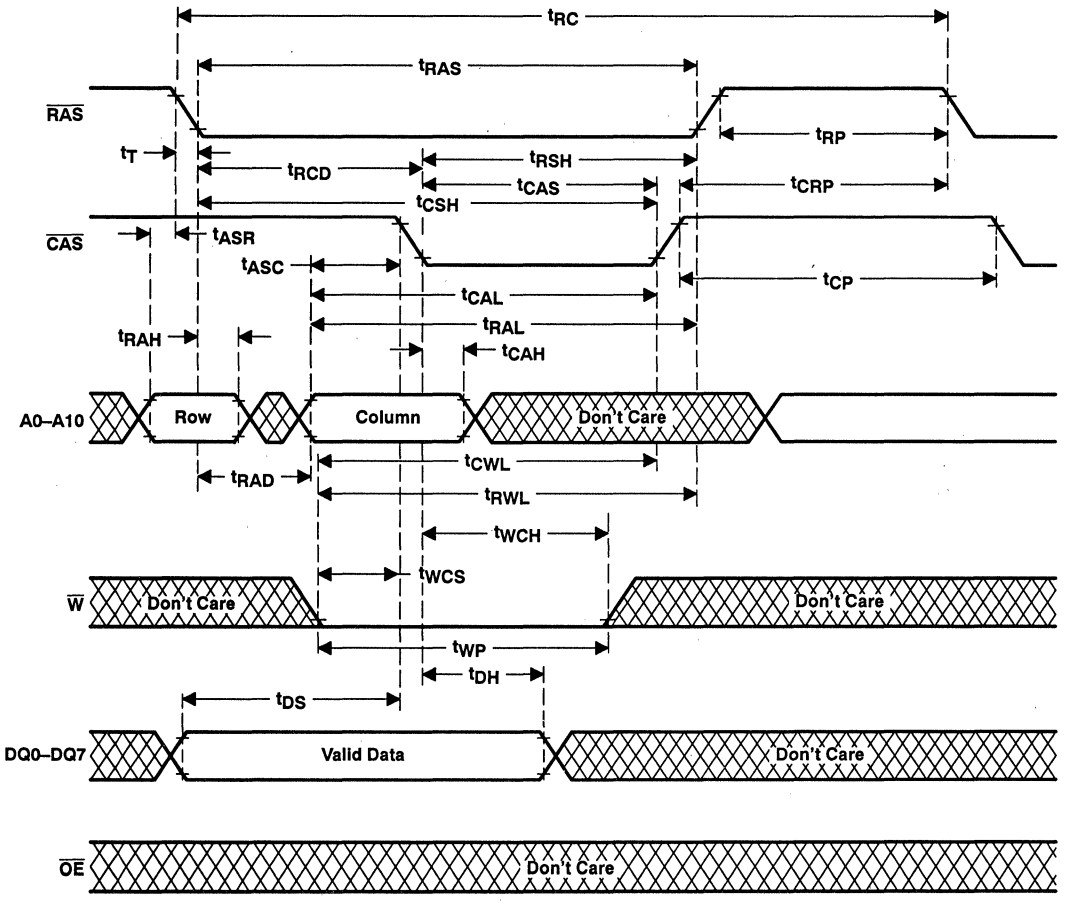
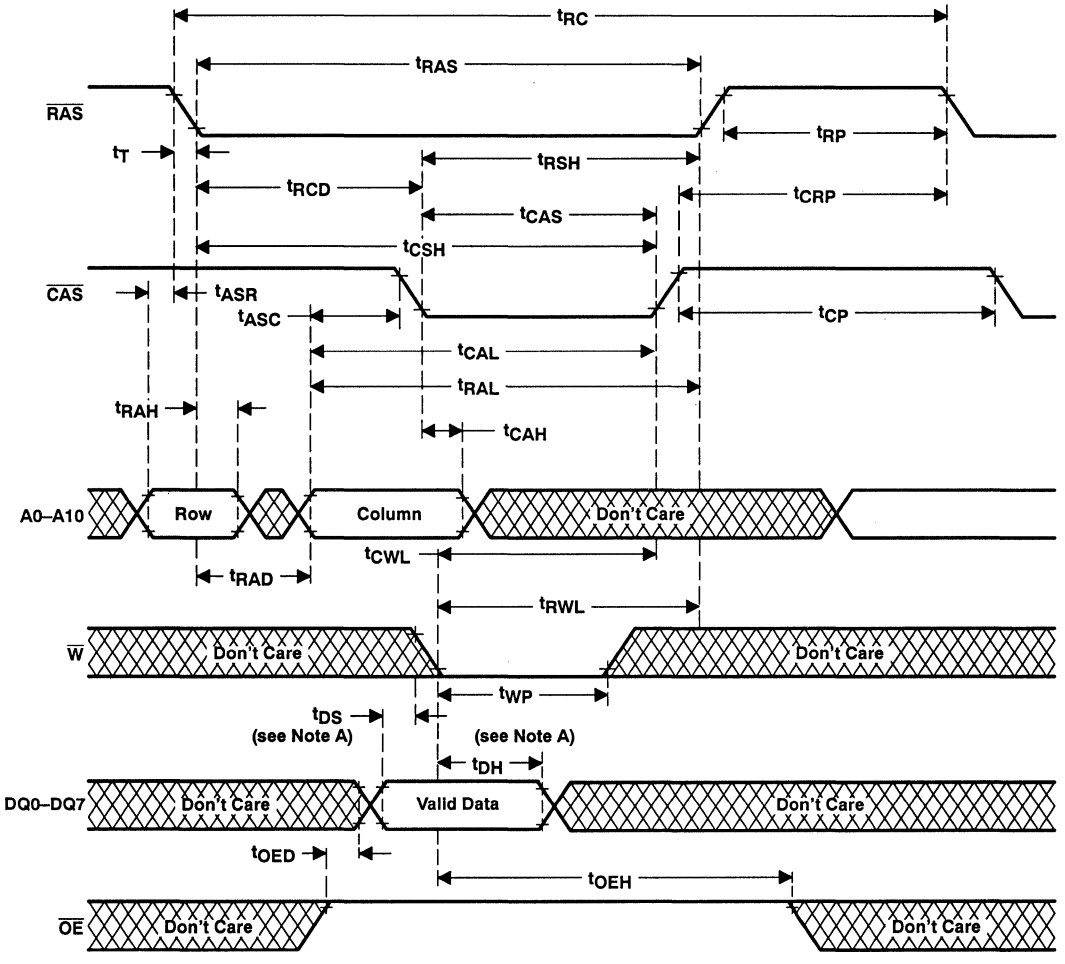


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 4. Write Cycle Timing

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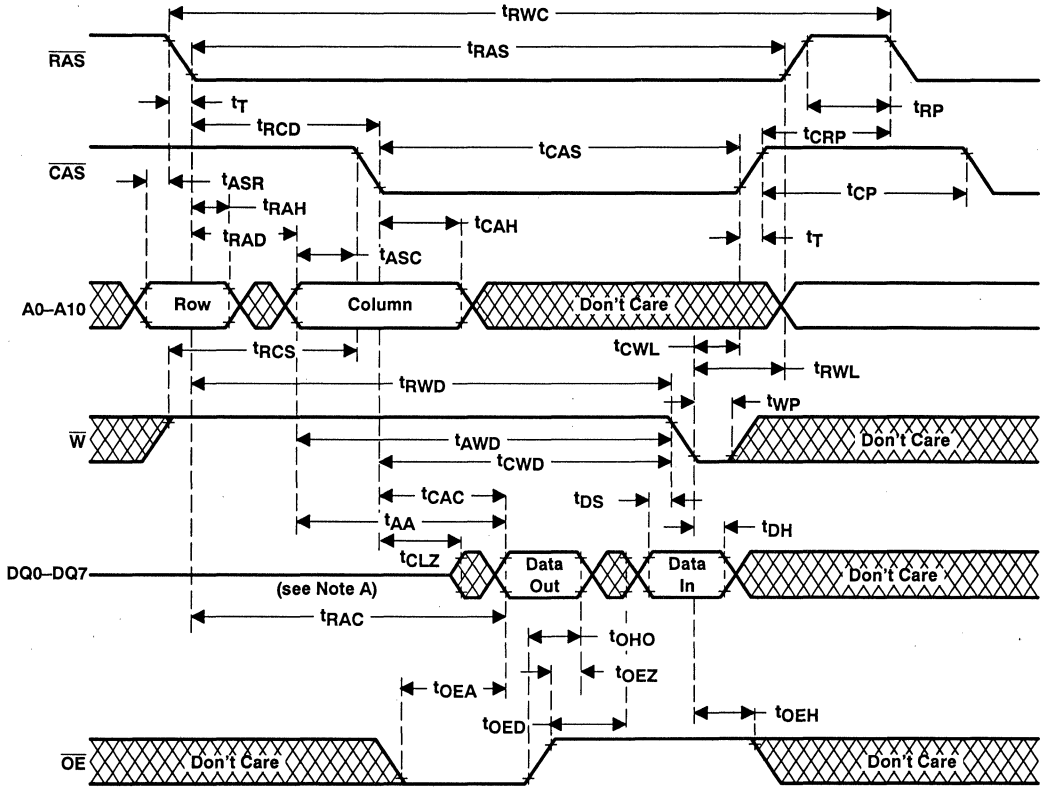
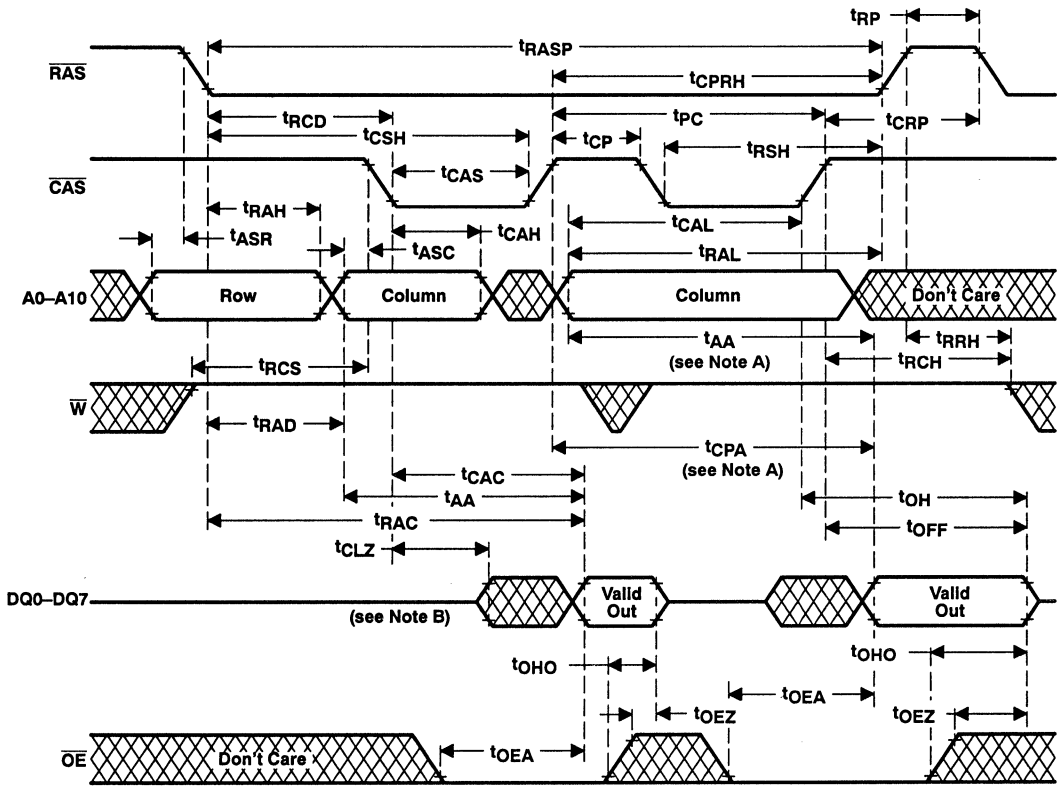
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
C. A write cycle or read-modify-write cycle can be intermixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

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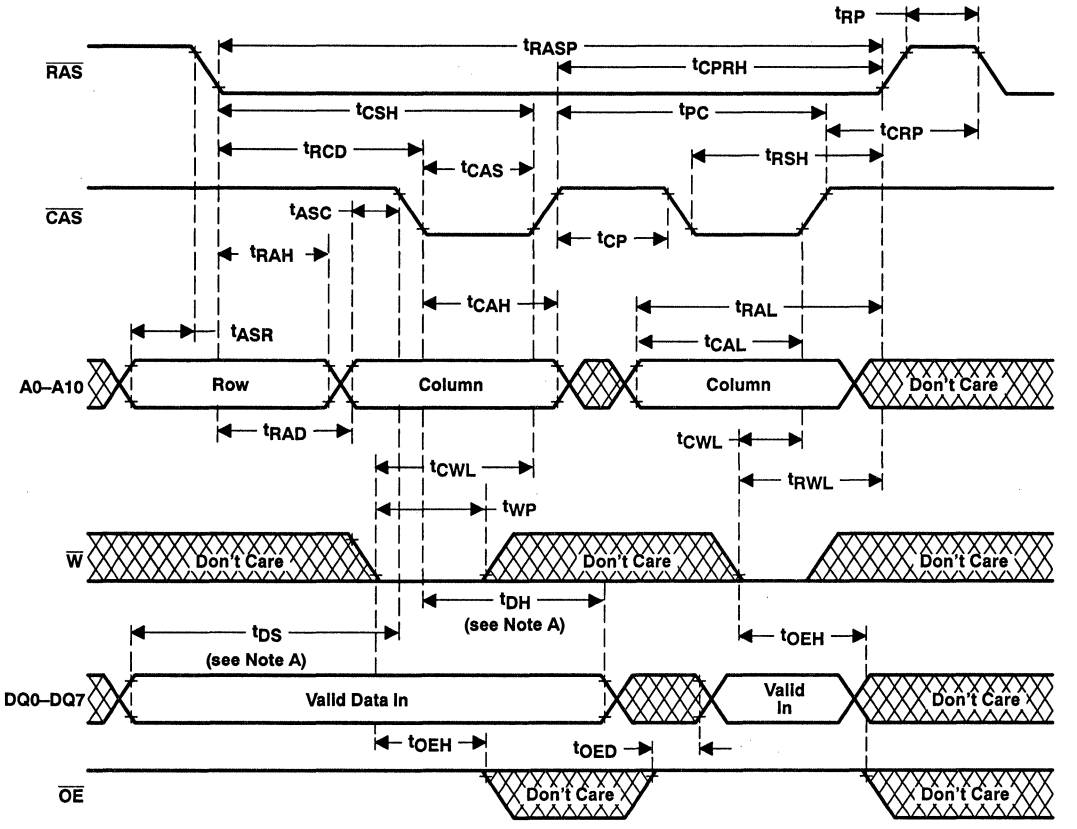
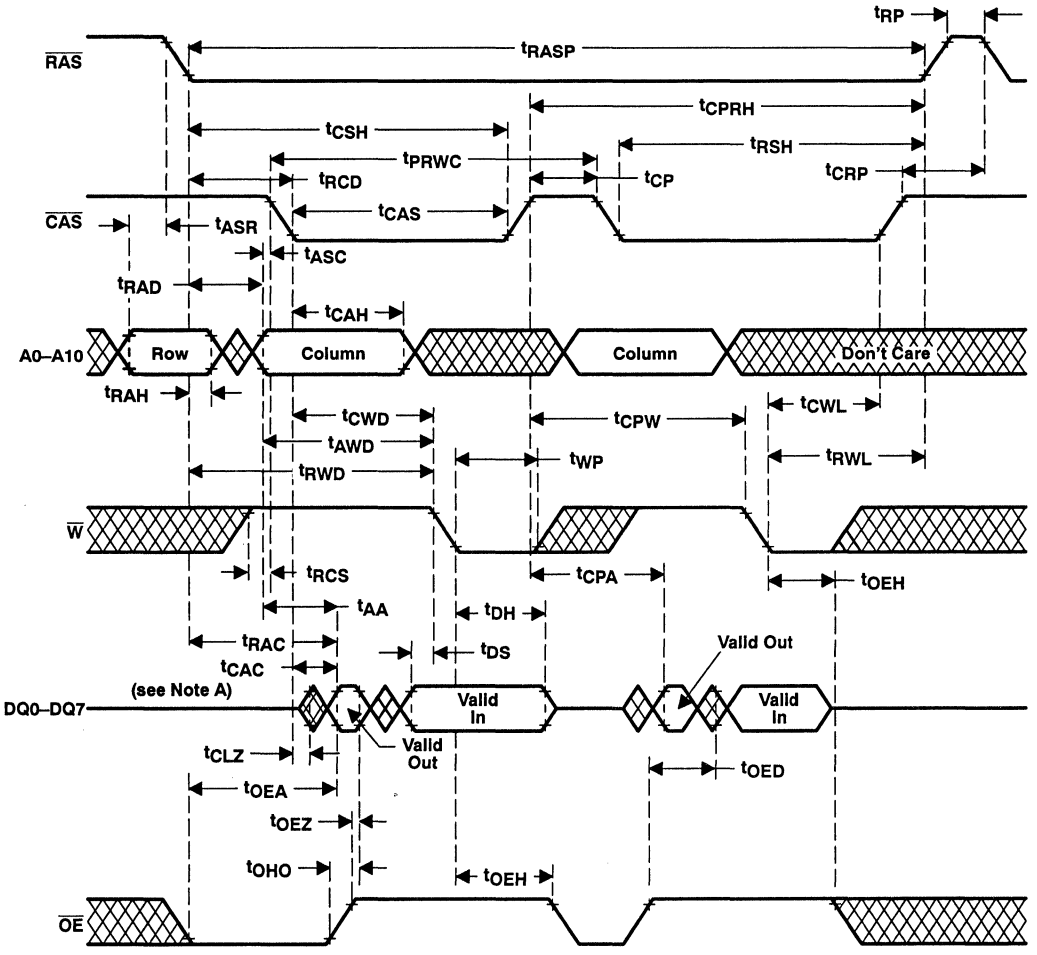
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
B. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

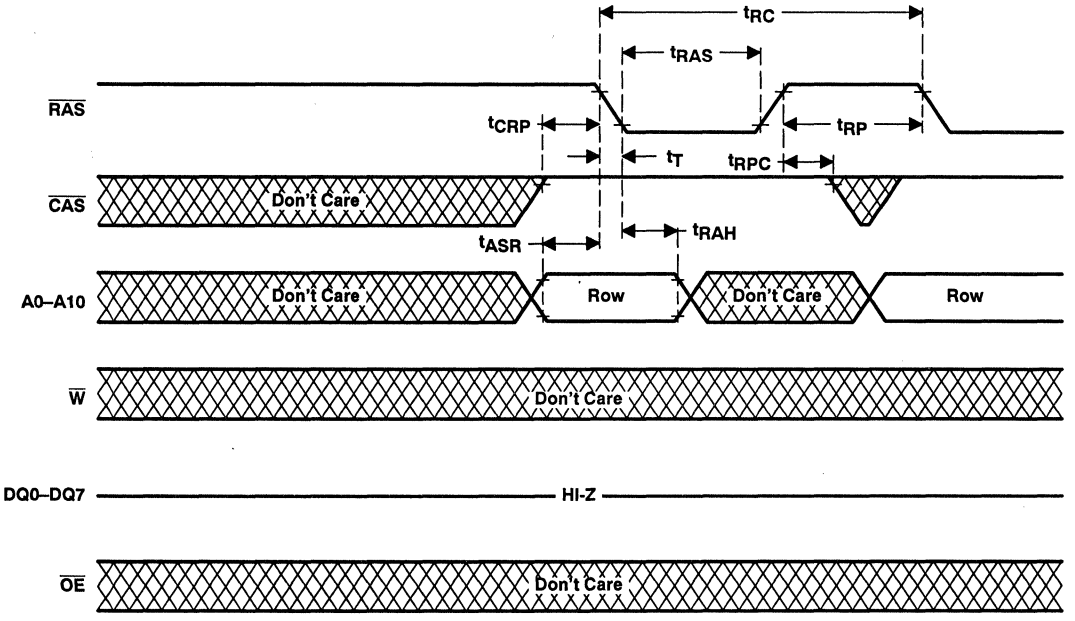

Figure 9. $\overline{\text{RAS}}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

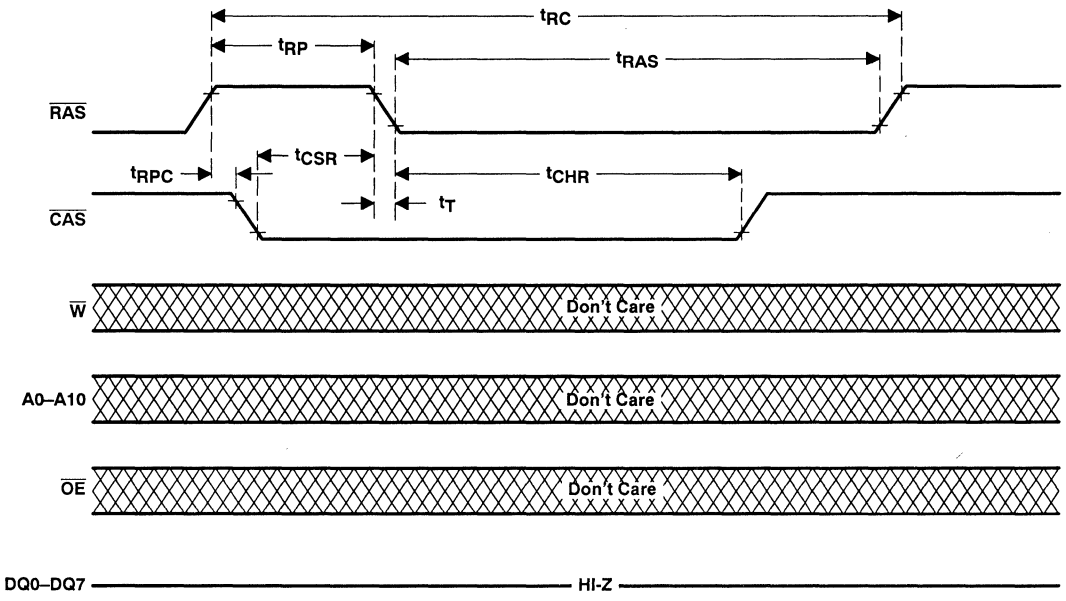

Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

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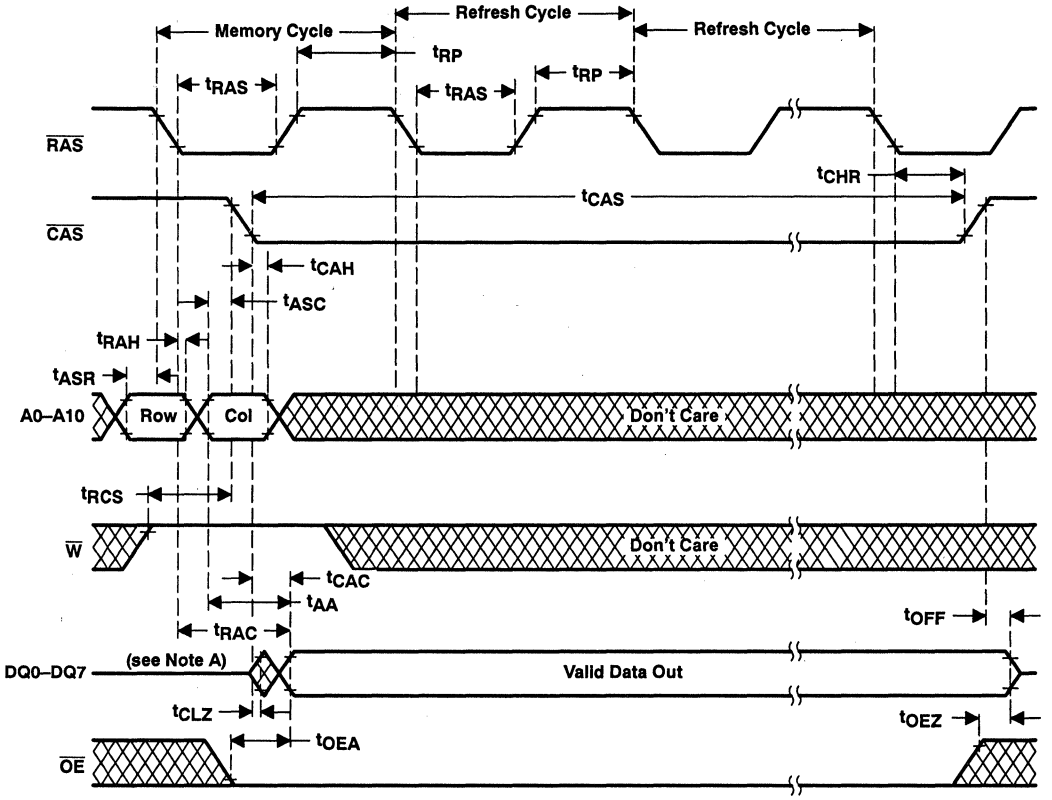
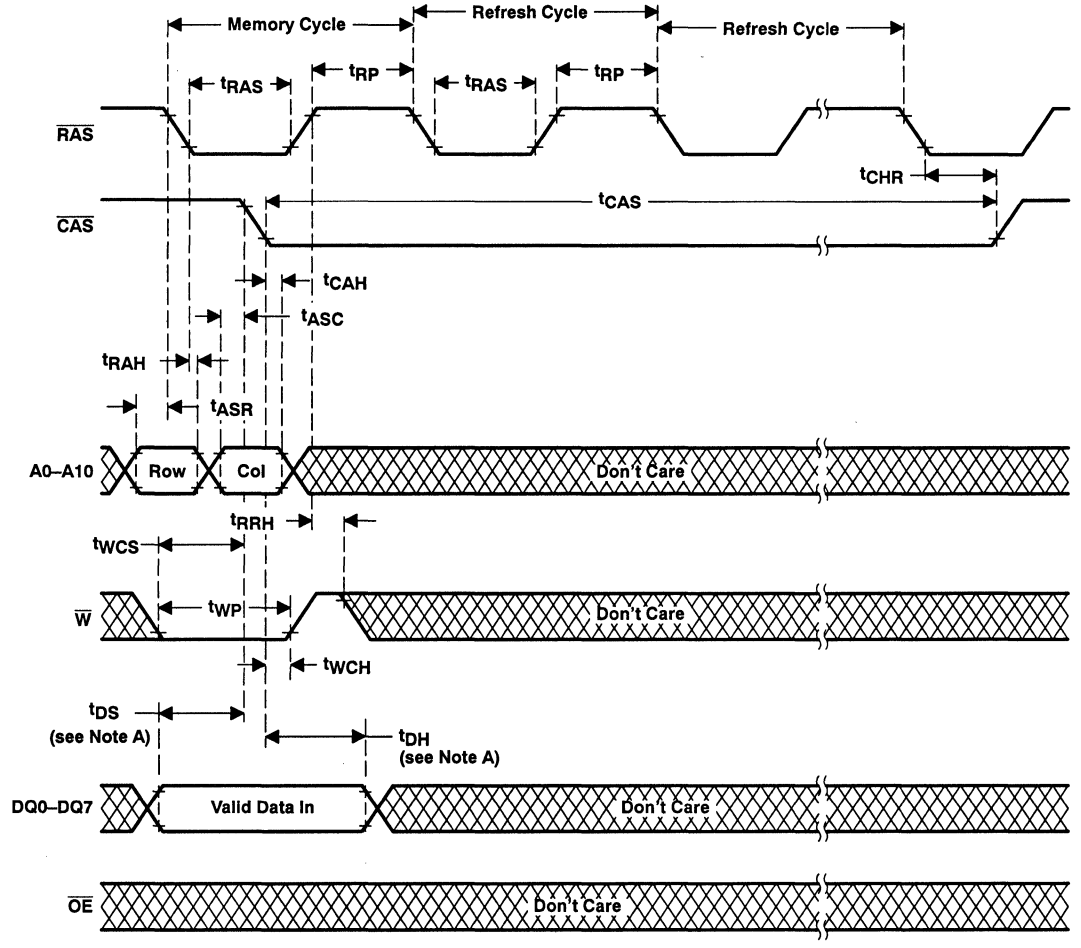
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 12. Hidden Refresh Cycle (Write)

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PARAMETER MEASUREMENT INFORMATION

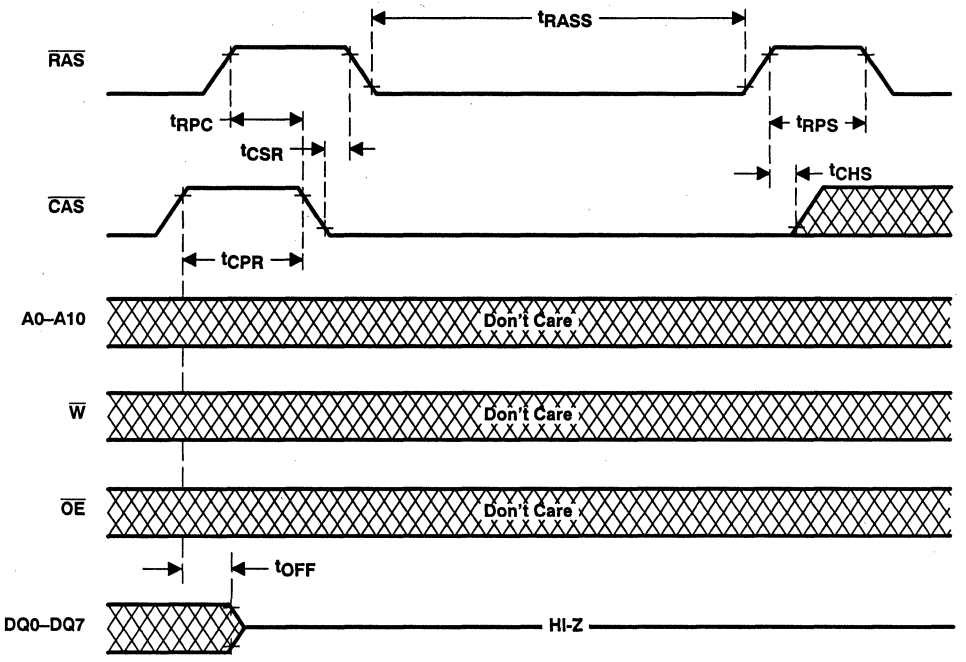
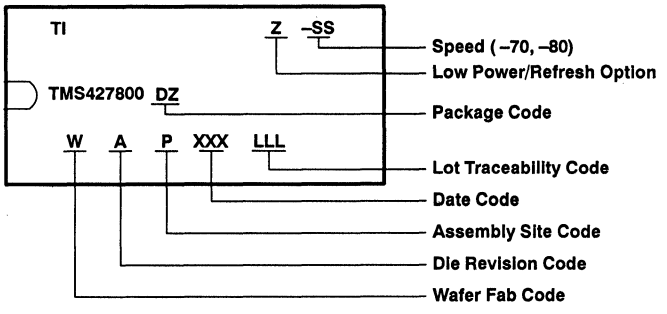


Figure 13. Self Refresh Timing

device symbolization



PRODUCT PREVIEW

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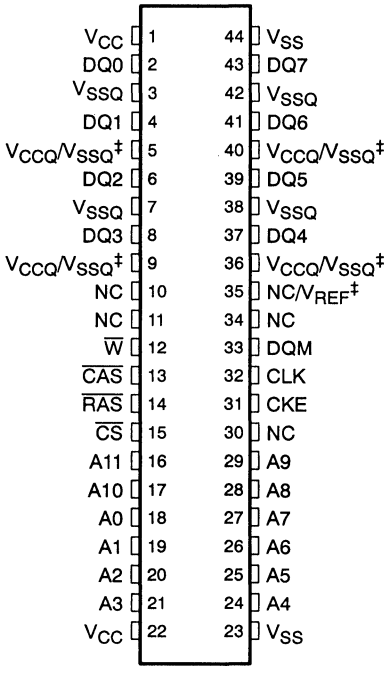
SMOS682–JANUARY 1993

- **Organization . . . 1M × 8 × 2 Banks**
- **3.3 V-Power Supply (10% Tolerance)**
- **Two Banks For On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 100-MHz Data Rates**
- **Burst Length Programmable to 1, 2, 4, or 8**
- **Programmable Output Sequence – Serial or Interleave**
- **Chip Select and Clock Enable For Enhanced System Interfacing**
- **Cycle-By-Cycle DQ Bus Mask Capability**
- **Programmable Read Latency From Column Address**
- **Self-Refresh Capability**
- **High-Speed, Low-Noise LVTTL and GTL Interfaces (SPICE Models Available)**
- **Interface Type (LVTTL or GTL) Automatically Sensed and Provided**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **4K Refresh (Total For Both Banks)**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME t_{CK} (MIN)	ACTV COMMAND TO READ OR WRT COMMAND t_{RCD} (MIN)	REFRESH TIME INTERVAL t_{REF} (MAX)
SDRAM-10	10 ns	30 ns	64 ms
SDRAM-12	12.5 ns	35 ns	64 ms
SDRAM-15	15 ns	40 ns	64 ms

DGE PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

‡ Pins 5, 9, 36, and 40 must be connected to V_{CCQ} and pin 35 must remain open (unconnected) for LVTTL Interface Operation. Pins 5, 9, 36, and 40 must be connected to V_{SSQ} and pin 35 must be connected to V_{REF} for GTL Interface Operation.

PIN NOMENCLATURE	
CLK	System Clock
$\overline{CS}$	Chip Select
CKE	Clock Enable
DQM	Data/Output Enable
A11	Bank Select
A0–A10	Address Inputs A0–A10 Row Addresses A0–A8 Column Addresses A10 Automatic Precharge Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Write Enable
DQ0–DQ7	SDRAM Data Inputs/Outputs
V_{CC}	Power Supply (3.3 V Typ)
V_{SS}	Ground
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{SSQ}	Ground for Output Drivers
V_{REF}	GTL Reference Voltage
NC	No External Connect

description

The Texas Instruments synchronous DRAM devices are high-speed 16 777 216-bit synchronous dynamic random-access memories, each organized as 2 banks of 1 048 576-words with 8-bits per word. The synchronous DRAM employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches. The synchronous DRAM series is

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compatible with both Low Voltage TTL (LVTTL) and Gunning Tranceiver Logic (GTL) input/output levels, by automatically sensing the interface arrangement and internally enabling the corresponding set of I/O drivers. These synchronous DRAMs are available in a variety of frequency performance ranges.

The synchronous DRAMs are available in a 400-mil, 44-pin surface mount TSOP II package (DGE suffix).

operation

All inputs of the synchronous DRAM are latched on the rising edge of the system (synchronous) clock. The synchronous DRAM outputs, DQ0–DQ7, are also referenced to the rising edge of CLK. The synchronous DRAM has two banks which are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles will refresh both banks alternately.

Five basic commands or functions control most operations of the synchronous DRAM:

- Bank activate/row address entry
- Column address entry/write operation
- Column address entry/read operation
- Bank deactivate
- $\overline{\text{CAS}}$-before $\overline{\text{RAS}}$ / self-refresh entry

Additionally, operation of the synchronous DRAM may be controlled by three methods: using chip select ($\overline{\text{CS}}$) to select/deselect the device; using DQM to enable/mask the DQ signals on a cycle-by-cycle basis; or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation. Refer to the following truth tables (Tables 1 through 3).

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Table 1. Basic Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9–A0	MNEMONIC
Mode register set	t = deac b = deac	L	L	L	L	X	X	A9=X A8=0 A7=0 A6=A5=X	MRS
Mode register read	t = deac b = deac	L	L	L	L	X	X	A9=X A8=1 A7=0 A6=A5=X	MRR
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column address entry/write operation with auto-deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column address entry/read operation with auto-deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	–	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control input inhibit/No operation	X	H	X	X	X	X	X	X	DESL

† For execution of these commands on cycle n, CKE (n–1) must be high and CKE (n) and DQM (n) are don't cares.
L = Logic low
H = Logic high
X = Don't care
V = Valid
t = Bank t
b = Bank b
actv = Activated
deac = Deactivated
BS = Logic high to select bank t; logic low to select bank b
SB = Bank selected by A11 at cycle n

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Table 2. CKE-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n–1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Continue current operation	X	L	L	X	X	X	X	–
Self-refresh entry‡	t = b = deac	H	L	L	L	L	H	SLFR
Power-down entry	t =b = no access§ operation	H	L	L	H	H	H	PDE
		H	L	H	X	X	X	PDE
Self-refresh/power-down exit	t =b = self-refresh/ power-down	L	H	L	H	H	H	–
		L	H	H	X	X	X	–
CLK suspend at n+1	t or b = access§ operation	H	L	X	X	X	X	HOLD
CLK suspend exit at n+1	t or b = access§ operation	L	H	X	X	X	X	–
CBR refresh‡	t = b = deac	H	H	L	L	L	H	REFR

† For execution of these commands, A0–A11 (n) and DQM (n) are don't cares.
‡ CBR or self refresh entry requires that all banks be deactivated, or in an idle state prior to the command entry.
n = CLK cycle number
L = Logic low
H = logic high
X = Don't care
V = Valid
t = Bank t
b = Bank b
actv = Activated
deac = Deactivated
burst = Data-in or data out cycle in progress at cycle n+1
§ An access operation refers to any READ (–P) or WRT (–P) command in progress at cycle n. Access operations include the cycle upon which the READ (–P) or WRT (–P) command is entered and all subsequent cycles through the completion of the access burst.

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Table 3. DQM-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	DQM (n)	D0–D7 (n)	$\overline{Q0}$–$\overline{Q7}$ (n+2)	MNEMONIC
–	t = deac and b = deac	X	N/A	HI-Z	–
–	t = actv and b = actv (no bursts)	X	N/A	HI-Z	–
Data-in enable	t = write or b = write	L	V	N/A	ENBL
Data-in mask	t = write or b = write	H	M	N/A	MASK
Data-out enable	t = read or b = read	L	N/A	V	ENBL
Data-out mask	t = read or b = read	H	N/A	HI-Z	MASK

† For execution of these commands, CKE (n–1) must be high and CKE (n) must be high. $\overline{CS}$ (n), $\overline{RAS}$ (n), $\overline{CAS}$ (n), $\overline{W}$ (n), and A0–A11 (n) are don't cares.
n = CLK cycle number
L = Logic low
H = logic high
X = Don't care
V = Valid
M = Masked input data
N/A = Not applicable
t = Bank t
b = Bank b
actv = Activated with no read or write operation in progress.
deac = Deactivated
write = Activated and accepting data-in on cycle n
read = activated and delivering data-out on cycle n+2

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burst sequence

All data for the SDRAM is written or read in a *burst* fashion. That is, a single starting address is entered into the device and then the SDRAM internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first may be at preceding as well as succeeding column addresses depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst. Refer to the following tables. The length of the burst sequence can be user-programmed to be either 1, 2, 4, or 8 accesses. After a read burst is completed (as determined by the programmed burst length) the outputs will be placed in a high-impedance state (see note below) until the next read access is initiated. Refer to the examples following the timing requirements and characteristics description (Figures 9 through 15).

NOTE: When using terminated DQ buses for GTL interfacing, turning off the output buffers at the device will result in the DQ lines pulling up to the terminating voltage, V_{TT}.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1 A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

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Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2 A1 A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data output cycle of a read burst may be be programmed to occur 1, 2, or 3 CLK cycles after the read command. Refer to the set mode register description. This feature allows the user to adjust the synchronous DRAM to operate in accordance with the system's capability to latch the data output from the synchronous DRAM. The delay between the READ command and the beginning of the output burst is known as *read latency* (also known as $\overline{CAS}$ latency). As described previously, after the initial output cycle has commenced, the data burst will occur at the CLK frequency without any intervening gaps. Use of minimum read latencies are restricted based on the particular maximum frequency rating of the synchronous DRAM.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. Note that the write latency is fixed and not determined by the mode register contents.

two-bank operation

The synchronous DRAM contains two independent banks, which can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank activate/row address entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank may be deactivated either automatically during a READ or a WRT command (READ-P or WRT-P) or by use of the deactivate banks (DEAC) command. Both banks may be deactivated at once by use of the DCAB command. Refer to Table 1 and the following bank deactivation description.

The availability of two banks allows enhanced performance and a wider variety of possible combinations and methods of data access for the user to choose from, based on the system needs.

two-bank row access operation

The two-bank feature allows the user to access information on random rows at a higher rate of operation than is possible with a standard DRAM. This may be accomplished by activating one bank with a row address as described previously. Then, while the data stream is being accessed to/from that bank, the second bank can be activated with another row address. When the data stream to/from the first bank is complete, the data stream to/from the second bank can commence without interruption. After the second bank is activated, the first bank could be deactivated to allow the entry of of new row address for the next round of accesses. In this manner, operation could continue on in an interleaved "ping-pong" fashion. Refer to the examples following the timing requirements and characteristics description. (Refer Figures 9 through 15.)

two-bank column access operation

The availability of two banks also allows the user to access data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), the user can use A11 to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Refer to the examples following the timing requirements and characteristics description. (Refer Figures 9 through 15.)

bank deactivation (precharge)

Both banks may be simultaneously deactivated (placed in precharge) by use of the DCAB command. The DCAB command is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ low, and A10 high on the rising edge of CLK. A single bank may be deactivated by use of the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 will select the bank to be precharged. A bank may also be deactivated automatically by use of A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, then the accessed bank (selected by A11) will automatically be deactivated upon completion of the access burst. If A10 is held low during READ or WRT command entry then that bank will remain active following the burst. The READ and WRT commands with automatic deactivation are denoted READ-P and WRT-P. Refer to Table 1.

chip select

$\overline{CS}$, or chip select, can be used to select or deselect the synchronous DRAM for command entry, such as might be required for multiple memory device decoding. If $\overline{CS}$ is held high on the rising edge of CLK, (DESL command) the device will not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ input until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command may be entered simultaneously on the same rising CLK edge of the select operation. The device may be selected/deselected on a cycle-by-cycle basis. (Refer to Table 1 and Table 2.) Note that use of $\overline{CS}$ will not affect an access burst that is in progress; the DESL command can only restrict $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the SDRAM.

data/output mask

Masking of individual data cycles within a burst sequence may be accomplished by use of the MASK command (see Table 3). During a write burst, if DQM is held high on the rising edge of CLK, then the incident (referenced to the same rising edge of CLK) data word on DQ0–DQ7 will be ignored. For a read burst, if DQM is held high on the rising edge of CLK, then DQ0–DQ7 referenced to the second next rising edge of CLK will be placed in HI-Z (see note below). Therefore, the application of DQM to data output cycles (READ burst) involves a latency of 2 CLK cycles, while the application of DQM to data-in cycles (WRITE burst) has no latency. Also note that the MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read or a write burst sequence. Refer to Figure 11 and the examples following the timing requirements and characteristics description.

NOTE: When using terminated DQ buses for GTL interfacing, turning off the output buffers at the device will result in the DQ lines pulling up to the terminating voltage, V_{TT}.

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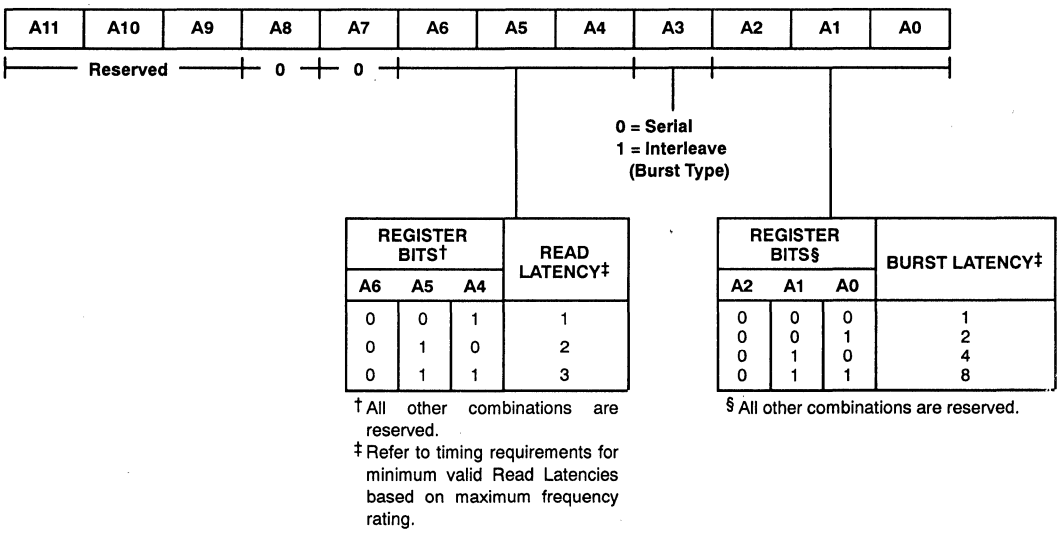
CLK suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE is made low during the execution of a READ (or READ-P) or WRT (or WRT-P) operation, then the state of the DQ bus occurring at the immediate next rising edge of CLK will be "frozen" at its current state and no further inputs will be accepted until CKE is returned high. This is known as a CLK suspend operation and its execution is denoted as a HOLD command. The device will resume operation from the point at which it was placed in suspension beginning with the second rising edge of CLK after CKE is returned high.

If CKE is brought low when no READ (or READ-P) or WRT (or WRT-P) command is in progress, then the device will enter power-down mode. If both banks are deactivated when power-down mode is entered, then power consumption will be reduced to the minimum. Power-down mode may be used during row active or CBR refresh periods to reduce input buffer power. After power-down mode has been entered, no further inputs will be accepted until CKE is returned high. When exiting power-down mode, new commands may be entered on the first CLK edge after CKE is returned high, provided that t_{CESP} is satisfied. If $t_{CESP} > t_{CK}$, then NOOP or DESL commands must be entered until t_{CESP} is met. Note that CLK must be active and stable (if CLK was turned off for power-down) before CKE is returned high. Refer to Table 2 and Figure 14. Also see the self-refresh description.

mode register set

The synchronous DRAM contains a mode register, which should be programmed by the user with the read latency length, the burst type, and the burst length. This is accomplished by executing a MRS command with the information being entered on the address lines A0–A8. Bits A9–A11 are reserved for later, or manufacturer's use. A logic 0 should always be entered on A7 and A8, but A9–A11 are don't care entries for the synchronous DRAM. (Refer to Figure 1.)



REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	1	1
0	1	0	2
0	1	1	3

† All other combinations are reserved.

‡ Refer to timing requirements for minimum valid Read Latencies based on maximum frequency rating.

REGISTER BITS§			BURST LATENCY‡
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

§ All other combinations are reserved.

Figure 1. Mode Register Programming

The MRS command is executed by holding $\overline{RAS}$ low, $\overline{CAS}$ low, $\overline{W}$ low, and the input mode word valid on A0–A8 on the rising edge of CLK (refer to Table 1). The MRS command can be executed only following the deactivation of both banks.

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mode register read

To read back the contents of the mode register, a MRR command can be entered, which is identical to the MRS command described previously, except that A8 should be held high instead of low. The DQ bus will enter the low impedance state on the first CLK edge after the MRR command is entered (refer to parameter t_{LZ}). The lower nibble of the mode register, bits 0, 1, 2, 3, will be available on the DQ1, DQ3, DQ4, and DQ6 outputs, correspondingly, at the fourth CLK edge after the MRR command is entered. The output data will be held for the time specified by t_{OH} after the fourth CLK edge. Bits 4, 5, 6 of the mode register will be available on the DQ1, DQ3, and DQ4 outputs, correspondingly, at the sixth CLK edge after the MRR command is entered. The output data will be held for the time specified by t_{OH} after the sixth CLK edge. A new command can be entered on or after the eighth CLK edge occurring after entry of the MRR command. Refer to Figure 2.

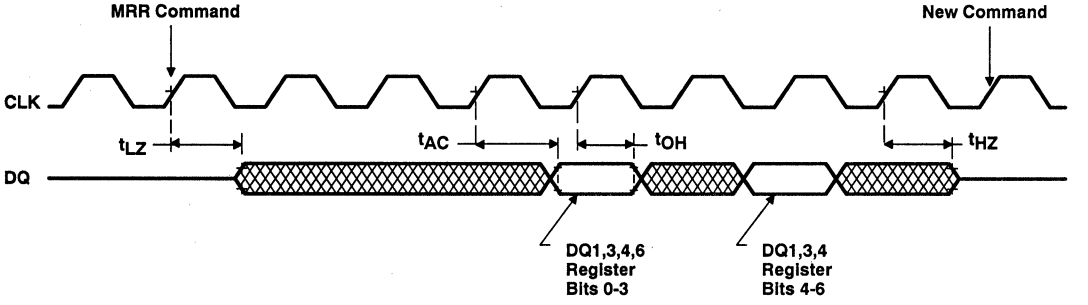

Figure 2. Mode Register Read

refresh

The synchronous DRAM must be refreshed at intervals not exceeding t_{REF} (refer to the parameter timing requirements), or data may not be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, or by performing 4096 $\overline{CAS}$-before-$\overline{RAS}$ (REFR) commands, or by placing the device in self-refresh. Regardless of the method used, refresh must be accomplished before t_{REF} has expired.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

Before performing a $\overline{CAS}$-before-$\overline{RAS}$ refresh, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ must be low, $\overline{CAS}$ must be low, and $\overline{W}$ must be high upon the rising edge of CLK (refer to Table 2). The refresh address is generated internally such that after 4096 REFR commands, both banks of the SDRAM will have been refreshed. The external address and bank select (A11) are ignored. Note that execution of a REFR command will automatically deactivate both banks upon completion of the internal CBR cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

self-refresh

To enter self-refresh, both banks of the synchronous DRAM must first be deactivated. Following this, a SLFR command should be executed (refer to Table 2). The SLFR command is identical to the REFR command decribed previously, except that CKE is low. Note that for proper entry of the SLFR command, CKE should be brought low only for the same rising edge of CLK that $\overline{RAS}$ and $\overline{CAS}$ are brought low and $\overline{W}$ is brought high. (Otherwise the device would enter power-down mode.) In the self-refresh mode, all refreshing signals are generated internally for both banks, with all external signals (except CKE) being ignored. Data can be retained by the device automatically for an indefinite period as long as power is maintained (consumption is reduced to a minimum). To exit self-refresh mode, CKE should be returned high. Following this, new commands can then

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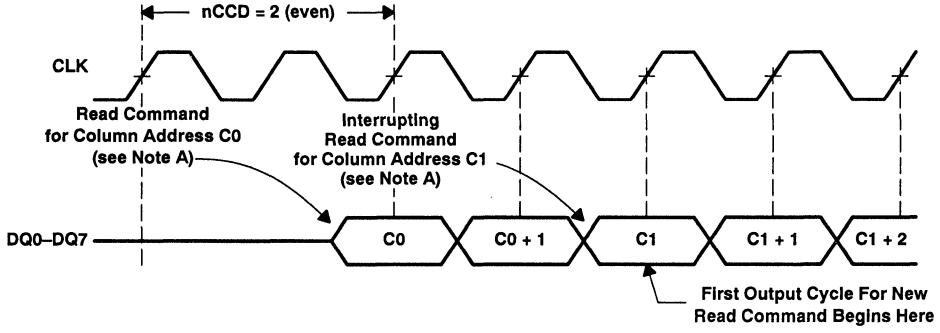
be issued after t_{RC} has expired. Note that if CLK is made inactive during self-refresh, it must be returned to an active and stable condition before CKE is brought high to exit self-refresh. Refer to Figure 15 following the timing requirements and electrical characteristics description.

interrupted bursts

A read or write may be interrupted before the burst sequence has been completed with no adverse performance, by entering certain superseding commands and providing that all timing requirements are met (refer to timing requirements and electrical characteristics). Note that the command interrupting either a read or a write burst should be entered only on an even number of cycles from the initial burst command (nCCD). Note also that interruption of READ-P and WRT-P operations is not supported.

Table 7. Read Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
DEAC, DCAB	Note that the DQ bus will be placed in high-impedance state when nHZP is satisfied or upon completion of the read burst, whichever occurs first. (Refer to Figure 16.)
WRT, WRT-P	The WRT command immediately supersedes the read burst in progress, but note that DQM must be made high nDOD CLK cycles previous to the WRT (or WRT-P) command entry to avoid DQ bus contention. (Refer to Figure 4.)
READ, READ-P	Current output cycles will continue until the programmed latency from the superseding READ (or READ-P) command has been met, after which the new output cycles will begin. (Refer to Figure 3.)
STOP	The DQ bus will be placed in high-impedance state two clock cycles after the stop command is entered or upon completion of the read burst, whichever occurs first. The bank will remain active.



NOTE A: For the purposes of this example Read Latency = 2, and Burst Length > 2.

Figure 3. Read Burst Interrupted By Read Command

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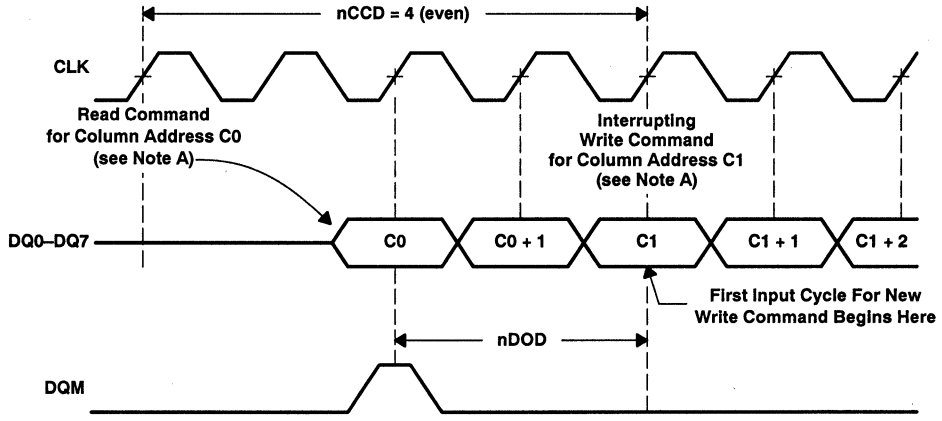


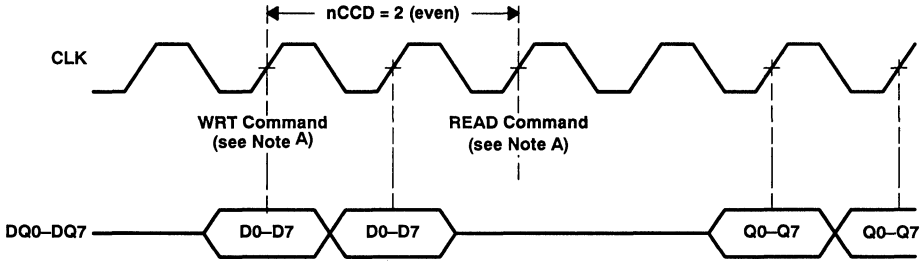
NOTE A: For the purposes of this example Read Latency = 2, and Burst Length > 2.

Figure 4. Read Burst Interrupted By Write Command

PRODUCT PREVIEW

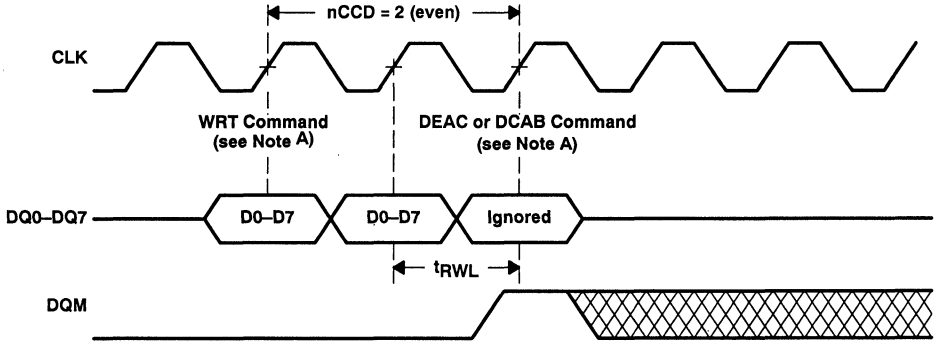
Table 8. Write Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. Note that DQM must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt. (Refer to Figure 6.)
WRT, WRT-P	The new WRT (or WRT-P) command and data-in immediately supersede the write burst in progress.
READ, READ-P	Data-in on previous cycle will be written. No further data-in will be accepted. (Refer to Figure 5.)
STOP	The data on the input pins at the time of the burst STOP command will not be written, and no further data will be accepted. The bank will remain active.



NOTE A: For the purposes of this example, Read Latency = 2, Burst Length > 2, and $t_{CK} = t_{RWL}$.

Figure 5. Write Burst Interrupted By Read Command



NOTE A: For the purposes of this example, Read Latency = 2, Burst Length > 2, and $t_{CK} = t_{RWL}$.

Figure 6. Write Burst Interrupted By DEAC/DCAB Command

power up

After power up to the full V_{CC} level, a 200-µs pause should be allowed (no input except CLK), after which both banks of the device must be deactivated (placed in precharge) and the mode register should be set. Eight REFR commands should then be performed to complete the device initialization. (Refer to Tables 1 and 2, and the set mode register description.)

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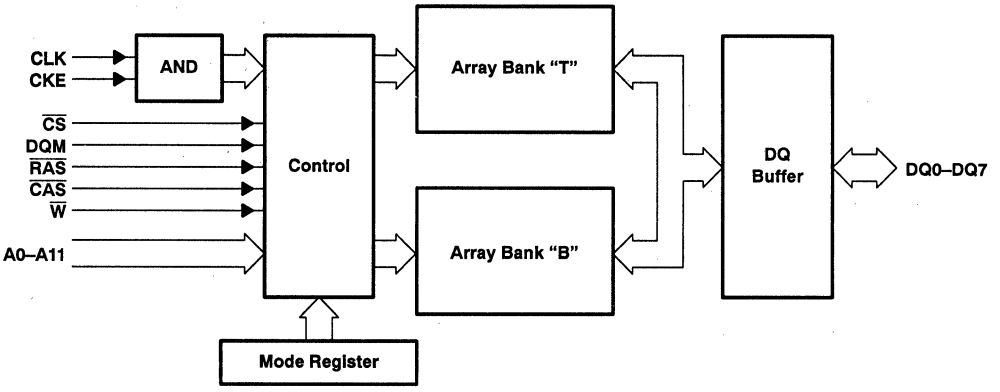
functional block diagram



absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) . . . . . – 0.5 to 4.6 V
Voltage range on V_{CC} . . . . . – 0.5 to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this datasheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER		LVTTL INTERFACING			GTL INTERFACING			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3	3.3	3.6	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{TT}	GTL terminator voltage				1.08	1.2	1.32	V
V_{REF}	GTL reference voltage				$2\ V_{TT}/3 - 2\%$	0.8	$2V_{TT}/3+2\%$	V
V_{IH}	High-level input voltage	2		$V_{CC}+0.3$	$V_{REF}+0.05$‡	1.2		V
V_{IL}	Low-level input voltage	– 0.3		0.8		0.4	$V_{REF}–0.05$‡	V
T_A	Operating free-air temperature	0		70	0		70	°C

‡ V_{IH} and V_{IL} levels are only for DC testing. For AC timing, V_{IH} of 1.2 V and V_{IL} of 0.4 V should be used.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			SDRAM-10			SDRAM-12			SDRAM-15			UNIT
					MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH}= −2 mA		LVTTL	2.4			2.4			2.4			V
		$\|I_{OH}\| \le 10\ \mu A$		GTL	V_{TT} − 0.05	1.2		V_{TT} − 0.05	1.2		V_{TT} − 0.05	1.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		LVTTL			0.4			0.4			0.4	V
		I_{OL} = 32 mA		GTL			0.4			0.4			0.4	
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}					±10			±10			±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC} + 0.3 V, Output disabled					±10			±10			±10	µA
I_{CC1}	Average read or write current	t_{RC} = min		1 bank active			90			80			70	mA
				2 banks active			160			150			125	mA
I_{CC2}	Standby current	Both banks deactivated	CKE = V_{IH}	LVTTL			16			16			16	mA
				GTL			20			20			20	
			CKE = V_{IL}	LVTTL			2			2			2	
				GTL			3			3			3	
			CKE = 0 V (CMOS)	LVTTL			1			1			1	
		One or both banks active	CKE = V_{IL}	LVTTL			4			4			4	
				GTL			5			5			5	
I_{CC3}	Consecutive CBR commands	t_{RC} = min					90			80			70	mA
I_{CC4}	Burst current, gapless burst	t_{CK} = min					120			100			80	mA
I_{CC6}	Self-refresh current	CKE = V_{IL}		LVTTL			2			2			2	mA
				GTL			3			3			3	mA
		CKE = 0 V (CMOS)		LVTTL			1			1			1	mA

NOTE 2: All specifications apply to the device after power-up initialization.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

		MIN	NOM	MAX	UNT
$C_{i(S)}$	Input capacitance, CLK input			7	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A11, $\overline{CS}$, DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$			5	pF
$C_{i(E)}$	Input capacitance, CKE input			5	pF
C_o	Output capacitance			10	pF

NOTE 3: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER†			SDRAM-10		SDRAM-12		SDRAM-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	CLK (system clock) cycle time	Read Latency = 1	30		35		40		ns
		Read Latency = 2	15		17.5		20		
		Read Latency = 3	10		12.5		15		
t_{CKH}	CLK (system clock) high pulse duration		3		3.5		4		ns
t_{CKL}	CLK (system clock) low pulse duration		3		3.5		4		ns
t_{AC}	Data-out access from CLK (see Note 4)	Read Latency = 1	28		33		38		ns
		Read Latency = 2	13		15		18		
		Read Latency = 3	8		10		12		
t_{OH}	Data-out hold from CLK		2		2		2		ns
t_{LZ}	CLK to DQ LO-Z (see Note 5)		0		0		0		ns
t_{HZ}	CLK to DQ HI-Z (see Note 6)			7		7		7	ns
t_{DS}	Data-in setup time		2		2		2		ns
t_{AS}	Address setup time		2		2		2		ns
t_{CS}	Control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM) setup time		2		2		2		ns
t_{CES}	CKE setup time (suspend entry/exit, power-down entry)		2		2		2		ns
t_{CESP}	CKE setup time (power-down exit) (see Note 7)		8		10		12		ns
t_{DH}	Data-in hold time		2		3		4		ns
t_{AH}	Address hold time		2		3		4		ns
t_{CH}	Control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQM) hold time		2		3		4		ns
t_{CEH}	CKE hold time		2		3		4		ns
t_{RC}	REFR command to ACTV, MRS, or REFR command; Self-refresh exit to ACTV, MRS, or REFR command		100		110		130		ns
t_{RAS}	ACTV command to DEAC or DCAB command		60	100 000	70	100 000	80	100 000	ns
t_{RCD}	ACTV command to READ or WRT command		30		35		40		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, or REFR command		40		40		50		ns
t_{APR}	Final data-out of READ-P operation to ACTV, MRS, or REFR command		t_{RP} + (nEP * t_{CK})						ns

† A command, data-in, or data-out is referenced at the rising transition of CLK.
Setup and hold times are referenced to the rising transition of CLK.
The reference level used for timing measurements is 1.4 V for LVTTL, and 0.8 V for GTL.
AC measurements assume t_T = 1 ns.
All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted.
All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted.
All specifications referring to consecutive commands are specified as consecutive commands for the same bank, unless otherwise noted.
Note that a CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during a HOLD operation).

NOTES: 4. t_{AC} is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data-out t_{AC} is referenced from the rising transition of CLK that is Read Latency – 1 cycles after the READ command.
5. t_{LZ} is measured from the rising transition of CLK that is Read Latency – 1 cycles after the READ command.
6. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
7. If $t_{CESP} > t_{CK}$, then NOOP or DESL commands must be entered until t_{CESP} is met. Note that CLK must be active and stable (if CLK was turned off for power-down) before CKE is returned high.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER†			SDRAM-10		SDRAM-12		SDRAM-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{APW}	Final data-in of WRT-P operation to ACTV, MRS, or REFR command		60		60		80		ns
t_{RWL}	Final data-in to DEAC or DCAB command		20		20		30		ns
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		20		25		30		ns
t_T	Transition time, all inputs (see Note 7)		1	5	1	5	1	5	ns
t_{REF}	Refresh interval			64		64		64	ms
nEP	Final data-out to DEAC or DCAB command	Burst Length > 1, Read Latency = 1	0		0		0		cycles
		Burst Length > 1, Read Latency = 2	–1		–1		–1		
		Burst Length > 1, Read Latency = 3	–2		–2		–2		
		Burst Length = 1, Read Latency = 1	1		1		1		
		Burst Length = 1, Read Latency = 2	0		0		0		
		Burst Length = 1, Read Latency = 3	–1		–1		–1		
nHZP	DEAC or DCAB interrupt of data-out burst to DQ HI-Z (see Note 8)	Read Latency = 1	1		1		1		cycles
		Read Latency = 2	2		2		2		
		Read Latency = 3	3		3		3		
nCCD	READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command (i = 1, 2, 3, . . .) (see Note 9)		2i		2i		2i		cycles
nCWL	Final data-in to READ command in either bank		1		1		1		cycles
nWCD	WRT command to first data-in		0	0	0	0	0	0	cycles
nDID	ENBL or MASK command to data-in		0	0	0	0	0	0	cycles
nDOD	ENBL or MASK command to data-out		2	2	2	2	2	2	cycles
nCLE	HOLD command to suspended CLK edge; HOLD operation exit to entry of any command		1	1	1	1	1	1	cycles
nRSA	MRS command to ACTV command		2		2		2		cycles
nCDD	DESL command to control input inhibit		0	0	0	0	0	0	cycles

† A command, data-in, or data-out is referenced at the rising transition of CLK.
Setup and hold times are referenced to the rising transition of CLK.
The reference level used for timing measurements is 1.4 V for LVTTL, and 0.8 V for GTL.
AC measurements assume t_T = 1 ns.
All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted.
All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted.
All specifications referring to consecutive commands are specified as consecutive commands for the same bank, unless otherwise noted.
Note that a CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

NOTES: 8. Transition time, t_T, is measured between V_{IH} and V_{IL}.
9. A data-out burst may be interrupted only on an even number of clock cycles after the initial READ command is entered (refer to nCCD). Note that interruption of READ-P and WRT-P operations is not supported.
10. A read or write burst can only be interrupted at even number cycle intervals after entry of the initial READ or WRT command. The nCCD specification applies only for the interruption of read or write bursts.

Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters

			SDRAM-10					SDRAM-12				SDRAM-15			UNITS
	Operating frequency		100	80	66	50	33	80	66	50	33	66	50	33	MHz
t_{CK}	CLK (system clock) cycle time		10	12.5	15	20	30	12.5	15	20	30	15	20	30	ns
	KEY PARAMETER		**NUMBER OF CYCLES REQUIRED**												
	Read latency, min programmed value		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	3	2	2	1	3	3	2	2	3	2	2	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		6	5	4	3	2	6	5	4	3	6	4	3	cycles
t_{RP}	DEAC or DCAB command to ACTV, MODE, or REFR command		4	4	3	2	2	4	3	2	2	4	3	2	cycles
t_{RC}	REFR command to ACTV, mode, or REFR command; self-refresh exit to ACTV, MODE, or REFR command		10	8	7	5	4	9	8	6	4	9	7	5	cycles
t_{RWL}	Final Data-in to DEAC or DCAB command		2	2	2	1	1	2	2	1	1	2	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	1	1	2	2	2	1	2	2	1	cycles
t_{APR}	Final data-out of READ-P operation to ACTV, MRS, or REFR command	Read Latency = 3	2	2	1	0	0	2	1	0	0	2	1	0	cycles
		Read Latency = 2	–	–	2	1	1	–	–	1	1	–	2	1	cycles
		Read Latency = 1	–	–	–	–	2	–	–	–	–	–	–	–	cycles
t_{APW}	Final data-in of WRT-P operation to ACTV, MODE or REFR command		6	5	4	3	2	5	4	3	2	6	4	3	cycles

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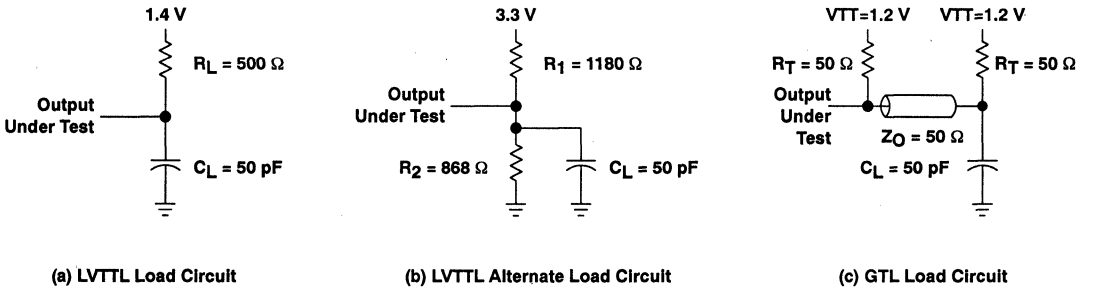
PARAMETER MEASUREMENT INFORMATION



(a) LVTTL Load Circuit (b) LVTTL Alternate Load Circuit (c) GTL Load Circuit

Figure 7. Synchronous DRAM Load Circuits

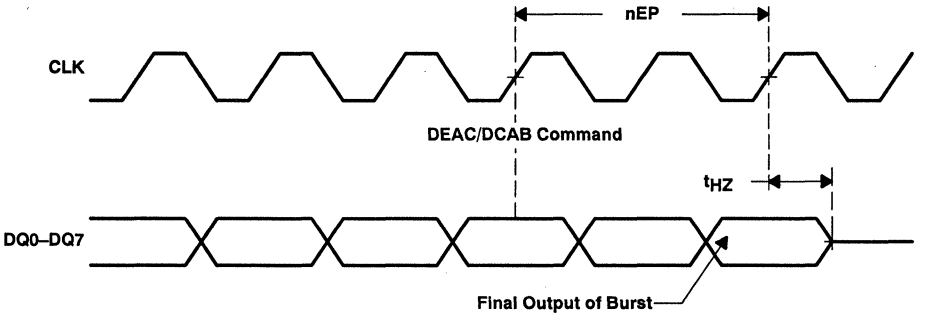


Figure 8. nEP (Assume Read Latency = 3)

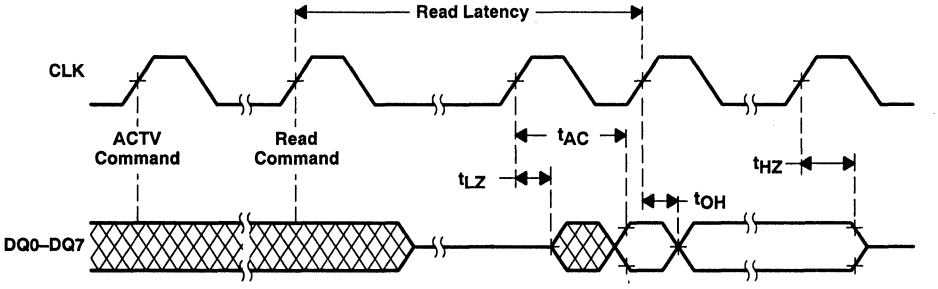


Figure 9. Output Parameters

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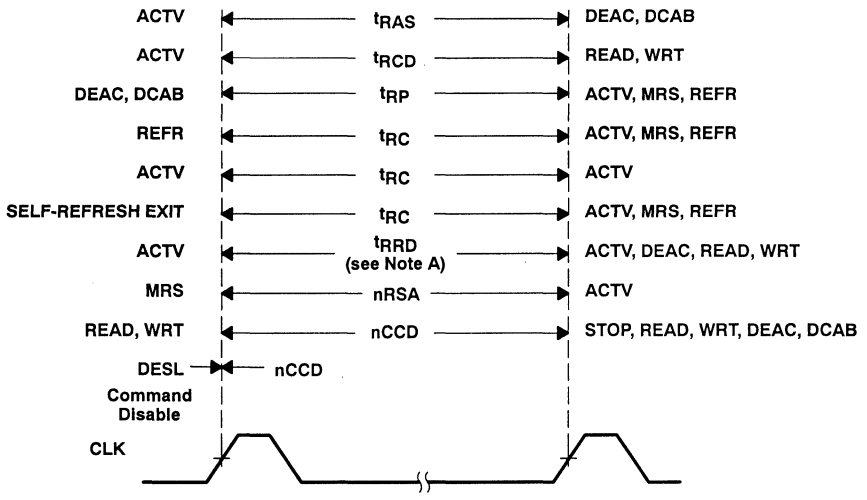
PARAMETER MEASUREMENT INFORMATION



NOTE A: t_{RRD} is specified for command execution in one bank to command execution in the other bank.

Figure 10. Command to Command Parameters

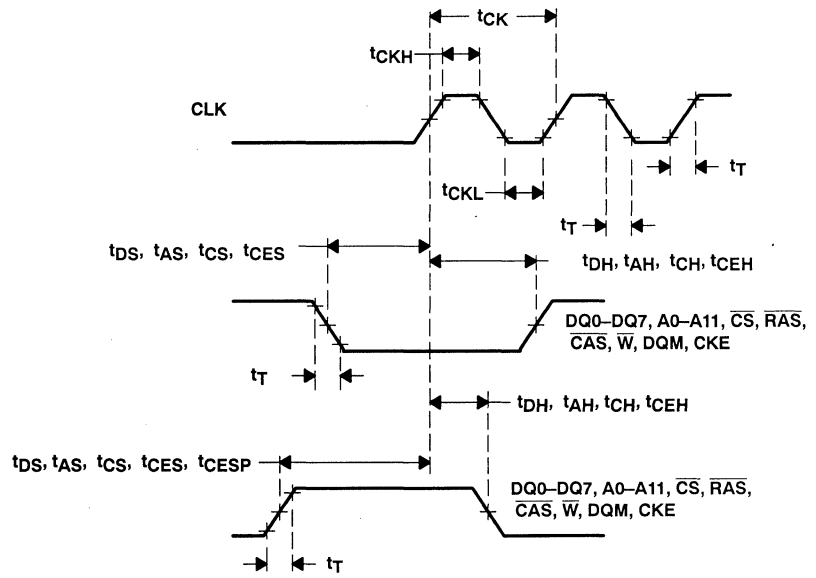


Figure 11. Input Attribute Parameters

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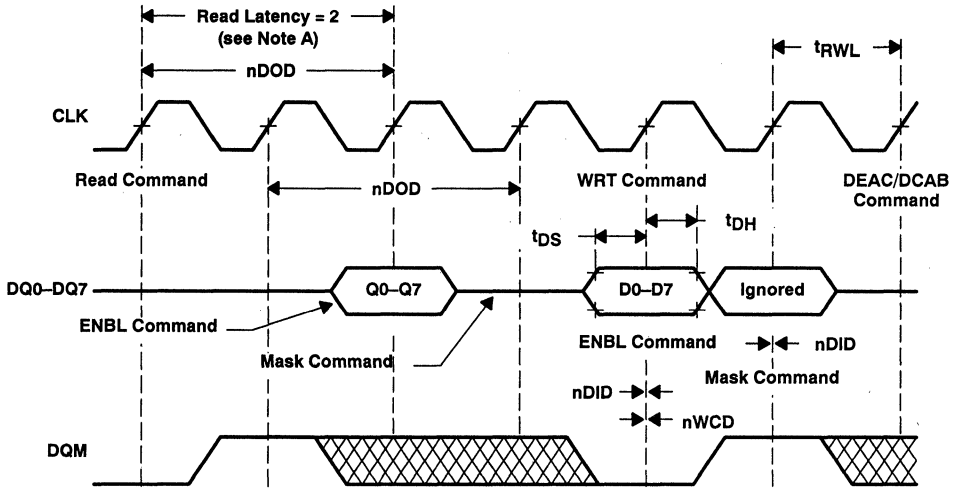
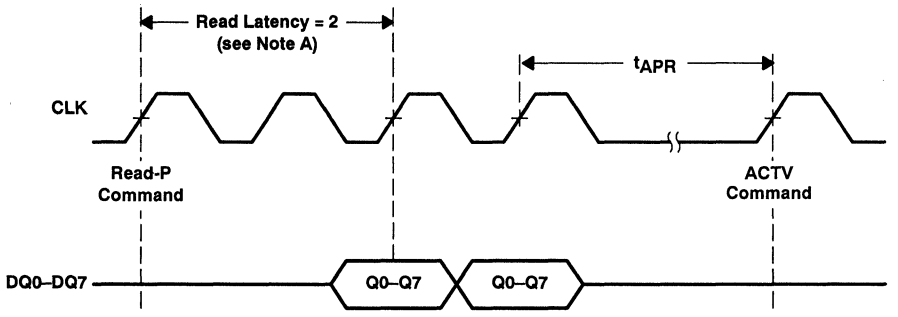
PARAMETER MEASUREMENT INFORMATION



NOTE A: For purposes of this example assume Read Latency = 2, and Burst Length = 2.

Figure 12. DQ Parameters



NOTE A: For purposes of this example assume Read Latency = 2, and Burst Length = 2.

Figure 13. Read Automatic Deactivate (Autoprecharge)

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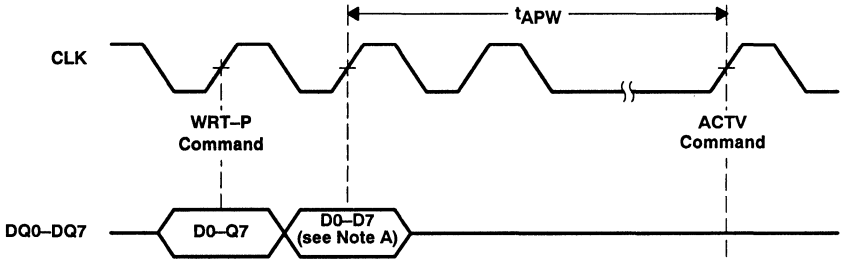
PARAMETER MEASUREMENT INFORMATION



NOTE A: For purposes of this example the Burst length = 2.

Figure 14. Write Automatic Deactivate (Autoprecharge)

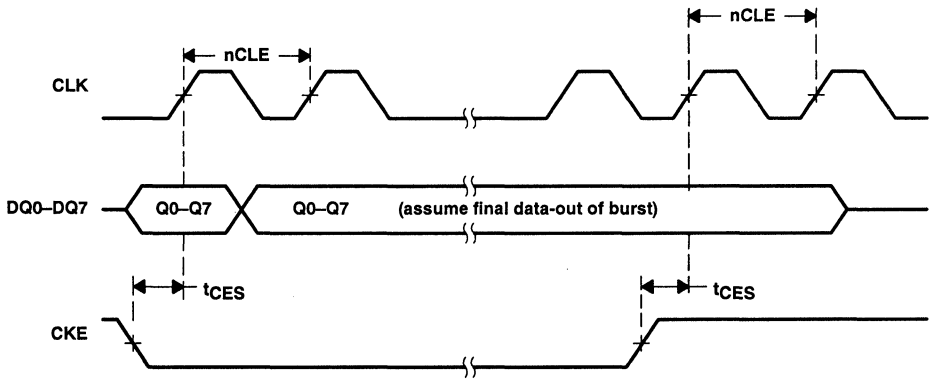


Figure 15. Figure 12. CLK Suspend Operation

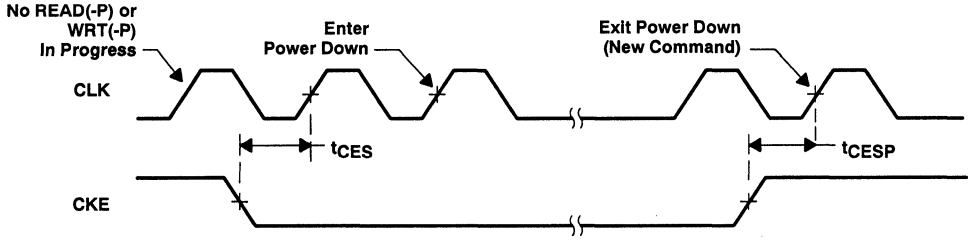
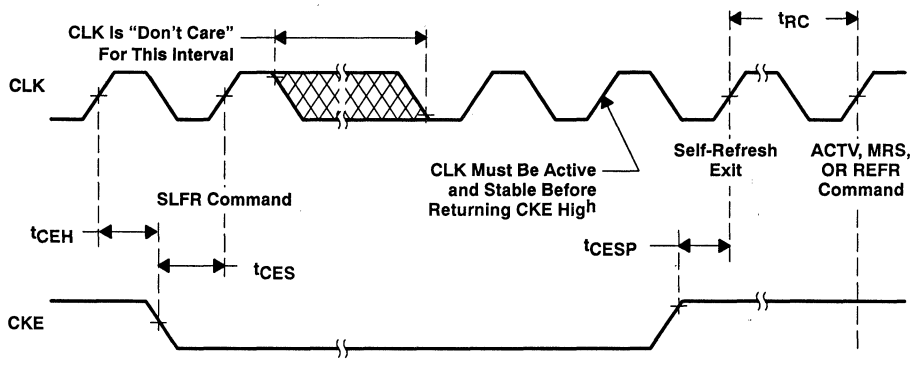


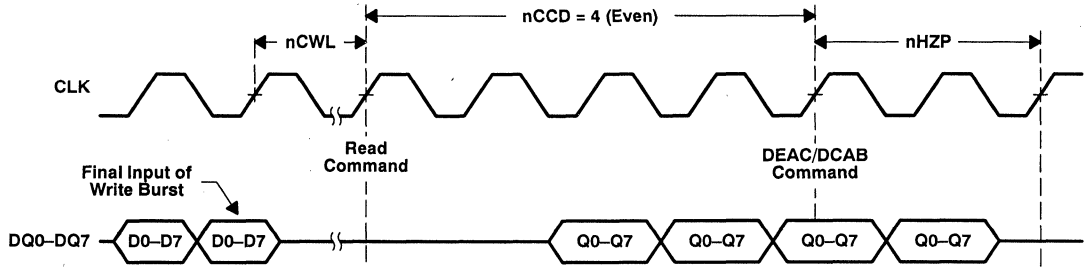
Figure 16. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION



NOTE: Assume both banks are previously deactivated.

Figure 17. Self-Refresh Entry/Exit



NOTE: Assume read latency = 2 and burst length = 8.

Figure 18. Write Burst Followed By DEAC/DCAB–Interrupted Read

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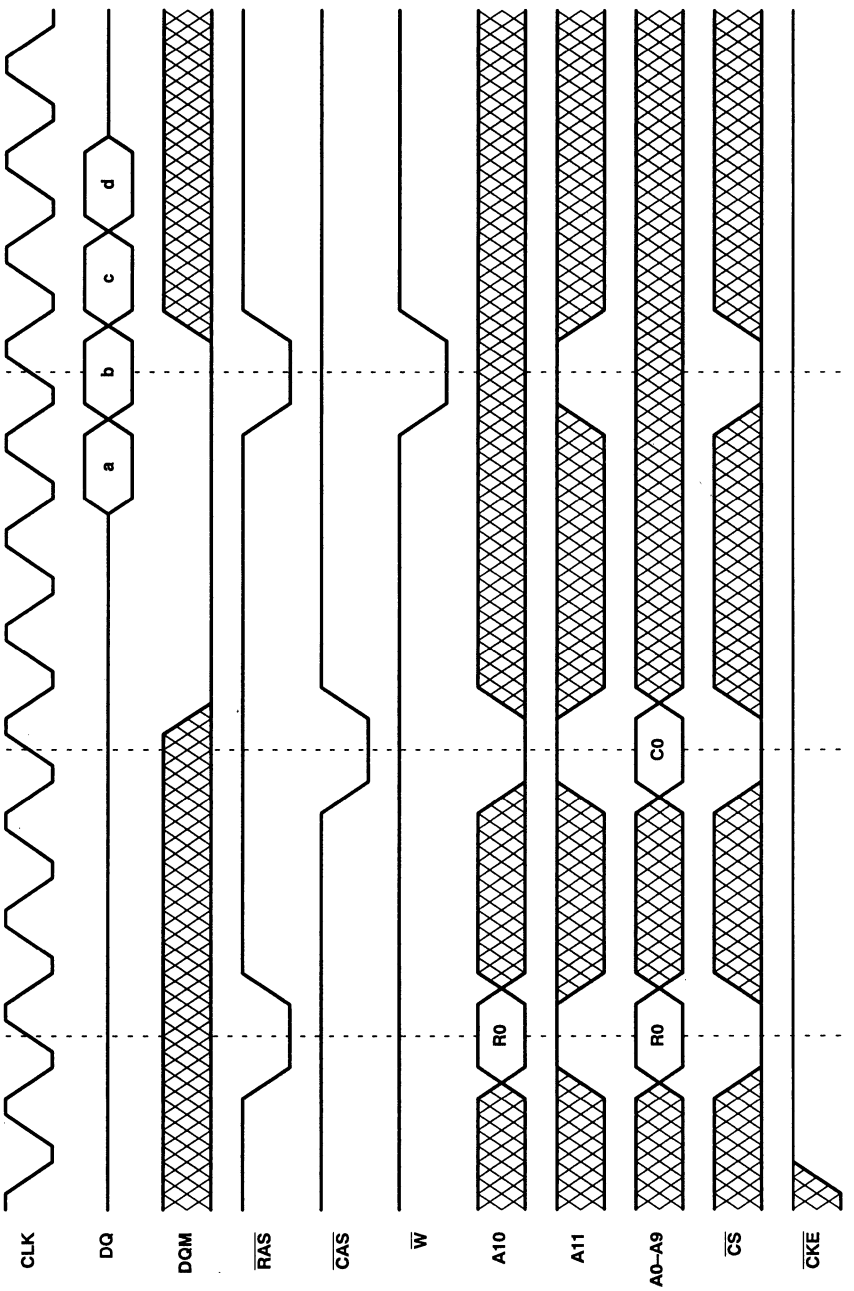


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
Q	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3

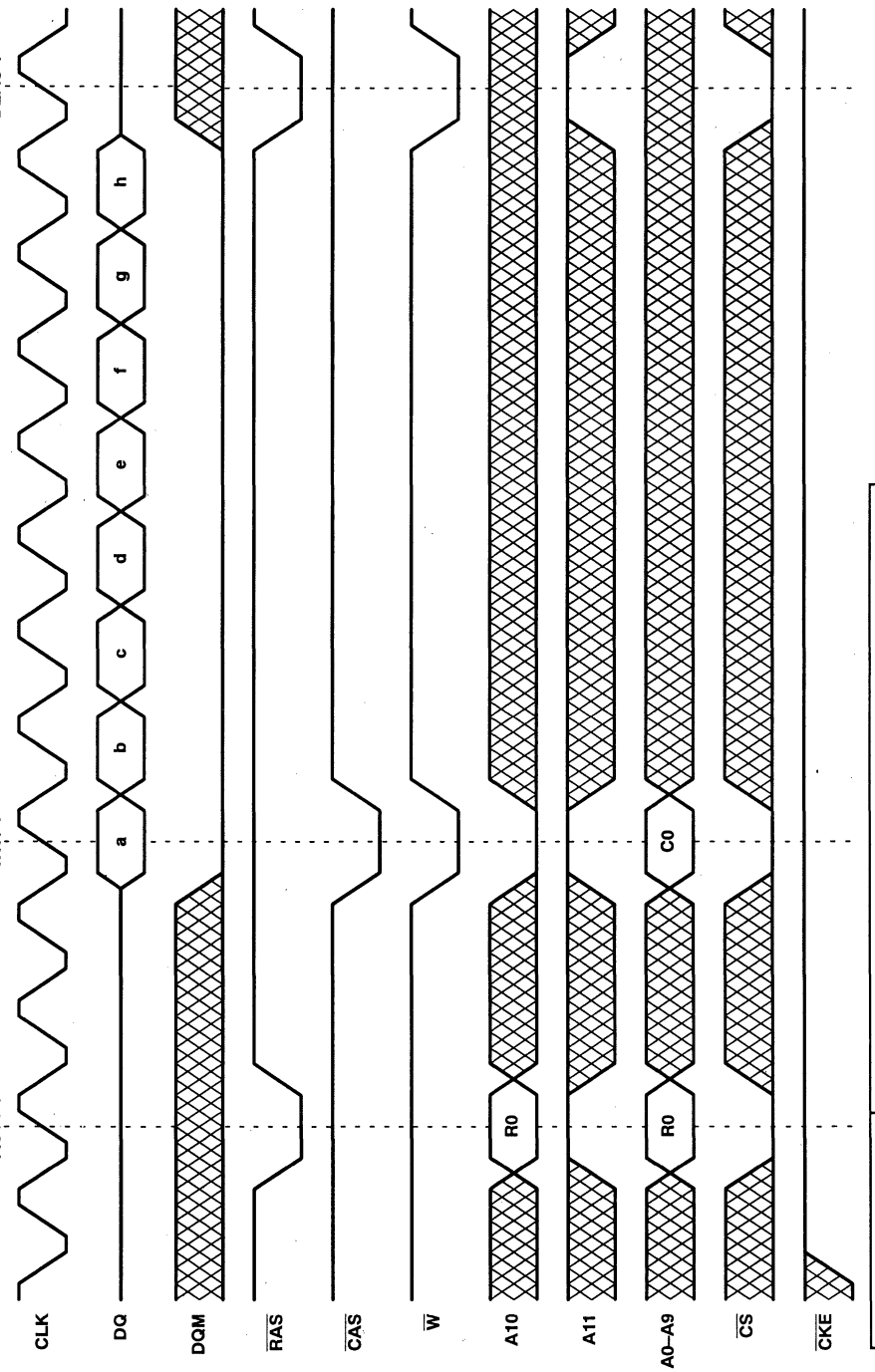
† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)

NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 19. Read Burst (Read Latency = 3, Burst Length =4)

PRODUCT PREVIEW

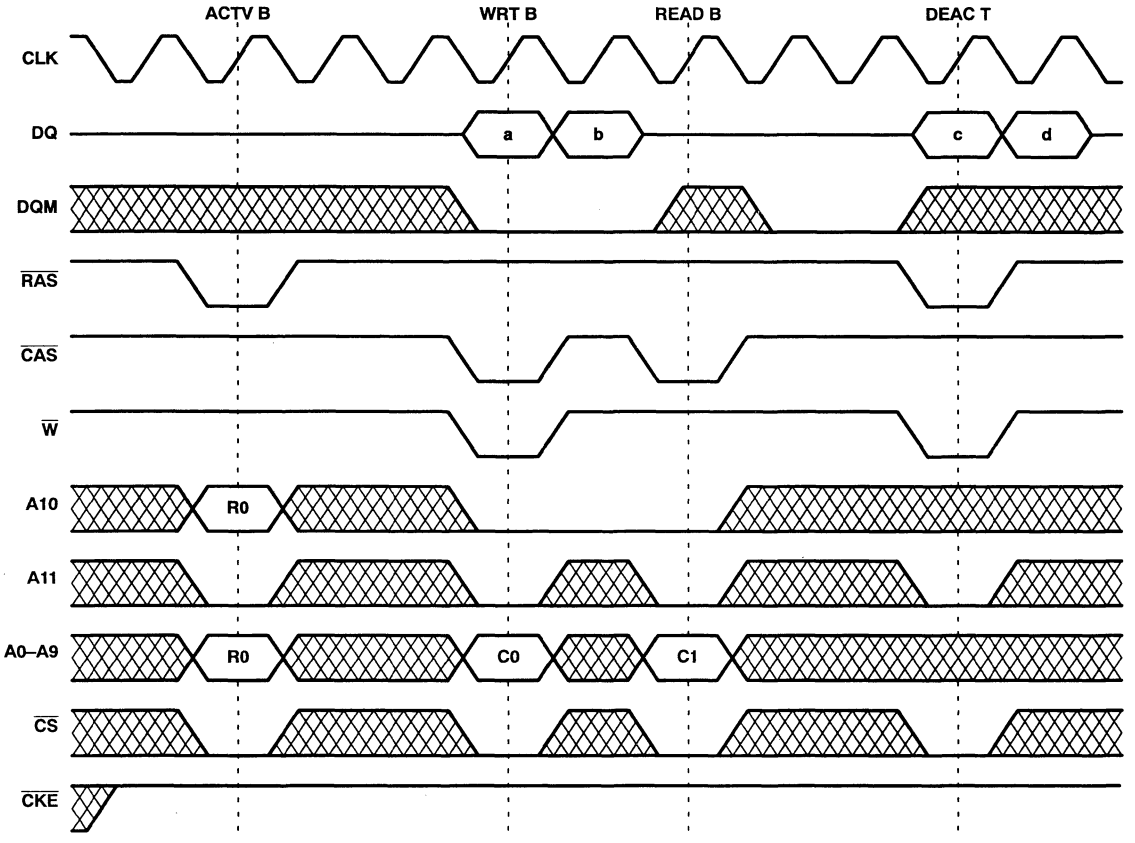
PRODUCT PREVIEW



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE							
			a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)

Figure 20. Write Burst (Burst Length = 8)



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
D	B	R0	C0†	C0 + 1		
Q	B	R0			C1‡	C1 + 1

† Column address sequence depends on programmed burst type and C0. (Refer to Table 4.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 4.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 21. Write-Read Burst (Read Latency = 3, Burst Length = 2)

PRODUCT PREVIEW

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)
‡ Column address sequence depends on programmed burst type and C1.(Refer to Table 6.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 22. Read-Write Burst With Automatic Deactivate (Read Latency = 3, Burst Length = 8)

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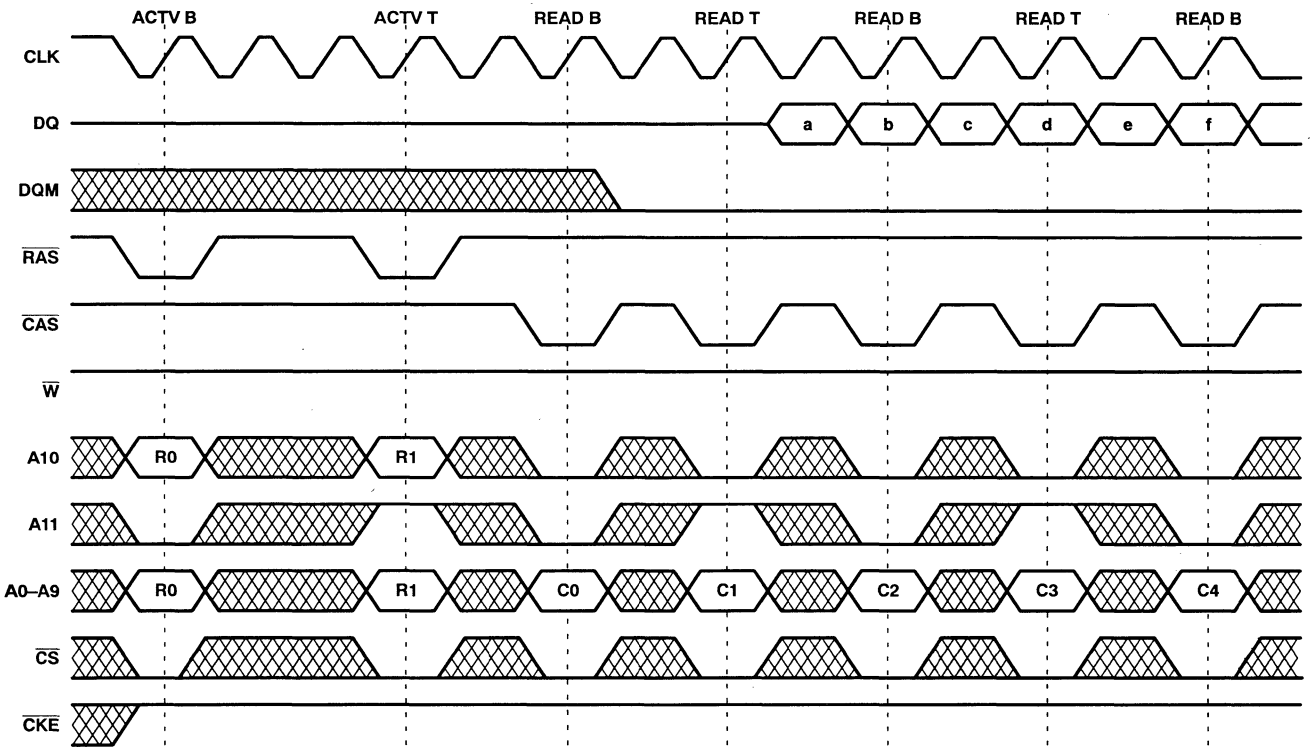
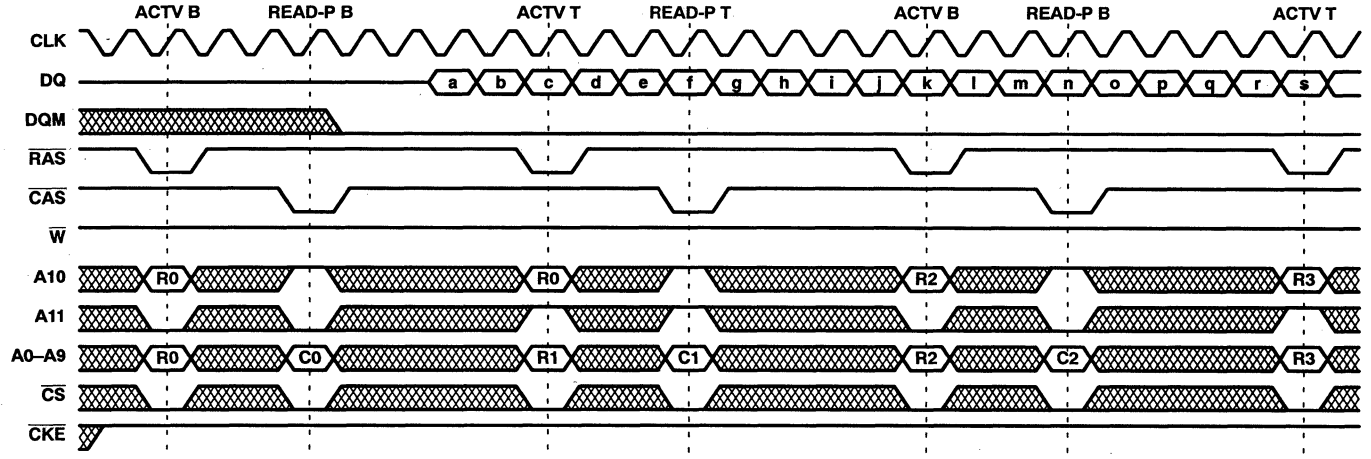


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	.	.
Q	B	R0	C0†	C0 + 1						
Q	T	R1			C1‡	C1 + 1				
Q	B	R0					C2§	C2 + 1		
.	.	.							.	.

† Column address sequence depends on programmed burst type and C0. (Refer to Table 4.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 4.)
§ Column address sequence depends on programmed burst type and C2. (Refer to Table 4.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 23. Two-Bank Column Interleaving (Read Latency = 3, Burst Length = 2)

PRODUCT PREVIEW



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	.	.
Q	B	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7													
Q	T	R1									C1‡	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7					
Q	B	R2																	C2§	C2+1	C2+2	.	.

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)
‡ Column address sequence depends on porgrammed burst type and C1.(Refer to Table 6.)
§ Column address sequence depends on porgrammed burst type and C2.(Refer to Table 6.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 24. Two-Bank Row Interleaving With Automatic Deactivate (Read Latency = 3, Burst Length = 8)

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BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	B	R0	C0†	C0+1	C0+2	C0+3				
D	T	R1					C1‡	C1+1	C1+2	C1+3

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 25. Read Burst Bank B, Write Burst Bank T (Read Latency = 3, Burst Length = 4)

PRODUCT PREVIEW

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	T	R0	C0†	C0+1	C0+2	C0+3				
Q	B	R1					C1‡	C1+1	C1+2	C1+3

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-10 at 100 MHz, the SDRAM-12 at 80 MHz, and the SDRAM-15 at 66 MHz.

Figure 26. Write Burst Bank T, Read Burst Bank B With Automatic Deactivate (Read Latency = 3, Burst Length = 4)

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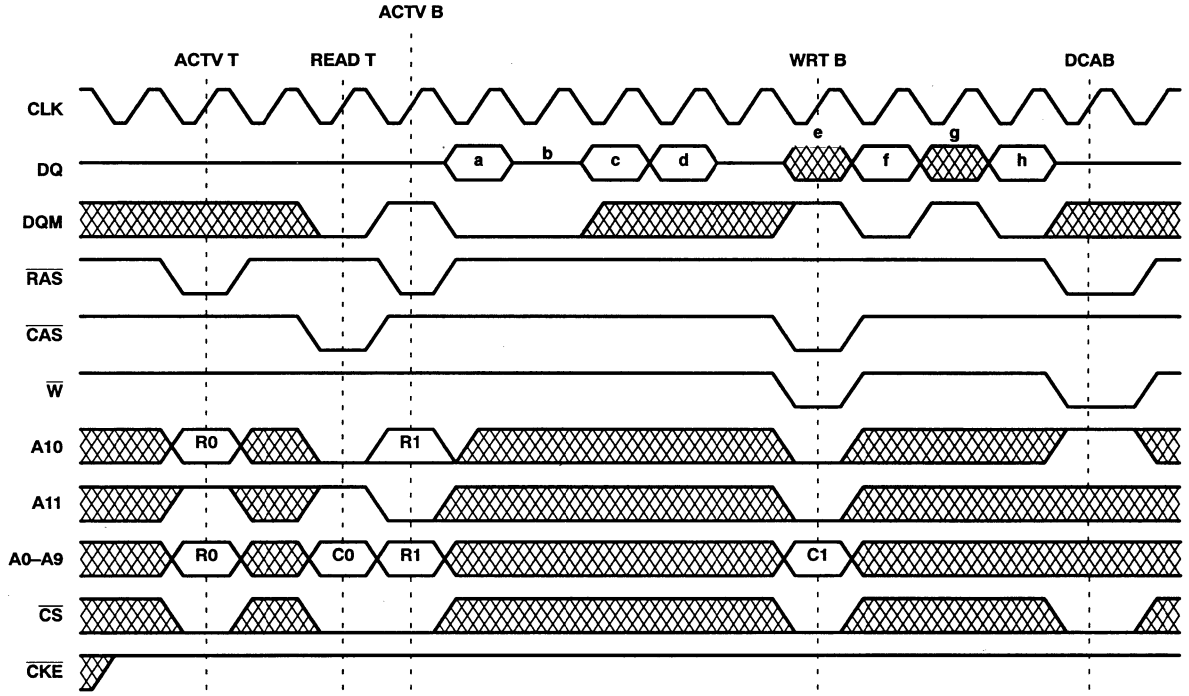

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-15 at 50 MHz.

Figure 27. Use Of DQM For Output and Data-In Cycle Masking (Read Burst Bank T, Write Burst Bank B, Deactivate All Banks) (Read Latency = 2, Burst Length = 4)

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE							
			a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column address sequence depends on programmed burst type and C0. (Refer to Table 6.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-12 at 50 MHz.

**Figure 28. Refresh Cycles (Refreshes Followed By Read Burst Followed By Refresh)
(Read Latency = 2, Burst Length = 8)**

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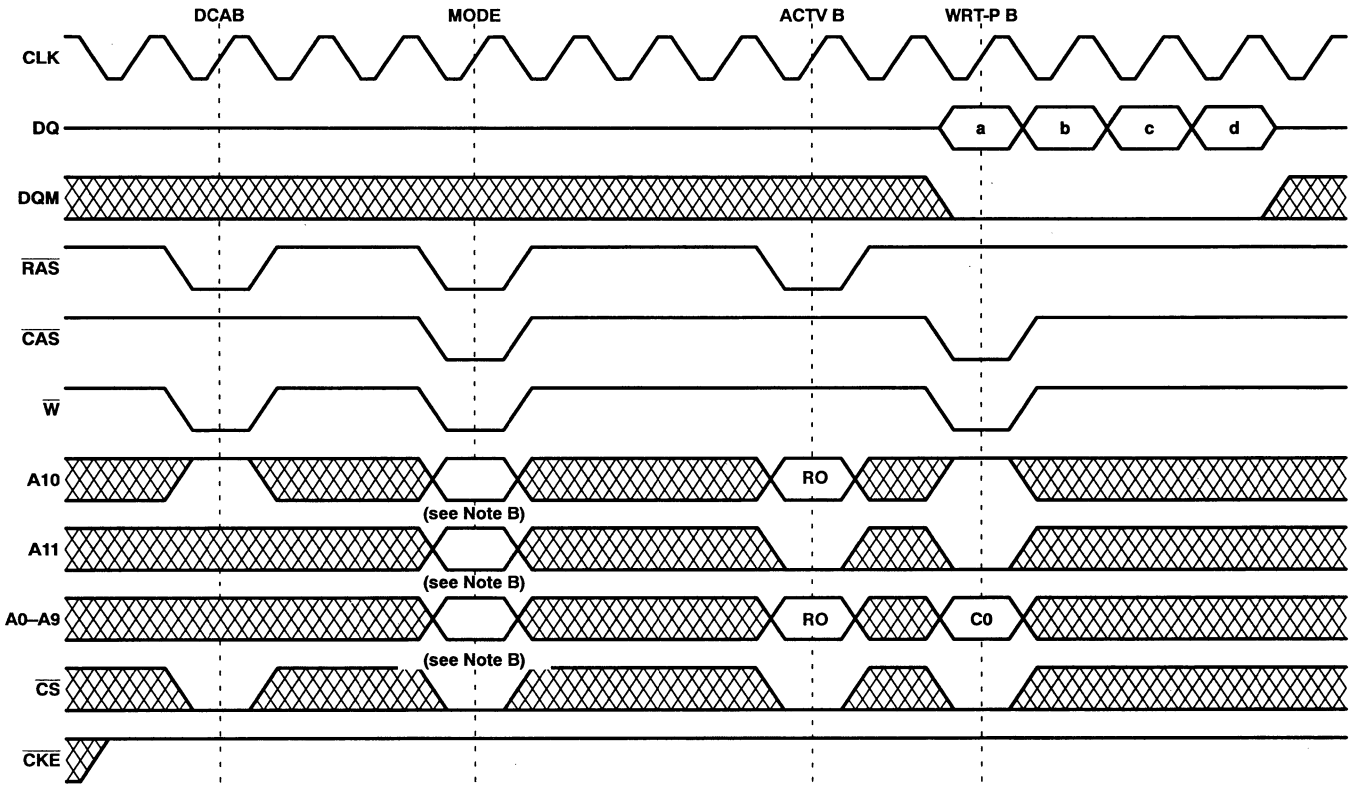

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d
D	B	R0	C0†	C0+1	C0+2	C0+3

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)

NOTES: A. This example illustrates minimum t_{RCD} for the SDRAM-15 at 66 MHz.
B. Refer to Figure 1, Mode Register Programming, on page 9.

Figure 29. Mode Register Programming (Deactivate All, Mode Program, Read Burst With Automatic Deactivate) (Read Latency = 2, Burst Length = 4)

PRODUCT PREVIEW

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3				
D	B	R1					C1‡	C1+1	C1+2	C1+3

† Column address sequence depends on programmed burst type and C0. (Refer to Table 5.)
‡ Column address sequence depends on programmed burst type and C1. (Refer to Table 5.)
NOTE: This example illustrates minimum t_{RCD} and nCL for the SDRAM-15 at 50 MHz.

Figure 30. Use Of $\overline{CKE}$ For Clock Gating (Hold) And Standby Mode (Read Burst Bank T With Hold, Write Burst Bank B, Standby Mode) (Read Latency = 2, Burst Length = 4)

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TM124EU9B	9 437 184-bit	(1024K × 9) Single-Sided	5-5
TM124EU9C	9 437 184-bit	(1024K × 9) Single-Sided	5-5
TM497EAD9B	33 554 432-bit	(4096K × 9) Single-Sided	5-13
TM497MBK36A	150 994 944-bit	(4096K × 36) Double-Sided (gold-tabbed)	5-21
TM497MBK36Q	150 994 944-bit	(4096K × 36) Double-Sided (solder-tabbed)	5-21
TM124BBK32	33 554 432-bit	(1024K × 32) Single-Sided (gold-tabbed)	5-29
TM124BBK32S	33 554 432-bit	(1024K × 32) Single-Sided (solder-tabbed)	5-29
TM248CBK32	67 543 040-bit	(2048K × 32) Double-Sided (gold-tabbed)	5-29
TM248CBK32S	67 543 040-bit	(2048K × 32) Double-Sided (solder-tabbed)	5-29
TM124MBK36	37 748 736-bit	(1024K × 36) Double-Sided (gold-tabbed)	5-39
TM124MBK36Q	37 748 736-bit	(1024K × 36) Double-Sided (solder-tabbed)	5-39
TM124MBK36B	37 748 736-bit	(1024K × 36) Single-Sided (gold-tabbed)	5-47
TM124MBK36R	37 748 736-bit	(1024K × 36) Single-Sided (solder-tabbed)	5-47
TM248NBK36B	75 497 472-bit	(2048K × 36) Double-Sided (gold-tabbed)	5-47
TM248NBK36R	75 497 472-bit	(2048K × 36) Double-Sided (solder-tabbed)	5-47
TM124MBK36C	37 748 736-bit	(1024K × 36) Single-Sided (gold-tabbed)	5-57
TM124MBK36S	37 748 736-bit	(1024K × 36) Single-Sided (solder-tabbed)	5-57
TM248NBK36C	75 497 472-bit	(2048K × 36) Double-Sided (gold-tabbed)	5-57
TM248NBK36S	75 497 472-bit	(2048K × 36) Double-Sided (solder-tabbed)	5-57
TM4100EAD9	37 748 736-bit	(4096K × 9) Single-Sided	5-67
TM4100GAD8	33 554 432-bit	(4096K × 8) Single-Sided	5-75
TM497GAD8A	33 554 432-bit	(4096K × 8) Single-Sided	5-83
TM16100GBD8	134 217 728-bit	(16 384K × 8) Double-Sided	5-91
TM16100EBD9	150 994 944-bit	(16 384K × 9) Double-Sided	5-99
TM497BBK32	134 217 728-bit	(4096K × 32) Double-Sided (gold-tabbed)	5-105
TM497BBK32S	134 217 728-bit	(4096K × 32) Double-Sided (solder-tabbed)	5-105
TM893CBK32	268 435 456-bit	(8192K × 32) Double-Sided (gold-tabbed)	5-105
TM893CBK32S	268 435 456-bit	(8192K × 32) Double-Sided (solder-tabbed)	5-105
TM497TBM40	167 772 160-bit	(4096K × 40) Double-Sided (gold-tabbed)	5-115

TM497TBM40S	167 772 160-bit	(4096K × 40) Double-Sided (solder-tabbed)	5-115
TM893VBM40	335 544 320-bit	(8192K × 40) Double-Sided (gold-tabbed)	5-115
TM893VBM40S	335 544 320-bit	(8192K × 40) Double-Sided (solder-tabbed)	5-115
TM496TBM40	167 772 160-bit	(4096K × 40) Double-Sided (gold-tabbed)	5-125
TM496TBM40S	167 772 160-bit	(4096K × 40) Double-Sided (solder-tabbed)	5-125
TM892VBM40	335 544 320-bit	(8192K × 40) Double-Sided (gold-tabbed)	5-125
TM892VBM40S	335 544 320-bit	(8192K × 40) Double-Sided (solder-tabbed)	5-125
TM124TBK40	41 943 040-bit	(1024K × 40) Single-Sided (gold-tabbed)	5-137
TM124TBK40S	41 943 040-bit	(1024K × 40) Single-Sided (solder-tabbed)	5-137
TM248VBK40	83 886 080-bit	(2048K × 40) Double-Sided (gold-tabbed)	5-137
TM248VBK40S	83 886 080-bit	(2048K × 40) Double-Sided (solder-tabbed)	5-137

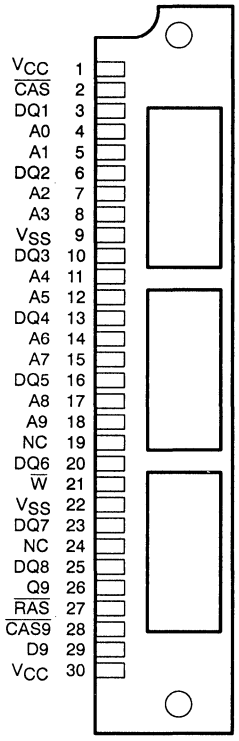
SMMS191D–JANUARY 1991–REVISED JANUARY 1993

- **Organization . . . 1 048 576 × 9**
- **Single 5-V Power Supply**
- **30-Pin Single In-Line Memory Module**
- **TM124EU9B . . . Utilizes Two 4-Megabit and One 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **TM124EU9C . . . Utilizes Three 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)	V_{CC} TOLERANCE
'124EU9B/C-6	60 ns	30 ns	110 ns	± 5%
'124EU9B/C-70	70 ns	35 ns	130 ns	± 10%
'124EU9B/C-80	80 ns	40 ns	150 ns	± 10%

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MEMORY MODULE†
(TOP VIEW)



† The package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A9	Address Inputs
CAS, CAS9	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
D9	Data In
NC	No Connect
Q9	Data Out
RAS	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
W	Write Enable

description

The TM124EU9B and TM124EU9C are dynamic random-access memory modules organized as 1048 576 × 9 (bit nine is generally used for parity) in 30-pin leadless single in-line memory modules (SIMMs).

The TM124EU9B is composed of two TMS44400, 1048 576 × 4-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS4C1024, 1048 576 ×1 bit dynamic RAM in a 20/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors.

The TM124EU9C is composed of two TMS44400, 1 048 576 × 4-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS44100, 4 194 304 ×1 bit dynamic RAM in a 20/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors.

The TM124EU9B and TM124EU9C each feature RAS access times of 60 ns, 70 ns, and 80 ns.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM124EU9B and TM124EU9C are characterized for operation from 0°C to 70°C.

operation

The TM124EU9B operates as two TMS44400s and one TMS4C1024 connected as shown in the functional block diagram.

The TM124EU9C operates as two TMS44400s and one TMS44100 connected as shown in the functional block diagram.

The common I/O features of the TM124EU9B and TM124EU9C dictate the use of early write cycles to prevent contention on the DQ lines.

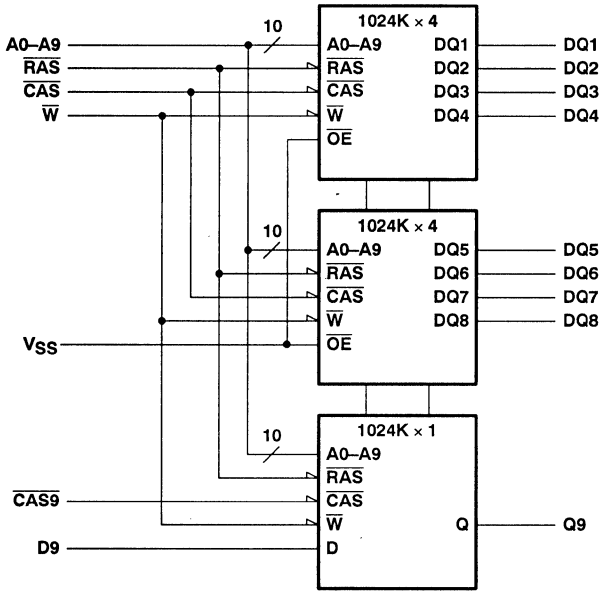
refresh

The refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. For the TM124EU9B, the nine least significant row addresses (A0–A8) must be refreshed every 8 ms as required by the TMS4C1024.

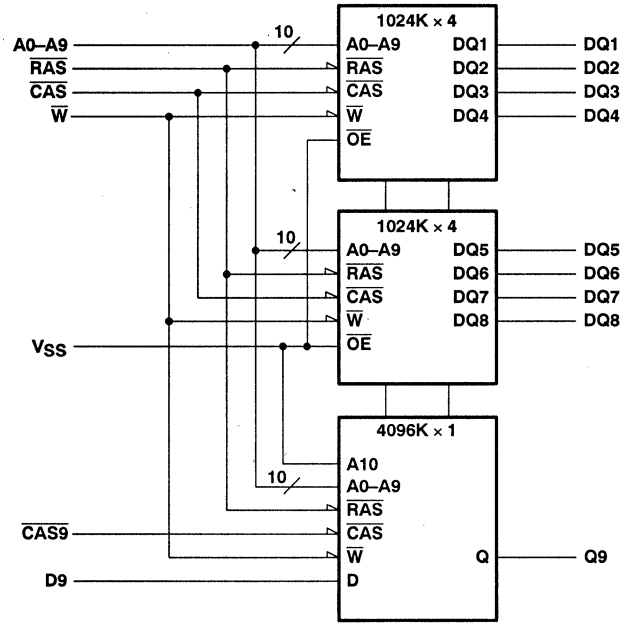
single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper.

functional block diagram (TM124EU9B)



functional block diagram (TM124EU9C)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 3 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM124EU9B-6 and TM124EU9C-6)	4.75	5	5.75	V
V_{CC}	Supply voltage (TM124EU9B-70/-80 and TM124EU9C-70/-80)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124EU9B-6 '124EU9C-6		'124EU9B-70 '124EU9C-70		'124EU9B-80 '124EU9C-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I=0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		315		270		240	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		6		6		6	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		315		270		240	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		270		240		210	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124EU9B '124EU9C		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		21	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ input		21	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ input		14	pF
$C_{i(CAS9)}$	Input capacitance, $\overline{CAS9}$ input		7	pF
$C_{i(DQ)}$	Input capacitance, data inputs/outputs		7	pF
$C_{i(D9)}$	Input capacitance, D9 input		5	pF
$C_{o(Q9)}$	Output capacitance on Q9 output		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124EU9B-6 '124EU9C-6		'124EU9B-70 '124EU9C-70		'124EU9B-80 '124EU9C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124EU9B-6 '124EU9C-6		'124EU9B-70 '124EU9C-70		'124EU9B-80 '124EU9C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time (see Note 11)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		12		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time (see Note 11)	10		10		10		ns

Continued next page.

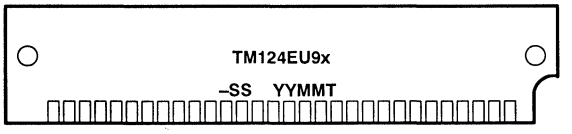
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124EU9B-6 '124EU9C-6		'124EU9B-70 '124EU9C-70		'124EU9B-80 '124EU9C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	17	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	22	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Distributed refresh time interval		16		16		16	ms
t_T	Transition time	3	50	3	50	3	50	ns

NOTES: 11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. The maximum value is specified only to assure access time.

device symbolization (on back side of module)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

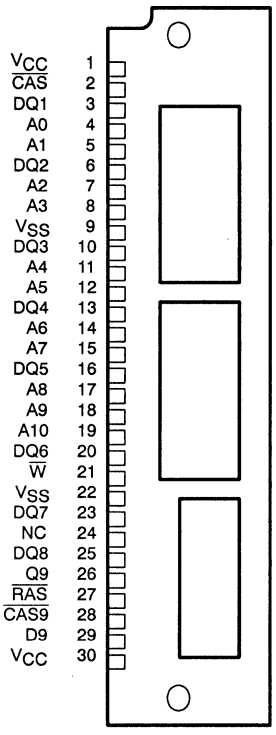
SMMS479–DECEMBER 1992

- **Organization . . . 4 194 304 × 9**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes One 4-Megabit and Two 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 32 ms (2048 Cycles)**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TM497EAD9B-60	60 ns	15 ns	110 ns
TM497EAD9B-70	70 ns	18 ns	130 ns
TM497EAD9B-80	80 ns	20 ns	150 ns
TM497EAD9B-10	100 ns	25 ns	180 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

AD SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1–DQ8	Data In / Data Out
D9	Data In
NC	No Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM497EAD9B is a 36M dynamic random-access memory module organized as 4 194 304 × 9 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin leadless single in-line memory module (SIMM).

This module is composed of two TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs in 24/28-lead plastic small-outline J-lead packages (SOJ), and one TMS44100DJ, 4 194 304 × 1-bit dynamic RAM in a 20/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors.

The TM497EAD9B is available in the AD single-sided, leadless module for use with sockets.

The TM497EAD9B is characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

operation

The TM497EAD9B operates as two TMS417400DZs and one TMS44100DJ connected as shown in the functional block diagram. Refer to the TMS417400 and TMS44100 data sheets for details of their operation. The common I/O feature of the TM497EAD9B dictates the use of early write cycles to prevent contention on D and Q.

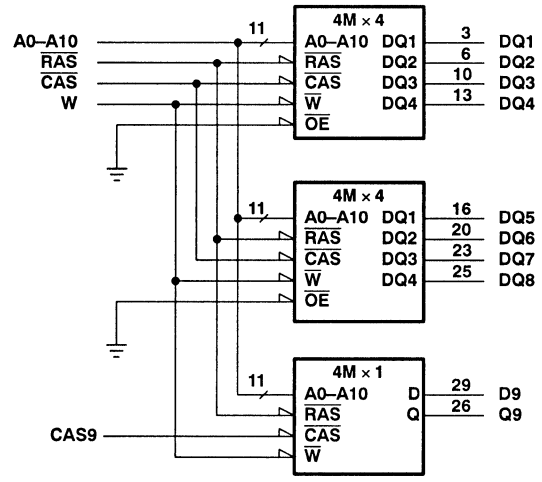
specifications

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. For the TM497EAD9B, the ten least significant row addresses (A0–A9) must be refreshed every 16 ms as required by the TMS44100.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 3 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497EAD9B-60		'497EAD9B-70		'497EAD9B-80		'497EAD9B-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		335		305		275		245	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		6		6		6		6	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		3		3		3		3	
I_{CC3}	Average refresh current (RAS only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		335		305		275		245	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		210		180		150		130	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(D)}$	Input capacitance, data input (pin D9)		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		21	pF
$C_{i(W)}$	Input capacitance, write-enable input		21	pF
$C_{o(DQ)}$	Output capacitance (pins DQ1–DQ8)		7	pF
C_o	Output capacitance (pin Q9)		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497EAD9B-60		'497EAD9B-70		'497EAD9B-80		'497EAD9B-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497EAD9B-60		'497EAD9B-70		'497EAD9B-80		'497EAD9B-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle time (see Note 7)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		20		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 9)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		75		ns
t_{DH}	Data hold time	10		15		15		20		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		75		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 11)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 11)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		20		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		75		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

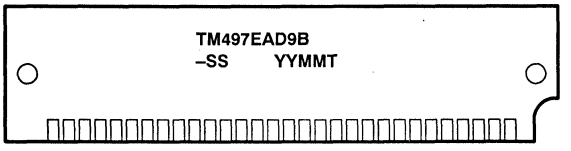
ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'497EAD9B-60		'497EAD9B-70		'497EAD9B-80		'497EAD9B-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	15	40	20	50	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		32		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 12: The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of the part number may vary.

ADVANCE INFORMATION

- **Organization . . . 4 194 304 × 36**
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 32 ms (2048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Separate $\overline{RAS}$ Control for Eighteen Data-In and Data-Out Lines, in Two Blocks**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
TM497MBK36A-60	60 ns	15 ns	30 ns	110 ns
TM497MBK36A-70	70 ns	18 ns	35 ns	130 ns
TM497MBK36A-80	80 ns	20 ns	40 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Presence Detect**
- **Gold-Tabbed Version Available:† TM497MBK36A**
- **Tin-Lead (Solder) Tabbed Version Available: TM497MBK36Q**

ADVANCE INFORMATION

description

The TM497MBK36A is a 144M dynamic random-access memory organized as four times 4 194 304 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs, each in 24/28-lead plastic small-outline J-lead packages (SOJs), and four TMS44100DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. Each TMS417400DZ and TMS44100DJ is described in the TMS417400 and TMS44100 data sheets (respectively).

The TM497MBK36A is available in a double-sided BK leadless module for use with sockets.

The TM497MBK36A features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497MBK36A operates as eight TMS417400DZs and four TMS44100DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS417400 and TMS44100 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

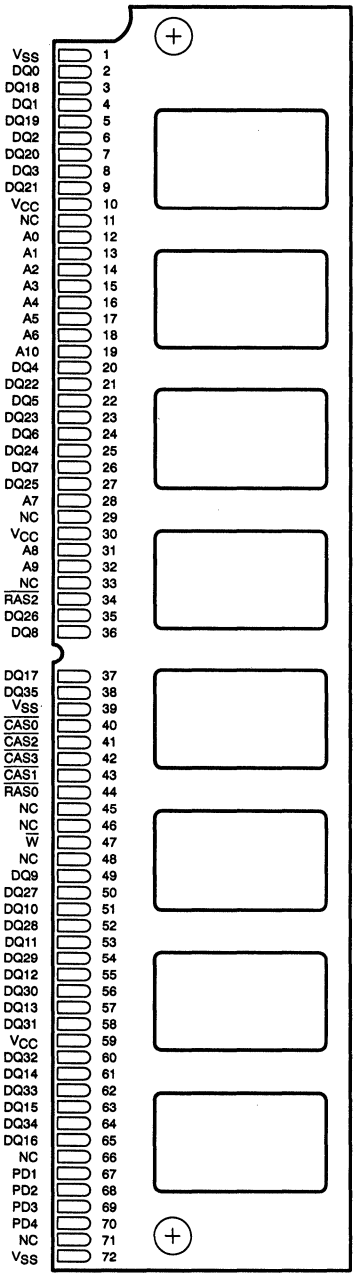
specifications

The refresh period is extended to 32 milliseconds and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A10 must be used as most significant refresh address line (lowest frequency) to assure correct refresh for both TMS417400 and TMS44100. A0–A9 address lines must be refreshed every 16 ms as required by the TMS44100 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

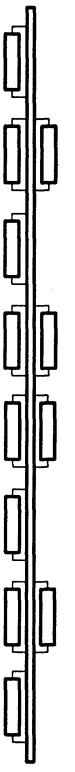
† Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

ADVANCE INFORMATION

BK SINGLE-IN-LINE PACKAGE† (TOP VIEW)



TM497MBK36AT (SIDE VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ7, DQ9–DQ16, DQ18–DQ25, DQ27–DQ34	Data In/Data Out
DQ8, DQ17, DQ26, DQ35	Parity
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497MBK36A	80 ns	V_{SS}	NC	NC	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC
	60 ns	V_{SS}	NC	NC	NC

† The packages shown here are for pinout reference only and are not drawn to scale.

Table 1. Connection Table

DATA BLOCK	$\overline{RASx}$	$\overline{CASx}$
DQ0–DQ7 DQ8	$\overline{RAS0}$	$\overline{CAS0}$
DQ9–DQ16 DQ17	$\overline{RAS0}$	$\overline{CAS1}$
DQ18–DQ25 DQ26	$\overline{RAS2}$	$\overline{CAS2}$
DQ27–DQ34 DQ35	$\overline{RAS2}$	$\overline{CAS3}$

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497MBK36A: Nickel plate and gold plate over copper
Contact area for TM497MBK36Q: Nickel plate and tin-lead over copper

ADVANCE INFORMATION

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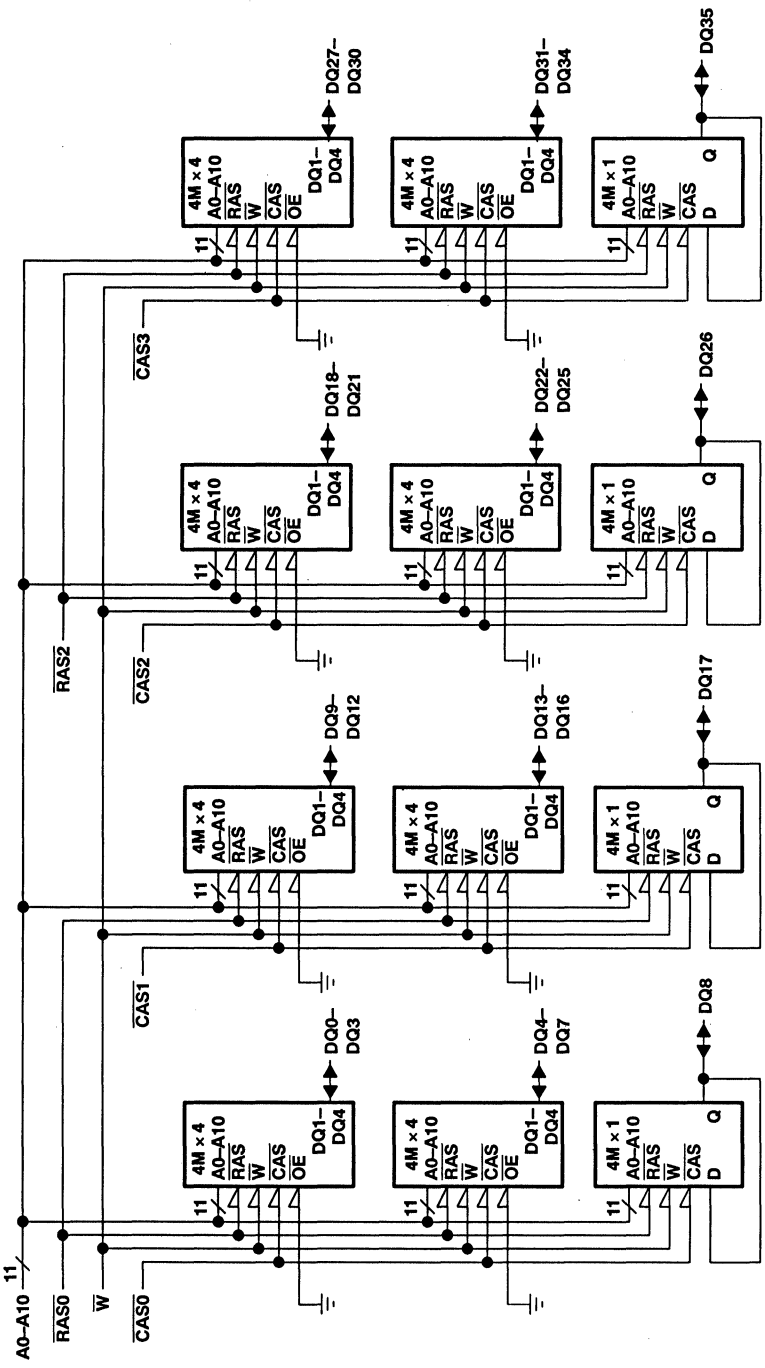
functional block diagram



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 12 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 120		± 120		± 120	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		1480		1240		1120	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		24		24		24	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		12		12		12	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1480		1240		1120	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		920		800		680	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			60	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			21	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			42	pF
$C_{i(W)}$	Input capacitance, write-enable input			84	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7	pF
$C_{o(MP)}$	Output capacitance on MP pins			12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable; start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.

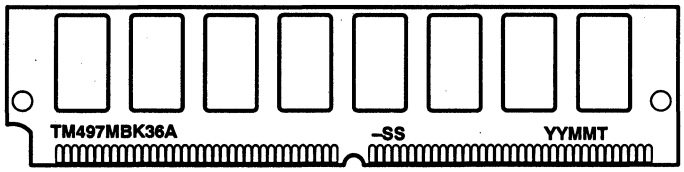
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'497MBK36A-60		'497MBK36A-70		'497MBK36A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		15		15		ns
t_{DH}	Data hold time	15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to guarantee access time.

ADVANCE INFORMATION

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
– SS = Speed Code

NOTE: Location of symbolization may vary.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
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- **Organization**
  TM124BBK32 . . . 1 048 576 × 32
  TM248CBK32 . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10 % Tolerance)**
- **72-pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124BBK32-Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248CBK32-Utilizes Sixteen 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Distributed Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, In Four Blocks**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
TM124BBK32-60	60 ns	15 ns	110 ns
TM124BBK32-70	70 ns	18 ns	130 ns
TM124BBK32-80	80 ns	20 ns	150 ns
TM248CBK32-60	60 ns	15 ns	110 ns
TM248CBK32-70	70 ns	18 ns	130 ns
TM248CBK32-80	80 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  - **TM124BBK32**
  - **TM248CBK32**
- **Tin-Lead (Solder) Tabbed Versions Available:**
  - **TM124BBK32S**
  - **TM248CBK32S**

description

TM124BBK32

The TM124BBK32 is a dynamic random-access memory organized as four times 1 048 576 × 8 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), mounted on a substrate together with decoupling capacitors. Each TMS44400 is described in the TMS44400 data sheet.

The TM124BBK32 is available in the single-sided BK leadless module for use with sockets.

The TM124BBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns and 80 ns. This device is rated for operation from 0°C to 70°C

TM248CBK32

The TM248CBK32 is a dynamic random-access memory organized as four times 2 097 152 × 8 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of sixteen TMS44400, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), mounted on a substrate together with decoupling capacitors. Each TMS44400 is described in the TMS44400 data sheet.

The TM248CBK32 is available in the double-sided BK leadless module for use with sockets.

The TM248CBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns and 80 ns. This device is rated for operation from 0°C to 70°C

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

operation

TM124BBK32

The TM124BBK32 operates as eight TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM124BBK32 dictates the use of early write cycles to prevent contention on D and Q.

TM248CBK32

The TM248CBK32 operates as sixteen TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation. The common I/O feature of the TM248CBK32 dictates the use of early write cycles to prevent contention on D and Q.

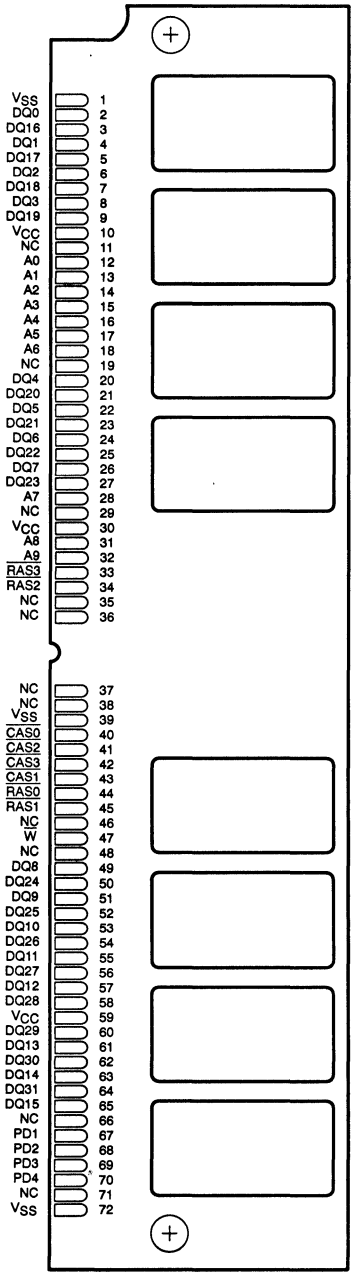
refresh

Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. A0-A9 address lines must be refreshed every 16 ms as required by the TMS44400 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

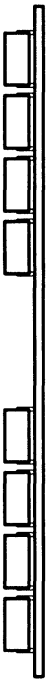
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124BBK32 AND TM248CBK32: Nickel plate and gold plate over copper.
Contact area for TM124BBK32S AND TM248CBK32S: Nickel plate and tin-lead over copper.

BK SINGLE IN-LINE MEMORY MODULE
(TOP VIEW)



TM124BBK32†
(SIDE VIEW)



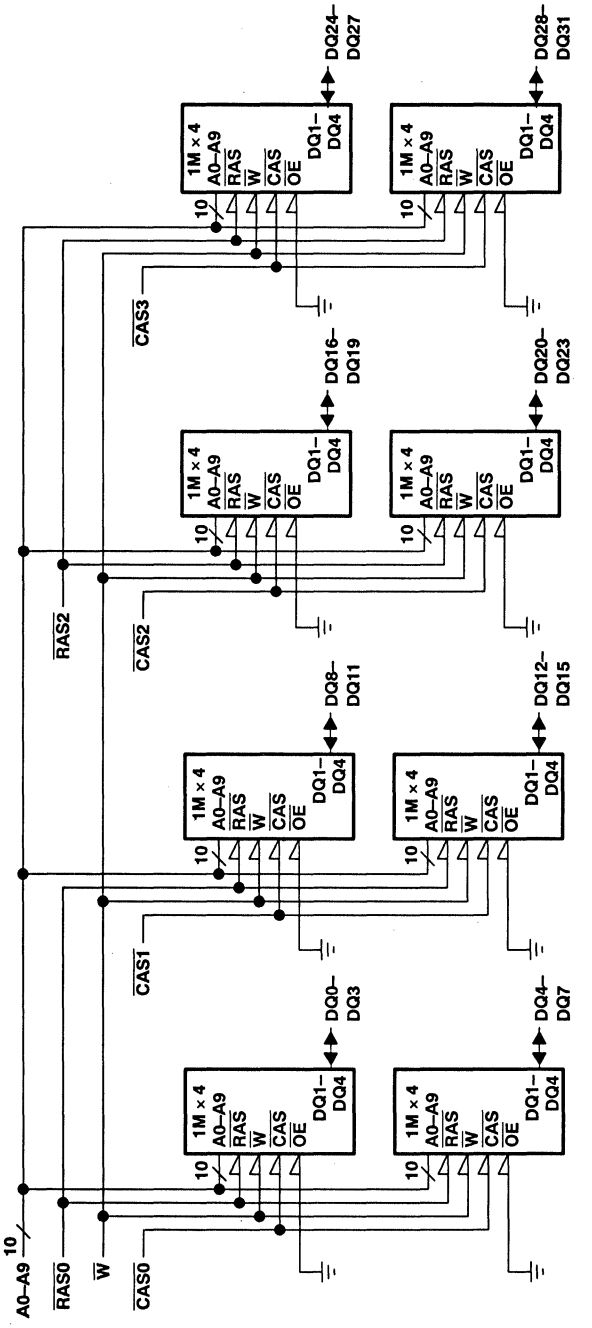
TM248CBK32†
(SIDE VIEW)

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124BBK32	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248CBK32	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are for pinout reference only and are not drawn to scale.

functional block diagram (for TM124BBK32 and TM248CBK32, Side 1)



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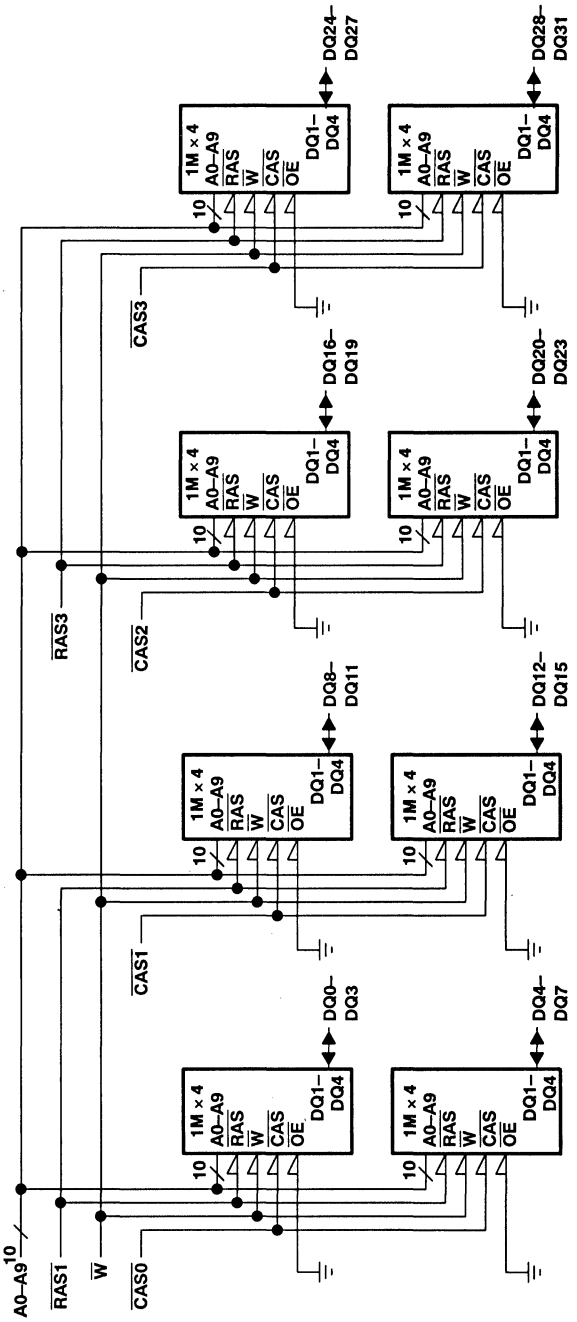
functional block diagram (for TM248CBK32, Side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124BBK32-60		'124BBK32-70		'124BBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		840		720		640	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248CBK32-60		'248CBK32-70		'248CBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±20		±20		±20	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±20		±20		±20	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		856		736		656	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		32		32		32	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		16		16		16	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1680		1440		1280	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		736		656		576	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature f = 1 MHz (see Note 5)

		'124BBK32		'248CBK32		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		40		80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		28		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		14		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		56		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended range of supply voltage and operating free-air temperature

		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time (see Note 11)	10		10		10		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		ns

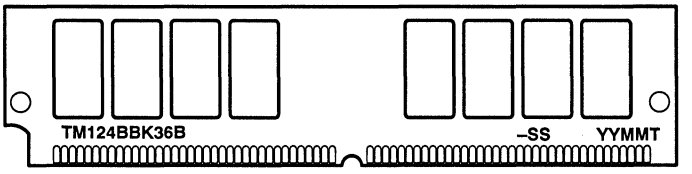
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PL}min, t_{ASC} should be greater than or equal to 5 ns.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended range of supply voltage and operating free-air temperature (concluded)

		'124BBK32-60 '248CBK32-60		'124BBK32-70 '248CBK32-70		'124BBK32-80 '248CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time (see Note 11)	10		10		10		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low	50		55		60		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	15		15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 11)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 11)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{WTS}	$\overline{W}$-low setup time (test mode only)	10		10		10		ns
t_{WTH}	$\overline{W}$-low hold time (test mode only)	10		10		10		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 11. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
12. Maximum value specified only to assure access time.

device symbolization (TM124BBK32 illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

- **Organization . . . 1 048 576 × 36**
- **Single 5-V Power Supply**
- **72-pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 1-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Separate $\overline{RAS}$ Control for Eighteen Data-In and Data-Out Lines, in Two Blocks**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{CAC}	ACCESS TIME t_{AA}	READ OR WRITE CYCLE	VCC TOLERANCE
'124MBK36-6	60 ns	15 ns	30 ns	110 ns	± 5%
'124MBK36-70	70 ns	18 ns	35 ns	130 ns	± 10%
'124MBK36-80	80 ns	20 ns	40 ns	150 ns	± 10%

- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Presence Detect**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **Long Refresh Period 16 ms (1024 Cycles)**
- **Low Power Dissipation**
- **3-State Output**
- **Gold-Tabbed Version Available:† TM124MBK36**
- **Tin-Lead (Solder) Tabbed Version Available: TM124MBK36Q**

description

The TM124MBK36 is a dynamic random-access memory organized as four times 1 048 576 × 9 (bit 9 is generally used for parity) in a 72 pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and four TMS4C1024DJ, 1 048 576 × 1-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS4C1024DJ is described in the TMS44400 and TMS4C1024 data sheets, respectively.

The TM124MBK36 is available in a double-sided BK leadless module for use with sockets.

The TM124MBK36 features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

operation

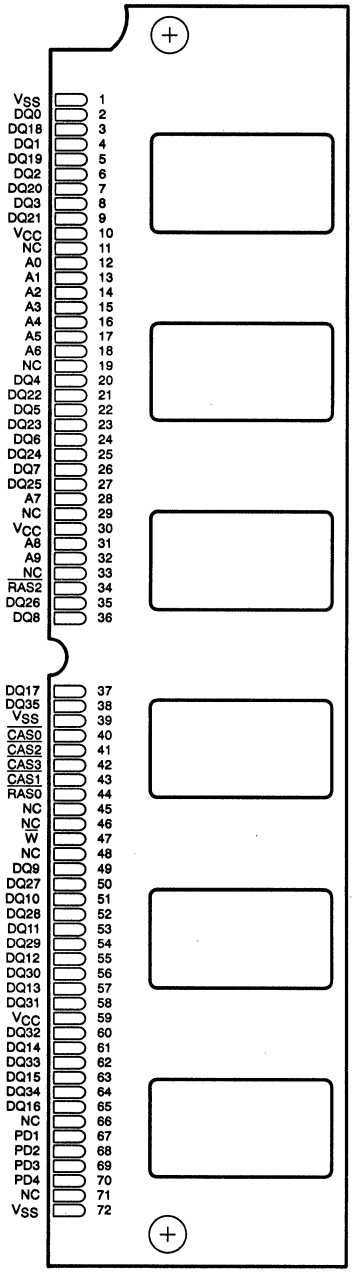
The TM124MBK36 operates as eight TMS44400DJs and four TMS4C1024DJs connected as shown in the functional block diagram and Table 1. Refer to the TMS44400 and TMS4C1024 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

refresh

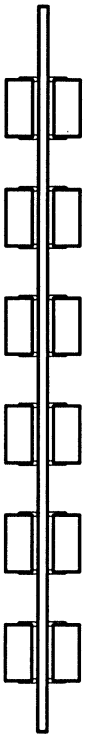
Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A9 must be used as most significant refresh address line (lowest frequency) to assure correct refresh for both TMS44400 and TMS4C1024. A0–A8 address lines must be refreshed every 8 ms as required by the TMS4C1024 DRAM. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE IN-LINE MODULE† (TOP VIEW)



TM124MBK36† (SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL PIN		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC

† The package shown here is for pinout reference only and is not drawn to scale.

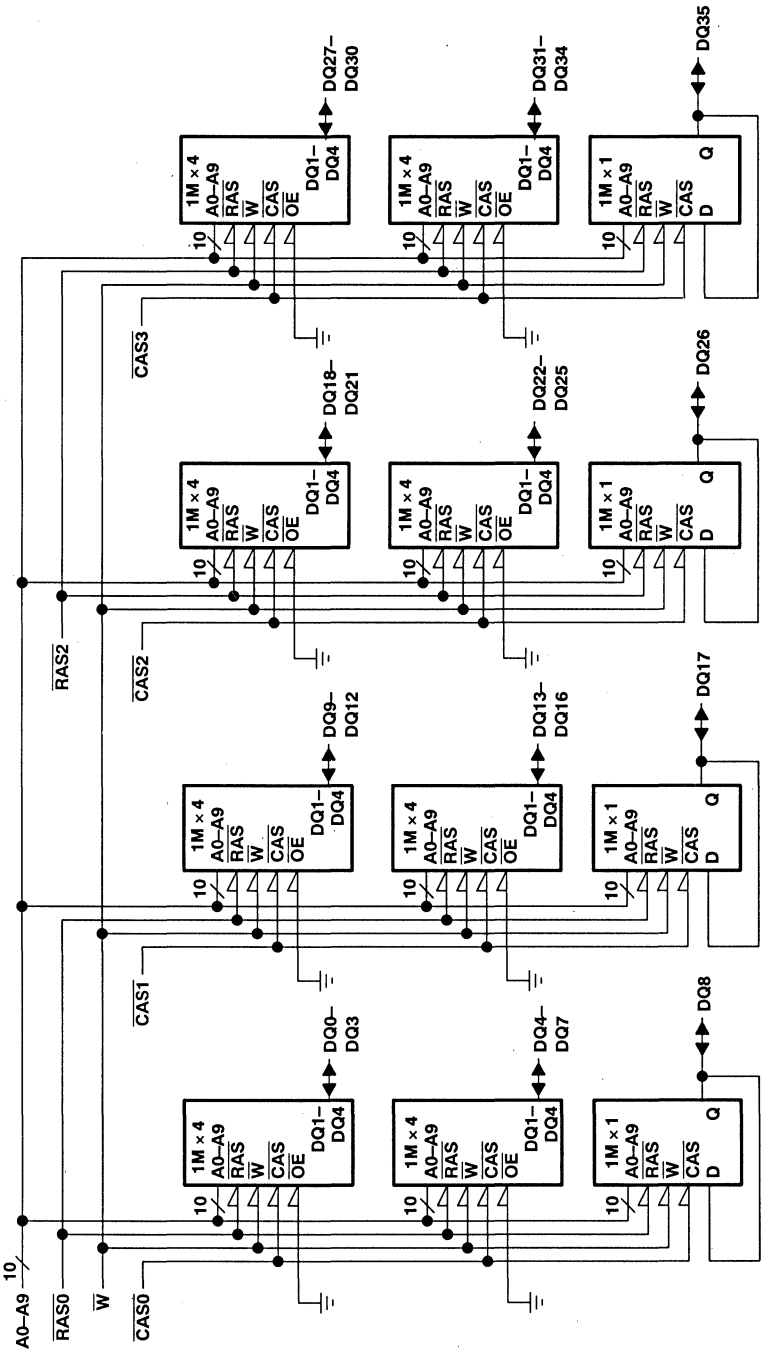
Table 1. Connection Table

DATA BLOCK	$\overline{RAS}x$	$\overline{CAS}x$
DQ–DQ7 DQ8	$\overline{RAS}0$	$\overline{CAS}0$
DQ9–DQ16 DQ17	$\overline{RAS}0$	$\overline{CAS}1$
DQ18–DQ25 DQ26	$\overline{RAS}2$	$\overline{CAS}2$
DQ27–DQ34 DQ35	$\overline{RAS}2$	$\overline{CAS}3$

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36: Nickel plate and gold plate over copper.
Contact area for TM124MBK36Q: Nickel plate and tin-lead over copper.

functional block diagram (TM124MBK36)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 12 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (TM124MBK36-6)	4.75	5	5.25	V
V_{CC}	Supply voltage (TM124MBK36-70/-80)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		1220		1040		940	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		24		24		24	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		12		12		12	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1200		1040		920	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		1000		880		760	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER			MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs				60	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs				19	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs				38	pF
$C_{i(W)}$	Input capacitance, write-enable input				76	pF
$C_{o(DQ)}$	Output capacitance	DQ8, DQ17, DQ26, DQ35			7	pF
		All other DQ pins			12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time (see Note 9)	10		10		10		ns

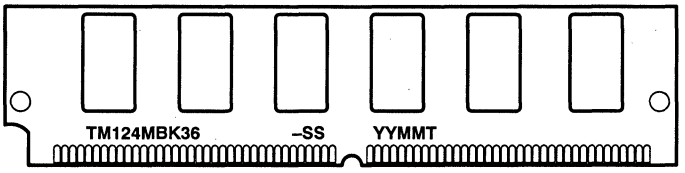
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124MBK36-6		'124MBK36-70		'124MBK36-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after RAS low (see Note 10)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		12		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after RAS low	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	17	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	3	50	3	50	3	50	ns

NOTES: 9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

SMMS137D–JANUARY 1991–REVISED JANUARY 1993

- **Organization**
  TM124MBK36B . . . 1 048 576 × 36
  TM248NBK36B . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-pin Leadless Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124MBK36B–Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and One 4-Megabit Quad-$\overline{CAS}$ Dynamic RAM in a Plastic Small-Outline J-Lead (SOJ) Package**
- **TM248NBK36B–Utilizes Sixteen 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 4-Megabit Quad-$\overline{CAS}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36B-60	60 ns	30 ns	15 ns	110 ns
'124MBK36B-70	70 ns	35 ns	18 ns	130 ns
'124MBK36B-80	80 ns	40 ns	20 ns	150 ns
'248NBK36B-60	60 ns	30 ns	15 ns	110 ns
'248NBK36B-70	70 ns	35 ns	18 ns	130 ns
'248NBK36B-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  – TM124MBK36B
  – TM248NBK36B
- **Tin-Lead (Solder) Tabbed Versions Available:**
  – TM124MBK36R
  – TM248NBK36R

description

TM124MBK36B

The TM124MBK36B is a dynamic random-access memory organized as four times 1 048 576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ dynamic RAM in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 or TMS44460 data sheet, respectively.

The TM124MBK36B is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

TM248NBK36B

The TM248NBK36B is a dynamic random-access memory organized as four times 2 097 152 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of sixteen TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and two TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ dynamic RAMs, each in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheet, respectively.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

The TM124NBK36B is available in the double-sided BK leadless module for use with sockets.

The TM124NBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

operation

TM124MBK36B

The TM124MBK36B operates as eight TMS44400DJs and one TMS44460DJ connected as shown in the functional block diagram and Table 1. The parity bits are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$. To ensure proper parity bit operation all memory accesses should include a $\overline{RAS2}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

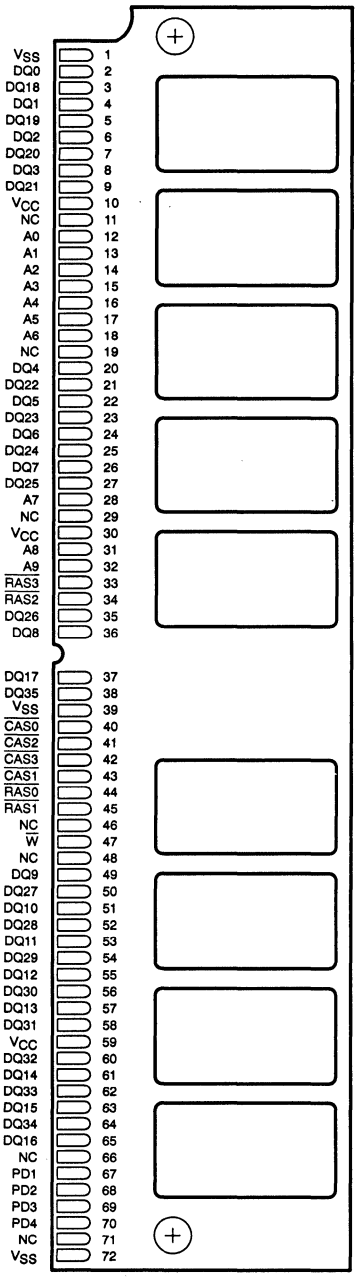
TM248NBK36B

The TM248NBK36B operates as sixteen TMS44400DJs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The parity bits are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$ on side 1 and $\overline{RAS3}$ on side 2. To ensure proper parity bit operation, all memory accesses should include a $\overline{RAS2}$ or $\overline{RAS3}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

SMMS137D–JANUARY 1991–REVISED JANUARY 1993

BK SINGLE IN-LINE MEMORY MODULE†

(TOP VIEW)

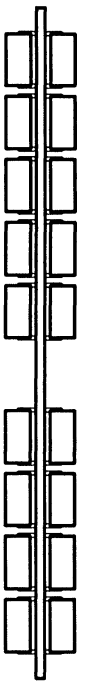


TM124MBK36B†

(SIDE VIEW)

TM248NBK36B†

(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36B	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36B	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are for pinout reference only and are not drawn to scale.

Table 1. Connection Table

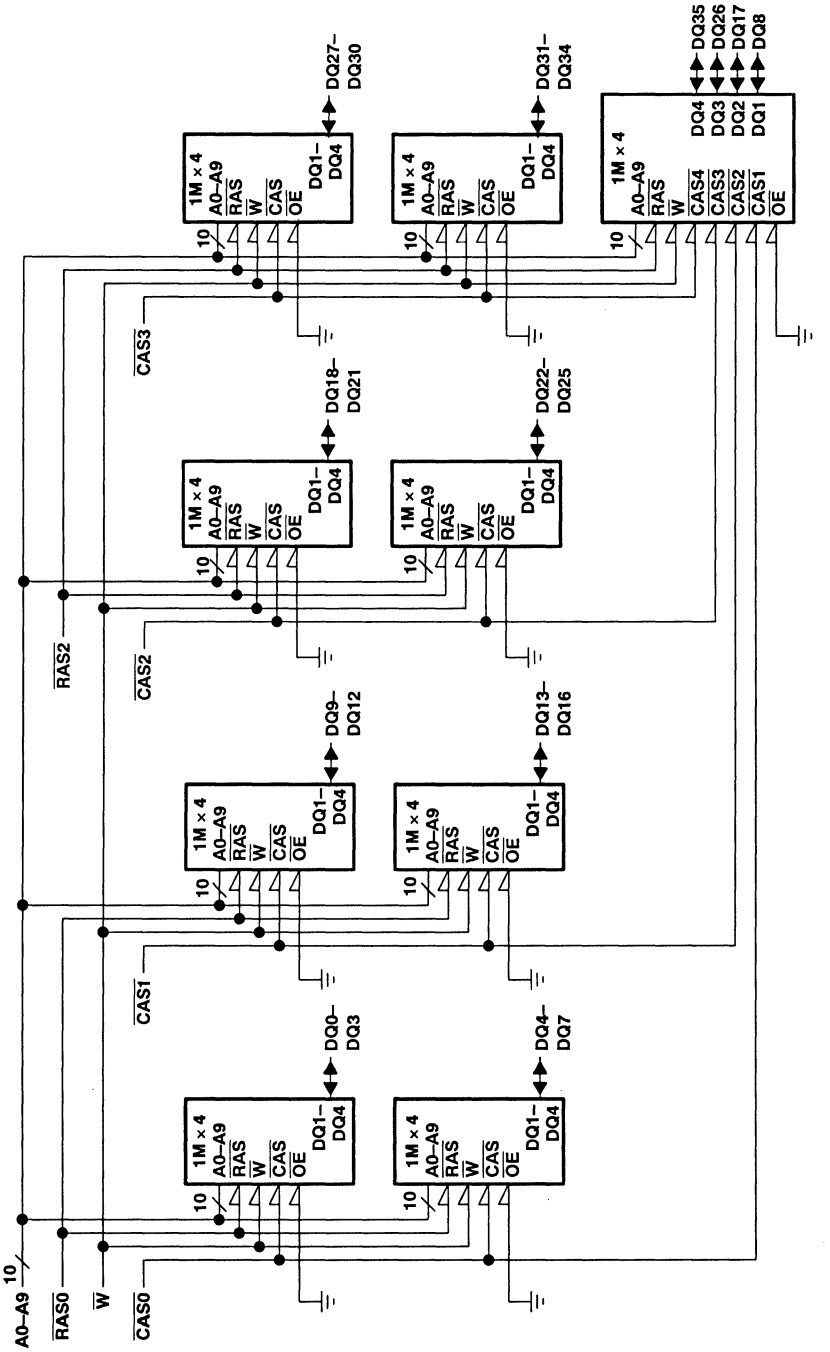
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36B only.

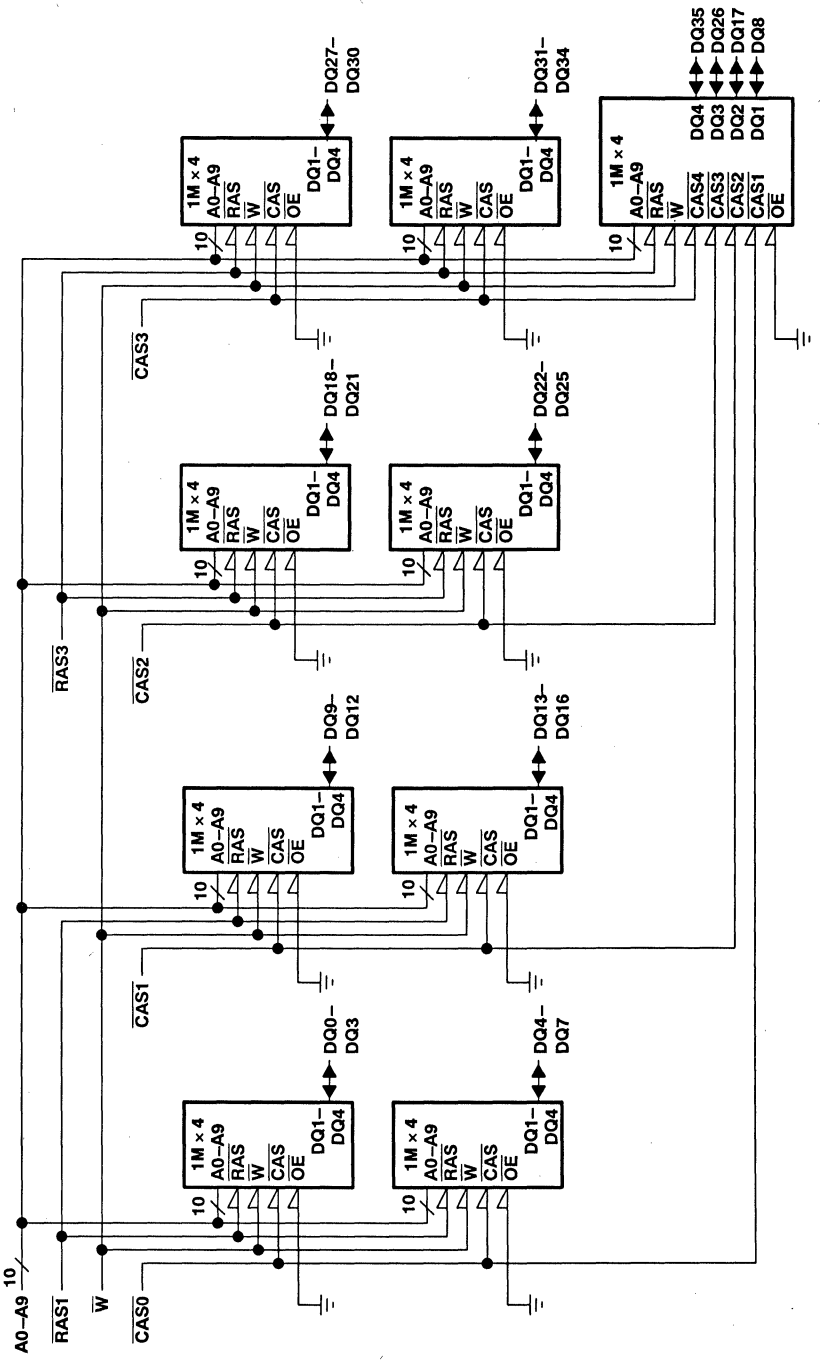
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36B and TM248NBK36B: Nickel plate and gold plate over copper
Contact area for TM124MBK36R and TM248NBK36R: Nickel plate and tin-lead over copper

functional block diagram (TM124MBK36B and TM248NBK36B, side 1)



functional block diagram (TM248NBK36B, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36B-60		'124MBK36B-70		'124MBK36B-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		945		810		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		945		810		720	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V $\overline{RAS}$ low, $\overline{CAS}$ cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248NBK36B-60		'248NBK36B-70		'248NBK36B-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		963		828		738	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		36		36		36	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		18		18		18	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1890		1620		1440	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V $\overline{RAS}$ low, $\overline{CAS}$ cycling		828		738		648	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36B			'248NBK36B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$C_{i(A)}$	Input capacitance, address inputs			45			90	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			35			35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			21			42	pF
$C_{i(W)}$	Input capacitance, write-enable input			63			126	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7			14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36B-60 '248NBK36B-60		'124MBK36B-70 '248NBK36B-70		'124MBK36B-80 '248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36B-60 '248NBK36B-60		'124MBK36B-70 '248NBK36B-70		'124MBK36B-80 '248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle time	130		153		175		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time (see Note 9)	10		10		10		ns

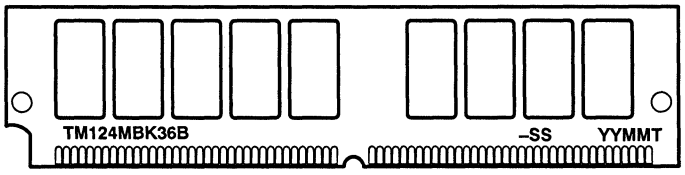
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124MBK36B-60 '248NBK36B-60		'124MBK36B-70 '248NBK36B-70		'124MBK36B-80 '248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

device symbolization (TM124MBK36B illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

SMMS138A–MARCH 1992–REVISED JANUARY 1993

- **Organization**
  TM124MBK36C . . . 1 048 576 × 36
  TM248NBK36C . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-pin Leadless Single In-Line Memory Module (SIMM)**
- **TM124MBK36C – Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 4-Megabit Quad-$\overline{CAS}$ Dynamic RAM in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248NBK36C – Utilizes Sixteen 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 4-Megabit Quad-$\overline{CAS}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36C-60	60 ns	30 ns	15 ns	110 ns
'124MBK36C-70	70 ns	35 ns	18 ns	130 ns
'124MBK36C-80	80 ns	40 ns	20 ns	150 ns
'248NBK36C-60	60 ns	30 ns	15 ns	110 ns
'248NBK36C-70	70 ns	35 ns	18 ns	130 ns
'248NBK36C-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  – TM124MBK36C
  – TM248NBK36C
- **Tin-Lead (Solder) Tabbed Versions**
  – TM124MBK36S
  – TM248NBK36S

description

TM124MBK36C

The TM124MBK36C is a dynamic random-access memory organized as four times 1 048 576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and two TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ dynamic RAMs, in 24/26-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheets, respectively.

The TM124MBK36C is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36C features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM248NBK36C

The TM248NBK36C is a dynamic random-access memory organized as four times 2 097 152 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of sixteen TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and four TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ dynamic RAMs, in 24/26-lead plastic small- outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 or TMS44460 data sheet, respectively.

The TM248NBK36C is available in the double-sided BK leadless module for use with sockets.

The TM248NBK36C features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

operation

TM124MBK36C

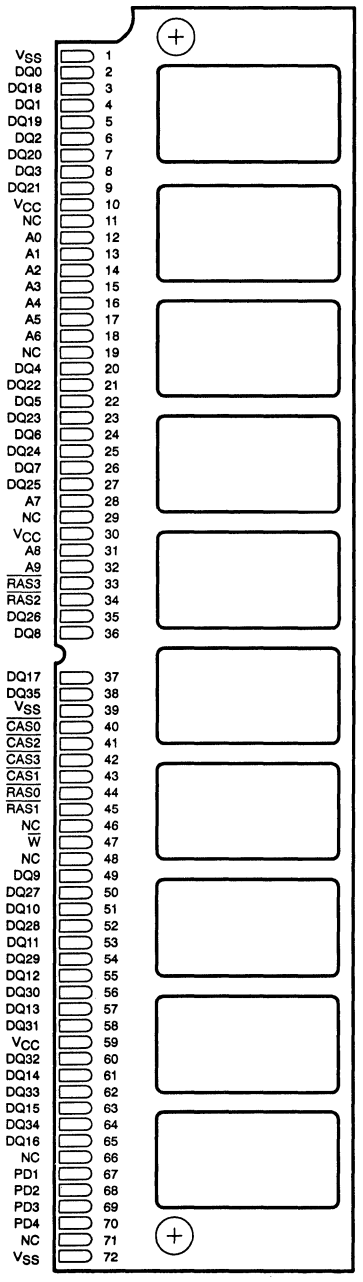
The TM124MBK36C operates as eight TMS44400DJs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

TM248NBK36C

The TM248NBK36C operates as sixteen TMS44400DJs and four TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

BK SINGLE IN-LINE MODULE†

(TOP VIEW)

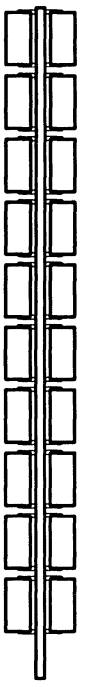


TM124MBK36C†

(SIDE VIEW)

TM248NBK36C†

(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36C	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36C	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are for pinout reference only and are not drawn to scale.

Table 1. Connection Table

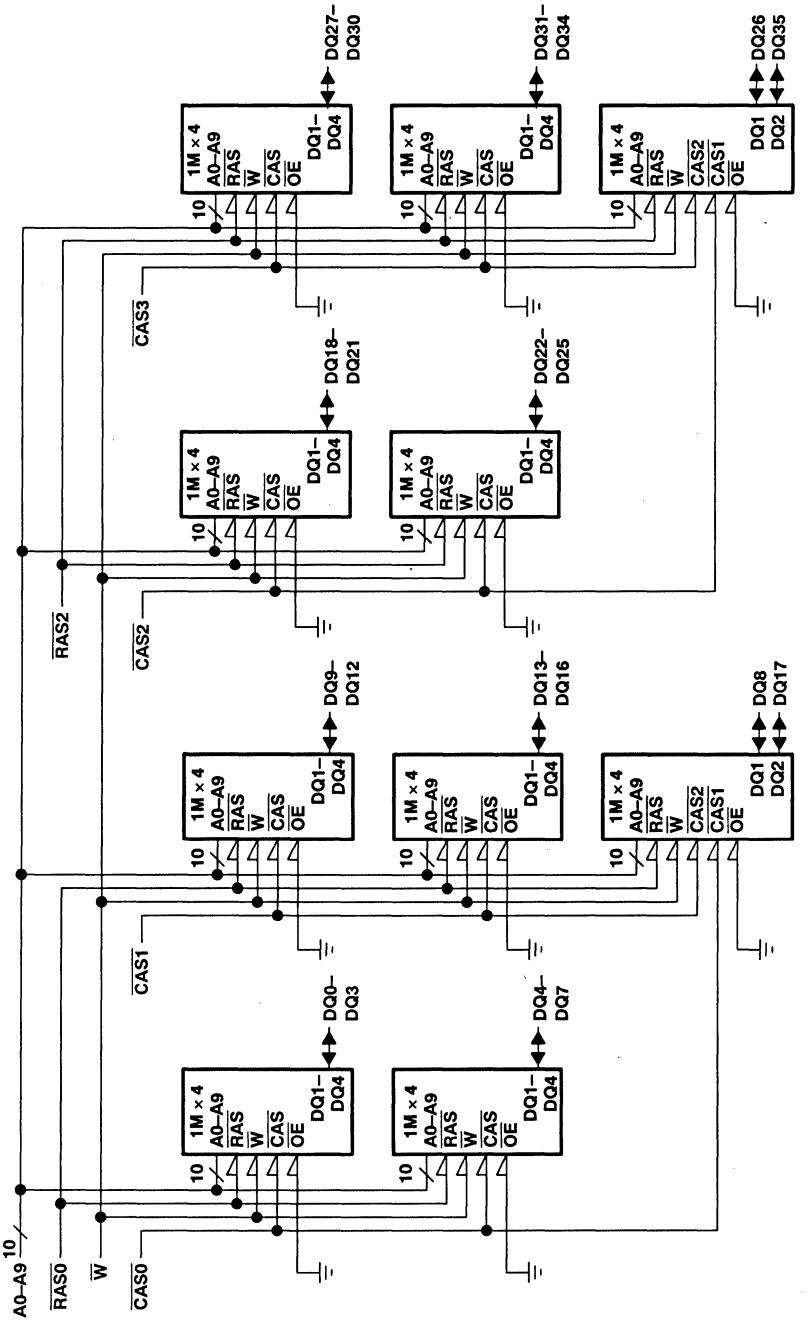
DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36C only.

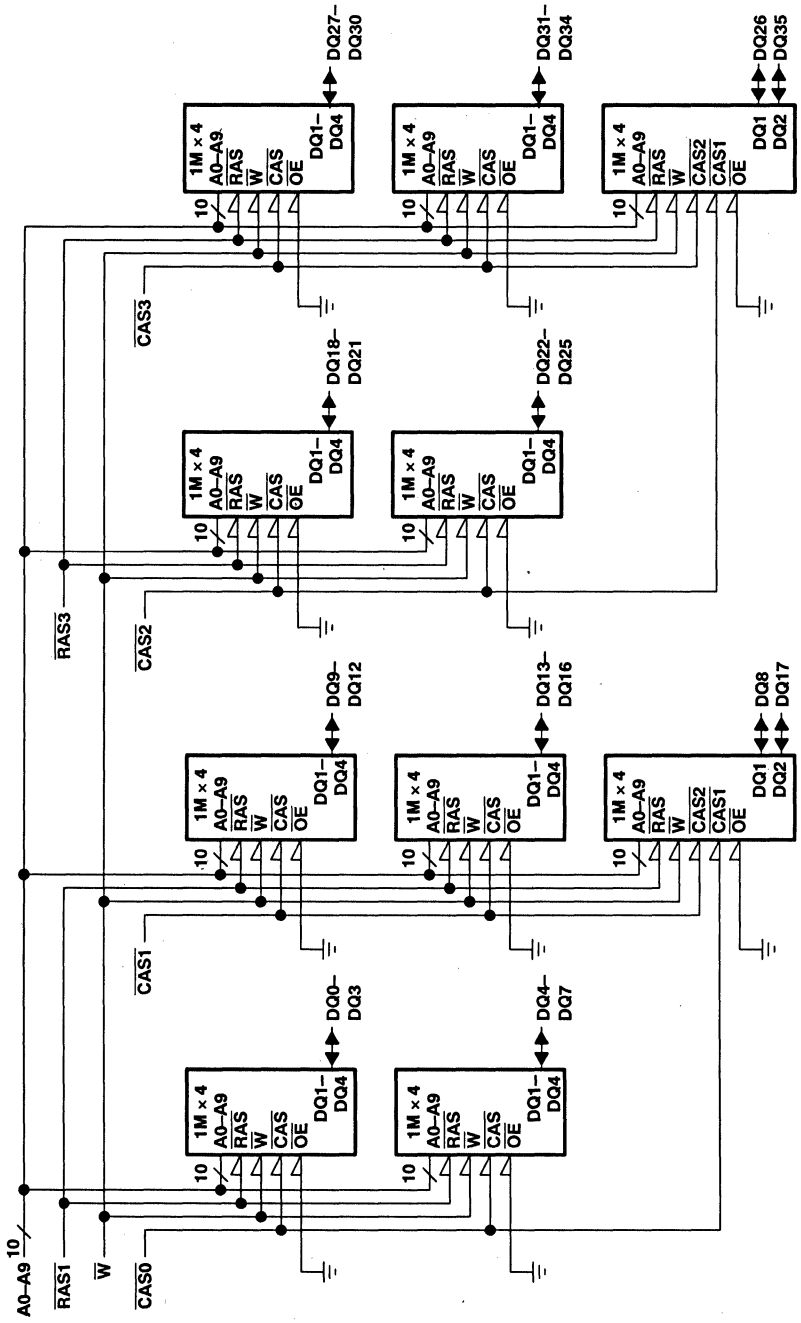
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36C and TM248NBK36C: Nickel plate and gold plate over copper
Contact area for TM124MBK36S and TM248NBK36S: Nickel plate and tin-lead over copper

functional block diagram (for TM124MBK36C and TM248NBK36C, Side 1)



functional block diagram (for TM248NBK36C, Side 2)



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 10 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36C-60		'124MBK36C-70		'124MBK36C-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1050		900		800	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		20		20		20	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		10		10		10	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1050		900		800	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		900		800		700	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248NBK36C-60		'248NBK36C-70		'248NBK36C-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1070		920		820	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		40		40		40	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		2100		1800		1600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		920		820		720	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36C			'248NBK36C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$C_{i(A)}$	Input capacitance, address inputs			50			100	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			35			35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			21			42	pF
$C_{i(W)}$	Input capacitance, write-enable input			70			140	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7			14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle time	130		153		175		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time (see Note 9)	10		10		10		ns

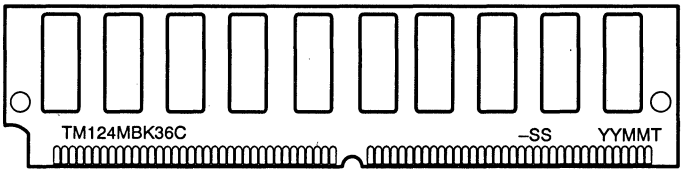
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	$\overline{W}$-high hold time (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

device symbolization (TM124MBK36C illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

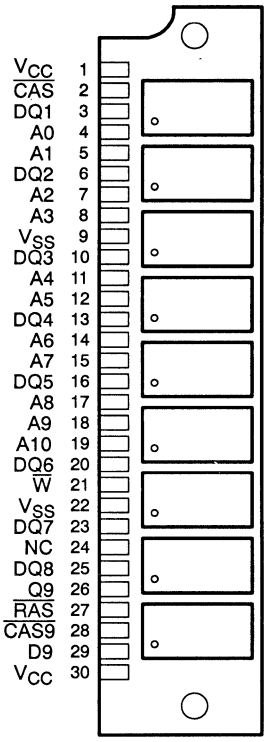
NOTE: Location of symbolization may vary.

- **Organization . . . 4 194 304 × 9**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Nine 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TM4100EAD9-60	60 ns	15 ns	110 ns
TM4100EAD9-70	70 ns	18 ns	130 ns
TM4100EAD9-80	80 ns	20 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE†
(TOP VIEW)



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
D9	Data In
NC	No Internal Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4100EAD9 is a dynamic random-access memory module organized as 4 194 304 × 9 [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin leadless single in-line memory module (SIMM).

This module is composed of nine TMS44100DJ, 4 194 304 × 1-bit dynamic RAMs each in a 20/26-lead plastic small-outline J-lead package (SOJ) mounted on a substrate with decoupling capacitors.

The TM4100EAD9 is available in the AD single-sided, leadless module for use with sockets.

The TM4100EAD9 is characterized for operation from 0°C to 70°C.

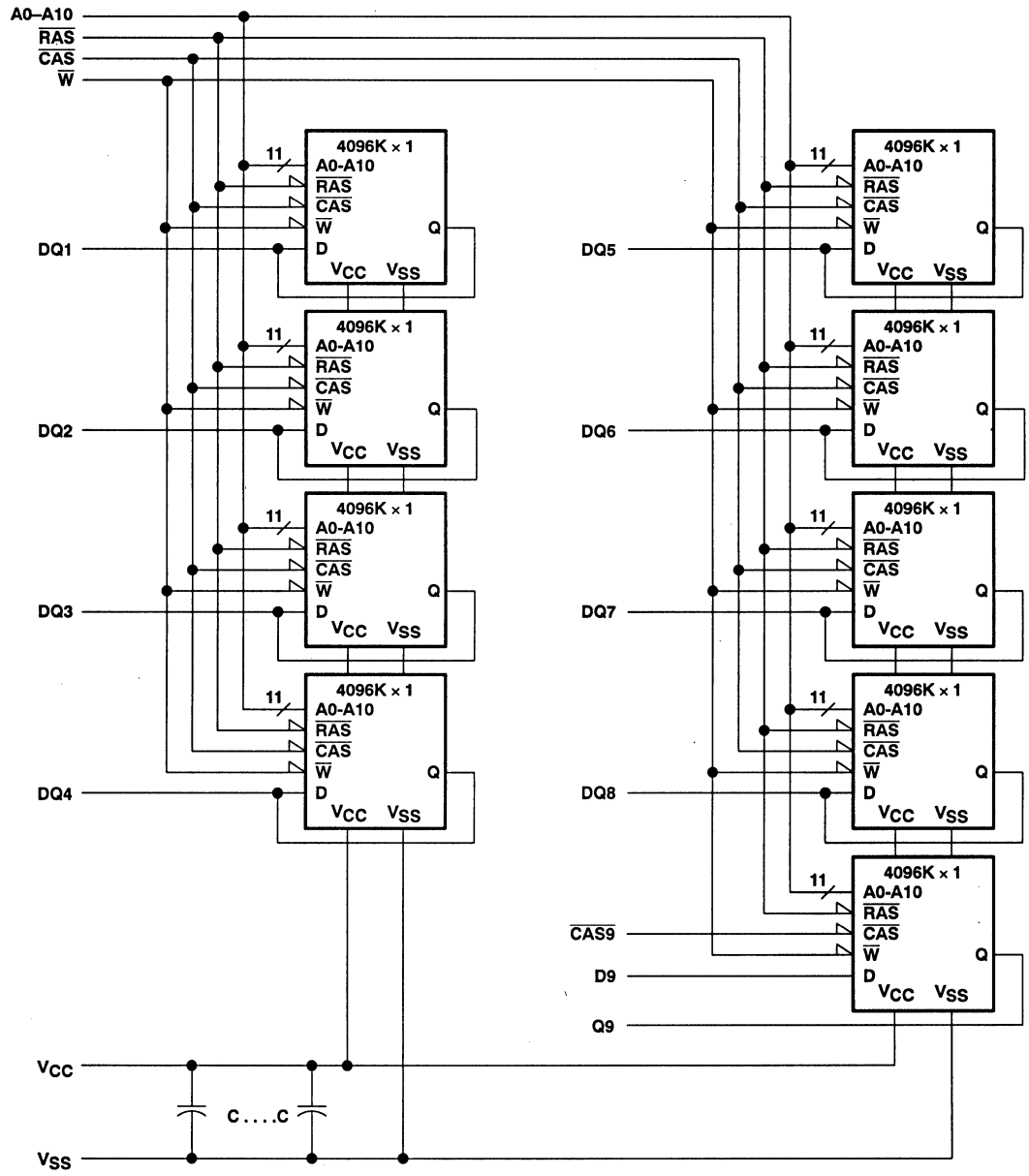
operation

The TM4100EAD9 operates as nine TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100EAD9 dictates the use of early write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		945		810		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	
I_{CC3}	Average refresh current (RAS only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		945		810		720	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		45	pF
$C_{i(D)}$	Input capacitance, data input (pin D9)		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		63	pF
$C_{i(W)}$	Input capacitance, write-enable input		63	pF
$C_{o(DQ)}$	Output capacitance (pins DQ1–DQ8)		12	pF
C_o	Output capacitance (pin Q9)		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle time (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{DH}	Data hold time (see Note 10)	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns

Continued next page.

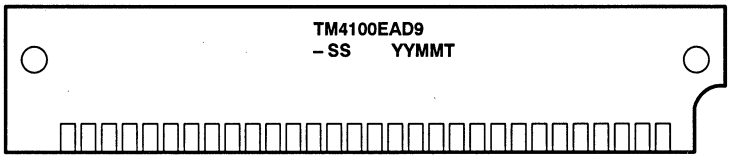
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of symbolization may vary.

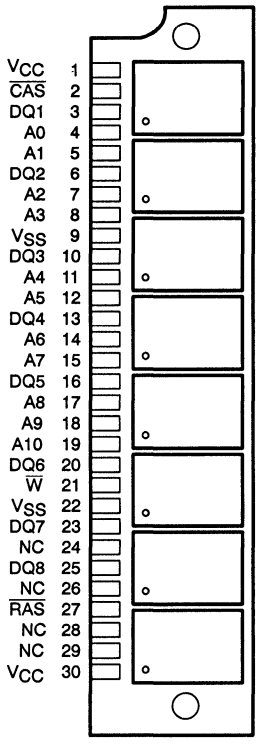
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

- **Organization . . . 4 194 304 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'4100GAD8-60	60 ns	30 ns	15 ns	110 ns
'4100GAD8-70	70 ns	35 ns	18 ns	130 ns
'4100GAD8-80	80 ns	40 ns	20 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE†
(TOP VIEW)



† The package shown is for pinout reference only.

description

The TM4100GAD8 is a dynamic random-access memory module organized as 4 194 304 × 8-bits in a 30-pin leadless single in-line memory module (SIMM).

The SIMM is composed of eight TMS44100DJ, 4 194 304 × 1-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJ), mounted on a substrate with decoupling capacitors.

The TM4100GAD8 is available in the AD single-sided, leadless module for use with sockets.

The TM4100GAD8 is characterized for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

operation

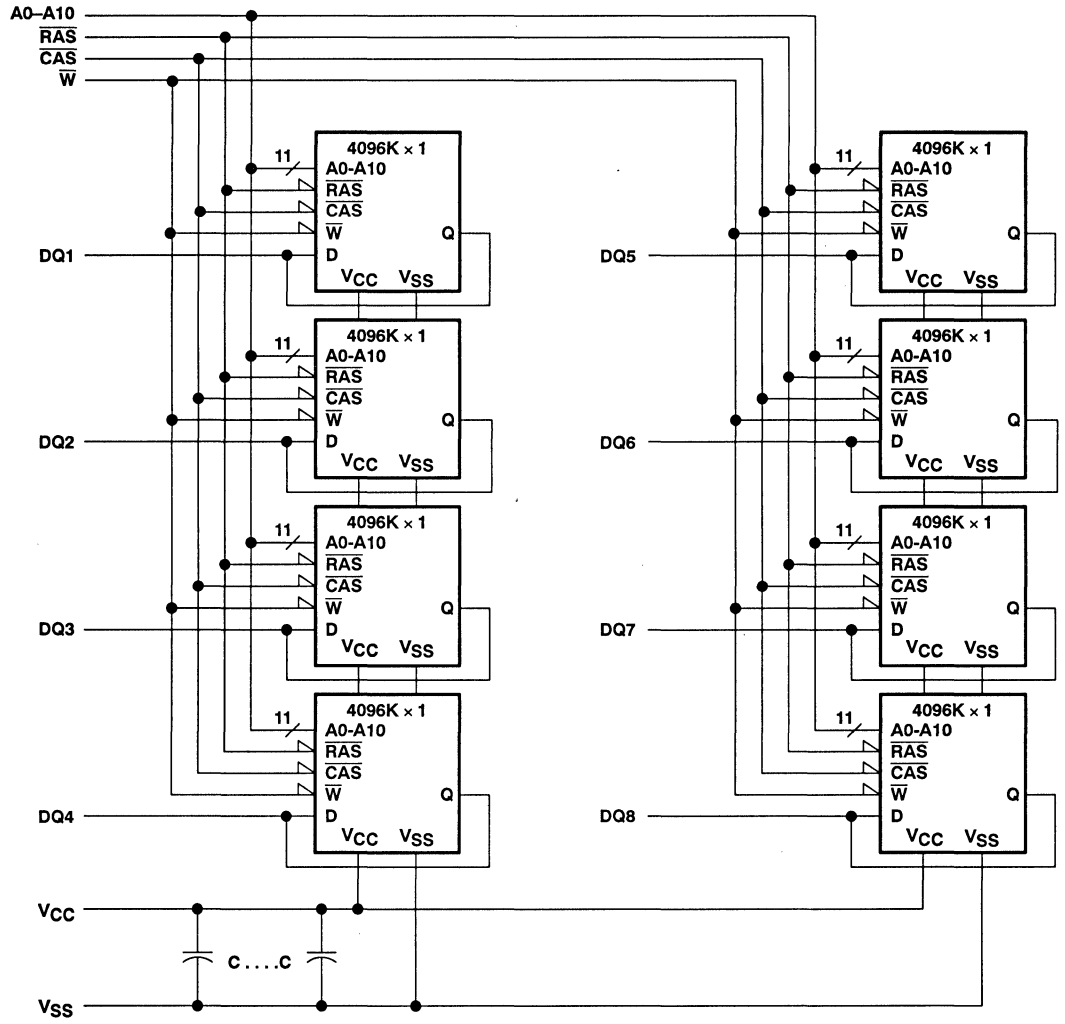
The TM4100GAD8 operates as eight TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100GAD8 dictates the use of early write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Supply voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		840		720		640	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high,		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $t_{c(P)}$ = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		56	pF
$C_{i(W)}$	Input capacitance, write-enable input		56	pF
C_o	Output capacitance (pins DQ1–DQ8)		12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns

Continued next page.

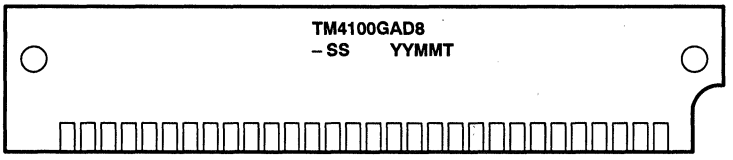
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UINT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTE 11: The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

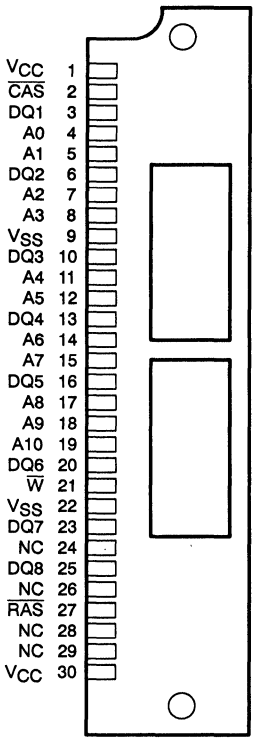
NOTE: The location of symbolization may vary.

- **Organization . . . 4 194 304 × 8**
- **Single 5-V Power Supply**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Two 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 32 ms (2048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497GAD8A-60	60 ns	30 ns	15 ns	110 ns
'497GAD8A-70	70 ns	35 ns	18 ns	130 ns
'497GAD8A-80	80 ns	40 ns	20 ns	150 ns
'497GAD8A-10	100 ns	50 ns	25 ns	180 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



† The package shown is for pinout reference only.

description

The TM497GAD8A is a 32M dynamic random-access memory module organized as 4 194 304 × 8-bits in a 30-pin leadless single in-line memory module (SIMM).

The SIMM is composed of two TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs in 24/28-lead plastic small-outline J-lead packages (SOJ), mounted on a substrate with decoupling capacitors.

The TM497GAD8A is characterized for operation from 0°C to 70°C.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

ADVANCE INFORMATION

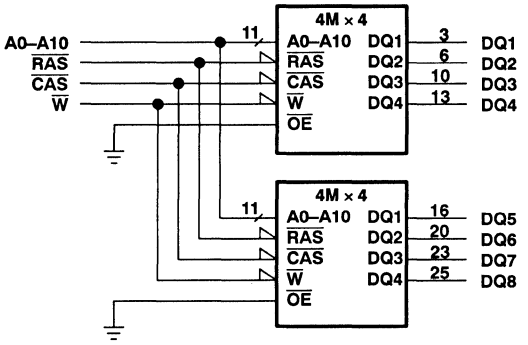
operation

The TM497GAD8A operates as two TMS417400DZs connected as shown in the functional block diagram. Refer to the TMS417400 data sheet for details of its operation. The common I/O feature of the TM497GAD8A dictates the use of early write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 2 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497GAD8A-60		'497GAD8A-70		'497GAD8A-80		'497GAD8A-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		240		220		200		180	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		4		4		4		4	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2		2	mA
I_{CC3}	Average refresh current (RAS-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		240		220		200		180	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		140		120		100		90	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		10	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		14	pF
$C_{i(W)}$	Input capacitance, write-enable input		14	pF
C_o	Output capacitance (pins DQ1–DQ8)		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497GAD8A-60		'497GAD8A-70		'497GAD8A-80		'497GAD8A-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable; start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497GAD8A-60		'497GAD8A-70		'497GAD8A-80		'497GAD8A-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{PC}	Random read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 9)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 9)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

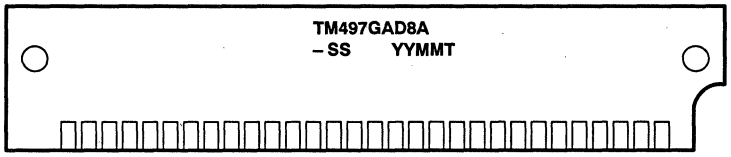
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'497GAD8A-60		'497GAD8A-70		'497GAD8A-80		'497GAD8A-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 10)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		32		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

ADVANCE INFORMATION

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of the part number may vary.

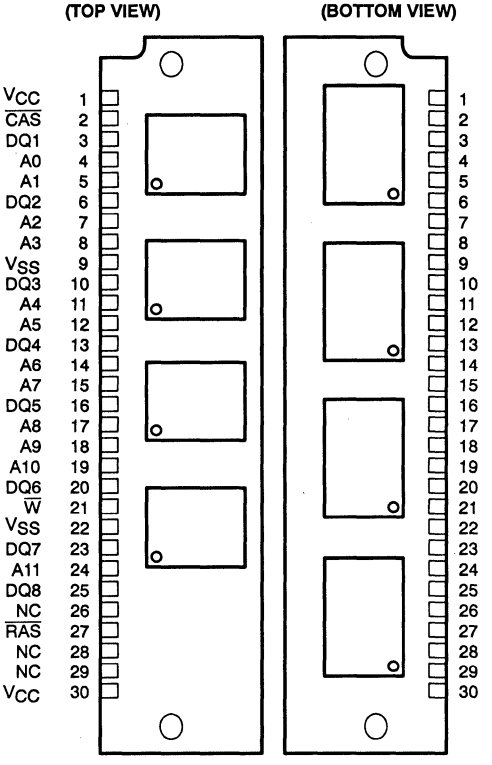
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

- **Organization . . . 16 777 216 × 8**
- **Single 5-V Power Supply**
- **30-Pin Single In-Line Memory Module (SIMM) for Use with Sockets**
- **Utilizes Eight 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 64 ms (4096 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'16100GBD8-60	60 ns	30 ns	15 ns	110 ns
'16100GBD8-70	70 ns	35 ns	18 ns	130 ns
'16100GBD8-80	80 ns	40 ns	20 ns	150 ns
'16100GBD8-10	100 ns	50 ns	25 ns	180 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

BD SINGLE-IN-LINE PACKAGE†



† The package shown is for pinout reference only.

description

The TM16100GBD8 is a 128M (dynamic) random-access memory module organized as 16 777 216 × 8 bits in a 30-pin leadless single in-line memory module (SIMM).

The SIMM is composed of eight TMS416100DZ, 16 777 216 × 1-bit dynamic RAMs in 24/28-lead plastic small-outline J-lead packages (SOJ), mounted on a substrate with decoupling capacitors.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The TM16100GBD8 is available in the BD double-sided, leadless module for use with sockets.

The TM16100GBD8 is characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

operation

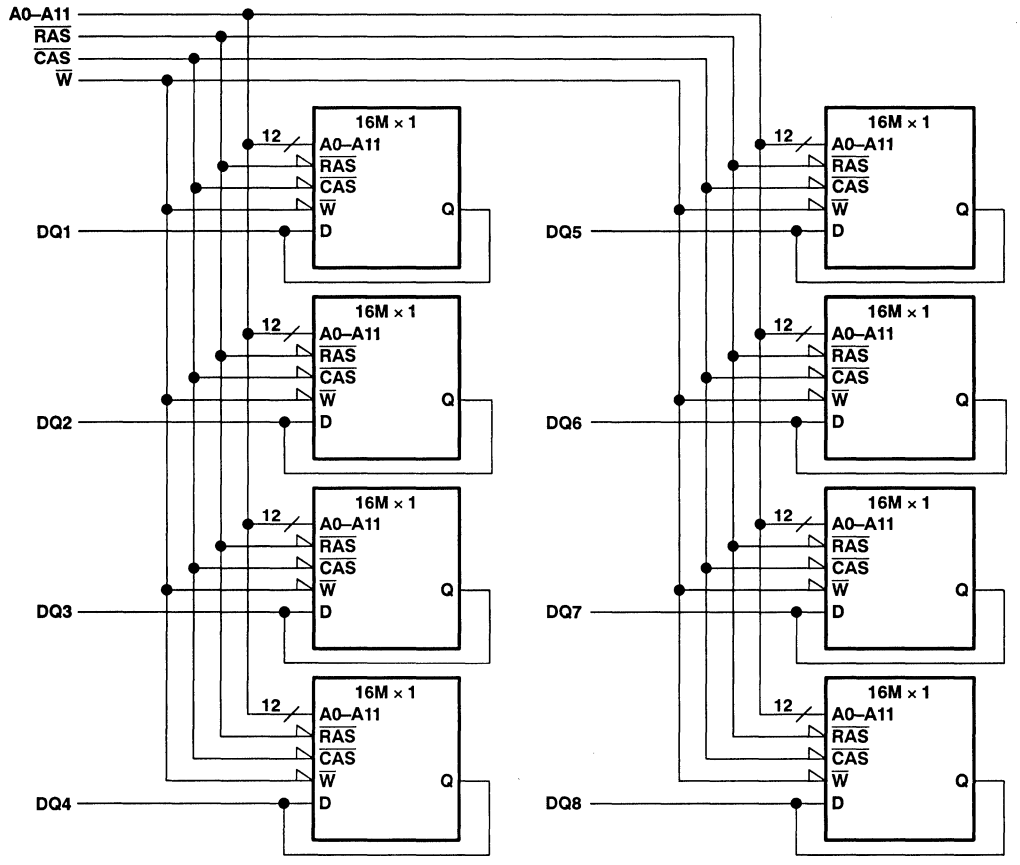
The TM16100GBD8 operates as eight TMS416100DZs connected as shown in the functional block diagram. Refer to the TMS416100 data sheet for details of its operation. The common I/O feature of the TM16100GBD8 dictates the use of early write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

functional block diagram



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'16100GBD8-60		'16100GBD8-70		'16100GBD8-80		'16100GBD8-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		720		640		560		480	mA
I_{CC2}	Standby Current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16		16	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8		8	mA
I_{CC3}	Average refresh current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		720		640		560		480	mA
I_{CC4}	Average page current (see Note 4)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		560		480		400		360	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		56	pF
$C_{i(W)}$	Input capacitance, write-enable input		56	pF
C_o	Output capacitance (pins DQ1–DQ8)		12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'16100GBD8-60		'16100GBD8-70		'16100GBD8-80		'16100GBD8-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable time; from start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'16100GBD8-60		'16100GBD8-70		'16100GBD8-80		'16100GBD8-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 9)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 9)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

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TEXAS INSTRUMENTS
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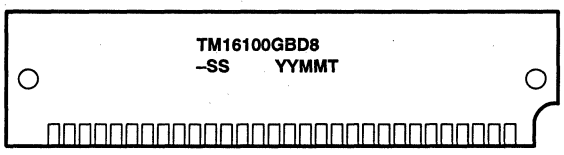
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'16100GBD8-60		'16100GBD8-70		'16100GBD8-80		'16100GBD8-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 10)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		64		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to guarantee access time.

ADVANCE INFORMATION

device symbolization



MM = Month Code
YY = Year Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of the part number may vary.

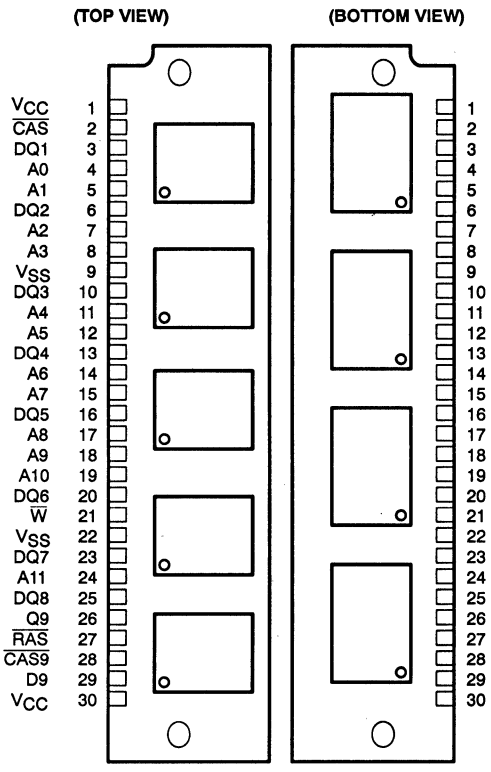
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

- **Organization . . . 16 777 216 × 9**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Nine 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 64 ms (4096 Cycles)**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance of Unmounted RAMs:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
TM16100EBD9-60	60 ns	15 ns	110 ns
TM16100EBD9-70	70 ns	18 ns	130 ns
TM16100EBD9-80	80 ns	20 ns	150 ns
TM16100EBD9-10	100 ns	25 ns	180 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free Air Temperature 0°C to 70°C**

BD SINGLE IN-LINE PACKAGE†



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1–DQ8	Data In / Data Out
D9	Data In
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM16100EBD9 is 144M dynamic random-access memory module organized as 16 777 216 bits [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin leadless single in-line memory module (SIMM).

The SIMM is composed of nine TMS416100, 16 777 216 × 1 bit dynamic RAMs, each in a 24/28-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors.

The TM16100EBD9 is available in the BD double-sided, leadless module for use with sockets.

The TM16100EBD9 is characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

ADVANCE INFORMATION

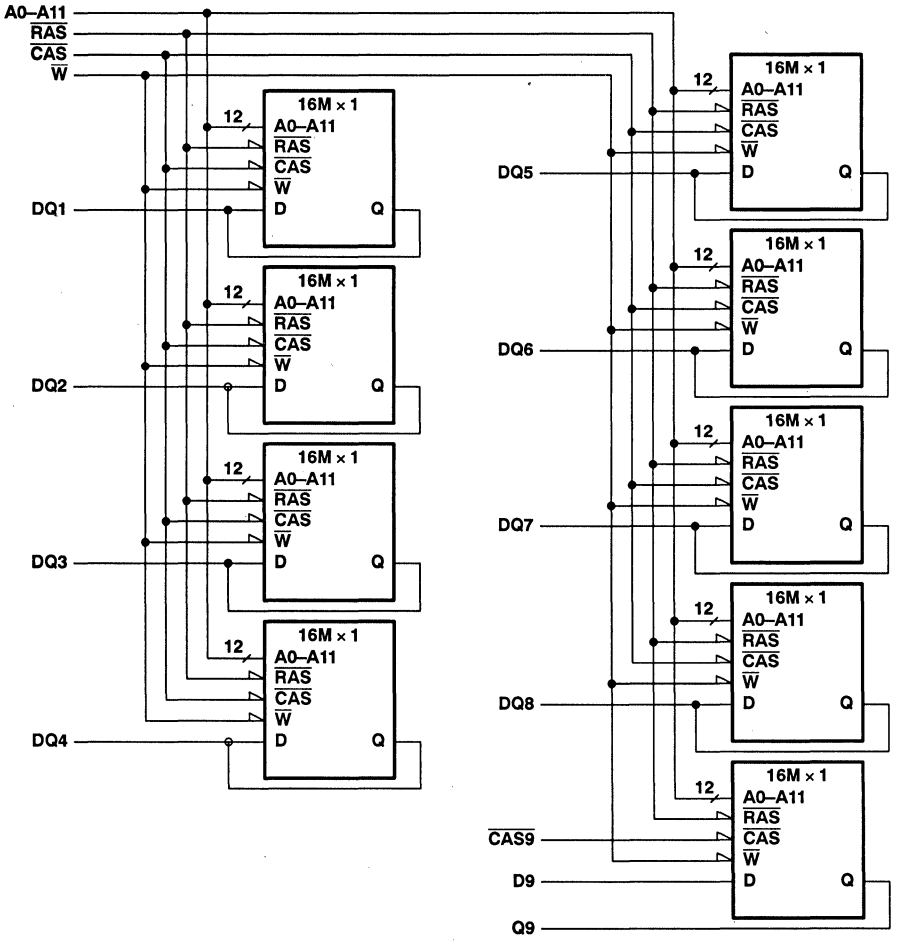
operation

The TM16100EBD9 operates as nine TMS416100s connected as shown in the functional block diagram. Refer to the TMS416100 data sheet for details of its operation. The common I/O feature of the TM16100EBD9 dictates the use of early write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation: ..... 9 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'16100EBD9-60		'16100EBD9-70		'16100EBD9-80		'16100EBD9-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		810		720		630		540	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} –0.2 V (CMOS)		9		9		9		9	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		810		720		630		540	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		630		540		450		405	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		45	pF
$C_{i(D)}$	Input capacitance, data input (D9 only)		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		63	pF
$C_{i(W)}$	Input capacitance, write-enable input		63	pF
$C_{o(DQ)}$	Output capacitance (DQ1–DQ8)		12	pF
C_o	Output capacitance (Q9 only)		7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'16100EBD9-60		'16100EBD9-70		'16100EBD9-80		'16100EBD9-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OH}	Output disable; from start of $\overline{CAS}$ high	3		3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	0	25	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'16100EBD9-60		'16100EBD9-70		'16100EBD9-80		'16100EBD9-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		180		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		55		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 9)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

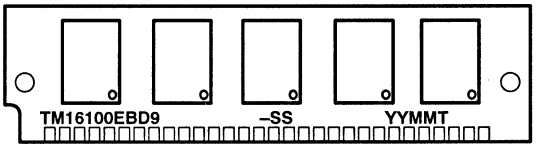
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'16100EBD9-60		'16100EBD9-70		'16100EBD9-80		'16100EBD9-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		64		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	3	30	ns

NOTE 11: The maximum value is specified only to assure access time.

device symbolization

The specifications contained in this data sheet are applicable to all TM16100EBD9s symbolized as shown in Figure 1.



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of the part number may vary.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
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- **Organization**
  TM497BBK32 . . . 4 194 304 × 32
  TM893CBK32 . . . 8 388 608 × 32
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497BBK32 – Utilizes Eight 16-Megabit Dynamic RAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893CBK32 – Utilizes Sixteen 16-Megabit Dynamic RAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 32 ms (2048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, in Four Blocks**
- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497BBK32-60	60 ns	30 ns	15 ns	110 ns
'497BBK32-70	70 ns	35 ns	18 ns	130 ns
'497BBK32-80	80 ns	40 ns	20 ns	150 ns
'893CBK32-60	60 ns	30 ns	15 ns	110 ns
'893CBK32-70	70 ns	35 ns	18 ns	130 ns
'893CBK32-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  TM497BBK32
  TM893CBK32
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM497BBK32S
  TM893CBK32S

ADVANCE INFORMATION

description

TM497BBK32

The TM497BBK32 is a 128M dynamic random-access memory organized as four times 4 194 304 × 8 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs, each in 24/28-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. The TMS417400DZ is described in the TMS417400 data sheet.

The TM497BBK32 SIMM is available in the single-sided BK leadless module for use with sockets.

The TM497BBK32 SIMM features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C

TM893CBK32

The TM893CBK32 is a 256M dynamic random-access memory organized as four times 8 388 608 × 8 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of sixteen TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs, each in 24-lead plastic small-outline J-lead packages (SOJs) mounted on a substrate with decoupling capacitors. The TMS417400DZ is described in the TMS417400 data sheet.

The TM893CBK32 is available in the double-sided BK leadless module for use with sockets.

The TM893CBK32 features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

operation

TM497BBK32

The TM497BBK32 operates as eight TMS417400DZs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

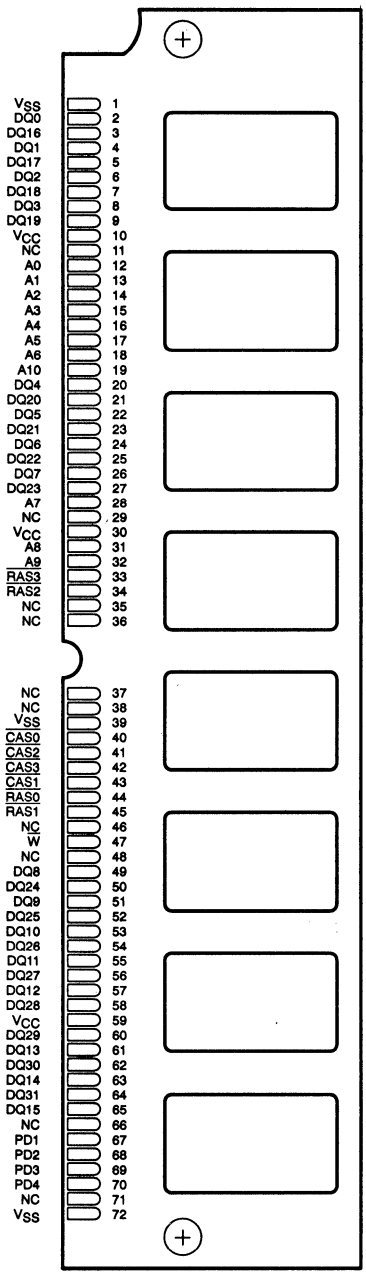
TM893CBK32

The TM893CBK32 operates as sixteen TMS417400DZs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ in order to retain data. Address line A10 must be used as the most significant refresh address line (lowest frequency) to assure correct refresh. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

BK SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



TM497BBK32†
(SIDE VIEW)

TM893CBK32†
(SIDE VIEW)

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

† Packages are shown for pinout reference only.

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497BBK32	80 ns	V_{SS}	NC	NC	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC
	60 ns	V_{SS}	NC	NC	NC
TM893CBK32	80 ns	NC	V_{SS}	NC	V_{SS}
	70 ns	NC	V_{SS}	V_{SS}	NC
	60 ns	NC	V_{SS}	NC	NC

† The packages shown here are for pinout reference only and are not drawn to scale.

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Table 1. Connection Table

DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8–DQ15	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ16–DQ23	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ24–DQ31	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM893CBK32 only.

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497BBK32 and TM893CBK32: Nickel plate and gold plate over copper
Contact area for TM497BBK32S and TM893CBK32S: Nickel plate and tin-lead over copper

ADVANCE INFORMATION

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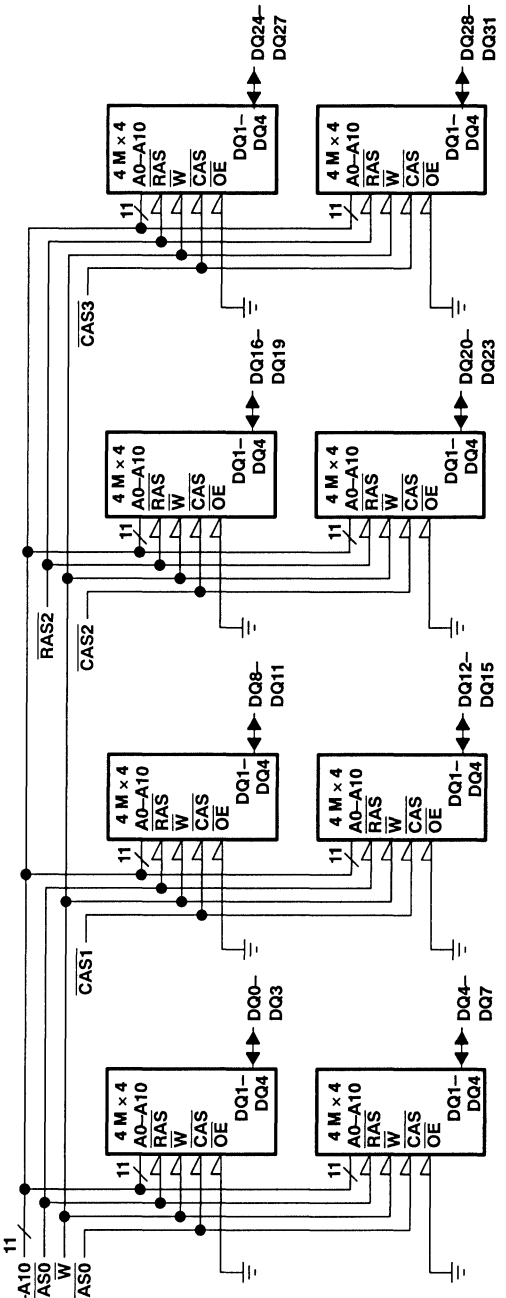
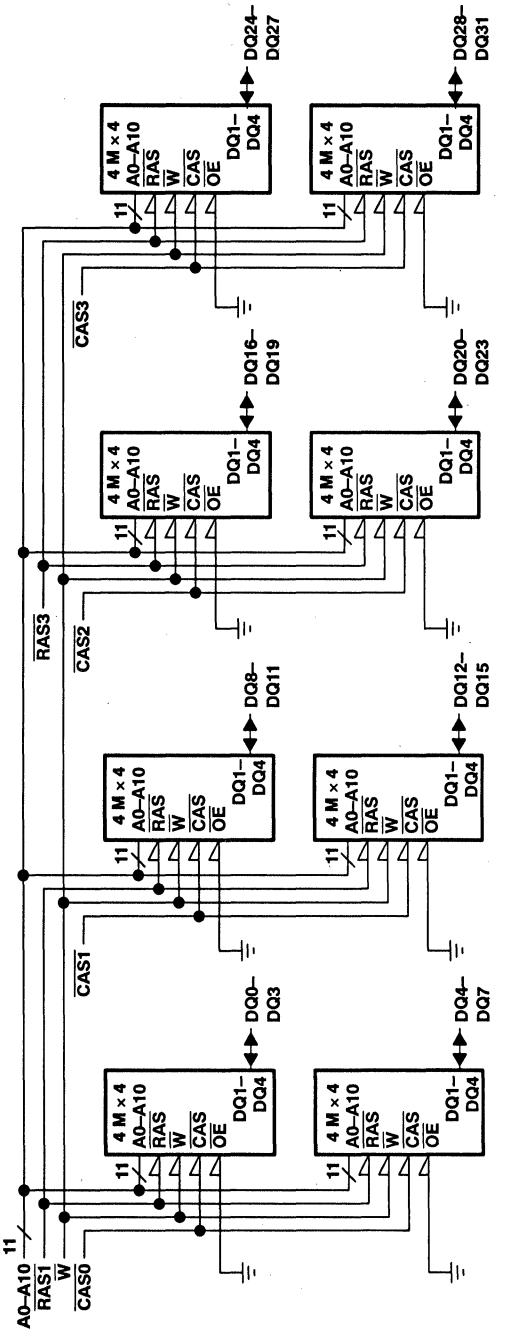
functional block diagram (TM497BBK32 and TM893CBK32, side 1)



ADVANCE INFORMATION

functional block diagram (TM893CBK32, side 2)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation (TM497BBK32) ..... 8 W
(TM893CBK32) ..... 16 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497BBK32-60		'497BBK32-70		'497BBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 80		± 80		± 80	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		960		880		800	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		960		880		800	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		560		480		400	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'893CBK32-60		'893CBK32-70		'893CBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 160		± 160		± 160	μA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	μA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		976		896		816	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		32		32		32	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), after 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (all 4 $\overline{RAS}$ active) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1920		1760		1600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		576		496		416	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'497BBK32			'893CBK32			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$C_{i(A)}$	Input capacitance, address inputs			40			80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			28			28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			14			28	pF
$C_{i(W)}$	Input capacitance, write-enable input			56			112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins			7			14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497BBK32-60 '893CBK32-60		'497BBK32-70 '893CBK32-70		'497BBK32-80 '893CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable from start of $\overline{CAS}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497BBK32-60 '893CBK32-60		'497BBK32-70 '893CBK32-70		'497BBK32-80 '893CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.

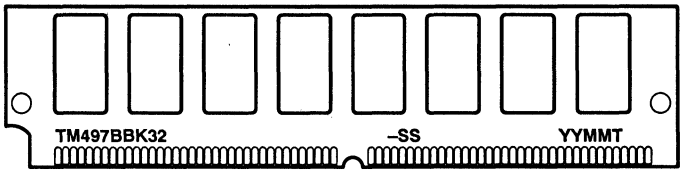
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'497BBK32-60 '893CBK32-60		'497BBK32-70 '893CBK32-70		'497BBK32-80 '893CBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 9)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

ADVANCE INFORMATION

device symbolization (TM497BBK32 Illustrated)



YY = **YEAR CODE**
MM = **MONTH CODE**
T = **ASSEMBLY SITE CODE**
–SS = **SPEED CODE**

NOTE: The location of the part number may vary.

SMMS450–DECEMBER 1992

- **Organization**
  TM497TBM40 . . . 4 194 304 × 40
  TM893VBM40 . . . 8 388 608 × 40
- **Single 5-V Power Supply**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497TBM40 – Utilizes Ten 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893VBM40 – Utilizes Twenty 16-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 32 ms (2048 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**
- **Low Power Dissipation**
- **V_{CC} Tolerance ± 10%**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'497TBM40-60	60 ns	30 ns	15 ns	110 ns
'497TBM40-70	70 ns	35 ns	18 ns	130 ns
'497TBM40-80	80 ns	40 ns	20 ns	150 ns
'893VBM40-60	60 ns	30 ns	15 ns	110 ns
'893VBM40-70	70 ns	35 ns	18 ns	130 ns
'893VBM40-80	80 ns	40 ns	20 ns	150 ns

- **Gold-Tabbed Versions Available:†**
  TM497TBM40
  TM893VBM40
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM497TBM40S
  TM893VBM40S

ADVANCE INFORMATION

description

TM497TBM40

The TM497TBM40 is a 160M dynamic random-access memory organized as 4M × 40 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of ten TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs, each in a 400-mil 24/28-lead plastic small-outline J-lead (SOJ) package mounted on a substrate together with decoupling capacitors. Each TMS417400DZ is described in the TMS417400 data sheet.

The TM497TBM40 can be used in systems with fewer than 40 data bits. In those applications, it is recommended that any unused DQ pins be connected to either V_{SS} or V_{CC} through a series resistor with a typical value between 5 kΩ and 10 kΩ.

The TM497TBM40 is available in the single-sided BM leadless module for use with sockets.

The TM497TBM40 is rated for operation from 0°C to 70°C. This device features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

TM893VBM40

The TM893VBM40 is a 320M dynamic random-access memory organized as 8M × 40 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of twenty TMS417400DZ, 4 194 304 × 4-bit dynamic RAMs, each in a 400-mil 24/28-lead plastic small-outline J-lead (SOJ) package mounted on a substrate with decoupling capacitors. Each TMS417400DZ is described in the TMS417400 data sheet.

The TM893VBM40 can be used in systems with fewer than 40 data bits. In those applications, it is recommended that any unused DQ pins be connected to either V_{SS} or V_{CC} through a series resistor with a typical value between 5 kΩ and 10 kΩ.

† Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

The TM893VBM40 is available in the double-sided BM leadless module for use with sockets.

The TM893VBM40 is rated for operation from 0°C to 70°C. This device features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

operation

TM497TBM40

The TM497TBM40 operates as ten TMS417400DZs connected as shown in the functional block diagram. Refer to the TMS417400 data sheet for details of operation.

TM893VBM40

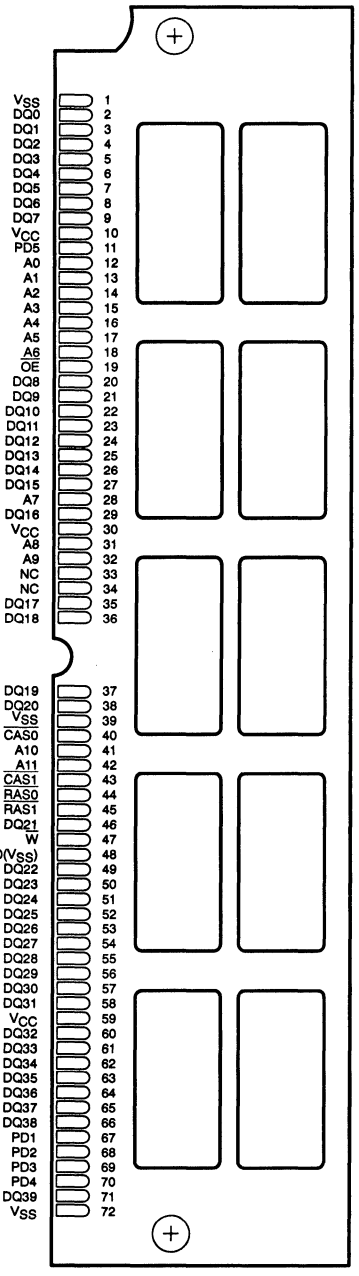
The TM893VBM40 operates as twenty TMS417400DZs connected as shown in the functional block diagram. Refer to the TMS417400 data sheet for details of operation.

single in-line-memory module and components

PC substrate: 1, 27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Contact area for TM497TBM40 and TM893VBM40: Nickel plate and gold plate over copper.
Contact area for TM497TBM40S and TM893VBM40S: Nickel plate and tin-lead over copper.

BM SINGLE-IN-LINE PACKAGE†

(TOP VIEW)

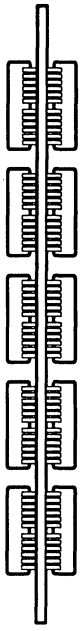


TM497TBM40
BM SINGLE-IN-LINE PACKAGE†

(SIDE VIEW)

TM893VBM40
BM SINGLE-IN-LINE PACKAGE†

(SIDE VIEW)



PIN NOMENCLATURE

A0–A10	Address Inputs
A11	NC – Reserved for 4K refresh version
$\overline{CAS0}$, $\overline{CAS1}$	Column-Address Strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row-Address Strobe
DQ0–DQ39	Data In/Data Out
$\overline{W}$	Write Enable
NC	No External Connection
V_{CC}	5-V Supply
V_{SS}	Ground
PD1–PD5	Presence Detects
$\overline{OE}$	Output Enable

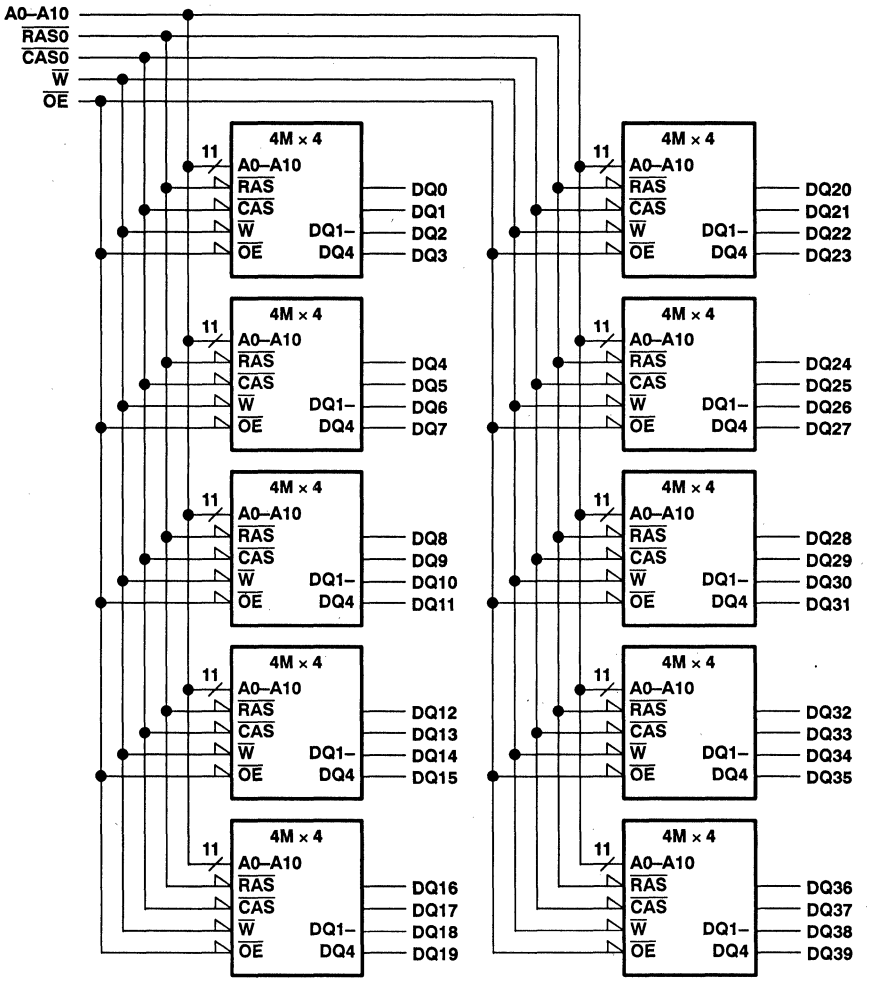
PRESENCE DETECT

SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)	PD5 (11)
TM497TBM40	80 ns	V_{SS}	NC	NC	V_{SS}	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC	V_{SS}
	60 ns	V_{SS}	NC	NC	NC	V_{SS}
TM893VBM40	80 ns	NC	V_{SS}	NC	V_{SS}	V_{SS}
	70 ns	NC	V_{SS}	V_{SS}	NC	V_{SS}
	60 ns	NC	V_{SS}	NC	NC	V_{SS}

† The packages shown here are for pinout reference only and are not drawn to scale.

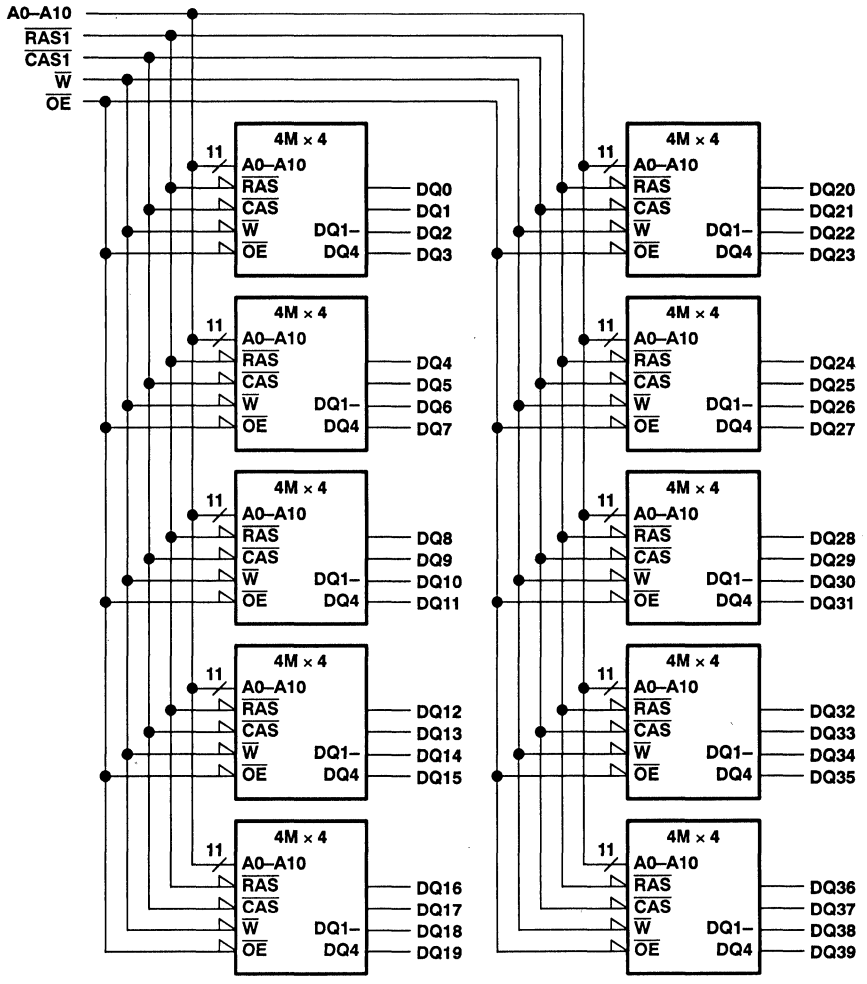
ADVANCE INFORMATION

functional block diagram (TM497TBM40 and TM893VBM40, side 1)



ADVANCE INFORMATION

functional block diagram (TM893VBM40, side 2)



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation (TM497TBM40) ..... 10 W
(TM893VBM40) ..... 20 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

PARAMETER		'497TBM40		'893VBM40		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inuts		50		100	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$ input		70		140	pF
$C_{i(W)}$	Input capacitance, $\overline{WE}$ input		70		140	pF
$C_{i(RC)}$	Input capacitance, $\overline{RAS}$, $\overline{CAS}$ inputs		70		70	pF
$C_{o(DQ)}$	Output capacitance, DQ pins		7		14	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

ADVANCE INFORMATION

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'497TBM40-60		'497TBM40-70		'497TBM40-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 100		± 100		± 100	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 4)	V_{CC} = 5.5 V, Minimum cycle		1200		1100		1000	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		20		20		20	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		10		10		10	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1200		1100		1000	mA
I_{CC4}	Average page current (see Note 5)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		700		600		500	mA

NOTES: 4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'893VBM40-60		'893VBM40-70		'893VBM40-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 200		± 200		± 200	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write current (One RAS active, see Note 4)	V_{CC} = 5.5 V, Minimum cycle		1220		1120		1020	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL),		40		40		40	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR), (One $\overline{RAS}$ active see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1220		1120		1020	mA
I_{CC4}	Average page current (One $\overline{RAS}$ active, see Note 5)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		620		520	mA

NOTES: 4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497TBM40-60 '893VBM40-60		'497TBM40-70 '893VBM40-70		'497TBM40-80 '893VBM40-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time $\overline{OE}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ low to output	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable $\overline{OE}$	0	15		18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'497TBM40-60 '893VBM40-60		'497TBM40-70 '893VBM40-70		'497TBM40-70 '893VBM40-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle	155		181		205		ns
t_{PC}	Page-mode read or write (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-write	85		96		105		ns
t_{RASP}	$\overline{RAS}$ low pulse duration (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	$\overline{RAS}$ low pulse duration (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	$\overline{CAS}$ low pulse duration (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	$\overline{CAS}$ high pulse duration, page mode	10		10		10		ns
t_{RP}	$\overline{RAS}$ high pulse duration	40		50		60		ns
t_{WP}	$\overline{W}$ low pulse duration	15		15		15		ns
t_{ASC}	Column-address setup	0		0		0		ns
t_{ASR}	Row-address setup	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ setup (CBR refresh)	10		10		10		ns
t_{CAH}	Column-address hold time	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time	10		10		10		ns
t_{RCH}	Read hold time from $\overline{CAS}$ high (see Note 12)	0		0		0		ns

Continued next page.

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

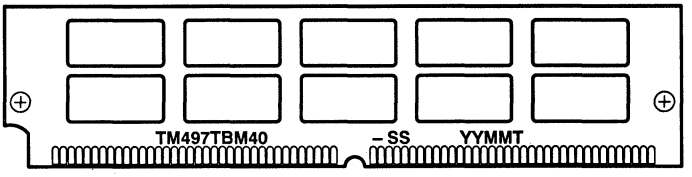
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		'497TBM40-60 '893VBM40-60		'497TBM40-70 '893VBM40-70		'497TBM40-80 '893VBM40-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RRH}	Read hold time from $\overline{RAS}$ high (see Note 12)	5		5		5		ns
t_{WCH}	Write hold time from $\overline{CAS}$ low	15		15		15		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	$\overline{W}$ low from column address (RMW)	55		63		70		ns
t_{CHR}	$\overline{CAS}$ high from $\overline{RAS}$ (CBR)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	$\overline{CAS}$ high from $\overline{RAS}$ low	60		70		80		ns
t_{CSR}	$\overline{RAS}$ low from $\overline{CAS}$ (CBR)	10		10		10		ns
t_{CWD}	$\overline{W}$ low from cas low (RMW)	40		46		50		ns
t_{OEH}	$\overline{OE}$ hold time	15		18		20		ns
t_{OED}	OE to data delay	15		18		20		ns
t_{ROH}	RAS high from $\overline{OE}$ low	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	20	45	20	52	20	60	ns
t_{RPC}	$\overline{RAS}$ low to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	$\overline{W}$ low from $\overline{RAS}$ low (RMW)	85		98		110		ns
t_{CPRH}	$\overline{CAS}$ high to $\overline{RAS}$ high	35		40		45		ns
t_{CPW}	$\overline{CAS}$ high to $\overline{W}$	60		68		75		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to assure access time.

ADVANCE INFORMATION

device symbolization (TM497TBM40 illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

TM496TBM40, TM496TBM40S 4 194 304 BY 40-BIT DYNAMIC RAM MODULE
TM892VBM40, TM892VBM40S 8 388 608 BY 40-BIT DYNAMIC RAM MODULE

- **Organization**
  TM496TBM40 . . . 4 194 304 × 40
  TM892VBM40 . . . 8 388 608 × 40
- **Single 5-V Power Supply**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM496TBM40 – Utilizes Ten 16-Megabit Dynamic RAMs In Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM892VBM40 – Utilizes Twenty 16-Megabit Dynamic RAMs In Plastic Small-Outline J-Lead Packages (SOJ)**
- **Long Refresh Period . . . 64 ms (4096 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **Low Power Dissipation**
- **V_{CC} Tolerance ± 10%**

- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'496TBM40-60	60 ns	30 ns	15 ns	110 ns
'496TBM40-70	70 ns	35 ns	18 ns	130 ns
'496TBM40-80	80 ns	40 ns	20 ns	150 ns
'892VBM40-60	60 ns	30 ns	15 ns	110 ns
'892VBM40-70	70 ns	35 ns	18 ns	130 ns
'892VBM40-80	80 ns	40 ns	20 ns	150 ns

- **Operating Free-Air-Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  TM496TBM40
  TM892VBM40
- **Tin-Lead (Solder) Tabbed Versions Available:**
  TM496TBM40S
  TM892VBM40S

ADVANCE INFORMATION

description

TM496TBM40

The TM496TBM40 is a 160M dynamic random-access memory organized as 4M × 40 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of ten TMS416400DZ, 4 194 304 × 4-bit dynamic RAMs, each in a 400-mil 24/28-lead plastic small-outline J-lead (SOJ) package mounted on a substrate together with decoupling capacitors. Each TMS416400DZ is described in the TMS416400 data sheet.

The TM496TBM40 can be used in systems with fewer than 40 data bits. In those applications, it is recommended that any unused DQ pins be connected to either V_{SS} or V_{CC} through a series resistor with a typical value between 5 kΩ and 10 kΩ.

The TM496TBM40 is available in the single-sided BM leadless module for use with sockets.

The TM496TBM40 is rated for operation from 0°C to 70°C. This device features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

TM892VBM40

The TM892VBM40 is a 320M dynamic random-access memory organized as 8M × 40 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of twenty TMS416400DZ, 4 194 304 × 4-bit dynamic RAMs, each in a 400-mil 24/28-lead plastic small-outline J-lead (SOJ) package mounted on a substrate with decoupling capacitors. Each TMS416400DZ is described in the TMS416400 data sheet.

The TM892VBM40 can be used in systems with fewer than 40 data bits. In those applications, it is recommended that any unused DQ pins be connected to either V_{SS} or V_{CC} through a series resistor with a typical value between 5 kΩ and 10 kΩ.

The TM892VBM40 is available in the double-sided BM leadless module for use with sockets.

† Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

The TM892VBM40 is rated for operation from 0°C to 70°C. This device features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

operation

TM496TBM40

The TM496TBM40 operates as ten TMS416400DZs connected as shown in the functional block diagram. Refer to the TMS416400 data sheet for details of operation.

TM892VBM40

The TM892VBM40 operates as twenty TMS416400DZs connected as shown in the functional block diagram. Refer to the TMS416400 data sheet for details of operation.

single in-line memory module and components

PC substrate: 1, 27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Contact area for TM496TBM40 and TM892VBM40: Nickel plate and gold plate over copper
Contact area for TM496TBM40S and TM892VBM40S: Nickel plate and tin-lead over copper

TEXAS INSTRUMENTS
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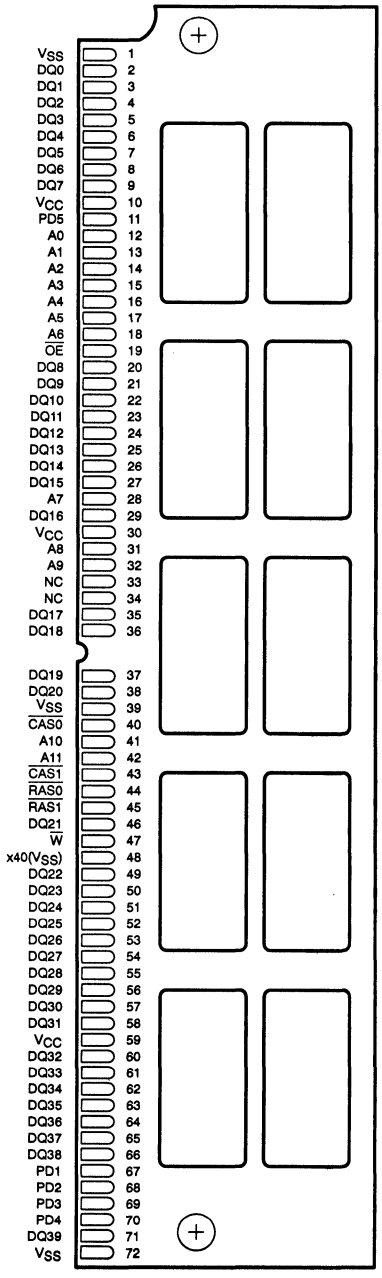
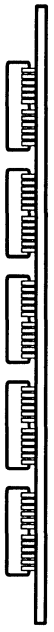
BM SINGLE-IN-LINE PACKAGE†

(TOP VIEW)



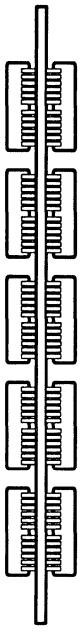
TM496TBM40
BM SINGLE-IN-LINE PACKAGE†

(SIDE VIEW)



TM892VBM40
BM SINGLE-IN-LINE PACKAGE†

(SIDE VIEW)



PIN NOMENCLATURE

A0–A11	Address Inputs
$\overline{CAS0}$, $\overline{CAS1}$	Column-Address Strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row-Address Strobe
DQ0–DQ39	Data In/Data Out
$\overline{W}$	Write Enable
NC	No External Connection
V_{CC}	5-V Supply
V_{SS}	Ground
PD1–PD5	Presence Detects
$\overline{OE}$	Output Enable

PRESENCE DETECT

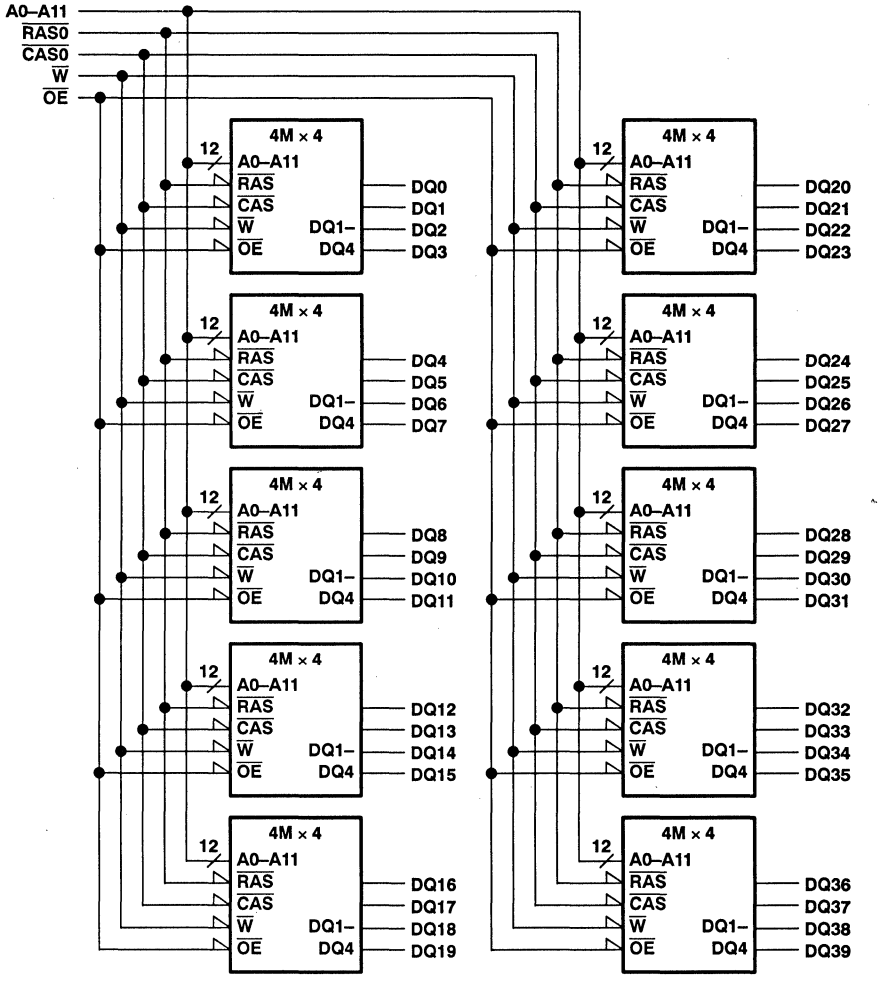
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (68)	PD4 (70)	PD5 (11)
TM496TBM40	80 ns	V_{SS}	NC	NC	V_{SS}	V_{SS}
	70 ns	V_{SS}	NC	V_{SS}	NC	V_{SS}
	60 ns	V_{SS}	NC	NC	NC	V_{SS}
TM892VBM40	80 ns	NC	V_{SS}	NC	V_{SS}	V_{SS}
	70 ns	NC	V_{SS}	V_{SS}	NC	V_{SS}
	60 ns	NC	V_{SS}	NC	NC	V_{SS}

† The packages shown here are for pinout reference only and are not drawn to scale.

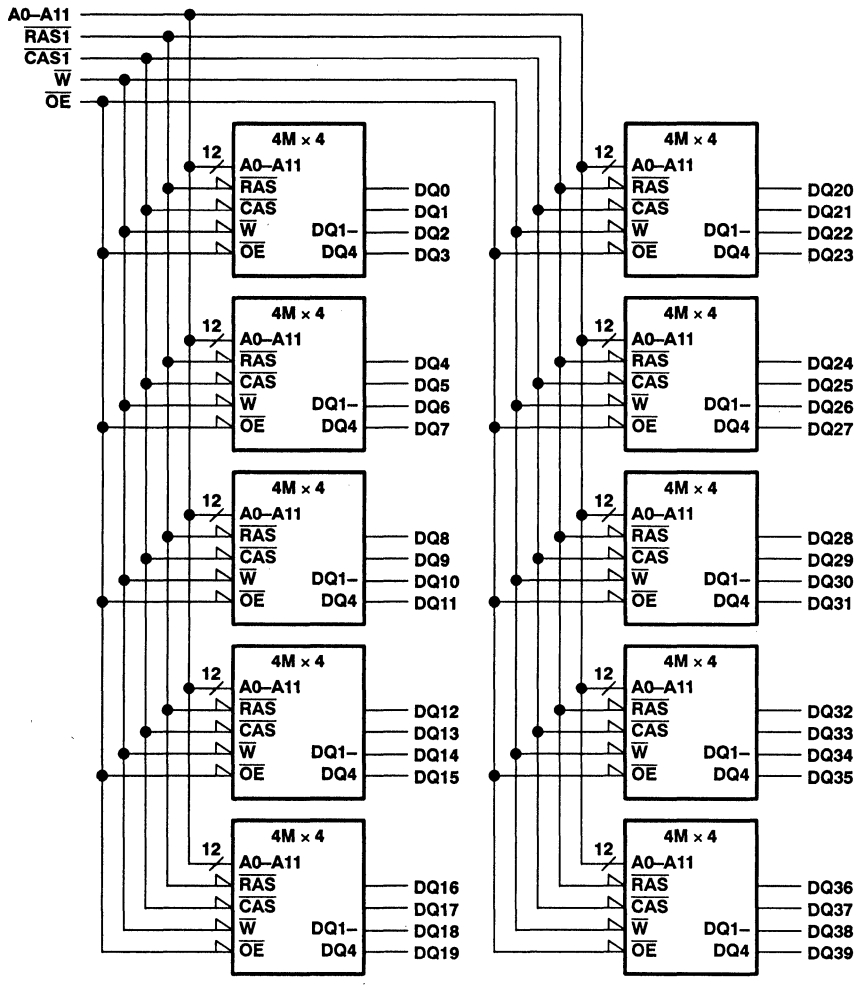
ADVANCE INFORMATION

ADVANCE INFORMATION

functional block diagram (TM496TBM40 and TM892VBM40, side 1)



functional block diagram (TM892VBM40, side 2)



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation (TM496TBM40) ..... 10 W
(TM892VBM40) ..... 20 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

		'496TBM40		'892VBM40		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inuts		50		100	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$ input		70		140	pF
$C_{i(W)}$	Input capacitance, $\overline{WE}$ input		70		140	pF
$C_{i(RC)}$	Input capacitance, $\overline{RAS}$, $\overline{CAS}$ inputs		70		70	pF
$C_{o(DQ)}$	Output capacitance, DQ pins		7		14	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'496TBM40-60		'496TBM40-70		'496TBM40-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 100		± 100		± 100	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 4)	V_{CC} = 5.5 V, Minimum cycle		900		800		700	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		20		20		20	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		10		10		10	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		900		800		700	mA
I_{CC4}	Average page current (see Note 5)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		700		600		500	mA

NOTES: 4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'892VBM40-60		'892VBM40-70		'892VBM40-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 200		± 200		± 200	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write current (One RAS active, see Note 4)	V_{CC} = 5.5 V, Minimum cycle		920		820		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL),		40		40		40	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR), (One $\overline{RAS}$ active see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		920		820		720	mA
I_{CC4}	Average page current (One $\overline{RAS}$ active, see Note 5)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		620		520	mA

NOTES: 4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'496TBM40-60 '892VBM40-60		'496TBM40-70 '892VBM40-70		'496TBM40-80 '892VBM40-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time $\overline{OE}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ low to output	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable $\overline{OE}$	0	15		18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'496TBM40-60 '892VBM40-60		'496TBM40-70 '892VBM40-70		'496TBM40-70 '892VBM40-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time (CAS-before RAS refresh only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns

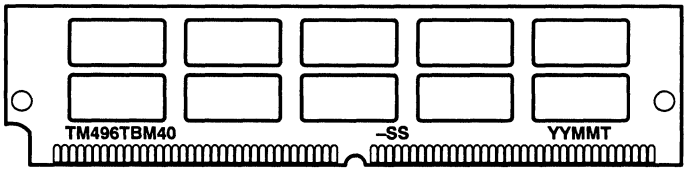
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Reference to the later of $\overline{CAS}$ or $\overline{W}$ in write operation.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		'496TBM40-60 '892VBM40-60		'496TBM40-70 '892VBM40-70		'496TBM40-80 '892VBM40-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	OE to data delay	15		18		20		ns
t_{ROH}	RAS hold time referenced to $\overline{OE}$	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, RAS low to $\overline{W}$ low (Read-write operation only)	85		98		110		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		ns
t_{REF}	Refresh time interval		64		64		64	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to guarantee access time.

device symbolization (TM496TBM40 illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
– SS = Speed Code

NOTE: Location of symbolization may vary.

ADVANCE INFORMATION

TM124TBK40, TM124TBK40S 1 048 576 BY 40-BIT DYNAMIC RAM MODULE
TM248VBK40, TM248VBK40S 2 097 152 BY 40-BIT DYNAMIC RAM MODULE

- **Organization**
  TM124TBK40 . . . 1 048 576 × 40
  TM248VBK40 . . . 2 097 152 × 40
- **Single 5-V Power Supply**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124TBK40 – Utilizes Ten 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248VBK40 – Utilizes Twenty 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJ)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **Low Power Dissipation**
- **V_{CC} Tolerance ± 10%**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124TBK40-60	60 ns	30 ns	15 ns	110 ns
'124TBK40-70	70 ns	35 ns	18 ns	130 ns
'124TBK40-80	80 ns	40 ns	20 ns	150 ns
'248VBK40-60	60 ns	30 ns	15 ns	110 ns
'248VBK40-70	70 ns	35 ns	18 ns	130 ns
'248VBK40-80	80 ns	40 ns	20 ns	150 ns

- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Version Available:†**
  TM124TBK40
  TM248VBK40
- **Tin-Lead (Solder) Tabbed Version Available:**
  TM124TBK40S
  TM248VBK40S

description

TM124TBK40

The TM124TBK40 is a 40M dynamic random-access memory organized as 1 048 576 × 40 in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of ten TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in a 300-mil 20/26-lead plastic small-outline J-lead package (SOJ) mounted on a substrate together with decoupling capacitors. Each TMS44400DJ is described in the TMS44400 data sheet.

The TM124TBK40 can be used in systems with fewer than 40 data bits. In those applications, it is recommended that any unused DQ pins be connected to either V_{SS} or V_{CC} through a series resistor with a typical value between 5 kΩ and 10 kΩ.

The TM124TBK40 is available in the single-sided BK leadless module for use with sockets.

The TM124TBK40 is rated for operation from 0°C to 70°C. This device features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

TM248VBK40

The TM248VBK40 is a 80M dynamic random-access memory organized as 2 097 152 × 40 in a 72-pin single in-line memory module (SIMM). The SIMM is composed of twenty TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in a 300-mil 20/26-lead plastic small-outline J-lead (SOJ) package mounted on a substrate with decoupling capacitors. Each TMS44400DJ is described in the TMS44400 data sheet.

The TM248VBK40 can be used in systems with fewer than 40 data bits. In those applications, it is recommended that any unused DQ pins be connected to either V_{SS} or V_{CC} through a series resistor with a typical value between 5 kΩ and 10 kΩ.

The TM248VTBK40 is available in the double-sided BK leadless module for use with sockets.

The TM248VTBK40 is rated for operation from 0°C to 70°C. This device features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns.

† Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

ADVANCE INFORMATION

operation

TM124TBK40

The TM124TBK40 operates as ten TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation.

TM248VBK40

The TM248VBK40 operates as twenty TMS44400DJs connected as shown in the functional block diagram. Refer to the TMS44400 data sheet for details of operation.

single in-line memory module and components

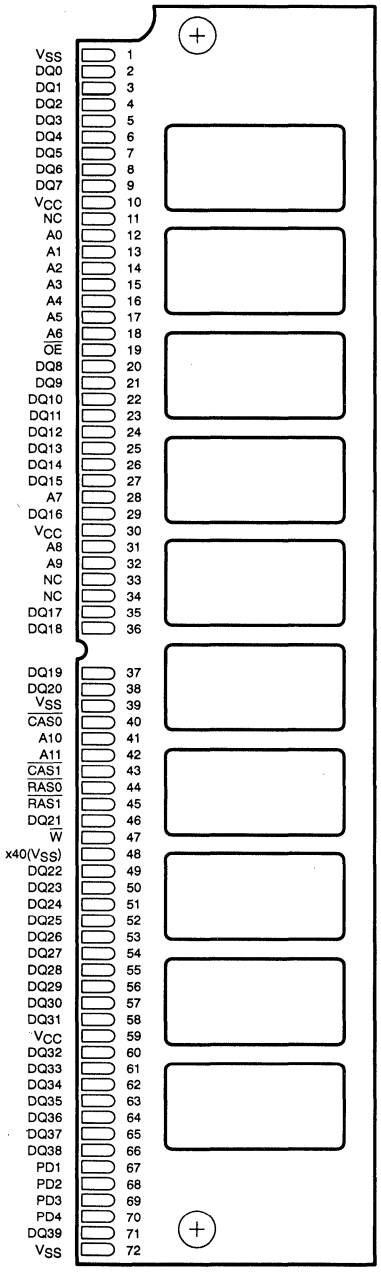
PC substrate: 1, 27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Contact area for TM124TBK40 and TM248VBK40: Nickel plate and gold plate over copper.
Contact area for TM124TBK40S and TM248VBK40S: Nickel plate and tin-lead over copper.

SMMS140–JANUARY 1993

ADVANCE INFORMATION

BK SINGLE-IN-LINE PACKAGE†

(TOP VIEW)

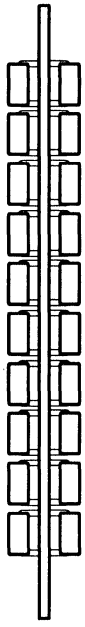


TM124TBK40
BK SINGLE IN-LINE PACKAGE†

(SIDE VIEW)

TM248VBK40
BK SINGLE IN-LINE PACKAGE†

(SIDE VIEW)



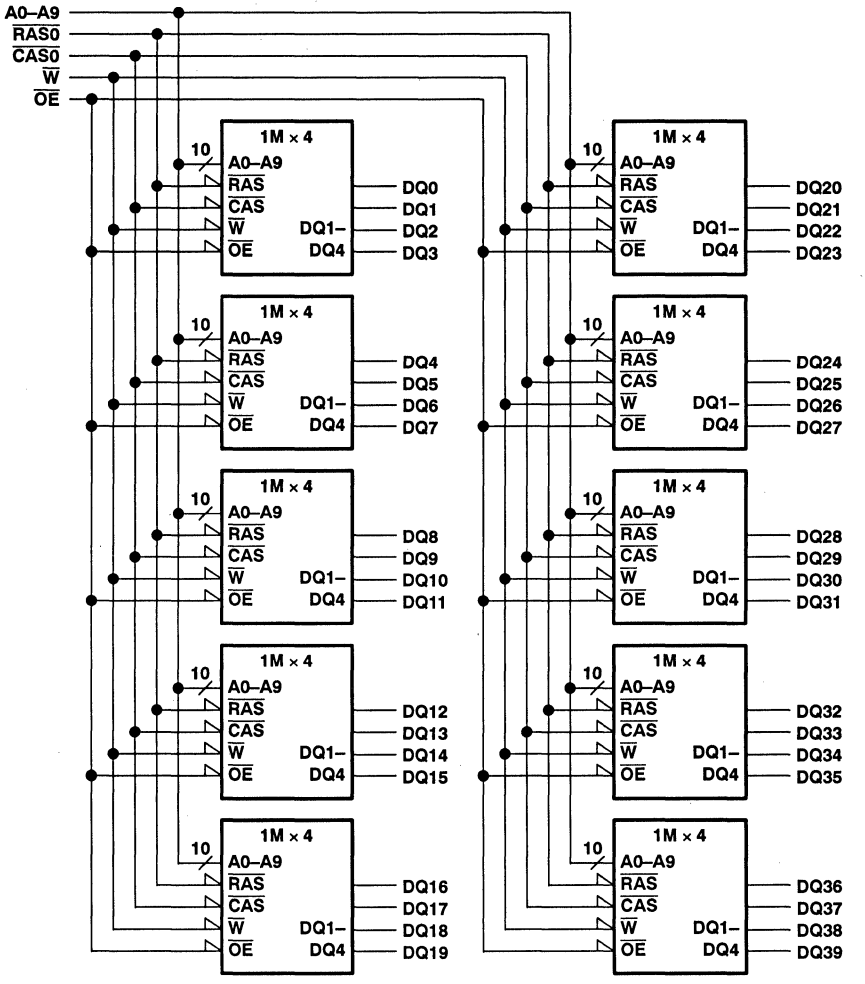
PIN NOMENCLATURE	
A0–A9	Address Inputs
A10, A11	NC – Reserved for 4M/8M × 40
$\overline{CAS0}$, $\overline{CAS1}$	Column-Address Strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row-Address Strobe
DQ0–DQ39	Data In/Data Out
$\overline{W}$	Write Enable
NC	No External Connection
V_{CC}	5-V Supply
V_{SS}	Ground
PD1–PD4	Presence Detects
$\overline{OE}$	Output Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124TBK40	80 ns	V_{SS}	V_{SS}	V_{SS}	V_{SS}
	70 ns	V_{SS}	V_{SS}	NC	V_{SS}
	60 ns	V_{SS}	V_{SS}	V_{SS}	NC
TM248VBK40	80 ns	NC	NC	V_{SS}	V_{SS}
	70 ns	NC	NC	NC	V_{SS}
	60 ns	NC	NC	V_{SS}	NC

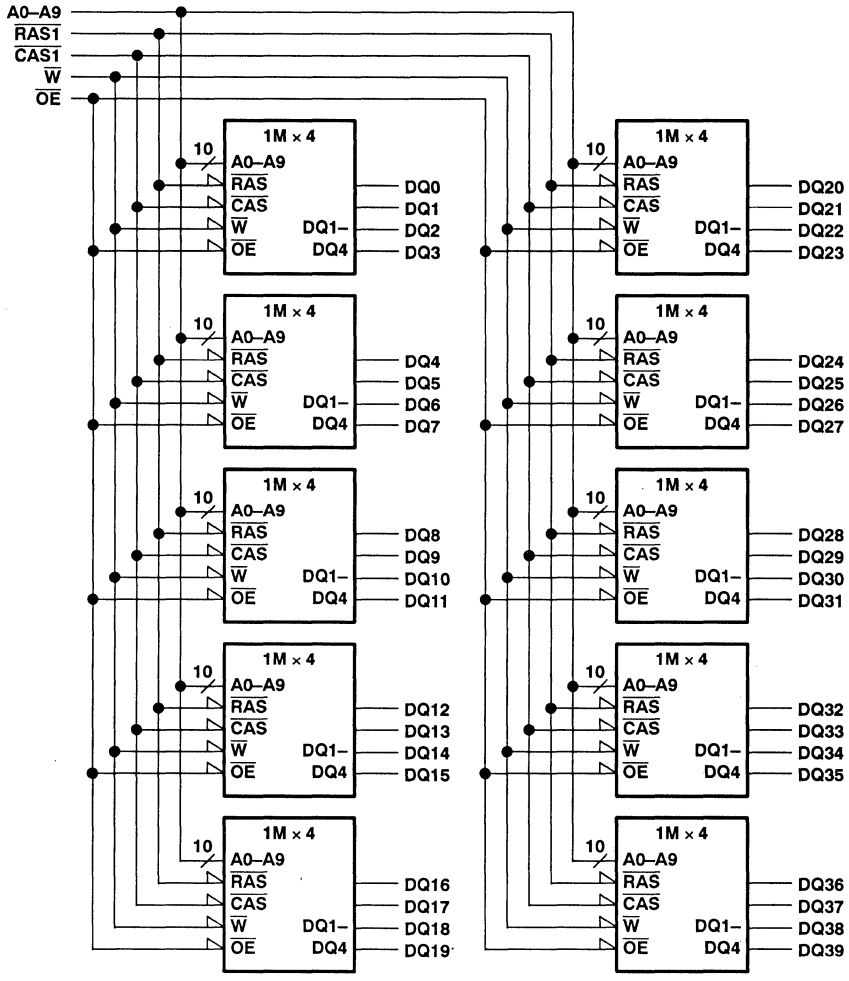
† The packages shown here are for pinout reference only and are not drawn to scale.

ADVANCE INFORMATION

functional block diagram (TM124TBK40 and TM248VBK40, side 1)



functional block diagram (TM248VBK40, side 2)



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation (TM124TBK40) ..... 10 W
(TM248VBK40) ..... 20 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

		'124TBK40		'248VBK40		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inuts		50		100	pF
$C_{i(\overline{OE})}$	Input capacitance, $\overline{OE}$ input		70		140	pF
$C_{i(\overline{W})}$	Input capacitance, $\overline{WE}$ input		70		140	pF
$C_{i(RC)}$	Input capacitance, $\overline{RAS}$, $\overline{CAS}$ inputs		70		70	pF
$C_{o(DQ)}$	Output capacitance, DQ pins		7		14	pF

NOTE 3: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124TBK40-60		'124TBK40-70		'124TBK40-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 100		± 100		± 100	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 4)	V_{CC} = 5.5 V, Minimum cycle		1050		900		800	mA
I_{CC2}	Standby current	After 1 memory cycle, RAS and CAS high, V_{IH} = 2.4 V (TTL)		20		20		20	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		10		10		10	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1050		900		800	mA
I_{CC4}	Average page current (see Note 5)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		900		800		700	mA

NOTES: 4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248VBK40-60		'248VBK40-70		'248VBK40-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 200		± 200		± 200	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write current (One RAS active, see Note 4)	V_{CC} = 5.5 V, Minimum cycle		1070		920		820	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		40		40		40	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR), (One $\overline{RAS}$ active see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1070		920		820	mA
I_{CC4}	Average page current (One $\overline{RAS}$ active, see Note 5)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		920		820		720	mA

NOTES: 4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

ADVANCE INFORMATION

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124TBK40-60 '248VBK40-60		'124TBK40-70 '248VBK40-70		'124TBK40-80 '248VBK40-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column-address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time $\overline{OE}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable $\overline{OE}$	0	15		18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124TBK40-60 '248VBK40-60		'124TBK40-70 '248VBK40-70		'124TBK40-70 '248VBK40-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-write cycle	155		181		205		ns
t_{PC}	Page-mode read or write (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-write	85		96		105		ns
t_{CP}	$\overline{CAS}$ high pulse duration	10		10		10		ns
t_{CAS}	$\overline{CAS}$ low pulse duration (see Note 9)	15	10 000	18	10 000	20	10 000	ns
t_{RP}	$\overline{RAS}$ high pulse duration	40		50		60		ns
t_{RAS}	$\overline{RAS}$ low pulse duration (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{RASP}	$\overline{RAS}$ low pulse width, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{WP}	$\overline{W}$ low pulse duration	15		15		15		ns
t_{ASC}	Column-address setup	0		0		0		ns
t_{ASR}	Row-address setup	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WCS}	$\overline{W}$ low before $\overline{CAS}$ low (early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ setup (CBR refresh)	10		10		10		ns
t_{CWL}	$\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{CAH}	Column address hold time	10		15		15		ns
t_{RAH}	Row-address hold time	10		10		10		ns
t_{AR}	Column-address hold time from $\overline{RAS}$ (see Note 12)	50		55		60		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.

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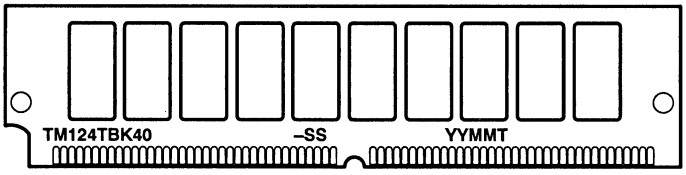
timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		'124TBK40-60 '248VBK40-60		'124TBK40-70 '248VBK40-70		'124TBK40-80 '248VBK40-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{DHR}	Data hold time from $\overline{RAS}$ (see Note 12)	50		55		60		ns
t_{RCH}	Read hold time from $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Read hold time from $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Write hold time from $\overline{CAS}$ low (early write operation only)	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{OEH}	$\overline{OE}$ hold time	15		18		20		ns
t_{CSH}	$\overline{CAS}$ high from $\overline{RAS}$ low	60		70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{CWD}	$\overline{W}$ low from $\overline{CAS}$ low (RMW)	40		46		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RWD}	$\overline{W}$ low from $\overline{RAS}$ low (RMW)	85		98		110		ns
t_{AWD}	$\overline{W}$ low from column address (RMW)	55		63		70		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		ns
t_{ROH}	$\overline{RAS}$ high from $\overline{OE}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ high from $\overline{RAS}$ (CBR)	15		15		20		ns
t_{CSR}	$\overline{RAS}$ low from $\overline{CAS}$ (CBR)	10		10		10		ns
t_{RPC}	$\overline{RAS}$ low to $\overline{CAS}$ low	0		0		0		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. The maximum value is specified only to assure access time.

ADVANCE INFORMATION

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

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TMS27LV010A	1 048 576-bit	(128K × 8) Low Voltage EPROM/OTP PROM	6-203

The following EPROM and OTP PROM devices are also available from Texas Instruments. Contact your local TI Field Sales Office for more information.

TMS27C128	131 072-bit	(16K × 8) CMOS EPROM
TMS27PC128	131 072-bit	(16K × 8) CMOS OTP PROM

TMS27C256 262 144-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC256 262 144-BIT PROGRAMMABLE READ-ONLY MEMORY

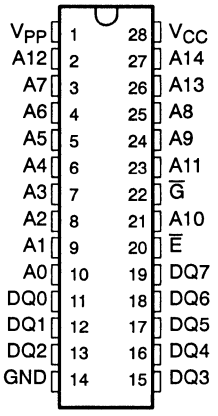
This Data Sheet is Applicable to All TMS27C256s and TMS27PC256s Symbolized with Code "B" as Described on Page 11.

- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 256K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

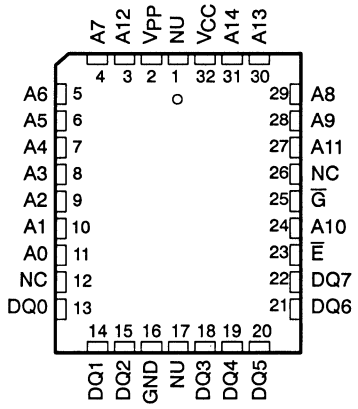
V_{CC} ± 10%	
'27C/PC256-10	100 ns
'27C/PC256-12	120 ns
'27C/PC256-15	150 ns
'27C/PC256-17	170 ns
'27C/PC256-20	200 ns
'27C/PC256-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**
- **256K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C256)**

J AND N PACKAGES†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A14	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
V_{PP}	13-V Programming Power Supply

description

The TMS27C256 series are 262 144-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC256 series are 262 144-bit, one-time electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C256 and the TMS27PC256 are pin compatible with 28-pin 256K MOS ROMs, PROMs, and EPROMs.

The TMS27C256 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 OTP PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC256 OTP PROM is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix).

The TMS27C256 and TMS27PC256 are offered with two choices of temperature ranges of 0°C to 70°C (JL, NL, and FML suffixes) and – 40°C to 85°C (JE, NE, and FME suffixes). The TMS27C256 and the TMS27PC256 are also offered with 168-hour burn-in on both temperature ranges (JL4, FML4, JE4, and FME4 suffixes); see table below.

All package styles conform to JEDEC standards.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C256-XXX	JL	JE	JL4	JE4
TMS27PC256-XXX	NL	NE	NL4	NE4
TMS27PC256-XXX	FML	FME	FML4	FME4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming . All programming signals are TTL level. These devices are programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	04

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C256s or TMS27PC256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS27C256 and TMS27PC256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL or CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C256)

Before programming, the TMS27C256 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C256, the window should be covered with an opaque label.

initializing (TMS27PC256)

The one-time programmable TMS27PC256 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The 256K EPROM and OTP PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code, which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 04.

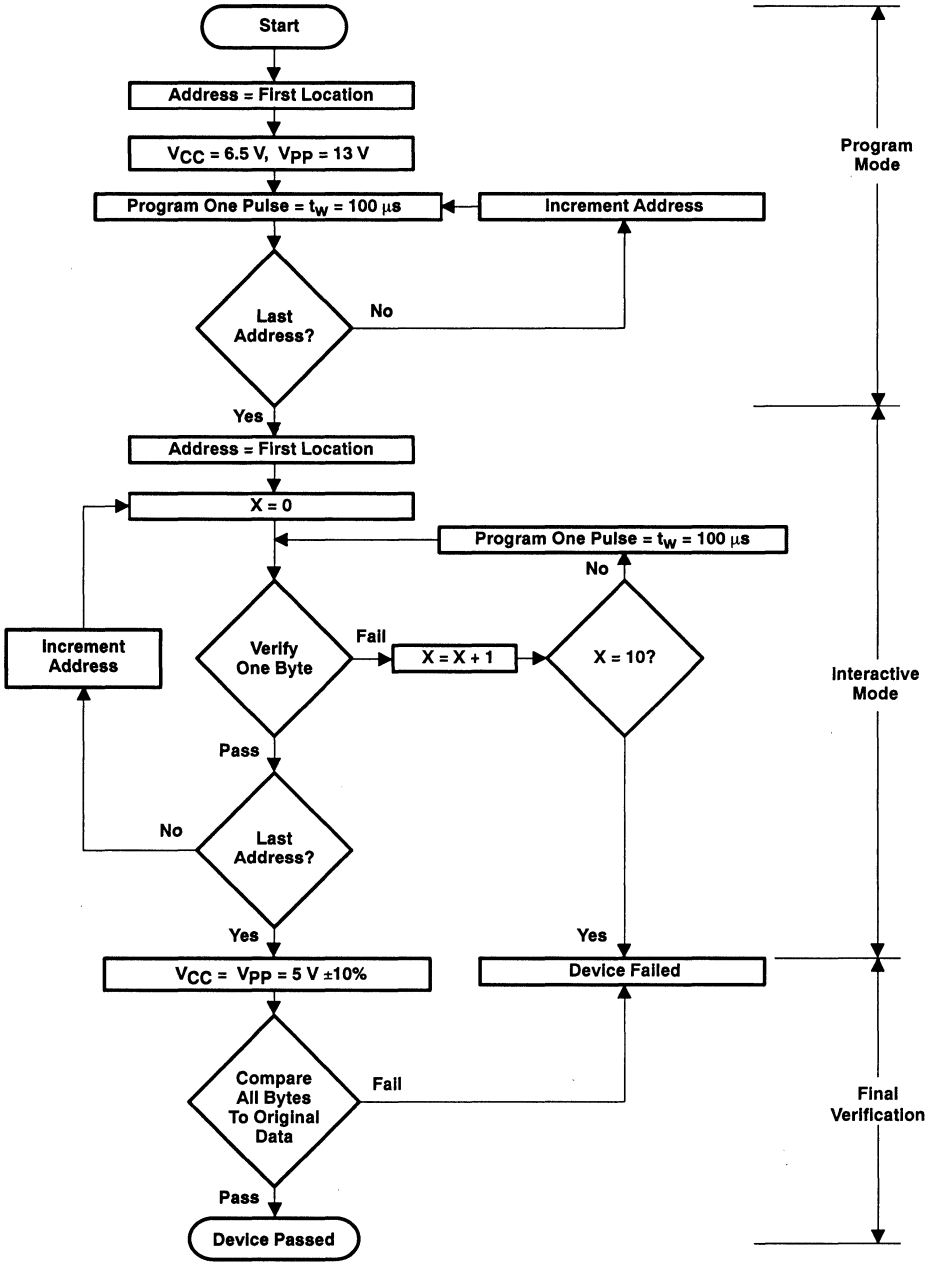
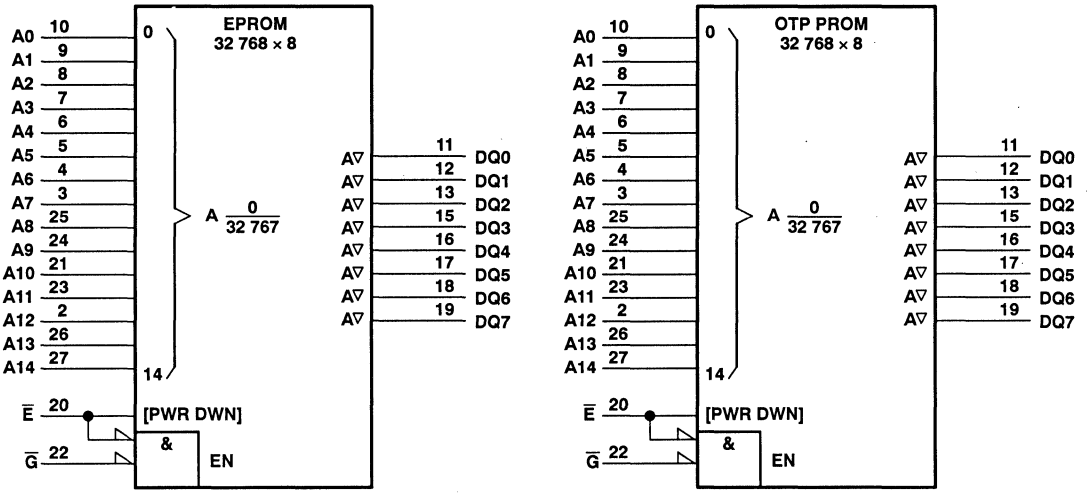


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C256-_ _JL and JL4, '27PC256-_ _NL, NL4, FML, and FML4) ..... 0° C to 70°C
Operating free-air temperature range ('27C256-_ _JE and JE4, '27PC256-_ _NE, NE4, FME, and FME4) ..... − 40° C to 85°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	−0.5		0.2	
T_A	Operating free-air temperature	'27C256-_ _JL, JL4 '27PC256-_ _NL, NL4, FML, FML4	0		70	°C
T_A	Operating free-air temperature	'27C256-_ _JE, JE4 '27PC256-_ _NE, NE4, FME, FME4	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level dc output voltage		$I_{OH} = -2.5$ mA	3.5			V
			$I_{OH} = -20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level dc output voltage		$I_{OL} = 2.1$ mA			0.4	V
			$I_{OL} = 20$ µA			0.1	
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		250	500	µA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	250	
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at $T_A = 25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	10	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		10	14	pF

†Typical values are at $T_A = 25°C$ and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C256-10 '27PC256-10		'27C256-12 '27PC256-12		'27C256-15 '27PC256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C256-17 '27PC256-17		'27C256-20 '27PC256-20		'27C256-25 '27PC256-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.50 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (Reference page 9.)
4. Common test conditions apply for the t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 3)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	95	100	105	µs
$t_{su(A)}$	Address setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (Reference page 9.)

PARAMETER MEASUREMENT INFORMATION

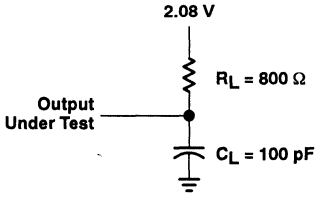
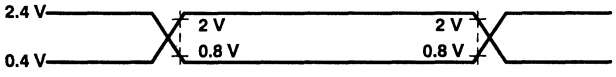


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

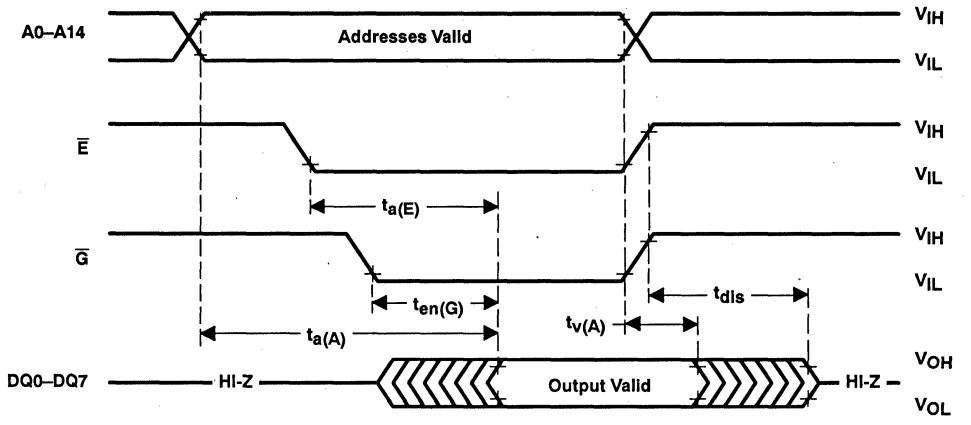
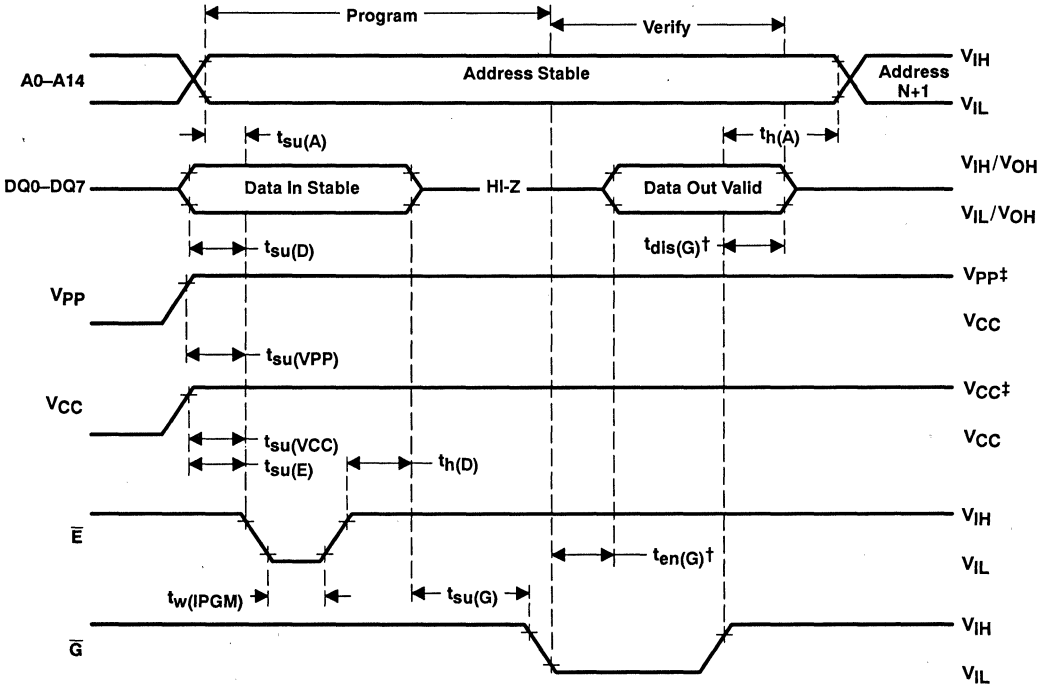


Figure 3. Read Cycle Timing

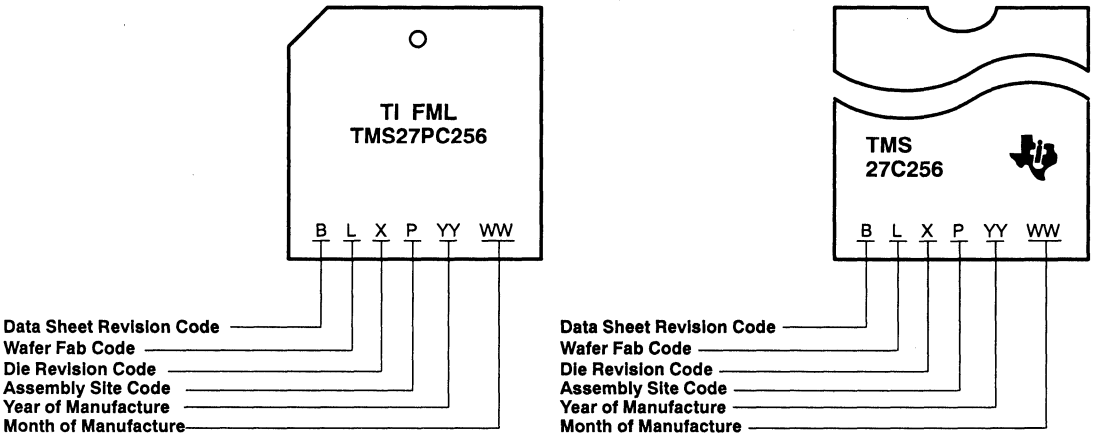


† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

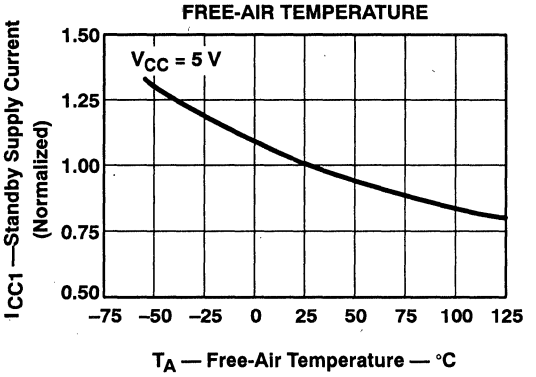
device symbolization

This data sheet is applicable to all TI TMS27C256 CMOS EPROMs and TMS27PC256 CMOS OTP PROMs with the data sheet revision code "B" as shown below.

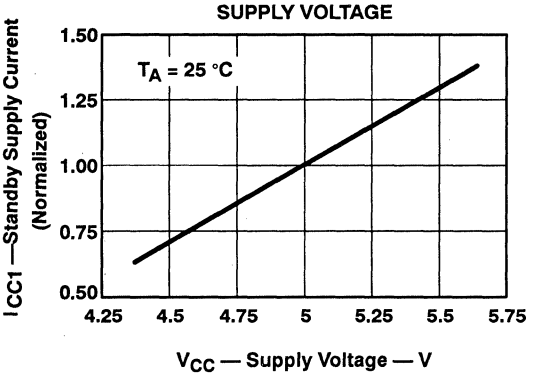


TYPICAL TMS27C/PC256 CHARACTERISTICS

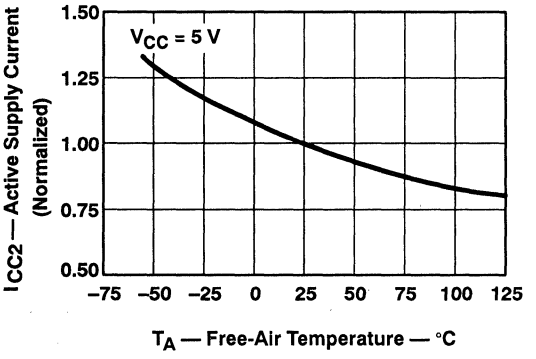
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



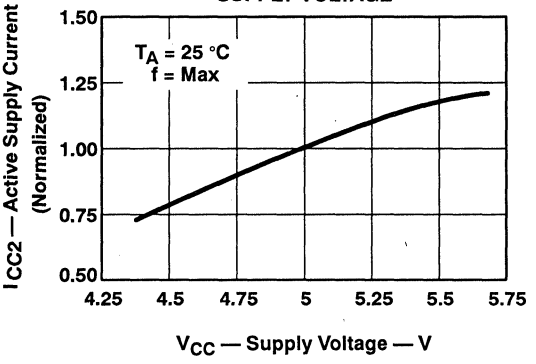
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



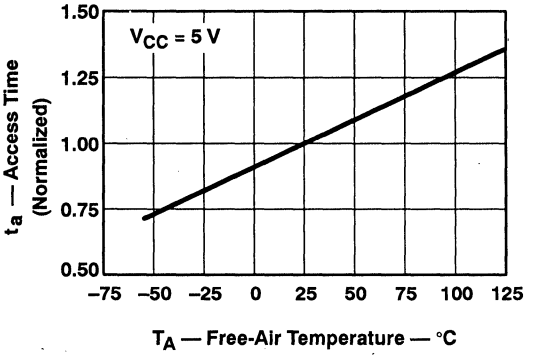
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



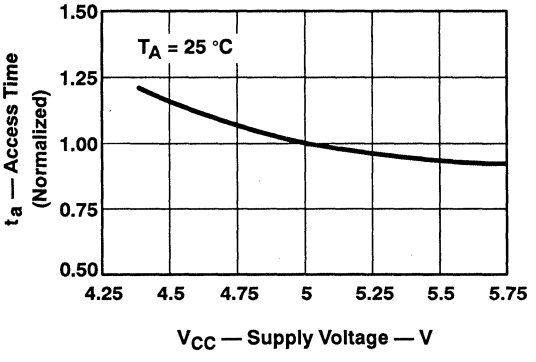
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



TMS27C510 524 288-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC510 524 288-BIT PROGRAMMABLE READ-ONLY MEMORY

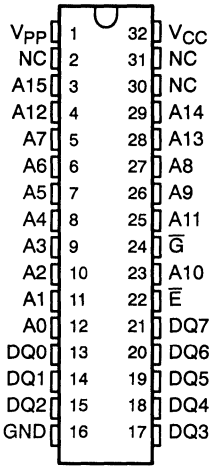
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 1 Meg MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

  V_{CC} ± 10%

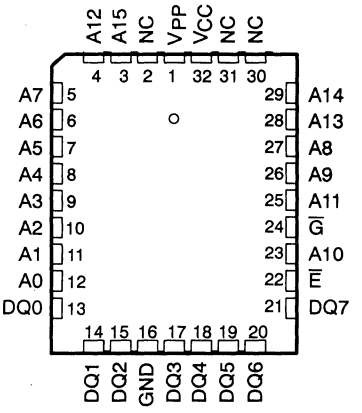
'27C510-12	120 ns
'27C/PC510-15	150 ns
'27C/PC510-17	170 ns
'27C/PC510-20	200 ns
'27C/PC510-25	250 ns

- **Power Saving CMOS Technology**
- **Very High Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-In, and Choices of Operating Temperature Range**
- **512K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C510)**

J AND N PACKAGES†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† Packages shown are for pinout reference only.

description

The TMS27C510 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC510 series are 524 288-bit, one-time electrically programmable read-only memories.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Programming Power Supply

These devices are fabricated using power saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C510 and the TMS27PC510 are pin compatible with 32-pin 1-megabit MOS ROMs, PROMs, and EPROMs.

The TMS27C510 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C510 is available with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C510 is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC510 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC510 is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC510 is specified for operation from 0°C to 70°C, and – 40°C to 85°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C510-XXX	JL	JE	JL4	JE4
TMS27PC510-XXX	NL, FML	NE, FME	—	NE4, FME4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. These devices are programmable by a SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation are in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13.0 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H	V_H
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	15

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C510s or TMS27PC510s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 to DQ7.

latchup immunity

Latchup immunity on the TMS27C510 and TMS27PC510 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

powerdown

Active I_{CC} current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C510)

Before programming, the TMS27C510 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 15 watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C510, the window should be covered with an opaque label. After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light.

initializing (TMS27PC510)

The one-time programmable TMS27PC510 PROM is provided with all bits in logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart of Figure 1, which can reduce programming time to a nominal of 7 seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 13.0 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., $A0 = V_{IL}$ accesses the manufacturer code which is output on DQ0–DQ7; $A0 = V_{IH}$ accesses the device code which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 15.

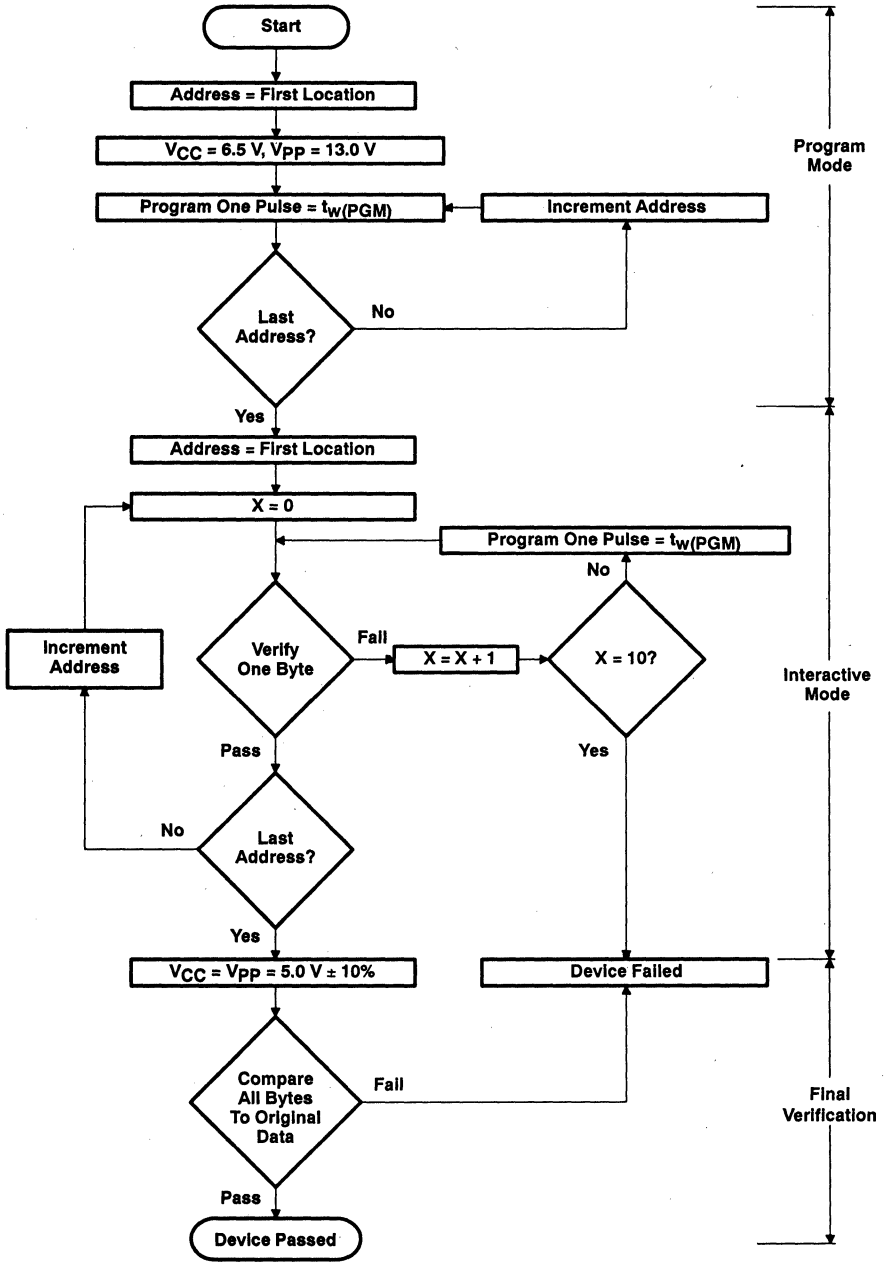
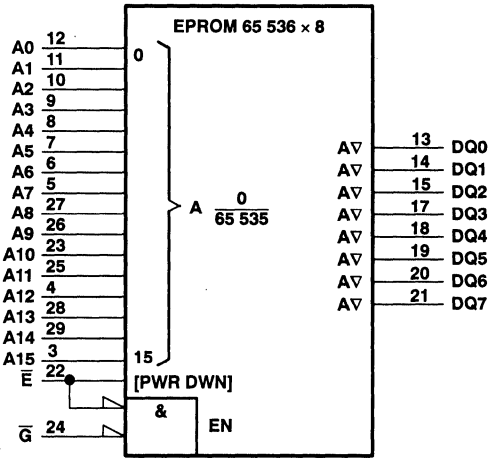
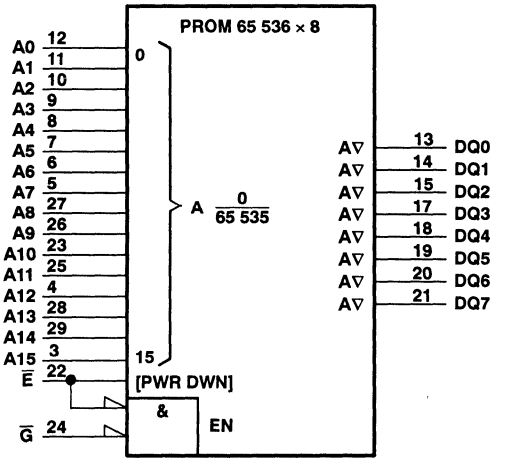


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C510-_ _ JL and JL4;
'27PC510-_ _ NL, FML, NE, and FME) ..... 0°C to 70°C
Operating free-air temperature range ('27C510-_ _ JE, JE4, NE4, and FME4) ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	−0.5		0.2	
T_A	Operating free-air temperature (see Table, page 2)		(see Table, page 2)			°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH}=-2.5$ mA	3.5			V
			$I_{OH}=-20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL}=2.1$ mA			0.4	V
			$I_{OL}=20$ µA			0.1	
I_I	Input current (leakage)		$V_I=0$ to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O=0$ to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{IH}$		250	500	µA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	250	
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at $T_A=25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I=0$, f = 1 MHz		6	10	pF
C_o	Output capacitance	$V_O=0$, f = 1 MHz		10	14	pF

† Typical values are at $T_A=25°C$ and nominal voltages.
‡ Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C510-12		'27C510-15 '27PC510-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		120		150	ns
$t_{a(E)}$	Access time from chip enable			120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C510-17 '27PC510-17		'27C510-20 '27PC510-20		'27C510-25 '27PC510-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming, V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic 1 and 0.8 V for logic 0. (Reference page 8.)
4. Common test conditions apply for the t_{dis} except during programming.

PARAMETER MEASUREMENT INFORMATION

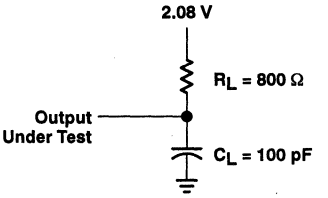
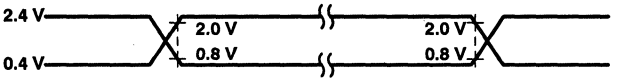


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

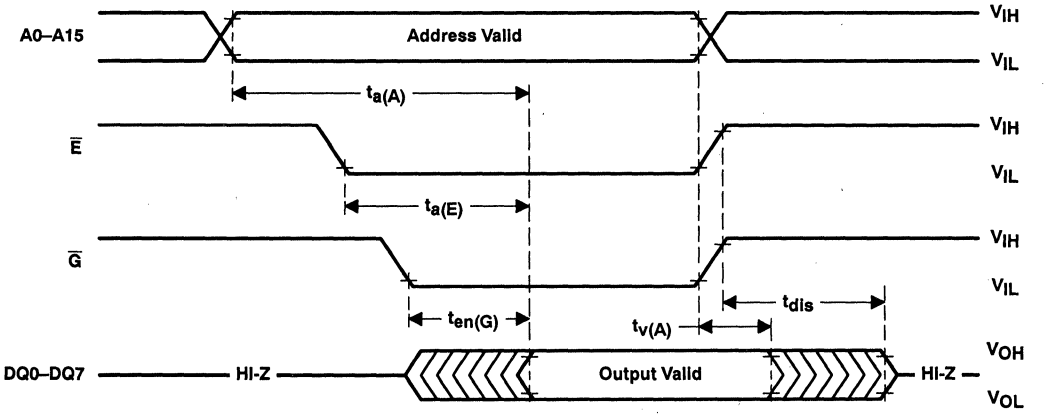
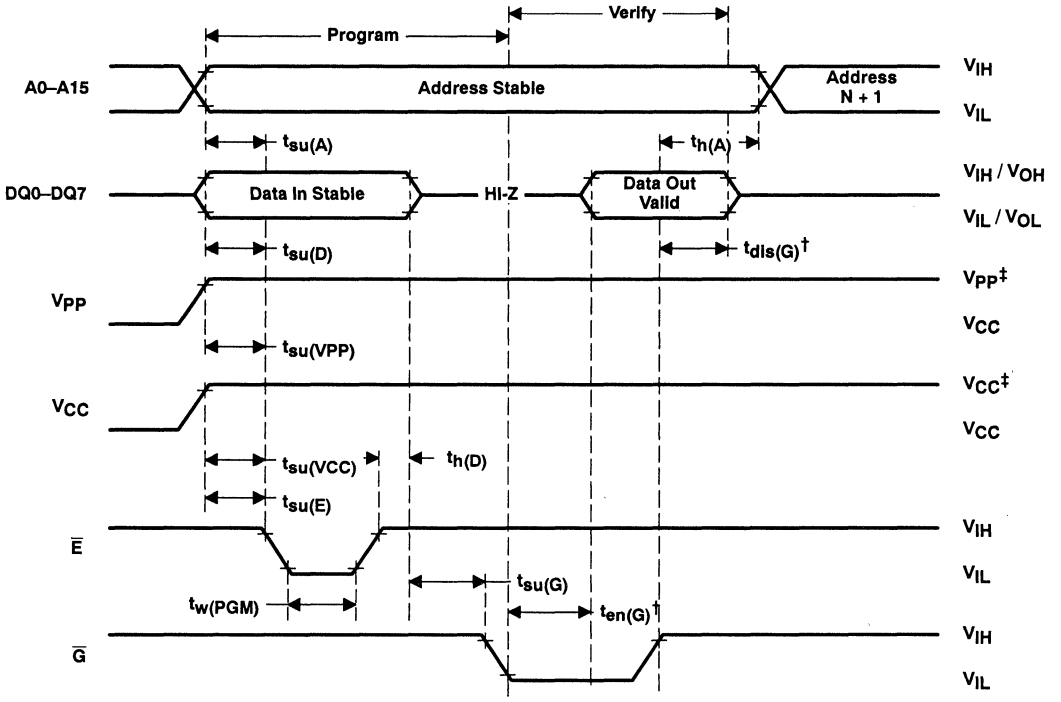


Figure 3. Read Cycle Timing

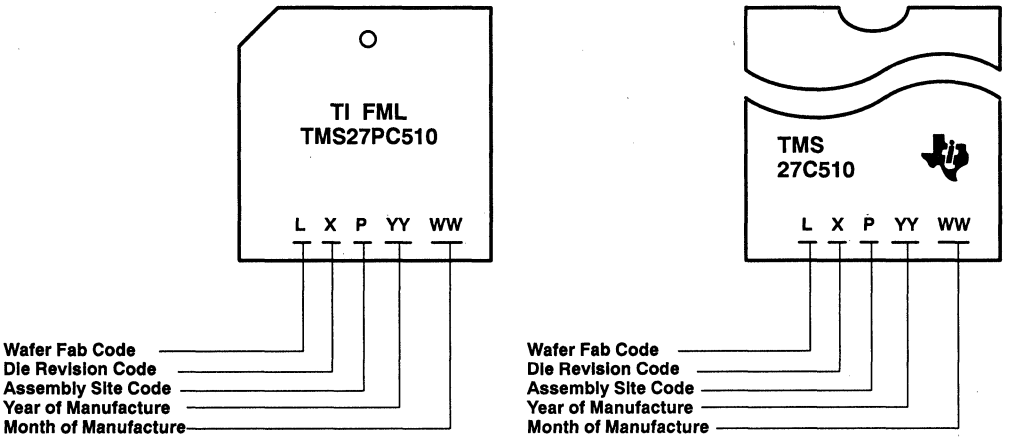
PARAMETER MEASUREMENT INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13.0-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

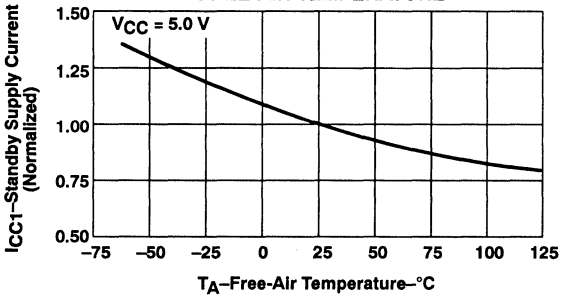
Figure 4. Program Cycle Timing

device symbolization

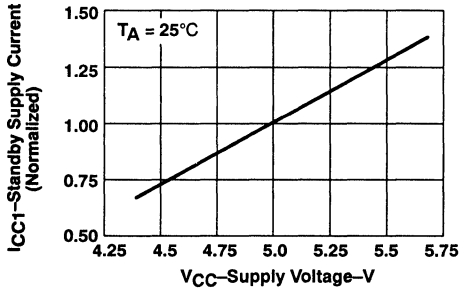


TYPICAL TMS27C/P0C510 CHARACTERISTICS

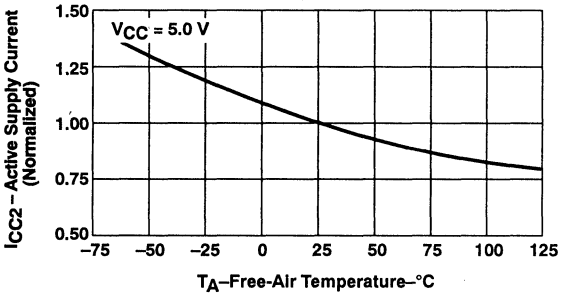
STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE



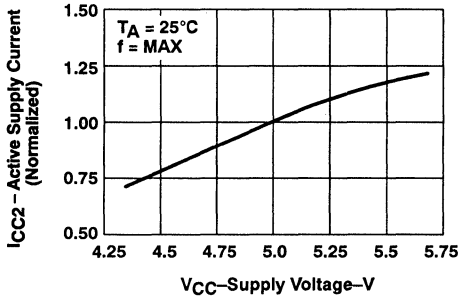
STANDBY SUPPLY CURRENT vs SUPPLY VOLTAGE



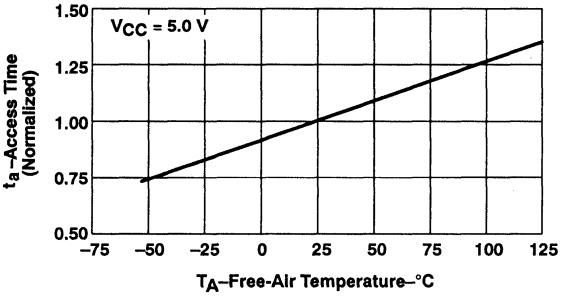
ACTIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE



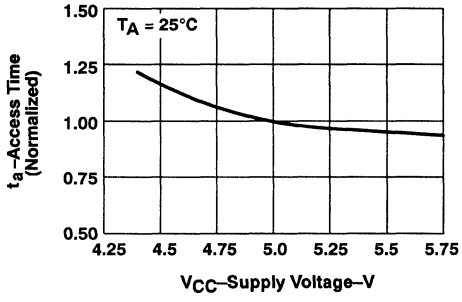
ACTIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



ACCESS TIME vs FREE-AIR TEMPERATURE



ACCESS TIME vs SUPPLY VOLTAGE



TMS27C512 524 288-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC512 524 288-BIT PROGRAMMABLE READ-ONLY MEMORY

This Data Sheet is Applicable to All TMS27C512s and TMS27PC512s Symbolized with Code "B" as Described on Page 12.

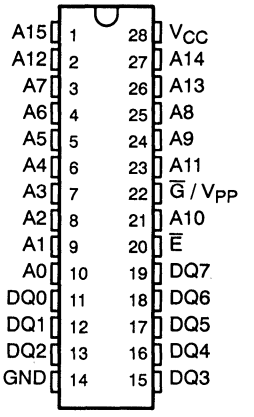
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 512K MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

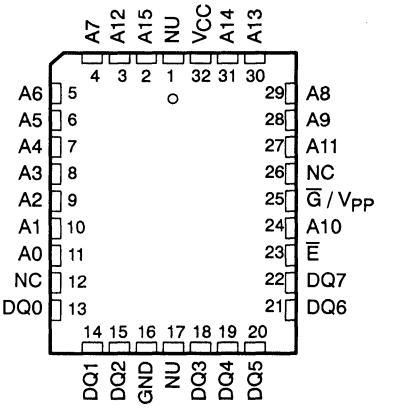
'27C/PC512-10	100 ns
'27C/PC512-12	120 ns
'27C/PC512-15	150 ns
'27C/PC512-20	200 ns
'27C/PC512-25	250 ns

- **Power Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **Active . . . 158 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-in, and Choices of Operating Temperature Ranges**
- **512K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C512)**

J AND N PACKAGES†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† The packages are shown for pinout reference only.

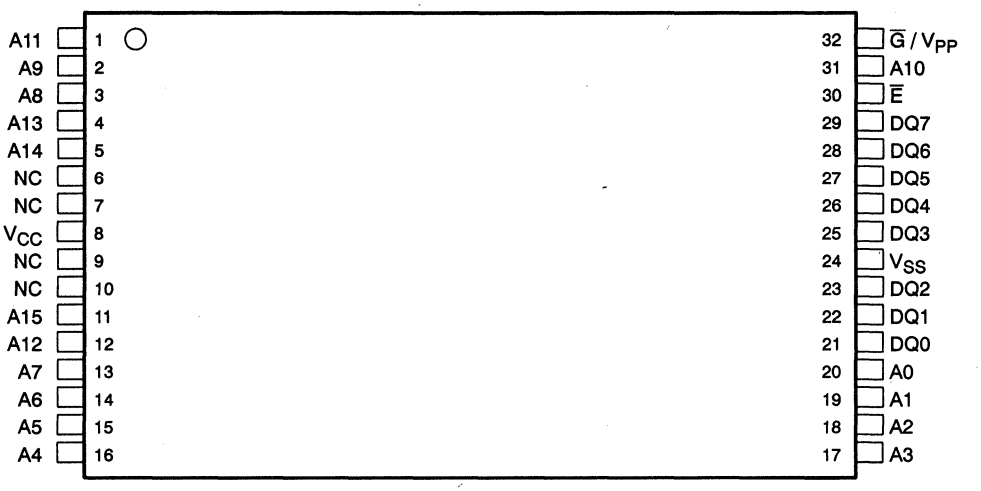
description

The TMS27C512 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

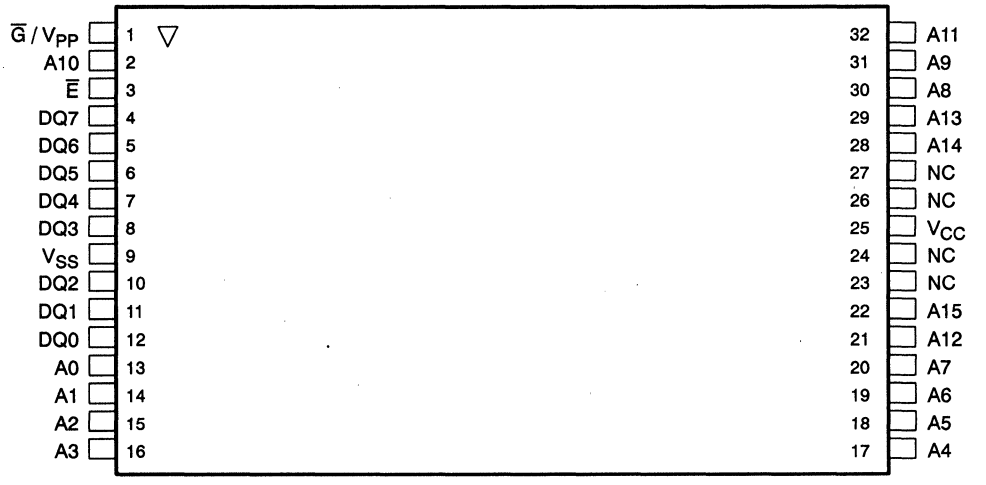
The TMS27PC512 series are 524 288-bit, one-time electrically programmable read-only memories.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$ / V_{PP}	13-V Programming Power Supply
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
DQ0–DQ7	Inputs (Programming) / Outputs
V_{CC}	5-V Power Supply

TMS27PC512†
DD PACKAGE
(TOP VIEW)



TMS27PC512†
DU PACKAGE
REVERSE PINOUT
(TOP VIEW)



† The packages shown are for pinout reference only.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C512 and the TMS27PC512 are pin compatible with 28-pin 512K MOS ROMs, PROMs, and EPROMs.

The TMS27C512 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is also supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), and in a 32-lead thin small-outline package (DD and DU suffixes).

The TMS27C512 and TMS27PC512 are offered with two choices of temperature ranges of 0°C to 70°C (JL, NL, FML, and DDL suffixes) and – 40°C to 85°C (JE, NE, FME, and DDE suffixes). The TMS27C512 and TMS27PC512 are also offered with a 168-hour burn-in on both temperature ranges (JL4, NL4, FML4, DDL4, JE4, NE4, FME4, and DDE4 suffixes); see table below.

All package styles conform to JEDEC standards.

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C512-xxx	JL	JE	JL4	JE4
TMS27PC512-xxx	NL	NE	NL4	NE4
TMS27PC512-xxx	FML	FME	FML4	FME4
TMS27PC512-xxx	DDL	DDE	DDL4	DDE4
TMS27PC512-xxx	DUL	DUE	DUL4	DUE4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. The device is programmed using TI's SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ / V_{PP}	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	85

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C512s or TMS27PC512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ / V_{PP} pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS27C512 and TMS27PC512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL / CMOS signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C512)

Before programming, the TMS27C512 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C512, the window should be covered with an opaque label.

initializing (TMS27PC512)

The one-time programmable TMS27PC512 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and OTP PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of seven seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{G}$ / V_{PP} = 13 V, V_{CC} = 6.5 V, and $\overline{E}$ = V_{IL}. Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5 V, $\overline{G}$ / V_{PP} = V_{IL}, and $\overline{E}$ = V_{IL}.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified when $\overline{G}$ / V_{PP} and $\overline{E}$ = V_{IL}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code, which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 85.

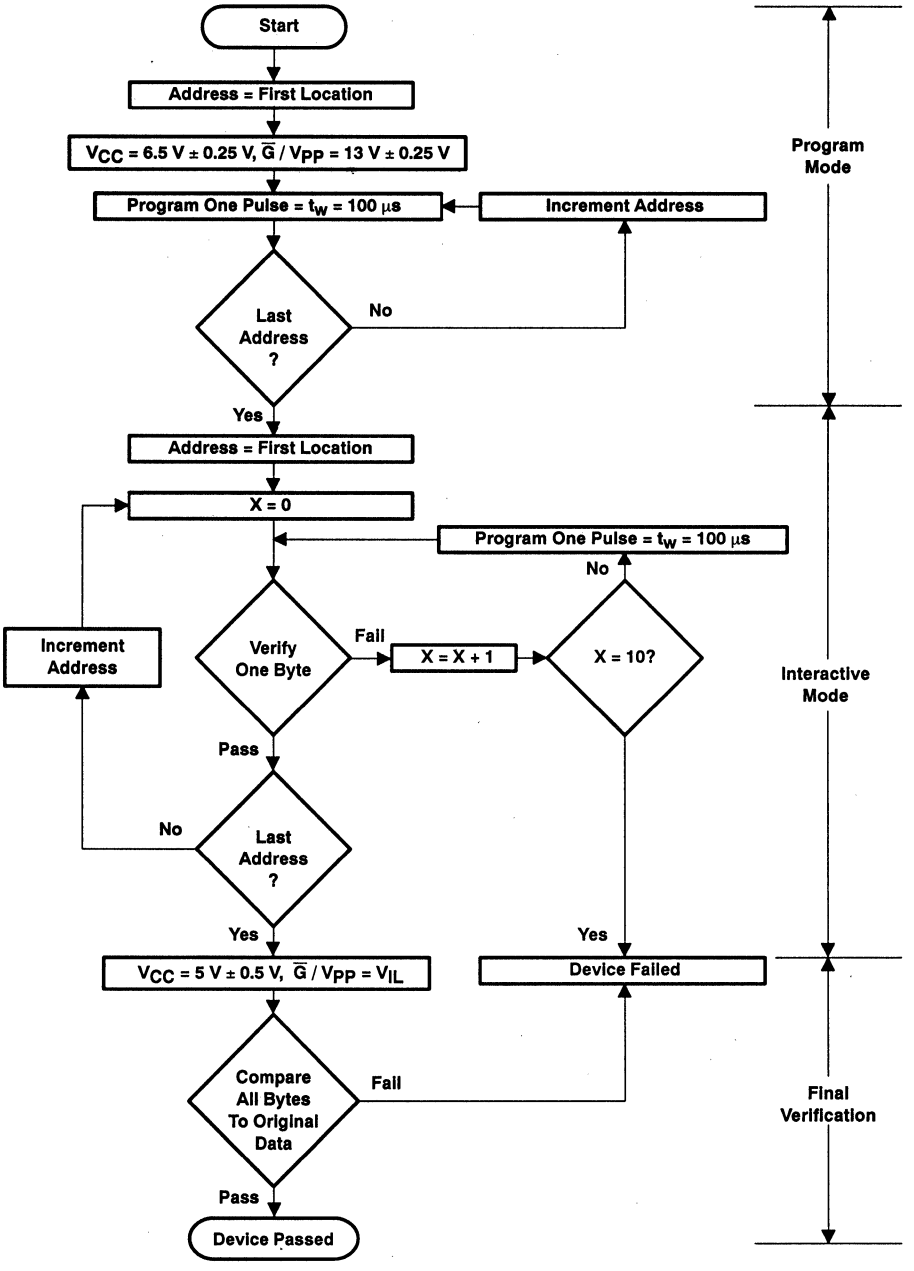
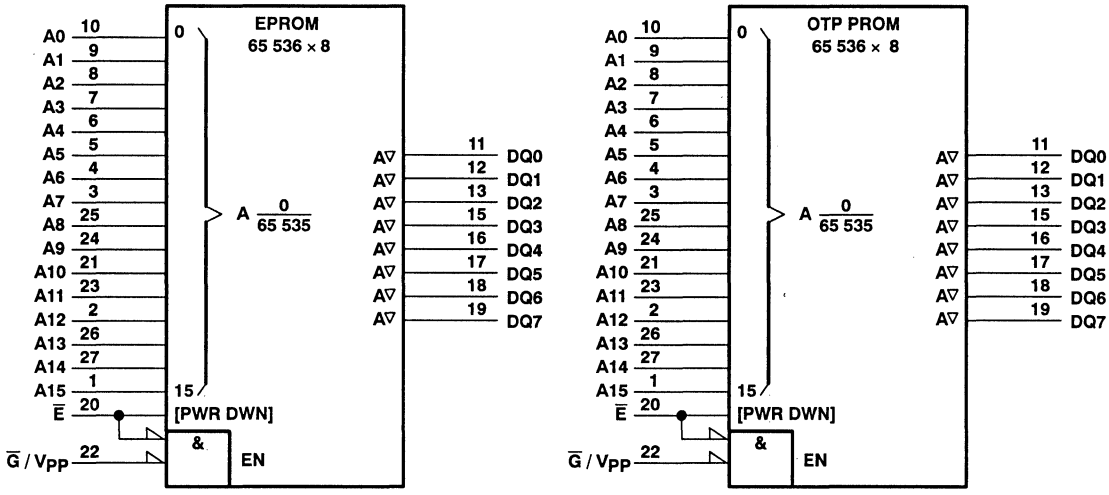


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C512-_ _JL and JL4, '27PC512-_ _NL and NL4, FML and FML4, DDL and DDL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C512-_ _JE and JE4, '27PC512-_ _NE and NE4, FME and FME4, DDE and DDE4) ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
$\overline{G}$ / V_{PP}	Supply voltage	SNAP! Pulse programming algorithm	12.75	13	13.25	V
V_{IH}	High-level dc input voltage	TTL	2		V_{CC}+1	V
		CMOS	V_{CC} – 0.2		V_{CC}+1	
V_{IL}	Low-level dc input voltage	TTL	– 0.5		0.8	V
		CMOS	– 0.5		0.2	
T_A	Operating free-air temperature	TMS27C512-_ _JL, JL4 TMS27PC512-_ _NL, NL4, FML, FML4, DDL, DDL4	0		70	°C
T_A	Operating free-air temperature	TMS27C512-_ _JE, JE4 TMS27PC512-_ _NE, NE4, FME, FME4, DDE, DDE4	– 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as $\overline{G}$ / V_{PP} and removed after or at the same time as $\overline{G}$ / V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = – 2.5 mA	3.5			V
			I_{OH} = – 20 µA	V_{CC} – 0.1			
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 µA			0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	µA
I_{PP}	$\overline{G}$ / V_{PP} supply current (during program pulse)		$\overline{G}$ / V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		250	500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF
$C_{G\,/\,VPP}$	$\overline{G}$ / V_{PP} input capacitance	$\overline{G}$ / V_{PP} = 0, f = 1 MHz		20	25	pF

† Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	TMS27C/PC512-10		TMS27C/PC512-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		100		120	ns
$t_{a(E)}$	Access time from chip enable			100		120	ns
$t_{en(G)}$	Output enable time from $\overline{G}$ / V_{PP}			55		55	ns
t_{dis}	Output disable time from $\overline{G}$ / V_{PP} or $\overline{E}$, whichever occurs first†		0	45	0	45	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ / V_{PP}, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	TMS27C/PC512-15		UNIT
			MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		150	ns
$t_{a(E)}$	Access time from chip enable			150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$ / V_{PP}			75	ns
t_{dis}	Output disable time from $\overline{G}$ / V_{PP} or $\overline{E}$, whichever occurs first†		0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ / V_{PP}, whichever occurs first†		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	TMS2C/PC512-20		TMS27C/PC512-25		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		200		250	ns
$t_{a(E)}$	Access time from chip enable			200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$ / V_{PP}			75		100	ns
t_{dis}	Output disable time from $\overline{G}$ / V_{PP} or $\overline{E}$, whichever occurs first†		0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ / V_{PP}, whichever occurs first†		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.50 V and $\overline{G}$ / V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$ / V_{PP}	0		130	ns

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Reference page 10.)
4. Common test conditions apply for t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.50 V and $\overline{G}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

		MIN	TYP	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	95	100	105	µs
$t_{su(A)}$	Address setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	$\overline{G}$ / V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{h(VPP)}$	$\overline{G}$ / V_{PP} hold time	2			µs
$t_{rec(PG)}$	$\overline{G}$ / V_{PP} recovery time	2			µs
t_{EHD}	Data valid from $\overline{E}$ low			1	µs
$t_{r(PG)G}$	$\overline{G}$ / V_{PP} rise time	50			ns

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Reference below.)

PARAMETER MEASUREMENT INFORMATION

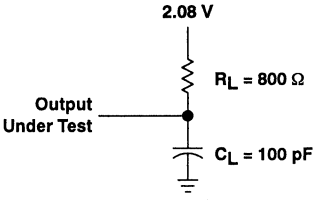
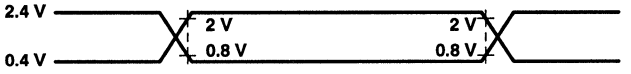


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

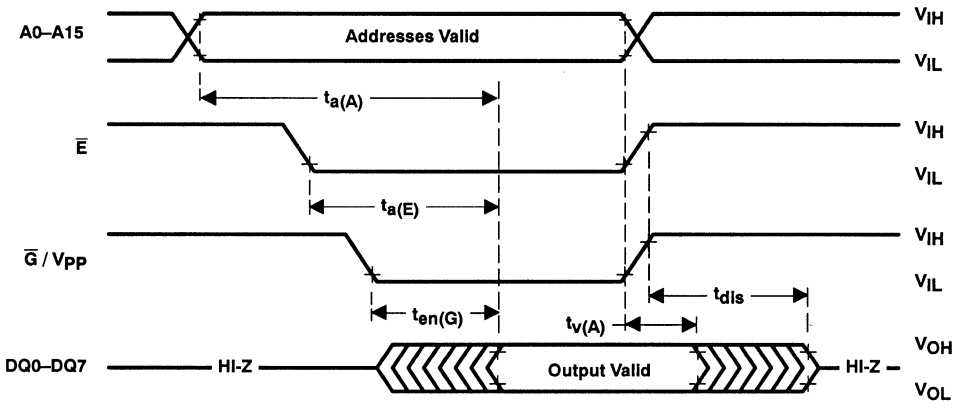
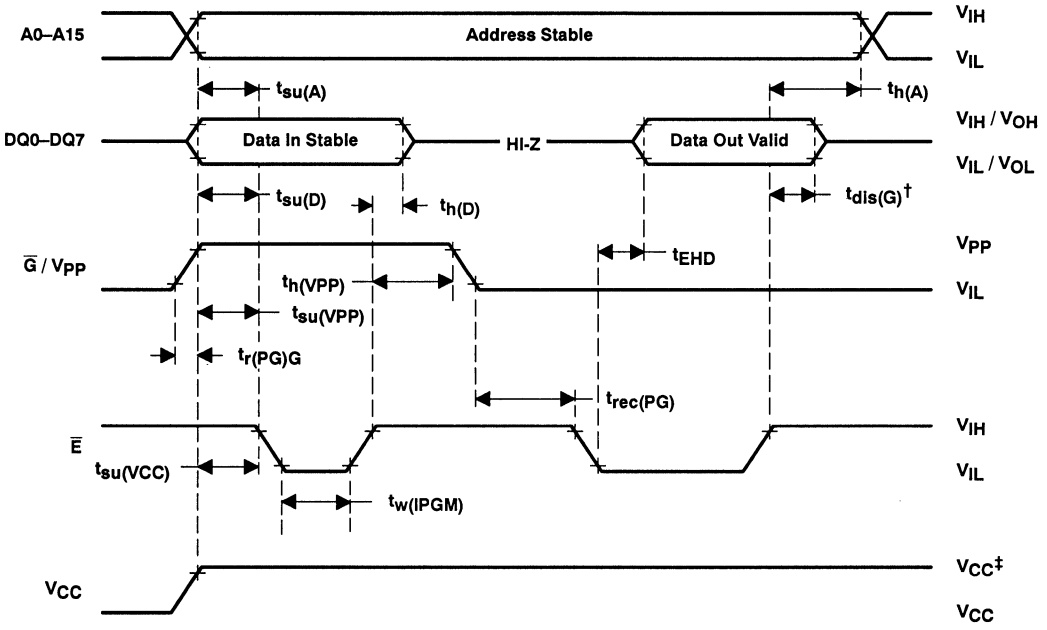


Figure 3. Read Cycle Timing

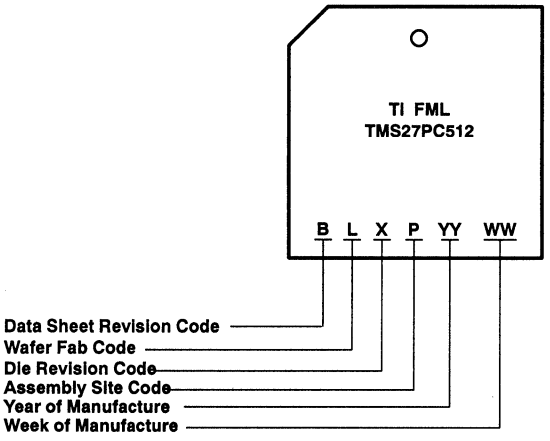


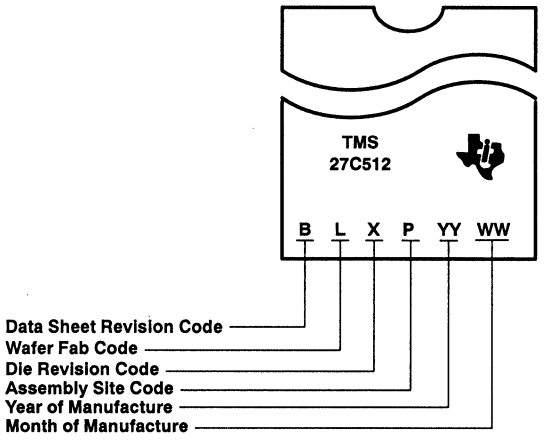
† $t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.
‡ 13-V $\overline{G}$ / V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

device symbolization

This data sheet is applicable to all TI TMS27C512 CMOS EPROMs and TMS27PC512 CMOS OTP PROMs with the data sheet revision code "B" as shown below.





TMS27C010A 1 048 576-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC010A 1 048 576-BIT PROGRAMMABLE READ-ONLY MEMORY

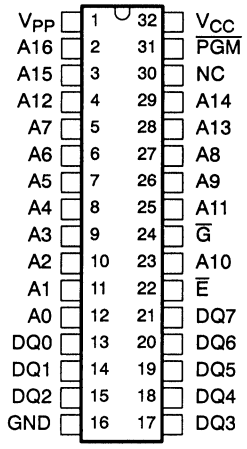
- **Organization . . . 128K × 8**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **Industry Standard 32-Pin Dual-In-line Package, 32-Lead Plastic Leaded Chip Carrier, and 32-Lead Thin Small-Outline Package**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

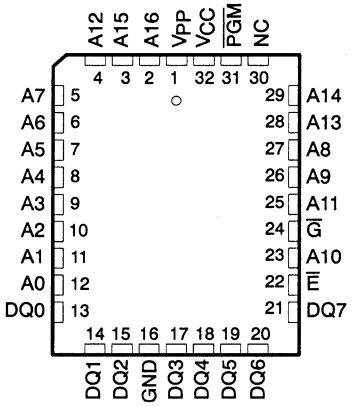
'27C010A-10	100	ns
'27C/PC010A-12	120	ns
'27C/PC010A-15	150	ns
'27C/PC010A-20	200	ns

- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-In and Choices of Operating Temperature Ranges**

J AND N PACKAGES†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

description

The TMS27C010A series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

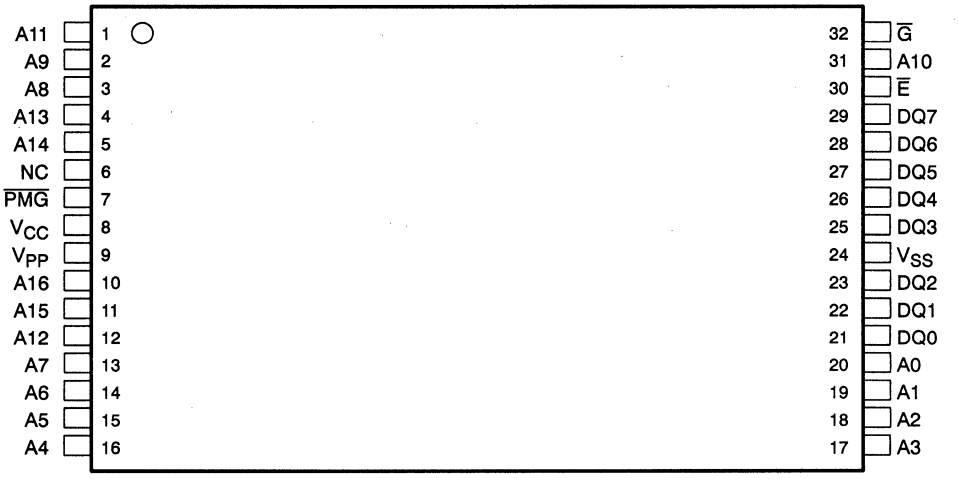
The TMS27PC010A series are 1 048 576-bit, one-time electrically programmable read-only memories.

PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

‡ Only in program mode.

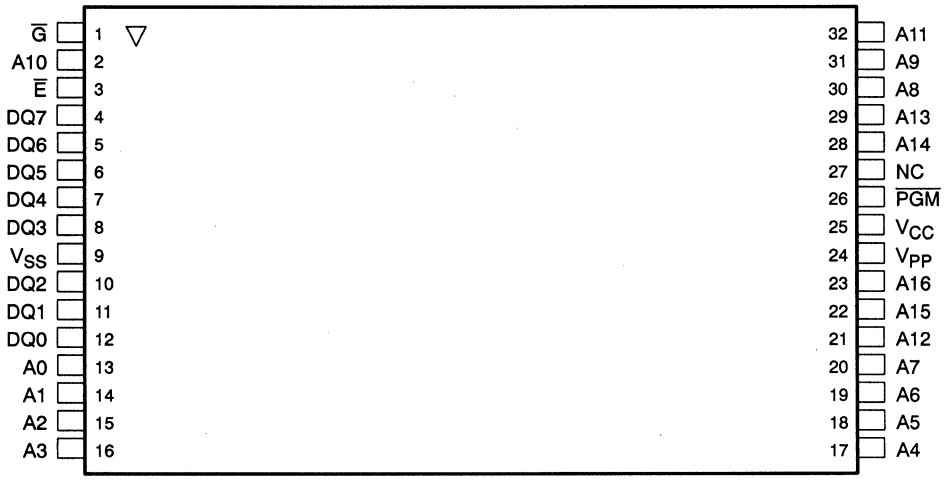
TMS27PC010A . . . DD PACKAGE†

(TOP VIEW)



TMS27PC010A . . . DU PACKAGE†
REVERSE PINOUT

(TOP VIEW)



† The packages shown are for pinout reference only.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C010A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C010A is also offered with two choices of temperature ranges, 0°C to 70°C (JL suffix) and –40°C to 85°C (JE suffix). The TMS27C010A is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffix). (See table below.)

The TMS27PC010A OTP PROM is offered in a dual-in-line plastic package (N suffix), a 32-pin, plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), and a 32-lead TSOP package (DD and DU suffixes). The TMS27PC010A is offered with two choices of temperature ranges, 0°C to 70°C (NL, FML, DDL, and DUL suffixes) and – 40°C to 85°C (NE, FME, DDE, and DUE suffixes). (See table below.)

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C010A-xxx	JL	JE	JL4	JE4
TMS27PC010A-xxx	NL	NE	NL4	NE4
	FML	FME	FML4	FME4
	DDL	DDE		
	DUL	DUE		

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	D6

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C010As or TMS27PC010As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C010A and TMS27PC010A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C010A)

Before programming, the TMS27C010A EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C010A, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27PC010A)

The one-time programmable TMS27PC010A PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C010A and TMS27PC010A are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of thirteen seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\text{ V} \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

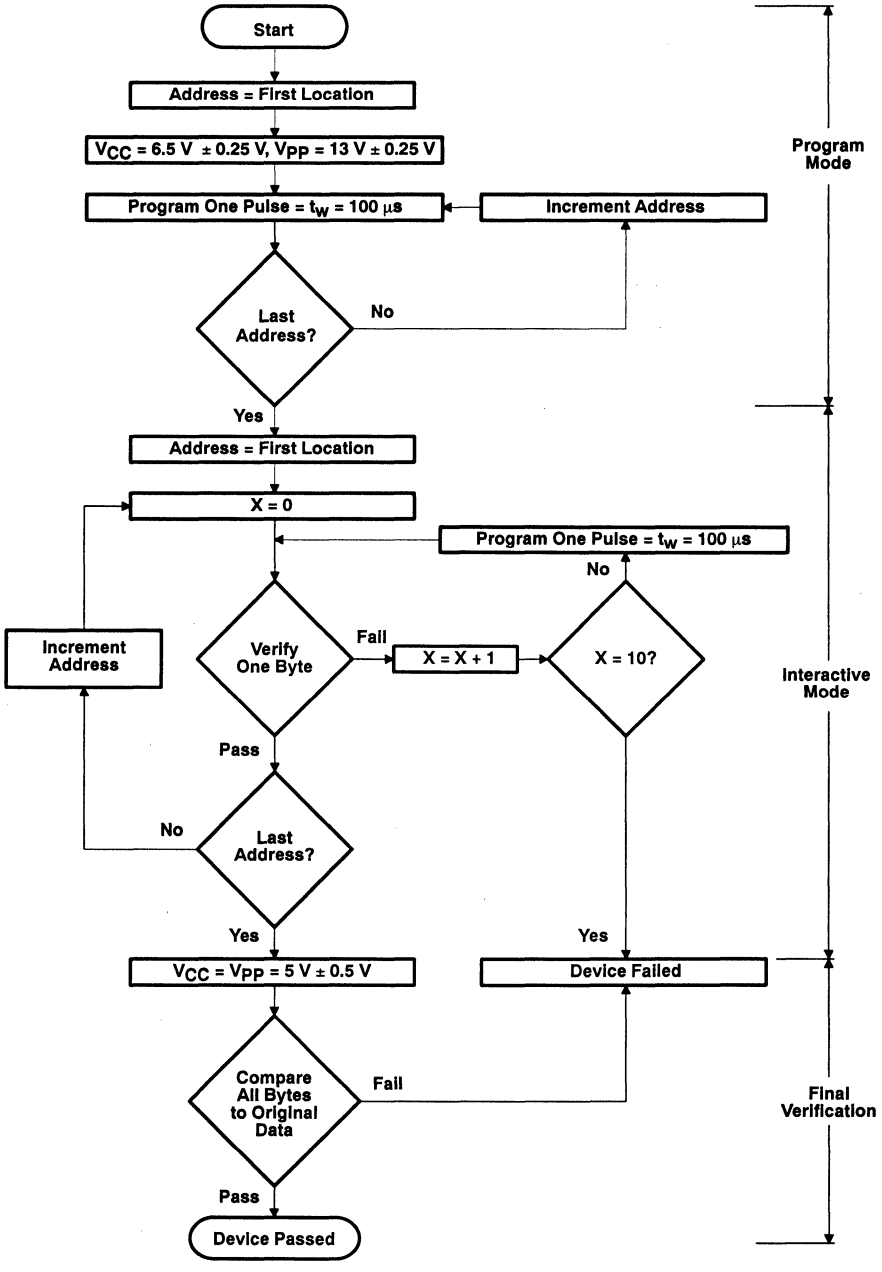


Figure 1. SNAP! Pulse Programming Flowchart

signature mode

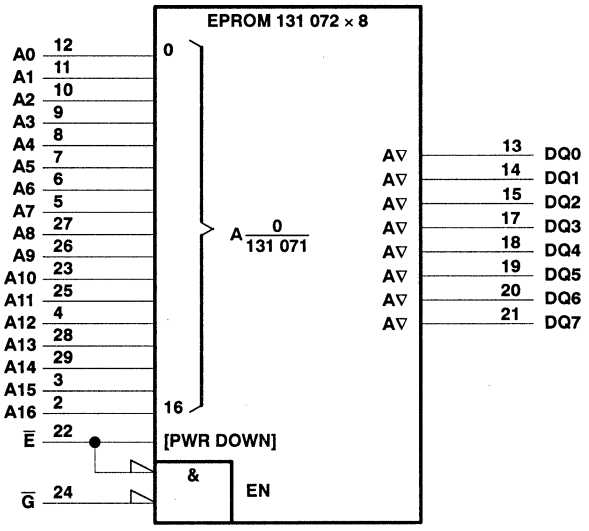
The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for these devices is 97D6. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D6 (Hex), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	0	D6

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, $V_{PP} = V_{CC}$.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J package illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range, All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C010A-_ _JL and JL4,
'27PC010A-_ _NL, FML, DDL, and DUL) ..... 0°C to 70°C
Operating free-air temperature range ('27C010A-_ _JE and JE4,
'27PC010A-_ _NE, FME, DDE, and DUE) ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			'27C010A-10 '27C010A/PC010A-12 '27C010A/PC010A-15 '27C010A/PC010A-20			UNIT
			MIN	TYP	MAX	
V_{CC} Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
	SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP} Supply voltage	Read mode (see Note 3)		V_{CC}−0.6	V_{CC}	V_{CC}+0.6	V
	SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH} High-level dc input voltage		TTL	2.0		V_{CC}+0.5	V
		CMOS	V_{CC}−0.2		V_{CC}+0.5	
V_{IL} Low-level dc input voltage		TTL	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	
T_A Operating free-air temperature		'27C010A-_ _JL,JL4 '27PC010A-_ _NL, FML, DDL, DUL	0		70	°C
T_A Operating free-air temperature		'27C010A-_ _JE,JE4 '27PC010A-_ _NE, FME, DDE, DUE	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = –20 μA	V_{CC}–0.2		V
			I_{OH} = –2.5 mA	3.5		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 5.5 V		500	μA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 5.5 V		100	
I_{CC2}	V_{CC} supply current (active) (output open)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V, t_{cycle} = minimum cycle time†, outputs open		30	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_o	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27C010A-10		'27C010A-12 '27PC010A-12		'27C010A-15 '27PC010A-15		'27C010A-20 '27PC010A-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		100		120		150		200	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	50	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		ns

¶ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).

PARAMETER MEASUREMENT INFORMATION

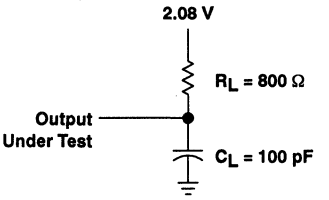
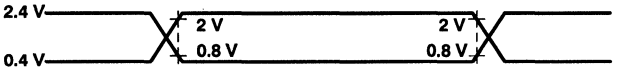


Figure 2. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

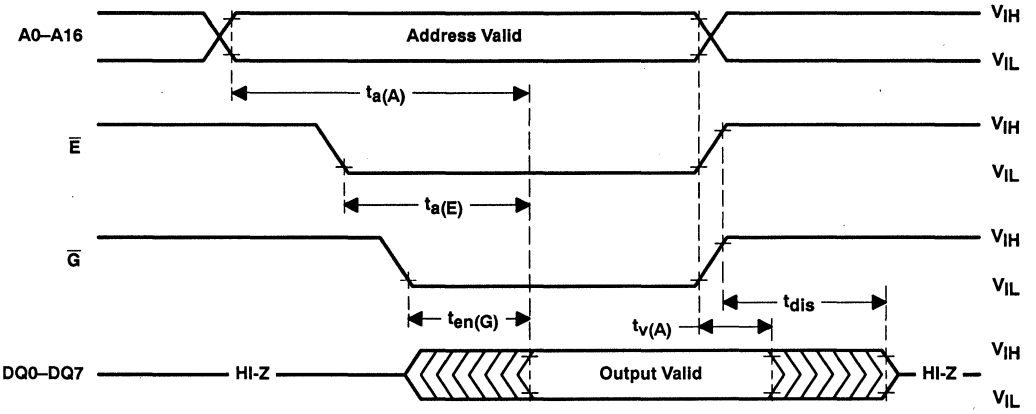
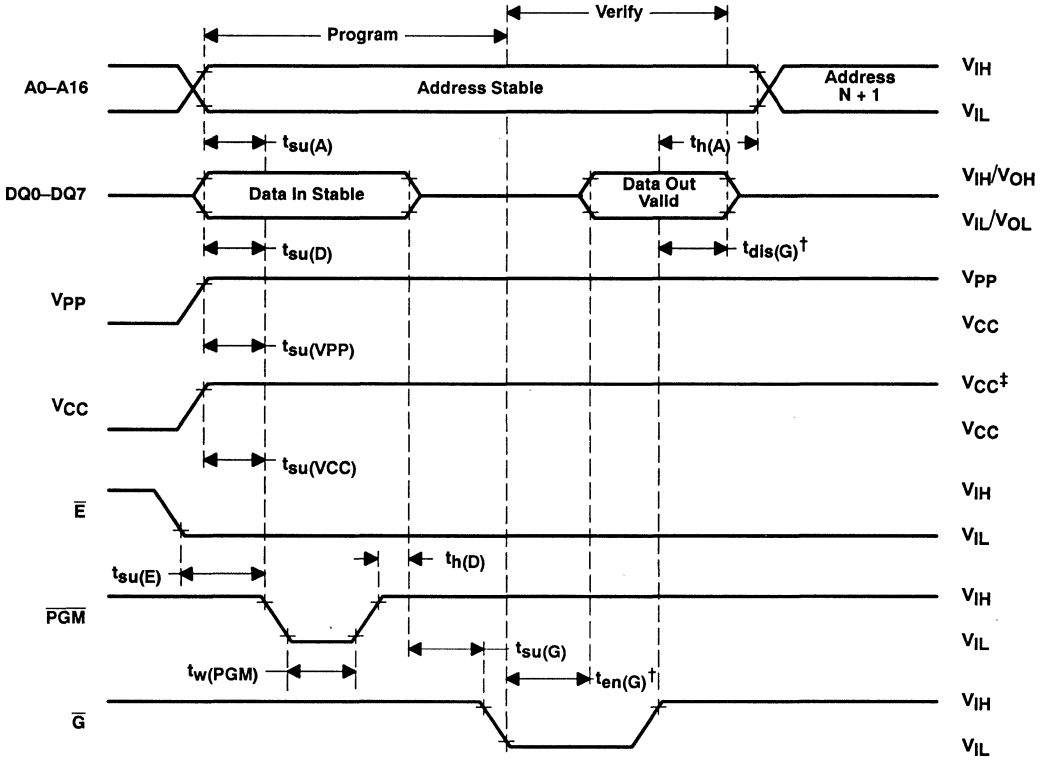


Figure 3. Read Cycle Timing

PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

TMS27C210A 1 048 576-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC210A 1 048 576-BIT PROGRAMMABLE READ-ONLY MEMORY

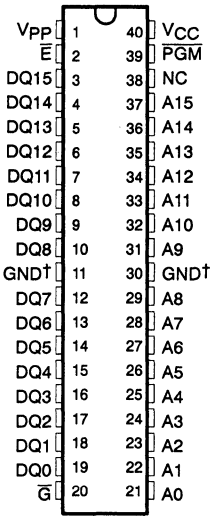
SMLS310B–NOVEMBER 1990–REVISED NOVEMBER 1992

- **Wide-Word Organization . . . 64K × 16**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **40-Pin Dual-In-Line Package and 44-Lead Plastic Leaded Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **±10% V_{CC} Tolerance**
- **Max Access/Min Cycle Time**

'27C210A-10	100	ns
'27C/PC210A-12	120	ns
'27C/PC210A-15	150	ns
'27C/PC210A-20	200	ns
'27C/PC210A-25	250	ns

- **16-Bit Output For Use in Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-In and Choices of Operating Temperature Ranges**

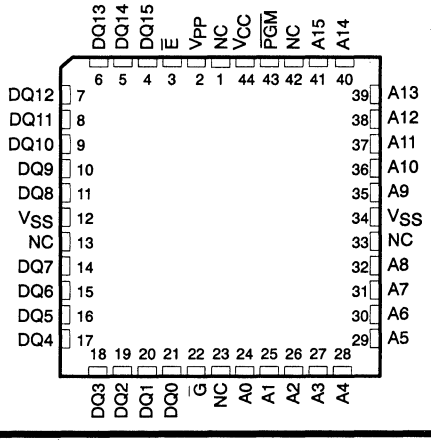
J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
DQ0–DQ15	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 must be connected externally to ground.
‡ Only in program mode.

FN PACKAGE
(TOP VIEW)



description

The TMS27C210A series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC210A series are 1 048 576-bit, one-time electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C210A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C210A is also offered with two choices of temperature ranges, 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C210A is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes).

The TMS27PC210A OTP PROM is offered in a 44-pin plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC210A is offered with two choices of temperature ranges, 0°C to 70°C (FNL suffix) and –40°C to 85°C (FNE suffix). The TMS27PC210A is also offered with 168 hour burn-in on both temperature ranges (FNL4 and FNE4 suffixes). (See table below.)

EPROM AND OTP PROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C210A-xx	JL	JE	JL4	JE4
TMS27PC210A-xx	FNL	FNE	FNL4	FNE4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation for the TMS27C210A and TMS27PC210A are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ15	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	AB

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C210As or TMS27PC210As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C210A and TMS27PC210A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 50 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure (TMS27C210A)

Before programming, the TMS27C210A is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C210A the window should be covered with an opaque label.

initializing (TMS27PC210A)

The one-time programmable TMS27PC210A PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C210A and TMS27PC210A are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can program in a nominal time of seven seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (sixteen bits) on pins DQ0 through DQ15. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0–DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 97AB. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code AB (Hex), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	0	1	0	1	0	1	1	AB

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A15 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

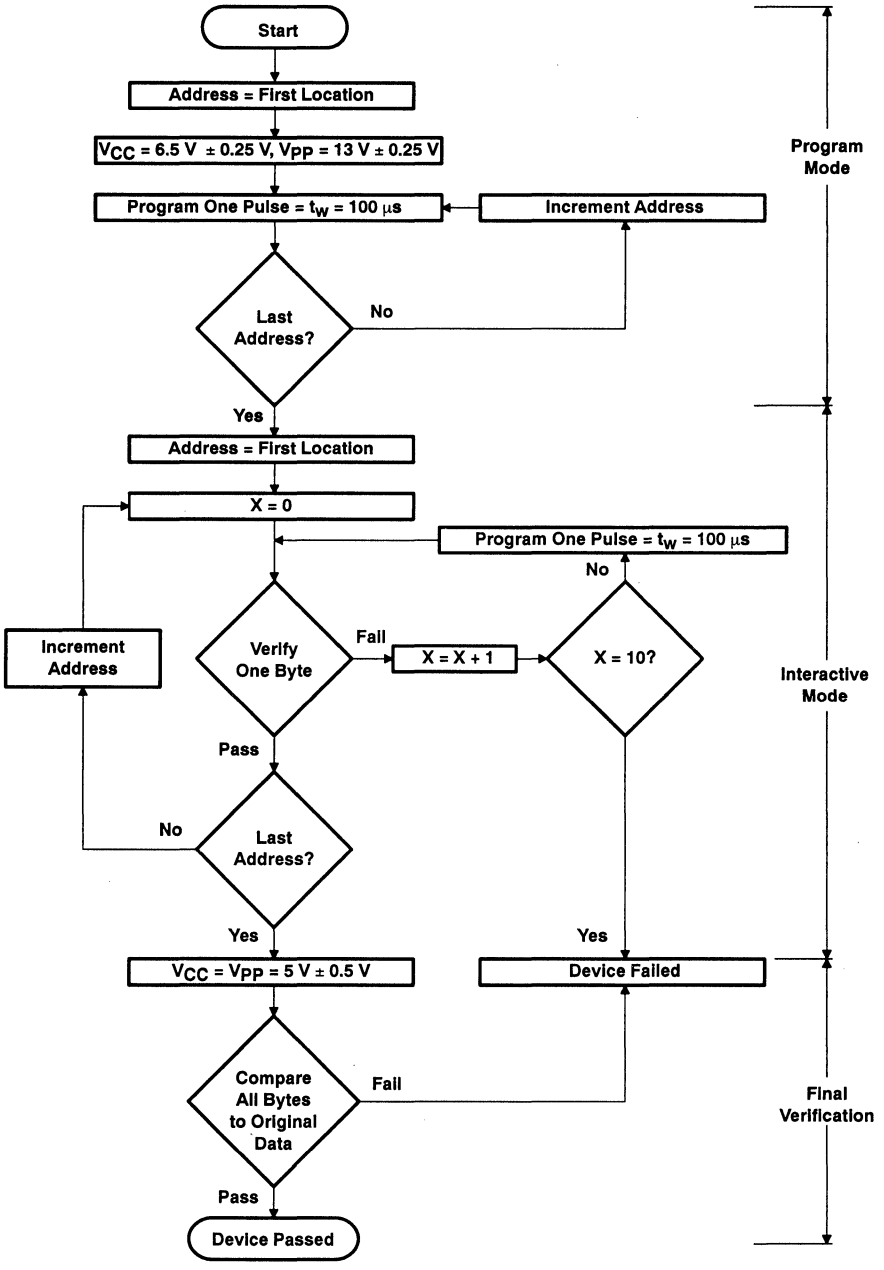
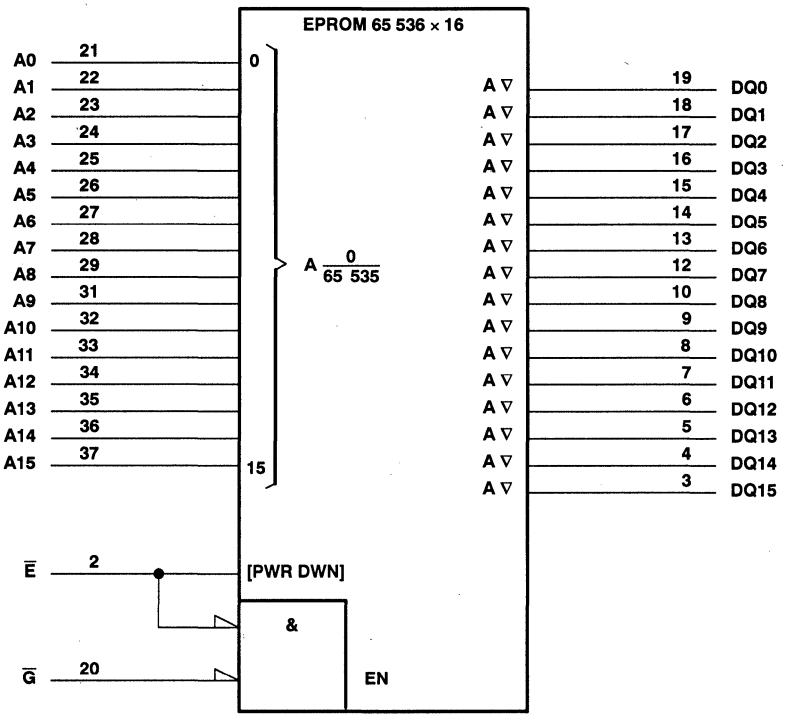


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C210A-_ _JL and JL4, '27PC210A-_ _FNL) ..... 0° C to 70°C
Operating free-air temperature range ('27C210A-_ _JE and JE4) ..... − 40° C to 85°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27C210A-10 TMS27C/PC210A-12 TMS27C/PC210A-15 TMS27C/PC210A-20 TMS27C/PC210A-25			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.5	5	5.5	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode	$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level dc input voltage	TTL	2		$V_{CC}+0.5$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	
T_A	Operating free-air temperature	'27C210A-_ _JL, JL4 '27PC210A-_ _FNL	0		70	°C
T_A	Operating free-air temperature	'27C210A-_ _JE, JE4	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		$I_{OH}=-20\ \mu A$	$V_{CC}-0.2$		V
			$I_{OH}=-2$ mA	2.4		
V_{OL}	Low-level dc output voltage		$I_{OL}=2.1$ mA		0.4	V
			$I_{OL}=20\ \mu A$		0.1	
I_I	Input current (leakage)		$V_I=0$ to 5.5 V		±1	µA
I_O	Output current (leakage)		$V_O=0$ to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{IH}$		500	µA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open†		50	mA

† Minimum cycle time = maximum address access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	$V_I=0$, f = 1 MHz		8	12	pF
C_O	Output capacitance	$V_O=0$, f = 1 MHz		12	15	pF

‡ Capacitance measurements are made on a sample basis only.
§ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 & 4)	'27C210A-10		'27C210A-12 '27PC210A-12		'27C210A-15 '27PC210A-15		'27C210A-20 '27PC210A-20		'27C210A-25 '27PC210A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			100		120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC testing waveform)

4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low). (reference AC testing waveform)

PARAMETER MEASUREMENT INFORMATION

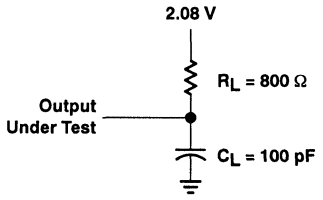
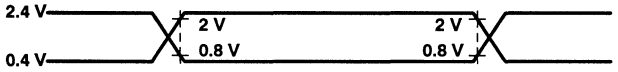


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

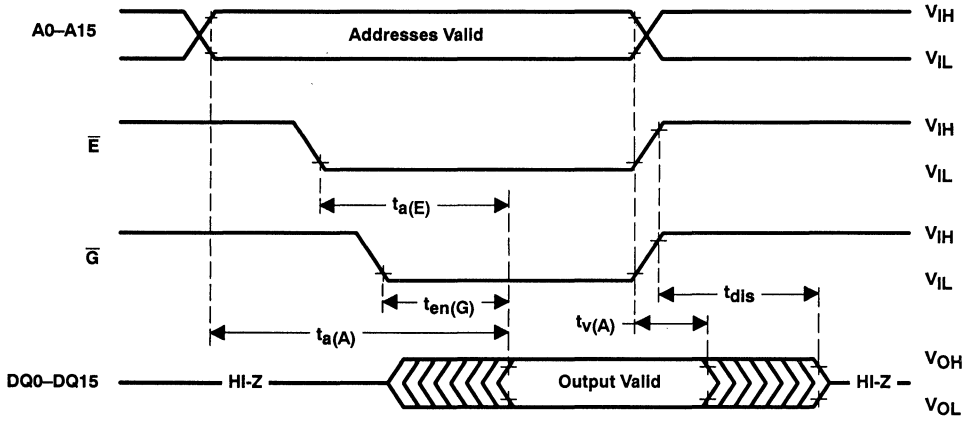
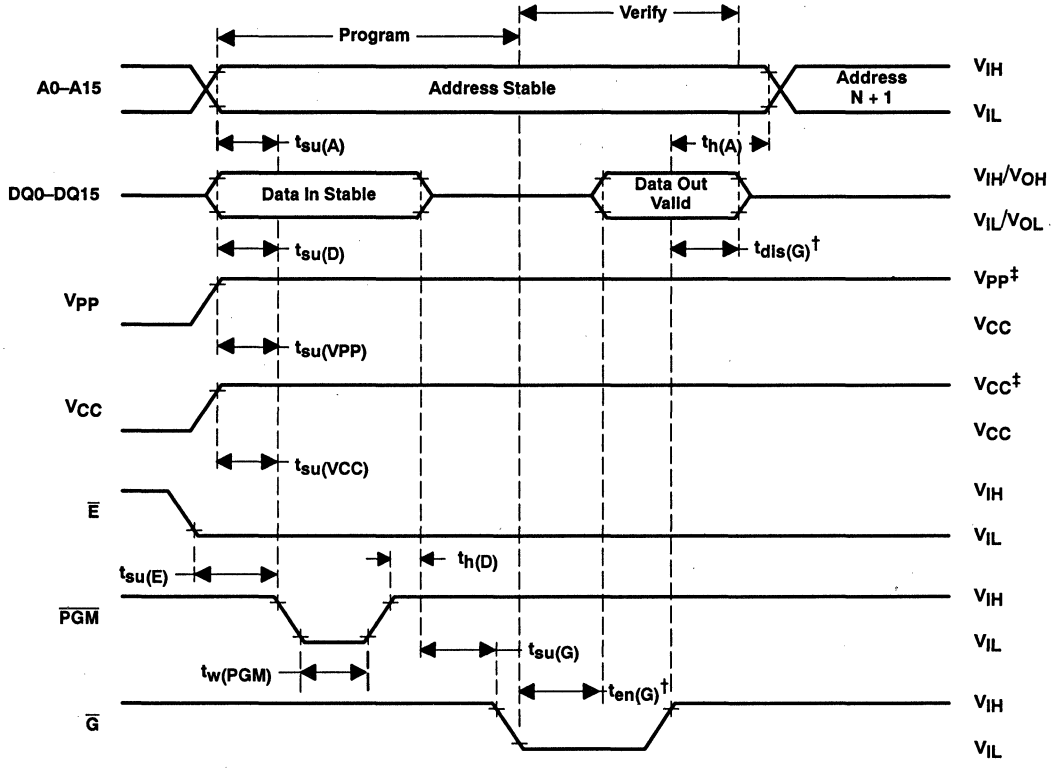


Figure 3. Read Cycle Timing

PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

TMS27C020 2 097 152 BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC020 2 097 152 BIT PROGRAMMABLE READ-ONLY MEMORY

ADVANCE INFORMATION

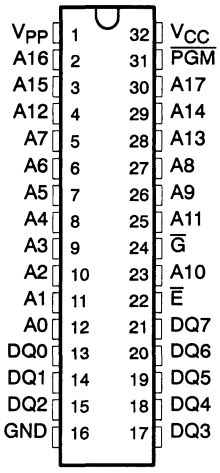
- Organization . . . 256K × 8
- Single 5-V Power Supply
- Operationally Compatible With Existing Megabit EPROMs
- Industry Standard 32-Pin Dual-In-line Package and 32-Lead Plastic Leaded Chip Carrier
- All Inputs/Outputs Fully TTL Compatible
- ±10% V_{CC} Tolerance
- Max Access/Min Cycle Time

  V_{CC} ± 10%

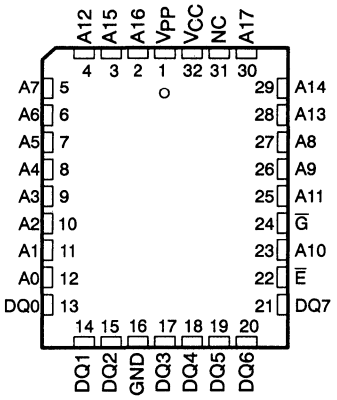
'27C/PC020-12	120 ns
'27C/PC020-15	150 ns
'27C/PC020-20	200 ns
'27C/PC020-25	250 ns

- 8-Bit Output For Use in Microprocessor-Based Systems
- Very High-Speed SNAP! Pulse Programming
- Power Saving CMOS Technology
- 3-State Output Buffers
- 400 mV Minimum DC Noise Immunity With Standard TTL Loads
- Latchup Immunity of 250 mA on All Input and Output Pins
- No Pullup Resistors Required
- Low Power Dissipation (V_{CC} = 5.5 V)
  - — Active . . . 165 mW Worst Case
  - — Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)
- PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges

J PACKAGE†
(TOP VIEW)



TMS27PC020†‡
FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply§

† Packages are shown for pinout reference only.
‡ The ADVANCE INFORMATION notice applies to this package.
§ Only in program mode.

description

The TMS27C020 series are 2 097 152-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC020 series are one-time electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C020 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C020 is also offered with two choices of temperature ranges of 0° to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C020 is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC020 is offered in a 32-lead plastic leaded chip carrier using 1,25 mm (50 mil) lead spacing (FM suffix). The TMS27PC020 is offered with a temperature range of 0°C to 70°C.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS. TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C020-XXX	JL	JE	JL4	JE4
TMS27PC020-XXX	FML			

These EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation for the TMS27C020 and TMS27PC020 are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V) on A9 for the signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	32

† X can be V_{IL} or V_{IH}
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C020s or TMS27PC020s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C020 and TMS72PC020 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure

Before programming, the TMS27C020 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C020, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The TMS27C020 and TMS27PC020 are programmed using the TI SNAP! Pulse programming algorithm, illustrated by the flowchart in Figure 1, which programs in a nominal time of twenty-six seconds. Actual programming time will vary as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for the TMS27C020 is 9732. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 32 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	0	1	1	0	0	1	0	32

† $\overline{E}$ = $\overline{G}$ = V_{IL}, A1–A8 = V_{IL}, A9 = V_H, A10–A17 = V_{IL}, V_{PP} = V_{CC}.

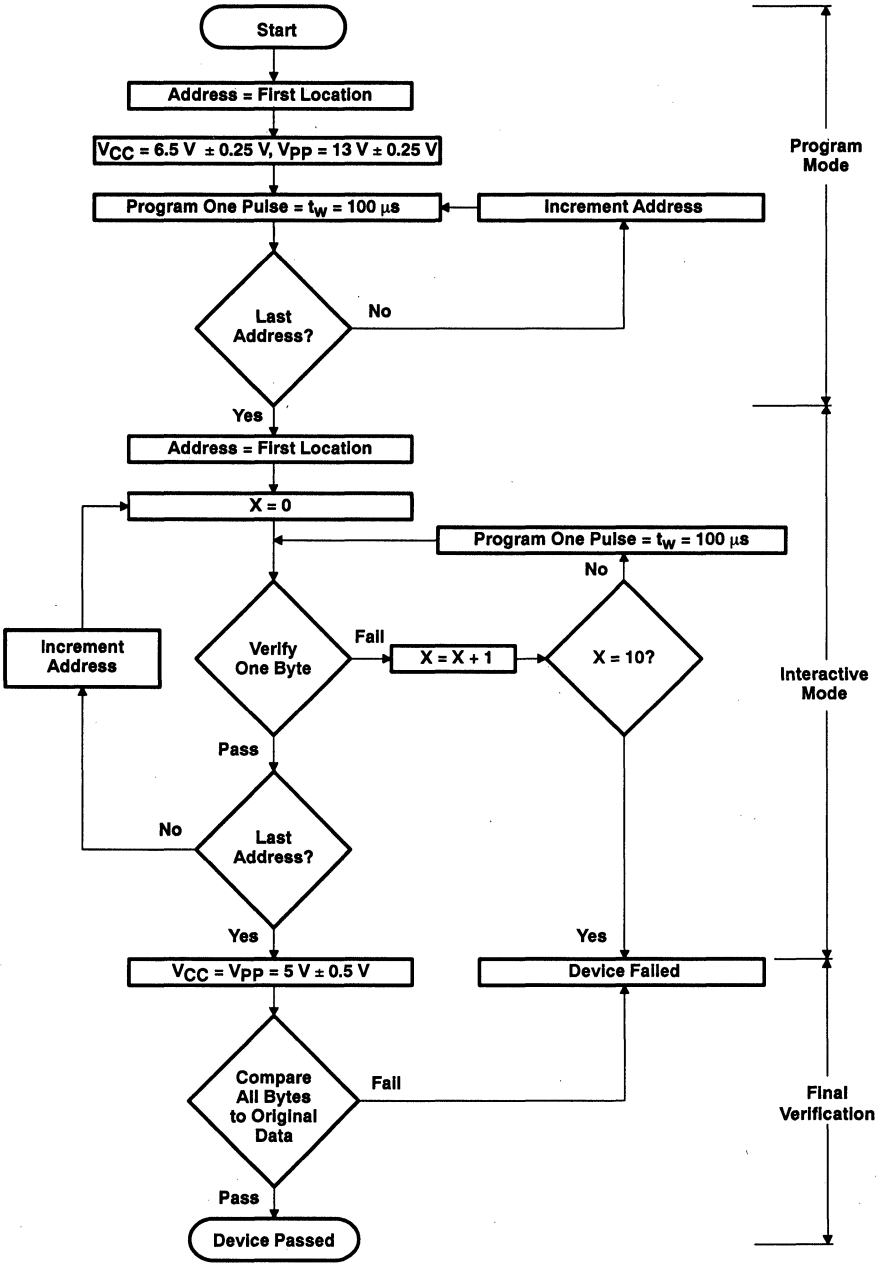
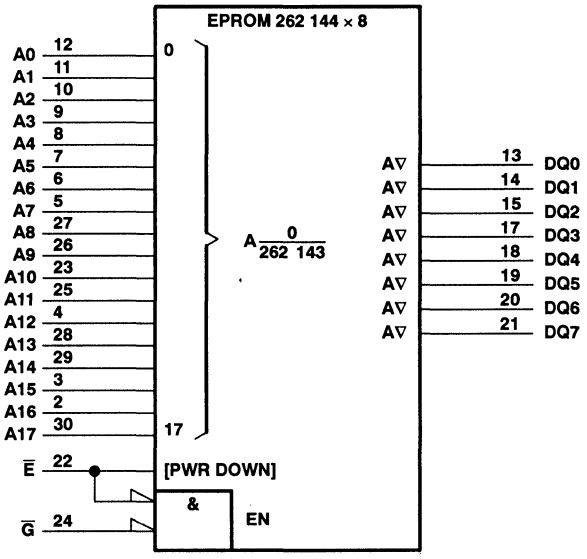


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C020-_ _ JL and JL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C020-_ _JE and JE4) ..... − 40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$	V_{CC}	$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+0.5$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		GND+0.2	
T_A	Operating free-air temperature		'27C020-_ _JL, JL4	0		70	°C
T_A	Operating free-air temperature		'27C020-_ _JE, JE4	− 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = −20 μA	V_{CC} − 0.2		V
			I_{OH} = − 2 mA	2.4		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 5.5 V		500	μA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 5.5 V		100	
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V t_{cycle} = minimum cycle time, outputs open†		30	mA

† Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 & 4)	'27C020-12 '27PC020-12		'27C020-15 '27PC020-15		27C020-20 27PC020-20		'27C020-25 '27PC020-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		120		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			120		150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	60	0	60	0	80	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		ns

¶ Value calculated from 0.5-V delta to measured output level. This parameter is sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic logic low. (reference AC Testing Wave Form)

PARAMETER MEASUREMENT INFORMATION

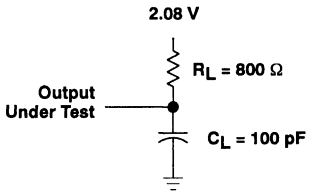
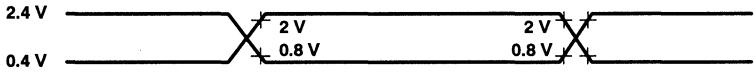


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

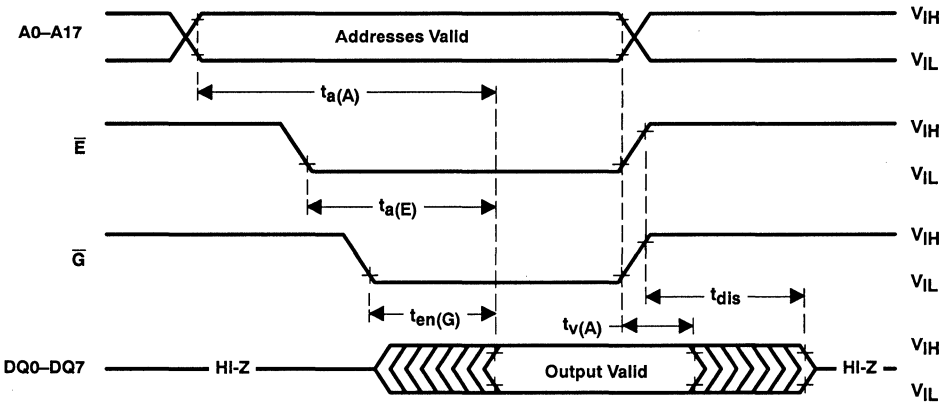
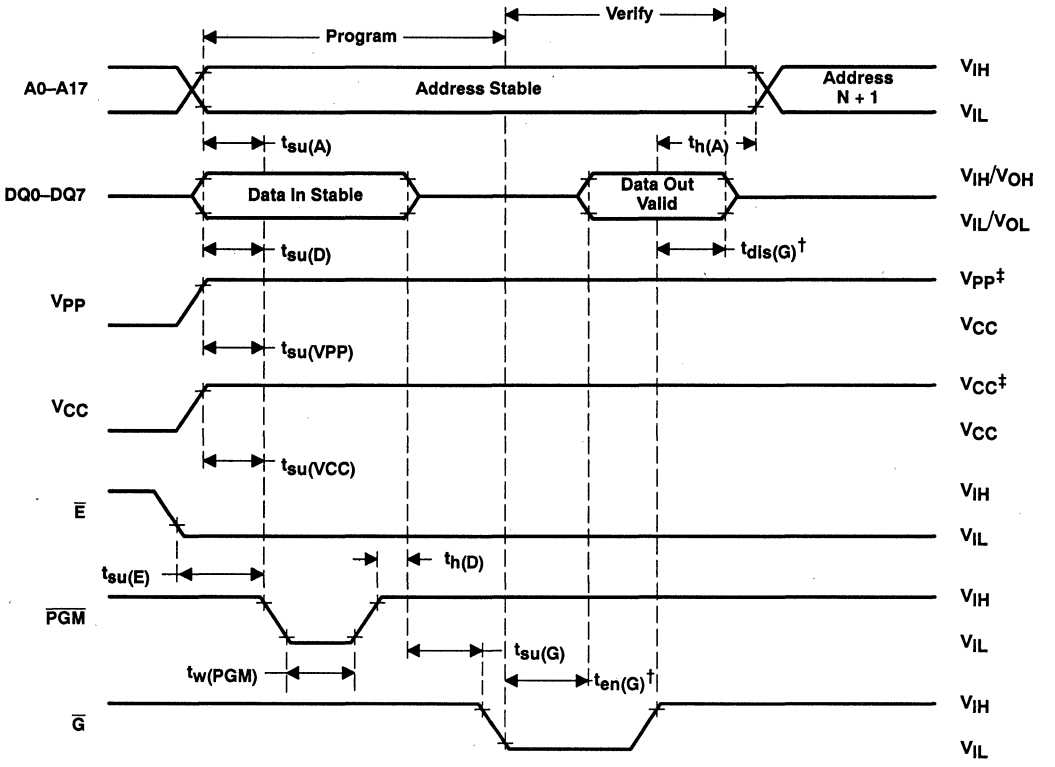


Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

TMS27C040 4 194 304-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC040 4 194 304-BIT PROGRAMMABLE READ-ONLY MEMORY

SMLS040D–NOVEMBER 1990–REVISED JANUARY 1993

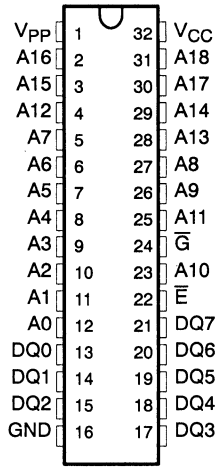
- **Organization . . . 512K × 8**
- **Single 5-V Power Supply**
- **Industry Standard 32-Pin Dual In-Line Package and 32-Lead Plastic Leaded Chip Carrier**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

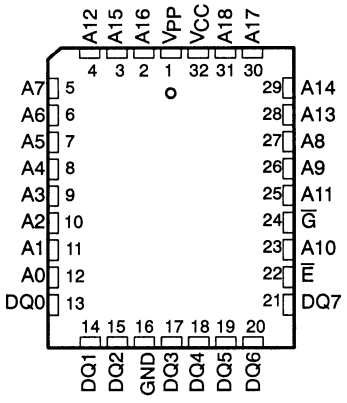
'27C/PC040-10	100 ns
'27C/PC040-12	120 ns
'27C/PC040-15	150 ns

- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Assured DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Cas E (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Two Operating Temperature Ranges**

TMS27C040
J PACKAGE†
(TOP VIEW)



TMS27PC040
FM PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

description

The TMS27C040 series are 4 194 304-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC040 series are 4 194 304-bit, one-time electrically programmable read-only memories.

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits. Each output can drive one Series 74

PIN NOMENCLATURE	
A0–A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

‡ Only in program mode.

TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS27C040 is offered in a 600-mil ceramic dual-in-line package (J suffix). The TMS27C040 is offered with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C040 is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC040 is offered in a 32-lead plastic leaded chip carrier package (FM suffix). The TMS27PC040 is characterized for operation from 0°C to 70°C (FML suffix).

FUNCTION	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR OPERATING TEMPERATURE RANGES WITH PEP4 168 HR. BURN-IN	
	0°C TO 70°C	–40 °C TO 85°C	0°C TO 70°C	–40 °C TO 85°C
TMS27C040-XXX	JL	JE	JL4	JE4
TMS27PC040-XXX	FML			

These EPROMs and PROMS operate from a single 5-V supply (in the read mode), and they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V) on A9 for the signature mode.

MODE	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	DQ0-DQ7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Signature Mode	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H	V_{IL}	MFG Code 97
						V_{IH}	Device Code 50

† X can be V_{IL} or V_{IH}
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C040s or TMS27PC040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C040 and TMS27PC040 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure (TMS27C040)

Before programming, the TMS27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2 . A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27PC040)

The one-time programmable TMS27PC040 PROM is provided with all bits in logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C040 and TMS27PC040 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$, and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the TMS27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

† $\overline{E} = \overline{G} = V_{IL}$, A1-A8 = V_{IL}, A9 = V_H, A10-A18 = V_{IL}, $V_{PP} = V_{CC}$.

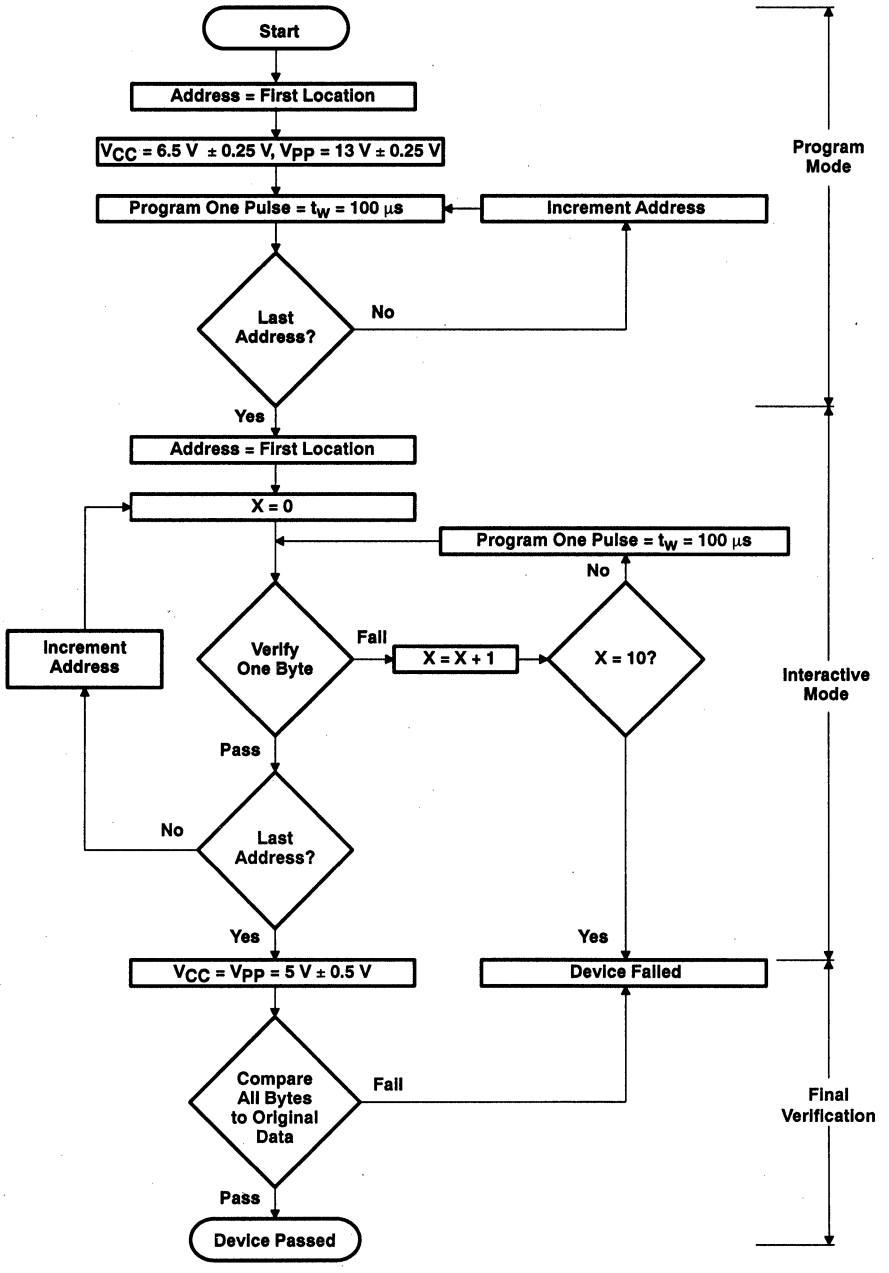
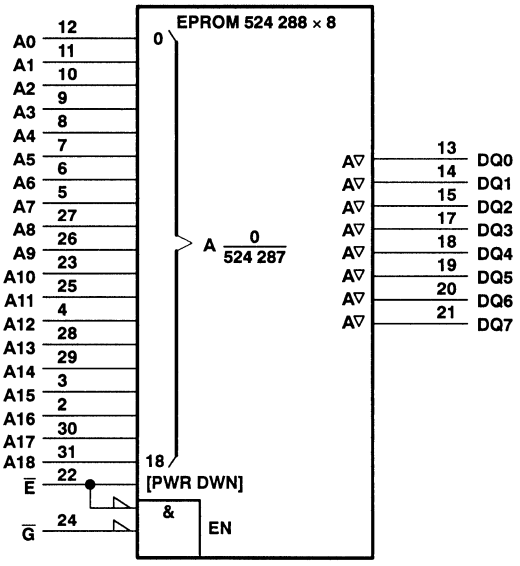


Figure 1. SNAP! Pulse Programming Flow Chart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C040-_ _JL and JL4;'27PC040-_ _FML) ..... 0°C to 70°C
Operating free-air temperature range ('27C040-_ _JE and JE4) ..... − 40°C to 85°C
Storage temperature range ..... −65°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode		V_{CC} − 0.6		V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC} + 0.5	V
			CMOS	V_{CC} − 0.2		V_{CC} + 0.5	
V_{IL}	Low-level dc input voltage		TTL	− 0.5		0.8	V
			CMOS	− 0.5		0.2	V
T_A	Operating free-air temperature	'27C040-_ _JL and JL4 '27PC040-_ _FML		0		70	°C
T_A	Operating free-air temperature	'27C040-_ _JE and JE4		− 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = − 400 μA	2.4		V
			I_{OH} = − 20 μA	V_{CC} − 0.1		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 μA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	μA
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V t_{cycle} = minimum cycle time, outputs open‡		50	mA

‡ Minimum cycle time = maximum access time.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$		4	8	pF
C_O	Output capacitance	$V_O = 0$		8	12	pF

† Capacitance measurements are made on sample basis only.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 & 4)	'27C/PC040-10		'27C/PC040-12		'27C/PC040-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first§		0		0		0		ns

§ Value calculated from 0.5-V delta to measured output level.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic logic low. (reference AC Testing Wave Form)

PARAMETER MEASUREMENT INFORMATION

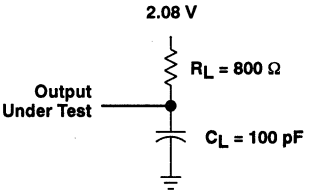
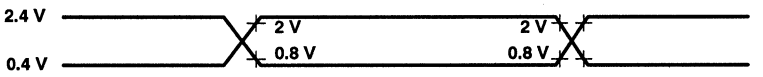


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

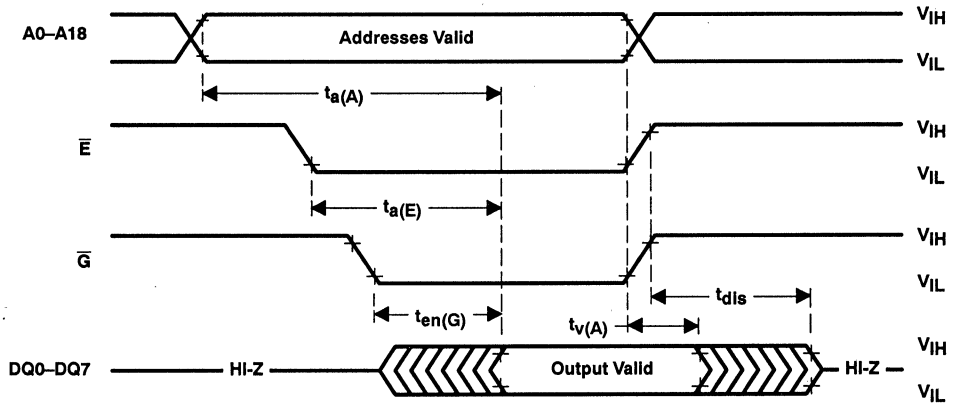
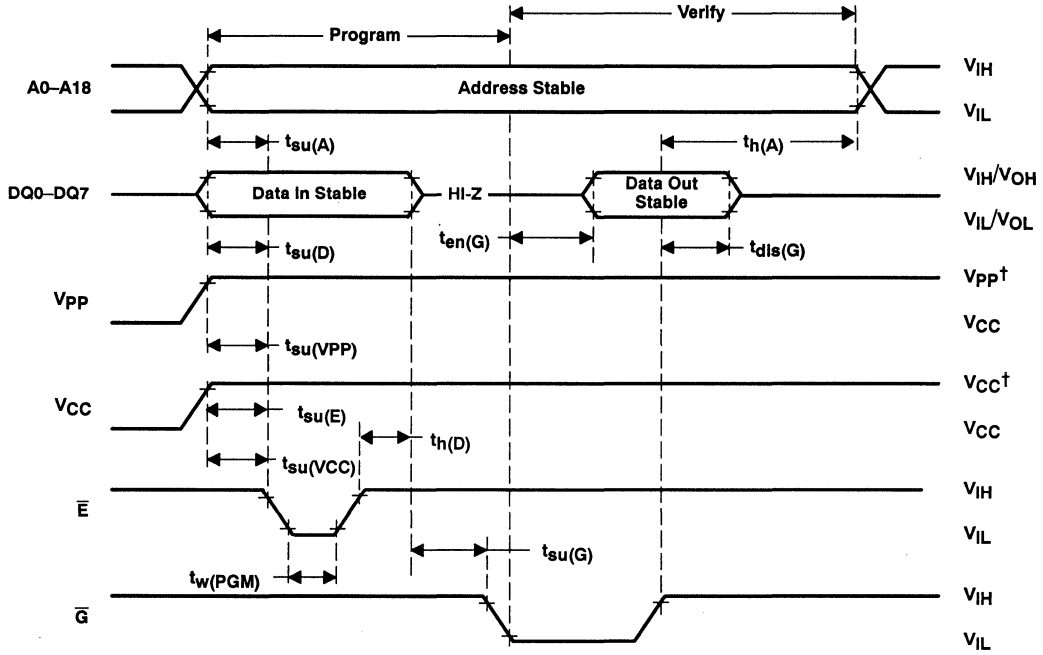


Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

TMS27C240 4 194 304-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC240 4 194 304-BIT PROGRAMMABLE READ-ONLY MEMORY

- **Wide-Word Organization . . . 256K × 16**
- **Single 5-V Power Supply**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operations (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**
  V_{CC} ± 10%

'27C/PC240-10	**100 ns**
'27C/PC240-12	**120 ns**
'27C/PC240-15	**150 ns**

- **16-Bit Output For Use In Microprocessor-Based Systems**
- **Very High Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**

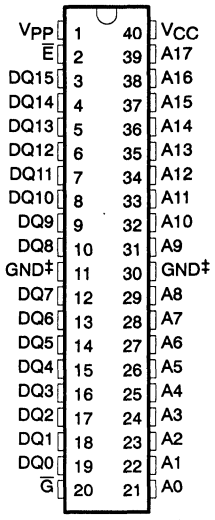
description

The TMS27C240 series are 4 194 304-bit, ultraviolet-light erasable, electrically programmable read-only memories.

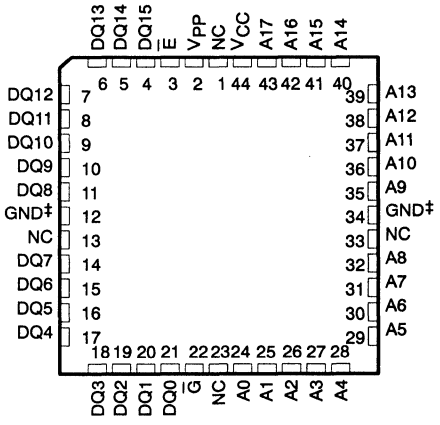
The TMS27PC240 series are 4 194 304-bit, one-time electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by

TMS27C240 J PACKAGE†
(TOP VIEW)



TMS27PC240 FN PACKAGE†
(TOP VIEW)



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0–A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
DQ0–DQ15	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply§

‡ Pins 11 and 30 (J package) and pins 12 and 34 (FN package) must be connected externally to ground.
§ Only in program mode.

Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C240 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C240 is also offered with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C240 is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC240 OTP PROM is offered in a 44-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC240 is characterized for a temperature range of 0°C to 70°C.

	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C240-XXX	JL	JE	JL4	JE4
TMS27PC240-XXX	FNL	FNE	N/A	N/A

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), and they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming . All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The eight modes of operation for the TMS27C240 and TMS27PC240 are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	I/O
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	DQ0–DQ7 DQ8–DQ15
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X†	V_{CC}	V_{CC}	X	X	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	Mfg Code 0097
Signature Mode (Device)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IH}	Device Code 0030

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C240s or TMS27PC240s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C240 and TMS27PC240 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C240)

Before programming, the TMS27C240 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C240, the window should be covered with an opaque label.

initializing (TMS27PC240)

The one-time programmable TMS27PC240 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C240 and TMS27PC240 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ15. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP}$ = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 31 for the J package) is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0–DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 9730. A0 low selects the manufacturer's code 97 (hex), and A0 high selects the device code 30 (hex), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	0	1	1	0	0	0	0	30

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A17 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

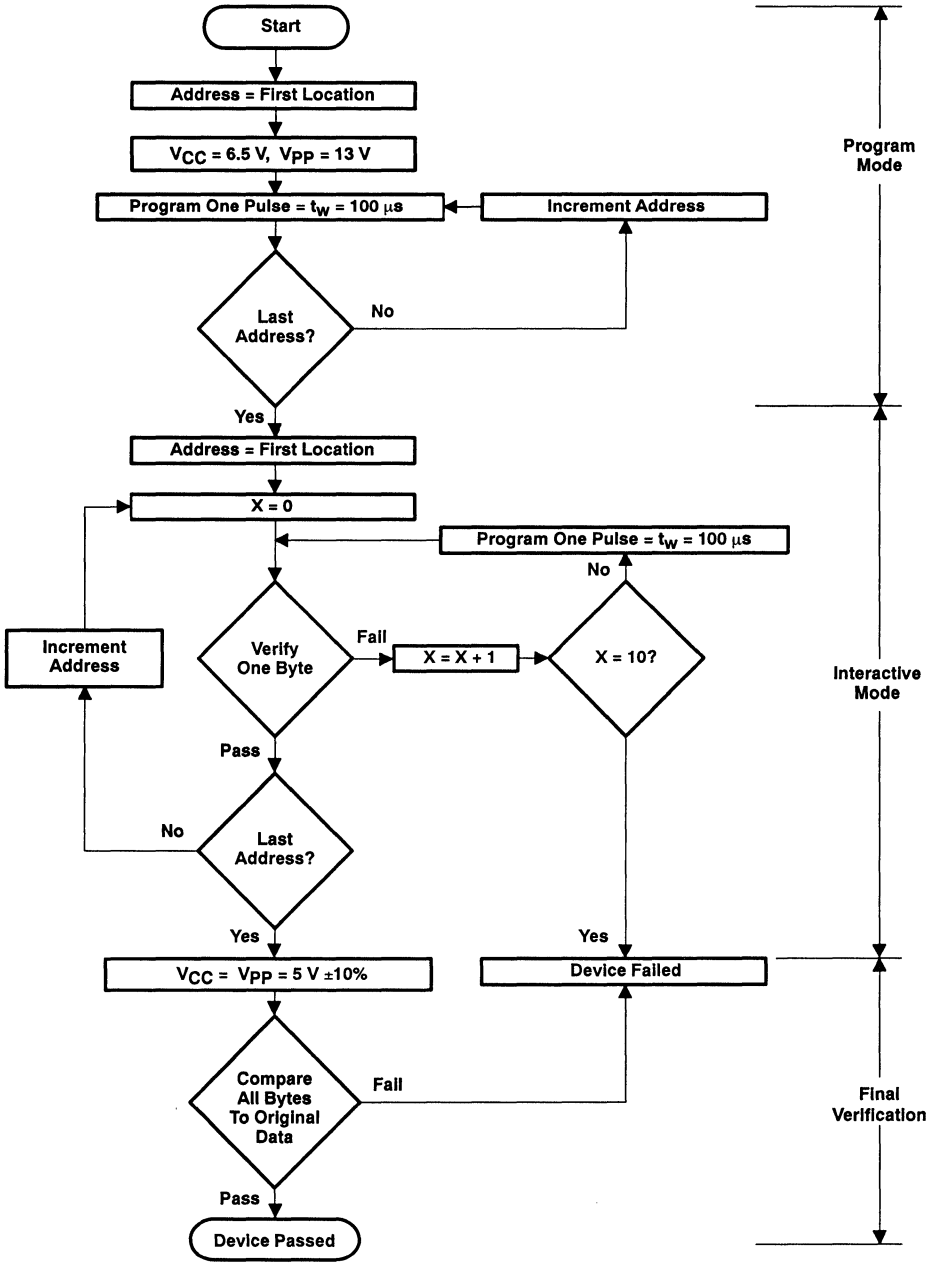
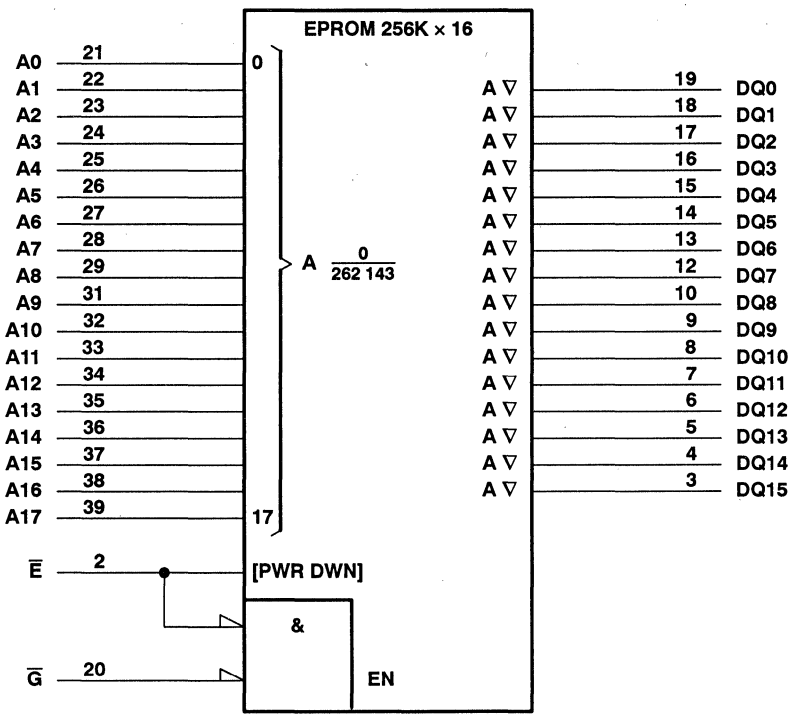


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 13 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C240-_ _JL and JL4,
'27PC240-_ _FNL) ..... 0° C to 70° C
Operating free-air temperature range ('27C240-_ _JE and JE4) ..... − 40° C to 85° C
Storage temperature range ..... −65°C to 150° C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+0.5$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+0.5$	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature		'27C240-_ _JL, JL4 '27PC240-_ _FNL	0		70	°C
T_A	Operating free-air temperature		'27C240-_ _JE, JE4	−40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		$I_{OH}=-400\ \mu A$	2.4		V
			$I_{OH}=-20\ \mu A$	$V_{CC}-0.1$		
V_{OL}	Low-level dc output voltage		$I_{OL}=2.1$ mA		0.4	V
			$I_{OL}=20\ \mu A$		0.1	
I_I	Input current (leakage)		$V_I=0$ to 5.5 V		±1	µA
I_O	Output current (leakage)		$V_O=0$ to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		50	mA
I_{CC1}	VCC supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{IH}$		1	mA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	µA
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open		50	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I=0$		4	8	pF
C_O	Output capacitance	$V_O=0$		8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 & 4)	'27C/PC240-10		'27C/PC240-12		'27C/PC240-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 3)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

PARAMETER MEASUREMENT INFORMATION

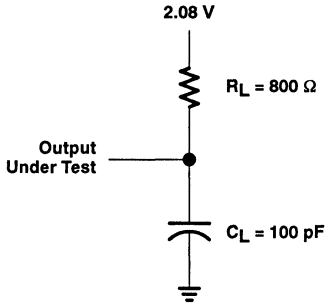
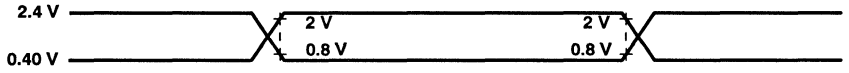


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

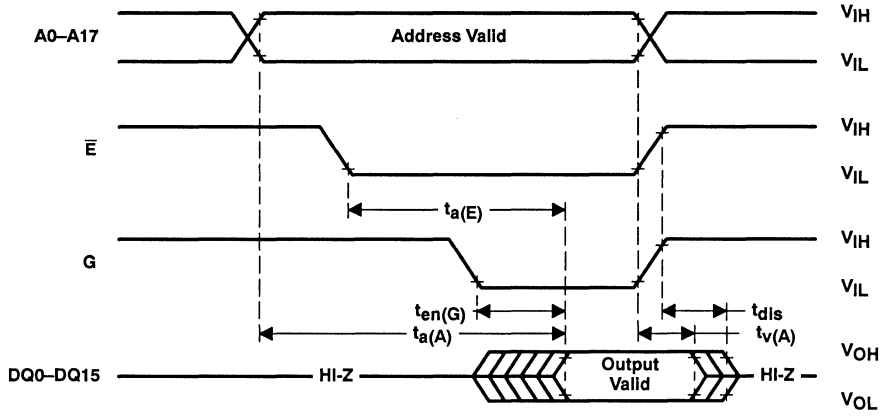
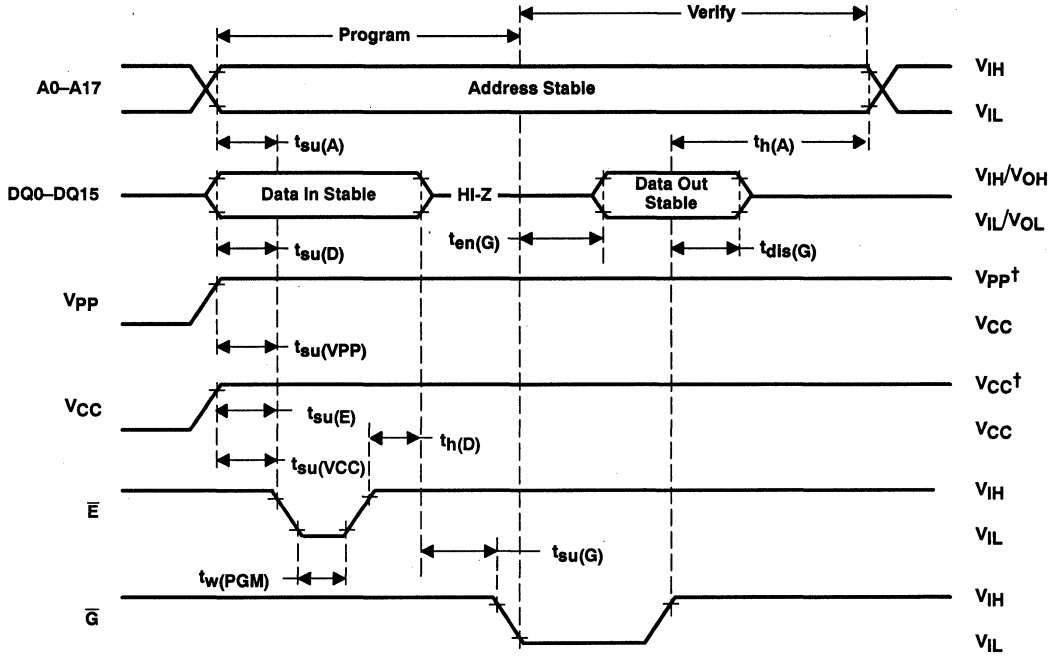


Figure 3. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Programming Cycle Timing (SNAP! Pulse Programming)

TMS27C400 4 194 304-BIT UV ERASABLE PROGRAMMABLE READ-ONLY MEMORY
TMS27PC400 4 194 304-BIT PROGRAMMABLE READ-ONLY MEMORY

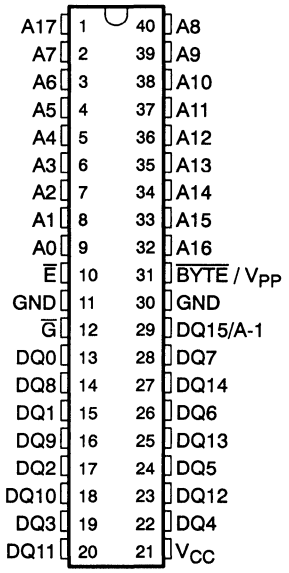
SMLS400A–OCTOBER 1992–REVISED JANUARY 1993

- **Word-Wide (256K × 16) or Byte-Wide (512K × 8) Configurable**
- **4-Megabit Mask ROM Compatible**
  - **40-Lead CERDIP Package**
  - **40-Lead PDIP Package**
- **Single 5-V Power Supply**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

  '27C/PC400-10 100 ns
  '27C/PC400-12 120 ns
  '27C/PC400-15 150 ns
- **Very High Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Guaranteed DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Ranges**

TMS27C400
J AND N PACKAGES
(TOP VIEW)



PIN NOMENCLATURE	
A0–A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
DQ0–DQ14	Inputs (Programming)/Outputs
DQ15/A-1	Input (Programming). Output (Word-Wide Read Mode), Byte Select (Byte-Wide Read Mode)
$\overline{BYTE}$	Word/Byte Enable
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply (Program Mode Only)

ADVANCE INFORMATION

description

The TMS27C400 is a 4 194 304-bit ultraviolet-light erasable, electrically programmable read-only memory, organized as 262 144 words of 16 bits each. A byte enable switch allows the device to be addressed as a 524 288 × 8-bit device. The TMS27C400 is pinout and functionally compatible with 40-pin 4-megabit Mask ROMs.

The TMS27PC400 is a 4 194 304-bit, one-time electrically programmable (OTP) read-only memory, organized as 262 144 words of 16 bits each. A byte enable switch allows the device to be addressed as a 524 288 × 8-bit device. The TMS27PC400 is pinout and functionally compatible with 4-megabit Mask ROMs in a 40-pin dual-in-line plastic package (N suffix).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27C400 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C400 is also offered with two choices of temperature ranges of 0°C to 70°C and – 40°C to 85°C (JL and JE suffixes). The TMS27C400 is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC400 OTP PROM is offered in a 40-pin dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC400 is also offered with two choices of temperature ranges, 0°C to 70°C and – 40°C to 85°C (NL and NE suffixes). The TMS27PC400 is also offered with 168 hour burn-in on both temperature ranges (NL4 and NE4 suffixes). (See table below.)

	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HR. BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
TMS27C400-xx	JL	JE	JL4	JE4
TMS27PC400-xx	NL	NE	NL4	NE4

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

ADVANCE INFORMATION

operation

The following table lists modes of operation for the TMS27C400 and TMS27PC400. The read mode requires a single 5-V supply. All inputs are TTL level except V_{CC}, $\overline{BYTE}$ / V_{PP} during programming (13 V for SNAP! Pulse), and A9 for signature modes (12 V).

MODE	$\overline{E}$	$\overline{G}$	$\overline{BYTE}$ / V_{PP}	V_{CC}	A9	A0	DQ15/A-1	DQ8–DQ14	DQ0–DQ7
Read (Word)	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	X	DQ15	DQ8–DQ14	DQ0–DQ7
Read (Upper Byte)	V_{IL}	V_{IL}	V_{IL}	V_{CC}	X	X	V_{IH}	HI-Z	DQ8–DQ15
Read (Lower Byte)	V_{IL}	V_{IL}	V_{IL}	V_{CC}	X	X	V_{IL}	HI-Z	DQ0–DQ7
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	X	X	HI-Z	HI-Z	HI-Z
Standby	V_{IH}	X†	X	V_{CC}	X	X	HI-Z	HI-Z	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In	Data In	Data In
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z	HI-Z	HI-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	0B	00H	97H
Signature Mode (Dev)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IH}	0B	00H	54H

† All X's can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more TMS27C400s or TMS27PC400s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

word-wide mode

With $\overline{BYTE}$ / V_{PP} at V_{IH}, outputs DQ8–DQ15 present the upper eight bits of data for the address selected, and outputs DQ0–DQ7 present the lower eight bits of data when $\overline{E}$ and $\overline{G}$ are appropriately enabled.

byte-wide mode

With $\overline{BYTE}/V_{PP}$ at V_{IL}, outputs DQ8–DQ14 are disabled. Two selectable bytes of data determined by the logic state on DQ15/A-1 will appear on outputs DQ0–DQ7. When DQ15/A-1=V_{IH}, the upper byte or eight bits of data will appear on outputs DQ0–DQ7. When DQ15/A-1=V_{IL}, the lower byte or eight bits of data will appear on outputs DQ0–DQ7.

latchup immunity

Latchup immunity on the TMS27C400 and TMS27PC400 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C400)

Before programming, theTMS27C400 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W•s/cm^2. A 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C400, the window should be covered with an opaque label.

initializing (TMS27PC400)

The one-time programmable TMS27PC400 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C400 and TMS27PC400 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is $\overline{BYTE}$ / V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, and $\overline{G}$ = V_{IH}. Once the initial location is selected, the data is presented in parallel (16 bits) on pins DQ0–DQ15. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at $\overline{BYTE}$ / V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, and $\overline{G}$ = V_{IL}. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with V_{CC} = $\overline{BYTE}$ / V_{PP} = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining a high level input on $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with $\overline{BYTE}$ / V_{PP} = 13 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

ADVANCE INFORMATION

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 39) is forced to 12 V. Two identifier bytes are accessed by toggling A0. A0 low selects the manufacturer's code (0097 HEX), and A0 high selects the device code (0054 HEX), as shown by the table below. All other addresses must be held low.

IDENTIFIER	A0	DQ8-DQ15	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer's Code	V_{IL}	All 0	H	L	L	H	L	H	H	H	0097
Device Code	V_{IH}	All 0	L	H	L	H	L	H	L	L	0054

NOTE: $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A17 = V_{IL}, $\overline{BYTE}$ / V_{PP} = V_{CC}.

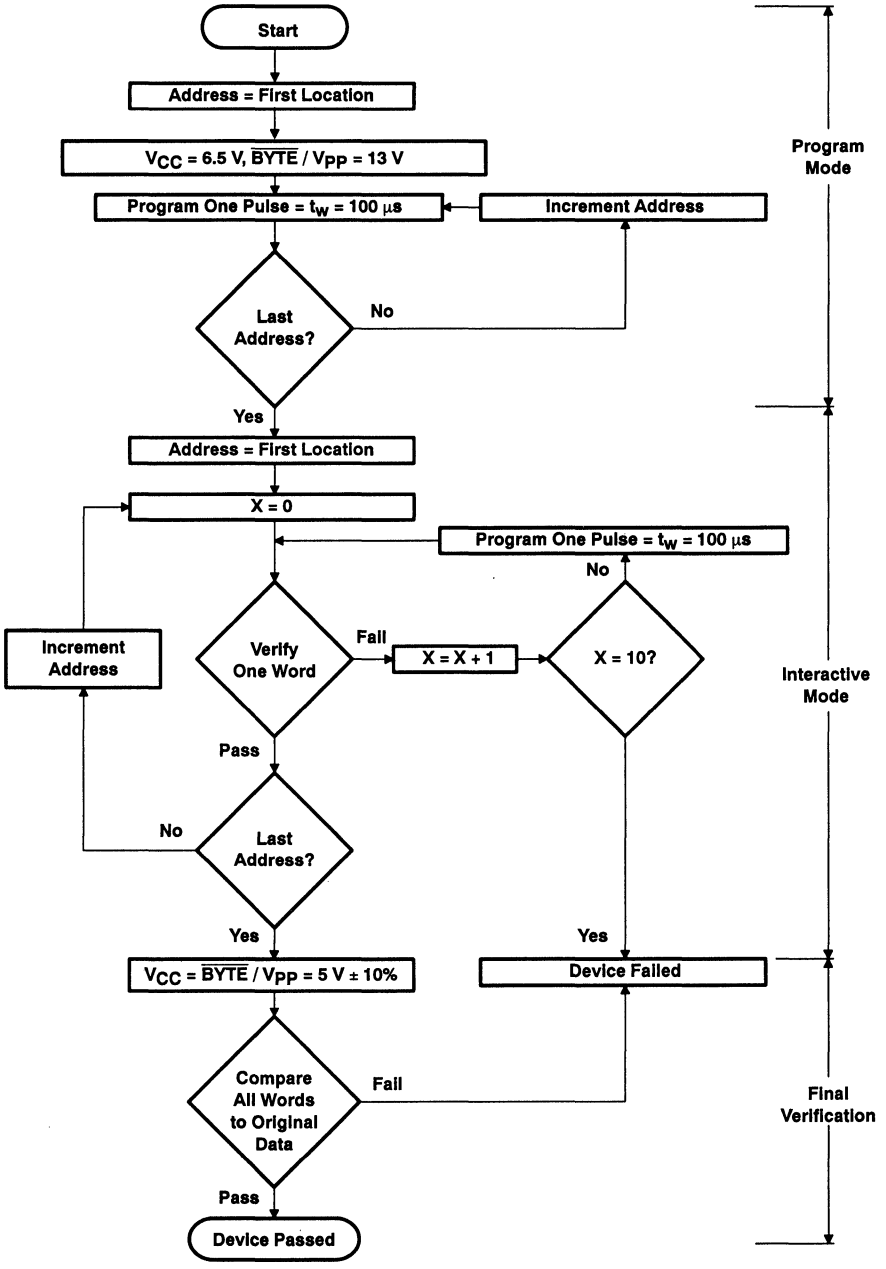
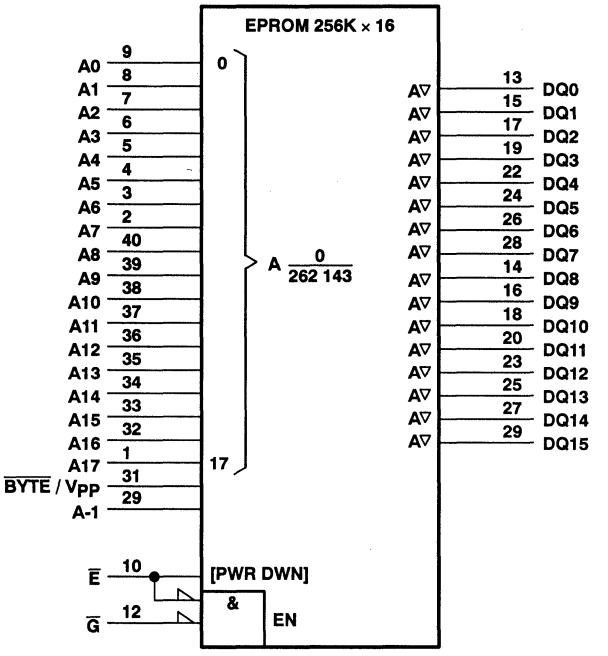


Figure 1. SNAP! Pulse Programming Flowchart

ADVANCE INFORMATION

ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, $\overline{BYTE}$ / V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('27C400_ _JL and JL4, '27PC400_ _NL and NL4) ..... 0°C to 70°C
Operating free-air temperature range ('27C400_ _JE and JE4, '27PC400_ _NE and NE4) ..... −40°C to 85°C
Storage temperature range ..... −65°C to 125°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				TMS27C/PC400-10 TMS27C/PC400-12 TMS27C/PC400-15			UNIT
				MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse Programming algorithm		6.25	6.5	6.75	
BYTE/ V_{PP}	Supply voltage	Read mode (WORD) Read mode (BYTE) (see Note 3)		V_{IH} −0.5		V_{CC} + 0.5 V_{IL}	V
		SNAP! Pulse Programming algorithm		12.75	13	13.25	
V_{IH}	High-level input voltage		TTL	2		V_{CC}+ 0.5	V
			CMOS	V_{CC} − 0.2		V_{CC}+ 0.5	
V_{IL}	Low-level input voltage		TTL	− 0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature		'27C400_ _JL, JL4 '27PC400_ _NL, NL4	0		70	°C
			'27C400_ _JE, JE4 '27PC400_ _NE, NE4	−40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as $\overline{BYTE}$/ V_{PP} and removed after or at the same time as $\overline{BYTE}$ / V_{PP}. The device must not be inserted into or removed from the board when $\overline{BYTE}$ / V_{PP} or V_{CC} is applied.

3. $\overline{BYTE}$ / V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming $\overline{BYTE}$ / V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = − 2.5 mA	2.4		V
			I_{OH} = − 20 µA	V_{CC} − 0.1		
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 µA		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	$\overline{BYTE}$ / V_{PP} operating current		$\overline{BYTE}$ / V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$\overline{BYTE}$ / V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL} t_{cycles} = 5 MHz outputs open		50	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0		4	8	pF
C_O	Output capacitance	V_O = 0		8	12	pF
$C_{BYTE / VPP}$	$\overline{BYTE}$/ V_{PP} capacitance	$\overline{BYTE}$ / V_{PP} = 0		18	25	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

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switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

		TEST CONDITIONS (SEE NOTES 4, 5, & 6)	'27C/PC400-10		'27C/PC400-12		'27C/PC400-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns,		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)
5. Common test conditions apply for t_{dis} except during programming.
6. $t_{a(A)}$ includes access time from DQ15/A-1 in Byte Wide Read Mode.

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switching characteristics for programming: V_{CC} = 6.5 V and $\overline{BYTE}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and $\overline{BYTE}/V_{PP}$ = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	$\overline{BYTE}$ / V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

PARAMETER MEASUREMENT INFORMATION

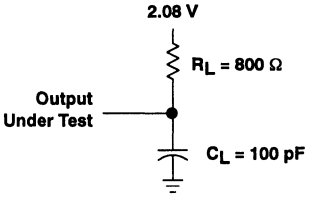
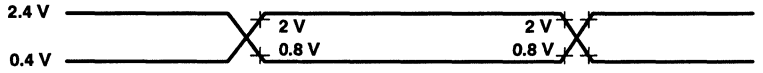


Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

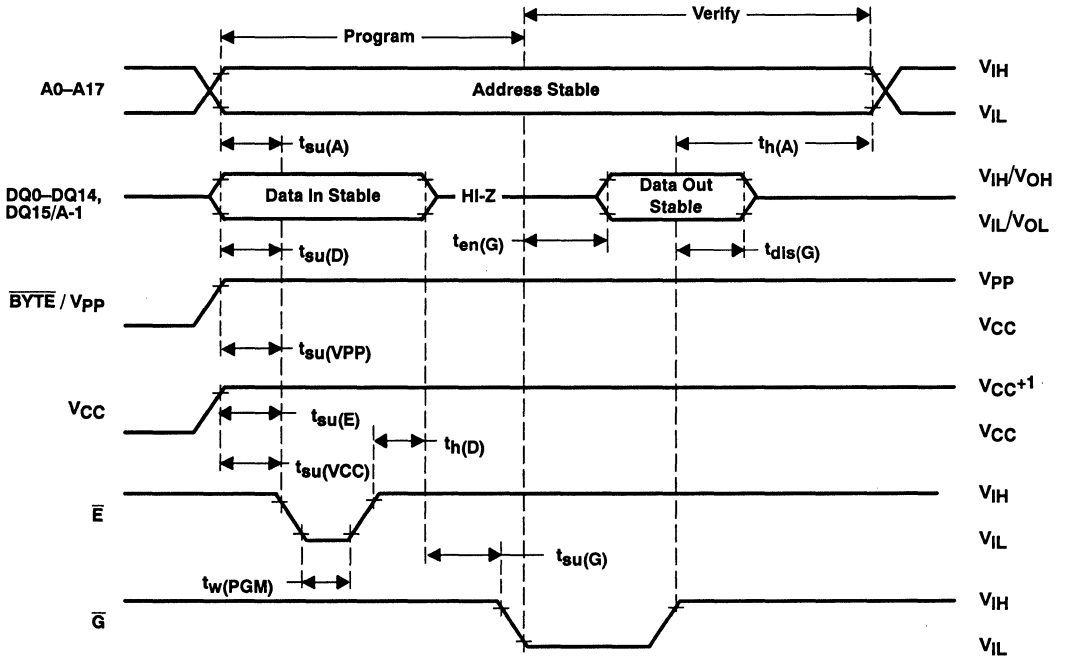
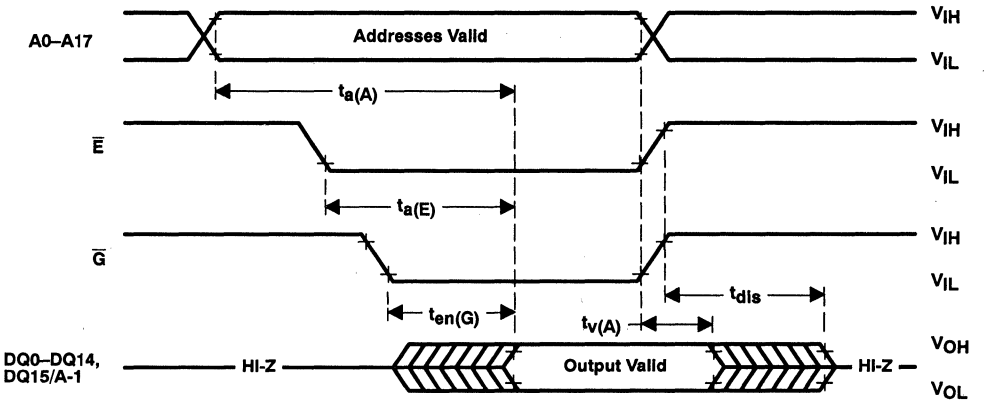


Figure 3. Program Cycle Timing (Snap! Pulse Programming)

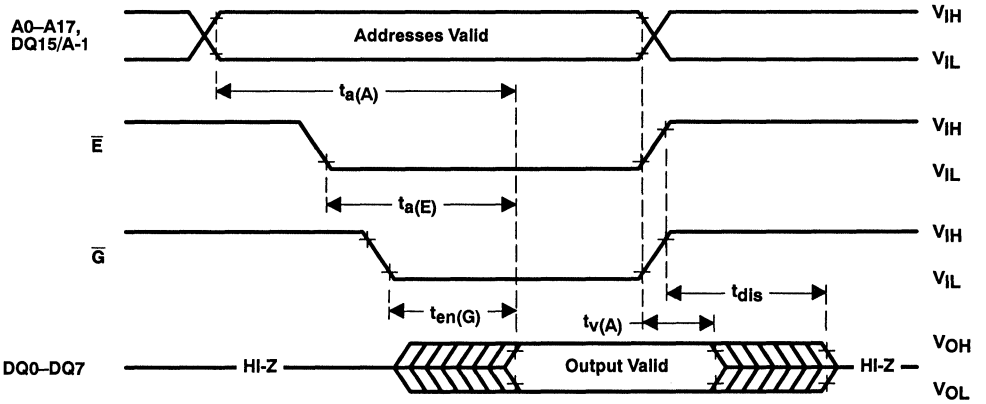
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE: $\overline{BYTE}$ / V_{PP} = V_{IH}

Figure 4. Read Cycle Timing: Word-Wide Read Mode



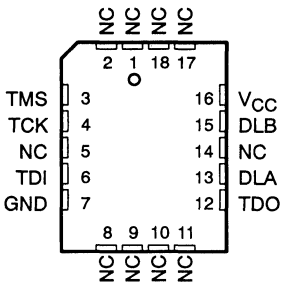
NOTE: $\overline{BYTE}$ / V_{PP} = V_{IL}
DQ8–DQ14 = HI-Z

Figure 5. Read Cycle Timing: Byte-Wide Read Mode

ADVANCE INFORMATION

- **Member of Texas Instruments SCOPE™ Family of Testability Products**
- **IEEE 1149.1 Serial Test Bus Compatible**
- **Organization . . . 2048 x 8-Bit Flash Memory**
- **TCK Frequency (V_{CC} ± 10%)**
  '29F816-06 6.25 MHz
- **5-Volt Program/Erase/Read Operation**
- **4 Flash-Erasable Blocks (128, 384, 512, and 1024-Byte Size)**
- **Software Sequence Write/Erase Protection**
- **Lockbits**
- **Self-Timed Write/Erase Cycles**
- **Streaming Read/Write Modes**
- **32-Byte Page Programming Mode**
- **CMOS Technology**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **18-Pin Plastic Leaded-Chip Carrier Package (FM Suffix)**
- **Operating Free-Air Temperature Range 0°C to 70°C**

FM PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
TMS	Test Mode Select
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
DLA	Disable Lock A
DLB	Disable Lock B
V_{CC}	5-V Power Supply
GND	Ground
NC	No internal connection

description

The SCOPE Diary is a 16 384-bit, programmable storage device that can be electrically block-erased and reprogrammed. The SCOPE Diary is fabricated using HVCMOS FLOTOX technology for high reliability and very low power dissipation. It performs the erase/program operations automatically with a single 5-V supply voltage, and it can program a single byte or up to 32 bytes in one cycle.

All SCOPE Diary operations are accomplished via a 4-wire Test Access Port (TAP) interface. This interface complies with the IEEE 1149.1 Serial Test Bus standard (JTAG). The interface consists of two control signals: Test Mode Select (TMS) and Test Clock (TCK); and two test data pins: Test Data In (TDI) and Test Data Out (TDO). The JTAG Test Access Protocol defines how this 4-wire test bus is used to scan in instructions and data, execute instructions, and scan out the resulting data.

All test information is serially loaded into the chip via TDI and out of the chip via TDO. Three mandatory JTAG components are added to the Flash EEPROM array: a TAP controller, a set of test data registers, and an instruction register.

The TAP controller interfaces both the test data registers and the instruction register to the 4-wire test bus. The test data registers load and/or capture test data. The instruction register selects the test data register(s) to be accessed and the test to be performed. There are three types of test data registers: the Data Scan Registers (DSR), the Bypass Register (BR), and the Device Identification Register (IDR).

SCOPE is a trademark of Texas Instruments Incorporated.

The SCOPE Diary is divided into four independently flash-erasable blocks. These blocks are configured as 128, 384, 512, and 1024 bytes in size. These blocks can be prevented from being programmed or erased by programming any or all of the four write-once lockbits.

The SCOPE Diary features internal circuitry for self-timed programming, self-timed erasing, and completion polling. In the erased state, all bits are at a logical 1. To reprogram, all memory bits in a selected block are erased first, and then those bits (now logical 1s) are programmed accordingly. The SCOPE Diary supports a page programming mode that allows programming of up to 32 bytes in one cycle. During programming and erasing, the completion status is available, allowing the system to begin a new operation before the maximum specified timeout.

An on-chip power supply reference comparator protects the SCOPE Diary from write and erase commands during power up and power down. During normal operation, software sequences protect against inadvertent program and erase commands.

The SCOPE Diary is offered in an 18-pin plastic leaded-chip carrier package (FM suffix). It is characterized for operation from 0°C to 70°C.

The SCOPE Diary is available in a 10,000-cycle endurance version.

terms

clock

The term *clock* refers to the system test clock used by the controller and its target(s). The clock is input on TCK.

DMA

The SCOPE Diary supports the Direct Memory Access (DMA) extension to the 1149.1 standard. The DMA mode enables a continuous stream of bits to be scanned in or out of the SCOPE Diary.

host

The term *host* refers to the device directing the activity of the SCOPE Diary.

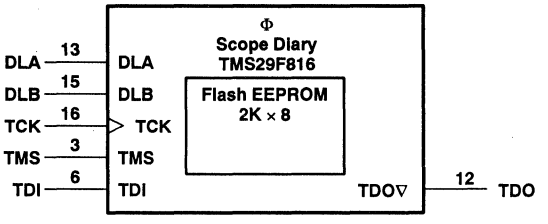
JTAG

The Joint Test Action Group (JTAG) is the originator of IEEE Standard 1149.1.

SCOPE

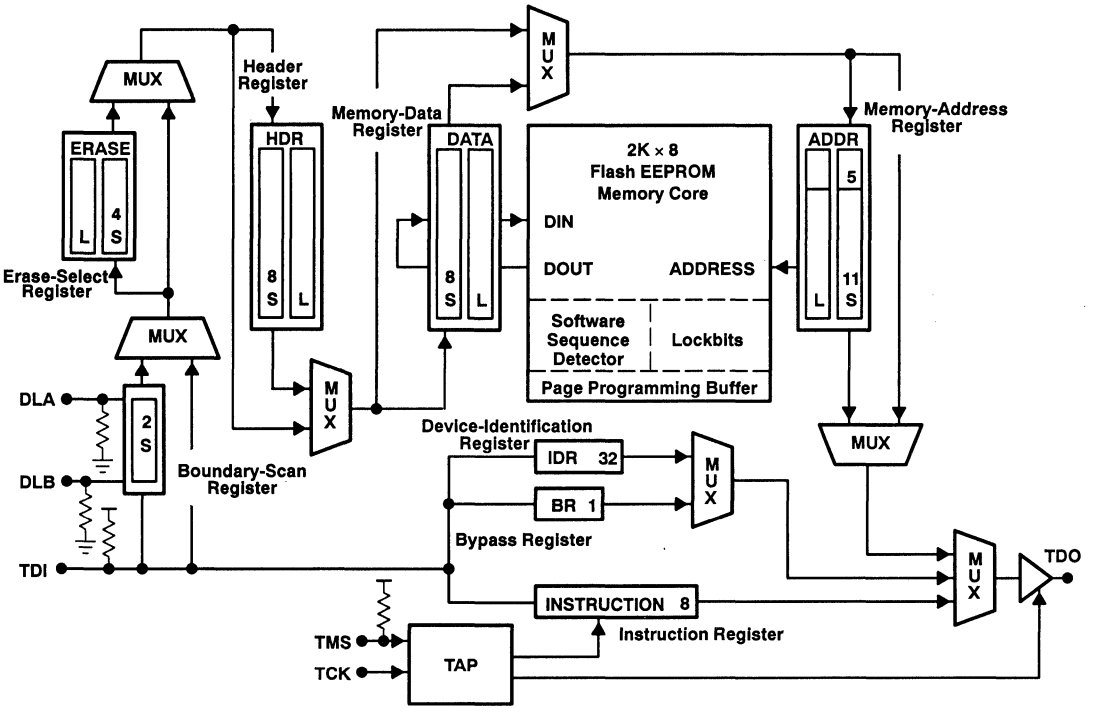
System Controllability and Observability Partitioning Environment (SCOPE) is the family name for Texas Instruments testability products.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12-1991.

functional block diagram



Terminal Functions

PIN NAME	PIN #	I/O	DESCRIPTION
TMS	3	I	Test Mode Select. Controls transition of TAP finite state machine. This input is sampled on the rising edge of TCK.
TCK	4	I	Test Clock. Input clock to TAP finite state machine. All changes in state are synchronous to the test clock TCK.
TDI	6	I	Test Data In. Data input to the internal register scan path. Data on this pin is sampled on the rising edge of TCK.
TDO	12	O	Test Data Out. Data output from the internal register scan path. Data is updated on this pin on the falling edge of TCK.
DLA	13	I	Disable Lock A. Controls lockbit functionality for memory array block 0. When DLA = V_{IL}, the state of lockbit 0 (LCK0) determines whether block 0 can be erased or programmed. When DLA = V_{IH}, block 0 can be erased or programmed regardless of the state of lockbit 0. When DLA = V_H ($V_H >> V_{CC}$), the SCOPE Diary enters a special manufacturing test mode.
DLB	15	I	Disable Lock B. Controls lockbit functionality for memory blocks 1, 2, and 3. When DLB = V_{IL}, the states of lockbits 1, 2, and 3 (LCK1, LCK2, LCK3) determine whether their respective blocks (1, 2, and 3) can be erased or programmed. When DLB = V_{IH}, blocks 1, 2, and 3 can be erased or programmed, regardless of the state of their associated lockbits.
V_{CC}	16	I	5-V Power Supply. (± 10% operating power supply connection.)
GND	7	I	Ground reference

Internal registers

Note that the most significant bit is farthest from the output (TDO) in all internal registers.

instruction

The instruction register is an 8-bit shift register with parallel inputs to monitor the SCOPE Diary status. The most significant bit (7) is a parity bit. The SCOPE Diary status is loaded into the instruction register during the *Capture-IR* controller state (see Figure 1). During the *Shift-IR* state, the status bits are shifted out as a new SCOPE Diary instruction is scanned into the instruction register.

Bit #	7	6	5	4	3	2	1	0
	IRP	P/EBS	SSS	LMS	VMS	P/ECES	0	1
	R-1†	R-0	R-0	R-0	R-0	R-0	R-0	R-1

†R = Read, -n = Value after reset

Bit 0: Always loaded with 1.

Bit 1: Always loaded with 0

Bit 2: **P/ECES – Program/Erase Contention Error Status**
0 = No error detected.
1 = Attempt to write to SCOPE Diary during busy state.

Bit 3: **VMS – Verify Mode Status**
0 = Normal operating mode.
1 = SCOPE Diary is in either program-verify or erase-verify mode.

Bit 4: **LMS – Lock Mode Status**
0 = Normal operating mode.
1 = SCOPE Diary is in lockbit mode.

Bit 5: **SSS – Software Sequence Status**
0 = Normal operating mode.
1 = Valid software sequence detected. The bit will be set within 2 μs after the SCOPE Diary detects a valid software sequence. The bit will remain set until one of the following occurs:
a) The sequence timer expires.
b) The active program or erase cycle is complete.
c) The CLRSWS command is issued.

Bit 6: **P/EBS – Program/Erase Busy Status**
0 = Normal operating mode.
1 = Busy state. The SCOPE Diary is executing a self-timed program or erase operation. The bit will be set within 2 μs after the BEGOPS instruction is executed. This bit will remain set until the operation is complete.

Bit 7: **IRP – Instruction Register Parity**
All valid commands to the instruction register are even parity.
0 = Parity error detected in previously loaded instruction. The SCOPE Diary will automatically place the BYPASS register into the data register scan path.
1 = No parity error in previously loaded instruction.

Figure 1. Instruction Register Status

boundary-scan

The boundary-scan register is a 2-bit register. Bit 0 of this register is connected to DLA; bit 1 is connected to DLB. This register can only be used to sample the connected inputs; therefore, values stored in the boundary-scan register during the *Update-DR* controller state will not be applied to the internal core logic.

device-identification

The device identification register returns the following 32-bit code when interrogated with the IDCODE command: *0000102Fh*. The device ID register is selected into the scan path during power-on reset or upon entering the *Test-Logic-Reset* state.

bypass

The bypass register is a 1-bit register. It allows data to transfer from TDI to TDO in one TCK clock cycle. The bypass register is selected into the scan path when a parity error is detected during the *Shift-IR* state.

memory-data

The memory-data register is an 8-bit register used to load data into the memory array during write operations. This register is also used to sample data from the memory array during read operations. The parallel-scan load path is connected to the memory core data outputs. The output of the register latch is connected to the data input of the memory core. The operation of the register is shown in Table 1.

Table 1. Memory-Data Register Operation

Opcode	Capture-DR	Shift-DR	Update-DR
DMARD	Memory Data to Scan	Data Stream from Array	Scan to Register Latch
DMAWR	Memory Data to Scan	Data Stream to Array	Scan to Register Latch
BYTERD	Memory Data to Scan	Normal Shift Operation	Scan to Register Latch
BYTEWR	Memory Data to Scan	Normal Shift Operation	Scan to Register Latch
ISTEST	Register Latch to Scan	Normal Shift Operation	Scan to Register Latch

memory-address

The memory-address register is a 16-bit register used to address the Flash EEPROM array during read and write operations. Bits 10 – 0 are used to address the Flash memory array. Bits 14 – 0 are used to address the software sequence detector. The operation of the register is shown in Table 2.

Table 2. Memory-Address Register Operation

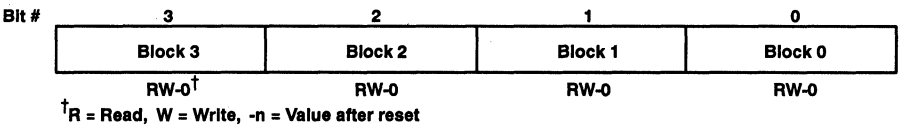
Opcode	Capture-DR	Shift-DR	Update-DR
LDADDR	Register Latch to Scan	Normal Operation	Scan to Register Latch
DMARD	Hold	Auto-Increment	Hold
DMAWR	Hold	Data Stream to Array	Hold
BYTERD	Register Latch to Scan	Normal Operation	Scan to Register Latch
BYTEWR	Register Latch to Scan	Normal Operation	Scan to Register Latch
ISTEST	Register Latch to Scan	Normal Operation	Scan to Register Latch

page programming buffer

The programming pages begin on 32-byte boundaries. Data being written to the SCOPE Diary is stored in the 32-byte page programming buffer until the memory-array programming cycle begins. The page buffer address mechanism does not automatically recognize page programming buffer loads that cross a page boundary. Bits 10 – 5 of the last address presented to the page programming buffer will be used as the page pointer when the memory array programming cycle begins. After an initial data value is loaded into the page programming buffer, all remaining bytes within the page programming buffer are initialized to FFh.

erase-select

The erase-select register is a 4-bit register used to select the Flash memory block(s) that will be erased during an erase cycle. Each bit in the register maps to one of the memory blocks (see Figure 2). To select a block for erasure, set the block's corresponding memory-control bit to logic 1. The operation of the register is shown in Table 3.



Bit 0: **Block 0 Erase Enable (address 0000 – 007F)**
0 = Erase disable
1 = Erase enable

Bit 1: **Block 1 Erase Enable (address 0080 – 01FF)**
0 = Erase disable
1 = Erase enable

Bit 2: **Block 2 Erase Enable (address 0200 – 03FF)**
0 = Erase disable
1 = Erase enable

Bit 3: **Block 3 Erase Enable (address 0400 – 07FF)**
0 = Erase disable
1 = Erase enable

Figure 2. Erase-Select Register

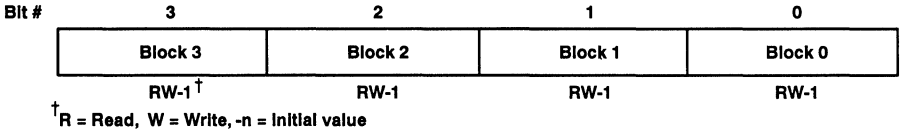
Table 3. Erase-Select Register Operation

Opcode	Capture-DR	Update-DR
ERABLK	Register Latch to Scan	Scan to Register Latch
ISTEST	Register Latch to Scan	Scan to Register Latch

lockbits

The lockbit register contains *four one-time-programmable, non-erasable bits.* The lockbits map one-to-one to the blocks in the array (bit 0 maps to block 0). The lockbit register is not located on the scan path; it is internal to the memory core. It can be accessed using the memory-address and memory-data registers.

To prevent a block from being programmed or erased, program a logic 0 in the block's corresponding bit position. Read and write operations to the lockbits are selected by the SETLOCK instruction. To program the lockbits, execute the DMAWR or BYTEWR instruction sequences while in the lock mode. The lockbit register is shown in Figure 3.



Bit 0: **Block 0 Lock Enable (address 0000 – 007F)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 1: **Block 1 Lock Enable (address 0080 – 01FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 2: **Block 2 Lock Enable (address 0200 – 03FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 3: **Block 3 Lock Enable (address 0400 – 07FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Figure 3. Lockbit Register

header

The header register is an 8-bit register used to control the mode of operation during a DMAWR instruction. The register is cleared to zero on power up and upon entering the *Test-Logic-Reset* state. When the register is cleared (all bits to logic 0), the SCOPE Diary uses a state-transition mode to synchronize the DMA write operation. If the register is not cleared, the contents will be used as a shift data input pattern match to synchronize the start of the DMA write operation.

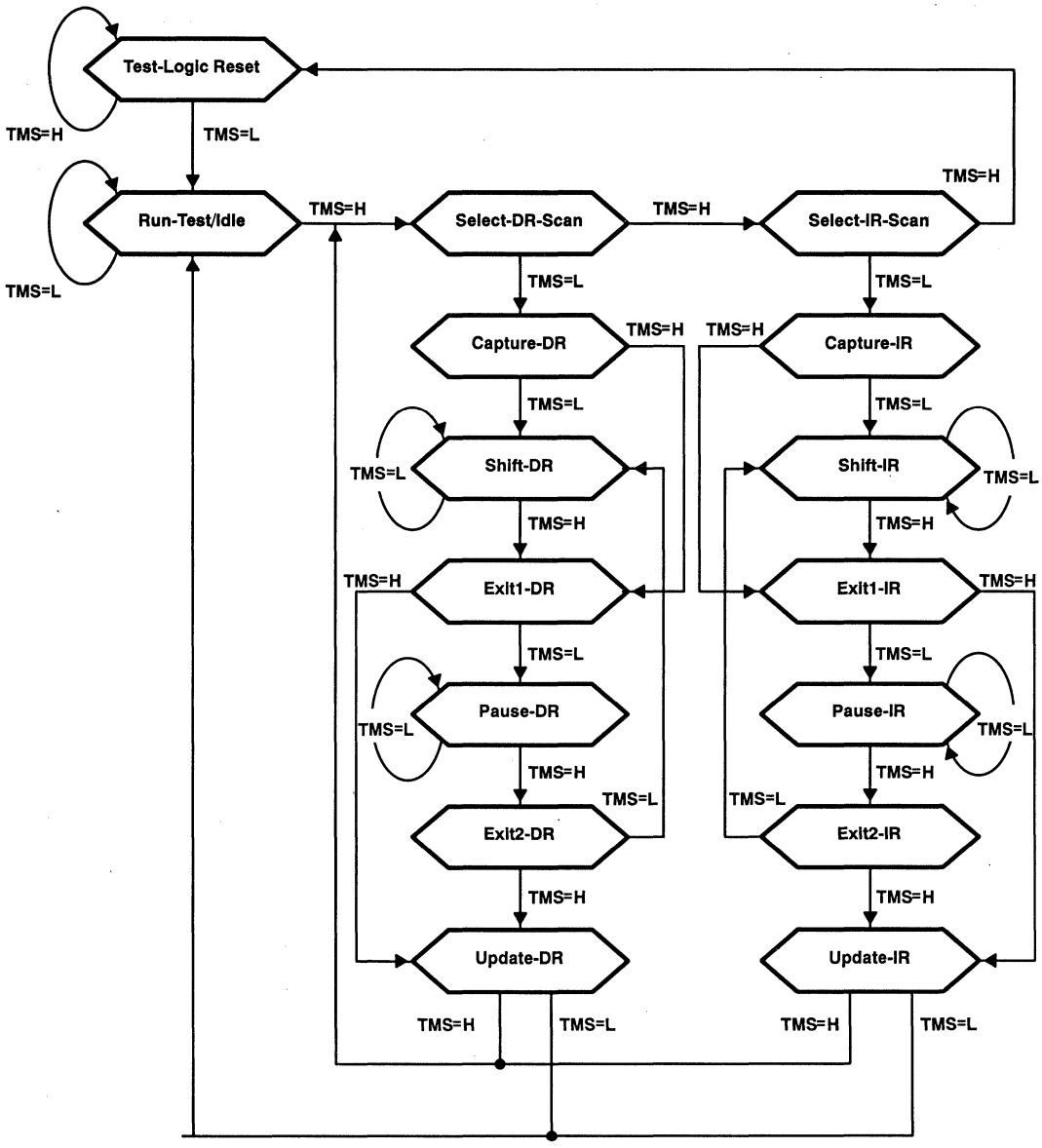


Figure 4. TAP State Diagram

TAP state diagram description (see Figure 4)

The SCOPE Diary TAP controller accepts TCK and TMS signals compatible with IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten transient states (indicated by two exiting arrows) in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any other state is a transient state.

There are two main paths through the state diagram; one accesses selected data registers, and one accesses the instruction register.

Test-Logic-Reset

In this state, the test logic is inactive, and an internal reset signal is applied to all registers in the SCOPE Diary. During SCOPE Diary operation, the TAP returns to the *Test-Logic-Reset* state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level when it is left unconnected or when a board defect causes it to be open-circuited.

Run-Test/Idle

The TAP *must* pass through this state before executing any test operations. The TAP may retain this state indefinitely. No registers are modified while the SCOPE Diary is in the *Run-Test/Idle* state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states. TAP exits them on the next TCK cycle.

Capture-DR

Selected data registers are placed in the scan path (between TDI and TDO). The current instruction determines whether or not the data is loaded or captured into the scan path. The TAP exits the state on the rising edge of TCK.

Shift-DR

In this state, data is shifted serially through the selected data registers, from TDI to TDO, on each TCK cycle. The first shift occurs after the first TCK cycle after entering this state. (No shifting occurs during the TCK cycle in which the TAP changes from *Capture-DR* to *Shift-DR* or from *Exit2-DR* to *Shift-DR*.)

In *Shift-DR*, on the falling edge of TCK, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the *Test-Logic-Reset* state since the last scan operation, TDO enables to the level present before it was last disabled. If the TAP has passed through the *Test-Logic-Reset* state since the last operation, TDO enables to a high level.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the *Shift-DR* state from either *Exit1-DR* or *Exit2-DR* without recapturing the data registers. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from *Shift-DR* to *Exit1-DR*.

Pause-DR

The TAP can remain in this state indefinitely. The *Pause-DR* state allows you to suspend and resume shift operations without losing data.

Update-DR

In the *Update-DR* state, the current instruction determines whether or not the latches in the selected data registers are updated with data from the scan path.

TAP state diagram description (continued)

Capture-IR

In the *Capture-IR* state, the instruction register is preloaded with the IR status word, and then it is placed in the scan path. The TAP exits the state on the rising edge of TCK.

Shift-IR

In this state, data is shifted serially through the instruction register, from TDI to TDO, on each TCK cycle. The first shift occurs after the first TCK cycle after entering this state. (No shifting occurs during the TCK cycle in which the TAP changes from *Capture-IR* to *Shift-IR* or from *Exit2-IR* to *Shift-IR*.) In *Shift-IR*, on the falling edge of TCK, TDO goes from the high-impedance state to the active state.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the *Shift-IR* state from either *Exit1-IR* or *Exit2-IR* without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from *Shift-IR* to *Exit1-IR*.

Pause-IR

The TAP can remain in this state indefinitely. The *Pause-IR* state allows you to suspend and resume shift operations without losing data.

Update-IR

In the *Update-IR* state, the instruction register latches are updated with the new instruction from the scan path.

instructions

standard SCOPE instructions

The SCOPE Diary supports a subset of the standard SCOPE instruction set. The defined instructions are shown in Table 4. All other SCOPE instructions select the default BYPASS instruction.

Table 4. Standard SCOPE Instructions

Opcode	Code	Description
BYPASS	FFh	Select Bypass Register
EXTEST	00h	External Boundary Test (see Note 1)
IDCODE	81h	ID Register Scan
SAMPLE	82h	Boundary Sample

NOTE 1: During operation, the EXTEST instruction behaves identically to the SAMPLE instruction.

SCOPE Diary-specific instructions

The SCOPE Diary supports specific instructions to control the operation of the Flash EEPROM array. The defined instructions are shown in Table 5. All undefined opcodes select the BYPASS instruction.

Table 5. SCOPE Diary-Specific Instructions

Opcode	Code	Description
BEGOPS	69h	Begin Operation in Progress
BYTERD	63h	Byte Read
BYTEWR	E4h	Byte Write
CLRERR	6Ah	Clear Conflict Error Flag
CLRLOCK	66h	Exit Lock Mode
CLRSWS	EBh	Clear Software Sequence
DMARD	E1h	DMA Read
DMAWR	E2h	DMA Write
ERABLK	E7h	Erase Block Register Select
ISTEST	6Ch	Internal Self Test
LDADDR	60h	Load Address Register
LOADHDR	E8h	Header Register Select
SETLOCK	65h	Enter Lock Mode

BEGOPS Begin Operation in Progress

Scan Path TDI → bypass → TDO

Description The BEGOPS instruction is used to initiate a program, erase, or verify mode operation after the appropriate software sequence has been issued. This instruction must be executed within 9 ms of the last write operation, and the software sequence status bit in the instruction register must be set, or the selected operation will not begin. If the time-out condition is not met, the software sequence commands must be re-issued. Once the BEGOPS instruction is loaded, it is not executed until the diary is placed in the *Run-Test/Idle* state.

BYPASS Select Bypass Register

Scan Path TDI → bypass → TDO

Description The BYPASS instruction conforms to the 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register during the *Update-DR* state.

BYTERD Byte Read

Scan Path TDI → memory-data → memory-address → TDO

Description The BYTERD instruction is used to read the value stored in a memory array location. During the read operation, the contents of the memory-address register point to the value. This value is captured in the memory-data register during the *Update-DR* state.

BYTEWR Byte Write

Scan Path TDI → memory-data → memory-address → TDO

Description The BYTEWR instruction performs two operations. It can write 8-bit values into both the software sequence detector and the page programming buffer. The contents of the memory-address register and the contents of the memory-data register are presented to the memory core during the *Update-DR* state. On the rising edge of TCK, upon leaving the *Update-DR* state, an internal write signal is applied to either the software sequence detector or the page programming buffer.

CLRERR Clear Conflict Error Flag

Scan Path TDI → bypass → TDO

Description The CLRERR instruction is used to reset the program/erase conflict flag. The conflict flag (status bit 2 in the instruction register) will be set if any write operations are issued while the SCOPE Diary is programming or erasing. After the conflict flag is set, the SCOPE Diary won't recognize any sequence commands. The conflict flag will remain set until the CLRERR instruction is executed.

CLRLOCK Exit Lock Mode

Scan Path TDI → bypass → TDO

Description The CLRLOCK instruction is used to exit the lock mode. When the lock mode is disabled, all read and programming operations are directed to the memory array. The normal mode is indicated when status bit 4 is cleared in the instruction register.

CLRSWS Clear Software Sequence

Scan Path TDI → bypass → TDO

Description The CLRSWS instruction is used to clear software sequence operations. The instruction will reset or cancel any software sequence up until the BEGOPS instruction is executed. The CLRSWS instruction will also clear status bit 5 (valid software sequence detected) in the instruction register. The CLRSWS instruction will not interrupt an erase or program operation once the operation has started.

DMARD DMA Read

Scan Path TDI → (ignored) / memory-data → TDO

Description The DMARD instruction is used to perform streaming data reads from the Flash EEPROM memory array. During the read operation, upon entering the *Shift-DR* state, the contents of the memory array will be shifted out beginning with the currently addressed location. The memory-address register is automatically incremented on each byte boundary while performing the DMARD operation. Input data on the TDI pin is discarded and does not pass through to the TDO output pin.

DMAWR DMA Write

Scan Path TDI → memory-data → memory-address → TDO

Description The DMAWR instruction allows a streaming method of writing address/data pairs to the SCOPE Diary. During the *Shift-DR* state, the SCOPE Diary will automatically generate write strobes to the memory core on each 24-bit address/data pair boundary. The SCOPE Diary supports two modes of synchronizing the write operation with the incoming address/data pairs; state-transition mode and stream-header mode. The contents of the header register determine the selected mode.

ERABLK Erase Block Register Select

Scan Path TDI → erase-block → TDO

Description The ERABLK instruction is used to access the erase-block select register. Data loaded into the ERABLK register is presented to the memory core during the *Update-DR* state.

EXTEST External Boundary Test

Scan Test TDI → boundary-scan → TDO

Description The EXTEST instruction is used to check the board connectivity of the DLA and DLB input pins. During an EXTEST operation, DLA and DLB inputs to the internal control logic can be sampled by the scan path, but not driven.

IDCODE ID Register Scan

Scan Path TDI → id → TDO

Description The IDCODE instruction is used to read the device identification data. During the *Capture-DR* state, the 32-bit device identification code (0000102Fh) is loaded into the ID register. The IDCODE instruction is automatically loaded during SCOPE Diary power-on reset or upon entry to the *Test-Logic-Reset* state.

ISTEST Internal Self Test

Scan Path TDI → boundary-scan → erase-block → header → memory-data → memory-address → TDO

Description The ISTEST instruction is used to test scan path data registers. During the *Capture-DR* state, all of the register latched values are transferred to the scan path (except the boundary scan register which transfers the values of DLA and DLB to the scan path).

LDADDR Load Address Register

Scan Path TDI → memory-address → TDO

Description The LDADDR instruction is used to load the memory-address register. The 16-bit value loaded from the scan path points to an address and is presented to the memory array during the *Update-DR* state.

LOADHDR Header Register Select

Scan Path TDI → header → TDO

Description The LOADHDR instruction is used to access the header register. Loading any value from 01h to FFh selects header mode synchronization during DMA write operations. Loading the header register with 00h selects state-transition mode synchronization for DMA write operations. During the LOADHDR operation, the header register is selected into the DR scan path.

SAMPLE Boundary Sample

Scan Path TDI → boundary-scan → TDO

Description The SAMPLE instruction is used to check the board connectivity of the DLA and DLB input pins. During a SAMPLE operation, DLA and DLB inputs to the internal control logic can be sampled by the scan path, but not driven.

SETLOCK Enter Lock Mode

Scan Path TDI → bypass → TDO

Description The SETLOCK instruction is used to enable the lock mode. When the lock mode is enabled, read and programming operations are directed to the lockbits. The lock mode operation is indicated when status bit 4 is set in the instruction register. The SCOPE Diary will remain in the lock mode until the CLRLOCK instruction is executed. While in the lock mode, all read operations capture the state of the lockbits in the data-memory register. While reading the lockbits, the four most significant bits are set to logic 1.

operation

TAP state controller

Operation of the TAP state controller conforms to the IEEE 1149.1 Serial Test Bus standard. The state flow diagram is shown in Figure 4 on page 8.

loading and executing instructions

All bus sequences that load and execute instructions start with the TAP in the *Run-Test/Idle* state. To initialize the TAP to *Run-Test/Idle* from any other state, apply the 6-cycle sequence shown in Table 6.

Table 6. TAP Reset Sequence

Cycle	1	2	3	4	5	6
TMS	1	1	1	1	1	0
TCK						
TDI†	X	X	X	X	X	X
TDO	(See Note 2)	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
TAP State	Undefined	Undefined	Undefined	Undefined	Test-Logic-Reset	Run-Test/Idle

† X denotes a don't care.

NOTE 2: TDO will become high-impedance on falling edge of TCK.

sequence timing

The SCOPE Diary contains internal timing logic to simplify programming and erase operations. Once the host initiates a programming or erasing operation, that operation will automatically continue to completion. The host does not need to intervene until the operation is finished. To check the status of the operation, poll status bit 6 of the instruction register.

software sequence

The host initiates all of the SCOPE Diary's internal memory operations by issuing a sequence of address/data pairs (forming a specific software sequence) to the SCOPE Diary. The correct address/data pairs must be received in a specific order and within a specific time period to be recognized as a valid software sequence by the SCOPE Diary. Once a sequence has begun, the SCOPE Diary starts an internal sequence timer. Each consecutive address/data pair must be received within a 9 ms time period. After each address/data pair, the timer is reset to receive the next sequence pair. If the time between consecutive address/data pairs exceeds the timer limit, the internal state of the sequence detector will be reset, and the host must re-issue the software sequence from the beginning. If the SCOPE Diary detects a valid software sequence, status bit 5 of the instruction register will be set within 2 μs and will remain set as long as the SCOPE Diary is unlocked for the operation. The host may terminate a software sequence at any point by either letting the internal time limit expire, or by issuing a CLRSWS command. The software sequences recognized by the SCOPE Diary are shown in Table 7.

Table 7. SCOPE Diary Software Sequences

Operation	Address/Data Pair Sequence
Programming	5555h / AAh 2AAAh / 55h 5555h / A0h
Erasing	5555h / AAh 2AAAh / 55h 5555h / 80h 5555h / AAh 2AAAh / 55h 5555h / 10h
Program-Verify	5555h / AAh 2AAAh / 55h 5555h / B0h
Erase-Verify	5555h / AAh 2AAAh / 55h 5555h / D0h
Exit-Verify	5555h / AAh 2AAAh / 55h 5555h / F0h

page programming buffer

The page programming buffer is a 32-byte buffer that the host loads with the data to be programmed into the memory array. This buffer is internal to memory and can be accessed using the memory-address and memory-data registers. The page programming buffer is automatically selected by internal control logic after it detects a valid program software sequence. The contents of this buffer are automatically set to FFh, so any bits not specifically cleared by the host will not be programmed. Up to 32 bytes can be programmed in one cycle.

Address/data pairs must be loaded into the page programming buffer within the same time constraints as the software sequence. If the sequence timer is allowed to expire during a page programming buffer load, the internal control logic will terminate the programming operation and clear the software sequence detector (indicated by status bit 5 in the instruction register). During a programming operation, data that has been loaded into the internal page programming buffer is automatically transferred into the memory array.

operation initiation

The SCOPE Diary differs from typical software sequence-controlled memory devices because the selected programming or erasing operation does not automatically begin at the end of the internal sequence time out. To initiate the selected operation, the host must issue the BEGOPS command to the SCOPE Diary and enter the *Run-Test/Idle* state before the internal sequence timer expires. If the timer expires, the internal sequence detector will be cleared, and the selected operation must be re-initiated from the beginning. Status bit 6 in the instruction register indicates a successful program or erase operation. This bit will be set within 2 μs after the BEGOPS instruction is executed.

reset

The SCOPE Diary test bus logic is cleared either by internal circuitry at power-up, or by entry to the *Test-Logic-Reset* state. All internal data scan path registers are set to logic 0, and the instruction register is loaded with the IDCODE instruction. Entering the *Test-Logic-Reset* state will not clear a pending software sequence or interrupt an executing self-timed program or erase cycle.

erase-verify mode

The erase-verify mode allows the host to verify the adequacy of erasure. Once the SCOPE Diary has been placed in the verify mode, it will remain in that state (indicated in the instruction register when status bit 3 is a logical 1) until the exit-verify mode sequence has been issued. When in the erase-verify mode, the internal voltage applied to the read select lines (wordlines) is reduced by a preset margin. To verify that the array has been erased, the host reads the memory block and checks that all bits are set to logic 1.

program-verify mode

The program-verify mode allows the host to verify the adequacy of programming. Once the SCOPE Diary has been placed in the program-verify mode, it will remain in this state (indicated in the instruction register when status bit 3 is a logical 1) until the exit-verify mode sequence has been issued. When in the program-verify mode, the internal voltage applied to the read-select lines (wordlines) is increased by a preset margin. To verify that a programming operation was successful, the host reads the previously programmed locations and checks that the data values are correct.

JTAG extensions

DMA read

The DMA read mode allows any number of sequential bits to be read from the SCOPE Diary while remaining in the *Shift-DR* state. During a DMA read operation, the contents of the memory array will be shifted out beginning with the address location contained in the memory-address register. Upon entry to the *Shift-DR* state, an internal modulo 8 counter is triggered. This counter is used to increment the contents of the memory-address register on byte boundaries. After the data from the last byte in the memory array has been read, the next data will be read from the byte at the beginning of the memory array.

DMA write

The DMA write mode simplifies data transfer to the SCOPE Diary. This mode allows data to be continuously streamed into the SCOPE Diary while remaining in the *Shift-DR* state. Compared to normal modes of data transfer, the DMA write extensions enable systems with a large number of devices in the scan path to realize a significant reduction of clock cycles.

In the DMA write mode, an internal modulo 24 counter is used to automatically transfer address/data pairs to the memory core while bypassing the *Update-DR* state. To initiate a DMA write data transfer, the internal modulo 24 counter must be triggered (synchronized) when the first bit of an address/data pair is at the TDI input pin. The SCOPE Diary supports two methods of DMA synchronization: state-transition mode and header mode. The host determines which method of DMA synchronization is used.

state-transition mode

The host selects state-transition mode by clearing the header register (all bits to logic 0). When the state-transition mode is selected, incoming scan path data is ignored during first entry to the *Shift-DR* state. The first entry to *Pause-DR* indicates proper alignment at the TDI input pin of the first address/data pair. Re-entry to the *Shift-DR* state triggers the modulo 24 counter and enables the address/data pair to be written to the memory core. Address/data pairs can then be streamed continuously to the SCOPE Diary with internal transfers occurring automatically on 24-bit boundaries.

header mode

The host selects the header mode by loading the header register with a value from 01h to FFh. When the header mode is selected, incoming scan path data is ignored until a byte (matching the contents of the header register) arrives indicating the arrival of valid address/data pairs. When this header byte is detected, the internal modulo 24 counter is triggered. Address/data pairs can then be streamed continuously to the SCOPE Diary with internal transfers occurring automatically on 24-bit boundaries.

In either state-transition or header mode, the host places the SCOPE Diary in the *Update-DR* state to end a DMA write operation. Because placing the SCOPE Diary in the *Update-DR* state ends the operation, the host must *never* place the SCOPE Diary in this state until the DMA write operation is complete. The host may place the SCOPE Diary in the *Pause-DR* state at any time.

operation examples

Note that in this section, the letter "n" denotes a value from 0h to Fh, and the letter "x" denotes a don't care.

reading examples

reading using the byte mode

Step 1. Load the BYTERD instruction.
Step 2. Scan in 16-bit address = *nnnn* and 8-bit data = *xx.*
Step 3. Scan out 16-bit address = *nnnn* and 8-bit data = *nn.*

reading using the DMA mode

Step 1. Load the LDADDR instruction.
Step 2. Scan in 16-bit address = *nnnn.*
Step 3. Load the DMARD instruction.
Step 4. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values, the address register is automatically incremented on byte boundaries.

lockbit examples

reading lockbits using the byte mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the BYTERD instruction.
Step 3. Scan in 16-bit address = 0000 and 8-bit data = *xx.*
Step 4. Scan out 16-bit address = 0000 and 8-bit data = F*n.*
Step 5. Load the CLRLOCK instruction.

reading lockbits using the DMA mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the DMARD instruction.
Step 3. Scan out the 8-bit lock value = F*n.*
Step 4. Load the CLRLOCK instruction.

programming lockbits using the byte mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the BYTEWR instruction.
Step 3. Scan in address = 5555 and data = AA, go to *Run-Test/Idle.*
Step 4. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 5. Scan in address 5555 and data = A0; go to *Run-Test/Idle.*
Step 6. Scan in address = 0000, and data = F*n*; go to *Run-Test/Idle.*
Step 7. Load the BEGOPS instruction; go to *Run-Test/Idle.*
Step 8. Load the CLRLOCK instruction.

programming lockbits using the DMA mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the DMAWR instruction.
Step 3. Synchronize SCOPE Diary using either state-transition mode or header mode.
Step 4. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 5. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 6. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 7. Continue looping in *Shift-DR* to scan in address = 0000 and data = F*n*.
Step 8. Load the BEGOPS instruction; go to *Run-Test/Idle*.
Step 9. Load the CLRLOCK instruction.

flash erase examples

erasing a block using the byte mode

Step 1. Load the ERABLK instruction.
Step 2. Scan in the 4-bit erase-block-select value = *n*.
Step 3. Load the BYTEWR instruction.
Step 4. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 5. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 6. Scan in address = 5555 and data = 80; go to *Run-Test/Idle*.
Step 7. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 8. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 9. Scan in address = 5555 and data = 10; go to *Run-Test/Idle*.
Step 10. Poll the SCOPE Diary until valid sequence is detected.
Step 11. Load the BEGOPS instruction; go to *Run-Test/Idle*.

erasing a block using the DMA mode

Step 1. Load the ERABLK instruction.
Step 2. Scan in the 4-bit erase-block-select value = *n*.
Step 3. Load the DMAWR instruction.
Step 4. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 5. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 6. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 7. Continue looping in *Shift-DR* to scan in address = 5555 and data = 80.
Step 8. Continue looping in *Shift-DR* to scan in address = 5555 and data = AA.
Step 9. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 10. Continue looping in *Shift-DR* to scan in address = 5555 and data = 10.
Step 11. Poll SCOPE Diary until valid sequence is detected.
Step 12. Load the BEGOPS instruction; go to *Run-Test/Idle*.

verifying block erasure using the byte mode

select the erase-verify mode:

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = D0; go to *Run-Test/Idle*.

read out the erased block:

Step 5. Load the BYTERD instruction.
Step 6. Scan in 16-bit address = *nnnn* and 8-bit data = *xx*.
Step 7. Scan out 16-bit address = *nnnn* and 8-bit data = FF; at the same time, scan in 16-bit address = *nnnn*+1 and data = *xx*.
Step 8. Repeat Step 7 until entire block is read. All bits will be a logic 1 if the block is properly erased.

exit the erase-verify mode:

Step 9. Load the BYTEWR instruction.
Step 10. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 11. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 12. Scan in address = 5555 and data = F0; go to *Run-Test/Idle*.

verifying block erasure using the DMA mode

select the erase-verify mode:

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = D0.

read out the erased block:

Step 6. Load the LDADDR instruction.
Step 7. Scan in 16-bit data starting address = *nnnn* of the block you want to verify.
Step 8. Load the DMARD instruction.
Step 9. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values from the addressed block. All bits will be a logic 1 if the block is properly erased.

exit the erase-verify mode:

Step 10. Load the DMAWR instruction.
Step 11. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 12. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 13. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 14. Continue looping in *Shift-DR* to scan in address = 5555 and data = F0.

verifying programming using the byte mode

select the program-verify mode:

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = B0; go to *Run-Test/Idle*.

read out the programmed data:

Step 5. Load the BYTERD instruction.
Step 6. Scan in 16-bit address = *nnnn* and 8-bit data = *xx*.
Step 7. Scan out 16-bit address = *nnnn* and 8-bit data = *nn*; at the same time, scan in 16-bit address=*nnnn* + 1 and data = *xx*.
Step 8. Repeat Step 7 until desired memory locations are read and verified.

exit the program-verify mode

Step 9. Load the BYTEWR instruction.
Step 10. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 11. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 12. Scan in address = 5555 and data = F0; go to *Run-Test/Idle*.

verifying programming using the DMA mode

select the program-verify mode:

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = B0.

read out the programmed data:

Step 6. Load the LDADDR instruction.
Step 7. Scan in 16-bit starting address = *nnnn* of the data you want to verify.
Step 8. Load the DMARD instruction.
Step 9. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values starting from the addressed location. Verify that the output data stream matches the programmed data.

exit the program-verify mode:

Step 10. Load the DMAWR instruction.
Step 11. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 12. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 13. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 14. Continue looping in *Shift-DR* to scan in address = 5555 and data = F0.

programming examples

programming a single byte using the byte mode

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 4. Scan in address = 5555 and data = A0; go to *Run-Test/Idle.*
Step 5. Scan in address = *nnnn* and data = *nn*; go to *Run-Test/Idle.*
Step 6. Load the BEGOPS instruction; go to *Run-Test/Idle.*

programming a single byte using the DMA mode

Step 7. Load the DMAWR instruction.
Step 8. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 9. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 10. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 11. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 12. Continue looping in *Shift-DR* to scan in address = *nnnn* and data = *nn.*
Step 13. Load the BEGOPS instruction; go to *Run-Test/Idle.*

programming a page using the byte mode

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle.*
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle.*
Step 4. Scan in address = 5555 and data = A0; go to *Run-Test/Idle.*
Step 5. Scan in address = *nnnn* and data = *nn*; go to *Run-Test/Idle.*
Step 6. Go to Step 5 while there are address/data pairs to load within the 32-byte page.
Step 7. Load the BEGOPS instruction, go to *Run-Test/Idle.*

programming a page using the DMA mode

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 6. Continue looping in *Shift-DR* to scan in address = *nnnn* and data = *nn*.
Step 7. Go to Step 6 while there are address/data pairs to load within the 32-byte page.
Step 8. Load the BEGOPS instruction; go to *Run-Test/Idle*.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 3) ..... – 0.6 V to 7 V
Input voltage range: All except DLA (see Note 3) ..... – 0.6 V to 6.5V
Input voltage range: DLA (see Note 3) ..... – 0.6 V to 15 V
Output voltage (see Note 3) ..... – 0.6 V to V_{CC} + 0.6V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: Voltage values are with respect to GND (substrate).

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	TTL	2		V_{CC} + 1	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level input voltage	TTL	–0.5		0.8	V
		CMOS	GND – 0.2		GND+ 0.2	
TA	Operating free-air temprature		0		70	°C
	Endurance cycles				10 000	Cycles

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –2.0 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	DLA, DLB	V_I = –2.4 V		75	150	µA
		DLA, DLB	V_I = 0 V			±10	
		TDI, TMS, TCK	V_I = 0.4		– 10	– 50	
		TDI, TMS, TCK	$V_I = V_{CC}$ = 5.5 V			±10	
I_O	Output current (leakage)		V_O = 0.1 to V_{CC}			±10	µA
I_{CC1}	V_{CC} average supply current (active read)		t_{cycle} = 160 ns, outputs open			20	mA
I_{CC2}	V_{CC} average supply current (active write)		t_{cycle} = 15 ms			15	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_I	Input capacitance	V_I = 0, f = 1 MHz		4	7	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		8	12	pF

† Typical values are at T_A = 25°C and nominal voltages..
‡ Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions

PARAMETER		MIN	MAX	UNIT
t_{DA}	TDO valid from falling edge of TCK		74	ns
t_{DZ}	TDO disable time from falling edge of TCK		35	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_{CYC}	TCK cycle time	160		ns
$t_{W(TCKH)}$	Pulse duration, TCK high	50		ns
$t_{W(TCKL)}$	Pulse duration, TCK low	70		ns
$t_{SU(TMS)}$	TMS input setup time	15		ns
$t_{IH(TMS)}$	TMS input hold time	5		ns
$t_{SU(TDI)}$	TDI input setup time	6		ns
$t_{IH(TDI)}$	TDI input hold time	15		ns

internal timing requirements

	PARAMETER	MIN	MAX	UNIT
t_{SSS}	Software sequence status bit valid from software sequence		2	μs
t_{PEBS}	Program erase busy status bit valid from BEGOPS execution		2	μs
t_{ST}	Sequence timer limit	9		ms

PARAMETER MEASUREMENT INFORMATION

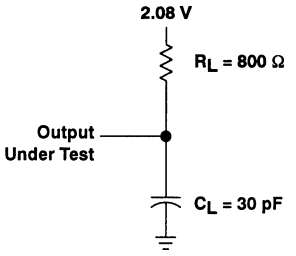
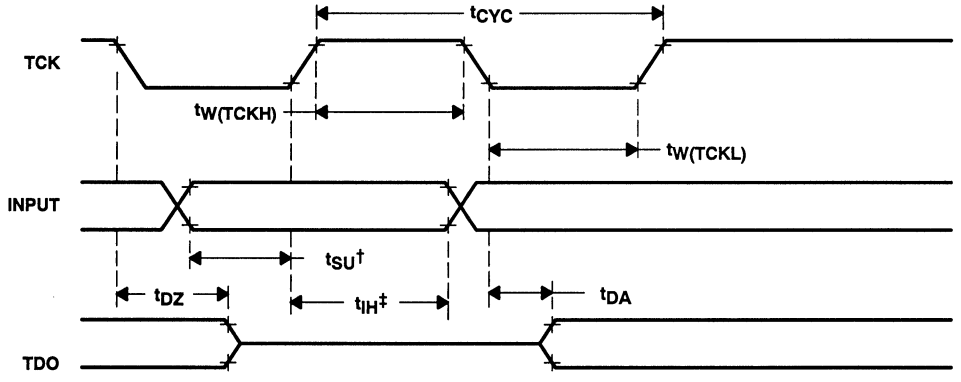


Figure 5. AC Test Output Load Circuit

AC testing input/output wave forms

AC testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs. Each device should have a 0.1-μF ceramic capacitor connected between V_{CC} and GND as close as possible to the device pins.



† t_{SU} represents TDI input setup time and TMS input setup time.
‡ t_{IH} represents TDI input hold time and TMS input hold time.

Figure 6. Timing Diagram

- **Organization . . . 128K × 8-Bit Flash Memory**
- **Pin Compatible with Existing 1-Megabit EPROMs**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time**

  V_{CC} ± 10%

'28F010-10	**100 ns**
'28F010-12	**120 ns**
'28F010-15	**150 ns**
'28F010-17	**170 ns**

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10 000, 1 000, and 100 Program/Erase Cycle Versions Available**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range: – 40°C to + 125°C**

description

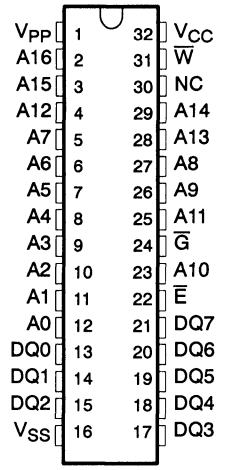
The TMS28F010 is a 1048 576-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed.

The TMS28F010 is available in 10 000, 1 000, and 100 program/erase endurance cycle versions.

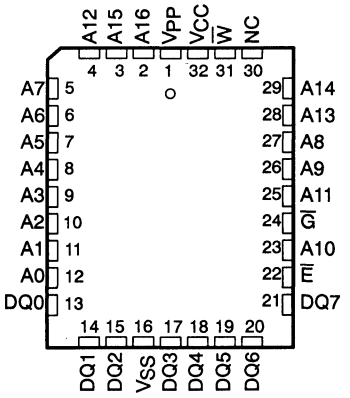
The TMS28F010 Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) centers, a 32-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FM suffix), a 32-lead thin small outline package (DD suffix), and a reverse pinout TSOP package (DU suffix).

The TMS28F010 is offered with three choices of temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes), –40°C to 85°C (NE, FME, DDE, and DUE suffixes), and –40°C to 125°C (NQ, FMQ, DDQ, and DUQ suffixes). All package types are offered with 168 hour burn-in (4 suffix).

N PACKAGE†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0–DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground

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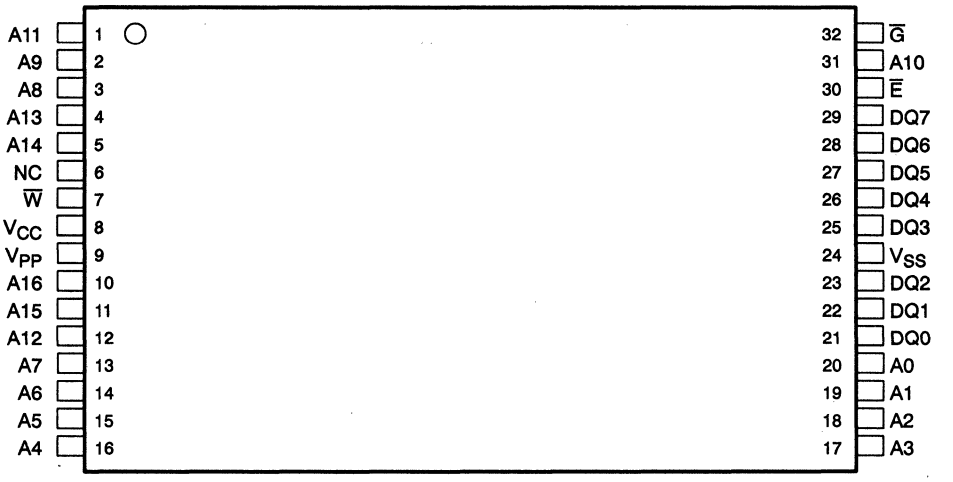
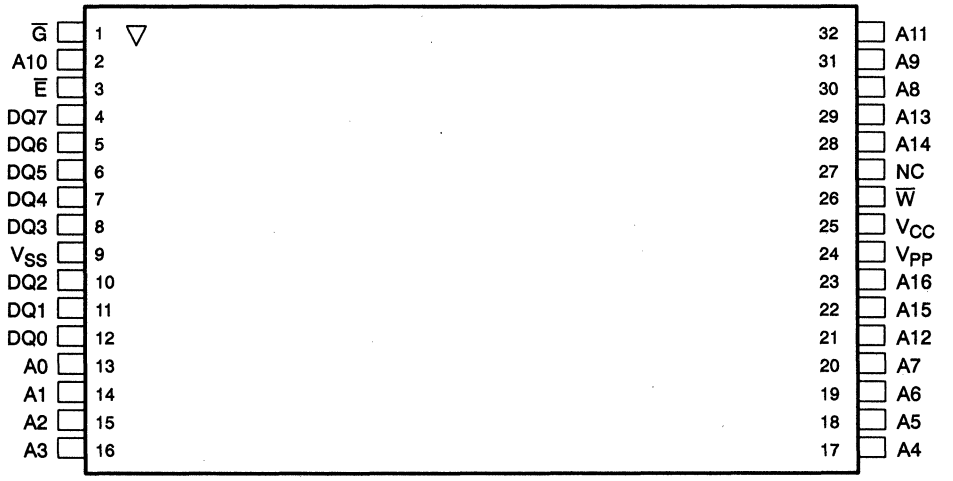
DD PACKAGE†

(TOP VIEW)



DU PACKAGE†
REVERSE PINOUT

(TOP VIEW)



† The packages shown are for pinout reference only.

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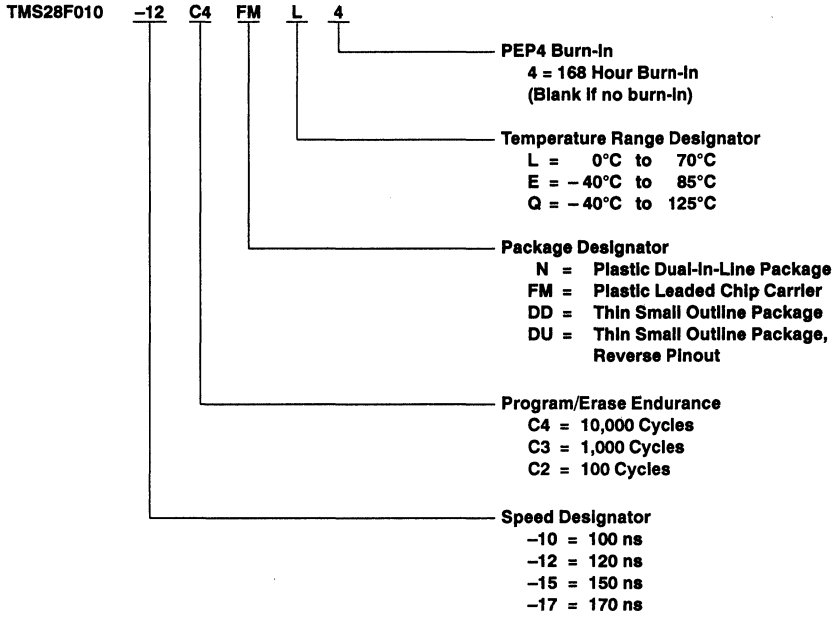
device symbol nomenclature



ADVANCE INFORMATION

functional block diagram

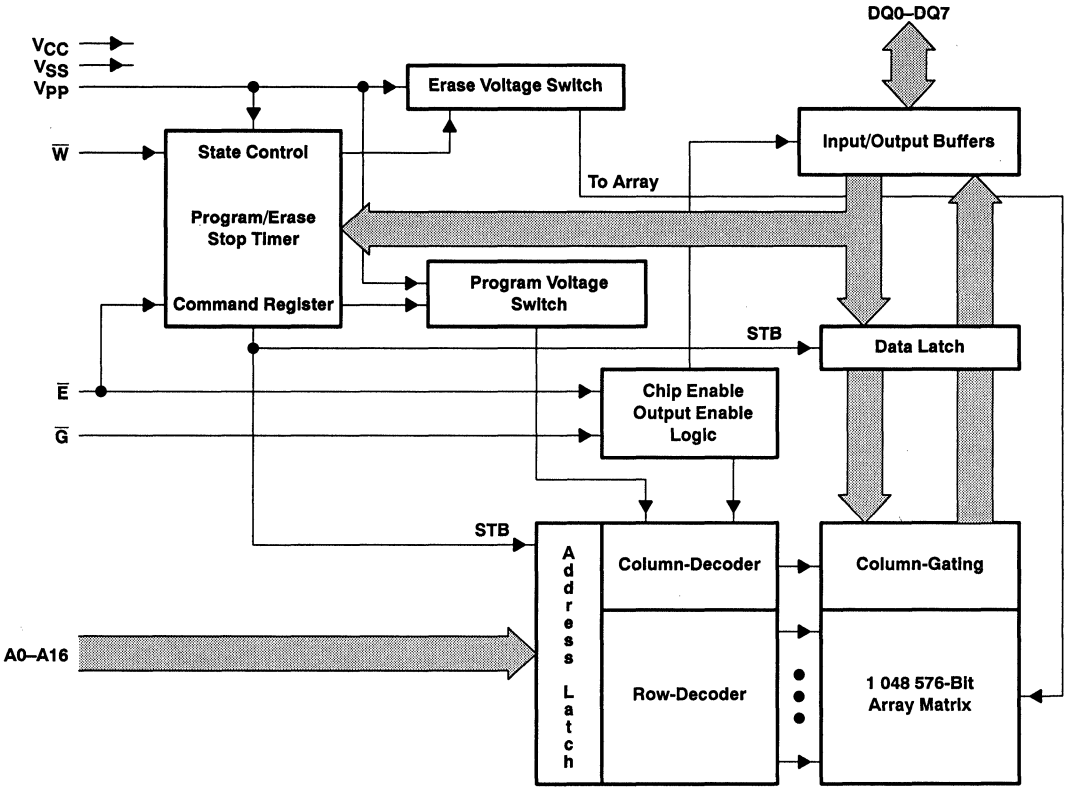


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Table 1. Operation Modes

MODE†		FUNCTION						
		V_{PP}§ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X†	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	HI-Z
	Signature Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_H‡	V_{IH}	MFG Code 97h
					V_{IH}			Device Code 75h
Read/Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	HI-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}
‡ 11.5 V < V_H < 13.0 V
§ $V_{PPL} \le V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F010s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices.

To read the output of the TMS28F010, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 μA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F010 draws active current when it is deselected during programming, erasure, or program/erase verification. It will continue to draw active current until the operation is terminated.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 (pin 26) is forced to V_H. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer's code 97h, and A0 high selects the device code 75h, as shown in the signature mode table below:

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	97
Device Code	V_{IH}	0	1	1	1	0	1	0	1	75

† $\overline{E}$ = $\overline{G}$ = V_{IL}, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, V_{PP} = V_{PPL}.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1's, may be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

ADVANCE INFORMATION

command register

The command register controls the program and erase functions of the TMS28F010. The signature mode may be activated using the command register in addition to the above method. When V_{PP} is high, the contents of the command register, and therefore the function being performed, may be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} will require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION (see Note 1)	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Signature Mode	3	Write	X	90h	Read	0000 0001	97h 75h
Set-up Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA†	A0h	Read	X	EVD
Set-up Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

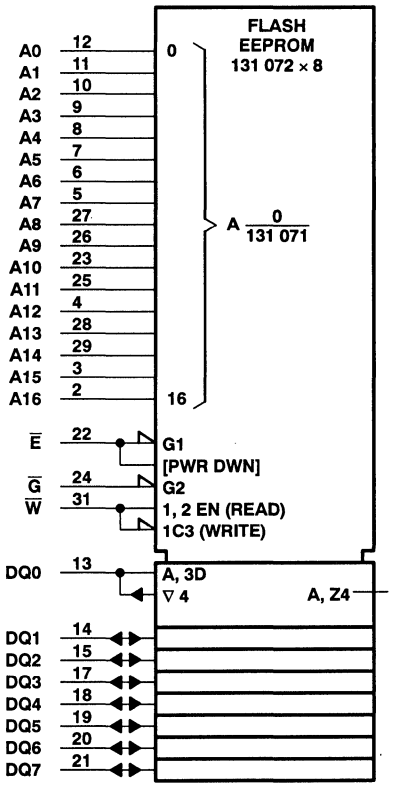
NOTE 1: Modes of operation are defined in Table 1.

† Description of Terms

EA Address of memory location to be read during erase verify.
RA Address of memory location to be read.
PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD Data read from location RA during the read operation.
EVD Data read from location EA during erase verify.
PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD Data read from location PA during program verify.

ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

ADVANCE INFORMATION

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. Also, when the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different, valid command is written to the command register.

signature mode command

The signature mode is activated by writing 90h into the command register. The manufacturer's code (97h) is identified by the value read from address location 0000h, and the device code (75h) is identified by the value read from address location 0001h.

set-up erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = 12$ V, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up erase command, 20h, into the command register. After the TMS28F010 is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase verify, read, or reset command is received.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F010 applies a margin voltage to each byte. If FFh is read from the byte, then all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, then an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F010.

set-up program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = 12$ V, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up program command, 40h, into the command register. The programming operation will be invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 μs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program verify, read, or reset command is received.

program-verify command

The TMS28F010 can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed.

The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation will end on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F010 applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming can continue to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

reset command

To reset the TMS28F010 after set-up erase command or set-up program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F010 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

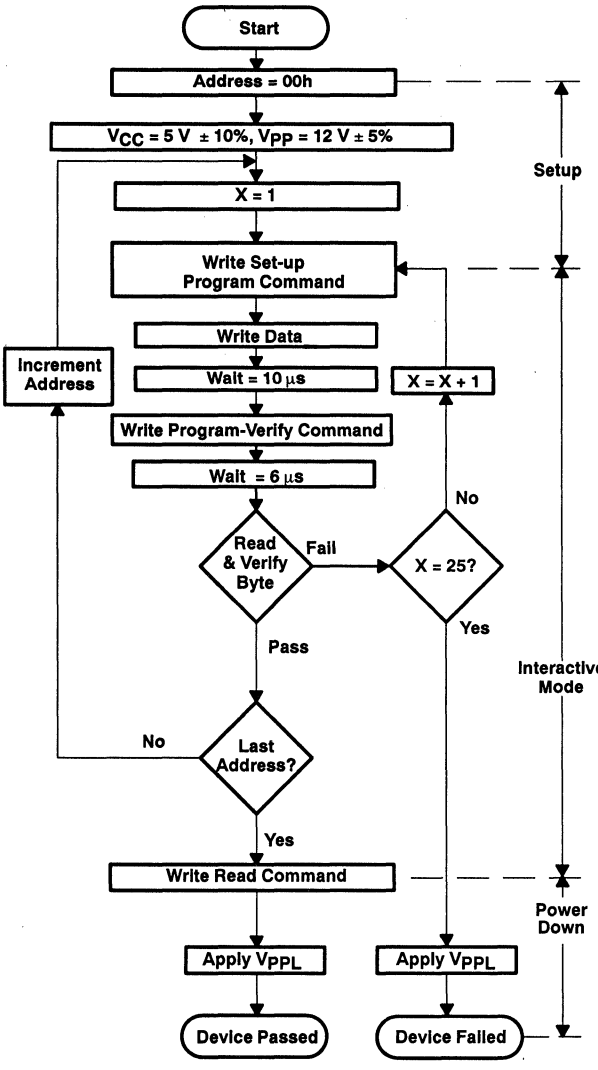
Fasterase algorithm

The TMS28F010 is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices may be erased in parallel. Since each Flash EEPROM may erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished. See Figure 3, Parallel Erase Flow Diagram.

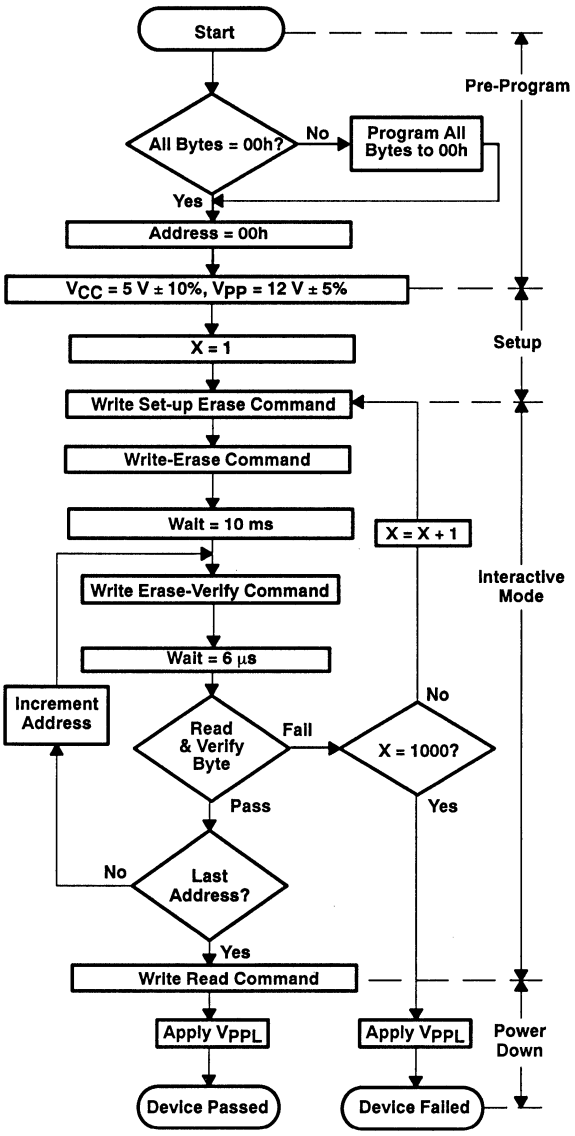
Examples of how to mask a device during parallel erase include driving the device's $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a setup erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for Vpp to Ramp to V_{PPH} (see Note 2) Initialize Pulse Count
Write	Set Up Program Write	Data = 40h
Write	Write Data	Valid Address/Data
Standby		Wait = 10 µs
Write	Program-Verify	Data = C0h; Ends Program Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for Vpp to Ramp to V_{PPL} (see Note 3)

NOTES: 2. Refer to the recommended operating conditions for the value of V_{PPH}.
3. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

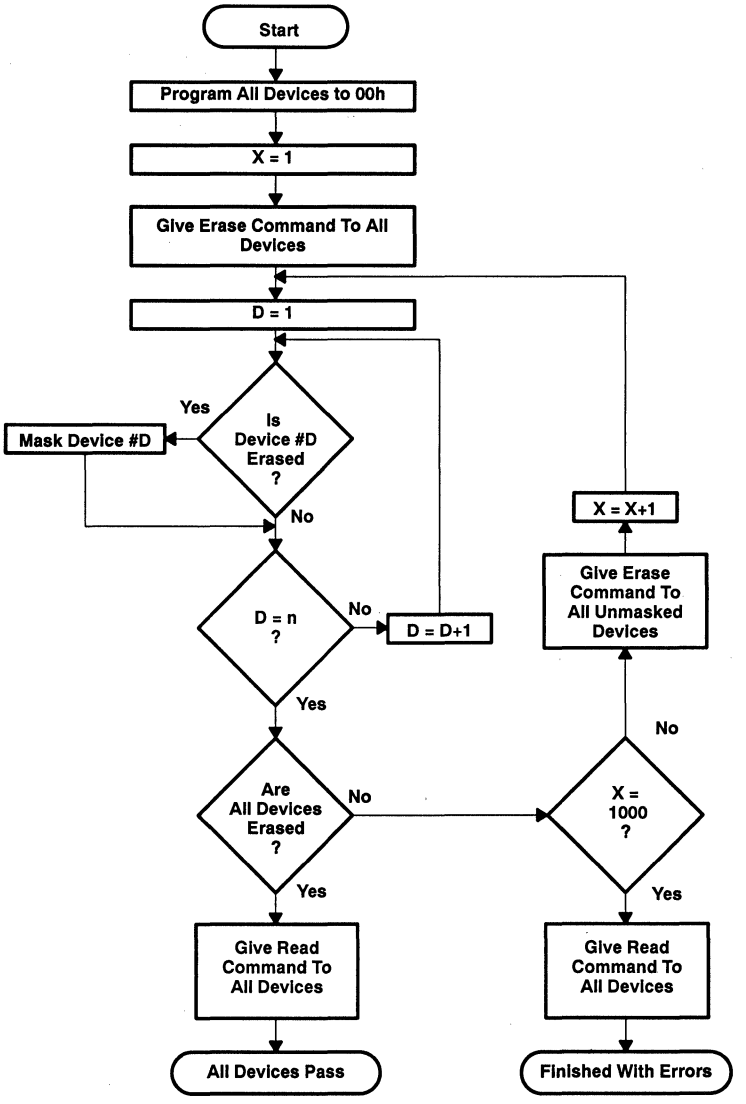


Bus Operation	Command	Comments
		Entire Memory Must = 00h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait for Vpp to Ramp to V_{PPH} (see Note 2)
		Initialize Pulse Count
Write	Set Up Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Byte to Verify; Data = A0h; Ends the Erase Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Erasure; Compare Output to FFh
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for Vpp to Ramp to V_{PPL} (see Note 3)

NOTES: 2 Refer to the recommended operating conditions for the value of V_{PPH}.
3 Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm

ADVANCE INFORMATION



NOTE: n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 5): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 (see Note 5) ..... −0.6 V to 13.5 V
Output voltage range (see Note 6) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program
(NL, FML, DDL, DUL) ..... 0°C to 70°C
Operating free-air temperature range during read/erase/program
(NE, FME, DDE, DUE) ..... − 40°C to 85°C
Operating free-air temperature range during read/erase/program
(NQ, FMQ, DDQ, DUQ) ..... − 40° C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to GND.
5. The voltage on any input pin may undershoot to –2.0 V for periods less than 20 ns.
6. The voltage on any output pin may overshoot to 7.0 V for periods less than 20 ns.

ADVANCE INFORMATION

recommended operating conditions

				'28F010-10 '28F010-12 '28F010-15 '28F010-17			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		V_{CC} + 2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	–0.5		0.8	V
			CMOS	GND – 0.2		GND+0.2	

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4			V
			I_{OH} = – 100 µA	V_{CC} – 0.4			
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA			0.45	V
			I_{OL} = 100 µA			0.1	
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	µA
		A9	VI = 0 to 13 V			± 200	
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, read mode			200	µA
			VPP = V_{PPL}			±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP4}	VPP supply current (during program/erase verify) (see Note 7)		V_{PP} = V_{PPH}			5.0	mA
I_{CCS}	V_{CC} supply current (stand-by)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			100	µA
I_{CC1}	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, outputs open			30	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, programming in progress			10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, erasure in progress			15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, program/erase-verify in progress			15	mA

NOTE 7: Not 100% tested; characterization data available.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0 , f = 1MHz			6	pF
C_O	Output capacitance	V_O = 0 , f = 1 MHz			12	pF

† Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

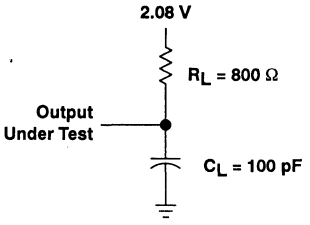
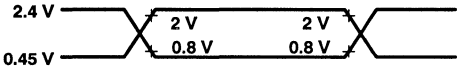


Figure 4. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

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switching characteristics over full ranges of recommended operating conditions

DESCRIPTION		TEST CONDITIONS	ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from chip enable		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from output enable		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Read cycle time		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, output enable low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{wr(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first.

AC characteristics–write/erase/program operations

DESCRIPTION		ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
			MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVWL}	0		0		0		0		ns
$t_{h(A)}$	Address hold time	t_{WLAX}	55		60		60		70		ns
$t_{su(D)}$	Data setup time	t_{DVWH}	50		50		50		50		ns
$t_{hw(D)}$	Data hold time	t_{WHDX}	10		10		10		10		ns
$t_{wr(W)}$	Write recovery time before read	t_{WHGL}	6		6		6		6		µs
$t_{rr(W)}$	Read recovery time before write	t_{GHWL}	0		0		0		0		µs
$t_{su(E)}$	Chip enable setup time before write	t_{ELWL}	20		20		20		20		ns
$t_{h(E)}$	Chip enable hold time	t_{WHEH}	0		0		0		0		ns
$t_{w(W)}$	Write pulse duration (see Note 8)	t_{WLWH}	60		60		60		60		ns
$t_{wh(W)}$	Write pulse duration high	t_{WHWL}	20		20		20		20		ns
$t_{c(W)B}$	Duration of programming operation	t_{WHWH1}	10		10		10		10		µs
$t_{c(E)B}$	Duration of erase operation	t_{WHWH2}	9.5	10	9.5	10	9.5	10	9.5	10	ms
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{su(E)P}$	Chip enable, setup time to V_{PP} ramp	t_{EHVP}	100		100		100		100		ns
$t_{s(P)R}$	V_{PP} rise time	t_{VPPR}	1		1		1		1		µs
$t_{s(P)F}$	V_{PP} fall time	t_{VPPF}	1		1		1		1		µs

NOTE 8: Rise/fall time ≤ 10 ns.

alternative $\overline{CE}$-controlled writes

DESCRIPTION		ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVEL}	0		0		0		0		ns
$t_{hE(A)}$	Address hold time	t_{ELAX}	75		80		80		90		ns
$t_{su(D)}$	Data setup time	t_{DVEH}	50		50		50		50		ns
$t_{hE(D)}$	Data hold time	t_{EHDX}	10		10		10		10		ns
$t_{wr(E)}$	Write recovery time before read	t_{EHGL}	6		6		6		6		µs
$t_{rr(E)}$	Read recovery time before write	t_{GHEL}	0		0		0		0		µs
$t_{su(W)}$	Write enable setup time before chip enable	t_{WLEL}	0		0		0		0		ns
$t_{h(W)}$	Write enable hold time	t_{EHWH}	0		0		0		0		ns
$t_{w(E)}$	Write pulse duration	t_{ELEH}	70		70		70		80		ns
$t_{wh(E)}$	Write pulse duration high	t_{EHEL}	20		20		20		20		ns
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{c(W)B}$	Duration of programming operation	t_{EHEH}	10		10		10		10		µs

PARAMETER MEASUREMENT INFORMATION

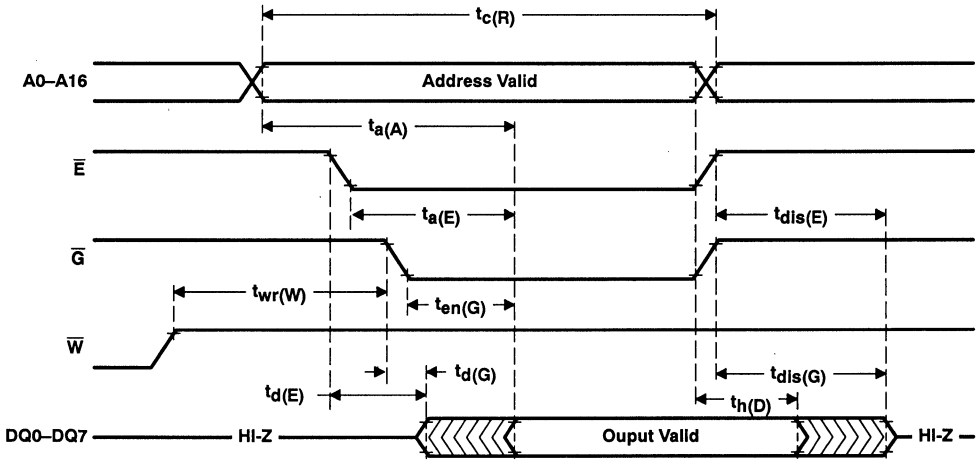

Figure 5. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

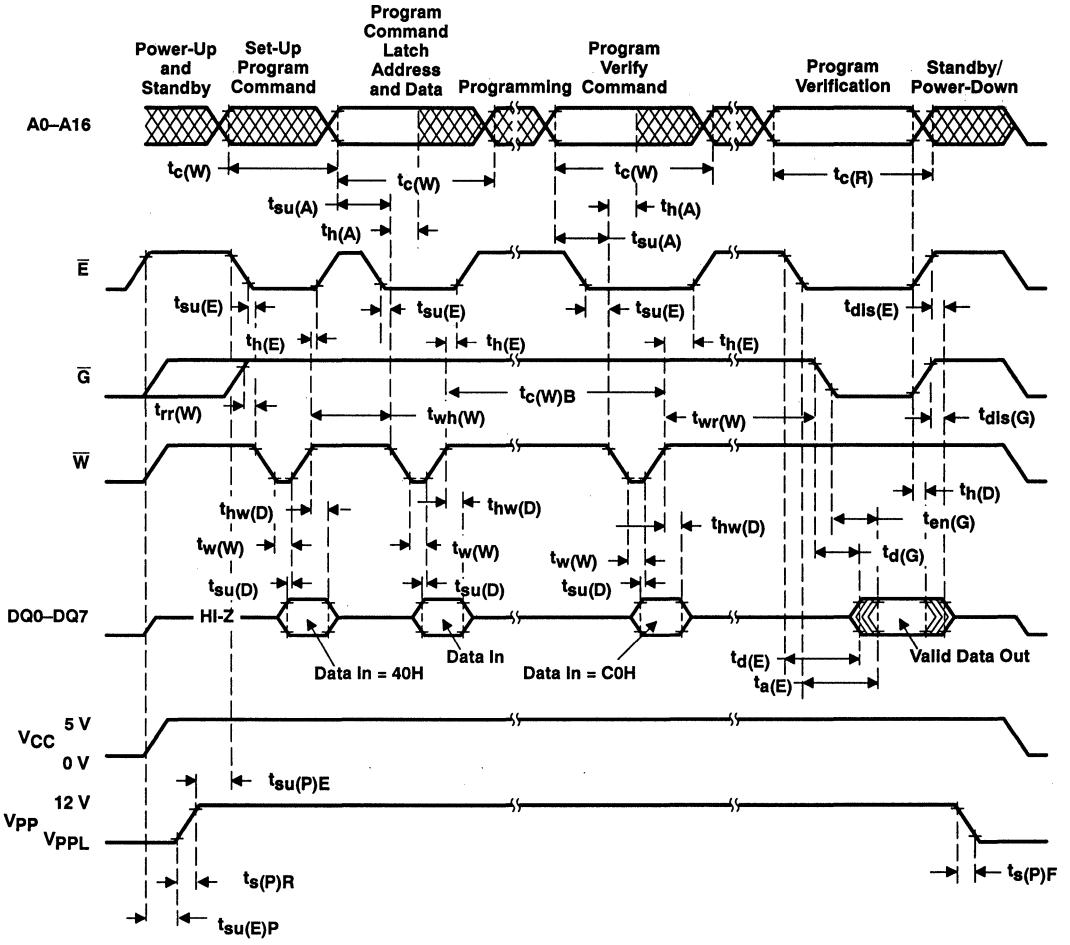


Figure 6. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

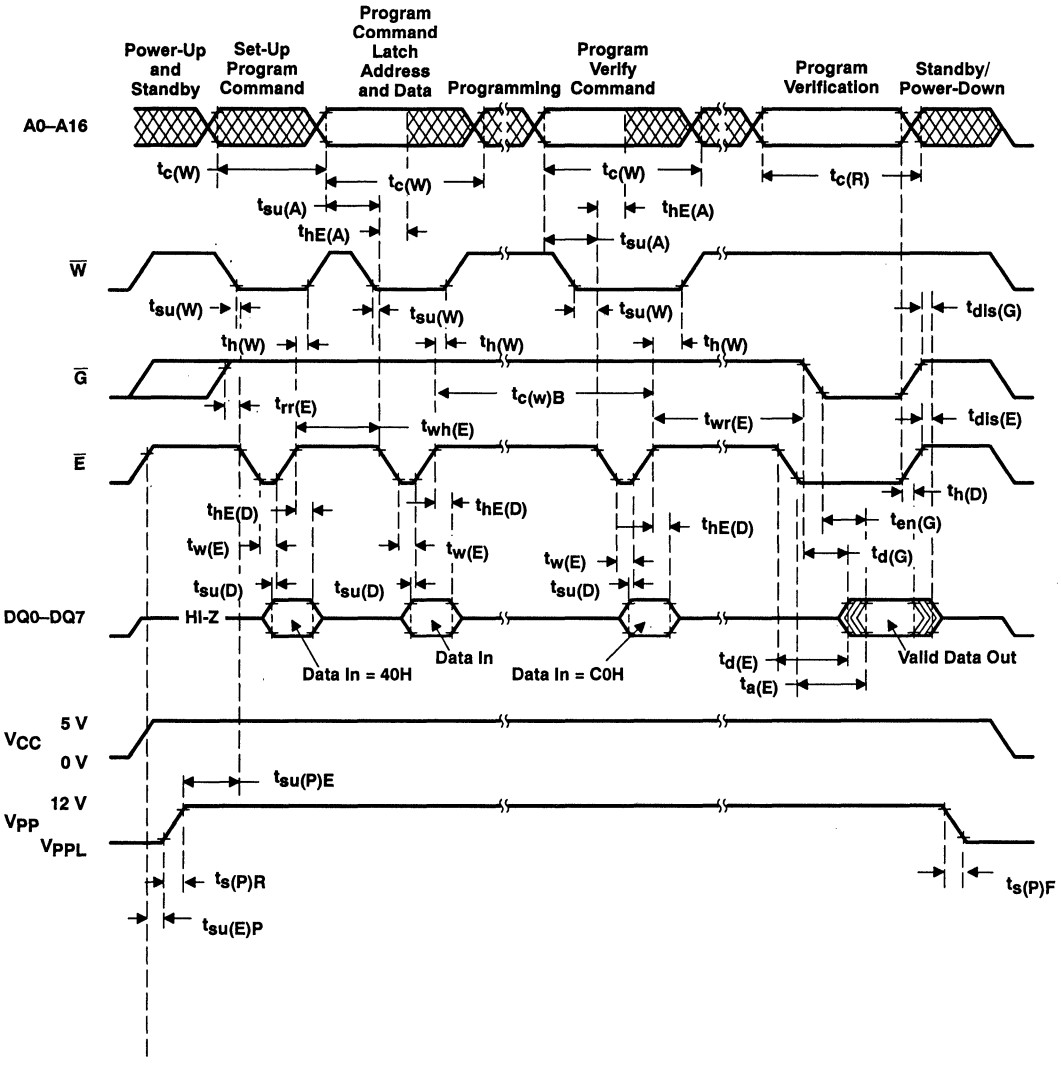


Figure 7. Write Cycle (Alternative $\overline{CE}$-Controlled Writes) Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

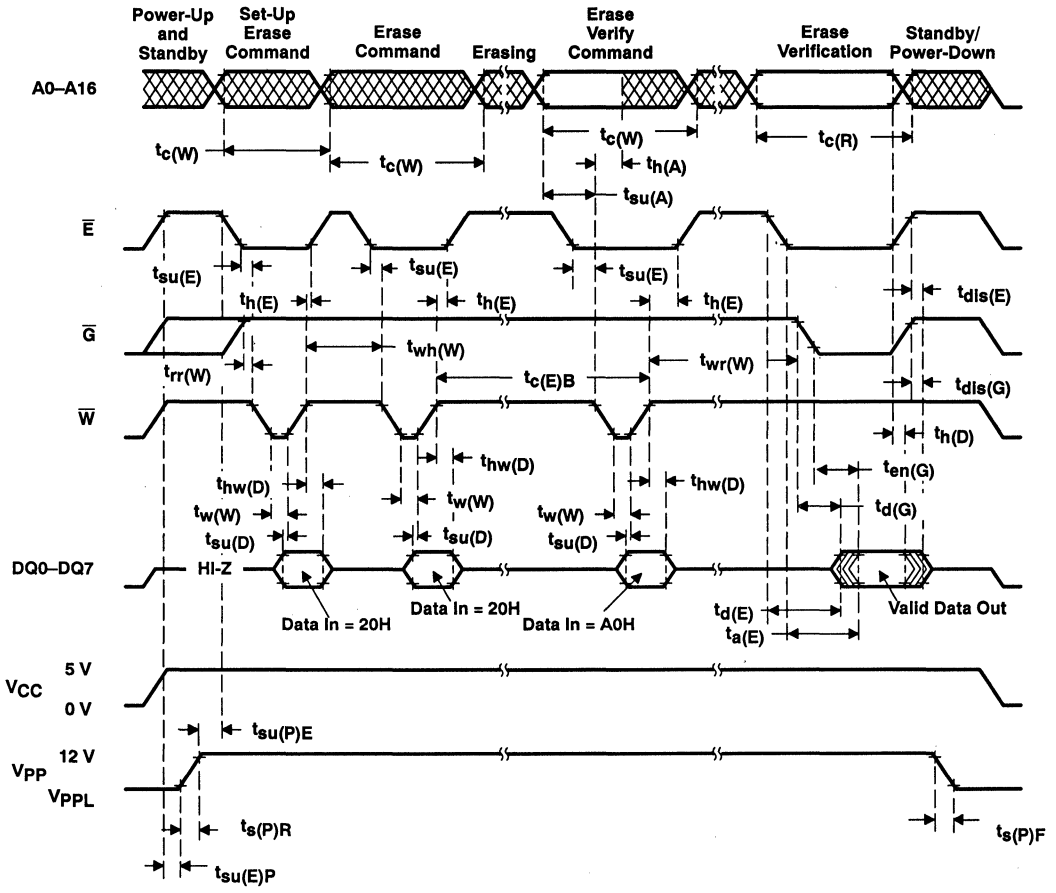


Figure 8. Flash-Erase Cycle Timing

- **Organization . . . 64K × 8-Bit Flash Memory**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time:**
  V_{CC} ± 10%

'28F512-10	**100 ns**
'28F512-12	**120 ns**
'28F512-15	**150 ns**
'28F512-17	**170 ns**

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10 000, 1 000 and 100 Program/Erase Cycle Versions**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range: – 40°C to + 125°C**

description

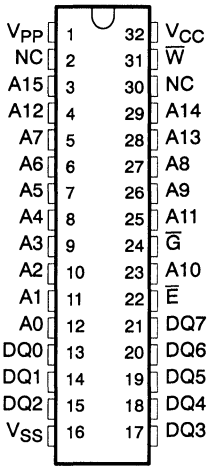
The TMS28F512 is a 524 288-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed.

The TMS28F512 is available in 10 000, 1 000, and 100 program/erase endurance cycle versions.

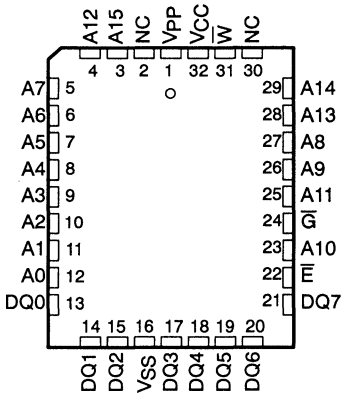
The TMS28F512 Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) centers, a 32-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FM suffix), a 32-lead thin small outline package (DD suffix), and a reverse pinout TSOP package (DU suffix).

The TMS28F512 is offered with three choices of temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes), –40°C to 85°C (NE, FME, DDE, and DUE suffixes), and –40°C to 125°C (NQ, FMQ, DDQ, and DUQ suffixes). All package types are offered with 168 hour burn-in (4 suffix).

N PACKAGE†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† The packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
$\overline{W}$	Write Enable
DQ0–DQ7	Data In/Data Out
V_{CC}	5-V Power Supply
V_{PP}	12-V Power Supply
V_{SS}	Ground

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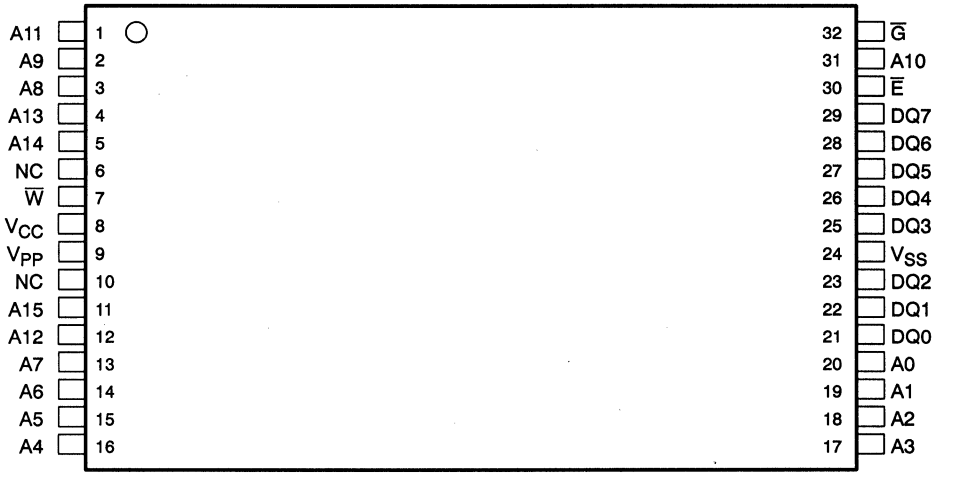
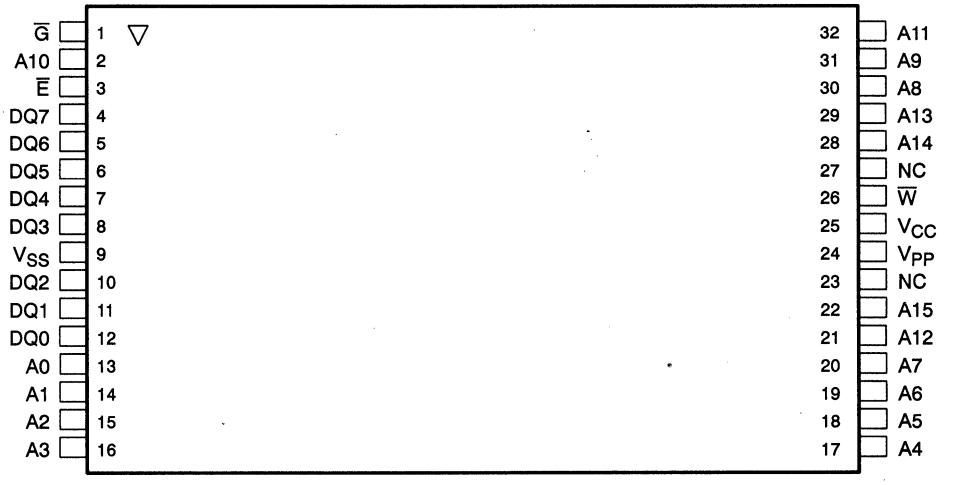
DD PACKAGE†

(TOP VIEW)



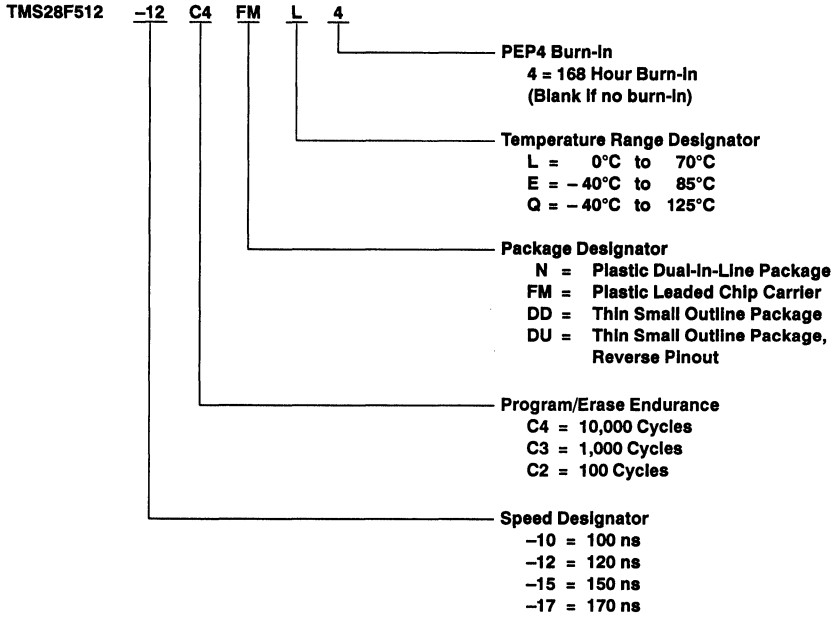
DU PACKAGE†
REVERSE PINOUT

(TOP VIEW)



† The packages shown are for pinout reference only.

device symbol nomenclature



ADVANCE INFORMATION

functional block diagram

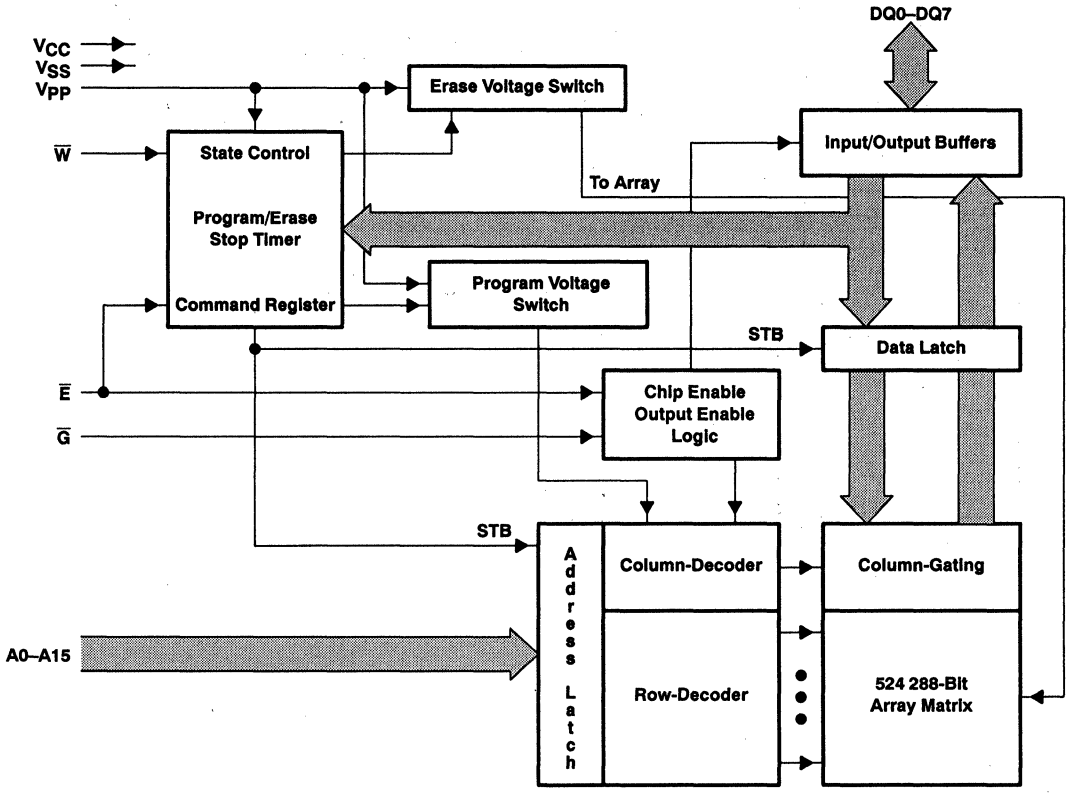


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Table 1. Operation Modes

MODE†		FUNCTION						
		V_{PP}§ (1)	$\overline{E}$ (22)	$\overline{G}$ (24)	A0 (12)	A9 (26)	$\overline{W}$ (31)	DQ0–DQ7 (13–15, 17–21)
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X†	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	HI-Z
	Signature Mode	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_H‡	V_{IH}	MFG Code 97h
					V_{IH}			Device Code 73h
Read/Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	HI-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}
‡ 11.5 V < V_H < 13.0 V
§ $V_{PPL} \leq V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices.

To read the output of the TMS28F512, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 μA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F512 draws active current when it is deselected during programming, erasure, or program/erase verification. It will continue to draw active current until the operation is terminated.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 (pin 26) is forced to V_H. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer's code 97h, and A0 high selects the device code 73h, as shown in the signature mode table below:

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	97
Device Code	V_{IH}	0	1	1	1	0	0	1	1	73

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A15 = V_{IL}, $V_{PP} = V_{PPL}$.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1's, may be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

ADVANCE INFORMATION

command register

The command register controls the program and erase functions of the TMS28F512. The signature mode may be activated using the command register in addition to the above method. When V_{PP} is high, the contents of the command register, and therefore the function being performed, may be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} will require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION (see Note 1)	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Signature Mode	3	Write	X	90h	Read	0000 0001	97h 73h
Set-up Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA†	A0h	Read	X	EVD
Set-up Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

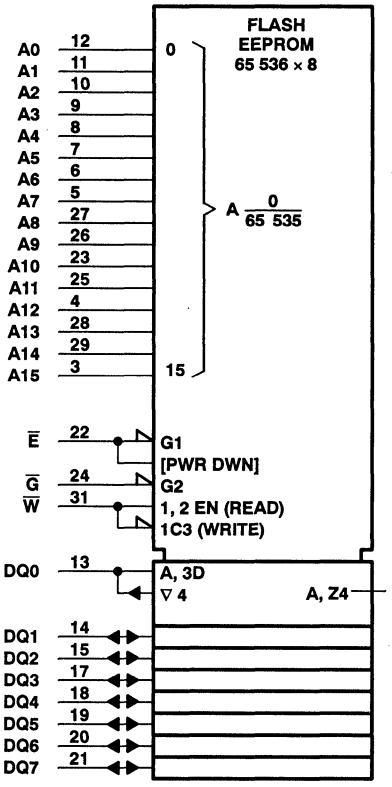
NOTE 1: Modes of operation are defined in Table 1.

† Description of Terms

EA Address of memory location to be read during erase verify.
RA Address of memory location to be read.
PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD Data read from location RA during the read operation.
EVD Data read from location EA during erase verify.
PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD Data read from location PA during program verify.

ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

ADVANCE INFORMATION

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. Also, when the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different, valid command is written to the command register.

signature mode command

The signature mode is activated by writing 90h into the command register. The manufacturer's code (97h) is identified by the value read from address location 0000h, and the device code (73h) is identified by the value read from address location 0001h.

set-up erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = 12$ V, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up erase command, 20h, into the command register. After the TMS28F512 is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase verify, read, or reset command is received.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the byte to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F512 applies a margin voltage to each byte. If FFh is read from the byte, then all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, then an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F512.

set-up program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = 12$ V, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up program command, 40h, into the command register. The programming operation will be invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program verify, read, or reset command is received.

program-verify command

The TMS28F512 can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed.

The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation will end on the rising edge of $\overline{W}$.

While verifying a byte, the TMS28F512 applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming can continue to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

reset command

To reset the TMS28F512 after set-up erase command or set-up program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F512 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

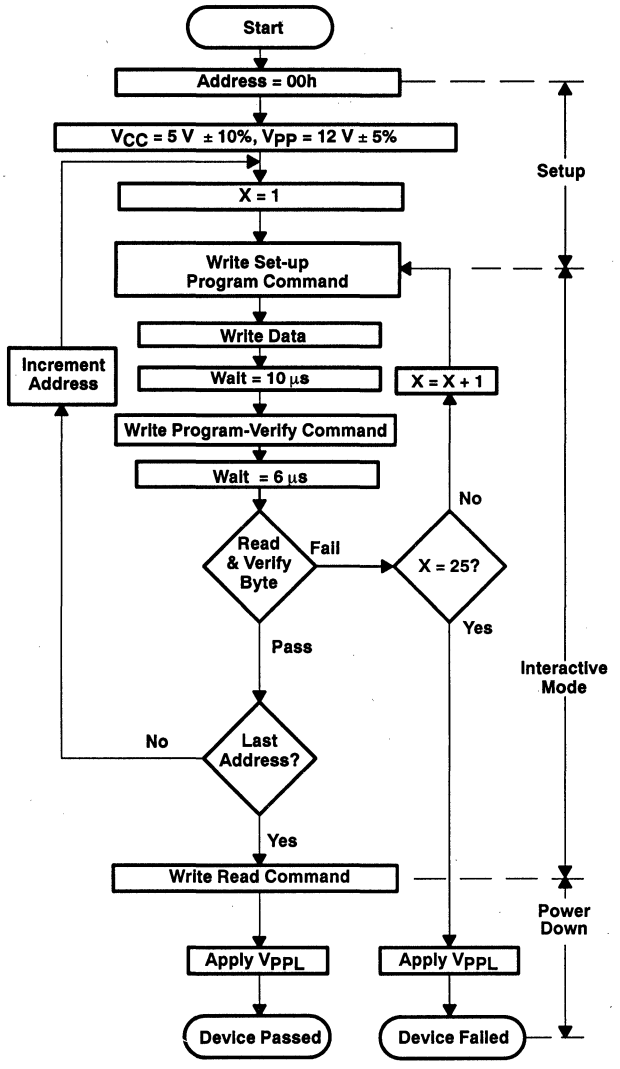
Fasterase algorithm

The TMS28F512 is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices may be erased in parallel. Since each Flash EEPROM may erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished. See Figure 3, Parallel Erase Flow Diagram.

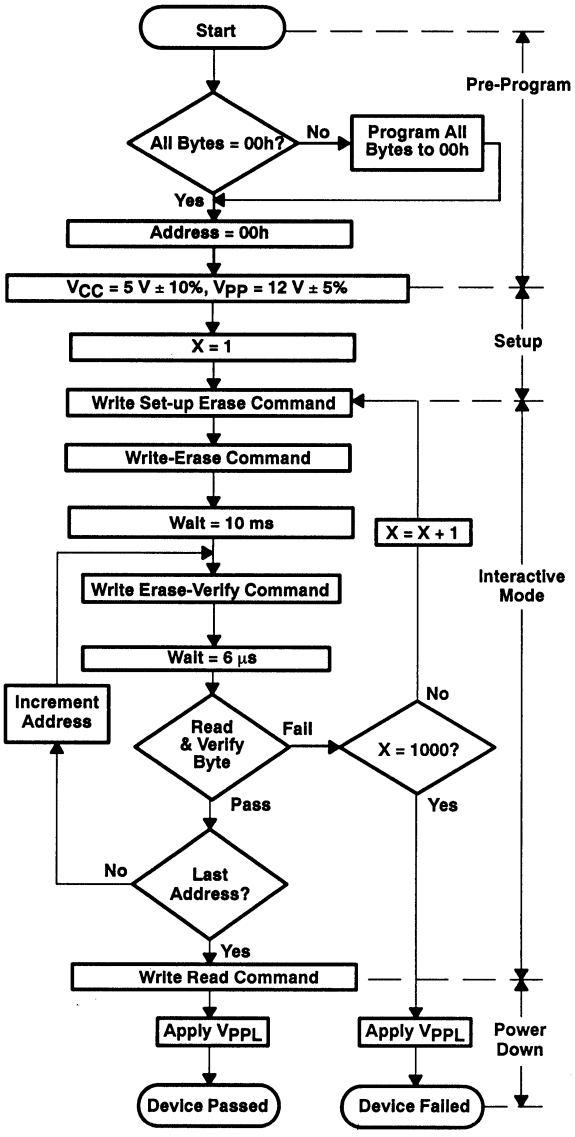
Examples of how to mask a device during parallel erase include driving the device's $\overline{E}$ pin high, writing the read command (00h) to the device when the others receive a setup erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.



Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for V_{PP} to Ramp to V_{PPH} (see Note 2)
		Initialize Pulse Count
Write	Set Up Program Write	Data = 40h
Write	Write Data	Valid Address/Data
Standby		Wait = 10 µs
Write	Program-Verify	Data = C0h; Ends Program Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for V_{PP} to Ramp to V_{PPL} (see Note 3)

NOTES: 2. Refer to the recommended operating conditions for the value of V_{PPH}.
3. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm



Bus Operation	Command	Comments
		Entire Memory Must = 00h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait for V_{PP} to Ramp to V_{PPH} (see Note 2)
		Initialize Pulse Count
Write	Set Up Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Byte to Verify; Data = A0h; Ends the Erase Operation
Standby		Wait = 6 µs
Read		Read Byte to Verify Erasure; Compare Output to FFh
Write	Read	Data = 00h; Resets Register for Read Operations
Standby		Wait for V_{PP} to Ramp to V_{PPL} (see Note 3)

NOTES: 2 Refer to the recommended operating conditions for the value of V_{PPH}.
3 Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm

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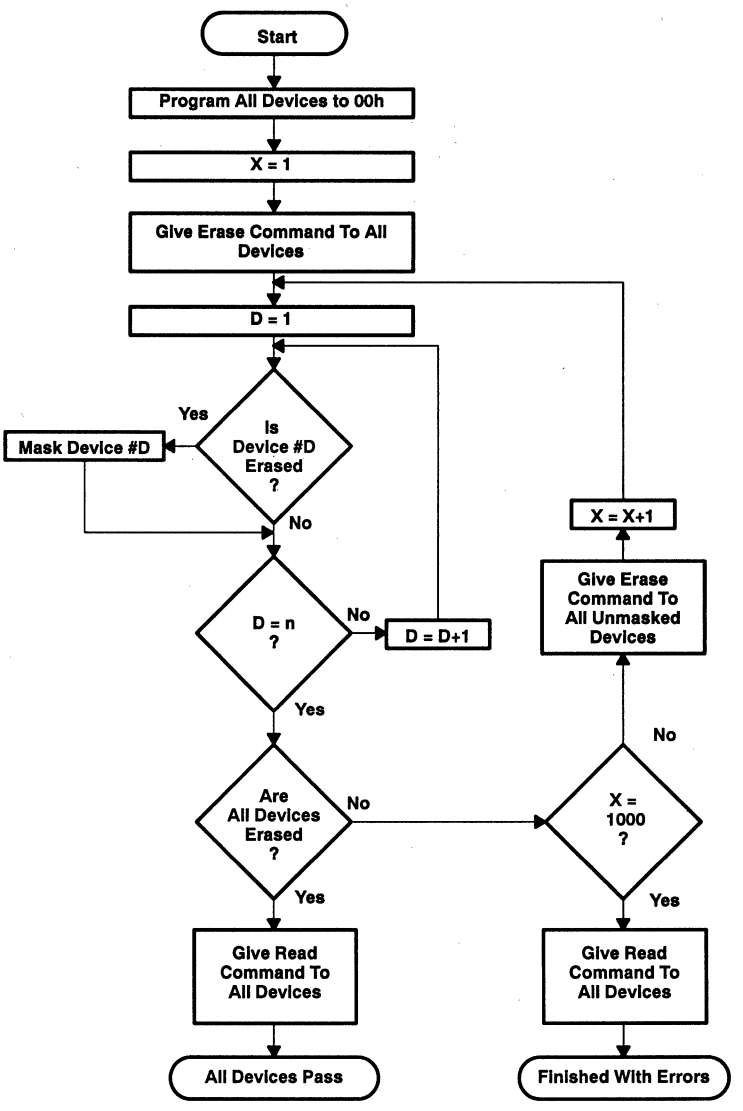

NOTE: n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 5): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 (see Note 5) ..... −0.6 V to 13.5 V
Output voltage range (see Note 6) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program
(NL, FML, DDL, DUL) ..... 0°C to 70°C
Operating free-air temperature range during read/erase/program
(NE, FME, DDE, DUE) ..... − 40°C to 85°C
Operating free-air temperature range during read/erase/program
(NQ, FMQ, DDQ, DUQ) ..... − 40° C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to GND.
5. The voltage on any input pin may undershoot to –2.0 V for periods less than 20 ns.
6. The voltage on any output pin may overshoot to 7.0 V for periods less than 20 ns.

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recommended operating conditions

				'28F512-10 '28F512-12 '28F512-15 '28F512-17			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		V_{CC} + 2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	–0.5		0.8	V
			CMOS	GND – 0.2		GND+0.2	

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4			V
			I_{OH} = – 100 µA	V_{CC} – 0.4			
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA			0.45	V
			I_{OL} = 100 µA			0.1	
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	µA
		A9	VI = 0 to 13 V			± 200	
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, read mode			200	µA
			VPP = V_{PPL}			±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 7)		V_{PP} = V_{PPH}			30	mA
I_{PP4}	VPP supply current (during program/erase verify) (see Note 7)		V_{PP} = V_{PPH}			5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			100	µA
I_{CC1}	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, outputs open			30	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, programming in progress			10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, erasure in progress			15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, program/erase-verify in progress			15	mA

NOTE 7: Not 100% tested; characterization data available.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0 , f = 1MHz			6	pF
C_O	Output capacitance	V_O = 0 , f = 1 MHz			12	pF

† Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

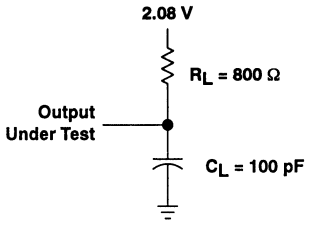
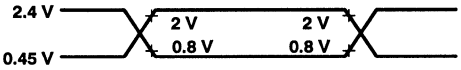


Figure 4. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

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switching characteristics over full ranges of recommended operating conditions

DESCRIPTION		TEST CONDITIONS	ALTERNATE SYMBOL	'28F512-10		'28F512-12		'28F512-15		'28F512-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load Input $t_r \le 20$ ns Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from chip enable		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from output enable		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Read cycle time		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, output enable low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{wr(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first.

AC characteristics–write/erase/program operations

DESCRIPTION		ALTERNATE SYMBOL	'28F512-10		'28F512-12		'28F512-15		'28F512-17		UNIT
			MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVWL}	0		0		0		0		ns
$t_{h(A)}$	Address hold time	t_{WLAX}	55		60		60		70		ns
$t_{su(D)}$	Data setup time	t_{DVWH}	50		50		50		50		ns
$t_{hw(D)}$	Data hold time	t_{WHDX}	10		10		10		10		ns
$t_{wr(W)}$	Write recovery time before read	t_{WHGL}	6		6		6		6		µs
$t_{rr(W)}$	Read recovery time before write	t_{GHWL}	0		0		0		0		µs
$t_{su(E)}$	Chip enable setup time before write	t_{ELWL}	20		20		20		20		ns
$t_{h(E)}$	Chip enable hold time	t_{WHEH}	0		0		0		0		ns
$t_{w(W)}$	Write pulse duration (see Note 8)	t_{WLWH}	60		60		60		60		ns
$t_{wh(W)}$	Write pulse duration high	t_{WHWL}	20		20		20		20		ns
$t_{c(W)B}$	Duration of programming operation	t_{WHWH1}	10		10		10		10		µs
$t_{c(E)B}$	Duration of erase operation	t_{WHWH2}	9.5	10	9.5	10	9.5	10	9.5	10	ms
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{su(E)P}$	Chip enable, setup time to V_{PP} ramp	t_{EHVP}	100		100		100		100		ns
$t_{s(P)R}$	V_{PP} rise time	t_{VPPR}	1		1		1		1		µs
$t_{s(P)F}$	V_{PP} fall time	t_{VPPF}	1		1		1		1		µs

NOTE 8: Rise/fall time ≤ 10 ns.

alternative $\overline{CE}$-controlled writes

DESCRIPTION		ALTERNATE SYMBOL	'28F512-10		'28F512-12		'28F512-15		'28F512-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVEL}	0		0		0		0		ns
$t_{hE(A)}$	Address hold time	t_{ELAX}	75		80		80		90		ns
$t_{su(D)}$	Data setup time	t_{DVEH}	50		50		50		50		ns
$t_{hE(D)}$	Data hold time	t_{EHDX}	10		10		10		10		ns
$t_{wr(E)}$	Write recovery time before read	t_{EHGL}	6		6		6		6		µs
$t_{rr(E)}$	Read recovery time before write	t_{GHEL}	0		0		0		0		µs
$t_{su(W)}$	Write enable setup time before chip enable	t_{WLEL}	0		0		0		0		ns
$t_{h(W)}$	Write enable hold time	t_{EHWH}	0		0		0		0		ns
$t_{w(E)}$	Write pulse duration	t_{ELEH}	70		70		70		80		ns
$t_{wh(E)}$	Write pulse duration high	t_{EHEL}	20		20		20		20		ns
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{c(W)B}$	Duration of programming operation	t_{EHEH}	10		10		10		10		µs

PARAMETER MEASUREMENT INFORMATION

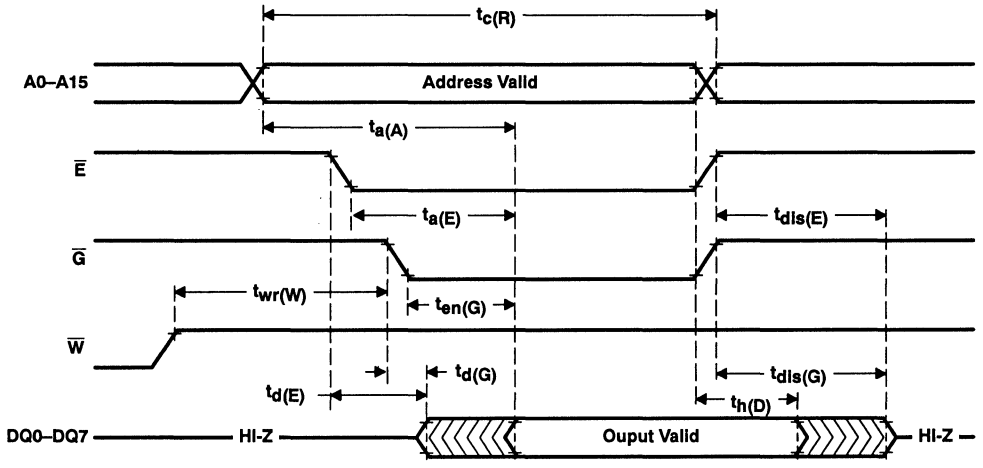

Figure 5. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

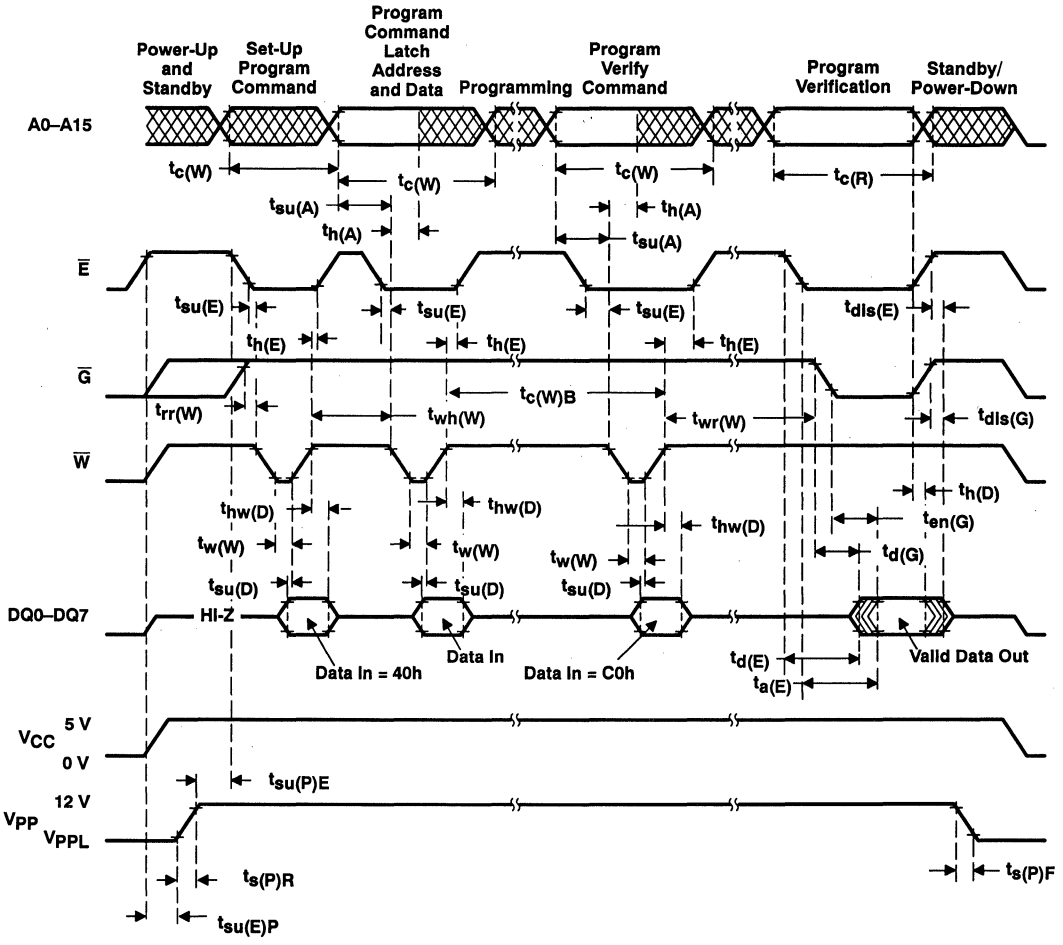

Figure 6. Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

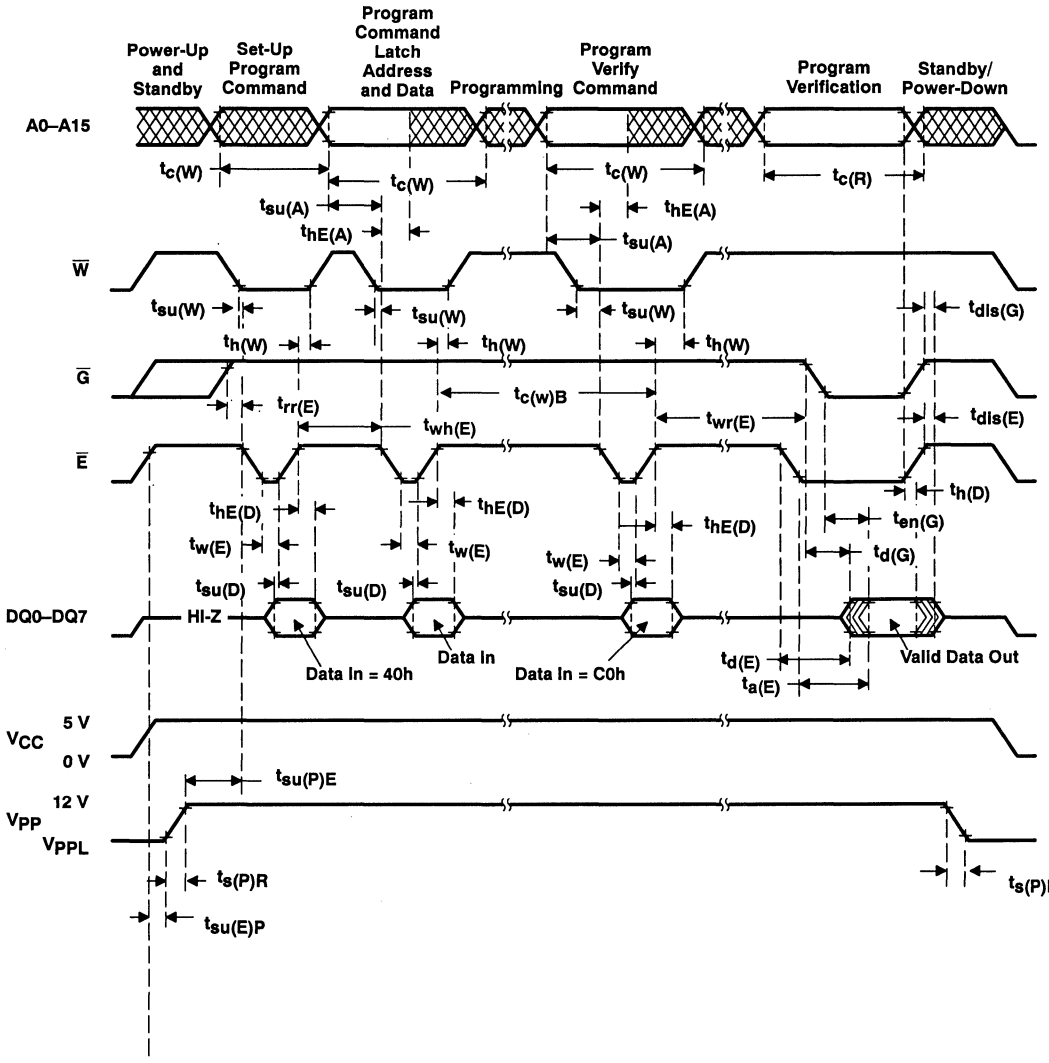


Figure 7. Write Cycle (Alternative $\overline{CE}$-Controlled Writes) Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

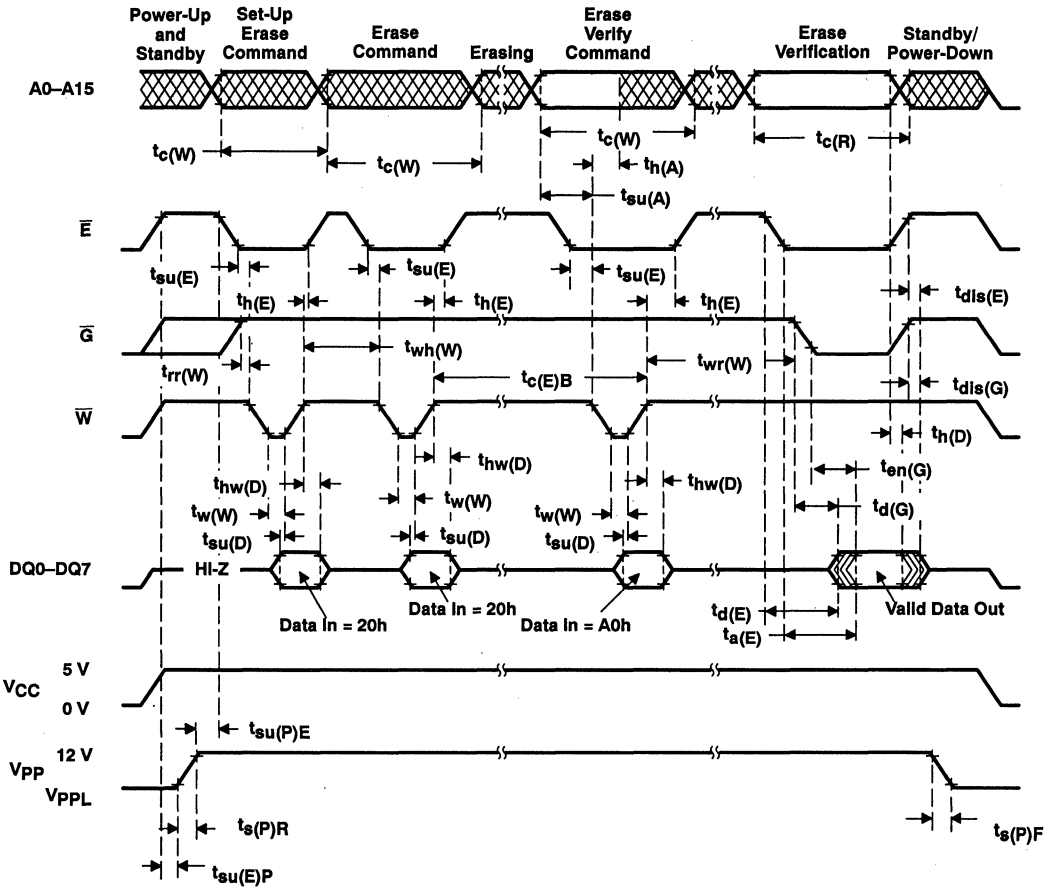


Figure 8. Flash-Erase Cycle Timing

- **Organization . . . 64K × 16 Flash Memory**
- **Pin Compatible with Existing 1-Megabit EPROMs**
- **All Inputs/Outputs TTL Compatible**
- **Maximum Access/Minimum Cycle Time:**
  V_{CC} ± 10%

'28F210-10	**100 ns**
'28F210-12	**120 ns**
'28F210-15	**150 ns**
'28F210-17	**170 ns**

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10 000, 1 000, and 100 Program/Erase Cycles**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range: – 40°C to + 125°C**

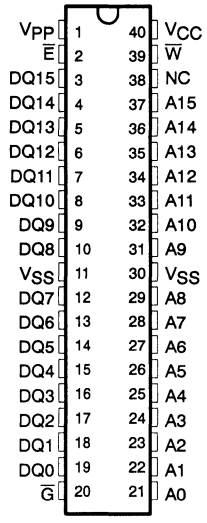
description

The TMS28F210 is a 1048 576-bit, programmable read-only memory that can be electrically bulk-erased and reprogrammed.

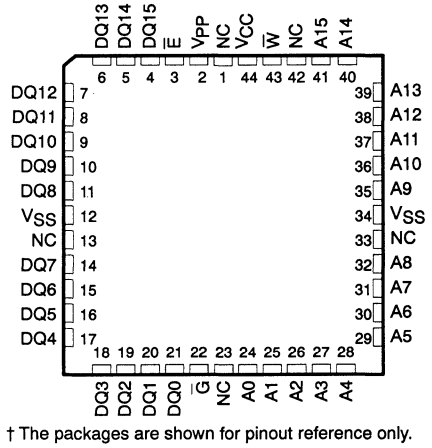
The TMS28F210 is available in 10 000, 1 000, and 100 program/erase endurance cycle versions.

The TMS28F210 Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) center and a 44-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FN suffix). The TMS28F210 is offered with three choices of temperature ranges of 0°C to 70°C (NL and FNL suffixes), –40°C to 85°C (NE and FNE suffixes), and –40°C to 125°C (NQ and FNQ suffixes). All packages are offered with 168-hour burn-in.

N PACKAGE†
(TOP VIEW)



FN PACKAGE†
(TOP VIEW)



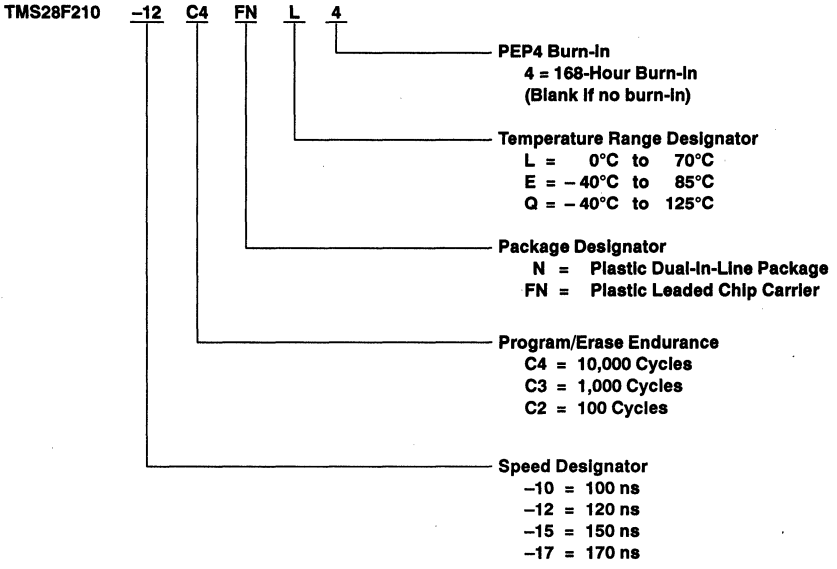
† The packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{SS}	Ground
NC	No Connection
$\overline{W}$	Program
DQ0–DQ15	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	12-V Power Supply‡

‡ Only in program mode.

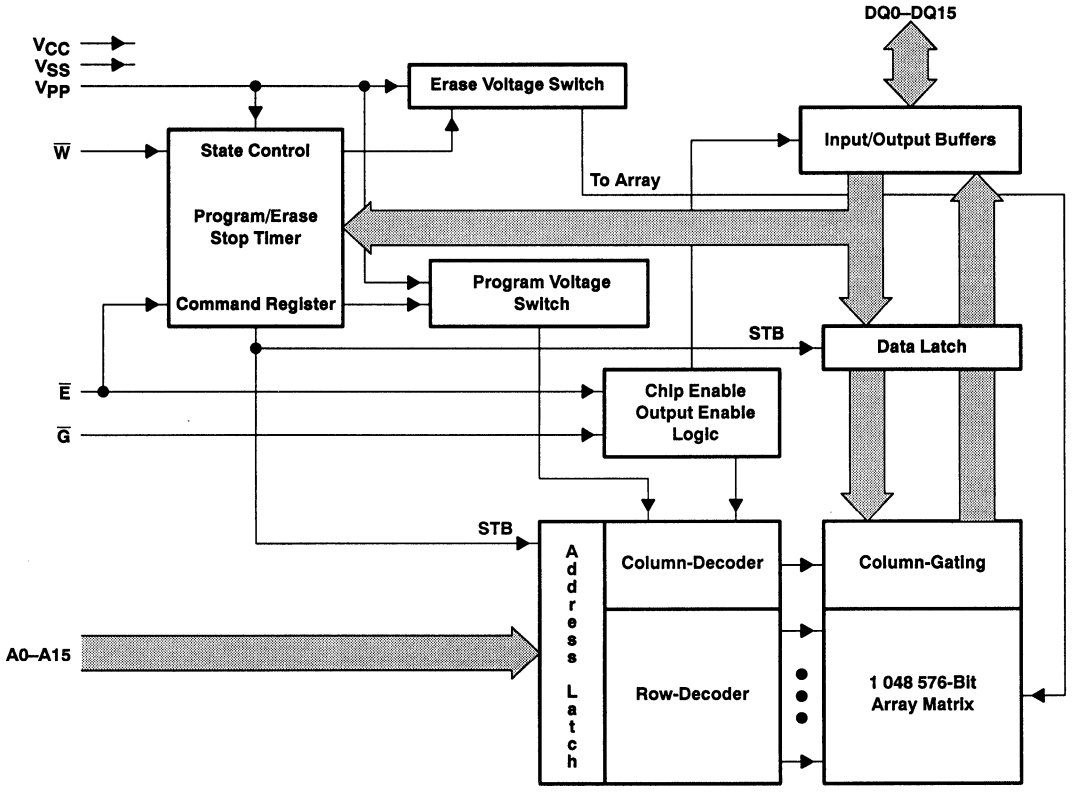
PRODUCT PREVIEW

device symbol nomenclature



PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Table 1. Operation Modes

MODE†		FUNCTION						
		V_{PP}§	$\overline{E}$	$\overline{G}$	A0	A9	$\overline{W}$	DQ0–DQ15
	N PACKAGE	1	2	20	21	31	39	3–10, 12–19
	FN PACKAGE	2	3	22	24	35	43	21–14, 11–4
Read	Read	V_{PPL}	V_{IL}	V_{IL}	X†	X	V_{IH}	Data Out
	Output Disable	V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPL}	V_{IH}	X	X	X	X	HI-Z
	Signature	V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_H‡	V_{IH}	MFG Code 0097h
					V_{IH}			Device Code 00E5h
Read/ Write	Read	V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	HI-Z
	Standby and Write Inhibit	V_{PPH}	V_{IH}	X	X	X	X	HI-Z
	Write	V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}
‡ 11.5 V < V_H < 13.0 V
§ $V_{PPL} \le V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

PRODUCT PREVIEW

operation

read/output disable

When the outputs of two or more TMS28F210s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices.

To read the output of the TMS28F210, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 50 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 μA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F210 draws active current when it is deselected during programming, erasure, or program/erase verification. It will continue to draw active current until the operation is terminated.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 (pin 31, J package; pin 35, FN package) is forced to V_H. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer's code 0097h, and A0 high selects the device code 00E5h, as shown in the signature mode table below:

IDENTIFIER†	PINS‡									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer Code	V_{IL}	1	0	0	1	0	1	1	1	0097
Device Code	V_{IH}	1	1	1	0	0	1	0	1	00E5

† $\overline{E}$ = $\overline{G}$ = V_{IL}, A1–A8 = V_{IL}, A9 = V_H, A10–A15 = V_{IL}, V_{PP} = V_{PPL}.
‡ Upper 8 data bits will read 0.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1s, may be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

command register

The command register controls the program and erase functions of the TMS28F210. The signature mode may be activated using the command register in addition to the above method. When V_{PP} is high, the contents of the command register, and therefore the function being performed, may be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1-μF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} will require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION (see Note 1)	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read	1	Write	X	0000h	Read	RA	RD
Signature Mode	3	Write	X	0090h	Read	0000 0001	0097h 00E5h
Set-up Erase/Erase	2	Write	X	0020h	Write	X	20h
Erase Verify	2	Write	EA†	00A0h	Read	X	EVD
Set-up Program/Program	2	Write	X	0040h	Write	PA	PD
Program Verify	2	Write	X	00C0h	Read	X	PVD
Reset	2	Write	X	00FFh	Write	X	00FFh

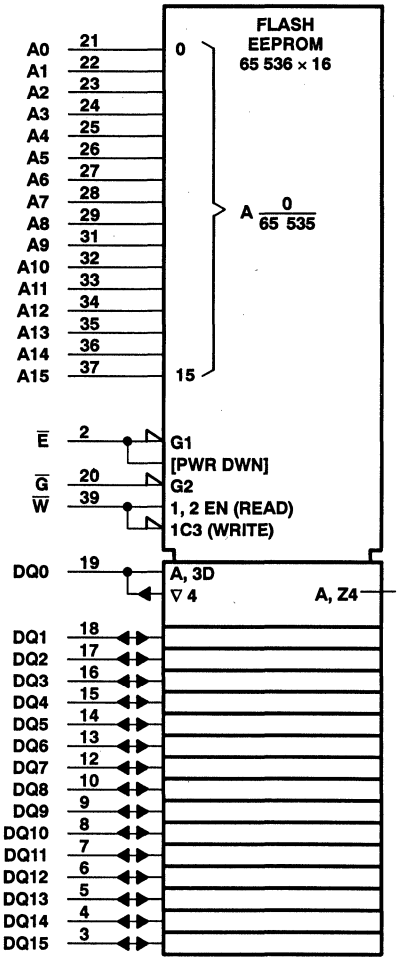
NOTE 1: Modes of operation are defined in Table 1.

† Description of Terms

EA Address of memory location to be read during erase verify.
RA Address of memory location to be read.
PA Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD Data read from location RA during the read operation.
EVD Data read from location EA during erase verify.
PD Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD Data read from location PA during program verify.

PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

PRODUCT PREVIEW

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 0000h into the command register invokes the read operation. Also, when the device is powered up, the default contents of the command register are 0000h and the read operation is enabled. The read operation remains enabled until a different, valid command is written to the command register.

signature mode command

The signature mode is activated by writing 0090h into the command register. The manufacturer's code (97h) is identified by the value read from address location 0000h, and the device code (00E5h) is identified by the value read from address location 0001h.

set-up erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, V_{PP} = 12 V, and V_{CC} = 5 V. To enter the erase mode, write the set-up erase command, 0020h, into the command register. After the TMS28F210 is in the erase mode, writing a second erase command, 0020h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, 00A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase verify, read, or reset command is received.

erase-verify command

All words must be verified following an erase operation. After the erase operation is complete, an erased word can be verified by writing the erase-verify command, 00A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the word to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

To determine whether or not all the words have been erased, the TMS28F210 applies a margin voltage to each word. If FFFFh is read from the word, then all bits in the designated word have been erased. The erase-verify operation continues until all of the words have been verified. If FFFFh is not read from a word, then an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F210.

set-up program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, V_{PP} = 12 V, and V_{CC} = 5 V. To enter the programming mode, write the set-up program command, 0040h, into the command register. The programming operation will be invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, 00C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program verify, read, or reset command is received.

program-verify command

The TMS28F210 can be programmed sequentially or randomly because it is programmed one word at a time. Each word must be verified after it is programmed.

The program-verify operation prepares the device to verify the most recently programmed word. To invoke the program-verify operation, 00C0h must be written into the command register. The program-verify operation will end on the rising edge of $\overline{W}$.

While verifying a word, the TMS28F210 applies an internal margin voltage to the designated word. If the true data and programmed data match, programming can continue to the next designated word location; otherwise, the word must be reprogrammed. Figure 1 shows how commands and bus operations are combined for word programming.

reset command

To reset the TMS28F210 after set-up erase command or set-up program command operations without changing the contents in memory, write 00FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F210 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

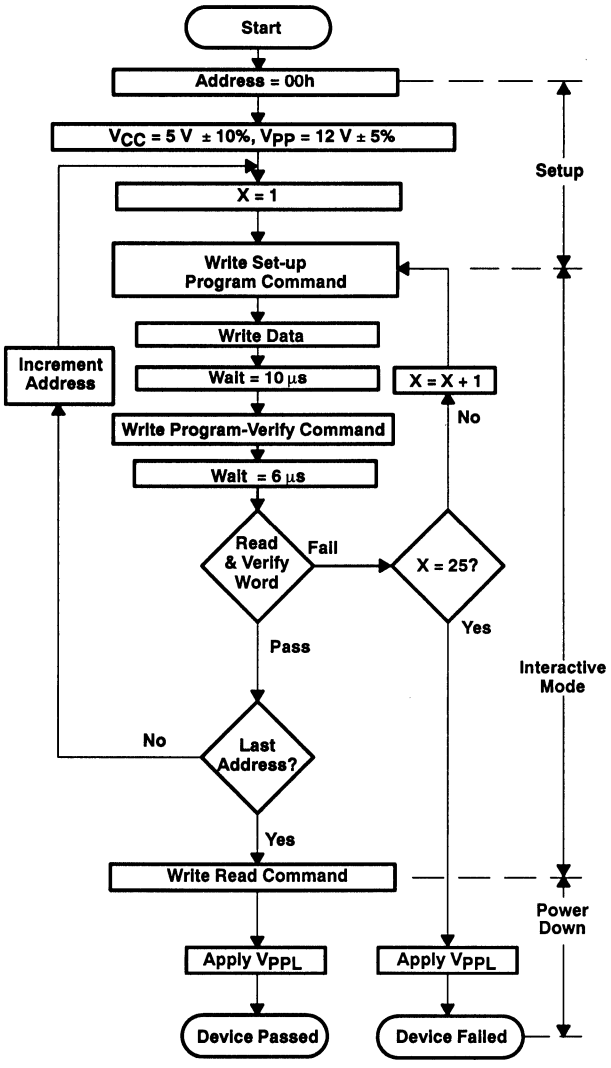
Fasterase algorithm

The TMS28F210 is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices may be erased in parallel. Since each Flash EEPROM may erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished. See Figure 3, Parallel Erase Flow Diagram.

Examples of how to mask a device during parallel erase include driving the device's $\overline{E}$ pin high, writing the read command (0000h) to the device when the others receive a setup erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.

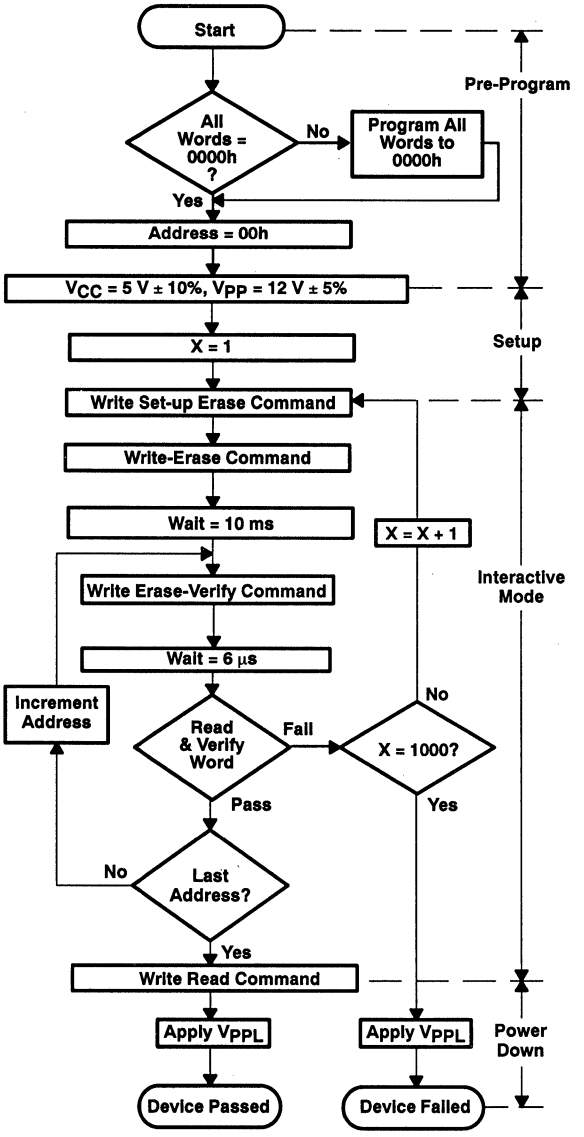


Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for VPP to Ramp to VPPH (see Note 2) Initialize Pulse Count
Write	Set Up Program Write	Data = 0040h
Write	Write Data	Valid Address/Data
Standby		Wait = 10 µs
Write	Program-Verify	Data = 00C0h; Ends Program Operation
Standby		Wait = 6 µs
Read		Read Word to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 0000h; Resets Register for Read Operations
Standby		Wait for VPP to Ramp to VPPL (see Note 3)

NOTES: 2. Refer to the recommended operating conditions for the value of V_{PPH}.
3. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

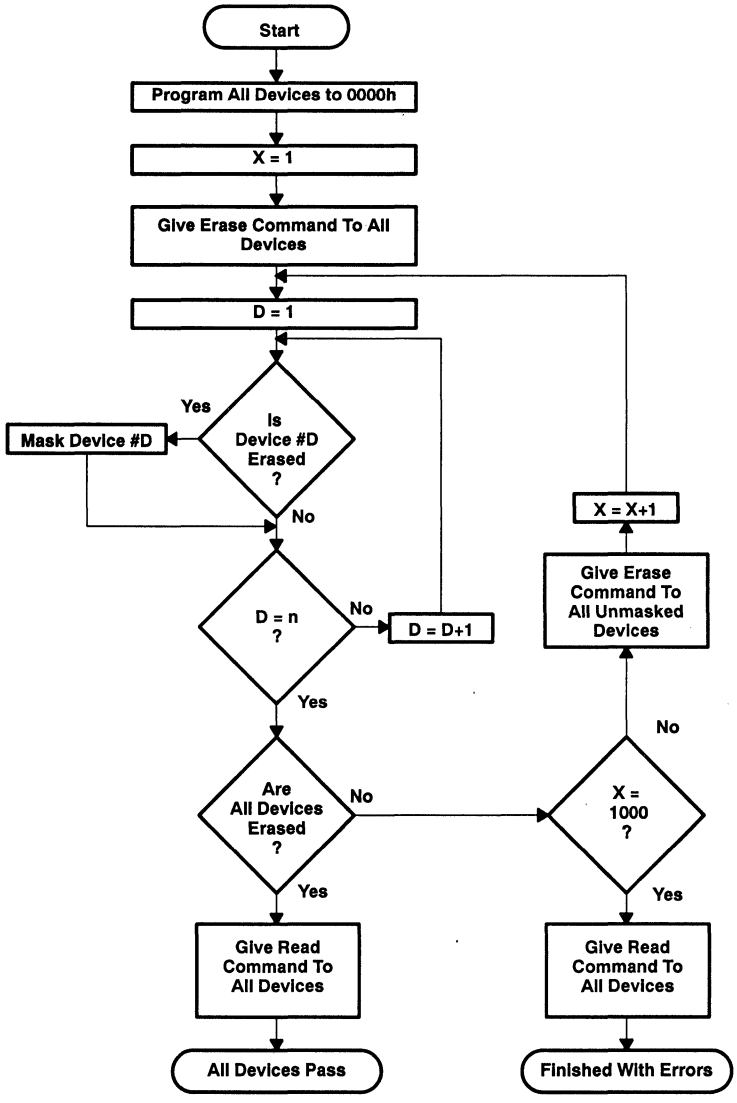
PRODUCT PREVIEW



Bus Operation	Command	Comments
		Entire Memory Must = 0000h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait for V_{PP} to Ramp to V_{PPH} (see Note 2)
		Initialize Pulse Count
Write	Set Up Erase	Data = 0020h
Write	Erase	Data = 0020h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Word to Verify; Data = 00A0h; Ends the Erase Operation
Standby		Wait = 6 µs
Read		Read Word to Verify Erasure; Compare Output to FFFFh
Write	Read	Data = 0000h; Resets Register for Read Operations
Standby		Wait for V_{PP} to Ramp to V_{PPL} (see Note 3)

NOTES: 2 Refer to the recommended operating conditions for the value of V_{PPH}.
3 Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm



NOTE: n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 5): All inputs except A9 ..... −0.6 V to V_{CC} + 1 V
A9 (see Note 5) ..... −0.6 V to 13.5 V
Output voltage range (see Note 6) ..... −0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program (NL, FNL) ..... 0°C to 70°C
Operating free-air temperature range during read/erase/program (NE, FNE) ..... − 40°C to 85°C
Operating free-air temperature range during read/erase/program (NQ, FNQ) ..... − 40° C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to GND.
5. The voltage on any input pin may undershoot to −2.0 V for periods less than 20 ns.
6. The voltage on any output pin may overshoot to 7.0 V for periods less than 20 ns.

PRODUCT PREVIEW

recommended operating conditions

				'28F210-10 '28F210-12 '28F210-15 '28F210-17			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	During write/read/flash erase		4.5	5	5.5	V
V_{PP}	Supply voltage	During read only (V_{PPL})		0		V_{CC} + 2	V
		During write/read/flash erase (V_{PPH})		11.4	12	12.6	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} − 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	GND − 0.2		GND+0.2	

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	2.4			V
			I_{OH} = – 100 µA	V_{CC} – 0.4			
V_{OL}	Low-level output voltage		I_{OL} = 5.8 mA			0.45	V
			I_{OL} = 100 µA			0.1	
I_I	Input current (leakage)	All except A9	V_I = 0 to 5.5 V			±1	µA
		A9	VI = 0 to 13 V			± 200	
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current (read/standby)		V_{PP} = V_{PPH}, read mode			200	µA
			VPP = V_{PPL}			±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 7)		V_{PP} = V_{PPH}			50	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 7)		V_{PP} = V_{PPH}			50	mA
I_{PP4}	VPP supply current (during program/erase verify) (see Note 7)		V_{PP} = V_{PPH}			5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			100	µA
I_{CC1}	V_{CC} supply current (active read)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, f = 6 MHz, outputs open			50	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, programming in progress			10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, erasure in progress			15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 7)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, V_{PP} = V_{PPH}, program/erase-verify in progress			15	mA

NOTE 7: Not 100% tested; characterization data available.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0 , f = 1MHz			6	pF
C_O	Output capacitance	V_O = 0 , f = 1 MHz			12	pF

† Capacitance measurements are made on sample basis only.

PARAMETER MEASUREMENT INFORMATION

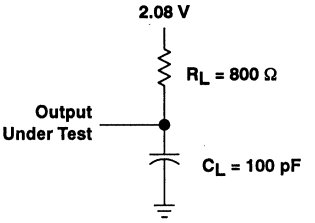
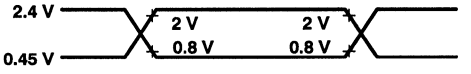


Figure 4. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-μF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

PRODUCT PREVIEW

switching characteristics over full ranges of recommended operating conditions

DESCRIPTION		TEST CONDITIONS	ALTERNATE SYMBOL	'28F210-10		'28F210-12		'28F210-15		'28F210-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load Input $t_r \le 20$ ns Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from chip enable		t_{ELQV}		100		120		150		170	ns
$t_{en(G)}$	Access time from output enable		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Read cycle time		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, output enable low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{wr(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first.

AC characteristics–write/erase/program operations

DESCRIPTION		ALTERNATE SYMBOL	'28F210-10		'28F210-12		'28F210-15		'28F210-17		UNIT
			MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVWL}	0		0		0		0		ns
$t_{h(A)}$	Address hold time	t_{WLAX}	55		60		60		70		ns
$t_{su(D)}$	Data setup time	t_{DVWH}	50		50		50		50		ns
$t_{hw(D)}$	Data hold time	t_{WHDX}	10		10		10		10		ns
$t_{wr(W)}$	Write recovery time before read	t_{WHGL}	6		6		6		6		µs
$t_{rr(W)}$	Read recovery time before write	t_{GHWL}	0		0		0		0		µs
$t_{su(E)}$	Chip enable setup time before write	t_{ELWL}	20		20		20		20		ns
$t_{h(E)}$	Chip enable hold time	t_{WHEH}	0		0		0		0		ns
$t_{w(W)}$	Write pulse duration (see Note 8)	t_{WLWH}	60		60		60		60		ns
$t_{wh(W)}$	Write pulse duration high	t_{WHWL}	20		20		20		20		ns
$t_{c(W)B}$	Duration of programming operation	t_{WHWH1}	10		10		10		10		µs
$t_{c(E)B}$	Duration of erase operation	t_{WHWH2}	9.5	10	9.5	10	9.5	10	9.5	10	ms
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{su(E)P}$	Chip enable, setup time to V_{PP} ramp	t_{EHVP}	100		100		100		100		ns
$t_{s(P)R}$	V_{PP} rise time	t_{VPPR}	1		1		1		1		µs
$t_{s(P)F}$	V_{PP} fall time	t_{VPPF}	1		1		1		1		µs

NOTE 8: Rise/fall time ≤ 10 ns.

PRODUCT PREVIEW

alternative $\overline{CE}$-controlled writes

DESCRIPTION		ALTERNATE SYMBOL	'28F010-10		'28F010-12		'28F010-15		'28F010-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	t_{AVAV}	100		120		150		170		ns
$t_{su(A)}$	Address setup time	t_{AVEL}	0		0		0		0		ns
$t_{hE(A)}$	Address hold time	t_{ELAX}	75		80		80		90		ns
$t_{su(D)}$	Data setup time	t_{DVEH}	50		50		50		50		ns
$t_{hE(D)}$	Data hold time	t_{EHDX}	10		10		10		10		ns
$t_{wr(E)}$	Write recovery time before read	t_{EHGL}	6		6		6		6		µs
$t_{rr(E)}$	Read recovery time before write	t_{GHEL}	0		0		0		0		µs
$t_{su(W)}$	Write enable setup time before chip enable	t_{WLEL}	0		0		0		0		ns
$t_{h(W)}$	Write enable hold time	t_{EHWH}	0		0		0		0		ns
$t_{w(E)}$	Write pulse duration	t_{ELEH}	70		70		70		80		ns
$t_{wh(E)}$	Write pulse duration high	t_{EHEL}	20		20		20		20		ns
$t_{su(P)E}$	V_{PP} setup time to chip enable low	t_{VPEL}	1.0		1.0		1.0		1.0		µs
$t_{c(W)B}$	Duration of programming operation	t_{EHEH}	10		10		10		10		µs

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

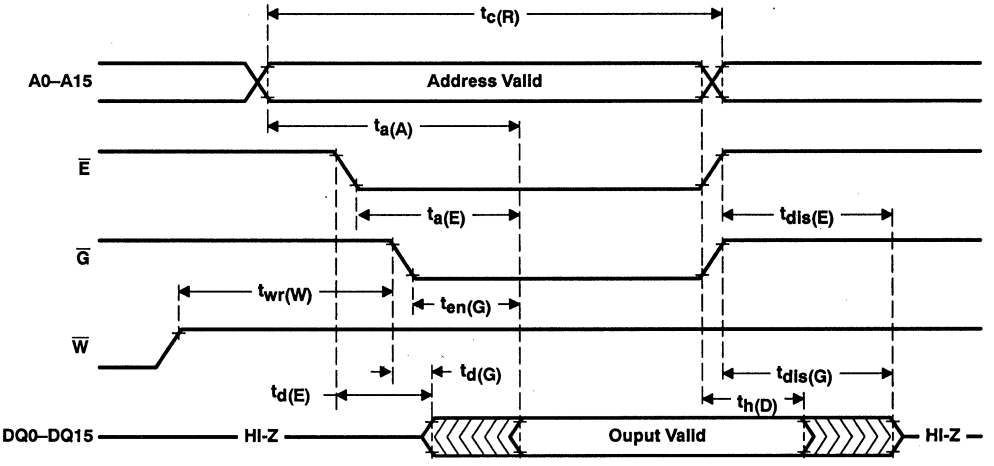


Figure 5. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

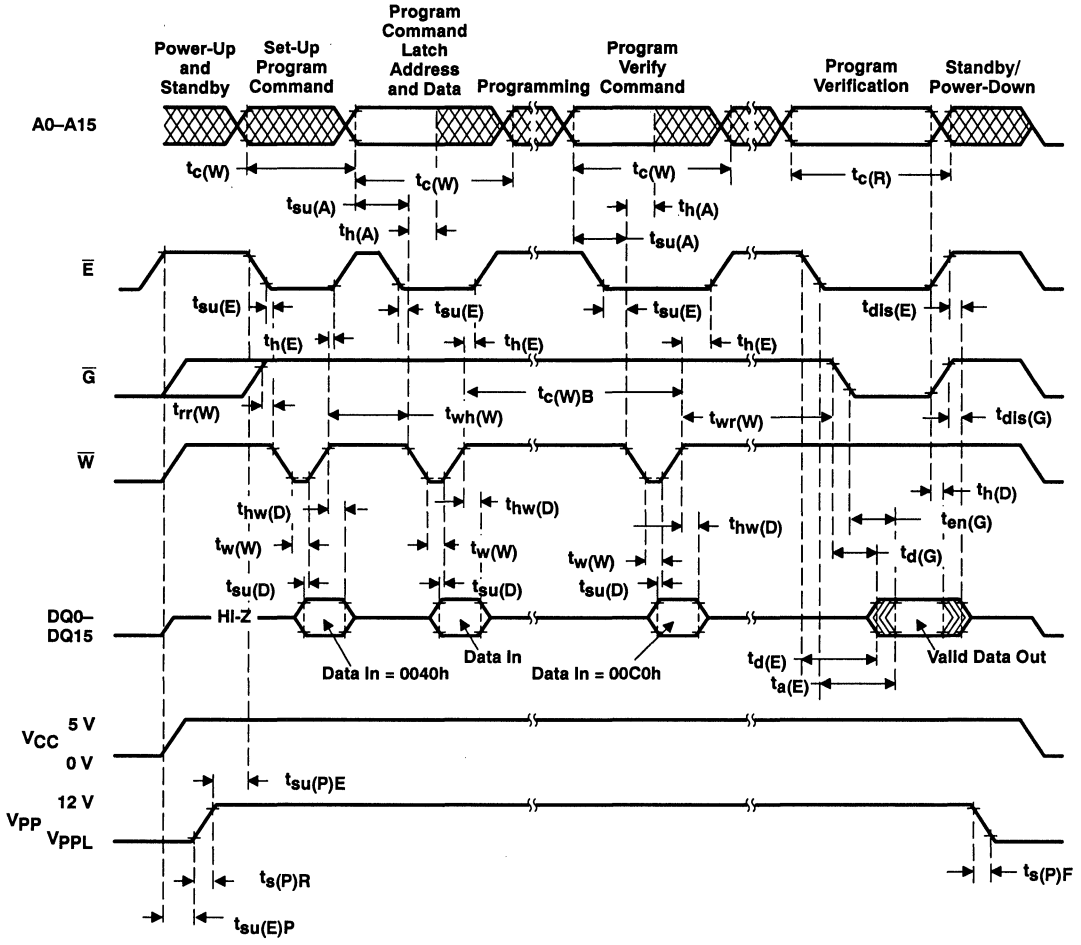


Figure 6. Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

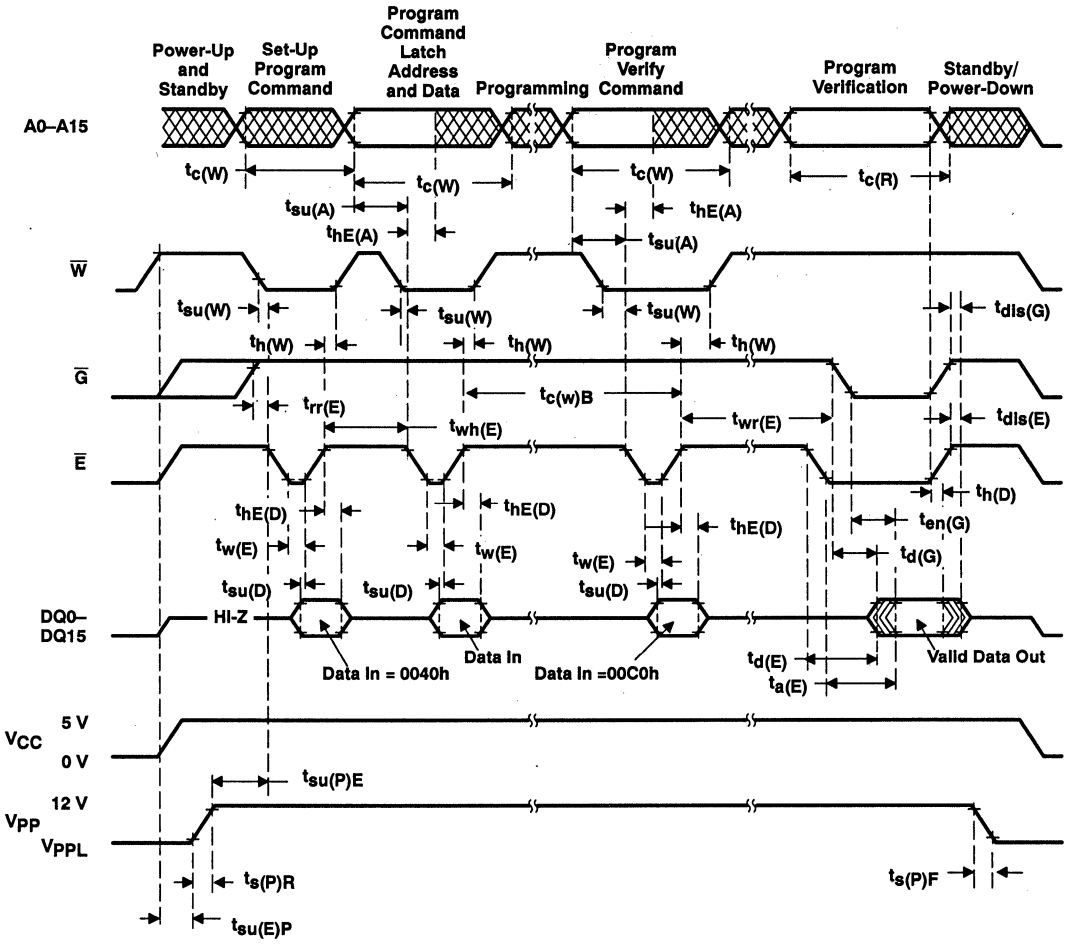


Figure 7. Write Cycle (Alternative $\overline{CE}$-Controlled Writes) Timing

PARAMETER MEASUREMENT INFORMATION

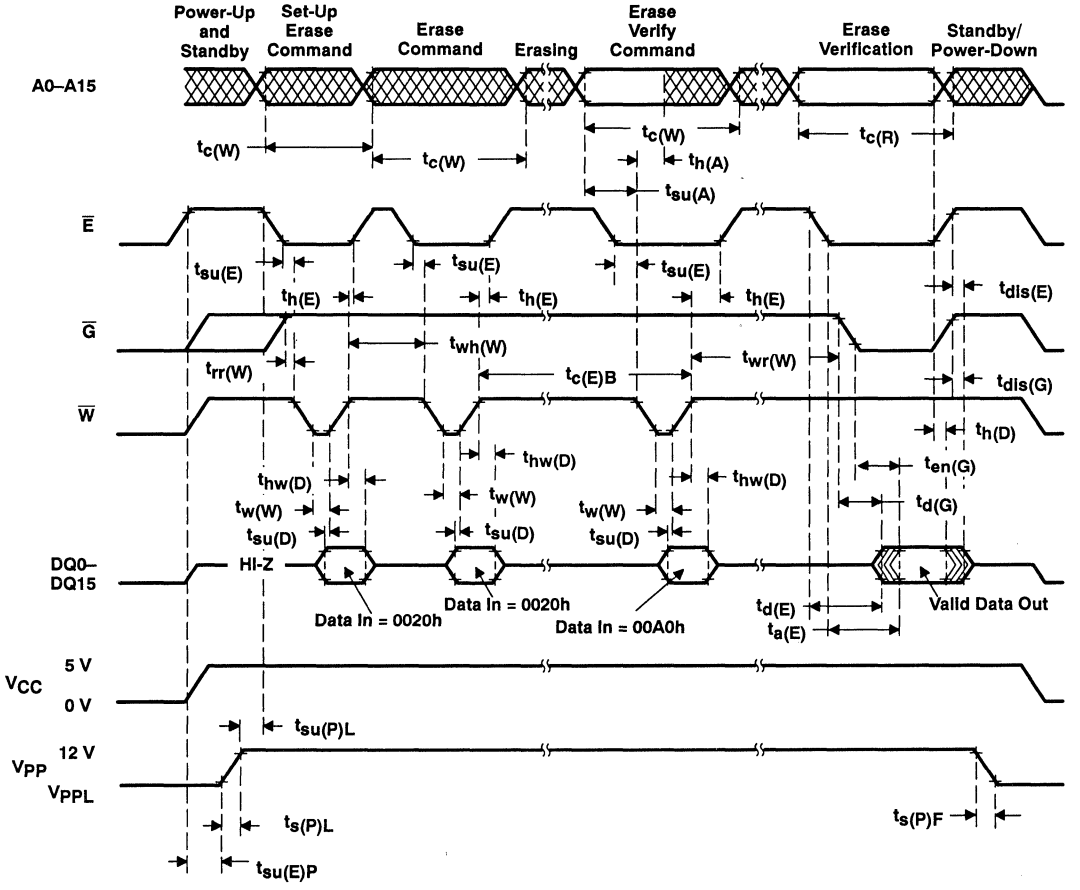
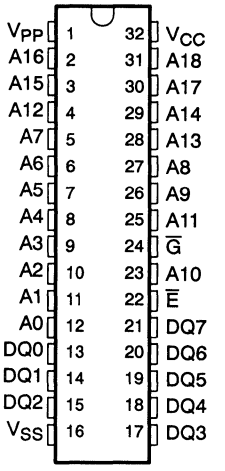


Figure 8. Flash-Erase Cycle Timing

PRODUCT PREVIEW

- **Organization . . . 512K × 8**
- **Separately Erasable 32K Byte Blocks**
- **Two Power Supplies (5 V and 12 V)**
- **100% TTL-Level Control Inputs**
- **Fully Automated On-Chip Erase and Byte Program Operations**
- **RAM-Like Write Setup/Read Timings for Standard Processor Interface**
- **10 000, 1000, and 100 Program/Erase Cycle Versions**
- **Automotive Temperature Range: – 40°C to 125°C**
- **Low Power Dissipation (V_{CC} = 5.50 V)**
  - **Active Write . . . 55 mW**
  - **Active Read . . . 165 mW**
  - **Electrical Erase . . . 82.5 mW**
  - **Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Pin Compatible With Existing 4-Megabit EPROMS**
- **All Inputs/Outputs TTL Compatible**
- **Chip Erase Before Reprogramming**

N PACKAGE†
(TOP VIEW)



† The package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
V_{PP}	12-V Power Supply
V_{CC}	5-V Power Supply
V_{SS}	Ground

description

The TMS28F040 is a 4 194 304 bit, programmable read-only memory that can be electrically erased (bulk-erased and block-erased) and re-programmed. This device is offered in 32-pin plastic DIP and 40-pin TSOP packages. The TMS28F040 is organized as 16 independent 32K byte blocks. Blocks may be dynamically marked read-only by configuring soft protection registers with command sequences. Embedded byte write and chip/block erase functions are fully automated by an on-chip write state machine (WSM), thus releasing the system processor for other tasks. A suspend/resume feature allows access to unaltered memory blocks during erase operations.

The TMS28F040 Flash EEPROM is offered in a dual in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) centers, a 40-lead thin small outline package (DD suffix), and reverse pinout TSOP package (DU suffix). The TMS28F040 is offered with two choices of temperature ranges of 0°C to 70°C (NL, DDL, and DUL suffixes) and – 40°C to 125°C (NQ, DDQ, and DUQ suffixes).

operation

Device operations are selected by writing JEDEC standard commands with conventional microprocessor timings into a command register through the I/O pins (DQ0–DQ7) while $V_{PP} = V_{PPH}$. The device is always in the read-only mode when $V_{PP} = V_{PPL}$. The content of the command register acts as input to an on-chip state machine. The command register latches commands as issued by system software and is not altered by write state machine (WSM) actions. It defaults to read array mode upon initial power-up. With an appropriate command written to the command register, standard processor accesses output stored data, device/mfg codes, or output status of program/erase operations for validation. The functions associated with altering memory contents are program, erase, protection, and status. These functions are accessed via the command register and validated through the status register. The signature register may be accessed while $V_{PP} \leq V_{PPH}$ by applying $A9 = V_{ID}$. High voltage (V_{PPH}) on V_{PP} enables device erasure and programming.

PRODUCT PREVIEW

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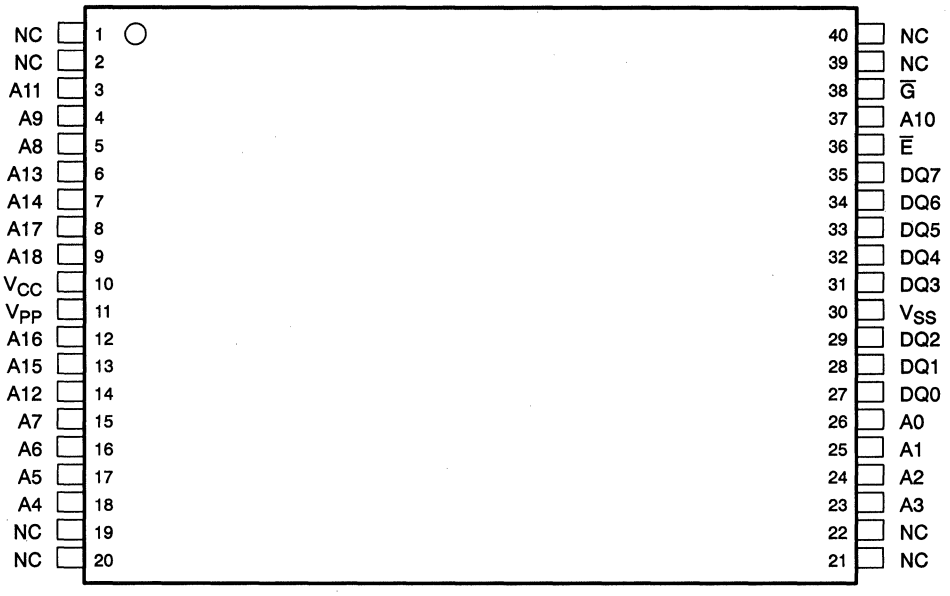
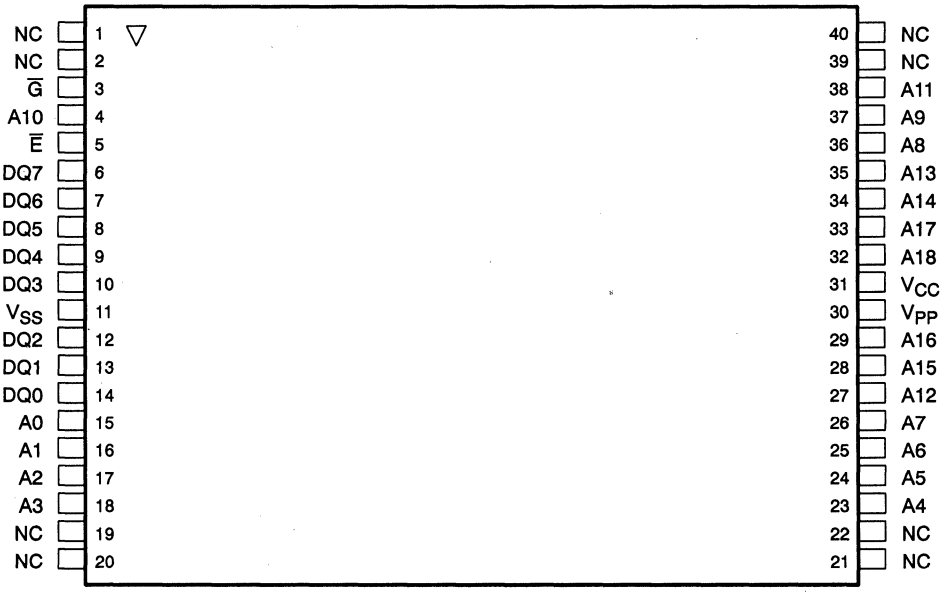
DD PACKAGE†
(TOP VIEW)

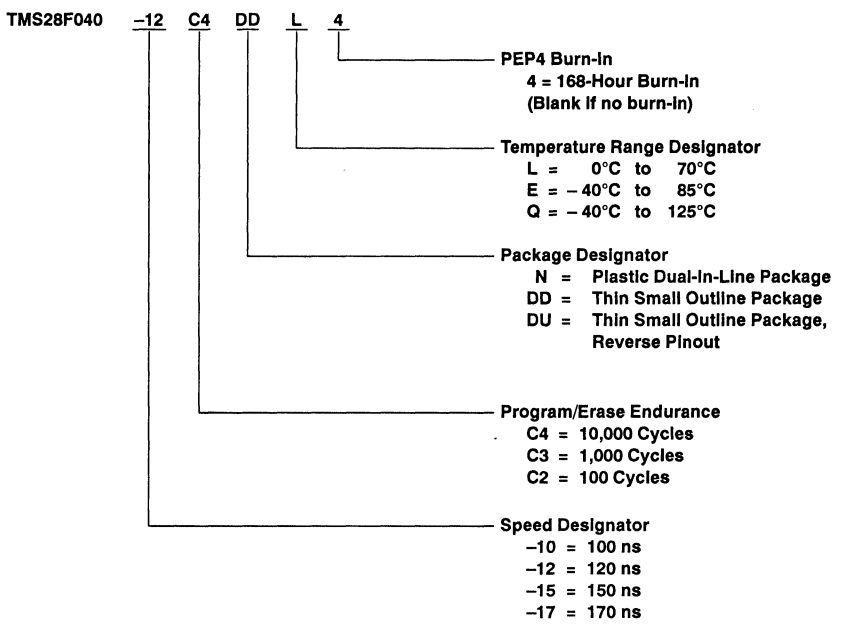


DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)



† The package shown is for pinout reference only.

device symbol nomenclature



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functional block diagram

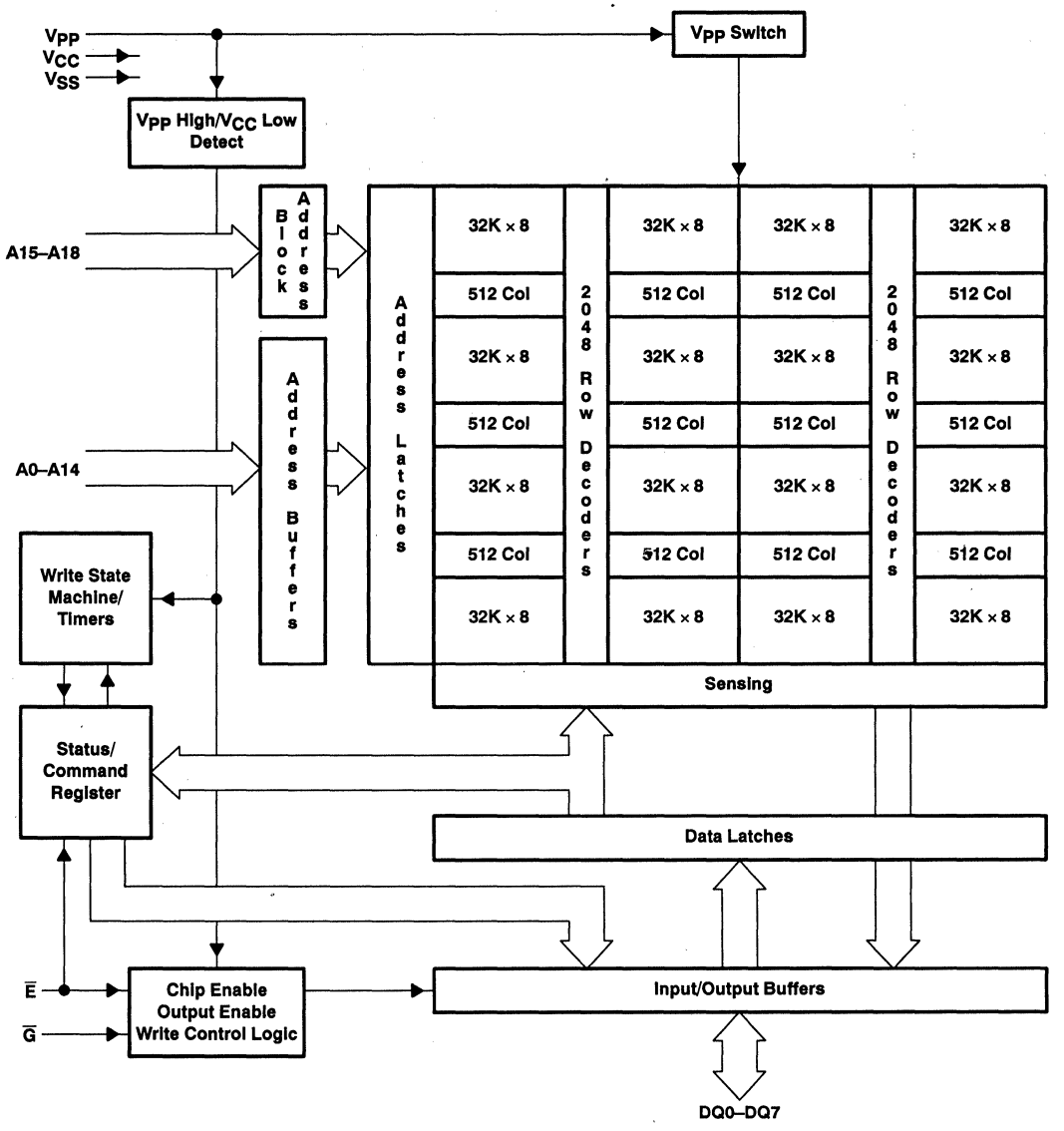

Table 1. Operation Modes

MODE	$\overline{E}$	$\overline{G}$	V_{PP}	A9	A0	DQ0–DQ7
Read-Only	V_{IL}	V_{IL}	V_{PPL}	X	X	DOUT
Read	V_{IL}	V_{IL}	X	X	X	DOUT
Output Disable	V_{IL}	V_{IH}	V_{PPL}	X	X	High-Z
Standby	V_{IH}	X	X	X	X	High-Z
Signature (Mfr)	V_{IL}	V_{IL}	X	V_{ID}	V_{IL}	97h
Signature (Device)	V_{IL}	V_{IL}	X	V_{ID}	V_{IH}	79h
Write	V_{IL}	V_{IH}	V_{PPH}	X	X	DIN

NOTES: 1. X can be V_{IL} or V_{IH} for control pins or addresses, and V_{PPL} or V_{PPH} for V_{PP}.
2. Write/Erase operations will continue during standby until completed.
3. Block erase, chip erase, and byte programming commands are assured only when $V_{PP} = V_{PPH}$.

access modes

The TMS28F040 is configured as read-only while $V_{PP} = V_{PPL}$. Commands to initiate status reads and program/erase operation are possible with $V_{PP} = V_{PPH}$. The memory address space consists of sixteen 32K × 8-bit blocks indexed by address inputs A15–A18.

read access

While $V_{PP} = V_{PPL}$, the TMS28F040 is configured for read-only access; program and erase operations are not available. When $V_{PP} = V_{PPH}$, a read cycle must assert $\overline{G}$ low with $\overline{E} = V_{IL}$. Hardware signature read is always available.

write access

Write access is available when $V_{PP} = V_{PPH}$. Commands, data, and addresses are latched by the TMS28F040 using the $\overline{E}$ input. A write cycle is defined as $\overline{E}$ switching low with $\overline{G}$ high and $V_{PP} = V_{PPH}$. Command or program data are latched on the rising edge of $\overline{E}$. Addresses are latched on the falling edge of $\overline{E}$. Software signature, status, polling, suspend/resume, and program/erase commands are functional during write access.

read modes

The TMS28F040 always operates in one of three read modes. The read mode is latched by writing an initiation command and remains latched regardless of subsequent program and erase operations. Only the read memory mode is available when $V_{PP}=V_{PPL}$.

read memory data/poll bits

Upon initial power up, the device defaults to the read memory mode. This mode can also be set at any time by writing either of the commands FFh or 00h. The mode remains latched until one of the other two read modes is initiated. The read array commands are functional when $V_{PP}=V_{PPL}$ or V_{PPH}.

The data available while in the read memory mode, when $V_{PP}=V_{PPH}$, is dependent on the state of the write state machine. If the WSM is not performing a program or erase operation, the standard processor read cycles simply retrieve the array data. If the WSM is busy, the system processor may read the data poll bit (DQ7) and the toggle bit (DQ6) to test for operation progress and completion. The behavior of these bits is described in a later section.

read status register

The device contains a status register than can be read to determine the status of the automated program/erase operations. This register is read by writing the command 70h. Following the write command 70h, all subsequent read cycles output data from the status register until one of the other two read modes is initiated. The status register is updated automatically by the write state machine. The purpose and behavior of the bits of the status register are described in a separate section. The read status register command is functional when $V_{PP}=V_{PPH}$.

read signature mode

The signature operation outputs the manufacturer code (97h) and device code (79h). This mode can be entered through either a hardware or software operation.

The read signature mode may be latched through software by writing the command 90h. Upon latching 90h, asserting A0 = V_{IL} outputs the manufacturer code, while setting A0 = V_{IH} produces the device code. This mode remains effective until one of the other two read modes is initiated. The read signature command is functional when V_{PP}=V_{PPH} and is accessible from any operating mode.

Alternatively, the hardware implementation is achieved by setting $\overline{E}$=$\overline{G}$=V_{IL}, A9=V_{ID} and A0 = V_{IL} or V_{IH}. When A0 = V_{IL}, the output represents the manufacturer code. The device code is output when A0 = V_{IH}. The hardware signature access is not latched. Once A9 returns to V_{IL} or V_{IH}, the device returns to the previously latched read mode.

standby mode

When $\overline{E}$ = V_{IH}, the device is in standby mode where much of the circuitry is disabled resulting in lower power consumption. In this mode, the output pins (DQ0–DQ7) are placed in high-impedance state irrespective of $\overline{G}$. An erase/program operation will continue during standby until completed.

output disable

When $\overline{G}$ = V_{IH} or $\overline{E}$ = V_{IH}, the device outputs are disabled and the output pins (DQ0–DQ7) are placed in high-impedance state.

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write/erase modes

The TMS28F040 offers fully automated block erase, chip erase, and byte program operating modes. All pulse generation, preconditioning, and verification is handled by the on-chip write state machine. Upon initial power-up, the device defaults to reading memory data. Program and erase operations require two command cycles to initiate. Program and erase operations are accepted when V_{PP} = V_{PPH}. Attempting to initiate a program or erase operation while V_{PP} = V_{PPL} will leave the array contents unaltered. Additionally, if V_{PP} drops sufficiently below V_{PPH} during a program or erase operation, the operation will be aborted. If V_{CC} drops below V_{LKO}, any operation in progress will be aborted, new operations will be locked out, and the device will return to the read array mode. If any operation is in progress or suspended, write/erase mode commands will be ignored until the operation in progress completes.

block erase

Block erase will initialize the contents of a single unprotected block to all 1s. Block erase is initiated by the command sequence: block erase setup(20h) followed by block erase confirm(D0h). This command sequence is to ensure that memory contents are not accidentally erased. These commands are associated with a block address to be erased (A15–A18). Addresses are latched during the confirm command on the falling edge of $\overline{E}$. Command data is latched on the rising edge of $\overline{E}$. Block preconditioning, erase, and verify are handled by the write state machine, invisible to the system. Block erasure takes place when V_{PP} = V_{PPH} and V_{CC} > V_{LKO}. If the addressed block has been protected, the operation will abort with the erase status register flag SR.5 = V_{IH}.

chip erase

Chip erase is initiated by the command sequence: chip erase setup(30h) followed by chip erase confirm(30h). This command sequence is to ensure that memory contents are not accidentally erased. Command data is latched on the rising edge of $\overline{E}$. Chip erase is handled by the write state machine, invisible to the system. The chip erasure takes place only when V_{PP}=V_{PPH} and V_{CC} > V_{LKO}. Chip erase will set the memory contents of all unprotected blocks to 1s in a single erase operation. Individual blocks may be excluded from erasure by configuring the soft protection registers.

erase suspend/resume

The erase suspend command (B0h) allows interruption of a block erase operation in order to read data from an unaltered block of memory. Once the erase sequence is started, the erase suspend command (B0h) requests the write state machine to suspend the erase operation at predetermined breakpoints in the erase algorithm. The device operation status must be monitored to determine when the suspend has been executed (see related monitoring operation status section). After suspend has been granted, the read command should be written with appropriate address to read data from another block. V_{PP} is required to remain at V_{PPH} during the suspend so that the operation may be continued with a resume command. Block erase, chip erase, byte/word program, and soft protect commands are not accepted when any operation has been suspended. The erase sequence can be resumed with the erase resume command (D0h). An erase resume command must follow a suspend command before any other write/erase operation is allowed. If V_{PP} drops sufficiently below V_{PPH} during a suspended operation, the suspended operation will be aborted and a resume command must be given before another write/erase operation is accepted.

byte/word program

Byte programming is initiated by the command sequence: program setup (10h) followed by a write confirm command specifying address and data to be programmed. Addresses are latched during the confirm command on the falling edge of $\overline{E}$. Program data is latched on the rising edge of $\overline{E}$. Polling the device will determine when the program operation is complete. Ones (1s) cannot be programmed into any bit position and are ignored (e.g., programming FFh over an address location does not alter its data and does not return a fail condition).

soft protection

Data in the TMS28F040 is organized into sixteen separate 32K × 8-bit blocks indexed by address A15–A18. The device features the ability to protect the data stored in individual blocks from erasure and reprogramming. The protection mechanism is a bank of sixteen flags which can be set or reset through register commands. If a flag is set, it secures the data in the corresponding block by preventing all program/erase operations pertaining to that block. Upon power up, all flags are automatically cleared to allow unrestricted modification of the data array.

Alteration of the protection flags is a two bus-cycle process. On the first bus cycle, the software protect command, 0Fh, must be written to the device using the standard write cycle timings. On the next write strobe, a block address is latched into the address register on its falling edge and a keyword is latched into the data register on its rising edge. To have effect, the keyword must be one of the four patterns specifying the change as described in the command table. If data other than one of the four valid patterns is written on the second bus cycle, no change is made to the flag registers. Protection flags are not altered by V_{PP} transitions.

The benefit of this feature is that the end user can dynamically configure portions of the array as read-only. An attempt to alter data located in a protected block has no effect on its data. During an entire chip erase operation, protected blocks are unchanged and unprotected blocks are erased.

monitoring operation status

The status of the on-chip program and erase operations may be monitored when V_{PP}= V_{PPH}. The most complete monitoring method uses the status register. Alternatively, either the data poll bit (DQ7) or the toggle bit (DQ6) can be analyzed.

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Table 2. Status Register Bit Definitions

REGISTER BIT	DESCRIPTION		FUNCTION
	HIGH (1)	LOW (0)	
SR.7 (DQ7)	Ready	Busy	Write state machine ready
SR.6 (DQ6)	Suspended	In progress/completed	Erase suspended
SR.5 (DQ5)	Failure in chip/block erasure	Successful chip/block erasure	Erase status
SR.4 (DQ4)	Failure in byte program	Successful byte program	Program status
SR.3 (DQ3)	V_{PP} low detect/operation aborted	V_{PP} status ok	V_{PP} low
SR0–SR.2			Reserved

NOTES: 4. Register bits SR.7–SR.0 correspond with DQ7–DQ0 respectively.
5. The SR.7 bit must first be checked to determine program or erase completion before status bits are checked for program/erase success. The erase status bit (SR.5) and program status bit (SR.4) are set by the write state machine and can only be reset by the clear status register command (50h). Program/erase operations are not guaranteed when V_{PP} drops below V_{PPH}. If a command sequence error is detected (invalid confirm command), both the program (SR.4) and erase (SR.5) status bits will be set. Status bits SR.3–SR.0 are reserved and should be masked out when polling the status register.

status register

The status register bit definitions table summarizes this functional description. The status register can be monitored by issuing the read status register command, 70h, either before or after initiating a program/erase operation. After the read status register command is given, the status register remains available until the device is reset to the read array mode by the FFh or 00h commands or read signature mode 90h. Any number of memory modifications can be performed before returning to the read array mode.

The contents of the status register are updated automatically by the write state machine. After a program/erase command is issued and confirmed, the ready bit (DQ7) of the status register indicates that the operation is in progress. No other program/erase commands are effective when the ready bit is low. Polling the ready bit for V_{OH} determines when the operation is complete. Afterwards, the program status (DQ5), erase status (DQ4) and V_{PP} low (DQ3) bits of the status register can be analyzed to validate successful completion. If any of these are set, they can be cleared by issuing a clear status register command, 50h. To maximize system flexibility, no requirement is made to verify or clear the status bits before another operation is attempted. The status register is cleared only by the clear status register command so that any number of memory modifications may be made between status register checks. Any failure conditions that occur will accumulate in the status register between clear commands. The clear status register command is available when $V_{PP} = V_{PPH}$ and while no write erase operation is in progress or suspended.

The status register can be used to monitor the state of the device entering and exiting the suspend mode. After the suspend command (B0h) is given, the suspend bit (DQ6) will be set to V_{OH}. When a breakpoint is reached, the write state machine sets the ready bit DQ7 to V_{OH}. Ready bit DQ7 should be used to monitor when a suspend request has been granted, and the suspend bit DQ6 should be used to determine if a resume operation is necessary. If the write state machine is not busy, the suspend command is ignored and suspend bit DQ6 will not be set. To begin reading the array, one of the read array commands, 00h or FFh, must be issued if the device was in the read status register mode. After reading the array, the device can be returned to reading the status register by again writing 70h. The resume command, D0h, continues the erase operation and resets both the suspend and ready bits to V_{OL}.

V_{PP} low status bit DQ3 indicates a catastrophic V_{PP} supply failure during a program, erase, or suspend operation. This bit will be set if V_{PP} drops significantly below V_{PPH} while the write state machine is busy or suspended. Any operation that was in progress at that time will be aborted. The V_{PP} low status bit provides a valid indication of gross failure of the V_{PP} supply. V_{PP} loss for short duration or slightly below minimum operating levels might still corrupt data without the status register indicating a failure. It is left to the user to provide power supply integrity.

data polling and toggle bits

If the device is set in the read array mode before or during a program/erase operation, the poll bit and toggle bit will be available. One method to check for operation completion is to use the toggle bit (DQ6). This bit is available along with the data poll bit (DQ7) when the device is in the read array mode. While the write state machine is busy, the toggle bit switches logic states with each falling edge of $\overline{E}$ or $\overline{G}$. When the program or erasure is complete, the output pins automatically return to providing the data stored in the byte specified by the address pins. Therefore, when DQ6 stops toggling between two consecutive reads to the same address, the operation is complete. To confirm successful array modification, the status register may be read by issuing the read status register command, 70h.

By addressing an unaltered block, the toggle bit may also be used to determine when a suspend request has been granted. After the B0h command is given, the toggle bit will continue to switch logic states with each falling edge of $\overline{E}$ or $\overline{G}$ until the current operation is suspended. DQ6 stops toggling between two consecutive reads to the same address once the suspend request has been granted.

While the write state machine is busy, the data poll bit (DQ7) reflects the complement of the data stored in the seventh bit of the target data register. After the operation is complete, the device output pins automatically return to reading the byte specified by the address pins. Data bit DQ7 changing from complement to true indicates the end of an operation. When using this monitor method, the addresses should remain stable throughout the operation. During a block or chip erasure, the data poll bit (DQ7) is always low and returns high at successful completion. Should the device fail to erase or program, the data poll bit (DQ7) might not return to its uncomplemented state. Data polling is available after the second bus-cycle write sequence initiating a program/erase operation. The success of the modification can be verified when the byte data becomes available. The status register is always readable by issuing the read status register command, 70h.

Table 3. Command Definitions

COMMAND	BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS†	DATA†
Read Array	1	Write	X	00h			
Read Array	1	Write	X	FFh			
Signature	3	Write	X	90h	Read	IA	
Read Status Register	2	Write	X	70h	Read	X	SRD
Clear Status Register	1	Write	X	50h			
Automated Block Erase	2	Write	X	20h	Write	BA	D0h
Erase Suspend	1	Write	X	B0h			
Erase Resume	1	Write	X	D0h			
Automated Byte Program	2	Write	X	10h	Write	PA	PD
Automated Chip Erase	2	Write	X	30h	Write	X	30h
Soft Protect	2	Write	X	0Fh	Write	BA	PC

NOTES: 6. The command data is written through DQ0–DQ7.
7. Following the signature command, two read operations access the manufacturer code (97h) and device code (79h).

† Description of terms:
IA = signature address: 00000h for mfr code; 00001h for device code.
BA = any address within the block to be selected; latched on falling edge of $\overline{E}$.
PA = address of memory location to be programmed; latched on falling edge of $\overline{E}$.
SRD = data read from status register.
PD = data to be written at location PA. Data is latched on rising edge of $\overline{E}$.
PC = Protect Command.
: 00h = Clear all protection (enable chip W/E)
: FFh = Set all protection (disable chip W/E)
: F0h = Clear addressed block protection (enable block W/E)
: 0Fh = Set addressed block protection (disable block W/E)

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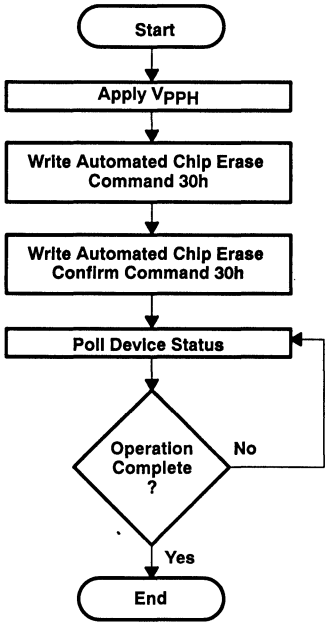

Figure 1. Automated Chip Erase Algorithm

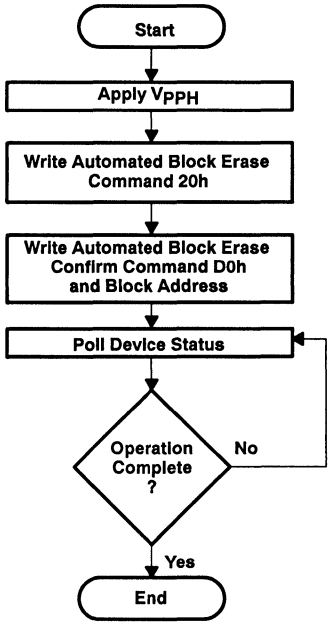

Figure 2. Automated Block Erase Algorithm

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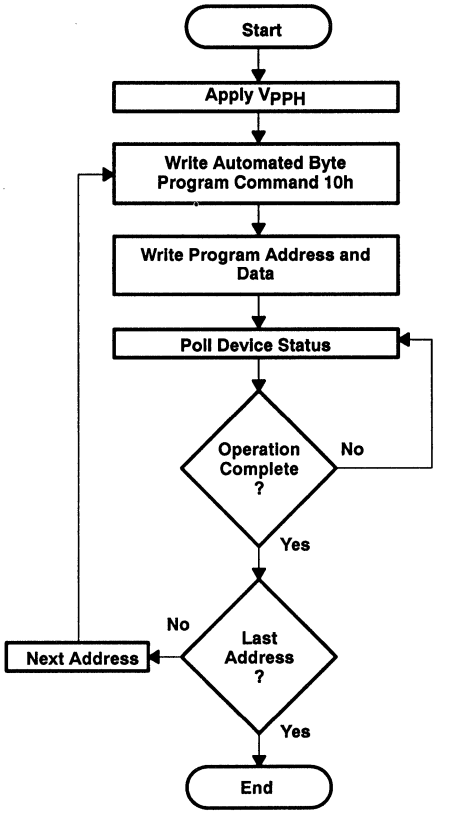

Figure 3. Automated Byte Program Algorithm

absolute maximum ratings over operating free-air termperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 8) ..... – 0.6 V to 7 V
Supply voltage, V_{PP} ..... – 0.2 V to 15 V
Input voltage range: All except A9 (see Note 9) ..... – 0.6 to 7 V
A9 (see Note 9) ..... –0.6 to 15 V
Output voltage ..... – 0.6 to 7 V
Operating free-air temperature range during read/erase/program
(NL, DDL, DUL) ..... 0°C to 70°C
Operating free-air temperature range during read/erase/program
(NQ, DDQ, DUQ) ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 8. All voltage values are with respect to the most negative supply voltage V_{SS}.
9. The voltage on any input pin may undershoot to –2.0 V for periods less than 20 ns.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		Operating Range	4.5	5	5.5	V
		V_{LKO}	Erase/Write Lock-Out	2.5			V
V_{PP}	Supply voltage	V_{PPL}	Read Mode	–2.0‡	0	V_{CC}+2	V
		V_{PPH}	Program/Erase Mode	11.4	12	12.6	V
V_{IH}	High-level input voltage	TTL		2		V_{CC}+0.5	V
		CMOS		V_{CC} – 0.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage	TTL		– 0.5		0.8	V
		CMOS		– 0.5		0.2	V
V_{ID}	A9 signature voltage			11.4		13	V
T_A	Operating free-air temperature	NL, DDL, DUL, suffix		0		70	°C
		NQ, DDQ, DUQ suffix		–40		125	

‡ Duration of V_{PP} undershoot must be < 20 ns.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	CMOS-output level	$I_{OH} = -20\ \mu A$	$V_{CC} - 0.2$		V
		TTL-output level	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Low-level output voltage	TTL-output level	$I_{OL} = 2.1$ mA		0.45	V
		CMOS-output level	$I_{OL} = 20\ \mu A$		0.1	V
I_I	Input current (leakage)		$V_I = 0$ to V_{CC}		±1	µA
I_O	Output current (leakage)		$\overline{E} = V_{IH}$, $V_O = 0$ to V_{CC}		±10	µA
I_{ID}	A9 signature mode current		A9 = V_{ID} MAX		200	µA
I_{CC1}	V_{CC} supply current (Standby)	TTL-input level	$\overline{E} = V_{IH}$, $V_{CC} = 5.5$ V		1	mA
		CMOS-input level	$\overline{E} = V_{CC} + 0.2$ V, $V_{CC} = 5.5$ V		100	µA
I_{CC2}	V_{CC} supply current (Read mode)		$\overline{E} = V_{IL}$, $V_{CC} = 5.5$ V, f = 6 MHz, $I_{OUT} = 0$ mA		40	mA
I_{CC3}	V_{CC} supply current (Program mode)		$V_{CC} = 5.5$ V, $\overline{G} = V_{IH}$, Programming in progress		30	mA
I_{CC4}	V_{CC} supply current (Erase mode)		$V_{CC} = 5.5$ V, $\overline{G} = V_{IH}$, Chip Erase in progress		30	mA
I_{CC5}	V_{CC} supply current (Erase Suspend)		$V_{CC} = 5.5$ V, $I_{OUT} = 0$ mA, Erase suspended, Block read at f = 6 MHz		40	mA
I_{PP1}	V_{PP} supply current (Standby)		GND ≤ V_{PP} ≤ V_{CC}, $\overline{E} = V_{IH}$		±10	µA
I_{PP2}	V_{PP} supply current (Read mode)		$V_{PP} = V_{PPH}$ MAX		200	µA
I_{PP3}	V_{PP} supply current (Program mode)		$V_{PP} = V_{PPH}$ MAX, Programming in progress		30	mA
I_{PP4}	V_{PP} supply current (Erase mode)		$V_{PP} = V_{PPH}$ MAX, Chip erase in progress		50	mA
I_{PP5}	V_{PP} supply current (Erase suspend)		$V_{PP} = V_{PPH}$ MAX, Erase suspended, Block read at f = 6 MHz		200	µA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	$V_I = 0$, f = 1 MHz		4	6	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		6	12	pF
C_{VPP}	V_{PP} input capacitance	$V_{PP} = 0$, f = 1 MHz		6	12	pF

switching characteristics over recommended operating free-air temperature range: read-only operation

DESCRIPTION		ALT. SYMBOL	'28F040-10		'28F040-12		'28F040-15		'28F040-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Read cycle time	t_{RC}	100		120		150		170		ns
t_{AVQV}	Access time from address	t_{ACC}		100		120		150		170	ns
	Output hold from Address, $\overline{E}$, or $\overline{G}$ change	t_{OH}	0		0		0		0		ns
t_{ELQV}	$\overline{E}$ to output valid	t_{CE}		100		120		150		170	ns
t_{ELQX}	$\overline{E}$ to output low Z	t_{LZ}	0		0		0		0		ns
t_{EHQZ}	$\overline{E}$ to output high Z	t_{HZ}		30		30		35		40	ns
t_{GLQV}	$\overline{G}$ to output valid	t_{OE}		50		55		60		65	ns
t_{GLQX}	$\overline{G}$ to output low Z	t_{OL}	0		0		0		0		ns
t_{GHQZ}	$\overline{G}$ to output high Z	t_{DF}		30		30		35		40	ns
t_{VCS}	V_{CC} setup time to valid read	t_{VCS}	20		20		20		20		µs
t_{GLWL}	$\overline{G}$ read setup time to $\overline{E}$ high†	t_{GLWL}	20		20		20		20		ns
t_{GLWH}	$\overline{G}$ read pulse duration†	t_{GLWH}	40		45		50		55		ns

† Required when $V_{PP} = V_{PPH}$.

switching characteristics over recommended operating free-air temperature range: write, erase, program operations

PARAMETER		ALT. SYMBOL	'28F040-10		'28F040-12		'28F040-15		'28F040-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Write cycle time	t_{WC}	100		120		150		170		ns
t_{AVWH}	Address setup time	t_{AS}	0		0		0		0		ns
t_{WHAX}	Address hold time	t_{AH}	45		50		55		60		ns
t_{GHWL}	$\overline{G}$ write setup time	t_{GHWL}	0		0		0		0		ns
t_{GHWH}	$\overline{G}$ write hold time	t_{GHWH}	5		5		5		5		ns
t_{VPWL}	V_{PP} setup to $\overline{E}$ write strobe‡	t_{VPS}	60		60		60		60		ns
t_{WLWH}	$\overline{E}$ write strobe pulse duration	t_{WP}	40		45		50		55		ns
t_{WHWL}	$\overline{E}$ write strobe pulse duration high	t_{WPH}	20		20		20		20		ns
t_{DVWH}	Data setup to $\overline{E}$ high	t_{DS}	20		20		20		20		ns
t_{WHDX}	Data hold time	t_{D}	10		10		10		10		ns
t_{VPPR}	V_{PP} rise time (90% V_{PPH})	t_{VPPR}	500		500		500		500		ns
t_{VPPH}	V_{PP} hold time	t_{VPPH}	0		0		0		0		ns
t_{WHWH1}	Duration of program operation	t_{WHWH1}	8.6	529	8.6	529	8.6	529	8.6	529	µs
t_{WHWH2}	Duration of block erase operation	t_{WHWH2}	0.1	62.5	0.1	62.5	0.1	62.5	0.1	62.5	s
t_{WHWH3}	Duration of chip erase operation	t_{WHWH3}	2.6	184	2.6	184	2.6	184	2.6	184	s

‡ $\overline{E}$ must equal V_{IH} during V_{PP} transitions.

PRODUCT PREVIEW

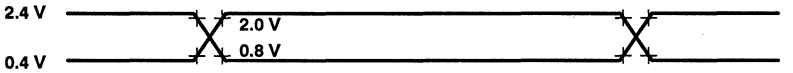
automated erase and programming performance†

PARAMETER	MIN	TYP	MAX	UNIT
Byte programming time	8.60	45	529	µs
Block erase time	0.10	2	62.5	s
Block programming time	0.28	1.5	17.3	s
Chip erase time	2.60	12.2	184	s
Chip programming time	2.26	23.6	277	s
Suspend latency time	0	3	10.1	ms

† All times include on-chip preconditioning, pulse generation, and verification.

PARAMETER MEASUREMENT INFORMATION

AC input/output reference waveform



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic high and 0.8 V logic low on both inputs and outputs. Each device should have a 0.1 µF ceramic capacitor between V_{CC} and V_{SS} as close as possible to the device pins.

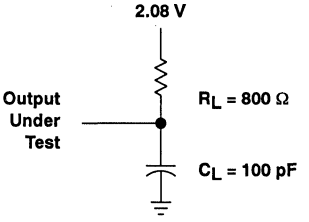


Figure 4. Output Load Circuit

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

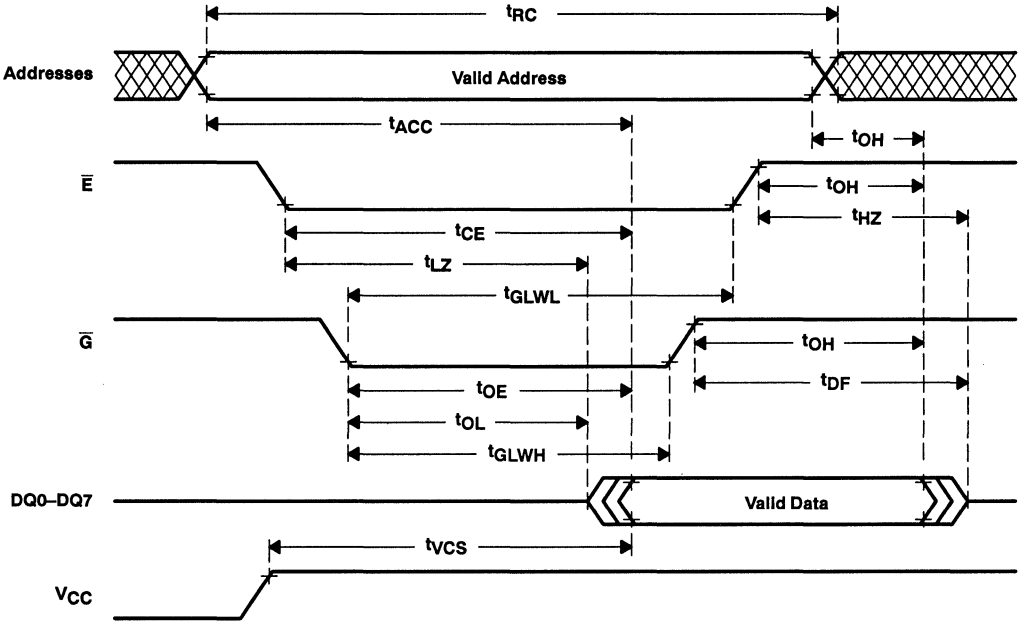
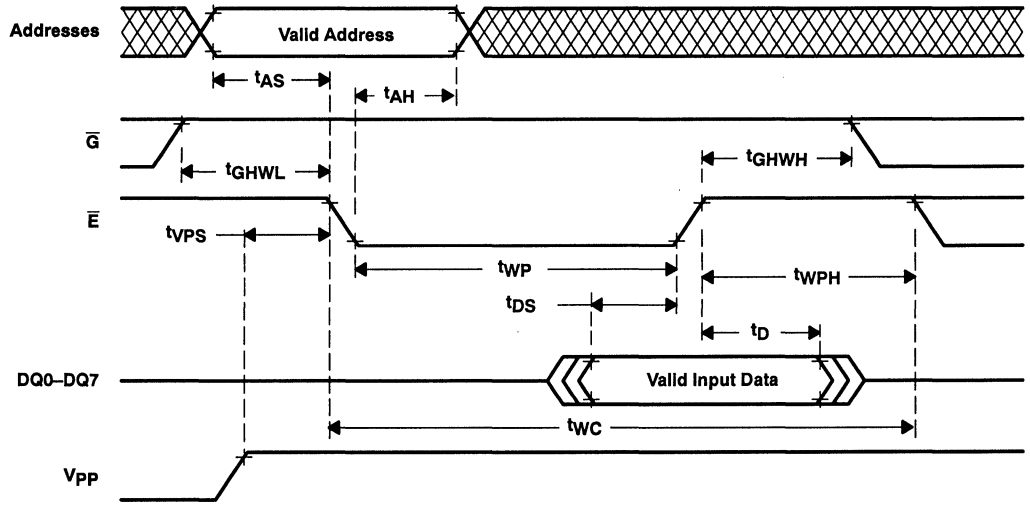


Figure 5. AC Waveform for Read Operations

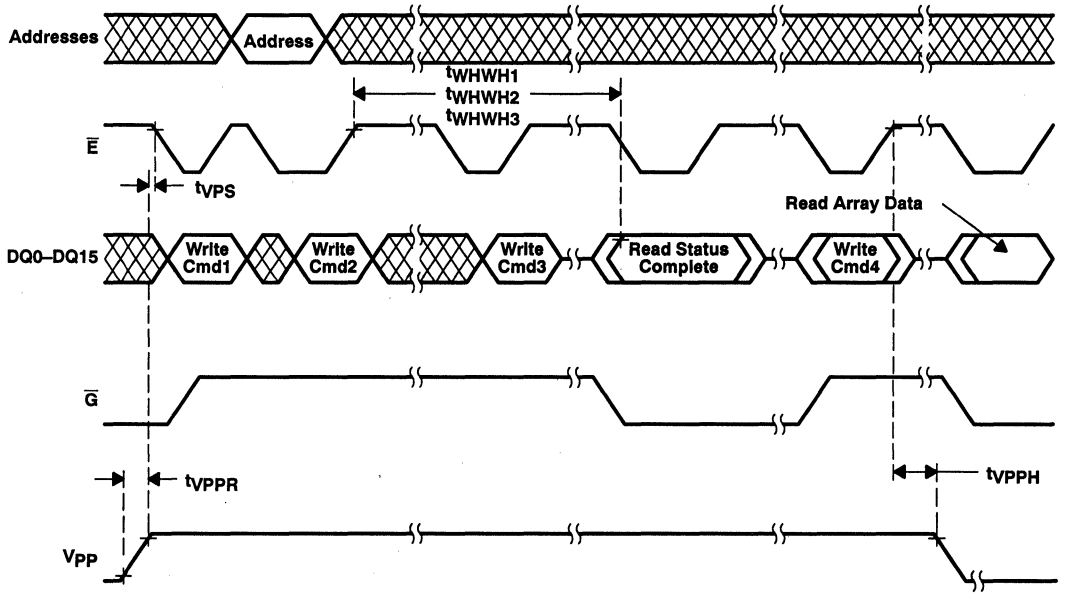


NOTE: Addresses are latched on the falling edge of $\overline{E}$.
Command and Program data are latched on the rising edge $\overline{E}$.

Figure 6. AC Waveform for Write Operations

PRODUCT PREVIEW

PROGRAM/ERASE INFORMATION



Command	Cmd1		Cmd2		Cmd3		Read		Cmd4		Read
Program	10h		data		70h		status		00h		array
Chip Erase	30h		30h		70h		status		00h		array
Block Erase	20h		D0h		70h		status		00h		array

NOTE: Addresses are latched on the falling edge of $\overline{E}$.
Command and Program data are latched on the rising edge $\overline{E}$.

Figure 7. AC Waveform for Program/Erase Operations

PRODUCT PREVIEW

TMS27LV010A 1 048 576-BIT UV ERASABLE LOW VOLTAGE PROGRAMMABLE ROM
TMS27LV010A 1 048 576-BIT LOW VOLTAGE ONE-TIME PROGRAMMABLE ROM

SMLS113–DECEMBER 1992

ADVANCE INFORMATION

- **Organization . . . 128K × 8**
- **Single 3.3-V Power Supply**
- **Operationally Compatible With Existing 1-Megabit EPROMs**
- **Industry Standard 32-Pin Dual-In-line Package (DIP), 32-Lead Plastic Leaded Chip Carrier (PLCC), and 32-Lead Thin Small Outline Package (TSOP)**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

V_{CC} ± 10%		
'27LV010A-20	200	ns
'27LV010A-25	250	ns
'27LV010A-30	300	ns

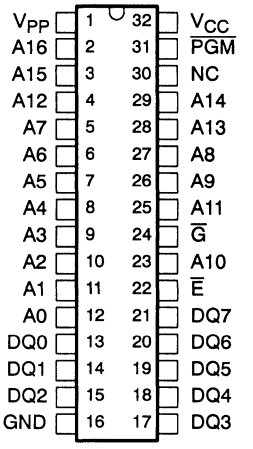
- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Very High-Speed Low Voltage SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 3.6 V)**
  - **Active . . . 54 mW Worst Case**
  - **Standby . . . 0.09 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168 Hour Burn-In and Choices of Operating Temperature Ranges**

description

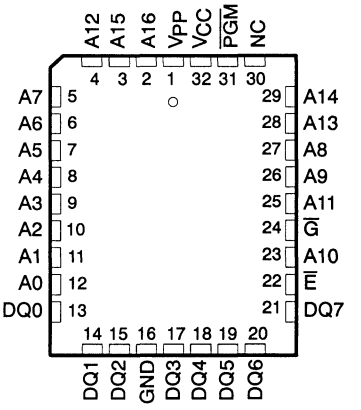
The TMS27LV010A EPROM series are 1 048 576-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27LV010A OTP PROM series are 1 048 576-bit, one-time, electrically programmable read-only memories.

J AND N PACKAGES†
(TOP VIEW)



FM PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A16	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	3.3-V Supply
V_{PP}	12.75-V Power Supply‡

‡ Only in program mode.

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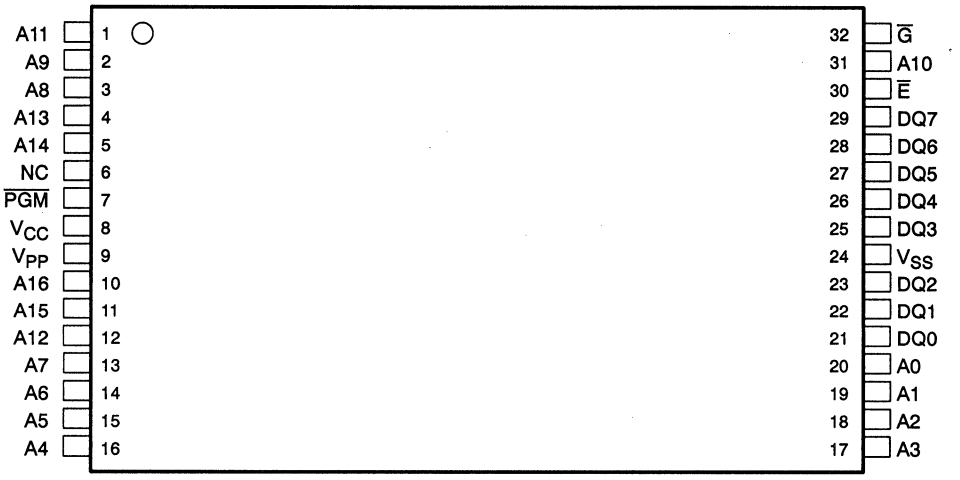
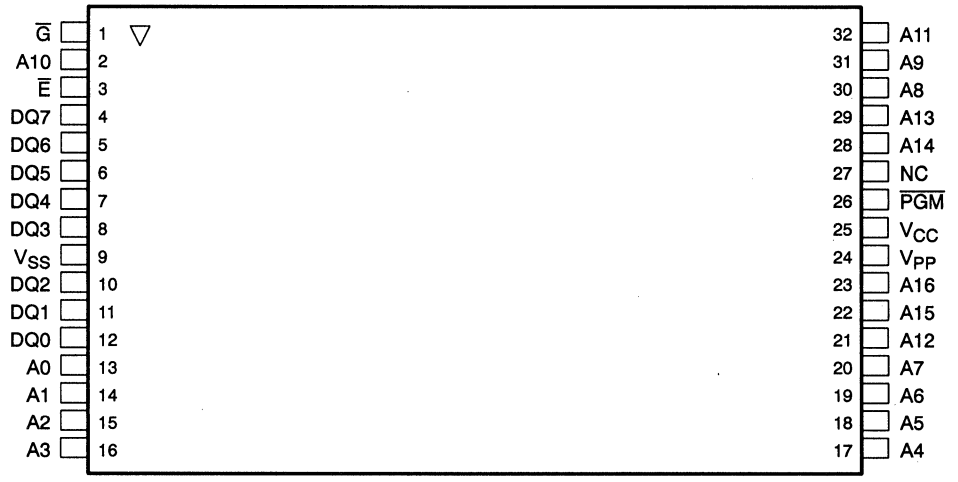
ADVANCE INFORMATION

TMS27LV010A OTP PROM
DD PACKAGE†
(TOP VIEW)



TMS27LV010A OTP PROM
DU PACKAGE†
REVERSE PINOUT
(TOP VIEW)



† The packages shown are for pinout reference only.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The TMS27LV010A EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27LV010A EPROM CDIP is also offered with two choices of temperature ranges, 0°C to 70°C and –40°C to 85°C (JL and JE suffixes). The TMS27LV010A EPROM CDIP is also offered with 168 hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27LV010A OTP PROM is offered in a plastic dual-in-line package (N suffix), a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix), and a 32-lead thin small-outline package (DD and DU suffixes). TMS27LV010A OTP PROM is offered with two choices of temperature ranges of 0°C to 70°C (NL, FML, DDL, and DUL suffixes) and – 40°C to 85°C (NE, FME, DDE, and DUE suffixes). (See table below.)

TMS27LV010A	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168 HOUR BURN-IN VS TEMPERATURE RANGES	
	0°C to 70°C	– 40°C to 85°C	0°C to 70°C	– 40°C to 85°C
EPROM	JL	JE	JL4	JE4
OTP PROM	FML	FME	FML4	FME4
	NL	NE	NL4	NE4
	DDL	DDE	DDL4	DDE4
	DUL	DUE	DUL4	DUE4

These EPROMs and OTP PROMs operate from a single 3.3-V supply (in the read mode), thus are ideal for use in portable systems. One other 12.75-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the Low Voltage SNAP! Pulse programming algorithm. The Low Voltage SNAP! Pulse programming algorithm uses a V_{PP} of 12.75 V and a V_{CC} of 5 V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

ADVANCE INFORMATION

operation

The seven modes of operation are listed in the following table. The read mode requires a single 3.3-V supply. All inputs are TTL level except for V_{PP} during programming (12.75 V for Low Voltage SNAP! Pulse), and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	D7

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

ADVANCE INFORMATION

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read/output disable

When the outputs of two or more TMS27LV010A EPROMs or TMS27LV010A OTP PROMs are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27LV010A EPROM and OTP PROM is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 15 mA to 250 μA by applying a high TTL input on $\overline{E}$ and to 25 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27LV010A EPROM)

Before programming, the TMS27LV010A EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27LV010A EPROM, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

initializing (TMS27LV010A OTP PROM)

The one-time programmable TMS27LV010A OTP PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

Low Voltage SNAP! Pulse programming

The TMS27LV010A EPROM is programmed using the TI Low Voltage SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of thirteen seconds. Actual programming time will vary as a function of the programmer used.

The Low Voltage SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 12.75 V, V_{CC} = 5 V, $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the Low Voltage SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 3.3\ V \pm 10\%$.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 12.75 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

ADVANCE INFORMATION

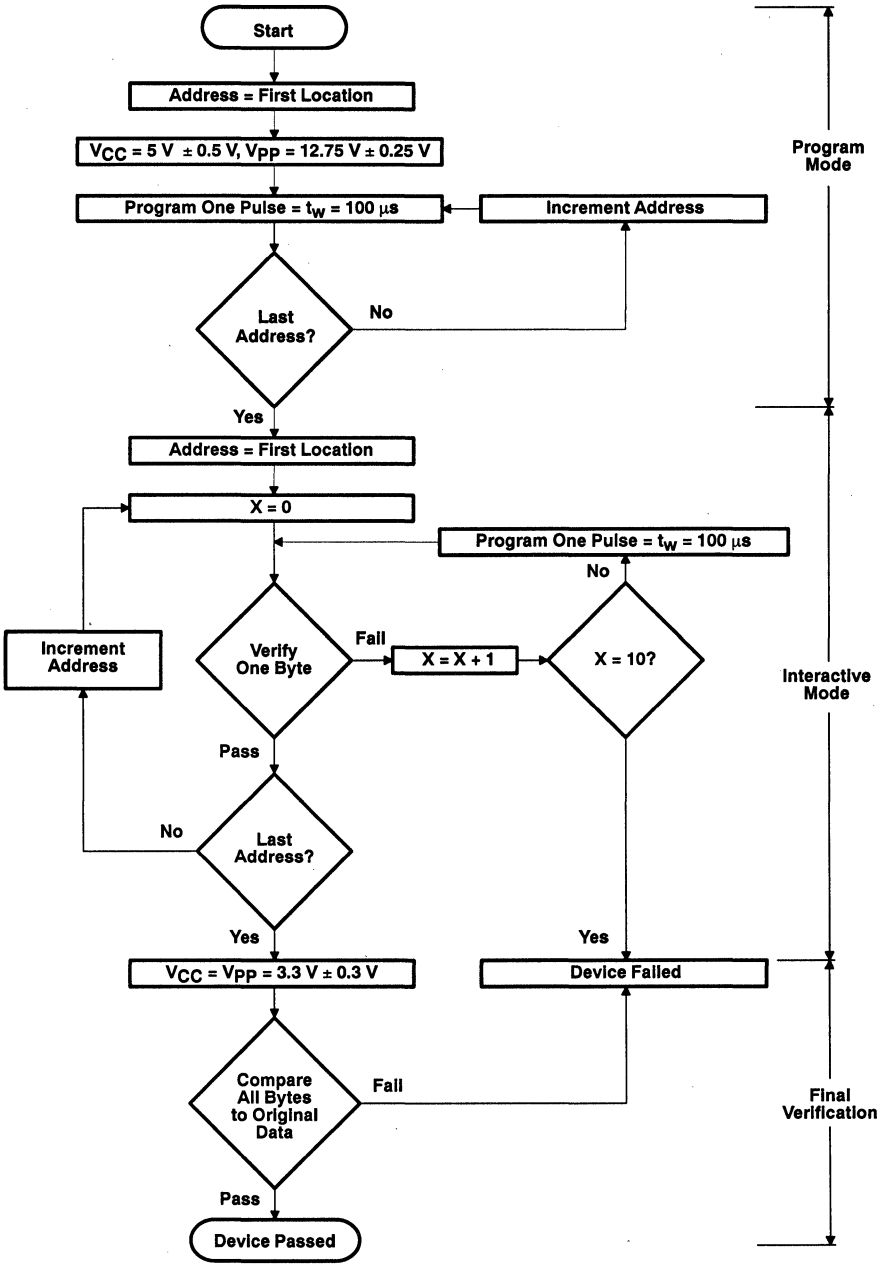


Figure 1. Low Voltage SNAP! Pulse Programming Flowchart

signature mode

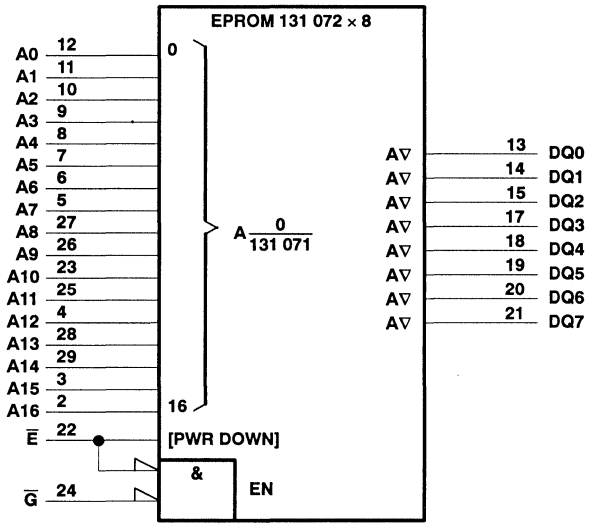
The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for these devices is 97D7. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D7 (Hex), as shown by the signature mode table below.

signature mode†

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	1	D7

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, $V_{PP} = V_{CC}$.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. J package illustrated.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.6 V to 7 V
Supply voltage range, V_{PP} ..... –0.6 to 14 V
Input voltage range, All inputs except A9 ..... –0.6 to VCC + 1 V
A9 ..... –0.6 to 13.5 V
Output voltage range, with respect to VSS (see Note 1) ..... –0.6 V to VCC + 1 V
Operating free-air temperature range (JL, NL, FML, DDL, and DUL) ..... 0°C to 70°C
Operating free-air temperature range (JE, NE, FME, DDE, and DUE) ..... –40°C to 85°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS27LV010A-20 TMS27LV010A-25 TMS27LV010A-30			UNIT
			MIN	TYP	MAX	
V_{CC} Supply voltage	Read mode (see Note 2)		3	3.3	3.6	V
	Low Voltage SNAP! programming algorithm		4.5	5	5.5	V
V_{PP} Supply voltage	Read mode (see Note 3)		V_{CC}–0.6	V_{CC}	V_{CC}+0.6	V
	Low Voltage SNAP! Pulse programming algorithm		12.5	12.75	13	V
V_{IH} High-level dc input voltage		TTL	2.0		V_{CC}+0.5	V
		CMOS	V_{CC}–0.2		V_{CC}+0.5	
V_{IL} Low-level dc input voltage		TTL	–0.5		0.8	V
		CMOS	–0.5		GND+0.2	

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. During programming, V_{PP} must be maintained at 12.75 V ± 0.25 V.

ADVANCE INFORMATION

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −100 µA	V_{CC}−0.2		V
			I_{OH} = −2 mA	2.4		
V_{OL}	Low-level output voltage		I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 µA		0.2	
I_I	Input current (leakage)		V_I = 0 to 3.6 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 3.6 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 12.75 V		30	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{E}$ = V_{IH}, V_{CC} = 3.6 V		250	µA
		CMOS-input level	$\overline{E}$ = V_{CC} ± 0.2 V, V_{CC} = 3.6 V		25	
I_{CC2}	V_{CC} supply current (active) (output open)		$\overline{E}$ = V_{IL}, V_{CC} = 3.6 V, $\overline{G}$ = V_{IH}, F = 5 MHz		15	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		4	8	pF
C_o	Output capacitance	V_O = 0, f = 1 MHz		6	10	pF

† Capacitance measurements are made on sample basis only.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'27LV010A-20		'27LV010A-25		'27LV010A-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input t_r ≤ 20 ns, Input t_f ≤ 20 ns		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first§		0	35	0	35	0	35	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		ns

§ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).
5. Common test conditions apply for t_{dis} except during programming.

ADVANCE INFORMATION

switching characteristics for programming: V_{CC} = 5 V and V_{PP} = 12.75 V (Low Voltage SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 5 V and V_{PP} = 12.75 V (Low Voltage SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	Low Voltage SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

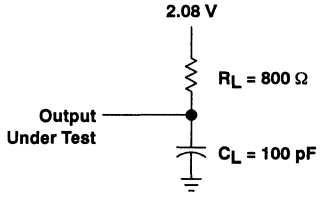
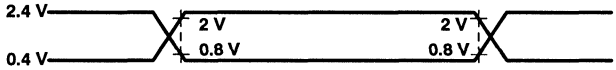


Figure 2. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

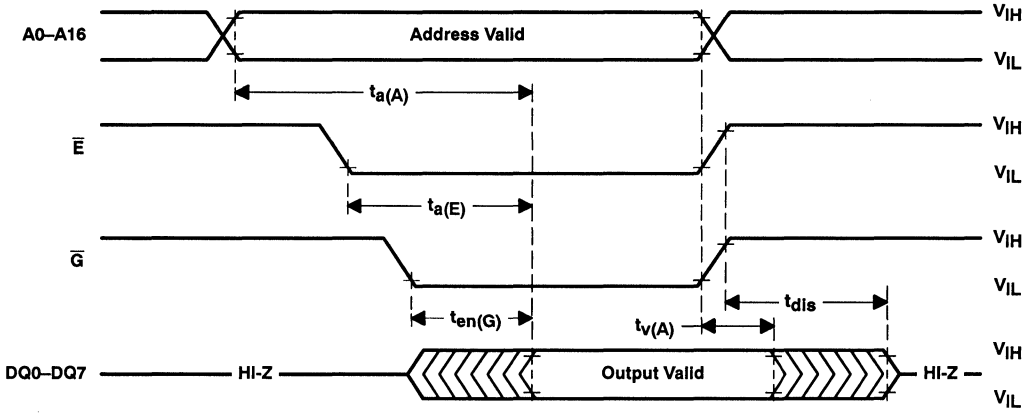
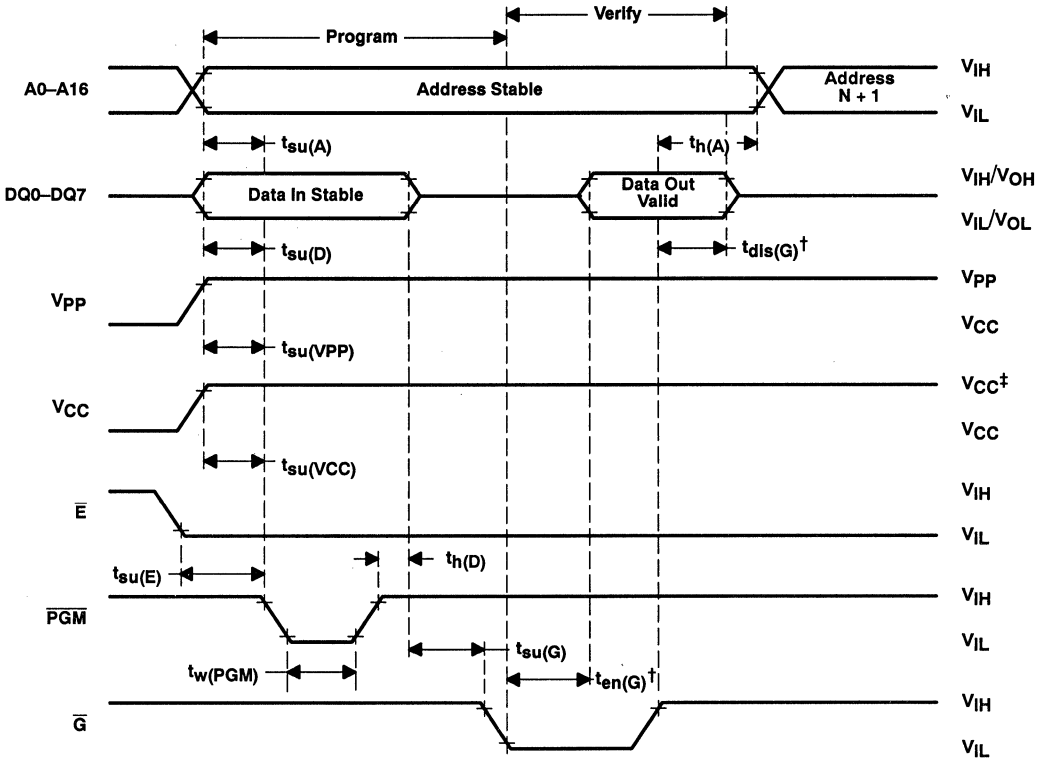


Figure 3. Read Cycle Timing

ADVANCE INFORMATION

PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 12.75-V V_{PP} and 5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (Low Voltage SNAP! Pulse Programming)

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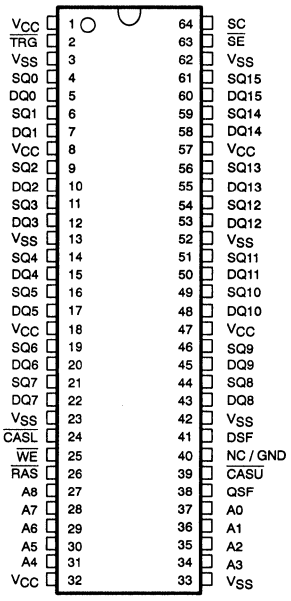
- **DRAM : 262 144 Words × 16 Bits SAM: 256 Words × 16 Bits**
- **Dual Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{CASL}$, $\overline{CASU}$) Provides Flexibility**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **Long Refresh Period . . . Every 8 ms (Max)**
- **DRAM Port is Compatible With the TMS45160**
- **Up to 45-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial Register Starting Locations**
- **$\overline{SE}$ Controlled Register Status QSF**
- **Split Serial Data Register for Simplified Real-Time Register Reload**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe / Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WE}$	DRAM Write Enable Select
DSF	Special Function Select
QSF	Special Function Output
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: Not connected internally to V_{SS})

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(rd\ W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55160-70	70 ns	20 ns	130 ns	45 ns	22 ns	165 mA	205 mA
TMS55160-80	80 ns	25 ns	150 ns	50 ns	30 ns	160 mA	195 mA

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description

The TMS55160 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each, interfaced to a serial data register [serial access memory (SAM)], organized as 256 words of 16 bits each. The TMS55160 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55160 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55160 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block write feature. The block write mode allows sixteen bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column address locations. As many as 64 bits of data can be written to memory during each $\overline{\text{CAS}}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles without reloading. The TMS55160 also offers byte control. Byte control can be applied in read cycles, write cycles, block write cycles, load mask register cycles, and load color register cycles.

The TMS55160 offers a split-register transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This real-time register reload implementation allows truly continuous serial data. For applications not requiring real-time register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 45 MHz. During the split-register transfer reads, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

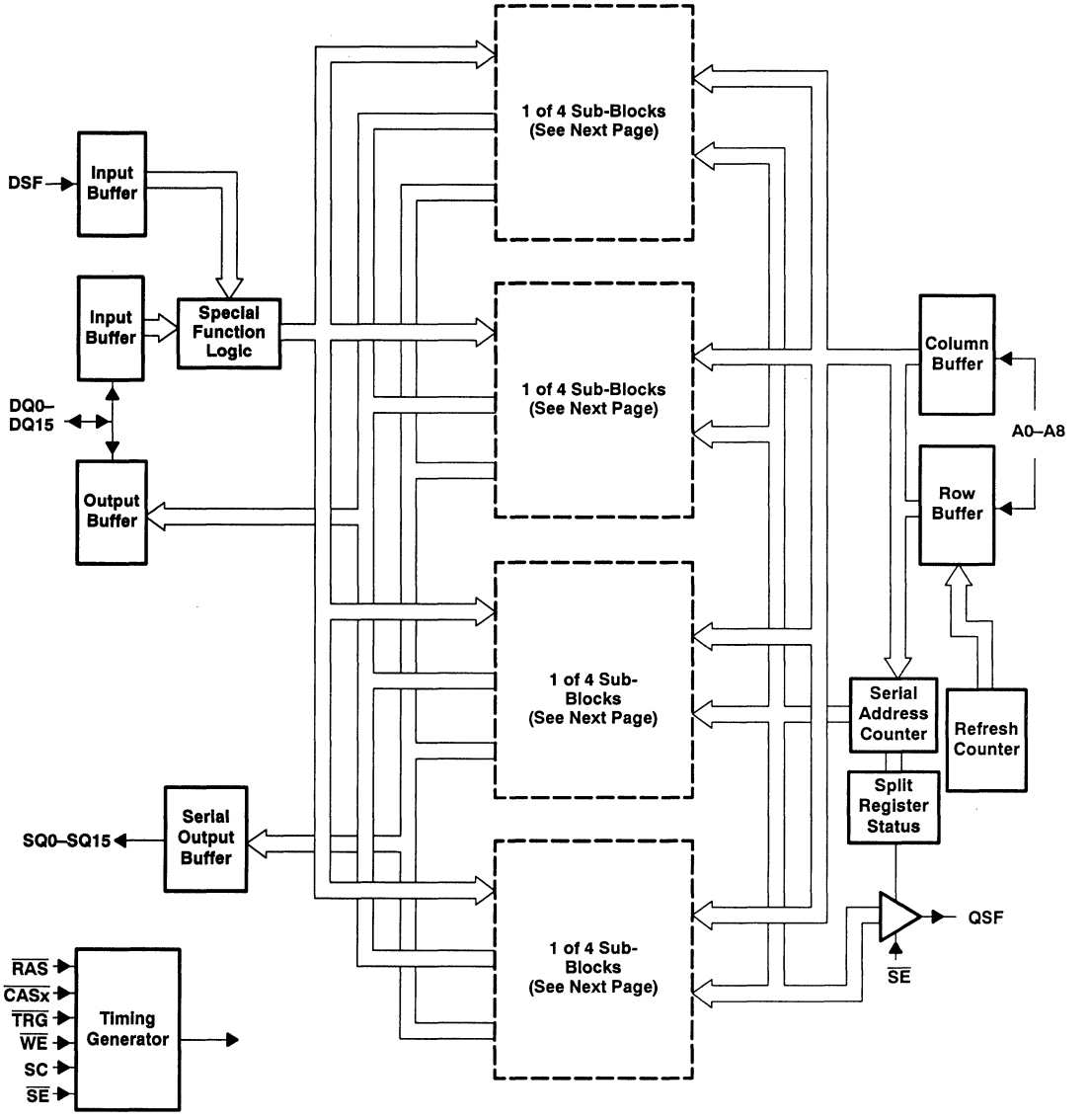
All inputs, outputs, and clock signals on the TMS55160 are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS55160 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS55160 is offered in a 64-pin super-small-outline gull-wing leaded package for direct surface mounting.

The TMS55160 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)

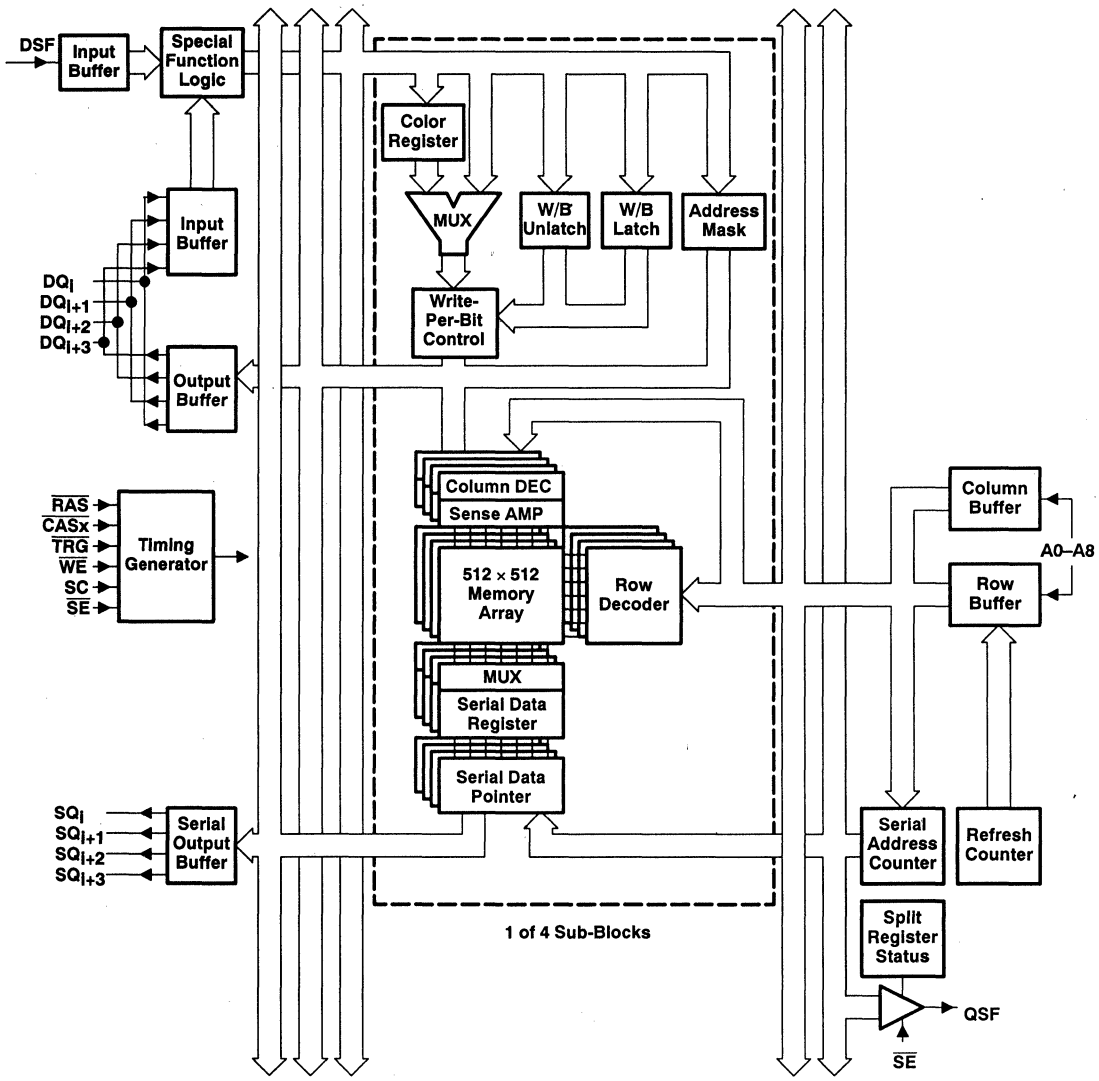


Table 1. Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS‖		DQ0–DQ15†		
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx	RAS	CASL CASU WE	MNE CODE
Reserved (do not use)	0	0	0	0	X	X	X	X	X	—
CAS-before-RAS refresh (option reset)§	0	X	1	0	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)¶	0	X	1	1	X	X	X	X	X	CBRN
Read transfer	1	0	1	0	X	Row Addr	Tap Point	X	X	RT
Split-register read transfer	1	0	1	1	X	Row Addr	Tap Point	X	X	SRT
DRAM write (non-persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (non-persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (non-masked)	1	1	1	0	0	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (non-masked)	1	1	1	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write mask register #	1	1	1	1	0	Refresh Addr	X	X	Write Mask	LMR
Load color register	1	1	1	1	1	Refresh Addr	X	X	Color Data	LCR

† DQ0–DQ15 are latched on either the first CASx falling edge or the falling edge of WE, whichever occurs later.
‡ Logic 0 is selected when either or both CASL and CASU are low.
§ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at RAS.
¶ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode.
# Load Write Mask Register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.
‖ The column address and block address are latched on the first CASx falling edge.
X = Don't care.
Col Mask = 1: Write to address/column enabled.
Write Mask = 1: Write to I/O enabled.

Table 2. Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row-address, tap point	
$\overline{CASx}$	Column address strobe, DQ output enable	Tap address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block write enable Write mask register load enable Color register load enable $\overline{CAS}$-before-$\overline{RAS}$ (option reset)	Split register transfer enable	
$\overline{RAS}$	Row address strobe	Row address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WE}$	Write enable		
QSF			Serial register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V Supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply, and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage cell locations. Nine row address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of $\overline{CASx}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the first falling edge of $\overline{CASx}$.

During the read transfer operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer will occur. At the first falling edge of $\overline{CASx}$, the column address bits A0–A8 are latched. The most significant column address bit (A8) selects which half of the row will be transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During the split register read transfer operation, address bit A7 is ignored at the falling edge of $\overline{CASx}$. An internal counter will select which half of the register will be used. If the high half of the SAM is currently in use, the low half of the SAM will be loaded with the low half of the DRAM half row, and vice versa. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WE}$, $\overline{TRG}$, $\overline{CASL}$, $\overline{CASU}$, and DSF onto the chip to invoke DRAM and read transfer functions of the TMS55160.

column-address strobe ($\overline{CASL}$, $\overline{CASU}$)

$\overline{CASL}$ and $\overline{CASU}$ are control inputs that latch the states of the column address and DSF to control DRAM and read transfer functions of the TMS55160. $\overline{CASx}$ also act as output enable for the DRAM output pins, DQ0–DQ15.

In DRAM operation, $\overline{CASL}$ enables data to be written to or read from the lower byte (DQ0–DQ7), and $\overline{CASU}$ enables data to be written to or read from the upper byte (DQ8–DQ15).

In read transfer operations, address bits A0–A8 will be latched at the first falling edge of $\overline{CASx}$ as the start postion (Tap) for the serial data output (SDQ0–SDQ15).

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or read transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins, DQ0–DQ15.

For read transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WE}$)

In DRAM operation, $\overline{WE}$ enables data to be written to the DRAM.

$\overline{WE}$ is also used to select the DRAM write-per-bit mode of operation. Holding $\overline{WE}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation. The TMS55160 supports both the non-persistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or the first falling edge of $\overline{CASx}$, similar to an address. DSF determines which of the following functions below are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- Block write
- Loading mask register for the persistent write-per-bit mode
- Loading color register for the block write mode
- Split-register read transfer

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CASx}$ is held high. Data will not appear at the outputs until after both $\overline{CASx}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{TRG}$ and $\overline{CASx}$ are low. Either $\overline{CASx}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In a read transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

The write-per-bit mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$.

serial data output (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data-out is the same polarity as data-in. The serial outputs are in the high-impedance (floating) state as long as serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55160 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial access operations $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low will enable the serial data output. $\overline{SE}$ high will disable the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, then the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF may change state upon crossing a boundary between the two SAM halves.

During the read transfer operation (non-split register), QSF may change state upon completing the cycle. This state is determined by the tap point being loaded during the transfer cycle. During the split-register read transfer operation, QSF may change state upon crossing a boundary between the two SAM halves.

QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, then QSF output will be in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS‖		DQ0–DQ15†		
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx	RAS	CASL CASU WE	MNE CODE
Reserved (Do not use)	0	0	0	0	X	X	X	X	X	—
CAS-before-RAS refresh (option reset)§	0	X	1	0	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)¶	0	X	1	1	X	X	X	X	X	CBRN
DRAM write (non-persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	DQ Mask	Valid Data	RWM
DRAM block write (non-persistent write-per-bit)	1	1	0	0	1	Row Addr	Blk Addr A2–A8	DQ Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	1	1	0	0	1	Row Addr	Blk Addr A2–A8	X	Col Mask	BWM
DRAM write (non-masked)	1	1	1	0	0	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (non-masked)	1	1	1	0	1	Row Addr	Blk Addr A2–A8	X	Col Mask	BW
Load write mask register#	1	1	1	1	0	Refresh Address	X	X	Write Mask	LMR
Load color register	1	1	1	1	1	Refresh Address	X	X	Color Data	LCR

† DQ0–DQ15 are latched on either the first CASx falling edge or the falling edge of WE, whichever occurs later.
‡ Logic 0 is selected when either or both CASL and CASU are low.
§ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at RAS.
¶ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode.
# Load Write Mask Register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.
‖ The column address and block address are latched on the first CASx falling edge.
X = Don't care.
Col Mask = 1: Write to address/column enabled.
Write Mask = 1: Write to I/O enabled.

refresh

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshes are accomplished by bringing either or both $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ low earlier than $\overline{\text{RAS}}$. The external row address is ignored and the refresh row address is generated internally. Two types of CBR refresh cycles are available. The CBR refresh (option reset) will end the persistent write-per-bit mode. The CBRN refresh (No Reset) will not end the persistent write-per-bit mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively, as long as the entire refresh is completed within the required time period $t_{rf(MA)}$. The output buffers remain in the high impedance state during the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, regardless of the state of $\overline{\text{TRG}}$.

hidden refresh

A hidden refresh is accomplished by holding both $\overline{\text{CASL}}$ and $\overline{\text{CASU}}$ low in the DRAM read cycle and cycling $\overline{\text{RAS}}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, the refreshed row addresses are generated internally during the hidden refresh. Hidden refresh will also end the persistent write-per-bit mode, regardless of the state of DSF at $\overline{\text{RAS}}$.

$\overline{\text{RAS}}$-only refresh

A $\overline{\text{RAS}}$-only refresh is accomplished by cycling $\overline{\text{RAS}}$ at every row address. Unless $\overline{\text{CASx}}$ and $\overline{\text{TRG}}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{\text{RAS}}$-only refresh. Strobing each of the 512 row addresses with $\overline{\text{RAS}}$ causes all bits in each row to be refreshed.

enhanced page mode

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row address setup, row address hold, and address multiplex. The maximum $\overline{\text{RAS}}$ low time and $\overline{\text{CAS}}$ page cycle time used determines the number of columns that may be accessed.

Unlike conventional page mode operations, the enhanced page mode allows the TMS55160 to operate at a higher data bandwidth. Data retrieval begins as soon as column address is valid rather than when $\overline{\text{CASx}}$ transitions low. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{\text{CASx}}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{\text{CASx}}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied.

byte control

Byte control can be applied in DRAM read cycles, write cycles, block write cycles, load mask register cycles, and load color register cycles. In byte operation, the column address (A0–A8) will be latched at the first falling edge of $\overline{CAS}$x. In read cycles, $\overline{CASL}$ enables the lower byte (DQ0–DQ7), and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) (Figure 1).

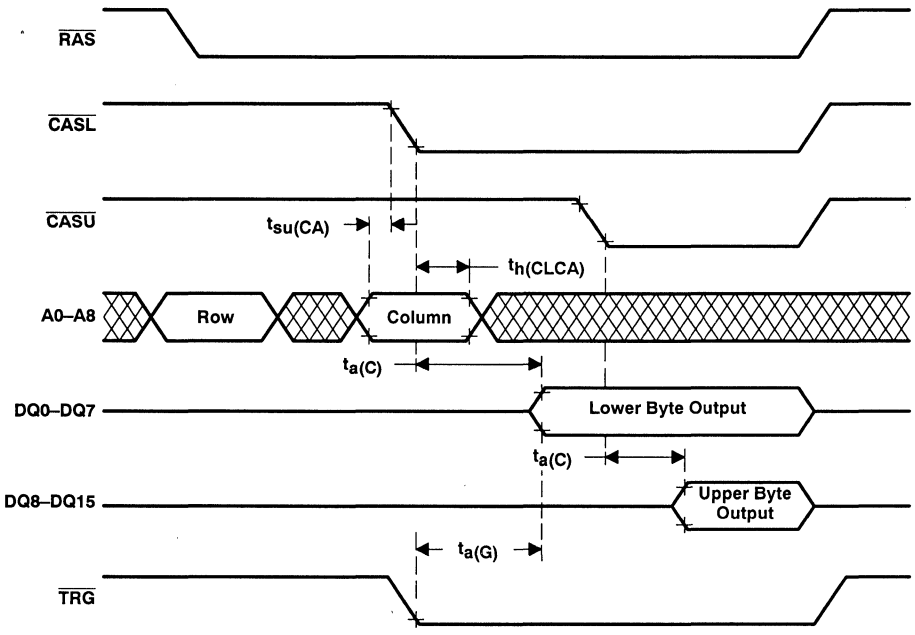


Figure 1. Example of a Byte Read

In byte write operation, $\overline{CASL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables data to be written to the upper byte (DQ8–DQ15). In an early write cycle $\overline{WE}$ is brought low prior to both $\overline{CASx}$ signals, and data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of $\overline{CASx}$ (Figure 2).

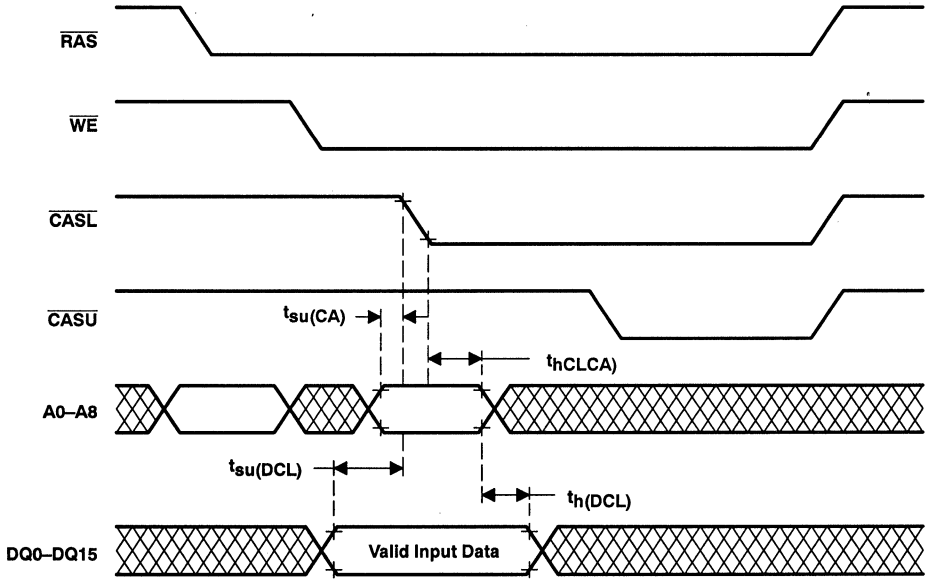


Figure 2. Example of an Early Write

For late-write or read-modify-write cycles, $\overline{WE}$ is brought low after either or both $\overline{CASL}$ and $\overline{CASU}$ fall. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{WE}$ (Figures 3 and 4).

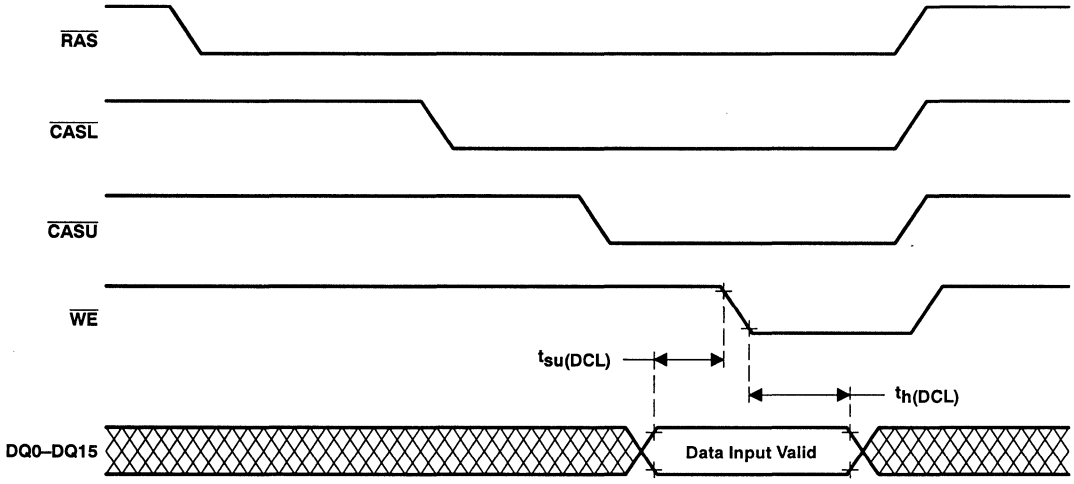


Figure 3. Example of a Late Write

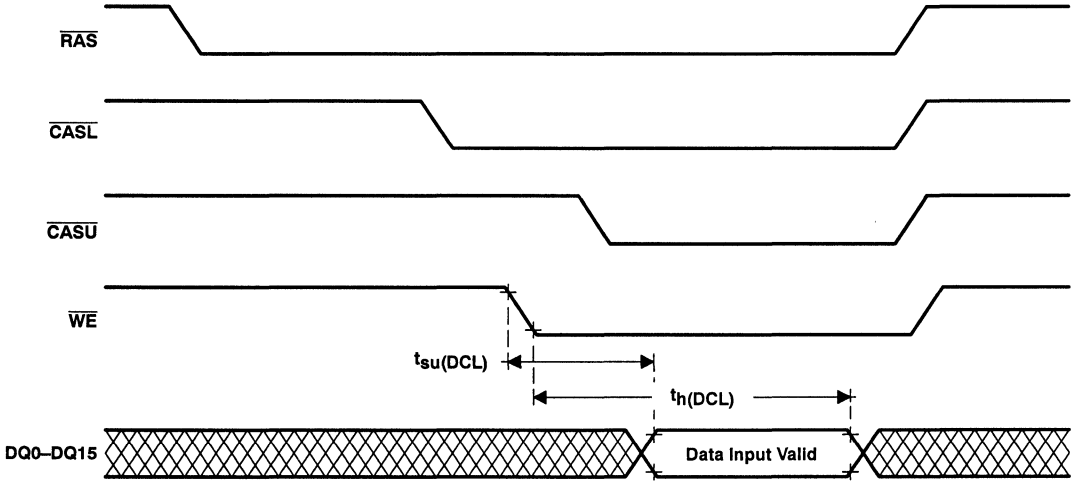


Figure 4. Example of a Late Write

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$.

If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the write operation will be performed without any masking. The TMS55160 offers two write-per-bit modes: the non-persistent write-per-bit and the persistent write-per-bit.

non-persistent write-per-bit

When $\overline{WE}$ is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the sixteen random I/Os are written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later. $\overline{CASL}$ enables the lower byte (DQ0–DQ7) to be written, and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) to be written, per the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O (Figure 5).

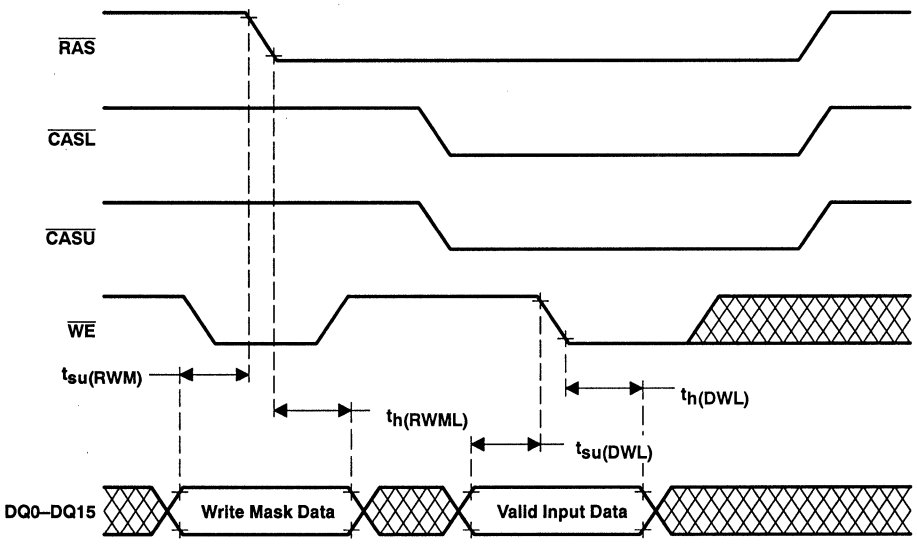
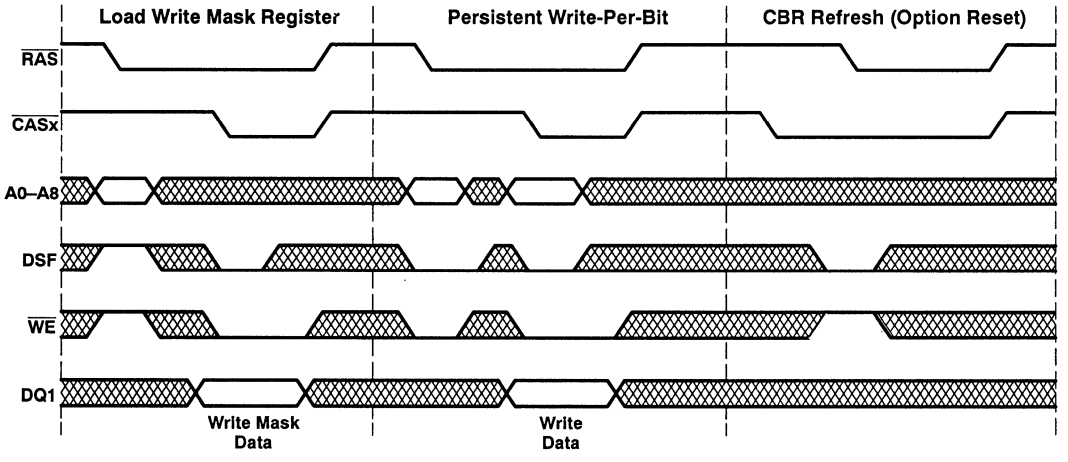


Figure 5. Example of Non-Persistent Write-Per-Bit (Late Write)

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load mask register cycle first. In the persistent write-per-bit mode, the write-per-bit mask will not be overwritten but will remain valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load write mask register cycle is performed using DRAM write cycle timing, except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the first falling edge of $\overline{CASx}$. A binary code is input to the write mask register via the random I/O pins and latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later. Byte write control can be applied to the write mask during the load mask register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the non-persistent write-per-bit mode, except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it will remain in this mode and will be reset only by a $\overline{CAS}$-before-$\overline{RAS}$ refresh with option reset cycle (Figure 6). A hidden refresh cycle will also end the persistent write-per-bit mode, regardless of the state of DSF.



Mask Data = 1 : Write to I/O Enabled
= 0 : Write to I/O Disabled

Figure 6. Example of a Persistent Write-Per-Bit

block write

The block write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants may have up to 4 consecutive columns written at a time with up to 4 DQs per column (see Figure 7).

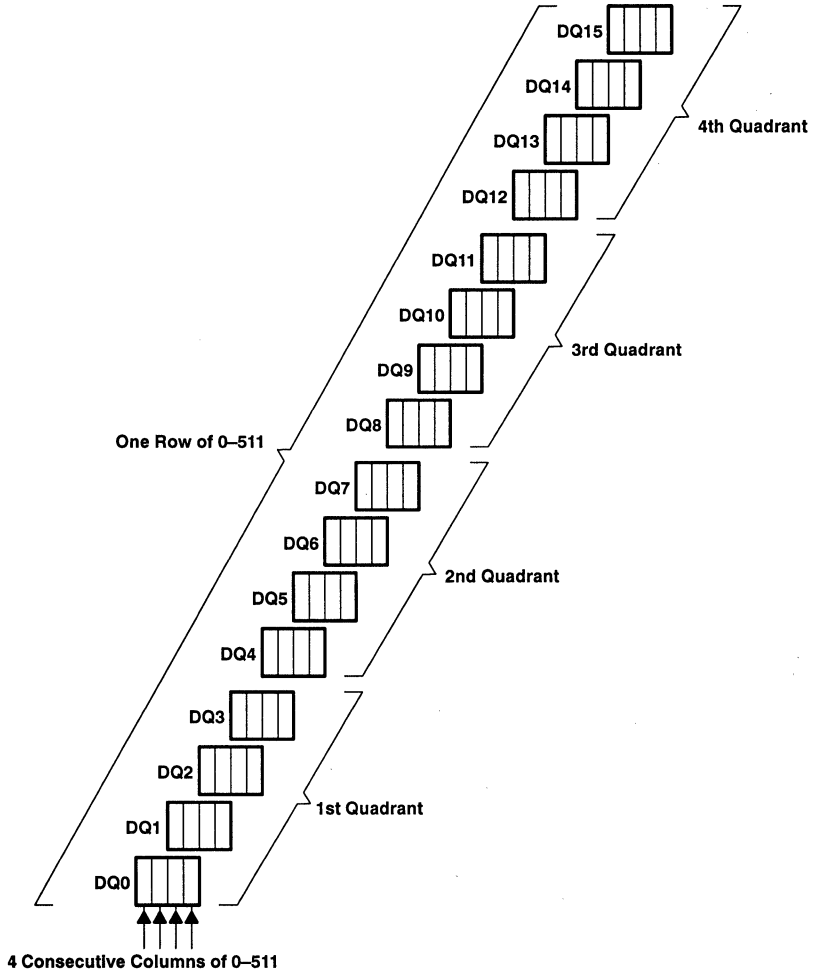


Figure 7. Block Write

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Non-persistent write-per-bit or persistent write-per-bit functions can be applied to the block write operation to provide write masking options. The DQ data is provided by 4 bits from the on-chip color register. Bits 0–3 from the 16-bit write mask, bits 0–3 from the 16-bit column mask and bits 0–3 from the 16-bit color data register configure the block write for the first quadrant, while bits 4–7, 8–11, 12–15, control the other quadrants in a similar fashion.

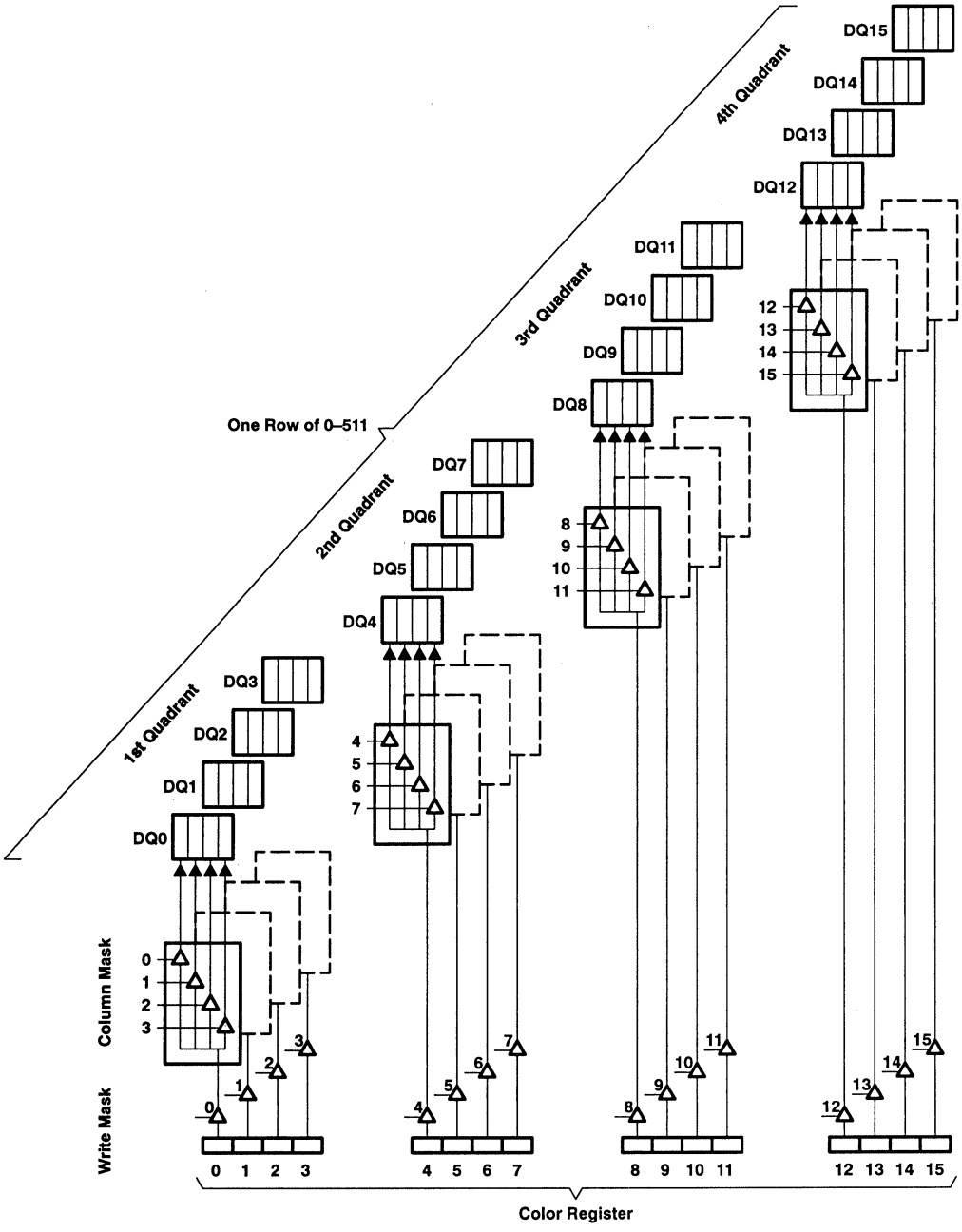


Figure 8. Block Write With Masks

Every 4 columns makes a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as below (Figure 9).

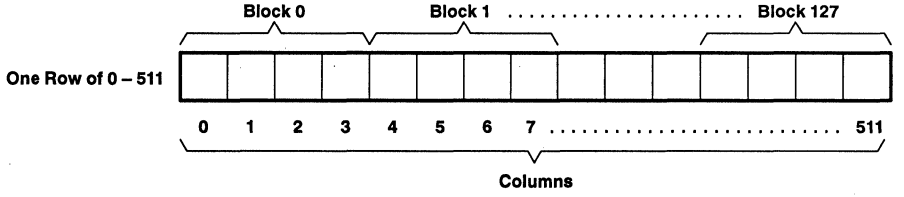


Figure 9. Block Columns Organization

During block write cycles, only the seven most significant column addresses (A2–A8) are latched on the first falling edge of $\overline{CASx}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. (Each one-megabit quadrant has the same block selected.)

A block write cycle is entered in a manner similar to a DRAM write cycle except with DSF held high on the first falling edge of $\overline{CASx}$. As in a DRAM write operation, $\overline{CASL}$ and $\overline{CASU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column mask data is input via the DQs and is latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later. The 16-bit color data register must be loaded prior to performing a block write, as described below. Refer to the write-per-bit section for details on use of the write mask capability, allowing additional performance options.

Example of block write:

block write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color data register =	1011	1011	1100	0111
write mask =	1110	1111	1111	1011
column mask =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color data register (101) to all four columns of Block 0. DQ3 is not written and retains its previous data due to the write mask register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color data register (1100) to columns 1–3 of its Block 0. Column 0 is not written and retains its previous data on all four DQs due to the column mask register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color data register to column 0 and column 2 of its Block 0. DQ13 retains its previous data on all columns, due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the following data pattern after the block write operation shown in the previous example.

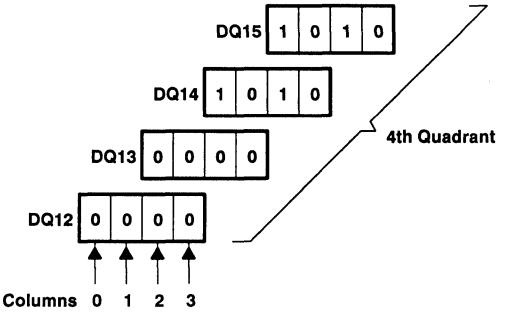
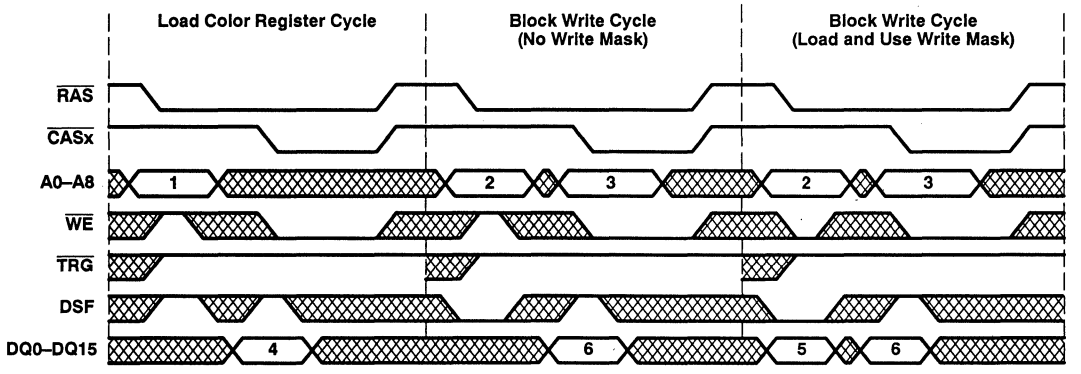


Figure 10. Example of Fourth Quadrant after Block Write

load color register

The load color register cycle is performed using normal DRAM write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$, $\overline{CASL}$, and $\overline{CASU}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later. If only one $\overline{CASx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load color register cycle is performed (Figure 10, Figure 11).

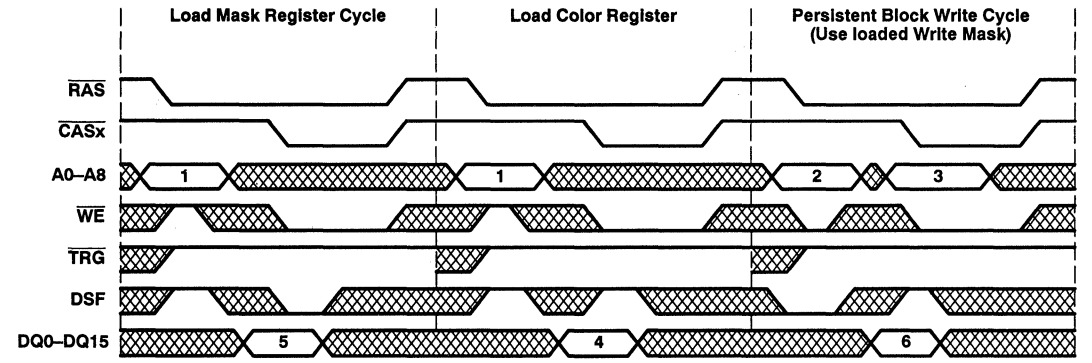


Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first $\overline{CASx}$ falling edge.
4. Color register data
5. Write mask data: DQ0–DQ15 are latched on $\overline{RAS}$ falling edge.
6. Column mask data: DQ_i–DQ_{i+3} (i=0,4,8,12) are latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later.

= Don't Care

Figure 11. Example of Block Writes With Write Masks



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first $\overline{CASx}$ falling edge.
4. Color register data
5. Write mask data: DQ0–DQ15 are latched on $\overline{CASx}$ falling edge.
6. Column Mask Data: DQ_i–DQ_{i+3} (i=0,4,8,12) are latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later.

= Don't Care

Figure 12. Example of a Persistent Block Write

DRAM to SAM transfer operation

During the DRAM to SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WE}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the read transfer operation or the split register read transfer operation will be performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	$\overline{CASx}$‡	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$	$\overline{RAS}$	$\overline{CASx}$ $\overline{WE}$	
Read transfer	1	0	1	0	X	Row Addr	Tap Point	X	X	RT
Split register read transfer	1	0	1	1	X	Row Addr	Tap Point	X	X	SRT

† DQ0–DQ15 are latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later.
‡ Logic 0 is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
X: = Don't care.

read transfer

A read transfer operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column address bits (A0–A8) are latched at the first falling edge of $\overline{CASx}$, where address bit A8 selects which half of the row will be transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data will be read out (Figure 13).

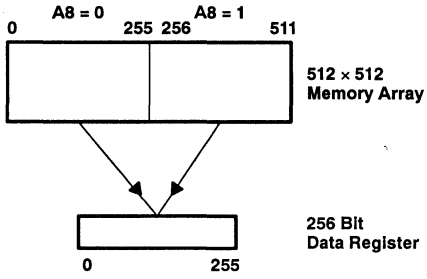


Figure 13. Read Transfer

A read transfer can be performed in three ways: early-load read transfer, real-time or mid-line-load read transfer, and late-load read transfer. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the read transfer cycle (Figure 14).

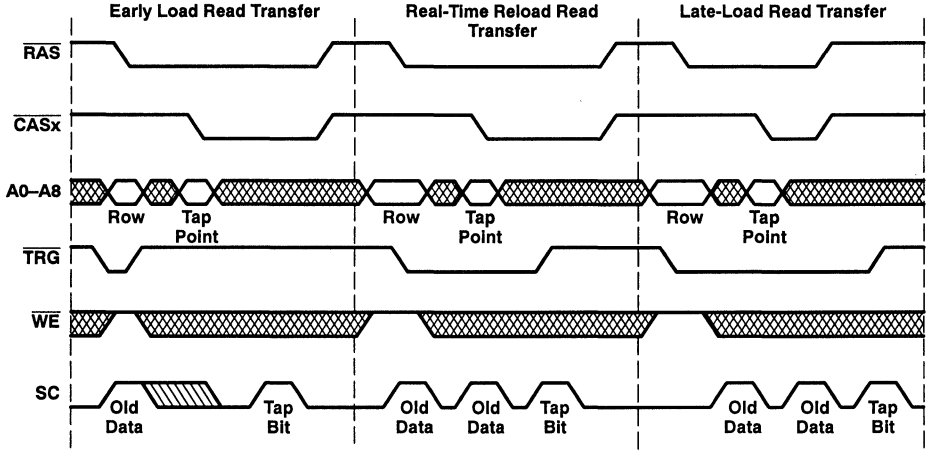


Figure 14. Examples of Read Transfer

split-register read transfer

In the split-register read transfer operation, the serial data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

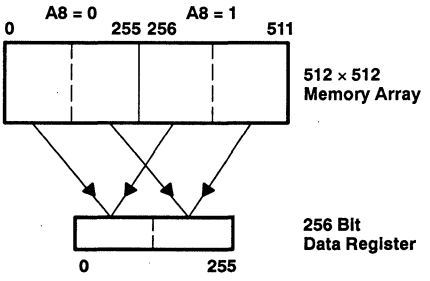
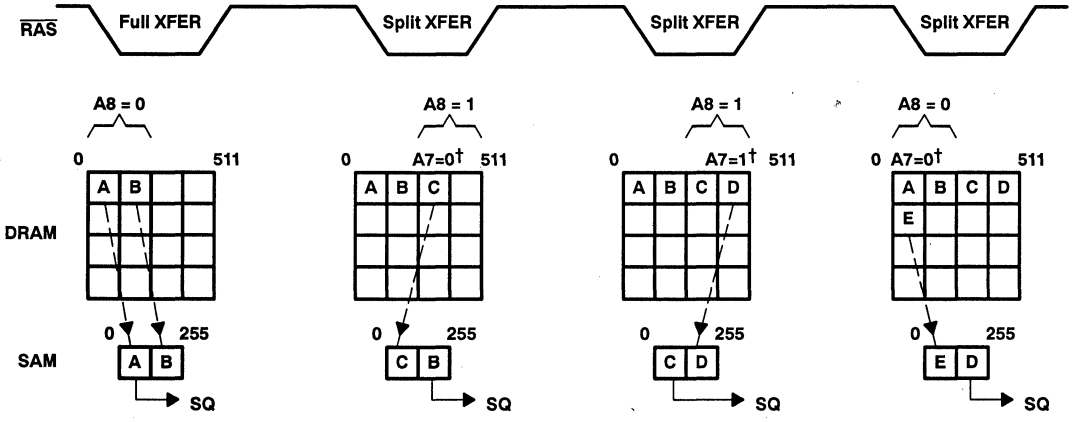


Figure 15. Split Register Read Transfer

To invoke a split-register read transfer cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column address bits (A0–A6 and A8) are latched at the first falling edge of $\overline{CAS}$x. Column address bit A8 selects which half of the row is to be transferred. Column address bits A0–A6 will select one of the 127 tap points in the specified half of the SAM. Column address bit A7 is ignored and the split register transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled

Figure 16. Example of Split-Register Read Transfer Operation

A read transfer (non-split register) must precede the first split register read transfer to ensure proper operation. After the read transfer cycle, the first split-register read transfer can follow immediately without any minimum SC clock requirement. However, there is a minimum requirement of a rising edge of SC between successive split-register read transfer cycles.

QSF indicates which half of the register is being accessed during serial access operation. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of SAM. QSF changes state upon completing a read transfer cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

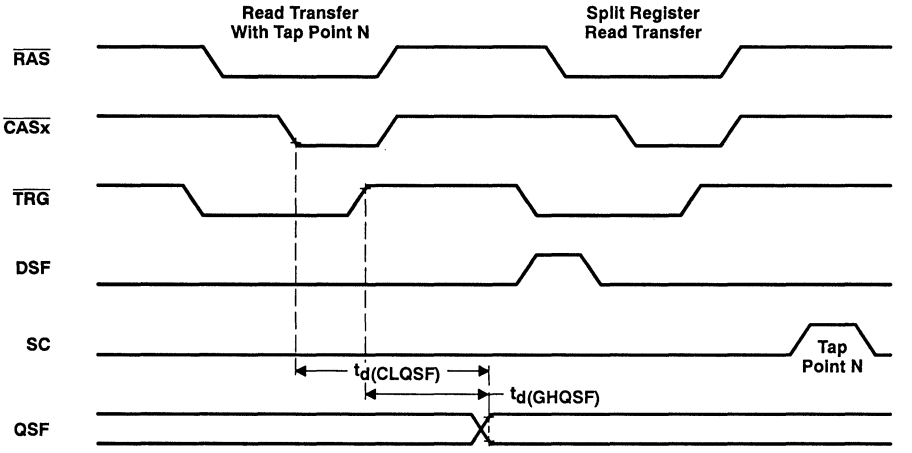


Figure 17. Example of a Split-Register Read Transfer After a Read Transfer

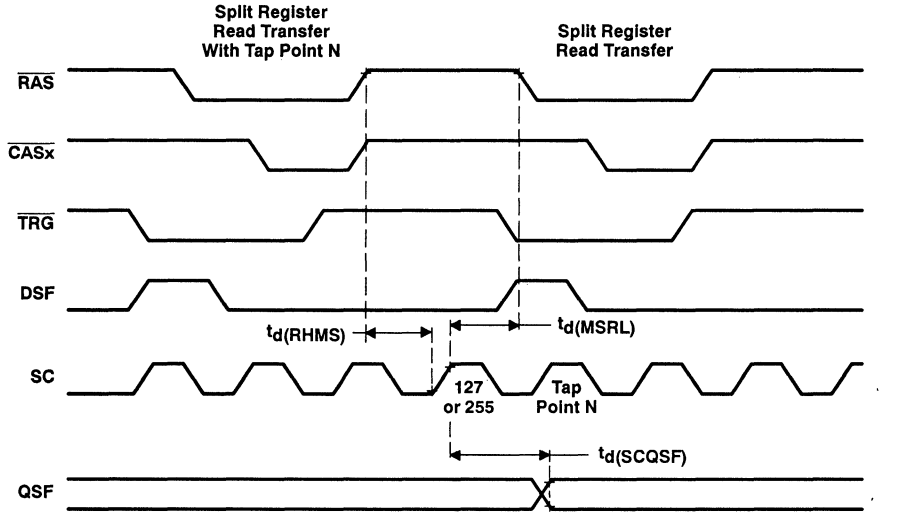


Figure 18. Example of Successive Split-Register Read Transfers

serial access operation

The serial read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during read transfer operations.

Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, then proceeding sequentially to the most significant bit (bit 255) and then wrapping around to the least significant bit (bit 0) (Figure 19).

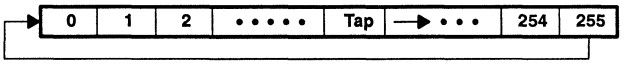


Figure 19. Serial Pointer Direction for Serial Read

For split-register operation, serial data can be read out from the active half of SAM by clocking SC starting at the tap point loaded by the preceding split-register transfer cycle. The serial pointer will then proceed sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register read transfer to the inactive half during this period, the serial pointer will point next to the tap point location loaded by that split register transfer (Figure 20).

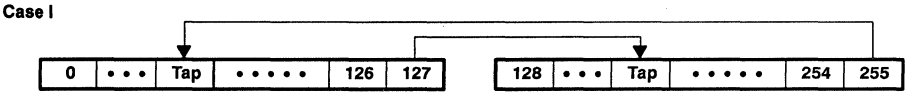


Figure 20. Serial Pointer for Split Register Read – Case I

If there is no split-register read transfer to the inactive half during this period, the serial pointer will point next to bit 128 or bit 0 respectively (Figure 21).

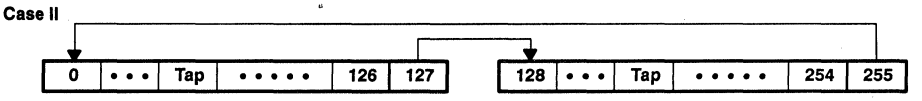


Figure 21. Serial Pointer for Split Register Read – Case II

power up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles to initialize the DRAM port. A read transfer cycle and two SC cycles are needed to initialize the SAM port.

After initialization the internal state of the TMS55160 is as follows:

	State After Initialization
QSF	Defined by the transfer cycle during initialization
Write mode	Non-persistent mode
Write mask register	Undefined
Color register	Undefined
Serial register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature†

Supply voltage range on any pin except DQ and SQ (see Note 1) ..... −1 V to 7 V
Voltage range on DQ and SQ (see Note 1) ..... −1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SAM PORT	TMS55160-70		TMS55160-80		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −1 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5.5 V, All other pins at 0 to V_{CC}			±10		±10	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V			±10		±10	µA
I_{CC1}	Operating current	See Note 4	Standby		165		160	mA
I_{CC1A}	Operating current	$t_{c(SC)}$ = MIN	Active		205		195	
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5	
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		50		45	
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		165		160	
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN	Active		195		185	
I_{CC4}	Page-mode current	$t_{c(P)}$ = MIN (see Note 5)	Standby		100		95	
I_{CC4A}	Page-mode current	$t_{c(SC)}$ = MIN	Active		130		125	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current	See Note 4	Standby		165		160	
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(SC)}$ = MIN	Active		205		195	
I_{CC6}	Data transfer current	See Note 4	Standby		165		160	
I_{CC6A}	Data transfer current	$t_{c(SC)}$ = MIN	Active		205		195	

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}. $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS55160-70		TMS55160-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CASx}$ (see Note 7)	$t_{d(RLCL)}$ = Max	t_{CAC}		20		20	ns
$t_{a(CA)}$	Access time from column address (see Note 7)	$t_{d(RLCL)}$ = Max	t_{AA}		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CASx}$ high (see Note 7)	$t_{d(RLCL)}$ = Max	t_{CPA}		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ (see Note 7)	$t_{d(RLCL)}$ = Max	t_{RAC}		70		80	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low (see Note 7)		t_{OEA}		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high (see Note 7)	C_L = 30 pF	t_{SCA}		20		25	ns
$t_{a(SE)}$	Access time of SQ or QSF from $\overline{SE}$ low (see Note 7)	C_L = 30 pF	t_{SEA}		15		20	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CASx}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output or QSF disable time from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	15	0	20	ns

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	TMS55160-70		TMS55160-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	130		150		ns
$t_{c(W)}$	Write cycle time	t_{WC}	130		150		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RMW}	170		195		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	45		50		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRMW}	85		90		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	130		150		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 9)	t_{SCC}	22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CASx}$ high	t_{CPN}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CASx}$ low (see Note 10)	t_{CAS}	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low	t_{WP}	10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CASx}$ low	t_{ASC}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CASx}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WE}$ before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SE)}$	Setup time, $\overline{SE}$ high before $\overline{RAS}$ low	t_{SER}	0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Setup time, data before $\overline{CASx}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Setup time, data before $\overline{WE}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Setup time, read command $\overline{WE}$ high before $\overline{CASx}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WE}$ low before $\overline{CASx}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write setup time, $\overline{WE}$ low before $\overline{CASx}$ high	t_{CWL}	15		20		ns
$t_{su(WRH)}$	Write setup time, $\overline{WE}$ low before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{WE}$ = low	t_{RWL}	15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CASx}$ low	t_{CAH}	10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CASx}$ low	t_{CFH}	10		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CASx}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS55160-70		TMS55160-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(TRG)}$	Hold time, TRG after $\overline{RAS}$ low	t_{THH}	10		15		ns
$t_{h(RWM)}$	Hold time, write mask, transfer enable after $\overline{RAS}$ low	t_{RWH}	10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write mask operation)	t_{MH}	10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low	t_{RFH}	10		10		ns
$t_{h(RLCA)}$	Hold time, column-address after $\overline{RAS}$ low (see Note 12)	t_{AR}	30		35		ns
$t_{h(CLD)}$	Hold time, data after $\overline{CASx}$ low	t_{DH}	15		15		ns
$t_{h(RLD)}$	hold time, data after $\overline{RAS}$ low (see Note 12)	t_{DHR}	35		35		ns
$t_{h(WLD)}$	Hold time, data after $\overline{WE}$ low	t_{DH}	15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WE}$ low after $\overline{CASx}$ high (see Note 13)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{CASx}$ low	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{RAS}$ low (see Note 12)	t_{WCR}	35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WE}$ low (see Note 14)	t_{OEH}	10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high	t_{SOH}	5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low	t_{FHR}	30		35		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high	t_{CSH}	70		80		ns
$t_{d(CHRL)}$	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high	t_{RSH}	20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CASx}$ low to $\overline{WE}$ low (see Notes 15 and 16)	t_{CWD}	45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note 17)	t_{RCD}	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	35		40		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CASx}$ high	t_{CAL}	35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (see Note 15)	t_{RWD}	95		105		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{WE}$ low (see Note 15)	t_{AWD}	60		65		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high (see Note 18)	t_{CHR}	10		15		ns
$t_{d(CLRL)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (see Note 18)	t_{CSR}	0		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low (see Note 18)	t_{RPC}	0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high for DRAM read cycles		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{OED}	15		15		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (real-time reload read transfer cycle only)	t_{RTH}	55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address	t_{RAD}	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. Read-modify-write operation only.
16. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
17. The maximum value is specified only to assure $\overline{RAS}$ access time.
18. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
19. Early-load read transfer cycle only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	TMS55160-70		TMS55160-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(CLSH)}$	Delay time, $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 20 and 21)	t_{TSL}	5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Notes 20 and 23)	t_{TRD}	−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 20)	t_{TSD}	10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	5		5		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early load read transfer cycles	t_{ASD}	25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	10		10		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CASx}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split read transfer cycles		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split read transfer cycles (see Note 24)	t_{SQD}		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CASx}$ low to QSF switching in transfer read or write cycles (see Note 24)	t_{CQD}		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read or write cycles (see Note 24)	t_{TQD}		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read or write cycles (see Note 24)	t_{RQD}		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 20. Real-time reload read transfer cycle only.
21. Early-load read transfer cycle only.
22. Memory to register (read) transfer cycles only.
23. Late-load read transfer cycle only.
24. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8V.

PARAMETER MEASUREMENT INFORMATION

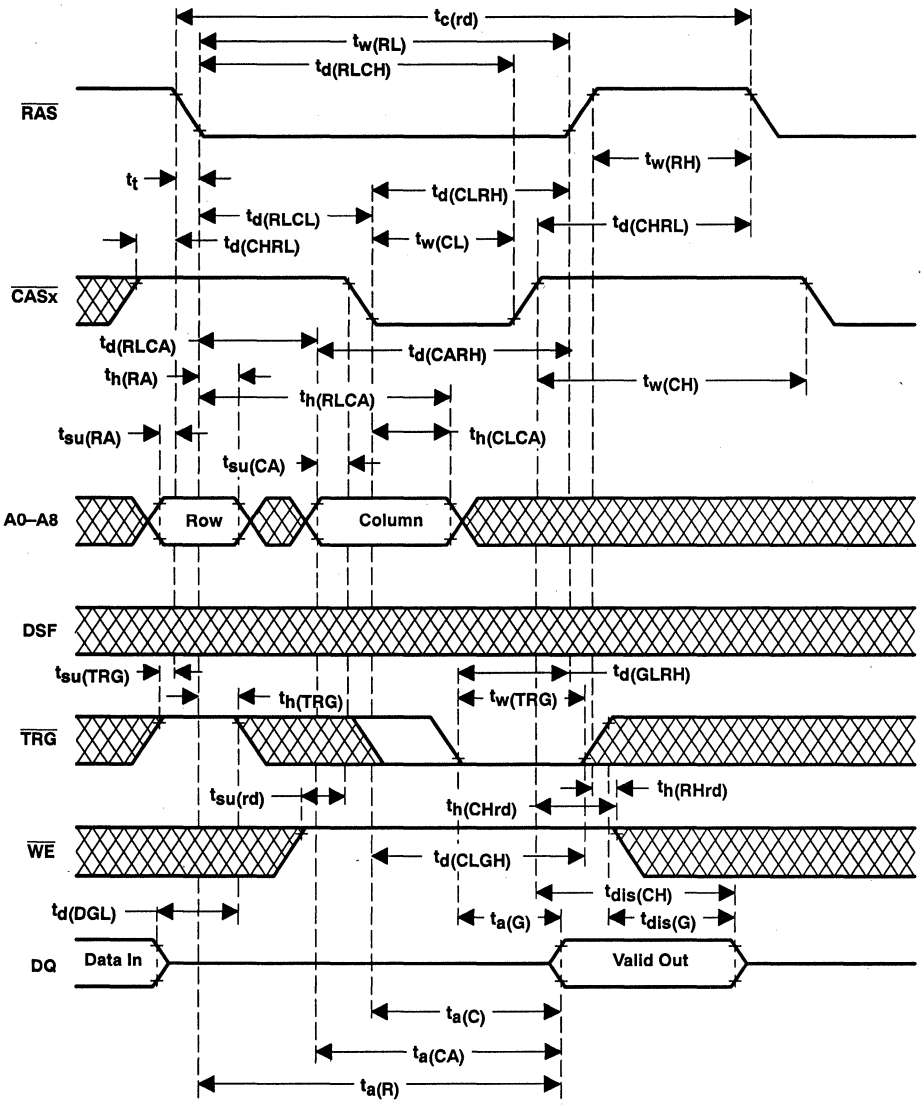


Figure 22. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

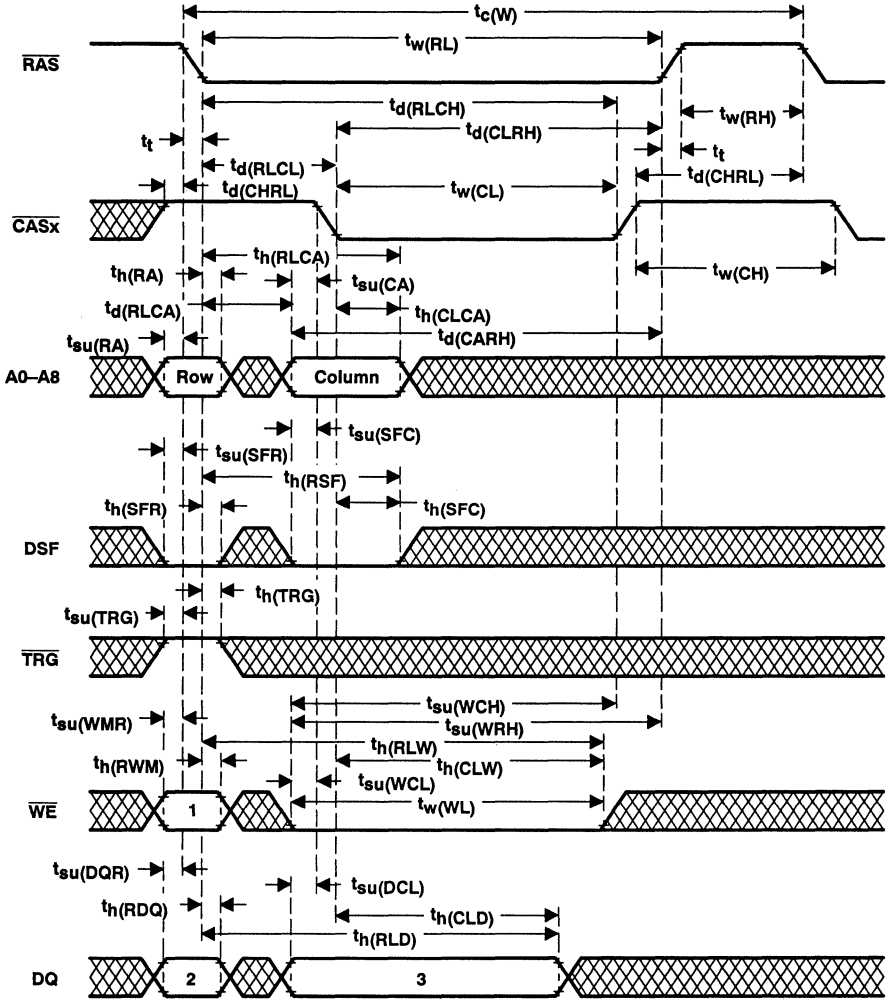


Figure 23. Early Write Cycle Timing

Table 5. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

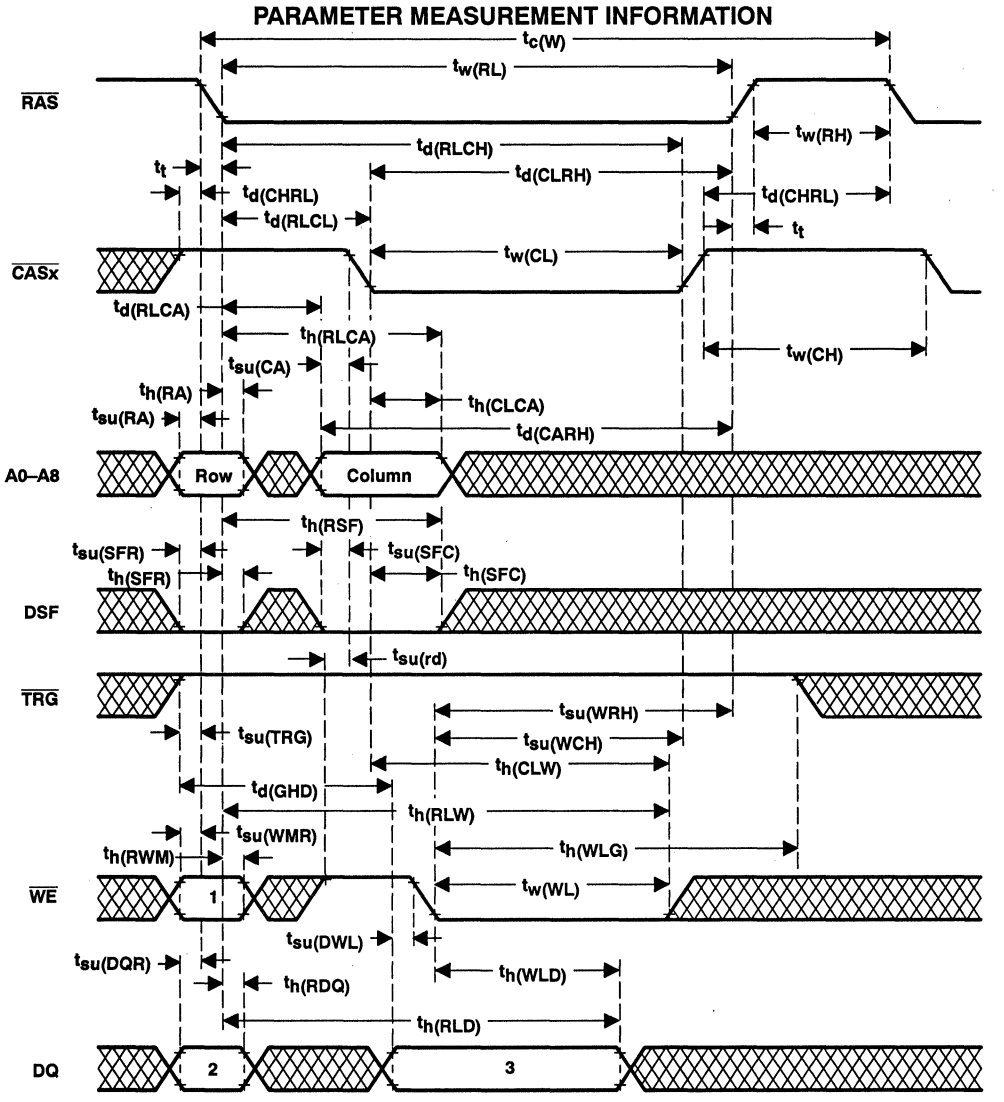
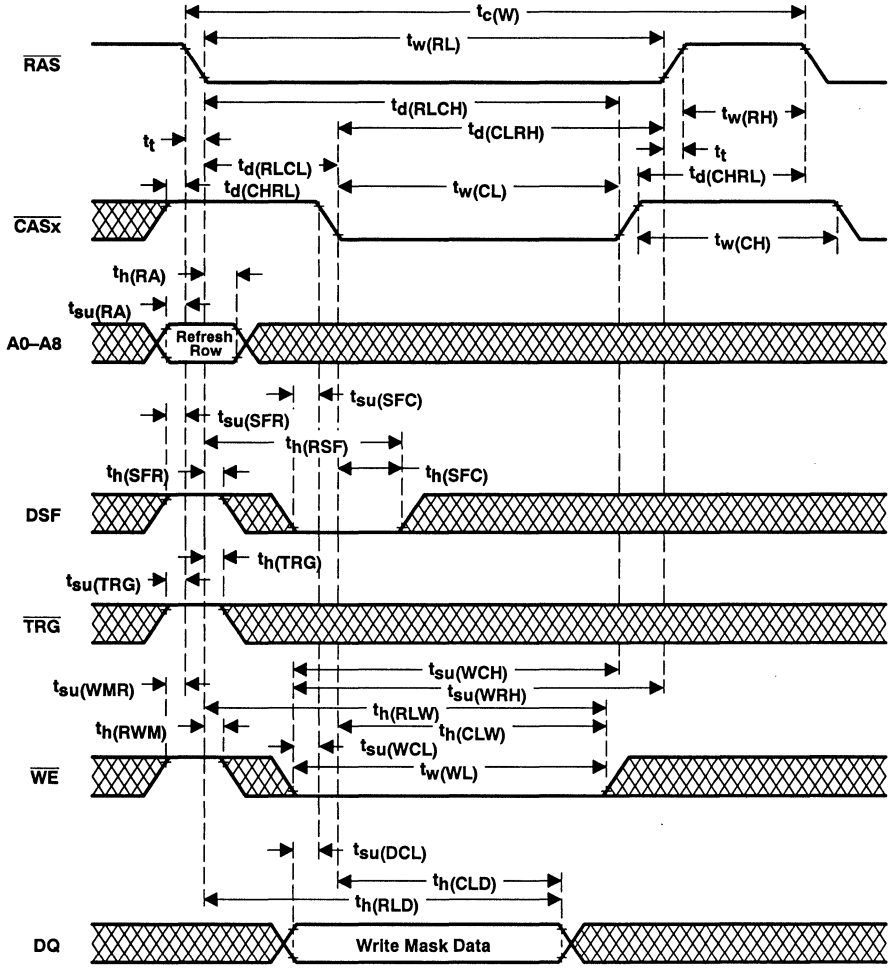


Figure 24. Late Write Cycle Timing (Output-Enable-Controlled Write)

Table 6. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

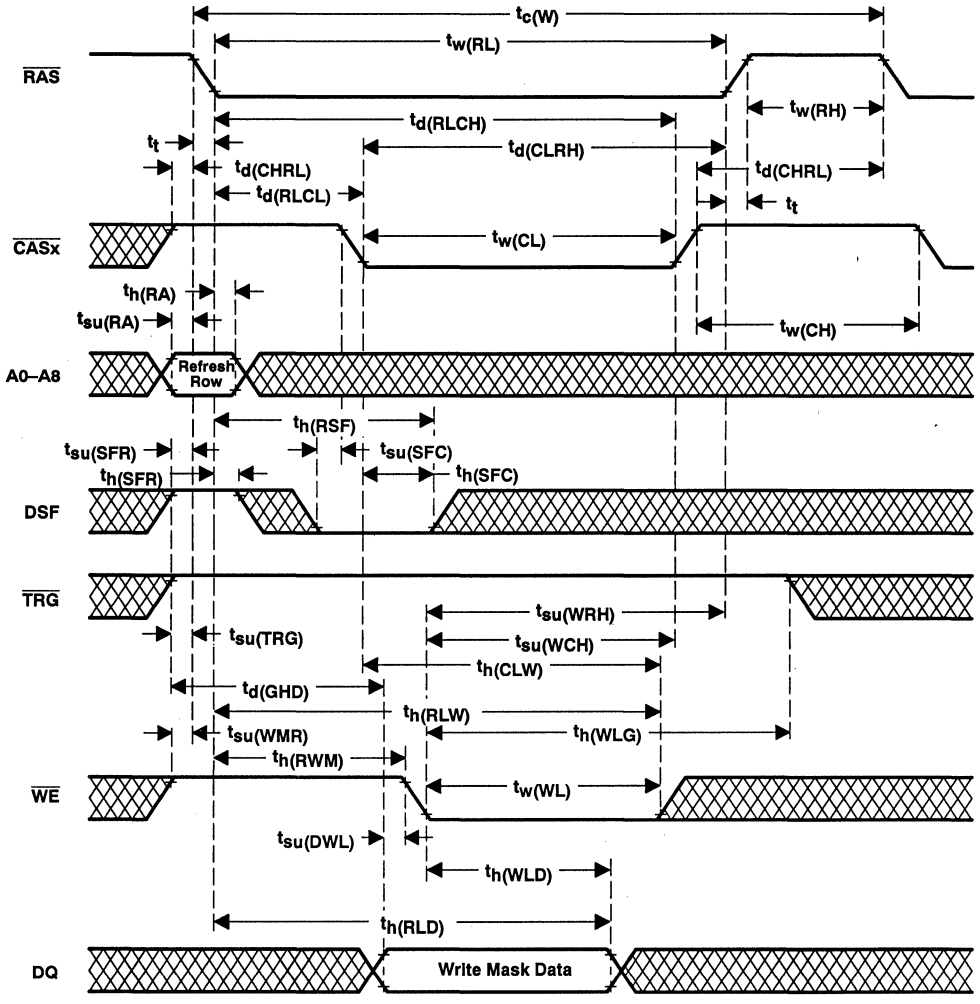
PARAMETER MEASUREMENT INFORMATION



† Load Mask register cycle will put the device into the persistent write-per-bit mode.

Figure 25. Load Mask Register Timing (Early Write Load)†

PARAMETER MEASUREMENT INFORMATION



† Load Mask register cycle will put the device into the persistent write-per-bit mode.

Figure 26. Load Mask Register Timing (Late Write Load)†

PARAMETER MEASUREMENT INFORMATION

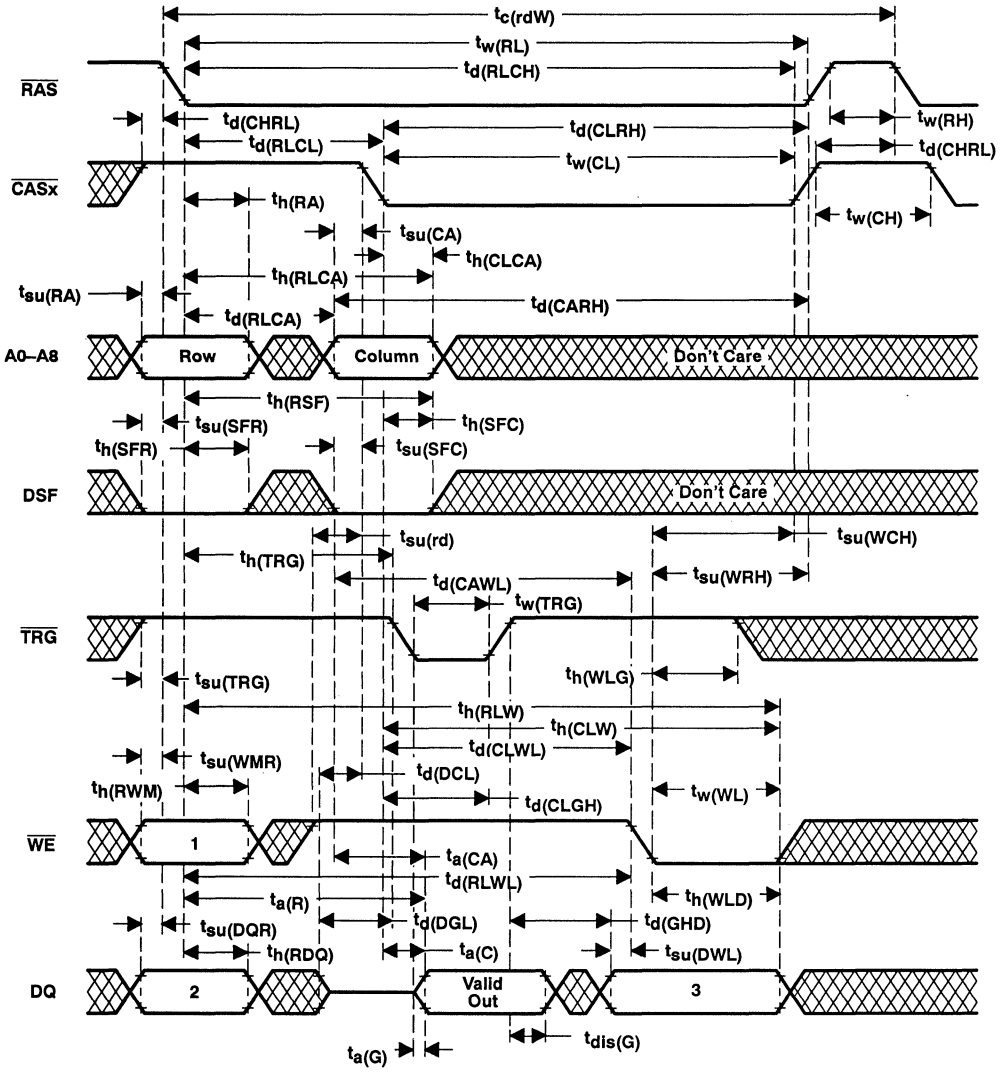
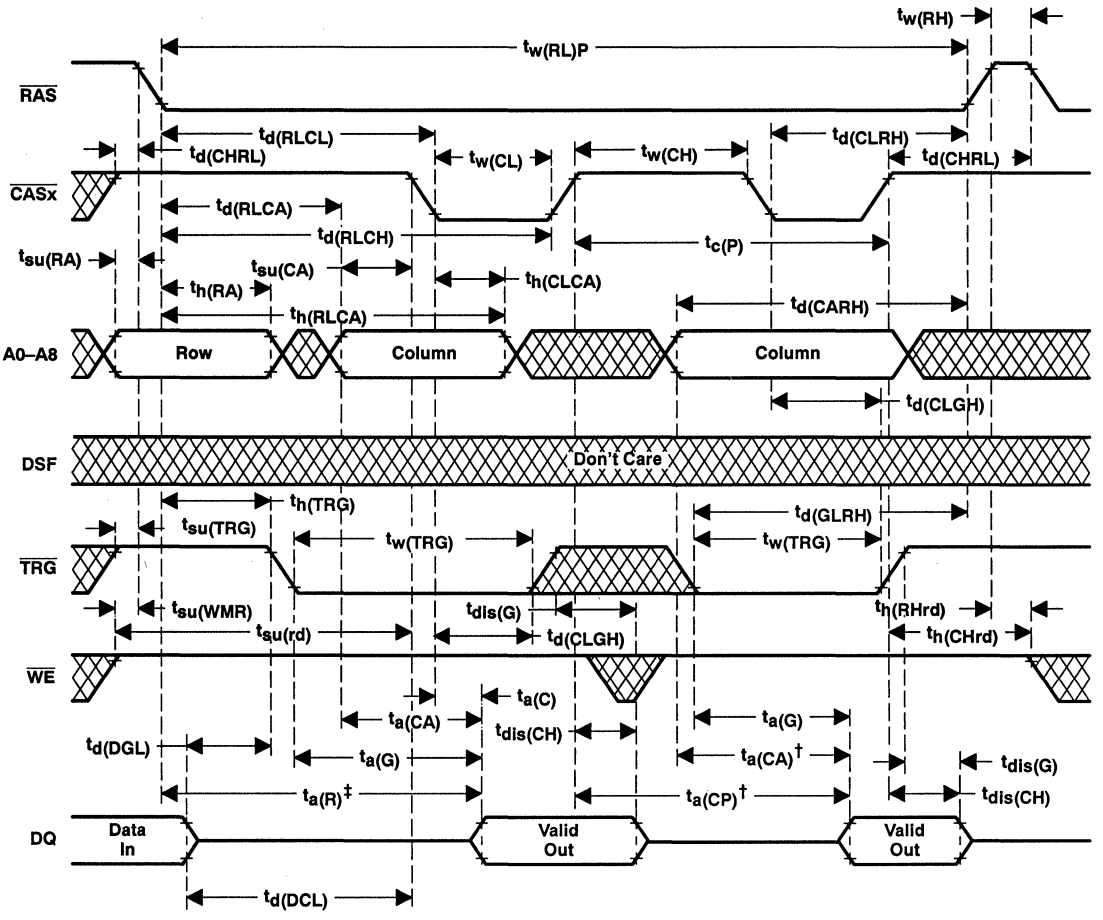


Figure 27. Read-Write/Read-Modify-Write Cycle Timing

Table 7. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

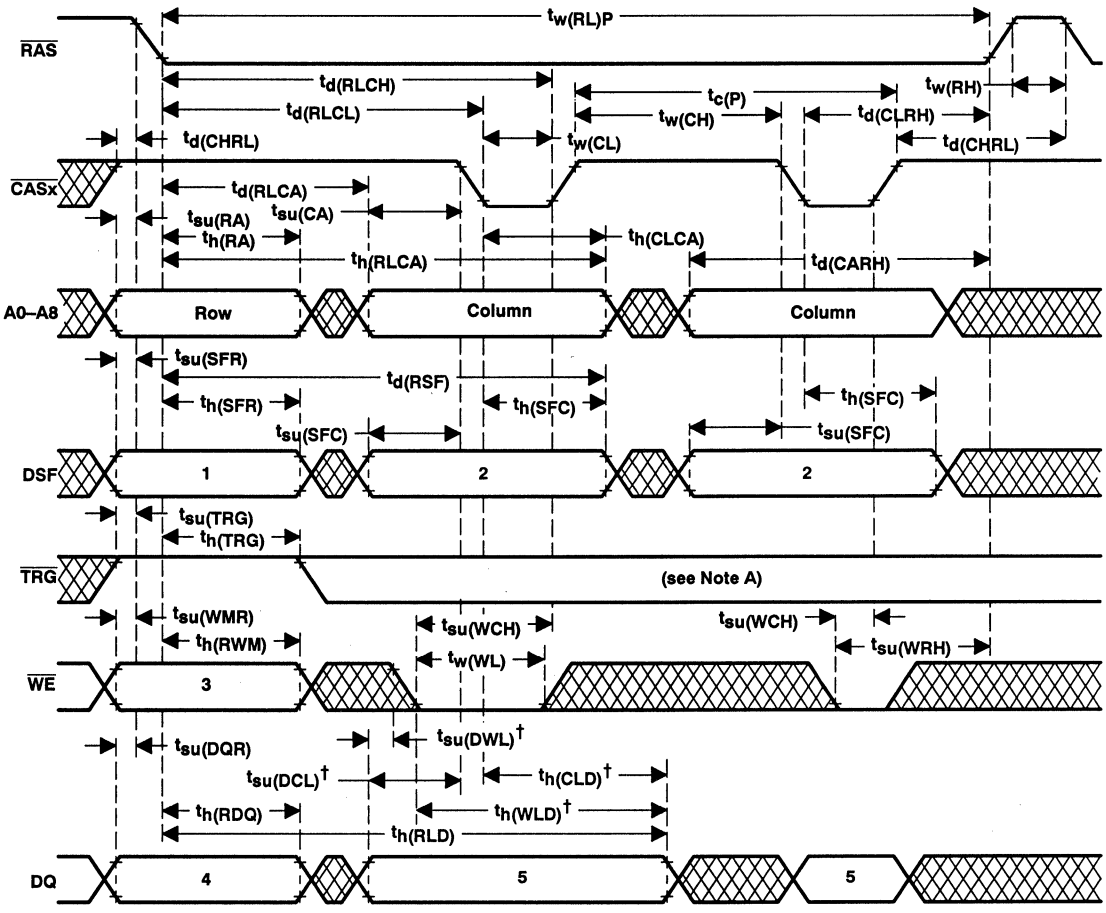
PARAMETER MEASUREMENT INFORMATION



† Access time $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.)

Figure 28. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first $\overline{WE}$ falling edge or the falling edge of $\overline{CASx}$, whichever occurs later.

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write features is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

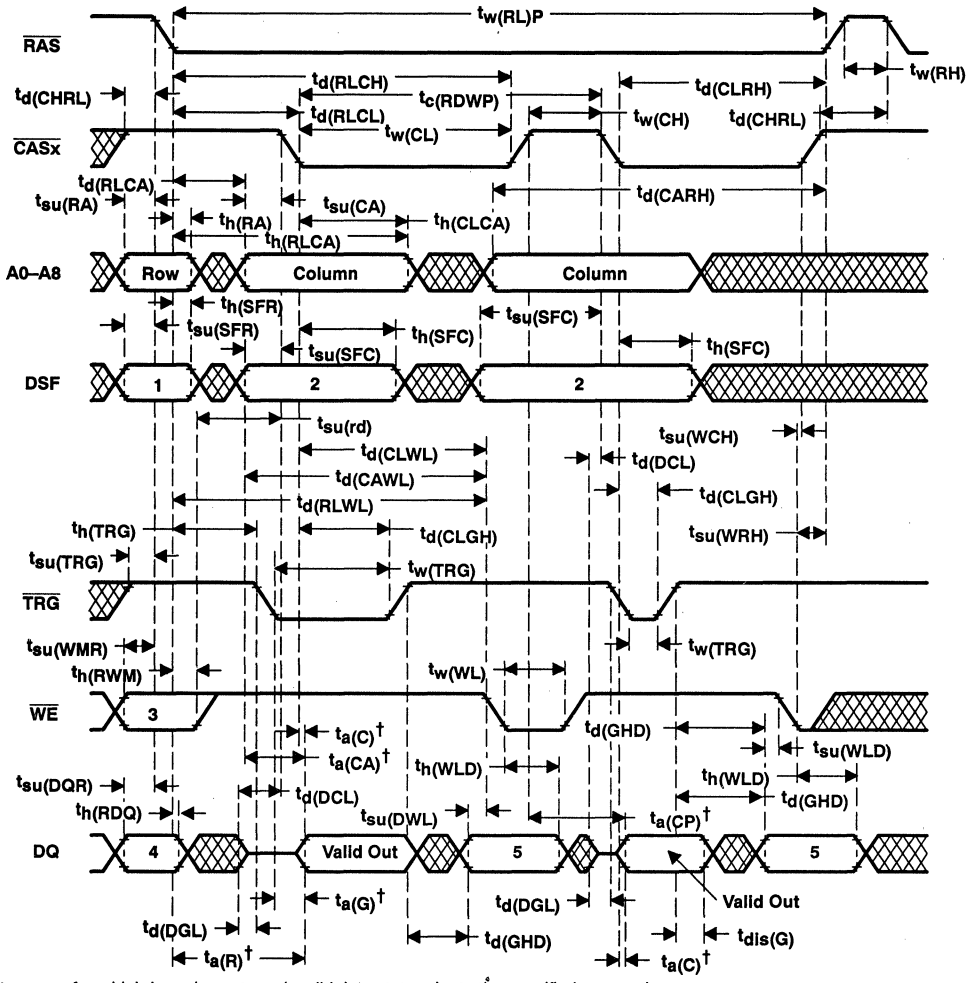
Figure 29. Enhanced Page-Mode Write Cycle Timing

Table 8. Write Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (non-masked)	L	L	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first $\overline{WE}$ falling edge or the falling edge of $\overline{CASx}$, whichever occurrs later.‡	H	L	H	Don't care	Write mask

‡ Load write mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CASx}$ is don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output may go from high-impedance to an invalid data state prior to the specified access time.

NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 30. Enhanced Page-Mode Read-Modify-Write Cycle Timing

Table 9. Write Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (non-masked)	L	L	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first $\overline{WE}$ falling edge or the falling edge of $\overline{CAS}$x, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load write mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$x is don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION

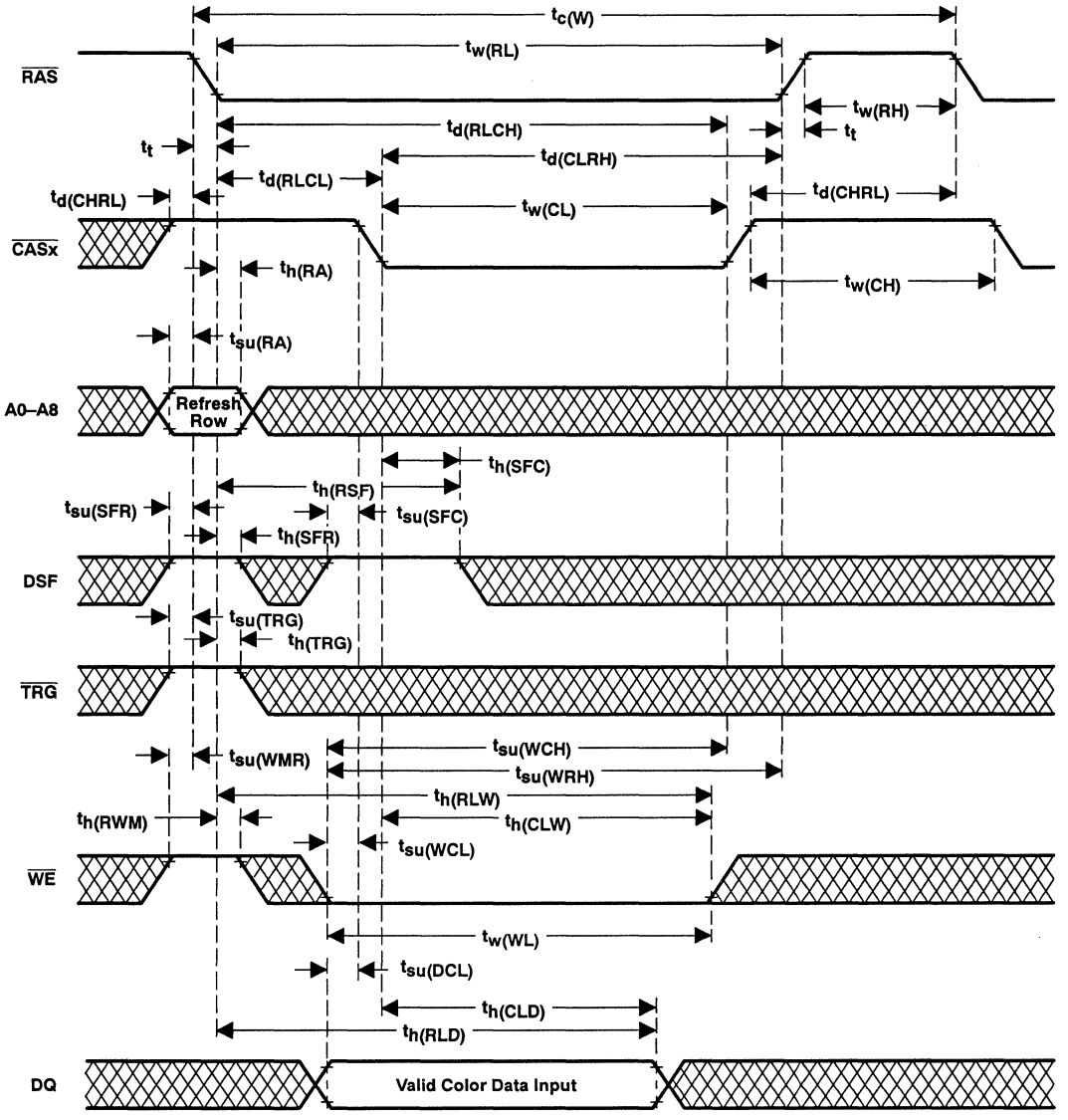


Figure 31. Load Color Register Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

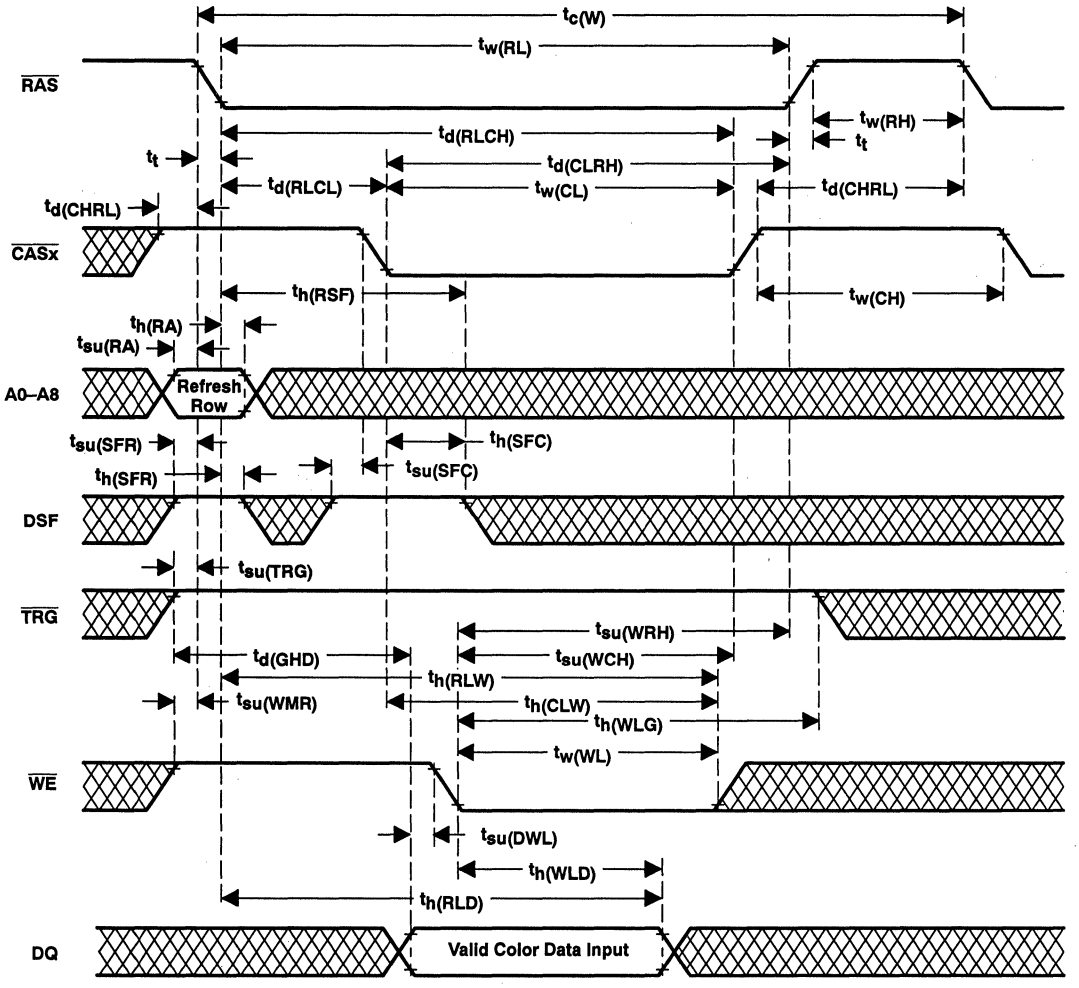


Figure 32. Load Color Register Timing (Late Write Load)

PARAMETER MEASUREMENT INFORMATION

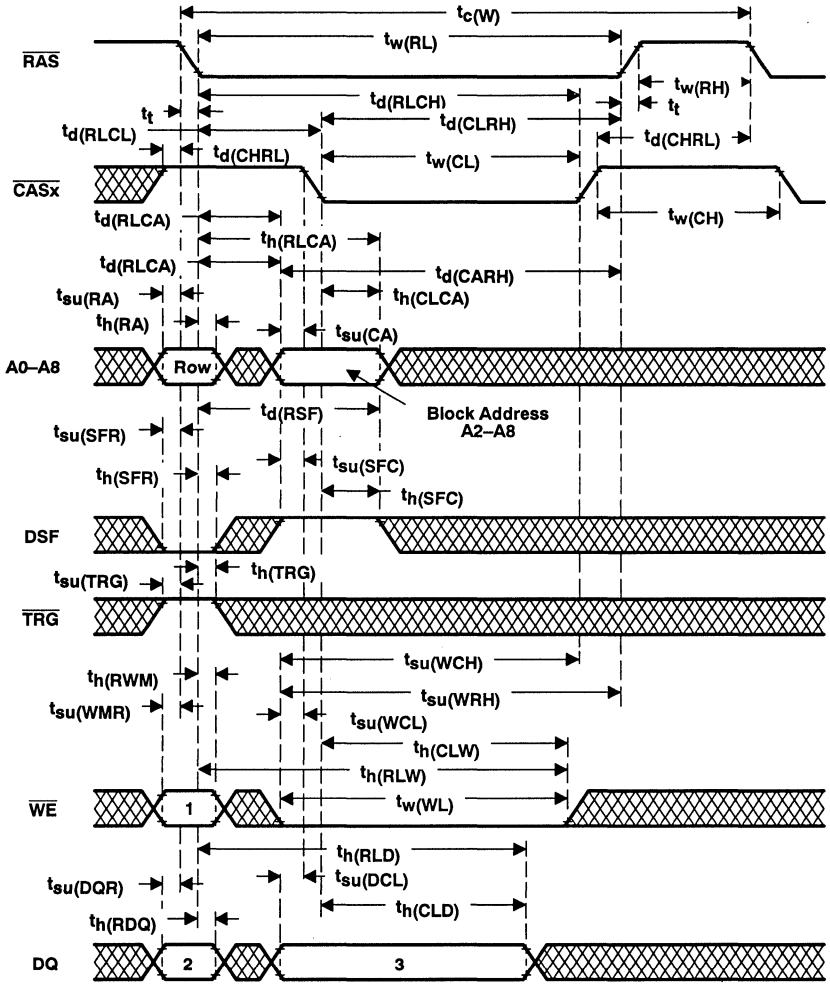


Figure 33. Block Write Timing (Early Write)

Table 10. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION

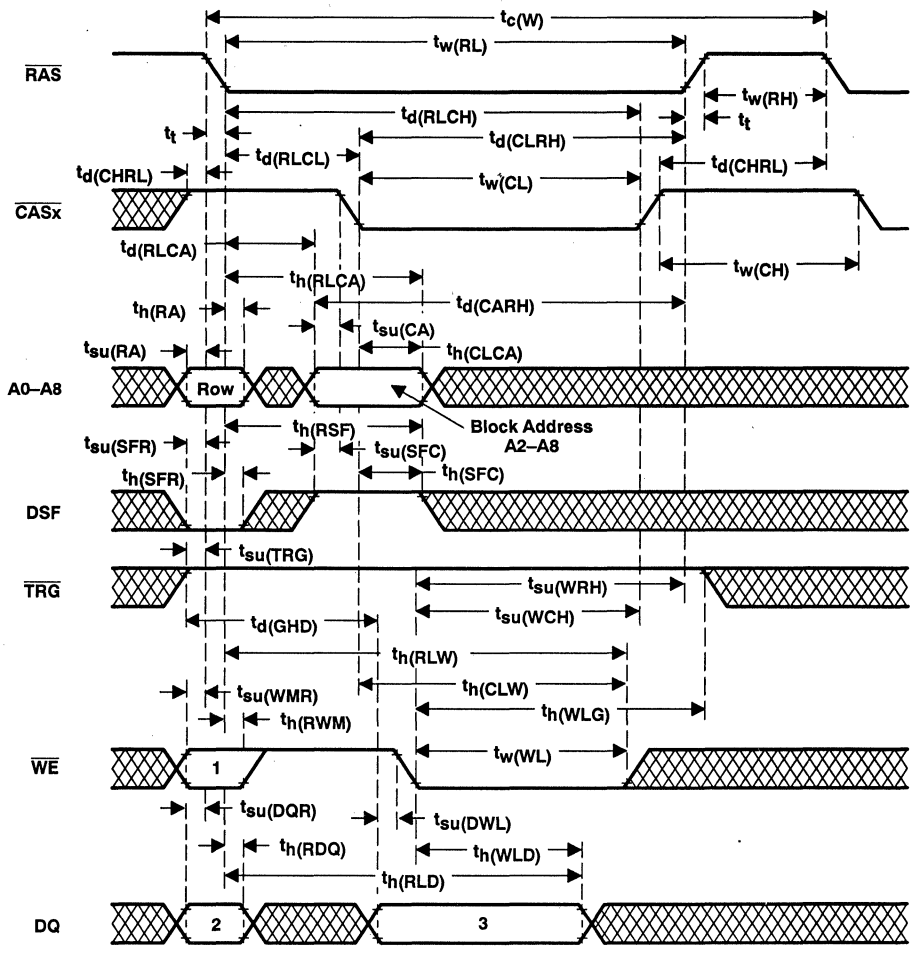


Figure 34. Block Write Timing (Late Write)

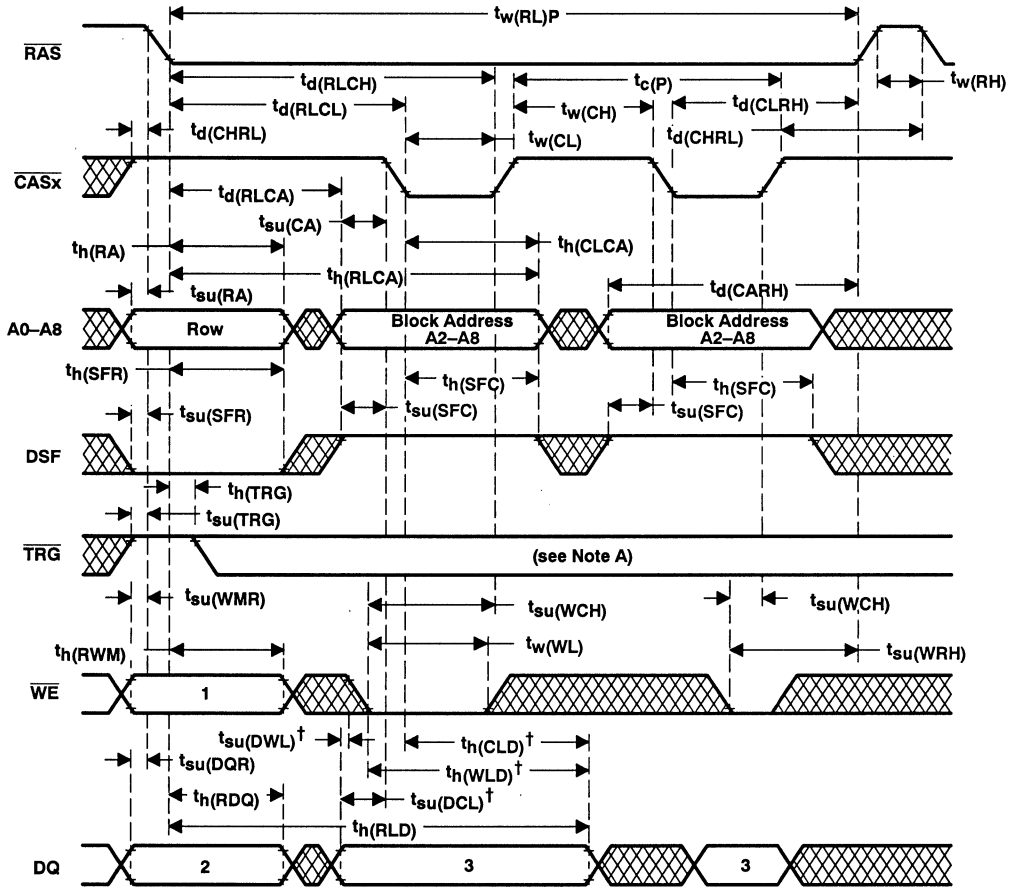
Table 11. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first $\overline{WE}$ falling edge or the falling edge of $\overline{CASx}$, whichever occures later.

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 35. Enhanced Page-Mode Block Write Cycle Timing

Table 12. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address $A_1 = 0$, $A_0 = 0$)
DQ_1 — column 1 (address $A_1 = 0$, $A_0 = 1$)
DQ_2 — column 2 (address $A_1 = 1$, $A_0 = 0$)
DQ_3 — column 3 (address $A_1 = 1$, $A_0 = 1$)

PARAMETER MEASUREMENT INFORMATION

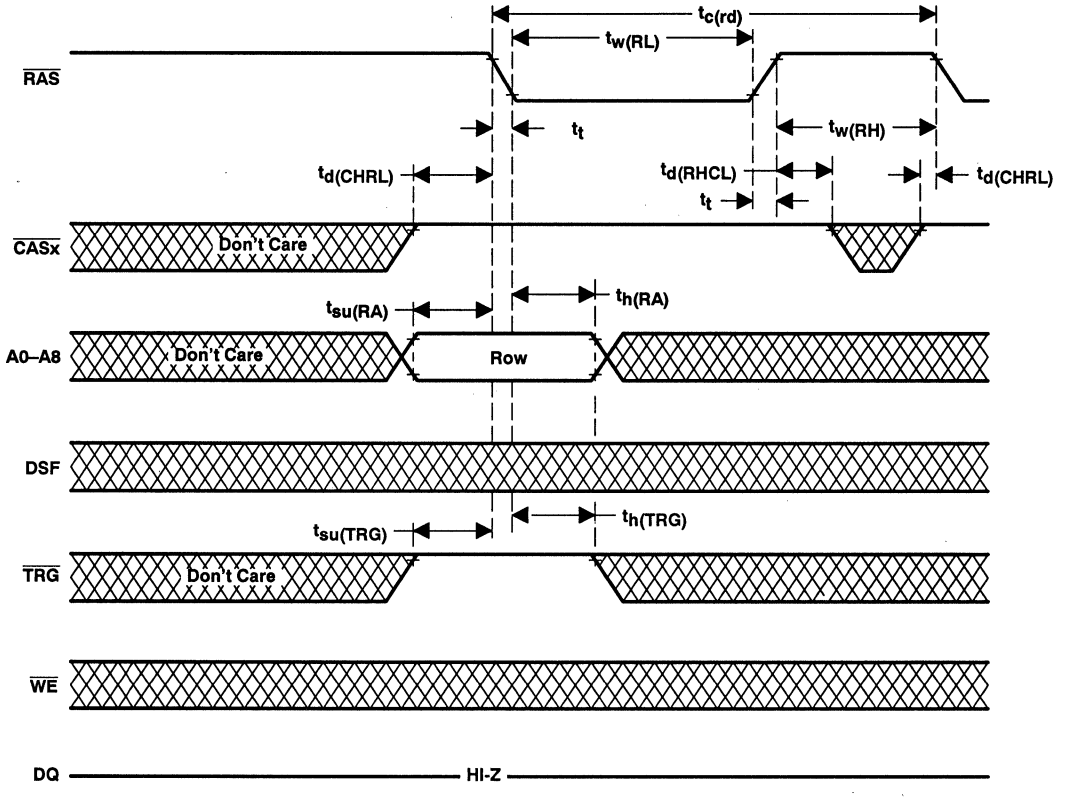


Figure 36. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

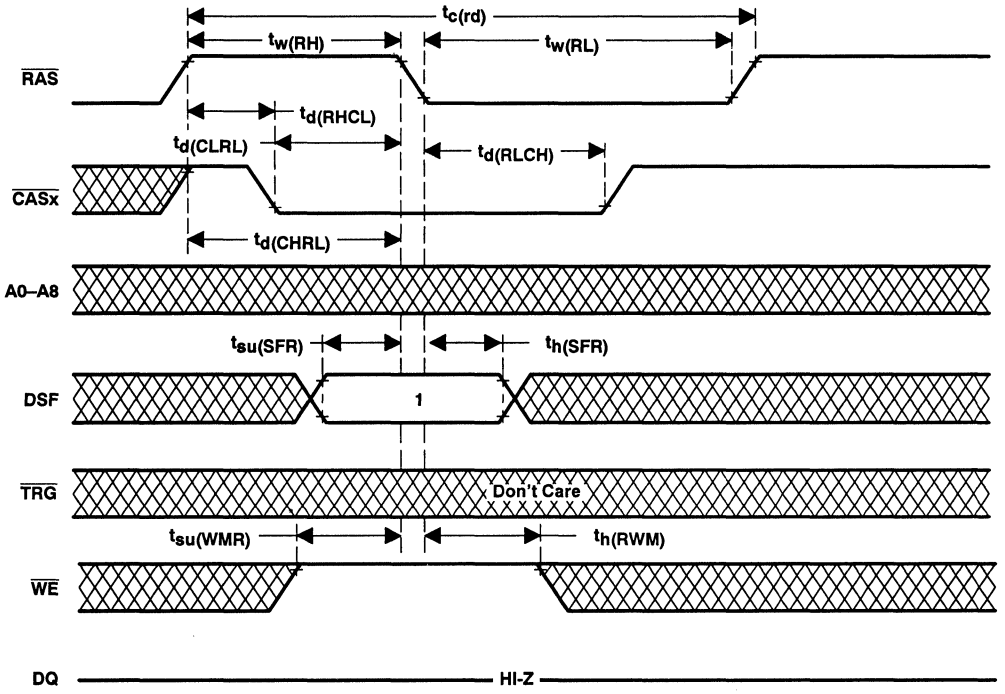
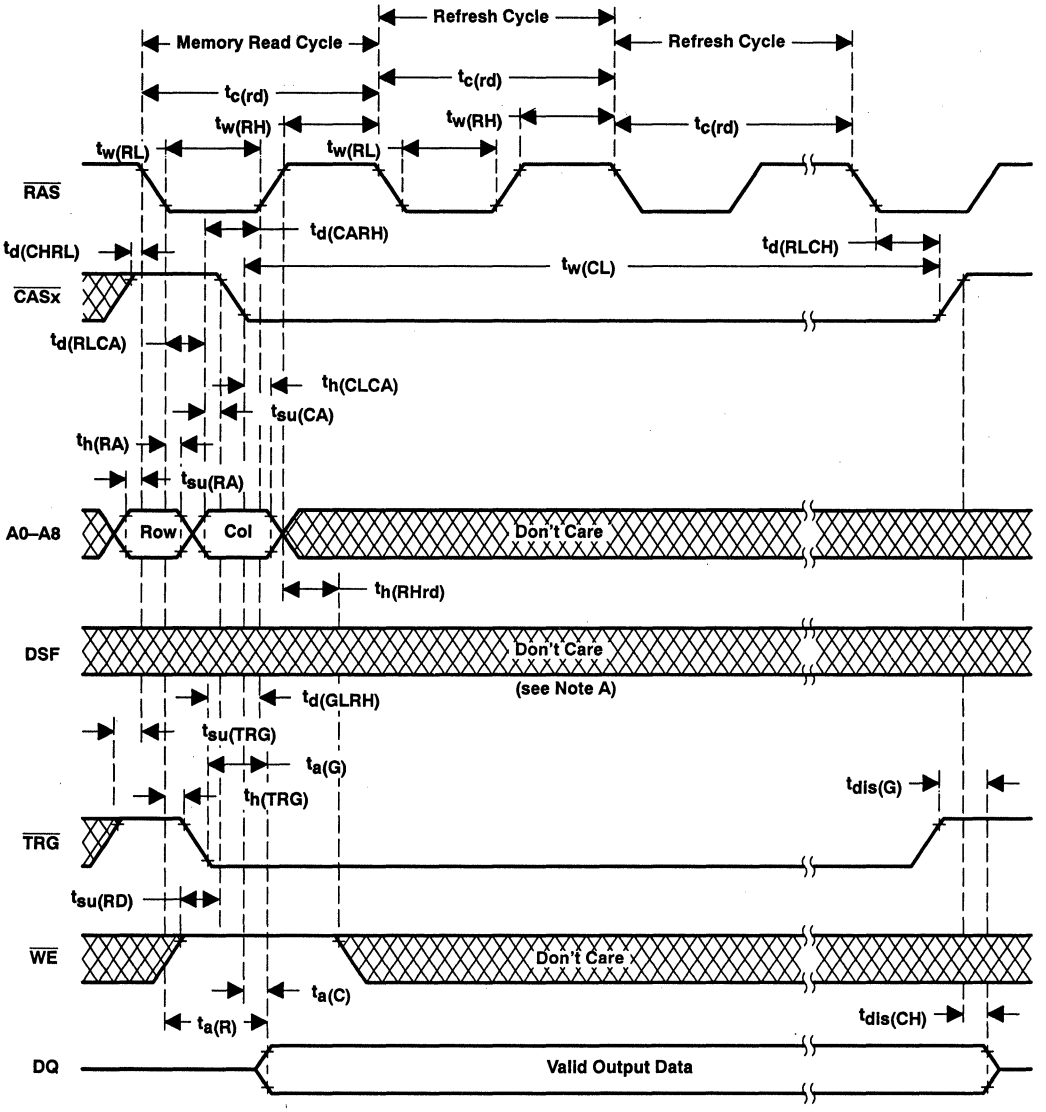


Figure 37. CAS-Before-RAS Refresh

Table 13. CBR Cycle State Table

CYCLE	STATE
	1
CAS-before-RAS refresh with option reset	0
CAS-before-RAS refresh with no reset	1

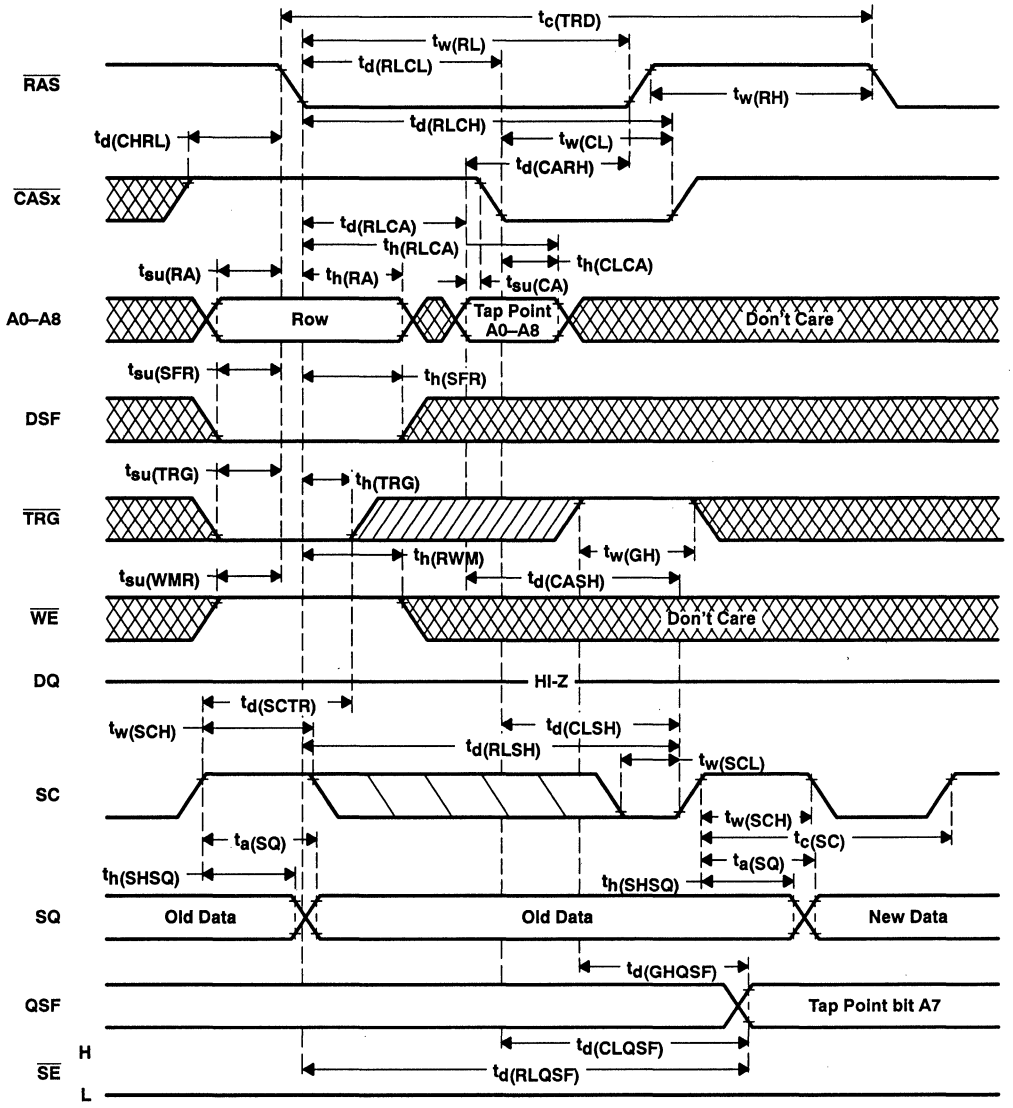
PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CAS}$-before-$\overline{RAS}$ refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at $\overline{RAS}$.

Figure 38. Hidden Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

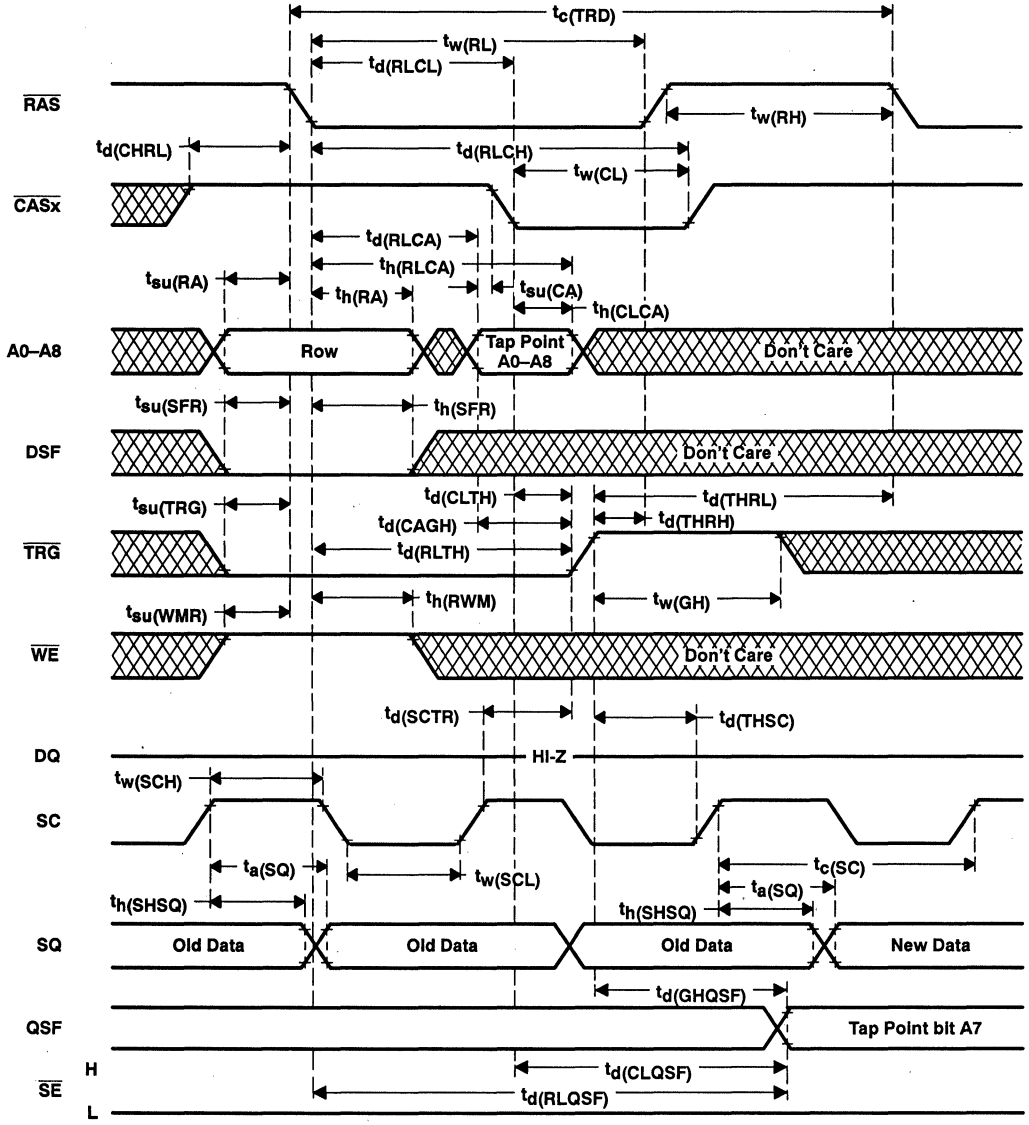
NOTES: A. Random mode (DQ outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: Register tap point, A8: which half of the transferred row.

Figure 39. Read Transfer Timing, Early Load Operations†

PARAMETER MEASUREMENT INFORMATION



† Late load operation is defined as $t_{d(THRH)} < 0$ ns.

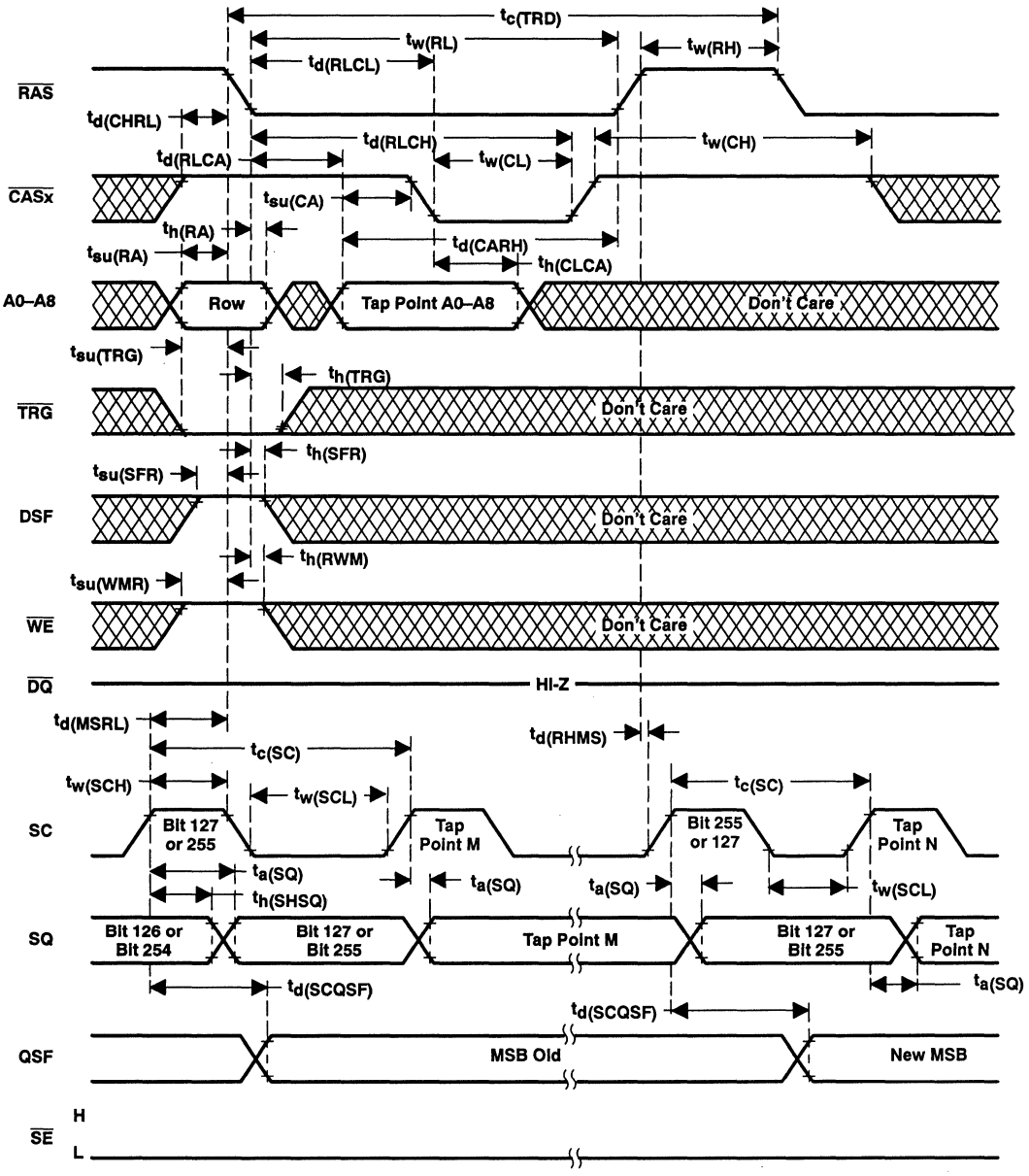
NOTES: A. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

B. Random mode (DQ outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

C. A0–A7: Register tap point, A8: which half of the transferred row.

Figure 40. Read Transfer Timing, Real-Time Reload Operation/Late Load Operation†

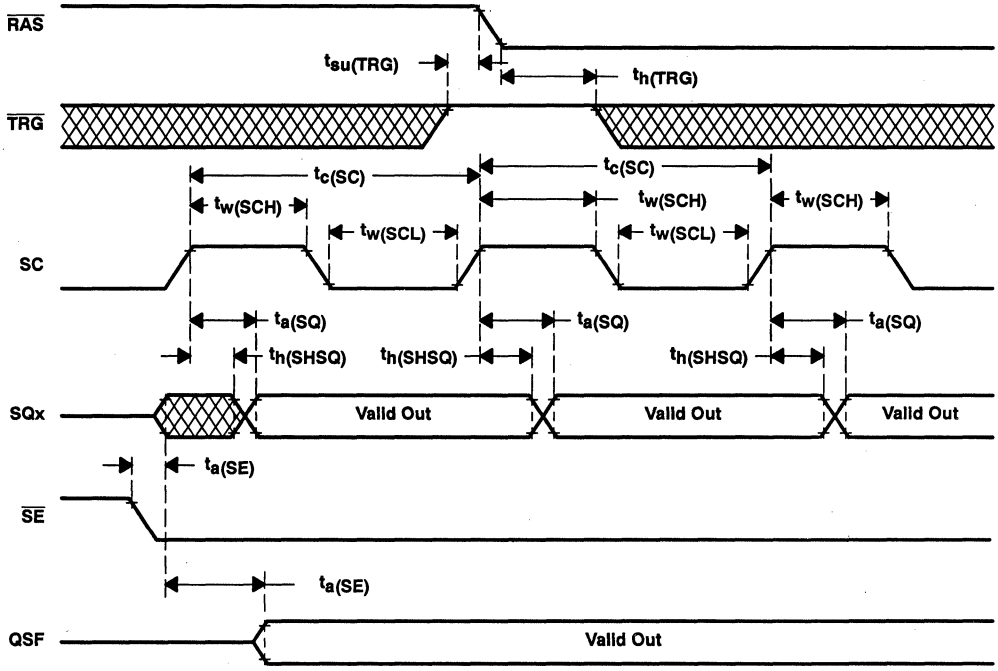
PARAMETER MEASUREMENT INFORMATION



NOTES: A. There must be a minimum of two SC clock cycles between any two split-register reload cycles, and between a transfer read cycle and a split-register cycle.
B. A0–A6: Tap point of the given half, A7: Don't care, A8: DRAM row half.

Figure 41. Split-Register Read Transfer Timing

PARAMETER MEASUREMENT INFORMATION

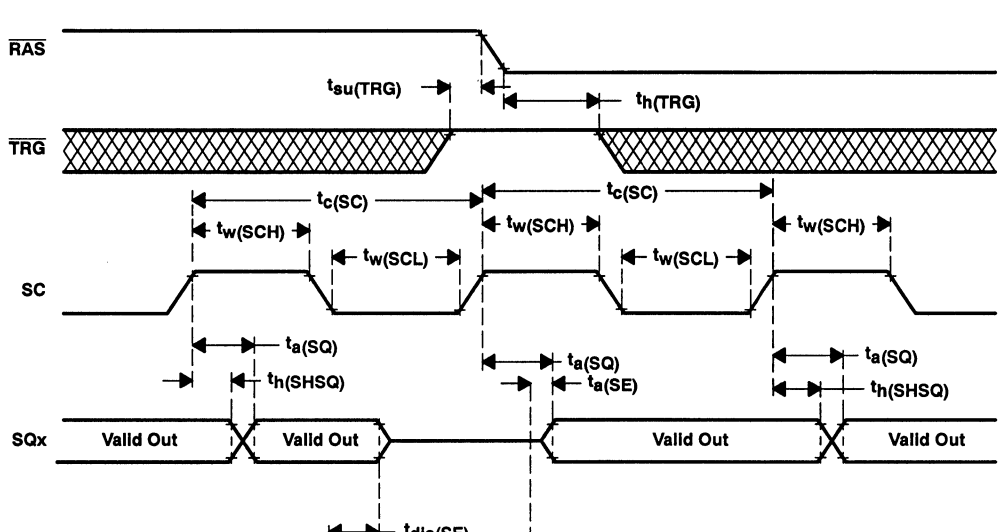


NOTES: A. While reading data through the serial data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

Figure 42. Serial Read Timing

PARAMETER MEASUREMENT INFORMATION

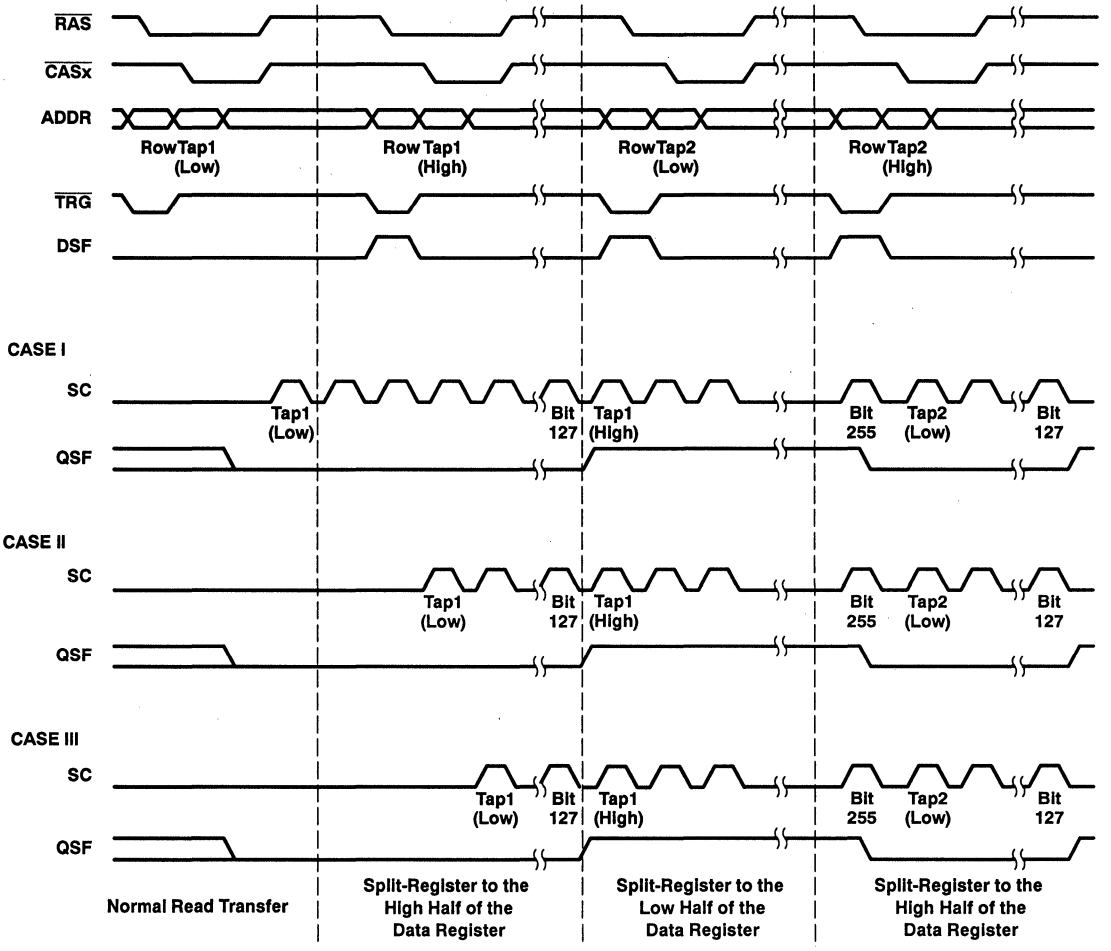


NOTES: A. While reading data through the serial data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

Figure 43. Serial Read Timing ($\overline{SE}$ Controlled Read)

OPERATING SEQUENCE INFORMATION

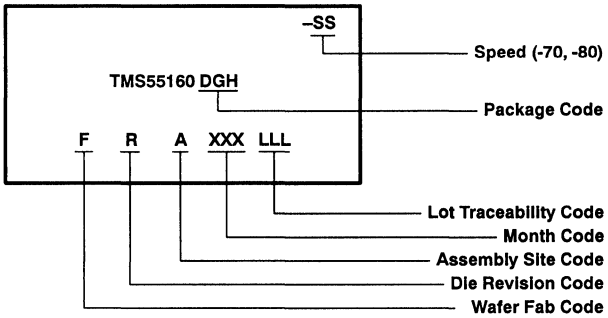


NOTES: A. In order to achieve proper split-register operation, a normal read transfer should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the normal read transfer cycle (CASE I), during the first split-register transfer cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the normal read transfer cycle and the first split-register cycle.

B. A split register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255). There is a minimum requirement of one rising edge of SC clock between two split-register transfer cycles.

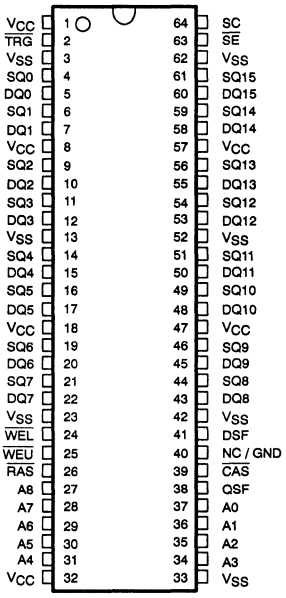
Figure 44. Split-Register Operating Sequence

device symbolization



- **DRAM : 262 144 Words × 16 Bits SAM: 256 Words × 16 Bits**
- **Dual Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{WEL}$, $\overline{WEU}$) Provides Flexibility**
- **Enhanced Page Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **Long Refresh Period: Every 8 ms (Max)**
- **DRAM Port Is Compatible With the TMS45165**
- **Up to 45-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial Register Starting Locations**
- **$\overline{SE}$ Controlled Register Status QSF**
- **Split Serial-Data Register for Simplified Realtime Register Reload**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE† (TOP VIEW)



† Package is shown for pinout rererence only.

PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ15	DRAM Data I/O, Write Mask Data
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WEL}$, $\overline{WEU}$	DRAM Byte Write Enable Selects
DSF	Special Function Select
QSF	Special Function Output
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: Not Connected Internally to V_{SS})

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(rd\ W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55165-70	70 ns	20 ns	130 ns	45 ns	22 ns	165 mA	205 mA
TMS55165-80	80 ns	25 ns	150 ns	50 ns	30 ns	160 mA	195 mA

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description

The TMS55165 Multiport Video RAM is a high-speed dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 16 bits each, interfaced to a serial data register [Serial Access Memory (SAM)], organized as 256 words of 16 bits each. The TMS55165 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55165 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55165 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block write feature. The block write mode allows sixteen bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column address locations. As many as 64 bits of data can be written to memory during each $\overline{\text{CAS}}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit allows masking any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles without reloading. The TMS55165 also offers byte write capability. Byte write control can be applied in write cycles, block write cycles, load mask register cycles, and load color register cycles.

The TMS55165 offers a split-register transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This real-time register reload implementation allows truly continuous serial data. For applications not requiring real-time register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 45 MHz. During the split register transfer reads, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, designated QSF, is included to indicate which half of the serial register is active at any given time in split register mode.

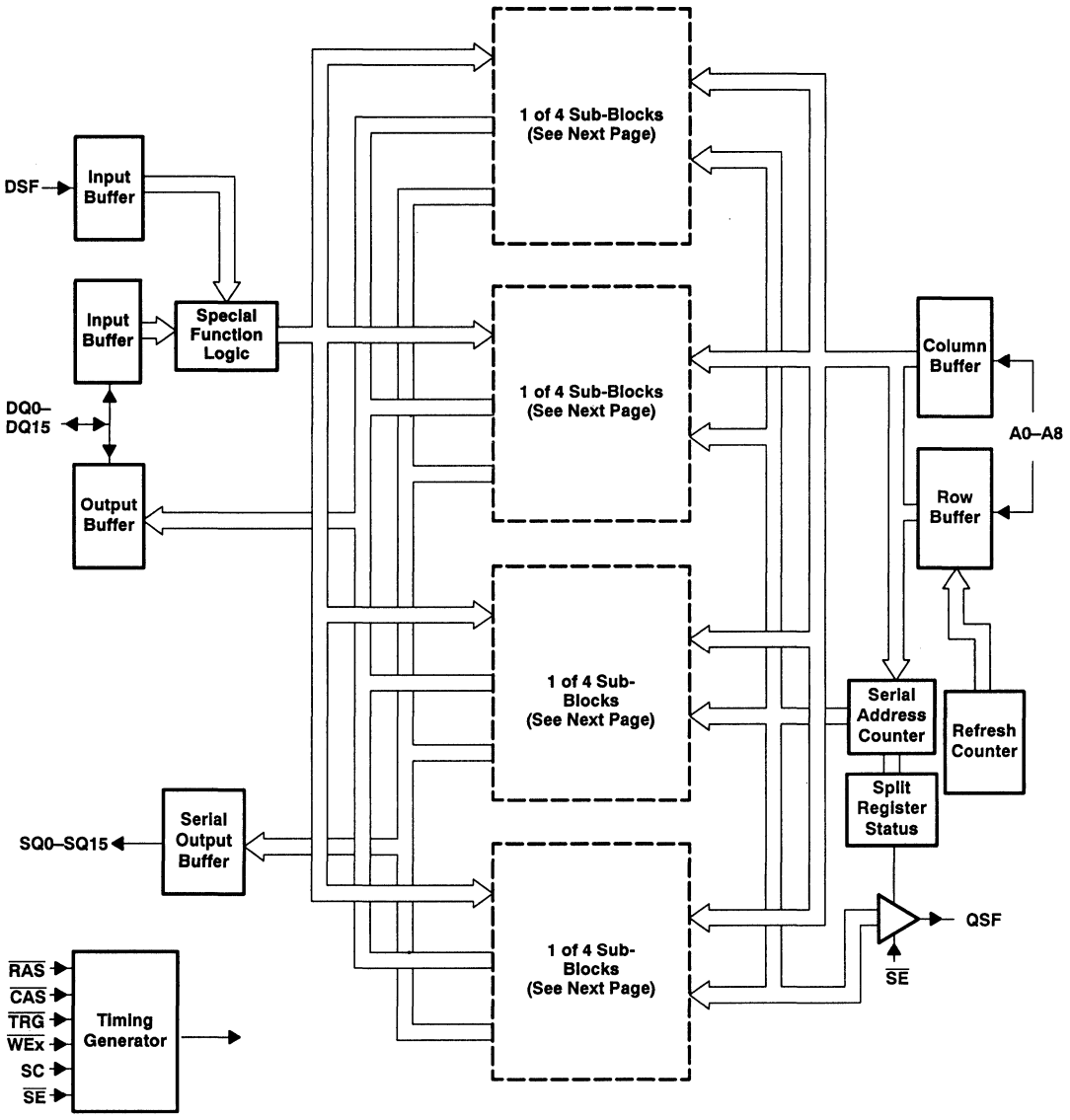
All inputs, outputs, and clock signals on the TMS55165 are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS55165 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS55165 is offered in a 64-pin super-small-outline gull-wing leaded package for direct surface mounting.

The TMS55165 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)

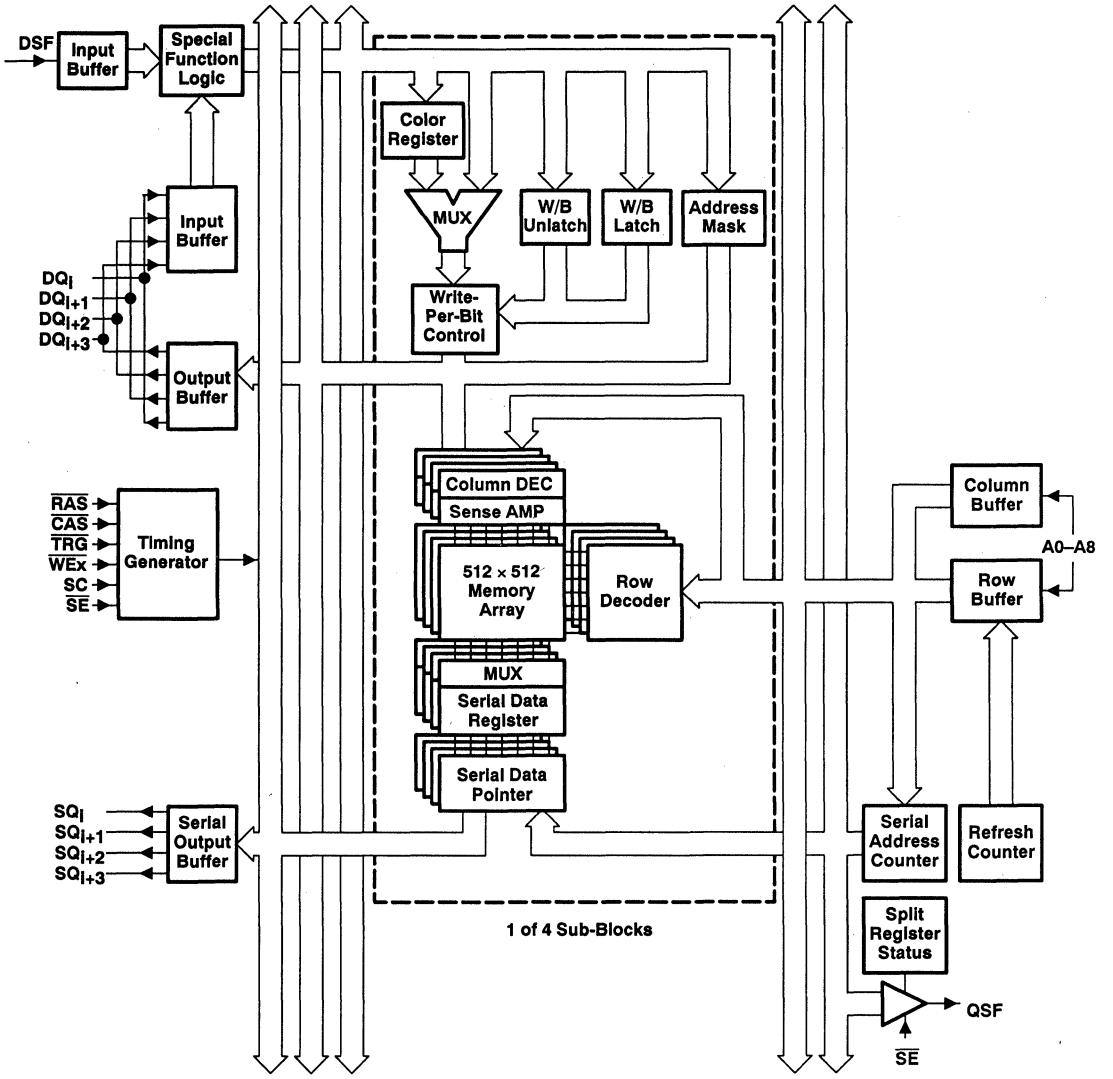


Table 1. Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15‡		MNE CODE
	CAS	TRG	WEx†	DSF	DSF	RAS	CAS	RAS	CAS WEL WEU	
Reserved (do not use)	0	0	0	0	X	X	X	X	X	—
CAS-before-RAS refresh (option reset)§	0	X	1	0	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)¶	0	X	1	1	X	X	X	X	X	CBRN
Read transfer	1	0	1	0	X	Row Addr	Tap Point	X	X	RT
Split-register read transfer	1	0	1	1	X	Row Addr	Tap Point	X	X	SRT
DRAM write (non-persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Add	Write Mask	Valid Data	RWM
DRAM block write (non-persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (non-masked)	1	1	1	0	0	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (non-masked)	1	1	1	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write mask register #	1	1	1	1	0	Refresh Addr	X	X	Write Mask	LMR
Load color register	1	1	1	1	1	Refresh Addr	X	X	Color Data	LCR

† Logic 0 is selected when either or both WEL and WEU are low.
‡ DQ0–DQ15 are latched on either the first WEx falling edge or the falling edge of CAS, whichever occurs later.
§ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at RAS.
¶ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode.
# Load Write Mask Register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.
X: = Don't care.
Column Mask: 1 = Write to address/column location enabled.
Write Mask: 1 = Write to I/O enabled.

Table 2. Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, column address	Row-address, Tap point	
$\overline{CAS}$	Column-address strobe, DQ output enable	Tap address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block write enable, Write mask register load enable, Color register load enable $\overline{CAS}$-before-$\overline{RAS}$ (option reset)	Split register transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WEL}$ / $\overline{WEU}$	Byte write enable, Write-per-bit enable		
QSF			Serial register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V Supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply, and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262 144 storage locations. Nine row address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$.

During the read transfer operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer will occur. At the falling edge of $\overline{CAS}$, the column address bits A0–A8 are latched. The most significant column address bit (A8) selects which half of the row will be transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During split register read transfer operation, address bit A7 is ignored at the falling edge of $\overline{CAS}$. An internal counter will select which half of the register will be used. If the high half of the SAM is currently in use, the low half of the SAM will be loaded with the low half of the DRAM half row, and vice versa. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WEL}$, $\overline{WEU}$, $\overline{TRG}$, $\overline{CAS}$, and DSF onto the chip to invoke DRAM and read transfer functions of the TMS55165.

column-address strobe ($\overline{CAS}$)

$\overline{CAS}$ is a control input that latches the states of the column address and DSF to control DRAM and read transfer functions of the TMS55165. When $\overline{CAS}$ is brought low during a transfer cycle, the address bits A0–A8 will be latched at the start position (tap) for the serial data output. $\overline{CAS}$ also acts as an output enable for the DRAM output pins, DQ0–DQ15.

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins, DQ0–DQ15.

For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WEU}$, $\overline{WEL}$)

In DRAM operation, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7), and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). Both $\overline{WEL}$ and $\overline{WEU}$ have to be held high together to select the read mode. Bringing either or both $\overline{WEL}$ and $\overline{WEU}$ low will select the write mode.

$\overline{WEL}$ and $\overline{WEU}$ are also used to select the DRAM write-per-bit mode of operation. If either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low as $\overline{RAS}$ falls during a DRAM write cycle, the write-per-bit operation is invoked. The TMS55165 supports both the non-persistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address. DSF determines which of the following functions below are invoked on a particular cycle:

- CBR refresh with reset (CBR)
- CBR refresh with no reset (CBRN)
- Block write
- Loading mask register for the persistent write-per-bit mode
- Loading color register for the block write mode
- Split-register read transfer

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The three-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance (floating) state as long as either $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. Either $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In a read transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

The write-per-bit mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$.

serial data output (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data-out is the same polarity as data-in. The serial outputs are in the high-impedance (floating) state as long as serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55165 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

serial enable ($\overline{SE}$)

During serial access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low will enable the serial data output. $\overline{SE}$ high will disable the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, then the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon crossing a boundary between the two SAM halves.

During the read transfer operation (non-split register), QSF may change state upon completing the cycle. This state is determined by the tap point being loaded during the transfer cycle. During the split-register read transfer operation, QSF may change state upon crossing a boundary between the two SAM halves.

QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, then QSF output will be in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	RAS FALL				CAS FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CAS	TRG	WEx‡	DSF	DSF	RAS	CAS	RAS	CAS WEL WEU	
Reserved (do not use)	0	0	0	0	X	X	X	X	X	—
CAS-before-RAS refresh (option reset)§	0	X	1	0	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)¶	0	X	1	1	X	X	X	X	X	CBRN
DRAM write (non-persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (non-persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	1	1	0	0	0	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	1	1	0	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
DRAM write (non-masked)	1	1	1	0	0	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (non-masked)	1	1	1	0	1	Row Addr	Block Addr A2–A8	X	Col Mask	BW
Load write mask register#	1	1	1	1	0	Refresh Address	X	X	Write Mask	LMR
Load color register	1	1	1	1	1	Refresh Address	X	X	Color Data	LCR

† DQ0–DQ15 are latched on either the first WEx falling edge or the falling edge of CAS, whichever occurs later.
‡ Logic 0 is selected when either or both WEL and WEU are low.
§ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at RAS.
¶ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode.
# Load Write Mask Register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.
X: = Don't care.
Column Mask: 1 = Write to address/column location enabled.
Write Mask: 1 = Write to I/O enabled.

refresh

CAS-before-RAS refresh

CAS-before-RAS refreshes are accomplished by bringing CAS low earlier than RAS. The external row address is ignored and the refresh address is generated internally. Two types of CBR refresh cycles are available. The CBR refresh (option reset) will end the persistent write-per-bit mode. The CBRN refresh (no reset) will not end the persistent write-per-bit mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively, as long as the entire refresh is completed within the required time period $t_{rf(MA)}$. Other cycles may be performed in between CAS-before-RAS cycles without disturbing the internal address generation. The output buffers remain in the high-impedance state during the CAS-before-RAS refresh cycles, regardless of the state of TRG.

hidden refresh

A hidden refresh is accomplished by holding $\overline{CAS}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the $\overline{CAS}$-before-$\overline{RAS}$ refresh, the refreshed row addresses are generated internally during the hidden refresh. Hidden refresh will also end the peristent write-per-bit mode, regardless of the state of $\overline{TRG}$.

$\overline{RAS}$ only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CAS}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

enhanced page mode

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row address setup, row address hold, and address multiplex. The maximum $\overline{RAS}$ low time and $\overline{CAS}$ page cycle time used determines the number of columns that may be accessed.

Unlike conventional page mode operations, the enhanced page mode allows the TMS55165 to operate at a higher data bandwidth. Data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied.

byte write operation

Byte write operations can be applied in DRAM write cycles, block write cycles, load mask register cycles, and load color register cycles.

Holding either or both $\overline{WEL}$ and $\overline{WEU}$ low will select the write mode. In normal write cycles, $\overline{WEL}$ enables data to be written to the lower byte (DQ0–DQ7), and $\overline{WEU}$ enables data to be written to the upper byte (DQ8–DQ15). For early write cycles, one of $\overline{WEx}$ is brought low before $\overline{CAS}$ falls. The other $\overline{WEx}$ can be brought low before $\overline{CAS}$ falls or after $\overline{CAS}$ falls. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{CAS}$ (see Figure 1).

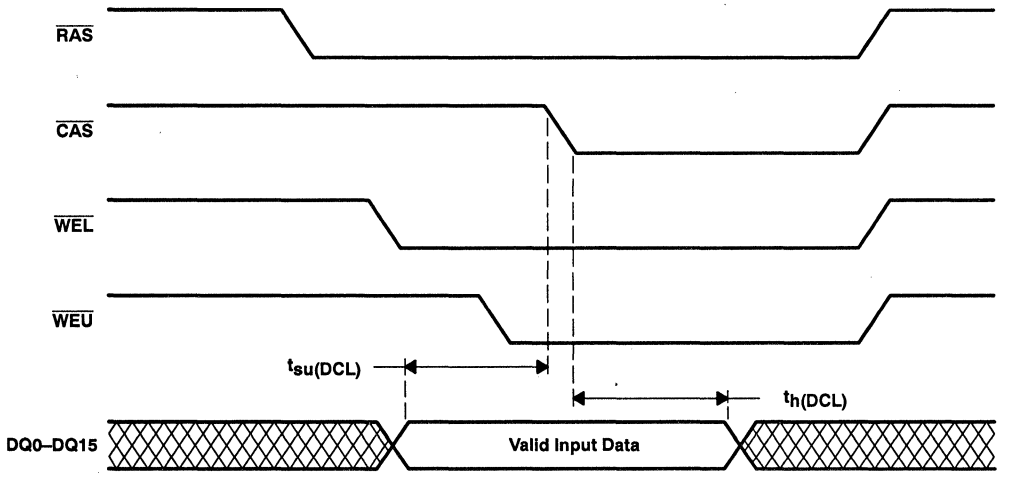


Figure 1. Example of an Early Write

For late write or read-modify-write cycles, $\overline{WEL}$ and $\overline{WEU}$ are both held high before $\overline{CAS}$ falls. After $\overline{CAS}$ falls, either or both $\overline{WEL}$ and $\overline{WEU}$ are brought low to select the corresponding byte or bytes to be written. Data will be strobed in by $\overline{WEL}$ and/or $\overline{WEU}$ with data setup and hold times for DQ0–DQ15 referenced to whichever $\overline{WEx}$ falls earlier (Figure 2).

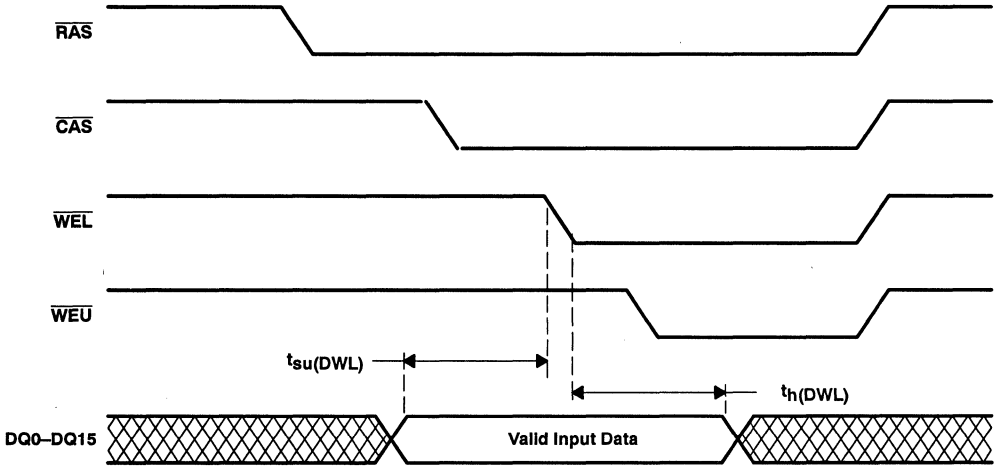


Figure 2. Example of a Late Write

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycles. The write-per-bit operation is invoked when either or both $\overline{WEL}$ and $\overline{WEU}$ are held low on the falling edge of $\overline{RAS}$. Either individual $\overline{WEx}$ will allow entry of the entire 16-bit mask on DQ0–DQ15. Byte control of the mask input is not allowed.

If both $\overline{WEL}$ and $\overline{WEU}$ are held high on the falling edge of $\overline{RAS}$, the write operation will be performed without any masking. The TMS55165 offers two write-per-bit modes: the non-persistent write-per-bit and the persistent write-per-bit.

non-persistent write-per-bit

When either or both $\overline{WEL}$ and $\overline{WEU}$ are low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the sixteen random I/Os are written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. $\overline{WEL}$ enables the lower byte (DQ0–DQ7) to be written, and $\overline{WEU}$ enables the upper byte (DQ8–DQ15) to be written per the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O (Figure 3).

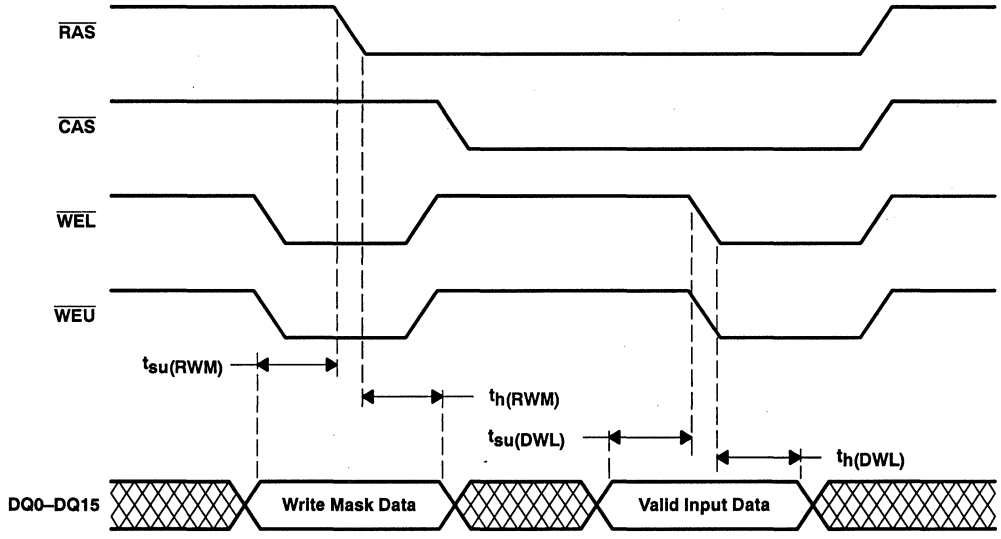
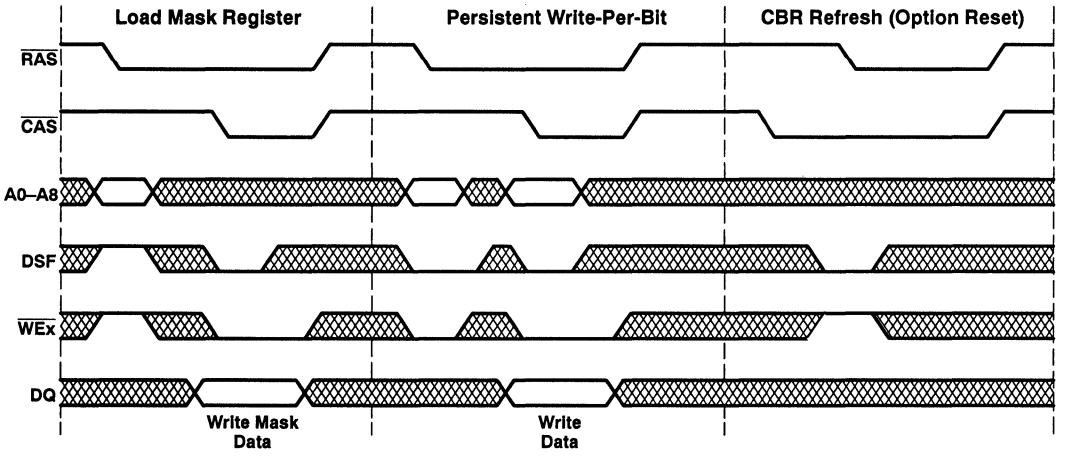


Figure 3. Example of Non-Persistent Write-Per-Bit (Late Write)

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load mask register cycle first. In the persistent write-per-bit mode, the write-per-bit mask will not be overwritten but will remain valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load write mask register cycle is performed using DRAM write cycle timing, except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the falling edge of $\overline{CAS}$. A binary code is input to the write mask register via the random I/O pins and latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. Byte write control can be applied to the write mask during load the write mask register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the non-persistent write-per-bit mode, except the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it will remain in this mode and will be reset only by a $\overline{CAS}$-before-$\overline{RAS}$ refresh with option reset cycle (Figure 4). A hidden refresh cycle will also end the persistent write-per-bit mode, regardless of the state of DSF.



Mask Data = 1 : Write to I/O Enabled
= 0 : Write to I/O Disabled

Figure 4. Example of Persistent Write-Per-Bit

block write

The block write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants may have up to 4 consecutive columns written at a time with up to 4 DQs per column (see Figure 5).

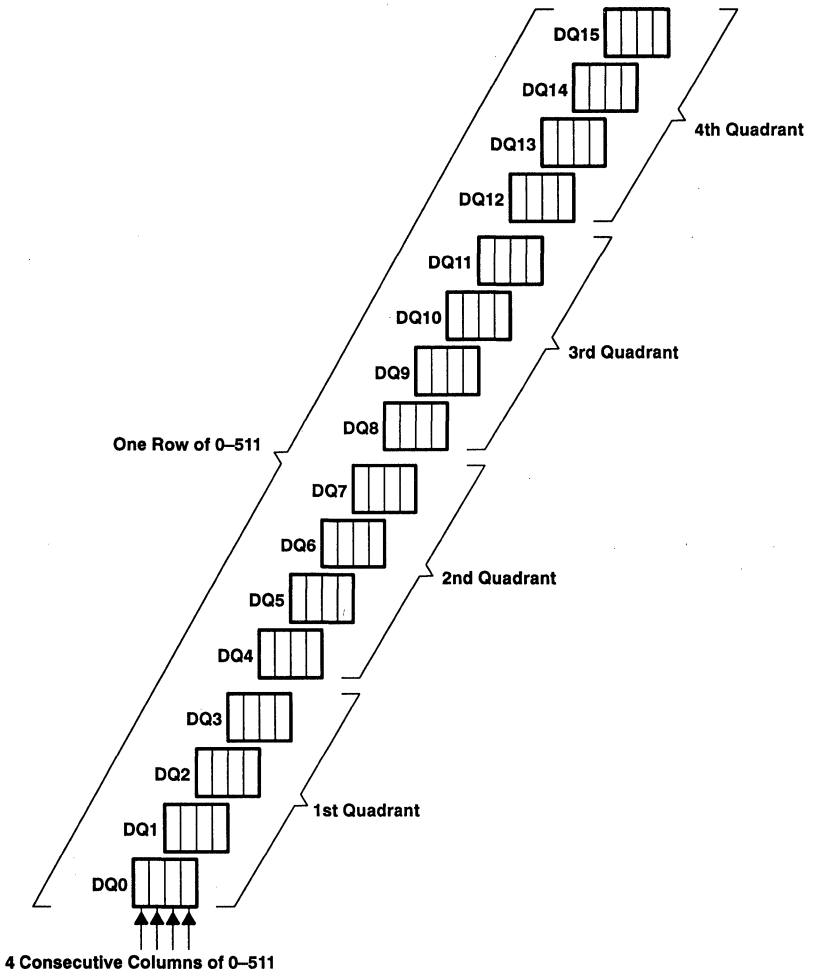


Figure 5. Block Write

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Non-persistent write-per-bit or persistent write-per-bit functions can be applied to the block write operation to provide write masking options. The DQ data is provided by 4 bits from the on-chip color register. Bits 0–3 from the 16-bit write mask, bits 0–3 from the 16-bit column mask and bits 0–3 from the 16-bit color data register configure the block write for the 1st quadrant, while bits 4–7, 8–11, 12–15, control the other quadrants in a similar fashion.

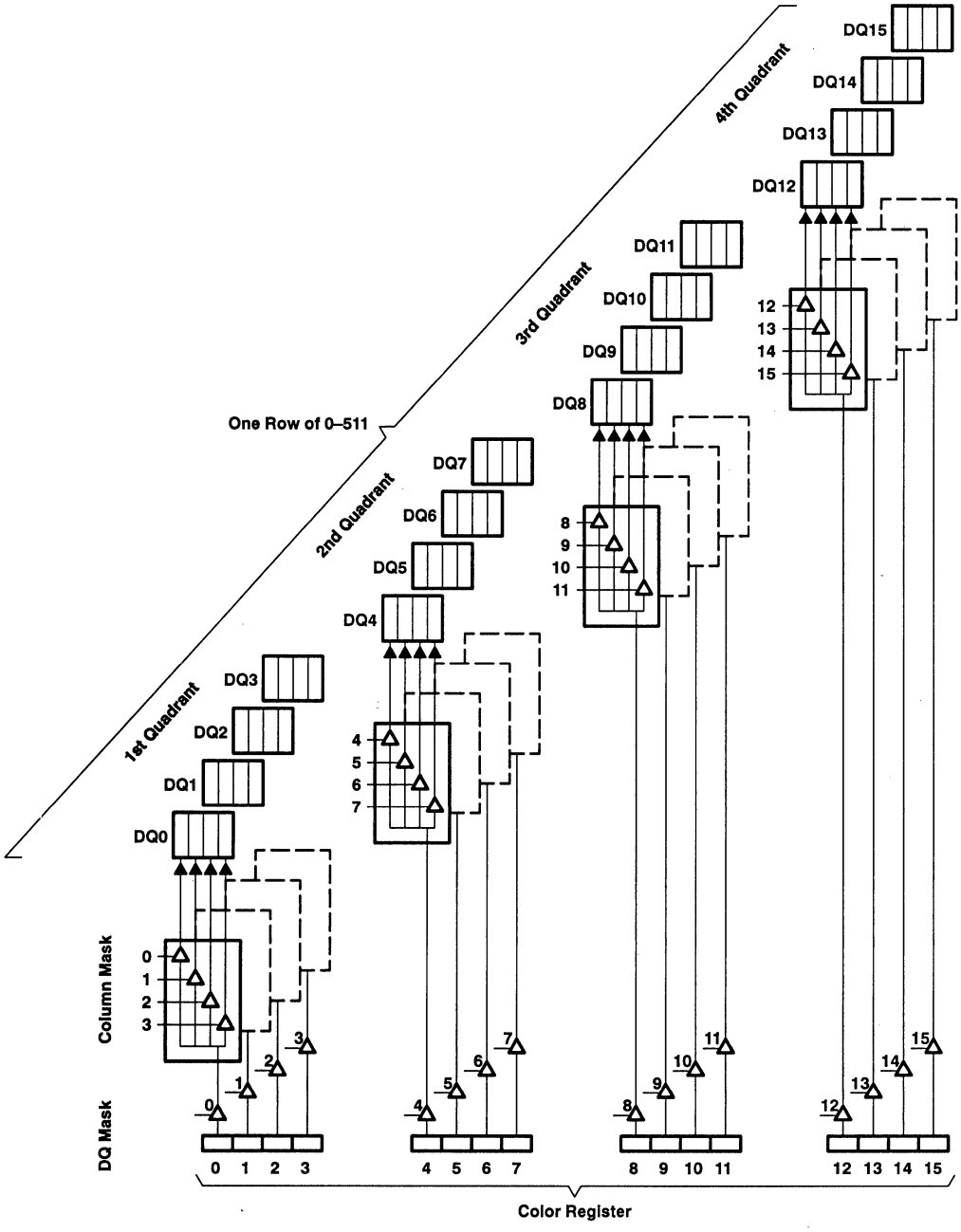


Figure 6. Block Write With Masks

Every 4 columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as below (Figure 7).

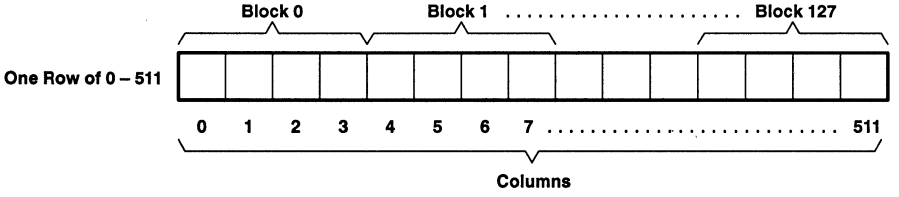


Figure 7. Block Organization

During block write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$ to decode one of the 128 blocks. Address bits A0–A1 are ignored. (Each one-megabit quadrant has the same block selected.)

A block write cycle is entered in a manner similar to a DRAM write cycle except with DSF held high on the falling edge of $\overline{CAS}$. As in a DRAM write operation, $\overline{WEL}$ and $\overline{WEU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column mask data is input via the DQs and is latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. The 16-bit color data register must be loaded prior to performing a block write, as described below. Refer to the write-per-bit section for details on use of the write mask capability, allowing additional performance options.

Example of block write:

block write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color data register =	1011	1011	1100	0111
write mask =	1110	1111	1111	1011
column mask =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color data register (101) to all four columns of Block 0. DQ3 is not written and retains its previous data due to the write mask register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color data register (1100) to columns 1–3 of its Block 0. Column 0 is not written and retains its previous data on all four DQs due to the column mask register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color data register to column 0 and column 2 of its Block 0. DQ13 retains its previous data on all columns, due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the following data pattern after the block write operation shown in the previous example.

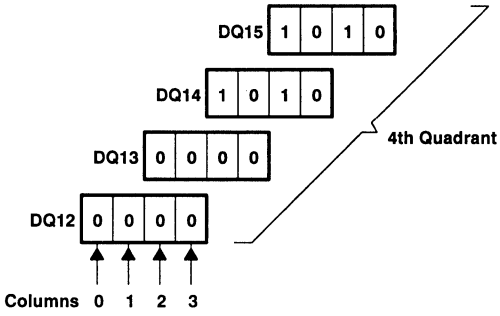
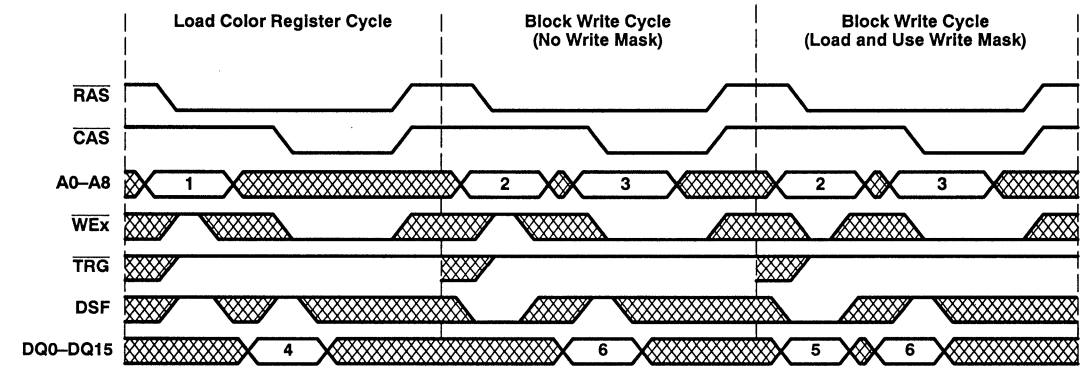


Figure 8. Example of Fourth Quandrant after Bock Write

load color register

The load color register cycle is performed using normal DRAM write cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later. If only one of the write enables is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load color register cycle is performed. (Figure 9, Figure 10).

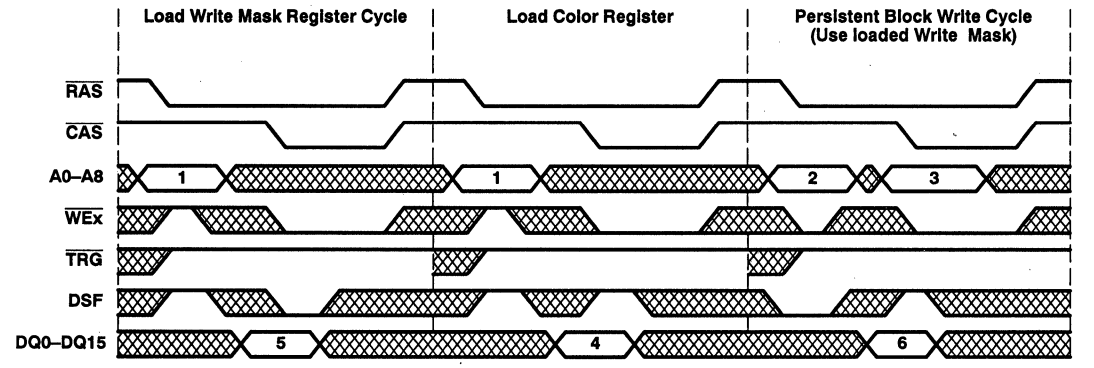


Legend:

2. Refresh Address
2. Row Address
2. Block Address (A2–A8)
2. Color Register Data
2. DQ Mask Data: DQ0–DQ15 are latched on $\overline{RAS}$ falling edge.
2. Column Mask Data: DQ_i–DQ_{i+3} (i=0,4,8,12) are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

= Don't Care

Figure 9. Example of Block Writes With Write Masks



Legend:

1. Refresh Address
2. Row Address
3. Block Address (A2–A8)
4. Color Register Data
5. Write mask data: DQ0–DQ15 are latched on $\overline{CAS}$ falling edge.
6. Column mask data: DQ_i–DQ_{i+3} (i=0,4,8,12) are latched on either the first $\overline{CASx}$ falling edge or the falling edge of $\overline{WE}$, whichever occurs later

= Don't Care

Figure 10. Example of a Persistent Block Write

DRAM to SAM transfer operation

During the DRAM to SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WEL}$ and $\overline{WEU}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the read transfer operation or the split register read transfer operation will be performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WEx}$‡	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$ $\overline{WEL}$ $\overline{WEU}$	
Read transfer	1	0	1	0	X	Row Addr	Tap Point	X	X	RT
Split-register read transfer	1	0	1	1	X	Row Addr	Tap Point	X	X	SRT

† DQ0–DQ15 are latched on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.
‡ Logic 0 is selected when either or both $\overline{WEL}$ and $\overline{WEU}$ are low.
X: = Don't care.

read transfer

A read transfer operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column address bits (A0–A8) are latched at the falling edge of $\overline{CAS}$, where address bit A8 selects which half of the row will be transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data will be read out (Figure 11).

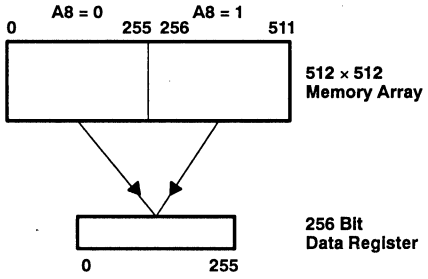


Figure 11. Read Transfer

A read transfer can be performed in three ways: early-load read transfer, real-time or mid-line-load read transfer, and late-load read transfer. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the read transfer cycle (Figure 12).

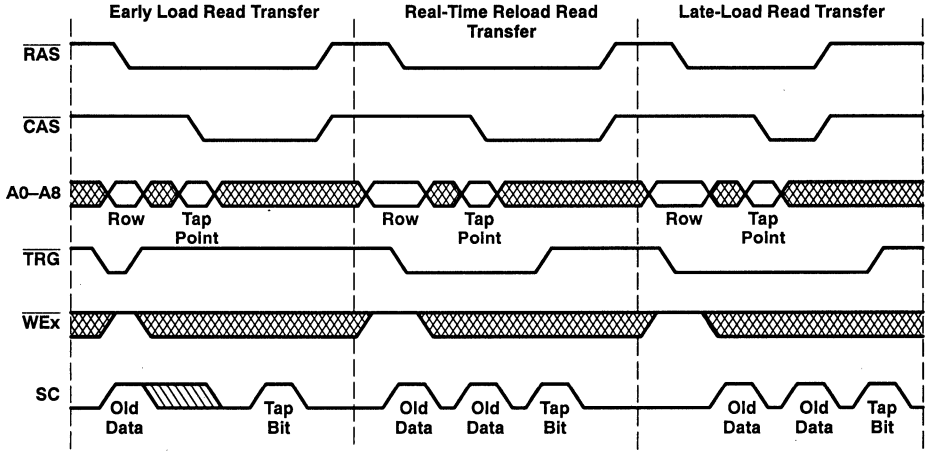


Figure 12. Examples of Read Transfer

split-register read transfer

In the split-register read transfer operation, the serial data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

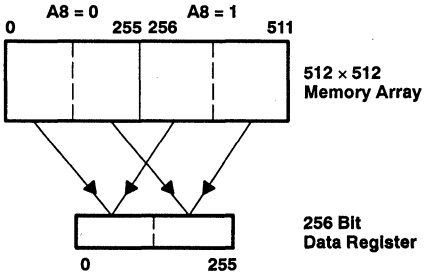
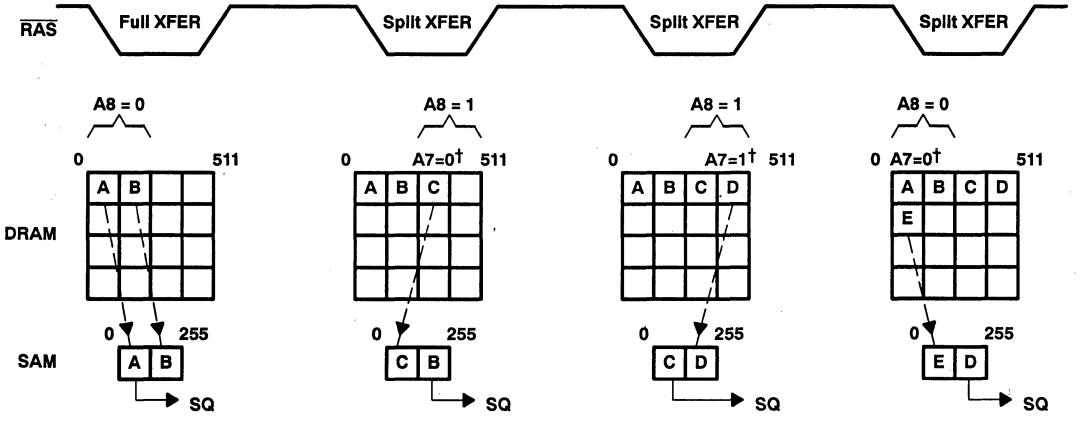


Figure 13. Split Register Read Transfer

To invoke a split-register read transfer cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column address bits (A0–A6 and A8) are latched at the falling edge of $\overline{CAS}$. Column address bit A8 selects which half of the row to be transferred. Column address bits A0–A6 will select one of the 127 tap points in the specified half of the SAM. Column address bit A7 is ignored and the split-register transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled

Figure 14. Example of Split-Register Read Transfer Operation

A read transfer (non split-register) must precede the first split-register read transfer to ensure proper operation. After the read transfer cycle, the first split-register read transfer can follow immediately without any minimum SC clock requirement. However, there is a minimum requirement of a rising edge of SC between successive split-register read transfer cycles.

QSF indicates which half of the register is being accessed during serial access operation. When QSF is low, the serial address pointer is accessing the lower (least significant) 128 bits of SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of SAM. QSF changes state upon completing a read transfer cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

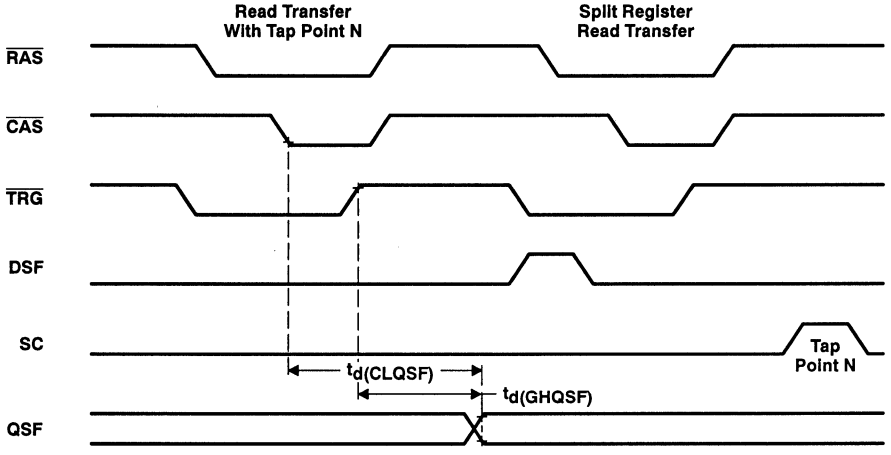


Figure 15. Example of a Split-Register Read Transfer After a Read Transfer

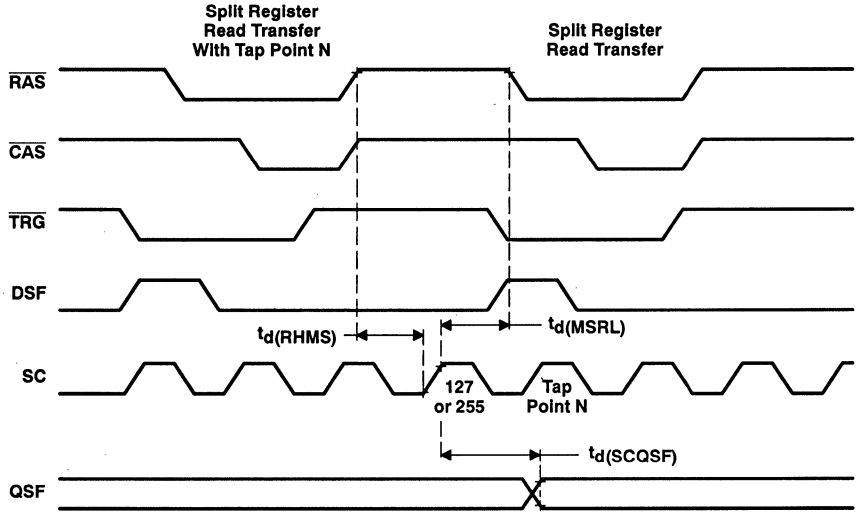


Figure 16. Example of Successive Split-Register Read Transfers

serial access operation

The serial read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during read transfer operations.

Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, then proceeding sequentially to the most significant bit (bit 255) and then wrapping around to the least significant bit (bit 0) (Figure 17).

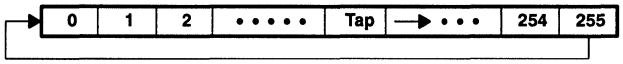


Figure 17. Serial Pointer Direction for Serial Read

For split-register operation, serial data can be read out from the active half of SAM by clocking SC starting at the tap point loaded by the preceding split-register transfer cycle. The serial pointer will then proceed sequentially to the most significant bit of the half, bit 127 or bit 255. If there is a split-register read transfer to the inactive half during this period, the serial pointer will point next to the tap point location loaded by that split register transfer (Figure 18).

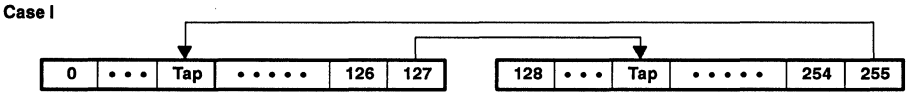


Figure 18. Serial Pointer for Split-Register Read – Case I

If there is no split-register read transfer to the inactive half during this period, the serial pointer will point next to bit 128 or bit 0 respectively (Figure 19).

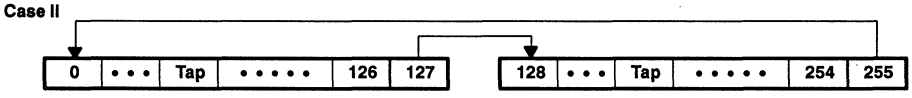


Figure 19. Serial Pointer for Split-Register Read – Case II

power up

To achieve proper device operation, an initial pause of 200 μs is required after power-up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles to initialize the DRAM port. A read transfer cycle and two SC cycles are required to initialize the SAM port.

After initialization, the internal state of the TMS55165 is as follows:

	State After Initialization
QSF	Defined by the transfer cycle during initialization
Write mode	Non-persistent mode
Write mask register	Undefined
Color register	Undefined
Serial register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature†

Supply voltage range on any pin except DQ and SQ (see Note 1) ..... –1 V to 7 V
Voltage range on DQ and SQ (see Note 1) ..... –1 V to 7 V
Voltage range on V_{CC} (see Note 1) ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SAM PORT	TMS55165-70		TMS55165-80		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 5.8 V, V_{CC} = 5.5 V All other pins at 0 to V_{CC}			±10		±10	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V			±10		±10	µA
I_{CC1}	Operating current	See Note 4	Standby		165		160	mA
I_{CC1A}	Operating current	$t_{c(SC)}$ = MIN	Active		205		195	
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5	
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		50		45	
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		165		160	
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN	Active		195		185	
I_{CC4}	Page-mode current	$t_{c(P)}$ = MIN (see Note 5)	Standby		100		95	
I_{CC4A}	Page-mode current	$t_{c(SC)}$ = MIN	Active		130		120	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current	See Note 4	Standby		165		160	
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(SC)}$ = MIN	Active		205		195	
I_{CC6}	Data transfer current	See Note 4	Standby		165		160	
I_{CC6A}	Data transfer current	$t_{c(SC)}$ = MIN	Active		205		195	

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}; $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS55165-70		TMS55165-80		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ (see Note 7)	$t_{d(RLCL)}$ = Max	t_{CAC}		20		20	ns
$t_{a(CA)}$	Access time from column address (see Note 7)	$t_{d(RLCL)}$ = Max	t_{AA}		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high (see Note 7)	$t_{d(RLCL)}$ = Max	t_{CPA}		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ (see Note 7)	$t_{d(RLCL)}$ = Max	t_{RAC}		70		80	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low (see Note 7)		t_{OEA}		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high (see Note 7)	C_L = 30 pF	t_{SCA}		20		25	ns
$t_{a(SE)}$	Access time of SQ or QSF from $\overline{SE}$ low (see Note 7)	C_L = 30 pF	t_{SEA}		15		20	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output or QSF disable time from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	15	0	20	ns

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

			TMS55165-70		TMS55165-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	130		150		ns
$t_{c(W)}$	Write cycle time	t_{WC}	130		150		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RMW}	170		195		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	45		50		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRMW}	85		90		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	130		150		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 9)	t_{SCC}	22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CPN}	10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 10)	t_{CAS}	20	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WEx}$ low	t_{WP}	10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CAS}$ low	t_{FSC}	0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WEx}$ before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		ns
$t_{su(SE)}$	Setup time, $\overline{SE}$ high before $\overline{RAS}$ low	t_{SER}	0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		ns
$t_{su(DCL)}$	Setup time, data before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Setup time, data before $\overline{WEx}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Setup time, read command $\overline{WEx}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WEx}$ low before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write setup time, $\overline{WEx}$ low before $\overline{CAS}$ high	t_{CWL}	15		20		ns
$t_{su(WRH)}$	Write setup time, $\overline{WEx}$ low before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{WEx}$ = low	t_{RWL}	15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CAS}$ low	t_{CFH}	10		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS55165-70		TMS55165-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		ns
$t_{h(TRG)}$	Hold time, TRG after $\overline{RAS}$ low	t_{THH}	10		15		ns
$t_{h(RWM)}$	Hold time, write mask, transfer enable after $\overline{RAS}$ low	t_{RWH}	10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write mask operation)	t_{MH}	10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low	t_{RFH}	10		10		ns
$t_{h(RLCA)}$	Hold time, column-address after $\overline{RAS}$ low (see Note 12)	t_{AR}	30		35		ns
$t_{h(CLD)}$	Hold time, data after $\overline{CAS}$ low	t_{DH}	15		15		ns
$t_{h(RLD)}$	hold time, data after $\overline{RAS}$ low (see Note 12)	t_{DHR}	35		35		ns
$t_{h(WLD)}$	Hold time, data after $\overline{WEx}$ low	t_{DH}	15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WEx}$ low after $\overline{CAS}$ high (see Note 13)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WEx}$ high after $\overline{RAS}$ high (see Note 13)	t_{RRH}	0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{CAS}$ low	t_{WCH}	15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WEx}$ low after $\overline{RAS}$ low (see Note 12)	t_{WCR}	35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WEx}$ low (see Note 14)	t_{OEH}	10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ after SC high	t_{SOH}	5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low	t_{FHR}	30		35		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	70		80		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{WEx}$ low (see Notes 15 and 16)	t_{CWD}	45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 17)	t_{RCD}	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	35		40		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WEx}$ low (see Note 15)	t_{RWD}	95		105		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{WEx}$ low (see Note 15)	t_{AWD}	60		65		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 18)	t_{CHR}	10		15		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 18)	t_{CSR}	0		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 18)	t_{RPC}	0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high for DRAM read cycles		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ	t_{OED}	15		15		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (real-time reload read transfer cycle only)	t_{RTH}	55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 19)	t_{RSD}	70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 17)	t_{RAD}	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. Read-modify-write operation only.
16. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
17. The maximum value is specified only to assure $\overline{RAS}$ access time.
18. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
19. Early-load read transfer cycle only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	TMS55165-70		TMS55165-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 20 and 21)	t_{TSL}	5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Notes 20 and 23)	t_{TRD}	–10		–10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 20)	t_{TSD}	10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	5		5		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early load read transfer cycles	t_{ASD}	25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	10		10		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CAS}$ low	t_{DZC}	0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split read transfer cycles		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split read transfer cycles (see Note 24)	t_{SQD}		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CAS}$ low to QSF switching in transfer read or write cycles (see Note 24)	t_{CQD}		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read or write cycles (see Note 24)	t_{TQD}		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read or write cycles (see Note 24)	t_{RQD}		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 20. Real-time reload read transfer cycle only.
21. Early-load read transfer cycle only.
22. Memory to register (read) transfer cycles only.
23. Late-load read transfer cycle only.
24. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8V.

PARAMETER MEASUREMENT INFORMATION

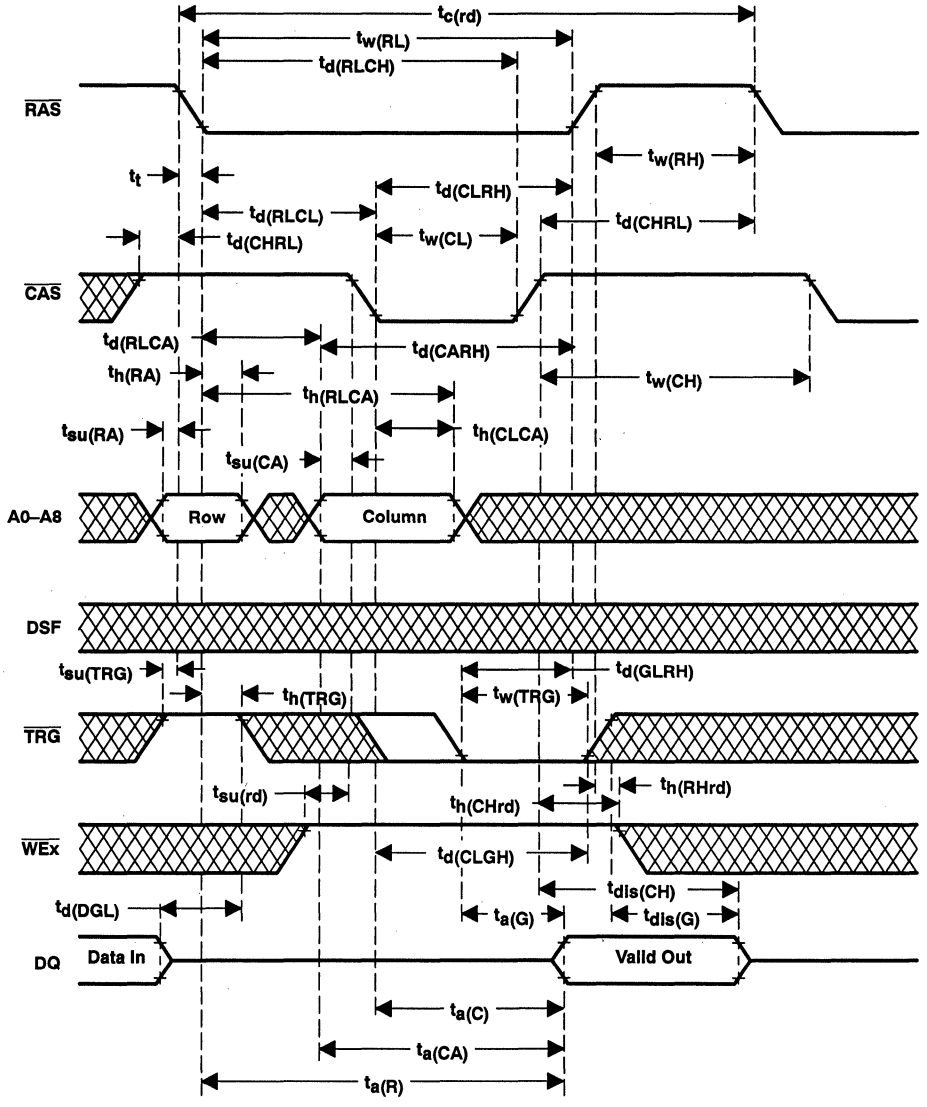


Figure 20. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

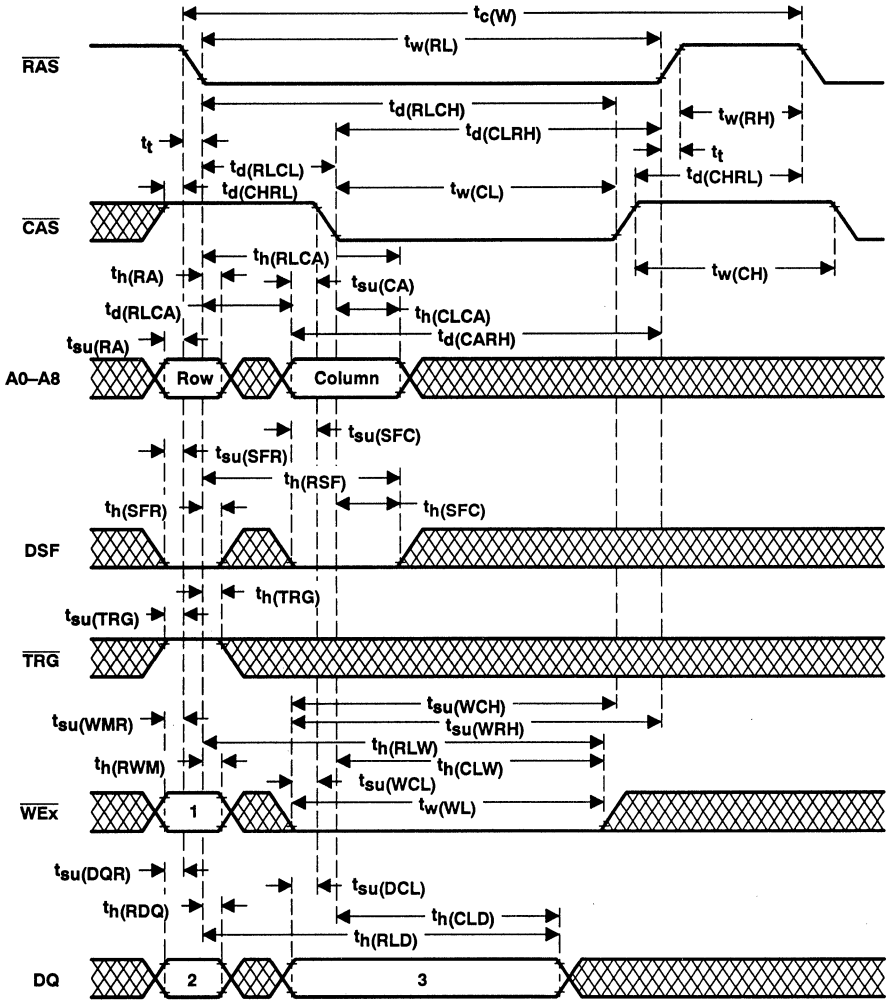


Figure 21. Early Write Cycle Timing

Table 5. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

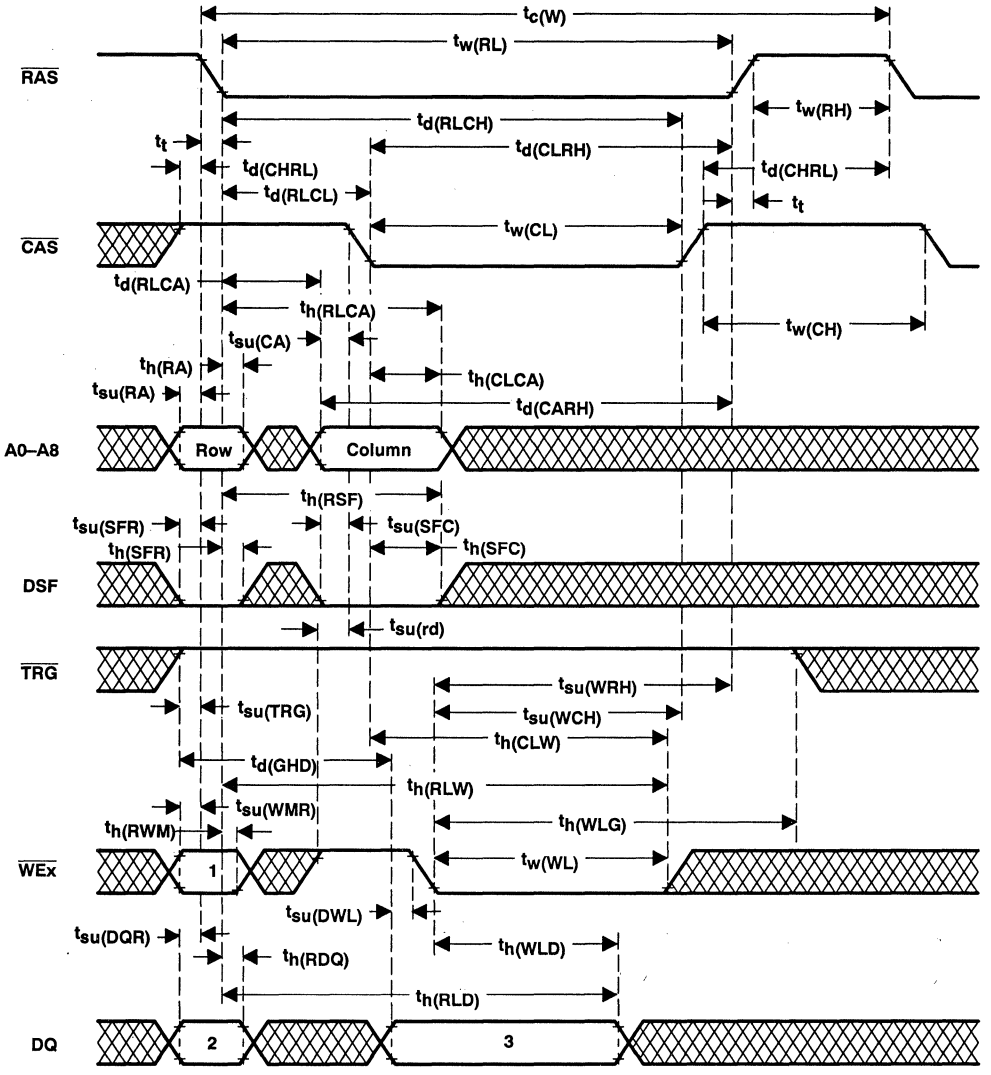
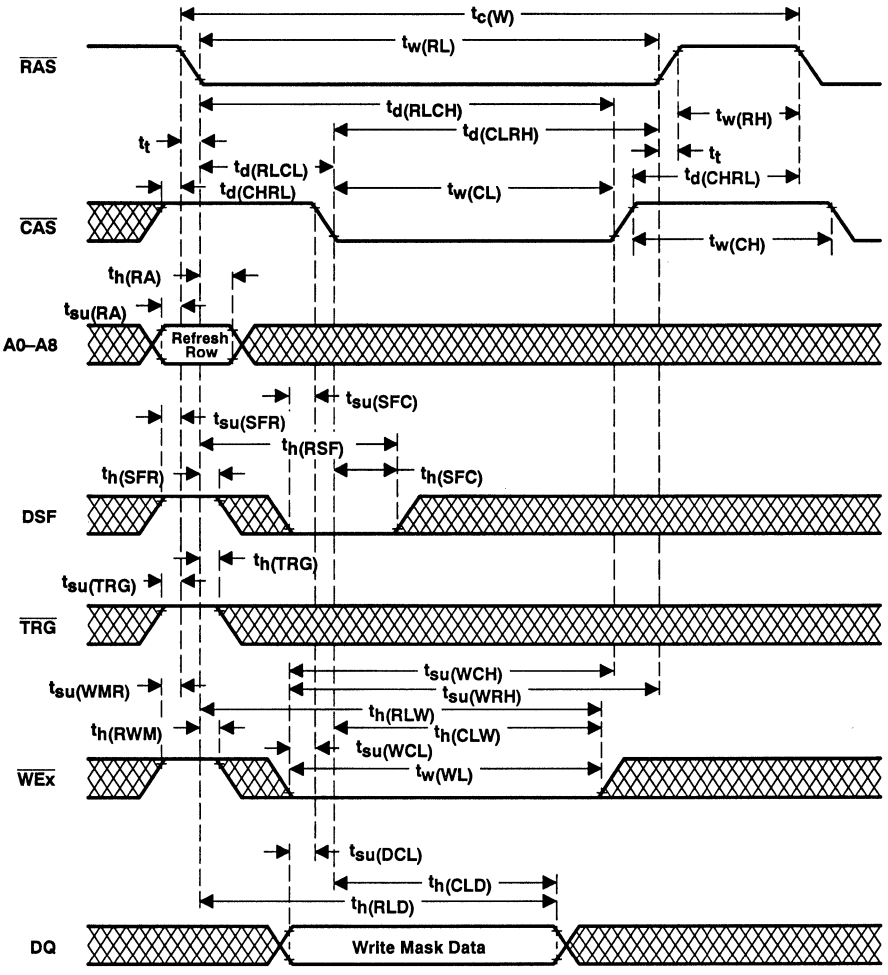


Figure 22. Late Write Cycle Timing (Output-Enable-Controlled Write)

Table 6. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

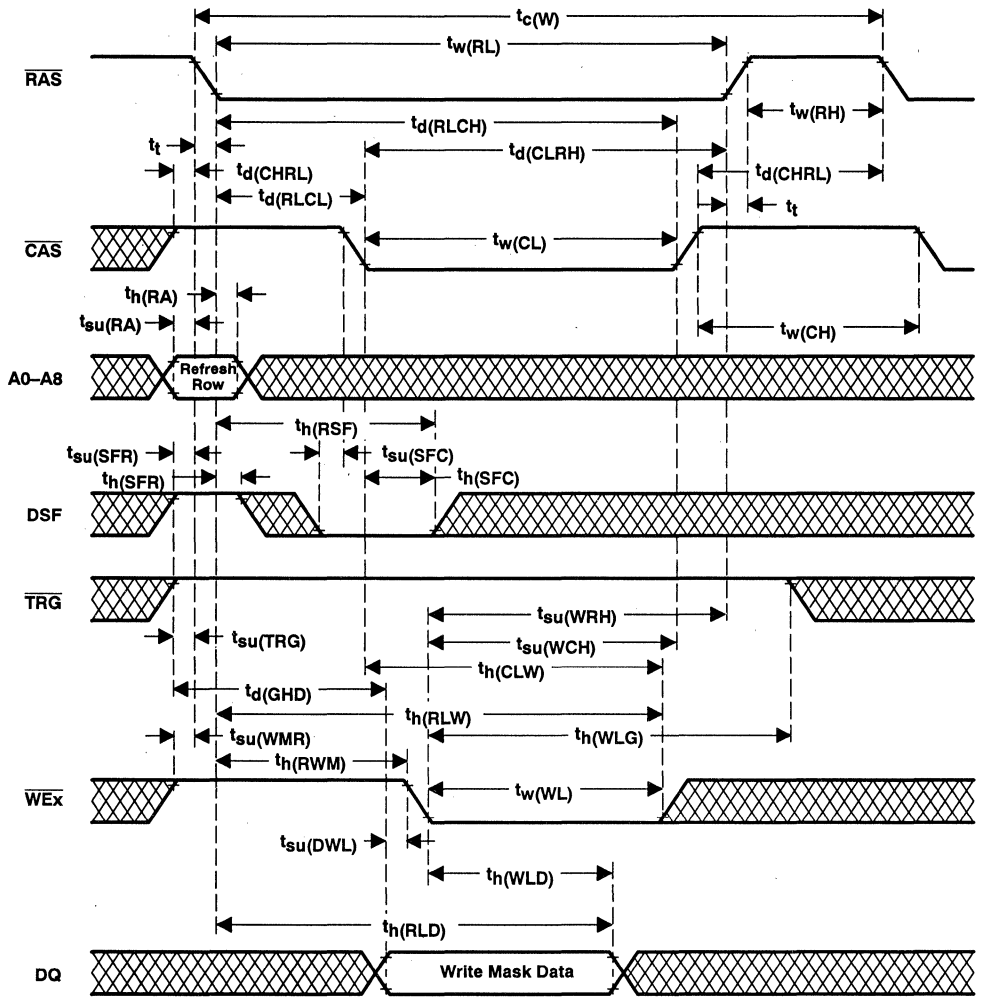
PARAMETER MEASUREMENT INFORMATION



† Load mask register cycle will put the device into the persistent write-per-bit mode.

Figure 23. Load Mask Register Timing (Early Write Load)†

PARAMETER MEASUREMENT INFORMATION



† Load mask register cycle will put the device into the persistent write-per-bit mode.

Figure 24. Load Mask Register Timing (Late Write Load)†

PARAMETER MEASUREMENT INFORMATION

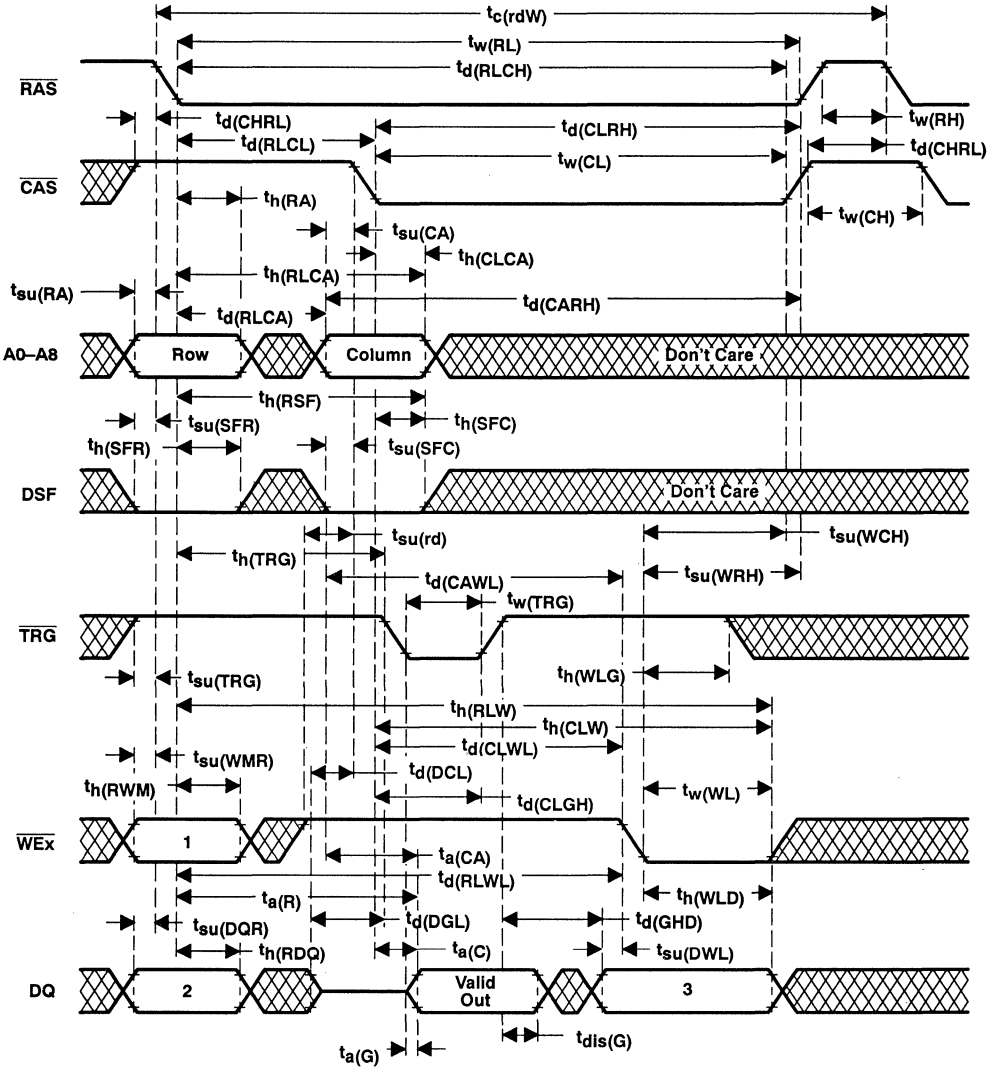
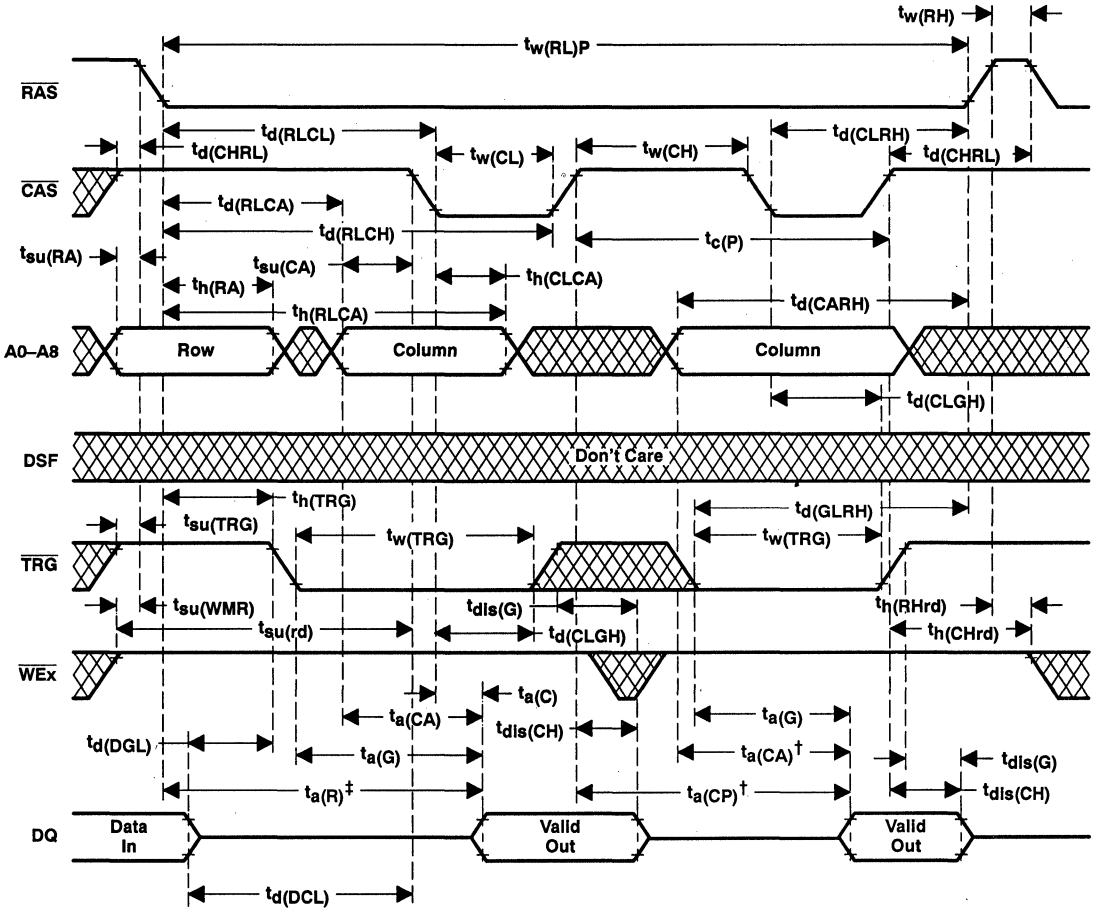


Figure 25. Read-Write/Read-Modify-Write Cycle Timing

Table 7. Write Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (non-masked)	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

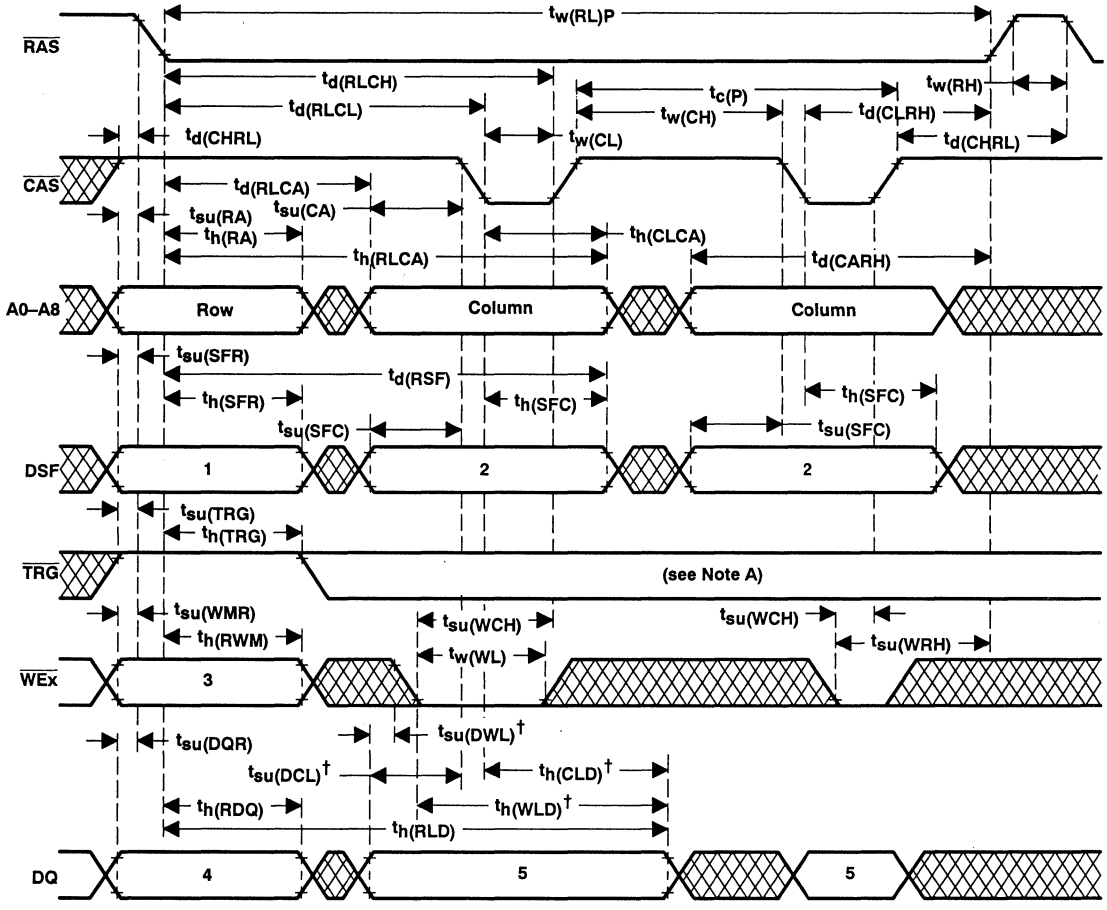
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.)

Figure 26. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write features is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

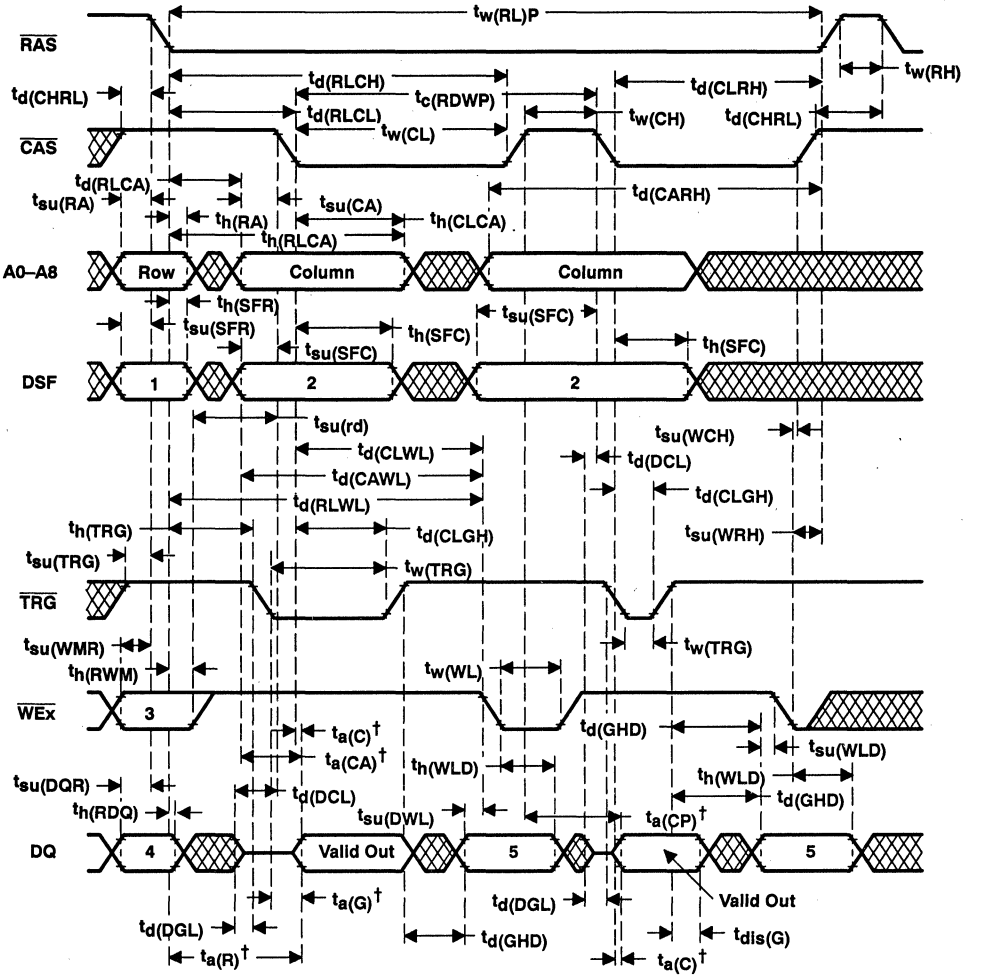
Figure 27. Enhanced Page-Mode Write Cycle Timing

Table 8. Write Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (non-masked)	L	L	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load write mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output may go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 28. Enhanced Page-Mode Read-Modify-Write Cycle Timing

Table 9. Write Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (non-masked)	L	L	H	Don't care	Valid data
Write operation with non-persistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first $\overline{WEx}$ falling edge or the falling edge of $\overline{CAS}$ whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load write mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$ is don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION

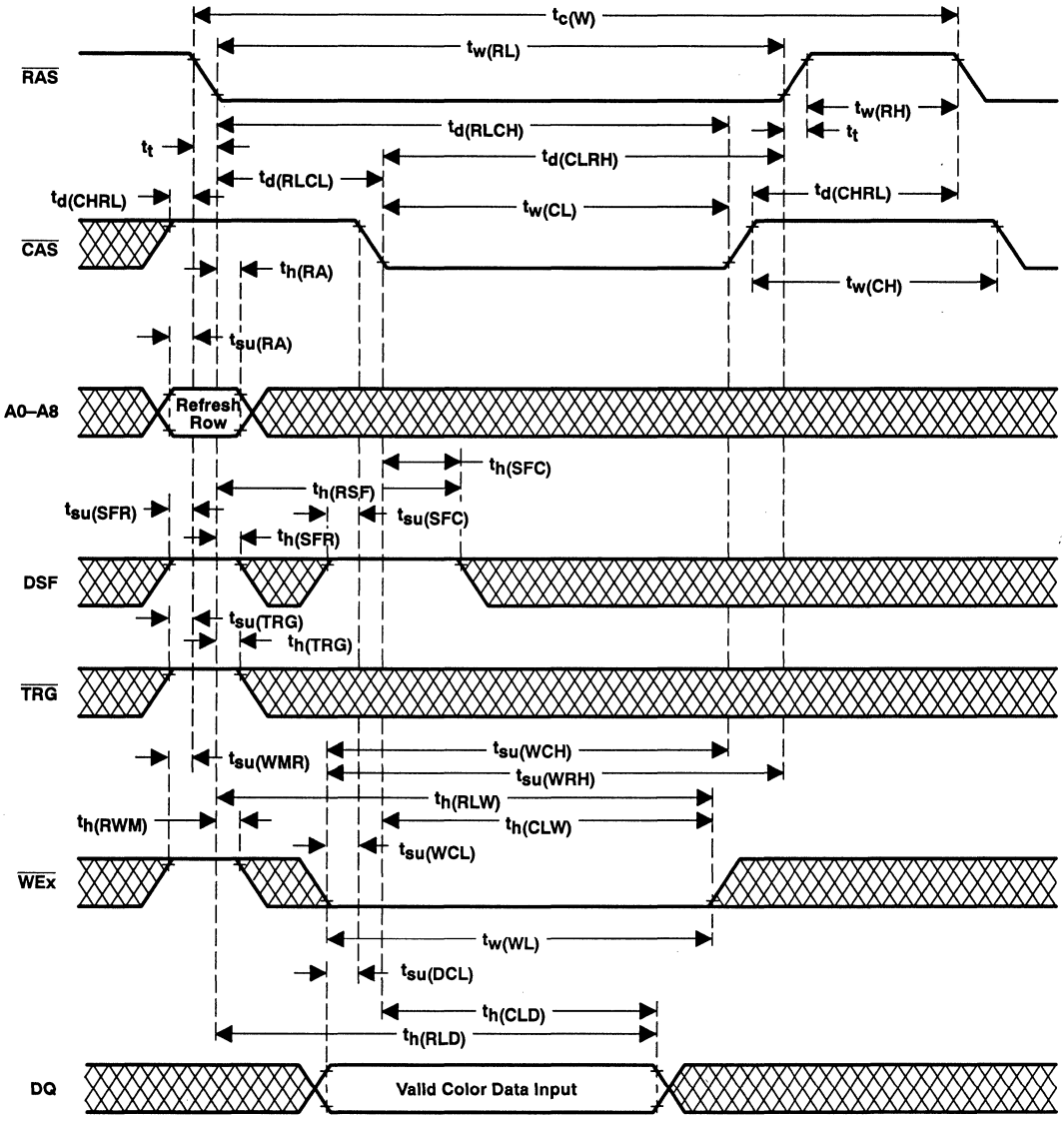


Figure 29. Load Color Register Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

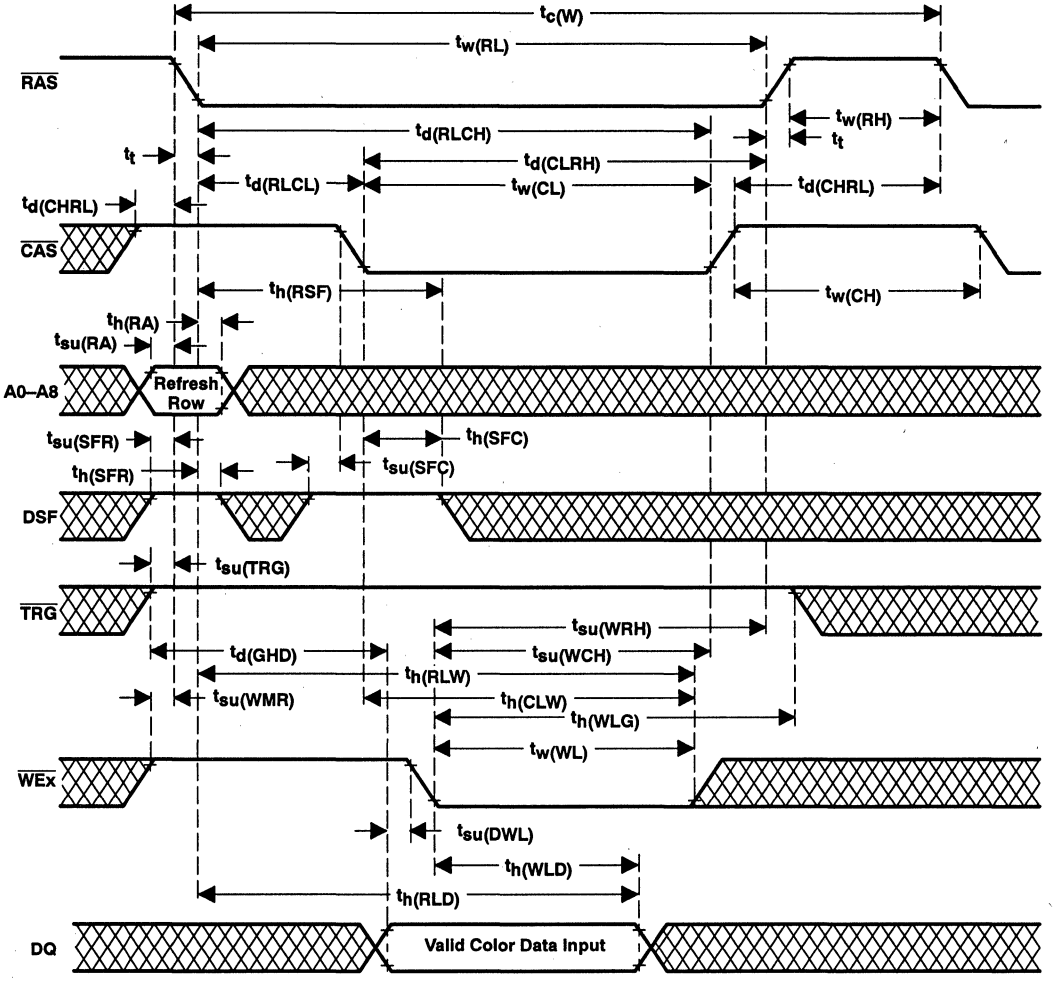


Figure 30. Load Color Register Timing (Late Write Load)

PARAMETER MEASUREMENT INFORMATION

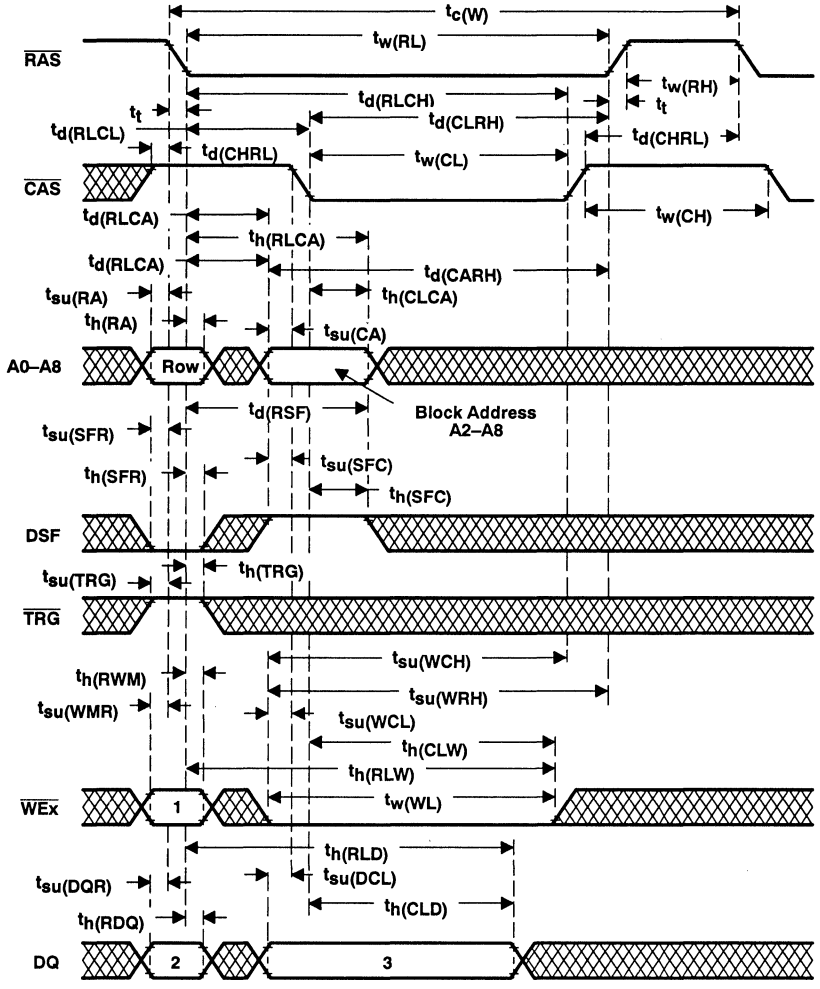


Figure 31. Block Write Timing (Early Write)

Table 10. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION

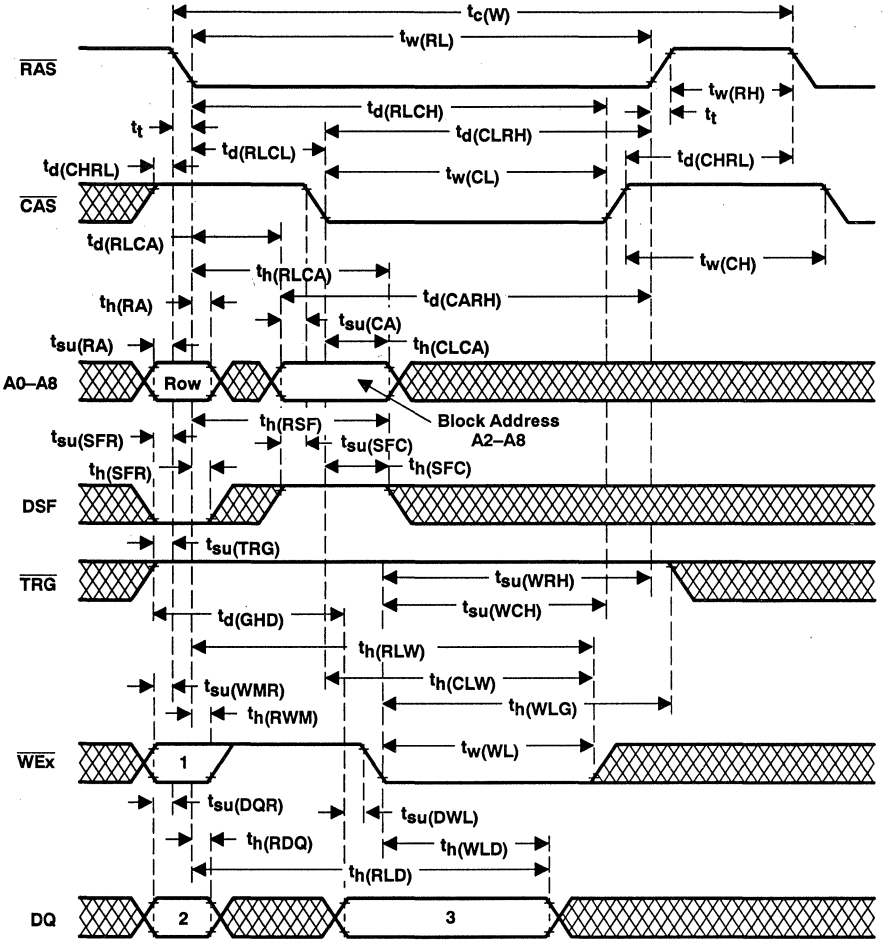


Figure 32. Block Write Timing (Late Write)

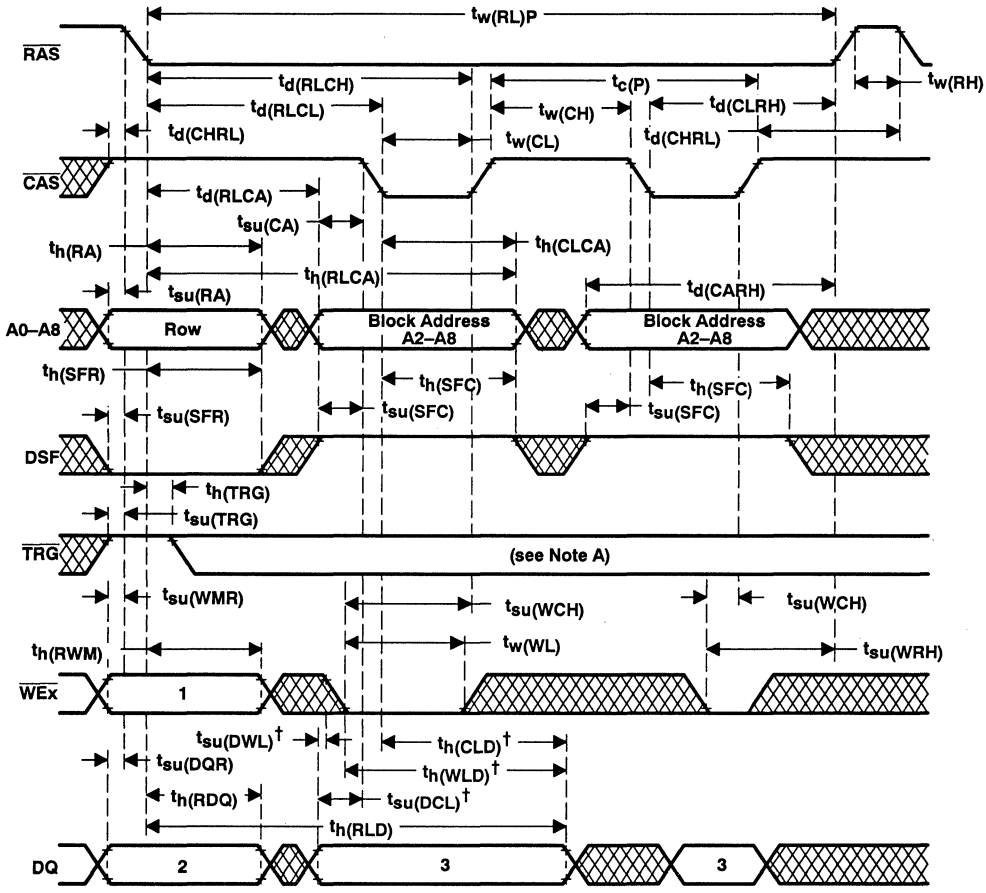
Table 11. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable
Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced the first $\overline{WE}x$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write features is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 33. Enhanced Page-Mode Block Write Cycle Timing

Table 12. Block Write Cycle State Table

CYCLE	STATE		
	1	2	3
Block write operation (non-masked)	H	Don't care	Column mask
Block write operation with non-persistent write-per-bit	L	Write mask	Column mask
Block write operation with persistent write-per-bit	L	Don't care	Column mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQ_i – DQ_{i+3}0: column write disable
(i = 0, 4, 8, 12) 1: column write enable

Example:
DQ_0 — column 0 (address A_1 = 0, A_0 = 0)
DQ_1 — column 1 (address A_1 = 0, A_0 = 1)
DQ_2 — column 2 (address A_1 = 1, A_0 = 0)
DQ_3 — column 3 (address A_1 = 1, A_0 = 1)

PARAMETER MEASUREMENT INFORMATION

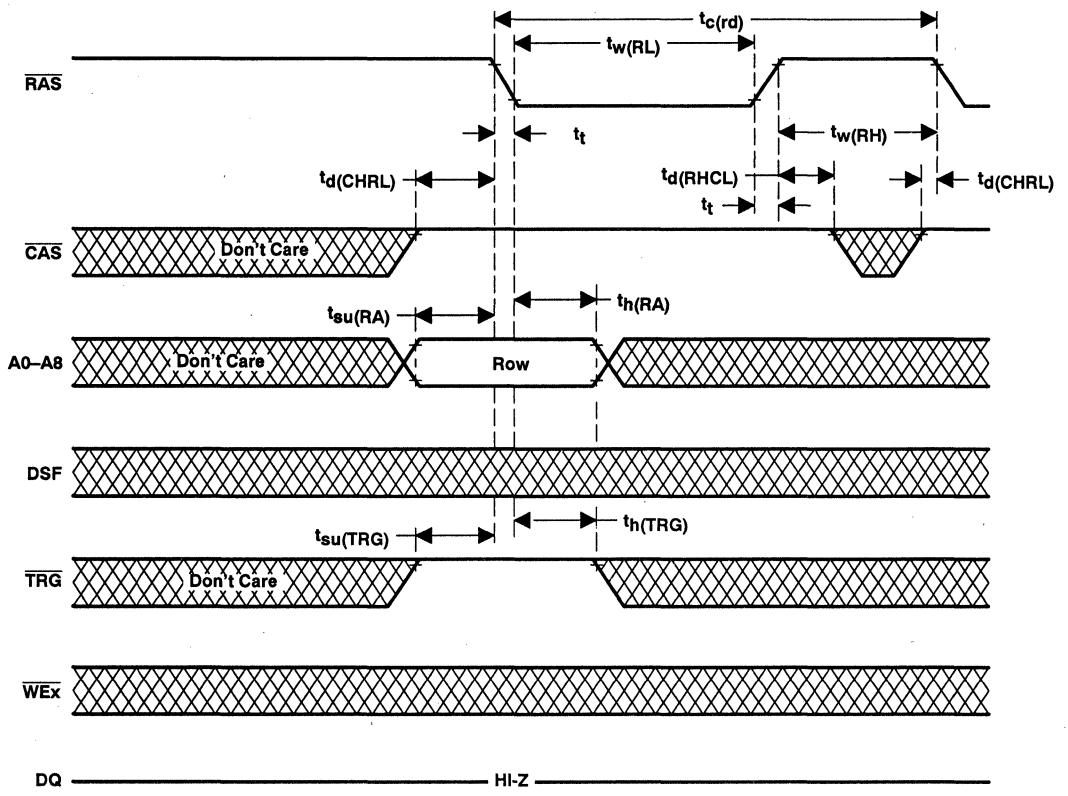


Figure 34. $\overline{\text{RAS}}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

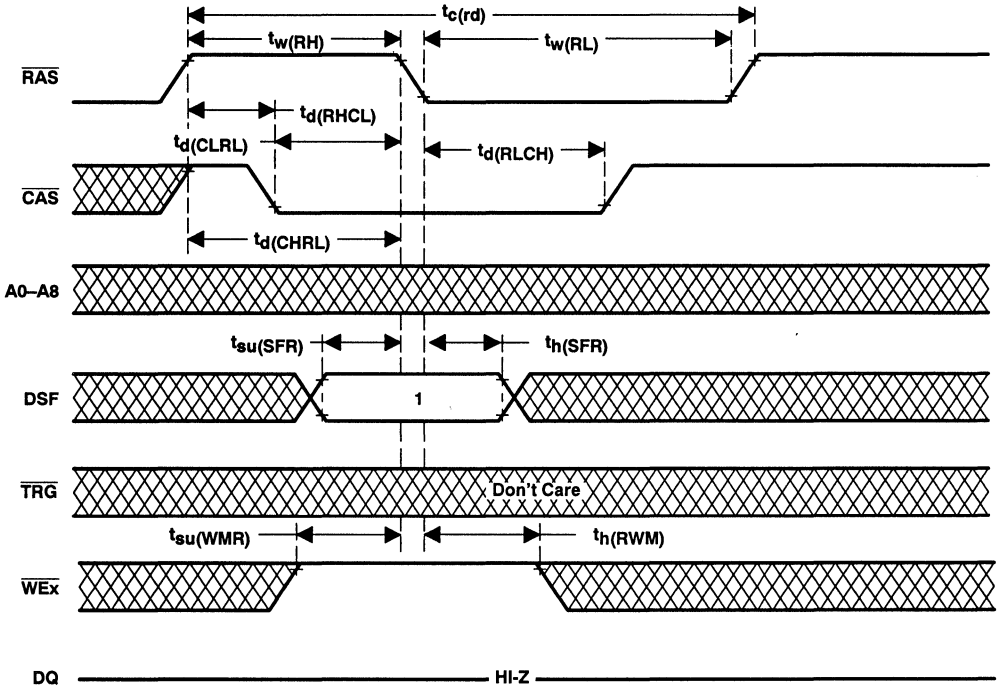


Figure 35. $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

Table 13. CBR Cycle State Table

CYCLE	STATE
	1
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with option reset	0
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with no reset	1

PARAMETER MEASUREMENT INFORMATION

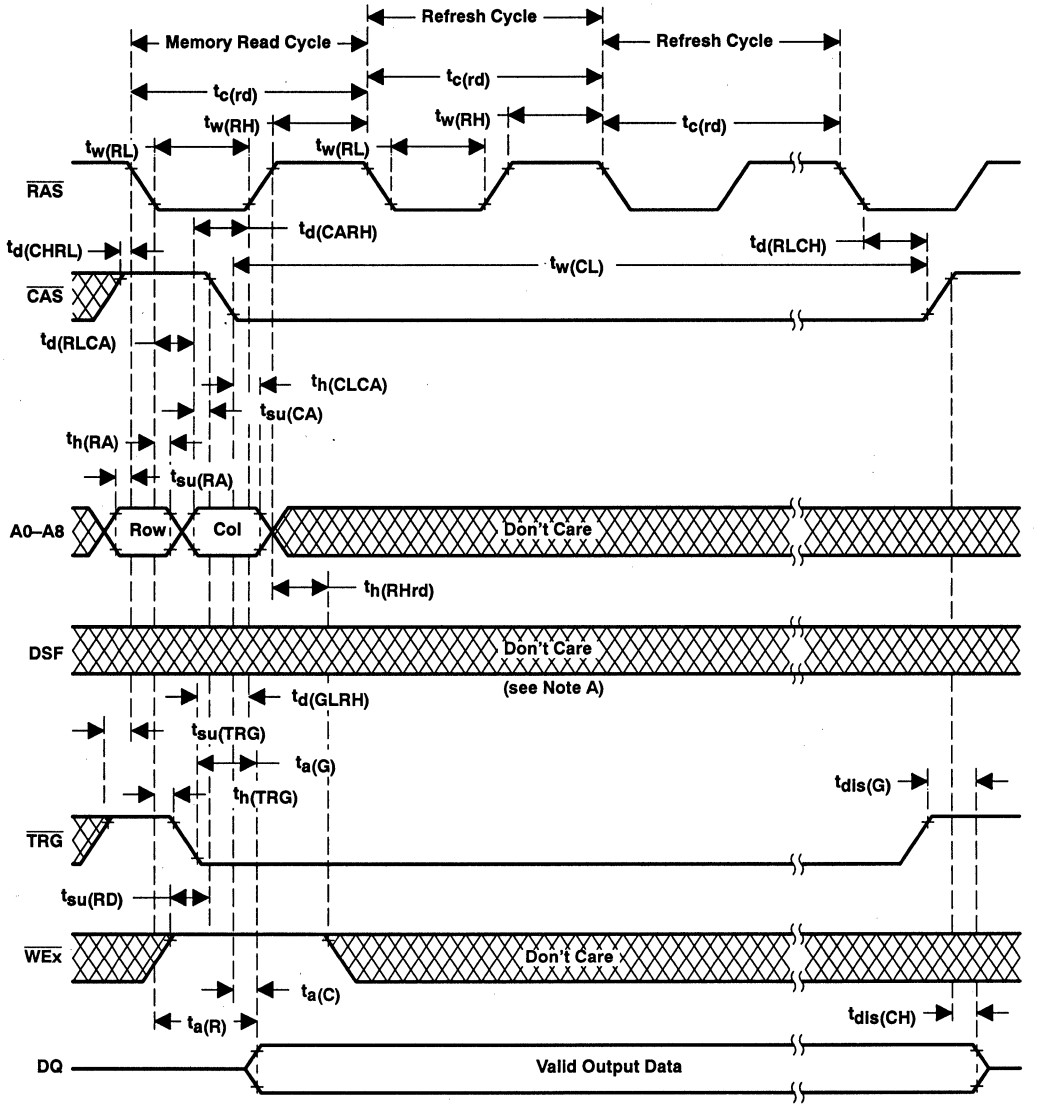
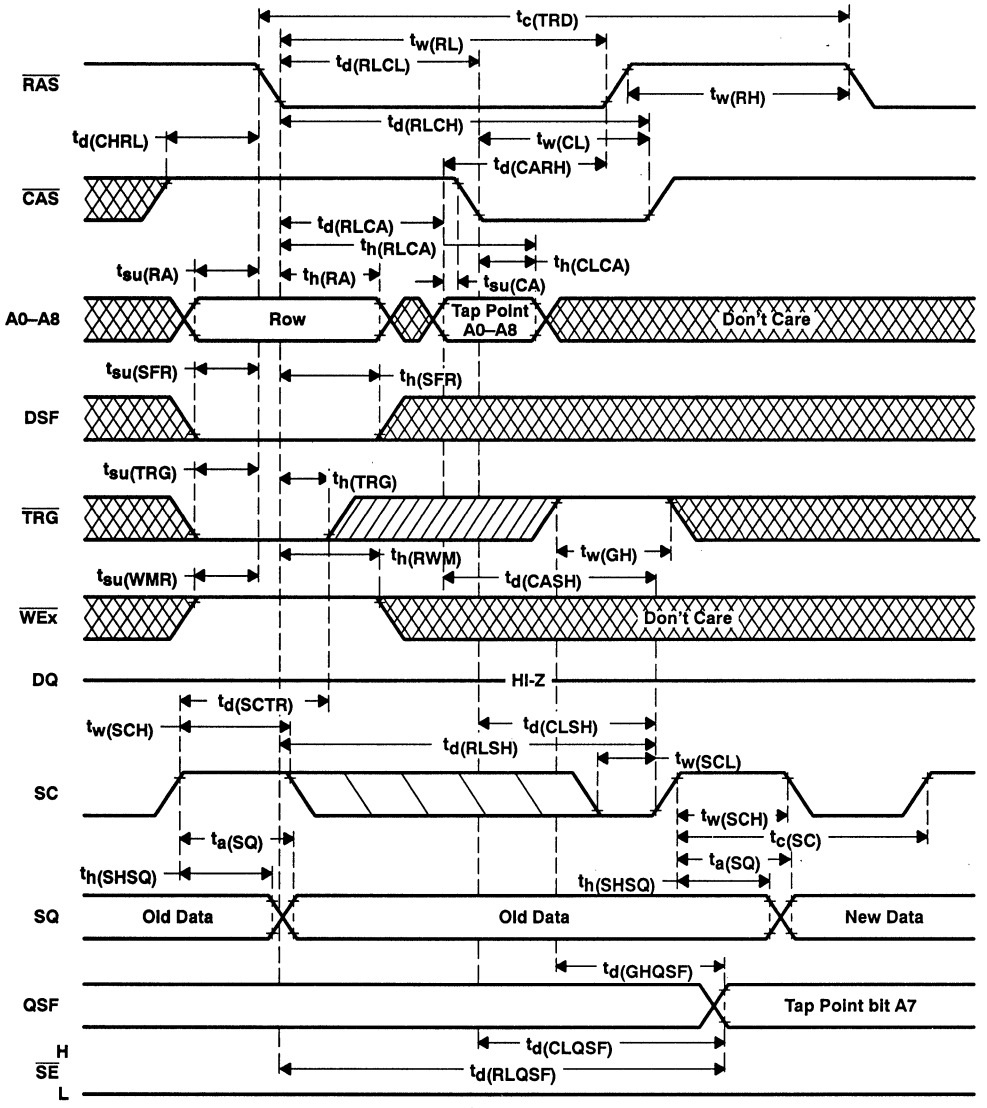


Figure 36. Hidden Refresh Cycle Timing

NOTE A: $\overline{CAS}$-before-$\overline{RAS}$ refresh (option reset) mode will end persistent write-per-bit mode. Hidden refresh will also end the persistent write-per-bit mode regardless of the state of DSF at $\overline{RAS}$.

PARAMETER MEASUREMENT INFORMATION



† Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

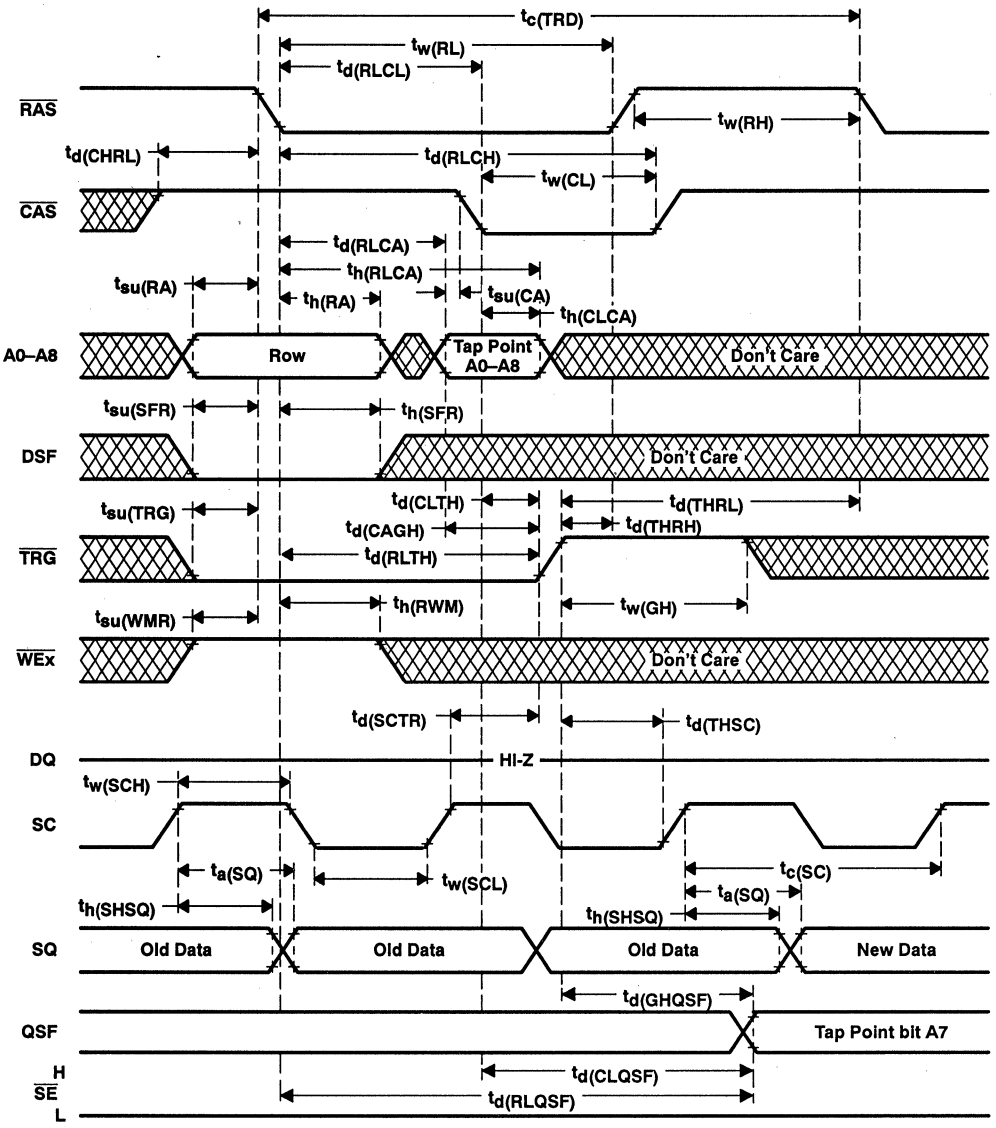
NOTES: A. Random mode (DQ outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: Register tap point, A8: which half of the transferred row.

Figure 37. Read Transfer Timing, Early Load Operation†

PARAMETER MEASUREMENT INFORMATION



† Late load operation is defined as $t_{d(THRH)} < 0$ ns.

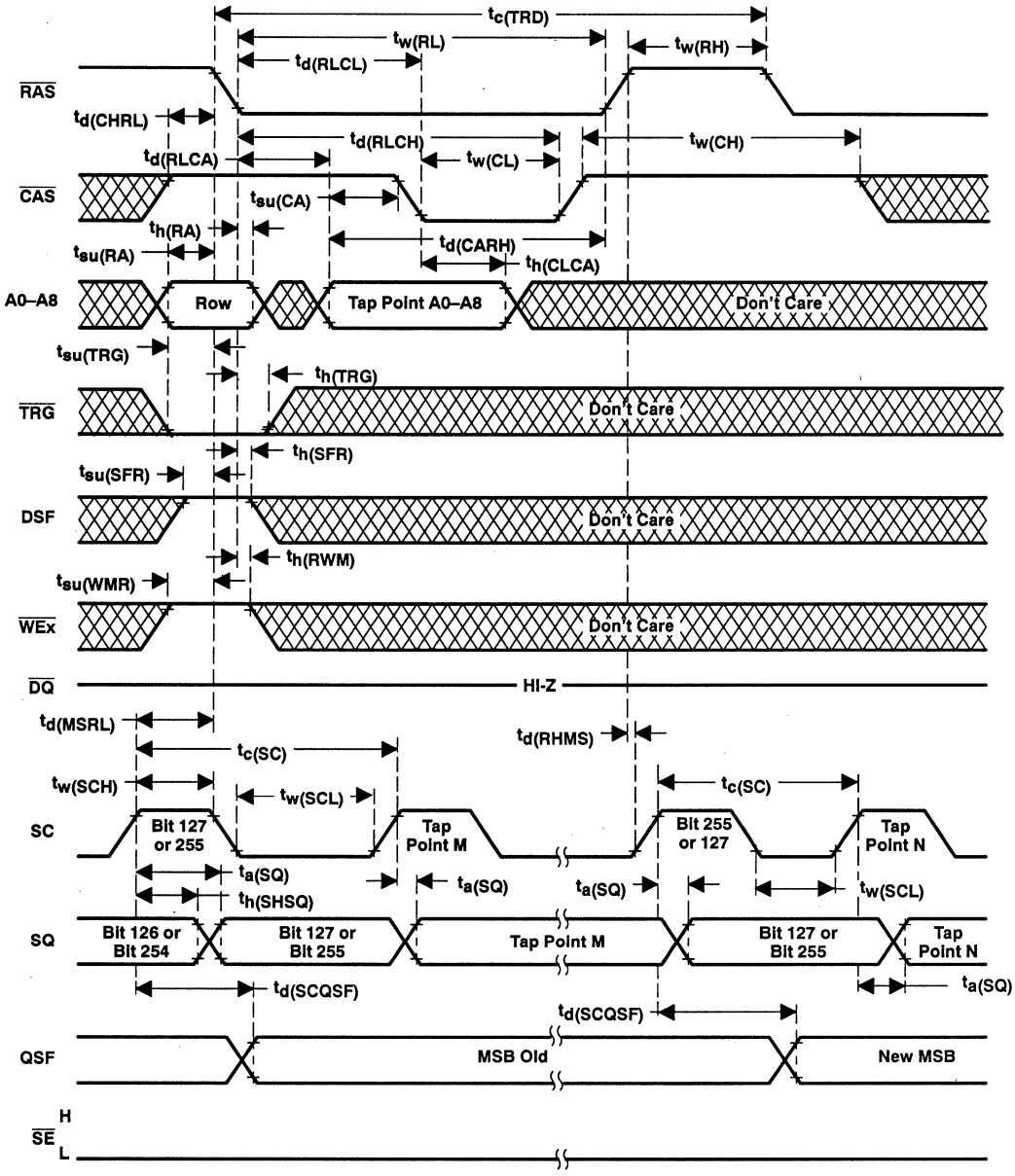
NOTES: A. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

B. Random mode (DQ outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

C. A0–A7: Register tap point, A8: which half of the transferred row.

Figure 38. Read Transfer Timing, Real-Time Reload Operation/Late Load Operation†

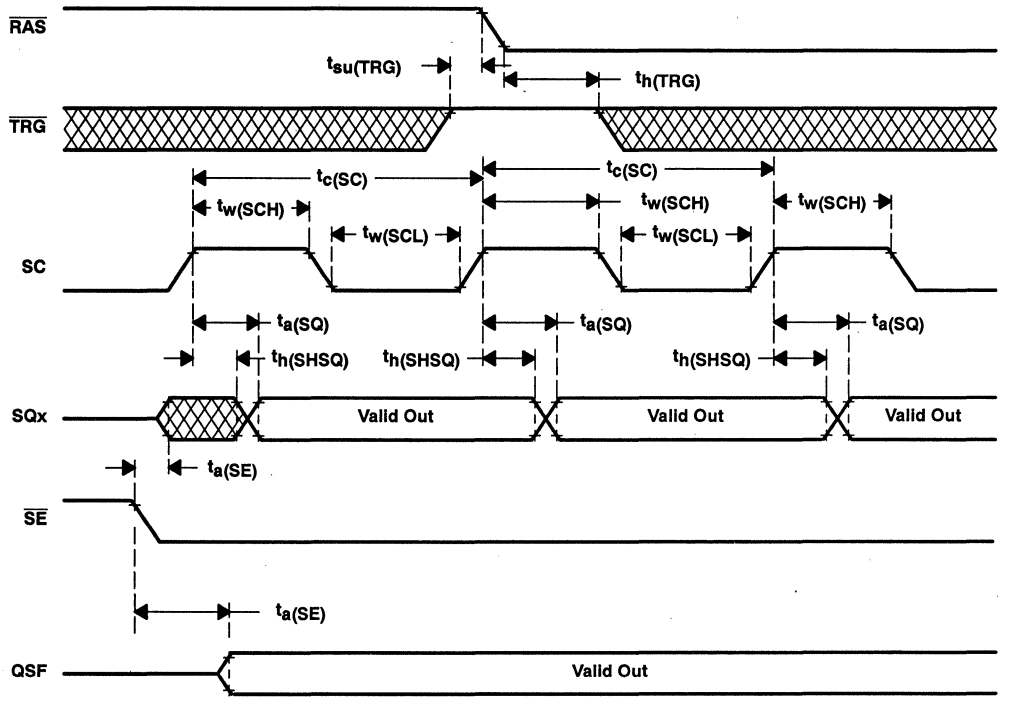
PARAMETER MEASUREMENT INFORMATION



NOTES: A. There is minimum requirement of one rising edge of SC clock between two split register transfer cycles.
B. A0–A6: Tap point of the given half, A7: Don't care, A8: DRAM row half.

Figure 39. Split-Register Read Transfer Timing

PARAMETER MEASUREMENT INFORMATION

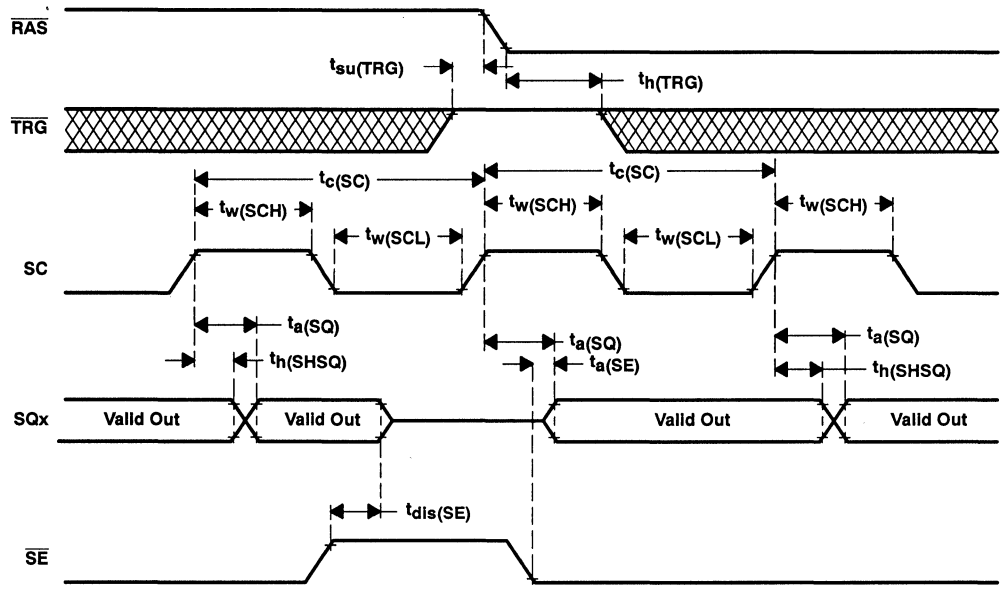


NOTES: A. While reading data through the serial data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.

B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

Figure 40. Serial Read Timing

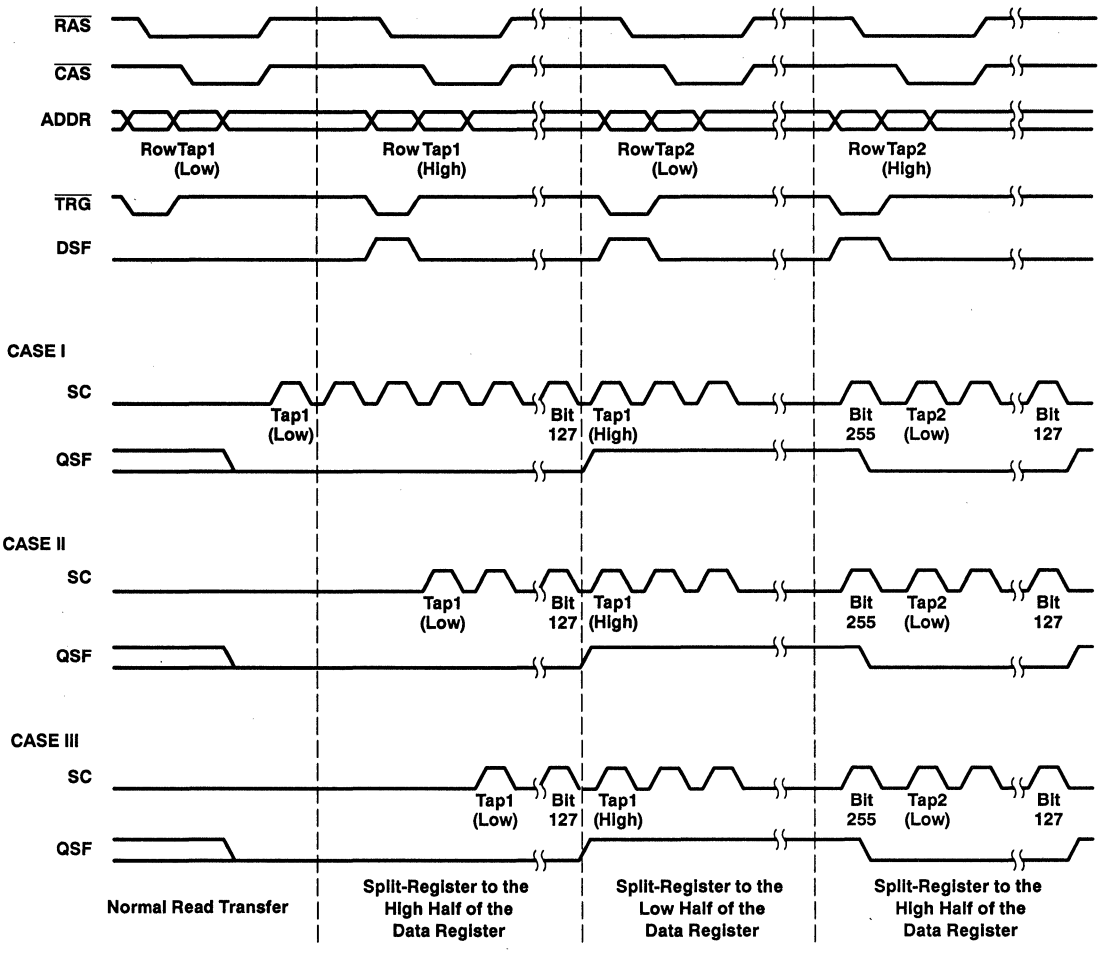
PARAMETER MEASUREMENT INFORMATION



NOTES: A. While reading data through the serial data register, the state of $\overline{TRG}$ is a don't care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory to register data transfer operation.
B. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

Figure 41. Serial Read Timing ($\overline{SE}$ Controlled Read)

OPERATING SEQUENCE INFORMATION

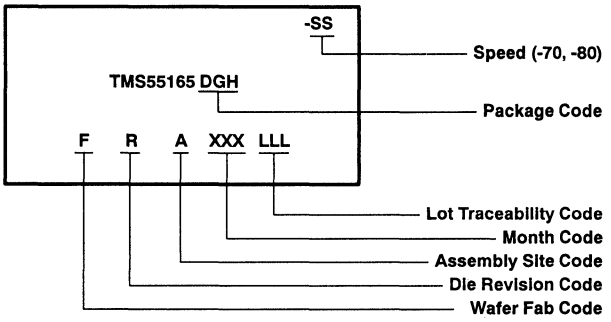


NOTES: A. In order to achieve proper split-register operation, a normal read transfer should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the normal read transfer cycle (CASE I), during the first split-register transfer cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the normal read transfer cycle and the first split-register cycle.

B. A split register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half. After the $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255). There is a minimum requirement of one rising edge of SC clock between two split-register transfer cycles.

Figure 42. Split-Register Operating Sequence

device symbolization

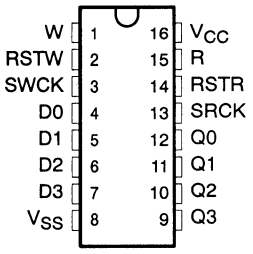


- **Organization . . . 262 264 × 4**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **Fast FIFO (First-In First-Out) Operation**
  - **Full Word Continuous Read/Write**
  - **Asynchronous Read/Write**
- **Fully-Static (Refresh Free)**
- **High-Speed Read/Write Operation**

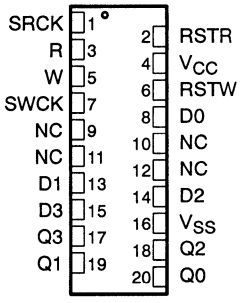
	ACCESS TIME (MAX)	CYCLE TIME READ (MIN)	CYCLE TIME WRITE (MIN)
TMS4C1050B-30	25 ns	30 ns	30 ns
TMS4C1050B-40	30 ns	40 ns	40 ns
TMS4C1050B-60	50 ns	60 ns	60 ns

- **Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)**
- **Plastic 16-Pin 300-mil-Wide DIP, 20-Pin 400-mil ZIP, or 20/26-Lead Surface-Mount (SOJ) Package**
- **Texas Instruments EPIC™ (Enhanced Performance Implanted CMOS) Technology**
- **Operating Free-Air Temperature 0°C to 70°C**
- **Fully Compatible With TMS4C1050**

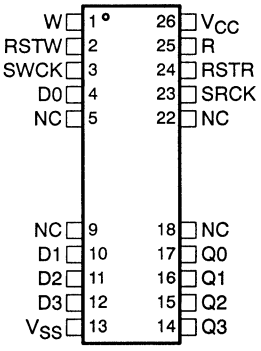
N PACKAGE†
(TOP VIEW)



SD PACKAGE†
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



† The packages are shown for pinout reference only.

PIN NOMENCLATURE	
D0–D3	Data-In
Q0–Q3	Data-Out
R	Read Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
W	Write Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground

description

The TMS4C1050B is a Field Memory (FMEM) which reads and writes data exclusively through serial ports, 4 bits wide. Maximum storage capacity is 262 264 words by four bits each. Addressing is controlled by write address and read address pointers which must be reset to zero before memory access begins.

Read and write access may occur asynchronously. When read access is delayed relative to write access, the TMS4C1050B functions like a First-In First-Out (FIFO) register. The amount of delay determines the length of the FIFO register.

Unlike a conventional FIFO register, data may be read as many times as desired after it is written into the storage array.

Minimum delay between writing into the device and reading out data is 600 SWCK cycles. Maximum delay is one full field (262 264 write cycles).

The TMS4C1050B employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

To achieve high density, dynamic data storage cells are employed as the main data memory . Self-refresh and arbitration logic are implemented in the TMS4C1050B, supplying a refresh-free system. This logic prevents any conflict between data-saving/data-loading/memory-refresh requests.

If the memory is to be used as a delay element only, it is not necessary to reset the address pointers. After the memory has been completely filled and the write address pointer reaches its maximum value, it will wrap around again to the first address of the main array (address 120). The read address pointer behaves in the same manner.

The TMS4C1050B is offered in a 16-pin dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 7,62-mm (300-mil) centers. This device is also offered in a 20-pin 400-mil ZIP package (SD suffix) and a 300-mil 20/26 J-lead plastic surface mount SOJ package (DJ suffix). The SOJ package is still in development, and the ADVANCE INFORMATION notice in this data sheet applies to this package. The TMS4C1050B is characterized for operation from 0°C to 70°C.

operation

write operation

The write operation is controlled by W and two clocks, SWCK and RSTW. It is accomplished by cycling SWCK and holding W high after the write address pointer reset operation (RSTW). Each write operation, beginning with RSTW, must contain at least 120 active write cycles (SWCK cycles while W is high). To transfer the last data written into the device (which at that time is still stored in the write line buffer) to the memory array, an RSTW operation is required after the last SWCK cycle.

reset write (RSTW)

The first positive transition of SWCK after RSTW going high, resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. The state of W may be high or low during any reset operation. Before RSTW may be brought high again for a further reset operation, it must have been low for at least two SWCK cycles.

data inputs (D0-D3) and write clock (SWCK)

The SWCK input latches the data inputs on chip when W is high and also increments the internal write address pointer. Data-in setup and hold times ($t_{su(D)}$, $t_{h(D)}$) are referenced to the rising edge of SWCK.

write enable (W)

W is used as a data-in enable/disable. A logic high on the W input enables the input, and a logic low disables the input and holds the internal write address pointer.

Note that W setup and hold times are referenced to the rising edge of SWCK.

read operation

The read operation is controlled by R and two clocks, SRCK and RSTR. It is accomplished by cycling SRCK and holding R high after a read address pointer reset operation (RSTR). Each read operation, which begins with RSTR, must contain at least 120 active read cycles (SRCK cycles while R is high).

reset read (RSTR)

The first positive transition of SRCK after RSTR goes high resets the read address pointers to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. The state of R may be high or low during any reset operation. Before RSTR may be brought high again for a further reset operation, it must have been low for at least two SRCK cycles.

data out (Q0-Q3) and read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R is high during a read operation. The SRCK input increments the internal read address pointer when R is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the positive transition of SRCK.

Output valid time [$t_{V(OUT)}$] is referenced to the rising edge of SRCK in the next cycle.

output enabling and disabling

When R changes state, the outputs will become enabled or disabled. However, SRCK must go low also, before a change of the state of R can be noticed at the outputs. The state of SRCK influences the outputs only during the first SRCK cycle following each change of state of R.

In order for the outputs to become enabled, R must go high and SRCK must go low. Enable time is determined by whichever transition (R going high or SRCK going low) occurs last. In order for the outputs to become disabled, R must go low and SRCK must go low. Disable time is determined by whichever transition (R going low or SRCK going low) occurs last. See the timing diagrams under read cycle timing (output enable and disable) for an illustration of enable and disable timing.

read enable (R)

R performs a double function. First, R gates the SRCK clock for incrementing the read pointer. When R is high before the rising edge of SRCK, the read pointer is incremented. When R is low, the read pointer is not incremented. R setup times ($t_{su(RH)}$ and $t_{su(RL)}$ and R hold times [$t_{h(R)}$] are referenced to the rising edge of the SRCK clock.

The second function of R is to enable and disable the outputs. See the appropriate section on output enabling and disabling.

power up and initialization

When powering up, the device is designed to begin proper operation after at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. This time is defined as $t_{POWER\text{-}OK}$. While it is acceptable to start the initialization sequence during V_{CC} ramp-up (before $t_{POWER\text{-}OK}$), the full sequence must be repeated at least once after $t_{POWER\text{-}OK}$. The required initialization sequence for the write pointers is as follows:

At least one SWCK clock cycle, followed by a reset write operation, followed by at least 130 dummy write operations with W at high level, followed by another reset write operation. All timing parameters must be within specifications for the initialization sequence. After initialization, the write address pointers are set to zero, and writing may begin.

The initialization sequence for the read pointers is analogous to write pointer initialization, and must be performed at least once after $t_{POWER\text{-}OK}$.

old/new data access

There must be a minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation, before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 120 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called old data.

In order to read out new data, i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined. It may be old data or new data or a combination of old and new data. Such a timing should be avoided.

internal operation

writing into memory

The first 120 words of data following the initial RSTW operation after power-up are written into a cache buffer (A) initially, and will never be stored elsewhere, to allow read-out of data later without the delay involved in retrieving it from the main memory array.

Starting from address 120, data is written into the write line buffer, top block, until this block (256 words long) is full. Further writing then occurs to the bottom block of the write line buffer, while the top block is transferred to the main memory array. By the time the bottom block is full, the top block has been transferred to memory and can be used again to receive new incoming data. The channeling of input data into the top or bottom block is controlled internally by the device and is transparent to the user.

After the 120-word long cache buffer has been filled with incoming data, the input line selector switches the connection of the input port over to the B line buffer to assure that the next field of data, which will arrive later after a subsequent RSTW operation, does not over write the content of the cache buffer. Each subsequent filling of the cache buffer toggles the connection of the input port between the A and the B line buffers with the 121st SWCK pulse. The A and B line buffers, as well as the input line selector, are static registers.

The connection of the output port will also be toggled between A and B line buffers by the 121st SWCK pulse, providing no read operation from a cache buffer is in progress at this time. The output port will always be connected to the line buffers opposite to the one connected to the input port. In case a read operation from a cache buffer is in progress when the 121st SWCK occurs, the toggling of the output port connection will be delayed until the cache buffer has been read out completely.

The requirement stated on page 2 that each write operation must contain at least 120 active SWCK cycles, exists in order to assure that the toggling of the input and output ports between the A line buffer and the B line buffer functions without errors as described above.

The serial write pointer stores the (column) address of the last input data word received, while the write counter stores the row address.

After the last word of a full write cycle has been latched in (with a positive transition of the SWCK clock), the write line buffer most likely will be partially filled without having been transferred to the main memory array. To assure that the information contained in the write line buffer is stored and cannot be lost, it is required that an RSTW operation be performed when write clocking has stopped.

In addition to transferring the partially filled write line buffer into the main memory array, this RSTW operation will also reset the write addresses (serial write pointer) to zero. Regardless of how much later a new write cycle starts, it is not necessary to perform another RSTW operation again at that time.

reading from memory

After an RSTR operation, data from the main memory array (starting at address 120) will be transferred to a read line buffer. Because this transfer requires some time, the first 120 words will be read out of the A or B line buffers, where they had been previously stored (see writing into memory above).

If the first RSTR operation occurs after the first RSTW operation but before the second RSTW operation, read access will be to the same buffer that data had been written into during the first write cycle. Thus old data will be read out.

If the first RSTR operation occurs after the second RSTW operation, i.e. after the writing in of new data has already started, then the delay between the second RSTW and the first RSTR operation determines whether old data or new data will be read out.

If this delay is less than 120 SWCK cycles, data will be read out from the line buffer that was written into during the previous write cycle; i.e., old data will be read out. A delay of less than 120 SWCK cycles also assures that all following data bits are old data, because replacement of old data by new data in the main memory array will occur later than the respective read access to each address in the array.

If this delay is more than 600 SWCK cycles, data will be read out from the line buffer that it was written into during the current write cycle; i.e., new data will be read out. A delay of more than 600 SWCK cycles also assures that all following data bits are new data, because replacement of old data by new data in the main memory array will occur before the respective read access to each address in the array.

If this delay is more than 120 words, words, but less than 600 SWCK cycles, data read out can be either old or new or a mixture of old and new data, because it cannot be predicted accurately whether a word accessed for reading has already been replaced by new data or not. Such a situation should be avoided.

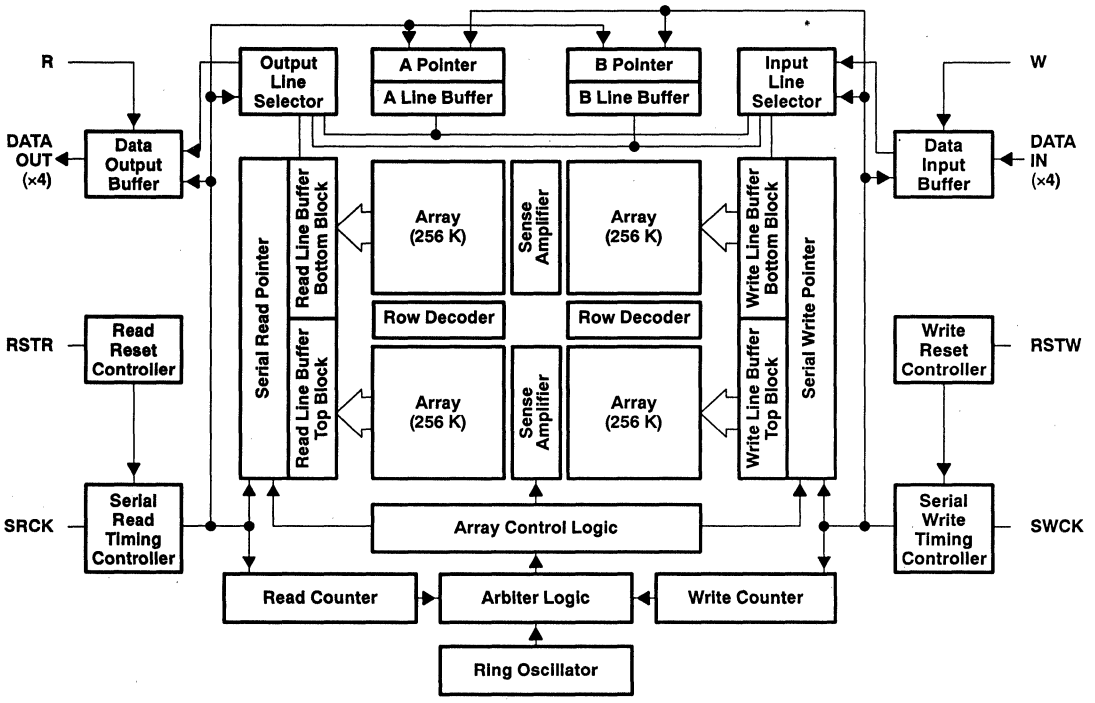
After the first 120 words are read out of the A or B line buffer, read transfer from the main memory array to the read line buffer is finished, and subsequent reading will occur from this buffer. Similar to the write operation, while one half of this buffer is being read out, the other half will be filled again by a new read transfer from the main memory array.

The serial read pointer stores the (column) address of the last data word read out, while the read counter stores the row address.

self-refresh and arbitration logic

The self-refresh and arbitration logic will keep the main memory information refreshed automatically without requiring any user action, control the address pointers for both read and write, and control the flow of information both into and out of the main memory.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1)	–1 V to 7 V
Supply voltage range on V_{CC}	0 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL} = – 1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4C1050B-30		'4C1050B-40		'4C1050B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, R low		±10		±10		±10	µA
I_{DD1}	Average operating current	Minimum write/read cycle, output open		50		45		35	mA
I_{DD2}	Standby current	After 1 RSTW/RSTR cycle, W and R low		10		10		10	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz			7	pF
C_o	Output capacitance	V_I = 0, f = 1 MHz			10	pF

† V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	'4C1050B-30		'4C1050B-40		'4C1050B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	(see Note 3)		25		30		50	ns
$t_{v(OUT)}$	Output valid time after SRCK high	(see Note 3)	6		6		6		ns
$t_{dis(CK)}$	Output disable time after SRCK low	(see Note 4)	4	15	4	15	4	15	ns
$t_{en(CK)}$	Output enable time after SRCK low	(see Note 3)	0	15	0	15	0	15	ns
$t_{en(RH)}$	Output enable time after R high	(see Note 3)	0	15	0	15	0	15	ns
$t_{dis(RL)}$	Output disable time after R low	(see Note 4)	4	15	4	15	4	15	ns

NOTES: 3. The load connected to each output is a 50-pF capacitor to ground, in parallel with a 218-Ω resistor to 1.31 V as illustrated by Figure 1.

4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output voltage waveforms, sufficiently low load resistors and capacitors have to be used, and the RC time constants of the load have to be taken into account.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'4C1050B-30		'4C1050B-40		'4C1050B-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time (see Note 6)	30		40		60		ns
$t_{c(R)}$	Read cycle time (see Note 6)	30		40		60		ns
$t_{w(R)}$	Pulse duration, R low	10		10		10		ns
$t_{w(W)}$	Pulse duration, W low	10		10		10		ns
$t_{w(RH)}$	Pulse duration, SRCK high	12		17		20		ns
$t_{w(RL)}$	Pulse duration, SRCK low	12		17		20		ns
$t_{w(WH)}$	Pulse duration, SWCK high	12		17		20		ns
$t_{w(WL)}$	Pulse duration, SWCK low	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{su(RH)}$	R-high setup time before SRCK high	0		0		0		ns
$t_{su(RL)}$	R-low setup time before SRCK high	0		0		0		ns
$t_{su(WH)}$	W-high setup time before SWCK high	0		0		0		ns
$t_{su(WL)}$	W-low setup time before SWCK high	0		0		0		ns
$t_{su(RSTR)}$	RSTR setup time before SRCK high	3		3		3		ns
$t_{su(RSTW)}$	RSTW setup time before SWCK high	3		3		3		ns
$t_{h(D)}$	Data hold time after SWCK high	6		6		6		ns
$t_{h(R)}$	R-hold time after SRCK high	6		6		6		ns
$t_{h(W)}$	W-hold time after SWCK high	6		6		6		ns
$t_{h(RSTR)}$	RSTR hold time after SRCK high	6		6		6		ns
$t_{h(RSTW)}$	RSTW hold time after SWCK high	6		6		6		ns
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IH} (MIN) = 2.4 V and V_{IL} (MAX) = 0.8 V. t_T is measured between V_{IH} (MIN) and V_{IL} (MAX).
6. All cycle times assume t_T = 3 ns.

PARAMETER MEASUREMENT INFORMATION

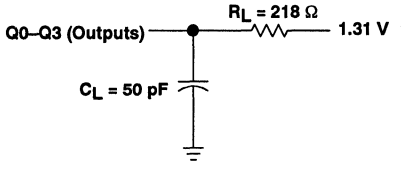


Figure 1. Load Circuit for Timing Parameters

PARAMETER MEASUREMENT INFORMATION

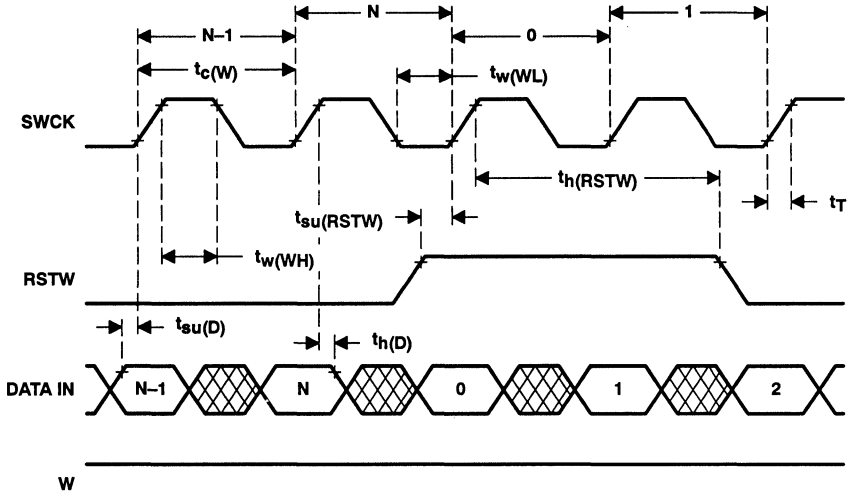


Figure 2. Write Cycle Timing (Reset Write)

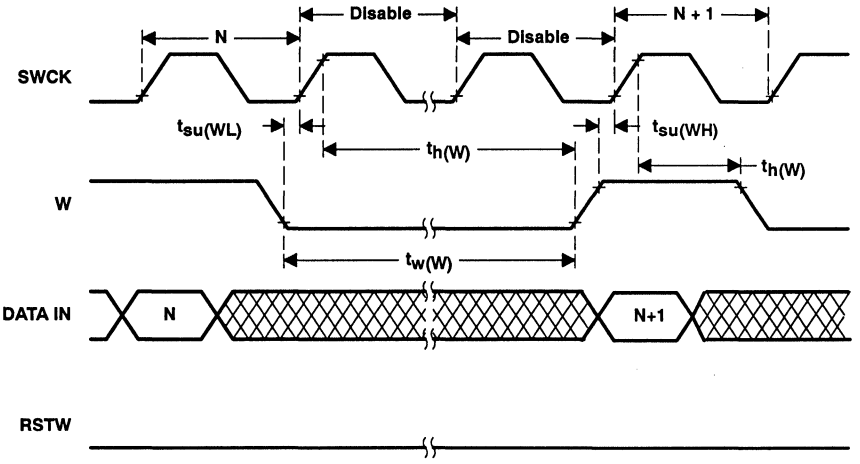


Figure 3. Write Cycle Timing (Write Enable)

PARAMETER MEASUREMENT INFORMATION

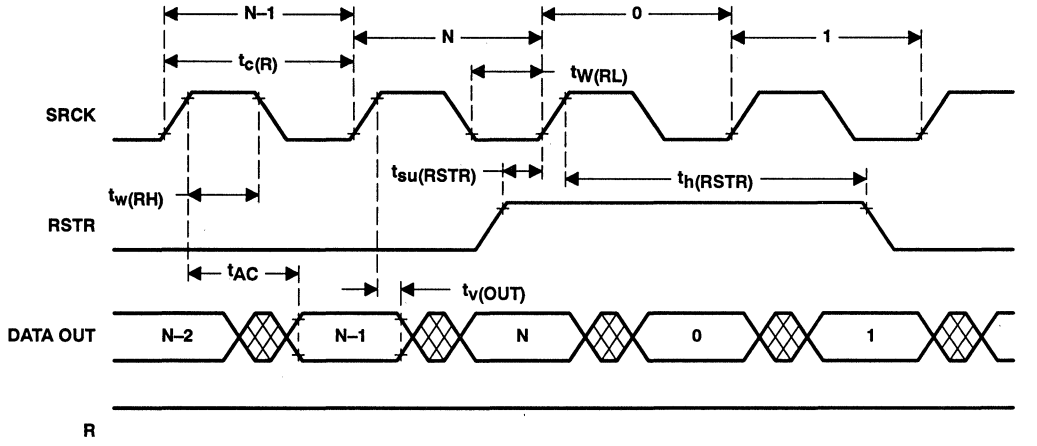


Figure 4. Read Cycle Timing (Reset Read)

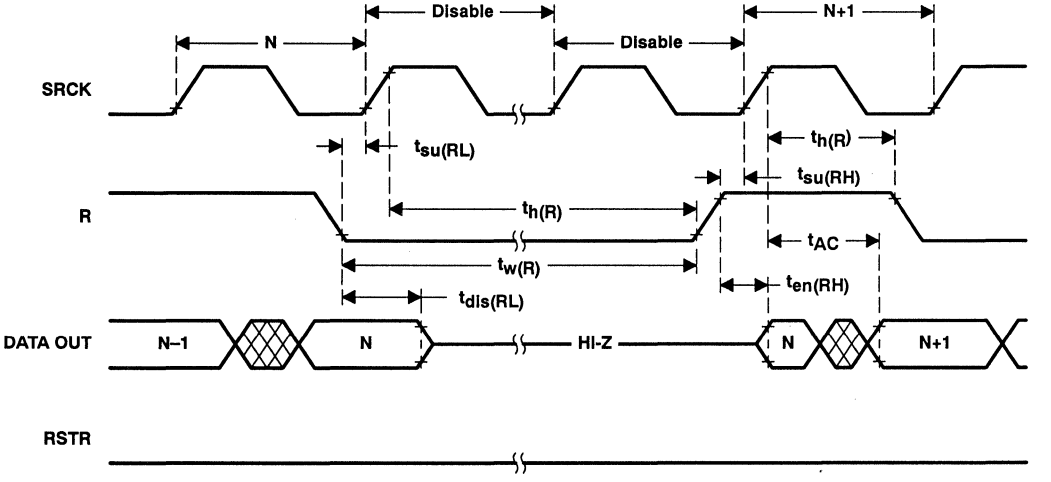


Figure 5. Read Cycle Timing (Read Enable)

PARAMETER MEASUREMENT INFORMATION

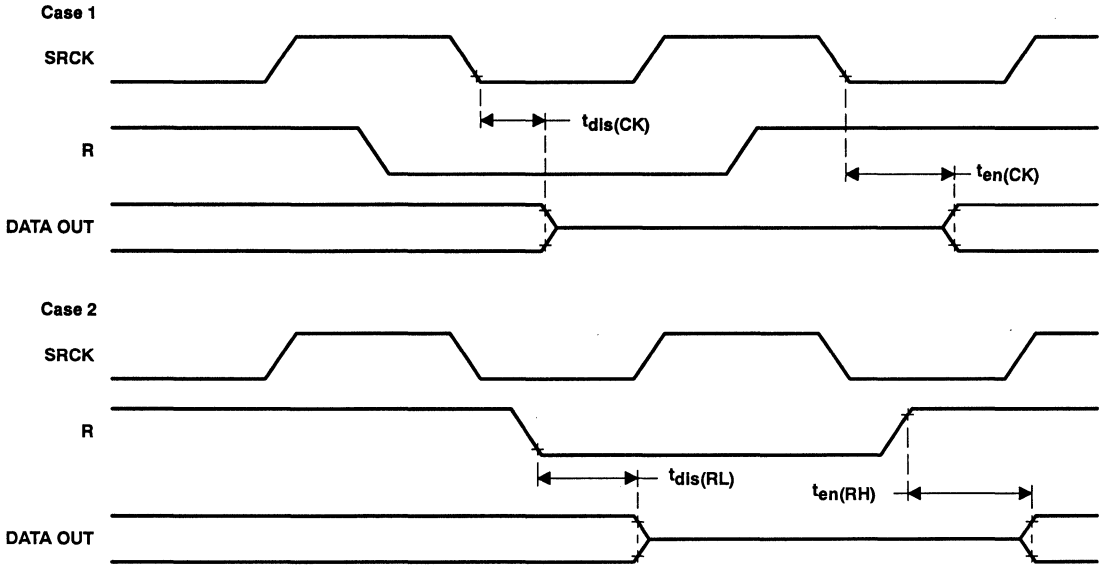


Figure 6. Read Cycle Timing (Output Enable and Disable)

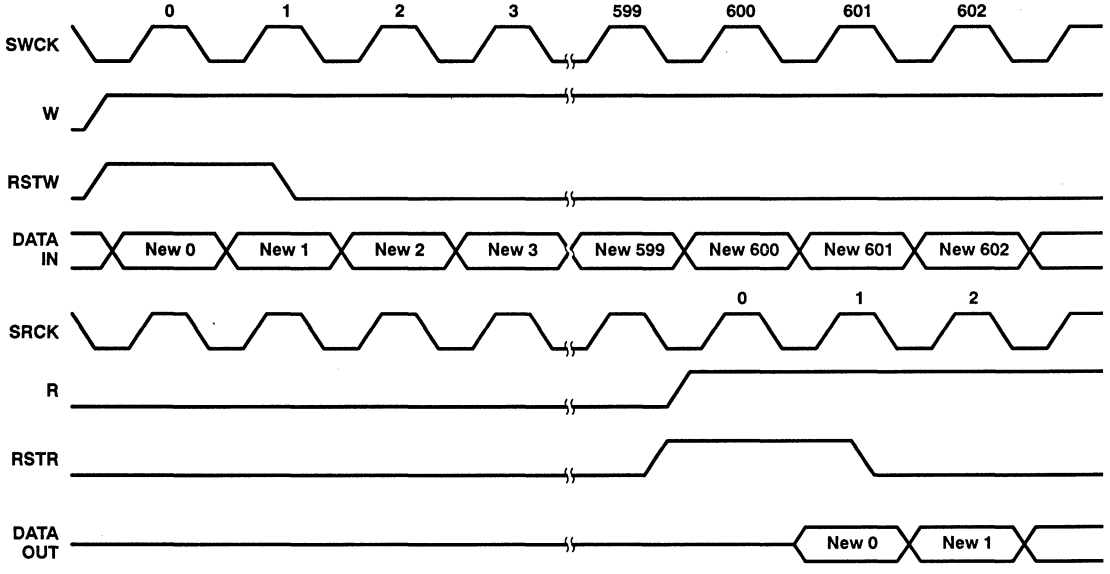


Figure 7. New Data Access Mode

PARAMETER MEASUREMENT INFORMATION

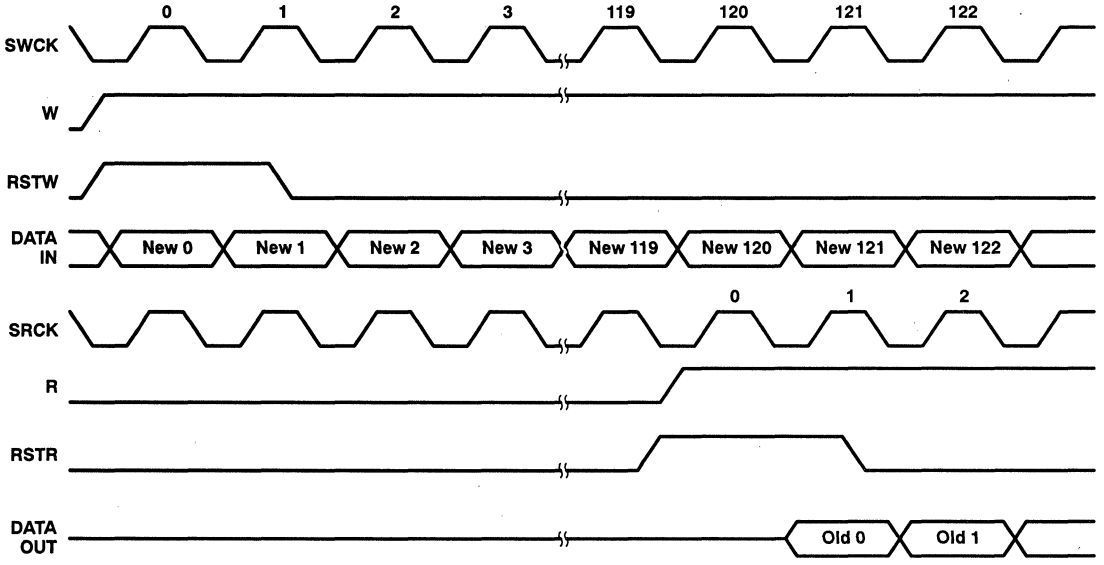


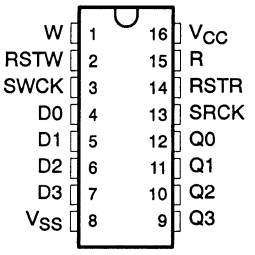
Figure 8. Old Data Access Mode

- **Organization . . . 262 264 × 4**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **Fast FIFO (First-In First-Out) Operation**
  - **Full Word Continuous Read/Write**
  - **Asynchronous Read/Write**
- **Fully Static (Refresh Free)**
- **High-Speed Read/Write Operation**
- **Cascade Connection Capability**
- **Max Access / Min Cycle Time**

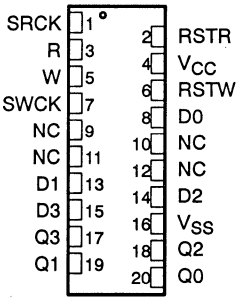
	ACCESS TIME (MAX)	CYCLE TIME READ (MIN)	CYCLE TIME WRITE (MIN)
TMS4C1060B-30	25 ns	30 ns	30 ns
TMS4C1060B-40	30 ns	40 ns	40 ns
TMS4C1060B-60	50 ns	60 ns	60 ns

- **Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)**
- **Plastic 16-Pin 300-mil-Wide DIP, 20-Pin 400-mil ZIP, or 20/26-Lead Surface-Mount (SOJ) Package**
- **Texas Instruments EPIC™ (Enhanced Performance Implanted CMOS) Technology**
- **Operating Free-Air Temperature 0°C to 70°C**
- **Fully Compatible With TMS4C1060**

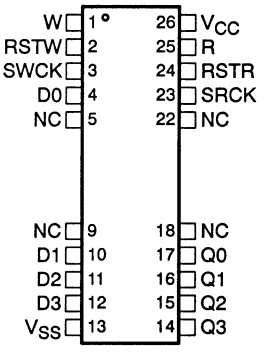
N PACKAGE†
(TOP VIEW)



SD PACKAGE†
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



† The packages are shown for pinout reference only.

description

The TMS4C1060B is a Field Memory (FMEM) which reads and writes data exclusively through serial ports, 4 bits wide. Maximum storage capacity is 262 264 words by four bits each. Addressing is controlled by write address and read address pointers which must be reset to zero before memory access begins.

Read and write access may occur asynchronously. When read access is delayed relative to write access, the TMS4C1060B functions like a First-In First-Out (FIFO) register. The amount of delay determines the length of the FIFO register.

PIN NOMENCLATURE	
D0–D3	Data-In
Q0–Q3	Data-Out
R	Read Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
W	Write Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground

Unlike a conventional FIFO register, data may be read as many times as desired after it is written into the storage array.

Minimum delay between writing into the device and reading out data is 600 SWCK cycles. Maximum delay is one full field (262 264 write cycles).

The TMS4C1060B employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

Dynamic data storage cells are employed as the main data memory to achieve high density. Self-refresh and arbitration logic are implemented within the TMS4C1060B, supplying a refresh-free system. This logic prevents any conflict between data-saving/data-loading/memory-refresh requests.

The write address counting scheme of the TMS4C1060B has been modified, relative to its read address counting scheme, to allow easy cascading of several memory devices. The timing of output enabling and disabling is clock edge controlled.

If the memory is to be used as a delay element only, it is not necessary to reset the address pointers. After the memory has been completely filled and the write address pointer reaches its maximum value, it will wrap around again to the first address of the main array (address 120). The read address pointer behaves in the same manner.

The TMS4C1060B is offered in a 16-pin dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 7,62-mm (300-mil) centers. The device is also offered in a 20-pin 400-mil ZIP package (SD suffix) and a 300-mil 20/26 J-lead plastic surface mount SOJ package (DJ suffix). The TMS4C1060B is characterized for operation from 0°C to 70°C.

operation

write operation

The write operation is controlled by W and two clocks, SWCK and RSTW. It is accomplished by cycling SWCK and holding W high after the write address pointer reset operation (RSTW). Each write operation, beginning with RSTW, must contain at least 120 active write cycles (SWCK cycles while W is high). To transfer the last data written into the device (which at that time is still stored in the write line buffer) to the memory array, an RSTW operation is required after the last SWCK cycle.

reset write (RSTW)

The first positive transition of SWCK after RSTW going high resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. The state of W may be high or low during any reset operation. Before RSTW may be brought high again for a further reset operation, it must have been low for at least two SWCK cycles.

data inputs (D0–D3) and write clock (SWCK)

The SWCK input latches the data inputs on chip when W is high and also increments the internal write address pointer. Data-in setup and hold times ($t_{su(D)}$, $t_{h(D)}$) are referenced to the rising edge of SWCK.

write enable (W)

W is used as a data-in enable/disable. A logic high on the W input enables the input, and a logic low disables the input and holds the internal write address pointer.

Note that W setup and hold times are referenced to the rising edge of SWCK.

read operation

The read operation is controlled by R and two clocks, SRCK and RSTR. It is accomplished by cycling SRCK and holding R high after a read address pointer reset operation (RSTR). Each read operation, which begins with RSTR, must contain at least 120 active read cycles (SRCK cycles while R is high).

reset read (RSTR)

The first positive transition of SRCK after RSTR goes high resets the read address pointers to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. The state of R may be high or low during any reset operation. Before RSTR may be brought high again for a further reset operation, it must have been low for at least two SRCK cycles.

data out (Q0–Q3) and read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R is high during a read operation. The SRCK input increments the internal read address pointer when R is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the positive transition of SRCK.

Output valid time [$t_{V(OUT)}$] is referenced to the rising edge of SRCK in the next cycle.

output enabling and disabling

The state of R is latched in by the read clock . SRCK determines whether the outputs will be enabled or disabled. If R is high at the rising edge of SRCK, the outputs will be enabled. If R is low at the rising edge of SRCK, the outputs will be disabled. R setup and hold times are referenced to the rising edge of SRCK.

read enable (R)

R performs a double function. First, R gates the SRCK clock for incrementing the read pointer. When R is high before the rising edge of SRCK, the read pointer is incremented. When R is low, the read pointer is not incremented. R setup times [($t_{su(RH)}$ and $t_{su(RL)}$] and R hold times [$t_{h(R)}$] are referenced to the rising edge of the SRCK clock.

The second function of R is to enable and disable the outputs. See the appropriate section on output enabling and disabling.

power-up and initialization

When powering up, the device is designed to begin proper operation after at least 100 µs after V_{CC} has stabilized to a value within the range of recommended operating conditions. This time is defined as $t_{POWER\text{-}OK}$. While it is acceptable to start the initialization sequence during V_{CC} ramp-up (before $t_{POWER\text{-}OK}$), the full sequence must be repeated at least once after $t_{POWER\text{-}OK}$. The required initialization sequence for the write pointers is as follows:

At least one SWCK clock cycle, followed by a reset write operation, followed by at least 130 dummy write operations with W at high level, followed by another reset write operation. All timing parameters must be within specifications for the initialization sequence. After initialization, the write address pointers are set to zero, and writing may begin.

The initialization sequence for the read pointers is analogous to write pointer initialization, and must be performed at least once after $t_{POWER\text{-}OK}$.

old/new data access

There must be minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation, before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 120 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called old data.

In order to read out new data, i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined. It may be old data or new data or a combination of old and new data. Such a timing should be avoided.

cascade operation

The TMS4C1060B has been designed to allow easy cascading of multiple memory devices, in order to obtain a higher storage depth or a longer delay than can be achieved with only one memory device. See the interconnection diagram on page 11 for details.

As illustrated in the timing diagram on page 11, the positive SRCK/SWCK edge at the beginning of a clock cycle serves to initiate read-out, whereas writing in is initiated by the positive SWCK/SRCK edge at the end of a cycle. This differs from the functionality of the TMS4C1050B, in which both the read-out and the write-in are initiated at the beginning of a clock cycle.

Internal operation

writing into memory

The first 120 words of data following the initial RSTW operation after power-up are written into a cache line buffer (A) initially, and will never be stored elsewhere, to allow read-out of data later without the delay involved in retrieving it from the main memory array.

Starting from address 120, data is written into the write line buffer, top block, until this block (256 words long) is full. Further writing then occurs to the bottom block of the write line buffer, while the top block is transferred to the main memory array. By the time the bottom block is full, the top block has been transferred to memory and can be used again to receive new incoming data. The channeling of input data into the top or bottom block is controlled internally by the device and is transparent to the user.

After the 120-word long cache buffer has been filled with incoming data, the input line selector switches the connection of the input port over to the B line buffer to assure that the next field of data, which will arrive later after a subsequent RSTW operation, does not overwrite the content of the cache buffer. Each subsequent filling of the cache buffer toggles the connection of the input port between the A and the B line buffers with the 121st SWCK pulse. The A and B line buffers, as well as the input line selector, are static registers.

The connection of the output port will also be toggled between A and B line buffers by the 121st SWCK pulse, providing no read operation from a cache buffer is in progress at this time. The output port will always be connected to the line buffers opposite to the one connected to the input port. In case a read operation from a cache buffer is in progress when the 121st SWCK occurs, the toggling of the output port connection will be delayed until the cache buffer has been read out completely.

The requirement stated on page 2 that each write operation must contain at least 120 active SWCK cycles, exists in order to assure that the toggling of the input and output ports between the A line buffer and the B line buffer functions without errors as described above.

The serial write pointer stores the (column) address of the last input data word received, while the write counter stores the row address.

After the last word of a full write cycle has been latched in (with a positive transition of the SWCK clock), the write line buffer most likely will be partially filled without having been transferred to the main memory array. To assure that the information contained in the write line buffer is stored and cannot be lost, it is required that an RSTW operation be performed when write clocking has stopped.

In addition to transferring the partially filled write line buffer into the main memory array, this RSTW operation will also reset the write addresses (serial write pointer) to zero. Regardless of how much later a new write cycle starts, it is not necessary to perform another RSTW operation again at that time.

reading from memory

After an RSTR operation, data from the main memory array (starting at address 120) will be transferred to a read line buffer. Because this transfer requires some time, the first 120 words will be read out of the A or B line buffers, where they had been previously stored (see writing into memory above).

If the first RSTR operation occurs after the first RSTW operation but before the second RSTW operation, read access will be to the same buffer that data had been written into during the first write cycle. Thus old data will be read out.

If the first RSTR operation occurs after the second RSTW operation (i.e., after the writing in of new data has already started), then the delay between the second RSTW and the first RSTR operation determines whether old data or new data will be read out.

If this delay is less than 120 SWCK cycles, data will be read out from the line buffer that was written into during the previous write cycle; i.e., old data will be read out. A delay of less than 120 SWCK cycles also assures that all following data bits are old data, because replacement of old data by new data in the main memory array will occur later than the respective read access to each address in the array.

If this delay is more than 600 SWCK cycles, data will be read out from the line buffer that it was written into during the current write cycle; i.e., new data will be read out. A delay of more than 600 SWCK cycles also assures that all following data bits are new data, because replacement of old data by new data in the main memory array will occur before the respective read access to each address in the array.

If this delay is more than 120 but less than 600 SWCK cycles, data read out can be either old or new or a mixture of old and new data, because it cannot be predicted accurately whether a word accessed for reading has already been replaced by new data or not. Such a situation should be avoided.

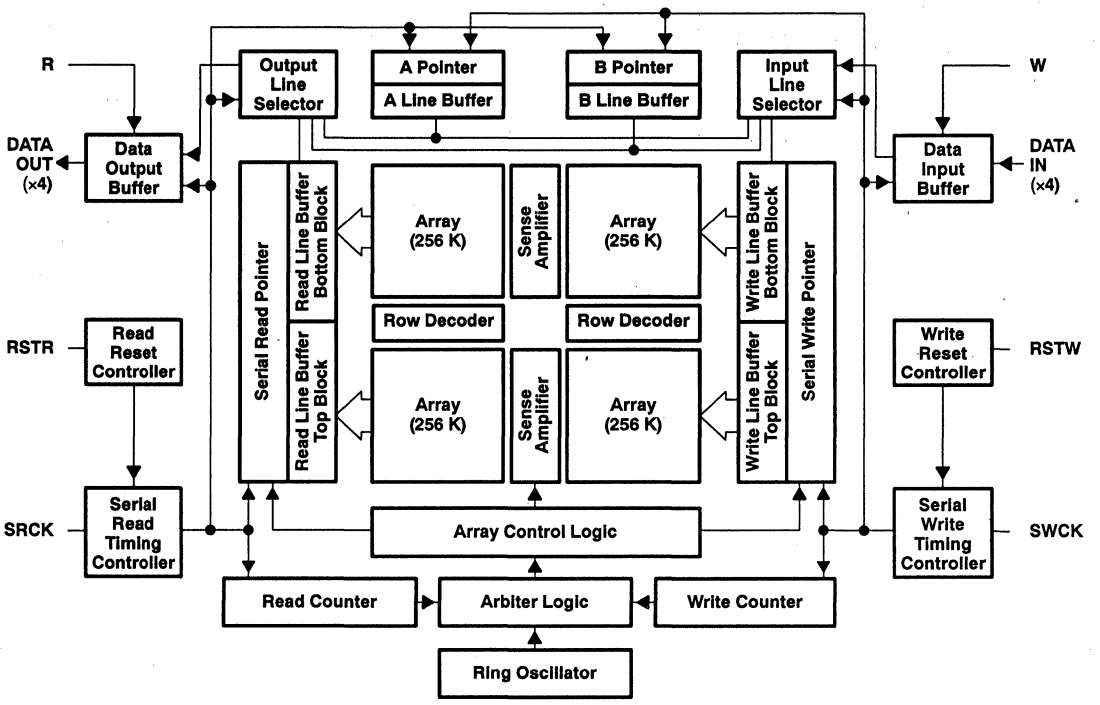
After the first 120 words are read out of the A or B line buffer, read transfer from the main memory array to the read line buffer is finished, and subsequent reading will occur from this buffer. Similar to the write operation, while one half of this buffer is being read out, the other half will be filled again by a new read transfer from the main memory array.

The serial read pointer stores the (column) address of the last data word read out, while the read counter stores the row address.

self-refresh and arbitration logic

The self-refresh and arbitration logic will keep the main memory information refreshed automatically without requiring any user action, control the address pointers for both read and write, and control the flow of information both into and out of the main memory.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1)	– 1 V to 7 V
Supply voltage range on V_{CC}	0 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL} = – 1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4C1060B-30		'4C1060B-40		'4C1060B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, R low		±10		±10		±10	µA
I_{DD1}	Average operating current	Minimum write/read cycle, output open		50		45		35	mA
I_{DD2}	Standby current	After 1 RSTW/RSTR cycle, W and R low		10		10		10	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz			7	pF
C_o	Output capacitance	V_I = 0, f = 1 MHz			10	pF

† V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	'4C1060B-30		'4C1060B-40		'4C1060B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	see Note 3		25		30		50	ns
$t_{v(OUT)}$	Output valid time after SRCK high	see Note 3	6		6		6		ns
$t_{dis(CK)}$	Output disable time after SRCK high	see Note 4	4	15	4	15	4	15	ns
$t_{en(CK)}$	Output enable time after SRCK high	see Note 3	0	15	0	15	0	15	ns

NOTES: 3. The load connected to each output is a 50-pF capacitor to ground in parallel with a 218-Ω resistor to 1.31 V as illustrated by Figure 1.

4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output voltage waveforms, sufficiently low load resistors and capacitors have to be used, and the RC time constants of the load have to be taken into account.

PARAMETER MEASUREMENT INFORMATION

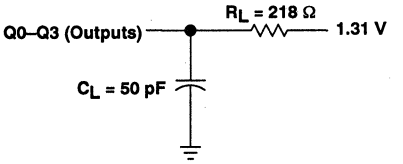


Figure 1. Load Circuit for Timing Parameters

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'4C1060B-30		'4C1060B-40		'4C1060B-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time (see Note 6)	30		40		60		ns
$t_{c(R)}$	Read cycle time (see Note 6)	30		40		60		ns
$t_{w(R)}$	Pulse duration, R low	10		10		10		ns
$t_{w(W)}$	Pulse duration, W low	10		10		10		ns
$t_{w(RH)}$	Pulse duration, SRCK high	12		17		20		ns
$t_{w(RL)}$	Pulse duration, SRCK low	12		17		20		ns
$t_{w(WH)}$	Pulse duration, SWCK high	12		17		20		ns
$t_{w(WL)}$	Pulse duration, SWCK low	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{su(RH)}$	R-high setup time before SRCK high	0		0		0		ns
$t_{su(RL)}$	R-low setup time before SRCK high	0		0		0		ns
$t_{su(WH)}$	W-high setup time before SWCK high	0		0		0		ns
$t_{su(WL)}$	W-low setup time before SWCK high	0		0		0		ns
$t_{su(RSTR)}$	RSTR setup time before SRCK high	3		3		3		ns
$t_{su(RSTW)}$	RSTW setup time before SWCK high	3		3		3		ns
$t_{h(D)}$	Data hold time after SWCK high	6		6		6		ns
$t_{h(R)}$	R-hold time after SRCK high	6		6		6		ns
$t_{h(W)}$	W-hold time after SWCK high	6		6		6		ns
$t_{h(RSTR)}$	RSTR hold time after SRCK high	6		6		6		ns
$t_{h(RSTW)}$	RSTW hold time after SWCK high	6		6		6		ns
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IH} (MIN) = 2.4 V and V_{IL} (MAX) = 0.8 V. t_T is measured between V_{IH} (MIN) and V_{IL} (MAX).
6. All cycle times assume t_T = 3 ns.

PARAMETER MEASUREMENT INFORMATION

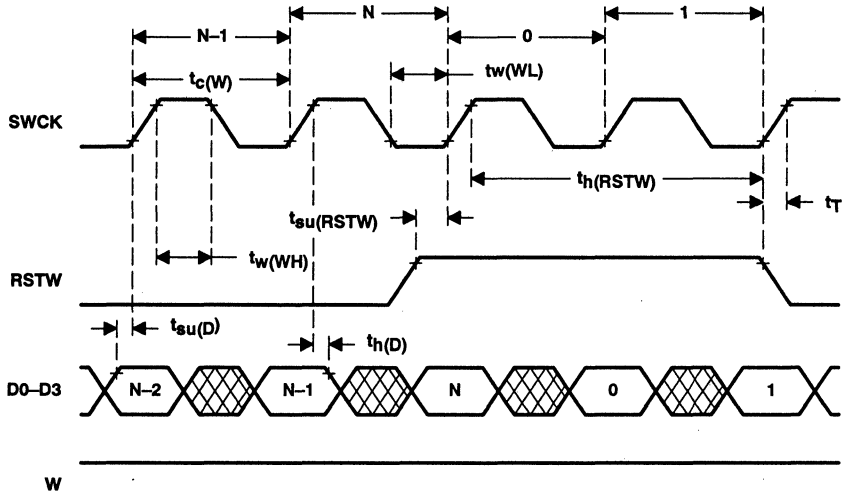


Figure 2. Write Cycle Timing (Reset Write)

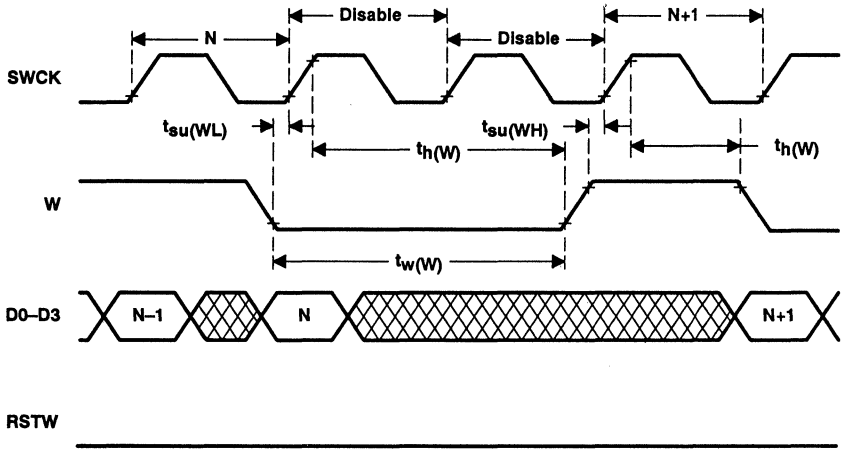


Figure 3. Write Cycle Timing (Write Enable)

PARAMETER MEASUREMENT INFORMATION

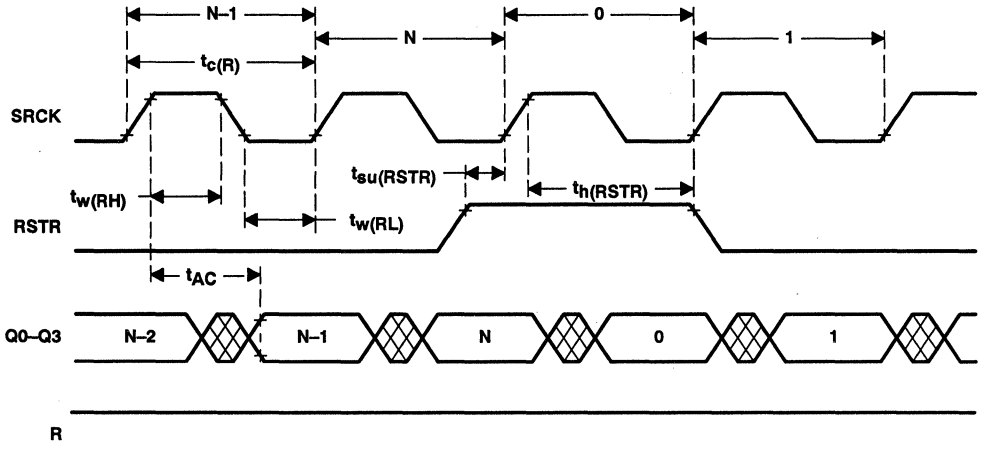


Figure 4. Read Cycle Timing (Reset Read)

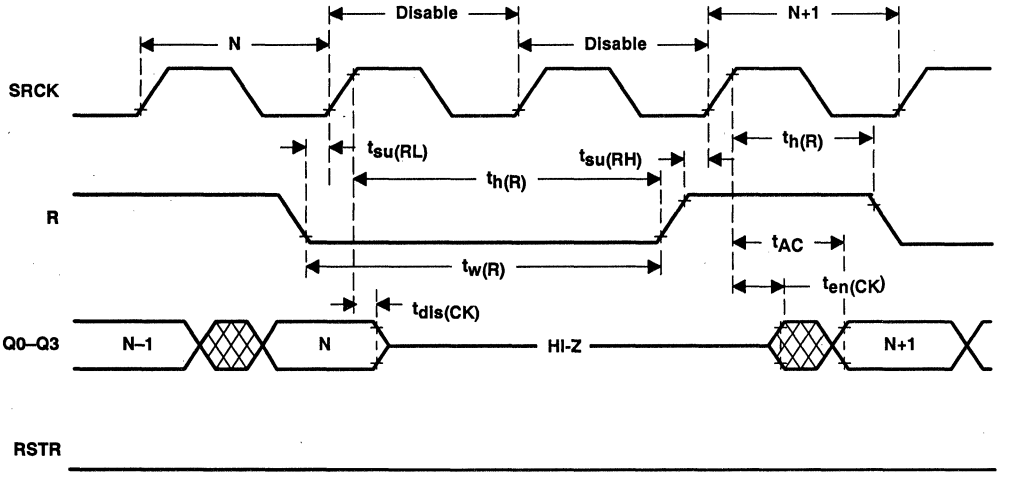


Figure 5. Read Cycle Timing (Read Enable)

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PARAMETER MEASUREMENT INFORMATION

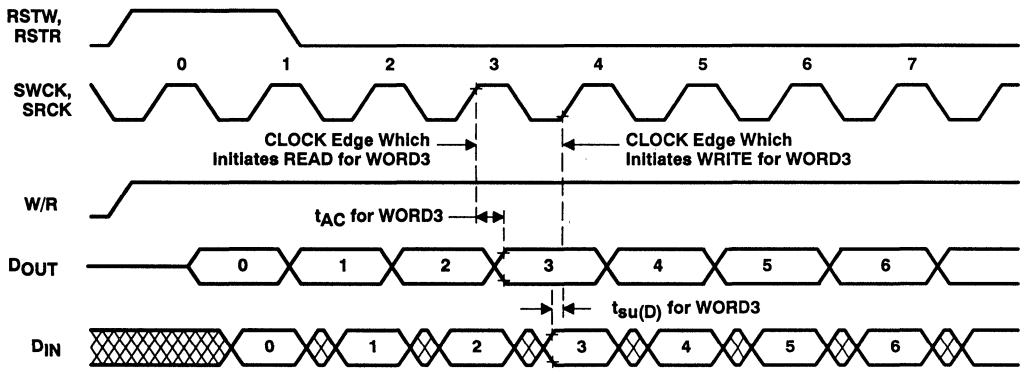


Figure 6. Cascade Mode

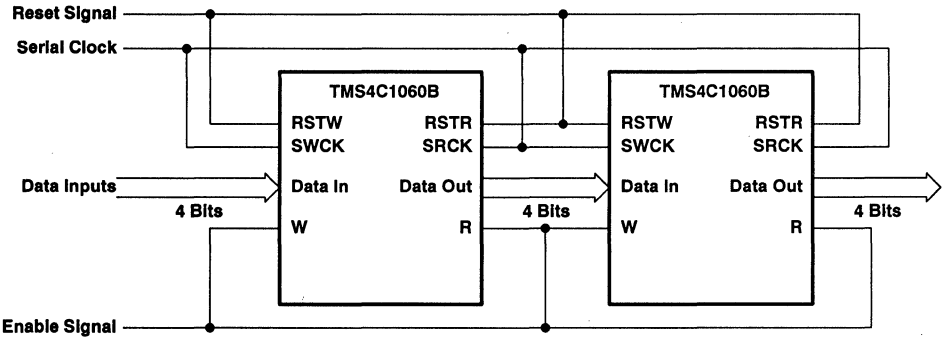


Figure 7. Cascade Operation—Signal Connections

PARAMETER MEASUREMENT INFORMATION

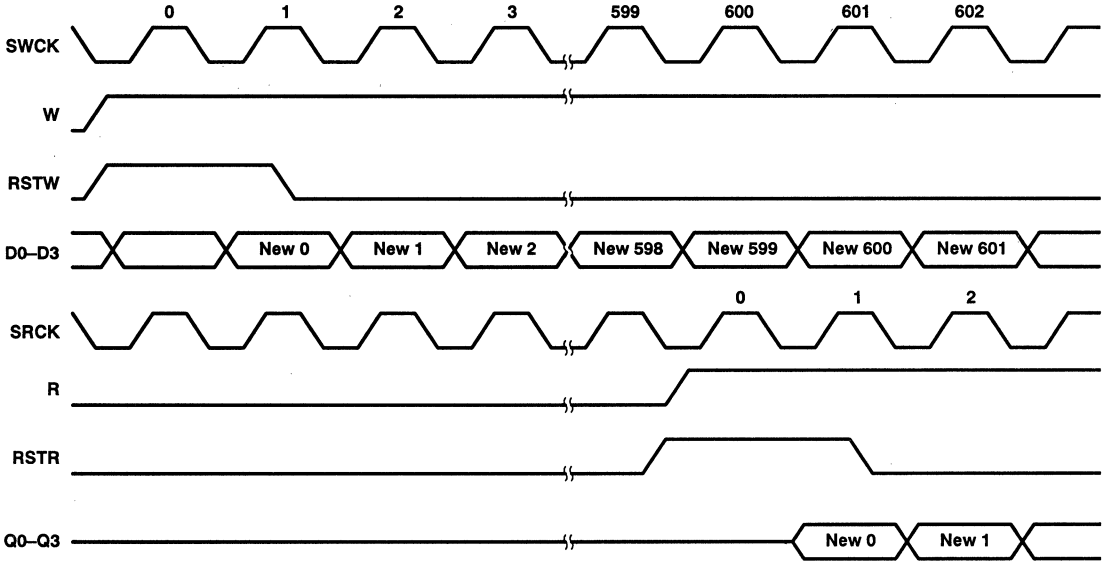


Figure 8. New Data Access Mode

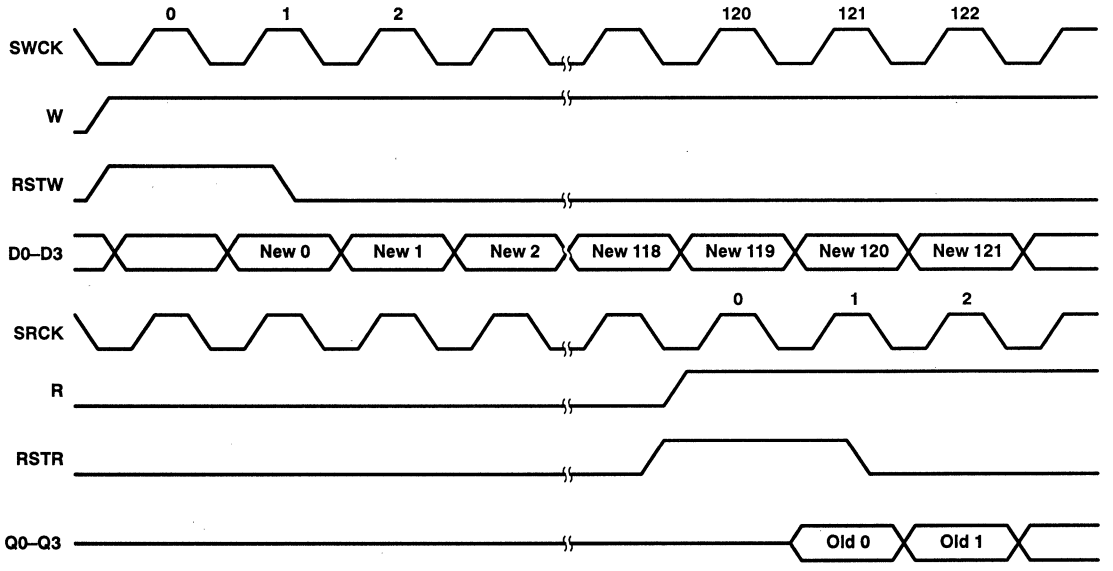


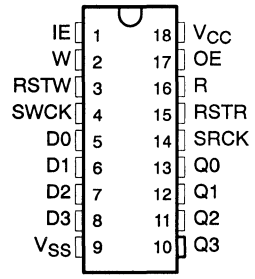
Figure 9. Old Data Access Mode

- **Organization . . . 262 264 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Fast FIFO (First-In First-Out) Operation**
  - **Full Word Continuous Read/Write**
  - **Asynchronous Read/Write**
- **Fully Static (Refresh Free)**
- **High Speed Read/Write Operation**
- **Cascade Connection Capability**
- **Max Access / Min Cycle Time**

	ACCESS TIME (MAX)	READ CYCLE TIME (MIN)	WRITE CYCLE TIME (MIN)
TMS4C1070B-30	25 ns	30 ns	30 ns
TMS4C1070B-40	30 ns	40 ns	40 ns
TMS4C1070B-60	50 ns	60 ns	60 ns

- **Write Mask Function By Input Enable**
- **Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)**
- **18-Pin 300-MIL DIP**
- **Texas Instruments EPIC™ (Enhanced Performance Implanted CMOS) Technology**
- **Operating Free-Air Temperature 0°C to 70°C**
- **1-Megabit DRAM Compatible Process Technology**
- **Fully Compatible With TMS4C1070**

N PACKAGE†
(TOP VIEW)



† The package is shown for pinout reference only.

PIN NOMENCLATURE	
D0–D3	Data Inputs
Q0–Q3	Data Outputs
R	Read Enable
OE	Output Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
W	Write Enable
IE	Input Enable
V_{CC}	5-V Power Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS4C1070B is a Field Memory (FMEM) that reads and writes data exclusively through serial ports, 4 bits wide. Maximum storage capacity is 262 264 words by four bits each. Addressing is controlled by write address and read address pointers which must be reset to zero before memory access begins.

Read and write access may occur asynchronously. When read access is delayed ralative to write access, the TMS4C1070B functions like a First-In First-Out (FIFO) register. The amount of delay determines the length of the FIFO register.

Unlike a conventional FIFO register, data may be read as many times as desired after it is written into the storage array.

Minimum delay between writing into the device and reading out data is 600 SWCK cycles. Maximum delay is one full field (262 264 write cycles).

The TMS4C1070B employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

Dynamic data storage cells are employed as the main data memory to achieve high density. Self-refresh and arbitration logic is implemented in the TMS4C1070B, supplying a refresh-free system. This logic prevents any conflict between data-saving/data-loading/memory-refresh requests.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The TMS4C1070B is similar in operation and functionality to the TMS4C1050B. Compared to TMS4C1050B, the TMS4C1070B has the following additional functions and features:

a. The input enable function of the TMS4C1070B allows the user to write into selected locations of the memory only, leaving the rest of the contents unchanged.
b. The write address counting scheme of the TMS4C1070B has been modified relative to its read address counting scheme to allow easy cascading of several memory devices.

If the memory is to be used as a delay element only, it is not necessary to reset the address pointers. After the memory has been completely filled and the write address pointer reaches its maximum value, it will wrap around again to the first address of the main array (address 120). The read address pointer behaves in the same manner.

The TMS4C1070B is offered in a 18-pin dual-in-line plastic package (N suffix). This device is characterized for operation from 0°C to 70°C.

operation

write operation

The write operation is controlled by W, IE and two clocks, SWCK and RSTW. The write operation is accomplished by cycling SWCK and holding W and IE high after the write address pointer reset operation (RSTW). Each write operation, beginning with RSTW, must contain at least 120 write cycles (SWCK cycles while W is high).

To transfer the last data written into the device (which at that time is still stored in the write line buffer) to the memory array, an RSTW operation is required after the last SWCK cycle.

reset write (RSTW)

The first positive transition of SWCK after RSTW going high resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. The state of W may be high or low during any reset operation. Before RSTW may be brought high again for a further reset operation, it must have been low for at least two SWCK cycles.

data inputs (D0–D3) and write clock (SWCK)

The SWCK input latches the data inputs on chip when W and IE are high and also increments the internal write address pointer, when W is high, regardless of the state of IE. Data-in setup and hold times [$t_{su(D)}$, $t_{h(D)}$] are referenced to the rising edge of SWCK.

write enable (W)

W is used as a data-in enable/diasble. A logic high on the W input enables the input, and a logic low disables the input and holds the internal write address pointer.

Note that W setup and hold times are referenced to the rising edge of SWCK.

ADVANCE INFORMATION

input enable (IE)

IE is used to enable/disable writing into memory. A logic high on the IE enables writing, and a logic low disables writing. The internal write address pointer is always incremented by cycling SWCK when W is high, regardless of IE logic level. Note that IE setup and hold times are referenced to the rising edge of SWCK.

Write Cycle Function Table

SWCK RISING EDGE			
W	IE	Write Address Pointer	D0–D3
H	H	Address Pointer Increment	Store Data
H	L		Not Store
L	X	Address Pointer Stop	Not Store

X = Don't Care

read operation

The read operation is controlled by four clocks, SRCK, RSTR, R, and OE. It is accomplished by cycling SRCK and holding R and OE high after a read address pointer reset operation (RSTR). Each read operation,which begins with RSTR, must contain at least 120 read cycles (SRCK cycles while R is high).

Read Cycle Function Table

SRCK RISING EDGE			
R	OE	Read Address Pointer	Q0–Q3
H	H	Address Pointer Increment	Data Out
H	L		HI-Z
L	H	Address Pointer Stop	Data Out
L	L		HI-Z

reset read (RSTR)

The first positive transition of SRCK after RSTR goes high resets the read address pointers to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. The state of R may be high or low during any reset operation. Before RSTR may be brought high again for a further reset operation, it must have been low for at least two SRCK cycles.

data outputs (Q0–Q3) and read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R and OE are high during a read operation. The SRCK input increments the internal read address pointer when R is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval (t_{AC}) that begins with the positive transition of SRCK. Output valid time [$t_{V(OUT)}$] is referenced to the rising edge of SRCK in the next cycle.

read enable (R)

R is used to enable/disable incrementing the internal read address pointer. A logic high on the R input enables pointer incrementing by the next following positive SRCK transition, and a logic low disables pointer incrementing. R setup and hold times are referenced to the rising edge of SRCK. The data at the outputs will be the data read out during the SRCK cycle prior to R going low.

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output enable (OE)

OE is used as a data out enable/disable. A logic high on the OE input enables the output, and a logic low disables the output. The internal read address pointer is always incremented by cycling SRCK when R is high, regardless of OE logic level. The outputs will be clocked into the high-impedance (floating) state by the next positive SRCK transition following OE being low. The disable time [$t_{dis(CK)}$] applies. The outputs will be enabled by the next positive SRCK transition following OE being high. The enable time [$t_{en(CK)}$] applies.

power-up and initialization

When powering up, the device is designed to begin proper operation after at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. This time is defined as $t_{POWER-OK}$. While it is acceptable to start the initialization sequence during V_{CC} ramp-up (before $t_{POWER-OK}$), the full sequence must be repeated at least once after $t_{POWER-OK}$. The required initialization sequence for the write pointers is as follows:

At least one SWCK clock cycle, followed by a reset write operation, followed by at least 130 dummy write operations with W and IE at high level, followed by another reset write operation. All timing parameters must be within specifications for the initialization sequence. After initialization, the write address pointers are set to zero, and writing may begin.

The initialization sequence for the read pointers is analogous to write pointer initialization, and must be performed at least once after $t_{POWER-OK}$.

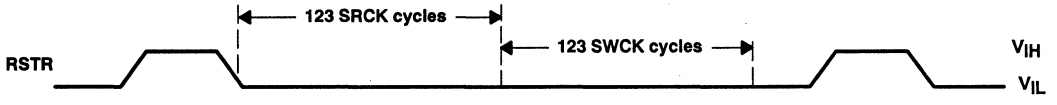
old/new data access

There must be a minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 120 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called old data.

In order to read out new data, i.e., the second field written in, the delay between RSTW operation and RSTR operation must be at least 600 SWCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined; it may be old data, or new data, or a combination of old and new data. Such a timing should be avoided.

An additional condition must be obeyed to read out new data when the SRCK frequency is much lower than SWCK (SRCK cycle time > 4 x SWCK cycle time). In this special case, at least 123 SRCK cycles followed by 123 SWCK cycles are necessary before the next RSTR is issued and the reading of new data may begin.



cascade operation

The TMS4C1070B has been designed to allow easy cascading of several memory devices in order to obtain a higher storage depth or a longer delay than can be achieved with only one memory device. See the interconnection diagram on page 14 for details.

As illustrated in the timing diagram on page 13, Figure 9, the positive SRCK/SWCK edge at the beginning of a clock cycle serves to initiate read-out, whereas writing in is initiated by the positive SWCK/SRCK edge at the end of a clock cycle. This differs from the functionality of the TMS4C1050B, in which both the read-out and the write-in are initiated at the beginning of a clock cycle.

Internal operation

writing into memory

The first 120 words of data following the initial RSTW operation after power-up are written into a cache line buffer, (A) initially, and will never be stored elsewhere, to allow read-out of data later without the delay involved in retrieving it from the main memory array.

Starting from address 120, data is written into the write line buffer, top block, until this block (256 words long) is full. Further writing then occurs to the bottom block of the write line buffer, while the top block is transferred to the main memory array. By the time the bottom block is full, the top block has been transferred to memory and can be used again to receive new incoming data. The channelling of input data into the top or bottom block is controlled internally by the device and is transparent to the user.

After the 120-word long cache buffer has been filled with incoming data, the input line selector switches the connection of the input port over to the B line buffer, to assure that the next field of data which will arrive later, after a subsequent RSTW operation, does not over-write the content of the cache buffer. Each subsequent filling of the cache buffer toggles the connection of the input port between the A and the B line buffers with the 121st SWCK pulse. The A and B line buffers, as well as the input line selector, are static registers.

The connection of the output port will also be toggled between the A and B line buffers by the 121st SWCK pulse, providing no read operation from a cache buffer is in progress at this time. The output port will always be connected to the line buffer opposite to the one connected to the input port. In case a read operation from a cache buffer is in progress when the 121st SWCK occurs, the toggling of the output port connection will be delayed until the cache buffer has been read out completely.

The requirement stated on page 2 that each write operation must contain at least 120 active SWCK cycles, exists in order to assure that the toggling of the input and the output ports between the A line buffer and the B line buffer functions without errors as described above.

The serial write pointer stores the (column) address of the last input data word received, while the write counter stores the row address.

After the last word of a full write cycle has been latched in (with a positive transition of the SWCK clock), the write line buffer most likely will be partially filled without having been transferred to the main memory array. To assure that the information contained in the write line buffer is stored and can not be lost, it is required that an RSTW operation be performed when write clocking has stopped.

In addition to transferring the partially filled write line buffer into the main memory array, this RSTW operation will also reset the write address (serial write pointer) to zero. Regardless of how much later a new write cycle starts, it is not necessary to perform another RSTW operation again at that time.

reading from memory

After an RSTR operation, data from the main memory array (starting at address 120) will be transferred to the read line buffer. Because this transfer requires some time, the first 120 words will be read out of the A or B line buffer, where they had been previously stored (see writing into memory).

If the first RSTR operation occurs after the first RSTW operation but before the second RSTW operation, read access will be to the same buffer that data had been written into during the first write cycle. Thus old data will be read out.

If this delay is less than 120 SWCK cycles, data will be read out from the line buffer that it was written into during the previous write cycle, i.e. old data will be read out. A delay of less than 120 SWCK cycles will also assure that all following data words are old data, because replacement of old data by new data in the main memory array will occur later than the respective read access to each address in the array.

If this delay is more than 600 SWCK cycles, then the data will be read out from the line buffer that it was written into during the current write cycle, i.e. new data will be read out. A delay of more than 600 SWCK cycles will also assure that all following data words are new data, because replacement of old data by new data in the main memory array will occur before the respective read access to each address in the array.

If this delay is more than 120 but less than 600 SWCK cycles, then the data read out can be either old or new or a mixture of old and new data, because it cannot be predicted accurately, whether a word accessed for reading has already been replaced by new data or not. Such a situation should be avoided.

After the first 120 words are read out of the A or B line buffer, read transfer from the main memory array to the read line buffer is finished, and subsequent reading will occur from this buffer. Similar to the write operation, while one half of this buffer is being read out, the other half will be filled again by a new read transfer from the main memory array.

The serial read pointer stores the (column) address of the last data word read out, while the read counter stores the row address.

self-refresh and arbitration logic

The self-refresh and arbitration logic will keep the main memory information refreshed automatically without requiring any user action, control the address pointers for both read and write, and control the flow of information both into and out of the main memory.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Supply voltage range on V_{CC} ..... 0 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL} = – 1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4C1070B-30		'4C1070B-40		'4C1070B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, OE low		±10		±10		±10	µA
I_{DD1}	Average operating current	Minimum write/read cycle, output open		50		45		35	mA
I_{DD2}	Average standby current	After 1 RSTW/RSTR cycle, W, R, OE low		10		10		10	mA

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	V_I = 0, f = 1 MHz			7	pF
C_O	Output capacitance	V_I = 0, f = 1 MHz			10	pF

† V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	'4C1070B-30		'4C1070B-40		'4C1070B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	see Note 3		25		30		50	ns
$t_{dis(CK)}$	Output disable time after SRCK high	see Note 4	4	15	4	15	4	15	ns
$t_{en(CK)}$	Output enable time after SRCK high	see Note 3	0	15	0	15	0	15	ns
$t_{v(OUT)}$	Output valid time after SRCK high	see Note 3	6		6		6		ns

NOTES: 3. The load connected to each output is a 50-pF capacitor to ground, in parallel with a 218-Ω resistor to 1.31 V. (See Figure 1.)
4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output voltage waveforms, sufficiently low load resistors and capacitors have to be used, and the RC time constants of the load have to be taken into account.

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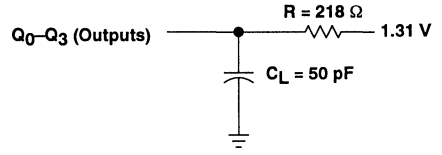

Figure 1. Load Circuit for Timing Parameters

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Notes 5 and 6)

		'4C1070B-30		'4C1070B-40		'4C1070B-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	30		40		60		ns
$t_{c(R)}$	Read cycle time	30		40		60		ns
$t_{w(R)}$	Pulse duration, R-low	10		10		10		ns
$t_{w(W)}$	Pulse duration, W-low	10		10		10		ns
$t_{w(IE)}$	Pulse duration, IE low	10		10		10		ns
$t_{w(OE)}$	Pulse duration, OE low	10		10		10		ns
$t_{w(RH)}$	Pulse duration, SRCK high	12		17		20		ns
$t_{w(RL)}$	Pulse duration, SRCK low	12		17		20		ns
$t_{w(WH)}$	Pulse duration, SWCK high	12		17		20		ns
$t_{w(WL)}$	Pulse duration, SWCK low	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{su(RH)}$	R-high setup time before SRCK high	0		0		0		ns
$t_{su(RL)}$	R-low setup time before SRCK high	0		0		0		ns
$t_{su(WH)}$	W-high setup time before SWCK high	0		0		0		ns
$t_{su(WL)}$	W-low setup time before SWCK high	0		0		0		ns
$t_{su(IEH)}$	IE high setup time before SWCK high	0		0		0		ns
$t_{su(IEL)}$	IE low setup time before SWCK high	0		0		0		ns
$t_{su(OEH)}$	OE high setup time before SRCK high	0		0		0		ns
$t_{su(OEL)}$	OE low setup time before SRCK high	0		0		0		ns
$t_{su(RSTR)}$	RSTR setup time before SRCK high	3		3		3		ns
$t_{su(RSTW)}$	RSTW setup time before SWCK high	3		3		3		ns
$t_{h(D)}$	Data hold time after SWCK high	6		6		6		ns
$t_{h(R)}$	R hold time after SRCK high	6		6		6		ns
$t_{h(W)}$	W hold time after SWCK high	6		6		6		ns
$t_{h(IE)}$	IE hold time after SWCK high	6		6		6		ns
$t_{h(OE)}$	OE hold time after SRCK high	6		6		6		ns
$t_{h(RSTR)}$	RSTR hold time after SRCK high	6		6		6		ns
$t_{h(RSTW)}$	RSTW hold time after SWCK high	6		6		6		ns
t_T	Input transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IH} (MIN) = 2.4 V and V_{IL} (MAX) = 0.8 V. t_T is measured between V_{IH} (MIN) and V_{IL} (MAX).
6. All cycle times assume t_T = 3 ns.

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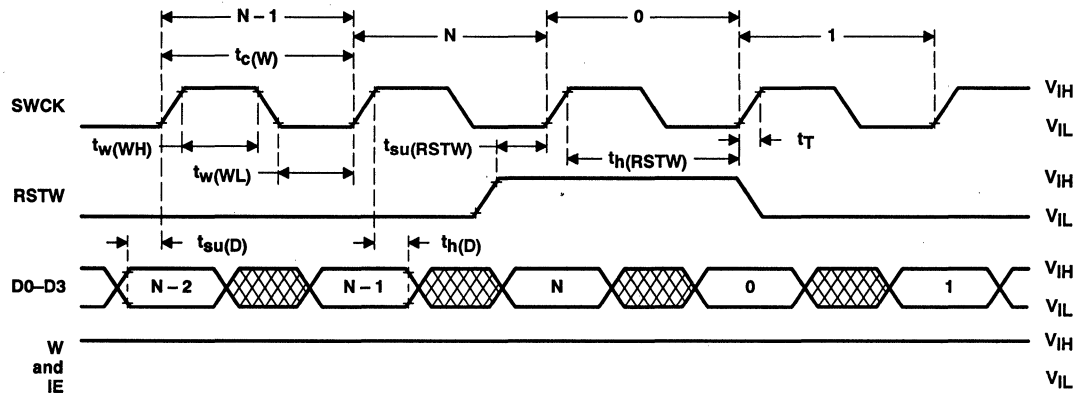

Figure 2. Write Cycle Timing (Reset Write)

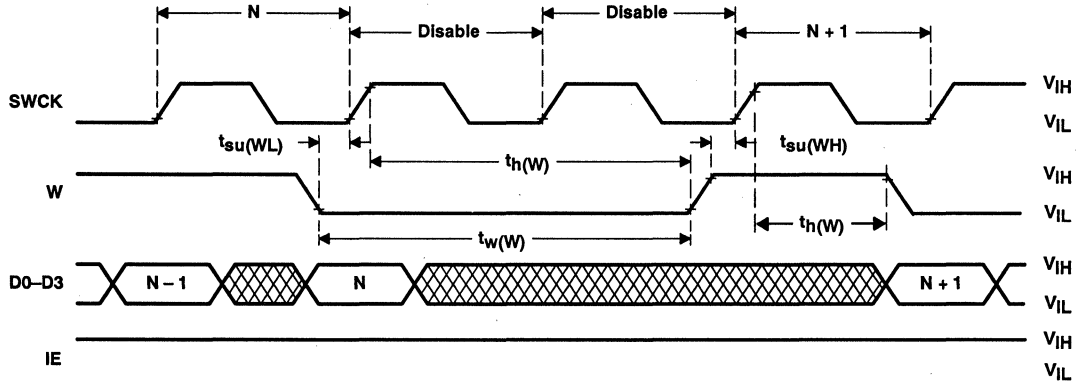

Figure 3. Write Cycle Timing (Write Enable)

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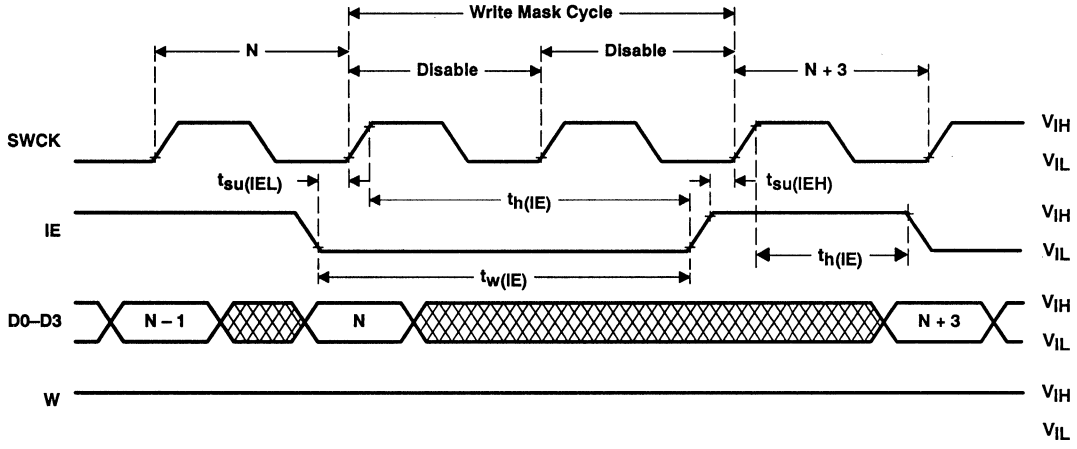

Figure 4. Write Cycle Timing (Input Enable = Write Mask Operation)

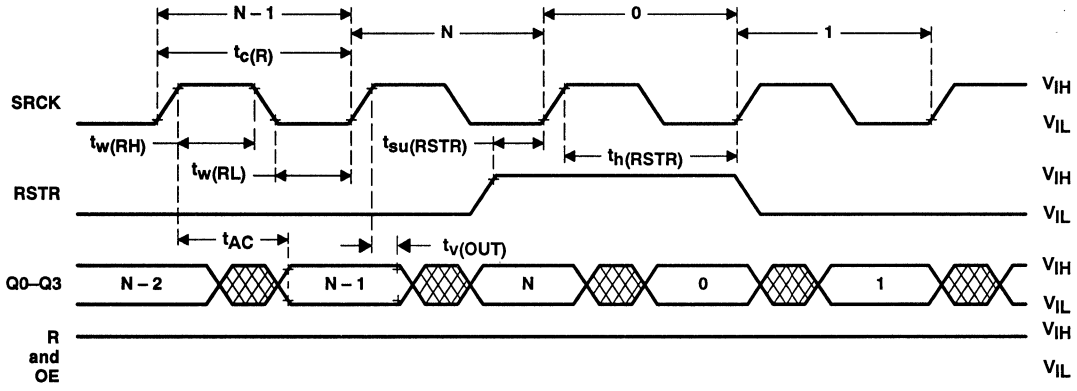

Figure 5. Read Cycle Timing (Reset Read)

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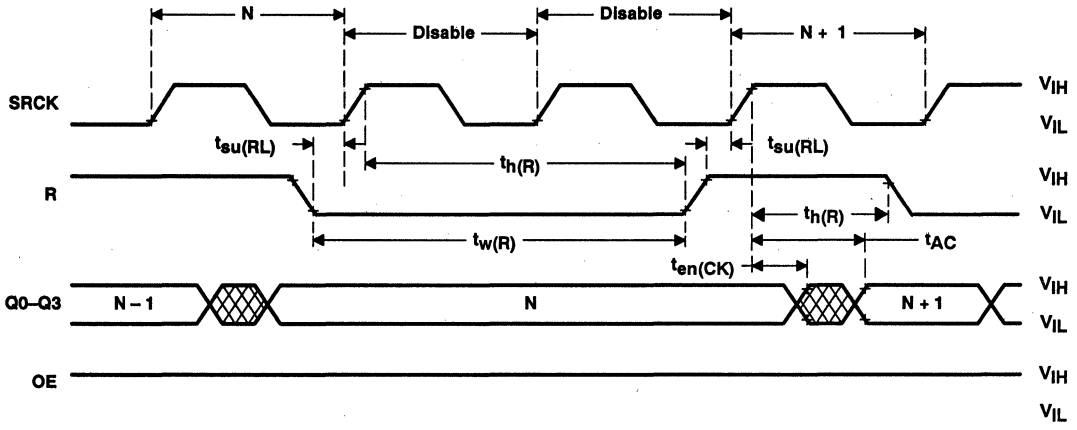

Figure 6. Read Cycle Timing (Read Enable)

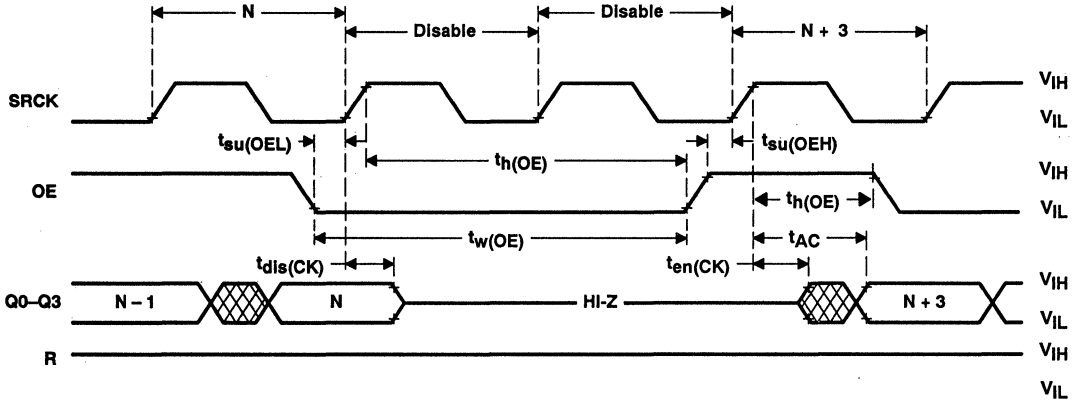

Figure 7. Read Cycle Timing (Output Enable)

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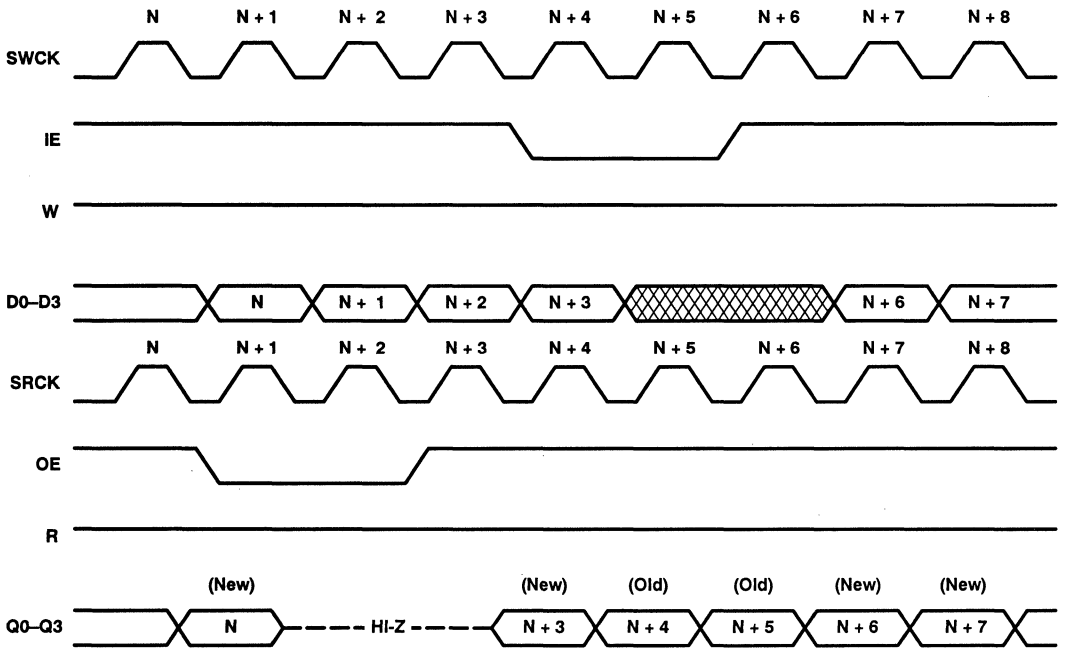

Figure 8. Write Mask Operation

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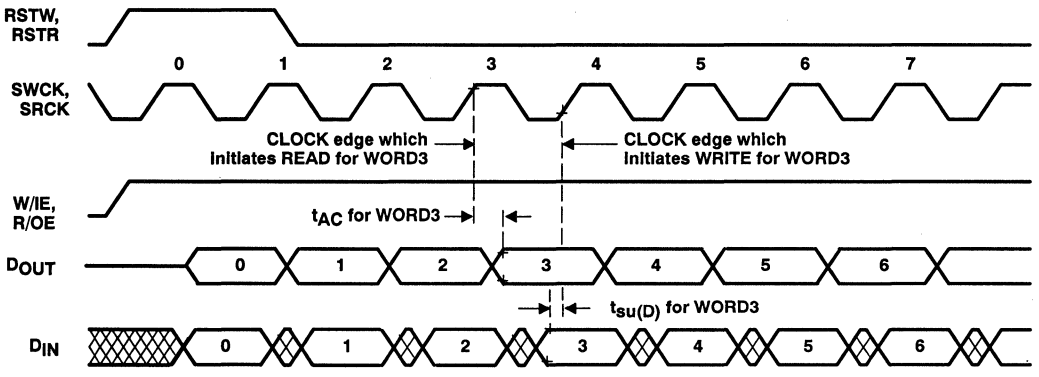

Figure 9. Cascade Mode

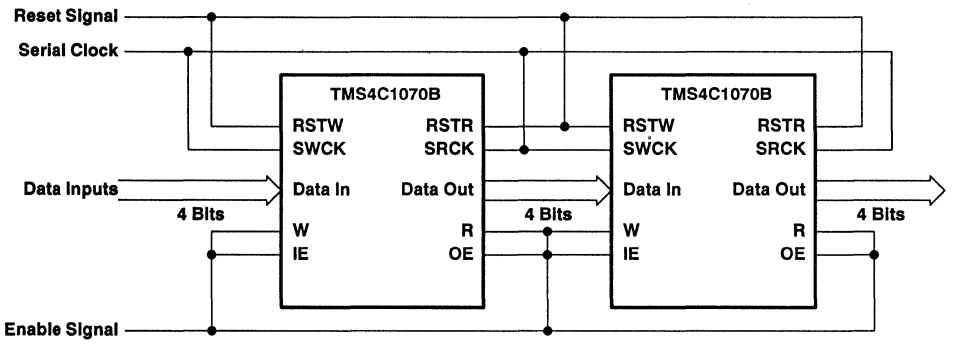

Figure 10. Cascade Operation—Signal Connections

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PARAMETER MEASURMENT INFORMATION

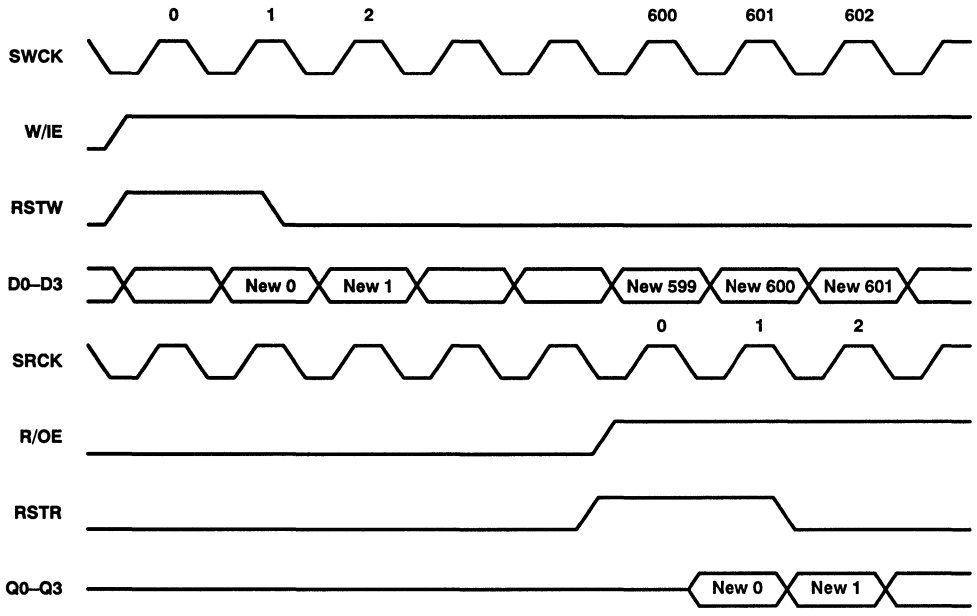

Figure 11. New Data Access Mode

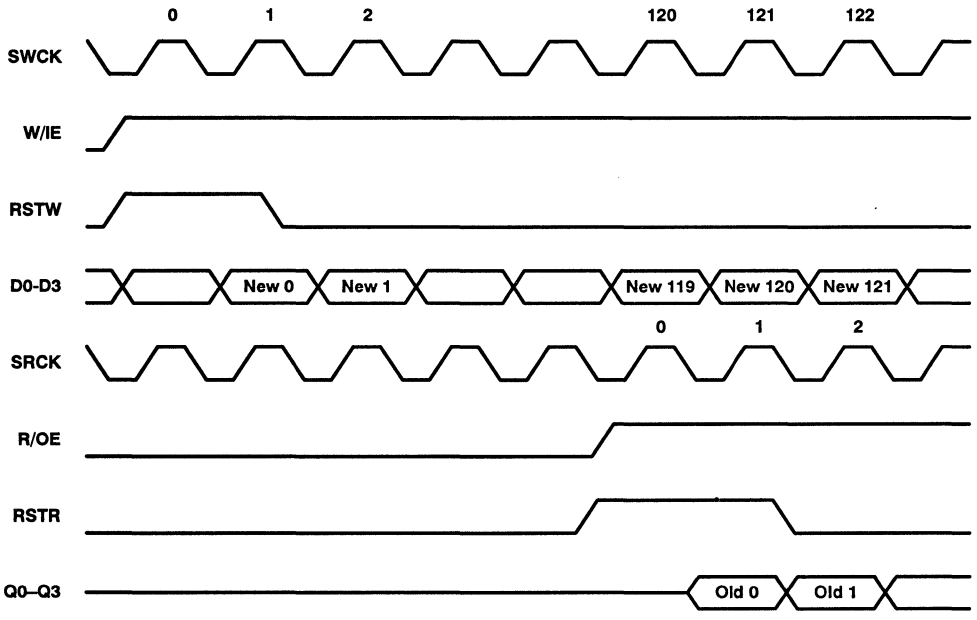

Figure 12. Old Data Access Mode

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CMS68F256	262 144-bit	(256K x 8 or 128K x 16) Flash Memory Card	8-45
CMS68F512	524 288-bit	(512K x 8 or 256K x 16) Flash Memory Card	8-45
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CMS209	1 048 576-bit	(64K x 16) OTP PROM Memory Card	8-65
CMS210	2 097 152-bit	(128K x 16) OTP PROM Memory Card	8-65
CMS213	524 288-bit	(64K x 8) OTP PROM Memory Card	8-65
CMS214	1 048 576-bit	(128K x 8) OTP PROM Memory Card	8-65
CMS216	2 097 152-bit	(256K x 8) OTP PROM Memory Card	8-65

- **Credit Card Size (85.6 mm × 54 mm × 3.4 mm)**
- **Single 5-V Power Supply (±5% Tolerance)**
- **Enhanced Page Mode Operation**
- **CMS405 – 2M × 18/2$\overline{RAS}$/2$\overline{CAS}$**
  CMS406 – 2M × 16/2$\overline{RAS}$/2$\overline{CAS}$
  CMS407 – 1M × 18/1$\overline{RAS}$/2$\overline{CAS}$
  CMS408 – 1M × 16/1$\overline{RAS}$/2$\overline{CAS}$
- **Operating Temperature . . . 0°C to 55°C**
- **Standard 60-Pin Two-Piece Connector**
- **CMOS Buffered Inputs on All Inputs Except $\overline{RAS}$ and DQ**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Performance Ranges:**

	ACCESS TIME	ACCESS TIME	READ OR WRITE CYCLE
	t_{RAC}	t_{CAC}	t_{RC}
CMS40x-7	70 ns	25 ns	130 ns
CMS40x-8	80 ns	27 ns	150 ns

description

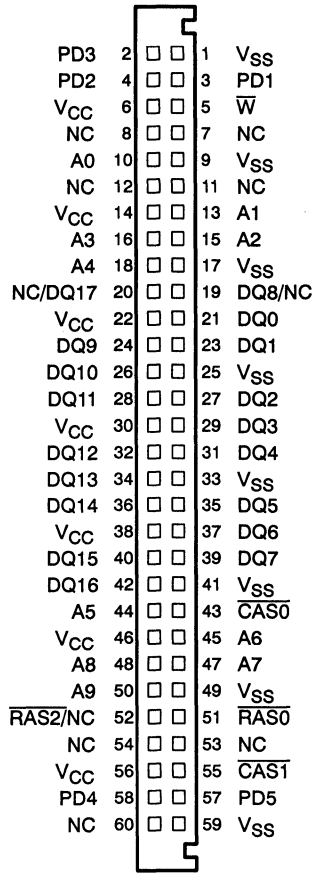
The CMS405/6/7/8 series are dynamic random-access memory cards designed to be used as internal system memory or as external add-on memory.

These cards have CMOS buffers added to the $\overline{CAS}$, $\overline{W}$, and address inputs to minimize loading caused by the module. $\overline{RAS}$ and data in/out remain compatible with Series 74 TTL.

The cards can operate in enhanced page mode. All address lines and data are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The common I/O features of the CMS405/6/7/8 dictate the use of early write cycles.

60-PIN MEMORY CARD (CONNECTOR VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$, $\overline{CAS1}$	Column-Address Strobe
DQ0–DQ17	Data Inputs/Outputs
PD1–PD5	Presence Detect
$\overline{RAS0}$, $\overline{RAS2}$	Row-Address Strobe
V_{CC}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable
NC	No Internal Connection

operation

The CMS405/6/7/8 cards are divided into separate banks of memory as shown in the functional block diagrams. Each bank is selectable using $\overline{RASx}$ and $\overline{CASx}$ as shown in the table below. $\overline{RAS0}$ and $\overline{RAS2}$ control which side of the DRAM banks are connected to the memory card DQ pins. Therefore, only one $\overline{RAS}$ signal may be active during any read or write cycle.

Table 1. Memory Bank Definition

DATA BLOCK	$\overline{RASx}$		$\overline{CASx}$
	Side 1	Side 2	
DQ0–DQ7, DQ8†	$\overline{RAS0}$	$\overline{RAS2}$	$\overline{CAS0}$
DQ9–DG16, DQ17†	$\overline{RAS0}$	$\overline{RAS2}$	$\overline{CAS1}$

† DQ8 and DQ17 are not available on CMS406 and CMS408; only side one is available on CMS407 and CMS408.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. The eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

specifications

Refresh period is extended to 16 ms. During this period, each of the 1024 rows must be strobed with $\overline{RAS}$ to retain data. The nine least significant row addresses (A0–A8) must be refreshed every 8 ms.

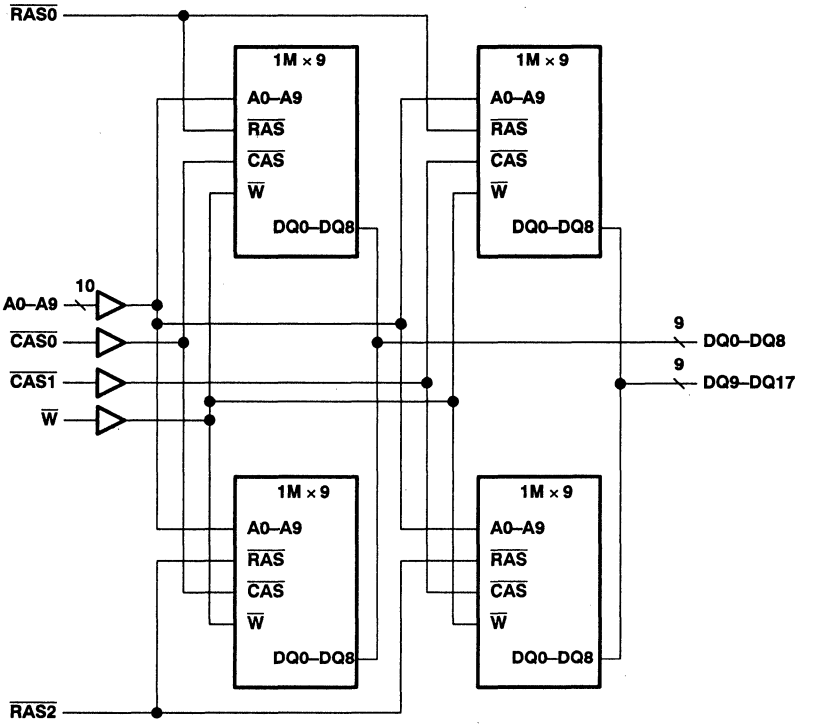
memory card components

– Meets JEDEC standard

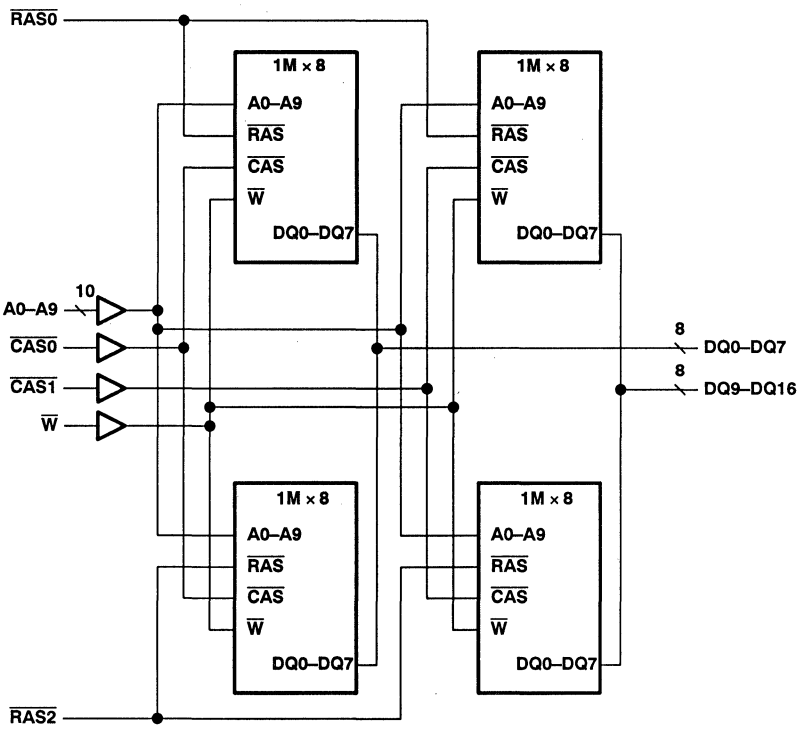
– UL approved materials

– Plugs into molex connector part number 53213-6011 or equivalent

CMS405 functional block diagram



CMS406 functional block diagram



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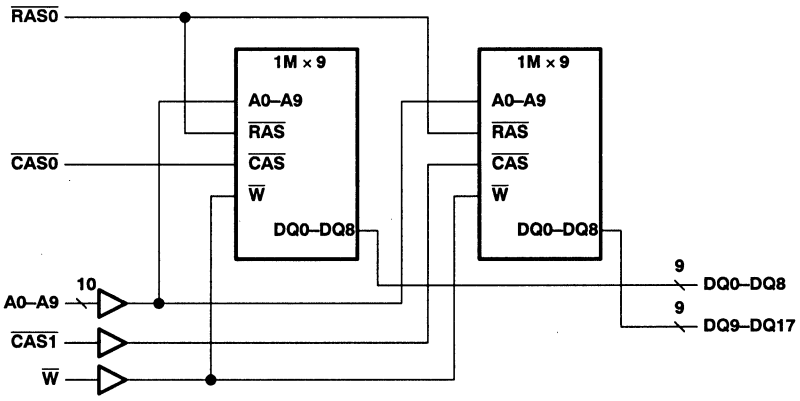
CMS407 functional block diagram



CMS408 functional block diagram

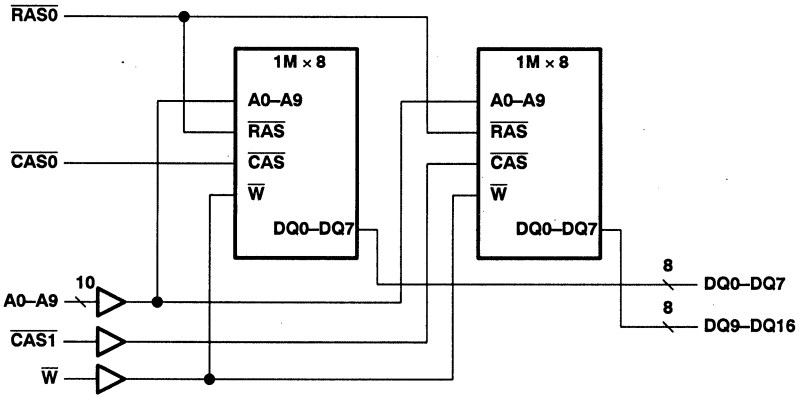


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Table 2. Pin Definition for Presence Detect

	CONFIGURATION			SPEED	
	PD1(3)	PD2(4)	PD3(2)	PD4(58)	PD5(57)
CMS405–8†	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}

† Presence detect is defined only for 80 ns version of the CMS405.

Table 3. Pin Definition

DEVICE	$\overline{RAS2}$/NC (52)	DQ8/NC (19)	DQ17/NC (20)
CMS405	$\overline{RAS2}$	DQ8	DQ17
CMS406	$\overline{RAS2}$	NC	NC
CMS407	NC	DQ8	DQ17
CMS408	NC	NC	NC

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range on any pin (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range on V_{CC} ..... −0.5 V to 6 V
Short circuit output current ..... 50 mA
Power dissipation (CMS405) ..... 11.5 W
Power dissipation (CMS406) ..... 9.5 W
Power dissipation (CMS407) ..... 6.5 W
Power dissipation (CMS408) ..... 5.5 W
Operating free-air temperature ..... 0°C to 55°C
Storage temperature ..... −40 °C to 85 °C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{CAS}$, $\overline{W}$, address lines	0.7 V_{CC}			V
		$\overline{RAS}$ and DQ lines	2.4		6.5	
V_{IL}	Low-level input voltage (see Note 2)	$\overline{CAS}$, $\overline{W}$, address lines			0.3 V_{CC}	V
		$\overline{RAS}$ and DQ lines	−1		0.8	
T_A	Operating free air temperature		0		55	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS405			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RASx}$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±60	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CASx}$ high			±20	µA

electrical characteristics over full range of recommended operating conditions (see Note 3)

PARAMETER		TEST CONDITIONS	CMS405-7		CMS405-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active at any time.		602		542	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All other signals stable, V_{CC} = 5.25 V.		25		25	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high.		1130		1010	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active at any time, $\overline{RAS}$ low, $\overline{CAS}$ cycling.		542		482	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS405		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		42	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins (DQ0–DQ7, DQ9–DQ16)		14	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins (DQ8, DQ17)		24	pF

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS406			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CAS}x$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RAS}x$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±40	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CAS}x$ high			±20	µA

electrical characteristics over full range of recommended operating conditions (see Note 3)

PARAMETER		TEST CONDITIONS	CMS406-7		CMS406-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active at any time.		418		378	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high. All other signals stable, V_{CC} = 5.25 V.		17		17	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high.		770		690	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active at any time, $\overline{RAS}$ low, $\overline{CAS}$ cycling.		378		338	mA

NOTE 3. $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS406		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		28	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS407			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CAS}x$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RAS}x$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±60	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CAS}x$ high			±10	µA

electrical characteristics over full range of recommended operating conditions (see Note 3)

PARAMETER		TEST CONDITIONS	CMS407-7		CMS407-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active at any time.		590		530	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All other signals stable, V_{CC} = 5.25 V.		13		13	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high.		590		530	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active at any time, $\overline{RAS}$ low, $\overline{CAS}$ cycling.		530		470	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS407		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		42	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins (DQ0–DQ7, DQ9–DQ16)		14	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins (DQ8, DQ17)		12	pF

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS408			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RASx}$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±40	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CASx}$ high			±10	µA

electrical characteristics over full range of recommended operating conditions (see Note 3)

PARAMETER		TEST CONDITIONS	CMS408-7		CMS408-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active any time.		410		370	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high. All other signals stable, V_{CC} = 5.25 V.		9		9	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high.		410		370	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle. Only one $\overline{RAS}$ active any time, $\overline{RAS}$ low, $\overline{CAS}$ cycling.		370		330	mA

NOTE 3. $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS408		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		28	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

A low-power battery-backup refresh mode is available. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 µs, holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all other input levels need to be kept stable at CMOS input levels.

All values remain the same as the standard memory card except the following:

PARAMETER		TEST CONDITIONS	CMS405L	CMS406L	CMS407L	CMS408L
I_{CC2}	Standby current	$\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = V_{CC} - 0.2$ V, $V_{IL} = 0$ V All other signals stable at V_{IH} or V_{IL}	5 mA	4 mA	3 mA	2 mA
I_{CC10}	Battery backup current	$t_{RC} = 125$ µs, $t_{RAS} < 1$ µs, $V_{IH} = V_{CC} - 0.2$ V, $V_{IL} = 0$ V All other signals stable at V_{IH} or V_{IL}	7 mA	5 mA	4 mA	3 mA
t_{REF}	Refresh	1024 Cycle	128 ms	128 ms	128 ms	128 ms

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		CMS40x-7		CMS40x-8		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		25		27	ns
t_{CAA}	Access time from column-address		42		47	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{CAP}	Access time from column precharge		47		52	ns
t_{CLZ}	$\overline{CAS}$ low to output in low Z	0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	25	0	27	ns

NOTE 4: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		CMS40x-7		CMS40x-8		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{PC}	Page mode read or write cycle time (see Note 5)	52		57		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	25	10 000	27	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high	50		60		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low	70	10 000	80	10 000	ns
t_{RASP}	Page mode, pulse duration, $\overline{RAS}$ low	70	100 000	80	100 000	ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	7		7		ns
t_{DS}	Data setup time before $\overline{CAS}$ low	0		0		ns

Continued next page

NOTE 5: To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

	PARAMETER	CMS40x-7		CMS40x-8		UNIT
		MIN	MAX	MIN	MAX	
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{WCS}	$\overline{W}$ low setup before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$ low setup before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$ low setup before $\overline{RAS}$ high	25		27		ns
t_{WSR}	$\overline{W}$ high setup ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	17		17		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		12		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see note 6)	55		60		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	55		60		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 7)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 7)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 6)	55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	7		7		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		27		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 8)	20	47	22	53	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 8)	15	28	17	33	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	42		47		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	17		17		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		ns
t_{REF}	Refresh time interval (distributed)		16		16	ns
t_T	Transition time (see Note 10)	3	50	3	50	ns

NOTES: 6. The minimum value is measured when t_{RCD} is set to t_{RCD} (min) as a reference.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. Maximum values specified to assure access times.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. All cycle times assume t_T = 5 ns.

- **Credit Card Size (85.6 mm × 54 mm × 3.4 mm)**
- **Single 5-V Power Supply (±5% Tolerance)**
- **Enhanced Page Mode Operation**
- **CMS409 – 4M × 18/1$\overline{RAS}$/2$\overline{CAS}$**
  CMS410 – 4M × 16/1$\overline{RAS}$/2$\overline{CAS}$
- **Operating Temperature 0°C to 55°C**
- **Standard 60-Pin Two-Piece Connector**
- **CMOS Buffered Inputs on All Inputs Except $\overline{RAS}$ and DQ**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{CAC}	READ OR WRITE CYCLE t_{RC}
CMS4xx-7	70 ns	25 ns	130 ns
CMS4xx-8	80 ns	27 ns	150 ns

description

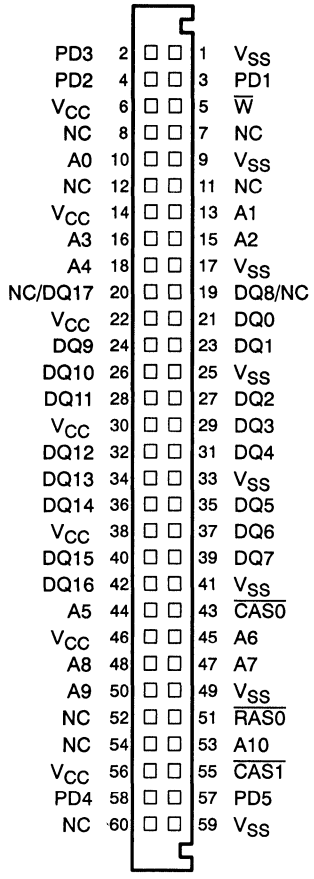
The CMS409/10 series are dynamic random-access memory cards designed to be used as internal system memory or as external add-on memory.

These cards have CMOS buffers added to the $\overline{CAS}$, $\overline{W}$, and address inputs to minimize loading caused by the module. $\overline{RAS}$ and data in/out remain compatible with Series 74 TTL.

The cards can operate in enhanced page mode. All address lines and data are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The common I/O features of the CMS409/10 dictate the use of early write cycles.

60-PIN MEMORY CARD (CONNECTOR VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$, $\overline{CAS1}$	Column-Address Strobe
DQ0–DQ17	Data Inputs/Outputs
PD1–PD5	Presence Detect
$\overline{RAS0}$	Row-Address Strobe
V_{CC}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable
NC	No Internal Connection

operation

The CMS409/10 cards are divided into separate banks of memory as shown in the functional block diagrams. Each bank is selectable using $\overline{CASx}$ as shown in the table below.

Table 1. Memory Bank Definition

DATA BLOCK	$\overline{RAS}$	$\overline{CASx}$
DQ0–DQ7, DQ8†	$\overline{RAS0}$	$\overline{CAS0}$
DQ9–DQ16, DQ17†	$\overline{RAS0}$	$\overline{CAS1}$

† DQ8 and DQ17 are not available on CMS410.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. The eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

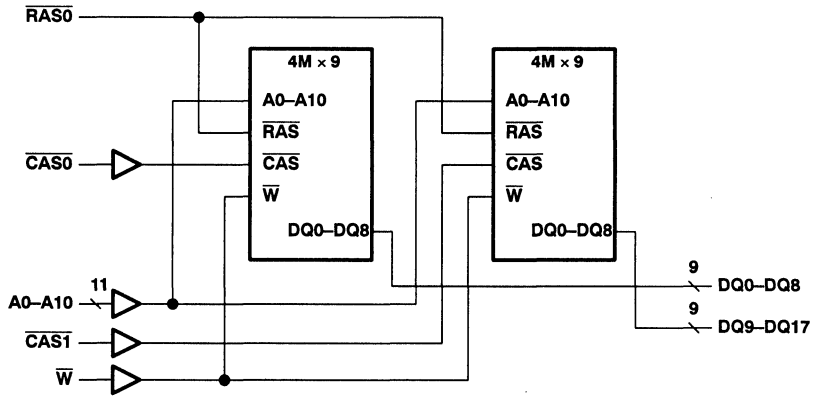
specifications

Refresh period is extended to 16 ms. During this period, each of the 1024 rows selected by A0–A9 must be strobed with $\overline{RAS}$ to retain data.

memory card components

- Meets JEDEC standard
- UL approved materials
- Plugs into molex connector part number 53213-6011 or equivalent

CMS409 functional block diagram



CMS410 functional block diagram

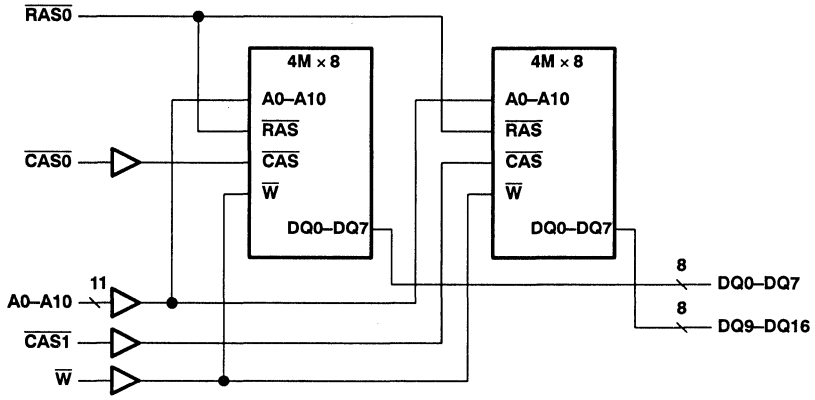


Table 2. Pin Definition

DEVICE	DQ8/NC (19)	DQ17/NC (20)
CMS409	DQ8	DQ17
CMS410	NC	NC

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range on V_{CC} ..... −0.5 V to 6 V
Short circuit output current ..... 50 mA
Power dissipation (CMS409) ..... 20 W
Power dissipation (CMS410) ..... 18 W
Operating free-air temperature ..... 0°C to 55°C
Storage temperature ..... −40 °C to 85 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{CAS}$, $\overline{W}$, address lines	0.7 V_{CC}			
		$\overline{RAS}$ and DQ lines	2.4		6.5	
V_{IL}	Low-level input voltage (See Note 2)	$\overline{CAS}$, $\overline{W}$, address lines			0.3 V_{CC}	
		$\overline{RAS}$ and DQ lines	−1		0.8	
T_A	Operating free-air temperature		0		55	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS409			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RASx}$ (leakage)	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±180	µA
I_O	Output current (leakage)	V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{CASx}$ high			±20	µA

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS409-7		CMS409-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle (see Note 3).		1670		1490	mA
I_{CC2}	Standby current	V_{CC} = 5.25 V, After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All other signals stable (see Note 3).		37		37	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3).		1670		1490	mA
I_{CC4}	Average page current	V_{CC} = 5.25 V, t_{PC} = minimum, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3).		1490		1310	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS409		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		126	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS410			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RASx}$ (leakage)	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±160	µA
I_O	Output current (leakage)	V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{CASx}$ high			±20	µA

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS410-7		CMS410-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle (see Note 3).		1490		1330	mA
I_{CC2}	Standby current	V_{CC} = 5.25 V After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high. All other signals stable, (see Note 3).		33		33	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3).		1490		1330	mA
I_{CC4}	Average page current	V_{CC} = 5.25 V, t_{PC} = minimum, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3).		1330		1170	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS410		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		112	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

A low-power, battery-backup refresh mode is available. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of125 μs, while holding $\overline{RAS}$ low for less than 1 μs. To minimize current consumption, all other input levels need to be kept stable at CMOS input levels.

All values remain the same as the standard memory card except those listed in the following table:

PARAMETER		TEST CONDITIONS	CMS409L	CMS410L
I_{CC2}	Standby current	$\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = V_{CC} - 0.2$, V, $V_{IL} = 0$ V All other signals stable at V_{IH} or V_{IL}	7 mA	6 mA
I_{CC10}	Battery backup current	t_{RC} = 125 μs, t_{RAS} < 1 μs, $V_{IH} = V_{CC}$–0.2 V, V_{IL} = 0 V All other signals stable at V_{IH} or V_{IL}	10 mA	9 mA
t_{REF}	Refresh	1024 cycle	128 ms	128 ms

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		CMS4xx-7		CMS4xx-8		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		25		27	ns
t_{CAA}	Access time from column-address		42		47	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{CAP}	Access time form column precharge		47		52	ns
t_{CLZ}	$\overline{CAS}$ low to output in low Z	0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	25	0	27	ns

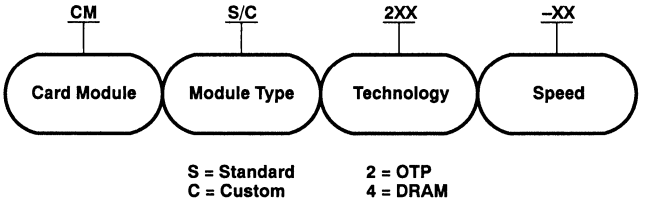
NOTE 4: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		CMS4xx-7		CMS4xx-8		
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{PC}	Page mode read or write cycle time (see Note 5)	52		57		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	25	10 000	27	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high	50		60		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low	70	10 000	80	10 000	ns
t_{RASP}	Page mode, pulse duration, $\overline{RAS}$ low	70	100 000	80	100 000	ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	7		7		ns
t_{DS}	Data setup time before $\overline{CAS}$ low	0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{WCS}	$\overline{W}$-low setup before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$-low setup before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$-low setup before $\overline{RAS}$ high	25		27		ns
t_{WSR}	$\overline{W}$-high setup ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	17		17		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see note 6)	55		60		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	55		60		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 7)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 7)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 6)	55		60		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	7		7		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		27		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 8)	20	47	22	53	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 8)	15	28	15	33	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	42		47		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	17		17		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		ns
t_{REF}	Refresh time interval		16		16	ns
t_T	Transition time (see Note 10)	3	50	3	50	ns

NOTES: 5. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns..
6. The minimum value is measured when t_{RCD} is set to t_{RCD}(min) as a reference.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. Maximum values specified to assure access times.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. All cycle times assume t_T = 5 ns.

TI memory card nomenclature



- **Credit Card Size (85.6 mm × 54 mm × 3.4 mm)**
- **Single 5-V Power Supply (±5% Tolerance)**
- **Enhanced Page Mode Operation**
- **CMS88D8MB36 – 2M × 36/4$\overline{RAS}$/4$\overline{CAS}$**
  CMS88D4MB36 – 1M × 36/2$\overline{RAS}$/4$\overline{CAS}$
- **Operating Temperature . . . 0°C to 55°C**
- **Standard 88-Pin Two-Piece Connector**
- **CMOS Buffered Inputs on All Inputs Except $\overline{RAS}$ and DQ**
- **3-State Unlatched Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{CAC}	READ OR WRITE CYCLE t_{RC}
CMS88D8MB36–7	70 ns	25 ns	130 ns
CMS88D8MB36–8	80 ns	27 ns	150 ns
CMS88D4MB36–7	70 ns	25 ns	130 ns
CMS88D4MB36–8	80 ns	27 ns	150 ns

description

The CMS88D8MB36 and CMS88D4MB36 series are dynamic random-access memory cards designed to be used as internal system memory or as external add-on memory.

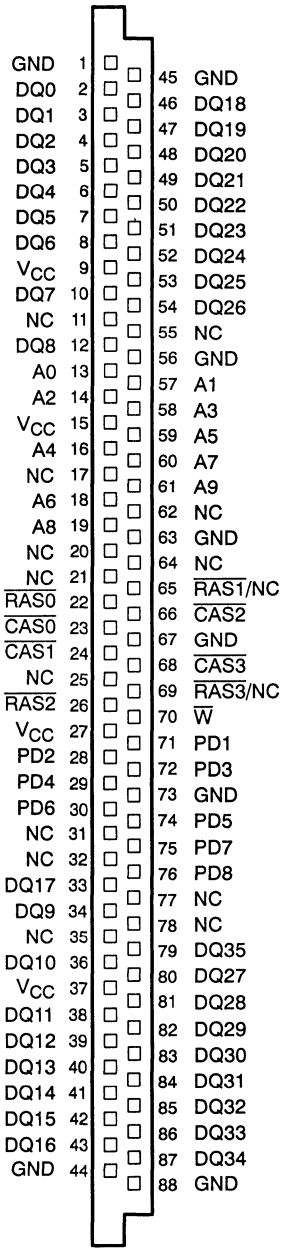
These cards have CMOS buffers added to the $\overline{CAS}$, $\overline{W}$, and address inputs to minimize loading caused by the module. $\overline{RAS}$ and data in/out remain compatible with Series 74 TTL.

The cards can operate in enhanced page mode. All address lines and data are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The common I/O features of the CMS88D8MB36 and CMS88D4MB36 dictate the use of early write cycles.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data Inputs/Outputs
PD1–PD8	Presence Detect
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable
NC	No Internal Connection

88-PIN MEMORY CARD
(CONNECTOR VIEW)



ADVANCE INFORMATION

operation

The CMS88D8MB36 and CMS88D4MB36 cards are divided into separate banks of memory. Each bank is selectable using $\overline{RAS}x$ and $\overline{CAS}x$ as shown in the table below. $\overline{RAS0}$–$\overline{RAS3}$ control which side of the DRAM banks are connected to the memory card DQ pins. Therefore, only two $\overline{RAS}$ signals may be active during any read or write cycle.

Table 1. Memory Bank Definition

DATA BLOCK	$\overline{RAS}x$		$\overline{CAS}x$	
	Side 1	Side 2	Side 1	Side 2
DQ0–DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$	$\overline{CAS0}$
DQ9–DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$	$\overline{CAS1}$
DQ18–DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$	$\overline{CAS2}$
DQ27–DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$	$\overline{CAS3}$

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. The eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

specifications

Refresh period is extended to 16 ms. During this period, each of the 1024 rows must be strobed with $\overline{RAS}$ to retain data.

memory card components

- Meets JEDEC standard
- UL approved materials

Table 2. Pin Definition for Presence Detect

DEVICE	CONFIGURATION					SPEED†			REFRESH CYCLE†	
	PD1(71)	PD2(28)	PD3(72)	PD4(29)	PD5(74)		PD6 (30)	PD7 (75)		PD8 (76)
CMS88D8MB36	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	–70 ns	V_{SS}	NC	SLOW	NC
CMS88D4MB36	V_{SS}	NC	V_{SS}	V_{SS}	NC	–80 ns	NC	V_{SS}	SELF	V_{SS}

† Applies to both CMS88D8MB36 and CMS88D4MB36 devices.

Table 3. Pin Definition

DEVICE	$\overline{RAS1}$/NC (65)	$\overline{RAS3}$/NC (69)
CMS88D8MB36	$\overline{RAS1}$	$\overline{RAS3}$
CMS88D4MB36	NC	NC

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range on V_{CC} ..... −0.5 V to 6 V
Short circuit output current ..... 50 mA
Power dissipation (CMS8D8MB36) ..... 22 W
Power dissipation (CMS8D4MB36) ..... 11 W
Operating free-air temperature ..... 0°C to 55°C
Storage temperature range ..... −40 °C to 85 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{CAS}$, $\overline{W}$, address lines	0.7 V_{CC}			V
		$\overline{RAS}$ and DQ lines	2.4		6.5	
V_{IL}	Low-level input voltage (see Note 2)	$\overline{CAS}$, $\overline{W}$, address lines			0.3 V_{CC}	V
		$\overline{RAS}$ and DQ lines	−1		0.8	
T_A	Operating free air temperature		0		55	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

ADVANCE INFORMATION

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
	Input current $\overline{RASx}$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±50	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CASx}$ high			±20	µA

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'88D8MB36-7		'88D8MB36-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle (see Note 3)		961		861	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, all other signals stable, V_{CC} = 5.25 V (see Note 3)		21		21	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3)		1850		1650	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3)		961		861	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		35	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

ADVANCE INFORMATION

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±10	µA
	Input current $\overline{RASx}$ (leakage)	V_I = 0 to 5.25 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}			±50	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.25 V, $\overline{CASx}$ high			±10	µA

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'88D4MB36-7		'88D4MB36-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle (see Note 3)		950		850	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high. All other signals stable, V_{CC} = 5.25 V (see Note 3)		11		11	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3)		950		850	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.25 V, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3)		950		850	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		35	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		7	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'88D8MB36-7 '88D4MB36-7		'88D8MB36-8 '88D4MB36-8		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CASx}$ low		25		27	ns
t_{CAA}	Access time from column-address		42		47	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{CPA}	Access time from column precharge		47		52	ns
t_{CLZ}	$\overline{CASx}$ low to output in low Z	0		0		ns
t_{OFF}	Output disable time after $\overline{CASx}$ high (see Note 4)	0	25	0	27	ns

NOTE 4: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'88D8MB36-7 '88D4MB36-7		'88D8MB36-8 '88D4MB36-8		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{PC}	Page mode read or write cycle time (see Note 5)	52		57		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	25	10 000	27	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high	50		60		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low	70	10 000	80	10 000	ns
t_{RASP}	Page mode, pulse duration, $\overline{RAS}$ low	70	100 000	80	100 000	ns
t_{wp}	Write pulse duration	22		22		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	7		7		ns
t_{DS}	Data setup time before $\overline{CAS}$ low	0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{WCS}	$\overline{W}$ low setup before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$ low setup before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$ low setup before $\overline{RAS}$ high	25		27		ns
t_{WSR}	$\overline{W}$ high setup ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	17		17		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		12		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see note 6)	55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	12		12		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	55		60		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 7)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 7)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 6)	55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	7		7		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		27		ns

NOTES: 5. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
6. The minimum value is measured when t_{RCD} is set to t_{RCD}(min) as a reference.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

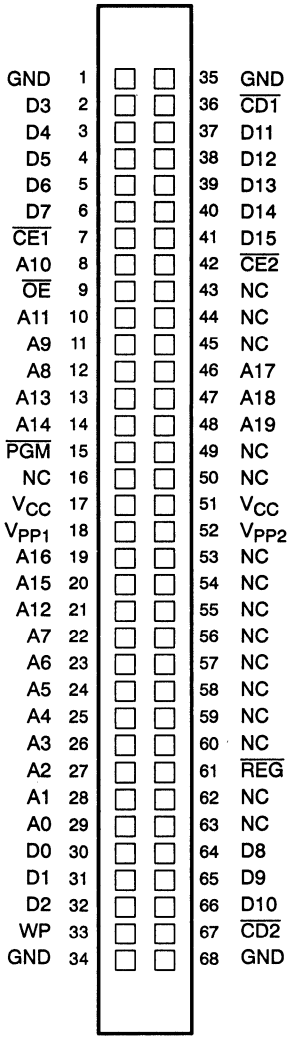
PARAMETER		'88D8MB36-7 '88D4MB36-7		'88D8MB36-8 '88D4MB36-8		UNIT
		MIN	MAX	MIN	MAX	
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 8)	20	47	22	53	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 8)	15	28	17	33	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	42		47		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	17		17		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		ns
t_{REF}	Refresh time interval		16		16	ms
t_T	Transition time (see Note 10)	3	50	3	50	ns

NOTES: 8. Maximum values specified to assure access times.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. All cycle times assume t_T = 5 ns.

ADVANCE INFORMATION

- **Industry Standard PCMCIA Cards**
- **Standard Card Size (85.6 mm × 54.0 mm × 3.3 mm)**
- **Single 5-V Power Supply (± 5% Tolerance)**
- **Utilize TSOP (Thin Small Outline Package) OTP PROM (One Time Programmable Read-Only Memory)**
- **68-Pin PCMCIA (Rev. 2.0) / JEIDA (Rev. 4.1) Compatible**
- **8-Bit or 16-Bit User-Configurable Organizations**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 55°C**
- **Standard 68 Pin Two-Piece Connector**
- **All Inputs and Outputs are Fully TTL Compatible**
- **3-State Output**

68-PIN MEMORY CARD† (CONNECTOR VIEW)



NC = No internal connection.

† Pinout shown is for maximum density card. See pin assignment table for specifics.

description

The CMS68Pxxx series are TI Standard Memory Cards designed to be used either as an internal memory system or as external add-on memory according to PCMCIA/JEIDA industry standard card specifications. These cards are offered with a memory size from 256K bytes to 1024K bytes of one time electrically programmable read only memory, and the card organization (×8 or ×16) is directly user-configurable. The cards comprise 2, 4, or 8 TMS27PC010As, each in a 32-lead plastic thin small outline package (TSOP). Refer to the TMS27PC010A data sheet for more information.

available organizations

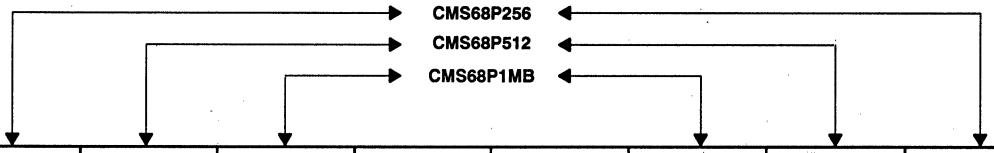
PART NUMBER	ORGANIZATION	ACCESS TIME	TOTAL DENSITY	CONNECTOR
CMS68P256-200, CMS68P256N-200‡	256K × 8 / 128K × 16	200 ns	256K-Bytes	Two-piece, 68 pin
CMS68P512-200, CMS68P512N-200‡	512K × 8 / 256K × 16	200 ns	512K-Bytes	Two-piece, 68 pin
CMS68P1MB-200, CMS68P1MBN-200‡	1 MEG × 8 / 512K × 16	200 ns	1024K-Bytes	Two-piece, 68 pin

‡ CMS68PxxxN devices do not include attribute memory.

ADVANCE INFORMATION

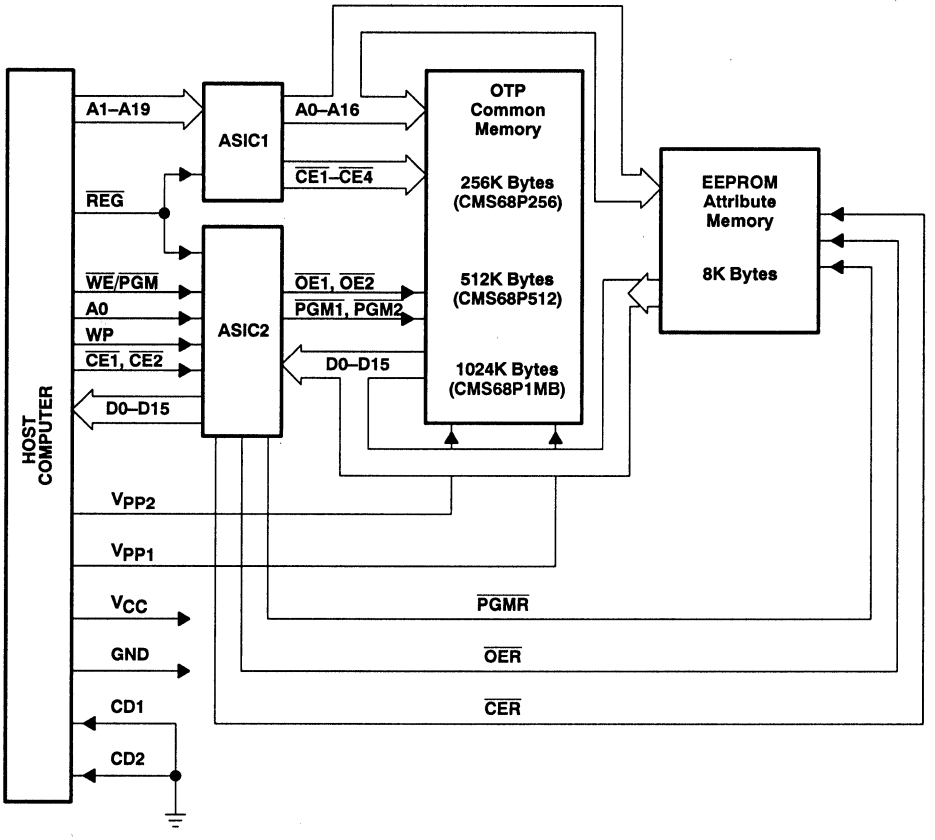
ADVANCE INFORMATION

pin assignments



CMS68P256	CMS68P512	CMS68P1MB	PIN NUMBER	PIN NUMBER	CMS68P1MB	CMS68P512	CMS68P256
GND	GND	GND	1	35	GND	GND	GND
D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	3	37	D11	D11	D11
D5	D5	D5	4	38	D12	D12	D12
D6	D6	D6	5	39	D13	D13	D13
D7	D7	D7	6	40	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15
A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC
A11	A11	A11	10	44	NC	NC	NC
A9	A9	A9	11	45	NC	NC	NC
A8	A8	A8	12	46	A17	A17	A17
A13	A13	A13	13	47	A18	A18	NC
A14	A14	A14	14	48	A19	NC	NC
$\overline{PGM}$	$\overline{PGM}$	$\overline{PGM}$	15	49	NC	NC	NC
NC	NC	NC	16	50	NC	NC	NC
V_{CC}	V_{CC}	V_{CC}	17	51	V_{CC}	V_{CC}	V_{CC}
V_{PP1}	V_{PP1}	V_{PP1}	18	52	V_{PP2}	V_{PP2}	V_{PP2}
A16	A16	A16	19	53	NC	NC	NC
A15	A15	A15	20	54	NC	NC	NC
A12	A12	A12	21	55	NC	NC	NC
A7	A7	A7	22	56	NC	NC	NC
A6	A6	A6	23	57	NC	NC	NC
A5	A5	A5	24	58	NC	NC	NC
A4	A4	A4	25	59	NC	NC	NC
A3	A3	A3	26	60	NC	NC	NC
A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	28	62	NC	NC	NC
A0	A0	A0	29	63	NC	NC	NC
D0	D0	D0	30	64	D8	D8	D8
D1	D1	D1	31	65	D9	D9	D9
D2	D2	D2	32	66	D10	D10	D10
WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	34	68	GND	GND	GND

functional block diagram



ADVANCE INFORMATION

pin description

SYMBOL	FUNCTION
A0–A19	Address inputs. Lines driven by the host which enable direct addressing of up to 1 megabyte of memory. Signal A0 is not used in word access mode. Signal A19 is the most significant bit.
D0–D15	Bidirectional data bus. The most significant bit is D15. Bit number and significance decrease downward to D0.
$\overline{CE1}$, $\overline{CE2}$	Active-low card. Enables signals driven by the host; $\overline{CE1}$ is used to enable even bytes, $\overline{CE2}$ to enable odd bytes. A multiplexing scheme based on A0, $\overline{CE1}$, and $\overline{CE2}$ allows 8-bit hosts to access all data on D0–D7 if desired.
$\overline{OE}$	Active-low signal. Driven by the host; used to gate memory-read data from the memory card.
$\overline{PGM}$	Programming enable signal.
V_{PP1}	Programming voltage 1.
V_{PP2}	Programming voltage 2.
$\overline{CD1}$, $\overline{CD2}$	Card detect. Signals for proper memory card insertion detection. The signals are connected to ground internally on the memory card.
WP	Write protect. Status signal of write protect. Switch on the memory card.
$\overline{REG}$	When active access to the memory card is limited to Attribute Memory used to record capacity and other configuration and attribute information.
V_{CC}	Power supply.
GND	Ground.
NC	No connection.

function table

FUNCTION MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{PGM}$	V_{PP2}	V_{PP1}	D8–D15	D0–D7
Standby	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Read (x8)	H H	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY OD-BY
Read (x16)	H	L	L	X	L	H	V_{CC}	V_{CC}	OD-BY	EV-BY
OD-BY Read	H	L	H	X	L	H	V_{CC}	V_{CC}	OD-BY	HI-Z
Write (x8)	H H	H H	L L	L H	H H	L L	V_{CC} V_{PP}	V_{PP} V_{CC}	XXX XXX	EV-BY OD-BY
Write (x16)	H	L	L	X	H	L	V_{PP}	V_{PP}	OD-BY	EV-BY
OD-BY Write	H	L	H	X	H	L	V_{PP}	V_{CC}	OD-BY	XXX

EV-BY = Even Byte
OD-BY = Odd Byte
HI-Z = High Impedance
X = V_{IL} or V_{IH}
XXX = Don't Care

attribute memory read function

FUNCTION MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$	V_{PP2}	V_{PP1}	D8–D15	D0–D7
Standby Mode	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Byte access (8 bits)	L L	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY Not Valid
Byte access (16 bits)	L	L	L	X	L	H	V_{CC}	V_{CC}	Not Valid	EV-BY
Odd-byte-only access	L	L	H	X	L	H	V_{CC}	V_{CC}	Not Valid	HI-Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.5 to 14 V
Input voltage range, (see Note 1) ..... – 0.5 to 6.5 V
Output voltage range, (see Note 1) ..... – 0.5 to V_{CC}
Operating free-air temperature range ..... – 0°C to 55°C
Storage temperature range ..... – 40°C to 70°C
Connector insertion cycles 10 000

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.75	5	5.25	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2.0		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.5	V
V_{IL}	Low-level input voltage		TTL	– 0.5		0.8	V
			CMOS	– 0.5		GND + 0.2	V
T_A	Operating free-air temperature			0		55	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage (except WP)		I_{OH} = 12 mA, V_I = 0.9 V_{CC}	3.7		V
			I_{OH} = 1.2 mA, V_I = 0.9 V_{CC}	4.4		
V_{OL}	Low-level output voltage (except CD1, CD2)		I_{OL} = 12 mA, V_I = 0.1 V_{CC}		0.5	V
			I_{OL} = 1.2 mA, V_I = 0.1 V_{CC}		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.25 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.25 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.25 V, $\overline{CEx}$ = V_{IH}		10	mA
		CMOS-input level	V_{CC} = 5.25 V, $\overline{CEx}$ = V_{CC} ± 0.2 V		2	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.25 V, $\overline{CEx}$ = V_{IL} t_{cycle} = Minimum cycle time†, outputs open		100	mA

† Minimum cycle time = maximum access time.

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	V_I = 0, f = 1 MHz			80	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz			80	pF

† Capacitance measurements are made on sample basis only.

switching characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	MIN	MAX	UNIT
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		200	ns
$t_{a(E)}$	Access time from chip enable			200	ns
$t_{en(G)}$	Output enable time from $\overline{OE}$			75	ns
t_{dis}	Output disable time from $\overline{OE}$ or $\overline{CEx}$, whichever occurs first‡		0	60	ns
$t_{v(A)}$	Output data valid time after change of address $\overline{CEx}$ or $\overline{OE}$ whichever occurs first		0		ns

‡ Value calculated from 0.5 V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing wave form).
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{OE}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{OE}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(GPM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2		10	µs
$t_{su(E)}$	$\overline{CE}$ setup time		2			µs
$t_{su(G)}$	$\overline{OE}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing wave form).

PARAMETER MEASUREMENT INFORMATION

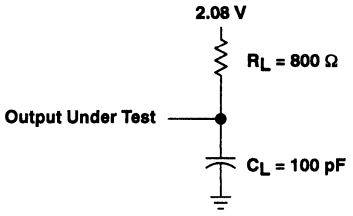
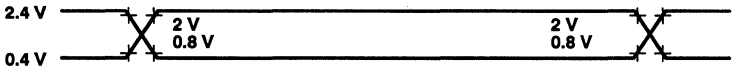


Figure 1. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

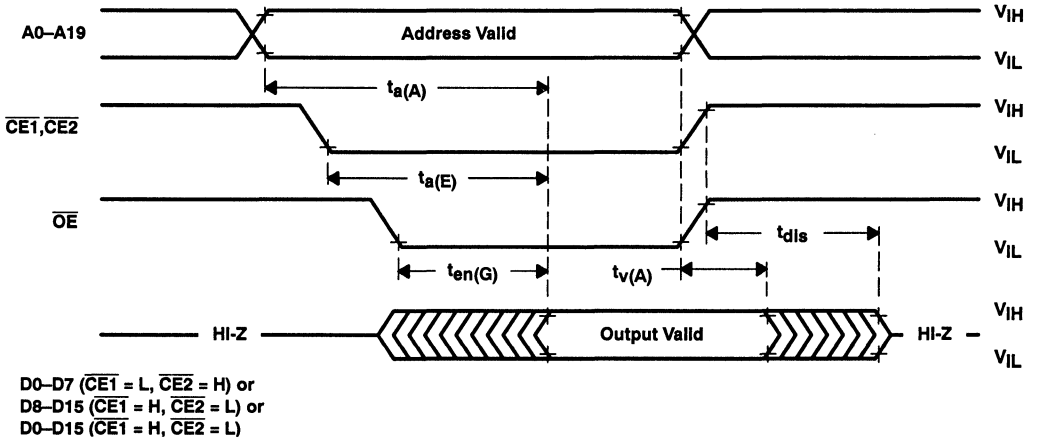


Figure 2. Read Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

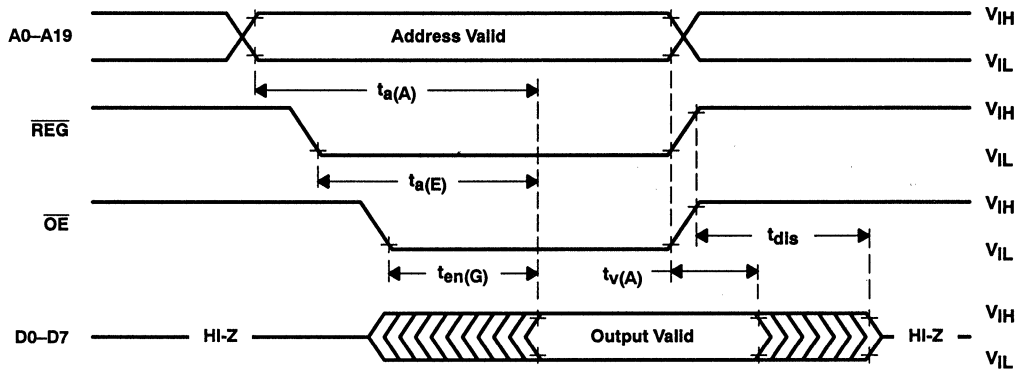
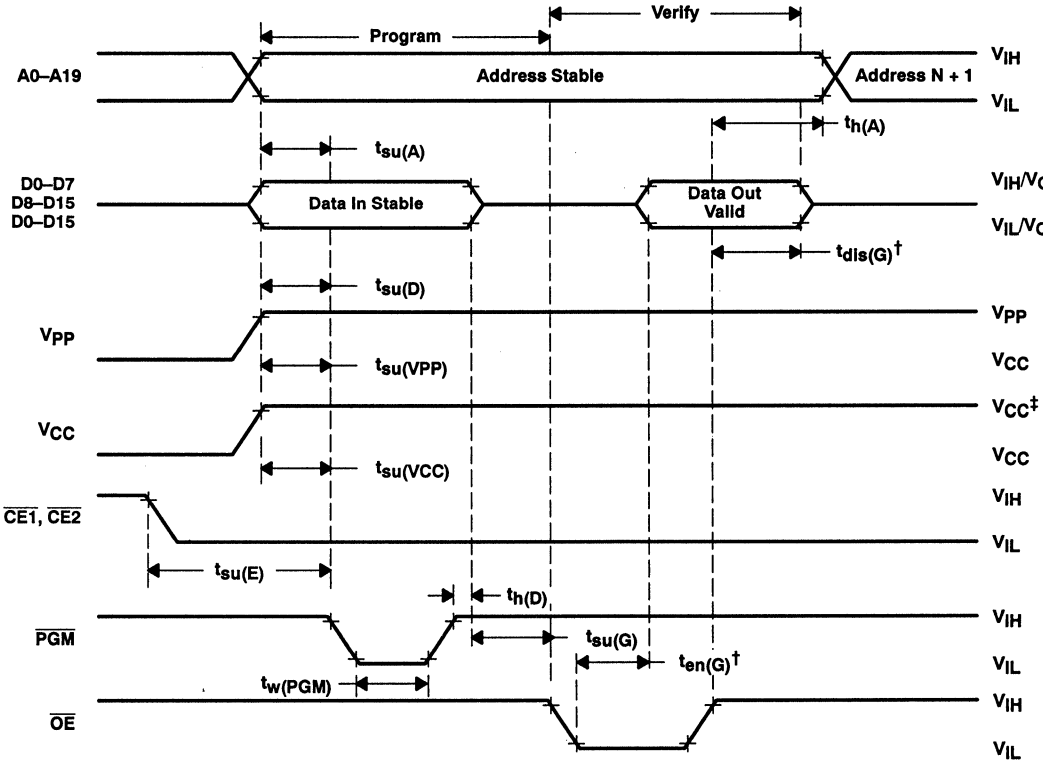


Figure 3. Attribute Memory Read Cycle Timing



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ V_{PP} = 13 V and V_{CC} = 6.5 V for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

PARAMETER MEASUREMENT INFORMATION

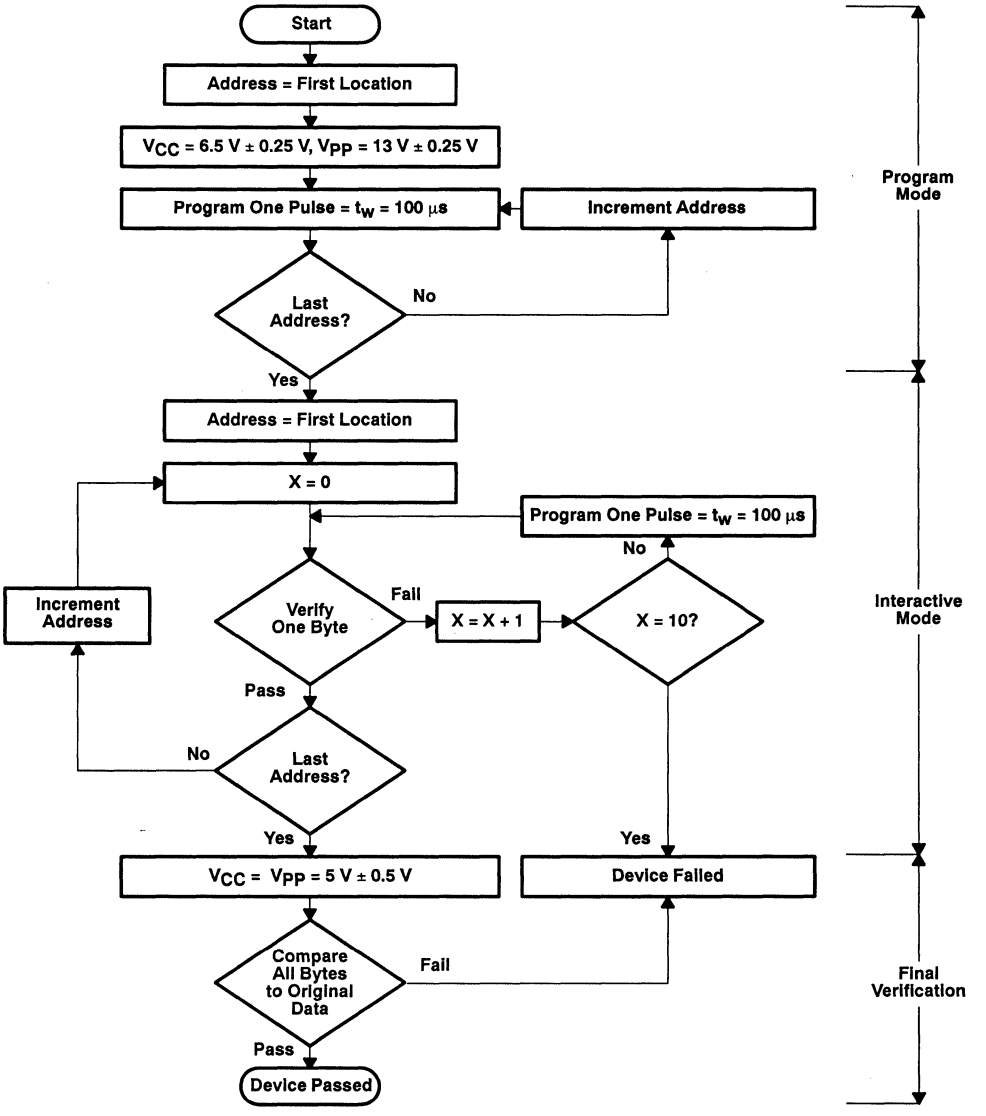
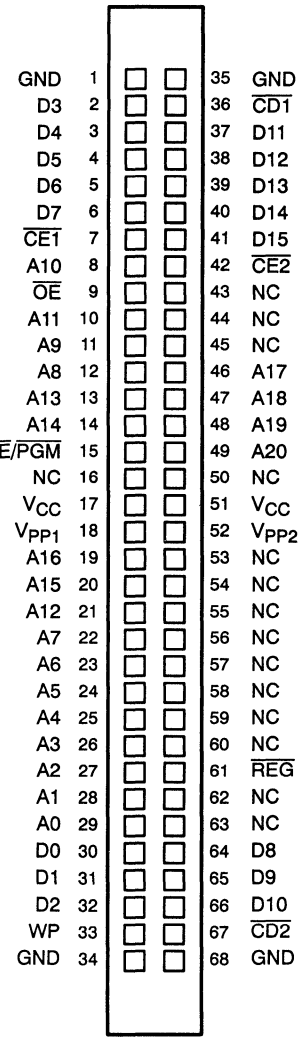


Figure 5. SNAP! Pulse Programming Flowchart

ADVANCE INFORMATION

- **Industry Standard PCMCIA Cards**
- **Standard Card Size (85,6 mm × 54,0 mm × 3,3 mm)**
- **Single 5-V Power Supply (± 5% Tolerance)**
- **Utilize TSOP-I (Thin Small Outline Package-Type I) Flash Memory Devices**
- **68-Pin PCMCIA (Rev. 2.0) / JEIDA (Rev. 4.0) Compatible**
- **8-Bit or 16-Bit User Configurable Organization**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 55°C**
- **Standard 68-Pin Two-Piece Connector**
- **All Input/Output Signals Fully TTL Compatible**
- **3-State Output**

68-PIN MEMORY CARD† (CONNECTOR VIEW)



† Pinout shown is for maximum density card. See pin assignment table for specifics.

NC – No internal connection

description

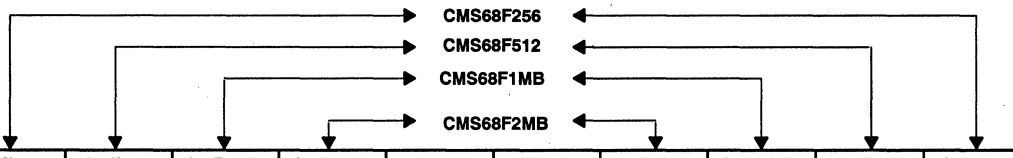
The CMS68Fxxx series are TI standard memory cards designed to be used either as an internal memory system or as external add-on memory according to PCMCIA/JEIDA industry standard card specifications. These cards are offered with a memory size from 256K bytes to 2048K bytes of Flash memory devices and the card organization (× 8 or × 16) is directly user configurable.

The cards are comprised of 2, 4, or 8 1M-byte or 2M-byte Flash memory devices in 32-lead plastic Thin Small Outline Packages (TSOP-I).

available organizations

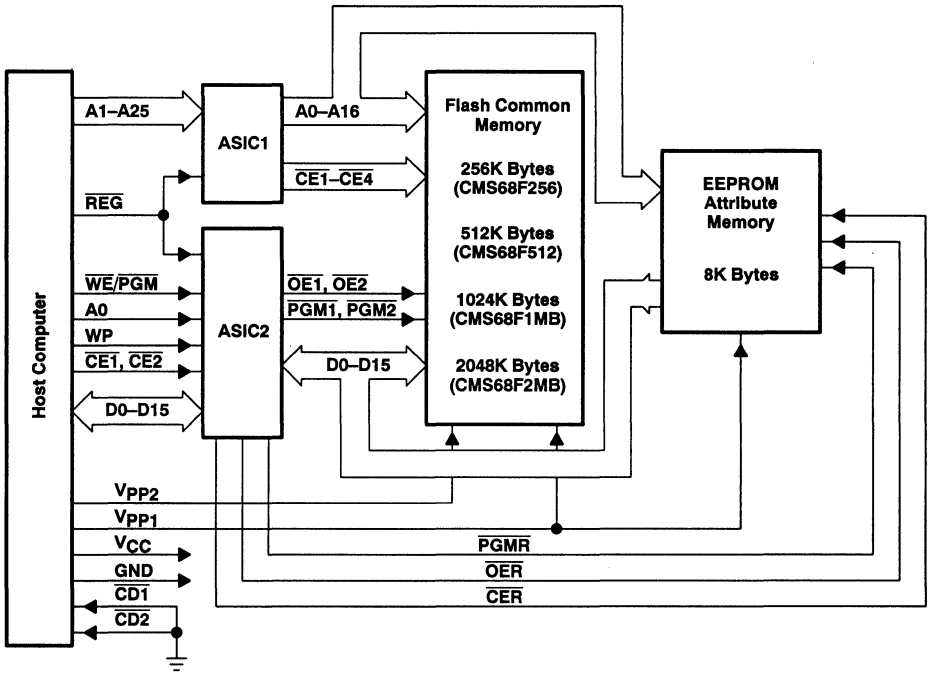
PART NUMBER	ORGANIZATION	ACCESS TIME	TOTAL DENSITY	CONNECTOR
CMS68F256-250	256K × 8 / 128K × 16	250 ns	256K-Bytes	Two-piece, 68 pin
CMS68F512-250	512K × 8 / 256K × 16	250 ns	512K-Bytes	Two-piece, 68 pin
CMS68F1MB-250	1M × 8 / 512K × 16	250 ns	1M-Bytes	Two-piece, 68 pin
CMS68F2MB-250	2M × 8 / 1M-Byte × 16	250 ns	2M-Bytes	Two-piece, 68 pin

pin assignments



'68F256	'68F512	'68F1MB	'68F2MB	PIN #	PIN #	'68F2MB	'68F1MB	'68F512	'68F256
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC	NC
A11	A11	A11	A11	10	44	NC	NC	NC	NC
A9	A9	A9	A9	11	45	NC	NC	NC	NC
A8	A8	A8	A8	12	46	A17	A17	A17	A17
A13	A13	A13	A13	13	47	A18	A18	A18	NC
A14	A14	A14	A14	14	48	A19	A19	NC	NC
$\overline{WE/PGM}$	$\overline{WE/PGM}$	$\overline{WE/PGM}$	$\overline{WE/PGM}$	15	49	A20	NC	NC	NC
NC	NC	NC	NC	16	50	NC	NC	NC	NC
V_{CC}	V_{CC}	V_{CC}	V_{CC}	17	51	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{PP1}	V_{PP1}	V_{PP1}	V_{PP1}	18	52	V_{PP2}	V_{PP2}	V_{PP2}	V_{PP2}
A16	A16	A16	A16	19	53	NC	NC	NC	NC
A15	A15	A15	A15	20	54	NC	NC	NC	NC
A12	A12	A12	A12	21	55	NC	NC	NC	NC
A7	A7	A7	A7	22	56	NC	NC	NC	NC
A6	A6	A6	A6	23	57	NC	NC	NC	NC
A5	A5	A5	A5	24	58	NC	NC	NC	NC
A4	A4	A4	A4	25	59	NC	NC	NC	NC
A3	A3	A3	A3	26	60	NC	NC	NC	NC
A2	A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	A1	28	62	NC	NC	NC	NC
A0	A0	A0	A0	29	63	NC	NC	NC	NC
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

functional block diagram



operation

There are seven modes of operation for the CMS68Fxxx described in the table below. The read mode requires a single 5-V supply.

operation table

FUNCTIONAL MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$ / $\overline{PGM}$	V_{PP2}	V_{PP1}	D15–D8	D7–D0
Standby	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Read (x8)	H H	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY OD-BY
Read (x16)	H	L	L	X	L	H	V_{CC}	V_{CC}	OD-BY	EV-BY
OD-BY Read	H	L	H	X	L	H	V_{CC}	V_{CC}	OD-BY	HI-Z
Write (x8)	H H	H H	L L	L H	H H	L L	V_{CC} V_{PP}	V_{PP} V_{CC}	XXX XXX	EV-BY OD-BY
Write (x16)	H	L	L	X	H	L	V_{PP}	V_{PP}	OD-BY	EV-BY
OD-BY Write	H	L	H	X	H	L	V_{PP}	V_{CC}	OD-BY	XXX

attribute memory read function

FUNCTIONAL MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$ / $\overline{PGM}$	V_{PP2}	V_{PP1}	D15–D8	D7–D0
Standby Mode	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Byte access (8 bits)	L L	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY Not Valid
Byte access (16 bits)	L	L	L	X	L	H	V_{CC}	V_{CC}	Not Valid	EV-BY
Odd-byte-only access	L	L	H	X	L	H	V_{CC}	V_{CC}	Not Valid	HI-Z

EV-BY = Even Byte
OD-BY = Odd Byte
HI-Z = High Impedance
X = V_{IL} or V_{IH}
H = High
L = Low

pin description

SYMBOL	FUNCTION
A0–A20	Address input lines, driven by the host, which enable direct addressing of up to 2 megabytes of memory. Signal A0 is not used in word access mode. Signal A20 is the most significant bit.
D0–D15	Bidirectional data bus The most significant bit is D15. Bit number and significance decrease downward to D0.
$\overline{CE1}$, $\overline{CE2}$	Active-low card enable signals driven by the host; $\overline{CE1}$ is used to enable even bytes, $\overline{CE2}$ for odd bytes. A multiplexing scheme based on A0, $\overline{CE1}$, $\overline{CE2}$ allows 8-bit hosts to access all data on D0–D7 if desired.
$\overline{OE}$	Active-low signal, driven by the host, which is used to gate memory read data from the memory card.
$\overline{WE}$/$\overline{PGM}$	Programming enable signal
V_{PP1}	Programming voltage 1
V_{PP2}	Programming voltage 2
$\overline{CD1}$, $\overline{CD2}$	Card detect signals for proper memory card insertion detection. The signals are connected to ground internally on the memory card.
WP	Status signal of Write Protect switch on the memory card.
$\overline{REG}$	When active, access to the memory card is limited to Attribute Memory used to record capacity and other configuration and attribute information.
V_{CC}	Power supply
GND	Ground
NC	No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) . . . . . – 0.5 to 14 V
Input voltage range, (see Note 1) . . . . . – 0.5 to 6.5 V
Output voltage range, (see Note 1) . . . . . – 0.5 to V_{CC}
Operating free-air temperature range . . . . . – 0°C to 55°C
Storage temperature range . . . . . – 20°C to 65°C
Connector insertion cycles 10 000

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{PPH}	Supply voltage		11.4		12.6	V
V_{PPL}	Supply voltage	Read Mode	0		6.5	V
V_{IH}	High-level input voltage	TTL	2.4		V_{CC} + 0.3	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.5	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	V
		CMOS	– 0.5		GND + 0.2	
T_A	Operating free-air temperature		0		55	°C

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage (except WP)		I_{OH} = 12 mA, V_I = 0.9 V_{CC}	3.7		V
			I_{OH} = 1.2 mA, V_I = 0.9 V_{CC}	4.4		
V_{OL}	Low-level output voltage (except CD1, CD2)		I_{OL} = 12 mA, V_I = 0.1 V_{CC}		0.5	V
			I_{OL} = 1.2 mA, V_I = 0.1 V_{CC}		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.25 V		±10	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±10	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.25 V		80	mA
I_{PP2}	V_{PP} write current		V_{PP} = V_{PPH}, Write in progress		60	mA
I_{PP3}	V_{PP} write verify current		V_{PP} = V_{PPH}, Erasure in progress		12	µA
I_{PP4}	V_{PP} erase verify current		V_{PP} = V_{PPH}, Erasure verify in progress		12	mA
I_{PP5}	V_{PP} leakage current		V_{PP} ≤ V_{CC}		±80	µA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{CEx}$ = V_{IH}, V_{CC} = 5.25 V		25	mA
		CMOS-input level	$\overline{CEx}$ = V_{CC} ± 0.2 V, V_{CC} = 5.25 V		20	
I_{CC2}	V_{CC} supply current (active, output open)		$\overline{CEx}$ = V_{IL}, V_{CC} = 5.25 V, I_{OUT} = 0 mA, f = 6 MHz		80	mA

capacitance over recommended ranges of supply voltage and free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz			8	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz			16	pF

† Capacitance measurements are made on sample basis only.
‡ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics for read-only operations for attribute memory over recommended ranges of supply voltage and operating free-air temperature (see Notes 2 and 3)

PARAMETER		TEST CONDITIONS (SEE NOTES 2 & 3)	MIN	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		200	ns
$t_{a(E)}$	Access time ROM chip enable			200	ns
$t_{en(G)}$	Output enable time from $\overline{OE}$			100	ns
t_{dis}	Output disable time from $\overline{OE}$ or $\overline{CEx}$, whichever occurs first¶		0	60	ns
$t_{v(A)}$	Output data valid time after change of address $\overline{CEx}$ or $\overline{OE}$ whichever occurs first		0		ns

¶ Value calculated from 0.5-V delta to measured output level.

NOTES: 2. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference input/output wave forms for timing parameters).
3. Common test conditions apply for t_{dis} except during programming.

timing requirements for read-only operations over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER	CHARACTERISTICS	MIN	MAX	UNIT
t_{avav} / t_{rc}	Read cycle time	250		ns
t_{elqv} / t_{ce}	Chip enable access time		250	ns
t_{avqv} / t_{acc}	Address access time		250	ns
t_{glqv} / t_{oe}	Output enable access time		120	ns
t_{elox} / t_{iz}	Chip enable to output in low-Z	5		ns
t_{ehqz}	Chip disable to output in high-Z		60	ns
t_{glqx} / t_{oiz}	Output enable to output in low-Z	5		ns
t_{ghqz} / t_{df}	Output disable to output in high-Z		60	ns
t_{oh}	Output hold from address $\overline{CE}$ or $\overline{OE}$ change (see Note 5)	5		ns
t_{whgl}	Write recovery time before read	6		µs

NOTES: 4. Rise/fall time ≤ 10 ns.
5. Read timing parameters during read/write operations are the same as during read-only operations.

timing requirements for write/erase operations over recommended ranges of supply voltage and operating free-air temperature (see Notes 4 and 5)

PARAMETER	CHARACTERISTICS	MIN	MAX	UNIT
t_{avav} / t_{wc}	Write cycle time	250		ns
t_{avwl} / t_{as}	Address setup time	0		ns
t_{wlax} / t_{ah}	Address hold time	100		ns
t_{dvwh} / t_{ds}	Data setup time	80		ns
t_{whdx} / t_{dh}	Data hold time	30		ns
t_{whgl}	Write recovery time before read	6		µs
t_{ghwl}	Read recovery time before read	0		µs
t_{wlox}	Output high-Z from write enable	5		ns
t_{whox}	Output low-Z from write enable		60	ns
t_{elwl} / t_{cs}	Chip enable setup time before write	40		ns
t_{wheh} / t_{ch}	Chip enable hold time	0		ns
t_{wlwh} / t_{wp}	Write pulse duration	100		ns
t_{whwl} / t_{wph}	Write pulse duration high	20		ns
t_{whwh1}	Duration of write operation (see Note 6)	10		µs
t_{whwh2}	Duration of erase operation (see Note 6)	9.5		ms
t_{vpel}	V_{PP} setup time to chip enable low	100		ns

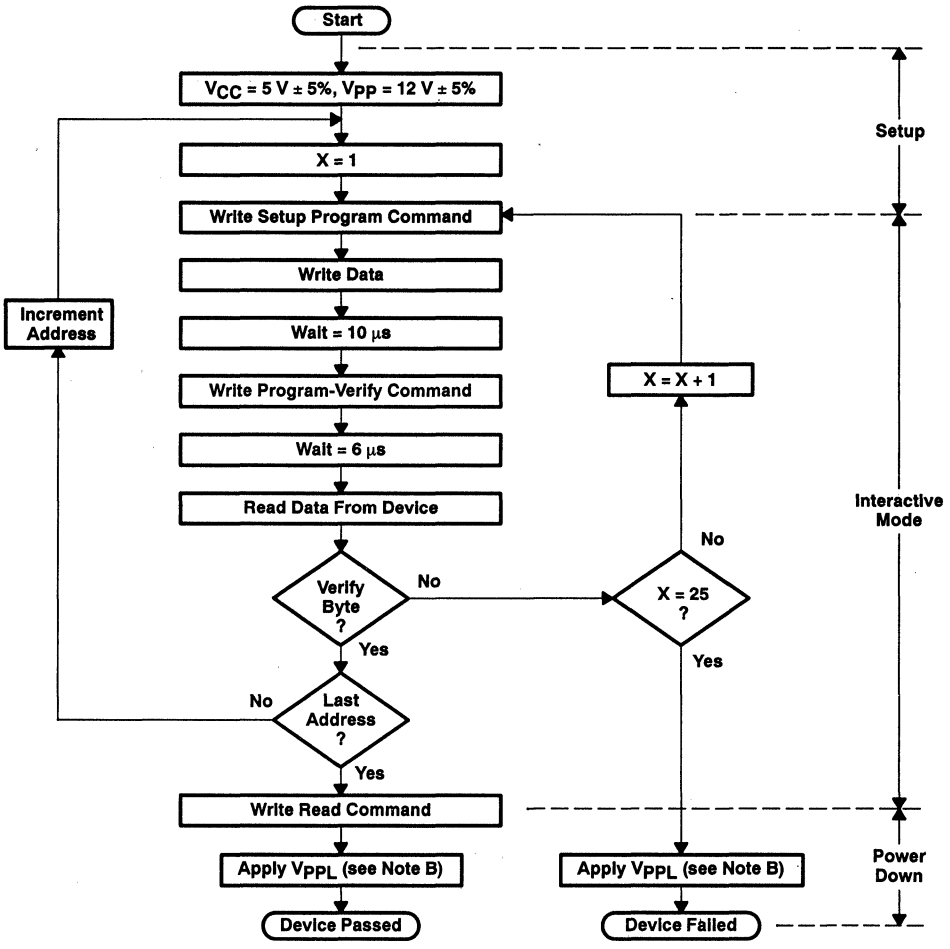
NCTES: 4. Rise/fall time ≤ 10 ns.
5. Read timing parameters during read/write operations are the same as during read-only operations. Refer to timing requirements for Read Operations.
6. The integrated stop timer terminates the write/erase operations, thereby eliminating the need for a maximum specification.

alternative $\overline{CE}$-controlled writes over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	CHARACTERISTICS	MIN	MAX	UNIT
t_{avav}	Write cycle time	250		ns
t_{avel}	Address setup time	0		ns
t_{elax}	Address hold time	100		ns
t_{dveh}	Data setup time	80		ns
t_{ehdx}	Data hold time	30		ns
t_{ehgl}	Write recovery time before read	6		µs
t_{ghel}	Read recovery time before read	0		µs
t_{wiel}	Write enable setup time before chip-enable	0		ns
t_{ehwh}	Write enable hold time	0		ns
t_{eleh}	Write pulse duration (see Note 7)	100		ns
t_{ehel}	Write pulse duration high	20		ns
t_{pel}	V_{PP} setup time to chip enable low	100		ns

NOTE 7: Chip Enable Controlled Writes: Write operations are driven by the valid condition of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse duration (with a longer Write Enable timing waveform) all set-up, hold, and inactive Write Enable times should be measured relative to the Chip Enable waveform.

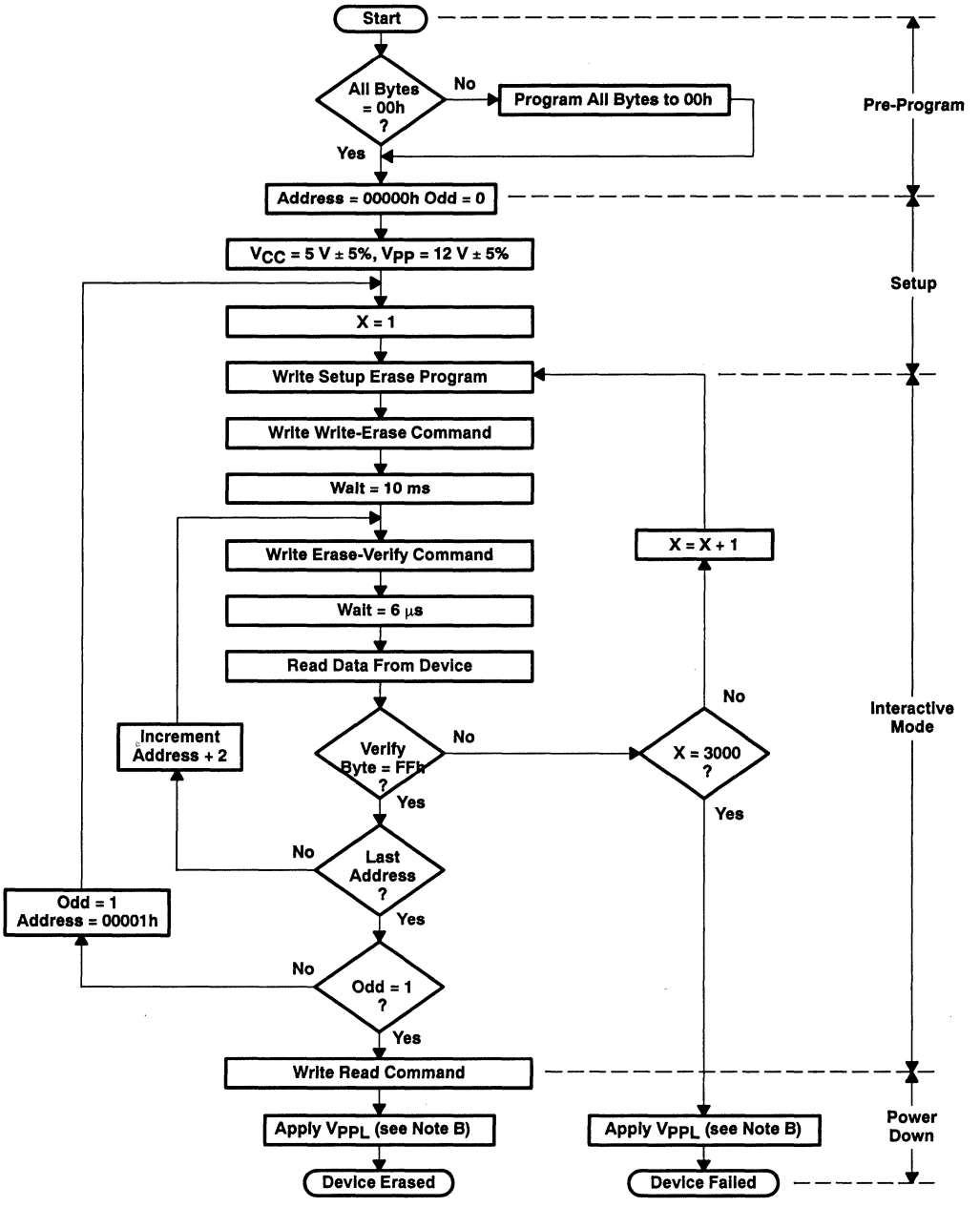
programming flowchart: write algorithm for byte-wide mode



BUS OPERATION	COMMAND	COMMENTS
Initialize Address Standby		Wait for V_{PP} ramp to V_{PPH} (see Note A) Initialize Pulse Count
Write	Setup Program	Data = 40h
Write	Write-Data	Valid Address Data
Standby		Wait = 10 µs
Write	Program Verify	Data = C0h; Ends Program Operation
Standby		Wait = 5 µs
Read		Read Byte to Verify Programming; Compare Output to Expected Output
Write	Read	Data = 00h; Register Reset for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

flash-erase flowchart: erase algorithm for byte-wide mode



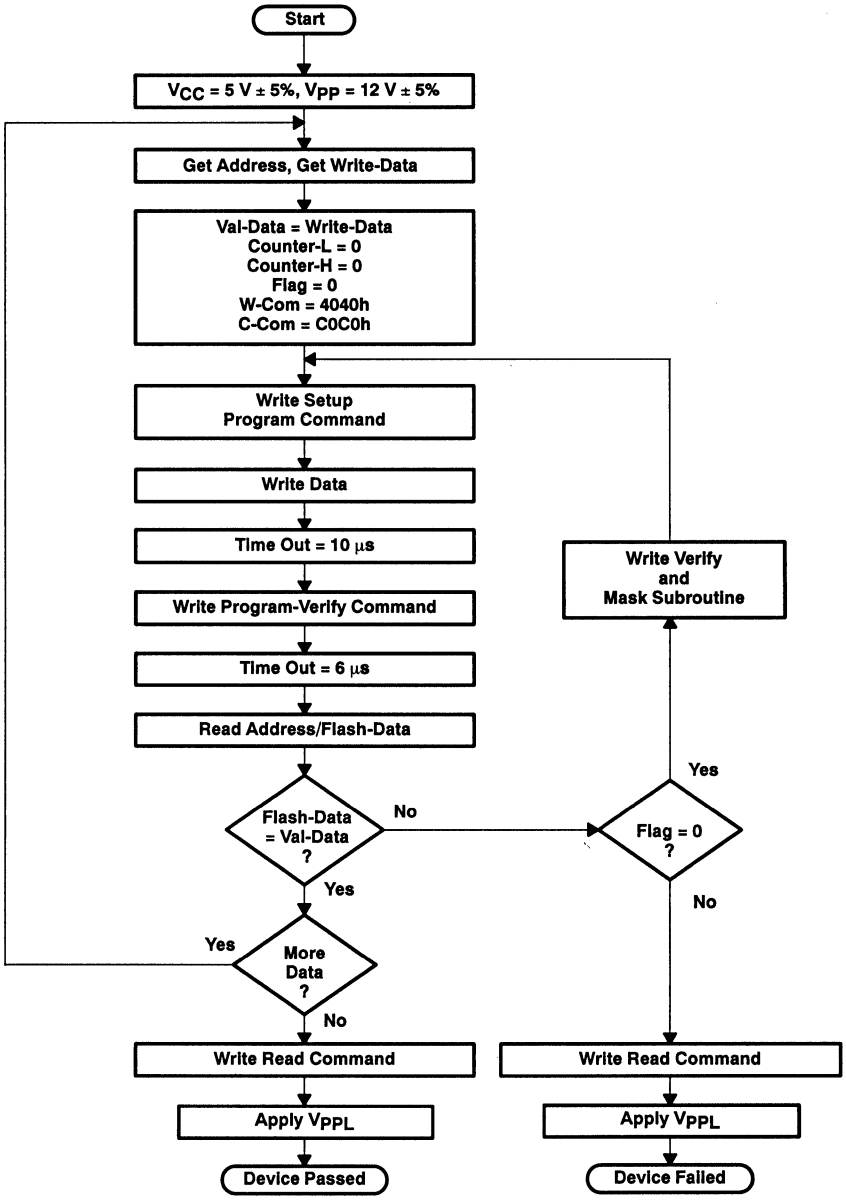
NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

flash-erase flowchart: erase algorithm for byte-wide mode (continued)

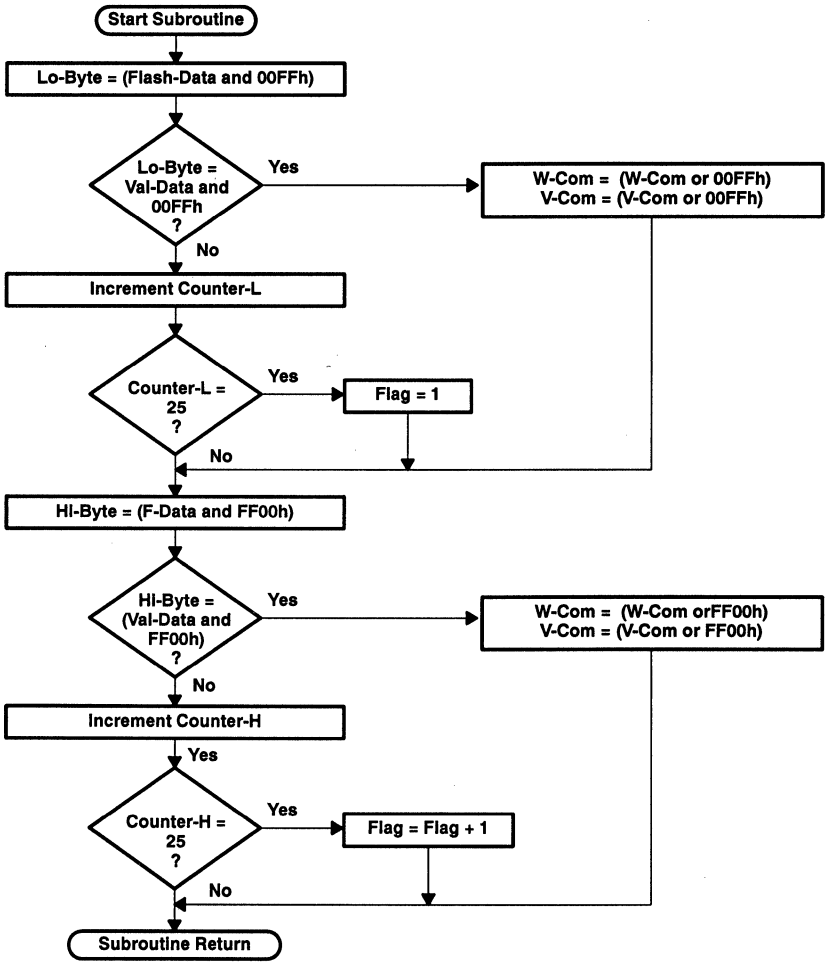
BUS OPERATION	COMMAND	COMMENTS
		Entire Memory Must = 00h Before Erasure Use Fastwrite Programming Algorithm
		Initialize Addresses
Standby		Wait = V_{PP} Ramp to V_{PPH} (see Note A)
		Initialize Pulse Count
Write	Setup Erase	Data = 20h
Write	Erase	Data = 20h
Standby		Wait = 9.5 ms
Write	Erase Verify	Address = Byte to Verify; Data = A0h; Ends the Erase Operation
Standby		Wait = 6 μs
Read		Read Byte to Verify Erasure; Compare Output to FFh
Write	Read	Data = 00h; Register Reset for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

programming flowchart: write algorithm for word-wide mode

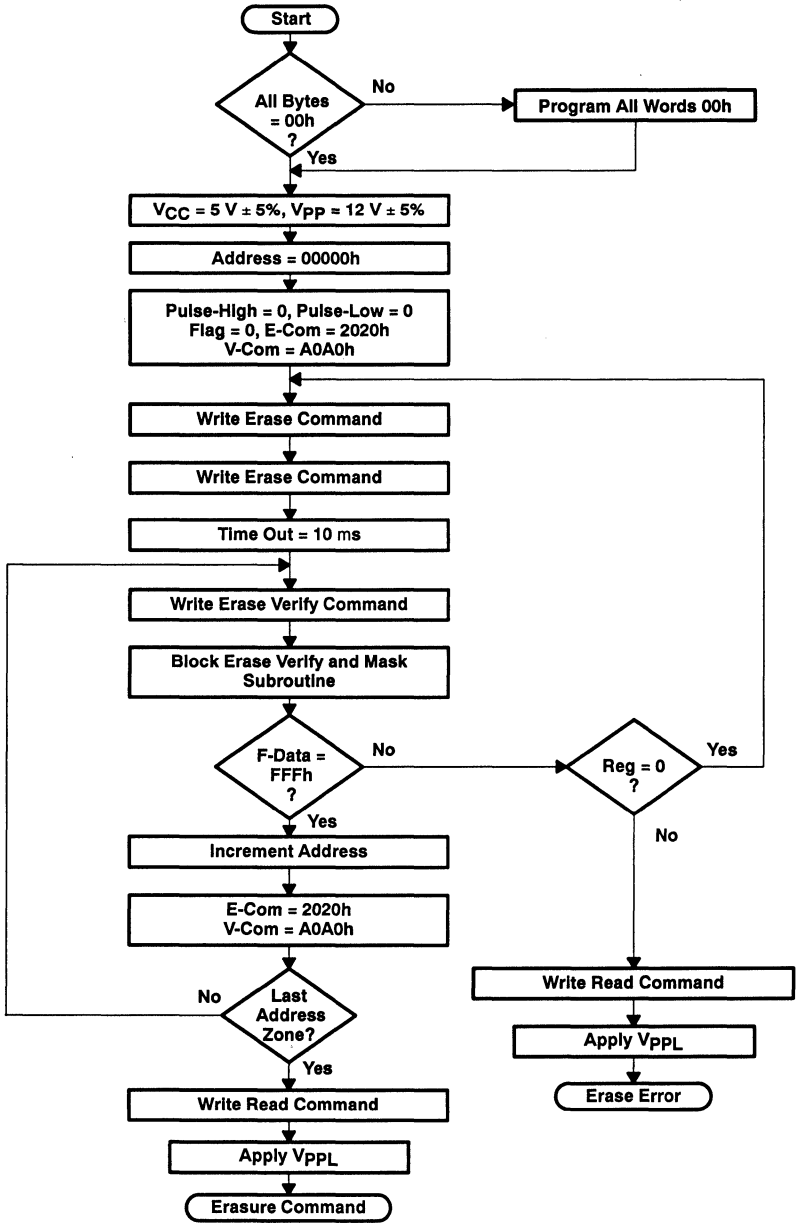


write verify and mask subroutine for read-write mode



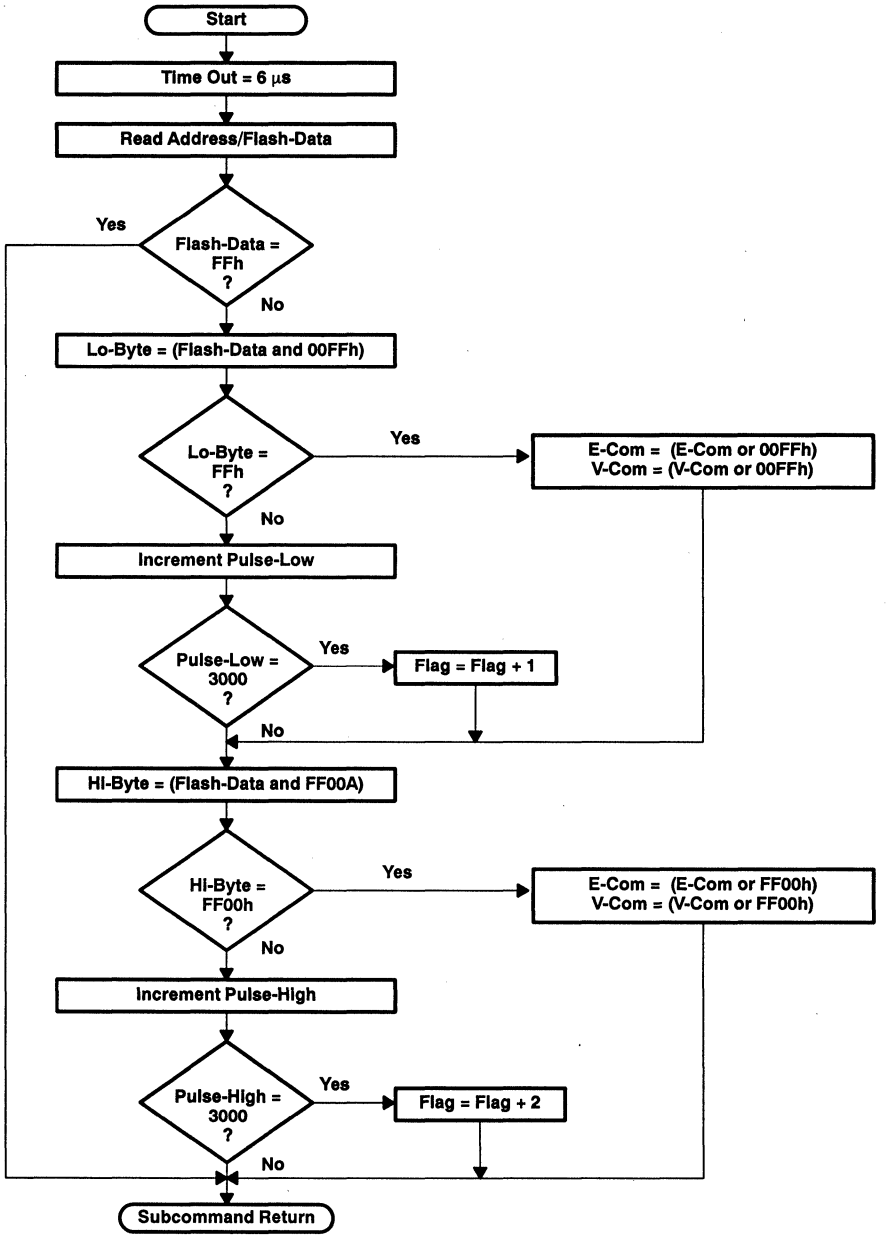
BUS OPERATION	COMMAND	COMMENTS
Write	Setup Program	Data = W-Com
Write	Write-Data	Valid Address Data (Write-Data)
Write	Program-Verify	Data = C-Com; Ends Programs Operations

erase algorithm for word-wide mode



BUS OPERATION	COMMAND	COMMENTS
Write	Erase	Data = 2020h
Write	Erase-Verify	Data = A0A0h

block erase verify and mask subroutine



PARAMETER MEASUREMENT INFORMATION

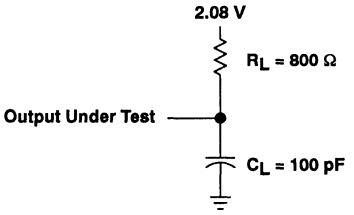
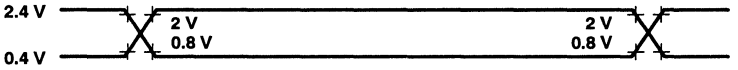


Figure 1. Load Circuit for Timing Parameters

Input/output wave forms for timing parameters



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

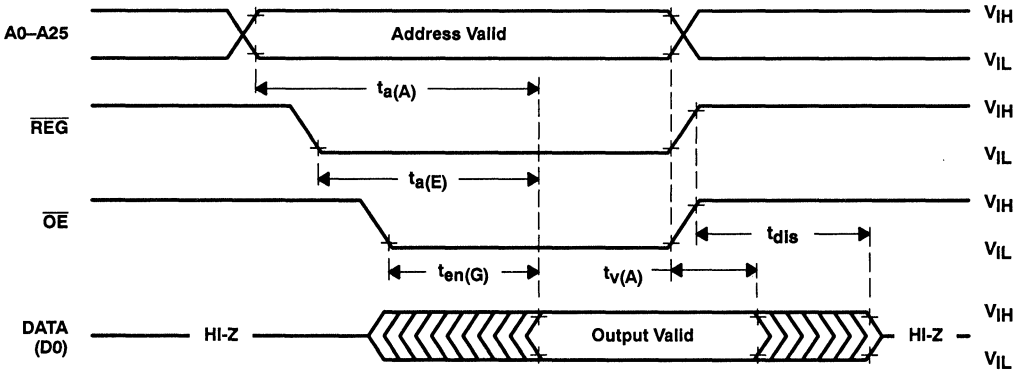
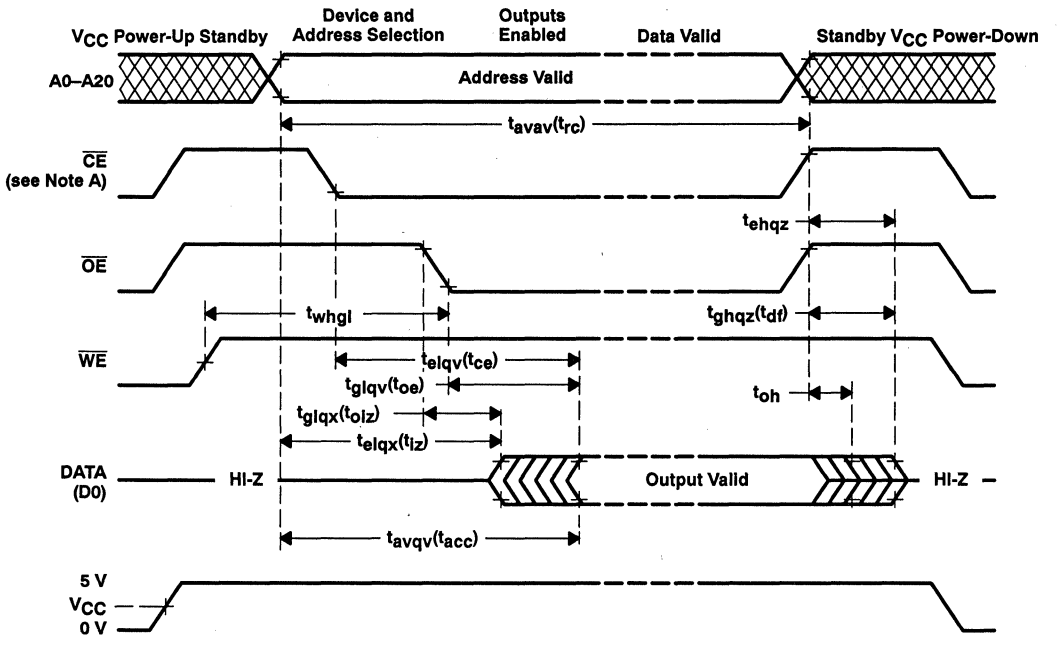


Figure 2. Attribute Memory Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 3. Read Operations Timing

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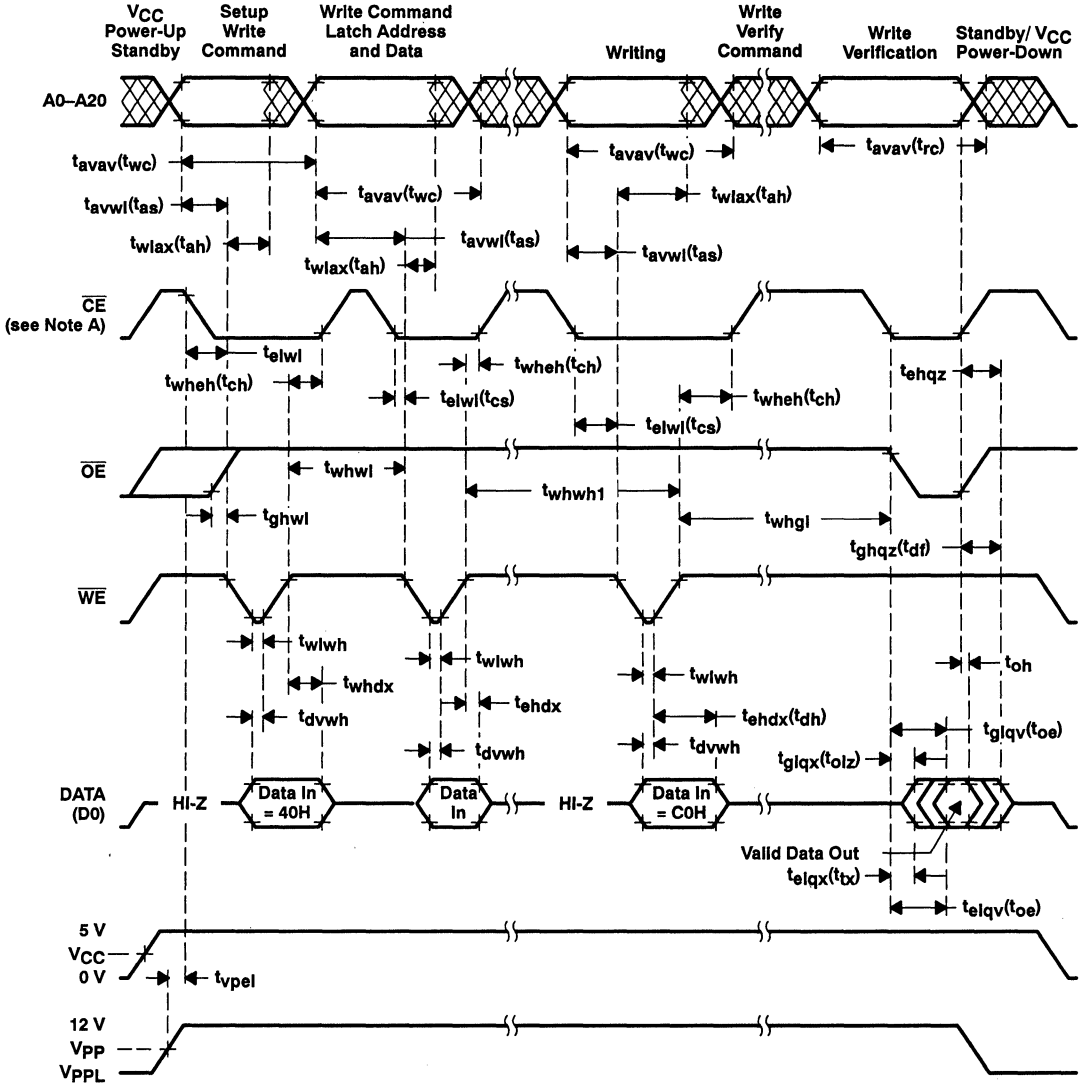
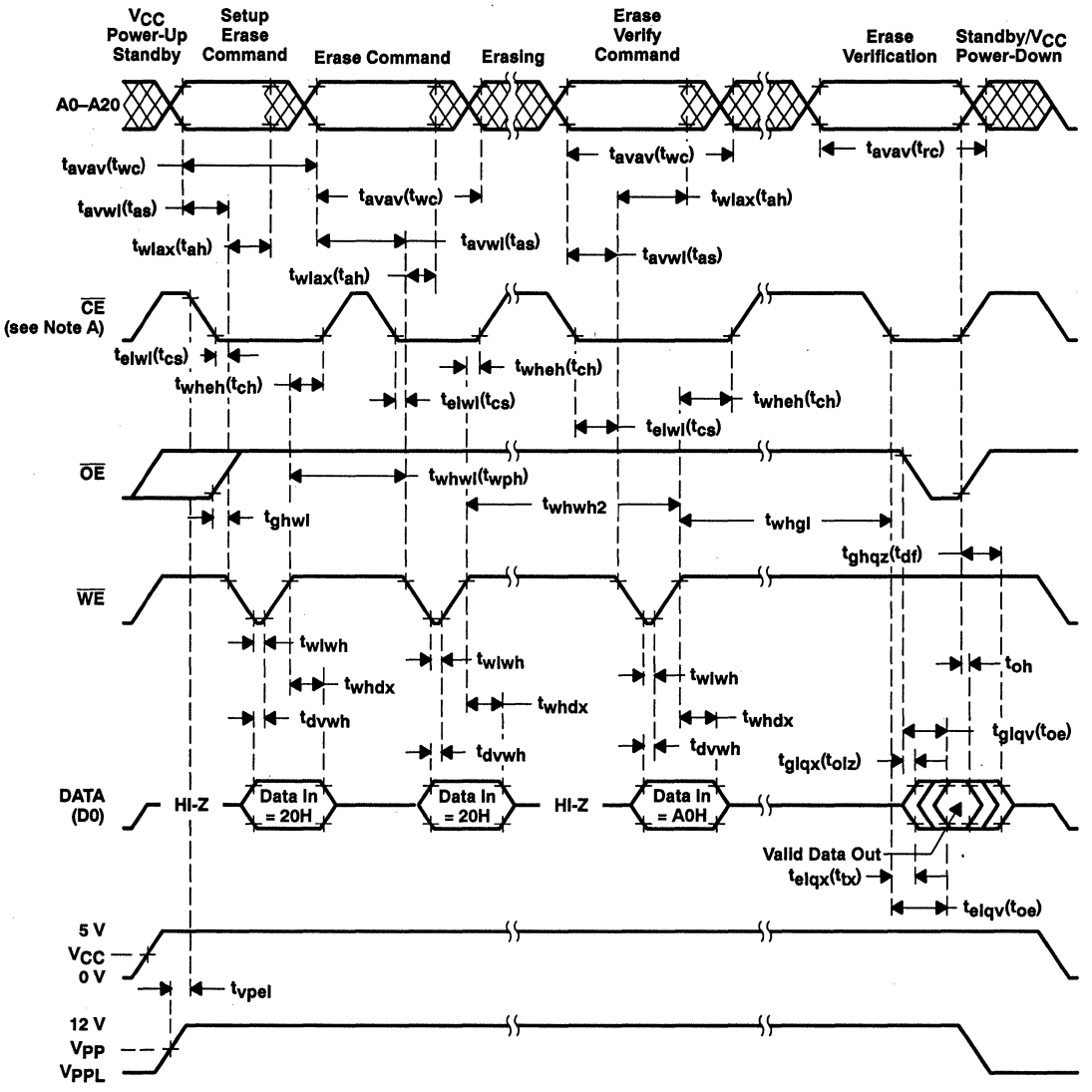
PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 4. Write Operations Timing

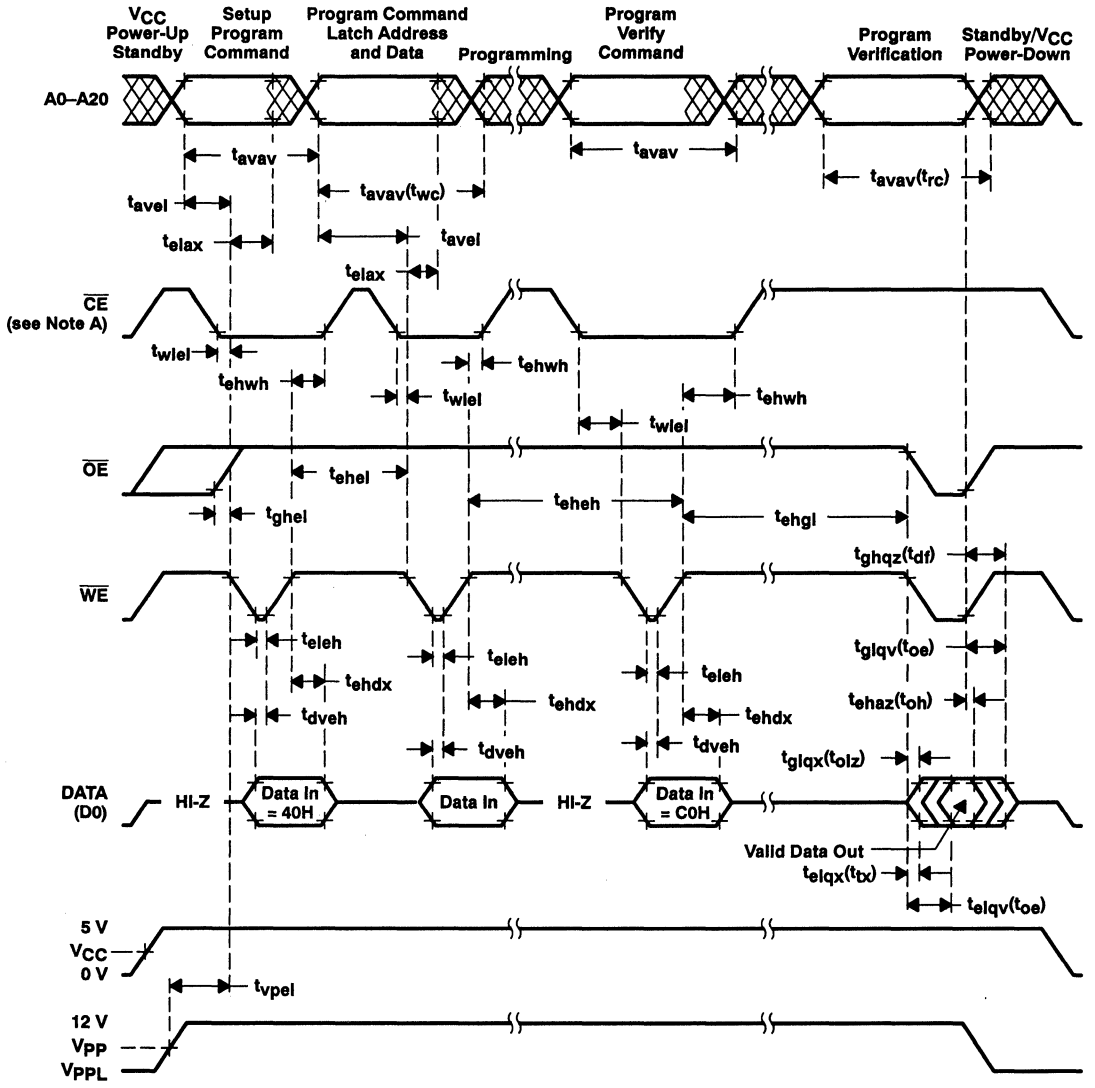
PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 5. Erase Operations Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{CE}$ refers to $\overline{CE1}$ and $\overline{CE2}$.

Figure 6. Write Operations Timing

- **Card Size (85 mm × 54 mm × 3.6 mm)**
- **Organization . . . From 64K × 8 to 256K × 16**
- **Single 5-V Power Supply (Read Mode)**
- **Utilizes QFP (Quad Flat Package) CMOS OTP PROMs (One Time Progammable Read-Only Memories)**
- **8-Bit or 16-Bit Data Width**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 55°C**
- **Standard 60-Pin Two-Piece Connector With Orientation Guide Allows Memory Technology/Capacity Upgrade/Downgrade**
- **All Inputs/Outputs and Clocks are Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**
  CMS2xx-200 200 ns Access Time (Max)
  CMS2xx-250 250 ns Access Time (Max)

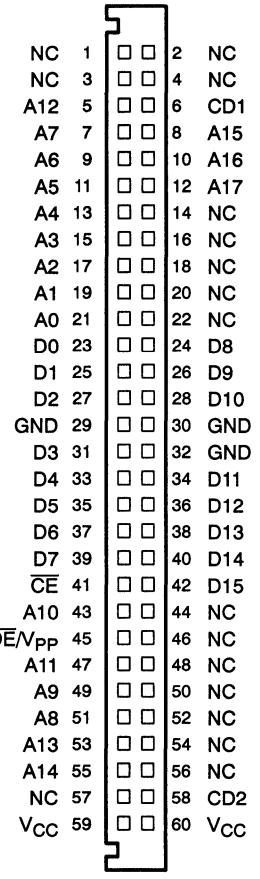
description

The CMS2xx series are TI standard Memory Cards designed to be used either as an internal memory system or as an external add-on memory.

These cards are offered with densities of 512K to 4 Megabit, one time electrically programmable read-only memories organized from 65 536 × 8 bits to 262 144 × 16 bits in a standard card package. A card is comprised of from 1 to 8 TMS27PC512s in 44-lead plastic quad flat packages (QFP) and one decoder in a 16-pin small outline package (SOP) mounted on top of the substrate together with three 0.1 μF decoupling capacitors.

The TMS27PC512 is described in the TMS27PC512 data sheet and is electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly.

60-PIN MEMORY CARD (CONNECTOR VIEW)



PIN NOMENCLATURE	
A0–A17	Address Input†
D0–D15	Data Output‡
$\overline{CE}$	Card Enable
$\overline{OE}$ / V_{PP}	Output Enable/Programming Voltage
CD1, CD2	Card Detect
GND	Ground
V_{CC}	5-V Power Supply
NC	No Connection

† Address signal A17 (pin12) is not connected for CMS209/213 and CMS210/214 cards. Address Signal A16 (pin 10) is not connected for CMS209/213 cards.

‡ Data out signals D8–D15 are not connected for all memory cards CMS213/214/216 organized by 8.

PRODUCT LIST	MEMORY CAPACITY (KB)	ORGANIZATION	ACCESS TIME (ns)	CONNECTOR TYPE
CMS209	128	64K × 16	200/250	Two-piece 60-pin
CMS210	256	128K × 16	200/250	Two-piece 60-pin
CMS212	512	256K × 16	200/250	Two-piece 60-pin
CMS213	64	64K × 8	200/250	Two-piece 60-pin
CMS214	128	128K × 8	200/250	Two-piece 60-pin
CMS216	256	256K × 8	200/250	Two-piece 60-pin

operation

The CMS2xx series operates as an array of TMS27PC512s and one decoder connected as shown in the functional block diagrams. The most significant address lines A16 and A17 are used to select one of the four possible device pairs. There are seven modes of operation listed in the following table.

programming

The CMS2xx series can be programmed using the TI SNAP! Pulse programming algorithm; refer to the TI TMS27PC512 data sheet for details of its operation.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAMMING INHIBIT	SIGNATURE MODE	
$\overline{CE}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{OE}/V_{PP}$	V_{IL}	V_{IH}	X	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X†	X	X	X	X	X	V_H‡	V_H
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
D0–D7	Data Out	HI–Z	HI–Z	Data In	Data Out	HI–Z	CODE	
							MFG	DEVICE
							97	85
D8–D15	Data Out	HI–Z	HI–Z	Data In	Data Out	HI–Z	97	85

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.
Refer to the appropriate TMS27PC512 data sheet for details of its operation.
This card has a device recognition mode.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.5 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... −0.5 V to 6.5 V
A9 ..... −0.5 V to 13.5 V
Output voltage range (see Note 1) ..... −0.5 V to V_{CC}
Operating free-air temperature range ..... 0°C to 55°C
Storage temperature range ..... −40°C to 70°C
Connector insertion cycle 5000

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	V
		Fast programming algorithm	5.75	6	6.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	V
$\overline{OE}/V_{PP}$	Supply voltage	Fast programming algorithm	12	12.5	13	V
		SNAP! Pulse programming algorithm	12.75	13.0	13.25	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
T_A	Operating free-air temperature		0		55	°C

NOTE 2: V_{CC} must be applied before or at the same time as $\overline{OE}/V_{PP}$ and removed after or at the same time as $\overline{OE}/V_{PP}$.

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -400$ mA	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 2.1$ mA		0.45	V
I_I	Input current (leakage)	$V_I = 0$ to 5.5 V		±10	μA
I_{OZH}	High-level output current (leakage)	All address inputs, $\overline{CE}$ or $\overline{OE} = V_{IH}$, $V_O = V_{CC}$		+10	μA
I_{OZL}	Low-level output current (leakage)	$\overline{CE}$ or $\overline{OE} = V_{IH}$, $V_O = 0$ V		−10	μA

PARAMETER			TEST CONDITIONS	CMS209	CMS210	CMS212	UNIT
I_{PP}	$\overline{OE}/V_{PP}$ supply current (during program pulse)		$V_{PP} = 13$ V	100	100	100	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{CE} = V_{IH}$ $V_{CC} = 5.5$ V	8	16	32	mA
		CMOS-input level	$\overline{CE} = V_{CC}$ $V_{CC} = 5.5$ V	7	14	28	mA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{CE} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open, address not complemented	100	100	100	mA

PARAMETER			TEST CONDITIONS	CMS213	CMS214	CMS216	UNIT
I_{PP}	$\overline{OE}/V_{PP}$ supply current (during program pulse)		$V_{PP} = 13$ V	50	50	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{CE} = V_{IH}$ $V_{CC} = 5.5$ V	4	8	16	mA
		CMOS-input level	$\overline{CE} = V_{CC}$ $V_{CC} = 5.5$ V	3.5	7	14	mA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{CE} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open, address not complemented	50	50	50	mA

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switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	CMS2xx-200		CMS2xx-250		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 PF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		200		250	ns
$t_{(CE)}$	Access time from chip enable			200		250	ns
$t_{en(OE/VPP)}$	Output enable time from $\overline{OE}$ /V_{PP}			75		120	ns
t_{dis}	Output disable time from $\overline{OE}$ /V_{PP} or $\overline{CE}$, whichever occurs first†		0	80	0	80	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{CE}$ or $\overline{OE}$ /V_{PP}, whichever occurs first†		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low.

4. Common test conditions apply for the t_{dis} except during programming.

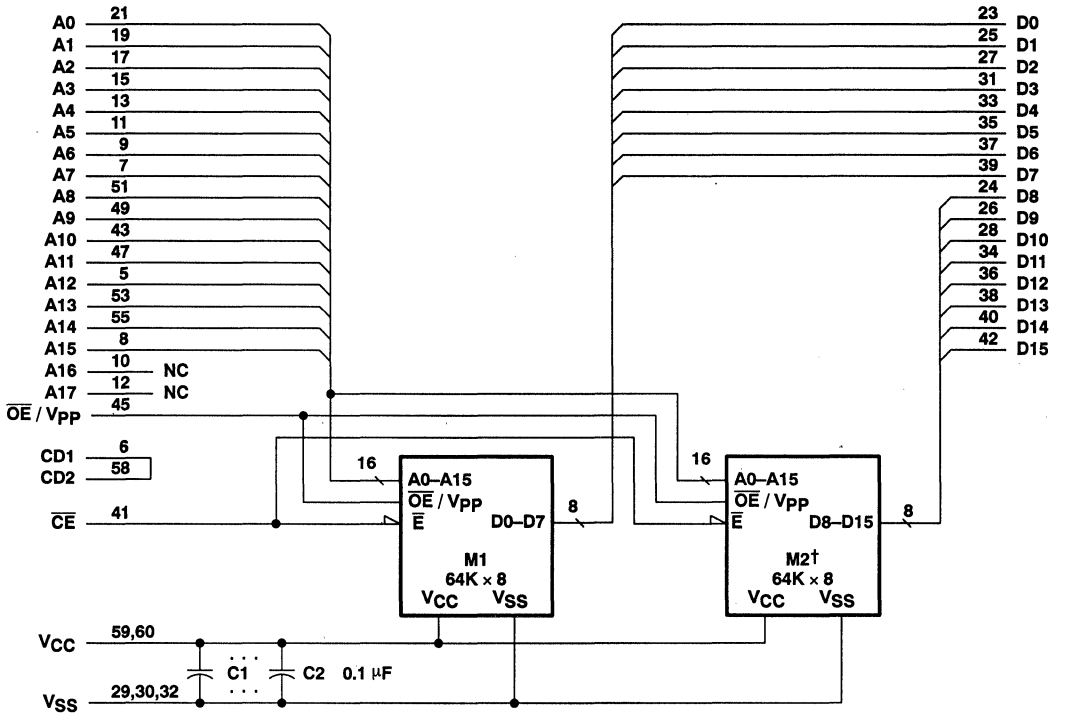
capacitance over recommended ranges of supply voltage and operating free-air temperature f = 1 MHz‡

PARAMETER			TEST CONDITIONS	MAX	UNIT
C_I	Input capacitance	CMS213	V_I = 0 V, f = 1 MHz, T_A = 25°C	10	pF
		CMS209		20	
		CMS214		20	
		CMS210		40	
		CMS216		40	
		CMS212		80	
$C_{I(OE/VPP)}$	Input capacitance, output enable/programming voltage	CMS213	V_I = 0 V, f = 1 MHz, T_A = 25°C	25	pF
		CMS209		50	
		CMS214		50	
		CMS210		100	
		CMS216		100	
		CMS212		200	
C_O	Output capacitance	CMS213	V_O= 0 V, f = 1 MHz, T_A = 25°C	15	pF
		CMS209		15	
		CMS214		30	
		CMS210		30	
		CMS216		60	
		CMS212		60	

‡ Capacitance measurements are made on sample basis only.

functional block diagram

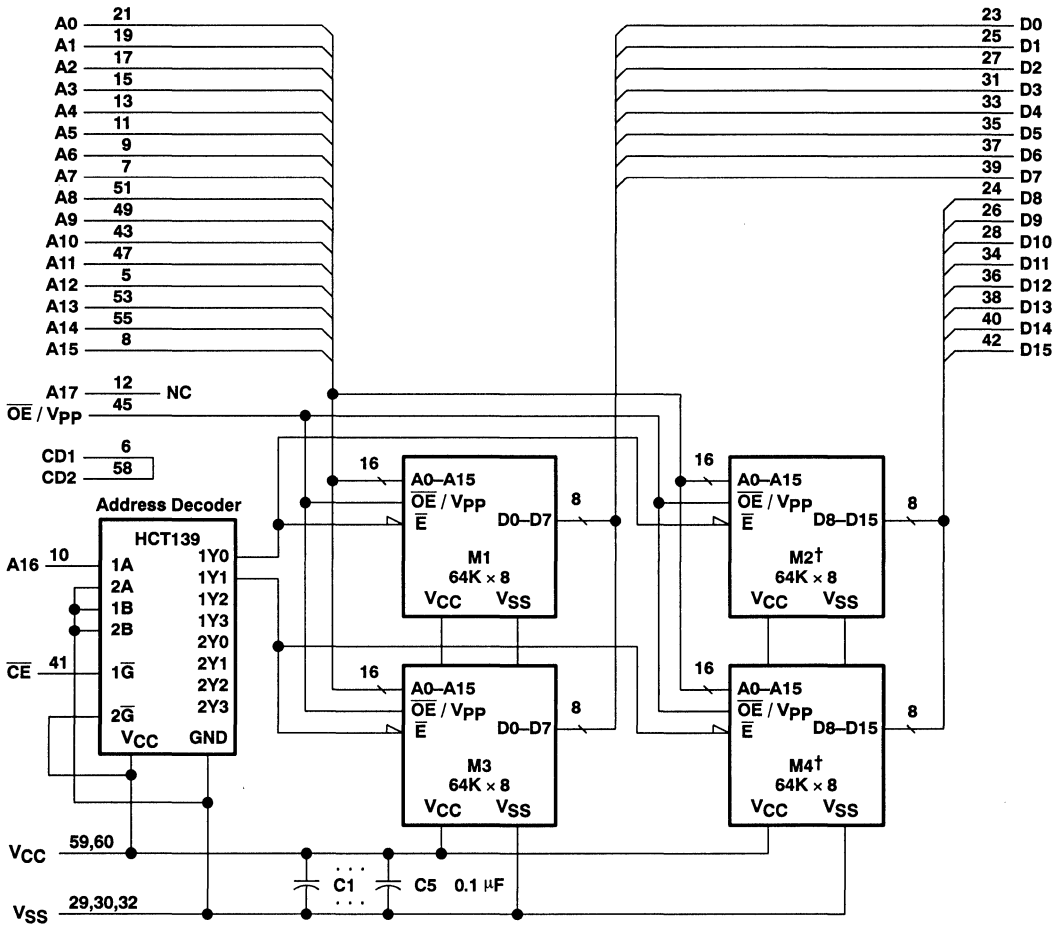
CMS209/CMS213



† Memory device M2 is used for CMS209 only.

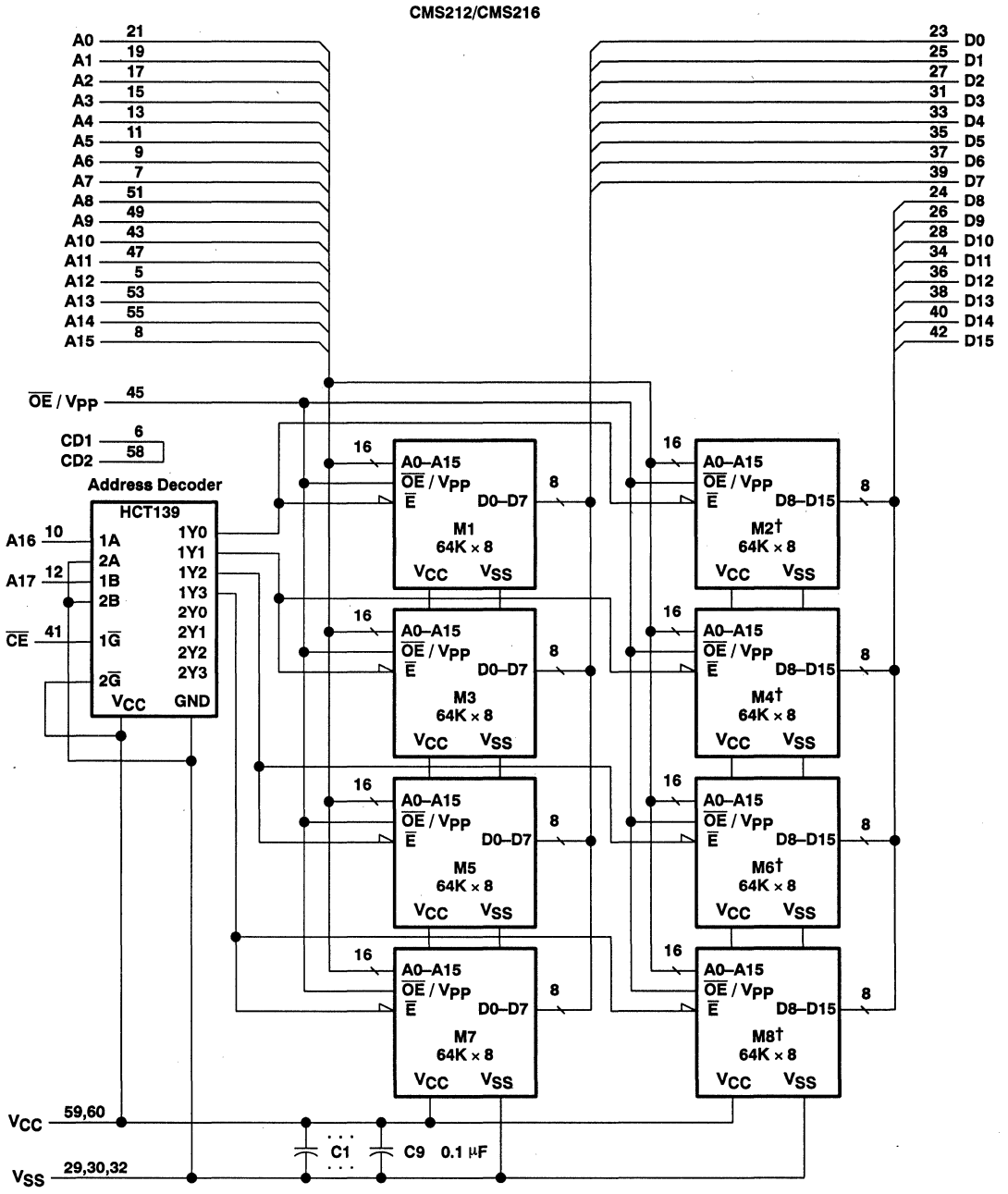
functional block diagram

CMS210/CMS214



† Memory devices M2 and M4 are used for CMS210 only.

functional block diagram



† Memory devices M2, M4, M6 and M8 are used for CMS212 only.

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DYNAMIC RAMS

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SMJ4C1024	1 048 576-bit	(1024K × 1) Enhanced Page Mode	9-27
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SMJ416100	16 777 216-bit	(16 385K × 1) Enhanced Page Mode	9-87
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VIDEO RAMS

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SMJ29F816	16 384-bit	(2K × 9) 5-V Flash EEPROM Serial JTAG Bus	9-285

This section contains Military MOS Memory data sheets.

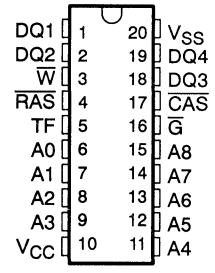
For additional information on Military devices and availability, please refer to the *Military Selection Guide* (literature number SCYC002), or contact your local TI Field Sales Office.

- – 55°C to 125°C Operating Free-Air Temperature Range
- Processed to MIL-STD-833, Class B
- Organization . . . 262 144 × 4
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

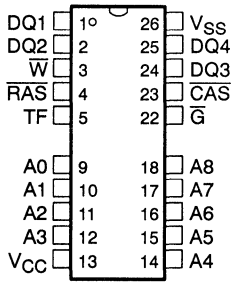
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44C256-80	80 ns	20 ns	40 ns	150 ns
SMJ44C256-10	100 ns	25 ns	45 ns	190 ns
SMJ44C256-12	120 ns	30 ns	55 ns	220 ns
SMJ44C256-15	150 ns	40 ns	70 ns	260 ns

- Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs and Clocks Are TTL Compatible
- Packaging Offered:
  - 20-Pin 300-Mil Ceramic DIP (JD Suffix)
  - 20-Lead Ceramic Surface-Mount Package (HJ Suffix)
  - 20-Terminal Low-Profile Leadless Ceramic Surface-Mount Package (HL Suffix)
  - 20-Terminal Leadless Ceramic Surface-Mount Package (FQ Suffix)
  - 20-Pin Ceramic Flat Pack (HK Suffix)
  - 20-Pin Ceramic Zig Zag In-Line Package (SV Suffix)

JD PACKAGE†
(TOP VIEW)

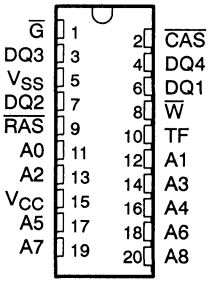


HJ, HL, AND FQ PACKAGES†
(TOP VIEW)

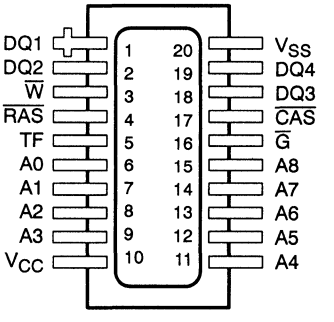


† The packages shown here are for pinout reference only. The HJ and FQ packages are actually 75% of the length of the JD package.

SV PACKAGE†
(TOP VIEW)



HK FLAT PACKAGE†
(TOP VIEW)



EPIC is a trademark of Texas Instruments Incorporated.

PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44C256 series are high-speed, 1 048 576-bit dynamic random access memories, organized as 262 144 words of four bits each. These devices employ EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

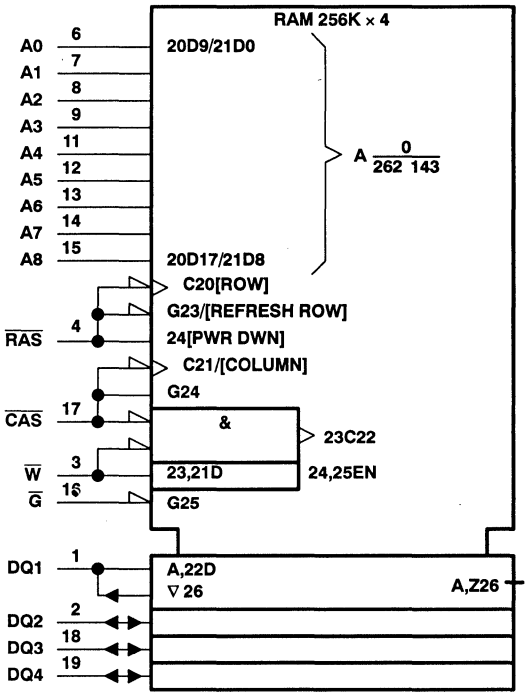
These devices feature maximum $\overline{RAS}$ access times of 80 ns, 100 ns,120 ns, and 150 ns. Maximum power dissipation is as low as 305 mW operating and 16.5 mW standby on 150-ns devices.

The EPIC technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a –1 V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

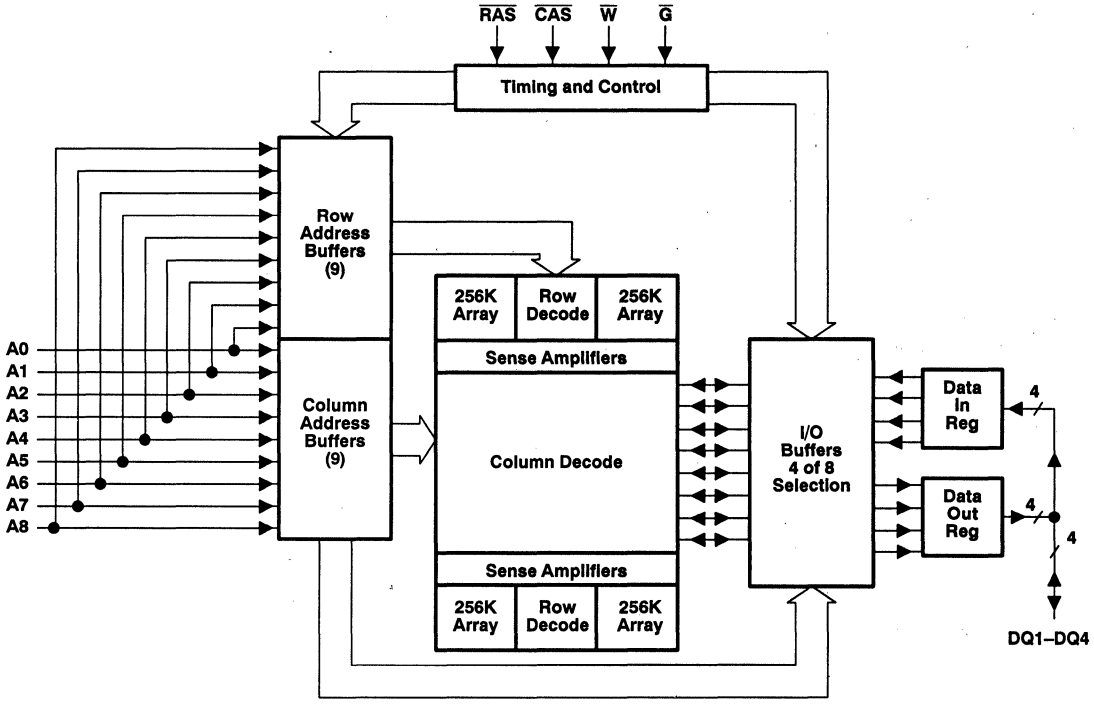
The SMJ44C256 is offered in 20-pin ceramic dual-in-line packages (JD suffix) and 20/26-terminal ceramic leadless carriers, 20/26-pin leaded carrier, a 20-pin flatpack, and a 20-pin ceramic zig-zag in-line package. They are specified for operation from –55°C to125°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the JD package.

functional block diagram



operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the SMJ44C256, $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation with $\overline{G}$ grounded.

data in (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines.

data out (DQ1–DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{G}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{\text{RAS}}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization (refresh) cycles is required after power-up to the full V_{CC} level.

test function pin

During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... 0 V to 7 V
Voltage range on any pin (see Note 1) ..... −1 V to 7 V
Short circuit output current ..... 50 mA
Continuous total power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	−55			°C
T_C	Case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10		±10	µA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		80		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or CBR)	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		75		65		55		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35		30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		HL/JD/FQ		HJ		HK		SV		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		6		7		8		9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7		7		8		8	pF
$C_{i(W)}$	Input capacitance, write-enable input		7		7		7		7	pF
C_O	Output capacitance		7		9		10		8	pF

NOTE 3: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30		40	ns
$t_{a(CA)}$	Access time from column-address	t_{AA}		40		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120		150	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		20		25		30		40	ns
$t_{a(CP)}$	Access time from column precharge	t_{CPA}		40		50		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}		20		25		30		35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 4)	t_{GOFF}		20		25		30		35	ns

NOTE 4: $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{G}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating temperature

		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		190		220		260		ns
$t_{c(rdW)}$	Cycle time, Read-write/read-modify-write	t_{RWC}	225		270		305		355		ns
$t_{c(P)}$	Cycle time, page-mode read or write (see Note 7)	t_{PC}	50		55		65		80		ns
$t_{c(PM)}$	Cycle time, page-mode read-modify-write	t_{PRWC}	115		135		150		175		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10 000	25	10 000	30	10 000	40	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		80		90		100		ns
$t_{w(RL)}$	Pulse duration, non-page-mode $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10 000	100	10 000	120	10 000	150	10 000	ns
$t_{w(RL)P}$	Pulse duration, page-mode $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100 000	100	100 000	120	100 000	150	100 000	ns
$t_{w(WL)}$	Pulse duration, write low	t_{WP}	15		15		20		25		ns
$t_{su(CA)}$	Setup time, column-address before $\overline{CAS}$ low	t_{ASC}	5		5		5		5		ns
$t_{su(RA)}$	Setup time, row-address before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data before $\overline{W}$ low (see Note 10)	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	t_{CWL}	20		25		30		40		ns
$t_{su(WRH)}$	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	t_{RWL}	20		25		30		40		ns
$t_{h(CA)}$	Hold time, column-address after $\overline{CAS}$ low (see Note 10)	t_{CAH}	15		20		20		25		ns
$t_{h(RA)}$	Hold time, row-address after $\overline{RAS}$ low	t_{RAH}	15		15		15		15		ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To assure $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.

timing requirements over recommended ranges of supply voltage and operating temperature (continued)

		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RLCA)}$	Column-address hold time, after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		100		ns
$t_{h(D)}$	Data hold time, after $\overline{CAS}$ low (see Note 10)	t_{DH}	15		20		25		30		ns
$t_{h(RLD)}$	Data hold time, after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		110		ns
$t_{h(WLGL)}$	Hold time, $\overline{G}$ high after $\overline{W}$ low	t_{GH}	20		25		30		40		ns
$t_{h(CHrd)}$	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	t_{RRH}	10		10		10		10		ns
$t_{h(CLW)}$	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		30		ns
$t_{h(RLW)}$	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 12)	t_{WCR}	65		75		90		105		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 15)	t_{CWD}	60		70		80		90		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	t_{RCD}	30	60	30	75	30	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	t_{RAD}	20	40	20	55	20	65	25	80	ns

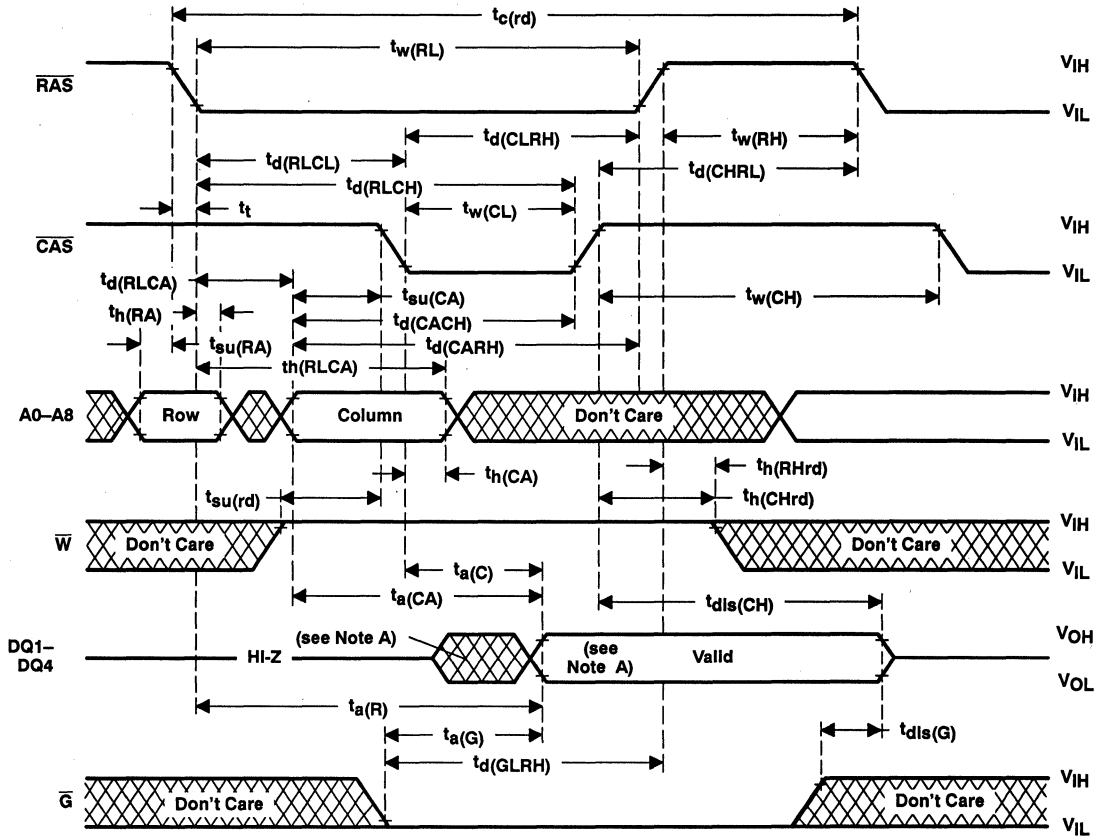
NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Maximum value specified only to assure access time.
14. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisified for a read cycle.
15. Read-modify-write operation only.

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)

		ALT. SYMBOL	'44C256-80		'44C256-10		'44C256-12		'44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	40		45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	40		45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 15)	t_{RWD}	130		150		170		200		ns
$t_{d(CAWL)}$	Delay time, column-address to $\overline{W}$ low (see Note 15)	t_{AWD}	80		95		105		120		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	20		25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		30		40		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time (see Note 17)	t_T									ns

NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
15. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
17. System transition times (rise and fall) are to be a minimim of 3 ns and a maximim of 50 ns.

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 1. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

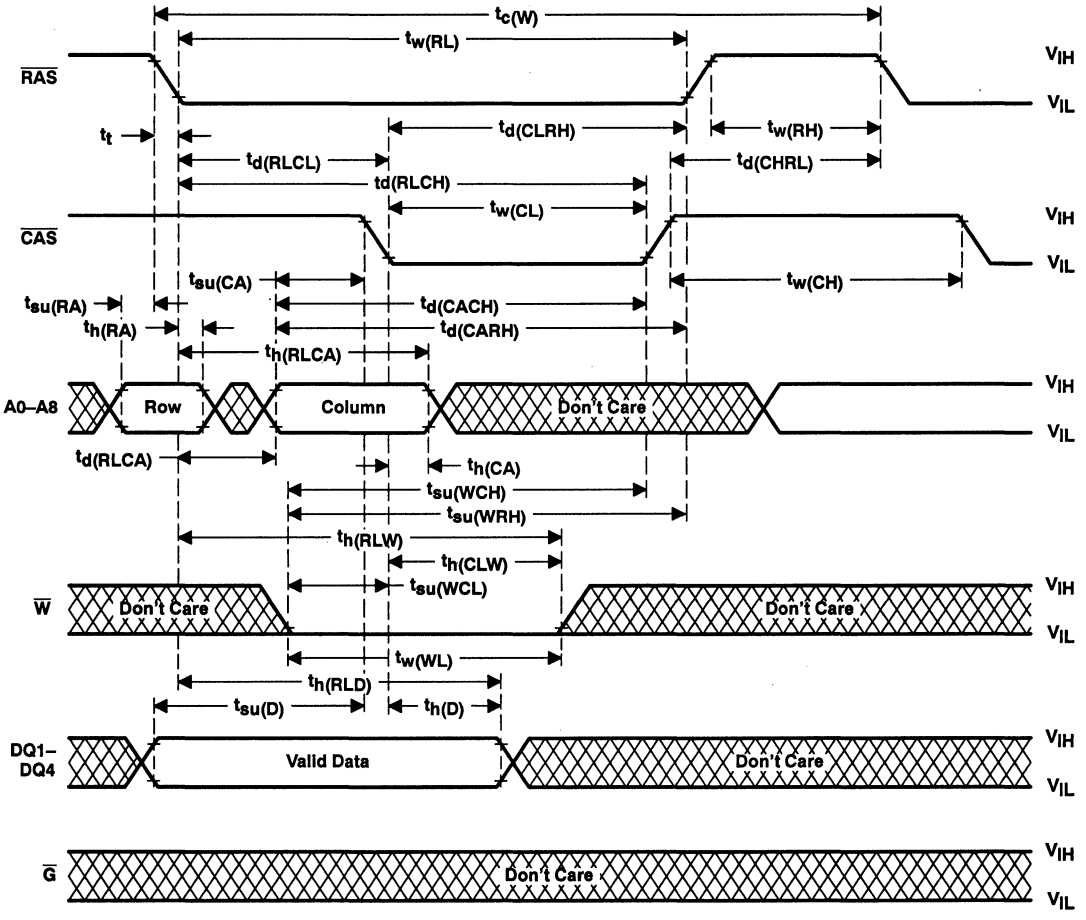


Figure 2. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

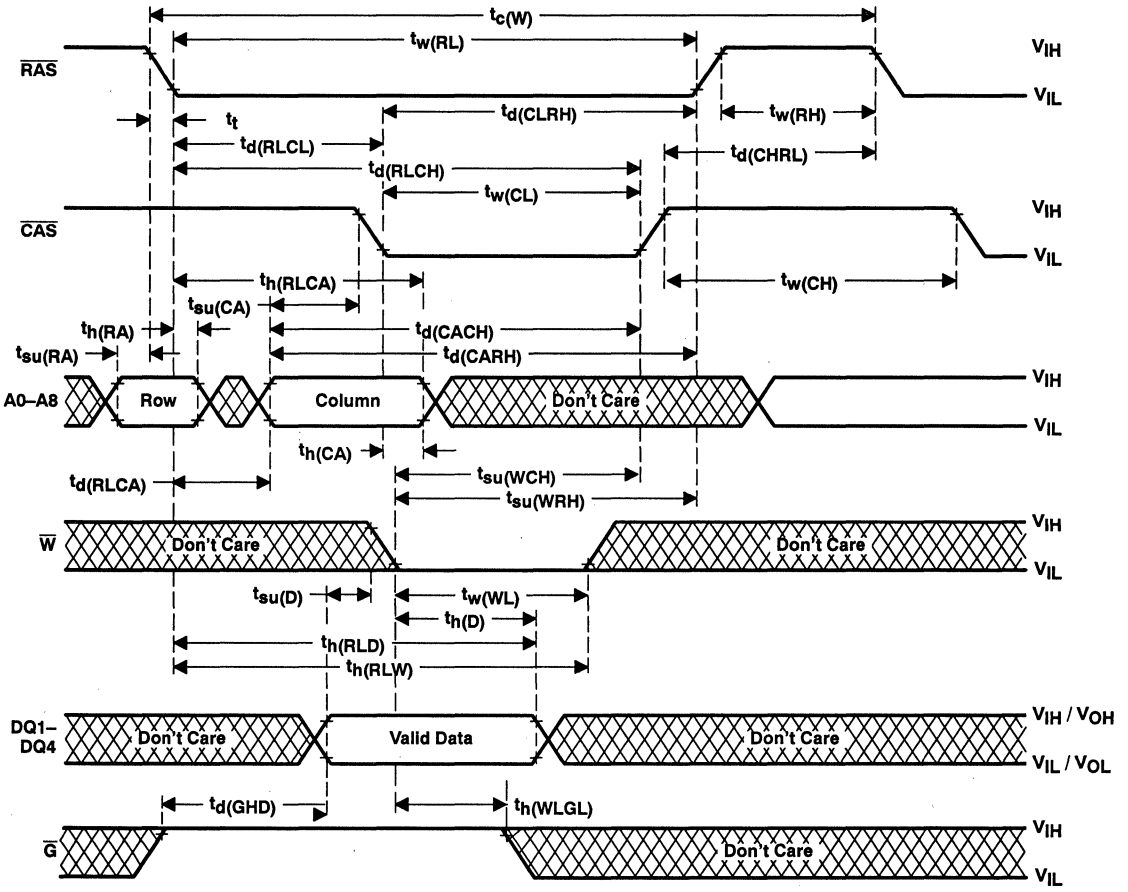
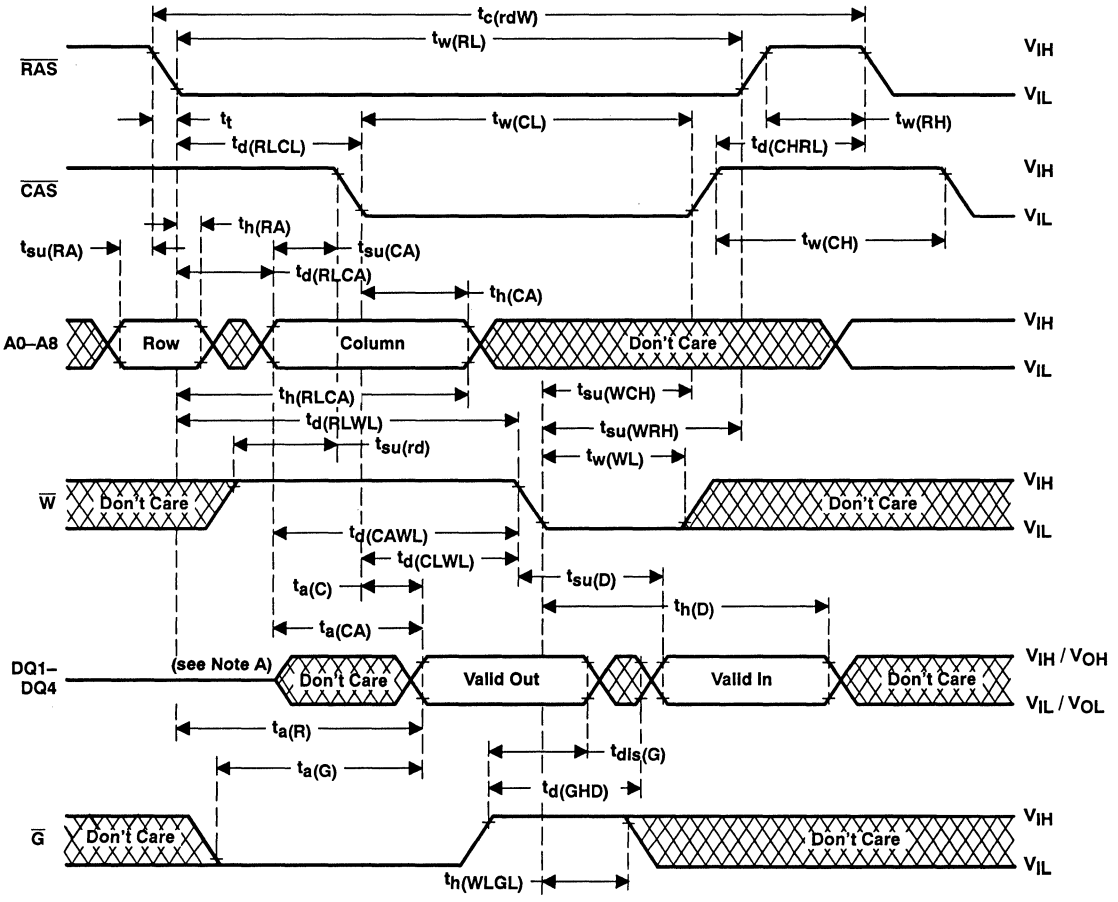


Figure 3. Write Cycle Timing

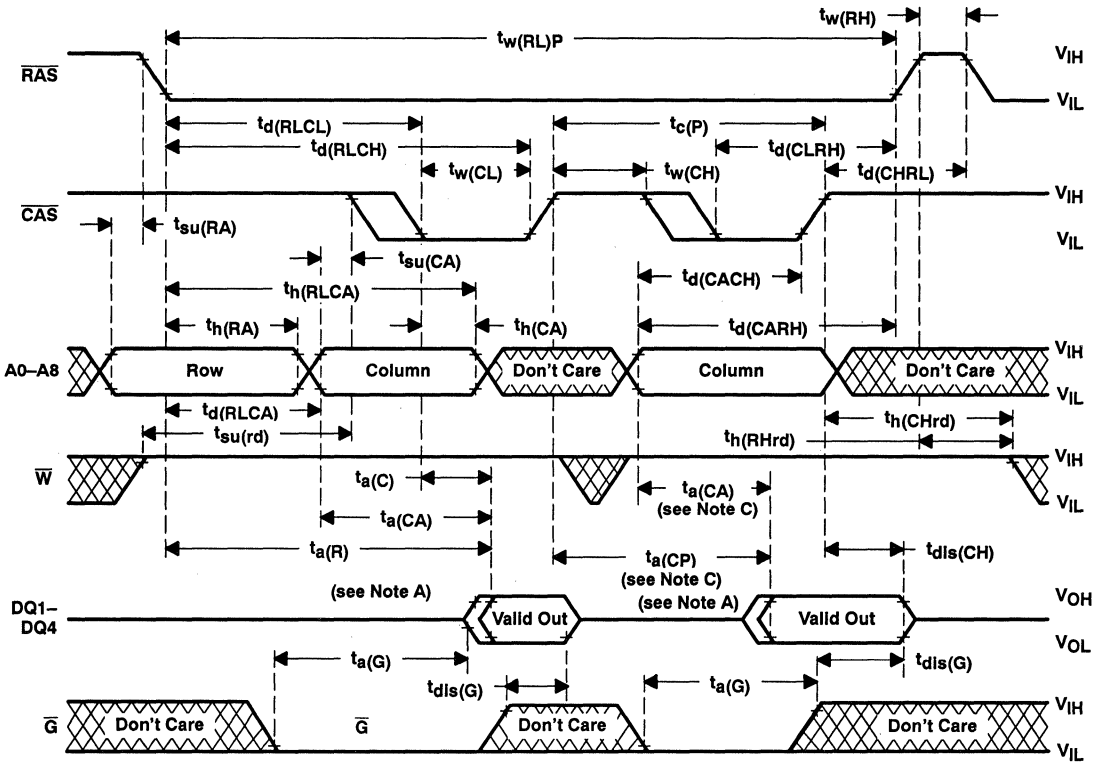
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from high impedance to an invalid data state prior to the specified access time.

Figure 4. Read-Write/Read-Modify-Write Cycle Timing

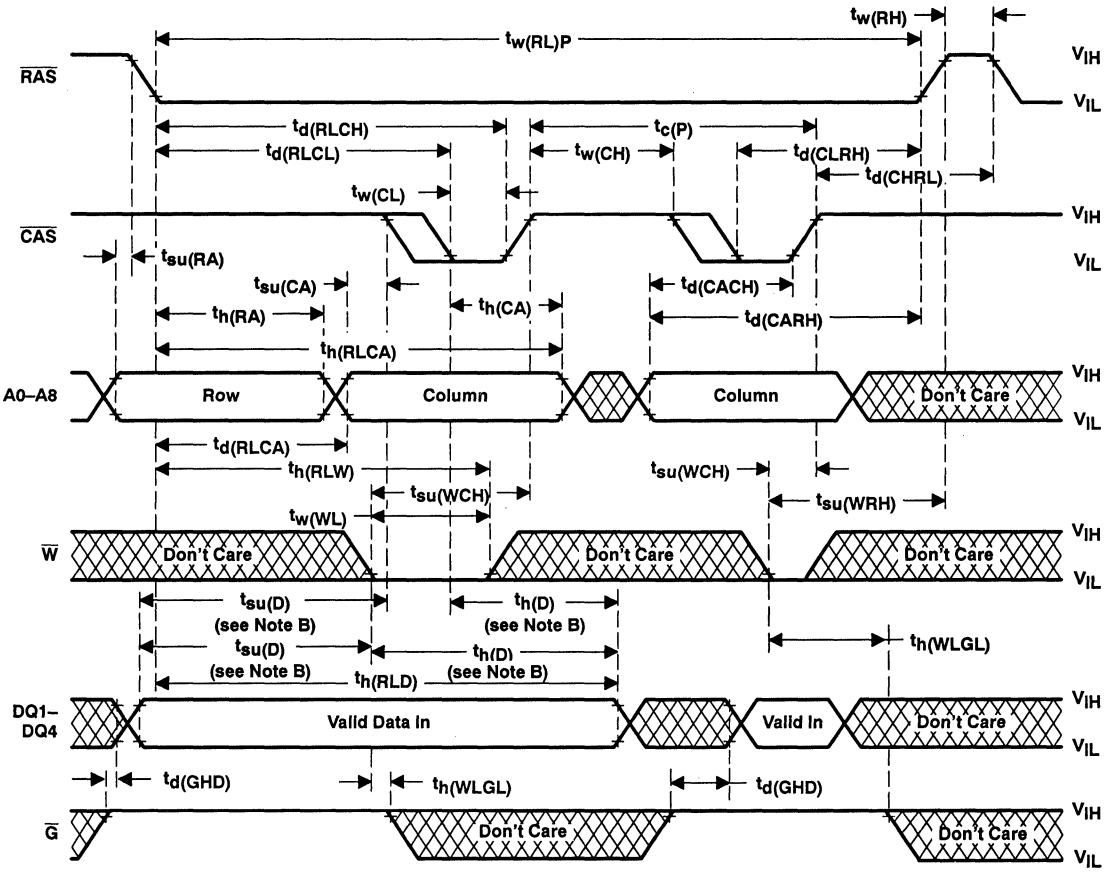
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from high-impedance to an invalid data state prior to the specified access time.
B. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

Figure 5. Enhanced Page-Mode Read Cycle Timing

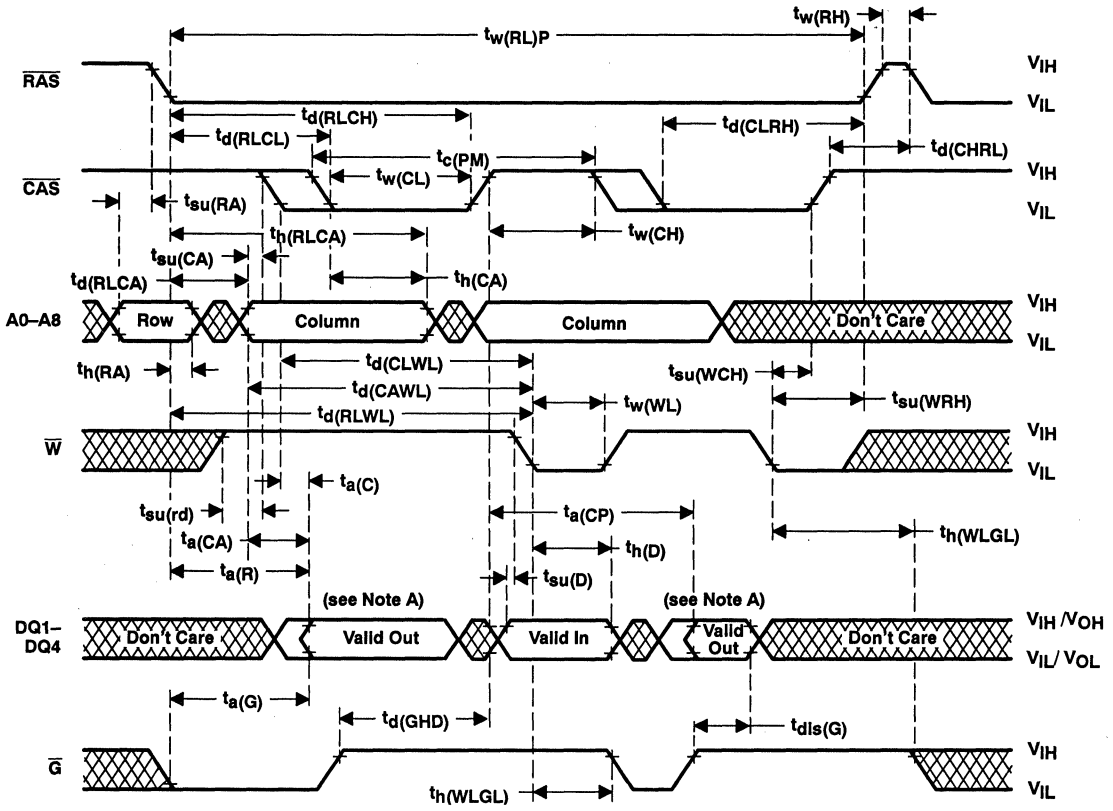
PARAMETER MEASUREMENT INFORMATION



NOTES: A. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
B. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

Figure 6. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from high-impedance to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

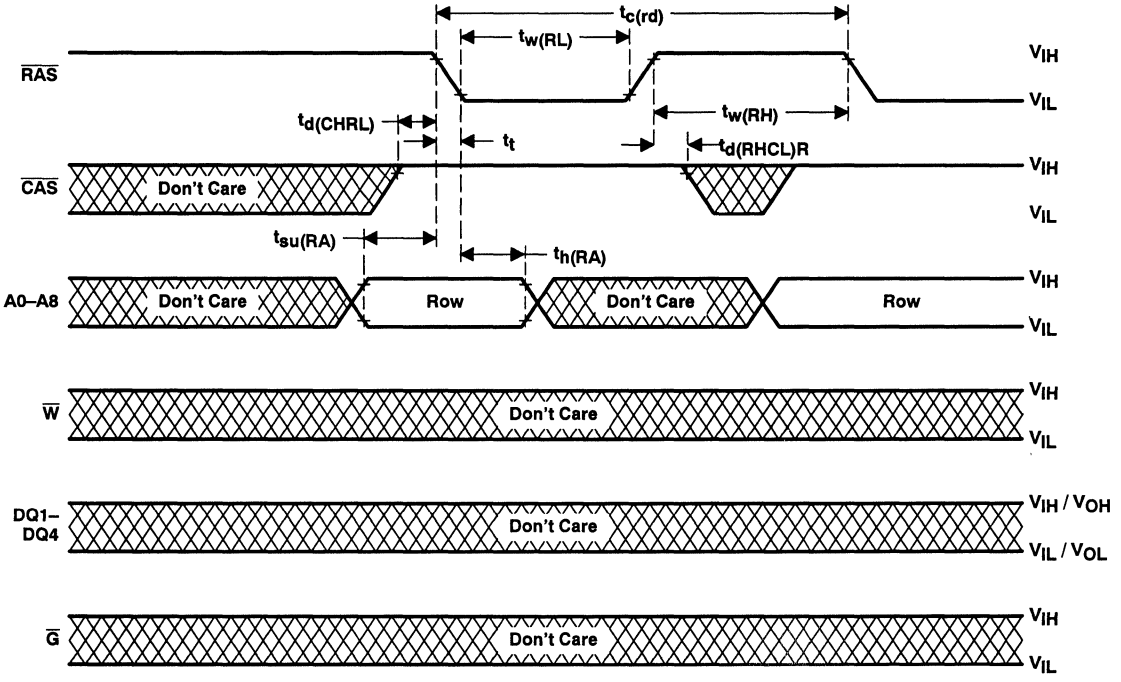


Figure 8. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

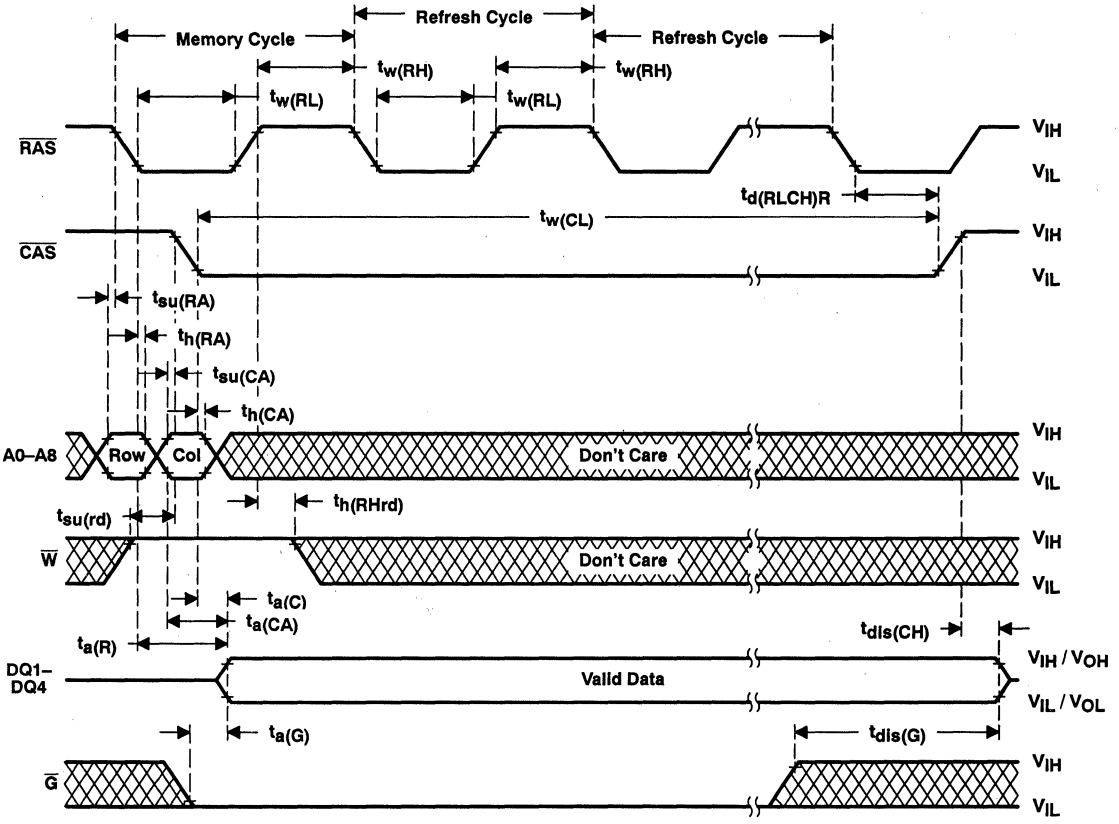


Figure 9. Hidden Refresh Cycle (Enhanced Page Mode)

PARAMETER MEASUREMENT INFORMATION

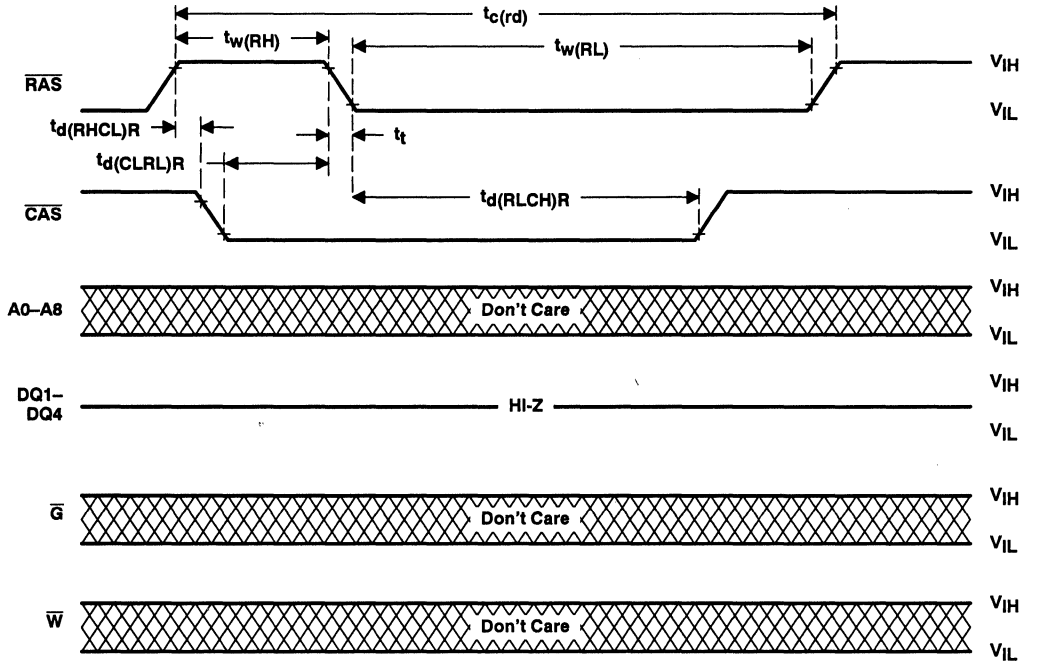
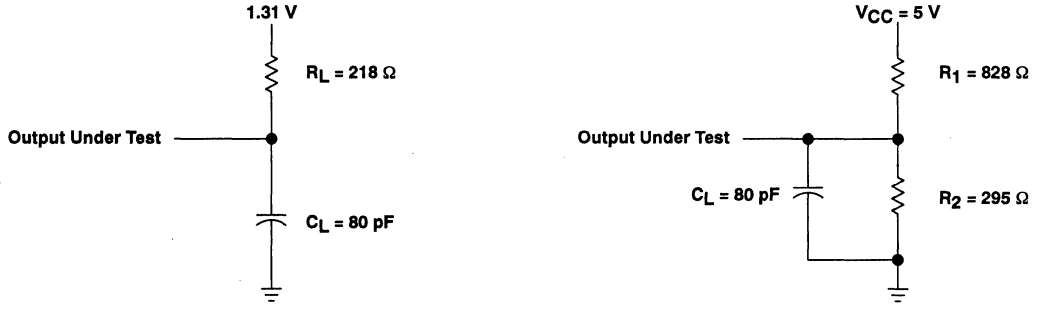


Figure 10. Automatic (CAS-Before-RAS) Refresh Cycle Timing



(a) Load Circuit (b) Alternate Load Circuit

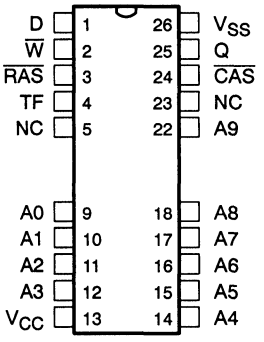
Figure 11. Load Circuits for Timing Parameters

- Processed to MIL-STD-883, Class B
- Operating Temperature Range . . . – 55°C to 125°C
- Organization . . . 1 048 576 × 1
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

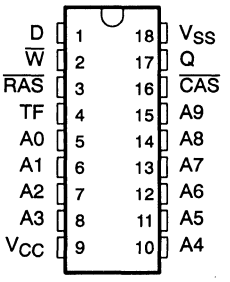
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4C1024-80	80 ns	20 ns	40 ns	150 ns
'4C1024-10	100 ns	25 ns	45 ns	190 ns
'4C1024-12	120 ns	30 ns	55 ns	220 ns
'4C1024-15	150 ns	40 ns	70 ns	260 ns

- Enhanced Page Mode Operation for Faster Memory Access
  - Higher Data Bandwidth Than Conventional Page-Mode Parts
  - Random Single-Bit Access Within a Row With a Column Address
- One of TI's CMOS Megabit DRAM Family Including:
  SMJ44C256 — 256K × 4 Enhanced Page Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs/Outputs and Clocks Are TTL Compatible
- Packaging Offered:
  - 18-Pin 300-Mil Ceramic DIP (JD Suffix)
  - 20/26-Lead Ceramic Surface Mount Package (HJ Suffix)
  - 20/26-Terminal Leadless Ceramic Surface Mount Package (FQ/HL Suffixes)
  - 20-Pin Ceramic Flat Pack (HK Suffix)
  - 20-Pin Ceramic Zig-Zag In-Line Package (SV Suffix)

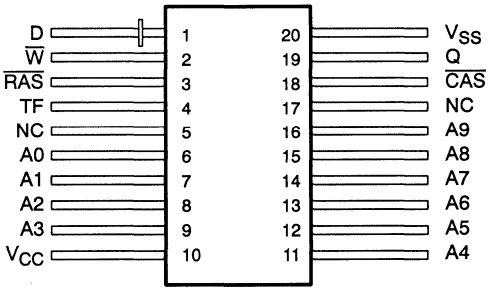
HJ / HL / FQ PACKAGES† (TOP VIEW)



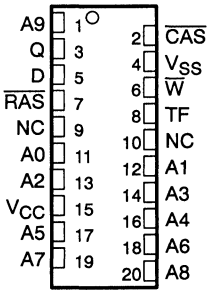
JD PACKAGE† (TOP VIEW)



HK PACKAGE† (TOP VIEW)



SV PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

EPIC is a trademark of Texas Instruments Incorporated.

description

The SMJ4C1024 is a high-speed, 1 048 576-bit dynamic random-access memory organized as 1 048 576 words of one bit each. It employs EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

This device features maximum $\overline{RAS}$ access times of 80 ns, 100 ns, 120 ns, and 150 ns. Maximum power dissipation is as low as 305 mW operating and 16.5 mW standby on 150 ns devices.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 140 mA typical, and a –1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4C1024 is offered in an 18-pin ceramic dual-in-line package (JD suffix), a 20/26-terminal ceramic leadless carrier package, a 20/26-pin leaded carrier package, a 20-pin flatpack, and a 20-pin ceramic zig-zag in-line package. They are characterized for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ4C1024 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the same $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Twenty address bit are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data-in is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The 3-state output buffers provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

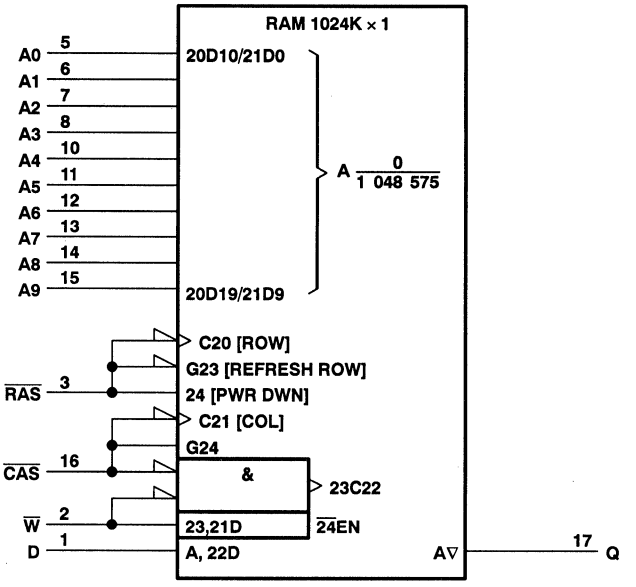
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved.

test function pin

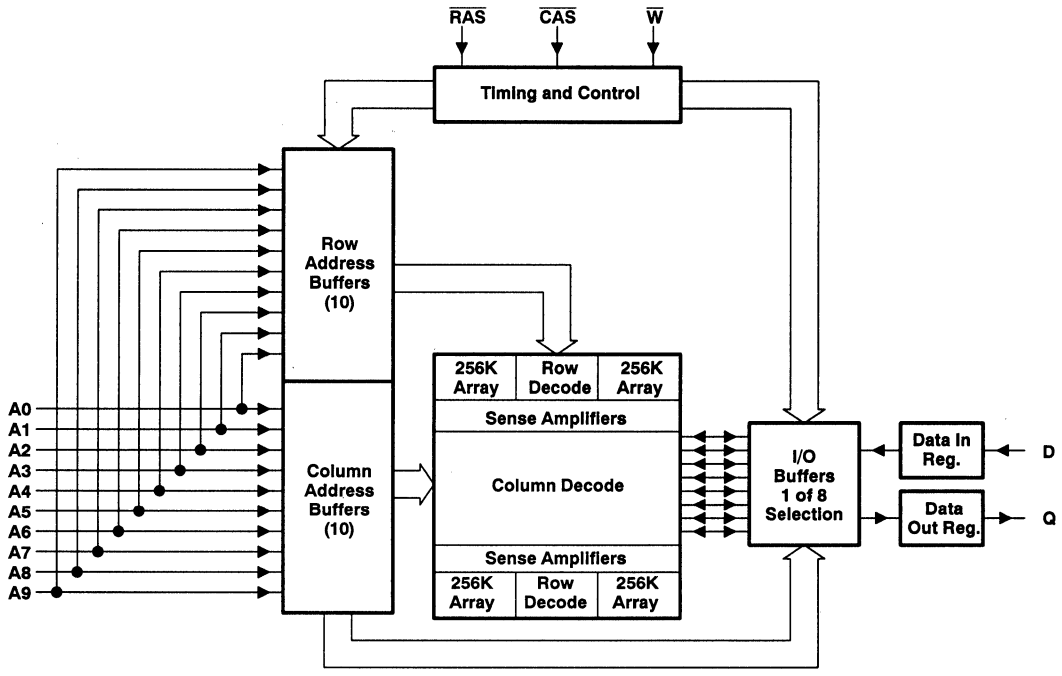
During normal device operation the TF pin must be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 18-pin JD package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature range ..... – 55°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Minimum operating free-air temperature	– 55			°C
T_C	Maximum operating case temperature	0		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		75		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3		3	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		70		65		55		50	mA
I_{CC4}	Average page current	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		45		35		30	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		HL / JD / FQ		HJ		HK		SV		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		6		7		8		9	pF
$C_{i(D)}$	Input capacitance, data input		5		5		6		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7		7		8		8	pF
$C_{i(W)}$	Input capacitance, write-enable input		7		7		7		7	pF
C_o	Output capacitance		7		9		10		8	pF

NOTE 3: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER		ALT. SYMBOL	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		20		25		30		40	ns
$t_{(CA)}$	Access time from column address	t_{AA}		40		45		55		70	ns
$t_{(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		80		100		120		150	ns
$t_{a(CP)}$	Access time from column precharge	t_{CPA}		40		40		60		75	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)	t_{OFF}		20		25		30		35	ns

NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven. The output is disabled by bringing $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	150		190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	150		190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	175		220		265		315		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	50		55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PRWC}	75		85		110		135		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10000	25	10000	30	10000	40	10000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	60		80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	80	10000	100	10000	120	10000	150	10000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	80	100000	100	100000	120	100000	150	100000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		3		3		3		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		0		ns
$t_{su(WCL)}$	W-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		0		ns
$t_{su(WCH)}$	W-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		30		40		ns
$t_{su(WRH)}$	W-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		30		40		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	12		15		15		20		ns

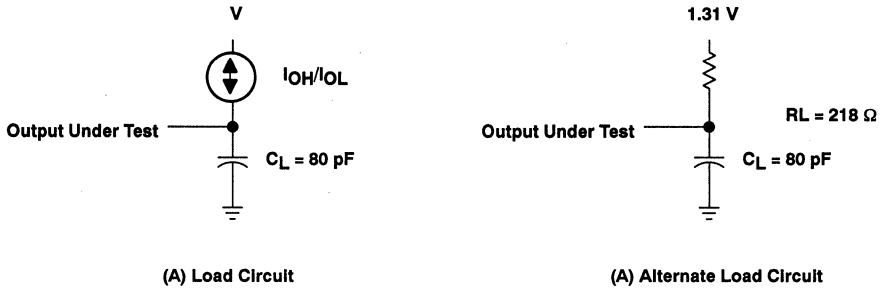
NOTES: 5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To assure $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	'4C1024-80		'4C1024-10		'4C1024-12		'4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RCLA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	60		70		80		100		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	15		20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	60		70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	15		20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	60		70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		40		50		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	22	60	28	75	28	90	33	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	17	40	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	40		45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	40		45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	80		100		130		160		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	40		45		65		80		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	20		25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8		8	ms
t_t	Transition time (see Note 17)	—	—		—		—		—		ns

NOTES: 10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set $t_{d(RLCL)}$ min as a reference.
13. Read -modify-write operation only.
14. Maximum value specified only to assure access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
17. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and a maximum of 50 ns.

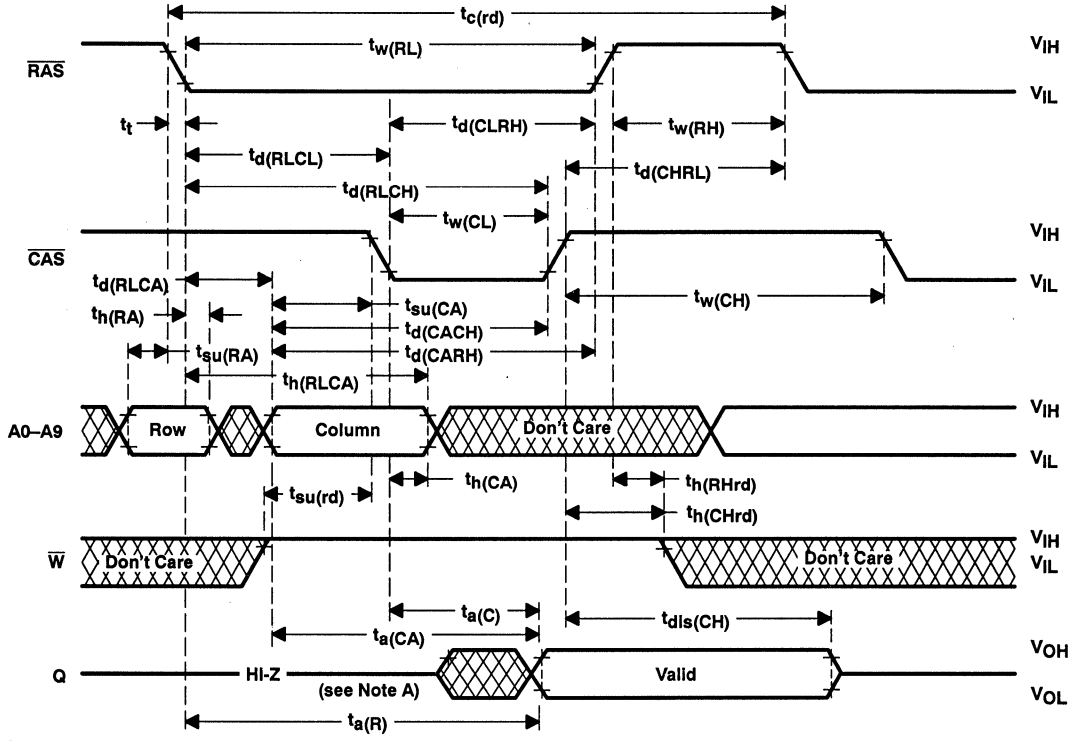
PARAMETER MEASUREMENT INFORMATION



(A) Load Circuit

(A) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters



NOTE A: Output may go from high impedance to an invalid state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

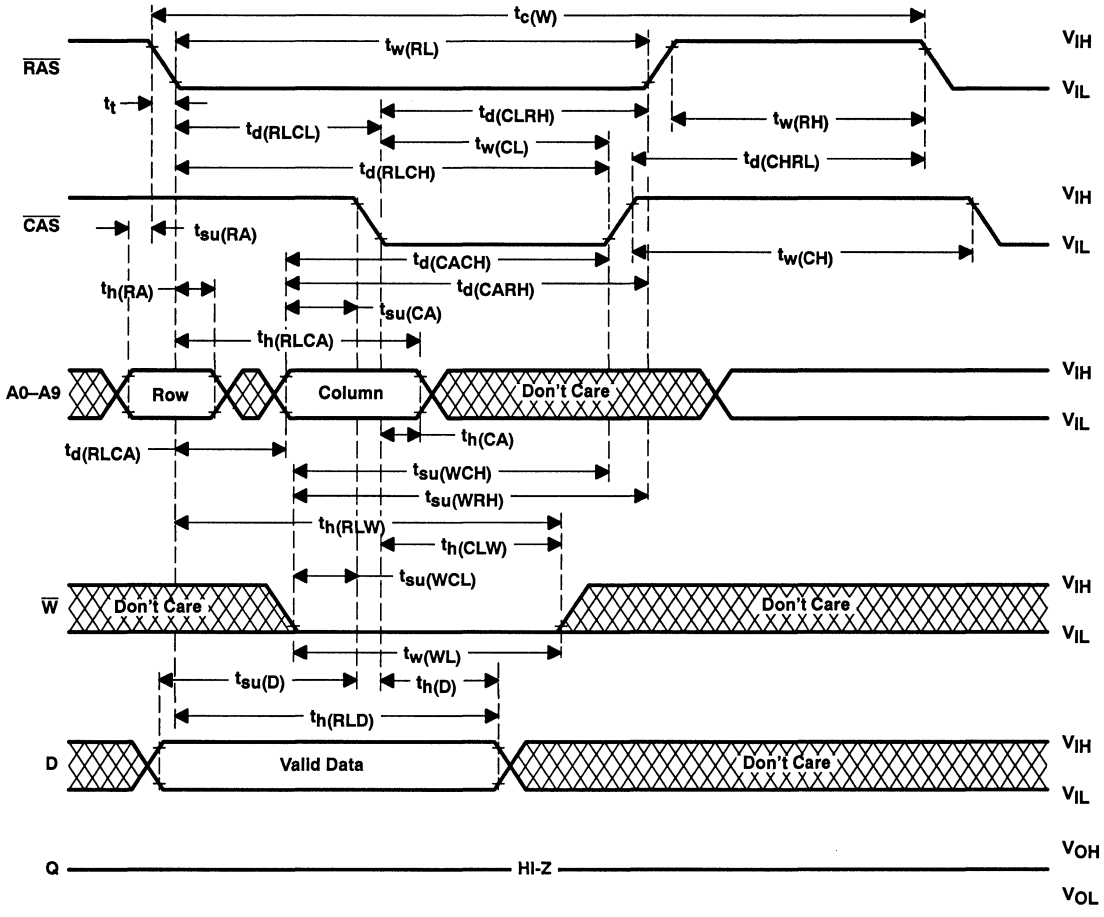


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

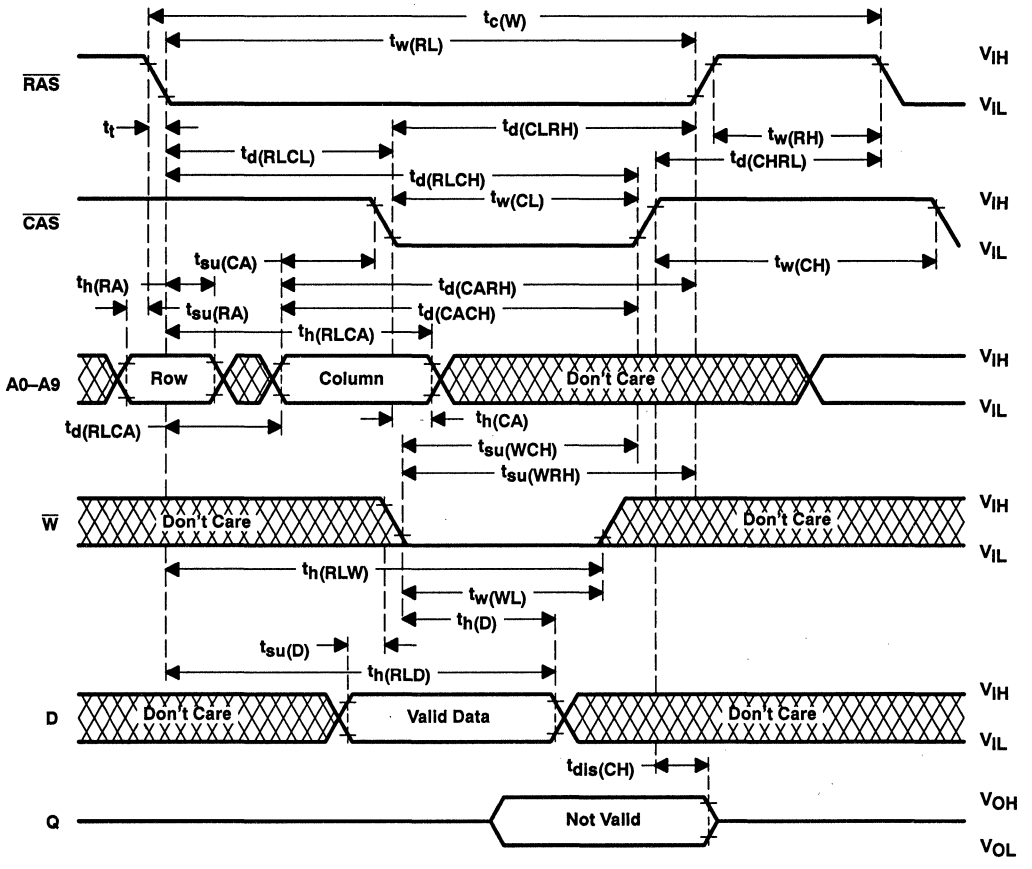
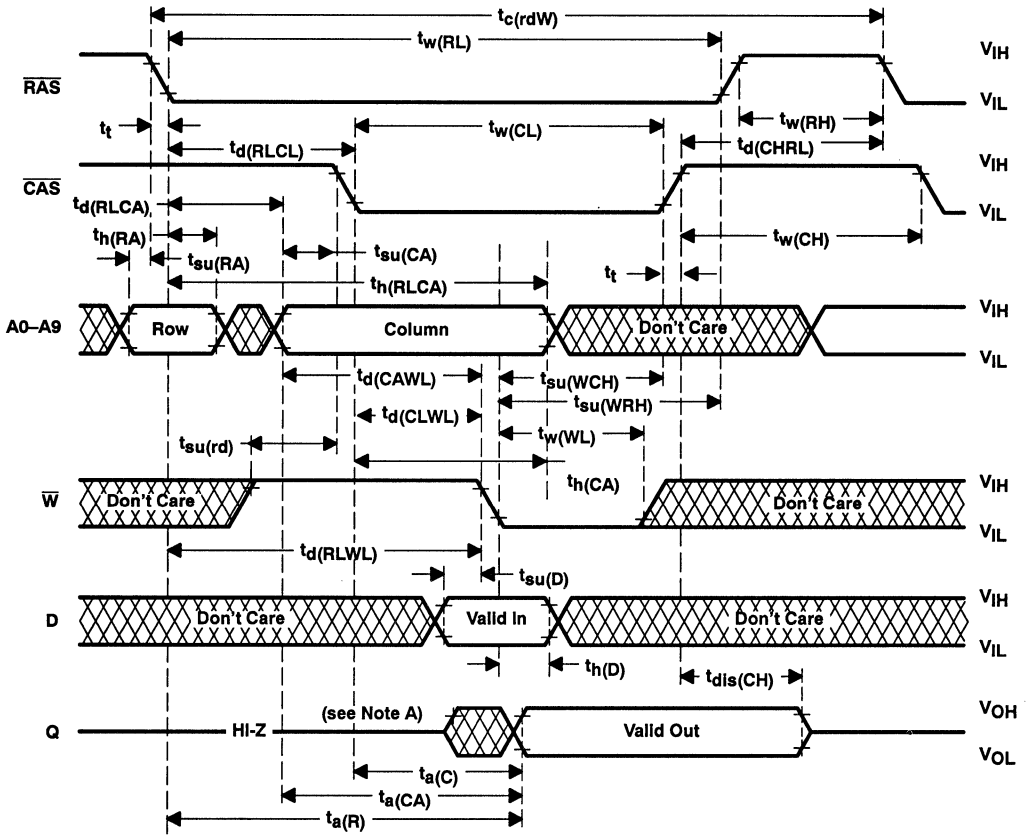


Figure 4. Write Cycle Timing

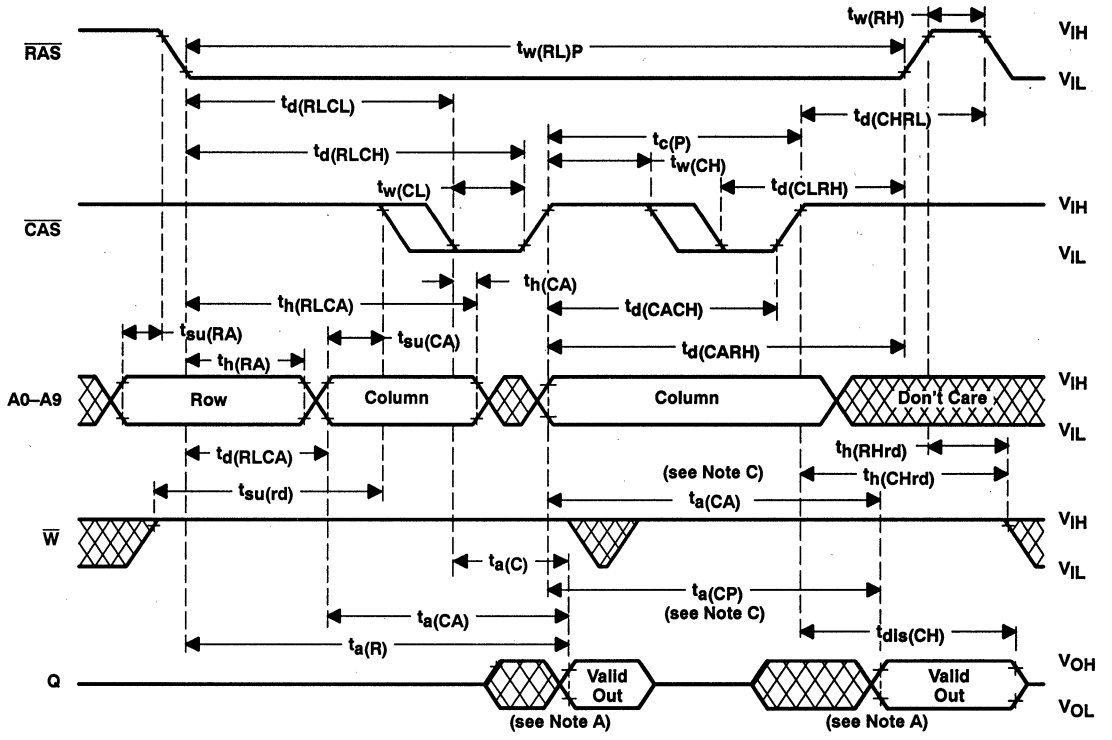
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from high-impedance to an invalid state prior to the specified access time.

Figure 5. Read-Write/Read-Modify-Write Cycle Timing

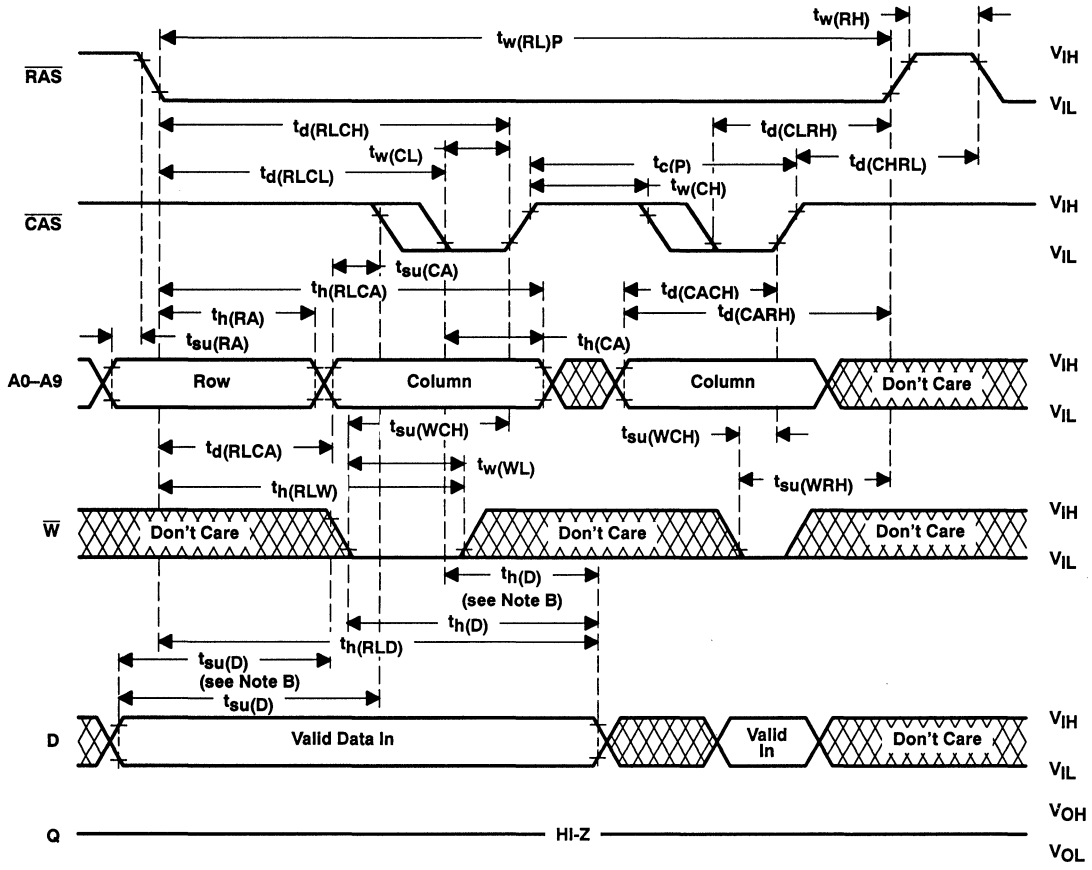
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from high impedance to an invalid state prior to the specified access time.
B. A write cycle or a read-modify cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
C. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

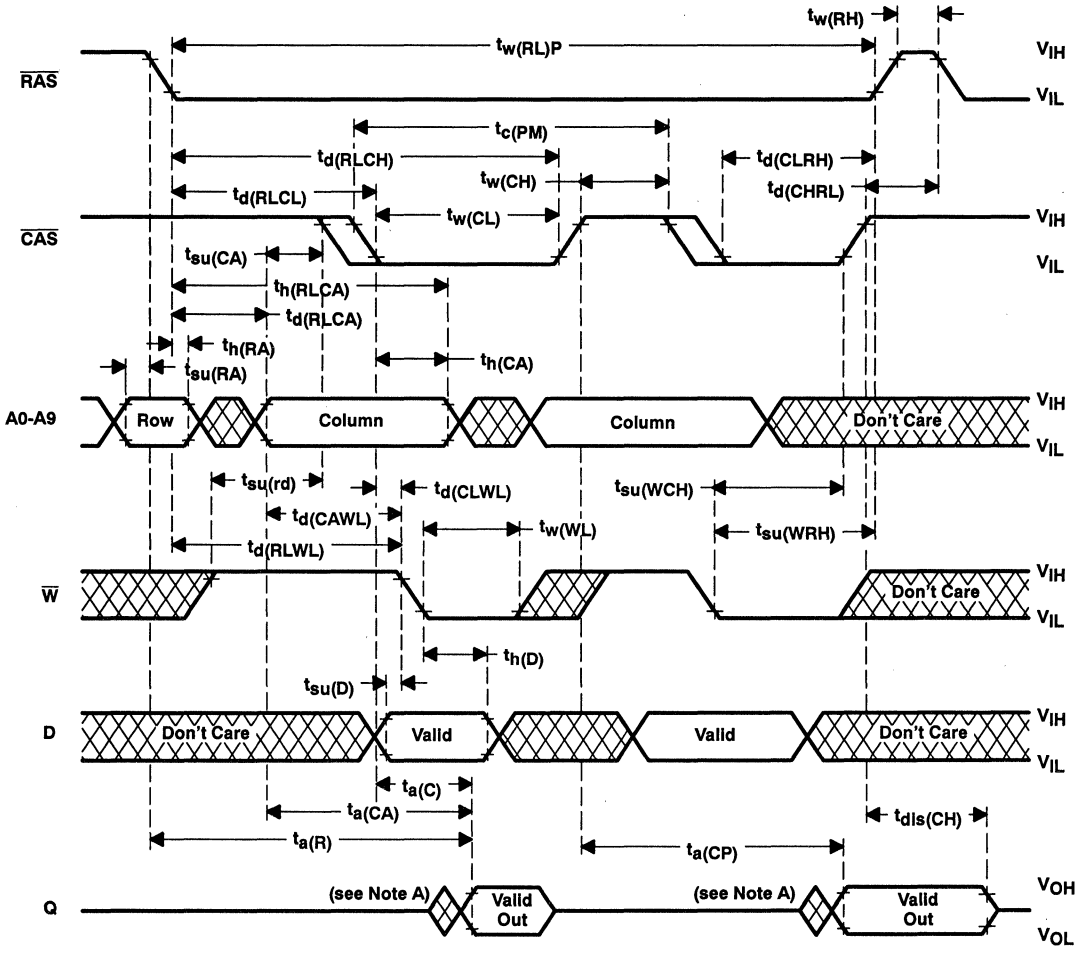
PARAMETER MEASUREMENT INFORMATION



NOTES: A. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.
B. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from high impedance to an invalid state prior to the specified access time.
B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

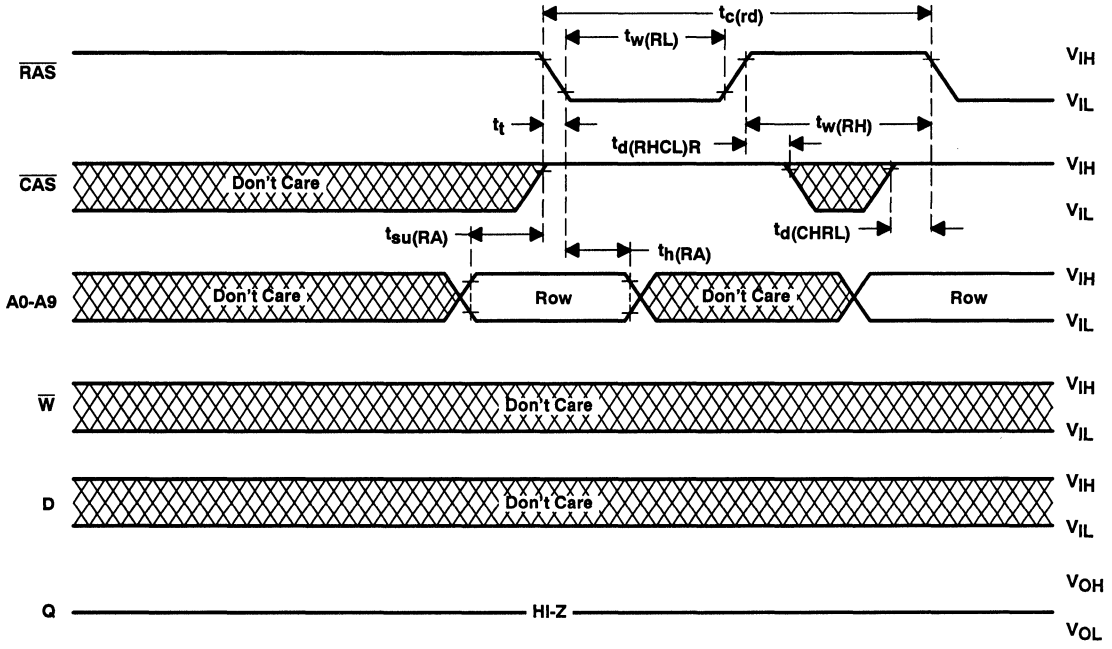


Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

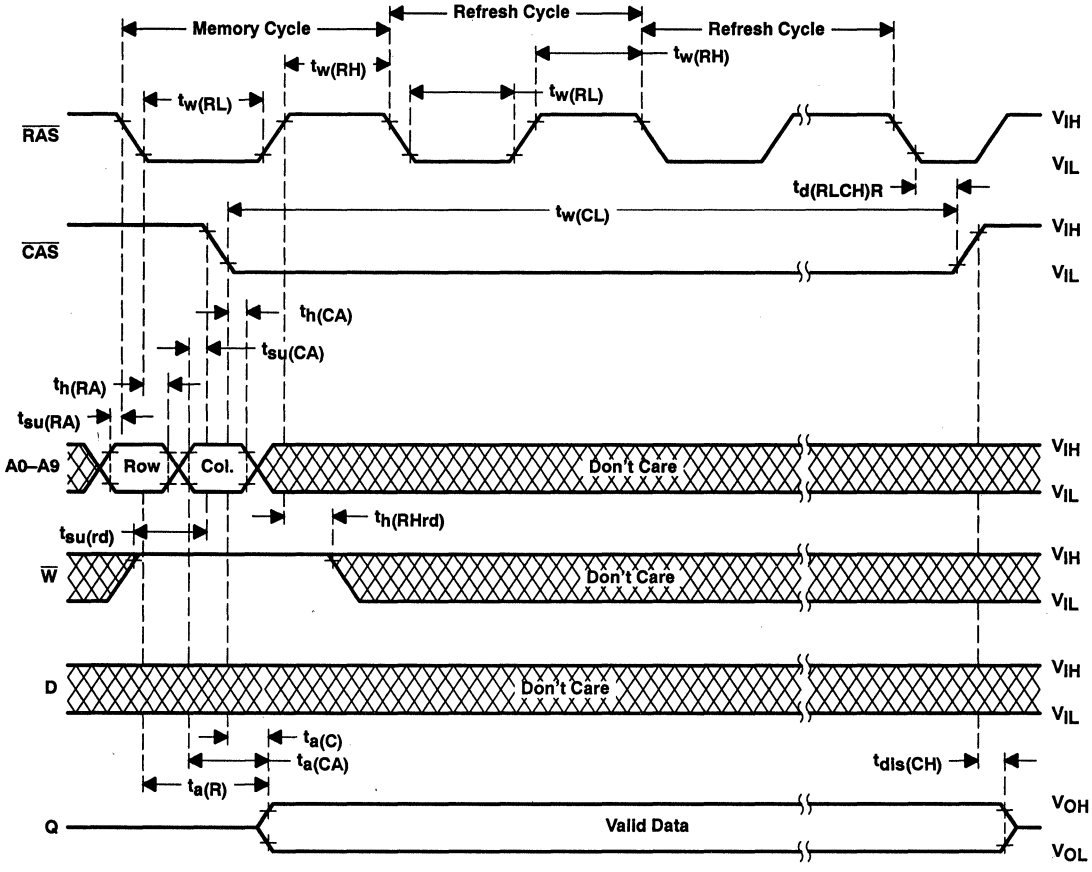


Figure 10. Hidden Refresh Cycle

PARAMETER MEASUREMENT INFORMATION

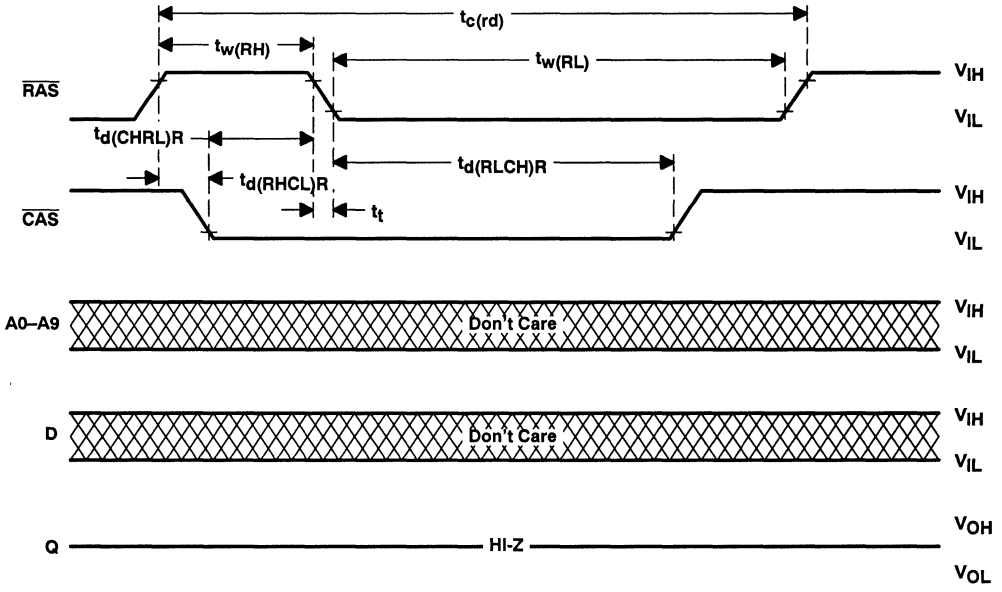


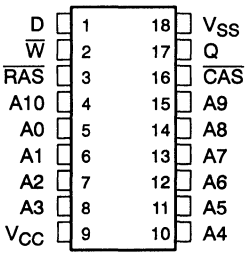
Figure 11. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Timing

- Processed to MIL-STD-883, Class B
- Military Temperature Range . . . –55 °C to 125°C
- Organization . . . 4 194 304 × 1
- Single 5-V Power Supply (±10% Tolerance)
- Performance Ranges:

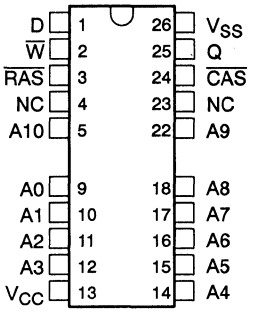
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44100-80	80 ns	20 ns	40 ns	150 ns
SMJ44100-10	100 ns	25 ns	50 ns	180 ns
SMJ44100-12	120 ns	30 ns	55 ns	210 ns

- Enhanced Page Mode Operation for Faster Memory Access
  - Higher Data Bandwidth Than Conventional Page-Mode Parts
  - Random Single-Bit Access Within a Row With a Column Address
- CAS-Before-RAS Refresh
- Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs/Outputs and Clocks are TTL Compatible
- Packaging Options:
  - 400 mil 20/26-Leadless Ceramic SOLCC (HM Suffix)
  - 18-Pin, 400 mil Ceramic DIP (JD Suffix)
  - 20-Pin, Ceramic Flatpack (HR Suffix)
  - 20-Pin, Ceramic CSOJ
  - Additional Package Options Planned

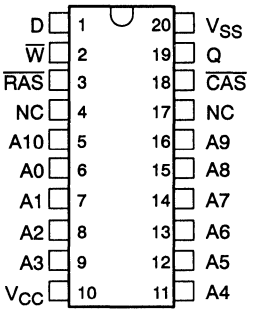
JD PACKAGE† (TOP VIEW)



HM AND CSOJ PACKAGES† (TOP VIEW)



HR PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44100 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 4 194 304 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power operation.

The SMJ44100 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 385 mW operating and 22 mW standby.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

The SMJ44100 is offered in a 400 mil 20/26-leadless ceramic surface mount SOLCC package (HM Suffix), 18-pin ceramic dual-in-line package (JD Suffix), 20-pin ceramic flatpack (HR Suffix) and a 20-pin leaded ceramic chip carrier (CSOJ). All packages are guaranteed for operation from – 55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44100 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on pins A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter t_{CSR}] and holding it low after $\overline{RAS}$ falls [see parameter t_{CHR}]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

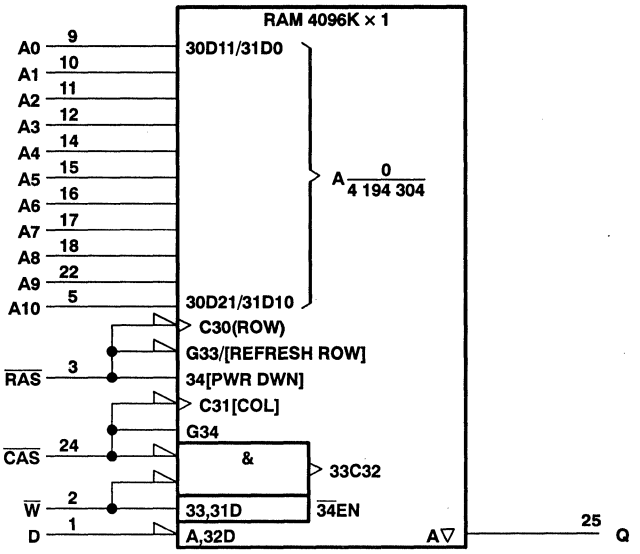
power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

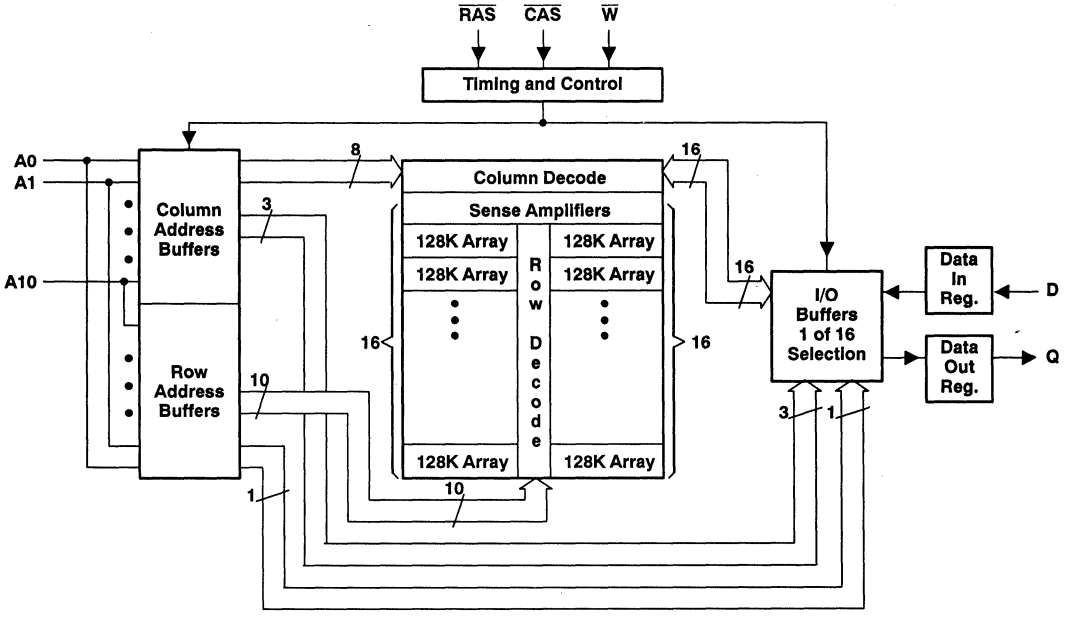
An industry standard Design For Test (DFT) mode is incorporated in the SMJ44100. A $\overline{CAS}$-before-$\overline{RAS}$ cycle with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data out pin will go high. If any one bit is different, the data out pin will go low. Any combination read, write, read-write, or page-mode can be used in test mode. The test mode function reduces test times by enabling the 4 meg DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and also column address 0 are not used. A $\overline{RAS}$ only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the HM package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... –1 V to 7 V
Voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature ..... –55°C to 125°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Min operating temperature	–55			°C
T_C	Max operating case temprature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44100-80		'44100-10		'44100-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or $\overline{CBR}$) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 5)

	PARAMETER	MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			7	pF
$C_{i(D)}$	Input capacitance, data inputs			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			10	pF
$C_{i(W)}$	Input capacitance, write-enable input			10	pF
C_o	Output capacitance			10	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage range and operating temperature

	PARAMETER	'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		40		50		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven. The output is disabled when $\overline{CAS}$ is brought high.

timing requirements over recommended ranges of supply voltage and operating temperature

		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	150		180		210		ns
t_{RWC}	Read-write cycle time	175		210		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	50		60		65		ns
t_{PRWC}	Page-mode read-write cycle time	70		85		95		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Write pulse duration	15		20		25		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Data hold time (see Note11)	15		20		25		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see Note 13)	60		75		90		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		20		25		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	40		50		55		ns

Continued next page.

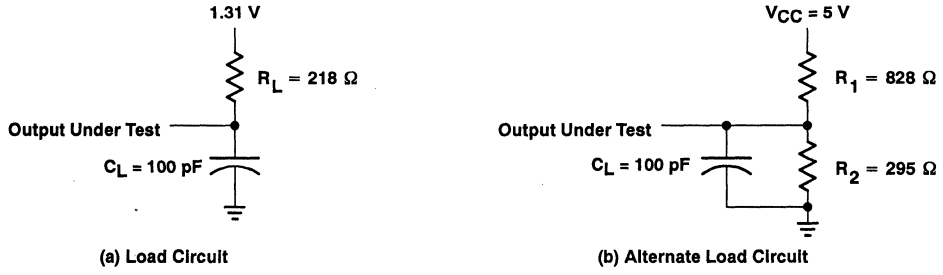
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. The minimum value is measured when t_{RDC} is set to t_{RCD} min as a reference.

timing requirements over recommended supply voltage range and operating temperature range

		'44100-80		'44100-10		'44100-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low(Read-write operation only)	20		25		30		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	80		100		120		ns
t_{CLZ}	$\overline{CAS}$ to output in low Z (see Note 15)							
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 16)							

NOTES: 14. Maximum value specified only to assure access time.
15. Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.
16. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.

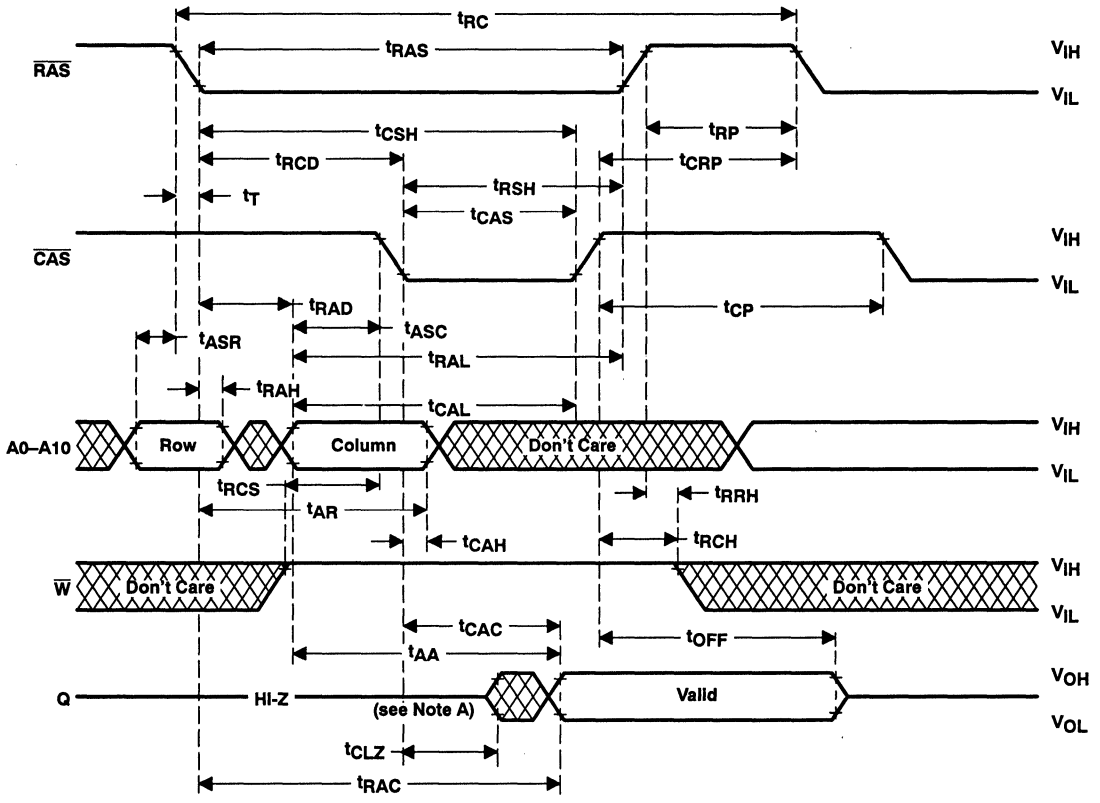
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

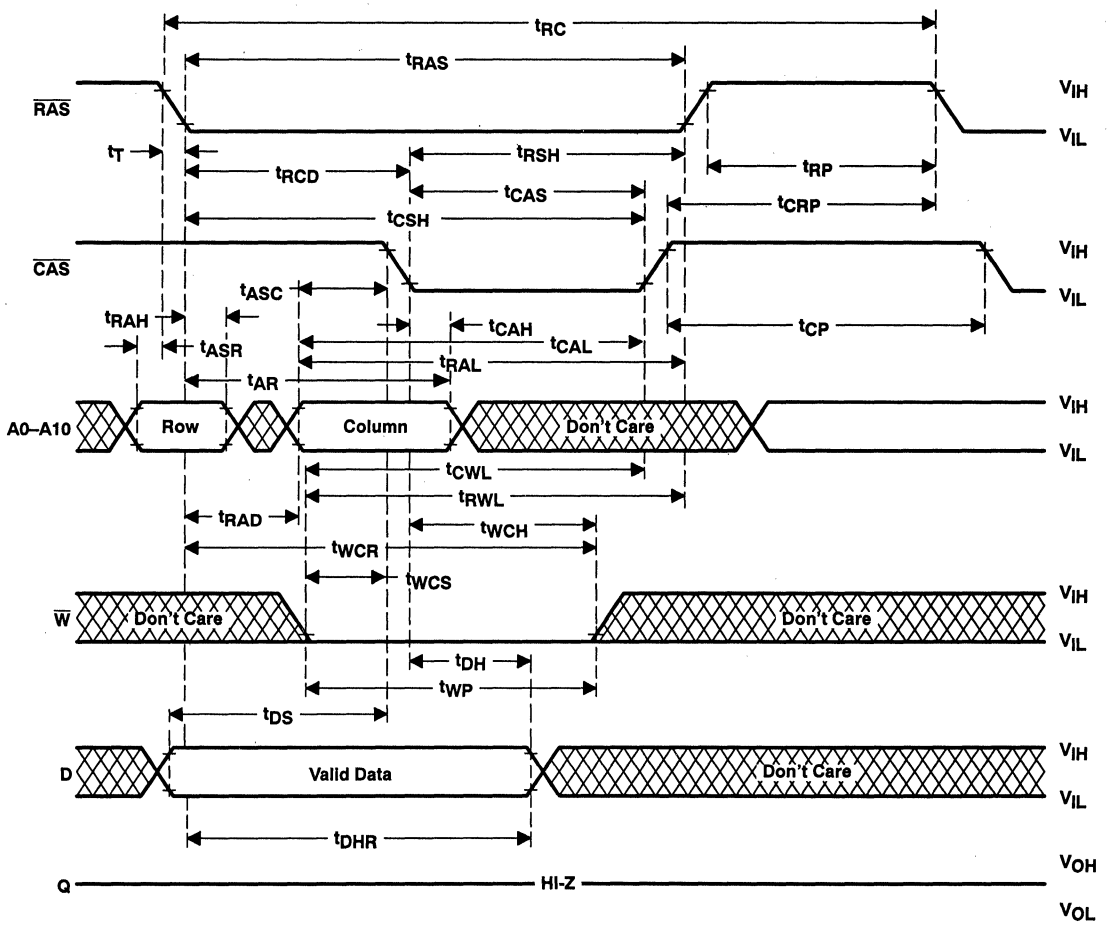
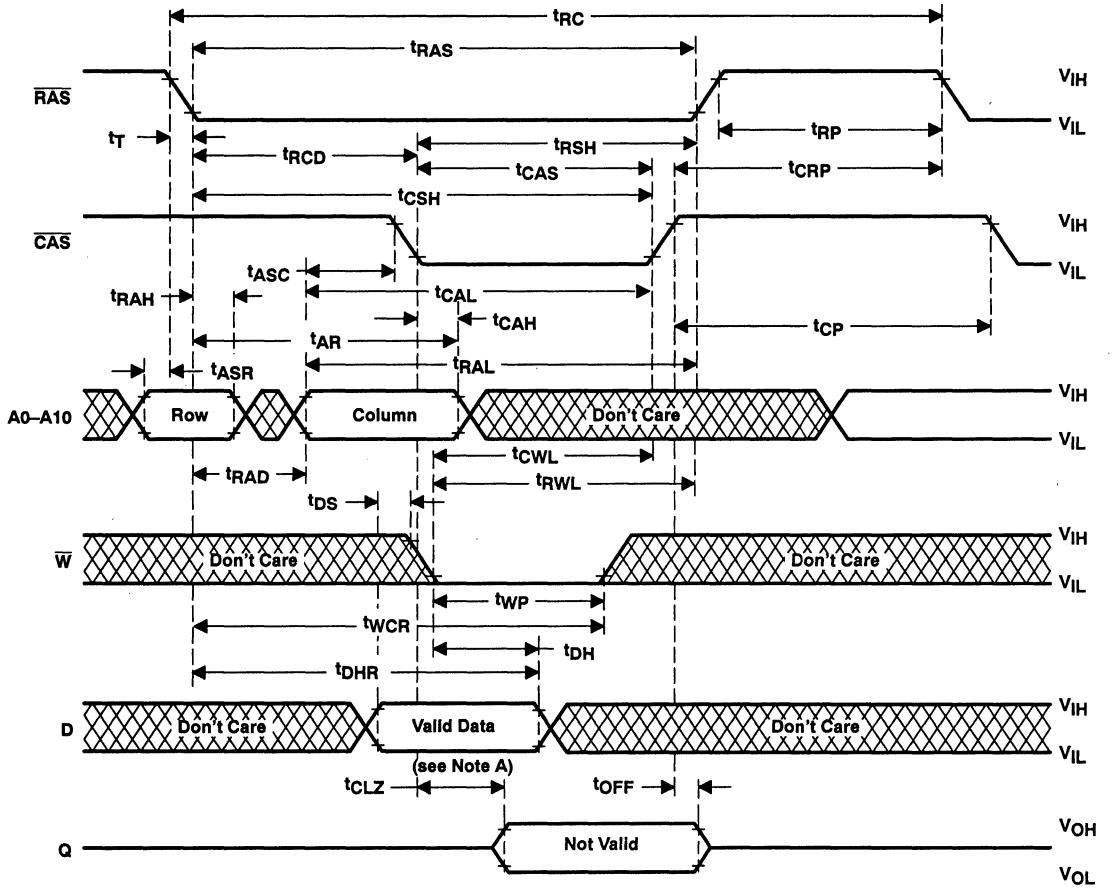


Figure 3. Early Write Cycle Timing

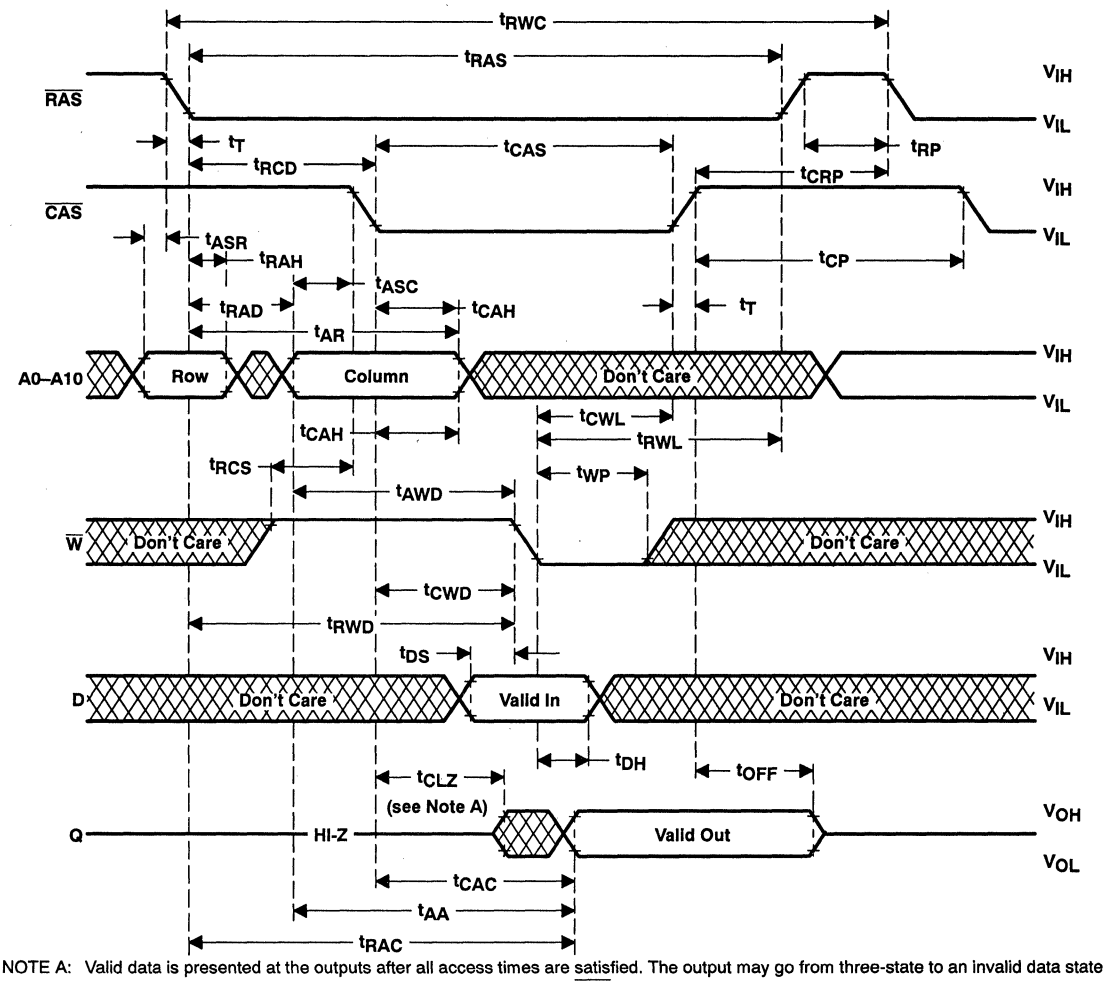
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 4. Write Cycle Timing

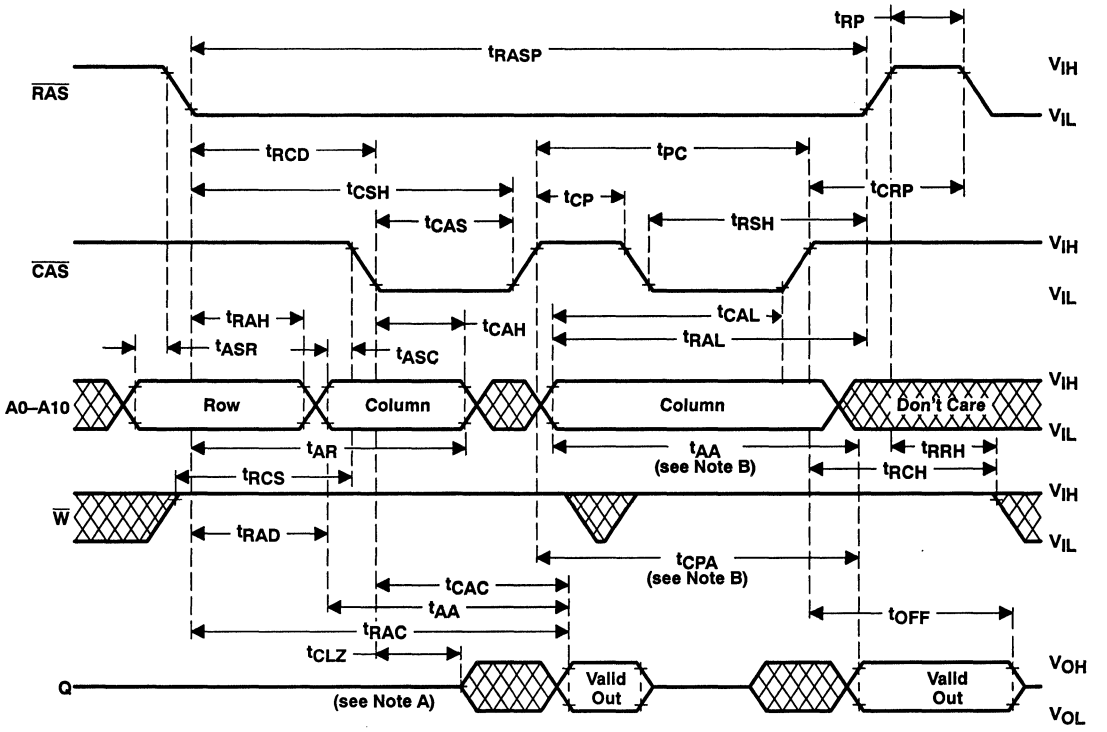
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

Figure 5. Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

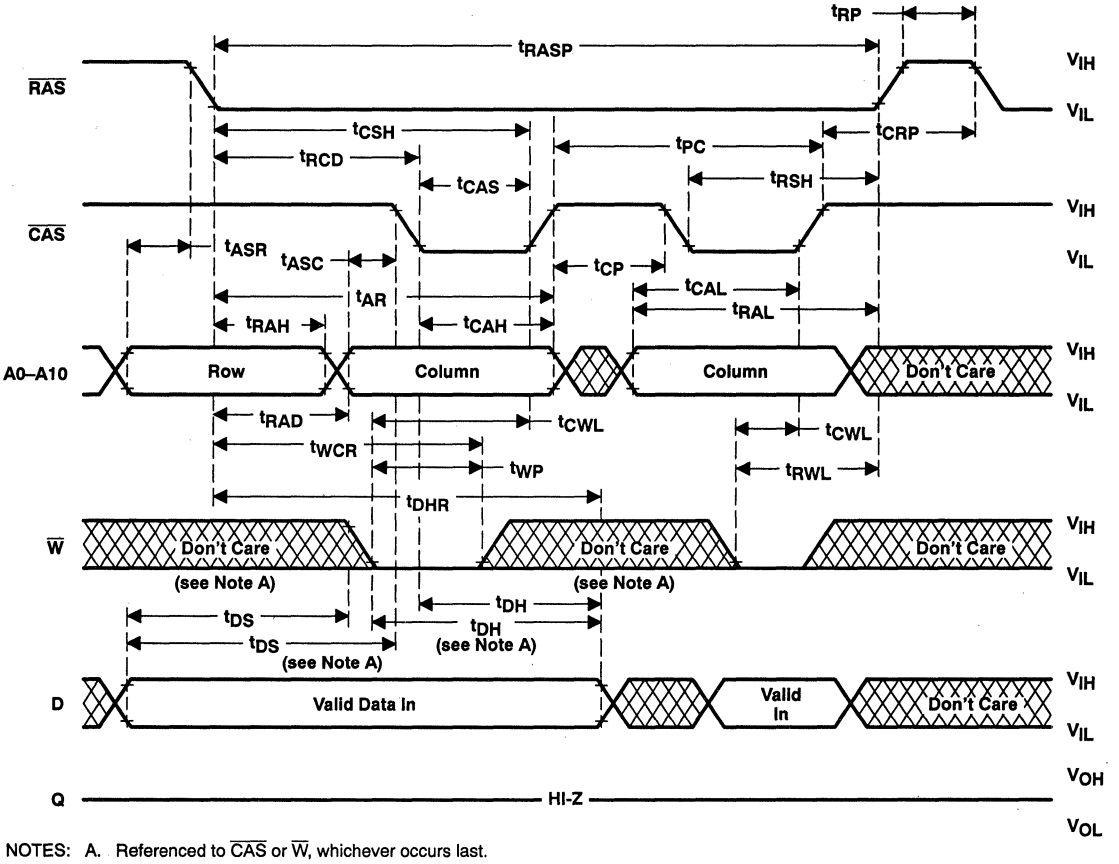


NOTES: A. Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

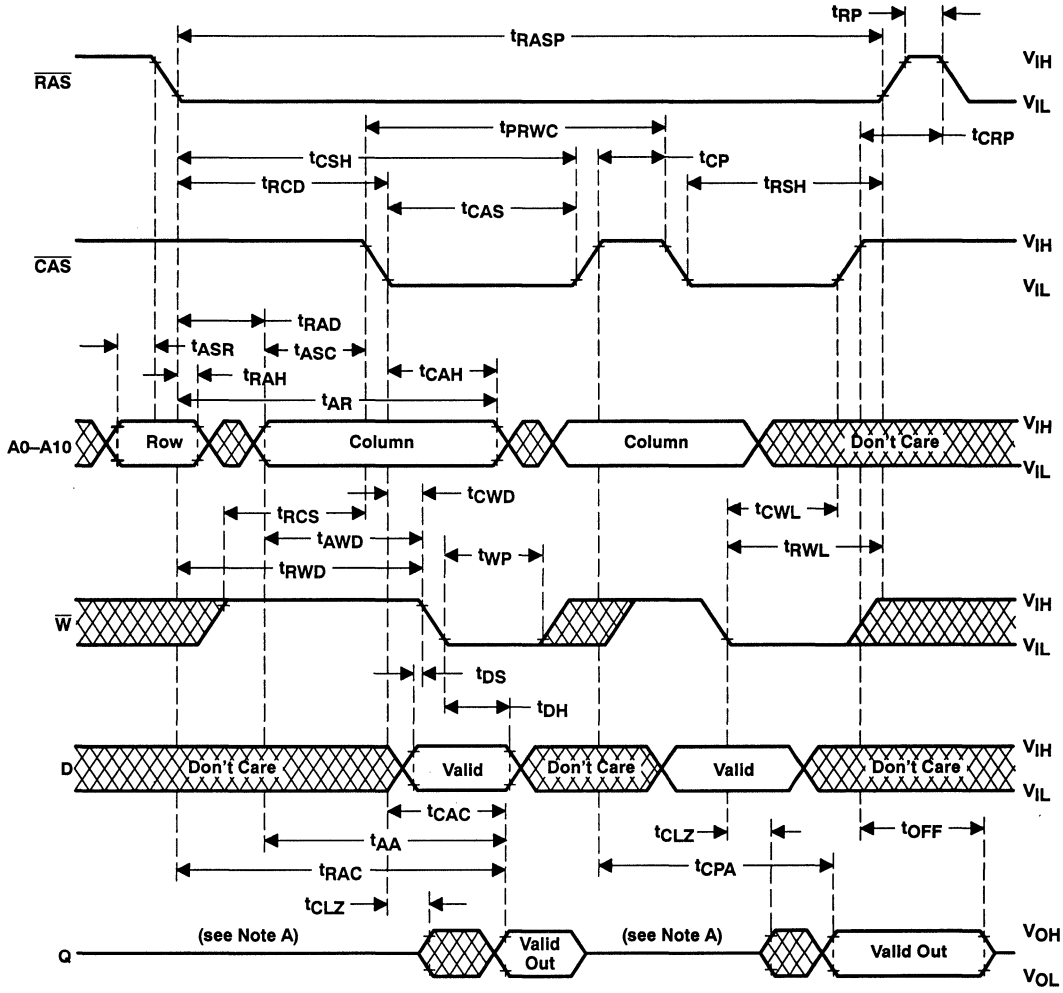
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with a write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

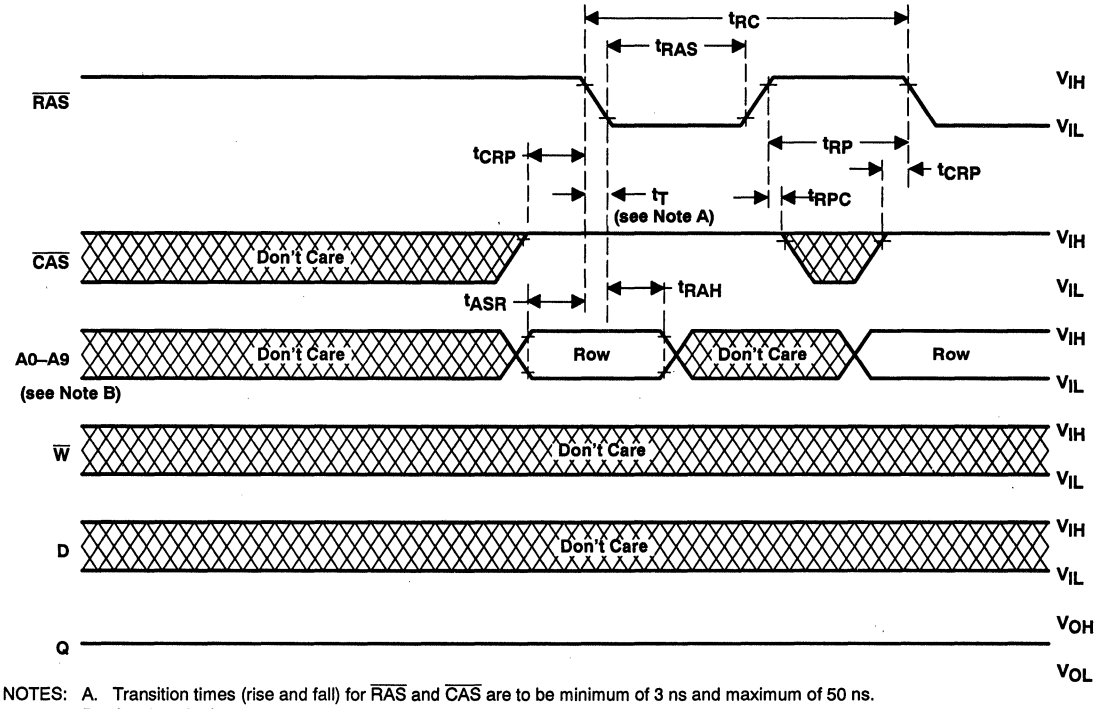


NOTES: A. Valid data is presented at the output after all access times are satisfied. The output may go from three-state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

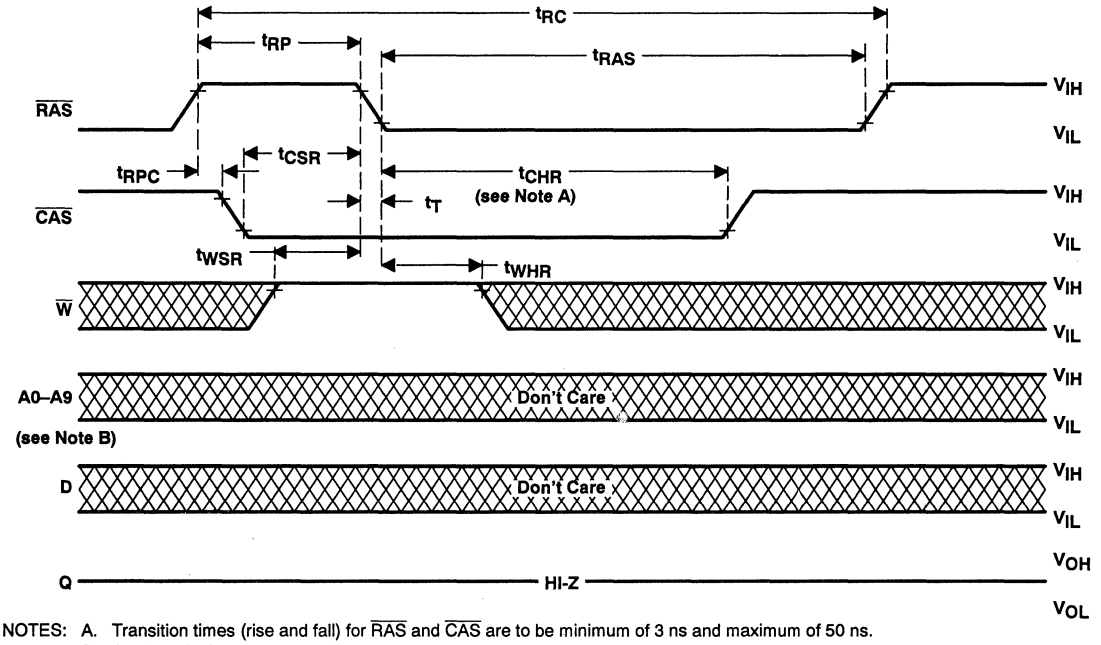
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
B. A10 is a don't care.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be minimum of 3 ns and maximum of 50 ns.
B. A10 is a don't care.

Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

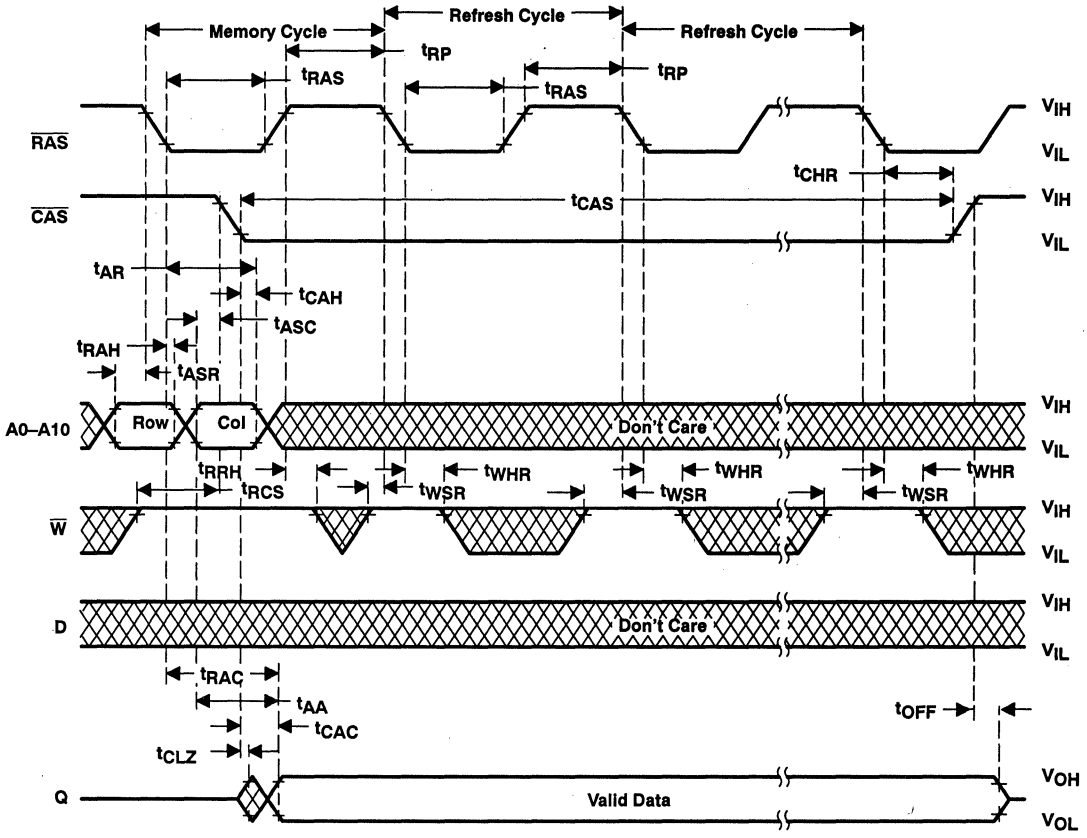


Figure 11. Hidden Refresh Cycle (Read)

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PARAMETER MEASUREMENT INFORMATION

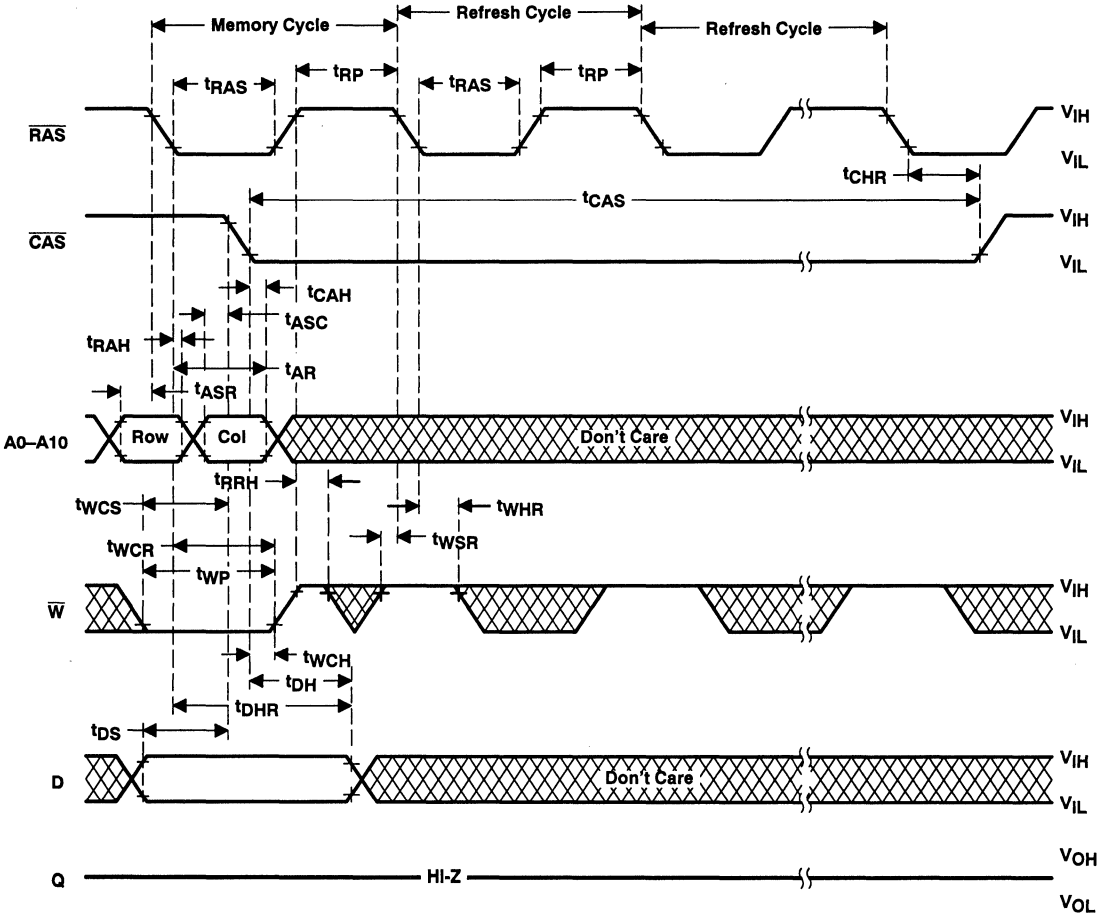

Figure 12. Hidden Refresh Cycle (Write)

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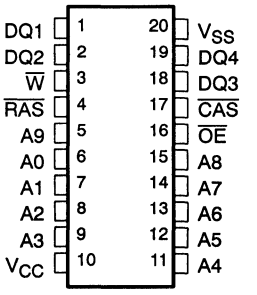
- **Processed to MIL-STD-883, Class B**
- **Military Temperature Range . . . –55 to 125°C**
- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

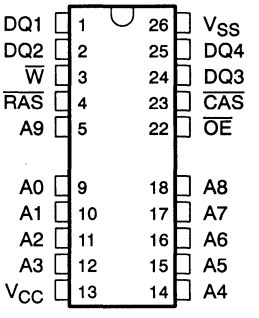
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44400-80	80 ns	20 ns	40 ns	150 ns
SMJ44400-10	100 ns	25 ns	50 ns	180 ns
SMJ44400-12	120 ns	30 ns	55 ns	210 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Packaging Options:**
  - **400-mil 20/26-Leadless Ceramic SOLCC (HM Suffix)**
  - **20-Pin, 400-Mil Ceramic DIP (JD Suffix)**
  - **20-Pin Ceramic Flatpack (HR Suffix)**
  - **20-Pin Ceramic CSOJ**
  - **Additional Package Options Planned**

JD AND HR PACKAGES†
(TOP VIEW)



HM AND CSOJ PACKAGES†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44400 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low-power operation.

The SMJ44400 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 360 mW operating and 22 mW standby.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ44400 is offered in a 400-mil 20/26-leadless ceramic surface mount SOLCC package (HM suffix), a 20-pin ceramic dual-in-line package (JD suffix), a 20-pin ceramic flatpack (HR suffix), and a 20-pin leaded ceramic chip carrier (CSOJ). All packages are characterized for operation from –55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44400 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

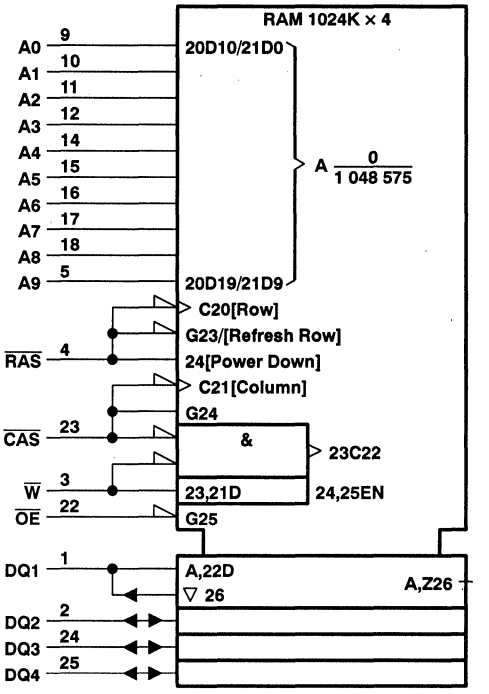
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

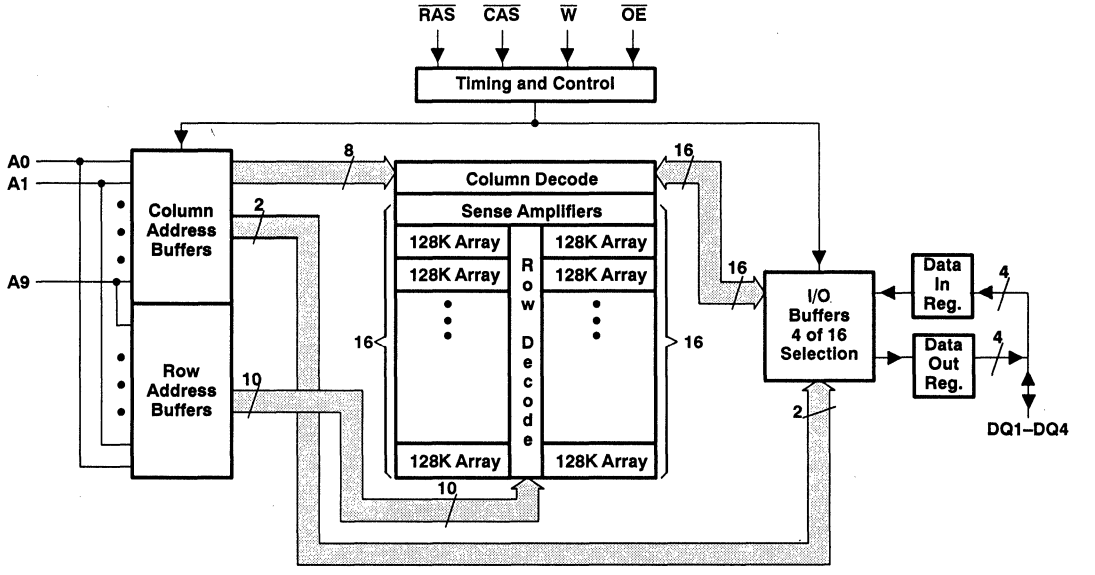
An industry standard Design For Test (DFT) mode is incorporated in the SMJ44400. A $\overline{CAS}$-before-$\overline{RAS}$ with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different, all the DQ pins will go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1M × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The pinouts illustrated are for the HM package.

functional block diagram



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absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Min operating temperature	– 55			°C
T_C	Max operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44400-80		'44400-10		'44400-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or $\overline{CBR}$)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			10	pF
$C_{i(W)}$	Input capacitance, write-enable input			10	pF
C_O	Output capacitance			10	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		40		45		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		25		30	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	150		180		210		ns
t_{RWC}	Read-write cycle time	205		245		285		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	50		60		65		ns
t_{PRWC}	Page-mode read-write cycle time	100		120		135		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Write pulse duration	15		20		25		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Data hold time (see Note 11)	15		20		25		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		20		25		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	Delay time, column-address to $\overline{W}$ low (Read-write operation only)	70		80		90		ns

Continued next page.

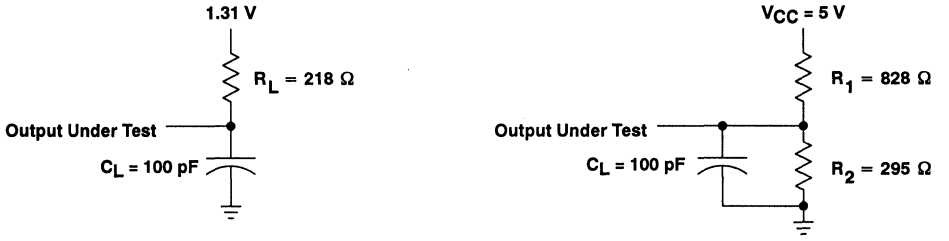
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	50		60		70		ns
t_{OEH}	$\overline{OE}$ command hold time	20		25		30		ns
t_{OED}	$\overline{OE}$ to data delay	20		25		30		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	20		25		30		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	110		135		160		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 15)							

NOTES: 13. Maximum value specified only to assure access time.
14. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
15. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

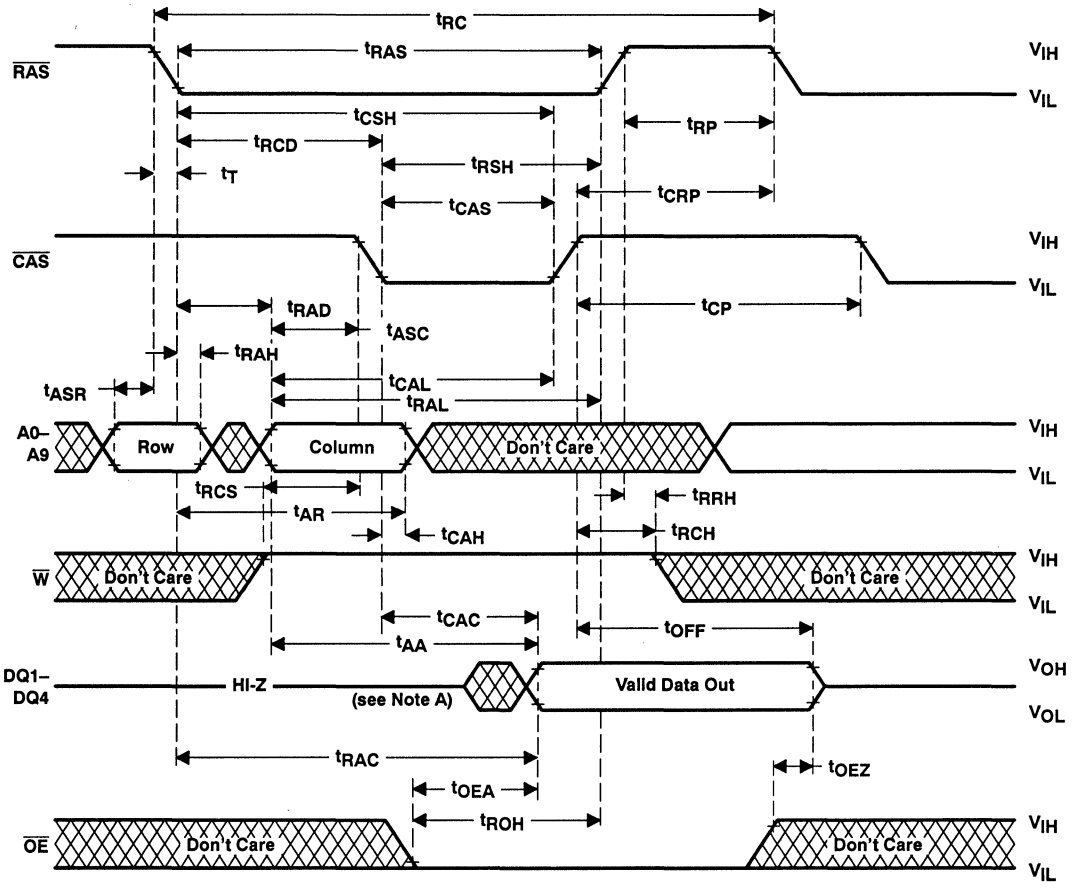
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

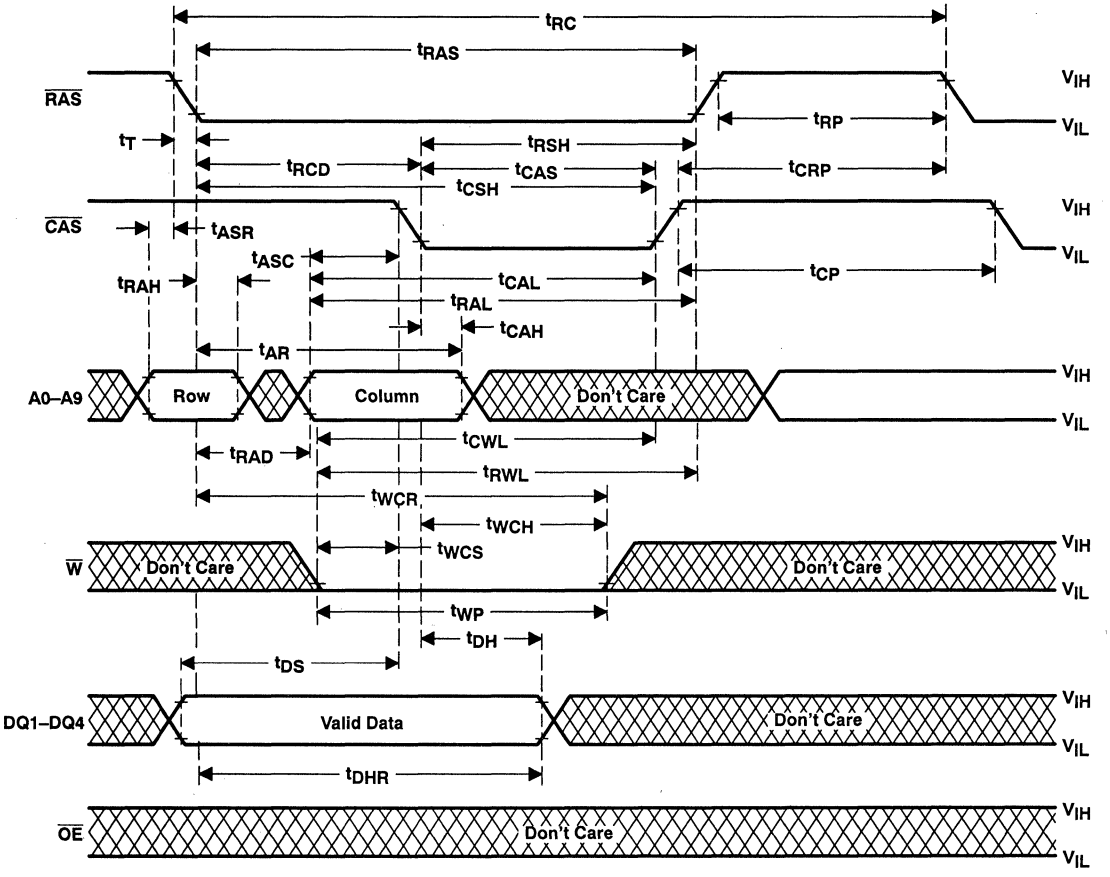


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

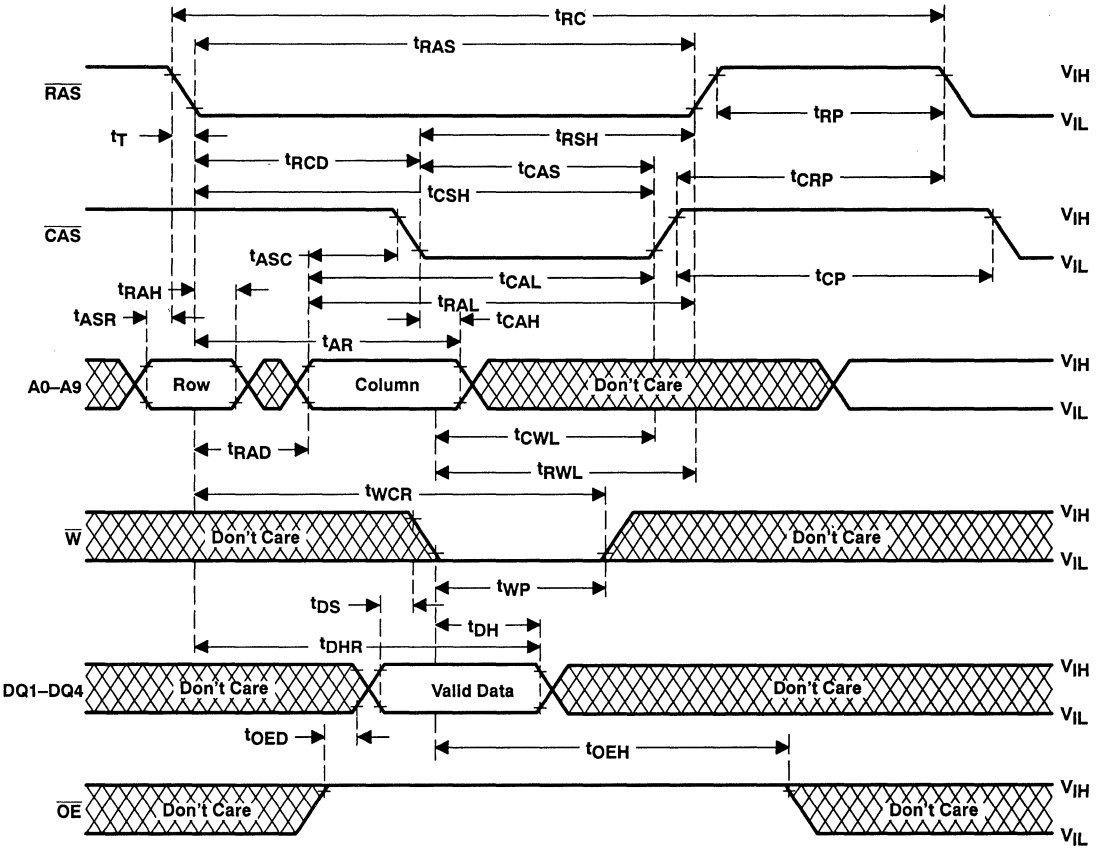
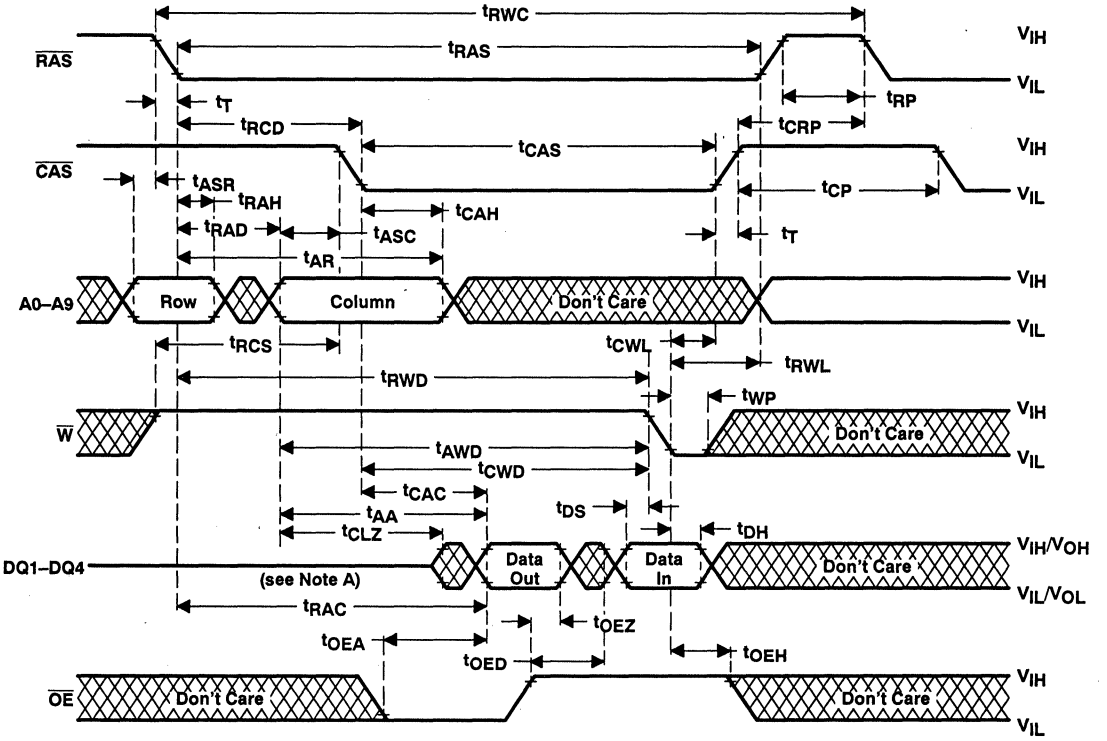


Figure 4. Write Cycle Timing

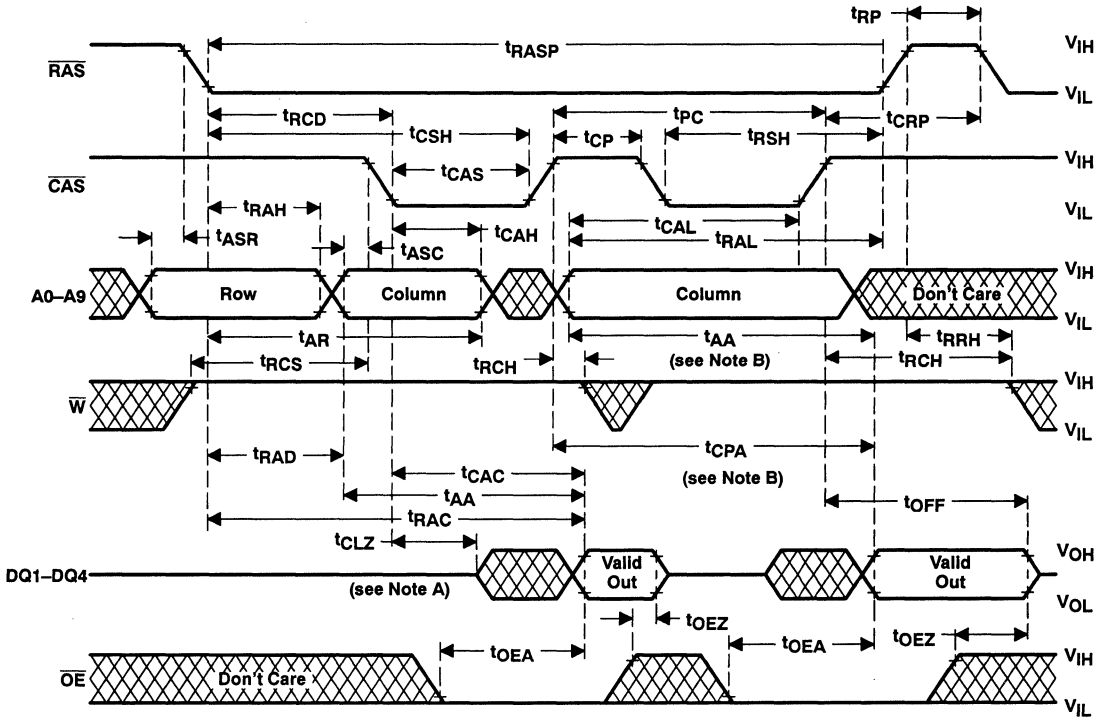
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

Figure 5. Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

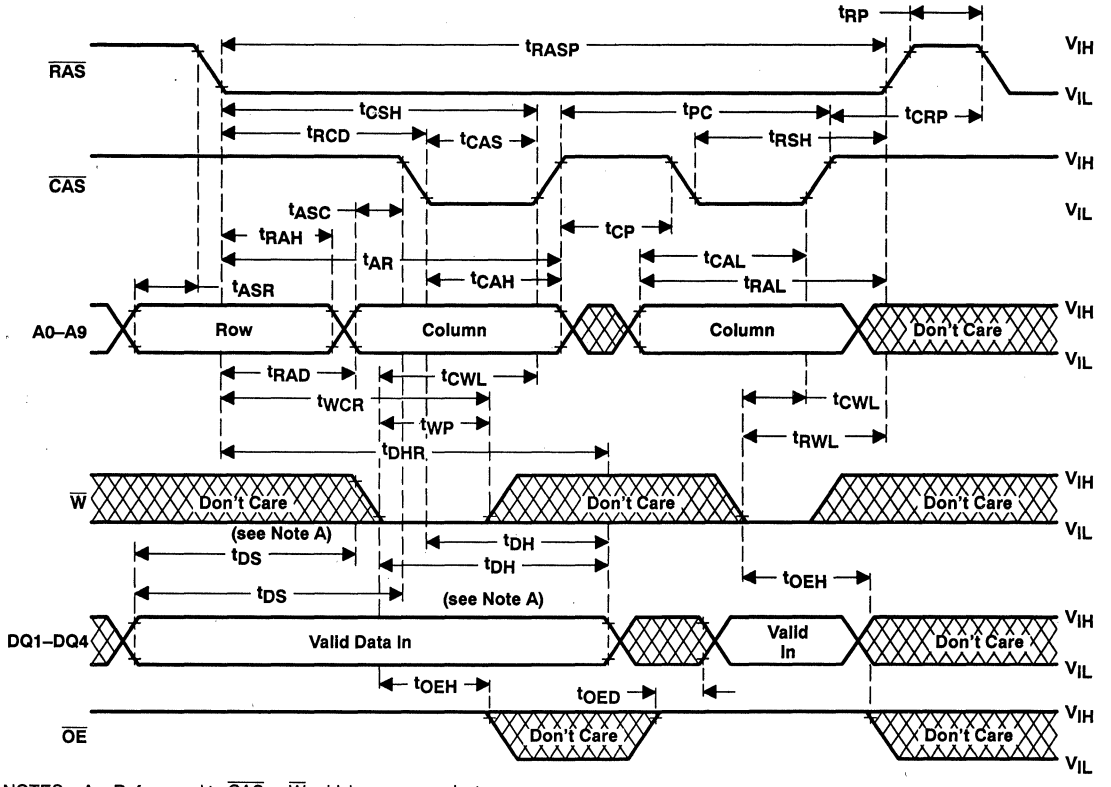


NOTES: A. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

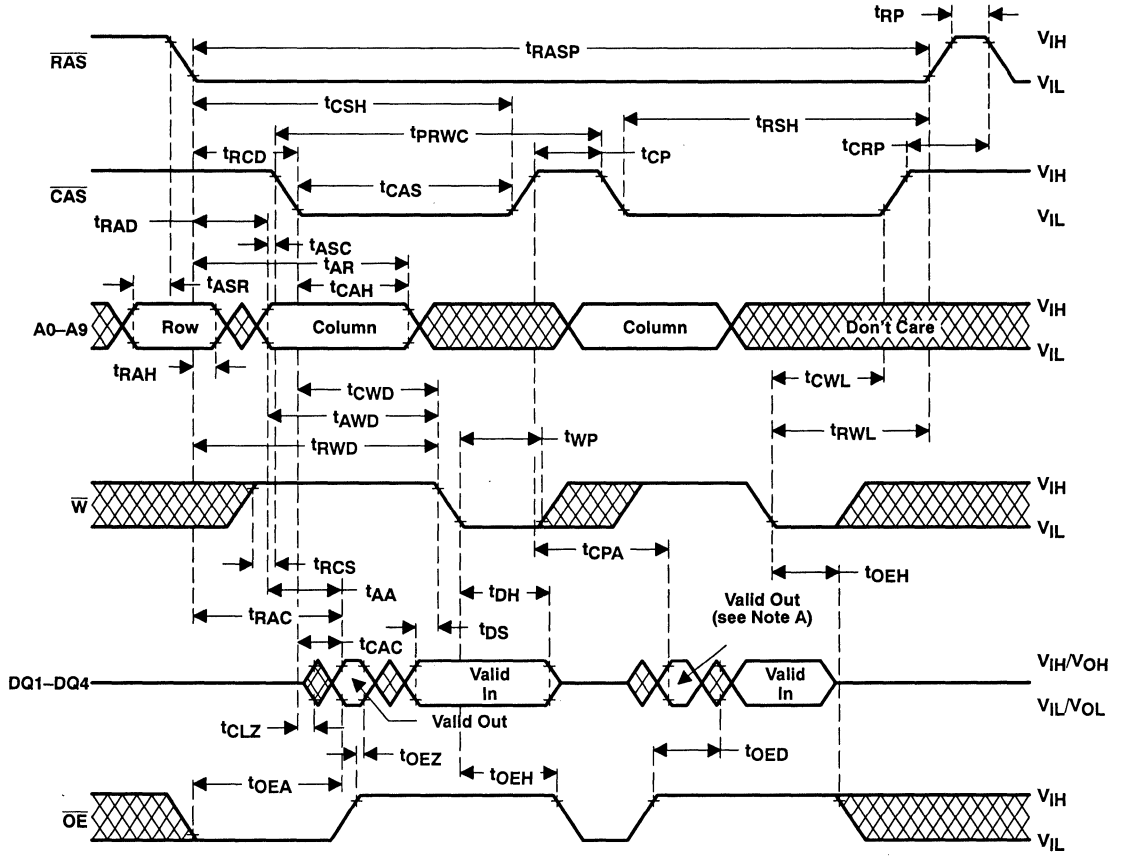
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

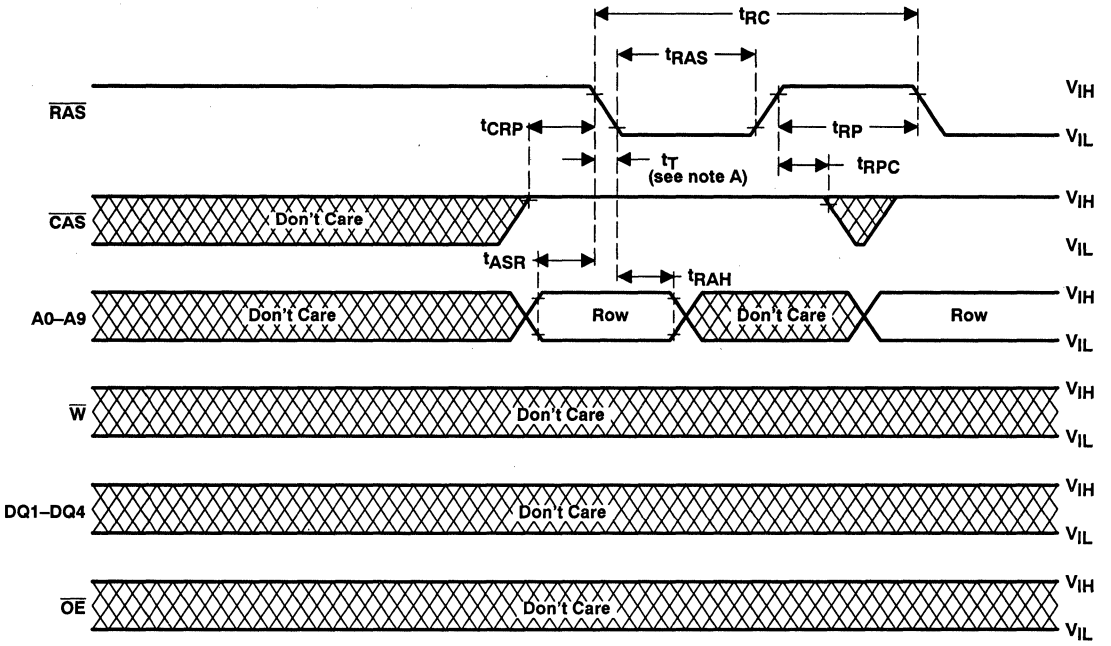


NOTES: A. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

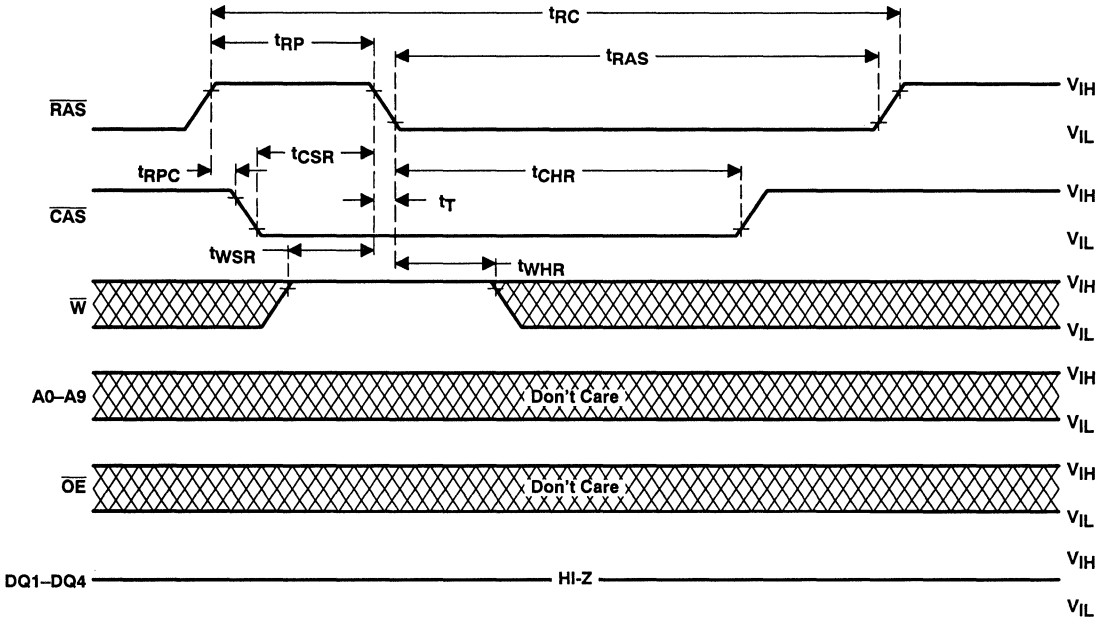
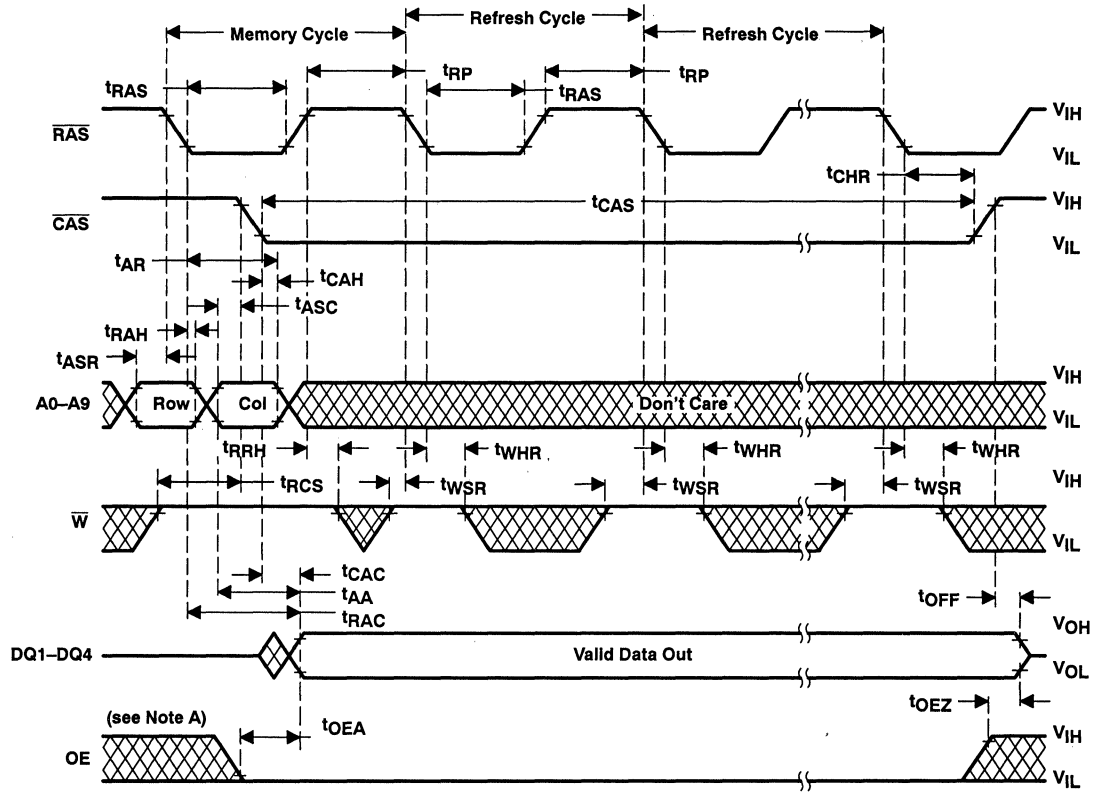


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION

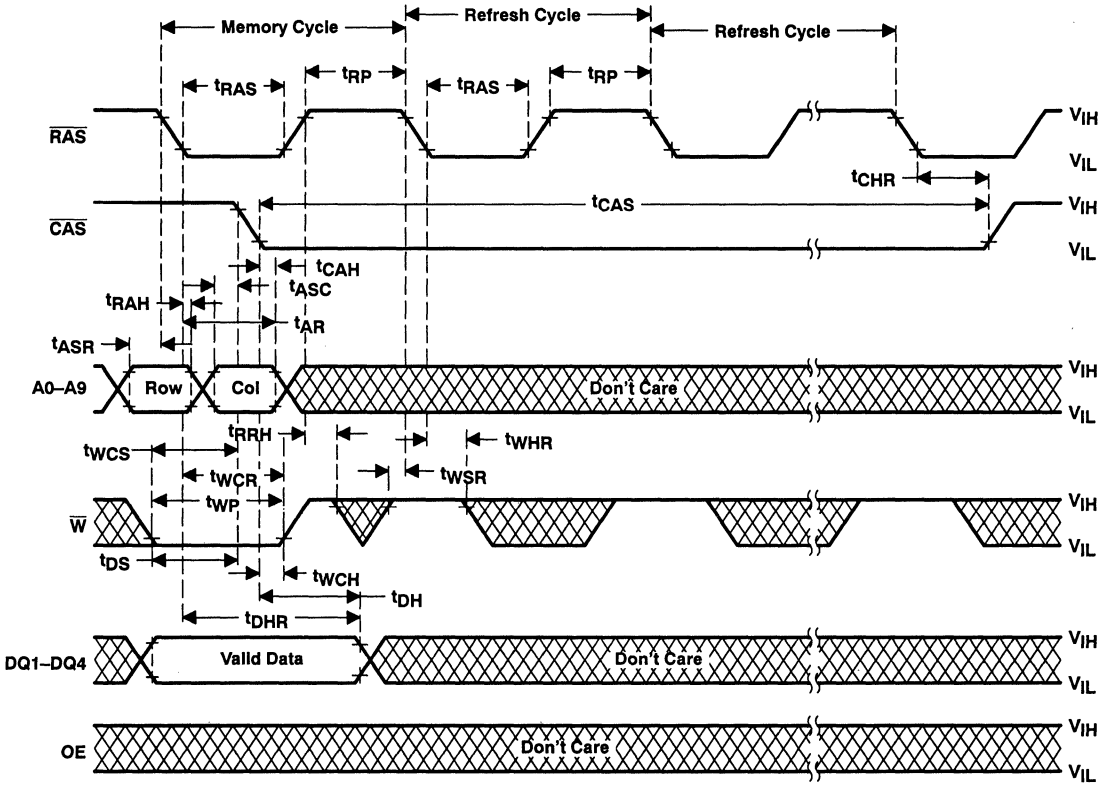


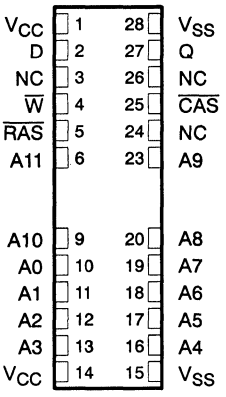
Figure 12. Hidden Refresh Cycle (Write)

- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

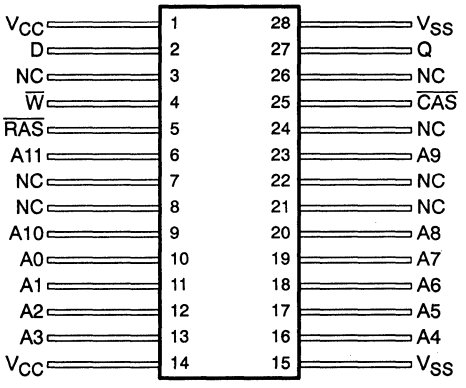
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
SMJ416100-60	60 ns	15 ns	30 ns	110 ns
SMJ416100-70	70 ns	18 ns	35 ns	130 ns
SMJ416100-80	80 ns	20 ns	40 ns	150 ns
SMJ416100-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycles Refresh in 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks Are TTL Compatible**
- **Operating Free-Air Temperature Range . . . – 55°C to 125°C**

FNC PACKAGE†
(TOP VIEW)



HKB PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

description

The SMJ416100 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 16 777 216-bit words by one bit each. They employ EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

All inputs, outputs, and clocks are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ416100 is offered in 450-mil 24/28-pin surface mount SOLCC (FNC suffix) and flatpack (HKB suffix) packages. The packages are characterized for operation from – 55°C to 125°C.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

EPIC is a trademark of Texas Instruments Incorporated.

The column address buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the SMJ416100 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Twelve column-address bits are set on A0 through A12 and latched onto the chip by the first column-address strobe ($\overline{CAS}$). Row address A11 is required during a normal access and during $\overline{RAS}$-only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 54 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

refresh

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

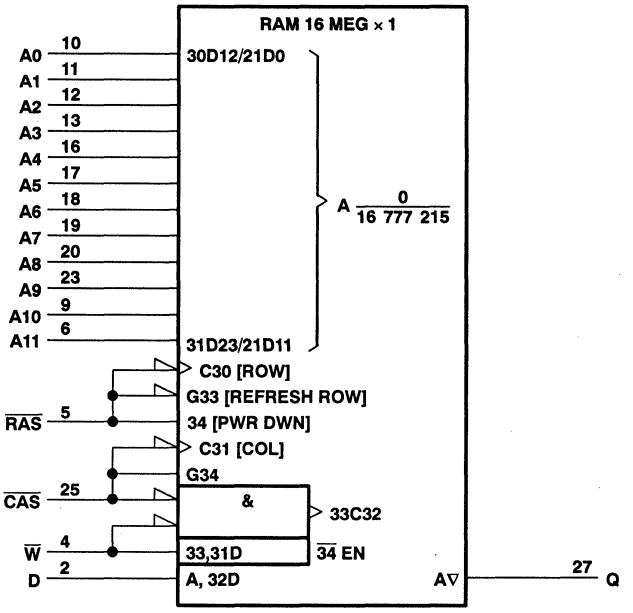
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

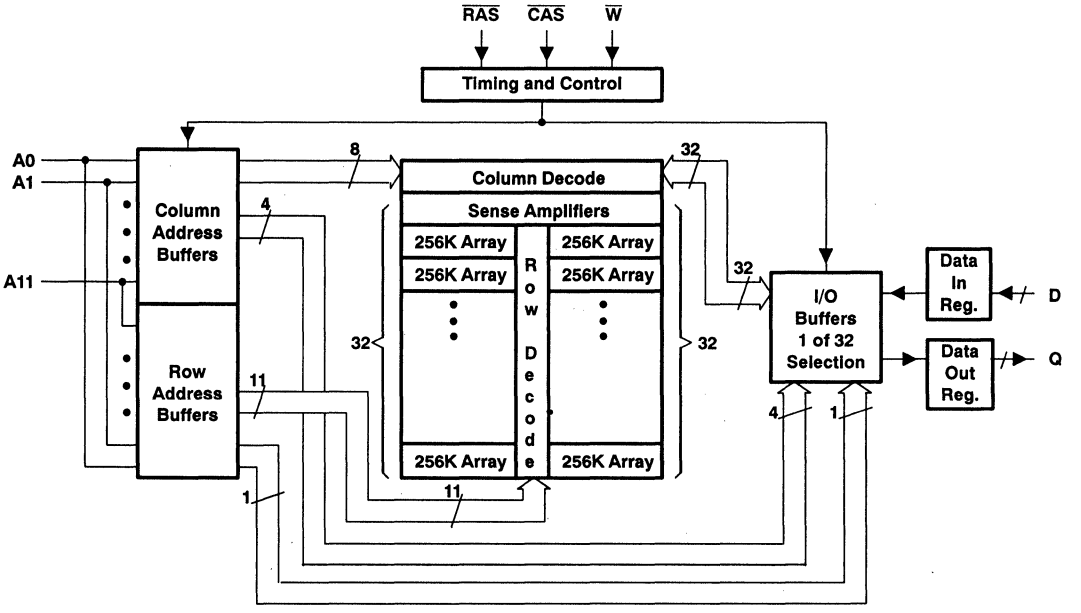
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ416100-60		SMJ416100-70		SMJ416100-80		SMJ416100-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		90		80		70		60	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70		60	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		65		60		55	mA
I_{CC7}	Standby current output enable‡ (see Note 5)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.
5. Measured with indicated conditions following a normal read cycle.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			9	pF
$C_{i(D)}$	Input capacitance, data input			8	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			8	pF
$C_{i(W)}$	Input capacitance, write-enable input			8	pF
C_O	Output capacitance			14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major changes. Samples are tested at 0 V and 25° C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		SMJ416100-60		SMJ416100-70		SMJ416100-80		SMJ416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 8)	0	15	0	18	0	20	0	25	ns

NOTE 7: Valid data is presented at the output after all access times are satisfied but may go from a high-impedance state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

8. t_{OFF} is specified when the output is no longer driven. The output is disabled by bringing $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		SMJ416100-60		SMJ416100-70		SMJ416100-80		SMJ416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 9)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 10)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 12)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 13)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 14)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

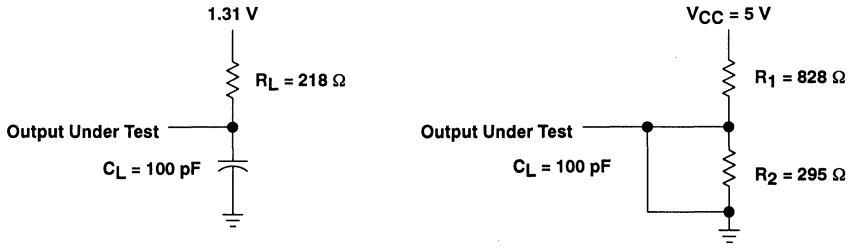
NOTES: 9. All cycle times assume t_T = 5 ns, referenced to V_{IH}(min) and V_{IL}(max)
10. To insure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
11. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
12. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
13. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		SMJ416100-60		SMJ416100-70		SMJ416100-80		SMJ416100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		100		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		64		64		64		64	ms

NOTE 15: The maximum value is specified only to insure access time.

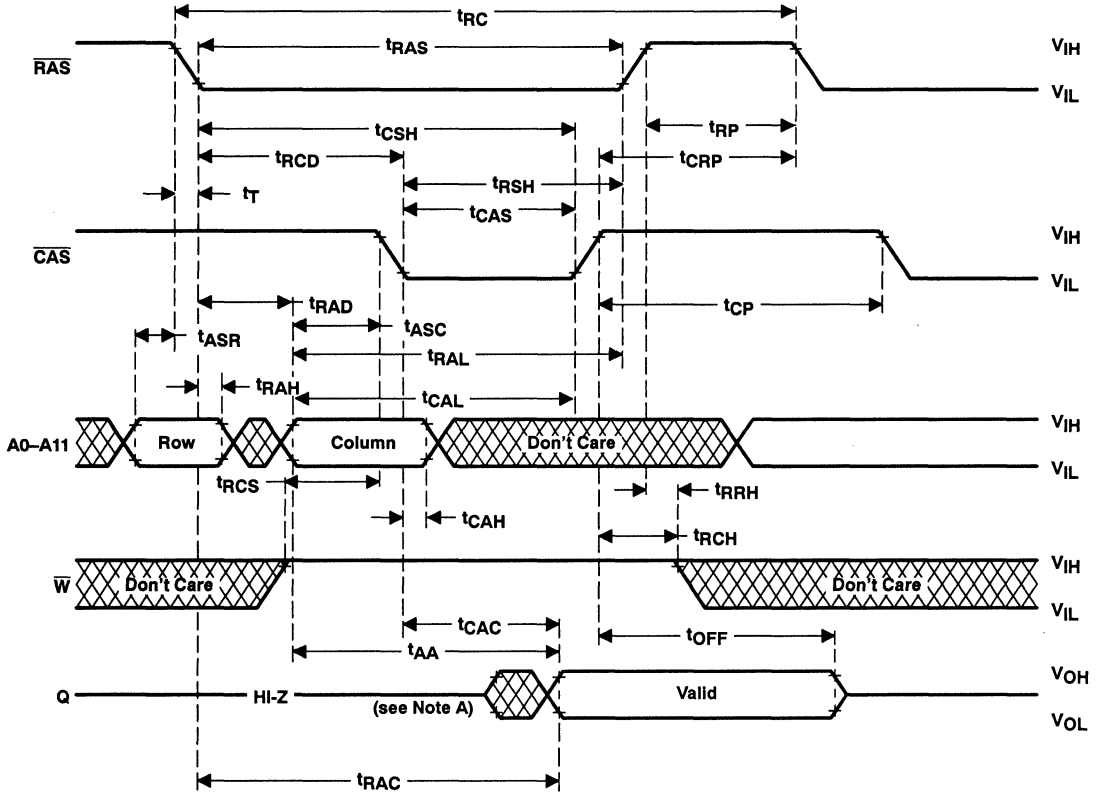
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits For Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

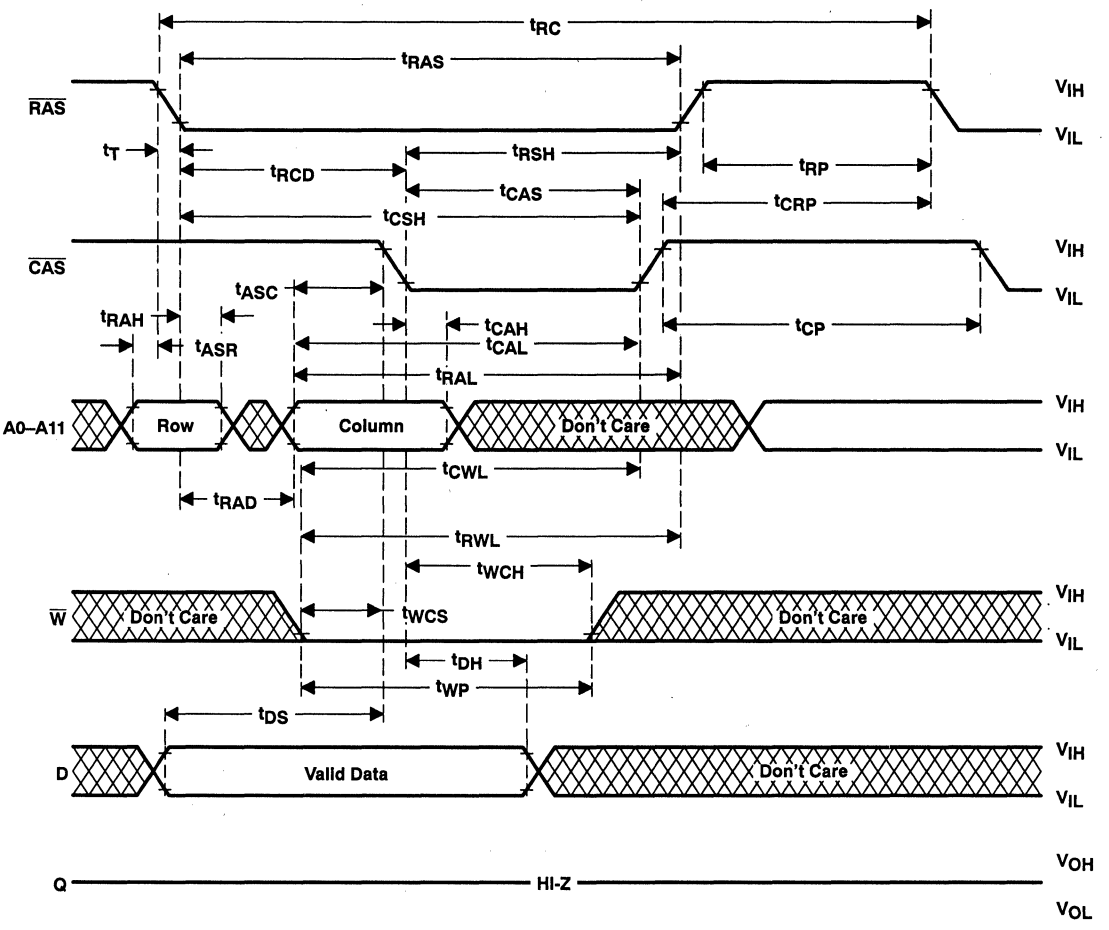


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

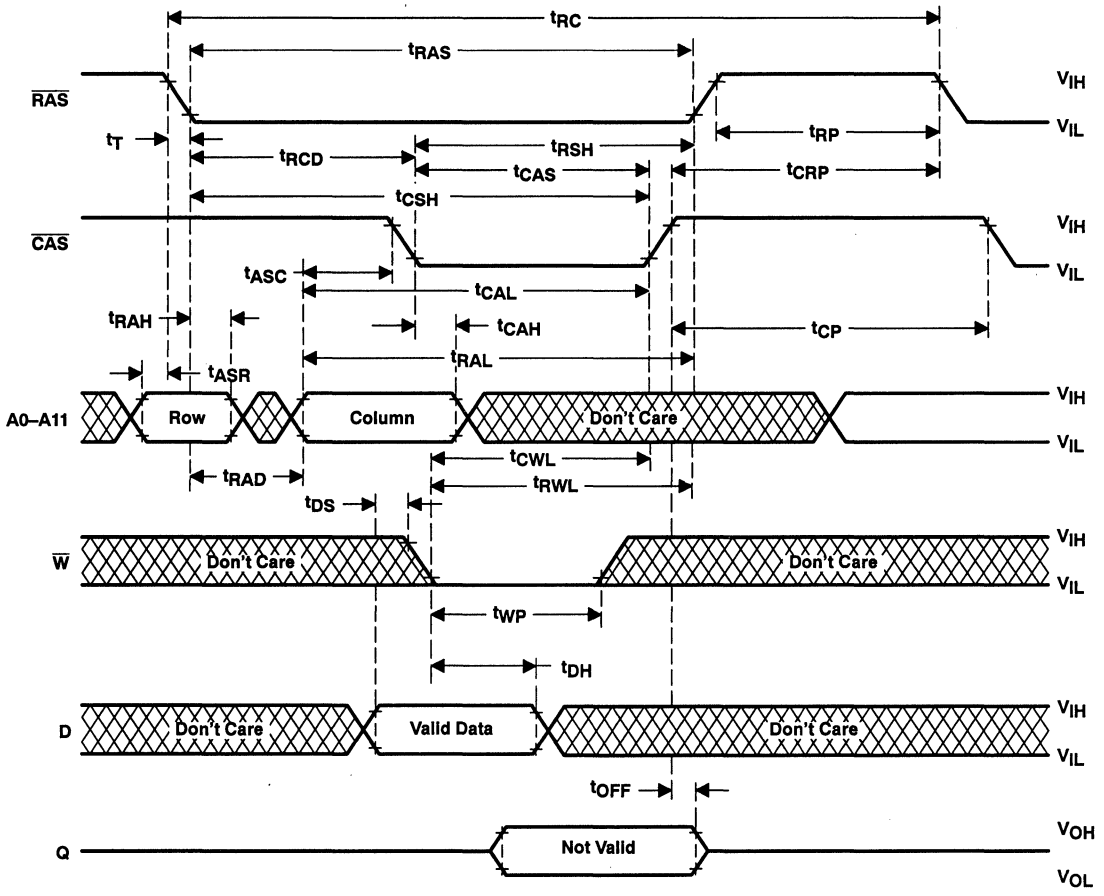
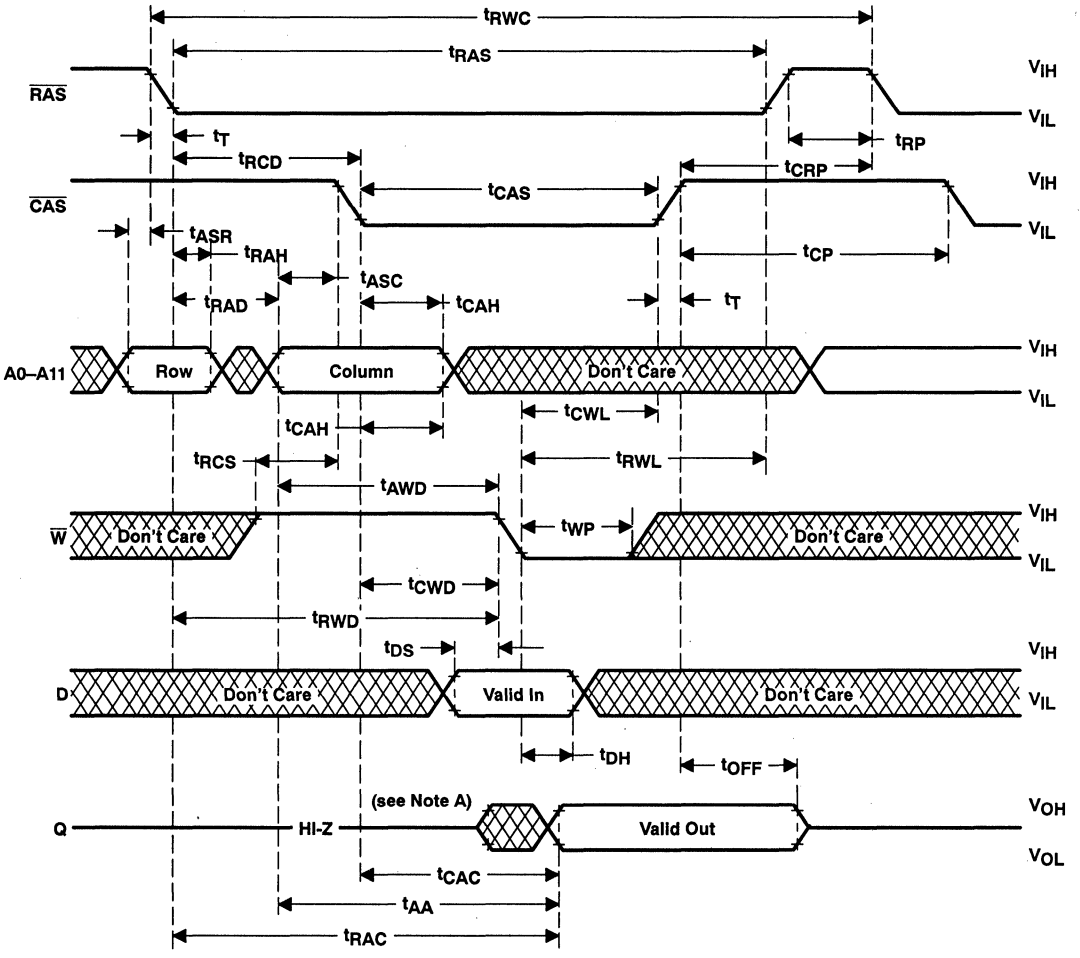


Figure 4. Write Cycle Timing

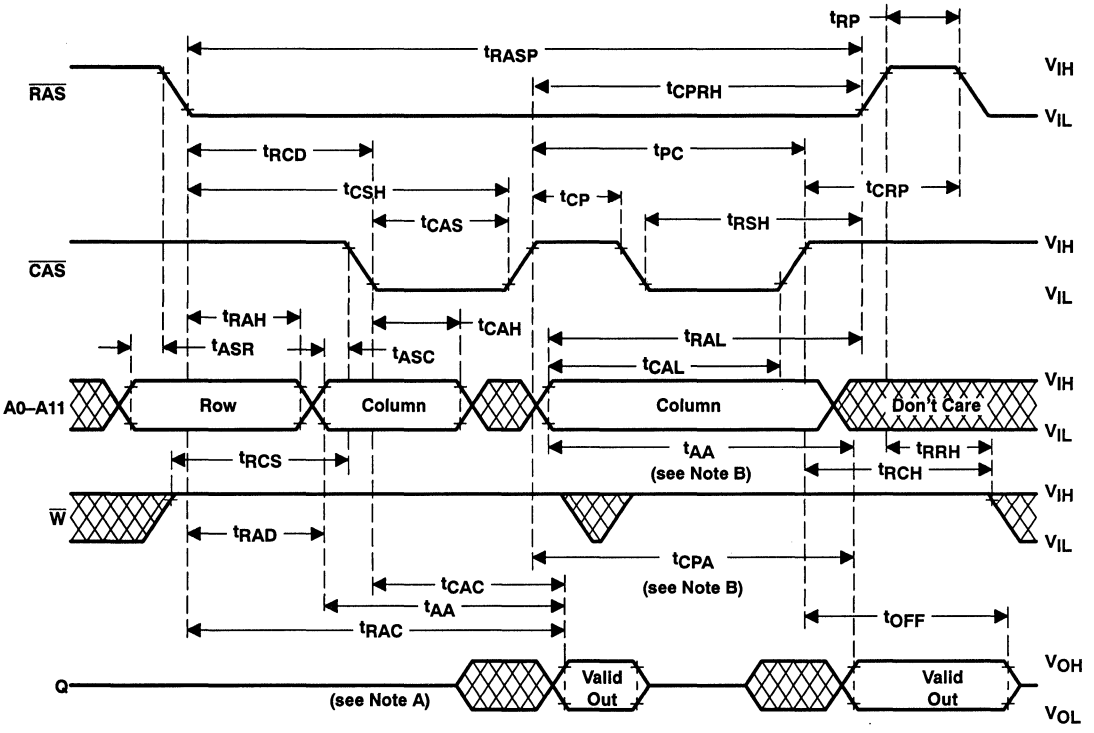
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

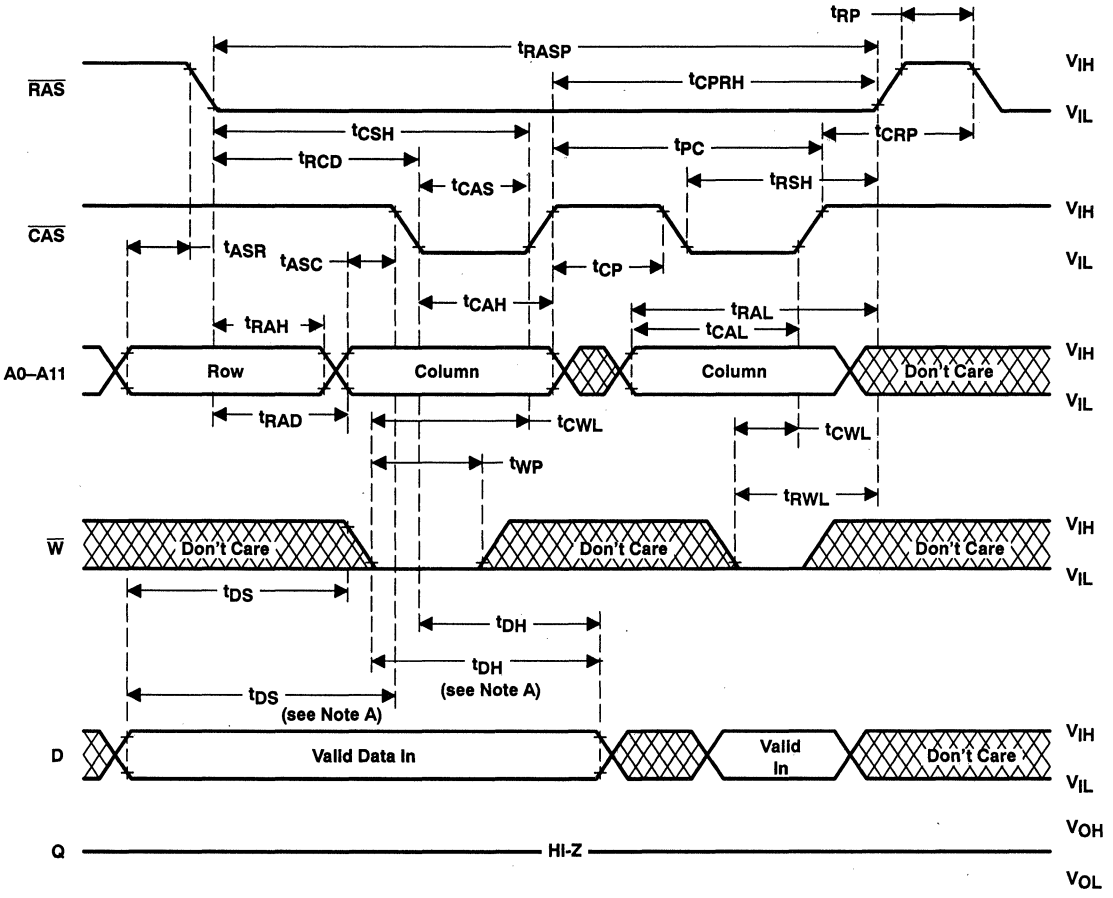
PARAMETER MEASUREMENT INFORMATION



NOTES: A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B: Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

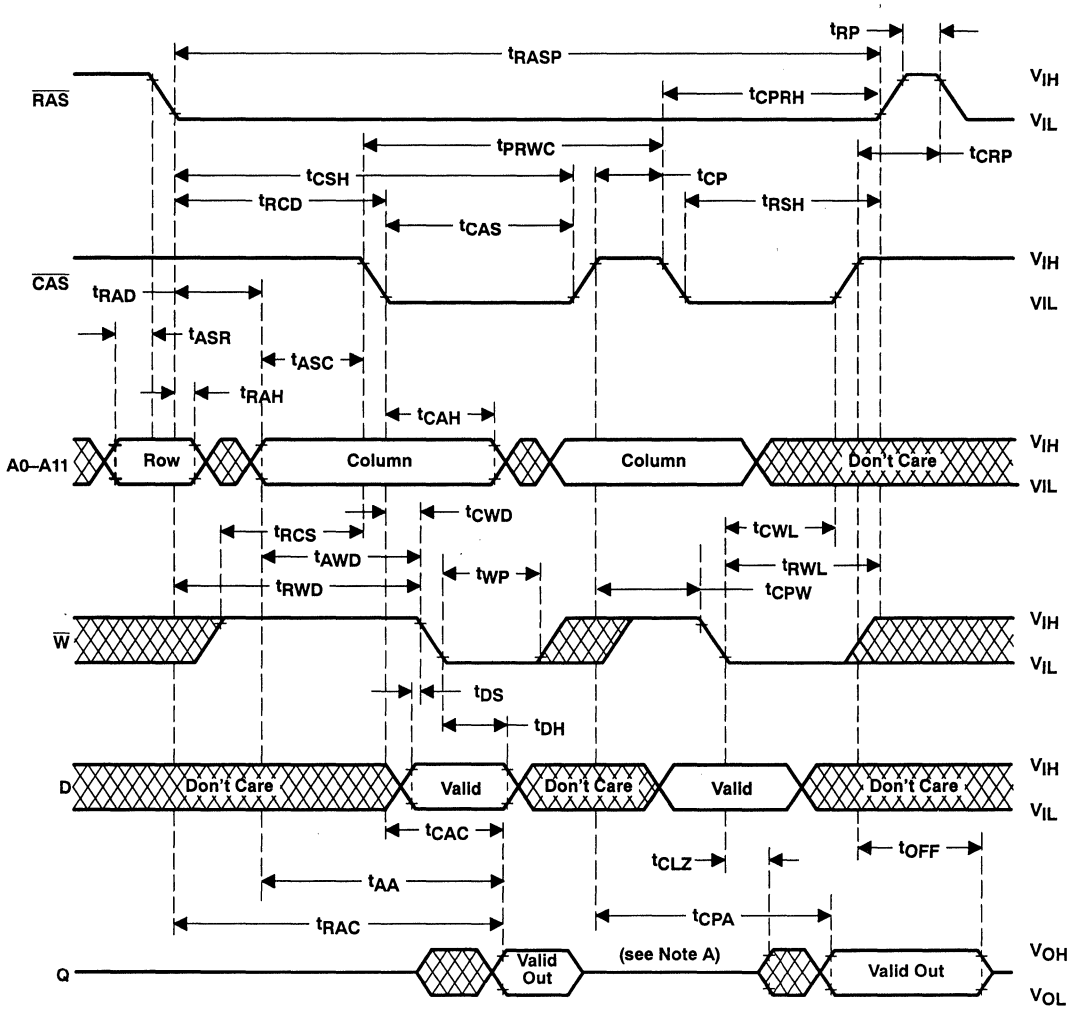
PARAMETER MEASUREMENT INFORMATION



NOTES: A: Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B: A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

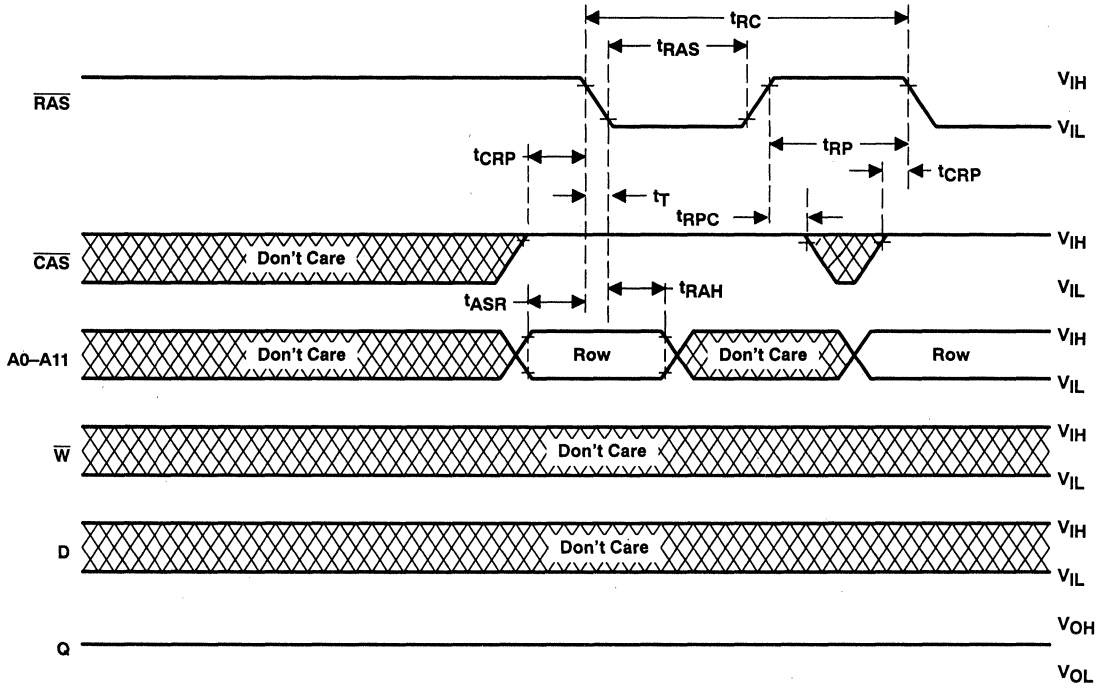


Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

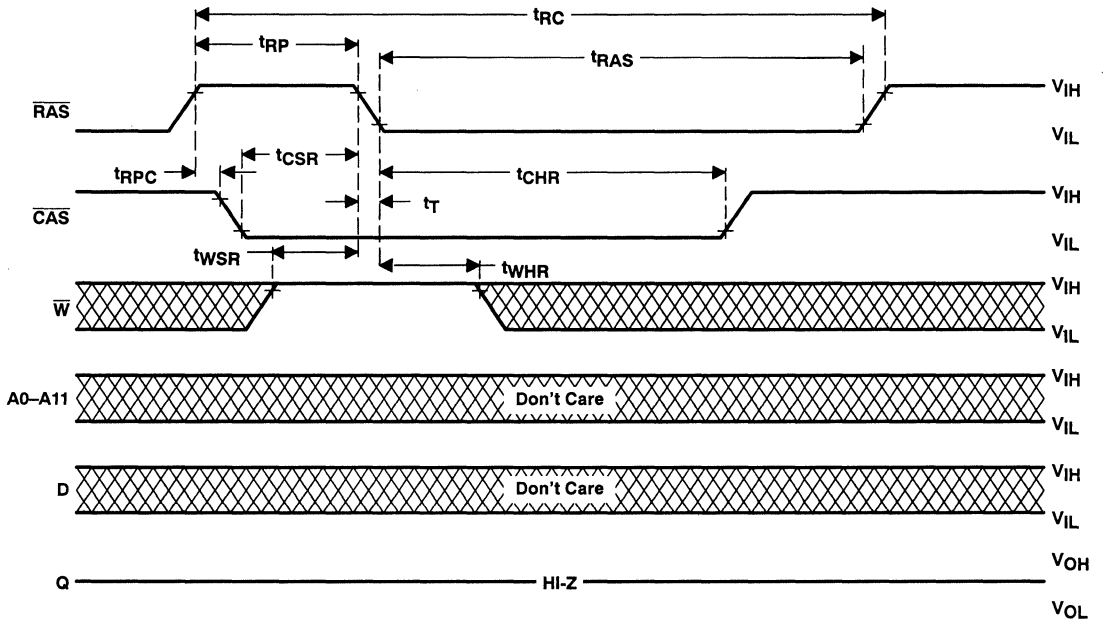


Figure 10. Automatic ($\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

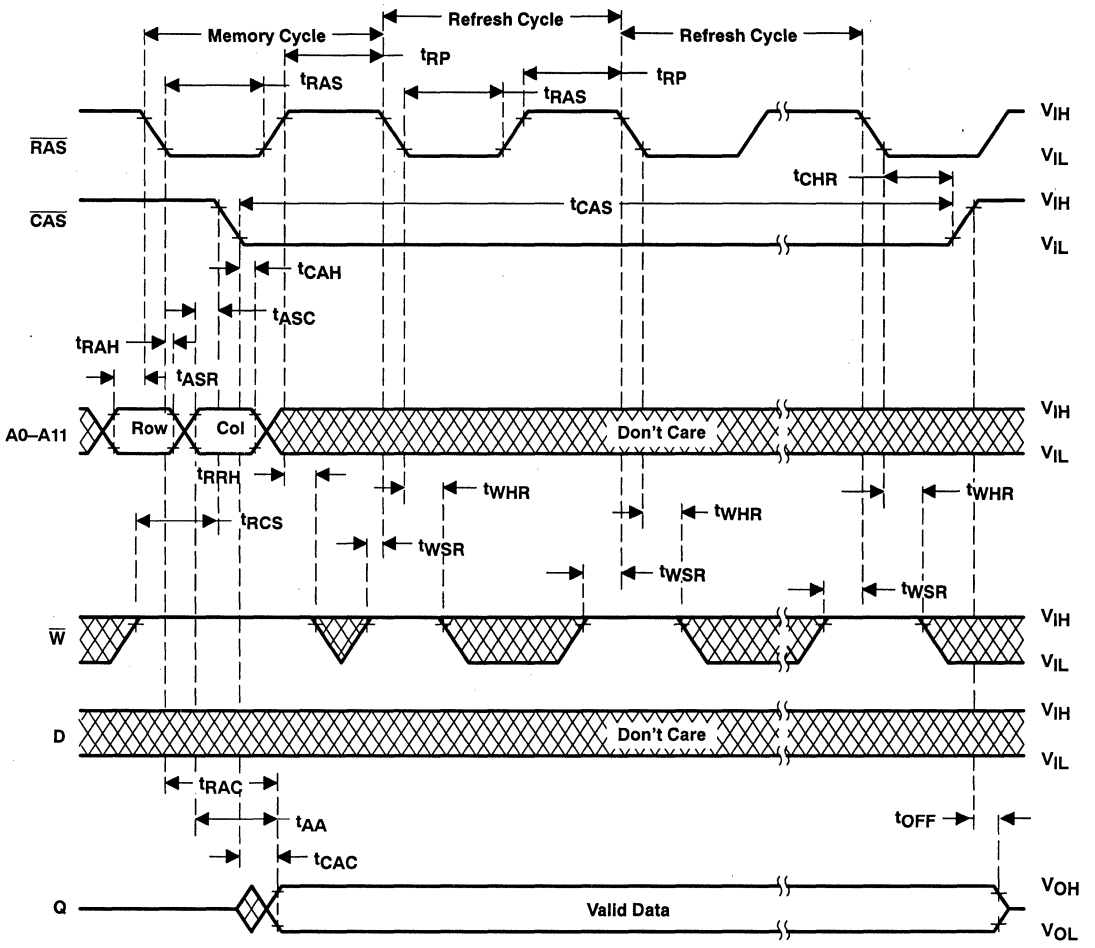


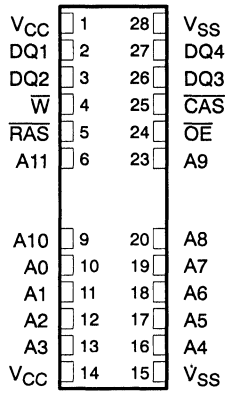
Figure 11. Hidden Refresh Cycle (Read)

- **Organization . . . 4 194 304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

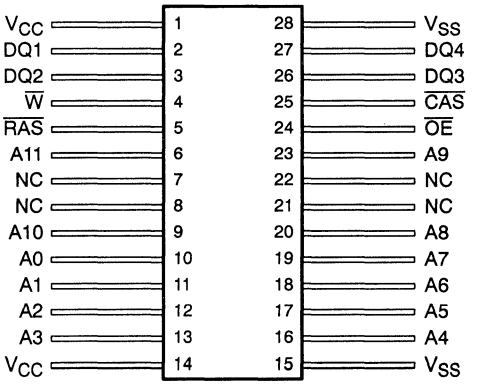
	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
SMJ416400-60	60 ns	15 ns	30 ns	110 ns
SMJ416400-70	70 ns	18 ns	35 ns	130 ns
SMJ416400-80	80 ns	20 ns	40 ns	150 ns
SMJ416400-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 4096 Cycles Refresh in 64 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range – 55°C to 125°C**

FNC PACKAGE†
(TOP VIEW)



HKB PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

description

The SMJ416400 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 4 194 304 words by four bits each. They employ EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

All inputs, outputs, and clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ416400 is offered in 450-mil 24/28-pin surface mount SOLCC (FNC suffix) and flatpack (HKB suffix) packages. The packages are characterized for operation from –55°C to 125°C.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the SMJ416400 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as "enhanced page mode". Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{OEA} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched onto the chip by the row address strobe $\overline{RAS}$. Ten column-address bits are set on A0 through A9 and latched onto the chip by the column address strobe ($\overline{CAS}$). Row address A11 is required during a normal access and during $\overline{RAS}$ only refresh as the device requires 4096 refresh cycles. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain for the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixty-four milliseconds to retain data. This can be achieved by strobing each of the 4096 rows (A0-A11). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

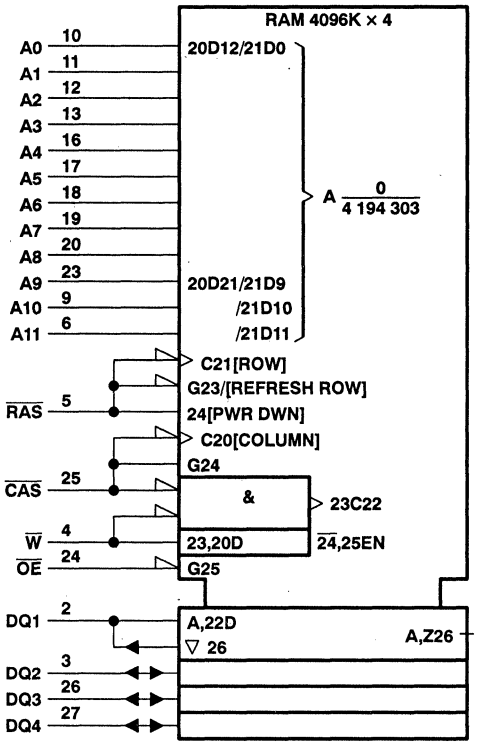
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

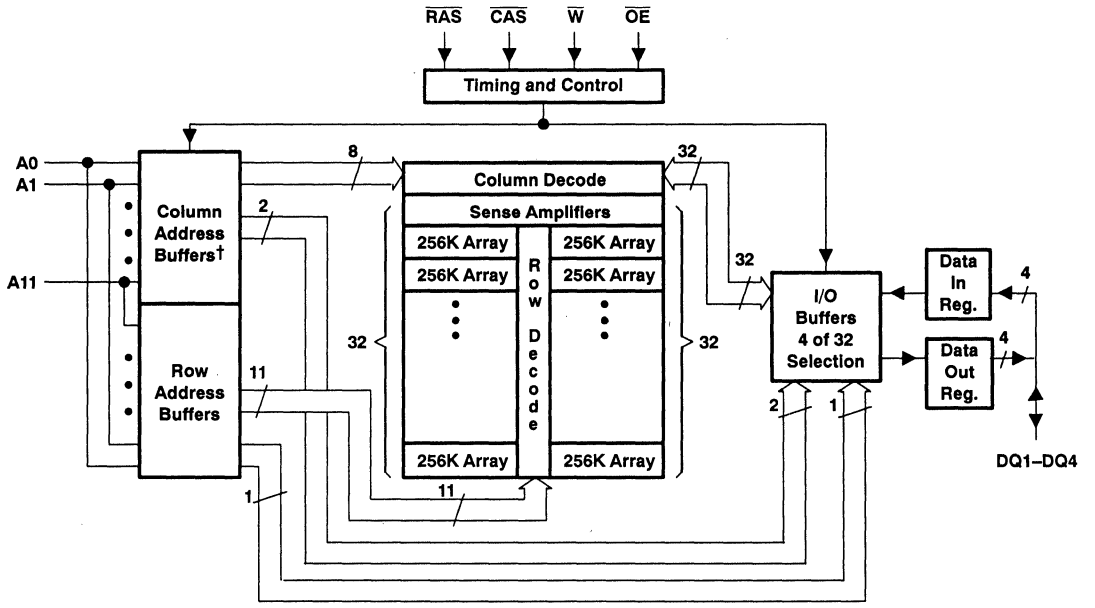
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



† Column Address 10 and Column Address 11 are not used.

absolute maximum ratings over operating free-air temperature†

Voltage on any pin (see Note 1) ..... –1 V to 7 V
Voltage range on V_{CC} ..... –1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... –55°C to 125°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	–55		125	°C

NOTE 2: Then algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'416400-60		'416400-70		'416400-80		'416400-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		90		80		70		60	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.05 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		90		80		70		60	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		65		60		55	mA
I_{CC7}	Standby current output enable‡ (see Note 5)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.
5. Measured with indicated conditions following a normal read cycle.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			8	pF
$C_{i(OE)}$	Input capacitance, output enable			8	pF
$C_{i(W)}$	Input capacitance, write-enable input			8	pF
C_O	Output capacitance			14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'416400-60		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 8)		15		18		20		25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 8)		15		18		20		25	ns

NOTES: 7. Valid data is presented at the outputs after all access times are satisfied but may go from a high-impedance state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

8. t_{OFF} and tOEZ are specified when the outputs are no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'416400-60		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 9)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 10)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 9)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 14)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

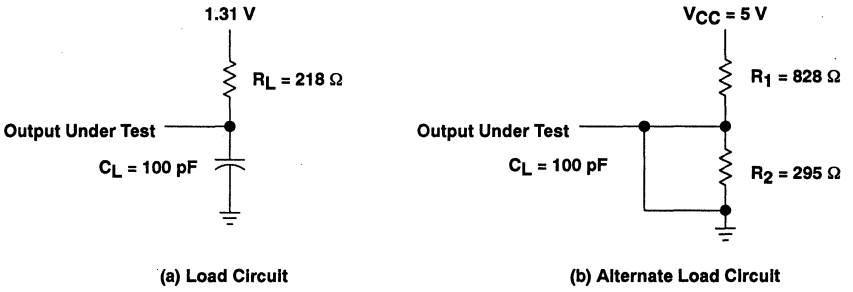
NOTES: 9. All cycle times assume t_T = 5 ns, referenced to $V_{IH(min)}$ and $V_{IL(max)}$.
10. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
11. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
12. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
13. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'416400-60		'416400-70		'416400-80		'416400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 5)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 5)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		135		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	55		63		70		80		ns
t_{REF}	Refresh time interval		64		64		64		64	ms

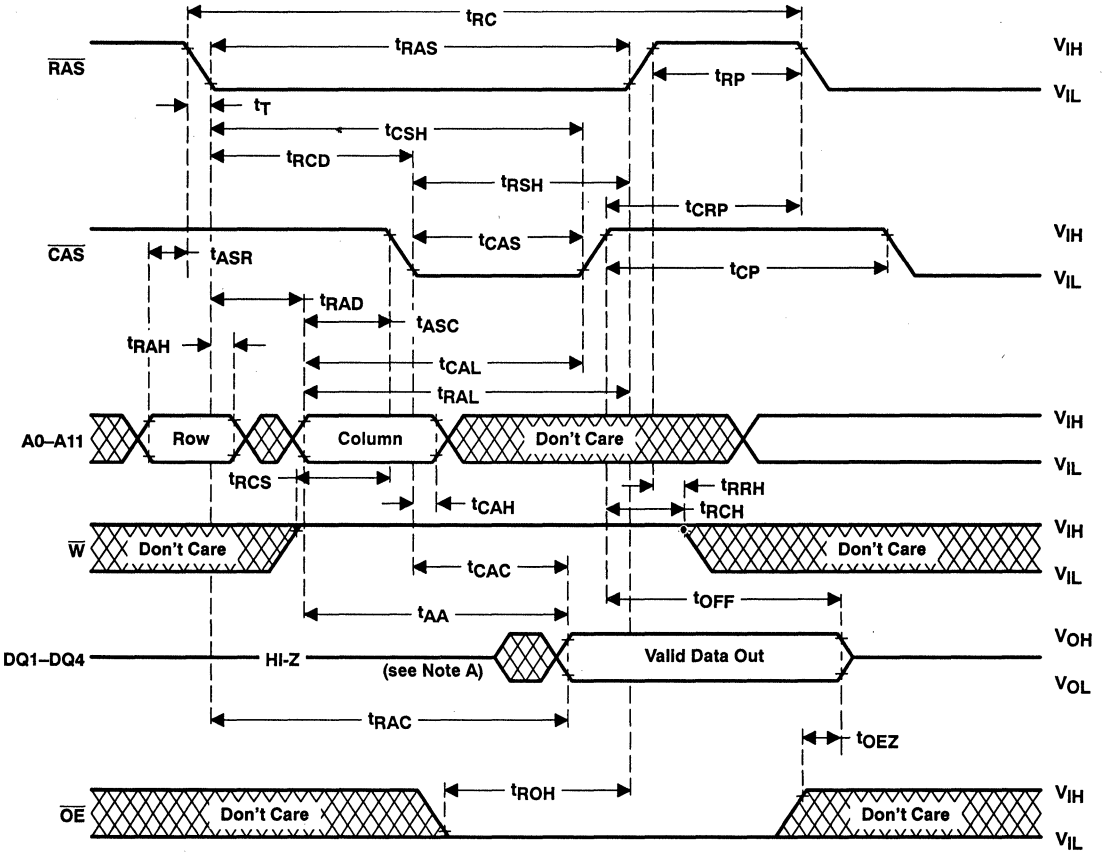
NOTE 15: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

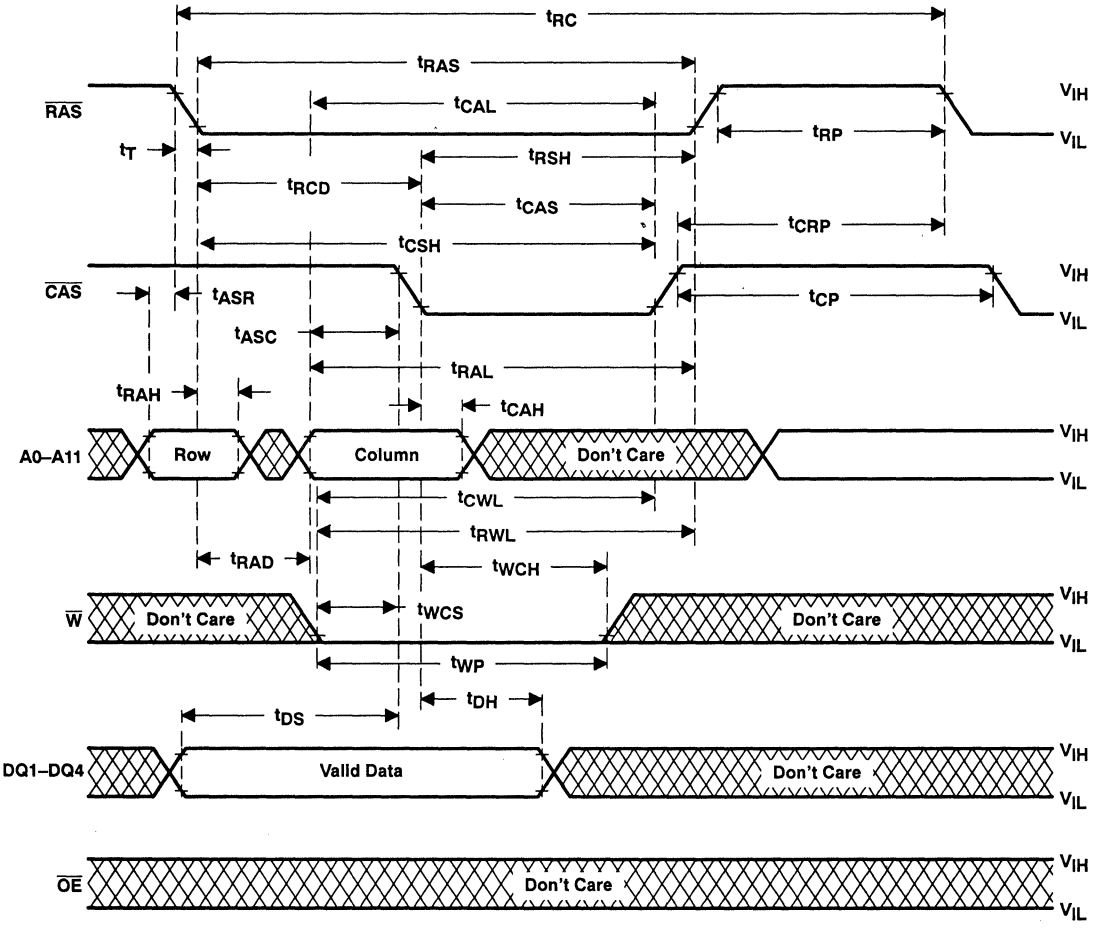


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

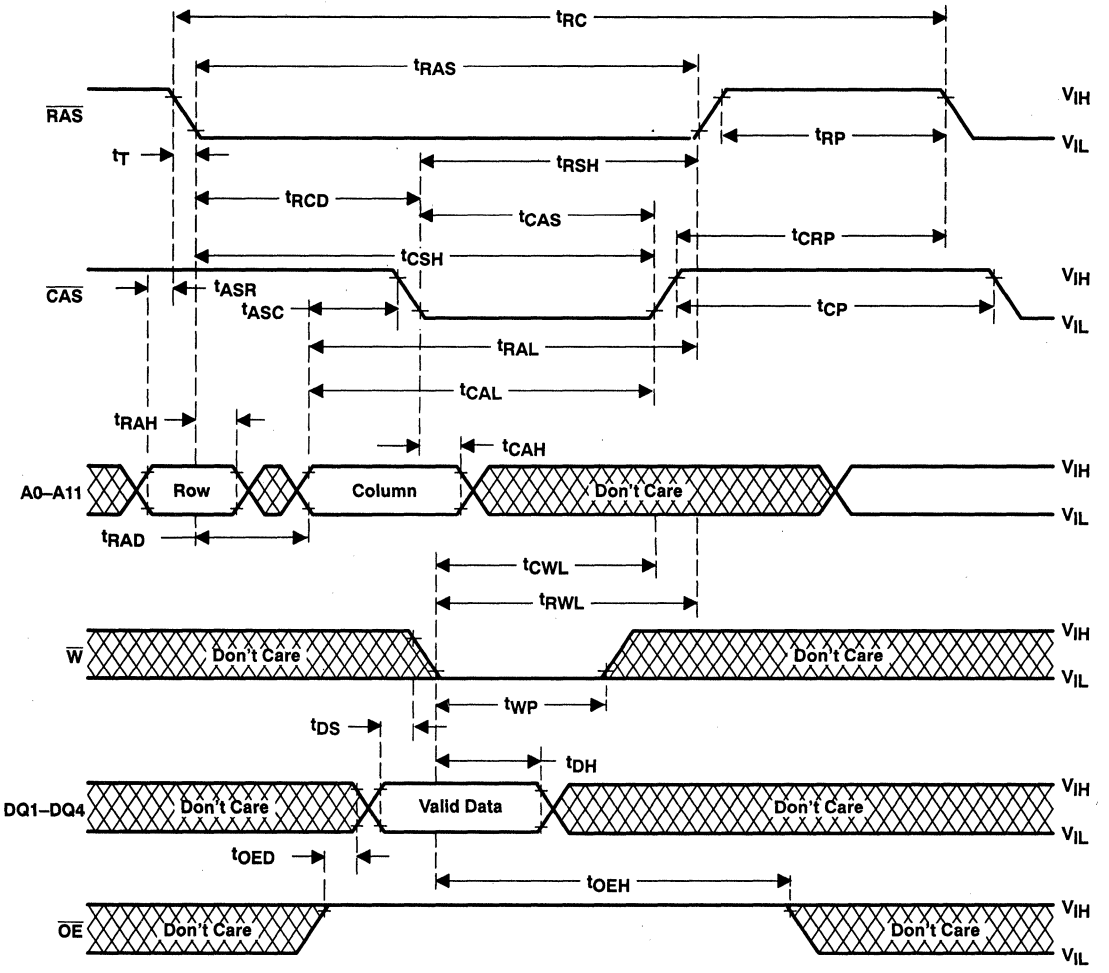
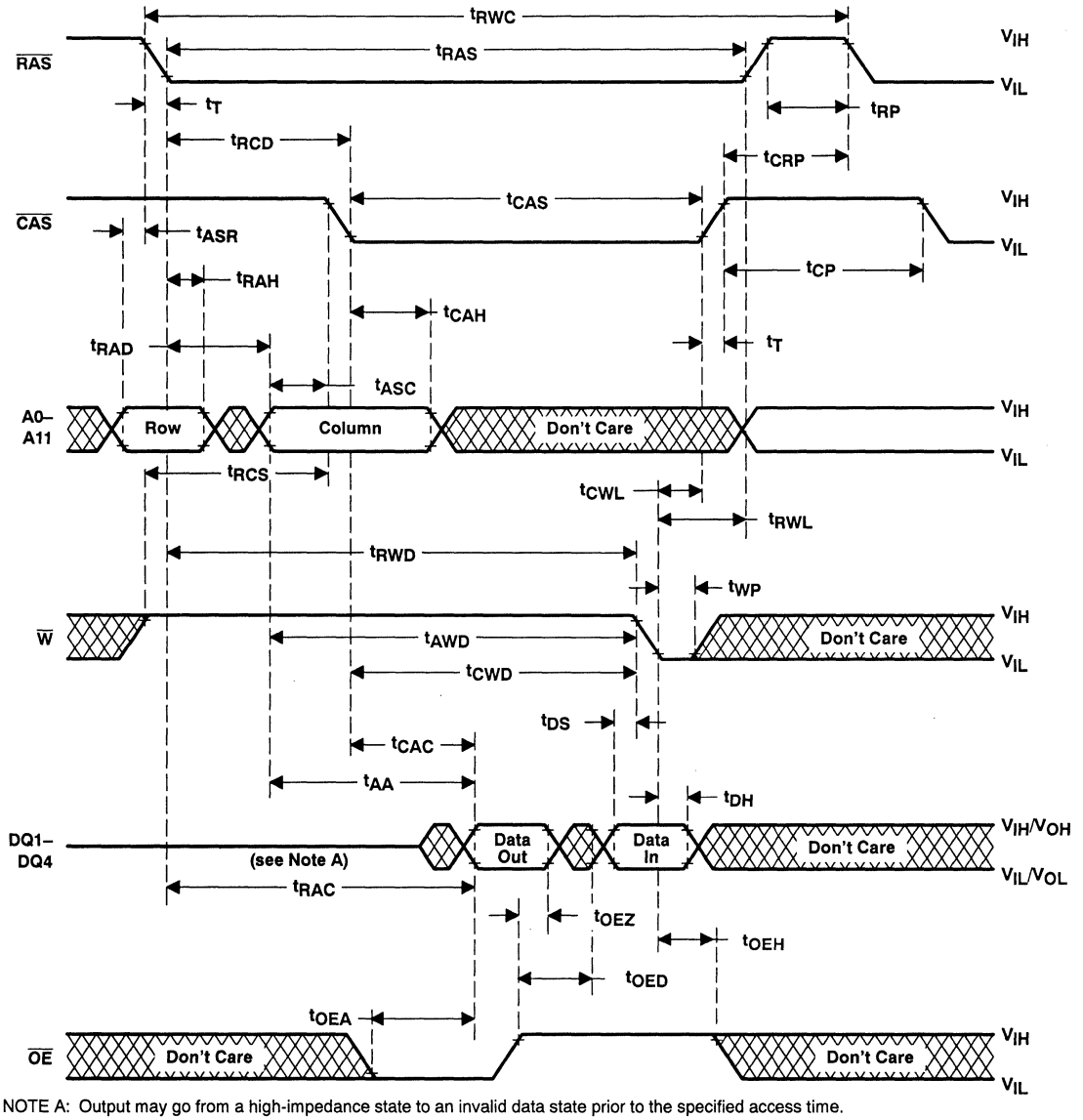


Figure 4. Write Cycle Timing

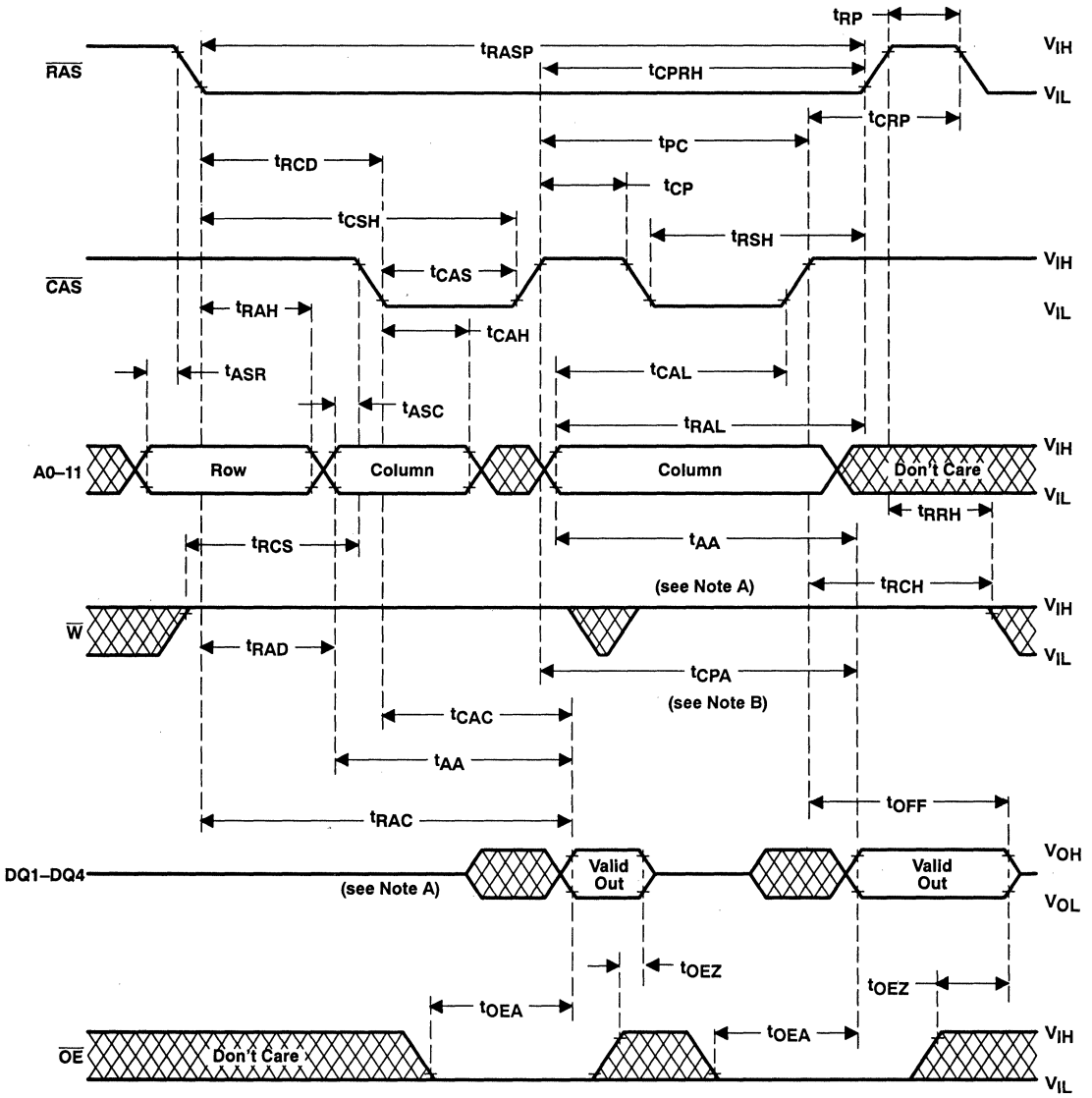
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

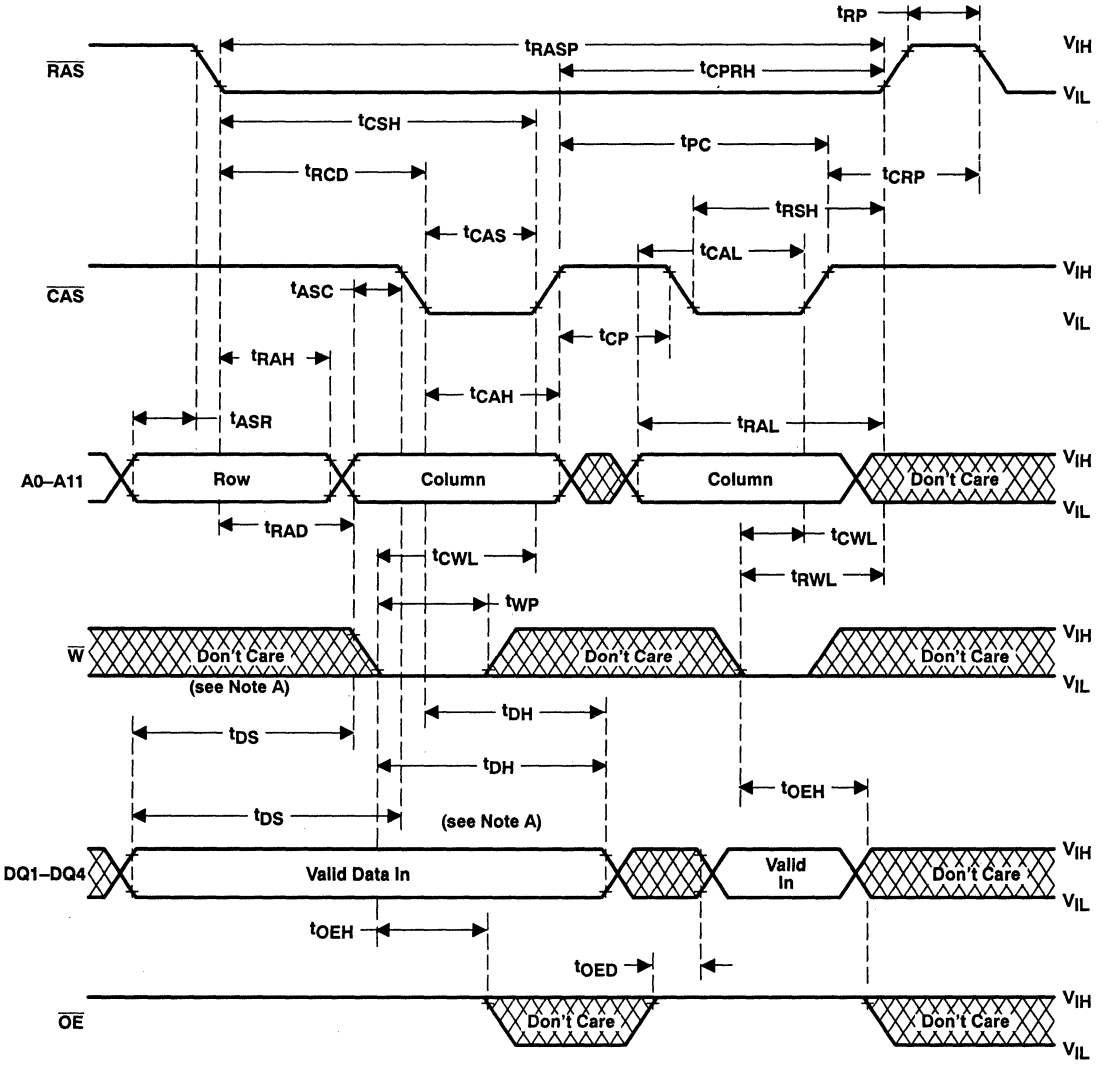
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

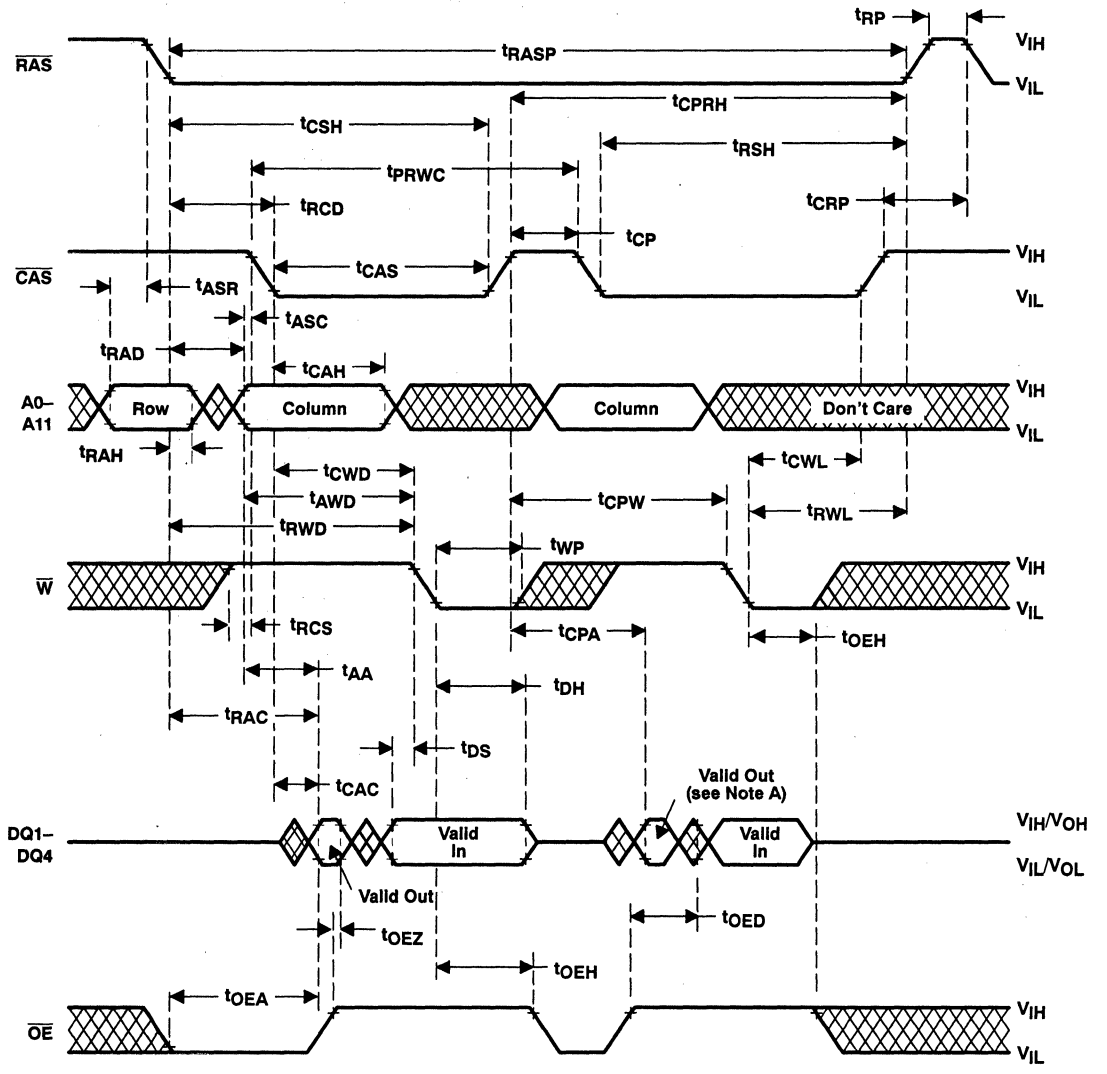
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

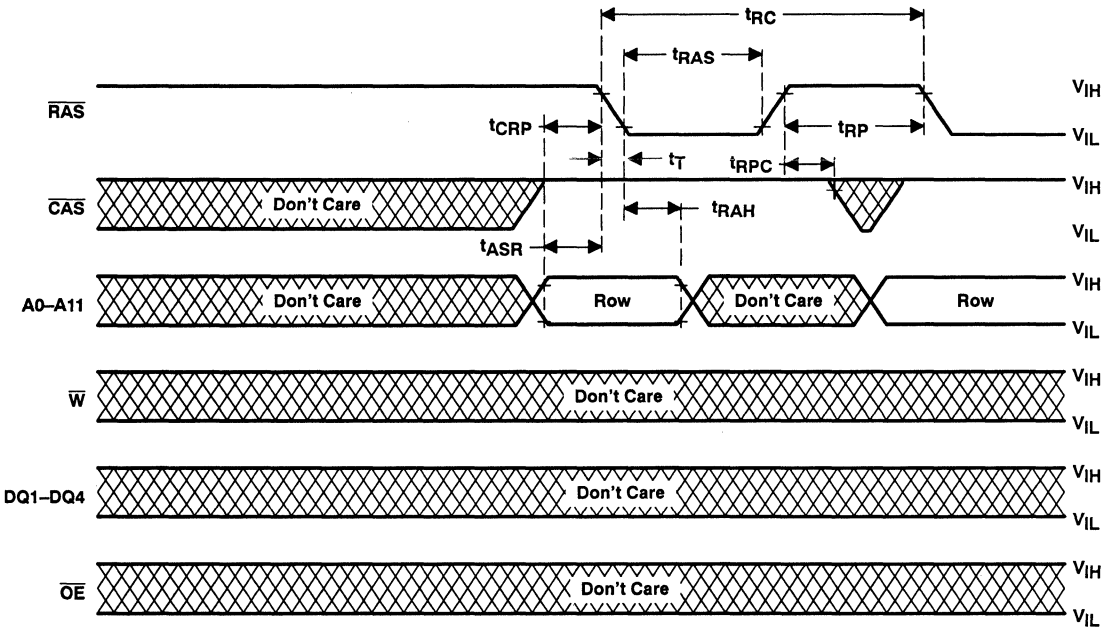


Figure 9. $\overline{RAS}$-Only Refresh Timing

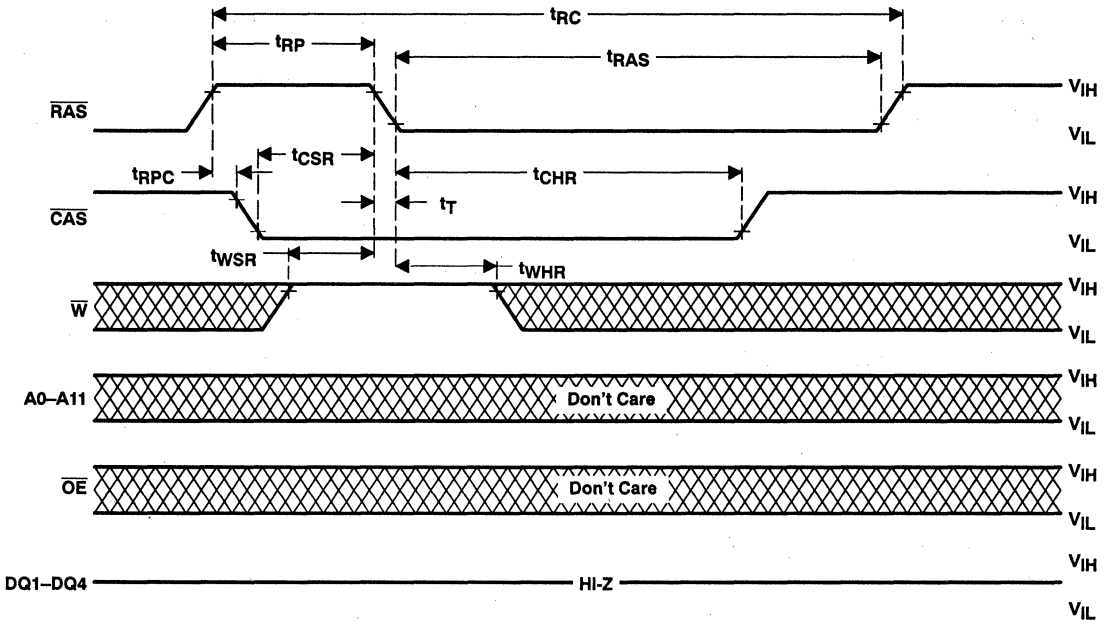


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

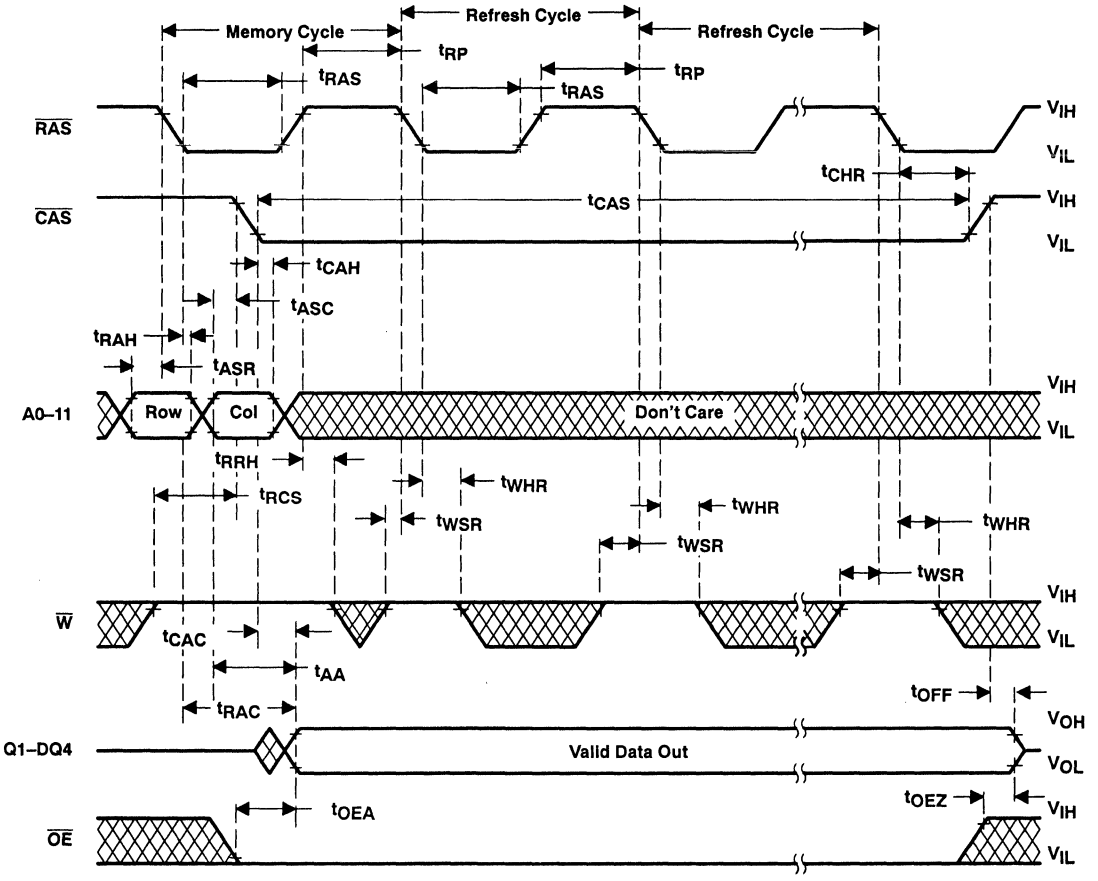


Figure 11. Hidden Refresh Cycle (Read)

- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
SMJ417100-60	60 ns	15 ns	30 ns	110 ns
SMJ417100-70	70 ns	18 ns	35 ns	130 ns
SMJ417100-80	80 ns	20 ns	40 ns	150 ns
SMJ417100-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 2048 Cycles Refresh in 32 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range – 55°C to 125°C**

description

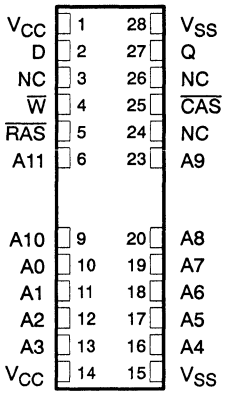
The SMJ417100 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 16 777 216-bit words by one bit each. They employ EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

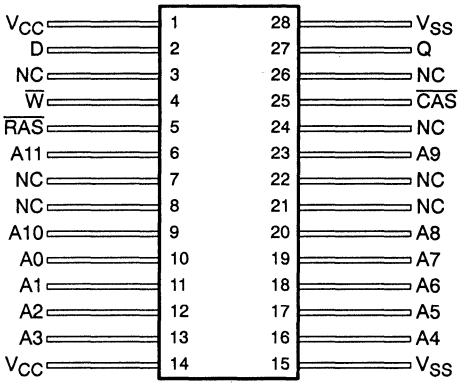
All inputs, outputs, and clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ417100 is offered in 450-mil 24/28-pin surface mount SOLCC (FNC suffix) and flatpack (HKB suffix) packages. The packages are characterized for operation from – 55°C to 125°C.

FNC PACKAGE†
(TOP VIEW)



HKB PACKAGE†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Internal Connection
Q	Data Out
$\overline{RAS}$	Row-Address strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$-low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the SMJ417100 to operate at a higher data bandwidth than conventional page-mode parts, since retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode.* Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{RAC} have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A11)

Twenty-four address bits are required to decode 1 of 16 777 216 storage cell locations. Twelve row-address bits are set on inputs A0 through A11 and latched during a normal access. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable $\overline{W}$ input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 54 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, or t_{CPA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

refresh

A refresh operation must be performed at least once every thirty-two milliseconds to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

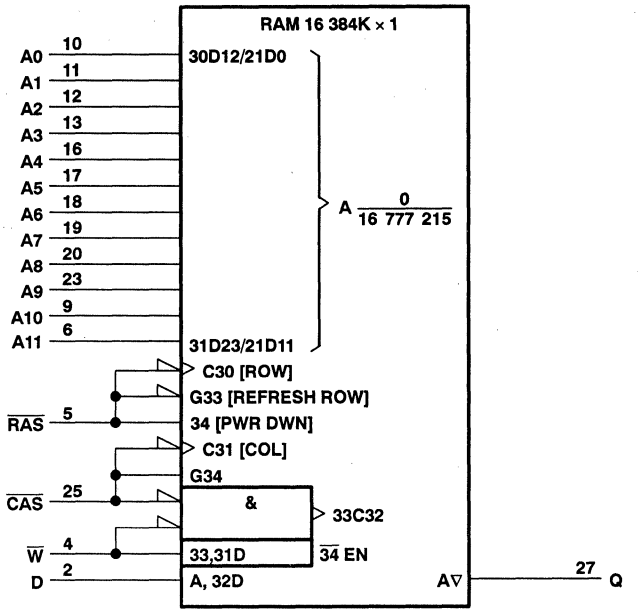
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

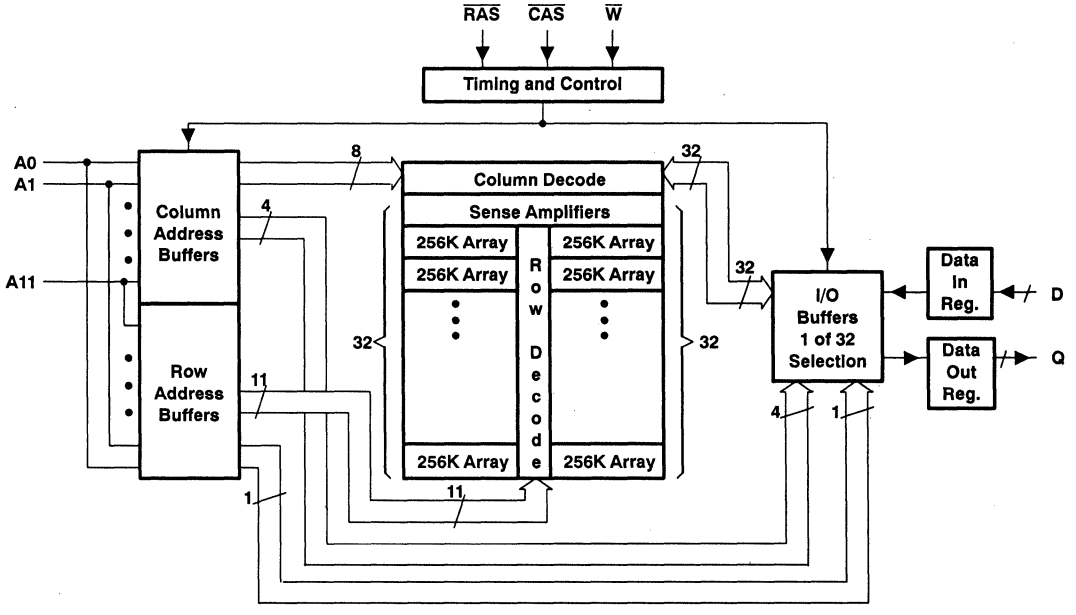
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1) ..... – 1 V to 7 V
Voltage on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		110		100		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		110		100		90		80	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		65		60		55	mA
I_{CC7}	Standby current output enable‡ (see Note 5)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.
5. Measured with indicated conditions following a normal read cycle.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			9	pF
$C_{i(D)}$	Input capacitance, data input			8	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			8	pF
$C_{i(W)}$	Input capacitance, write-enable input			8	pF
C_O	Output capacitance			14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25° C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 8)	0	15	0	18	0	20	0	25	ns

NOTES: 7. Valid data is presented at the output after all access times are satisfied but may go from a high-impedance state to an invalid data state prior to the specified access times as the output is driven when $\overline{CAS}$ goes low.

8. t_{OFF} is specified when the output is no longer dirven. The output is disabled by bringing $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 9)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	130		153		175		210		ns
t_{PC}	Page-mode read or write cycle time (see Note 10)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	60		68		75		85		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 12)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 13)	0		0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 12)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 14)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

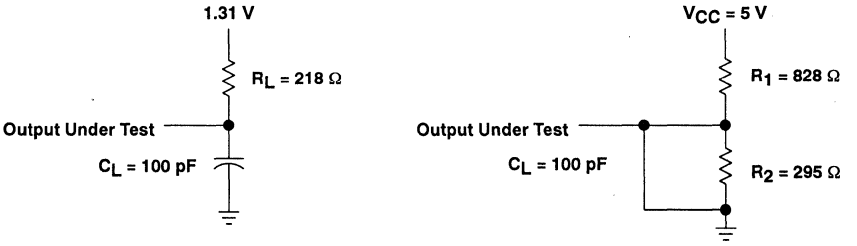
NOTES: 9. All cycle times assume t_T = 5 ns, referenced to V_{IH}(min) and V_{IL}(max).
10. To guarantee t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
11. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
12. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
13. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		SMJ417100-60		SMJ417100-70		SMJ417100-80		SMJ417100-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	30		35		40		45		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	15		18		20		25		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	60		70		80		100		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{REF}	Refresh time interval		32		32		32		32	ms

NOTE 15: The maximum value is specified only to assure access time.

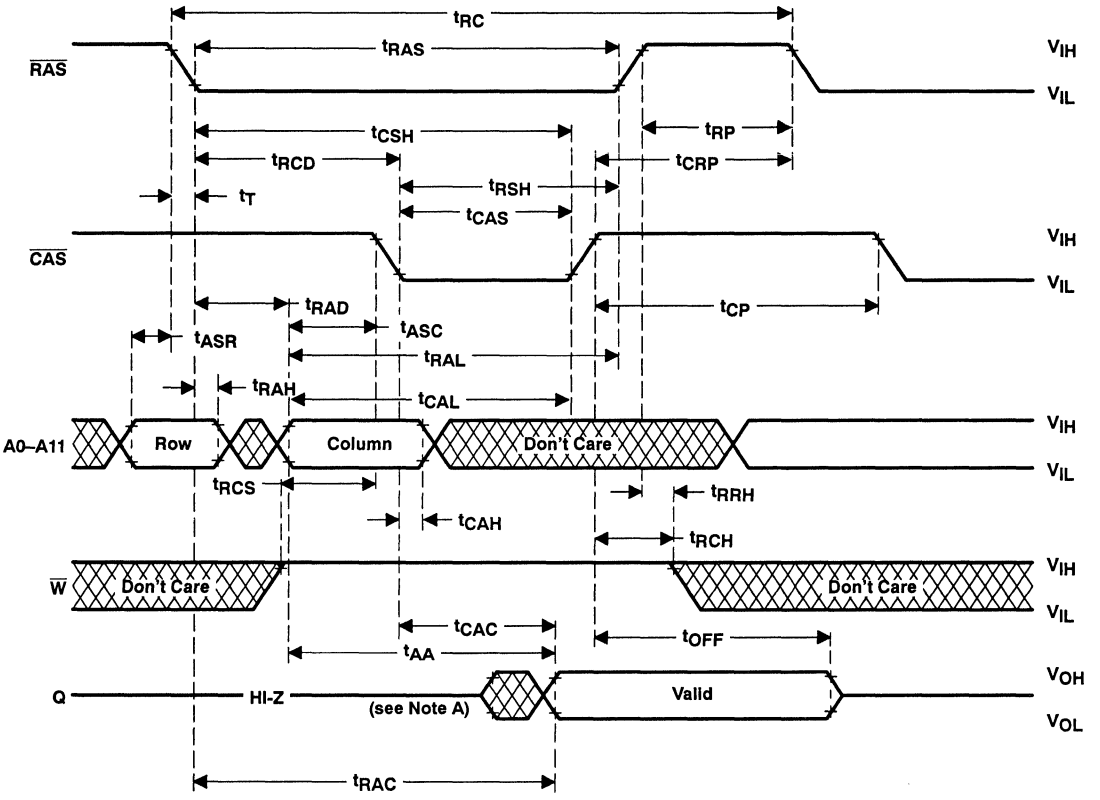
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

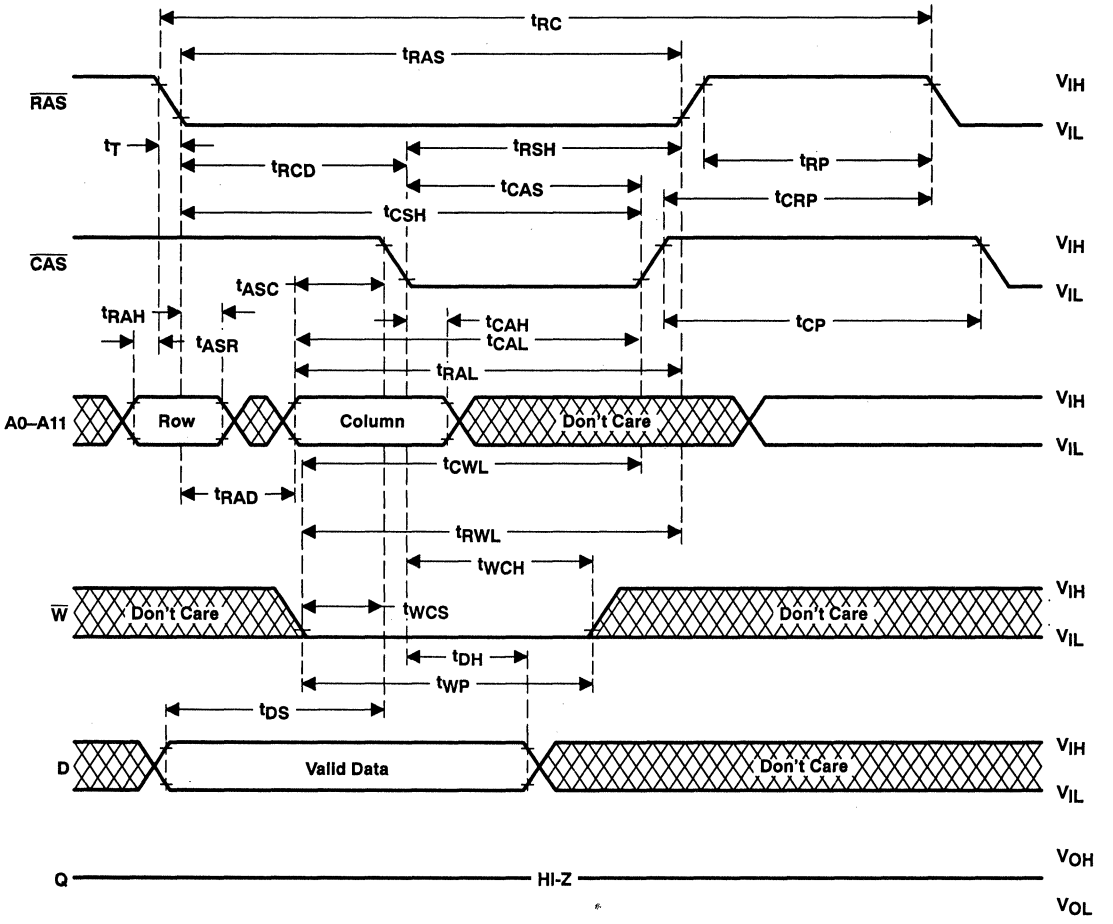


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

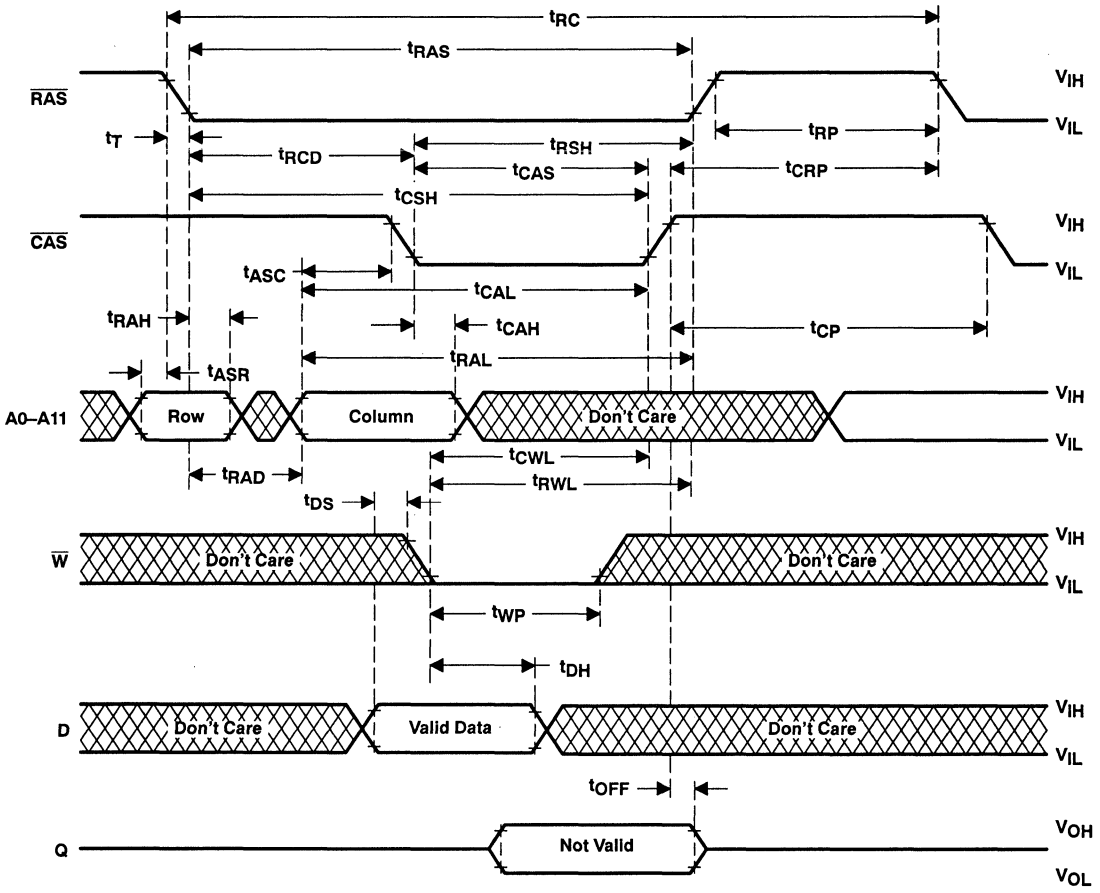
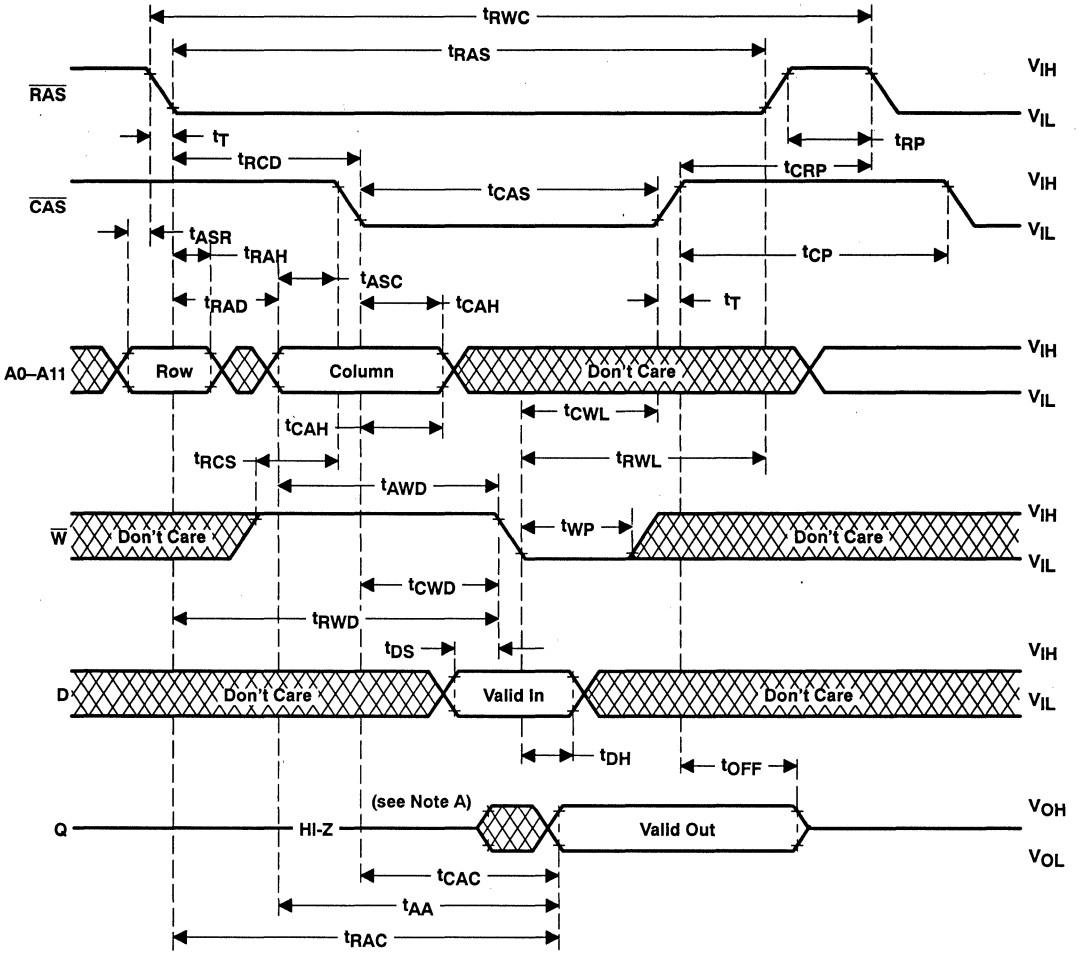


Figure 4. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

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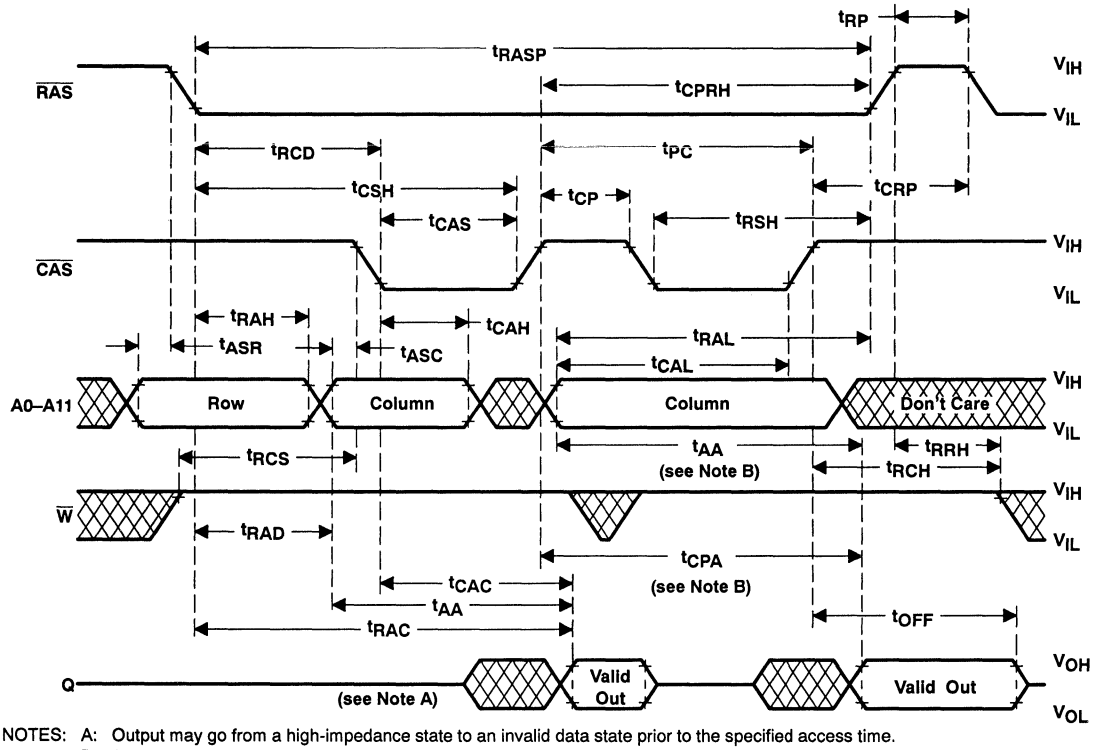
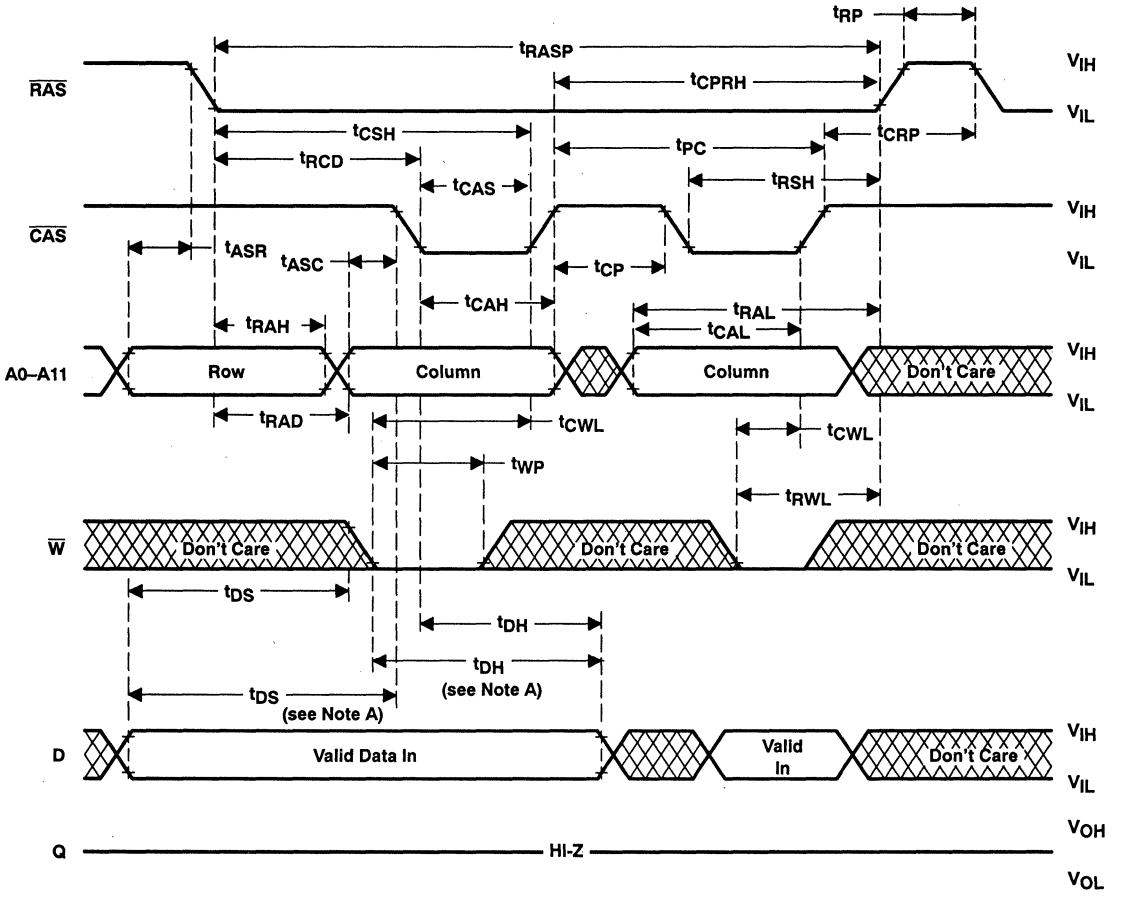
PARAMETER MEASUREMENT INFORMATION



NOTES: A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B: Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

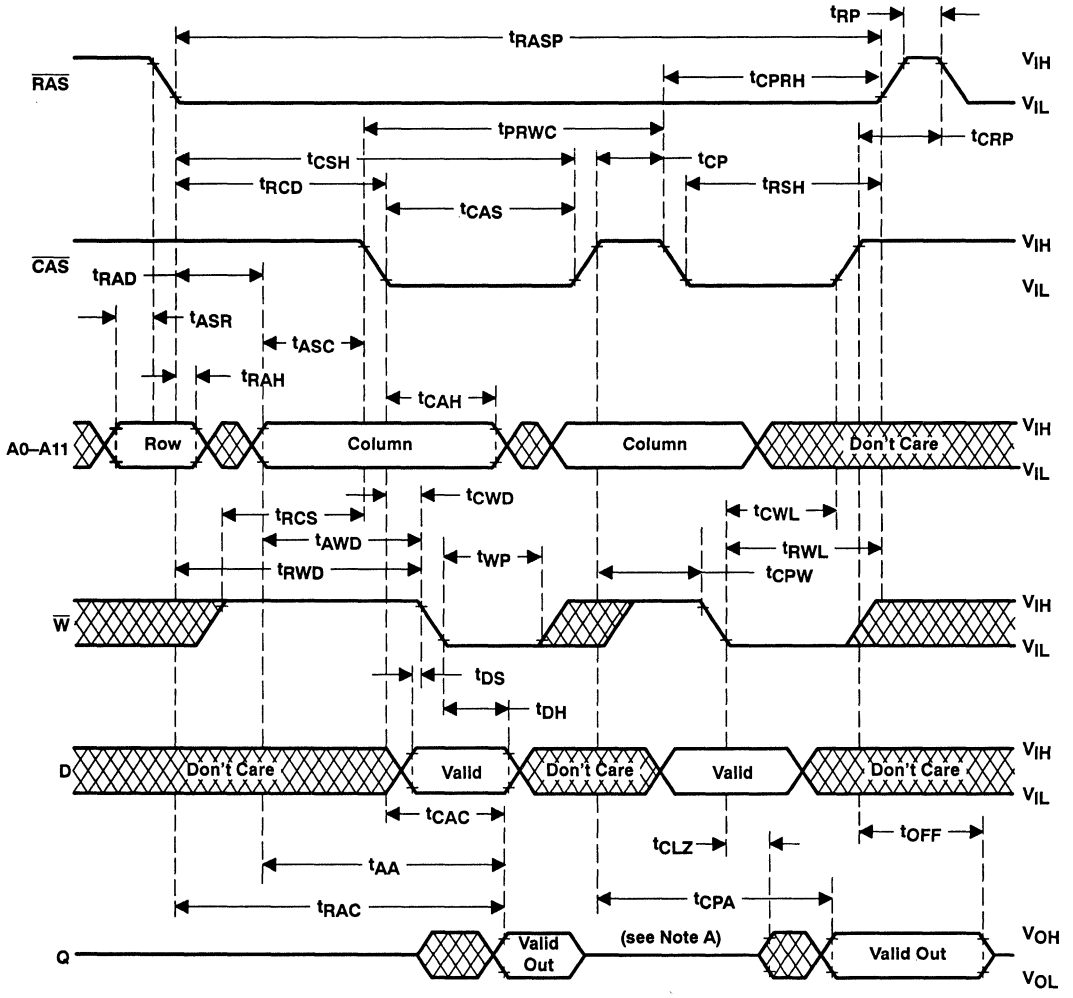
PARAMETER MEASUREMENT INFORMATION



NOTES: A: Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B: A read cycle or a read-write cycle can be intermixed with write cycle as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

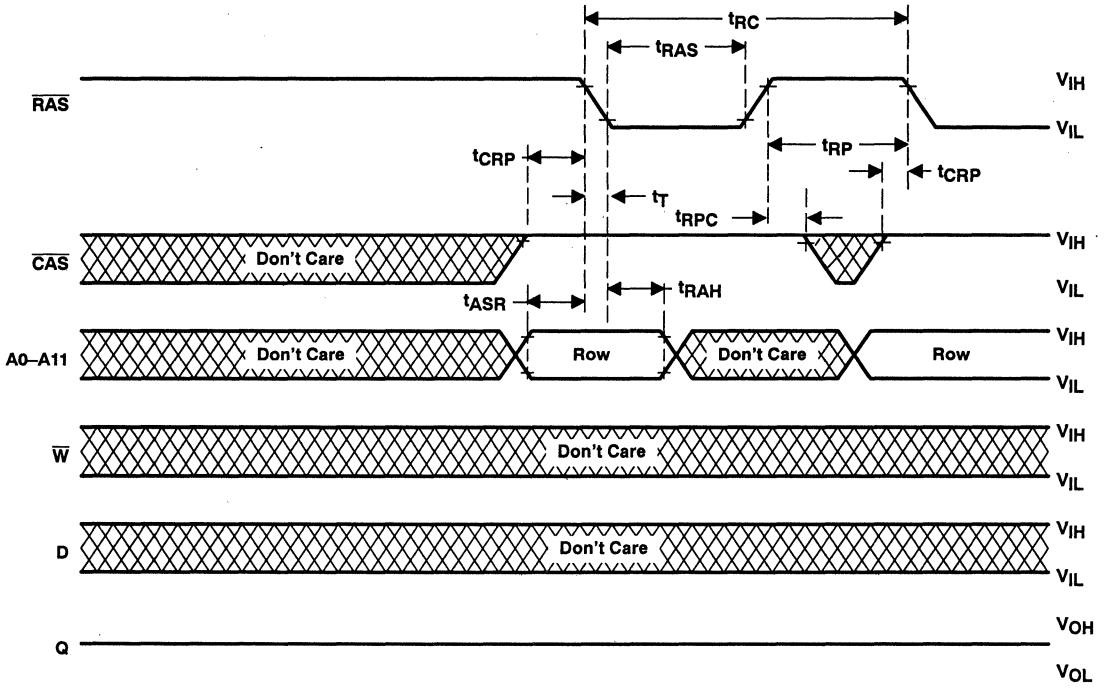


Figure 9. $\overline{RAS}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

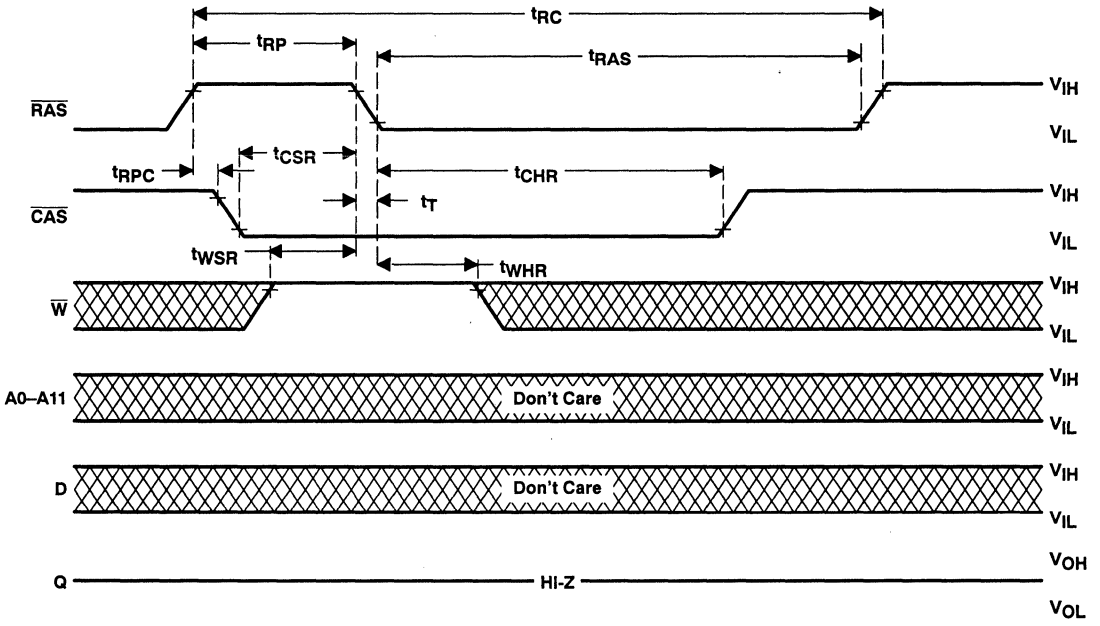

Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

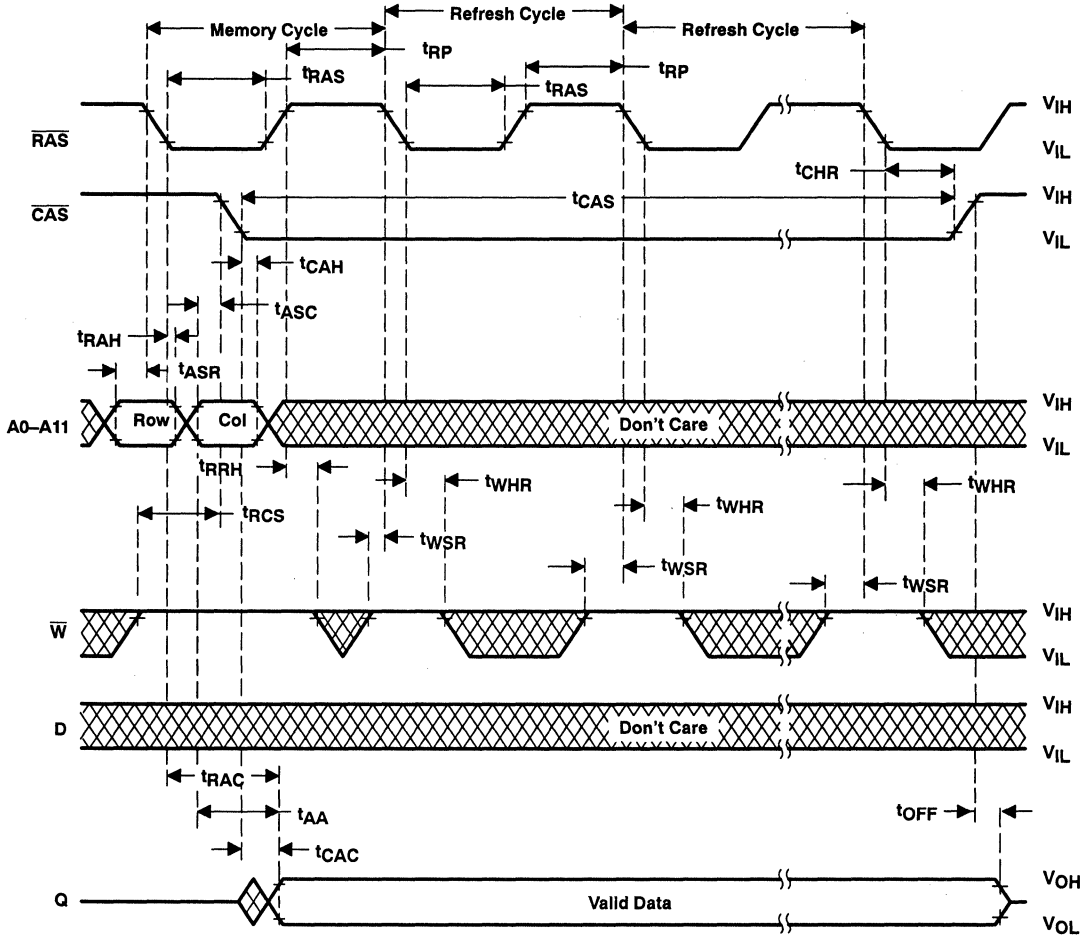

Figure 11. Hidden Refresh Cycle (Read)

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- **Organization . . . 4 194 304 × 4**
- **Single 5-V Power Supply (10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	READ OR WRITE CYCLE (MIN)
SMJ417400-60	60 ns	15 ns	30 ns	110 ns
SMJ417400-70	70 ns	18 ns	35 ns	130 ns
SMJ417400-80	80 ns	20 ns	40 ns	150 ns
SMJ417400-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 2048 Cycles Refresh in 32 ms**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **Operating Free-Air Temperature Range –55°C to 125°C**

description

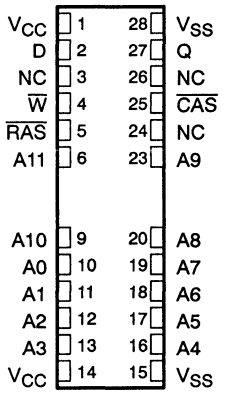
The SMJ417400 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 4 194 304-bit words by four bits each. They employ EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, 80 ns, and 100 ns.

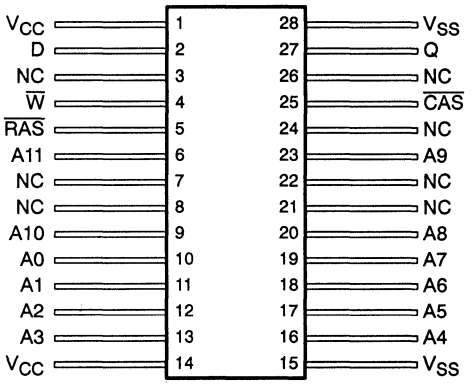
All inputs, outputs, and clocks are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ417400 is offered in a 450-mil 24/28-pin surface mount SOLCC (FNC suffix) and flatpack (HKB suffix) packages. The packages are characterized for operation from –55°C to 125°C.

FNC PACKAGE†
(TOP VIEW)



HKB PACKAGE†
(TOP VIEW)



† Packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A11	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by t_{RAS}, the maximum $\overline{RAS}$ low width.

The Column Address Buffers in this CMOS device are activated on the falling edge of $\overline{RAS}$. They act as a transparent or flow-through latch, while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the addresses into these buffers and also serves as an output enable.

This feature allows the SMJ417400 to operate at a higher data bandwidth than conventional page-mode parts, because retrieval begins as soon as the column address is valid, rather than when $\overline{CAS}$ transitions low. The performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) and t_{OEA} (access time from output enable) have been satisfied. In the event that the column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time is determined by the later occurrence of t_{CPA} or t_{CAC}.

address (A0–A10)

Twenty-two address bits are required to decode 1 of 4 194 304 storage cell locations. Eleven row-address bits are set on inputs A0 through A10 and latched onto the chip by the Row Address Strobe $\overline{RAS}$. Eleven column-address bits are set on A0 through A10. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data-in/data-out (DQ1–DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In the early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fan-out of two Series 74 TTL loads. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid at the latest occurrence of t_{RAC}, t_{AA}, t_{CAC}, t_{CPA}, or t_{OEA} and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output does not change, but retains the state just read.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every 32 milliseconds to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at a high (inactive) level, thus conserving power since the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after the specified precharge period, similar to a $\overline{RAS}$-only refresh cycle except with $\overline{CAS}$ held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal refresh address provides the refresh address during hidden refresh.

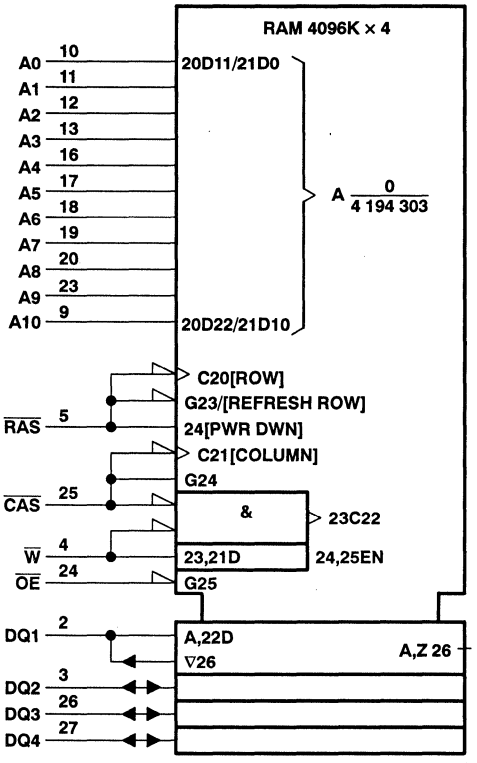
$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

power up

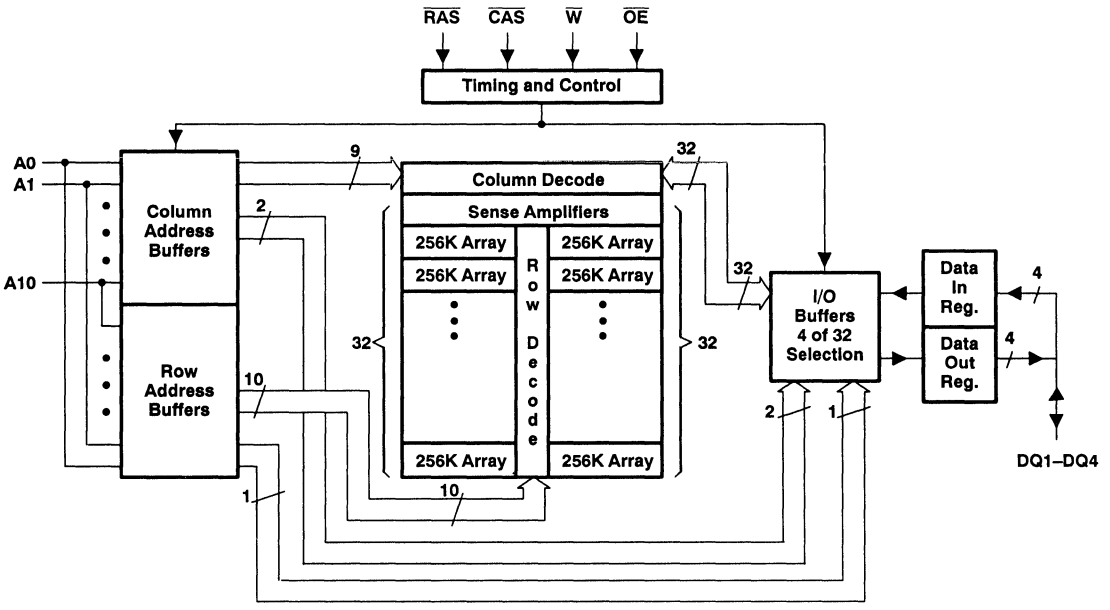
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ417400-60		SMJ417400-70		SMJ417400-80		SMJ417400-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V
I_I	Input current (leakage)‡	V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10		± 10	µA
I_O	Output current (leakage)‡	V_O = 0 to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		110		100		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		2		2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		1		1		1		1	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)‡	$\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		110		100		90		80	mA
I_{CC4}	Average page current (see Note 4)‡	$\overline{RAS}$ low, $\overline{CAS}$ cycling		70		65		60		55	mA
I_{CC7}	Standby current output enable (see Note 5)‡	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled		5		5		5		5	mA

‡ Minimum cycle, V_{CC} = 5.5 V.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one adddress change while $\overline{CAS}$ = V_{IH}.
5. Measured with indicated conditions following a normal read cycle.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			9	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			8	pF
$C_{i(OE)}$	Input capacitance, output enable			8	pF
$C_{i(W)}$	Input capacitance, write-enable input			8	pF
C_O	Output capacitance			14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major changes. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		SMJ417400-60		SMJ417400-70		SMJ417400-80		SMJ417400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40		45	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20		25	ns
t_{CPA}	Access time from column precharge		35		40		45		50	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20		25	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 8)	0	15	0	18	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 8)	0	15	0	18	0	20	0	25	ns

NOTES: 7. Valid data is presented at the outputs after all access times are satisfied but may go from a high-impedance state to an invalid data state prior to the specified access times, as the outputs are driven when $\overline{CAS}$ goes low.

8. t_{OFF} and t_{OEZ} are specified when the outputs are no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		SMJ417400-60		SMJ417400-70		SMJ417400-80		SMJ417400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 9)	110		130		150		180		ns
t_{RWC}	Read-write cycle time	155		181		205		245		ns
t_{PC}	Page-mode read or write cycle time (see Note 10)	40		45		50		55		ns
t_{PRWC}	Page-mode read-write cycle time	85		96		105		120		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	100 000	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 11)	60	10 000	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 12)	15	10 000	18	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		70		ns
t_{WP}	Write pulse duration	15		15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		0		ns
t_{DS}	Data setup time (see Note 13)	0		0		0		0		ns
t_{RCS}	Read setup before $\overline{CAS}$ low	0		0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		25		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		25		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		0		ns
t_{WSR}	$\overline{W}$-high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		15		ns
t_{DH}	Data hold time (see Note 13)	10		15		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 14)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 14)	5		5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		15		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns

Continued next page.

NOTES: 9. All cycle times assume t_T = 5 ns, referenced to $V_{IH(min)}$ and $V_{IL(max)}$.
10. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
11. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
12. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
13. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		SMJ417400-60		SMJ417400-70		SMJ417400-80		SMJ417400-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-write operation only)	55		63		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	40		46		50		60		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		25		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		25		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 15)	15	30	15	35	15	40	15	55	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		45		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)	20	45	20	52	20	60	20	75	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	85		98		110		135		ns
t_{CPRH}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		85		ns
t_{REF}	Refresh time interval		32		32		32		32	ms

NOTE 15: The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION

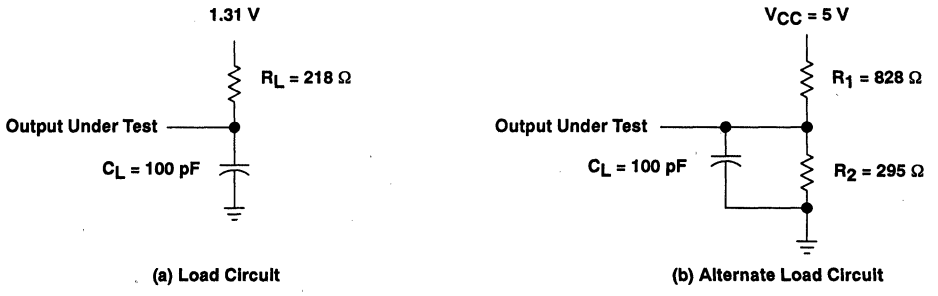
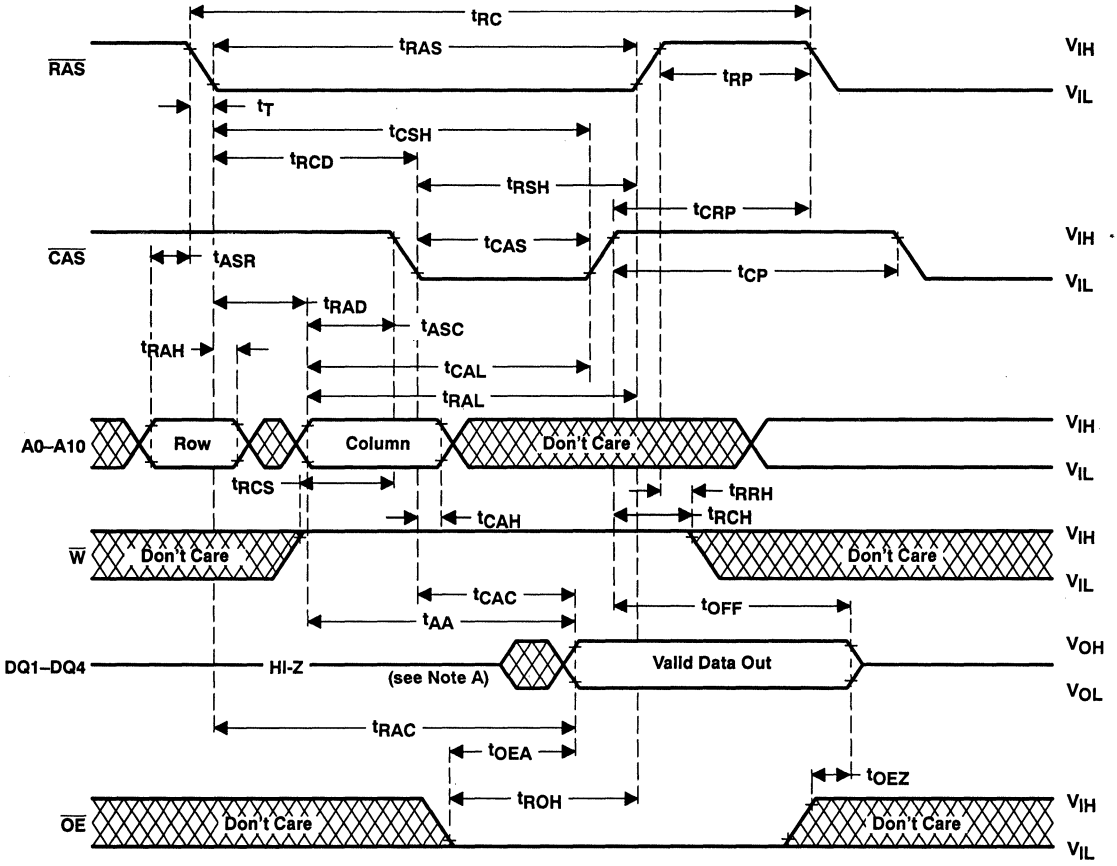


Figure 1. Load Circuits for Timing Parameters



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

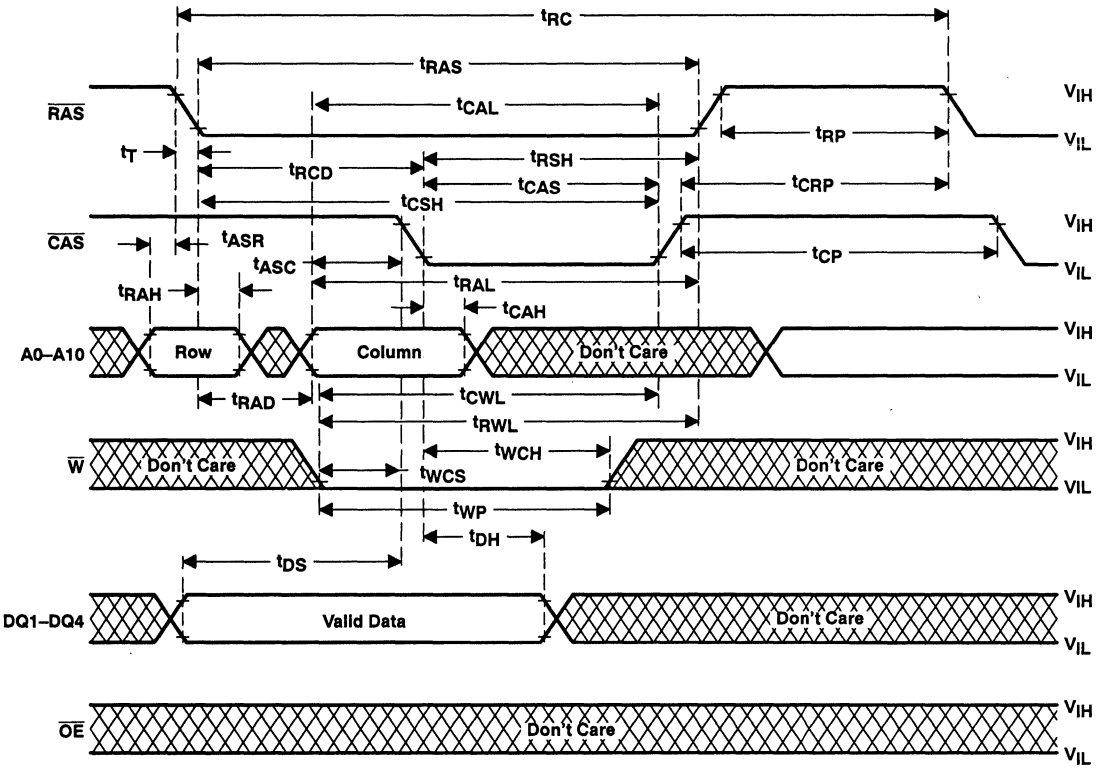


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

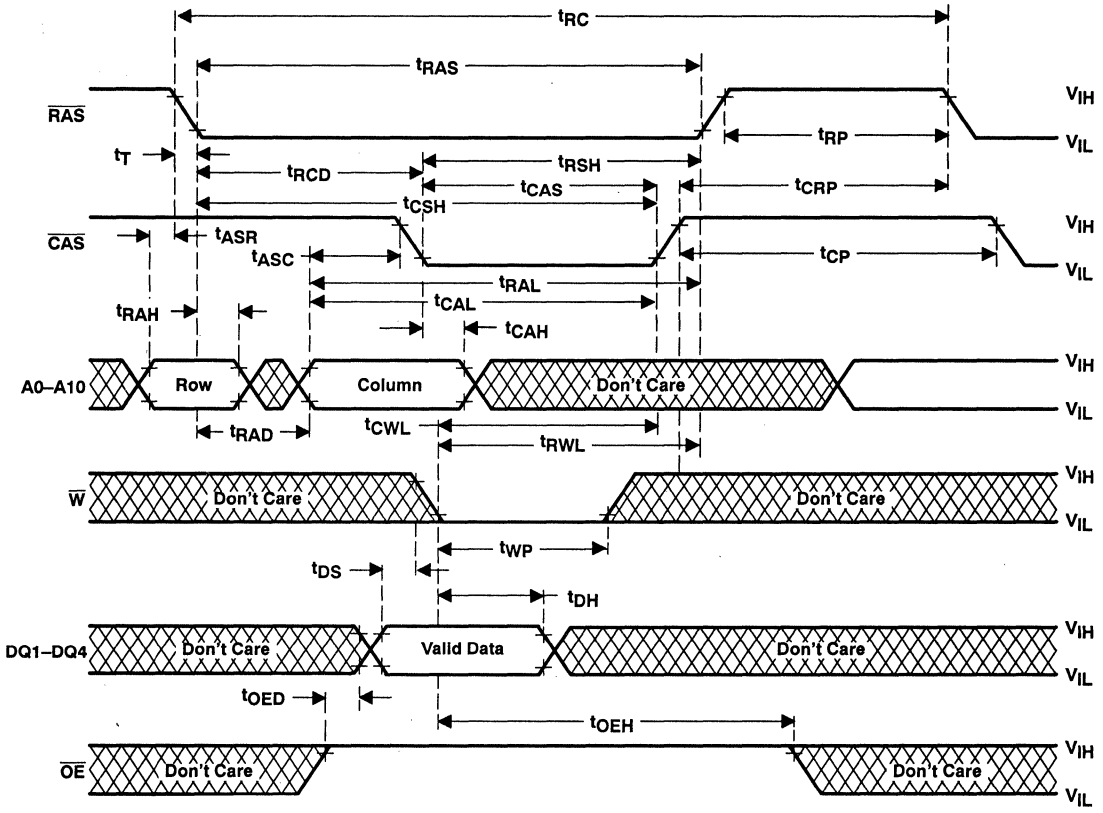
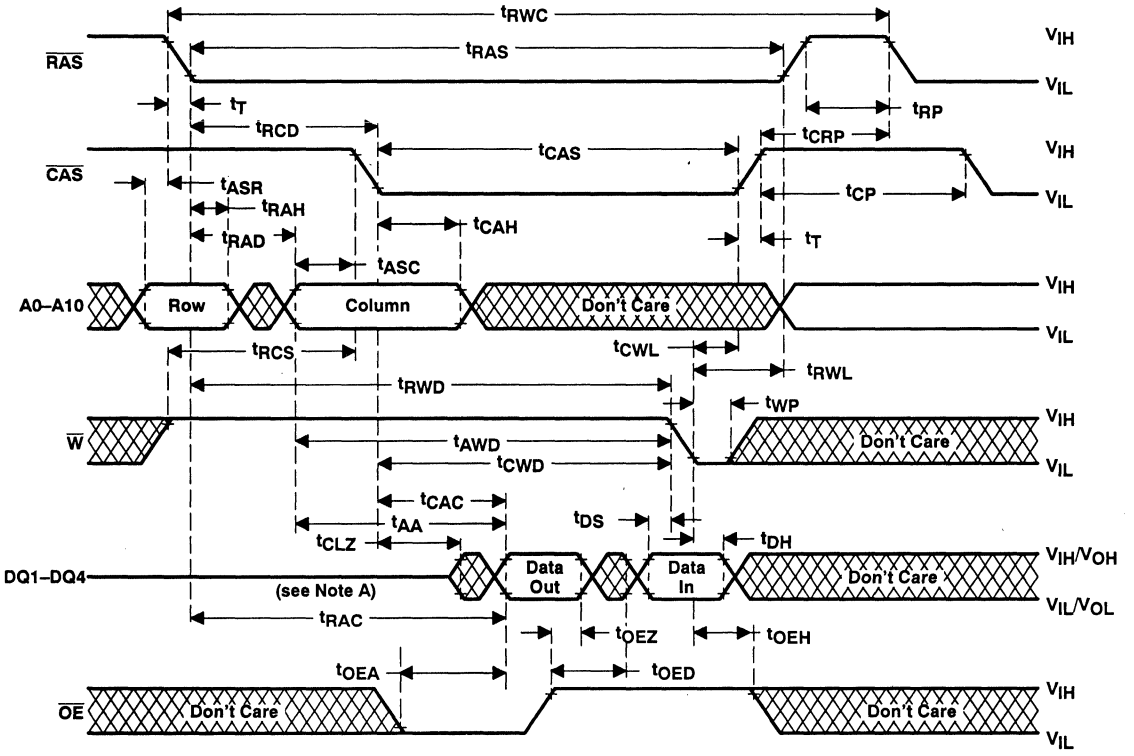


Figure 4. Write Cycle Timing

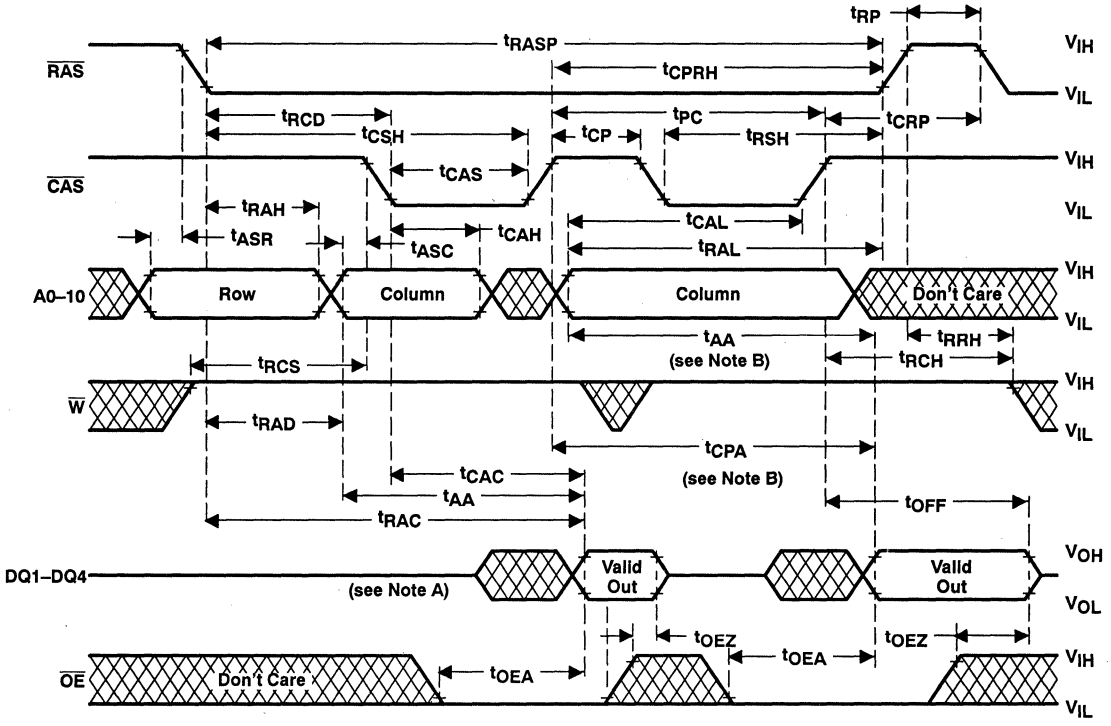
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Write Cycle Timing

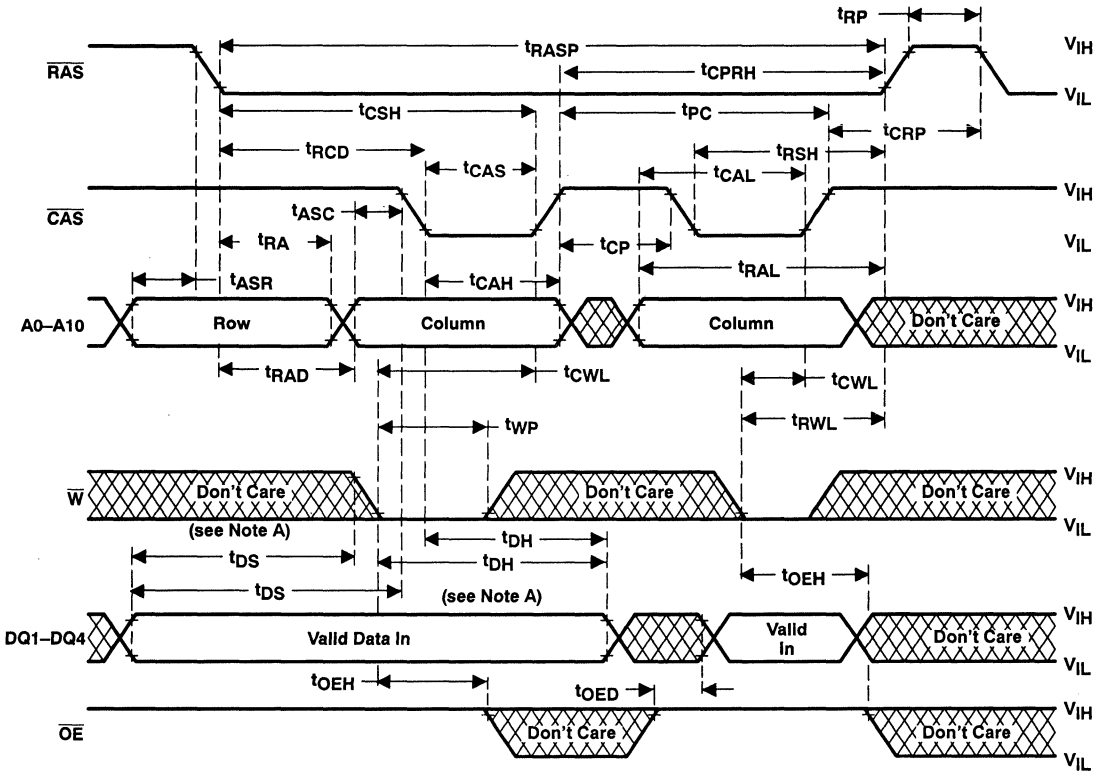
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

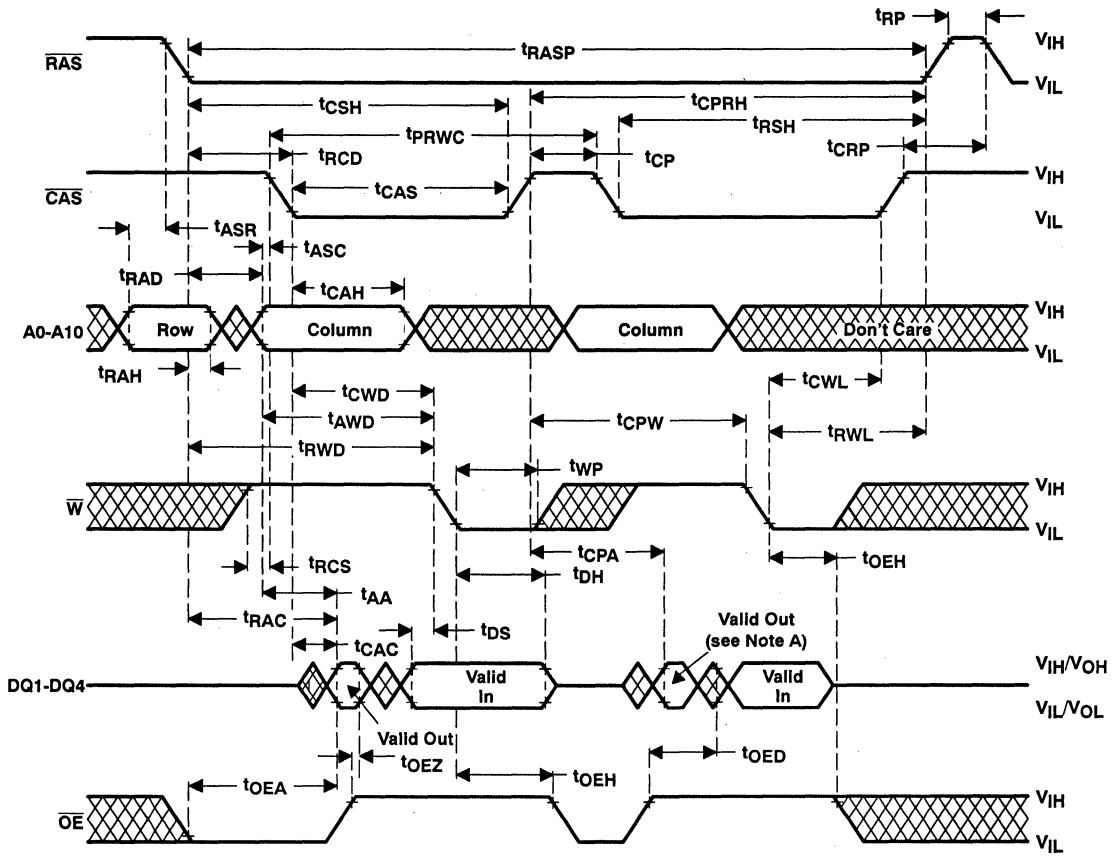
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

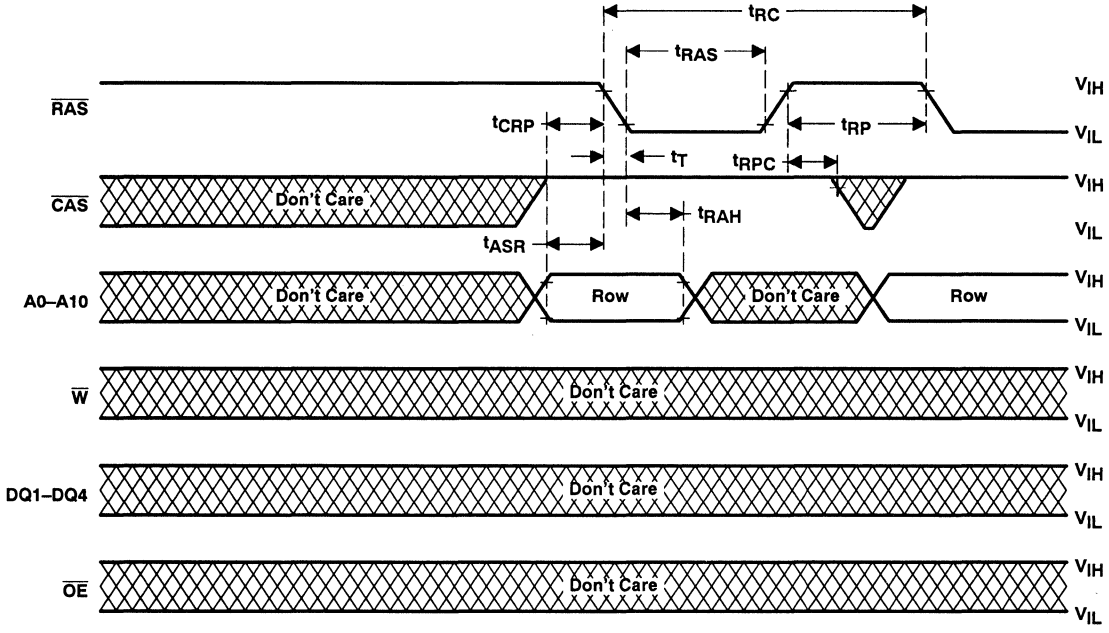


Figure 9. $\overline{RAS}$-Only Refresh Timing

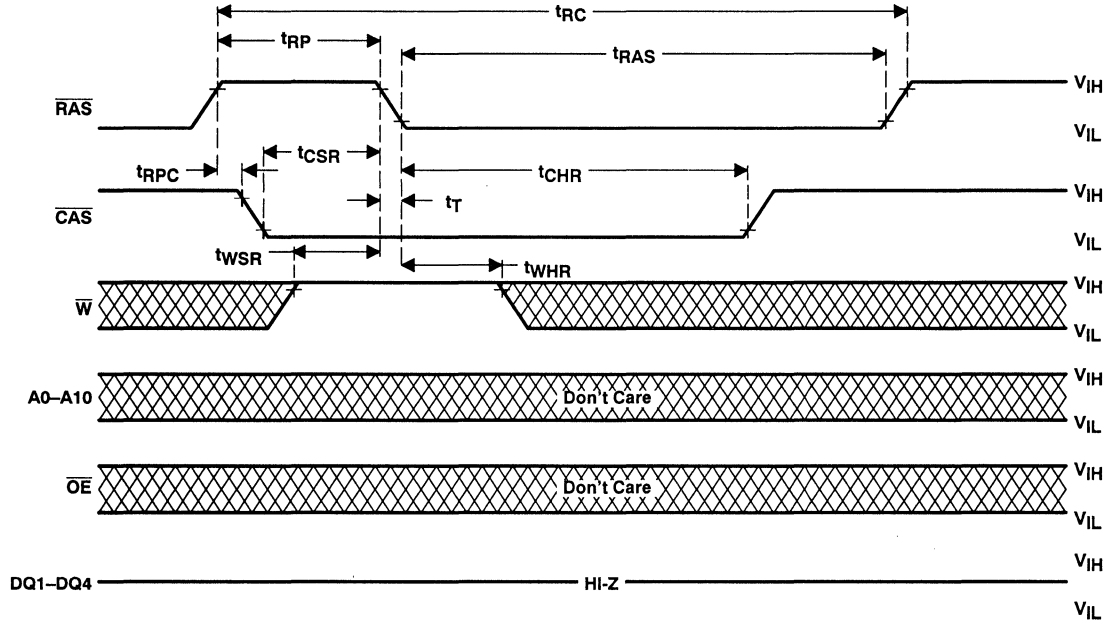


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

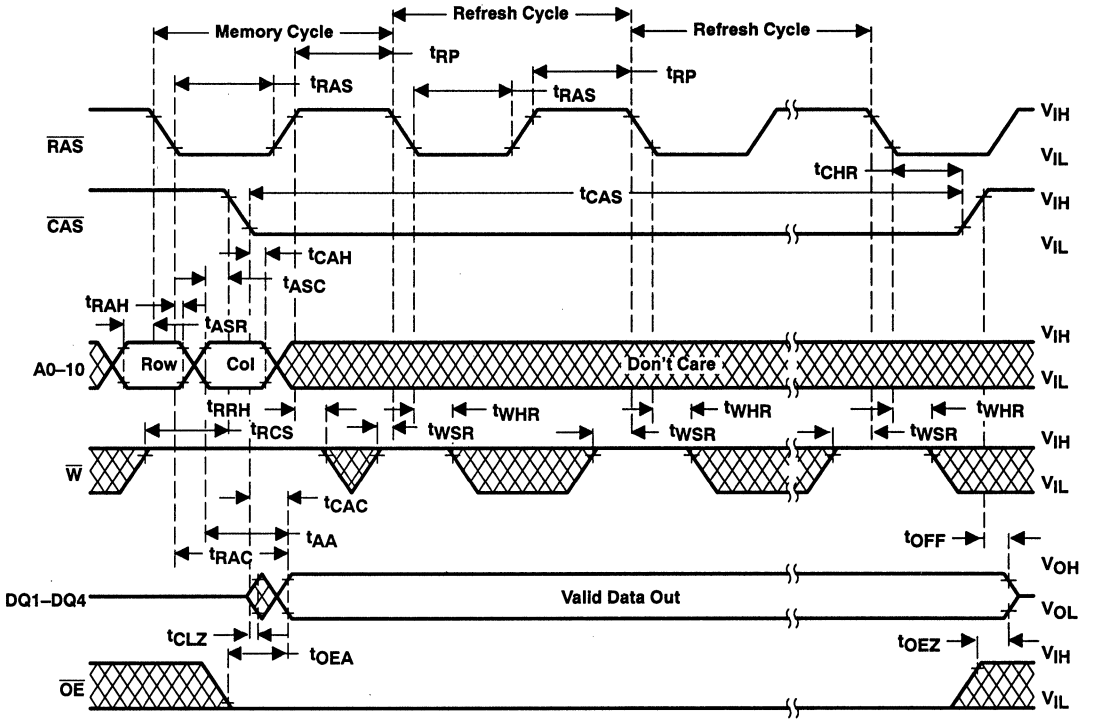
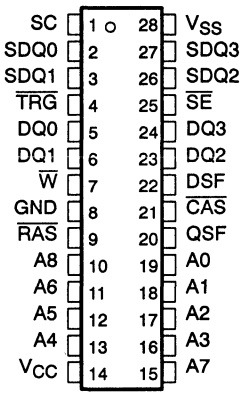


Figure 11. Hidden Refresh Cycle (Read)

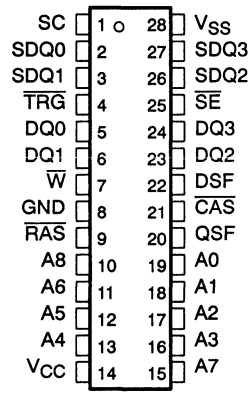
SGMS037B–JANUARY 1991–REVISED FEBRUARY 1993

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **Processed to MIL-STD-833, Class B**
- **DRAM: 262 144 Words × 4 Bits**
  SAM: 512 Words × 4 Bits
- **Dual Port Accessibility — Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register**
- **Write Per Bit Feature for Selective Write to Each RAM I/O**
- **Enhanced Page Mode Operation for Faster Access**
- **$\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes**
- **RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design**
- **Long Refresh Period . . . Every 8 ms (Max)**
- **Up to 33 MHz Uninterrupted Serial Data Streams**
- **3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams**
- **512 Selectable Serial Register Starting Locations**
- **Texas Instruments EPIC™ CMOS Process**
- **Packaging Options**
  - **28-pin Ceramic Side Brazed DIP (JD suffix)**
  - **28-pin Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)**
- **Split Serial Data Register for Simplified Realtime Register Reload**

JD PACKAGE
(TOP VIEW)



HJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0–DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0–SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
QSF	Split Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: not connected internally to V_{SS})

- **Performance Ranges:**

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$	V_{CC} TOLERANCE
'44C250-10	100 ns	25 ns	30 ns	20 ns	±10%
'44C250-12	120 ns	30 ns	35 ns	25 ns	±10%

description

The SMJ44C250 multiport video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each interfaced to a serial data register, or serial access memory (SAM), organized as 512 words of 4 bits each. The SMJ44C250 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer

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operations, the SMJ44C250 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SMJ44C250 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, a write mask register provides a persistent write-per-bit without repeated mask loading.

On the serial register, or SAM port, the SMJ44C250 offers a split-register transfer read (DRAM to SAM) option, which enables realtime register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

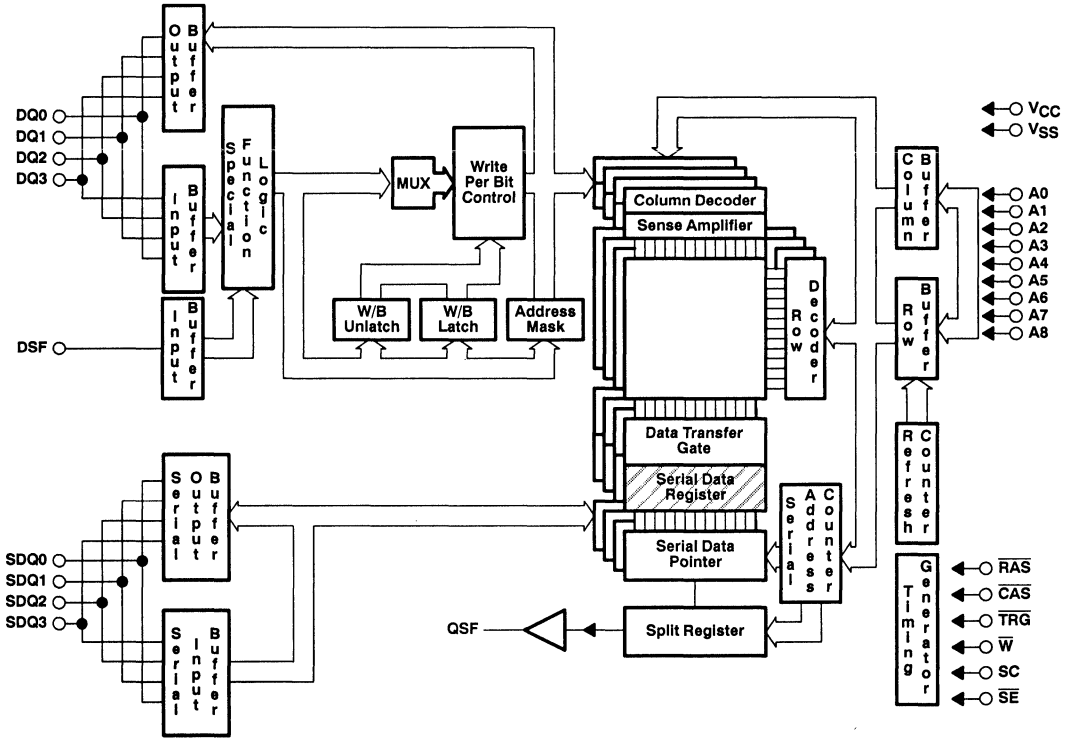
The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During a split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate open-drain output, designated QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The SMJ44C250 is offered both in a 28-pin 400-mil dual-in-line ceramic sidebrazed package (JD suffix) for through-hole row insertion, and in a 28-pin ceramic small outline J-leaded chip carrier package (HJ suffix) for surface-mount applications. The L suffix device is tested for operation from 0°C to 70°C. The M suffix device is tested for operation from – 55°C to 125°C.

The SMJ44C250 and other SMJ44C25x multiport video RAMs are supported by a broad line of video/graphic processors from Texas Instruments, including the SMJ34010 and the SMJ34020 graphics processors.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
DSF	Persistent Write-per-bit Enable Write-per-bit Mask Load Enable	Split Register Enable Alternate Write Transfer Enable	
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write-per-Bit Select	Transfer Write Enable	
QSF			Split Register Active Status
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND	System Ground (Important: not connected internally to V_{SS})		

operation

random access operation

Refer to Table 1, Functional Table (page 7), for random access and transfer operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a "T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See *transfer operation* for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0–A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and transfer functions of the SMJ44C250. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

The special function select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves three functions. First, during write cycles DSF invokes persistent write-per-bit operation. If $\overline{TRG}$ is high, $\overline{W}$ is low, and DSF is low on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF is high, the mask will not be reloaded but will retain the data from the last mask reload cycle.

Second, DSF is used to change the internally stored write-per-bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write-per-bit cycles. This feature allows systems with a common address and data bus to use the write-per-bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, the DSF pin is used to invoke the split-register transfer and serial access operation, described in the sections "transfer operation" and "serial operation".

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write-per-bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation. Two modes of write-per-bit operation are supported.

Case 1. If DSF is low on the falling edge of RAS, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF is high on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write-per-bit mask reload. This mode of operation is known as persistent write-per-bit, since the write-per-bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0–DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed in by $\overline{W}$ with data setup and hold times referenced to this signal.

The 3-state output buffers provide direct TTL compatibility (no pullup resistors required) with a fanout of two Series 74/54 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory-to-register or register-to-memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C250 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The SMJ44C250 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write-per-bit operations, the DQ pins are used to load the write-per-bit mask register described above under the $\overline{W}$ pin description.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND (Pin 8)

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Functional Table

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0–DQ3		FUNCTION
	CAS	TRG	W¶	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	X	X	CAS-before-RAS Refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate Transfer Write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial Write-Mode Enable (Pseudo-Transfer Write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory to Register Transfer (Transfer Read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split Register Transfer Read (Must Reload Tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and Use Write Mask, Write Data to DRAM
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent Write-Per-Bit, Write Data to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal Dram Read/Write (Nonmasked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load Write Mask

† R = Random access operation; T = Transfer operation.
‡ DQ0–DQ3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
¶ In persistent write-per-bit function, W must be high during the refresh cycles
Addr Mask = 1; write to address location enabled
Write Mask = 1; write to I/O enabled.

random port to serial port interface

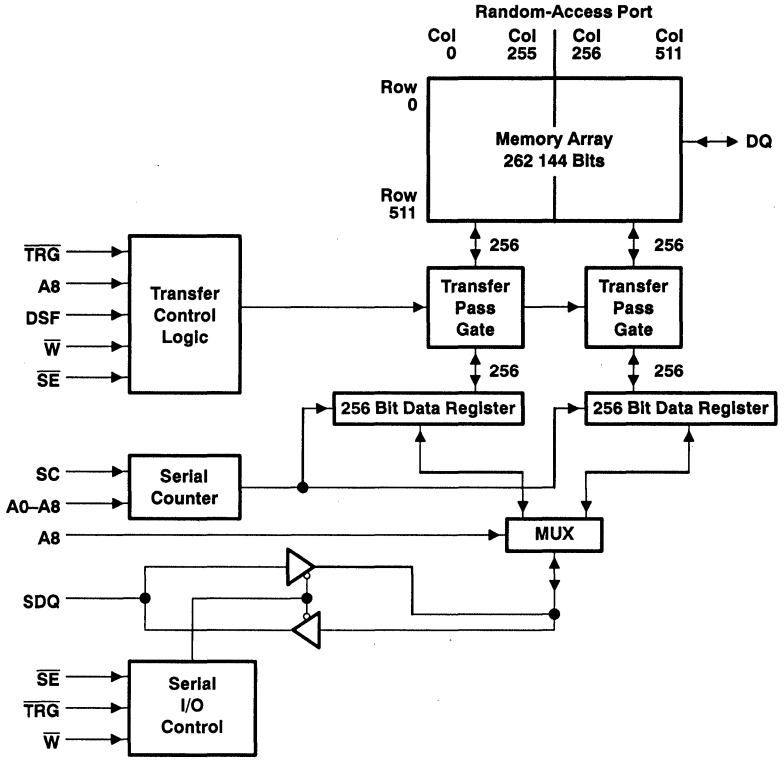


Figure 1. Block Diagram Showing One Random and One Serial I/O Interface

random-address space to serial-address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

split-register mode random-address to serial address-space mapping

In split-register transfer operations, the serial data register is split into halves, the low half containing bits 0–255 and the high half containing bits 256–511. When a split-register transfer cycle is performed, the tap address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit (A8) determines which register half will be reloaded from the memory array. The eight remaining column address bits (A0–A7) are used to select the SAM starting location for the register half selected by A8.

To insure proper operation when using the split-register read transfer feature, a non-split-register transfer must precede any split-register sequence. The serial start address must be supplied for every split-register transfer. (See Split Register Operating Sequence on page 36.)

transfer operations

As illustrated in Table 1, the SMJ44C250 supports five basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM to SAM)
5. Split-Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

NOTES: A. All transfer write operations will switch the SDQ pins into the input (write) mode. Before data can be clocked into the serial port via the SDQ pins and SC serial clock, it is necessary to switch the SDQ pins into input mode via a previous transfer write operation.
B. *Pseudo Transfer Write Mode* has the same meaning as the term "Write Mode Control Cycle" as used in some VRAM data sheets. Both modes, or control cycles, serve to switch the direction of the SDQs without an actual data transfer taking place.
C. All transfer read operations will switch the SDQ pins into the output (read) operation.
D. All transfer read operations and the pseudo transfer write operation perform a memory refresh on the selected row.

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. The SDQs are put into input mode by use of a transfer write cycle. This allows serial data to be input into the SAM. An alternative way to perform the transfer write cycle is by holding DSF high on the falling edge of $\overline{RAS}$. In this way, the state of $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0–A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

In the split-register transfer mode, the most significant column address bit (A8) selects which half of the register will be loaded from the memory array. The remaining eight addresses (A0–A7) determine the register starting location for the register to be loaded.

special function input (DSF)

In the read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split-register mode transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of the most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split-register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

In the write transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without permitting a pseudo write transfer with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The SMJ44C250 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0–SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode, and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The serial enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 2). If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls and DSF is low, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

QSF active status output

QSF is an open-drain output pin. During the split register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

QSF changes state upon crossing the boundary between the two register halves. When the SAM is not operating in split-register mode, the QSF output remains in the high-impedance state.

QSF is designed as an open drain output to allow OR-type of QSF outputs from several chips. Thus, an external pullup resistor is required for the zero-to-one transition on QSF, and the output rise time is determined by the load-capacitance and the value of the pullup resistor. The specification for QSF switching time assumes a pullup resistor of 820 Ω and a load capacitance of 30 pF illustrated as follows.

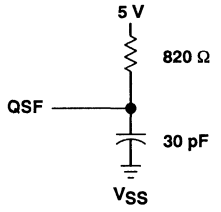


Figure 2. QSF Load Circuit

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
L	L	L	X	Register to memory (write) transfer, serial write mode enable
L	L	X	H	Alternate register to memory transfer
L	L	H	L	Serial write mode enable (pseudo write transfer)
L	H	X	L	Memory to register (read) transfer
L	H	X	H	Split-register read transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Alternate register to memory	H	Input Disabled
Serial write mode enable†	L	Input Enabled
Serial write mode enable†	H	Input Disabled
Memory to register	L	Output Enabled
Memory to register	H	Hi-Z

† Pseudo transfer write.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle, and two SC cycles.

absolute maximum ratings over operating temperature (unless otherwise noted)†

Input voltage on any pin except DQ and SDQ (see Note 1) ..... −1 V to 7 V
Input voltage on DQ and SDQ (see Note 1) ..... −1 V to V_{CC} + 1
Supply voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range:
SMJ44C250, L suffix ..... 0°C to70°C
SMJ44C250, M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.9		V_{CC} + 1	V
V_{IL}	Low-level input voltage (see Note 2)		−1		0.6	V
T_A	Operating free-air temperature	L suffix	0			°C
		M suffix	−55			
T_C	Operating case temperature	L suffix			70	°C
		M suffix			125	

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = – 5 mA	2.4		V
V_{OL}	Low level output voltage (see Note 4)	I_{OL} = 4.2 mA		0.4	V
I_I	Input leakage current	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins open		±1.0	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10	µA

PARAMETER			SAM PORT	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
I_{CC1} I_{CC1A}	Operation current $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum	(see Note 5)	Standby		100		90	mA
			Active		110		100	
I_{CC2} I_{CC2A}	Standby current, All clocks = V_{CC} $t_{c(SC)}$ = Minimum		Standby		15		15	
			Active		35		35	
I_{CC3} I_{CC3A}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		100		90	
			Active		110		100	
I_{CC4} I_{CC4A}	Page mode current, $t_{c(P)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		65		60	
			Active		70		65	
I_{CC5} I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		90		80	
			Active		110		100	
I_{CC6} I_{CC6A}	Data transfer current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		100		90	
			Active		110		100	

NOTES: 3. $\overline{SE}$ is disabled for SDQ output leakage tests.

4. The SMJ44C250 1-megabit video RAM may exhibit simultaneous switching noise as described in Texas Instruments *Advanced CMOS Logic Designer's Handbook*. This phenomenon exhibits itself upon the DQ pins when the SDQ pins are switched and upon the SDQ pins when DQ pins are switched. This may cause the V_{OL} and V_{OH} to exceed the data book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.

5. I_{CC} (standby) vs I_{CCA} (active) denotes the following:
I_{CC} (standby) denotes that the SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
I_{CCA} (active) denotes that the SAM port is active and the DRAM port is active (except for I_{CC2}).
I_{CC} is measured with no load on DQ or SDQ pins.

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		8	pF
$C_{o(QSF)}$	Output capacitance, QSF		14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 7)

NO.	PARAMETER		TEST CONDITIONS	ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
					MIN	MAX	MIN	MAX	
1	$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30	ns
2	$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
3	$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MIN	t_{CAP}		55		65	ns
4	$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MIN	t_{RAC}		100		120	ns
5	$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
6	$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		30		35	ns
7	$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		25	ns
8	$t_{a(QSF)}$	Access time of QSF from SC low	C_L = 30 pF			60		60	ns
9	$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 80 pF	t_{OFF}	0	20	0	20	ns
10	$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 80 pF	t_{OEZ}	0	20	0	20	ns
11	$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	20	0	20	ns

NOTES: 7. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 3).
8. Disable times are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating temperature†

NO.	PARAMETER		ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
12	$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	190		220		ns
13	$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
14	$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
15	$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
16	$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	105		125		ns
17	$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
18	$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
19	$t_{c(SC)}$	Serial clock cycle time (see Note 10)	t_{SCC}	30		35		ns
20	$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	20		30		ns
21	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 11)	t_{CAS}	25	75 000	30	75 000	ns
22	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
23	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 12)	t_{RAS}	100	75 000	120	75 000	ns
24	$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
25	$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
26	$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
27	$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
28	$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
29	$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low		0		0		ns
30	$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
31	$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
32	$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low (write mask operation)	t_{MS}	0		0		ns
33	$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
34	$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low (see Note 13)	t_{ESR}	0		0		ns
35	$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low		0		0		ns
36	$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
37	$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
38	$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
39	$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
40	$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
41	$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
42	$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 5 ns.

10. When the odd tap is used (tap address can be 0–511, and odd taps are 1,3,5, etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.
11. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
12. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
13. Register to memory (write) transfer cycles only.

timing requirements over recommended ranges of supply voltage and operating temperature (continued)†

NO.	PARAMETER		ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
43	$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
44	$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low		20		20		ns
45	$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns
46	$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
47	$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low (see Note 13)	t_{REH}	15		15		ns
48	$t_{h(RWM)}$	$\overline{W}$ hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
49	$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
50	$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low		15		15		ns
51	$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 14)	t_{AR}	45		45		ns
52	$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
53	$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 14)	t_{DHR}	45		50		ns
54	$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
55	$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 15)	t_{RCH}	0		0		ns
56	$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 15)	t_{RRH}	10		10		ns
57	$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
58	$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 14)	t_{WCR}	50		55		ns
59	$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 20)	t_{WCR}	25		30		ns
60	$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
61	$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
62	$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
63	$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
64	$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
65	$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 16 and 17)	t_{CWD}	55		65		ns
66	$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)	t_{RCD}	25	75	25	90	ns
67	$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
68	$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 16)	t_{RWD}	130		155		ns
69	$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 16)	t_{AWD}	85		100		ns
70	$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 19)	t_{CHR}	25		25		ns
71	$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 19)	t_{CSR}	10		10		ns
72	$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 19)	t_{RPC}	10		10		ns
73	$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		30		ns
74	$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ (see Note 16)		25		30		ns
75	$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register to memory (write) transfer cycles only.
14. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. Read-modify-write operation only.
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. Maximum value specified only to assure $\overline{RAS}$ access time.
19. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
20. Output enable controlled write. Outputs remain in the high-impedance state for the entire cycle.

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)†

NO.	PARAMETER		ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
76	$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{RSD}	130		140		ns
77	$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	40		45		ns
78	$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 21 and 22)	t_{TSL}	15		20		ns
79	$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 21)	t_{TRD}	−10		−10		ns
80	$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ (see Notes 13 and 21)	t_{SRS}	10		20		ns
81	$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		20		20		ns
82	$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 13)	t_{SRD}	25		30		ns
83	$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 24)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
84	$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 24)	t_{TSD}	35		40		ns
85	$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 25)	t_{SWS}	10		15		ns
86	$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		25		30		ns
87	$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles		20		25		ns
88	$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register to memory (write) transfer cycles only.
21. Memory to register (read) transfer cycles only.
22. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
23. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
24. Memory to register (read) and register to memory (write) transfer cycles only.
25. Serial data-in cycles only.
26. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

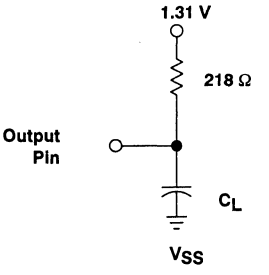


Figure 3. Load Circuit

PARAMETER MEASUREMENT INFORMATION

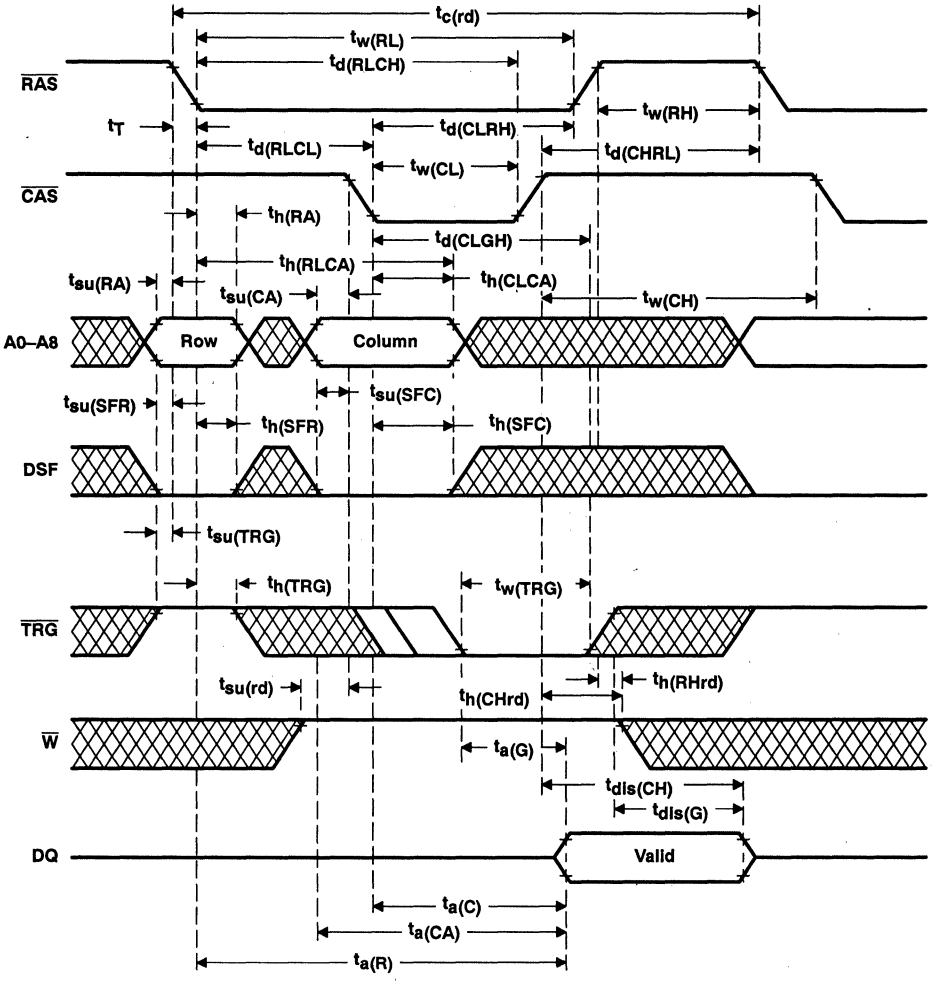
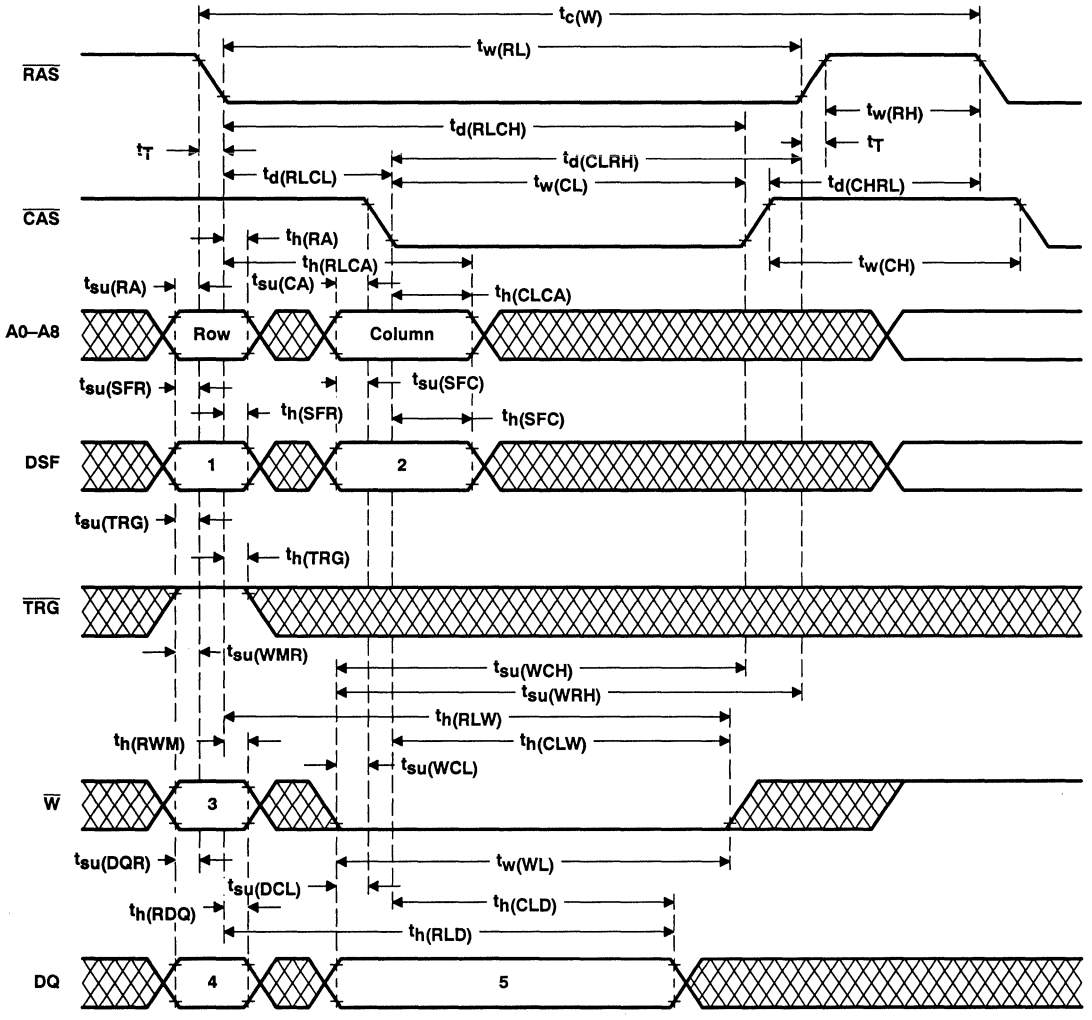


Figure 4. Read Cycle Timing

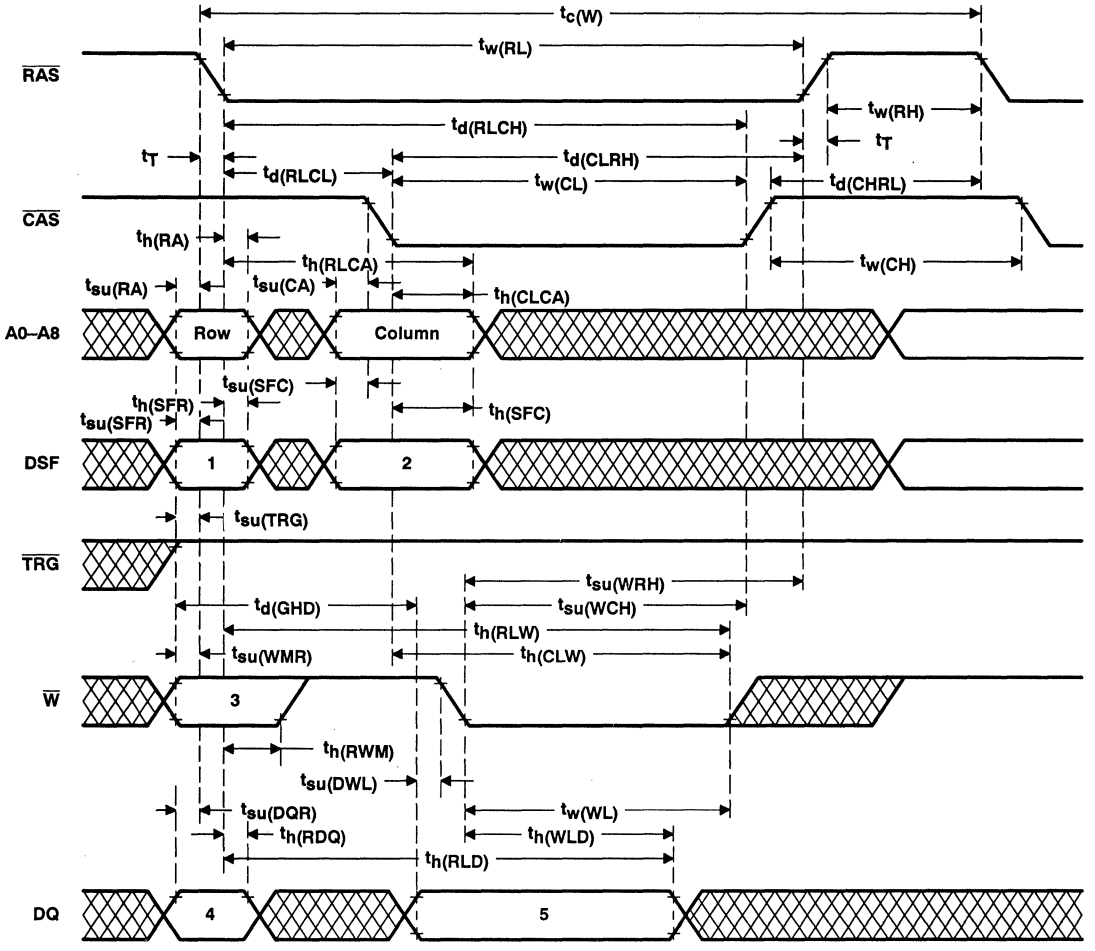
PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

Figure 5. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

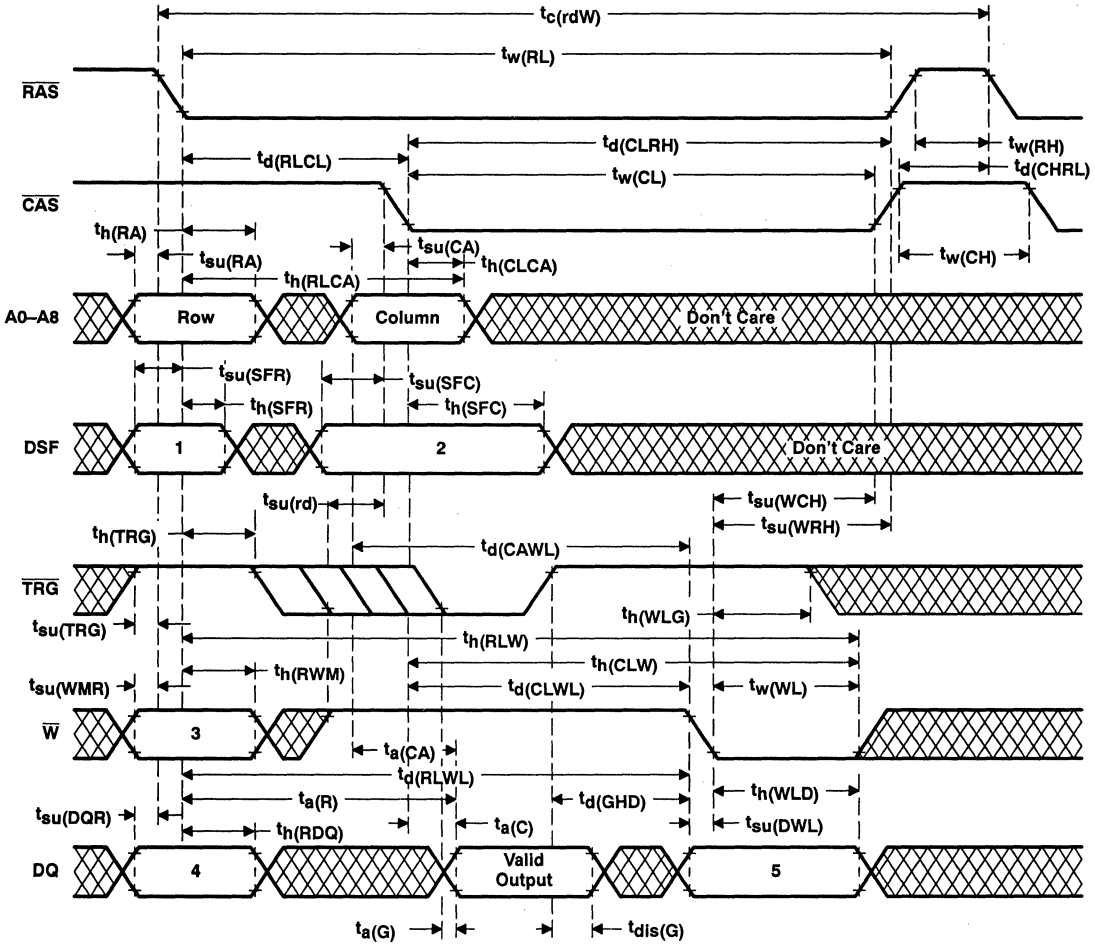
Figure 6. Delayed Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

write cycle state table

CYCLE	STATE				
	1	2	3	4	5
Write mask load/use write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't Care	Write Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

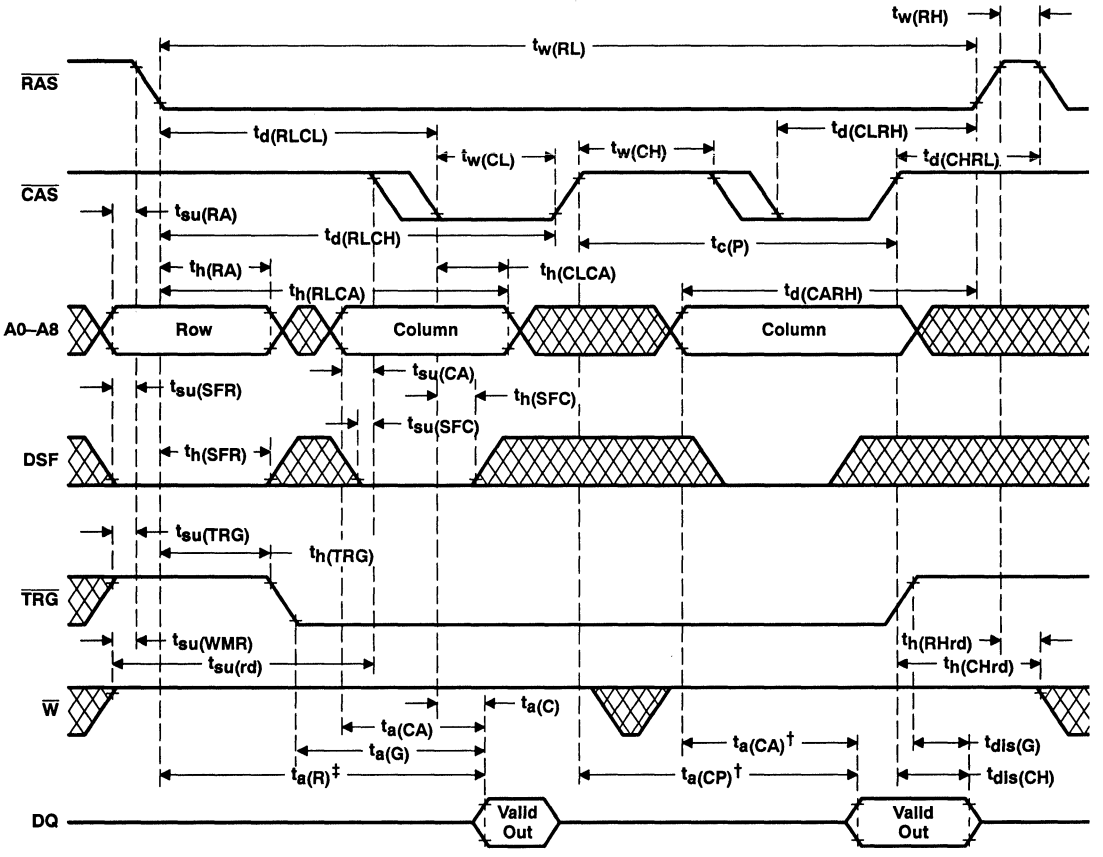
PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

Figure 7. Read-Write/Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



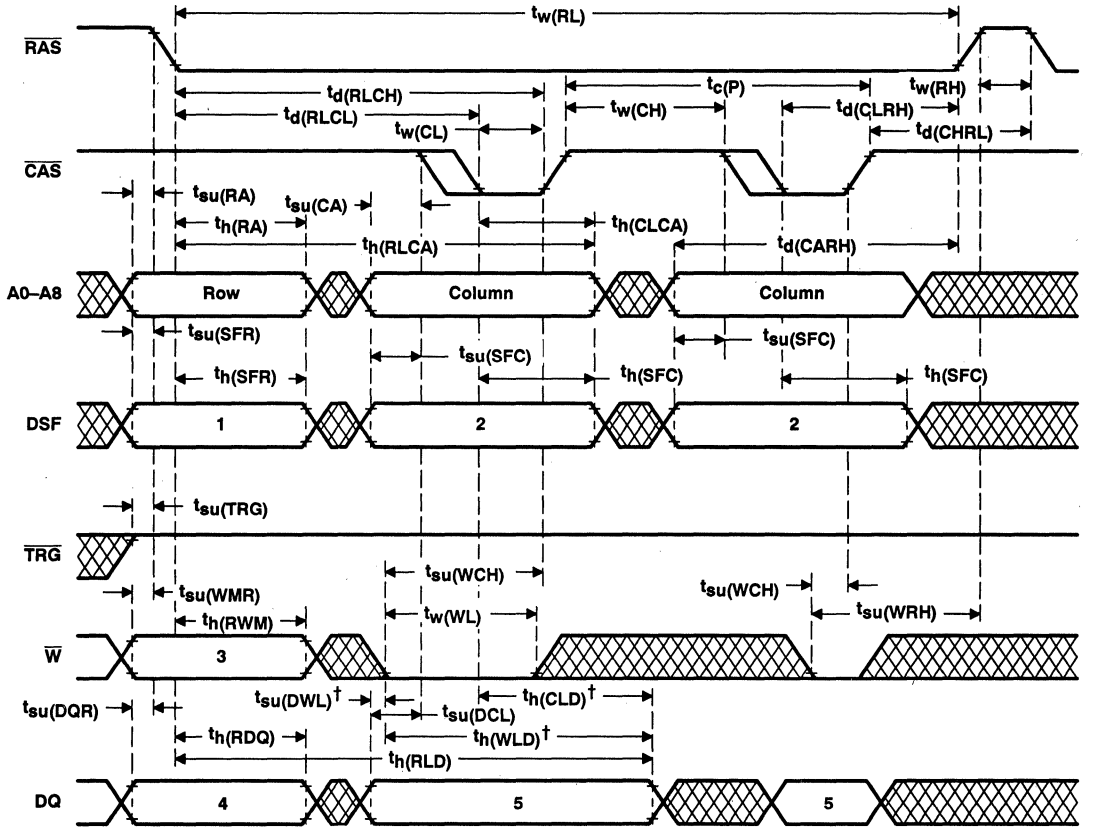
† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 8. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



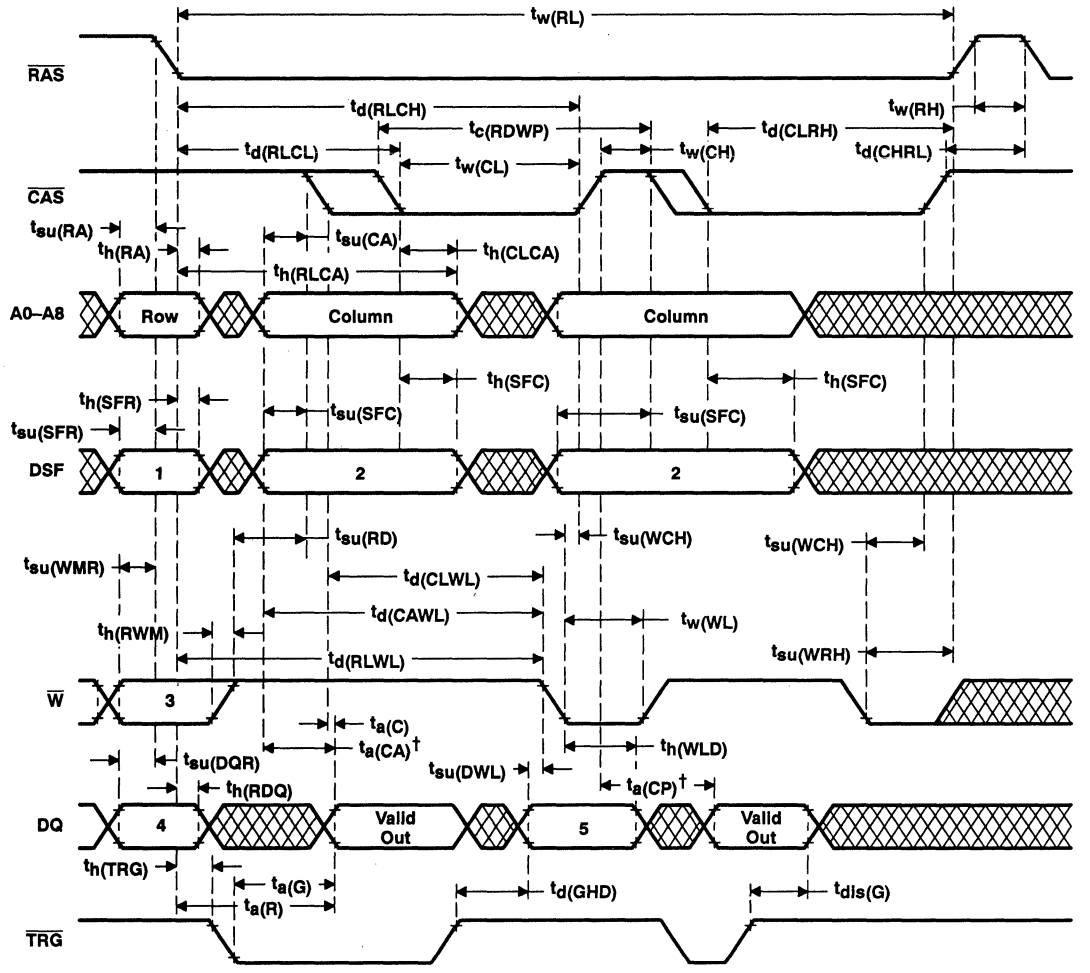
† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: A. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

B. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to assure page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 9. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

NOTES: A. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 10. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

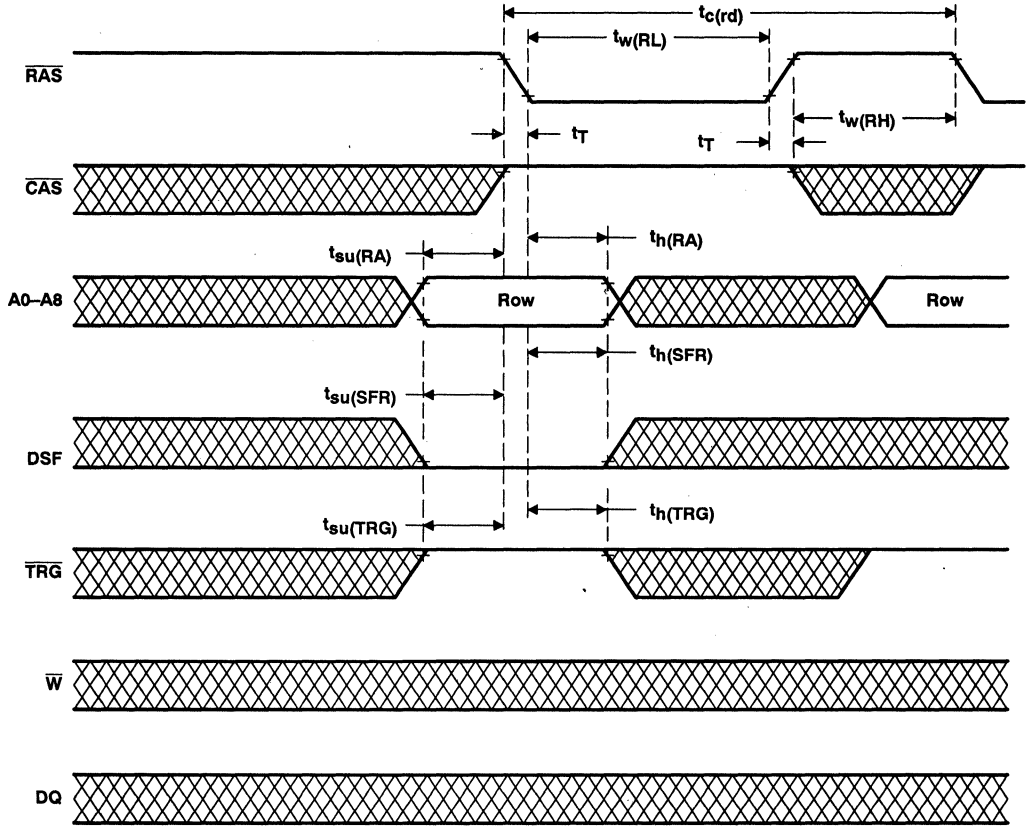


Figure 11. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

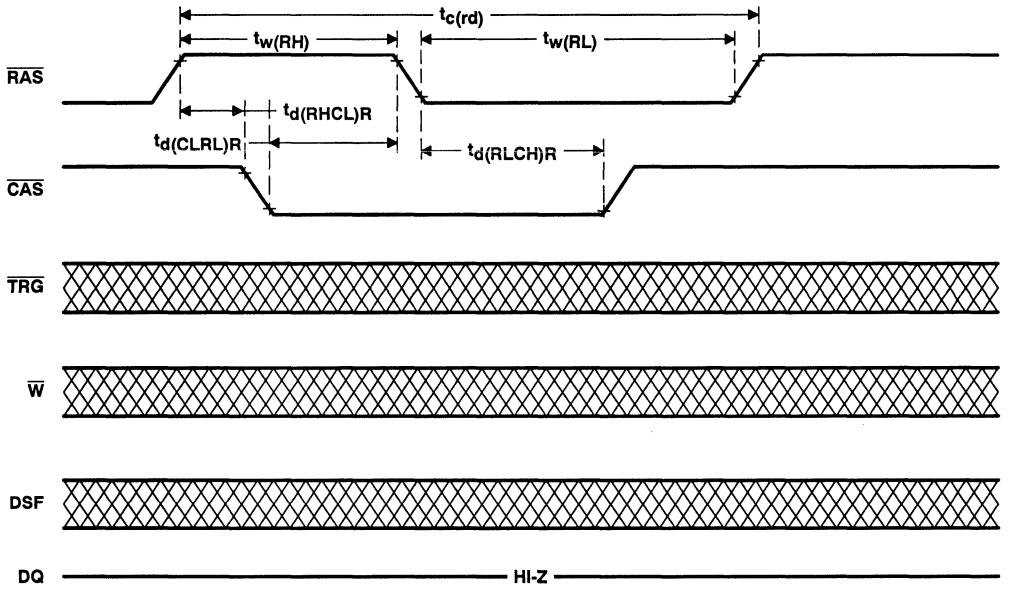


Figure 12. CAS-Before-RAS Refresh

PARAMETER MEASUREMENT INFORMATION

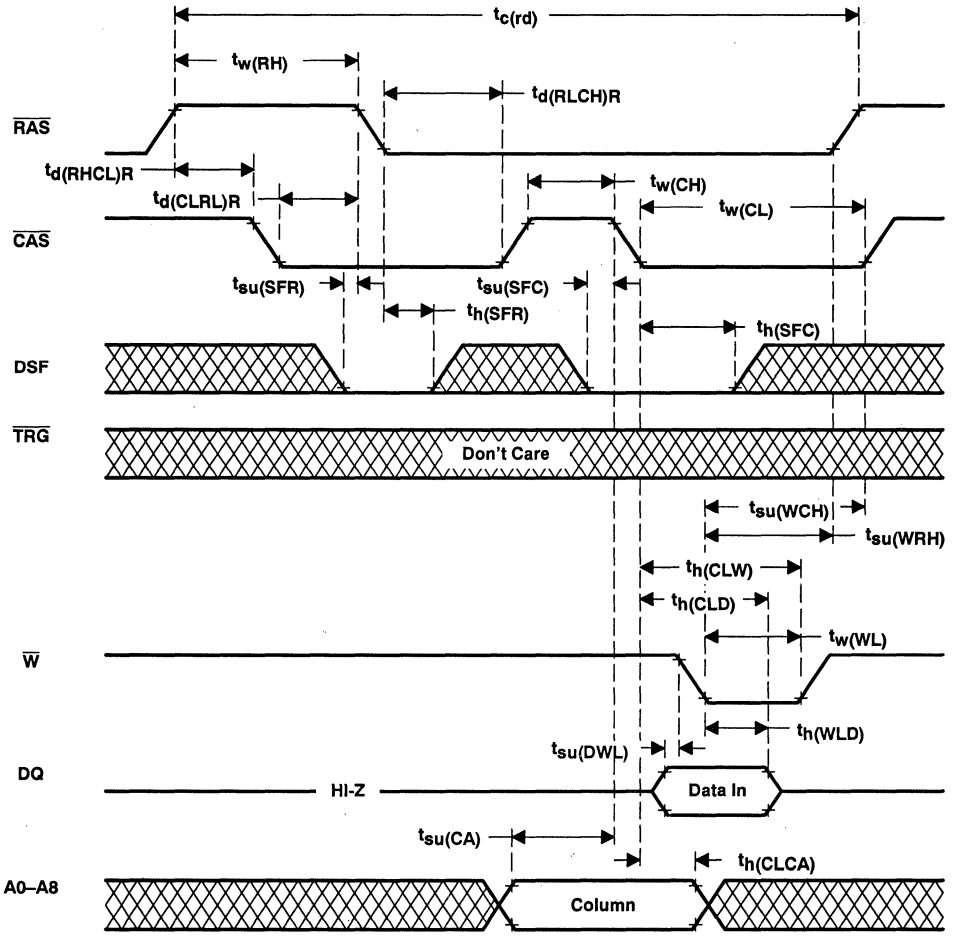


Figure 13. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Timing

PARAMETER MEASUREMENT INFORMATION

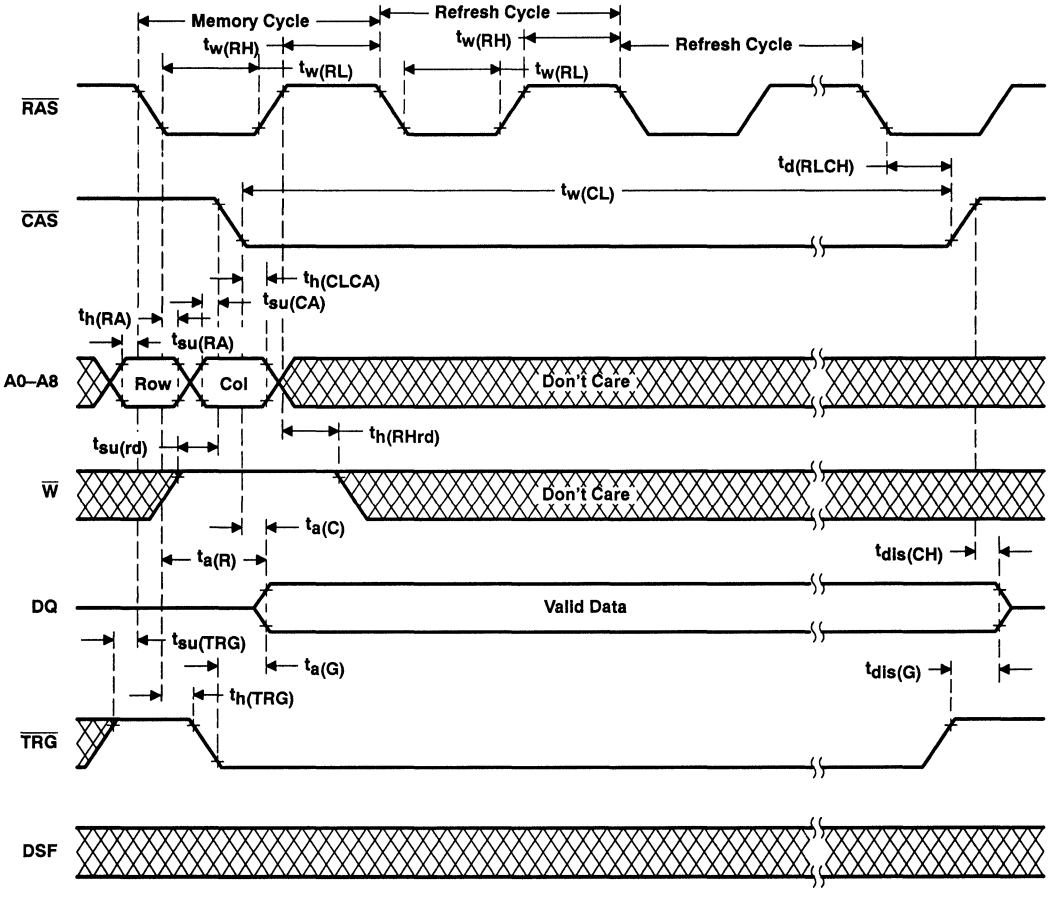
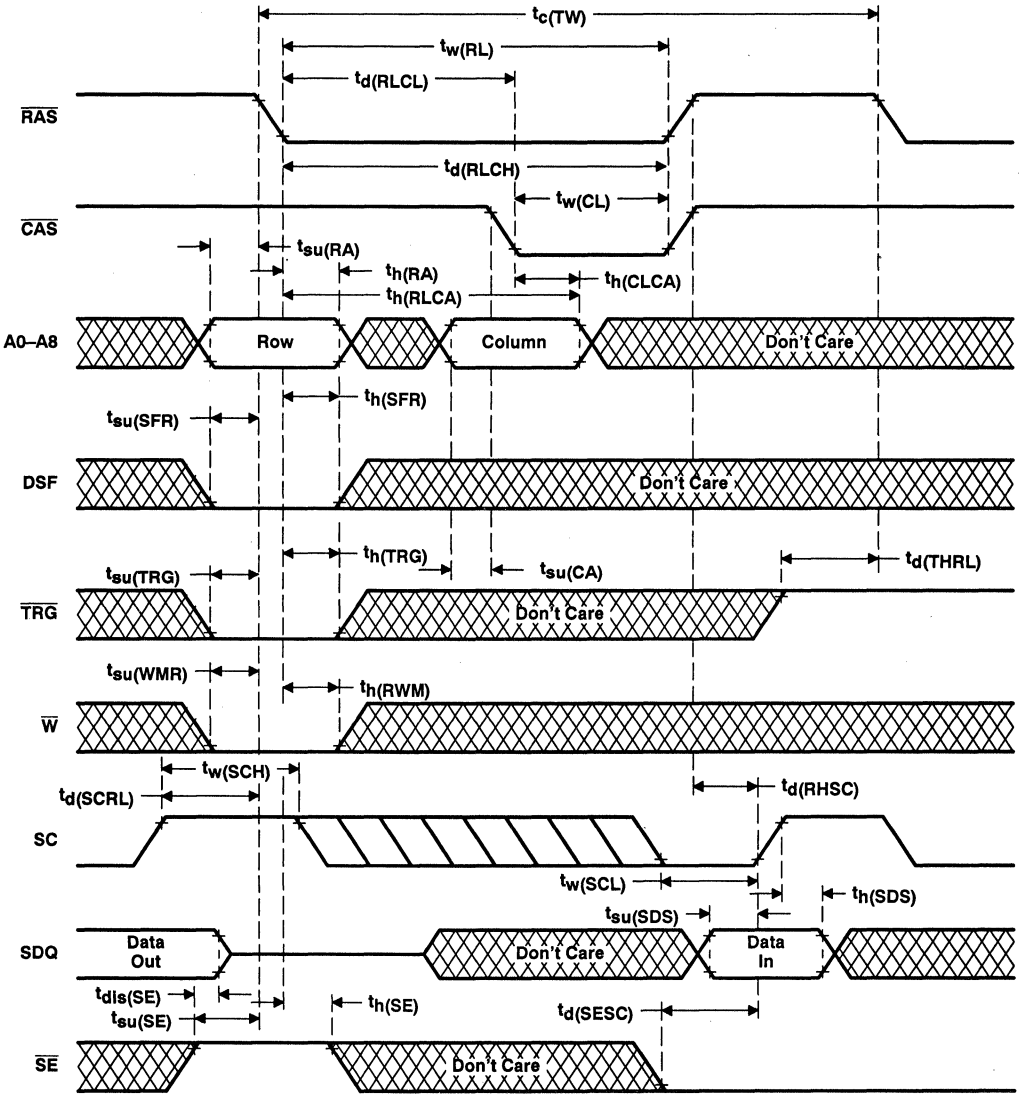


Figure 14. Hidden Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

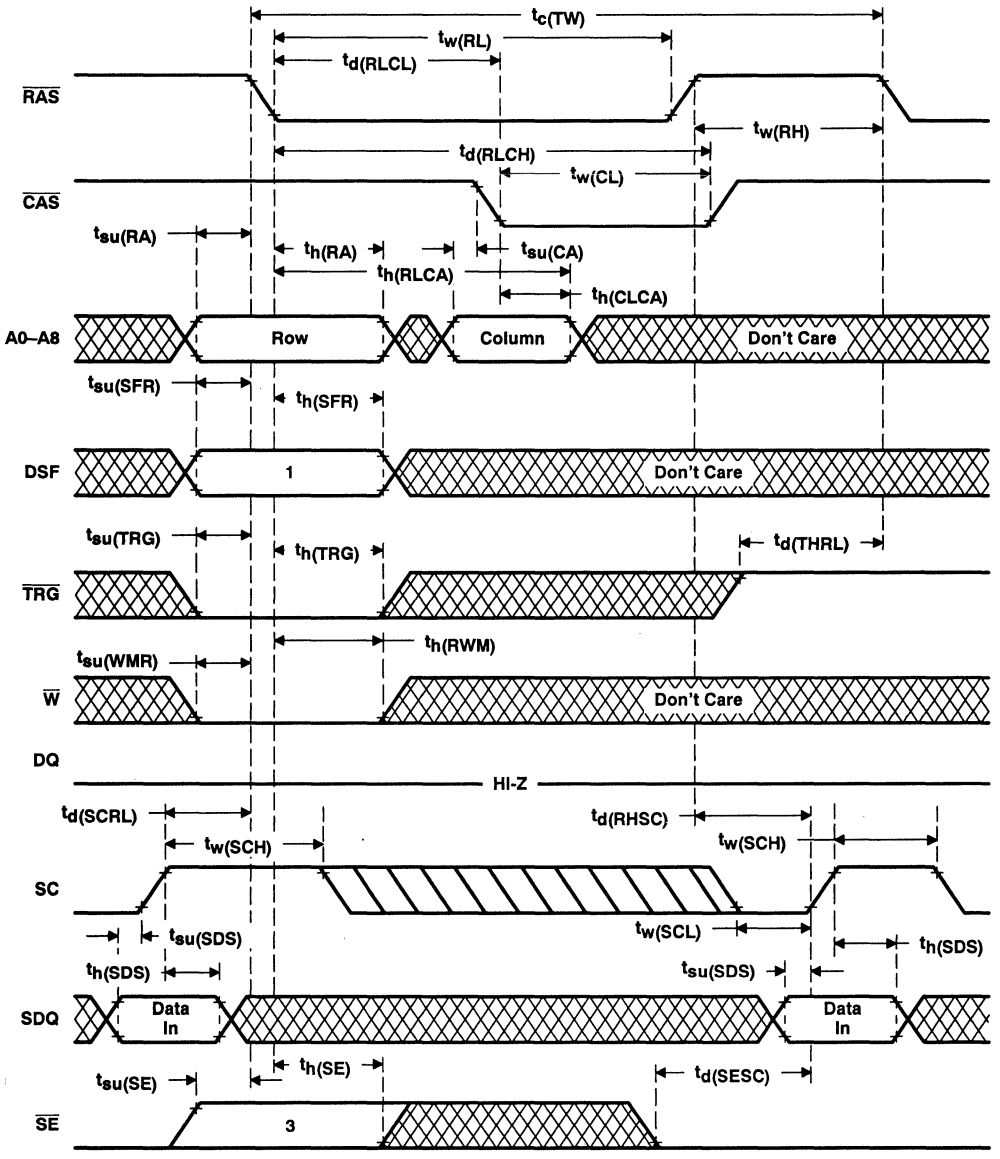
The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: A. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
B. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

Figure 15. Write-Mode Control Pseudo Write Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

B. See "Register Transfer Function Table" for logic state of "1" and "3".

C. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.

Figure 16. Data Register to Memory Timing, Serial Input Enabled

PARAMETER MEASUREMENT INFORMATION

register transfer function table

FUNCTION	$\overline{RAS}$ FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer	L	L	X	L
Register to memory transfer, alternate transfer write	L	L	H	X
Pseudo-transfer SDQ control, serial input enabled	L	L	L	H
Memory to register transfer	L	H	L	X
Split-register transfer	L	H	H	X

PARAMETER MEASUREMENT INFORMATION

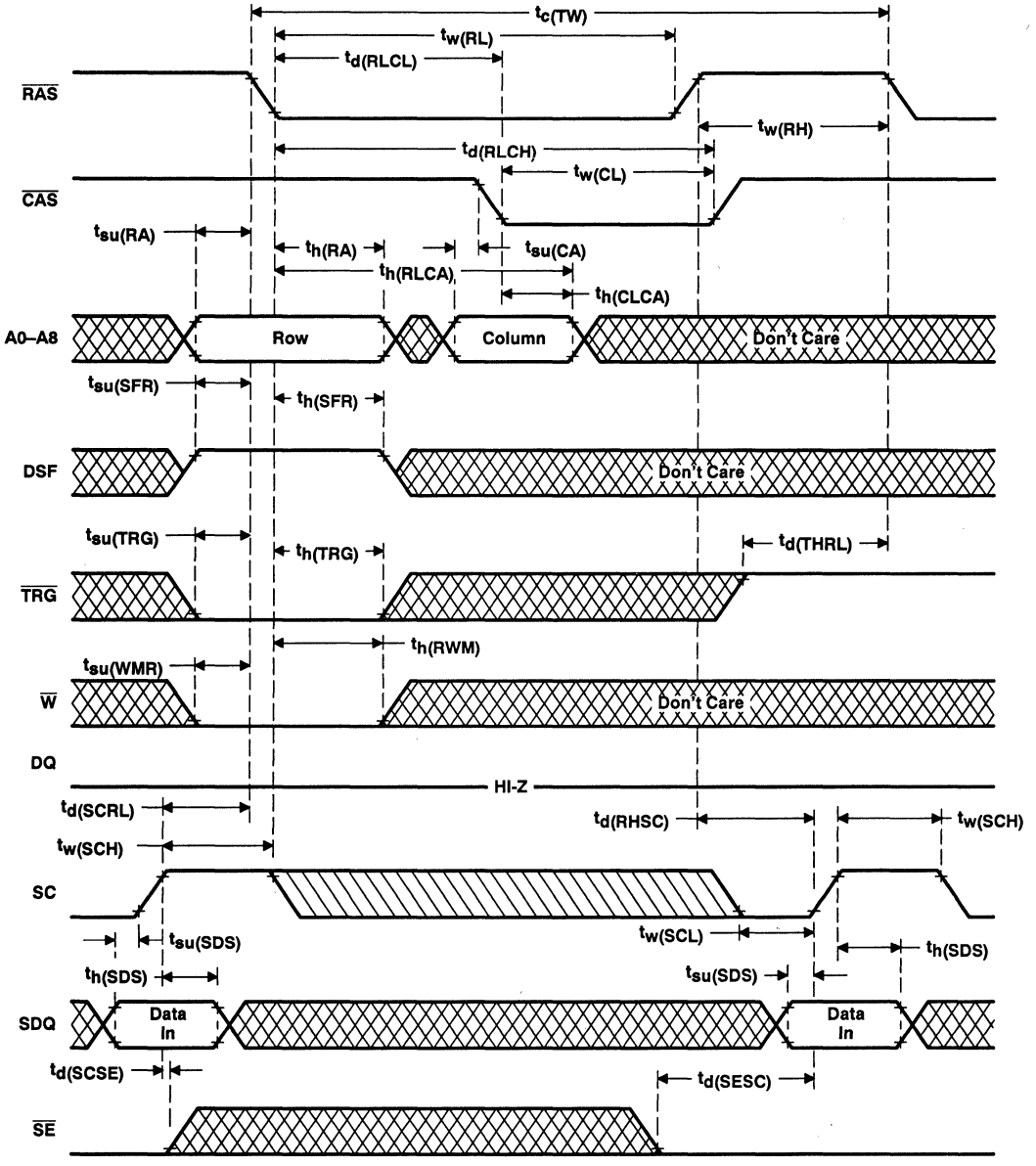
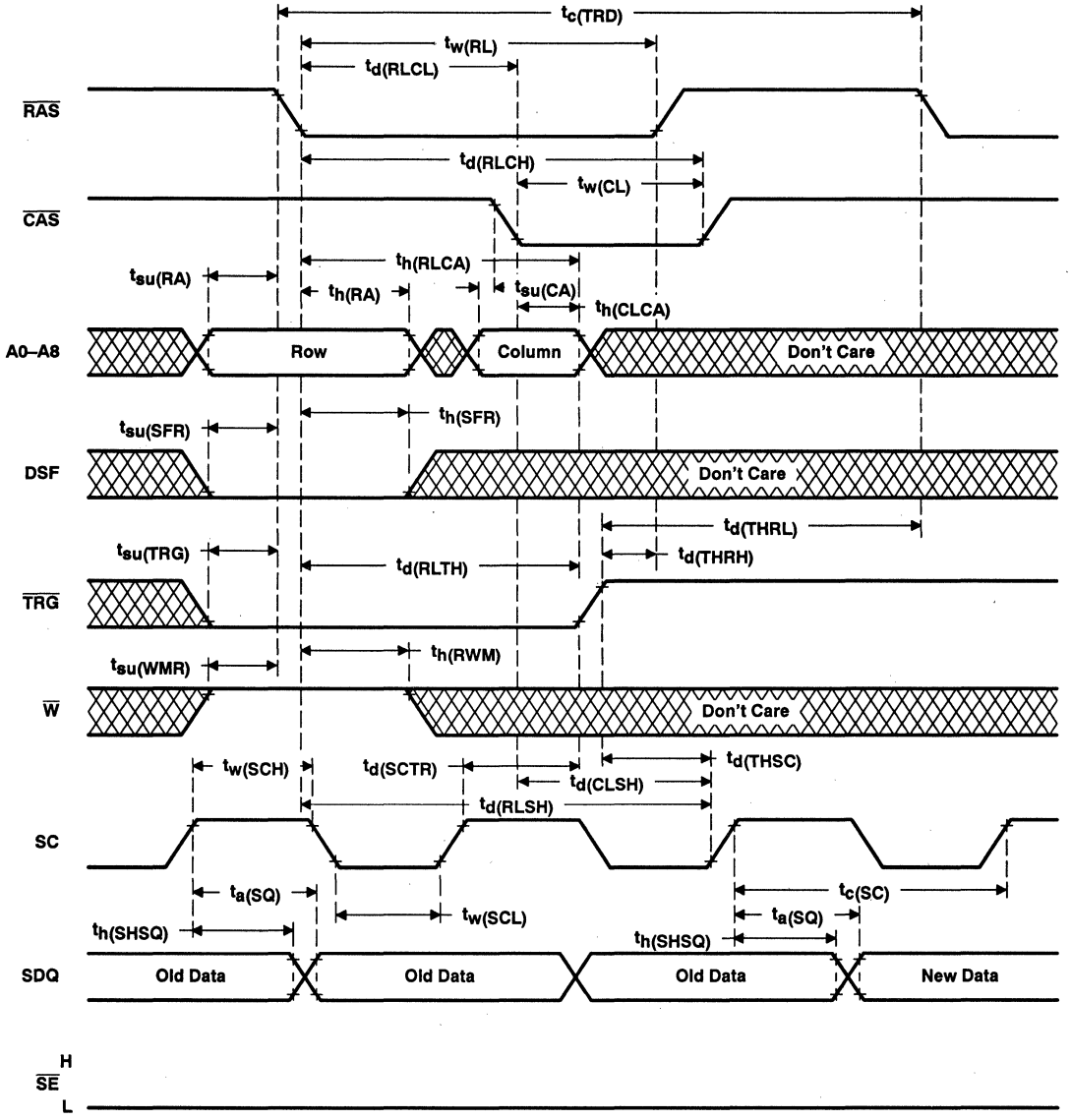


Figure 17. Alternate Data Register to Memory Timing

PARAMETER MEASUREMENT INFORMATION

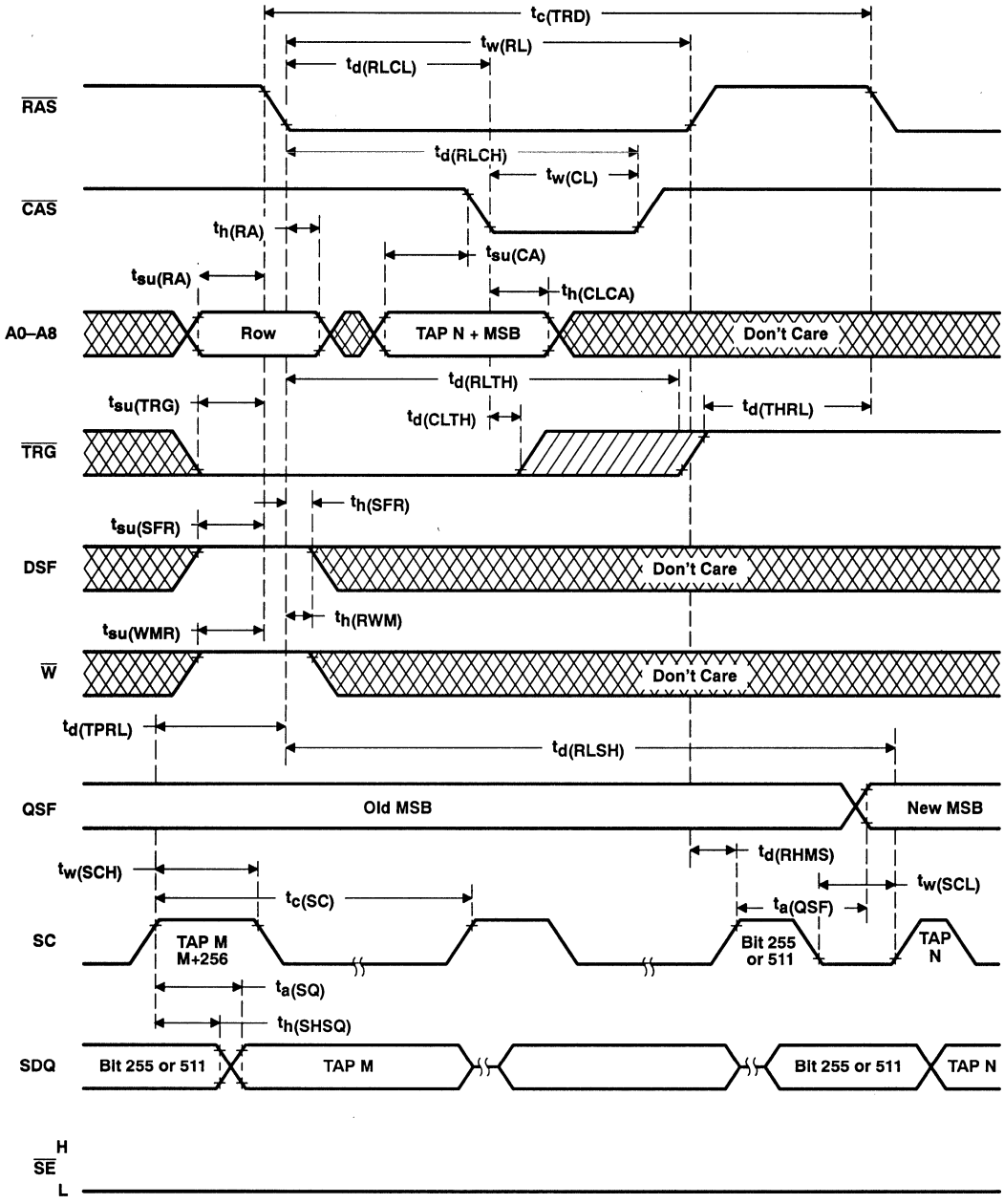


NOTES: A. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

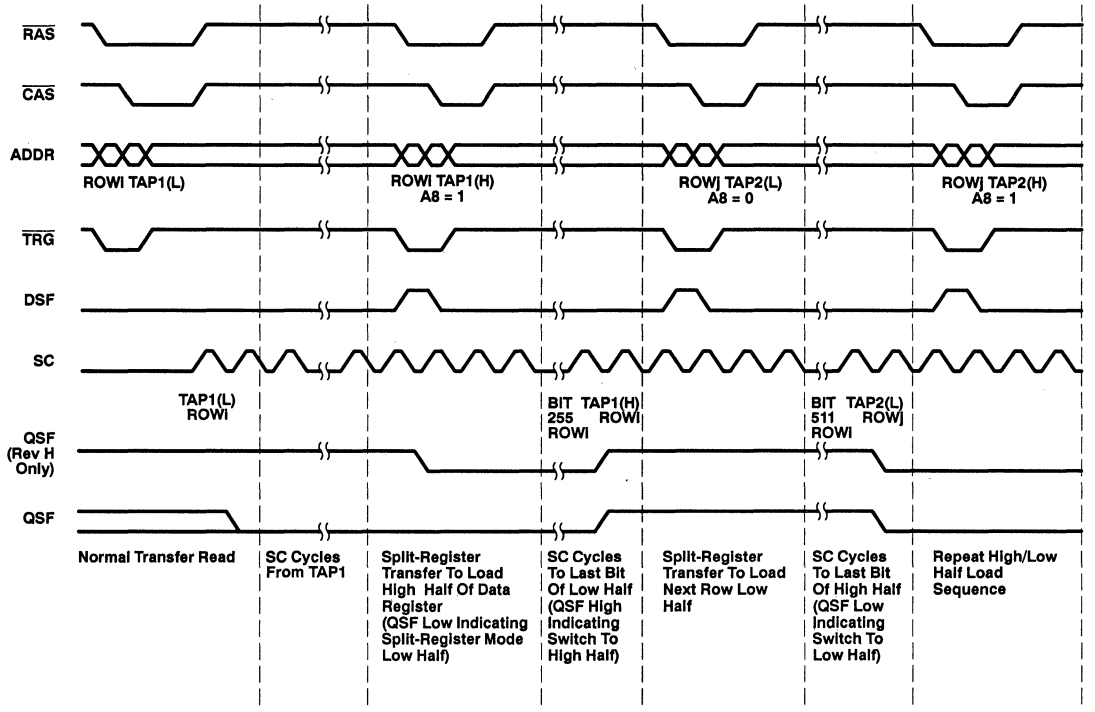
Figure 18. Memory to Data Register Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: There must be a minimum of two SC clocks cycle between any two split-register reload cycles, and a minimum of one SC clock cycle between a transfer read cycle and a split-register cycle.

Figure 19. Split-Register Mode Read Transfer Timing



NOTES: A. In the split-register mode, data can be transferred from different rows to the low and high halves of the data register.
B. When enabling or disabling the split-register mode, $t_{a(QSF)}$ is measured from $\overline{RAS}$ low in the transfer cycle.

Figure 20. Split-Register Operating Sequence

application notes

1. In order to achieve proper split-register operation, a normal read transfer followed by a minimum of one serial clock cycle should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. Serial access can then begin after the normal transfer cycle.
2. A split-register transfer into the inactive half is not allowed until $t_{d(TPRL)}$ is met. $t_{d(TPRL)}$ is the minimum delay time between the rising edge of the serial clock (SC) of the previously loaded tap point and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half.
3. After $t_{d(TPRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ condition. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the last serial clock (SC 255 or 511) of the active half.

PARAMETER MEASUREMENT INFORMATION

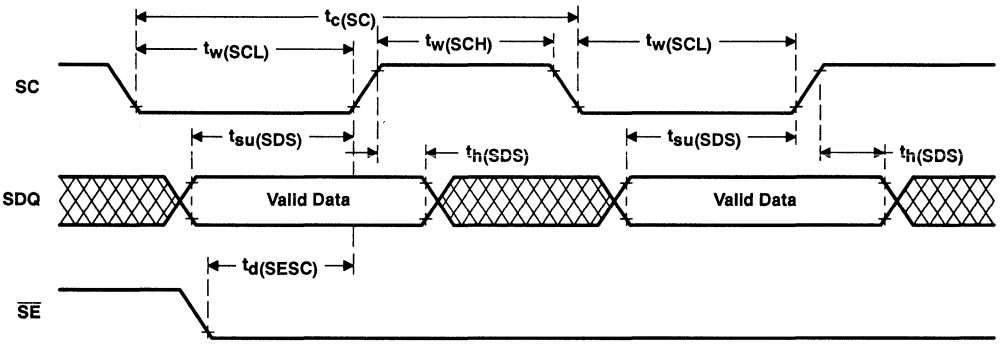
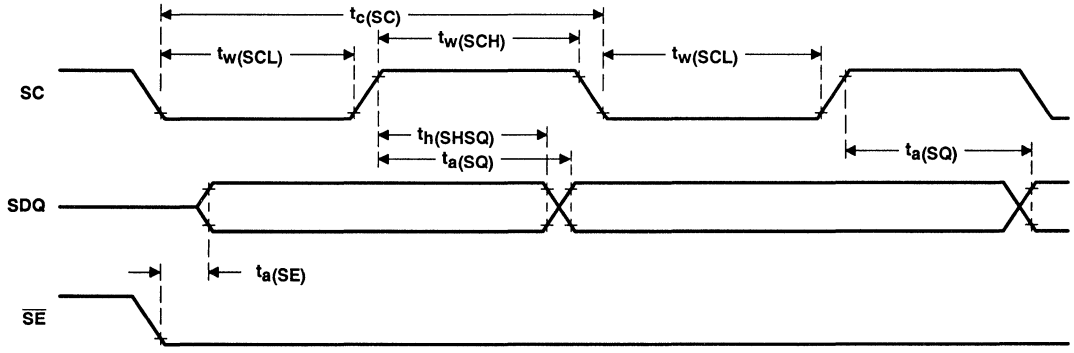


Figure 21. Serial Data-In Timing

The serial data-in cycle (SD) is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or transfer write cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will not take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.



NOTE A: When the odd tap is used (tap addresses can be 0–511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.

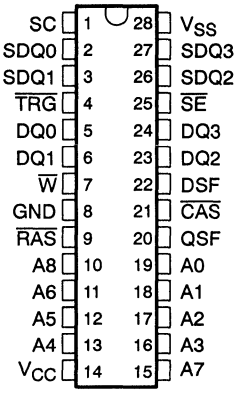
Figure 22. Serial Data-Out Timing

The serial data-out (SQ) cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

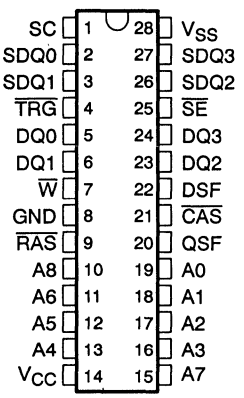
While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **Processed to MIL-STD-883, Class B**
- **DRAM: 262 144 Words × 4 Bits**
  SAM: 512 Words × 4 Bits
- **Dual Port Accessibility—Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register**
- **4 × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From an On-Chip Color Register**
- **Write Per Bit Feature for Selective Write to Each RAM I/O**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design**
- **Long Refresh Period . . . Every 8 ms (Max)**
- **Up to 33 MHz Uninterrupted Serial Data Streams**
- **3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams**
- **512 Selectable Serial Register Starting Locations**
- **Texas Instruments EPIC™ CMOS Process**
- **Packaging Options:**
  - **28-Pin Ceramic Sidebraze DIP (JD Suffix)**
  - **28-Pin Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)**
- **Split Serial Data Register for Simplified Realtime Register Reload**

JD PACKAGE†
(TOP VIEW)



HJ PACKAGE†
(TOP VIEW)



† Packages shown are for pinout reference only.

PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0–DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0–SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
QSF	Split Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: Not connected to internal V_{SS})

- **Performance Ranges:**

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$	V_{CC} TOLERANCE
'44C251-10	100 ns	25 ns	30 ns	20 ns	±10%
'44C251-12	120 ns	30 ns	35 ns	25 ns	±10%

description

The SMJ44C251 multiport video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each interfaced to a serial data register, or serial access memory (SAM), organized as 512 words of 4 bits each. The SMJ44C251 supports three basic

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types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the SMJ44C251 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SMJ44C251 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 4 block write mode. The block write mode allows four bits of data present in an on-chip color data register to be written to any combination of four adjacent column address locations. As many as 16 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask register provides a persistent write-per-bit without repeated mask loading.

On the serial register, or SAM port, the SMJ44C251 offers a split-register transfer read (DRAM TO SAM) option, which enables realtime register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

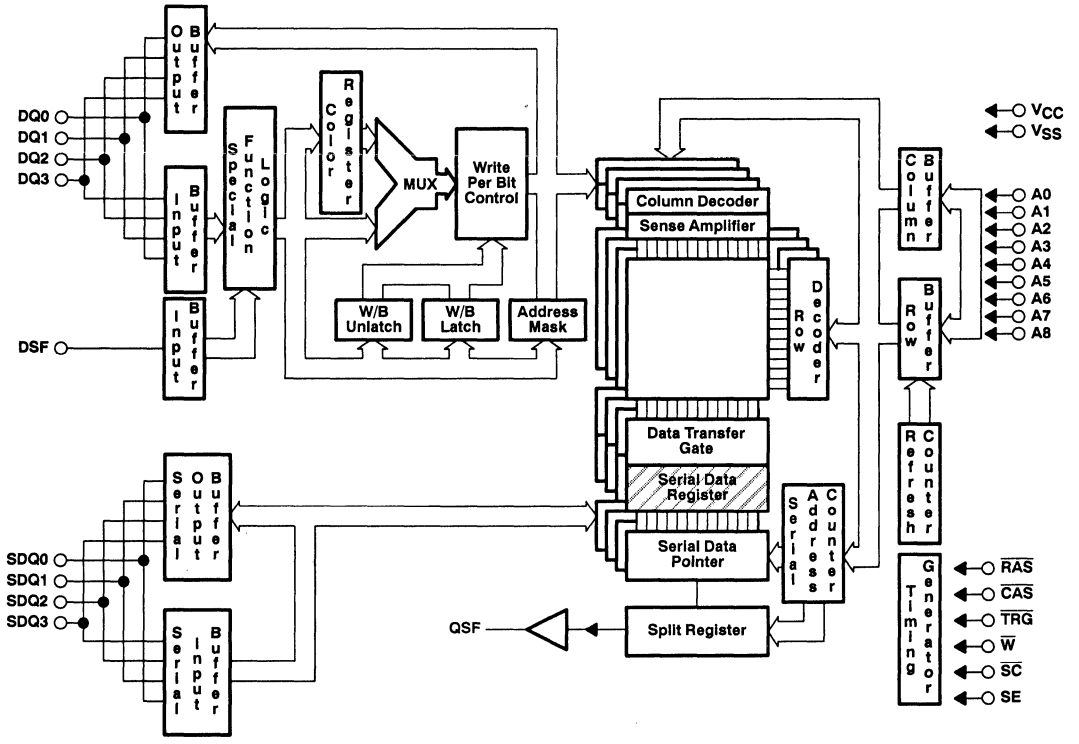
The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During a split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate open-drain output, designated QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The SMJ44C251 is offered both in a 28-pin 400-mil dual-in-line ceramic sidebrazed package (JD suffix) for through-hole row insertions, and in a 28-pin ceramic small outline J-leaded chip carrier package (HJ suffix) for surface-mount applications. The L suffix device is tested for operation from 0°C to 70°C. The M suffix device is tested for operation from – 55°C to 125°C.

The SMJ44C251 and other SMJ44C25x multiport video RAMs are supported by a broad line of video/graphic processors from Texas Instruments, including the SMJ34010 and the SMJ34020 graphics processors.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
DSF	Block Write Enable Persistent Write-per-Bit Enable Color Register Load Enable Write-per-Bit Mask Load Enable	Split Register Enable Alternate Write Transfer Enable	
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write-per-Bit Select	Transfer Write Enable	
QSF			Split Register Active Status
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND	System Ground (Important: not connected internally to V_{SS})		

operation

random access operation

Refer to Table 1, Functional Table (page 9), for random access and transfer operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a "T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See *transfer operation* for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0–A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and transfer functions of the SMJ44C251. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

The special function select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves four functions.

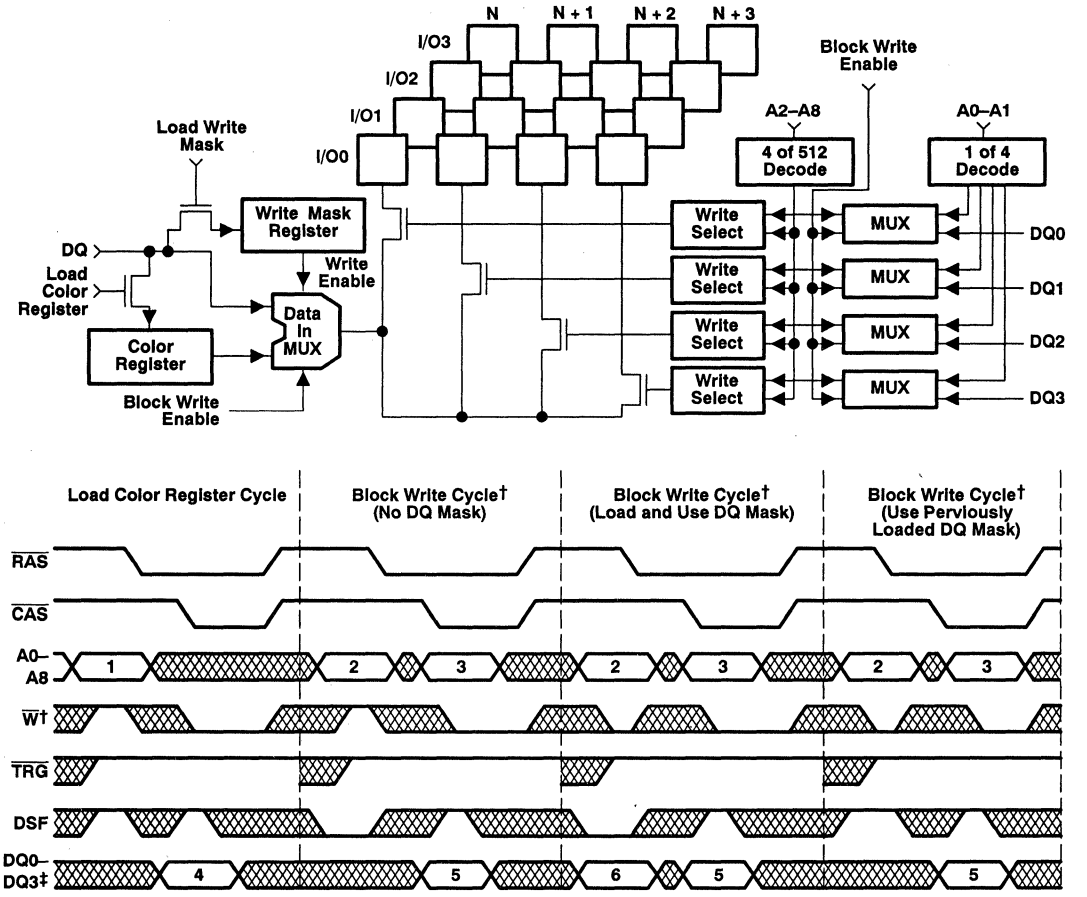
First, during write cycles DSF invokes persistent write-per-bit operation. If $\overline{TRG}$ is high, $\overline{W}$ is low, and DSF is low on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF is high, the mask will not be reloaded but will retain the data from the last mask reload cycle.

Second, DSF is used to change the internally stored write-per-bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write-per-bit cycles. This feature allows systems with a common address and data bus to use the write-per-bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, the DSF pin is used to load an on-chip four-bit data, or "color", register via the Load Color Register cycle. The contents of this register can subsequently be written to any combination of four adjacent column memory locations using the 4 × 4-Block Write feature. The load color register cycle is performed using normal write cycle timing except that DSF is held high on the falling edge of $\overline{RAS}$ and $\overline{CAS}$. Once the color register is loaded, it retains data until power is lost or until another load color register cycle is performed.

After loading the color register, the block write cycle can be enabled by holding DSF high on the falling edge of $\overline{CAS}$. During block write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of $\overline{CAS}$. The two least significant addresses (A0–A1) are replaced by the four DQ bits, which are also latched on the later of $\overline{CAS}$ or $\overline{W}$ falling. These four bits are used as an address mask and indicate which of the four column address locations addressed by A2–A8 will be written with the contents of the color register during the write cycle, and which ones will not. DQ0 enables a write to column address A1 = low, A0 = low; DQ1 enables a write to A1 = low, A0 = high; DQ2 enables a write to A1 = high, A0 = low; and DQ3 enables a write to A1 = high, A0 = high. A logic high level enables a write and a logic low level disables the write. A maximum of 16 bits can be written to memory during each $\overline{CAS}$ cycle (see Figure 1, Block Write Diagram).

Fourth, the DSF pin is used to invoke the split-register transfer and serial access operation, described in the sections "transfer operation" and "serial operation".



† $\overline{W}$ must be low during the Block Write Cycle.
‡ DQ0–DQ3 ($\overline{CAS}$) are latched on the later of $\overline{W}$ or $\overline{CAS}$ falling edge. DQ0–DQ3 ($\overline{RAS}$) are latched on $\overline{RAS}$ falling edge.
Legend:

1. Refresh Address
2. Row Address
3. Block Address (A2–A8)
4. Color Register Data
5. Column Mask Data
6. DQ Mask Data

= Don't Care

Figure 1. Block Write Diagram

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write-per-bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation. Two modes of write-per-bit operation are supported.

Case 1. If DSF is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF is high on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write-per-bit mask reload. This mode of operation is know as Persistent Write-Per-Bit, since the write-per-bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0–DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The 3-state output buffers provide direct TTL compatibility (no pullup resistors required) with a fanout of two Series 74/54 TTL loads. Data-out is the same polarity as Data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory-to-register or register-to-memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C251 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The SMJ44C251 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write-per-bit operations, the DQ pins are used to load the write-per-bit mask register described above under the $\overline{W}$ pin description.

During block write operations, the DQ pins are used to load the on-chip color register during the load color register cycle and are also used as a write enable during block write cycles.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND (Pin 8)

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Functional Table

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0–DQ3		FUNCTION
	CAS	TRG	W¶	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	X	X	CAS-before-RAS Refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate Transfer Write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial Write-Mode Enable (Pseudo-Transfer Write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory to Register Transfer (Transfer Read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split Register Transfer Read (Must Reload Tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and Use Write Mask, Write Data to DRAM
R	H	H	L	L	X	H	Row Addr	Col A2–A8	Write Mask	Addr Mask	Load and Use Write Mask, Block Write to DRAM
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent Write-Per-Bit, Write Data to DRAM
R	H	H	L	H	X	H	Row Addr	Col A2–A8	X	Addr Mask	Persistent Write-Per-Bit, Block Write to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal Dram Read/Write (Nonmasked)
R	H	H	H	L	X	H	Row Addr	Col A2–A8	X	Addr Mask	Block Write to DRAM (Nonmasked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load Write Mask
R	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	Load Color Register

† R = Random access operation; T = Transfer operation.
‡ DQ0–DQ3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
¶ In persistent write-per-bit function, W must be high during the refresh cycles
Addr Mask = 1; write to address location enabled
Write Mask = 1; write to I/O enabled.

random port to serial port interface

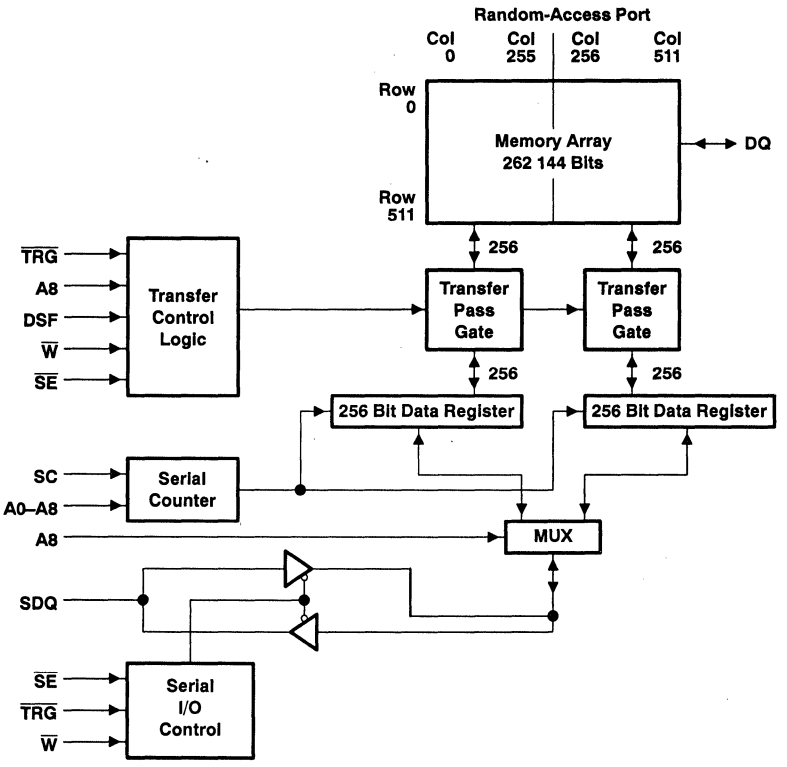


Figure 2. Block Diagram Showing One Random and One Serial I/O Interface

random address space to serial address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

split-register mode random-access to serial address-space mapping

In split-register transfer operations, the serial data register is split into halves, the low half containing bits 0–255 and the high half containing bits 256–511. When a split-register transfer cycle is performed, the tap address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit (A8) determines which register half will be reloaded from the memory array. The eight remaining column address bits (A0–A7) are used to select the SAM starting location for the register half selected by A8.

To insure proper operation when using the split-register read transfer feature, a non-split-register transfer must precede any split-register sequence. The serial start address must be supplied for every split-register transfer. (See Split Register Operating Sequence on page 38.)

transfer operations

As illustrated in Table 1, the SMJ44C251 supports five basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM to SAM)
5. Split-Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

NOTES: A. All transfer write operations will switch the SDQ pins into the input (write) mode. Before data can be clocked into the serial port via the SDQ pins and SC serial clock, it is necessary to switch the SDQ pins into input mode via a previous transfer write operation.
B. *Pseudo Transfer Write Mode* has the same meaning as the term "Write Mode Control Cycle" as used in some VRAM data sheets. Both modes, or control cycles, serve to switch the direction of the SDQs without an actual data transfer taking place.
C. All transfer read operations will switch the SDQ pins into the output (read) operation.
D. All transfer read operations and the pseudo transfer write operation perform a memory refresh on the selected row.

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. The SDQs are put into input mode by use of a transfer write cycle. This allows serial data to be input into the SAM. An alternative way to perform the transfer write cycle is by holding DSF high on the falling edge of $\overline{RAS}$. In this way, the state of $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0–A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

In the split-register transfer mode, the most significant column address bit (A8) selects which half of the register will be loaded from the memory array. The remaining eight addresses (A0–A7) determine the register starting location for the register to be loaded.

special function input (DSF)

In the read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split-register mode transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of the most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split-register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

In the write transfer mode, holding DSF high on the falling edge of RAS permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without permitting a pseudo write transfer, with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The SMJ44C251 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0–SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The serial enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 2). If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls and DSF is low, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

QSF active status output

QSF is an open-drain output pin. During the split register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

QSF changes state upon crossing the boundary between the two register halves. When the SAM is not operating in split-register mode, the QSF output remains in the high-impedance state.

QSF is designed as an open drain output to allow OR-type of QSF outputs from several chips. Thus, an external pullup resistor is required for the zero to one transition on QSF and the output rise time is determined by the load-capacitance and the value of the pullup resistor. The specification for QSF switching time assumes a pullup resistor of 820 Ω and a load capacitance of 30 pF illustrated as follows.

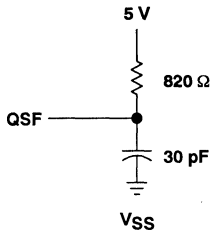


Figure 3. QSF Load Circuit

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
L	L	L	X	Register to memory (write) transfer, serial write mode enable
L	L	X	H	Alternate register to memory transfer
L	L	H	L	Serial write mode enable (pseudo write transfer)
L	H	X	L	Memory to register (read) transfer
L	H	X	H	Split-register read transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Alternate register to memory	H	Input Disabled
Serial write mode enable†	L	Input Enabled
Serial write mode enable†	H	Input Disabled
Memory to register	L	Output Enabled
Memory to register	H	HI-Z

† Pseudo transfer write.

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle, and two SC cycles.

absolute maximum ratings over operating temperature (unless otherwise noted)†

Input voltage range on any pin except DQ and SDQ (see Note 1) ..... −1 V to 7 V
Input voltage range on DQ and SDQ (see Note 1) ..... −1 V to V_{CC} + 1
Input voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range:
SMJ44C251, L suffix ..... 0°C to70°C
SMJ44C251, M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.9		V_{CC} + 1	V
V_{IL}	Low-level input voltage (see Note 2)		−1		0.6	V
T_A	Operating free-air temperature	L suffix	0			°C
		M suffix	−55			
T_C	Operating case temperature	L suffix			70	°C
		M suffix			125	

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = – 5 mA	2.4		V
V_{OL}	Low level output voltage (see Note 4)	I_{OL} = 4.2 mA		0.4	V
I_L	Input leakage current	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins open		±1.0	μA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10	μA

PARAMETER			SAM PORT	'44C251-10		'44C251-12		UNIT
				MIN	MAX	MIN	MAX	
I_{CC1} I_{CC1A}	Operation current $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum	(see Note 5)	Standby		100		90	mA
			Active		110		100	
I_{CC2} I_{CC2A}	Standby current, All clocks = V_{CC} $t_{c(SC)}$ = Minimum		Standby		15		15	
			Active		35		35	
I_{CC3} I_{CC3A}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		100		90	
			Active		110		100	
I_{CC4} I_{CC4A}	Page mode current, $t_{c(P)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		65		60	
			Active		70		65	
I_{CC5} I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		90		80	
			Active		110		100	
I_{CC6} I_{CC6A}	Data transfer current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		100		90	
			Active		110		100	

NOTES: 3. $\overline{SE}$ is disabled for SDQ output leakage tests.

4. The SMJ44C251 1-megabit video RAM may exhibit simultaneous switching noise as described in the Texas Instruments *Advanced CMOS Logic Designer's Handbook*. This phenomenon exhibits itself upon the DQ pins when the SDQ pins are switched and upon the SDQ pins when DQ pins are switched. This may cause the V_{OL} and V_{OH} to exceed the data book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.

5. I_{CC} (standby) vs I_{CCA} (active) denotes the following:
I_{CC} (standby) denotes that the SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
I_{CCA} (active) denotes that the SAM port is active and the DRAM port is active (except for I_{CC2}).
I_{CC} is measured with no load on DQ or SDQ pins.

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		8	pF
$C_{o(QSF)}$	Output capacitance, QSF		14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 7)

NO.	PARAMETER		TEST CONDITIONS	ALT. SYMBOL	'44C251-10		'44C251-12		UNIT
					MIN	MAX	MIN	MAX	
1	$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30	ns
2	$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
3	$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MIN	t_{CAP}		55		65	ns
4	$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MIN	t_{RAC}		100		120	ns
5	$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
6	$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		30		35	ns
7	$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		25	ns
8	$t_{a(QSF)}$	Access time of QSF from SC low	C_L = 30 pF			60		60	ns
9	$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 80 pF	t_{OFF}	0	20	0	20	ns
10	$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 80 pF	t_{OEZ}	0	20	0	20	ns
11	$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	20	0	20	ns

NOTES: 7. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 3).
8. Disable times are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating temperature†

NO.	PARAMETER		ALT. SYMBOL	'44C251-10		'44C251-12		UNIT
				MIN	MAX	MIN	MAX	
12	$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	190		220		ns
13	$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
14	$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
15	$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
16	$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{PRWC}	105		125		ns
17	$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
18	$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
19	$t_{c(SC)}$	Serial clock cycle time (see Note 10)	t_{SCC}	30		35		ns
20	$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	20		30		ns
21	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 11)	t_{CAS}	25	75 000	30	75 000	ns
22	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
23	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 12)	t_{RAS}	100	75 000	120	75 000	ns
24	$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
25	$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
26	$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
27	$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
28	$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
29	$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low		0		0		ns
30	$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
31	$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
32	$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low (write mask operation)	t_{MS}	0		0		ns
33	$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
34	$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low (see Note 13)	t_{ESR}	0		0		ns
35	$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low		0		0		ns
36	$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
37	$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
38	$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
39	$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
40	$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
41	$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
42	$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 5 ns.

10. When the odd tap is used (tap address can be 0–511, and odd taps are 1,3,5, etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.
11. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
12. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
13. Register to memory (write) transfer cycles only.

timing requirements over recommended ranges of supply voltage and operating temperature (continued)†

NO.	PARAMETER		ALT. SYMBOL	'44C251-10		'44C251-12		UNIT
				MIN	MAX	MIN	MAX	
43	$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
44	$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low		20		20		ns
45	$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns
46	$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
47	$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low (see Note 13)	t_{REH}	15		15		ns
48	$t_{h(RWM)}$	$\overline{W}$ hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
49	$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
50	$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low		15		15		ns
51	$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 14)	t_{AR}	45		45		ns
52	$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
53	$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 14)	t_{DHR}	45		50		ns
54	$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
55	$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 15)	t_{RCH}	0		0		ns
56	$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 15)	t_{RRH}	10		10		ns
57	$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
58	$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 14)	t_{WCR}	50		55		ns
59	$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 20)	t_{OEH}	25		30		ns
60	$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
61	$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
62	$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
63	$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
64	$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
65	$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 16 and 17)	t_{CWD}	55		65		ns
66	$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)	t_{RCD}	25	75	25	90	ns
67	$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
68	$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 16)	t_{RWD}	130		155		ns
69	$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 16)	t_{AWD}	85		100		ns
70	$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 19)	t_{CHR}	25		25		ns
71	$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 19)	t_{CSR}	10		10		ns
72	$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 19)	t_{RPC}	10		10		ns
73	$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		30		ns
74	$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ (see Note 16)		25		30		ns
75	$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register to memory (write) transfer cycles only.
14. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. Read-modify-write operation only.
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. Maximum value specified only to assure $\overline{RAS}$ access time.
19. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
20. Output enable controlled write. Output remains in the high-impedance state for the entire cycle.

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)†

NO.	PARAMETER		ALT. SYMBOL	'44C251-10		'44C251-12		UNIT
				MIN	MAX	MIN	MAX	
76	$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{RSD}	130		140		ns
77	$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	40		45		ns
78	$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 21 and 22)	t_{TSL}	15		20		ns
79	$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 21)	t_{TRD}	−10		−10		ns
80	$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low (see Notes 13 and 23)	t_{SRS}	10		20		ns
81	$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		20		20		ns
82	$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 13)	t_{SRD}	25		30		ns
83	$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 24)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
84	$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 24)	t_{TSD}	35		40		ns
85	$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 25)	t_{SWS}	10		15		ns
86	$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		25		30		ns
87	$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles		20		25		ns
88	$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register to memory (write) transfer cycles only.
21. Memory to register (read) transfer cycles only.
22. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
23. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
24. Memory to register (read) and register to memory (write) transfer cycles only.
25. Serial data-in cycles only.
26. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

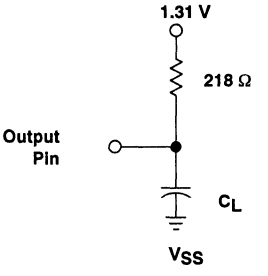


Figure 4. Load Circuit

PARAMETER MEASUREMENT INFORMATION

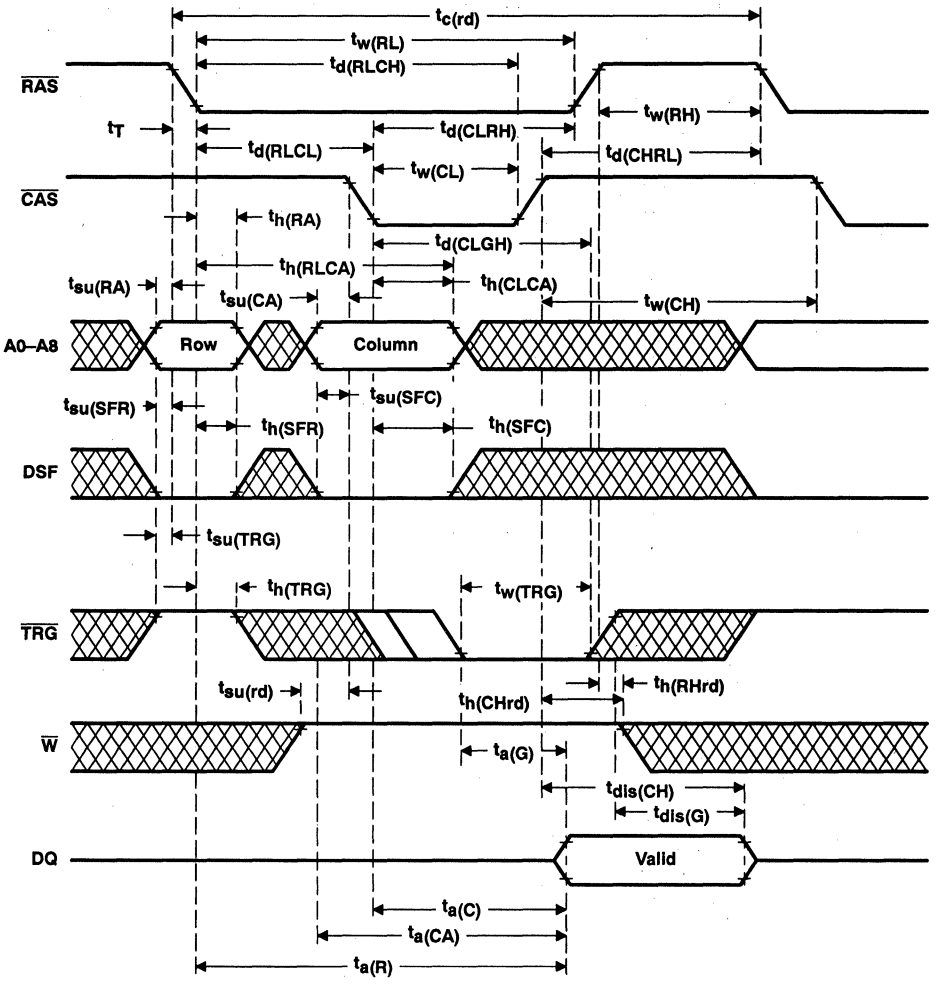
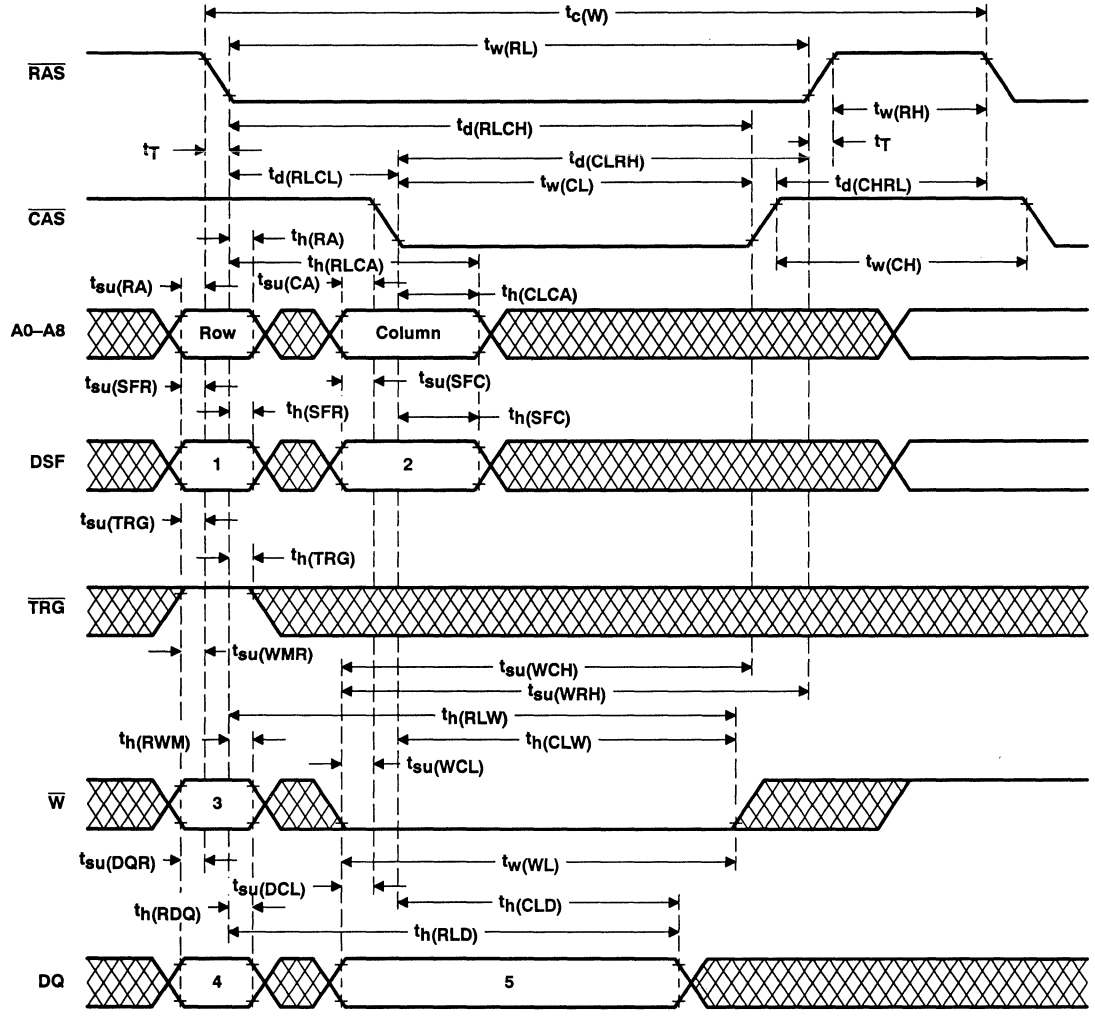


Figure 5. Read Cycle Timing

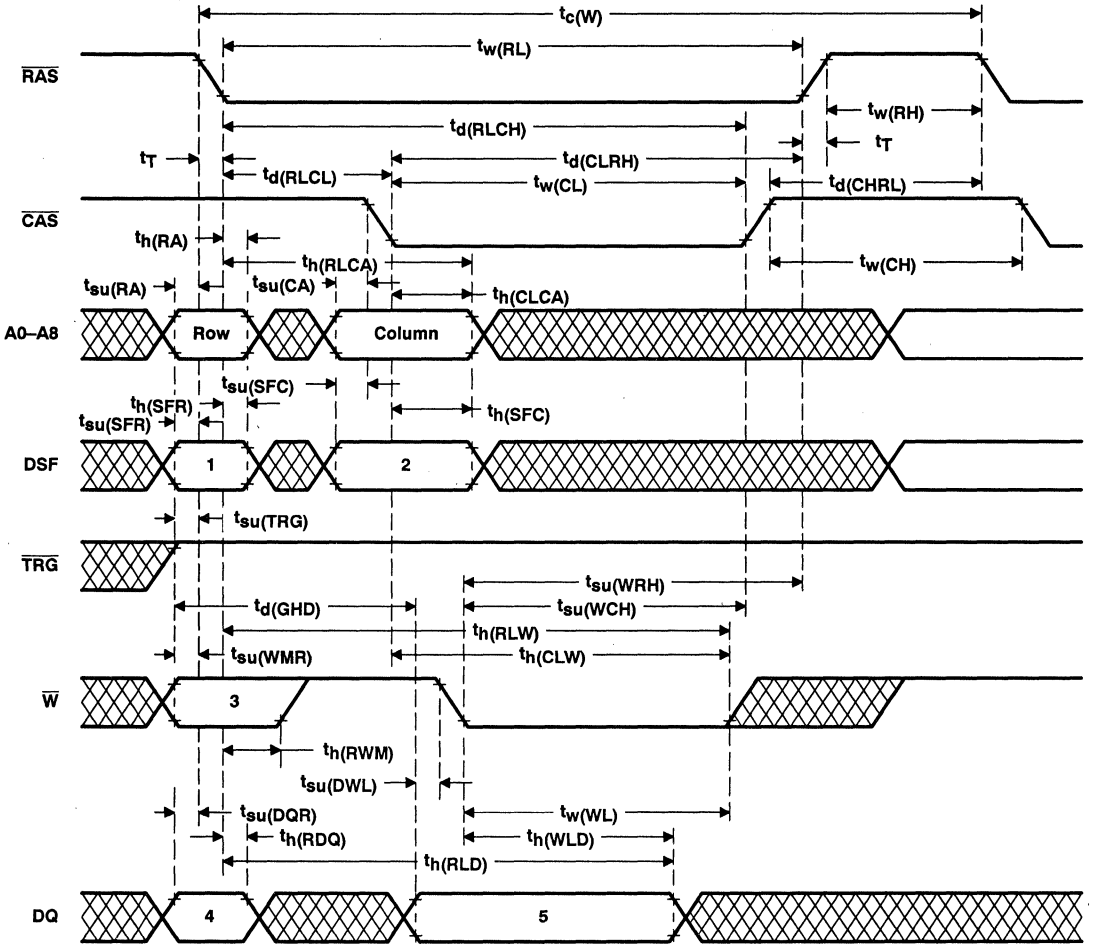
PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

Figure 6. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

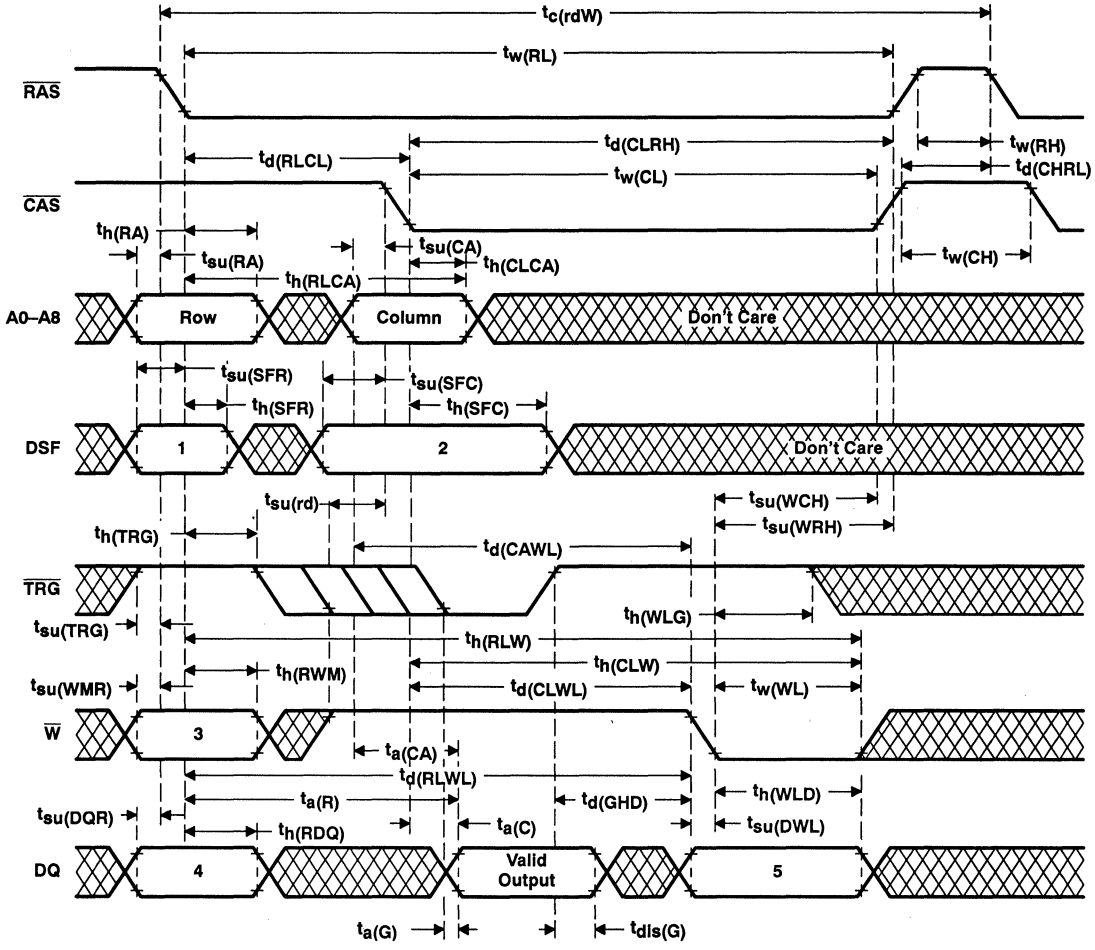
Figure 7. Delayed Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

write cycle state table

CYCLE	STATE				
	1	2	3	4	5
Write mask load/use, write DQs to I/Os	L	L	L	Write Mask	Valid Data
Write mask load/use, block write	L	H	L	Write Mask	Addr Mask
Use previous write mask, write DQs to I/Os	H	L	L	Don't Care	Valid Data
Use previous write mask, block write	H	H	L	Don't Care	Addr Mask
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't Care	Write Mask
Load color register on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	H	H	Don't Care	Color Data
Write mask disabled, block write to all I/Os	L	H	H	Don't Care	Addr Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

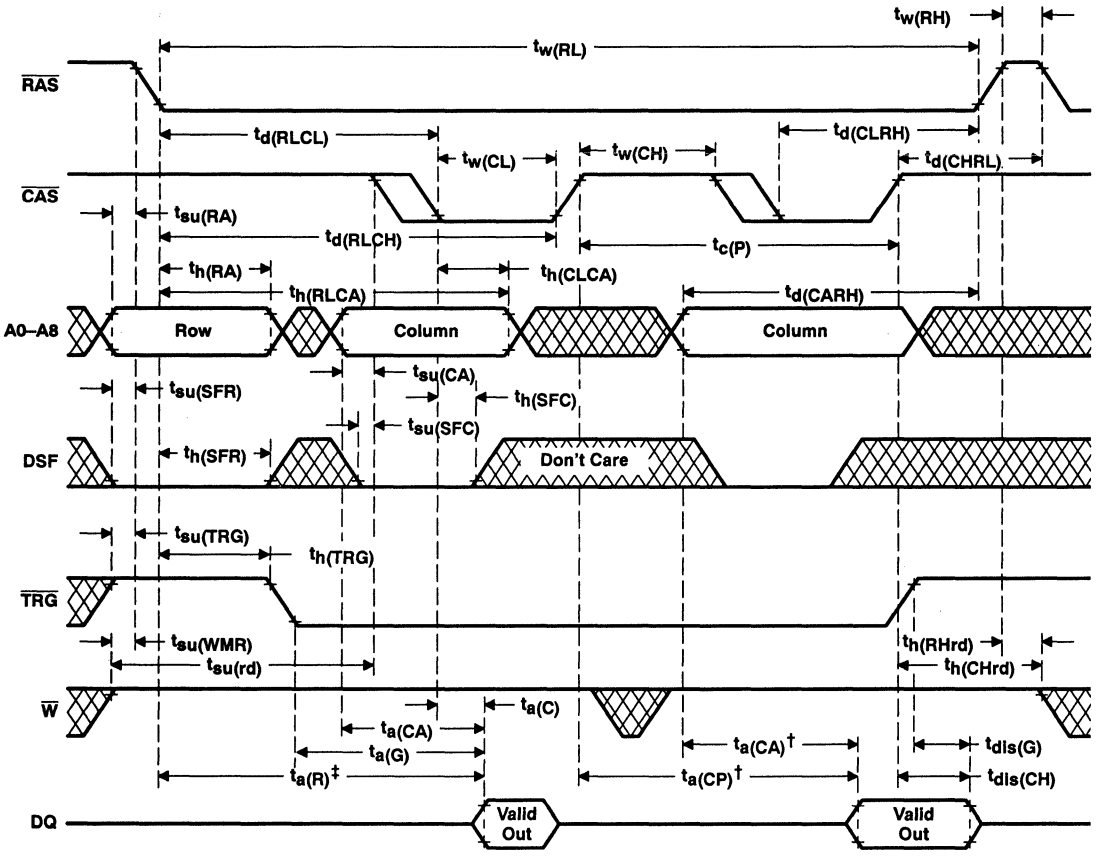
PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

Figure 8. Read-Write/Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



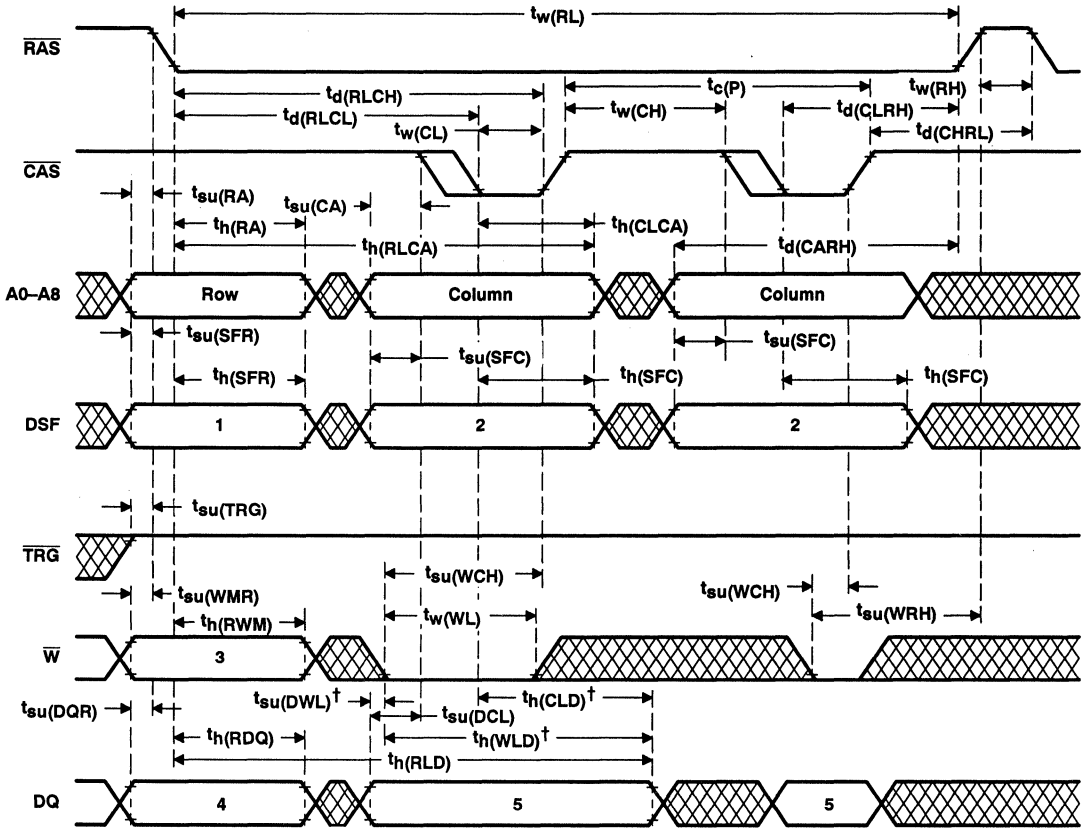
† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 9. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



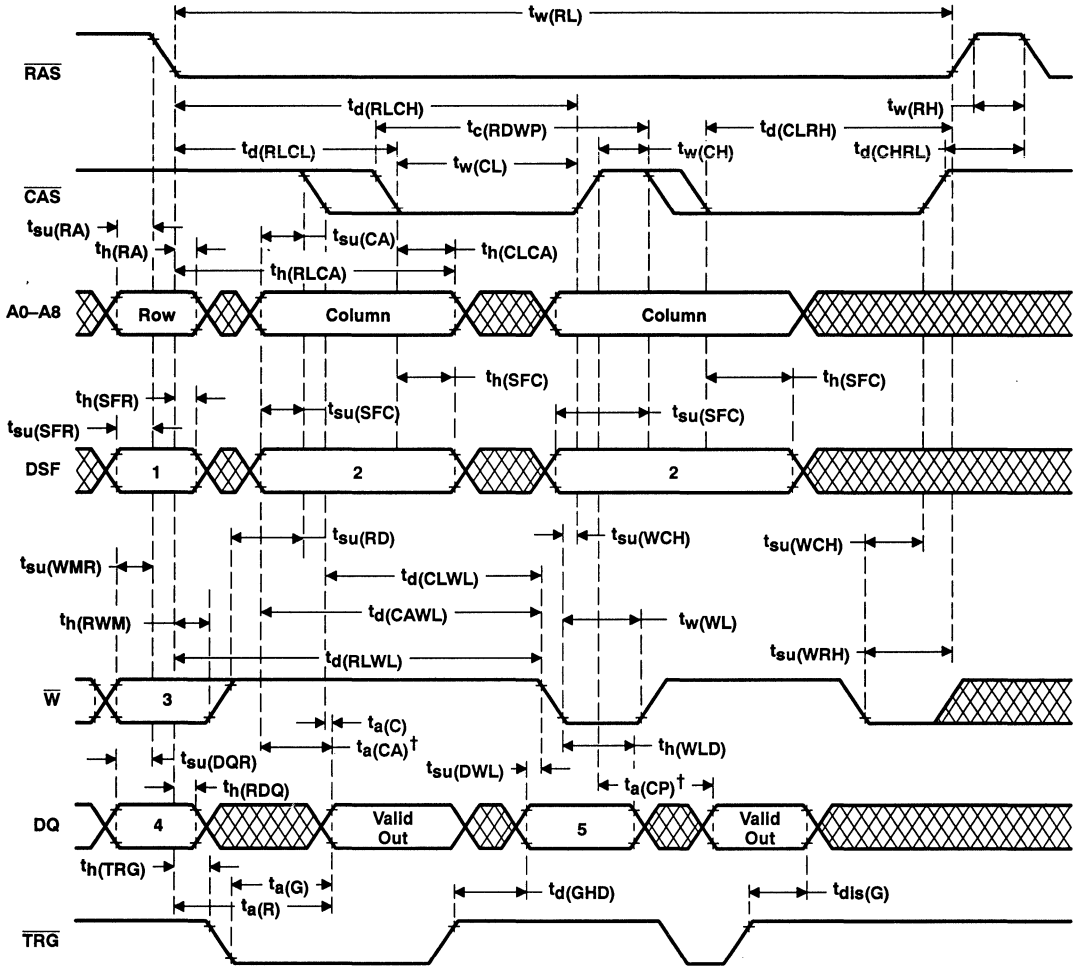
† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: A. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

B. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to assure page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 10. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

NOTES: A. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 11. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

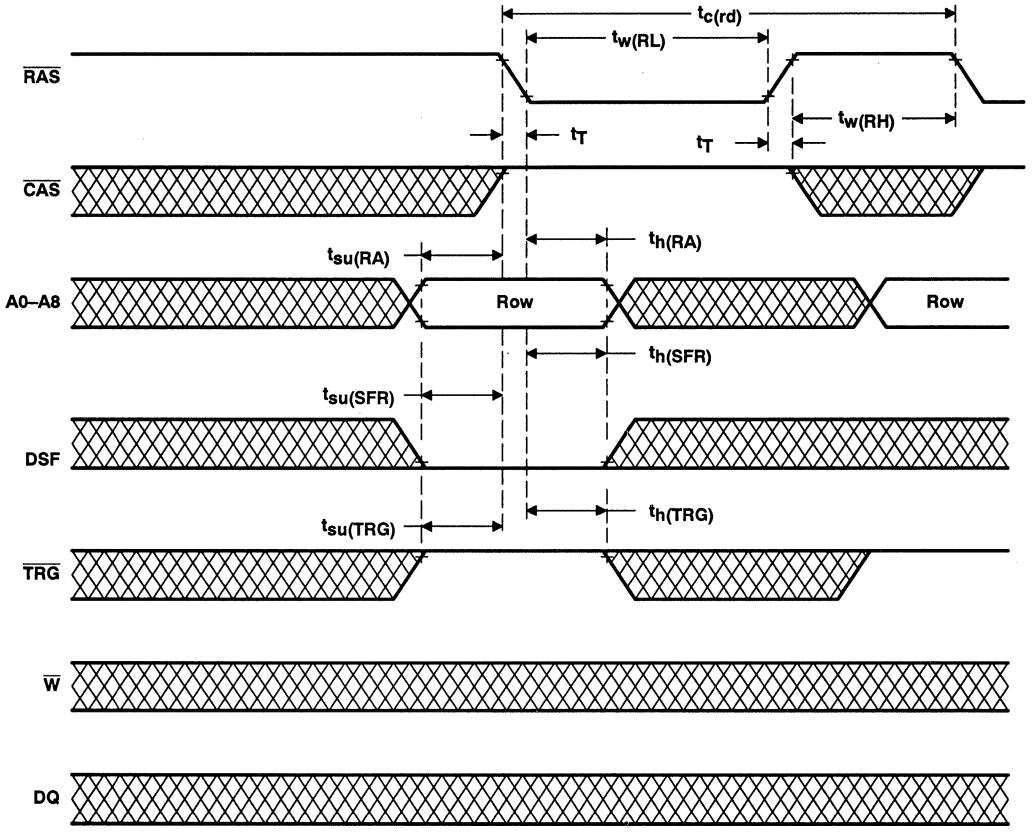


Figure 12. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

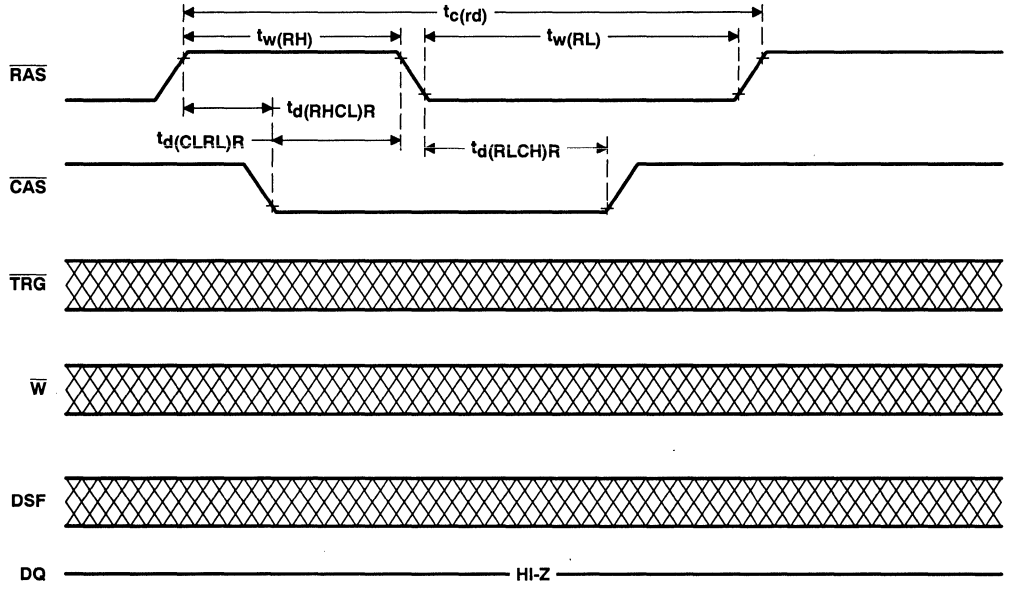


Figure 13. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

PARAMETER MEASUREMENT INFORMATION

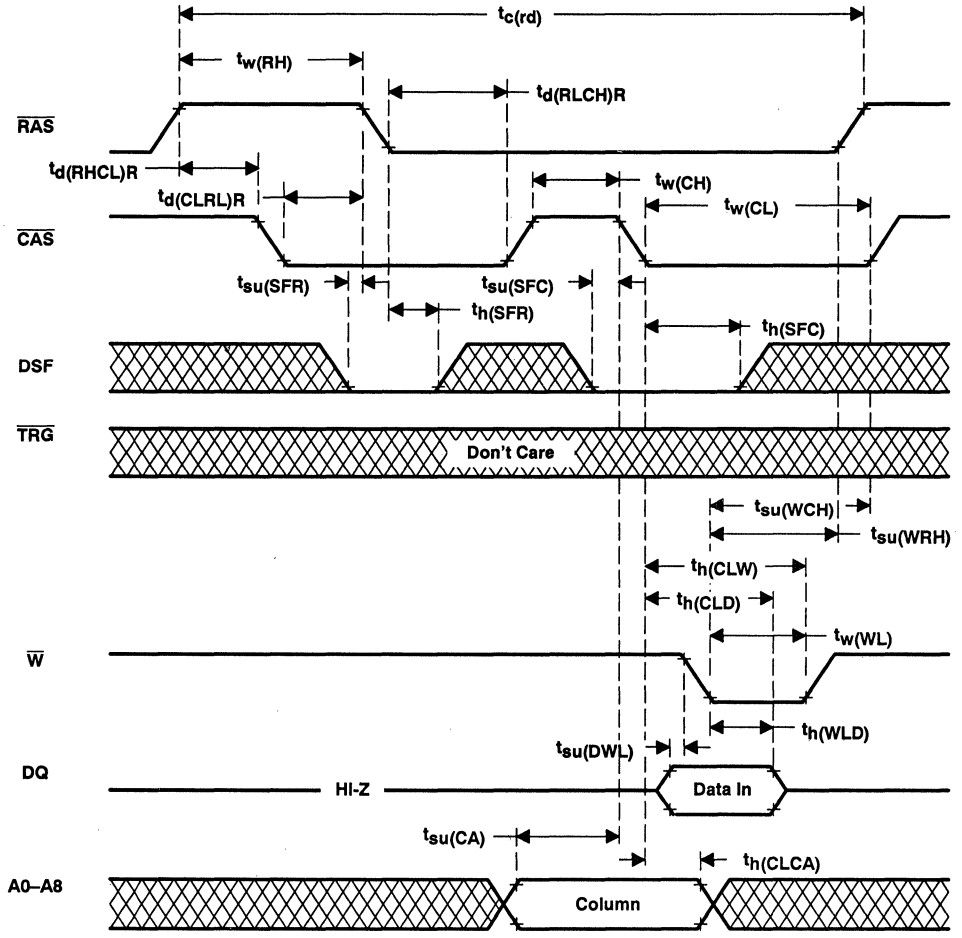


Figure 14. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Timing

PARAMETER MEASUREMENT INFORMATION

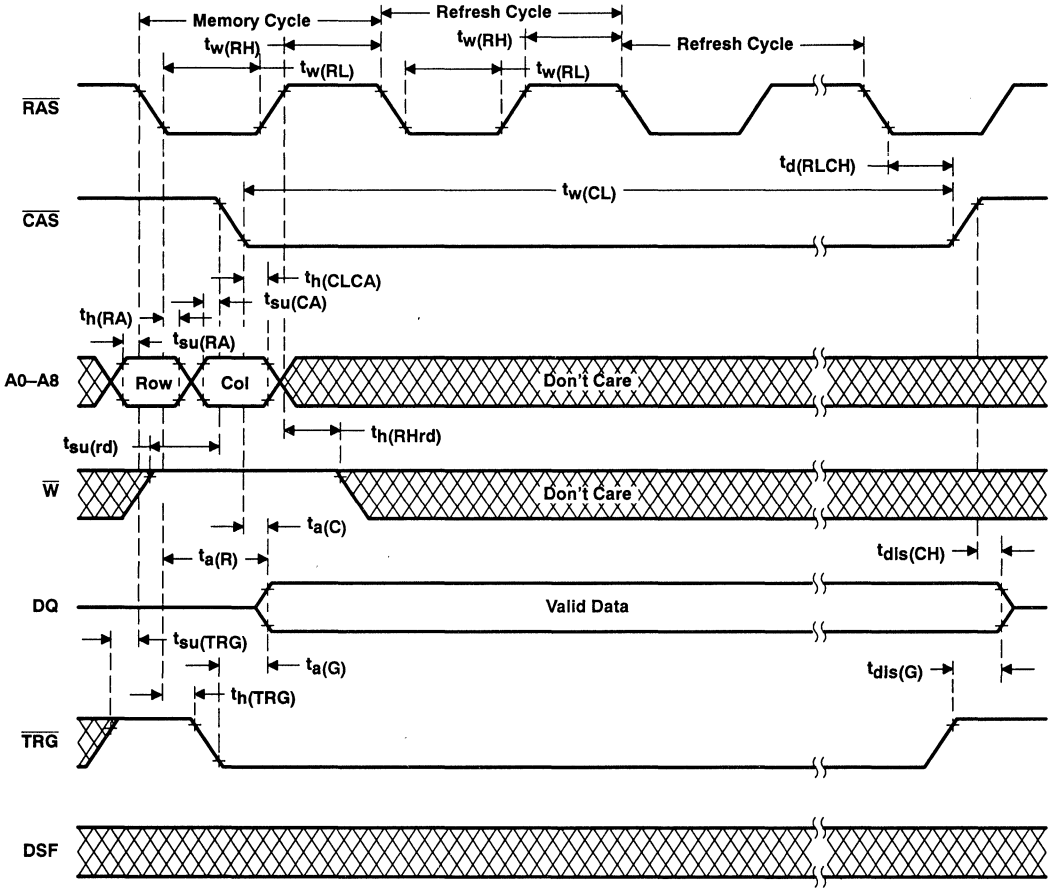
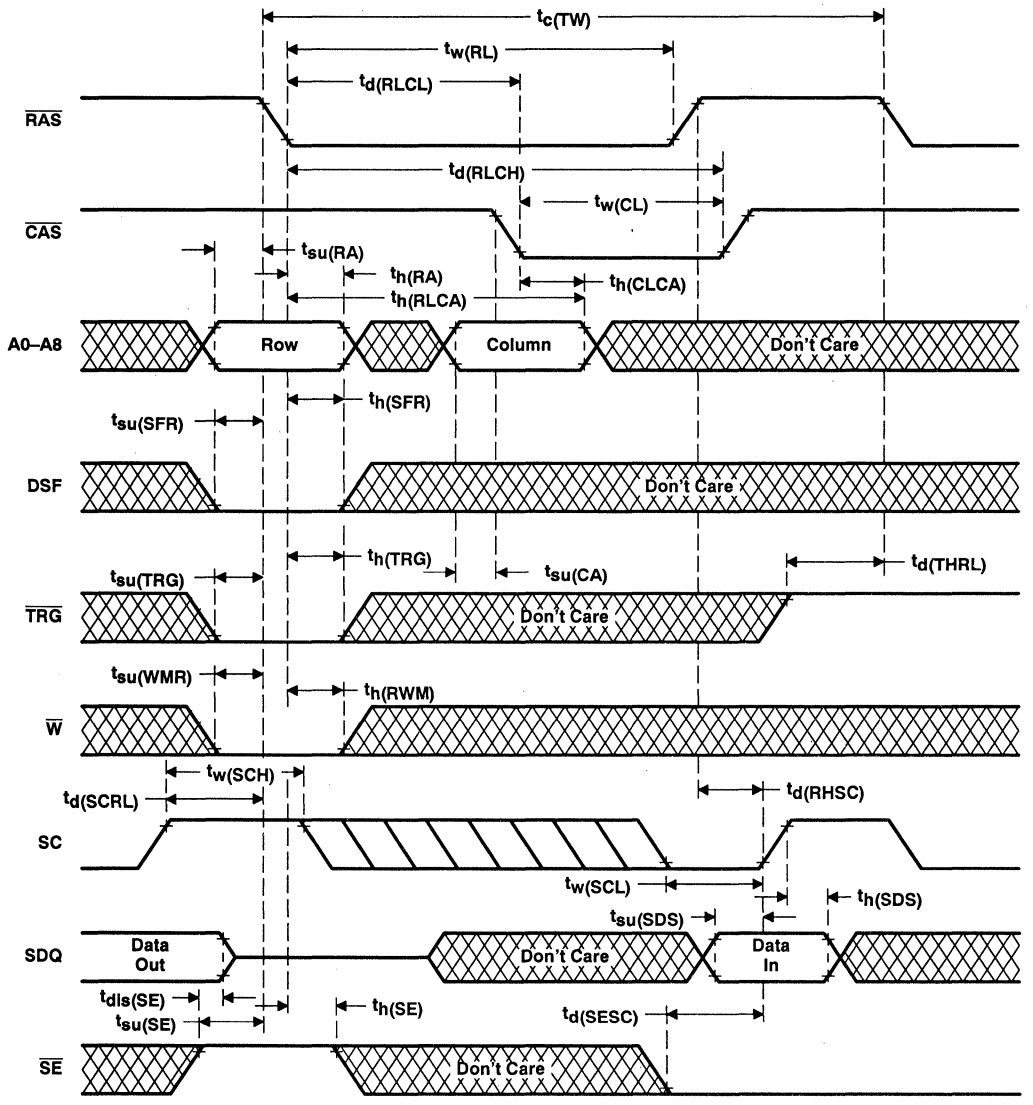


Figure 15. Hidden Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

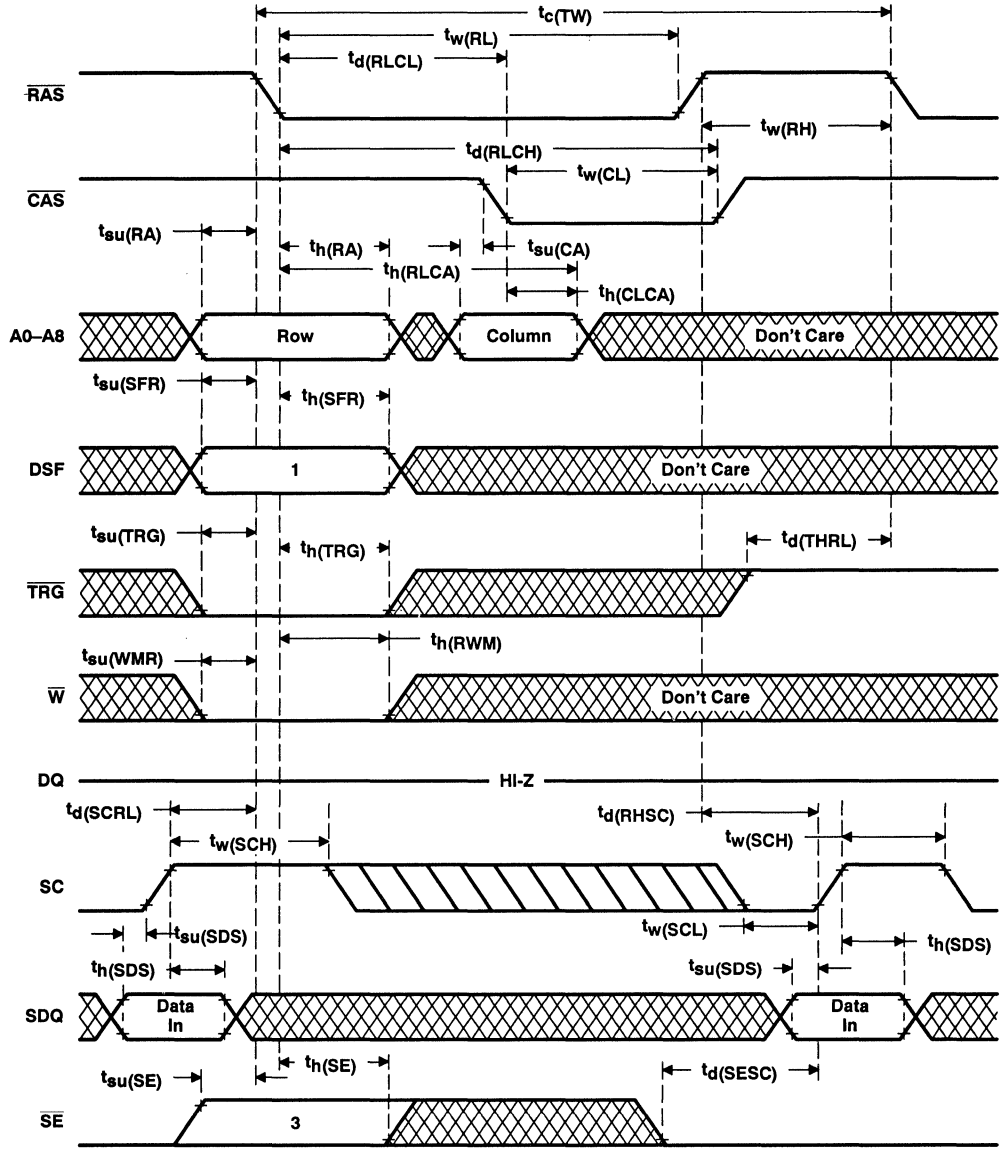
The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: A. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
B. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

Figure 16. Write-Mode Control Pseudo Write Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

B. See "Register Transfer Function Table" for logic state of "1" and "3".

C. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.

Figure 17. Data Register to Memory Timing, Serial Input Enabled

PARAMETER MEASUREMENT INFORMATION

register transfer function table

FUNCTION	$\overline{RAS}$ FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer	L	L	X	L
Register to memory transfer, alternate transfer write	L	L	H	X
Pseudo-transfer SDQ control, serial input enabled	L	L	L	H
Memory to register transfer	L	H	L	X
Split-register transfer	L	H	H	X

PARAMETER MEASUREMENT INFORMATION

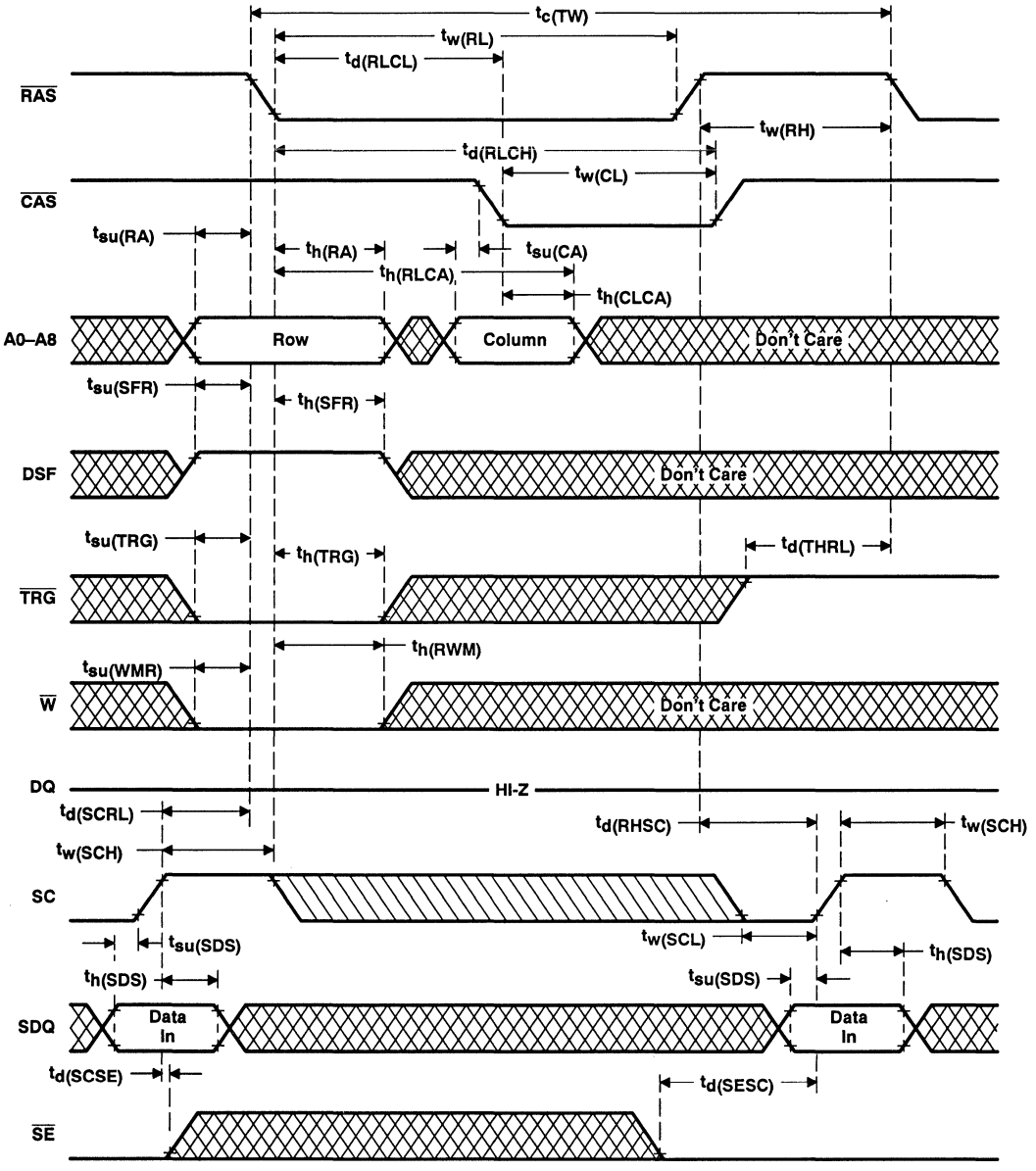
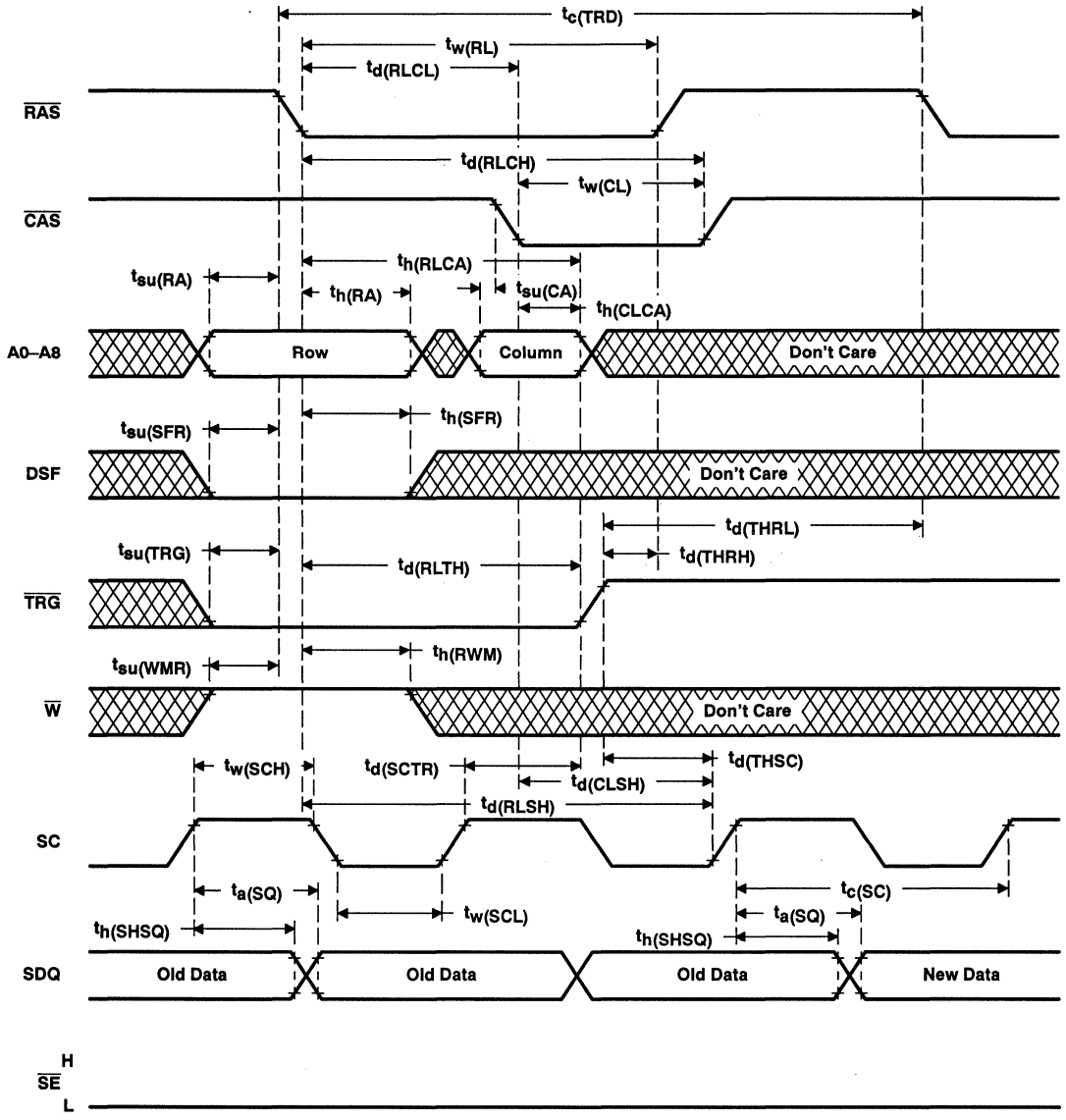


Figure 18. Alternate Data Register to Memory Timing

PARAMETER MEASUREMENT INFORMATION

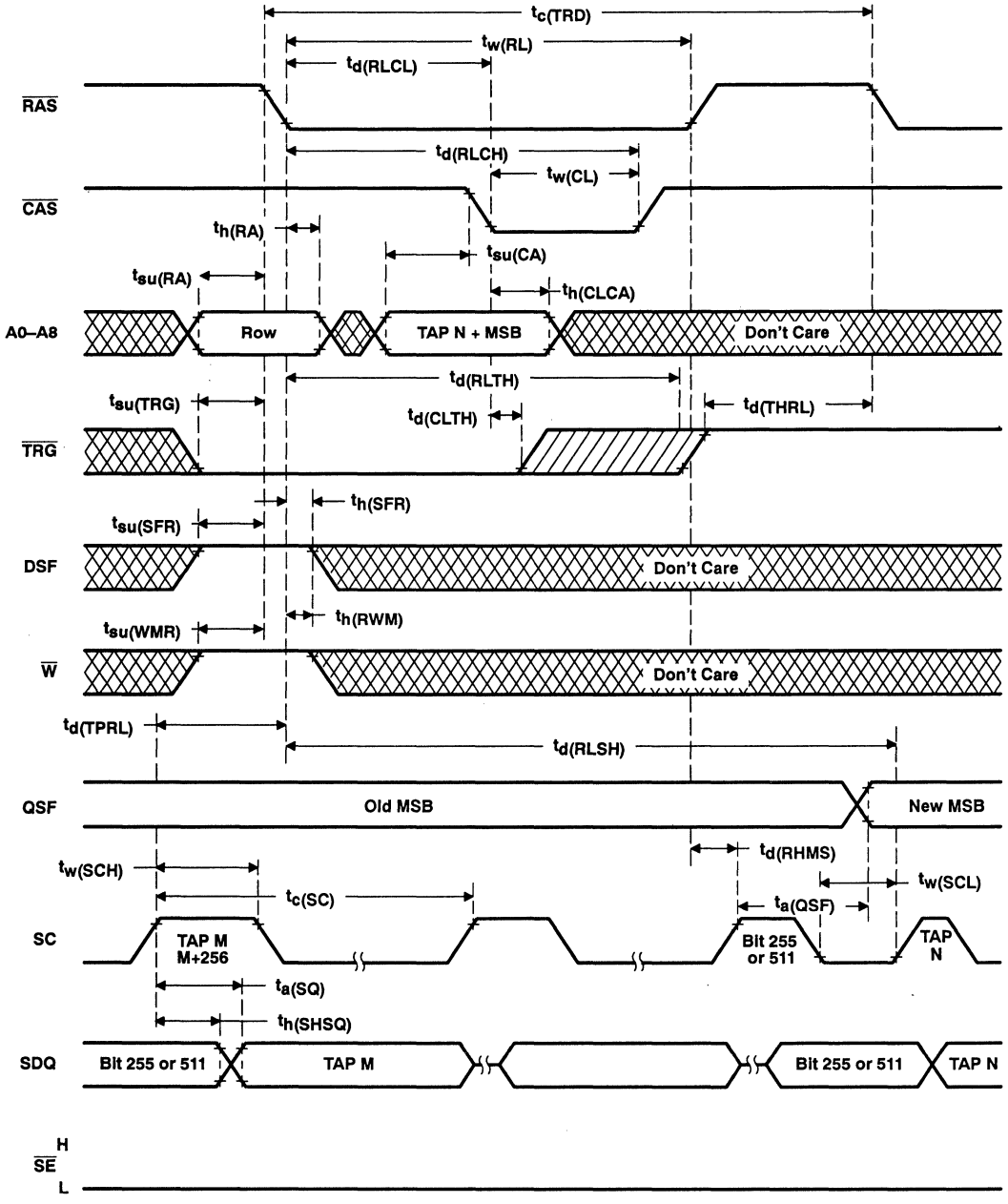


NOTES: A. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

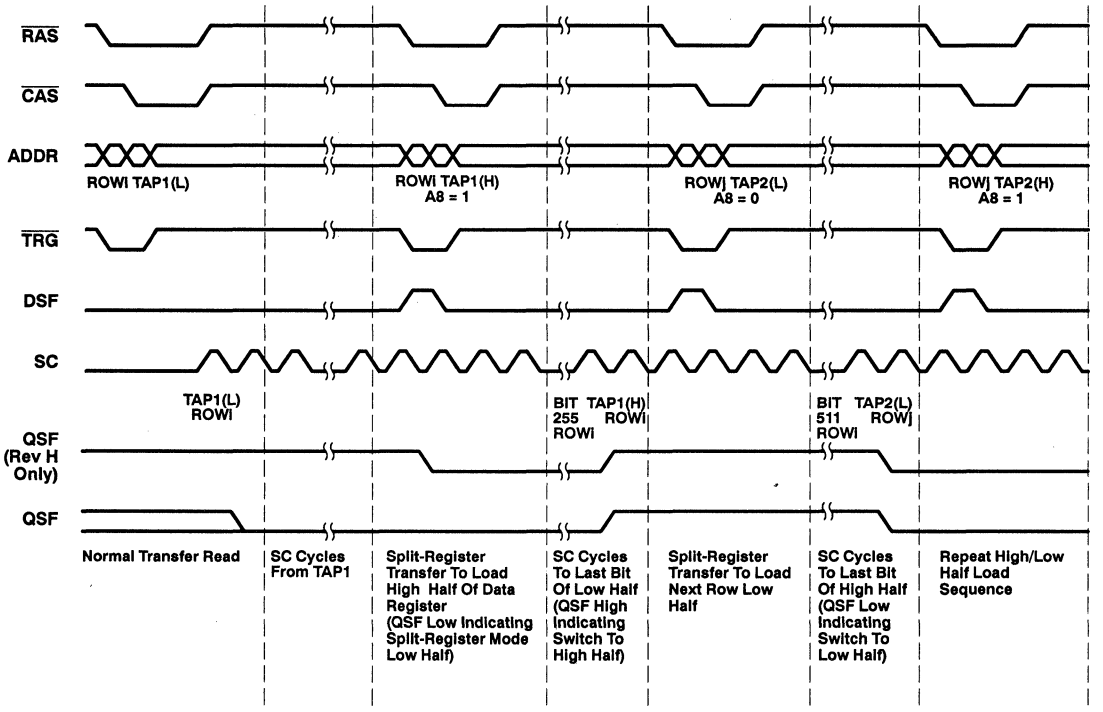
Figure 19. Memory to Data Register Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: There must be a minimum of two SC clocks cycle between any two split-register reload cycles, and a minimum of one SC clock cycle between a transfer read cycle and a split-register cycle.

Figure 20. Split-Register Mode Read Transfer Timing



NOTES: A. In the split-register mode, data can be transferred from different rows to the low and high halves of the data register.
B. When enabling or disabling the split-register mode, $t_{a(QSF)}$ is measured from $\overline{RAS}$ low in the transfer cycle.

Figure 21. Split-Register Operating Sequence

application notes

1. In order to achieve proper split-register operation, a normal read transfer followed by a minimum of one serial clock cycle should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. Serial access can then begin after the normal transfer cycle.
2. A split-register transfer into the inactive half is not allowed until $t_{d(TPRL)}$ is met. $t_{d(TPRL)}$ is the minimum delay time between the rising edge of the serial clock (SC) of the previously loaded tap point and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half.
3. After $t_{d(TPRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ condition. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the last serial clock (SC 255 or 511) of the active half.

PARAMETER MEASUREMENT INFORMATION

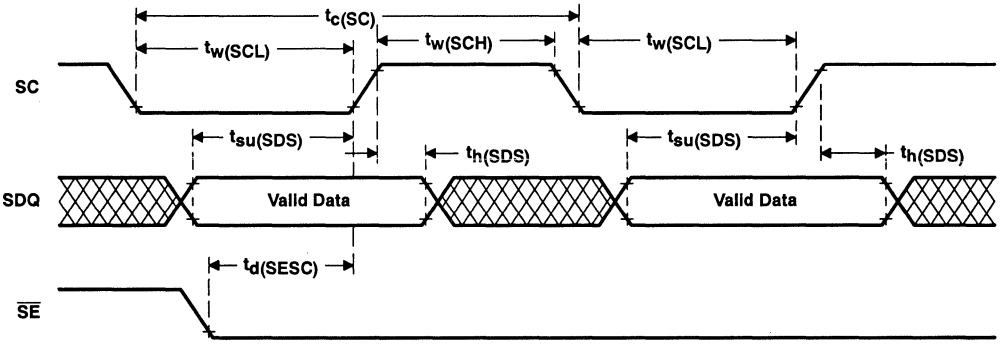
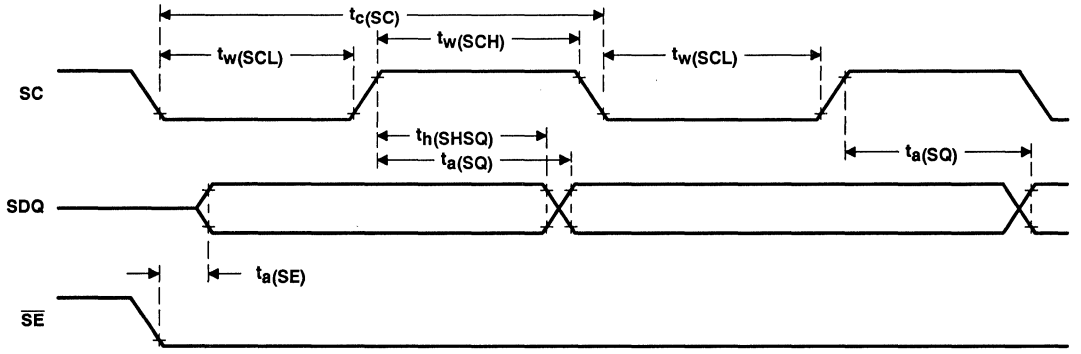


Figure 22. Serial Data-In Timing

The serial data-in cycle (SD) is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control or transfer write cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will not take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.



NOTE A: When the odd tap is used (tap addresses can be 0–511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.

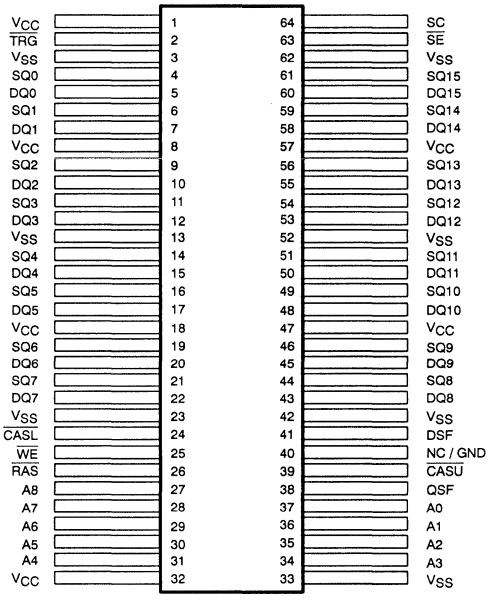
Figure 23. Serial Data-Out Timing

The serial data-out (SQ) cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

- Military Operating Temperature Range – 55°C to 125°C
- MIL-STD-883, Class B
- DRAM : 262 144 Words × 16 Bits SAM: 256 Words × 16 Bits
- Dual Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports
- Data Transfer Function From the DRAM to the Serial Data Register
- (4 × 4) × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register
- Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design
- Byte Write Control ($\overline{CASL}$, $\overline{CASU}$) Provides Flexibility
- Enhanced Page Mode Operation for Faster Access
- $\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes
- Long Refresh Period: Every 8 ms (Max)
- Up to 33-MHz Uninterrupted Serial Data Streams
- 256 Selectable Serial Register Starting Locations
- $\overline{SE}$ Controlled Register Status Signal
- Split Serial-Data Register for Simplified Realtime Register Reload
- 3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams
- All Inputs/Outputs and Clocks TTL Compatible
- Texas Instruments EPIC™ CMOS Process
- Designed to Work With the Industry-Leading Texas Instruments Graphics Family
- Ceramic Package:
  - 0.5-mm Fine Pitch Brazed Flatpack With Non-Conductive Tie-Bar
  - Pin Grid Array
- Performance:

HKC PACKAGE† (TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WE}$	DRAM Write Enable Selects
DSF	Special Function Select
QSF	Special Function Output
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: Not Connected Internally to V_{SS})

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(rd\ W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)
SMJ55160	80 ns	25 ns	150 ns	50 ns	30 ns

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PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

- **Military Operating Temperature Range – 55°C to 125°C**
- **MIL-STD-883, Class B**
- **DRAM : 262 144 Words × 16 Bits SAM: 256 Words × 16 Bits**
- **Dual Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{WEL}$, $\overline{WEU}$) Provides Flexibility**
- **Enhanced Page Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **Long Refresh Period: Every 8 ms (Max)**
- **Up to 33-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial Register Starting Locations**
- **$\overline{SE}$ Controlled Register Status Signal**
- **Split Serial-Data Register for Simplified Realtime Register Reload**
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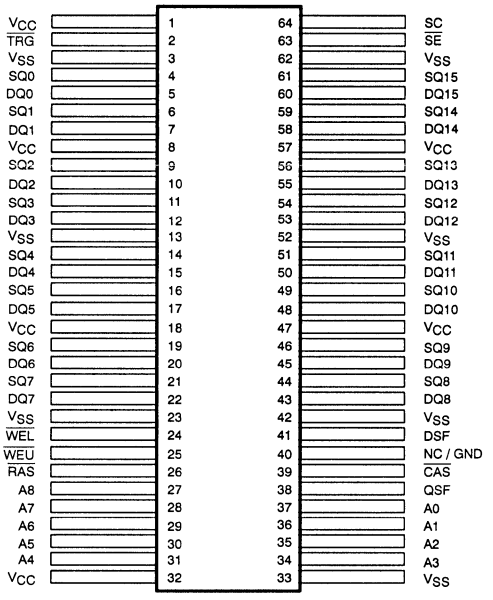
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Ceramic Package:**
  - **0.5-mm Fine Pitch Brazed Flatpack With Non-Conductive Tie-Bar**
  - **Pin Grid Array**
- **Performance:**

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(rd\ W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)
SMJ55165	80 ns	25 ns	150 ns	50 ns	30 ns

HKC PACKAGE
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
SQ0 –SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WEU}$, $\overline{WEL}$	DRAM Write Enable Selects
DSF	Special Function Select
QSF	Special Function Output
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: Not Connected Internally to V_{SS})

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

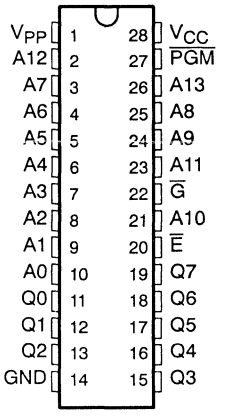
SGMS006C–AUGUST 1986–REVISED FEBRUARY 1993

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **Processed to MIL-STD-883, Class B**
- **Organization . . . 16K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 64K and 128K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

V_{CC} ± 5%	V_{CC} ± 10%	
'27C128-120		120 ns
	'27C128-15	150 ns
	'27C128-17	170 ns
	'27C128-20	200 ns
	'27C128-25	250 ns
	'27C128-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffer**
- **Low Power Dissipation**
  - **Active . . . 138 mW Worst Case**
  - **Standby . . . 1.7 mW Worst Case (CMOS-Input Levels)**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**

J PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q0–Q7	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12–13-V Power Supply

description

The SMJ27C128 series are 131 072-bit, ultraviolet-light erasable, electrically programmable read-only memory. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C128 is pin compatible with 28-pin 128K ROMs and EPROMs. They are offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from −55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. The Fast programming algorithm uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of two seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation for the SMJ27C128 are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
G (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q0–Q7 (11–13, 15–19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	83

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C128s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C128, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q0 through Q7.

latchup immunity

Latchup immunity on the SMJ27C128 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family,"* available through TI Field Sales Offices.

powerdown

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high input signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C128 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C128, the window should be covered with an opaque label.

SNAP! Pulse programming

The 128K EPROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of two seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{PGM}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

fast programming

The 128K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q0 through Q7. Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6 V, $\overline{G}$ = V_{IH}, $\overline{PGM}$ = V_{IL}, and $\overline{E}$ = V_{IL}. More than one SMJ27C128 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q0–Q7; A0 = V_{IH} accesses the device code, which is output on Q0–Q7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q7. The manufacturer code for these devices is 97, and the device code is 83.

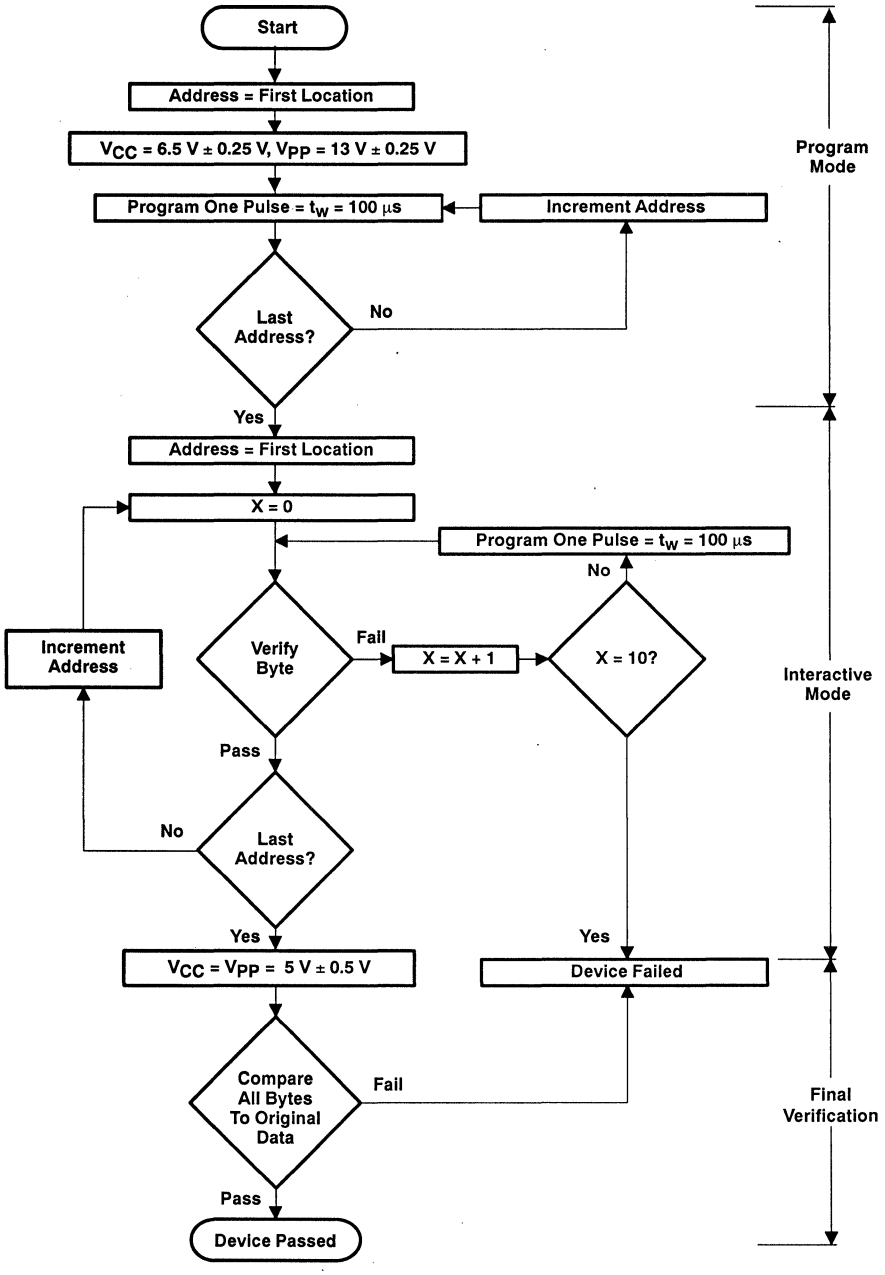


Figure 1. SNAP! Pulse Programming Flowchart

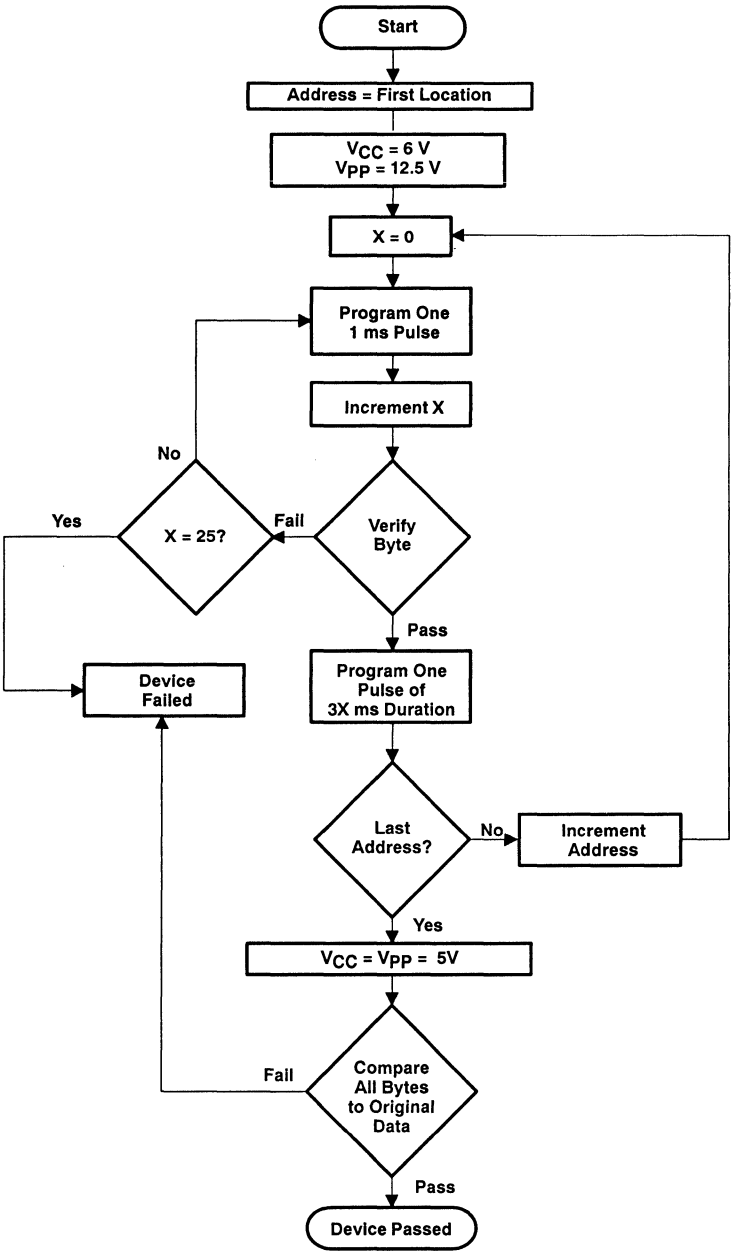
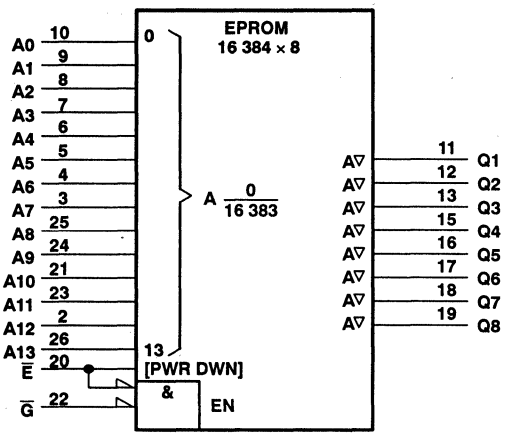


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... −55° C
Maximum operating case temperature ..... 125° C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				'27C128-120			'27C128-15 '27C128-17 '27C128-20 '27C128-25 '27C128-30			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
		Fast programming algorithm		5.75	6	6.25	5.75	6	6.25	V
		SNAP! Pulse programming algorithm		6.25	6.50	6.75	6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		$V_{CC}-0.6$		$V_{CC}+0.6$	$V_{CC}-0.6$		$V_{CC}+0.6$	V
		Fast programming algorithm		12	12.5	13	12	12.5	13	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		TTL	−0.5		0.8	−0.5		0.8	V
			CMOS	−0.5		0.2	−0.5		0.2	V
T_A	Operating free-air temperature			−55			−55			°C
T_C	Operating case temperature					125			125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -400$ mA	2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O = 0$ to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V			100	µA
I_{PP2}	V_{PP} supply current‡ (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	µA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			300	µA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		10	25	mA

† Typical values are at $T_A = 25°C$ and nominal voltages.
‡ This parameter has been characterized at 25°C and is not tested.

capacitance§

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$, f = 1 MHz		6	10	pF
C_O	Output capacitance	$V_O = 0$, f = 1 MHz		8	14	pF

† Typical values are at $T_A = 25°C$ and nominal voltages.
§ Capacitance measurements are made on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-120		'27C128-15		'27C128-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		120		150		170	ns
$t_{a(E)}$	Access time from chip enable			120		150		170	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		70		70	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-20		'27C128-25		'27C128-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not production tested.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
t_{dis}	Output disable time from $\overline{G}$		0		130	ns
t_{enG}	Output enable time from $\overline{G}$				150	ns
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs

NOTES: 4. For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2.0 V for logic high and 0.8 V for logic low for both inputs and outputs.
5. Common test conditions apply for t_{dis} except during programming.

PARAMETER MEASUREMENT INFORMATION

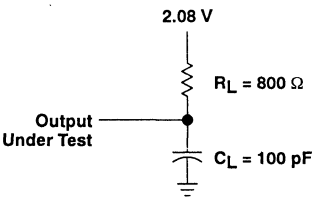
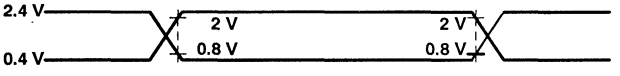


Figure 3. Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

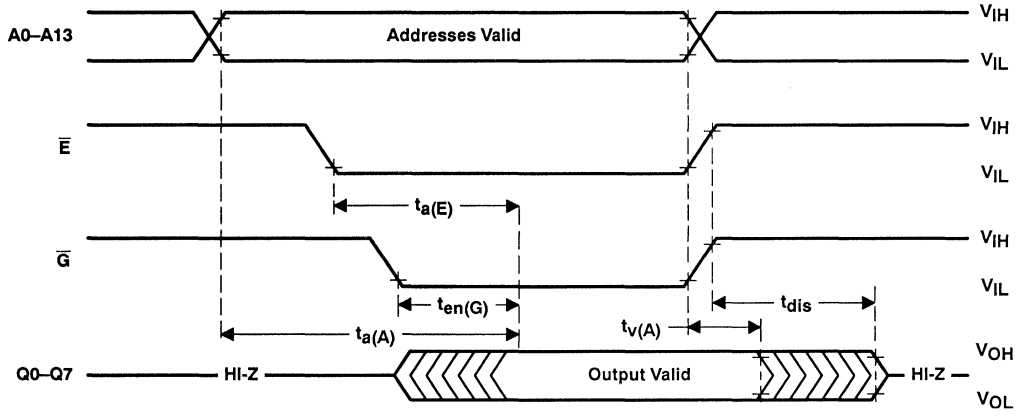


Figure 4. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

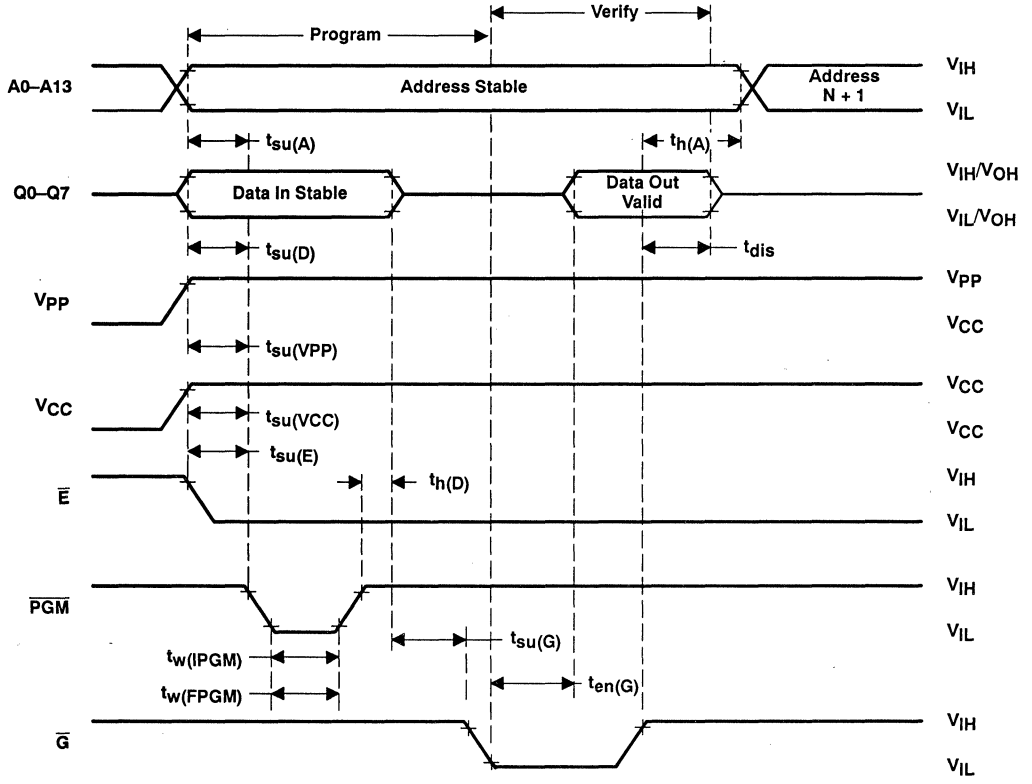


Figure 5. Program Cycle Timing

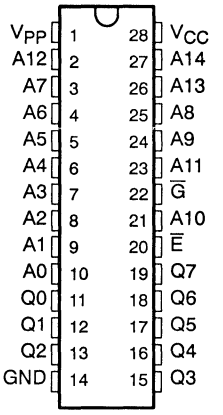
SGMS005D–MAY 1986–REVISED FEBRUARY 1993

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **MIL-STD-883C Class B High-Reliabillity Processing**
- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 128K and 256K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

'27C256-15	150 ns
'27C256-17	170 ns
'27C256-20	200 ns
'27C256-25	250 ns
'27C256-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **400 mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Low Power Dissipation**
  - **Active . . . 138 mW Worst Case**
  - **Standby . . . 1.7 mW Worst Case (CMOS Input Levels)**

J PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	5-V Power Supply
V_{PP}	Output Enable

description

The SMJ27C256 series are 262 144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C256 is pin compatible with 28-pin 256K ROMs and EPROMs. They are offered in a 600 mil dual-in-line ceramic package (J suffix) rated for operation from –55°C to 125°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other 12–13 V supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. The Fast programming algorithm uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation for the SMJ27C256 are listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTION (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q0–Q7 (11–13, 15–19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	04

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C256, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q0 through Q7.

latchup immunity

Latchup immunity on the SMJ27C256 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001; *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family."*

powerdown

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 300 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C256 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0s (lows) are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light.The recommended minimum exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C256, the window should be covered with an opaque label.

SNAP! Pulse programming

The 256K EPROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of 4 seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH} and $\overline{E}$ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

fast programming

The 256K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6 V, $\overline{G}$ = V_{IH} and $\overline{E}$ = V_{IL}. More than one SMJ27C256 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Fast programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V and V_{PP} = 12.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q0–Q7; A0 = V_{IH} accesses the device code, which is output on Q0–Q7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q7. The manufacturer code for these devices is 97, and the device code is 04.

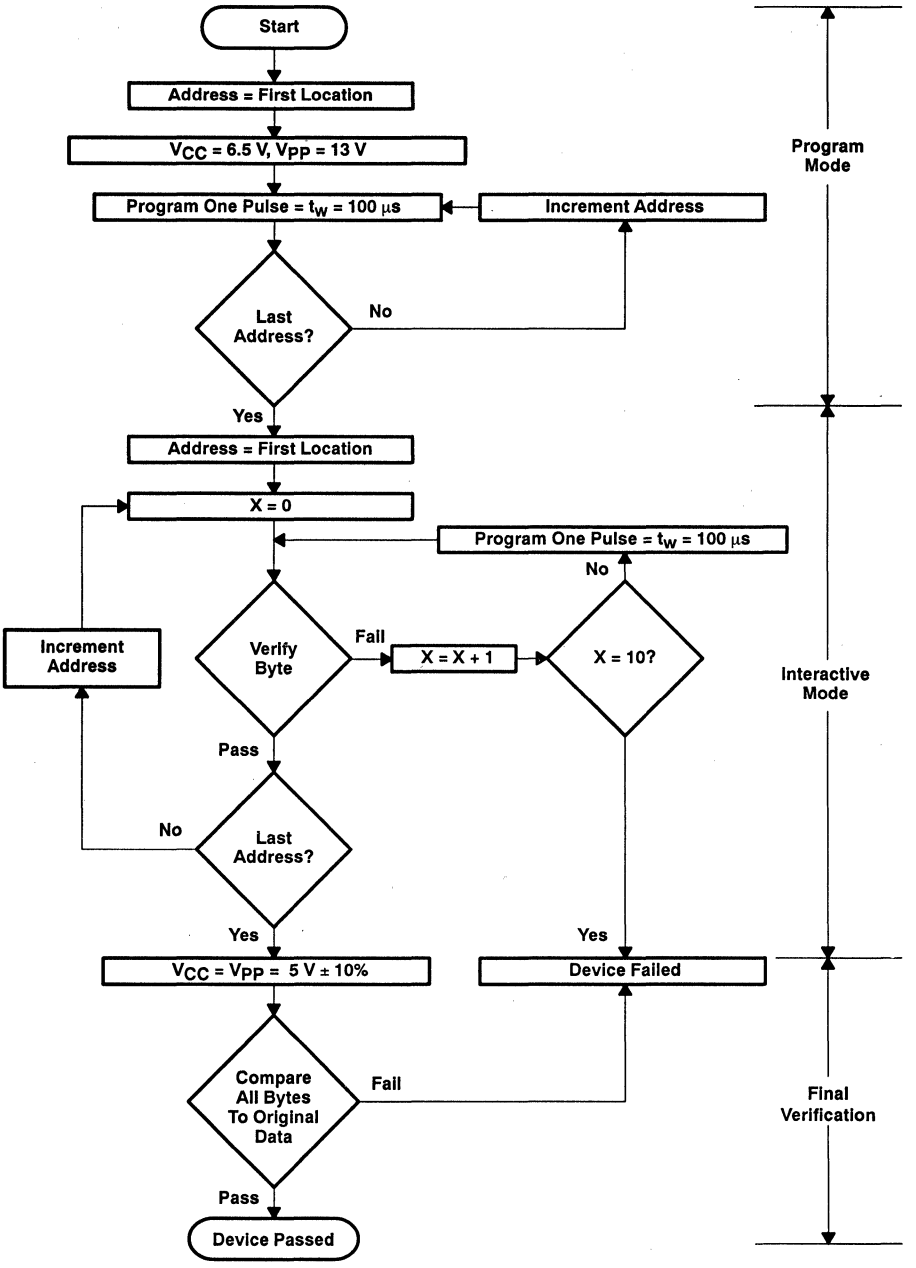


Figure 1. SNAP! Pulse Programming Flowchart

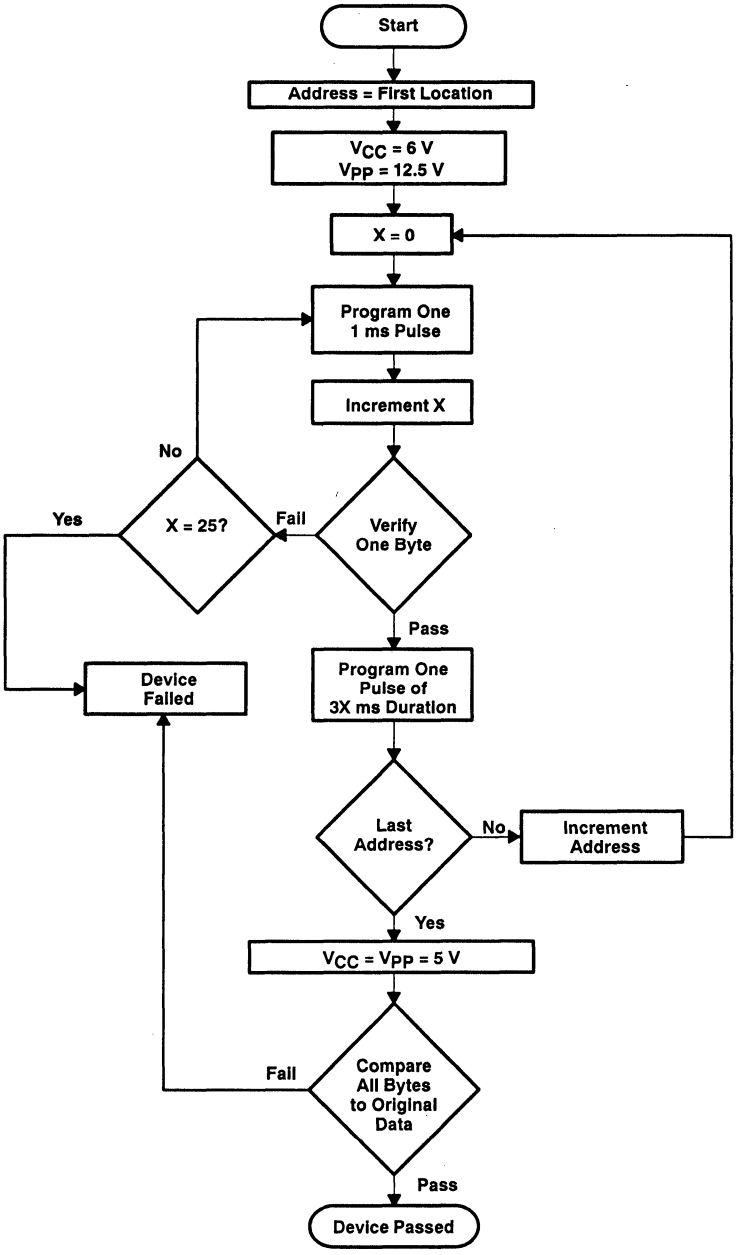
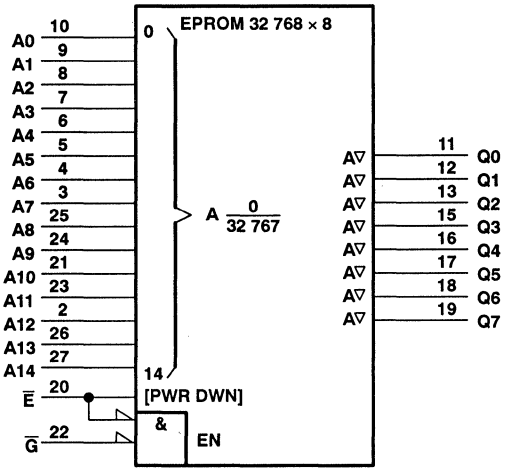


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... −55°C
Maximum operating case temperature ..... 125°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER				MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	Read mode (see Note 2)		4.5	5	5.5	V
		Fast programming algorithm		5.75	6	6.25	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply Voltage	Read mode (see Note 3)				$V_{CC}-0.6$	V
		Fast programming algorithm		12	12.5	13	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage (see Note 4)		TTL	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage (see Note 4)		TTL	−0.5		0.8	V
			CMOS	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (see Note 4)		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage (see Note 4)		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage) (see Note 4)		V_I = 0 to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V			100	μA
I_{PP2}	V_{PP} supply current‡ (during program pulse) (see Note 4)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply curent (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	μA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			300	
I_{CC2}	V_{CC} supply current (active) (see Note 4)		V_{CC} = 5.5 V, E = V_{IL}, t_{cycle} = minimum cycle time, outputs open		10	25	mA
I_{OS}	Output short circuit current (see Note 5)					100	mA

† Typical values are at T_A = 25°C and nominal voltages.
‡ This parameter has been characterized at 25°C and is not tested.

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}.
4. Valid during programming mode also.
5. V_{PP} may be one diode drop below V_{CC}. It may be connected to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and be removed simultaneously or after V_{PP}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 6 and 7)

PARAMETER		TEST CONDITIONS (SEE NOTES 6 AND 7)	'27C256-15		'27C256-17		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		150		170	ns
$t_{a(E)}$	Access time from chip enable			150		170	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			70		70	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first §		0	55	0	55	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first §		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 6 AND 7)	'27C256-20		'27C256-25		'27C256-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first §		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first §		0		0		0		ns

§ Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested. Timing measurements are made at 2.0 V for logic high and 0.8 V for logic low for both inputs and outputs.

NOTES: 6. For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V.
7. Common test conditions apply to t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 (SNAP! Pulse), T_A = 25°C (see Note 6)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
t_{dis}	Output disable time from $\overline{G}$		0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$				150	ns
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs

NOTE 6: For all switching characteristics and timing measurements, the input pulse levels are 0.4 V to 2.4 V.

PARAMETER MEASUREMENT INFORMATION

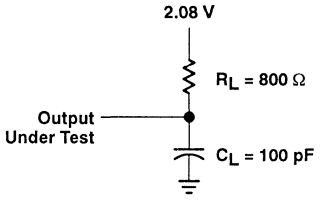
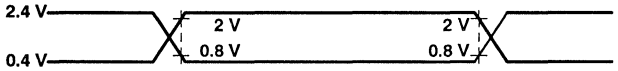


Figure 3. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

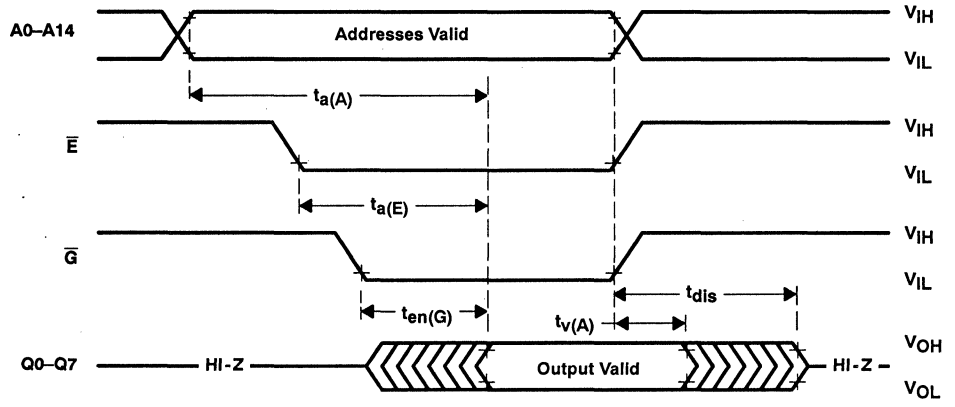
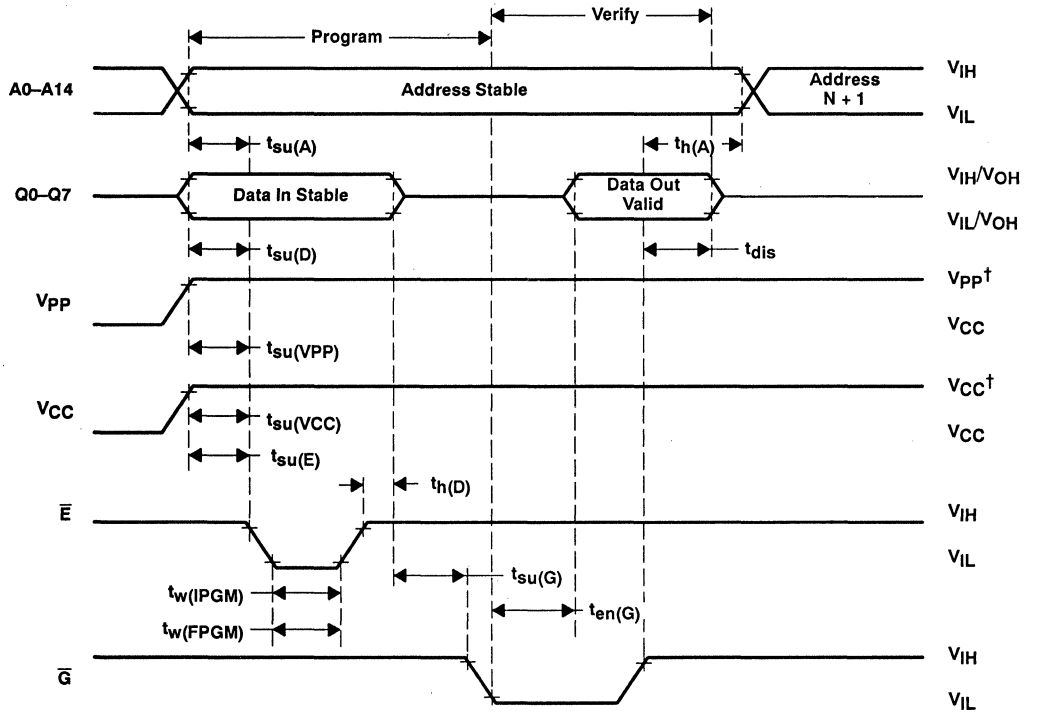


Figure 4. Read Cycle Timing



† 12.5-V V_{PP} and 6-V V_{CC} for Fast programming, 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 5. Program Cycle Timing

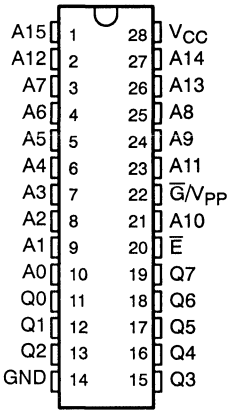
SGMS019B–SEPTEMBER 1987–REVISED FEBRUARY 1993

- **Military Operating Temperature Range . . . – 55°C to 125°C**
- **Processed to MIL-STD-883C, Class B**
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 512K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**

'27C512-20	200 ns
'27C512-25	250 ns
'27C512-30	300 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Low Power Dissipation**
  - **Active . . . 275 mW (Max)**
  - **Standby . . . 1.9 mW (Max) (CMOS Input Levels)**

J PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
GND	Ground
Q0–Q7	Outputs
V_{CC}	5-V Power Supply
$\overline{G}/V_{PP}$	Output Enable
GND	Ground

description

The SMJ27C512 series are 524 288-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors, and each output can drive one Series 54 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The SMJ27C512 is pin compatible with existing 28-pin 512K ROMs and EPROMs. They are offered in a 600-mil dual-in-line ceramic package (J suffix) rated for operation from –55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other 12–13 V supply is needed for programming, but all programming signals are TTL level. These devices are programmable by either Fast or SNAP! Pulse programming algorithms. Fast programming uses a V_{PP} of 12.5 V and a V_{CC} of 6 V for a nominal programming time of two minutes. SNAP! Pulse programming uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

The seven modes of operation for the SMJ27C512 are listed in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V for Fast, or 13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

FUNCTIN (PINS)	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}/V_{PP}$ (22)	V_{IL}	V_{IH}	X†	V_{PP}	V_{IL}	V_{PP}	V_{IL}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q0–Q7 (11–13, 15–19)	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	85

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C512, a low-level signal is applied to the $\overline{E}$ and $\overline{G}/V_{PP}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q0 through Q7.

power down

Active I_{CC} supply current can be reduced from 25 mA to 500 μA (TTL-level inputs) or 350 μA (CMOS-level inputs) by applying a high logic signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C512 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic 1 (high) state. Logic 0's (lows) are programmed into the desired locations. A programmed logic 0 (low) can be erased only by ultraviolet light. The recommended minimum ultraviolet light exposure dose (UV intensity × exposure time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C512, the window should be covered with an opaque label.

SNAP! Pulse programming

The 512K EPROM can be programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins Q0 to Q7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{G}/V_{PP}$ = 13 V, V_{CC} = 6.5 V, and $\overline{E} = V_{IL}$. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = 5 V, $\overline{G}/V_{PP} = V_{IL}$, and $\overline{E} = V_{IL}$.

fast programming

The 512K EPROM can be programmed using the Fast programming algorithm illustrated by the flowchart in Figure 2. During Fast programming, data is presented in parallel (eight bits) on pins Q0 through Q7. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when $\overline{G}/V_{PP}$ = 12.5 V, V_{CC} = 6 V, and $\overline{E} = V_{IL}$. More than one SMJ27C512 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = 5 V (see Figure 2).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with $\overline{G}/V_{PP}$ and $\overline{E} = V_{IL}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10); i.e., A0 = V_{IL} accesses the manufacturer code, which is output on Q0–Q7; A0 = V_{IH} accesses the device code, which is output on Q0–Q7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q7. The manufacturer code for these devices is 97, and the device code is 85.

latchup immunity

Latchup immunity on the SMJ27C512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, "*Design Considerations; Latchup Immunity of the HVCMOS EPROM Family*", available through TI Sales Offices.

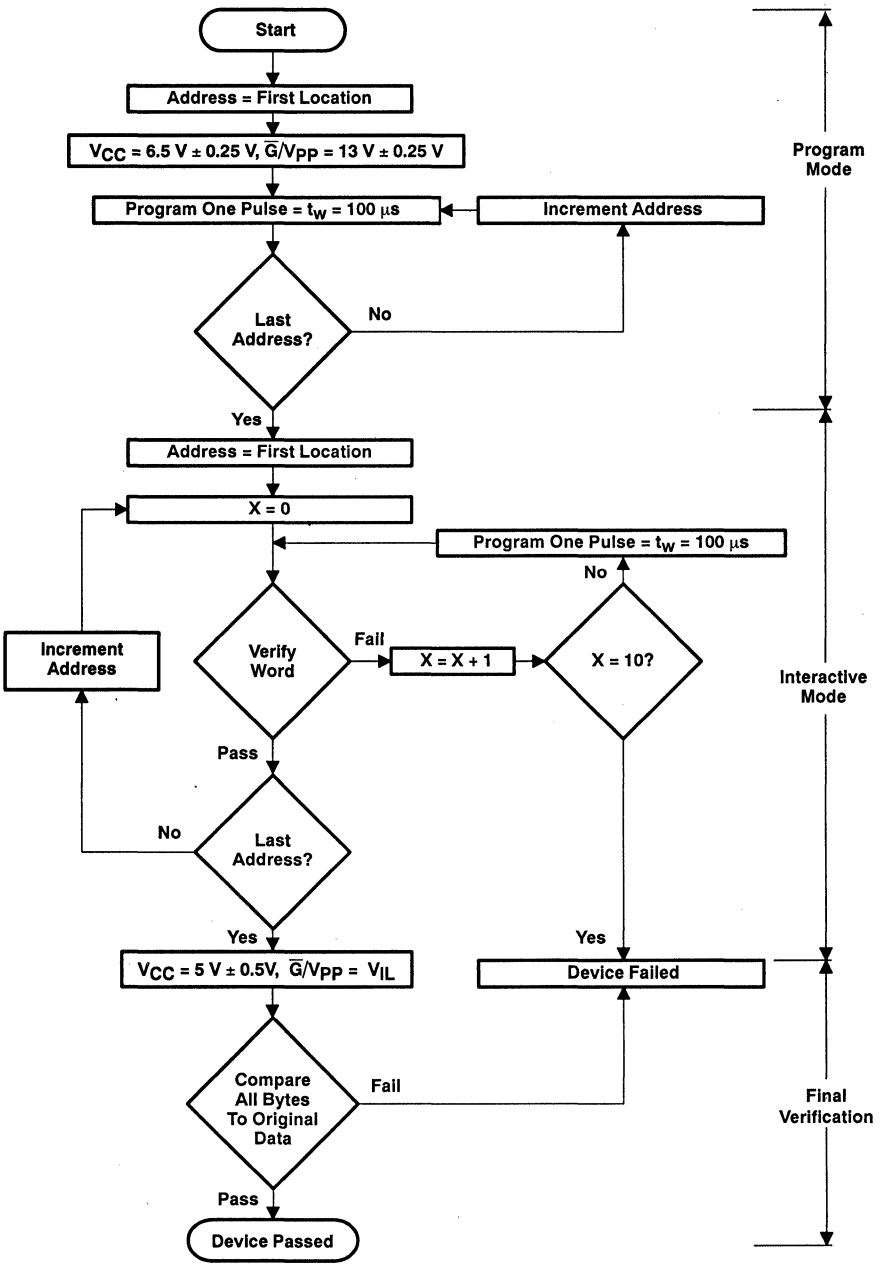


Figure 1. SNAP! Pulse Programming Flowchart

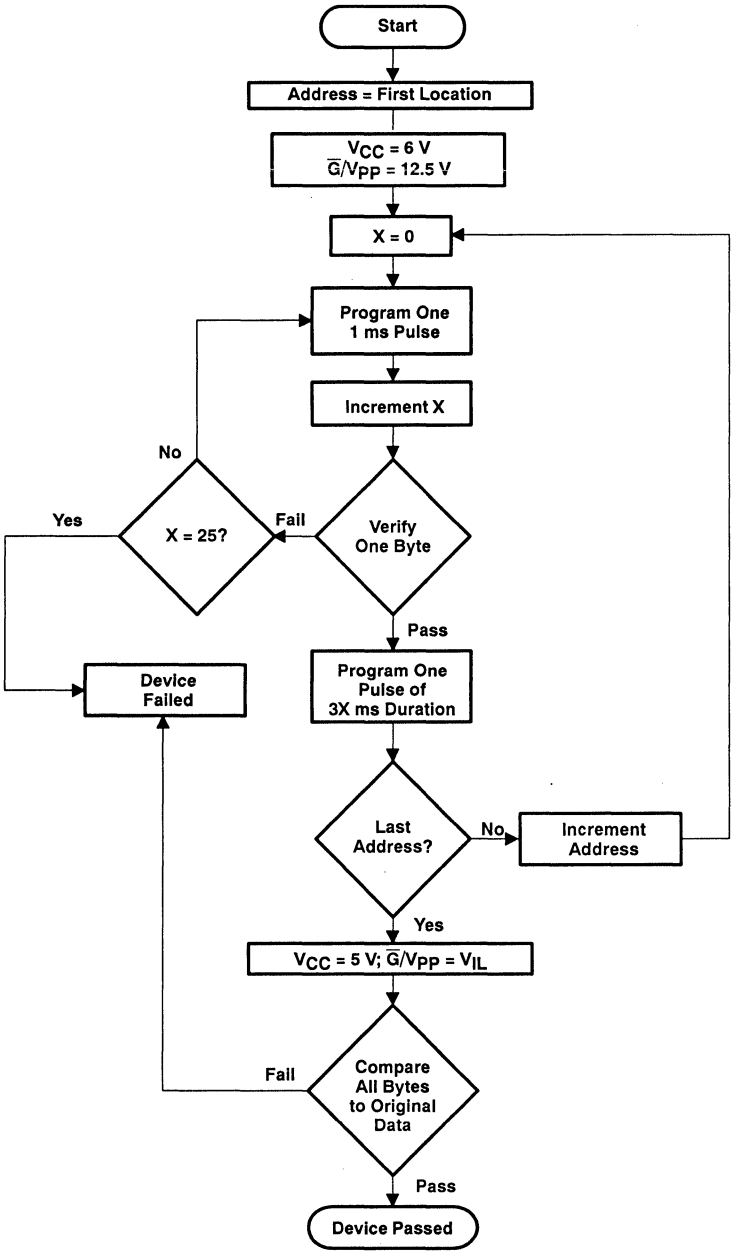
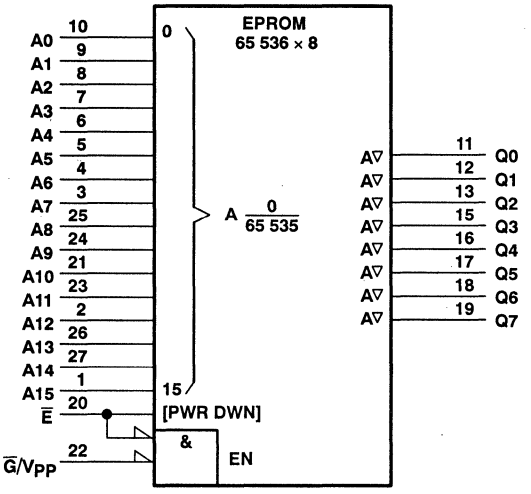


Figure 2. FAST Programming Flowchart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13.5 V
Output voltage range (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... −55°C
Maximum operating case temperature ..... 125°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				SM/SMJ27C512-20 SM/SMJ27C512-25 SM/SMJ27C512-30			UNIT
				MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	Read mode		4.5	5	5.5	V
		Fast programming algorithm		5.75	6	6.25	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
$\overline{G}/V_{PP}$	Supply voltage (see Note 3)	Fast programming algorithm		12	12.5	13	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		TTL	−0.5		0.8	V
			CMOS	GND −0.2		GND +0.2	V
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as $\overline{G}/V_{PP}$ and removed after or at the same time as $\overline{G}/V_{PP}$. The device must not be inserted into or removed from the board when $\overline{G}/V_{PP}$ or V_{CC} is applied.

3. $\overline{G}/V_{PP}$ can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level ouput voltage		I_{OH} = −400 µA	2.4			V
V_{OL}	Low-level ouput voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±10	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±10	µA
I_{PP}	$\overline{G}/V_{PP}$ supply current (during program pulse)‡		$\overline{G}/V_{PP}$ = 13 V		35	70	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}			500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}			325	µA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, E = V_{IL}, t_{cycle} = minimum cycle time, outputs open		35	50	mA

† Typical values are at T_A = 25°C and nominal voltages.

‡ This parameter has been characterized at 25°C and is not production tested.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz		6	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		8	pF
$C_{G/VPP}$	$\overline{G}/V_{PP}$ input capacitance	$\overline{G}/V_{PP}$ = 0, f = 1 MHz		20	pF

† Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	'27C512-20		'27C512-25		'27C512-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	See Figure 3		200		250		300	ns
$t_{a(E)}$	Access time from chip enable			200		250		300	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		100		120	ns
tdis	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not production tested.

recommended timing requirements for programming: V_{CC} = 6 V and V_{PP} = 12.5 V (Fast) or V_{CC} = 6.5 and V_{PP} =13 (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	Fast programming algorithm	0.95	1	1.05	ms
		SNAP! Pulse programming algorithm	95	100	105	µs
$t_{w(FPGM)}$	Final pulse duration	Fast programming only	2.85		78.75	ms
$t_{su(A)}$	Address setup time		2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$		0		130	µs
t_{EHD}	Data valid from $\overline{E}$ low				1	µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs
$t_{r(PG)G}$	V_{PP} rise time		50			ns
$t_{h(VPP)}$	V_{PP} hold time		2			µs
$t_{rec(PG)}$	V_{PP} recovery time		2			µs

NOTE 4: For all switching characteristics and timing measurements input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference page 9, AC testing waveforms).

PARAMETER MEASUREMENT INFORMATION

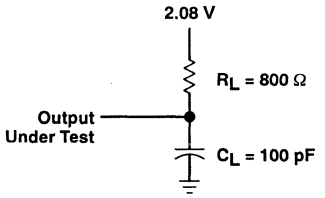
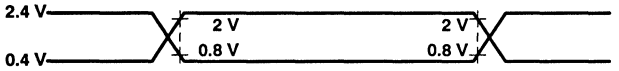


Figure 3. AC Testing Output Load Circuit

AC testing input/output wave forms



A.C. testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

PARAMETER MEASUREMENT INFORMATION

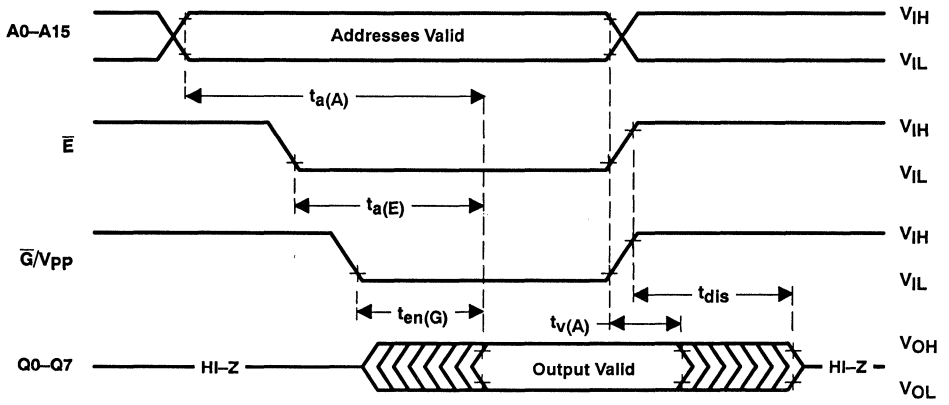
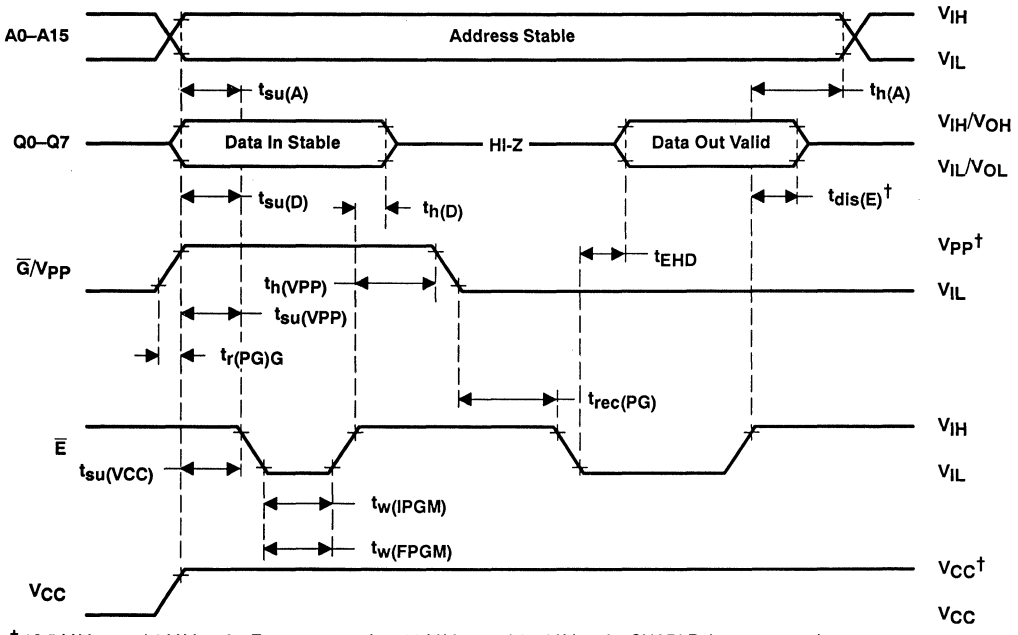


Figure 4. Read Cycle Timing

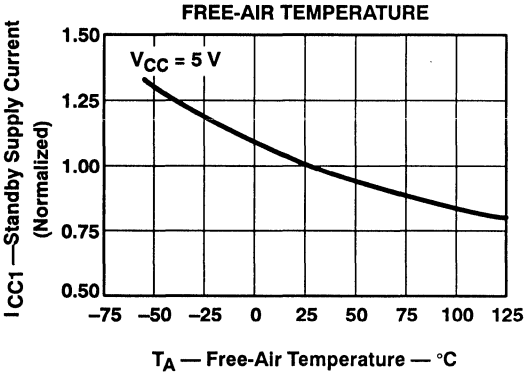


† 12.5-V V_{PP} and 6-V V_{CC} for Fast programming, 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

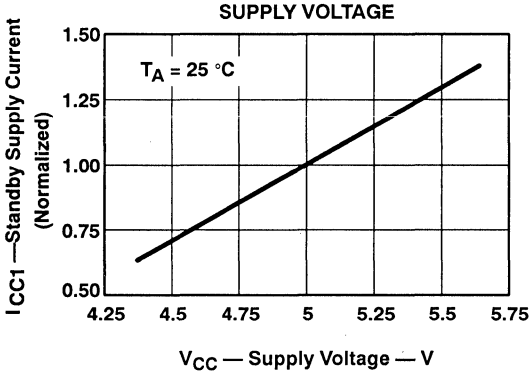
Figure 5. Program Cycle Timing

TYPICAL SMJ27C512 CHARACTERISTICS

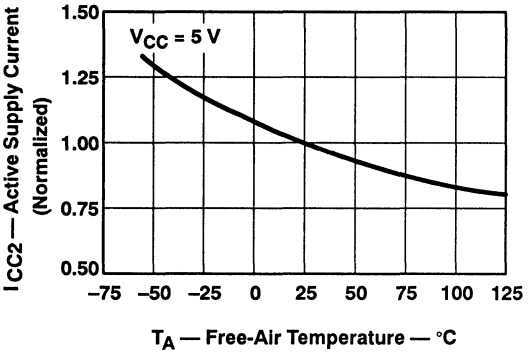
STANDBY SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



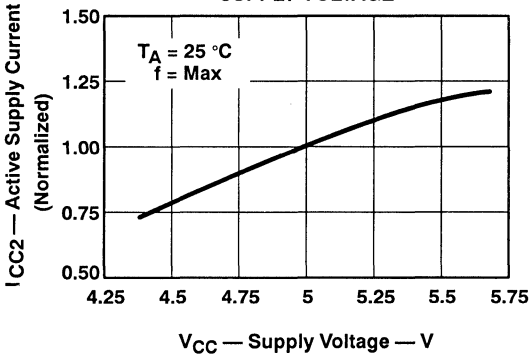
STANDBY SUPPLY CURRENT
vs
SUPPLY VOLTAGE



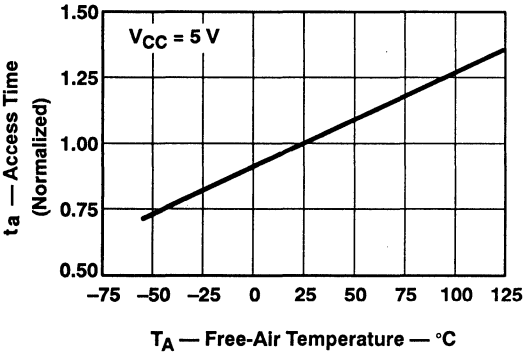
ACTIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



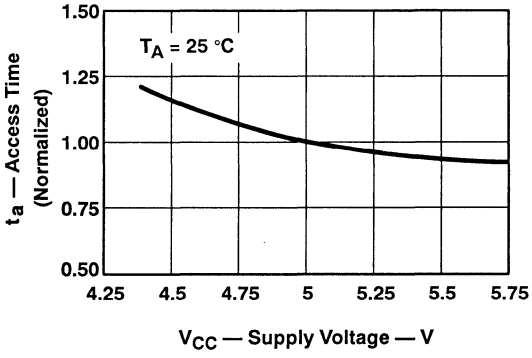
ACTIVE SUPPLY CURRENT
vs
SUPPLY VOLTAGE



ACCESS TIME
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
SUPPLY VOLTAGE



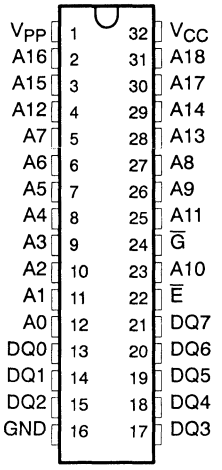
- **Military Operating Temperature Range – 55°C to 125°C**
- **Organization . . . 512K × 8**
- **Single 5-V Power Supply**
- **Industry Standard 32-Pin Dual-In-line Package**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%

'27C040-10	100 ns
'27C040-12	120 ns
'27C040-15	150 ns

- **8-Bit Output For Use in Microprocessor-Based Systems**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV DC Assured Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 385 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**

J PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
A0–A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
DQ0–DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

‡ Only in program mode.

description

The SMJ27C040 series are 4 194 304-bit, ultraviolet-light erasable, electrically programmable read-only memories.

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits. Each output can drive one Series 54. TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The SMJ27C040 is offered in a 32-pin 600-mil dual-in-line cerdip package (J suffix) rated for operation from – 55°C to 125°C.

Since this EPROM operates from a single 5-V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other (13V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The seven modes of operation are listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V), and V_H (12 V) on A9 for signature mode.

	FUNCTION						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	DQ0–DQ7
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	HI-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	HI-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	HI-Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Signature Mode	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_{IH}†	V_{IL}	MFG Code 97
						V_{IH}	Device Code 50

† X can be V_{IL} or V_{IH}
‡ V_H = 12 V ± 0.5 V

read/output disable

When the outputs of two or more SMJ27C040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins. Output data is accessed at pins Q0–Q7.

latchup immunity

Latchup immunity on the SMJ27C040 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 70 mA to 1 mA for a high TTL input on $\overline{E}$ and to 100 μA for a high CMOS input on $\overline{E}$. In this mode all outputs are in the high impedance state.

erasure (SMJ27C040)

Before programming, the SMJ27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2 . A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The SMJ27C040 and TMS27PC040 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, and $\overline{G}$ = V_{IH}. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ1 through DQ8. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IH}, and $\overline{G}$ = V_{IL}. If the correct data is not read, the programming is performed by pulling $\overline{G}$ high, then $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with V_{CC} = V_{PP} = 5 V ± 10%.

program inhibit

Programming may be inhibited by maintaining high level inputs on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits may be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the SMJ27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown by the signature mode table below.

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

† $\overline{E}$ = $\overline{G}$ = V_{IL}, A1–A8 = V_{IL}, A9 = V_H, A10–A18 = V_{IL}, V_{PP} = V_{CC}.

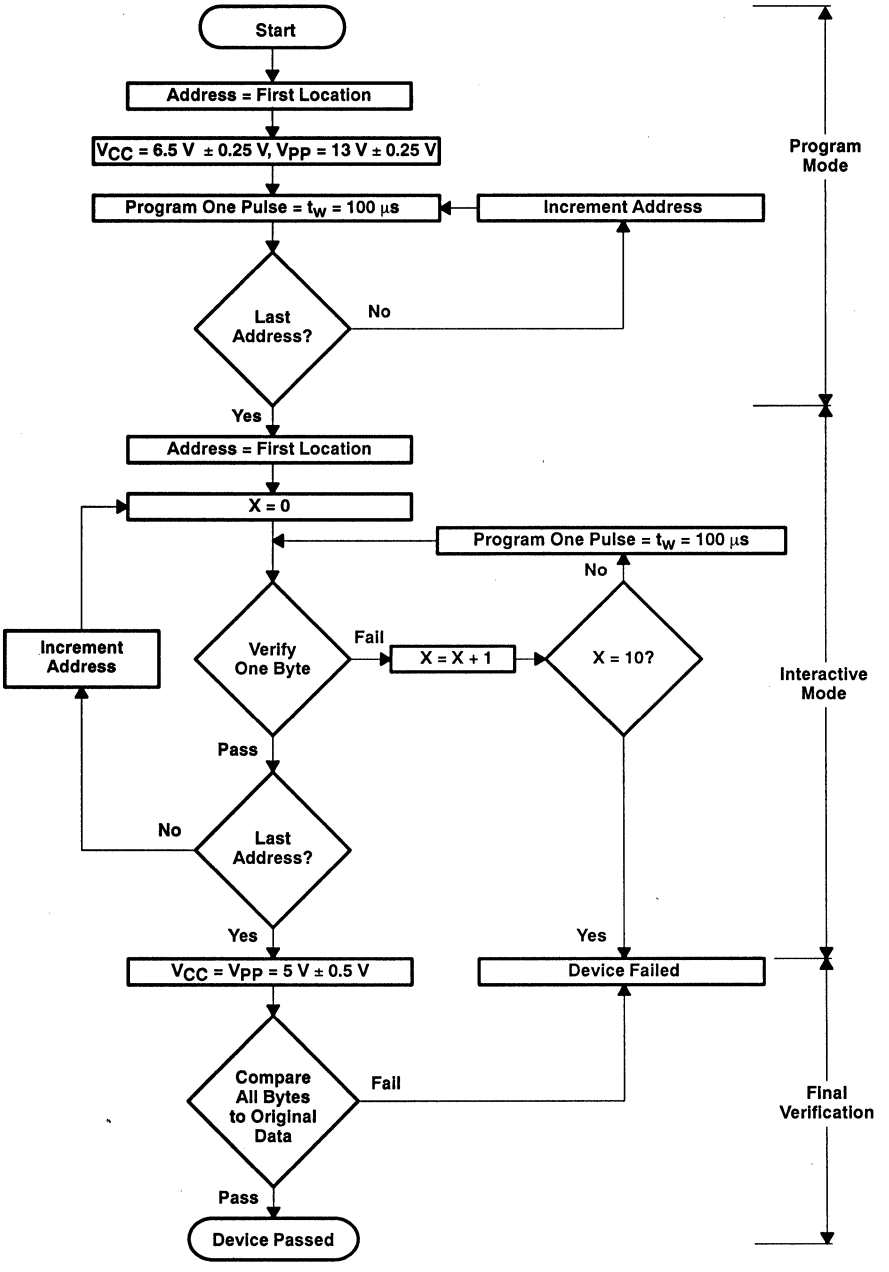
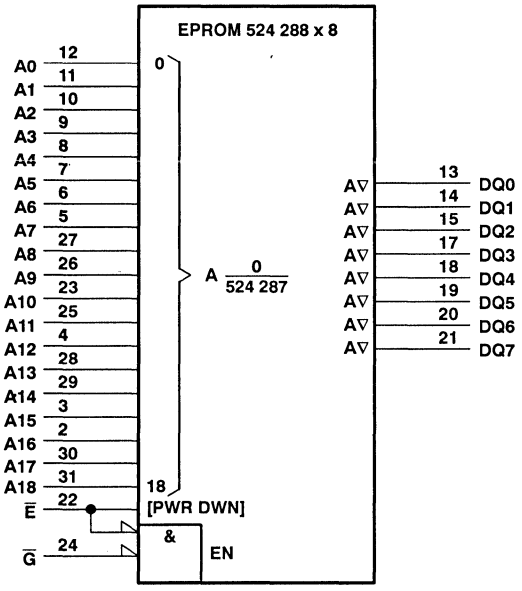


Figure 1. SNAP! Pulse Programming Flow Chart

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... −0.6 V to 14 V
Input voltage range (see Note 1), All inputs except A9 ..... −0.6 V to 6.5 V
A9 ..... −0.6 V to 13 V
Output voltage range, with respect to V_{SS} (see Note 1) ..... −0.6 V to V_{CC} + 1 V
Minimum operating free-air temperature ..... −55°C
Maximum operating case temperature ..... 125°C
Storage temperature range ..... −65°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	8	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 2)		V_{CC} − 0.6		V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} − 0.2		V_{CC}+0.5	
V_{IL}	Low-level input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 400 μA	2.4		V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA		0.4	V
I_I	Input current (leakage)		V_I = 0 to 5.5 V		±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	μA
I_{PP2}	V_{PP} supply current (during program pulse)‡		V_{PP} = 12.75 V, T_A – 25°C		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		CMOS-Input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	μA
I_{CC2}	V_{CC} supply current (active)		$\overline{E}$ = V_{IL}, V_{CC} = 5.5 V t_{cycle} = minimum cycle time, outputs open†		50	mA

† Minimum cycle time = maximum access time.
‡ This parameter is only sampled and not 100% tested.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz§ (V_{CC} = V_{PP} = 5 V ± 0.5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP¶	MAX	UNIT
C_i	Input capacitance	V_I = 0		4	8	pF
C_O	Output capacitance	V_O = 0		8	12	pF

§ Capacitance is sampled only at initial design and after any major change.
¶ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTE 4 AND 5)	'27C040-10		'27C040-12		'27C040-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	(see Figure 2) Input t_r ≤ 20 ns Input t_f ≤ 20 ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first#		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first#		0		0		0		ns

Value calculated from 0.5-V delta to measured output level. This parameter is only sampled and not 100% tested.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (Figure 2)
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 6)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C, (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2			µs
$t_{su(E)}$	$\overline{E}$ setup time		2			µs
$t_{su(G)}$	$\overline{G}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic logic low. (Figure 2)

PARAMETER MEASUREMENT INFORMATION

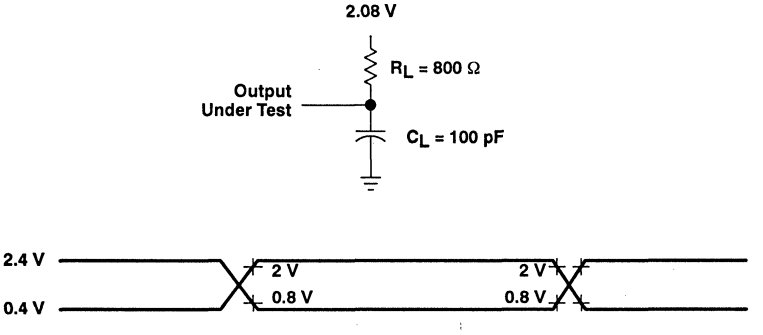


Figure 2. Output Load Circuit and Input/Output Wave Forms

PARAMETER MEASUREMENT INFORMATION

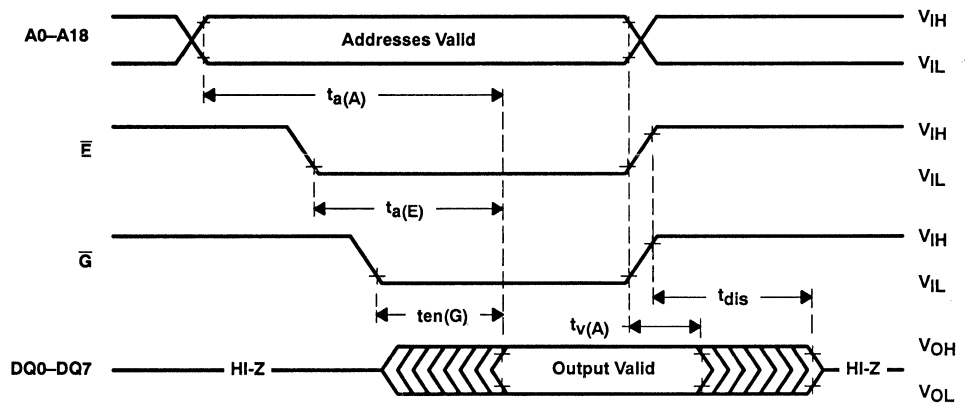
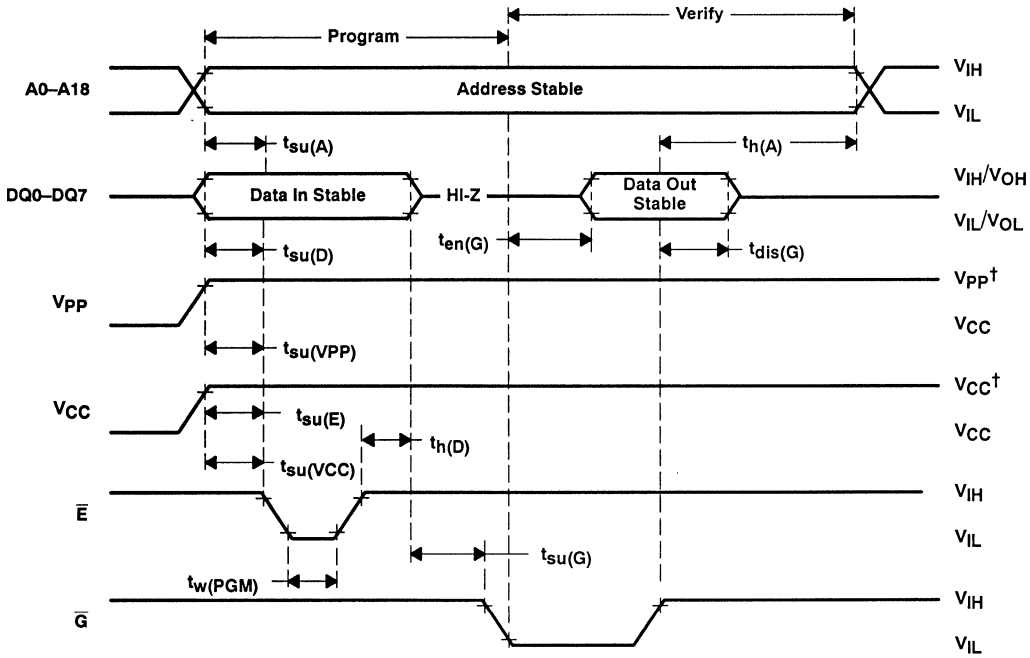


Figure 3. Read Cycle Timing

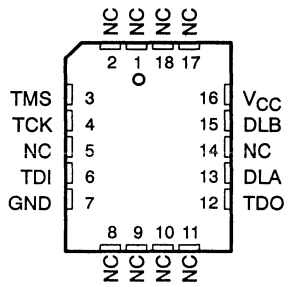


† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

- **Member of Texas Instruments SCOPE™ Family of Testability Products**
- **IEEE 1149.1 Serial Test Bus Compatible**
- **Organization . . . 2048 x 8-Bit Flash Memory**
- **TCK Frequency (V_{CC} ± 10%)**
  '29F816-06 . . . 6.25 MHz
- **5-V Program/Erase/Read Operation**
- **4 Flash-Erasable Blocks (128, 384, 512, and 1024-Byte Size)**
- **Software Sequence Write/Erase Protection**
- **Lockbits**
- **Self-Timed Write/Erase Cycles**
- **Streaming Read/Write Modes**
- **32-Byte Page Programming Mode**
- **CMOS Technology**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **18-Pin Leadless-Ceramic Chip Carrier Package (FG Suffix)**
- **Operating Free-Air Temperature Range – 55°C to 125°C**

FG PACKAGE†
(TOP VIEW)



† Package is shown for pinout reference only.

PIN NOMENCLATURE	
TMS	Test Mode Select
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
DLA	Disable Lock A
DLB	Disable Lock B
V_{CC}	5-V Power Supply
GND	Ground
NC	No internal connection

description

The SCOPE Diary is a 16 384-bit, programmable storage device that can be electrically block-erased and reprogrammed. The SCOPE Diary is fabricated using HVCMOS FLOTOX technology for high reliability and very low power dissipation. It performs the erase/program operations automatically with a single 5-V supply voltage, and it can program a single byte or up to 32 bytes in one cycle.

All SCOPE Diary operations are accomplished via a 4-wire Test Access Port (TAP) interface. This interface complies with the IEEE 1149.1 Serial Test Bus standard (JTAG). The interface consists of two control signals: Test Mode Select (TMS) and Test Clock (TCK); and two test data pins: Test Data In (TDI) and Test Data Out (TDO). The JTAG Test Access Protocol defines how this 4-wire test bus is used to scan in instructions and data, execute instructions, and scan out the resulting data.

All test information is serially loaded into the chip via TDI and out of the chip via TDO. Three mandatory JTAG components are added to the Flash EEPROM array: a TAP controller, a set of test data registers, and an instruction register.

The TAP controller interfaces both the test data registers and the instruction register to the 4-wire test bus. The test data registers load and/or capture test data. The instruction register selects the test data register(s) to be accessed and the test to be performed. There are three types of test data registers: the Data Scan Registers (DSR), the Bypass Register (BR), and the Device Identification Register (IDR).

SCOPE is a trademark of Texas Instruments Incorporated.

The SCOPE Diary is divided into four independently flash-erasable blocks. These blocks are configured as 128, 384, 512, and 1024 bytes in size. These blocks can be prevented from being programmed or erased by programming any or all of the four write-once lockbits.

The SCOPE Diary features internal circuitry for self-timed programming, self-timed erasing, and completion polling. In the erased state, all bits are at a logical 1. To reprogram, all memory bits in a selected block are erased first, and then those bits (now logical 1s) are programmed accordingly. The SCOPE Diary supports a page programming mode that allows programming of up to 32 bytes in one cycle. During programming and erasing, the completion status is available, allowing the system to begin a new operation before the maximum specified timeout.

An on-chip power supply reference comparator protects the SCOPE Diary from write and erase commands during power up and power down. During normal operation, software sequences protect against inadvertent program and erase commands.

The SCOPE Diary is offered in an 18-pin leadless ceramic chip carrier package (FG suffix). It is characterized for operation from – 55°C to 125°C.

The SCOPE Diary is available in a 1000-cycle endurance version.

terms

clock

The term *clock* refers to the system test clock used by the controller and its target(s). The clock is input on TCK.

DMA

The SCOPE Diary supports the Direct Memory Access (DMA) extension to the 1149.1 standard. The DMA mode enables a continuous stream of bits to be scanned in or out of the SCOPE Diary.

host

The term *host* refers to the device directing the activity of the SCOPE Diary.

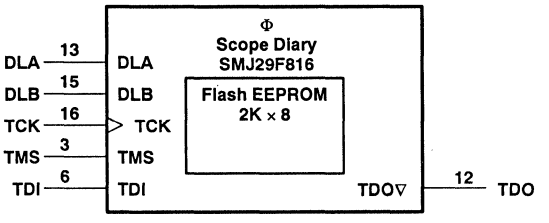
JTAG

The Joint Test Action Group (JTAG) is the originator of IEEE Standard 1149.1.

SCOPE

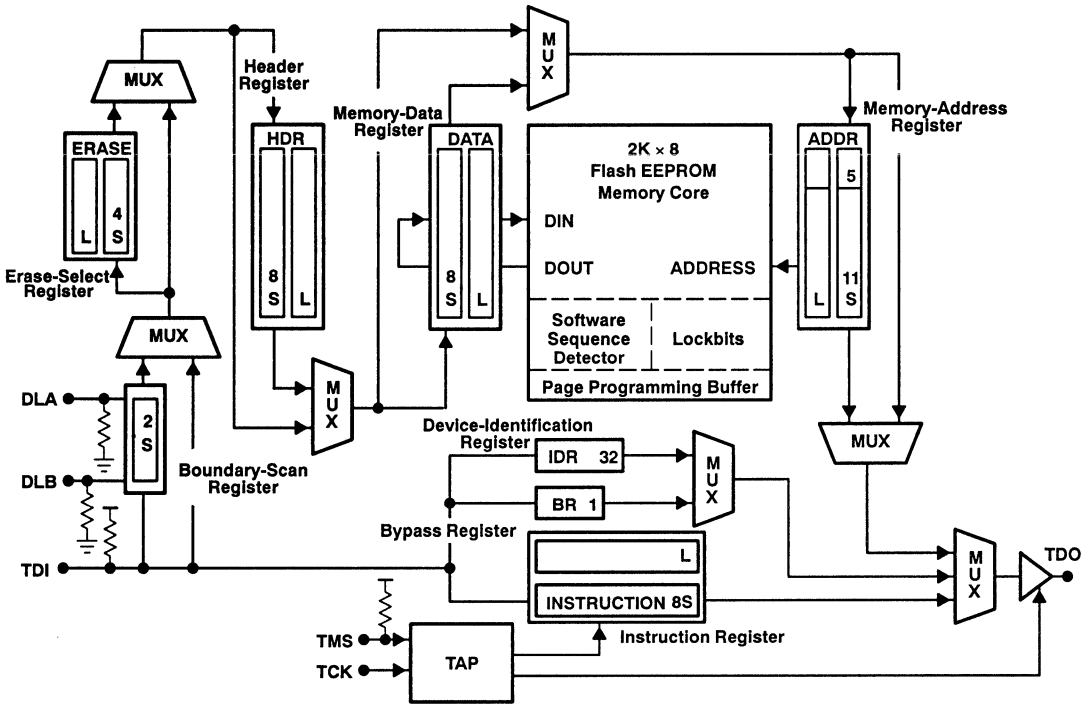
System Controllability and Observability Partitioning Environment (SCOPE) is the family name for Texas Instruments testability products.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12-1991.

functional block diagram



Terminal Functions

Pin Name	Pin #	I/O	Description
TMS	3	I	Test Mode Select. Controls transition of TAP finite state machine. This input is sampled on the rising edge of TCK.
TCK	4	I	Test Clock. Input clock to TAP finite state machine. All changes in state are synchronous to the test clock TCK.
TDI	6	I	Test Data In. Data input to the internal register scan path. Data on this pin is sampled on the rising edge of TCK.
TDO	12	O	Test Data Out. Data output from the internal register scan path. Data is updated on this pin on the falling edge of TCK.
DLA	13	I	Disable Lock A. Controls lockbit functionality for memory array block 0. When DLA = V_{IL}, the state of lockbit 0 (LCK0) determines whether block 0 can be erased or programmed. When DLA = V_{IH}, block 0 can be erased or programmed regardless of the state of lockbit 0. When DLA = V_H ($V_H >> V_{CC}$), the SCOPE Diary enters a special manufacturing test mode.
DLB	15	I	Disable Lock B. Controls lockbit functionality for memory blocks 1, 2, and 3. When DLB = V_{IL}, the states of lockbits 1, 2, and 3 (LCK1, LCK2, LCK3) determine whether their respective blocks (1, 2, and 3) can be erased or programmed. When DLB = V_{IH}, blocks 1, 2, and 3 can be erased or programmed, regardless of the state of their associated lockbits.
V_{CC}	16	I	5-V Power Supply. (± 10% operating power supply connection.)
GND	7	I	Ground reference

Internal registers

Note that the most significant bit is farthest from the output (TDO) in all internal registers.

Instruction

The instruction register is an 8-bit shift register with parallel inputs to monitor the SCOPE Diary status. The most significant bit (7) is a parity bit. The SCOPE Diary status is loaded into the instruction register during the *Capture-IR* controller state (see Figure 1). During the *Shift-IR* state, the status bits are shifted out as a new SCOPE Diary instruction is scanned into the instruction register.

Bit #	7	6	5	4	3	2	1	0
	IRP	P/EBS	SSS	LMS	VMS	P/ECES	0	1
	R-1†	R-0	R-0	R-0	R-0	R-0	R-0	R-1

†R = Read, -n = Value after reset

Bit 0: Always loaded with 1.

Bit 1: Always loaded with 0

Bit 2: **P/ECES – Program/Erase Contention Error Status**
0 = No error detected.
1 = Attempt to write to SCOPE Diary during busy state.

Bit 3: **VMS – Verify Mode Status**
0 = Normal operating mode.
1 = SCOPE Diary is in either program-verify or erase-verify mode. This bit will remain set until exit-verify software sequence is issued.

Bit 4: **LMS – Lock Mode Status**
0 = Normal operating mode.
1 = SCOPE Diary is in lockbit mode.

Bit 5: **SSS – Software Sequence Status**
0 = Normal operating mode.
1 = Valid software sequence detected. The bit will be set within 2 μs after the SCOPE Diary detects a valid software sequence. The bit will remain set until one of the following occurs:
a) The sequence timer expires.
b) The active program or erase cycle is complete.
c) The CLRSWS command is issued.

Bit 6: **P/EBS – Program/Erase Busy Status**
0 = Normal operating mode.
1 = Busy state. The SCOPE Diary is executing a self-timed program or erase operation. The bit will be set within 2 μs after the BEGOPS instruction is executed. This bit will remain set until the operation is complete.

Bit 7: **IRP – Instruction Register Parity**
All valid commands to the instruction register are even parity.
0 = Parity error detected in previously loaded instruction. The SCOPE Diary will automatically place the BYPASS register into the data register scan path.
1 = No parity error in previously loaded instruction.

Figure 1. Instruction Register Status

boundary-scan

The boundary-scan register is a 2-bit register. Bit 0 of this register is connected to DLA; bit 1 is connected to DLB. This register can only be used to sample the connected inputs; therefore, values stored in the boundary-scan register during the *Update-DR* controller state will not be applied to the internal core logic.

device-identification

The device identification register returns the following 32-bit code when interrogated with the IDCODE command: *0000102Fh*. The device ID register is selected into the scan path during power-on reset or upon entering the *Test-Logic-Reset* state.

bypass

The bypass register is a 1-bit register. It allows data to transfer from TDI to TDO in one TCK clock cycle. The bypass register is selected into the scan path when a parity error is detected during the *Shift-IR* state.

memory-data

The memory-data register is an 8-bit register used to load data into the memory array during write operations. This register is also used to sample data from the memory array during read operations. The parallel-scan load path is connected to the memory core data outputs. The output of the register latch is connected to the data input of the memory core. The operation of the register is shown in Table 1.

Table 1. Memory-Data Register Operation

Opcode	Capture-DR	Shift-DR	Update-DR
DMARD	Memory Data to Scan	Data Stream from Array	Scan to Register Latch
DMAWR	Memory Data to Scan	Data Stream to Array	Scan to Register Latch
BYTERD	Memory Data to Scan	Normal Shift Operation	Scan to Register Latch
BYTEWR	Memory Data to Scan	Normal Shift Operation	Scan to Register Latch
ISTEST	Register Latch to Scan	Normal Shift Operation	Scan to Register Latch

memory-address

The memory-address register is a 16-bit register used to address the Flash EEPROM array during read and write operations. Bits 10 – 0 are used to address the Flash memory array. Bits 14 – 0 are used to address the software sequence detector. The operation of the register is shown in Table 2.

Table 2. Memory-Address Register Operation

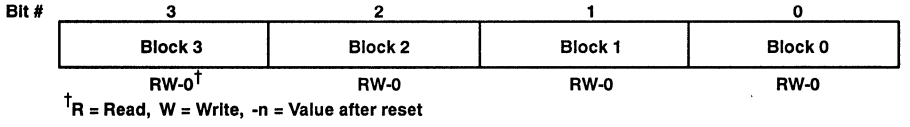
Opcode	Capture-DR	Shift-DR	Update-DR
LDADDR	Register Latch to Scan	Normal Operation	Scan to Register Latch
DMARD	Hold	Auto-Increment	Hold
DMAWR	Hold	Data Stream to Array	Hold
BYTERD	Register Latch to Scan	Normal Operation	Scan to Register Latch
BYTEWR	Register Latch to Scan	Normal Operation	Scan to Register Latch
ISTEST	Register Latch to Scan	Normal Operation	Scan to Register Latch

page programming buffer

The programming pages begin on 32-byte boundaries. Data being written to the SCOPE Diary is stored in the 32-byte page programming buffer until the memory-array programming cycle begins. The page buffer address mechanism does not automatically recognize page programming buffer loads that cross a page boundary. Bits 10 – 5 of the last address presented to the page programming buffer will be used as the page pointer when the memory array programming cycle begins. After an initial data value is loaded into the page programming buffer, all remaining bytes within the page programming buffer are initialized to FFh.

erase-select

The erase-select register is a 4-bit register used to select the Flash memory block(s) that will be erased during an erase cycle. Each bit in the register maps to one of the memory blocks (see Figure 2). To select a block for erasure, set the block's corresponding memory-control bit to logic 1. The operation of the register is shown in Table 3.



†R = Read, W = Write, -n = Value after reset

Bit 0: **Block 0 Erase Enable (address 0000 – 007F)**
0 = Erase disable
1 = Erase enable

Bit 1: **Block 1 Erase Enable (address 0080 – 01FF)**
0 = Erase disable
1 = Erase enable

Bit 2: **Block 2 Erase Enable (address 0200 – 03FF)**
0 = Erase disable
1 = Erase enable

Bit 3: **Block 3 Erase Enable (address 0400 – 07FF)**
0 = Erase disable
1 = Erase enable

Figure 2. Erase-Select Register

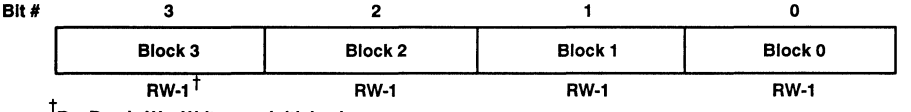
Table 3. Erase-Select Register Operation

Opcode	Capture-DR	Update-DR
ERABLK	Register Latch to Scan	Scan to Register Latch
ISTEST	Register Latch to Scan	Scan to Register Latch

lockbits

The lockbit register contains *four one-time-programmable, non-erasable bits*. The lockbits map one-to-one to the blocks in the array (bit 0 maps to block 0). The lockbit register is not located on the scan path; it is internal to the memory core. It can be accessed using the memory-address and memory-data registers.

To prevent a block from being programmed or erased, program a logic 0 in the block's corresponding bit position. Read and write operations to the lockbits are selected by the SETLOCK instruction. To program the lockbits, execute the DMAWR or BYTEWR instruction sequences while in the lock mode. The lockbit register is shown in Figure 3.



Bit 0: **Block 0 Lock Enable (address 0000 – 007F)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 1: **Block 1 Lock Enable (address 0080 – 01FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 2: **Block 2 Lock Enable (address 0200 – 03FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Bit 3: **Block 3 Lock Enable (address 0400 – 07FF)**
0 = Block program and erase disable
1 = Block program and erase enable

Figure 3. Lockbit Register

header

The header register is an 8-bit register used to control the mode of operation during a DMAWR instruction. The register is cleared to zero on power up and upon entering the *Test-Logic-Reset* state. When the register is cleared (all bits to logic 0), the SCOPE Diary uses a state-transition mode to synchronize the DMA write operation. If the register is not cleared, the contents will be used as a shift data input pattern match to synchronize the start of the DMA write operation.

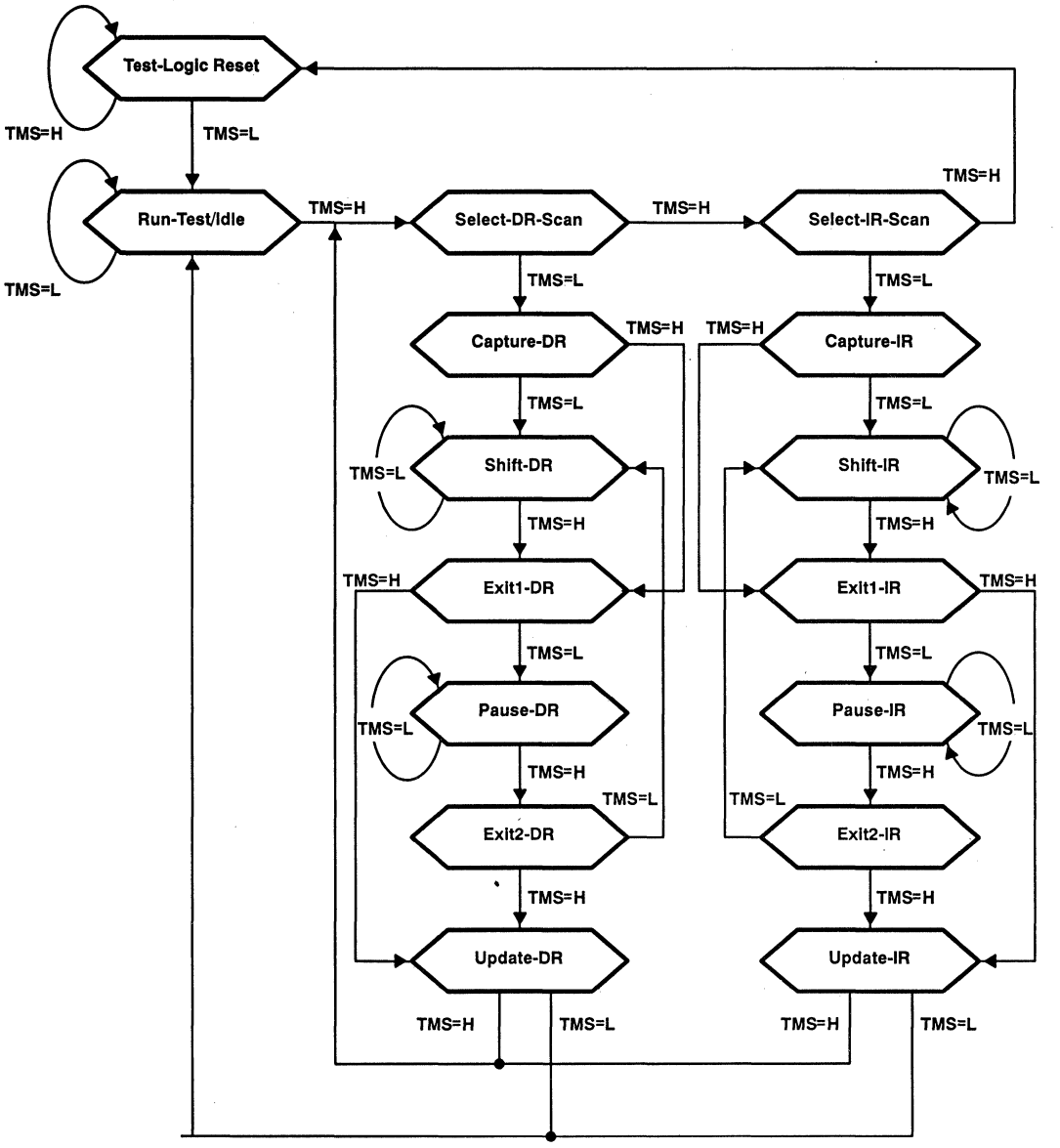


Figure 4. TAP State Diagram

TAP state diagram description (see Figure 4)

The SCOPE Diary TAP controller accepts TCK and TMS signals compatible with IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten transient states (indicated by two exiting arrows) in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any other state is a transient state.

There are two main paths through the state diagram; one accesses selected data registers, and one accesses the instruction register.

Test-Logic-Reset

In this state, the test logic is inactive, and an internal reset signal is applied to all registers in the SCOPE Diary. During SCOPE Diary operation, the TAP returns to the *Test-Logic-Reset* state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level when it is left unconnected or when a board defect causes it to be open-circuited.

Run-Test/Idle

The TAP *must* pass through this state before executing any test operations. The TAP may retain this state indefinitely. No registers are modified while the SCOPE Diary is in the *Run-Test/Idle* state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states. TAP exits them on the next TCK cycle.

Capture-DR

Selected data registers are placed in the scan path (between TDI and TDO). The current instruction determines whether or not the data is loaded or captured into the scan path. The TAP exits the state on the rising edge of TCK.

Shift-DR

In this state, data is shifted serially through the selected data registers, from TDI to TDO, on each TCK cycle. The first shift occurs after the first TCK cycle after entering this state. (No shifting occurs during the TCK cycle in which the TAP changes from *Capture-DR* to *Shift-DR* or from *Exit2-DR* to *Shift-DR*.)

In *Shift-DR*, on the falling edge of TCK, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the *Test-Logic-Reset* state since the last scan operation, TDO enables to the level present before it was last disabled. If the TAP has passed through the *Test-Logic-Reset* state since the last operation, TDO enables to a high level.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the *Shift-DR* state from either *Exit1-DR* or *Exit2-DR* without recapturing the data registers. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from *Shift-DR* to *Exit1-DR*.

Pause-DR

The TAP can remain in this state indefinitely. The *Pause-DR* state allows you to suspend and resume shift operations without losing data.

Update-DR

In the *Update-DR* state, the current instruction determines whether or not the latches in the selected data registers are updated with data from the scan path.

TAP state diagram description (continued)

Capture-IR

In the *Capture-IR* state, the instruction register is preloaded with the IR status word, and then it is placed in the scan path. The TAP exits the state on the rising edge of TCK.

Shift-IR

In this state, data is shifted serially through the instruction register, from TDI to TDO, on each TCK cycle. The first shift occurs after the first TCK cycle after entering this state. (No shifting occurs during the TCK cycle in which the TAP changes from *Capture-IR* to *Shift-IR* or from *Exit2-IR* to *Shift-IR*.) In *Shift-IR*, on the falling edge of TCK, TDO goes from the high-impedance state to the active state.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the *Shift-IR* state from either *Exit1-IR* or *Exit2-IR* without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from *Shift-IR* to *Exit1-IR*.

Pause-IR

The TAP can remain in this state indefinitely. The *Pause-IR* state allows you to suspend and resume shift operations without losing data.

Update-IR

In the *Update-IR* state, the instruction register latches are updated with the new instruction from the scan path.

instructions

standard SCOPE instructions

The SCOPE Diary supports a subset of the standard SCOPE instruction set. The defined instructions are shown in Table 4. All other SCOPE instructions select the default BYPASS instruction.

Table 4. Standard SCOPE Instructions

Opcode	Code	Description
BYPASS	FFh	Select Bypass Register
EXTEST	00h	External Boundary Test (see Note 1)
IDCODE	81h	ID Register Scan
SAMPLE	82h	Boundary Sample

NOTE 1: During operation, the EXTEST instruction behaves identically to the SAMPLE instruction.

SCOPE Diary-specific instructions

The SCOPE Diary supports specific instructions to control the operation of the Flash EEPROM array. The defined instructions are shown in Table 5. All undefined opcodes select the BYPASS instruction.

Table 5. SCOPE Diary-Specific Instructions

Opcode	Code	Description
BEGOPS	69h	Begin Operation in Progress
BYTERD	63h	Byte Read
BYTEWR	E4h	Byte Write
CLRERR	6Ah	Clear Conflict Error Flag
CLRLOCK	66h	Exit Lock Mode
CLRSWS	EBh	Clear Software Sequence
DMARD	E1h	DMA Read
DMAWR	E2h	DMA Write
ERABLK	E7h	Erase Block Register Select
ISTEST	6Ch	Internal Self Test
LDADDR	60h	Load Address Register
LOADHDR	E8h	Header Register Select
SETLOCK	65h	Enter Lock Mode

BEGOPS Begin Operation in Progress

Scan Path TDI → bypass → TDO

Description The BEGOPS instruction is used to initiate a program, erase, or verify mode operation after the appropriate software sequence has been issued. This instruction must be executed within 6 ms of the last write operation, and the software sequence status bit in the instruction register must be set, or the selected operation will not begin. If the time-out condition is not met, the software sequence commands must be re-issued. Once the BEGOPS instruction is loaded, it is not executed until the diary is placed in the *Run-Test/Idle* state.

BYPASS Select Bypass Register

Scan Path TDI → bypass → TDO

Description The BYPASS instruction conforms to the 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register during the *Update-DR* state.

BYTERD Byte Read

Scan Path TDI → memory-data → memory-address → TDO

Description The BYTERD instruction is used to read the value stored in a memory array location. During the read operation, the contents of the memory-address register point to the value. This value is captured in the memory-data register during the *Update-DR* state.

BYTEWR Byte Write

Scan Path TDI → memory-data → memory-address → TDO

Description The BYTEWR instruction performs two operations. It can write 8-bit values into both the software sequence detector and the page programming buffer. The contents of the memory-address register and the contents of the memory-data register are presented to the memory core during the *Update-DR* state. On the rising edge of TCK, upon leaving the *Update-DR* state, an internal write signal is applied to either the software sequence detector or the page programming buffer.

CLRERR Clear Conflict Error Flag

Scan Path TDI → bypass → TDO

Description The CLRERR instruction is used to reset the program/erase conflict flag. The conflict flag (status bit 2 in the instruction register) will be set if any write operations are issued while the SCOPE Diary is programming or erasing. After the conflict flag is set, the SCOPE Diary won't recognize any sequence commands. The conflict flag will remain set until the CLRERR instruction is executed.

CLRLOCK Exit Lock Mode

Scan Path TDI → bypass → TDO

Description The CLRLOCK instruction is used to exit the lock mode. When the lock mode is disabled, all read and programming operations are directed to the memory array. The normal mode is indicated when status bit 4 is cleared in the instruction register.

CLRSWS Clear Software Sequence

Scan Path TDI → bypass → TDO

Description The CLRSWS instruction is used to clear software sequence operations. The instruction will reset or cancel any software sequence up until the BEGOPS instruction is executed. The CLRSWS instruction will also clear status bit 5 (valid software sequence detected) in the instruction register. The CLRSWS instruction will not interrupt an erase or program operation once the operation has started.

DMARD DMA Read

Scan Path TDI → (ignored) / memory-data → TDO

Description The DMARD instruction is used to perform streaming data reads from the Flash EEPROM memory array. During the read operation, upon entering the *Shift-DR* state, the contents of the memory array will be shifted out beginning with the currently addressed location. The memory-address register is automatically incremented on each byte boundary while performing the DMARD operation. Input data on the TDI pin is discarded and does not pass through to the TDO output pin.

DMAWR DMA Write

Scan Path TDI → memory-data → memory-address → TDO

Description The DMAWR instruction allows a streaming method of writing address/data pairs to the SCOPE Diary. During the *Shift-DR* state, the SCOPE Diary will automatically generate write strobes to the memory core on each 24-bit address/data pair boundary. The SCOPE Diary supports two modes of synchronizing the write operation with the incoming address/data pairs; state-transition mode and stream-header mode. The contents of the header register determine the selected mode.

ERABLK Erase Block Register Select

Scan Path TDI → erase-block → TDO

Description The ERABLK instruction is used to access the erase-block select register. Data loaded into the ERABLK register is presented to the memory core during the *Update-DR* state.

EXTEST External Boundary Test

Scan Test TDI → boundary-scan → TDO

Description The EXTEST instruction is used to check the board connectivity of the DLA and DLB input pins. During an EXTEST operation, DLA and DLB inputs to the internal control logic can be sampled by the scan path, but not driven.

IDCODE ID Register Scan

Scan Path TDI → id → TDO

Description The IDCODE instruction is used to read the device identification data. During the *Capture-DR* state, the 32-bit device identification code (0000102Fh) is loaded into the ID register. The IDCODE instruction is automatically loaded during SCOPE Diary power-on reset or upon entry to the *Test-Logic-Reset* state.

ISTEST Internal Self Test

Scan Path TDI → boundary-scan → erase-block → header → memory-data → memory-address → TDO

Description The ISTEST instruction is used to test scan path data registers. During the *Capture-DR* state, all of the register latched values are transferred to the scan path (except the boundary scan register which transfers the values of DLA and DLB to the scan path).

LDADDR Load Address Register

Scan Path TDI → memory-address → TDO

Description The LDADDR instruction is used to load the memory-address register. The 16-bit value loaded from the scan path points to an address and is presented to the memory array during the *Update-DR* state.

LOADHDR Header Register Select

Scan Path TDI → header → TDO

Description The LOADHDR instruction is used to access the header register. Loading any value from 01h to FFh selects header mode synchronization during DMA write operations. Loading the header register with 00h selects state-transition mode synchronization for DMA write operations. During the LOADHDR operation, the header register is selected into the DR scan path.

SAMPLE Boundary Sample

Scan Path TDI → boundary-scan → TDO

Description The SAMPLE instruction is used to check the board connectivity of the DLA and DLB input pins. During a SAMPLE operation, DLA and DLB inputs to the internal control logic can be sampled by the scan path, but not driven.

SETLOCK Enter Lock Mode

Scan Path TDI → memory-data → TDO

Description The SETLOCK instruction is used to enable the lock mode. When the lock mode is enabled, read and programming operations are directed to the lockbits. The lock mode operation is indicated when status bit 4 is set in the instruction register. The SCOPE Diary will remain in the lock mode until the CLRLOCK instruction is executed. While in the lock mode, all read operations capture the state of the lockbits in the data-memory register. While reading the lockbits, the four most significant bits are set to logic 1.

operation

TAP state controller

Operation of the TAP state controller conforms to the IEEE 1149.1 Serial Test Bus standard. The state flow diagram is shown in Figure 4 on page 8.

loading and executing instructions

All bus sequences that load and execute instructions start with the TAP in the *Run-Test/Idle* state. To initialize the TAP to *Run-Test/Idle* from any other state, apply the 6-cycle sequence shown in Table 6.

Table 6. TAP Reset Sequence

Cycle	1	2	3	4	5	6
TMS	1	1	1	1	1	0
TCK						
TDI†	X	X	X	X	X	X
TDO	(See Note 2)	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z
TAP State	Undefined	Undefined	Undefined	Undefined	Test-Logic-Reset	Run-Test/Idle

† X denotes a don't care.

NOTE 2: TDO will become high-impedance on falling edge of TCK.

sequence timing

The SCOPE Diary contains internal timing logic to simplify programming and erase operations. Once the host initiates a programming or erasing operation, that operation will automatically continue to completion. The host does not need to intervene until the operation is finished. To check the status of the operation, poll status bit 6 of the instruction register.

software sequence

The host initiates all of the SCOPE Diary's internal memory operations by issuing a sequence of address/data pairs (forming a specific software sequence) to the SCOPE Diary. The correct address/data pairs must be received in a specific order and within a specific time period to be recognized as a valid software sequence by the SCOPE Diary. Once a sequence has begun, the SCOPE Diary starts an internal sequence timer. Each consecutive address/data pair must be received within a 6 ms time period. After each address/data pair, the timer is reset to receive the next sequence pair. If the time between consecutive address/data pairs exceeds the timer limit, the internal state of the sequence detector will be reset, and the host must re-issue the software sequence from the beginning. If the SCOPE Diary detects a valid software sequence, status bit 5 of the instruction register will be set within 2 μs and will remain set as long as the SCOPE Diary is unlocked for the operation. The host may terminate a software sequence at any point by either letting the internal time limit expire, or by issuing a CLRSWS command. The software sequences recognized by the SCOPE Diary are shown in Table 7.

Table 7. SCOPE Diary Software Sequences

Operation	Address/Data Pair Sequence
Programming	5555h / AAh 2AAAh / 55h 5555h / A0h
Erasing	5555h / AAh 2AAAh / 55h 5555h / 80h 5555h / AAh 2AAAh / 55h 5555h / 10h
Program-Verify	5555h / AAh 2AAAh / 55h 5555h / B0h
Erase-Verify	5555h / AAh 2AAAh / 55h 5555h / D0h
Exit-Verify	5555h / AAh 2AAAh / 55h 5555h / F0h

page programming buffer

The page programming buffer is a 32-byte buffer that the host loads with the data to be programmed into the memory array. This buffer is internal to memory and can be accessed using the memory-address and memory-data registers. The page programming buffer is automatically selected by internal control logic after it detects a valid program software sequence. The contents of this buffer are automatically set to FFh, so any bits not specifically cleared by the host will not be programmed. Up to 32 bytes can be programmed in one cycle.

Address/data pairs must be loaded into the page programming buffer within the same time constraints as the software sequence. If the sequence timer is allowed to expire during a page programming buffer load, the internal control logic will terminate the programming operation and clear the software sequence detector (indicated by status bit 5 in the instruction register). During a programming operation, data that has been loaded into the internal page programming buffer is automatically transferred into the memory array.

operation initiation

The SCOPE Diary differs from typical software sequence-controlled memory devices because the selected programming or erasing operation does not automatically begin at the end of the internal sequence time out. To initiate the selected operation, the host must issue the BEGOPS command to the SCOPE Diary and enter the *Run-Test/Idle* state before the internal sequence timer expires. If the timer expires, the internal sequence detector will be cleared, and the selected operation must be re-initiated from the beginning. Status bit 6 in the instruction register indicates a successful program or erase operation. This bit will be set within 2 μs after the BEGOPS instruction is executed.

reset

The SCOPE Diary test bus logic is cleared either by internal circuitry at power-up, or by entry to the *Test-Logic-Reset* state. All internal data scan path registers are set to logic 0, and the instruction register is loaded with the IDCODE instruction. Entering the *Test-Logic-Reset* state will not clear a pending software sequence or interrupt an executing self-timed program or erase cycle.

erase-verify mode

The erase-verify mode allows the host to verify the adequacy of erasure. Once the SCOPE Diary has been placed in the verify mode, it will remain in that state (indicated in the instruction register when status bit 3 is a logical 1) until the exit-verify mode sequence has been issued. When in the erase-verify mode, the internal voltage applied to the read select lines (wordlines) is reduced by a preset margin. To verify that the array has been erased, the host reads the memory block and checks that all bits are set to logic 1.

program-verify mode

The program-verify mode allows the host to verify the adequacy of programming. Once the SCOPE Diary has been placed in the program-verify mode, it will remain in this state (indicated in the instruction register when status bit 3 is a logical 1) until the exit-verify mode sequence has been issued. When in the program-verify mode, the internal voltage applied to the read-select lines (wordlines) is increased by a preset margin. To verify that a programming operation was successful, the host reads the previously programmed locations and checks that the data values are correct.

JTAG extensions

DMA read

The DMA read mode allows any number of sequential bits to be read from the SCOPE Diary while remaining in the *Shift-DR* state. During a DMA read operation, the contents of the memory array will be shifted out beginning with the address location contained in the memory-address register. Upon entry to the *Shift-DR* state, an internal modulo 8 counter is triggered. This counter is used to increment the contents of the memory-address register on byte boundaries. After the data from the last byte in the memory array has been read, the next data will be read from the byte at the beginning of the memory array.

DMA write

The DMA write mode simplifies data transfer to the SCOPE Diary. This mode allows data to be continuously streamed into the SCOPE Diary while remaining in the *Shift-DR* state. Compared to normal modes of data transfer, the DMA write extensions enable systems with a large number of devices in the scan path to realize a significant reduction of clock cycles.

In the DMA write mode, an internal modulo 24 counter is used to automatically transfer address/data pairs to the memory core while bypassing the *Update-DR* state. To initiate a DMA write data transfer, the internal modulo 24 counter must be triggered (synchronized) when the first bit of an address/data pair is at the TDI input pin. The SCOPE Diary supports two methods of DMA synchronization: state-transition mode and header mode. The host determines which method of DMA synchronization is used.

state-transition mode

The host selects state-transition mode by clearing the header register (all bits to logic 0). When the state-transition mode is selected, incoming scan path data is ignored during first entry to the *Shift-DR* state. The first entry to *Pause-DR* indicates proper alignment at the TDI input pin of the first address/data pair. Re-entry to the *Shift-DR* state triggers the modulo 24 counter and enables the address/data pair to be written to the memory core. Address/data pairs can then be streamed continuously to the SCOPE Diary with internal transfers occurring automatically on 24-bit boundaries.

header mode

The host selects the header mode by loading the header register with a value from 01h to FFh. When the header mode is selected, incoming scan path data is ignored until a byte (matching the contents of the header register) arrives indicating the arrival of valid address/data pairs. When this header byte is detected, the internal modulo 24 counter is triggered. Address/data pairs can then be streamed continuously to the SCOPE Diary with internal transfers occurring automatically on 24-bit boundaries.

In either state-transition or header mode, the host places the SCOPE Diary in the *Update-DR* state to end a DMA write operation. Because placing the SCOPE Diary in the *Update-DR* state ends the operation, the host must *never* place the SCOPE Diary in this state until the DMA write operation is complete. The host may place the SCOPE Diary in the *Pause-DR* state at any time.

operation examples

Note that in this section, the letter "n" denotes a value from 0h to Fh, and the letter "x" denotes a don't care.

reading examples

reading using the byte mode

Step 1. Load the BYTERD instruction.
Step 2. Scan in 16-bit address = *nnnn* and 8-bit data = *xx*.
Step 3. Scan out 16-bit address = *nnnn* and 8-bit data = *nn*.

reading using the DMA mode

Step 1. Load the LDADDR instruction.
Step 2. Scan in 16-bit address = *nnnn*.
Step 3. Load the DMARD instruction.
Step 4. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values, the address register is automatically incremented on byte boundaries.

lockbit examples

reading lockbits using the byte mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the BYTERD instruction.
Step 3. Scan in 16-bit address = 0000 and 8-bit data = *xx*.
Step 4. Scan out 16-bit address = 0000 and 8-bit data = F*n*.
Step 5. Load the CLRLOCK instruction.

reading lockbits using the DMA mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the DMARD instruction.
Step 3. Scan out the 8-bit lock value = F*n*.
Step 4. Load the CLRLOCK instruction.

programming lockbits using the byte mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the BYTEWR instruction.
Step 3. Scan in address = 5555 and data = AA, go to *Run-Test/Idle*.
Step 4. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 5. Scan in address 5555 and data = A0; go to *Run-Test/Idle*.
Step 6. Scan in address = 0000, and data = F*n*; go to *Run-Test/Idle*.
Step 7. Load the BEGOPS instruction; go to *Run-Test/Idle*.
Step 8. Load the CLRLOCK instruction.

programming lockbits using the DMA mode

Step 1. Load the SETLOCK instruction.
Step 2. Load the DMAWR instruction.
Step 3. Synchronize SCOPE Diary using either state-transition mode or header mode.
Step 4. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 5. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 6. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 7. Continue looping in *Shift-DR* to scan in address = 0000 and data = F*n*.
Step 8. Load the BEGOPS instruction; go to *Run-Test/Idle*.
Step 9. Load the CLRLOCK instruction.

flash erase examples

erasing a block using the byte mode

Step 1. Load the ERABLK instruction.
Step 2. Scan in the 4-bit erase-block-select value = *n*.
Step 3. Load the BYTEWR instruction.
Step 4. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 5. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 6. Scan in address = 5555 and data = 80; go to *Run-Test/Idle*.
Step 7. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 8. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 9. Scan in address = 5555 and data = 10; go to *Run-Test/Idle*.
Step 10. Poll the SCOPE Diary until valid sequence is detected.
Step 11. Load the BEGOPS instruction; go to *Run-Test/Idle*.

erasing a block using the DMA mode

Step 1. Load the ERABLK instruction.
Step 2. Scan in the 4-bit erase-block-select value = *n*.
Step 3. Load the DMAWR instruction.
Step 4. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 5. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 6. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 7. Continue looping in *Shift-DR* to scan in address = 5555 and data = 80.
Step 8. Continue looping in *Shift-DR* to scan in address = 5555 and data = AA.
Step 9. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 10. Continue looping in *Shift-DR* to scan in address = 5555 and data = 10.
Step 11. Poll SCOPE Diary until valid sequence is detected.
Step 12. Load the BEGOPS instruction; go to *Run-Test/Idle*.

verifying block erasure using the byte mode

select the erase-verify mode:

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = D0; go to *Run-Test/Idle*.

read out the erased block:

Step 5. Load the BYTERD instruction.
Step 6. Scan in 16-bit address = *nnnn* and 8-bit data = *xx*.
Step 7. Scan out 16-bit address = *nnnn* and 8-bit data = FF; at the same time, scan in 16-bit address = *nnnn*+1 and data = *xx*.
Step 8. Repeat Step 7 until entire block is read. All bits will be a logic 1 if the block is properly erased.

exit the erase-verify mode:

Step 9. Load the BYTEWR instruction.
Step 10. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 11. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 12. Scan in address = 5555 and data = F0; go to *Run-Test/Idle*.

verifying block erasure using the DMA mode

select the erase-verify mode:

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = D0.

read out the erased block:

Step 6. Load the LDADDR instruction.
Step 7. Scan in 16-bit data starting address = *nnnn* of the block you want to verify.
Step 8. Load the DMARD instruction.
Step 9. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values from the addressed block. All bits will be a logic 1 if the block is properly erased.

exit the erase-verify mode:

Step 10. Load the DMAWR instruction.
Step 11. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 12. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 13. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 14. Continue looping in *Shift-DR* to scan in address = 5555 and data = F0.

verifying programming using the byte mode

select the program-verify mode:

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = B0; go to *Run-Test/Idle*.

read out the programmed data:

Step 5. Load the BYTERD instruction.
Step 6. Scan in 16-bit address = *nnnn* and 8-bit data = *xx*.
Step 7. Scan out 16-bit address = *nnnn* + 1 and 8-bit data = *nn*; at the same time, scan in 16-bit address=*nnnn* + 1 and data = *xx*.
Step 8. Repeat Step 7 until desired memory locations are read and verified.

exit the program-verify mode

Step 9. Load the BYTEWR instruction.
Step 10. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 11. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 12. Scan in address = 5555 and data = F0; go to *Run-Test/Idle*.

verifying programming using the DMA mode

select the program-verify mode:

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = B0.

read out the programmed data:

Step 6. Load the LDADDR instruction.
Step 7. Scan in 16-bit starting address = *nnnn* of the data you want to verify.
Step 8. Load the DMARD instruction.
Step 9. Loop in *Shift-DR* to shift out a stream of 8-bit memory data values starting from the addressed location. Verify that the output data stream matches the programmed data.

exit the program-verify mode:

Step 10. Load the DMAWR instruction.
Step 11. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 12. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 13. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 14. Continue looping in *Shift-DR* to scan in address = 5555 and data = F0.

programming examples

programming a single byte using the byte mode

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = A0; go to *Run-Test/Idle*.
Step 5. Scan in address = *nnnn* and data = *nn*; go to *Run-Test/Idle*.
Step 6. Load the BEGOPS instruction; go to *Run-Test/Idle*.

programming a single byte using the DMA mode

Step 7. Load the DMAWR instruction.
Step 8. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 9. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 10. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 11. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 12. Continue looping in *Shift-DR* to scan in address = *nnnn* and data = *nn*.
Step 13. Load the BEGOPS instruction; go to *Run-Test/Idle*.

programming a page using the byte mode

Step 1. Load the BYTEWR instruction.
Step 2. Scan in address = 5555 and data = AA; go to *Run-Test/Idle*.
Step 3. Scan in address = 2AAA and data = 55; go to *Run-Test/Idle*.
Step 4. Scan in address = 5555 and data = A0; go to *Run-Test/Idle*.
Step 5. Scan in address = *nnnn* and data = *nn*; go to *Run-Test/Idle*.
Step 6. Go to Step 5 while there are address/data pairs to load within the 32-byte page.
Step 7. Load the BEGOPS instruction, go to *Run-Test/Idle*.

programming a page using the DMA mode

Step 1. Load the DMAWR instruction.
Step 2. Synchronize the SCOPE Diary using either state-transition mode or header mode.
Step 3. Loop in *Shift-DR* to scan in address = 5555 and data = AA.
Step 4. Continue looping in *Shift-DR* to scan in address = 2AAA and data = 55.
Step 5. Continue looping in *Shift-DR* to scan in address = 5555 and data = A0.
Step 6. Continue looping in *Shift-DR* to scan in address = *nnnn* and data = *nn*.
Step 7. Go to Step 6 while there are address/data pairs to load within the 32-byte page.
Step 8. Load the BEGOPS instruction; go to *Run-Test/Idle*..

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 3) ..... – 0.6 V to 7 V
Input voltage range: All except DLA (see Note 3) ..... – 0.6 V to 6.5V
Input voltage range: DLA (see Note 3) ..... – 0.6 V to 15 V
Output voltage (see Note 3) ..... – 0.6 V to V_{CC} + 0.6V
Operating free-air temperature range ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: Voltage values are with respect to GND (substrate).

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	TTL	2		V_{CC} + 1	V
		CMOS	V_{CC} – 0.2		V_{CC} + 0.2	
V_{IL}	Low-level input voltage	TTL	– 0.5		0.8	V
		CMOS	GND – 0.2		GND + 0.2	
T_A	Operating free-air temperature		– 55		125	°C
	Endurance cycles				1000	
	Programming operations				100 000	

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
I_I	Input current (leakage)	DLA, DLB	V_I = 2.4 V		75	165	µA
		DLA, DLB	V_I = 0 V			±10	
		TDI, TMS, TCK	V_I = 0.4		– 10	– 50	
		TDI, TMS, TCK	$V_I = V_{CC}$ = 5.5 V			±10	
I_O	Output current (leakage)		V_O = 0.1 to V_{CC}			±10	µA
I_{CC1}	V_{CC} average supply current (active read)		t_{cycle} = 160 ns, outputs open			20	mA
I_{CC2}	V_{CC} average supply current (active write)		t_{cycle} = 15 ms			15	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_I	Input capacitance	V_I = 0, f = 1 MHz		4	7	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		8	12	pF

† Typical values are at T_A = 25°C and nominal voltage.
‡ Capacitance measurements are made on sample basis only

switching characteristics over full ranges of recommended operating conditions

PARAMETER		MIN	MAX	UNIT
t_{DA}	TDO valid from falling edge of TCK		74	ns
t_{DZ}	TDO disable time from falling edge of TCK		45	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
t_{CYC}	TCK cycle time	160		ns
$t_{W(TCKH)}$	Pulse duration, TCK high	50		ns
$t_{W(TCKL)}$	Pulse duration, TCK low	70		ns
$t_{SU(TMS)}$	TMS input setup time	15		ns
$t_{IH(TMS)}$	TMS input hold time	5		ns
$t_{SU(TDI)}$	TDI input setup time	6		ns
$t_{IH(TDI)}$	TDI input hold time	15		ns

internal timing requirements

	PARAMETER	MIN	MAX	UNIT
t_{SSS}	Software sequence status bit valid from software sequence		2	μs
t_{PEBS}	Program erase busy status bit valid from BEGOPS execution		2	μs
t_{ST}	Sequence timer limit		6	ms
t_{ERA}	Erase cycle time		15	ms
t_{PGM}	Program cycle time		15	ms

PARAMETER MEASUREMENT INFORMATION

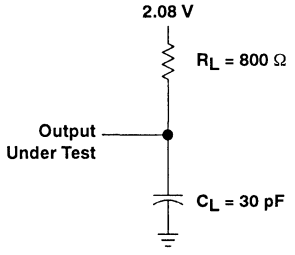
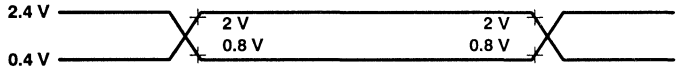
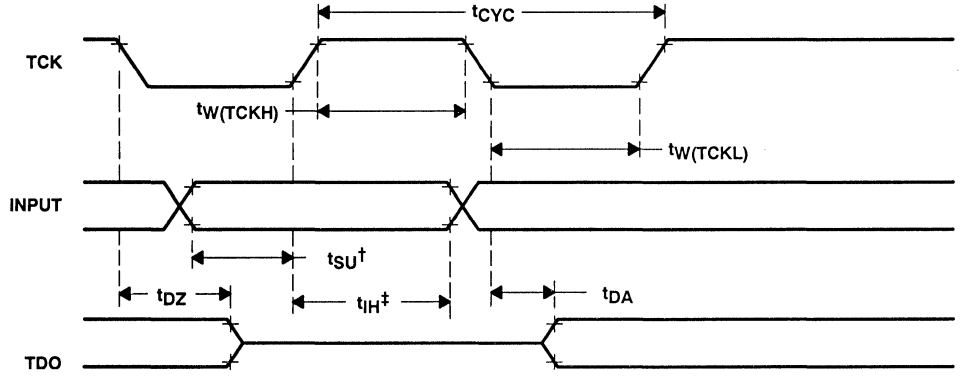


Figure 5. AC Test Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 for logic low. Timing measurements are made at 2 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and GND as close as possible to the device pins.



† t_{SU} represents TDI input setup time and TMS input setup time.
‡ t_{IH} represents TDI input hold time and TMS input hold time.

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EXPLANATION OF IEEE/IEC LOGIC SYMBOLS FOR MEMORIES

Introduction

The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

The current standards are IEC Publication 617-12, 1983, and ANSI/IEEE Standard 91-1984. Most of the data sheets in this data book include symbols prepared in accordance with these standards. The explanation that follows is necessarily brief and greatly condensed from the explanation given in the standards. This is not intended to be sufficient for people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

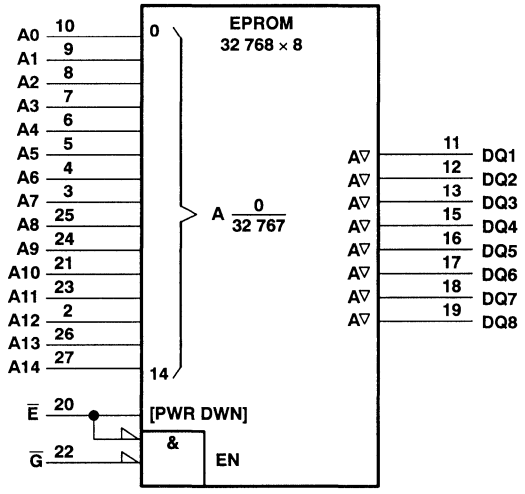
Explanation of a Typical Symbol For a Static Memory

The TMS27C400 symbol will be explained in detail. This symbol includes almost all the features found in the OTP PROMs and EPROMs.

The address inputs are arranged in order of their assigned binary weights and the range of addresses are shown as $A\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The outputs affected by these addresses are indicated by the letter A, as data inputs would also be if the device were a RAM.

The polarity indicator ⊾ indicates that the external low level causes the internal 1-state (the active or asserted state) at an input or that the internal 1-state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol o.

The TMS27C400 Symbol



The ▽ symbols indicate three-state outputs. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1-state, the outputs are enabled; when EN stands at its internal 0-state, the outputs stand at their high-impedance states. Sometimes the EN is a single input, but in the illustrated case, it is the output of a two-input AND gate. Both inputs (pins 20 and 22) are active low, so if either one of them goes high, the outputs will be disabled. The upper one of these two inputs (pin 20) has another function. When nonstandard labels and explanatory labels are used within symbols, they are enclosed within square brackets. Here we find the label "[PWR DWN]". This is intended to indicate that if pin 20 is high, the memory will go to a low-power standby state.

The Basics

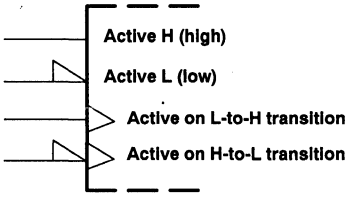
The next section illustrates the most common building blocks that are used in constructing symbols for memories. On the left are shown the symbols that specify the active levels for level-operated inputs, and the direction of active transition for dynamic inputs.

It is preferred to show all input lines on the left and all output lines on the right. When an exception is made to this left-to-right signal flow, an arrowhead is used to show the reverse signal flow. Three symbols are shown that indicate three-state, open-drain, and open-source outputs. If none of these are used, the output should be assumed to be totem-pole. The common control block is a point of replacement for inputs that affect an array of elements.

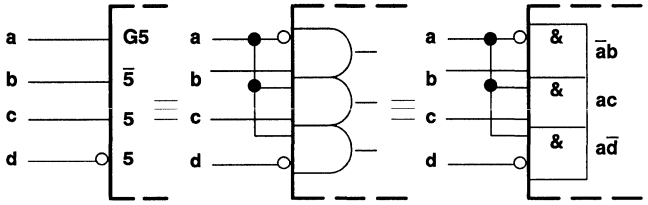
The drawings on the right define the three forms of dependency notation used in this book. At an input (or output) that affects other inputs or outputs, a letter (G, C, or Z) is placed followed by a number. That same number is placed at the affected inputs and outputs. The letter G indicates that an AND relationship exists; if the affecting input stands at the 0-state, it imposes that 0-state on the affected input or output. The letter C indicates a control relationship, usually between clock and a D (data) input. If the C input stands at its 0-state, the affected input is disabled. A D input is always an input to a storage element, which it either sets to the 1-state or resets to the 0-state, unless the D input is disabled to have no effect. Z dependency is used to transfer a signal from one place in a symbol to another, for example from the output at Z4 across to a terminal labeled "4", or from the output at Z5 back to the "5" where it serves as an input with no terminal attached.

Diagrammatic Summary

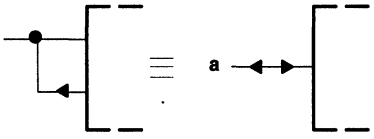
INPUTS



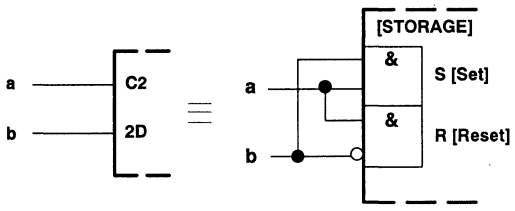
G (AND) DEPENDENCY



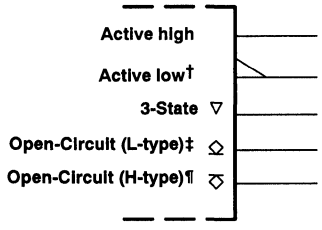
INPUT/OUTPUT



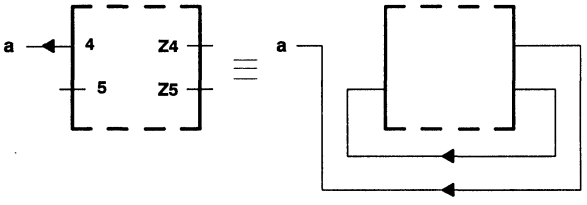
C (CONTROL) DEPENDENCY



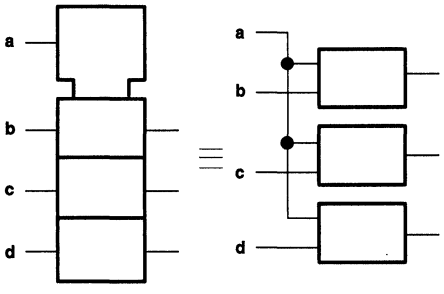
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



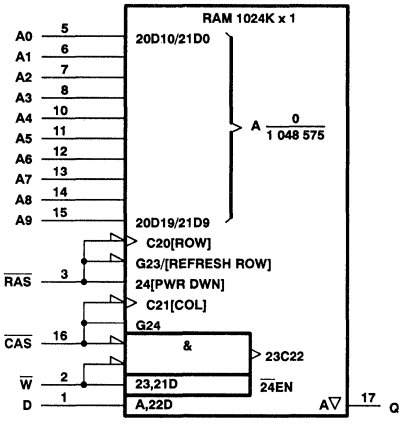
COMMON CONTROL BLOCK



† The active-low indicator may be used in combination with the 3-state and open-circuit indicators.
‡ L-types include N-channel open-drain and P-channel open-source outputs.
¶ H-types include P-channel open-drain and N-channel open-source outputs.

Explanation of a Typical Symbol for a Dynamic Memory

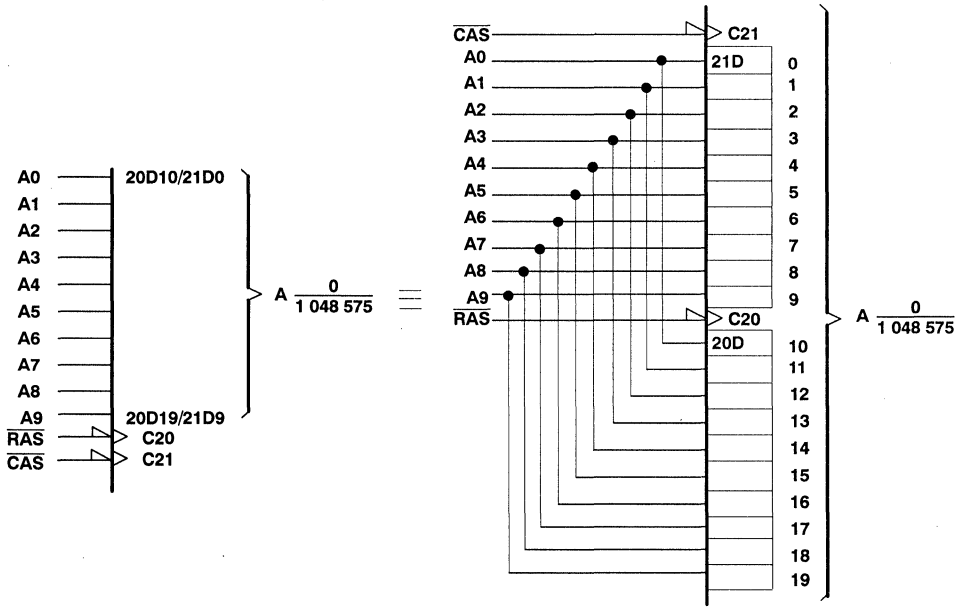
The TMS4C1024 Symbol



The TMS4C1024 symbol will be explained in detail for each operating function. The assumption is made that the previous sections have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

Addressing

The symbol above makes use of an abbreviated from to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.



When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the ten address registers 10 through 19. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the ten address registers 0 through 9. The outputs of the address registers are in 20 internal address lines that select 1 of 1 048 576 cells.

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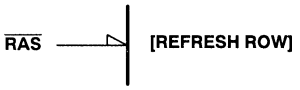
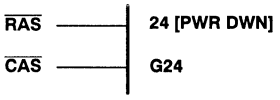
Refresh



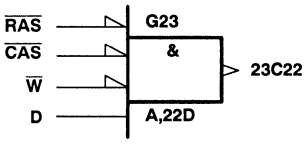
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required for refreshing are not indicated by the symbol.

Power Down



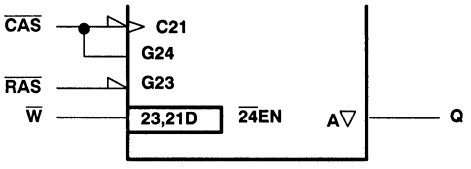
$\overline{CAS}$ is ANDed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

Write



By virtue of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ is already low ($\overline{RAS}$ is ANDed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

Read



The ANDed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be ANDed with the output of the latch (by G24 and 24). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, New York 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, New York 10018

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MOS MEMORY QUALITY AND RELIABILITY STRATEGY

Texas Instruments is committed to providing its customers with reliable, high quality memory products. MOS Memory management has applied a four point quality and reliability strategy to:

- Provide customers with the lowest cost of product ownership through quality, reliability, and service by:
  - On-time delivery to minimize customer inventory.
  - Quality performance that justifies ship-to-stock certification and eliminates the cost of component testing.
  - No system manufacturing fallout.
  - No warranty and service costs.
- Develop partnership relationships to service and solve customer problems and anticipate upcoming needs.
- Live quality improvement process from product creation and manufacturing through product sales via our total quality control approach of:
  - Quality Function Deployment.
  - Design-in and build-in quality and reliability.
  - In-control manufacturing.
  - Leadership customer service.
- Measure TI's performance by the customer's measurement and perception. The performance standard is continuous customer satisfaction.

Total Quality Control (TQC)

Total Quality Control at TI is a business management process encompassing all company functions. The goal of Total Quality Control (TQC) is continuous customer satisfaction. Utilizing a process of improvement through a positive feedback cycle, TQC is deployed in the MOS Memory Division from the initial design-in Q&R stage, in-control manufacturing, and customer service (see Figure 1).

Proper application of the concept of "PLAN-DO-CHECK-ACT" allows a positive feedback loop that creates continuous improvement and breakthrough, as opposed to the "FIX-FIX-FIX-FIX" results of a negative loop (see Figure 2).

Quality Function Deployment

Continuous customer satisfaction can be achieved only by fully understanding customer needs, then introducing innovative products that satisfy those needs. Quality Function Deployment (QFD) accomplishes both purposes at TI. QFD is a technique that systematically records the voice of the customer, identifying product and service attributes most important to the customer. QFD then blends these needs with the talents and innovations of a TI design team to define a manufacturable, reliable product solution for the customer.

Design-In Quality and Reliability

Quality and reliability improvements at TI start with the chip and package design. The objective of MOS Memory's Design-In Quality and Reliability (DIR) thrust is *first-pass qualification of new products, internally and at the customer.* The TI approach to DIR has been to understand customer requirements of a product, and to formalize this knowledge into a database that incorporates both reliability modeling knowledge, and "lessons learned" from historical problems and engineering evaluations. Before any new design is approved, the design is verified against a DIR "checklist". Design verification is planned to evolve to computer verification utilizing artificial intelligence.

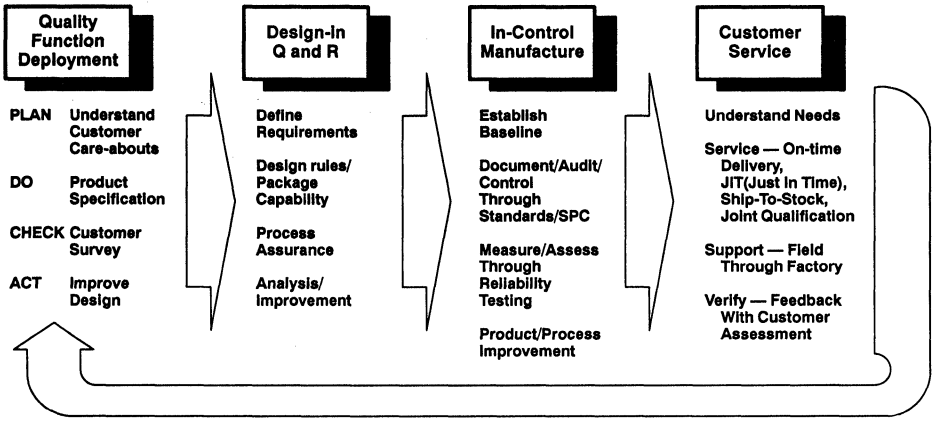


Figure 1. Total Quality Control

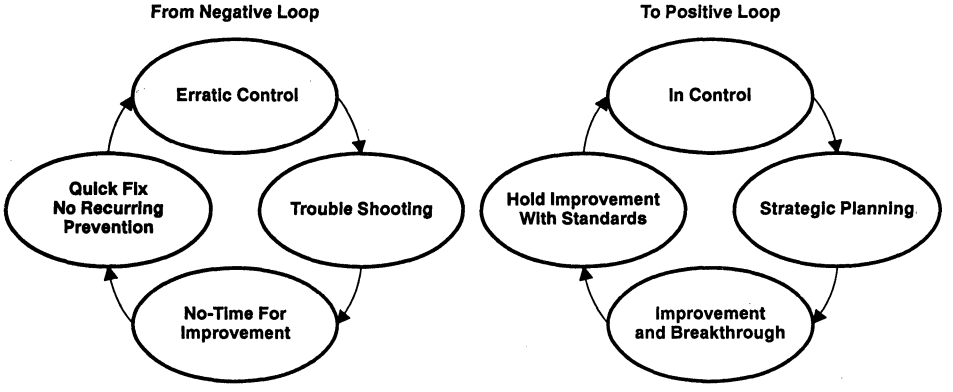


Figure 2. TQC Philosophy

In-Control Manufacturing

Documentation/Audit System

To assure in-control manufacturing, TI employs a hierarchical specification system. General specifications on all aspects of quality, reliability, and customer service are written and controlled by the central Quality and Reliability group. More detailed specifications control the operating practices of design, manufacturing, marketing, and other support organizations. These specifications follow guidelines set by the higher-level specifications, but concentrate on the type of business entity.

Regularly scheduled audits are performed within TI to ensure compliance with all specifications. The five types of audits performed are:

1. Self audit: An internal audit within each functional operation. This type of audit is conducted by persons within the operation and an additional person from outside the operation.
2. Cross-audit: An audit by persons independent of the operation being audited.
3. Group audit: An audit of an operation conducted by the Semiconductor Group audits and procedures function, which is a part of the central Quality and Reliability organization.
4. Procedures audit: An audit of lower-level specifications with respect to higher-level specifications.
5. Compliance audit: An audit of operating practices with respect to specifications.

Statistical Process Control (SPC)

Quality improvement is achieved through Statistical Process Control (SPC). SPC is applied throughout the manufacturing operations of the MOS Memory division. The objectives of SPC are:

– Control processes on a realtime basis.

– Improve process capability (CP).

– Reduce variability to target value (CPK).

– Eliminate "out-of-spec" lots.

– Achieve dependable delivery.

– Lower cost-of-quality.

Computer hardware and artificial intelligence software have been coupled to establish interactive control allowing the computer to generate realtime control charts and prompt adjustments to equipment and processes (see Figure 3).

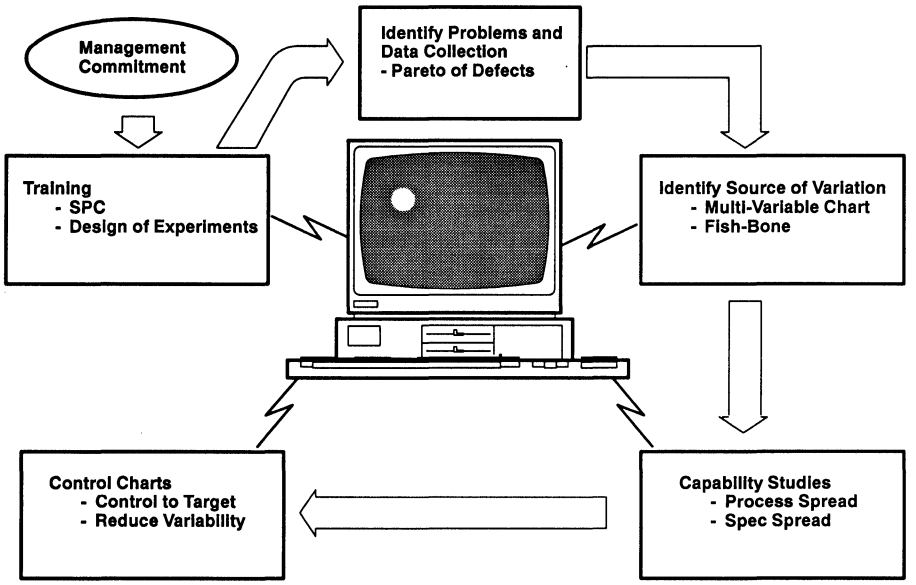


Figure 3. Computer-Aided Statistical Process Control

Die Fabrication Control

In addition to extensive SPC applications in our MOS fabrication centers, TI implements wafer-level quality and reliability controls.

Wafer-level quality control focuses on reduction of variability around target values (CPK) for key functionality parameters and controls the processes that affect these parameters. For example: Column access time (t_{CAC}) is a key DRAM parameter. One of the die manufacturing processes that affects t_{CAC} is the photo etch. To reduce variability of the target value of t_{CAC}, we control polysilicon width dimension at the photo etch process.

Wafer-level reliability controls address process control of known reliability hazards. For example: Excessive phosphorus use in die processing can lead to corrosion defects in the finished device. Wafer-level reliability controls require that phosphorus level control is built into the manufacturing process and that action is prescribed for out-of-control material. Other wafer-level reliability controls are shown in the following table.

Table 1. Wafer Reliability Controls

PARAMETER	CONTROL
Metal	Electromigration Testing, Grain Size, Silicon Nodule Monitor Step Coverage/Metal Necking Monitor Stress-Induced Metal Void Testing
Protective Overcoat	P.O. Integrity Stress Testing Thickness Monitor Refraction
Corrosion	% Phosphorus In Multilevel Oxide Monitor
Gate Oxide Integrity	Breakdown Voltage

Device Assembly Control

TI has also implemented assembly level reliability controls and SPC at critical assembly points (see Table 2) to ensure highly reliable device packaging. Each parameter has certain controls performed at appropriate frequencies to ensure that assembly processing is at qualified levels. Controls may be added or reduced after extensive testing has been performed. Results are carefully studied and fed back to preclude reliability problem introduction into the assembly process. Some of the parameters and controls are shown in Table 3.

Table 2. Major Assembly Steps Using SPC/SQC†

PLASTIC DEVICE ASSEMBLY	
Process	**Control Parameter**
Mount	% Coverage of Epoxy
Bond	Bond Strength
Mold	Temperature and Molding Parameters
Trim/Form	Lead Deflection (DIP)
CERAMIC DEVICE ASSEMBLY	
Bond	Bond Strength
Seal	Seal Furnace Temperature

†Statistical Process Control/Statistical Quality Control

Table 3. MOS Memory Assembly Level Reliability Controls

PARAMETER	CONTROL
P.O. Integrity	Contactless Wafer Mount on Tape Die Mount System Mold Compound Parameters
Chip/Crack	Visual Inspection Temp Cycle Saw Blade Conditions Poker Pin Height Wet Etch Monitor (EPROM)
Bond Integrity	Bond Strength Monitor Bond Parameters Bake/Bond Pull Monitor Capillary Change
Package Integrity	Visual Inspection Mold Press Parameters (Plastic) X-Ray Inspection (Plastic) Trim/Form (Plastic) Package Seal (Ceramic) Temp Cycle (Ceramic) Hermeticity Monitor (Ceramic)
Die Mount Integrity	Die-Shear Monitor Centrifuge Monitor X-Ray Inspect Leadframe Polyimide Pattern Inspect Pick-Up Arm Force
Contamination	Visual Inspection

Product Assessment/Improvement

Reliability Control System

The MOS Memory reliability control system (Figure 4) provides closed-loop-system feedback resulting in corrective actions and ongoing product improvements. Each new product, process, or major change to an existing product is internally qualified to industry leadership standards prior to production. This is followed by intensive monitoring during production ramp-up and reliability monitoring each month, once a product achieves final production release.

Reliability Development Issues

Soft Error: TI does extensive work in all phases of device development to minimize the effects of soft errors. Soft errors are caused by alpha particles emitted by the decay of small amounts of thorium and uranium located in device packaging materials. TI maintains an aggresive program of evaluating new mold compounds to ensure low alpha emmissivity. Certain device design and processing techniques are also applied to ensure a low soft error rate. The goal of device design and processing is to maximize the cell capacitance by employing an oxide-nitride dielectric, as opposed to an oxide dielectric. Also, the cell capacitance increases as the dielectric thickness decreases. Testing has shown that the trench capacitor used in dynamic RAMs has competitive soft error rates.

Channel Hot Electron: Channel hot electrons are caused by impact ionization in the drain pinch-off region. Electrons are accelerated toward the drain, collide with positive ions, and can be trapped in the gate oxide. This trapped charge can change the characteristics of the transistor by raising the V_T (threshold voltage). One method employed to reduce the effects of hot electrons is to add a lightly doped drain to reduce the electric field at the gate. Testing for channel hot electrons is performed at a low temperature (–10°C) and a high drain voltage.

Latch-up: A CMOS device can latch-up when the gain of the parasitic PNP+NPN transistors is greater than 1. These PNP+NPN transistors act as a silicon controlled rectifier (SCR). If enough current flows through the resistors, the transistors will turn on and the device will latch-up.

To control latch-up, the SCR gain must be controlled to less than or equal to one. Methods for improving latch-up immunity include incorporating guard rings between P+ and N+ diffusions, and isolating P+ and N+ diffusions.

Latch-up testing is performed to ensure our CMOS devices meet the minimum holding current for industry standards.

Customer Service

Quality, Reliability, Service, and the Cost of Ownership

The goal of Texas Instruments is to offer the best quality, reliability, and service in the semiconductor industry. The foundation for this approach is to ship consistent quality. Consistent quality allows ship-to-stock programs that foster the elimination of the customer's incoming inspection. Ship-to-stock quality, coupled with 100% on-time delivery to narrow shipping windows means support of the customer's just-in-time manufacturing program. This combination of quality, reliability, and service can be measured by a single index called "the cost of ownership". The "cost of ownership" is defined as being composed of the purchase price, quality adders (for incoming inspection and board rework), inventory adders (for maintenance of a buffer inventory for suppliers who cannot meet just-in-time delivery), in-house reliability adders (for system burn-in and rework), and field reliability adders (for warranty and post-warranty field repairs).

For more information about the cost of ownership concept, contact your local TI sales office and request the brochure "Texas Instruments Lowers Semiconductor Cost of Ownership", SSYB057.

Quality Improvement

Significant improvement in product quality has been achieved through:

– Better definition of customer's requirements.

– Greater emphasis on quality as a design criterion.

– Improved control of incoming materials.

– Intensive training of supervisors and operators.

– Extensive use of statistical process control.

– More automation of operations to minimize operator-related defects.

QUALIFICATION	PRODUCTION RAMP LOT ACCEPT	FINAL PRODUCTION RELEASE
Baseline process 3 – 6 diffusion lots Worst case customer qualification requirements TESTS 125°C Op life EFR† 85/85 Temperature cycle Pressure cooker test PSP/PVP‡ Static bias/storage Soft error Data retention bake Electromigration Package integrity ESD	Baseline process Reliability lot acceptance concurrent with qualifications Review of data once sufficient lots have been sampled TESTS Early Failure Rate† High temperature reverse bias§ Temperature cycle Pressure cooker test Bake 85/85§	Control each package/wafer fabrication site/device combination Ongoing reliability monitor of 125°C op life, data retention bake, temperature cycle, 85/85, autoclave, package integrity, and internal cavity moisture Control limits for each test based on product capability Early failure rate monitor

† DRAM – 125°C OPL, 80 hours
EPROM & OTP – 200°C bake, 44 hours (OTP in ceramic package)
‡ PSP: Pressure cooker, Solder dip, Pressure cooker
PVP: Pressure cooker, Vapor phase, Pressure cooker
§ Non–Volatile only

Figure 4. Reliability Control System

As is demonstrated in Figure 5, MOS Memory EPROM and DRAM outgoing quality has dramatically improved during the last few years. This significant improvement has occurred for all TI product lines and has been recognized publicly by many of our customers, who have given TI more than 70 major quality awards in the last several years. Included among these awards are Ford's Q-1 and TQE Awards, the U.S. Naval Quality Award, and the Deming Prize, which is Japan's most prestigious quality award.

Reliability Improvement

Low IC failure rates are achieved through design-in reliability, computer aided design, stringent qualification testing prior to product release, routine monitoring of released products, and an extensive failure mode tracking and feedback system for IC failures.

Each generation of MOS Memory products has exhibited a device failure rate improvement trend, and each new generation shows a step function improvement in quality and reliability over the previous generation (see Figures 5 and 6). Even though the memory device complexity increases in an ongoing manner, TI's failure rate by function has improved at an even faster pace. TI continues to emphasize reliability improvement as a major factor in reducing the total cost of ownership for our customers. Reliability improvement is reflected as a reduction in the expected field failures during system lifetime.

Up-to-date quality and reliability data for MOS Memory products is available. Please contact your local TI sales office for information.

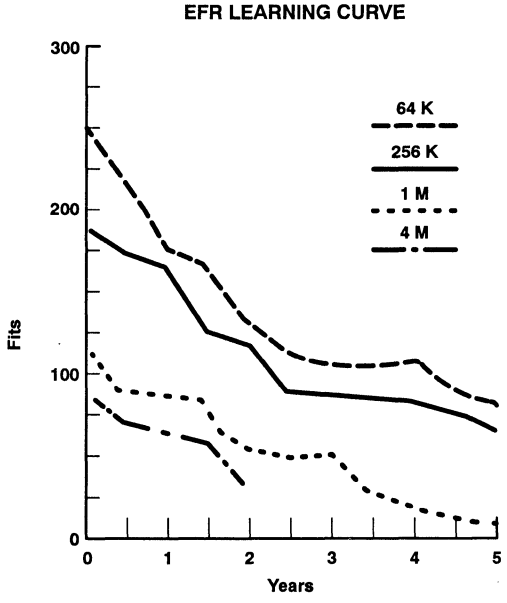


Figure 5. MOS Memory Quality Improvement

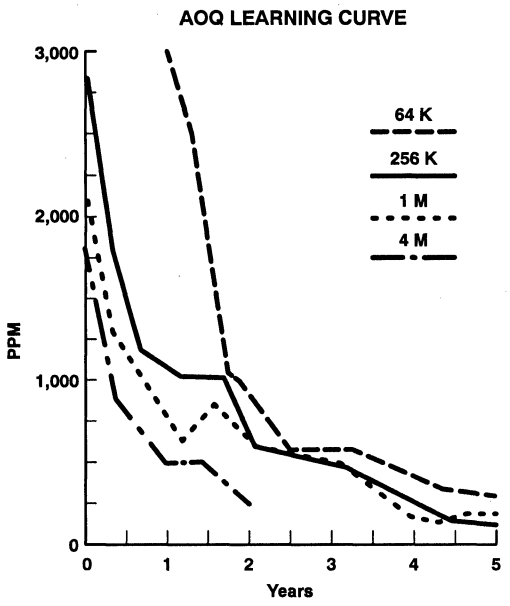
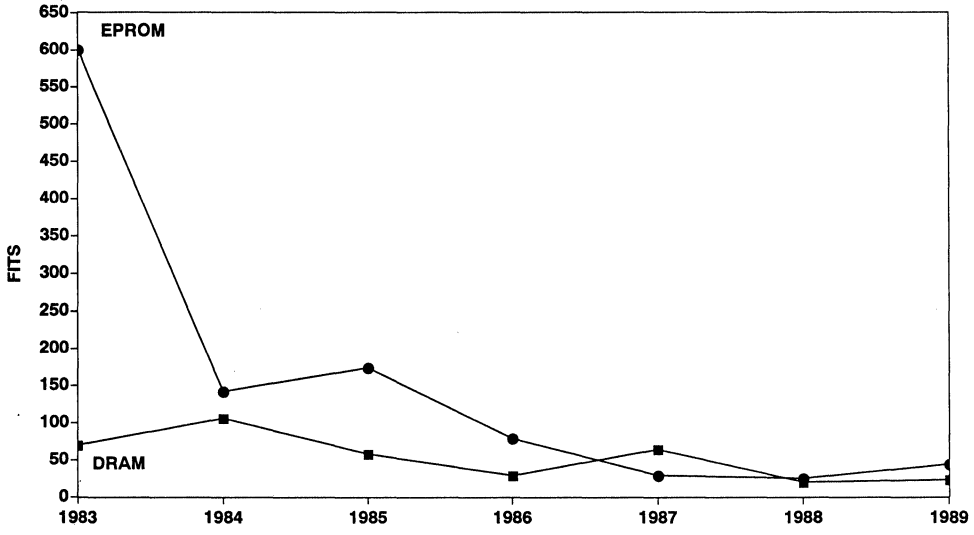


Figure 6. MOS Memory Reliability Improvement



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Scope

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) that are susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded person's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to, those listed:

1. All metal-oxide semiconductor (MOS) devices; e.g., CMOS, PMOS, etc.
2. Junction field-effect transistors (JFET)
3. Bipolar digital and linear circuits
4. Op-amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5. Hybrid microcircuits and assemblies containing any of the types of devices listed
6. Printed circuit boards and other types of assembly containing static-sensitive devices
7. Thin-film passive devices

Definitions

1. Electrostatic Discharge (ESD): A transfer of electrostatic charges between bodies at different electrostatic potentials caused by direct contact or electrostatic field induction.
2. Conductive material: Material having a surface resistivity of 10^5 Ω/square maximum.
3. Static dissipative material: Material having a surface resistivity between 10^5 and 10^9 Ω/square.
4. Antistatic material: Material having a surface resistivity between 10^9 and 10^{14} Ω/square
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or from a radioactive energy source in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883C

1. Devices are categorized according to their susceptibility to damage resulting from electrostatic discharges (ESD).

Category	ESD Sensitivity
Class 1	0 V – 1999 V
Class 2	2000 V – 3999 V
Class 3	4000 V and above

2. Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test, and shipment of completed equipment.

Applicable Reference Documents

The following reference documents (of latest issue) can provide additional information on ESD controls.

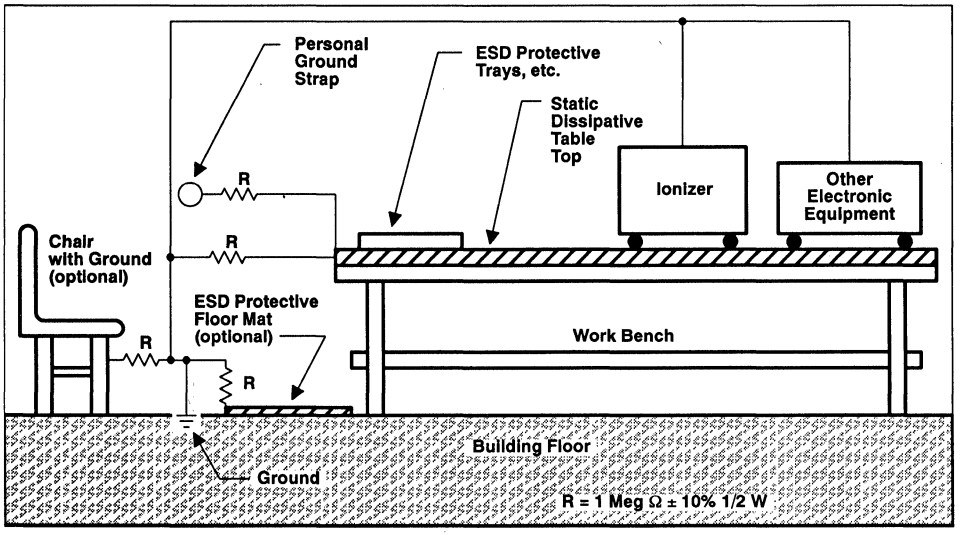
1. MIL-M-38510 Microcircuits, General Specification
2. MIL-STD-883 Test Methods and Procedures for Microelectronics
3. MIL-STD-19491 Semiconductor Devices, Packaging of
4. MIL-M-55565 Microcircuits, Packaging of
5. DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6. DOD-STD-1686 Electrostatic Discharge Control Program
7. NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
8. JEDEC Standard Publication 108

Facilities for Static-Free Workstation

The minimum acceptable static-free workstation shall consist of the work surface covered with static dissipative material attached to ground through a 1 MΩ ± 10% resistor, an attached grounding wrist strap with integral 1 MΩ ± 10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the static dissipative material. Ground shall utilize the standard building earth ground; refer to Figure 1. Conductive floor tile/carpet along with conductive shoes may be used in lieu of the conductive wrist straps for non-seated personnel. The Site Safety Engineer must review and approve all electrical connections at the static-free workstation prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free workstations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the static disspative work surface.

NOTE: Earth ground is not computer ground or RF ground or any other limited-type ground.

Figure 1. Static-Free Workstation

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Table 1. General Grounding Requirements

	Treated With Antistatic Solution or Made of Conductive Material	Grounded to Common Point	Static Dissipative Material
Handling Equipment/ Handtools	X		X
Metal Parts of Fixtures and Tools/Storage Racks		X	
Handling Trays/Tubes	X		X
Soldering Irons/Baths		X	
Table Tops/Floor Mats	X	X	X
Personnel		X Using Wrist Strap*	

* With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10 000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can be established only through routing electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1. Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2. Hard abused surfaces (floor, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3. Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4. Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the area supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at workstations and labels on static-sensitive parts and containers shall be consistent in color, symbols class, voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all workstations performing any handling operations with static-sensitive items. These signs shall contain the following information or its equivalent.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESD-sensitive items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESD-sensitive items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC-accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the area supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the 40%–60% relative humidity range.

Preparation for Working at Static-Free Workstation

A workstation with a static disspative work surface connected to ground through a 1 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free workstation (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free workstation. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the gounding wrist strap. If possible, the operator should avoid touching leads or contacts even though he or she is grounded.

CAUTION

Personnel shall never be attached without the presence of the 1 MΩ ± 10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. Operators must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist, which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any improperly prepared person, while at or near the work station, shall not touch or come in close proximity with any static-sensitive item. It is the responsibility of the operator and the area supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-rlated items, including information sheets, fluid containers, tools, and part carriers must be approved for use at the static-free workstation.

General Handling Procedures and Requirements

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at the static-free workstation. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.

3. Static-sensitive items are to remain in their protective containers except when actually in use at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard-grounded test gear on bench top.
6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in Preparation for Working at Static-Free Workstation.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

Packaging Requirements

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1. The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in General Handling Procedures and Requirements, item 2. Conductive magazines/boxes may be used in lieu of conductive bags.

Specific Handling Procedures for Static-Sensitive Items

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.

2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in Facilities for and Preparation for Working at Static-Free Workstation.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work-station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a customer. In that case, the QC engineer should contact the customer and negotiate an appropriate disposition.
4. It is the responsibility of the stockroom supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static-sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in the proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in ESD Labels and Signs in Work Areas.
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-senstive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.

8. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that the operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free workstation as discussed in Preparation for Working at a Static-Free Workstation. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with General Handling Procedures and Requirements, item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connectors shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semi-automatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the area supervisor to ensure that all personnel handling static-senstive items are familiar with this procedure and fully aware of the damage or possible degradation of these units inthe event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Customer-Returned-Item Handling Procedure

Receipt of ESD sensitive-labeled items is to be done at a static-free workstation and handled in accordance with applicable sections within this guideline.

Quality Control Provision

Sampling

Each manufacturing, stockroom, and testing operation handling ESD sensitive devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week)

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ± 10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week)

A visual inspection shall be made to determine full compliance with this specification at static-free workstations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded workstation.

Sleeve Protectors (minimum of once a week)

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week)

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electstatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month)

Conductive floors must have a resistance of not less than 100 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor three (3) feet apart shall be not less than100 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 99.

Records

Written records must be kept of all these QC audits.

Training

Training is applicable for all areas where individuals come in contact with ESD-sensitive devices. It is the responsibility of each area supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

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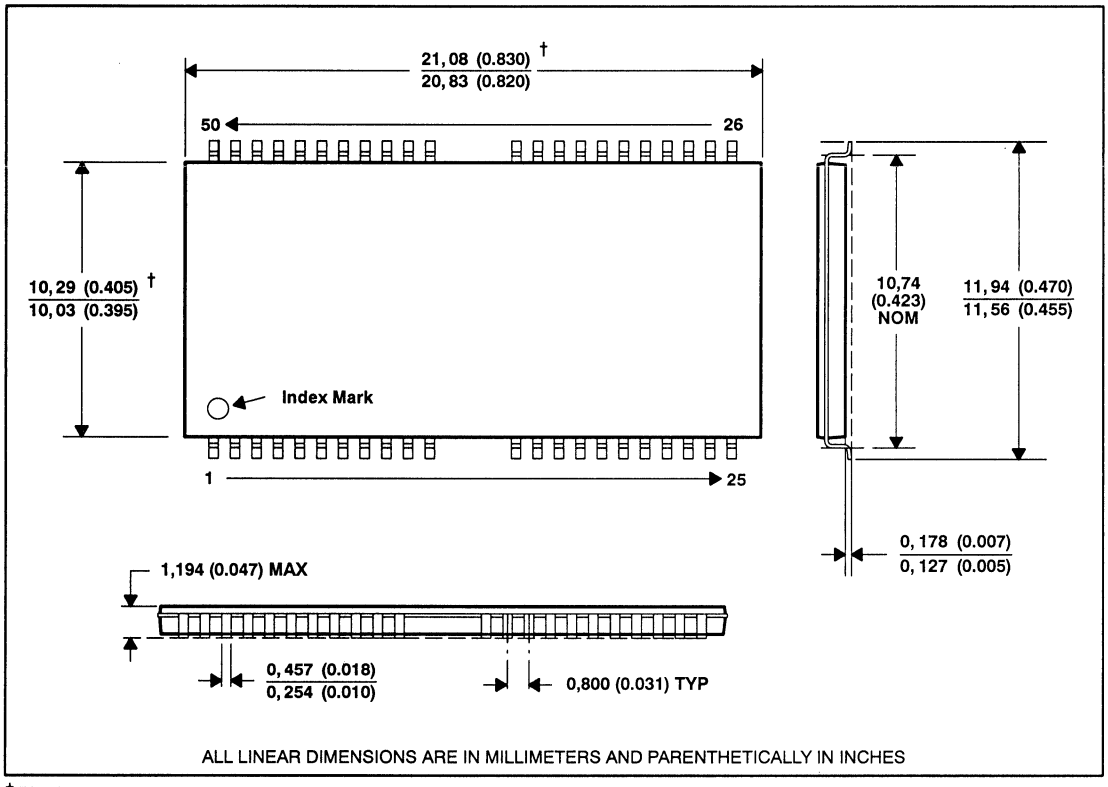
50/44-Lead Thin Small Outline Package (DC Suffix)‡

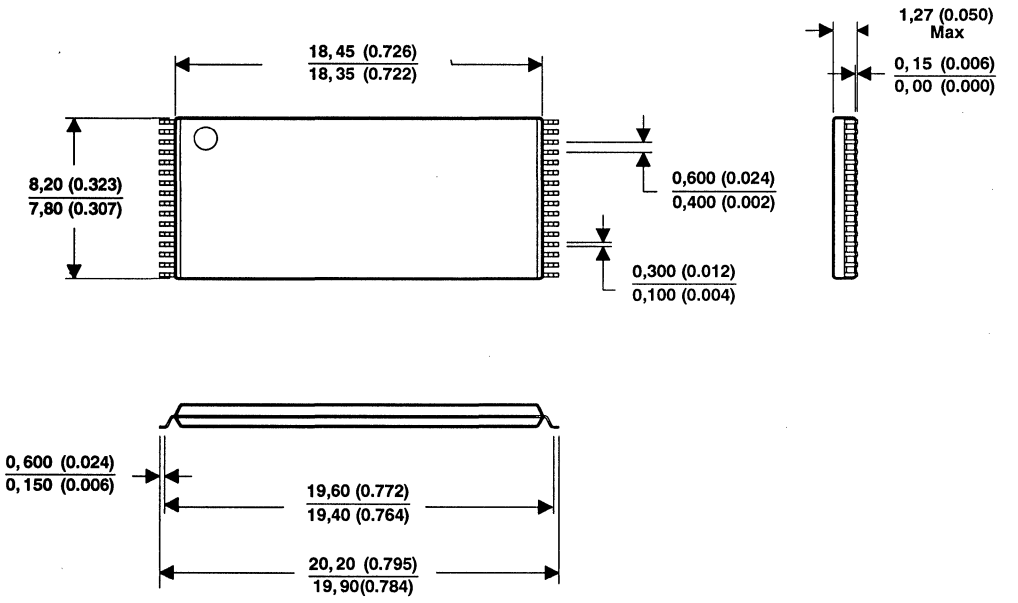


† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0, 254 mm (0.010) from the edge of the package bottom plastic.

‡ Applicable MOS Memory Devices:

TMS416160	TMS426160
TMS416160P	TMS426160P
TMS418160	TMS428160
TMS418160P	TMS428160P

32-Lead Plastic Thin Small-Outline J-Lead Package (TSOP) (DD Suffix/DU Suffix†)‡



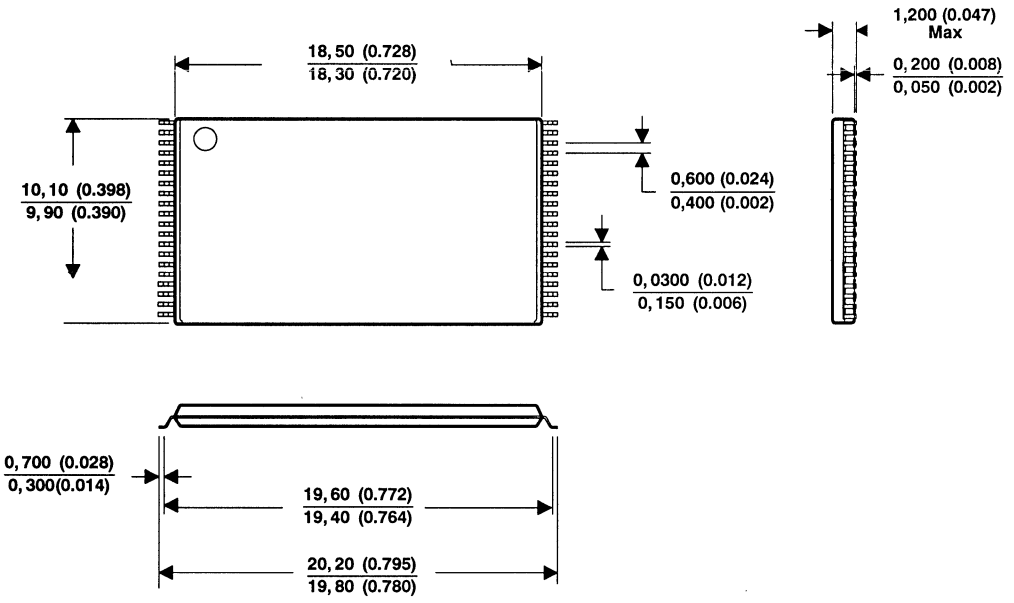
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† The DU suffix applies to the reverse form of the DD package shown above. All mechanical dimensions shown are applicable for both the DD and DU packages. Refer to the pinout drawings in the data sheet for correct pin numbers and index location for the DU package.

‡ Applicable MOS Memory Devices:

TM27LV010A
TMS27PC010A
TMS27PC512
TMS28F010
TMS28F512

40-Lead Plastic Thin Small-Outline J-Lead Package (TSOP) (DD Suffix/DU Suffix†)‡



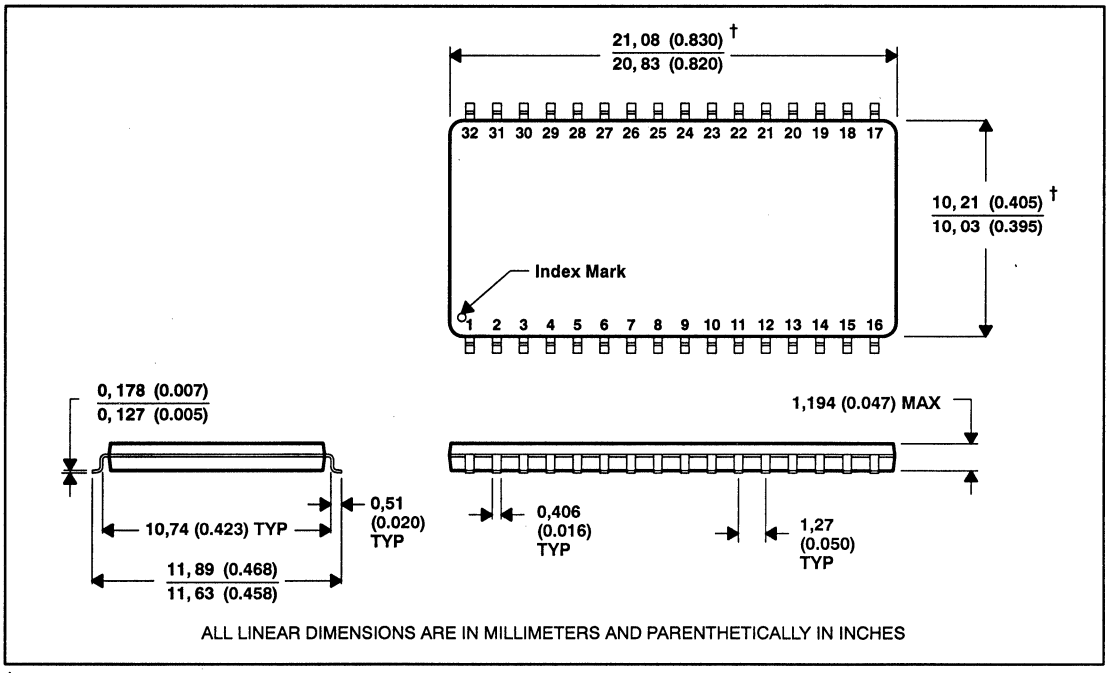
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† The DU suffix applies to the reverse form of the DD package shown above. All mechanical dimensions shown are applicable for both the DD and DU packages. Refer to the pinout drawings in the data sheet for correct pin numbers and index location for the DU package.

‡ Applicable MOS Memory Devices:

TMS28F040

32-Lead Plastic Thin Small Outline Package (TSOP) (DE Suffix)‡

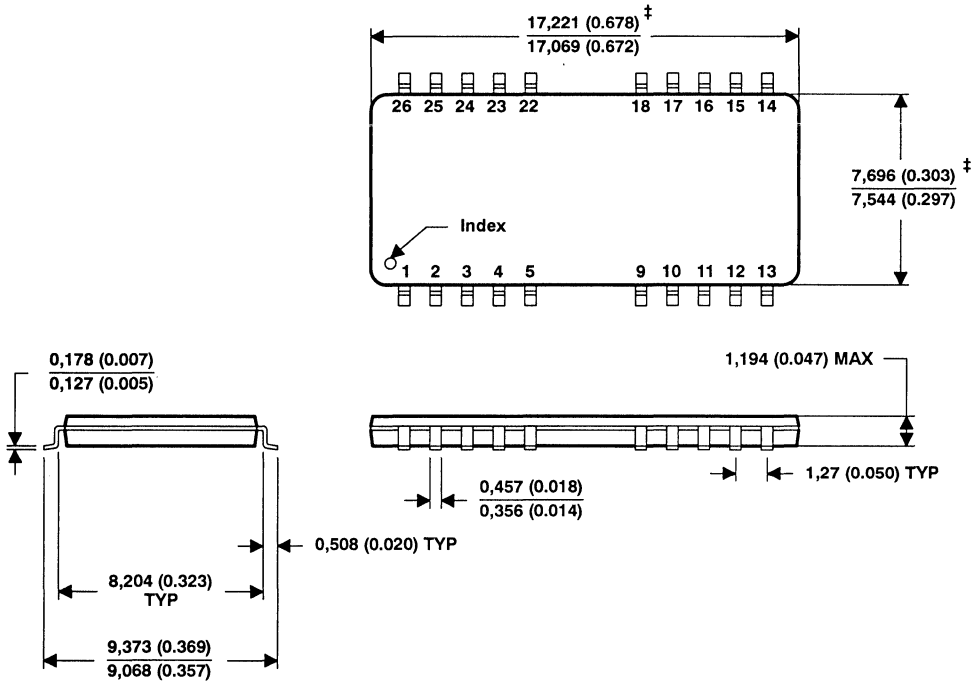


† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

‡ Applicable MOS Memory Devices:

TMS416800	TMS427800
TMS416800P	TMS427800P
TMS417800	TMS426800
TMS417800P	TMS426800P

20/26-Lead Small Outline Package (DGA Suffix/DGB Suffix†)§



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

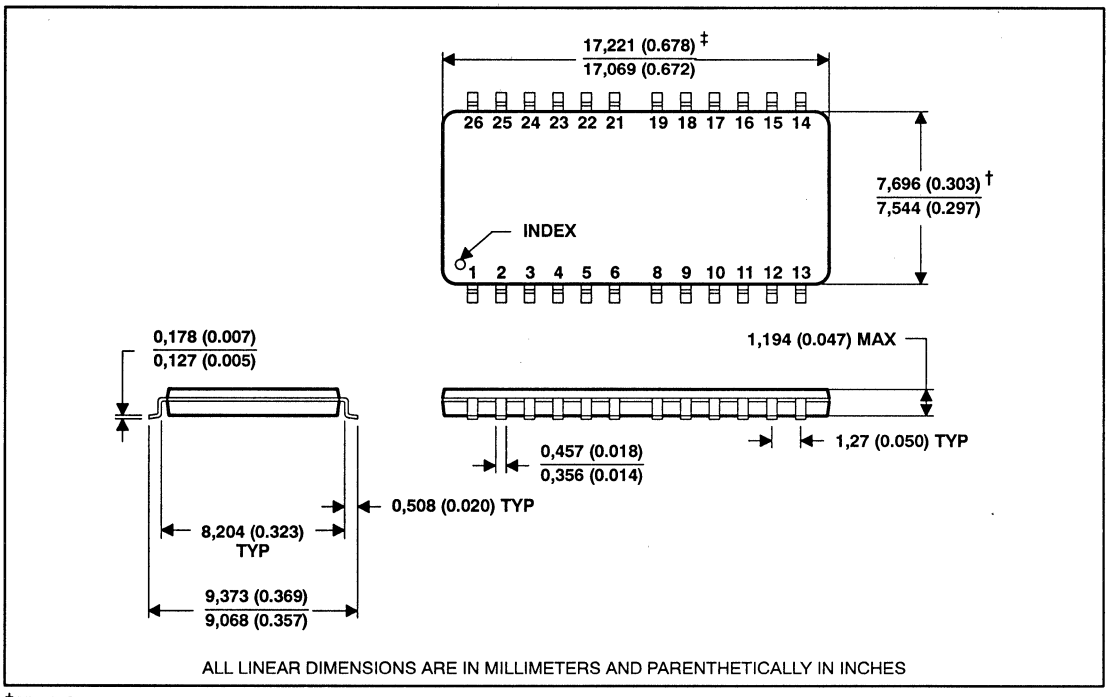
† The DGB package suffix applies to the reverse form of the DGA package shown above. All mechanical dimensions shown are applicable for both the DGA and DGB packages. Refer to the pinout drawings in the data sheet for correct pin numbers and index location for the DGB package.

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

§ Applicable MOS Memory Devices:

TMS44100	TMS46100
TMS44100P	TMS46100P
TMS44400	TMS46400
TMS44400P	TMS46400P

24/26-Lead Thin Small Outline Package (DGA Suffix/ DGB Suffix)†§



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† The DGB package suffix applies to the reverse form of the DGA package shown above. All mechanical dimensions shown are applicable for both the DGA and DGB packages. Refer to the pinout drawings in the data sheet for correct pin numbers and index location for the DGB package.

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

§ Applicable MOS Memory Devices:

TMS416100	TMS417400	TMS426400
TMS416100P	TMS417400P	TMS426400P
TMS416400	TMS426100	TMS427400
TMS416400P	TMS426100P	TMS427400P

NOTE: The package information on this page also applies to the Product Preview version of the TMS416100, TMS416100P, TMS416400, TMS416400P, TMS417400, and TMS417400P devices.

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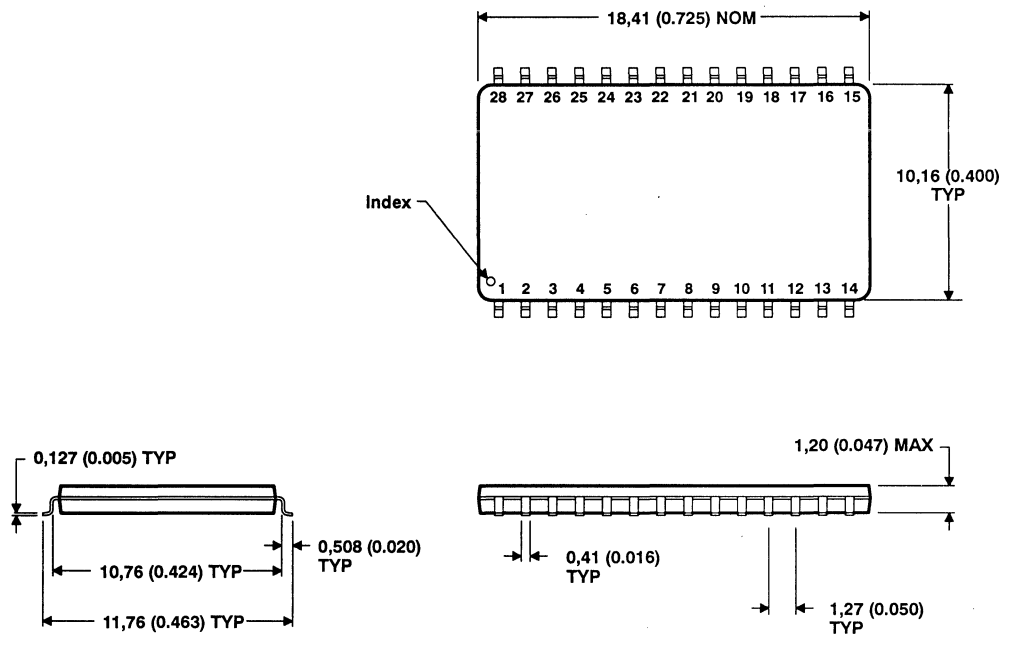
28-Lead Plastic Thin Small Outline Package (TSOP) (DGC Suffix)†

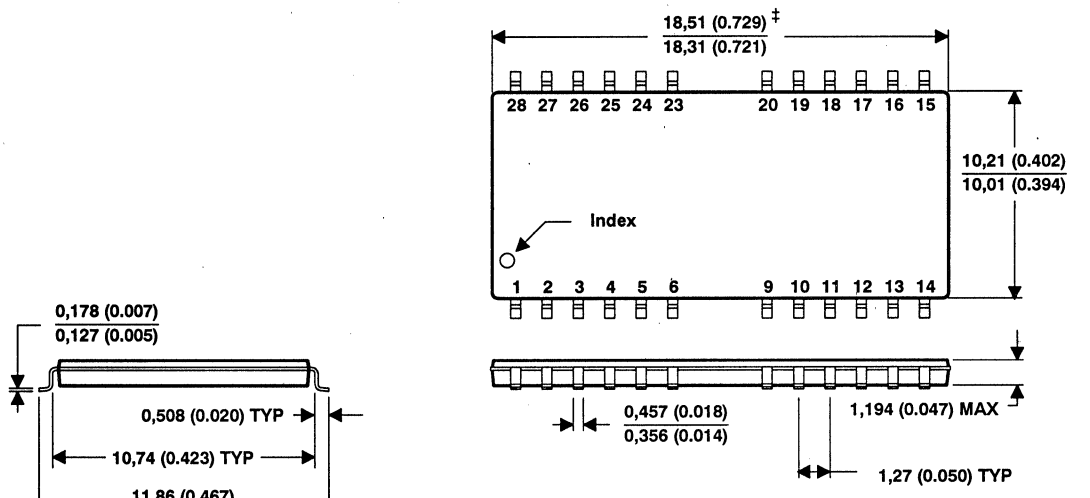


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS44800
TMS44800P

24/28-Lead Thin Small Outline Package (DGC Suffix/DGD Suffix†)§



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

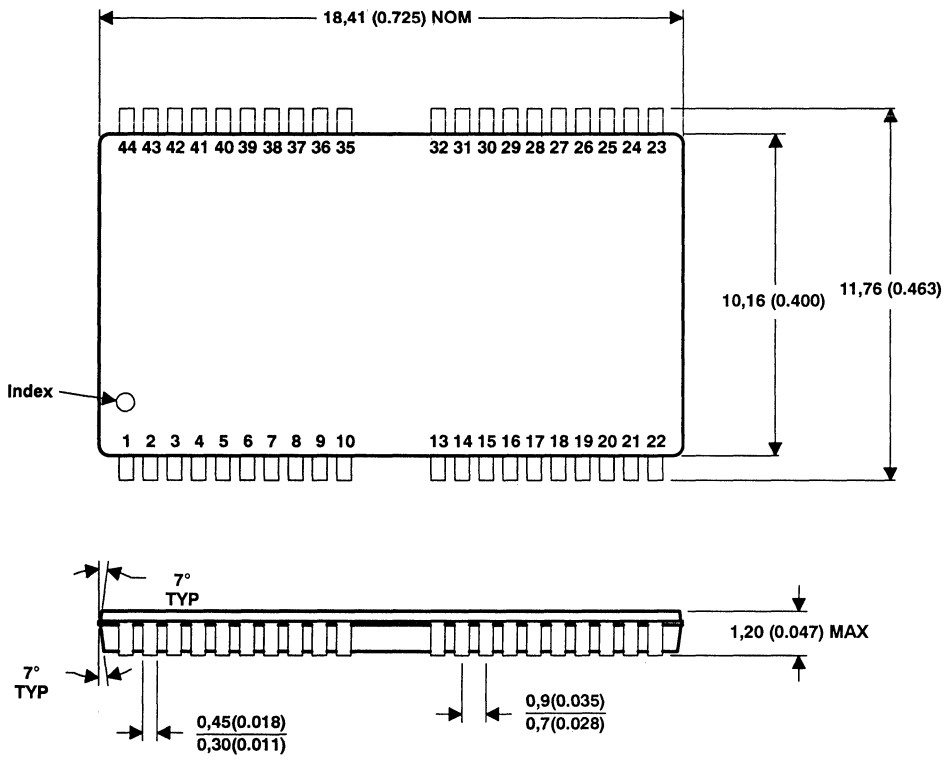
† The DGD package suffix applies to the reverse form of the DGC package shown above. All mechanical dimensions shown are applicable for both the DGC and DGD packages. Refer to the pinout drawings for correct pin numbers and index location for the DGD package.

‡ Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic .

§ Applicable MOS Memory Devices:

TMS416400
TMS416100
TMS417400

40/44-Lead Thin Small Outline Package (DGE Suffix)†

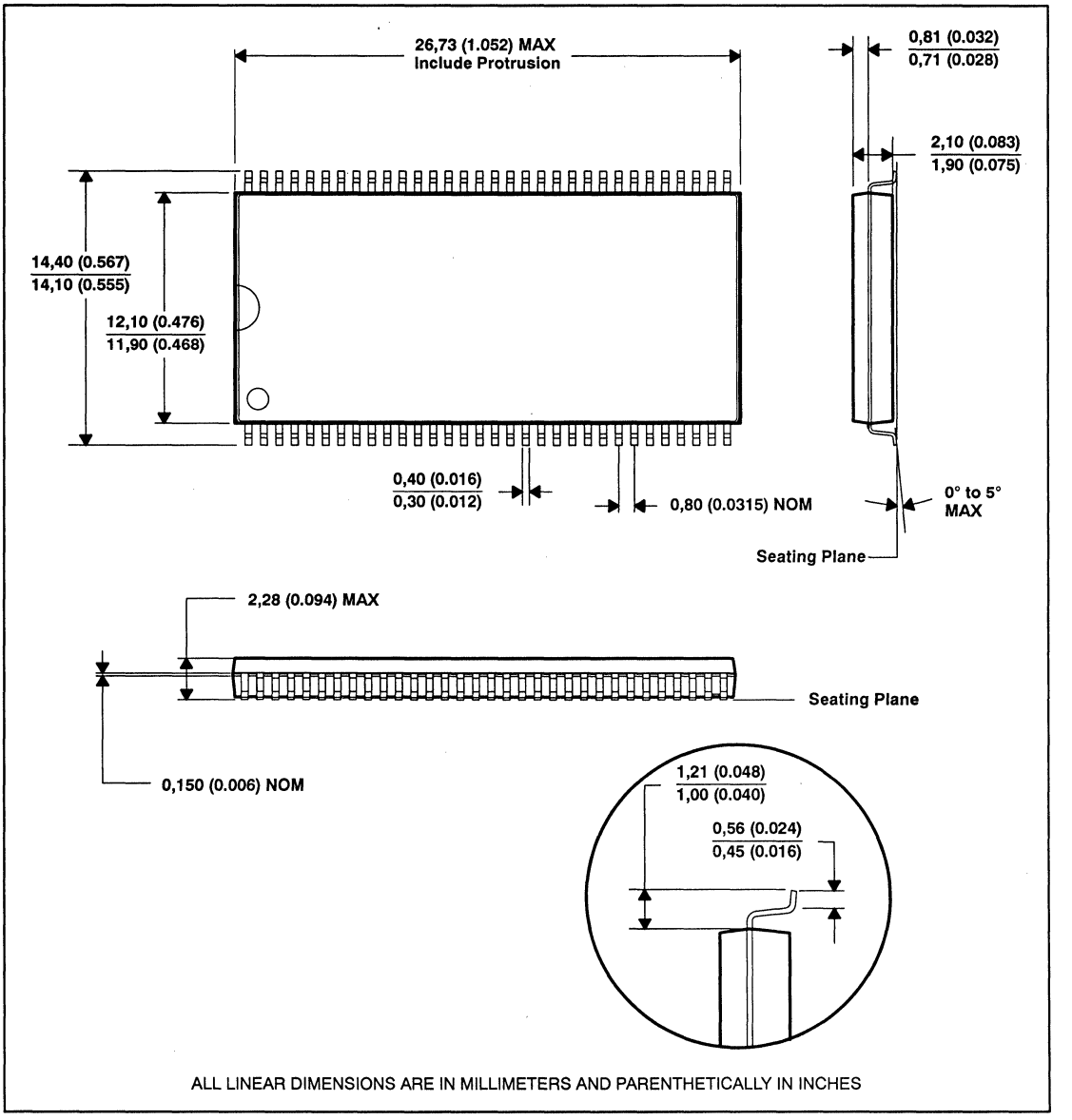


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

SDRAM	TMS45160P
TMS44165	TMS45165
TMS44165P	TMS45165P
TMS45160	

64-Lead Small Outline Package (DGH Suffix)†

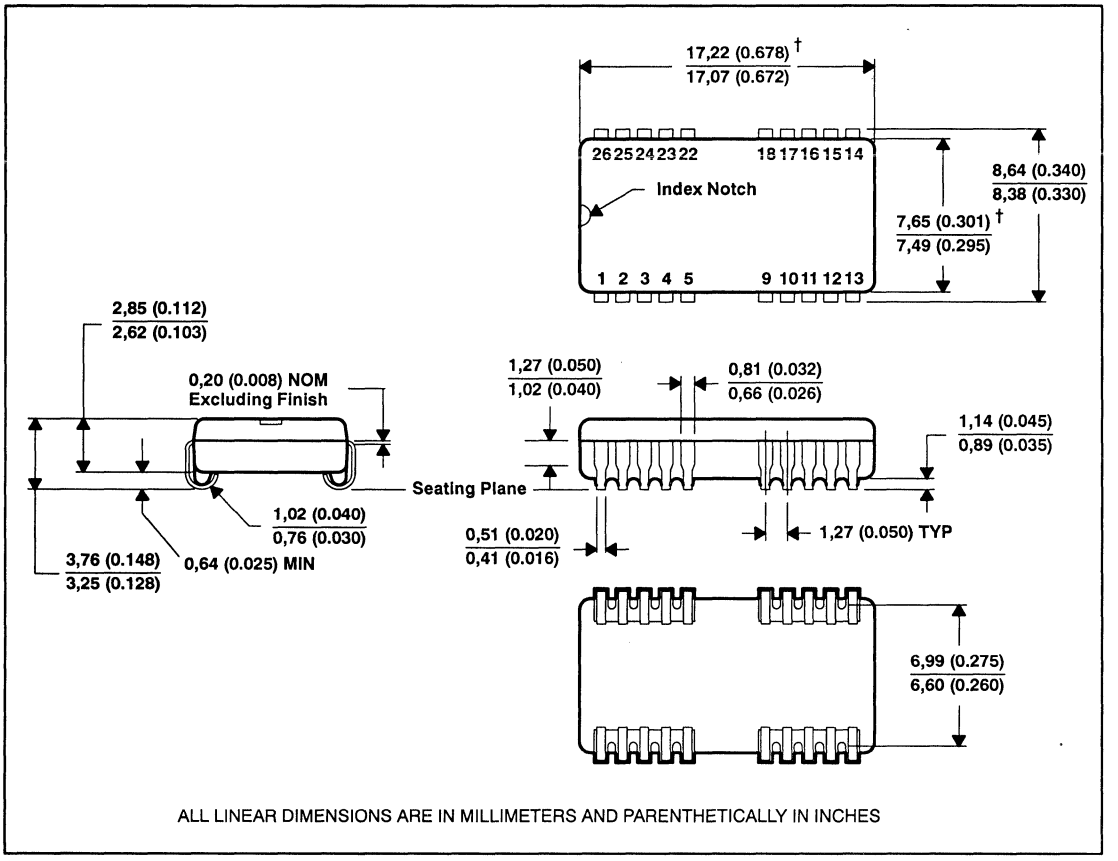


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS55160
TMS55165

20/26-Lead Plastic Small-Outline J-Lead Package (SOJ) (DJ Suffix)†‡

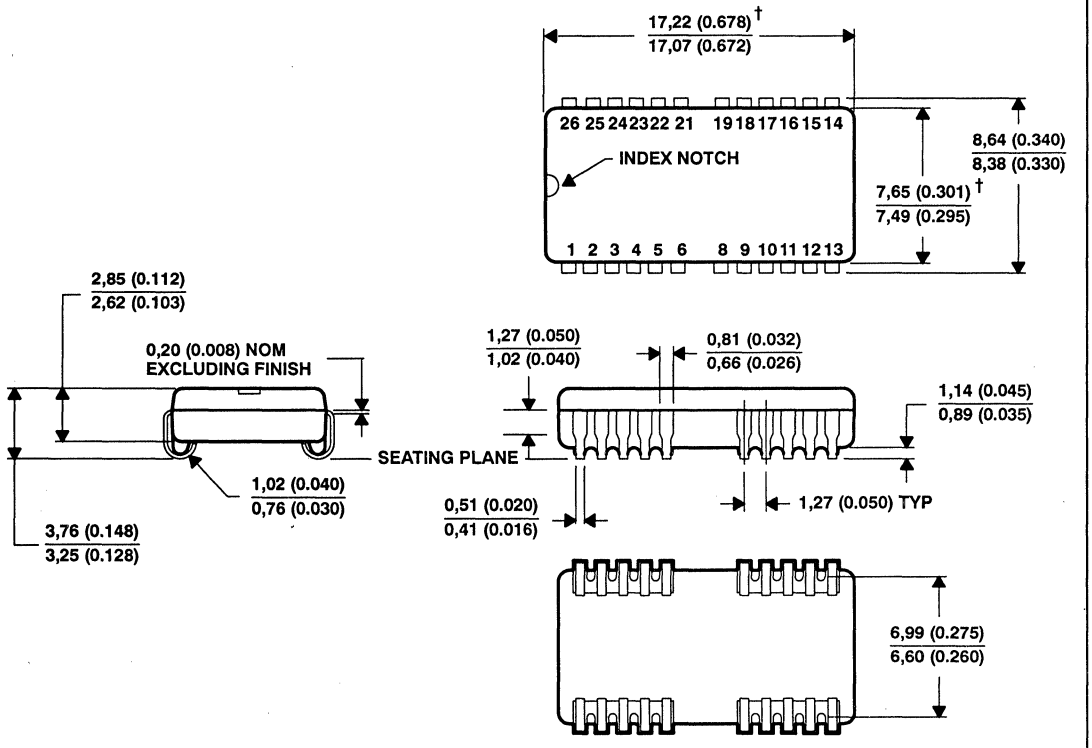


† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

‡ Applicable MOS Memory Devices:

TMS4C1024	TMS4C1060B	TMS44400	TMS4610P
TMS4C1025	TMS44100	TMS44400P	TMS46400
TMS4C1027	TMS44100P	TMS46100	TMS46400P
TMS4C1050B			

24/26-Lead Plastic Small-Outline J-Lead Package (SOJ) (DJ Suffix)‡



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

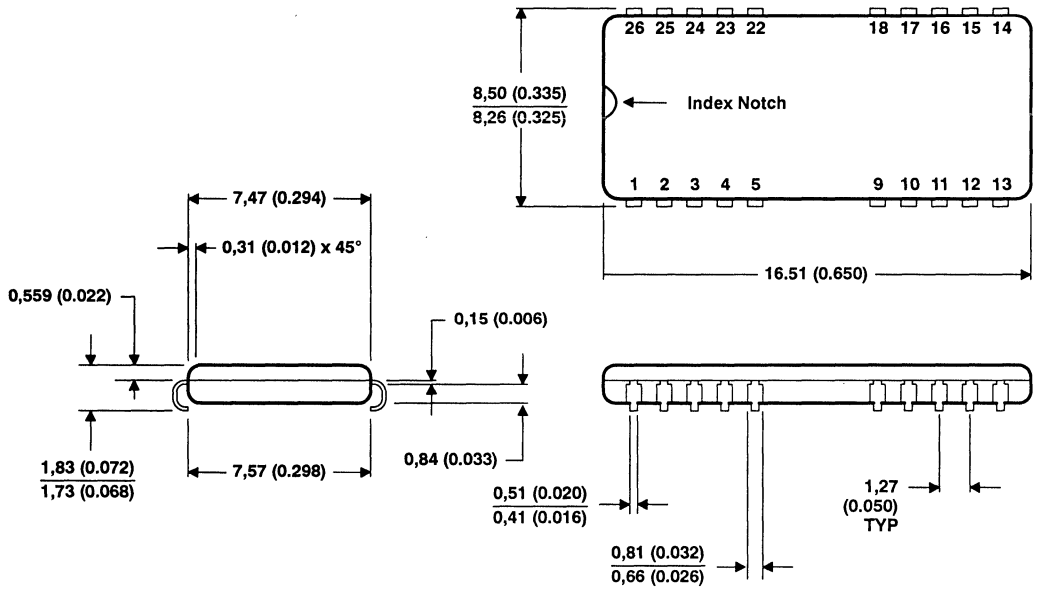
† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

‡ Applicable MOS Memory Devices:

TMS416100	TMS417400	TMS426400	TMS44C260
TMS416100P	TMS417400P	TMS426400P	TMS48C128
TMS416400	TMS426100	TMS427400	TMS48C138
TMS416400P	TMS426100P	TMS427400P	

NOTE: The package information on this page also applies to the Product Preview version of the TMS416100, TMS416100P, TMS416400, TMS416400P, TMS417400, and TMS417400P devices.

20/26 Thin Small-Outline J-Lead Package (DN)†

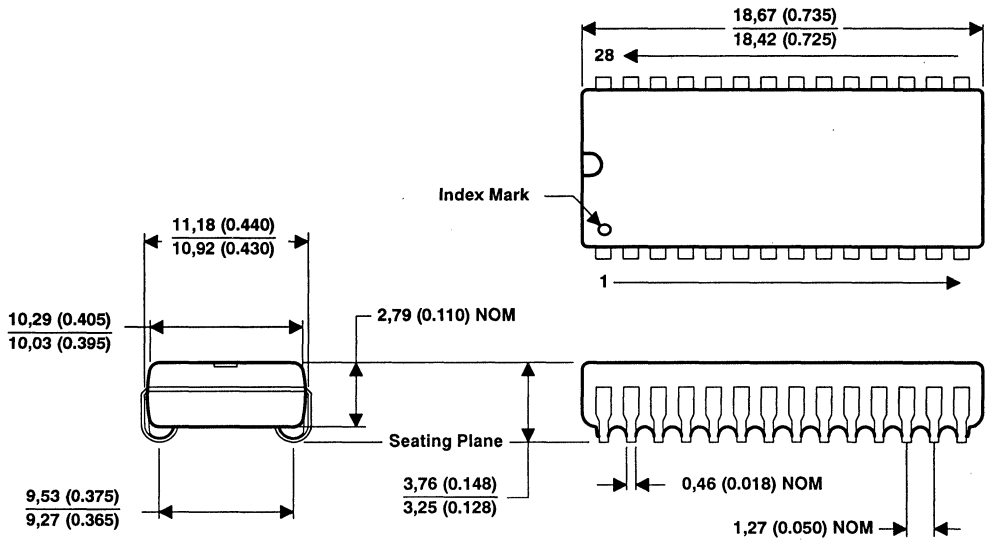


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS44C256
TMS4C1024
TMS4C1025
TMS4C1027

28-Lead Plastic Small Outline J-Lead Surface Mount Package (DZ Suffix)†

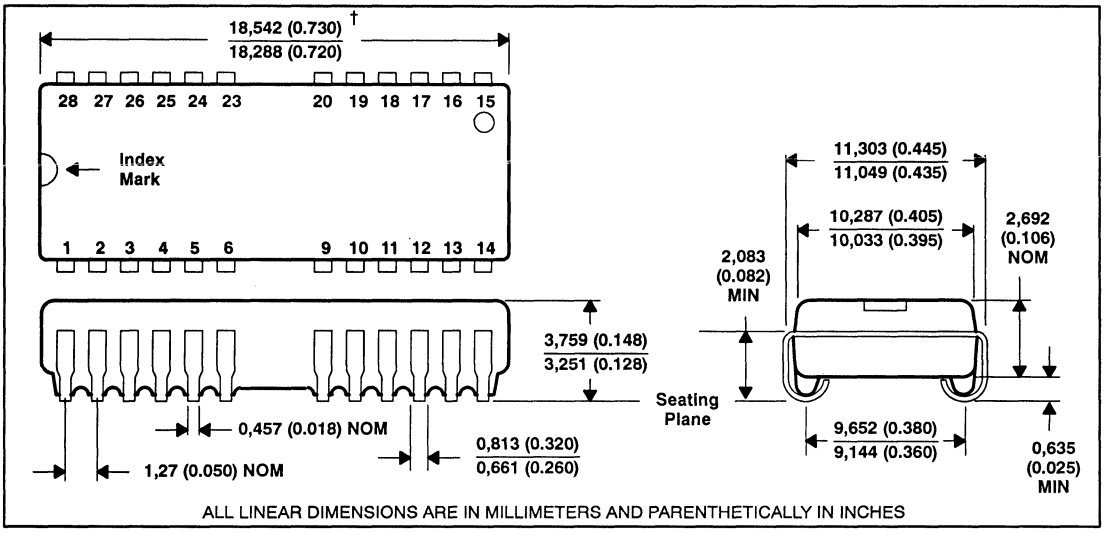


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS416800	TMS426800P
TMS416800P	TMS427800
TMS417800	TMS427800P
TMS417800P	TMS44800
TMS426800	TMS44800P

28/24-Lead Plastic Small Outline J-Lead Surface Mount Package (DZ Suffix)‡

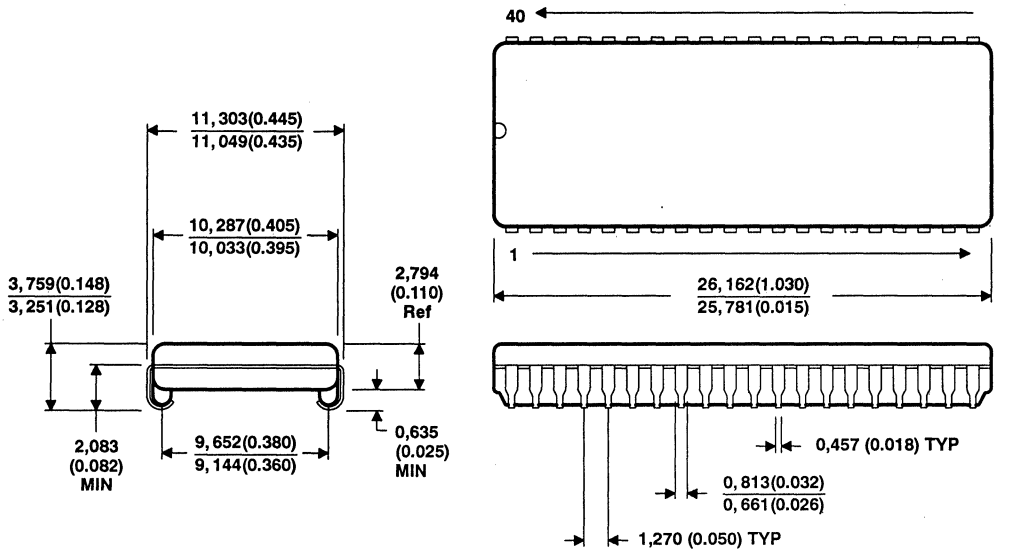


† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010) from the edge of the package bottom plastic.

‡ Applicable MOS Memory Devices:

TMS416100
TMS416400
TMS417400

40-Lead Plastic Small Outline J-Lead Surface Mount Package (DZ suffix)†

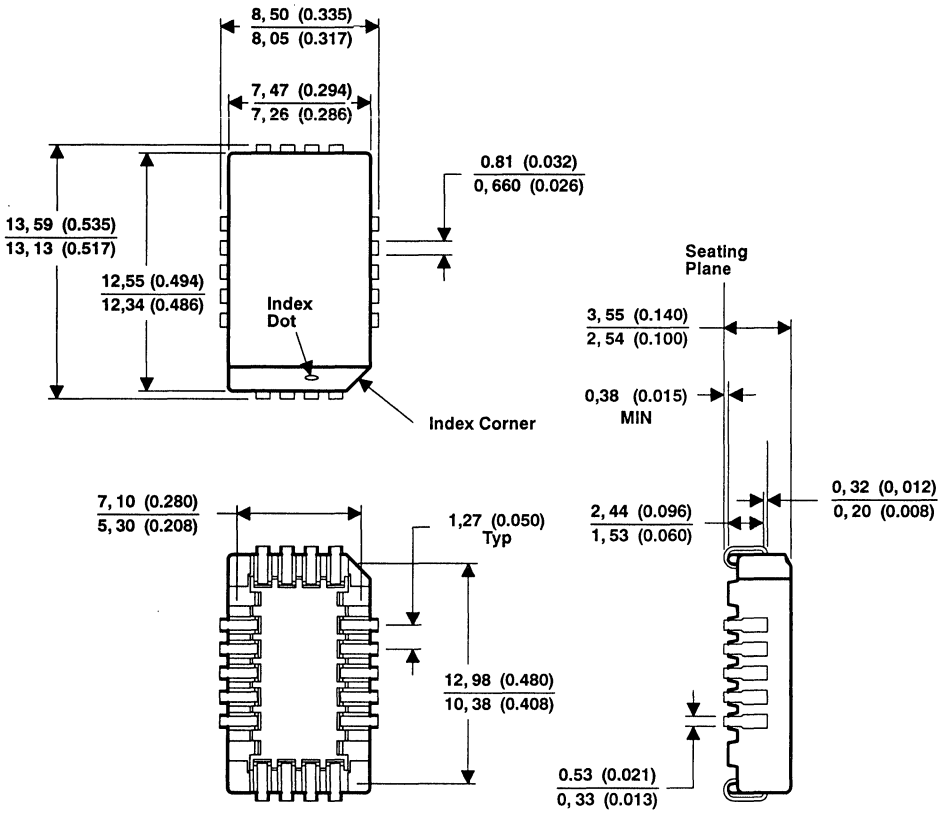


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS44165	TMS45160P
TMS44165P	TMS45165
TMS45160	TMS45165P

18-Lead Plastic Leaded Chip Carrier (PLCC) (FM Suffix)†

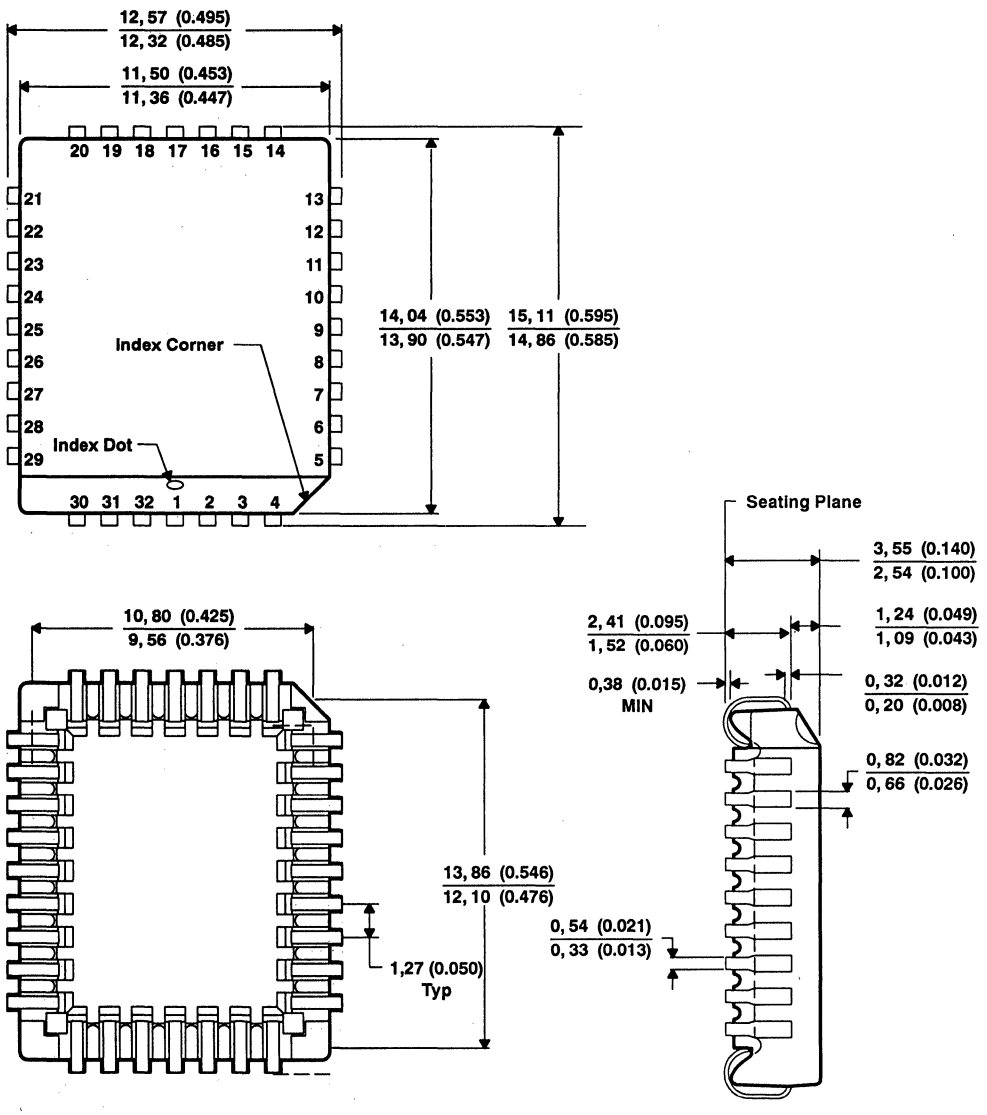


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS29F816

32-Lead Plastic Leaded Chip Carrier Package (PLCC) (FM suffix)†

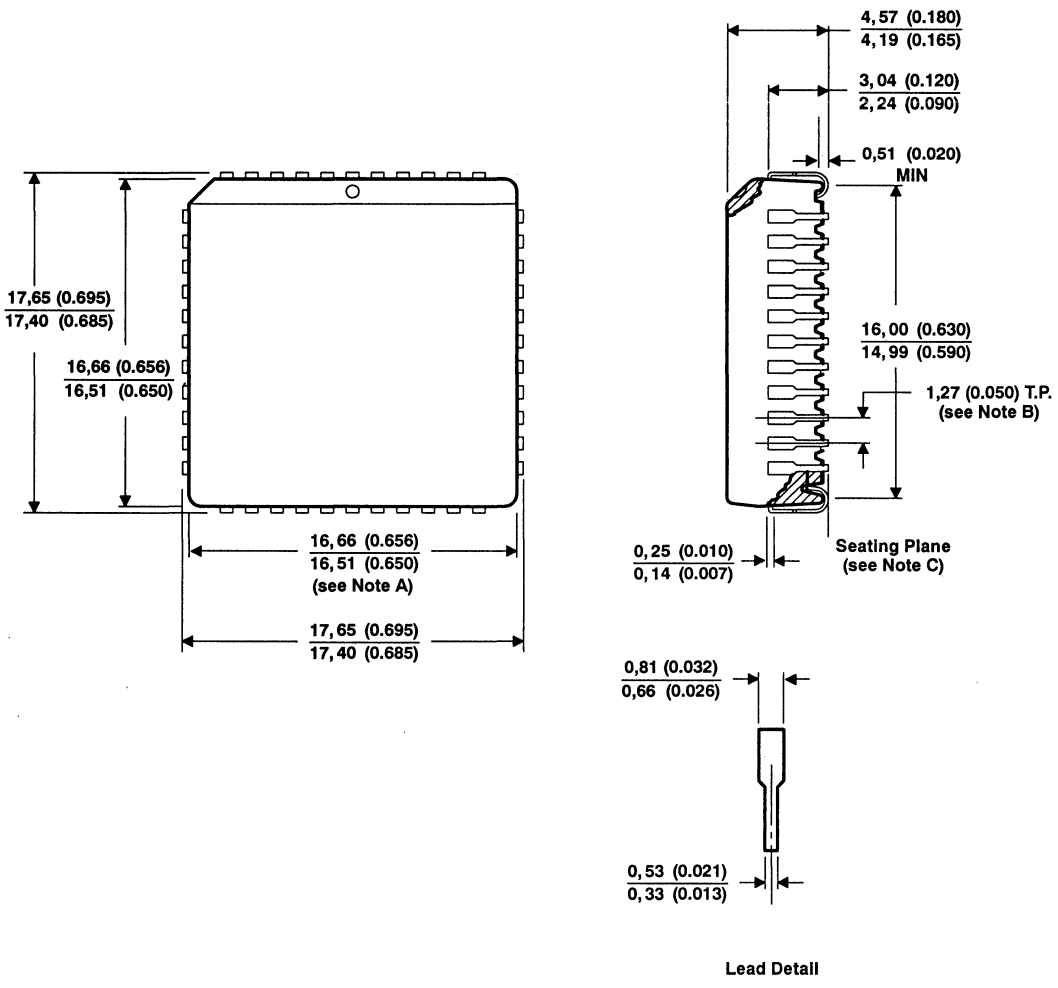


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TMS27LV010A	TMS27PC040	TMS27PC512
TMS27PC010A	TMS27PC256	TMS28F010
TMS27PC020	TMS27PC510	TMS28F512

44-Lead Plastic Leaded Chip Carrier Package (PLCC) (FN suffix)†



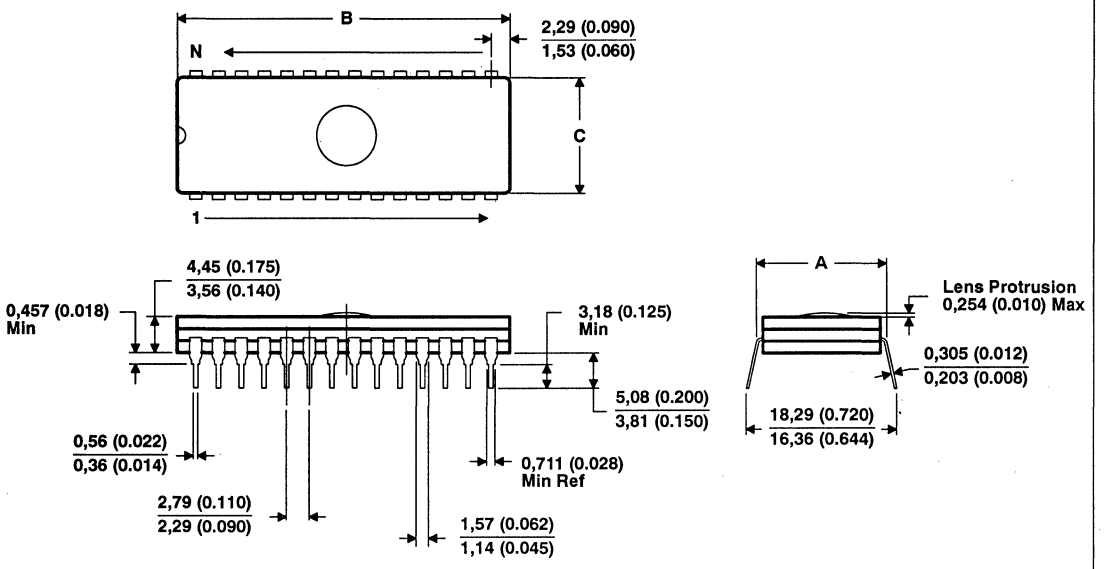
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by this dimension.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center of pin on each side.
C. The lead contact points are planar within 0,101 (0.004).

† Applicable MOS Memory Devices:

TMS27PC210A
TMS27PC240
TMS28F210

Ceramic Dual-In-Line Package (J Suffix)†



PIN / DIM	24	28	32	40
A (Max)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)
B (Max)	32,13 (1.265)	37,21 (1.465)	42,37 (1.668)	52,53 (2.068)
C (Max)	14,25 (0.561)	14,25 (0.561) ‡	14,25 (0.561)	14,25 (0.561)

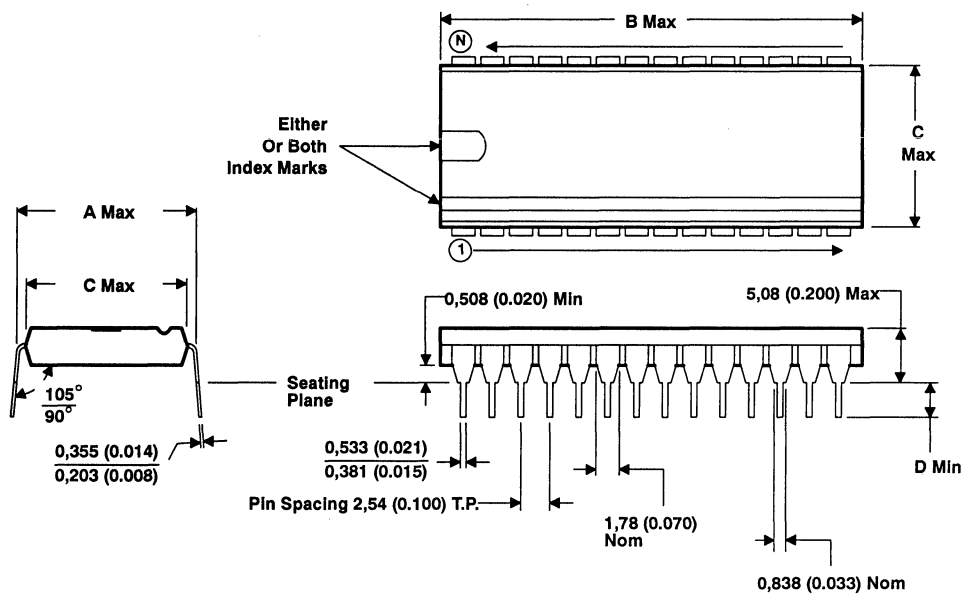
‡ This dimension pertains to TMS27C128, TMS27C256, and TMS27C512 only.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

28-PIN	32-PIN	40-PIN
TMS27C128	TMS27C010A	TMS27C210A
TMS27C256	TMS27C020	TMS27C240
TMS27C512	TMS27C040	TMS27C400
	TMS27C510	
	TMS27LV010A	

Plastic Dual-In-Line Package (N Suffix)†



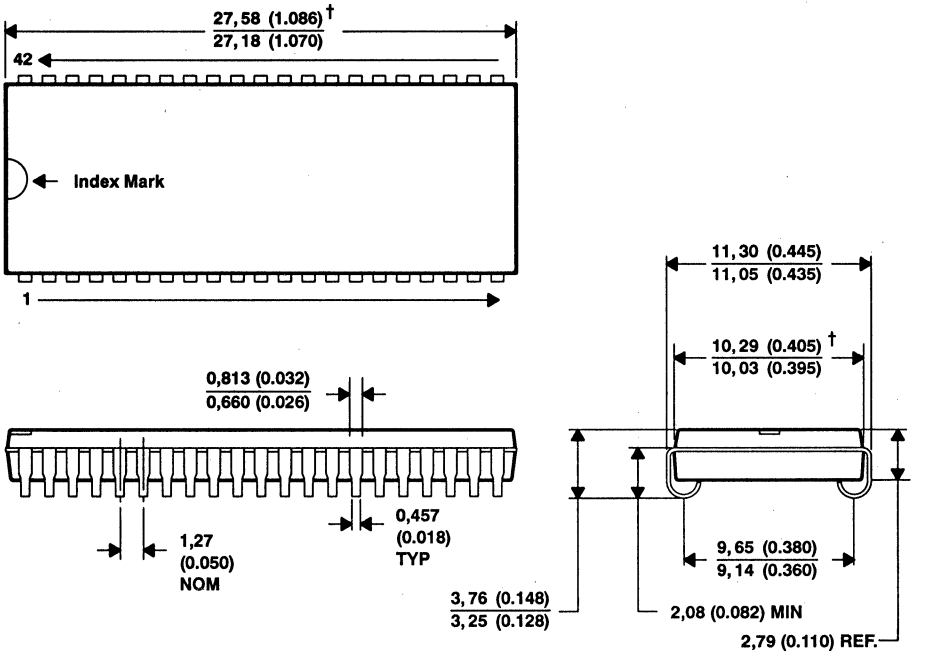
DIM \ PIN		16	18	20	28	32	40
A	(Max)	7,874 (0.325)	8,26 (0.325)	8,26 (0.325)	15,87 (0.625)	15,87 (0.625)	15,87 (0.625)
B	(Max)	20,32 (0.870)	22,86 (0.899)	25,40 (1.000)	39,70 (1.565)	41,42 (1.670)	52,70 (2.075)
C	(Max)	7,10 (0.270)	6,86 (0.270)	6,86 (0.270)	14,73 (0.580)	14,22 (0.560)	13,97 (0.550)
D	(Min)	3,00 (0.125)	3,00 (0.118)	3,00 (0.118)	2,93 (0.115)	3,18 (0.125)	2,54 (0.100)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

16-PIN	18-PIN	20-PIN	28-PIN	32-PIN	40-PIN
TMS4C1050B	TMS4C1024	TMS44C256	TMS27PC128	TMS27LV010A	TMS27PC400
TMS4C1060B	TMS4C1025		TMS27PC256	TMS27PC010A	TMS28F210
	TMS4C1027		TMS27PC512	TMS28F010	
	TMS4C1070B		TMS29F256	TMS28F040	
			TMS29F258	TMS28F512	
			TMS29F259		

42-Lead Plastic Small Outline J-Lead Surface Mount Package (RE Suffix)‡



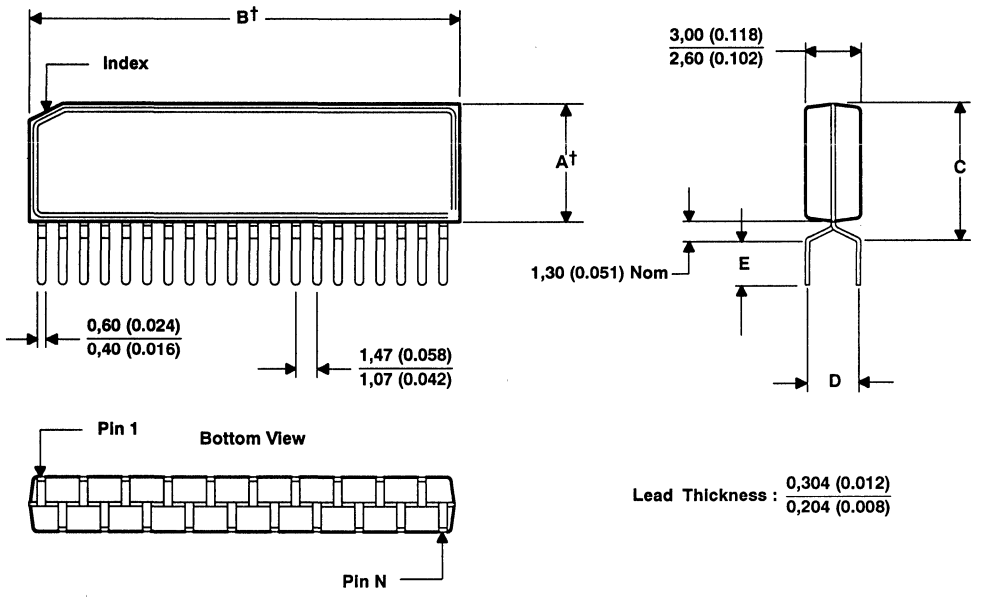
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0, 254 mm (0.010) from the edge of the package bottom plastic.

‡ Applicable MOS Memory Devices:

TMS416160	TMS426160
TMS416160P	TMS426160P
TMS418160	TMS428160
TMS418160P	TMS428160P

20-Lead Zig-Zag Plastic Package (SD Suffix)‡



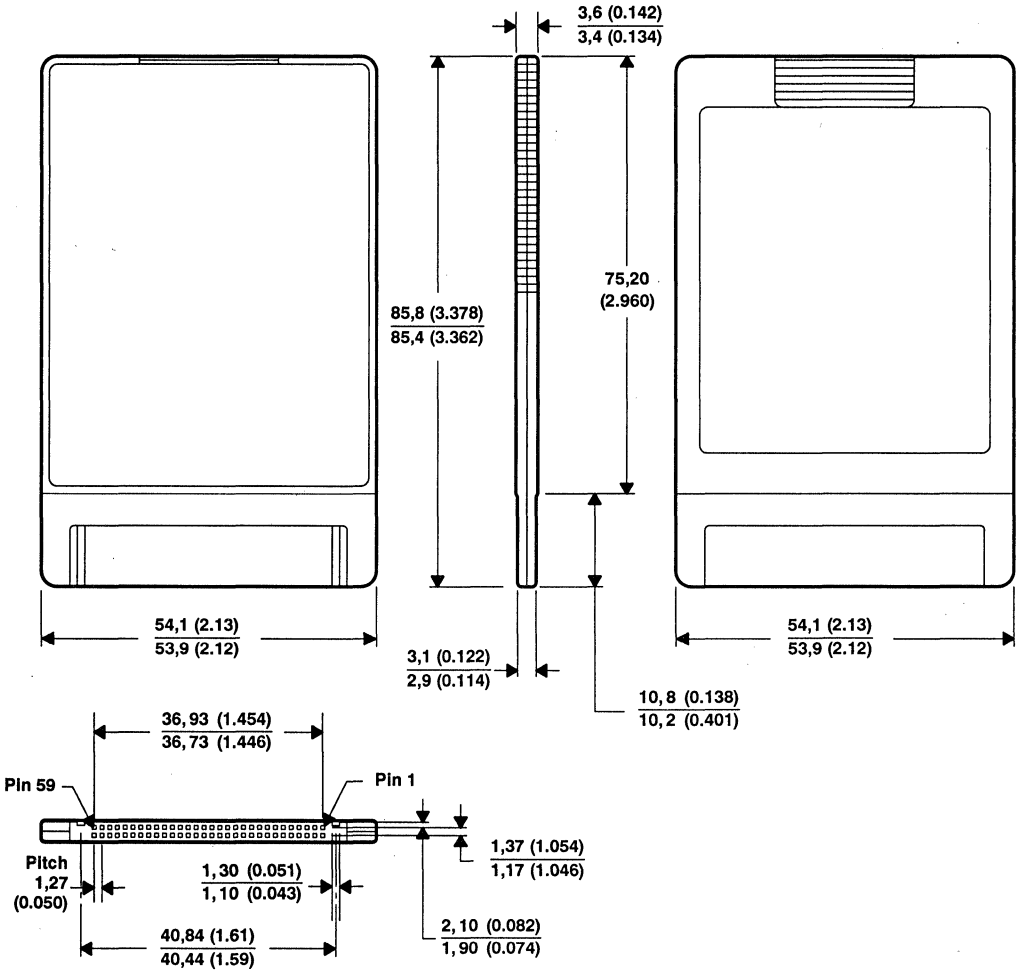
DIM \ PIN	16	20	24	28
A†	7,00 (0.276) 6,80 (0.268)	8,69 (0.342) MAX	8,74 (0.344) MAX	6,09 (0.342) NOM
B†	20,70 (0.815) 20,30 (0.799)	26,42 (1.040) MAX	31,29 (1.232) MAX	36,07 (1.420) NOM
C (MAX)	8,26 (0.325)	10,16 (0.400) MAX	10,16 (0.400)	10,16 (0.400)
D	2,79 (0.110) 2,29 (0.090)	2,79 (0.110) 2,29 (0.090)	2,64 (0.104) 2,44 (0.096)	2,64 (0.104) 2,44 (0.096)
E	3,30 (0.130) 3,00 (0.120)	3,30 (0.130) 3,00 (0.118)	3,25 (0.128) 2,95 (0.116)	3,25 (0.1268) 2.95 (0.116)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,125 (0.005).
‡ Applicable MOS Memory Devices:

TMS4C1024	TMS4C1060B	TMS44400	TMS46100P
TMS4C1025	TMS44C256	TMS44400P	TMS46400
TMS4C1027	TMS44100	TMS46100	TMS46400P
TMS4C1050B	TMS44100P		

60-Lead Memory Card†

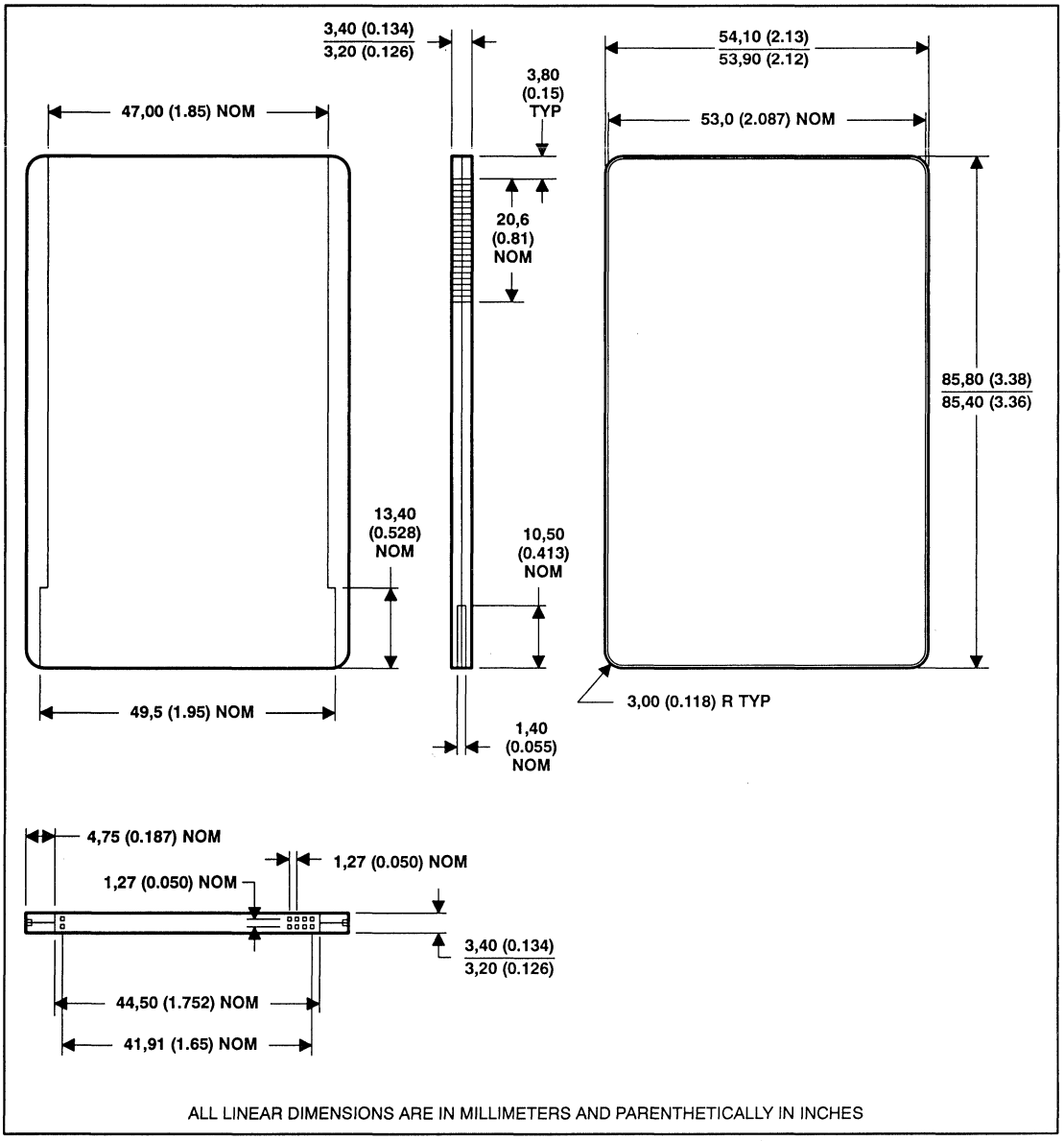


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

CMS209	CMS214	CMS403	CMS407
CMS210	CMS216	CMS404	CMS408
CMS212	CMS401	CMS405	CMS409
CMS213	CMS402	CMS406	CMS410

68-Lead Memory Card†

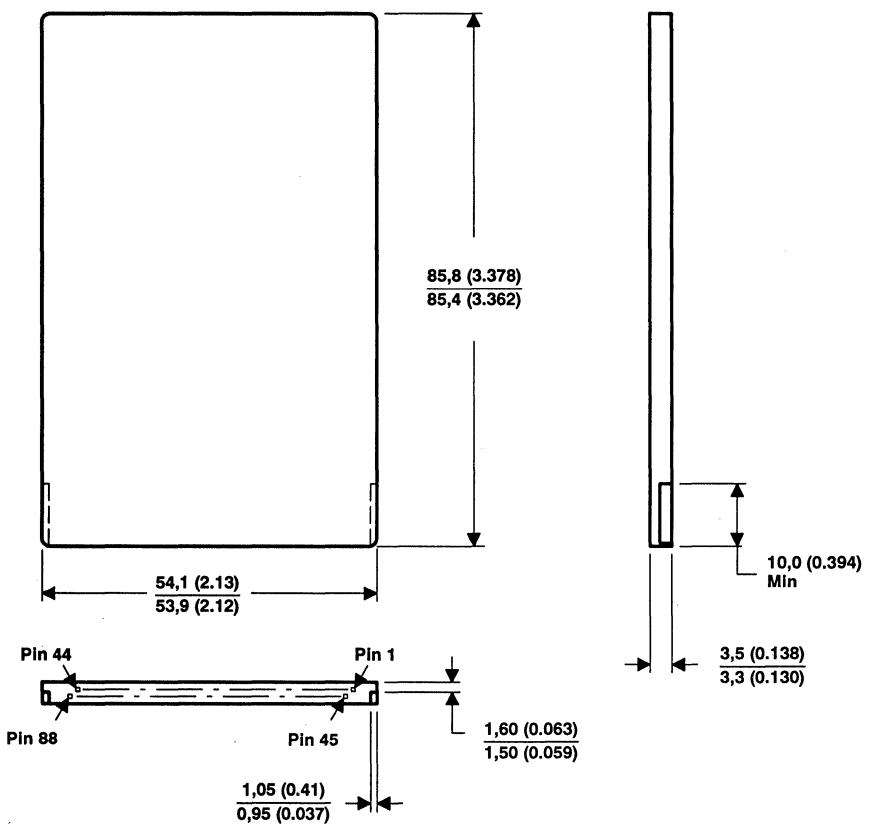


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

CMS68F256	CMS68P256
CMS68F512	CMS68P512
CMS68F1MB	CMS68P1MB
CMS68F2MB	

88-Lead Memory Card†



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

CMS88D4MB36
CMS88D8MB36

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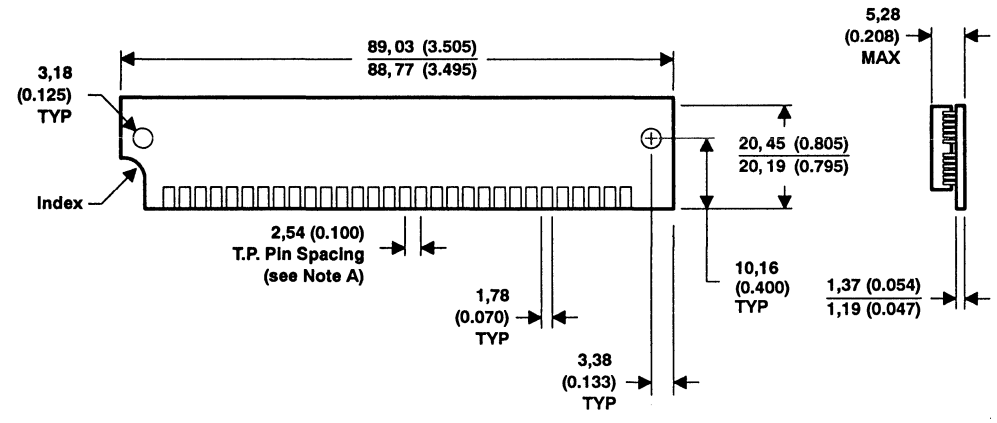
30-Lead AD Single-In-Line Memory Module

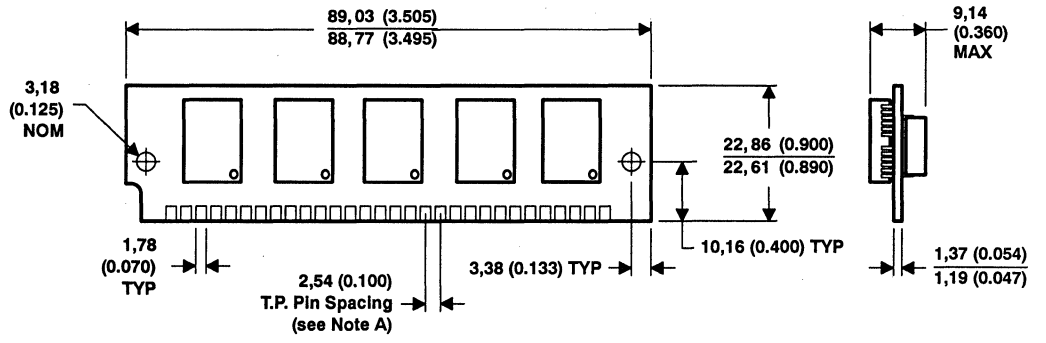


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TM024EAD9
TM024GAD8
TM4100EAD9
TM4100GAD8
TM497EAD9B
TM497GAD8A

30-Lead Single-/Double-Sided BD Single In-Line Memory Module†

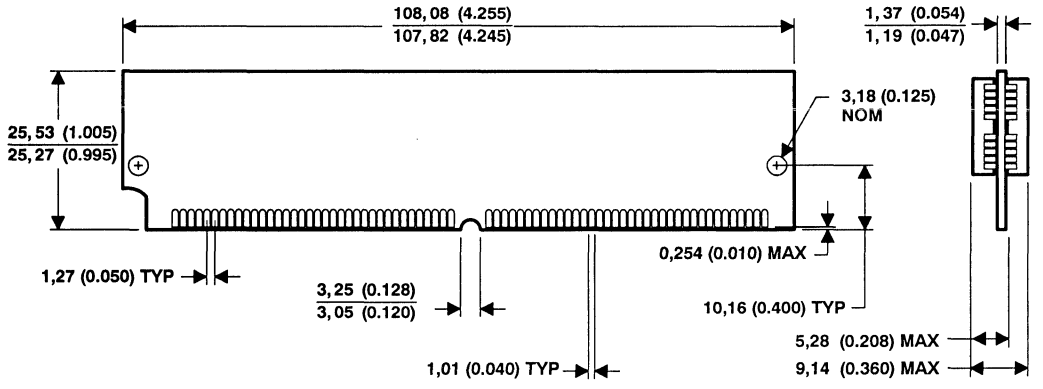


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TM16100EBD9
TM16100GBD8

72-Lead BK Single-/Double-Sided Memory Module†

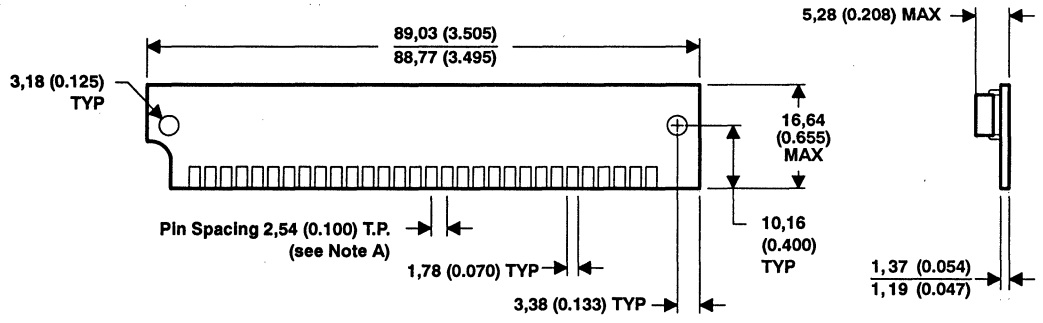


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

TM124BBK32·	TM248CBK32S	TM256KBK36R	TM512CBK32S
TM124BBK32S	TM248NBK36B	TM256KBK36S	TM512LBK36B
TM124MBK36	TM248NBK36C	TM496TBM40	TM512LBK36C
TM124MBK36B	TM248NBK36R	TM496TBM40S	TM512LBK36R
TM124MBK36C	TM248NBK36S	TM497BBK32	TM512LBK36S
TM124MBK36Q	TM248VBK40	TM497BBK32S	TM892VBM40
TM124MBK36R	TM248VBK40S	TM497MBK36A	TM892VBM40S
TM124MBK36S	TM256BBK32	TM497MBK36Q	TM893CBK32
TM124TBK40	TM256BBK32S	TM497TBM40	TM893CBK32S
TM124TBK40S	TM256KBK36B	TM497TBM40S	TM893VBM40
TM248CBK32	TM256KBK36C	TM512CBK32	TM893VBM40S

30-Lead U Single In-Line Memory Module†

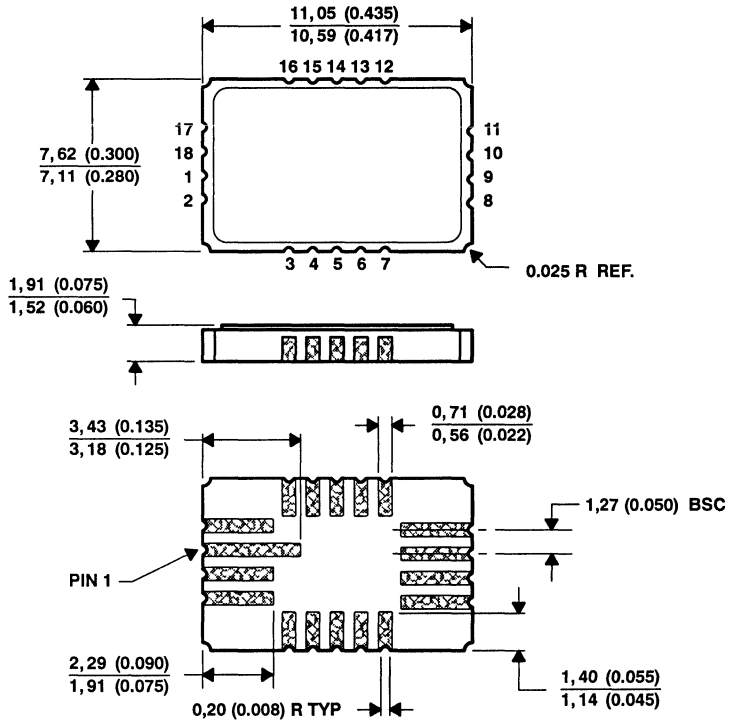


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Applicable MOS Memory Devices:

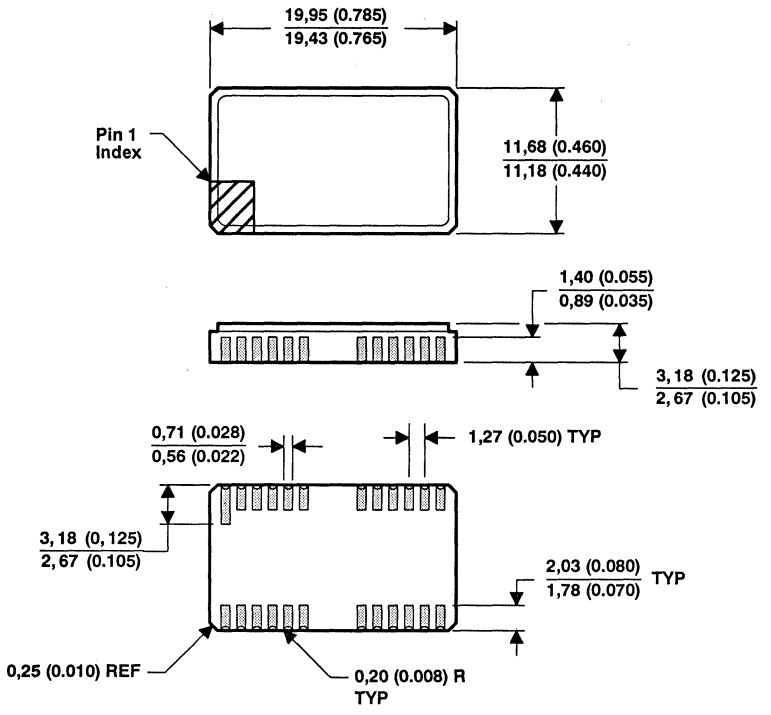
TM124EU9B
TM124EU9C
TM124GU8A

18-Lead Ceramic Chip Carrier Package (FG Suffix)



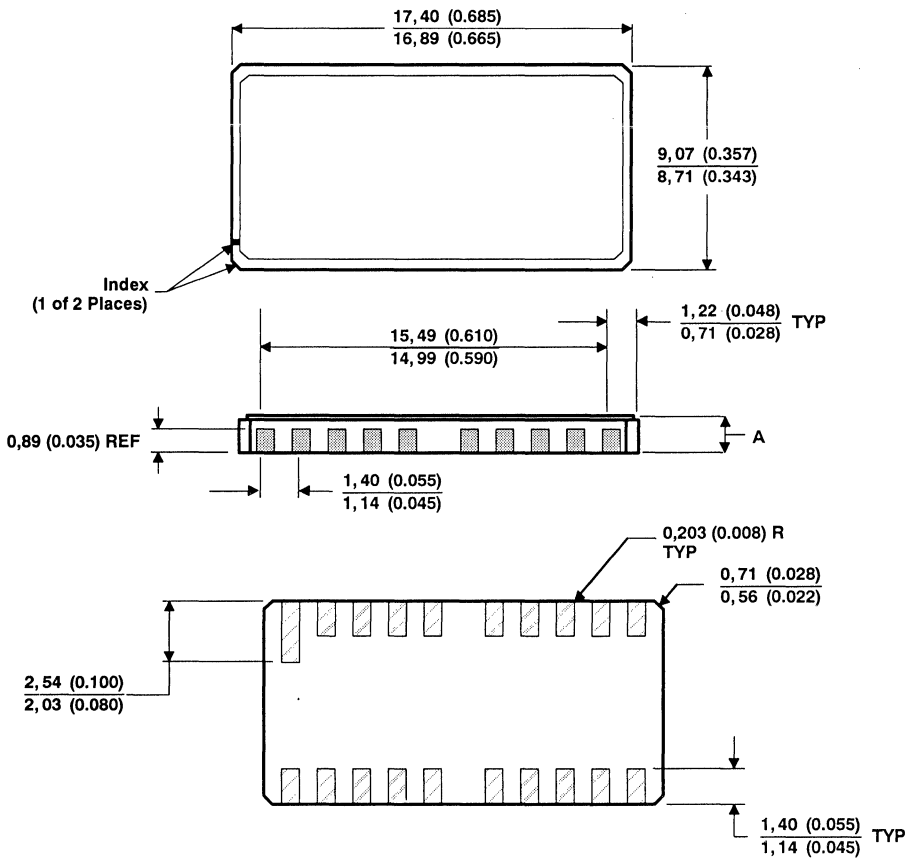
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

28/24-Lead Small Outline Leadless Ceramic Chip Carrier (FNC Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

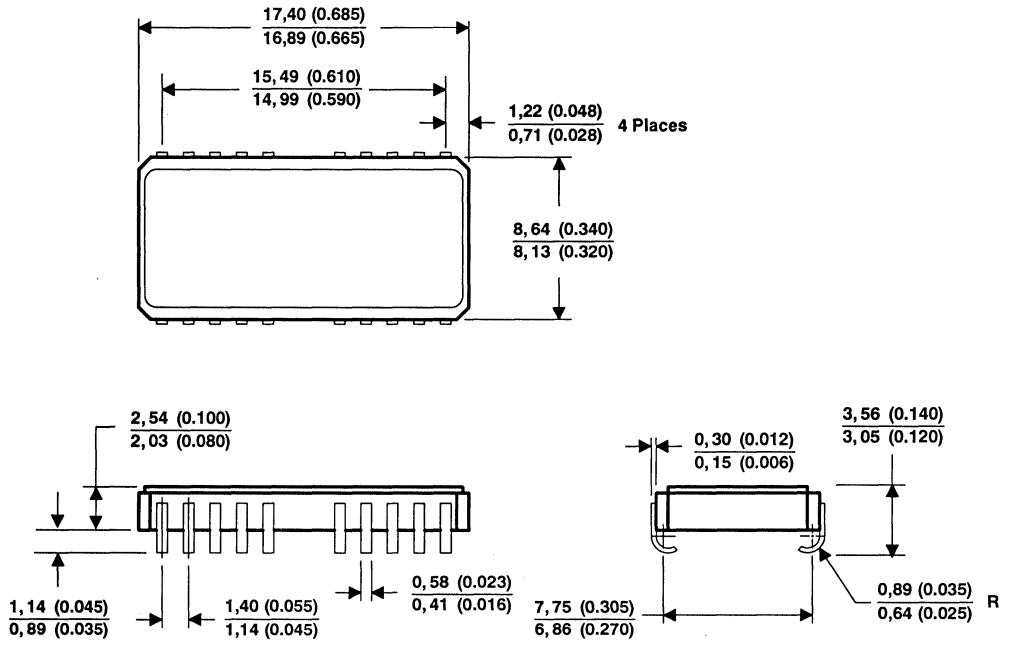
20-Lead Small-Outline Leadless Ceramic Chip Carrier (FQ and HL Suffixes)



PACKAGE SUFFIX	DIMENSION A
FQ	2,29 (0.090) / 1,52 (0.060)
HL	2,03 (0.080) / 1,52 (0.060)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-Lead Leaded Ceramic Chip Carrier (HJ Suffix)



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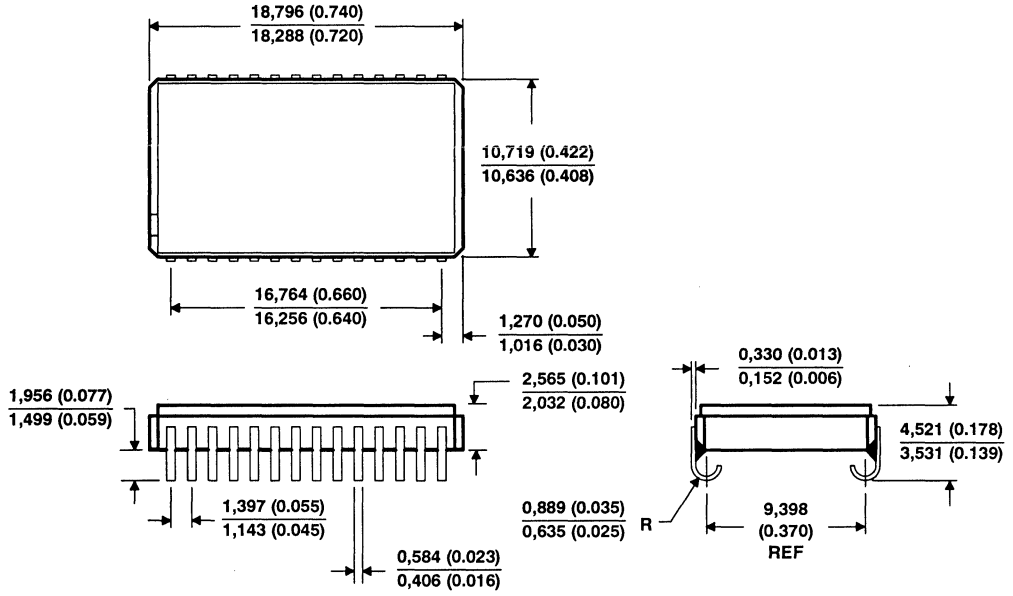
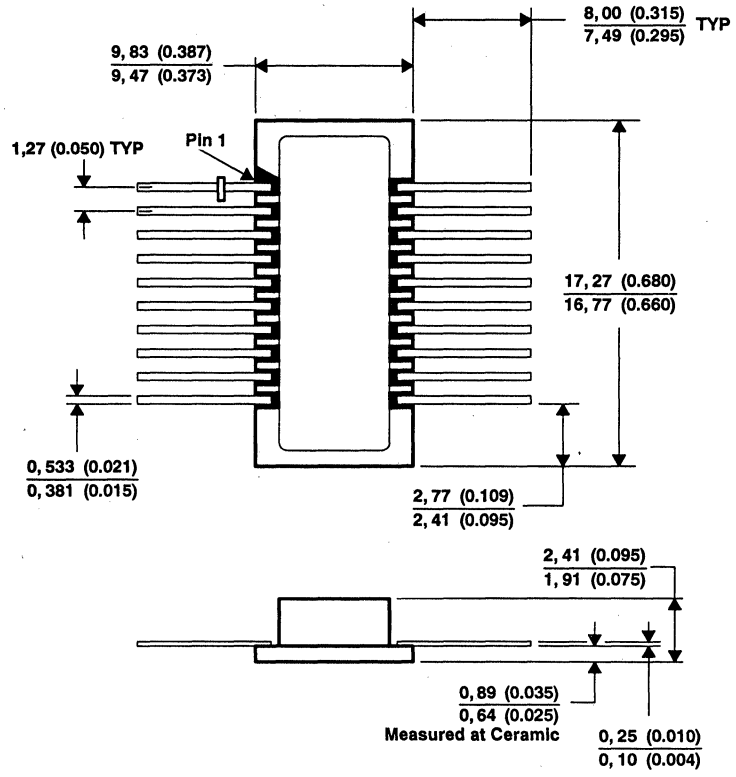
28-Lead Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)



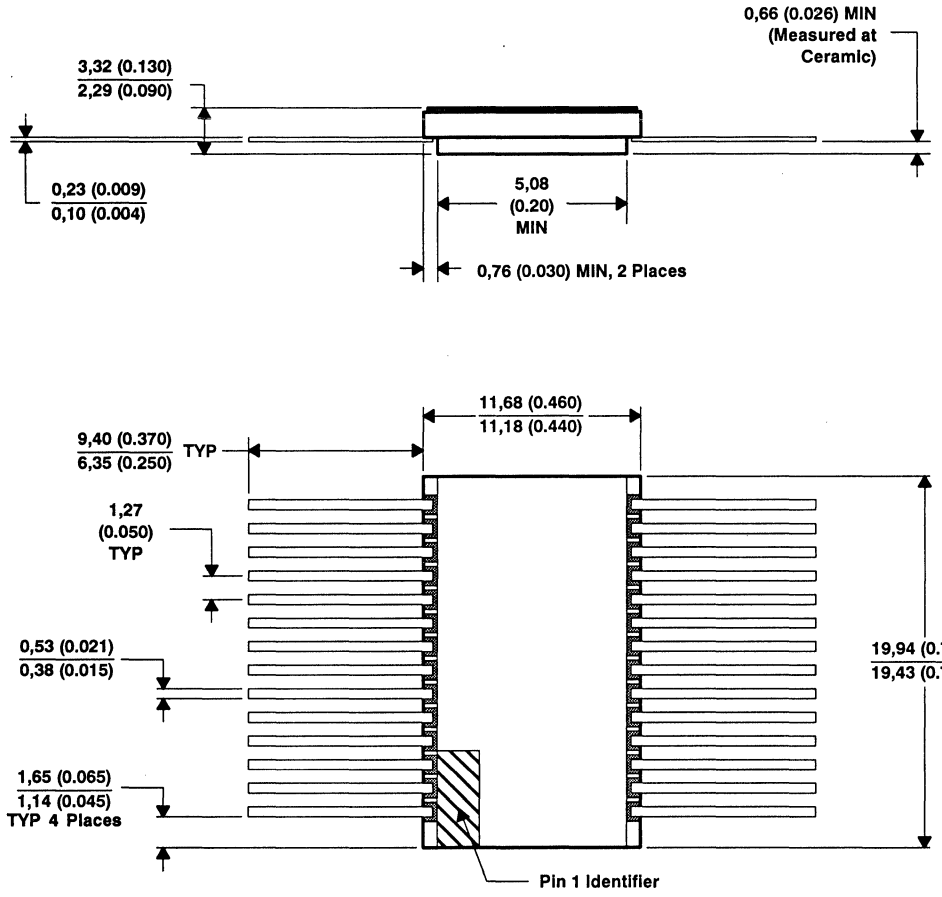
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-Lead Flatpack (HK Suffix)



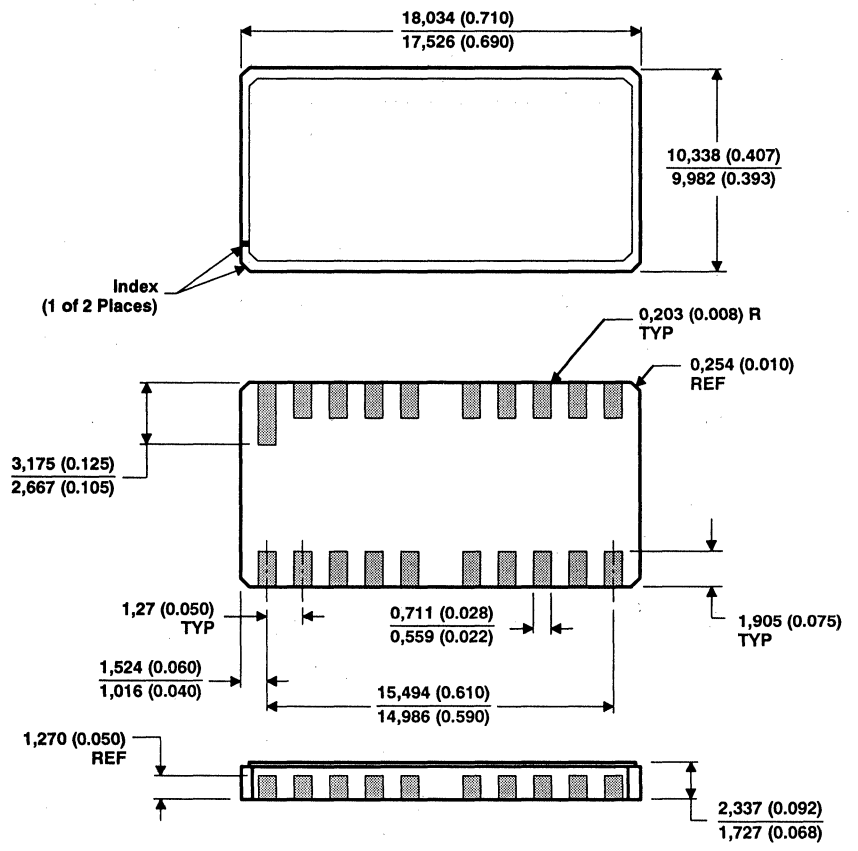
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

28-Lead Flatpack (HKB Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-Lead Small-Outline Leadless Ceramic Chip Carrier (HM Suffix)



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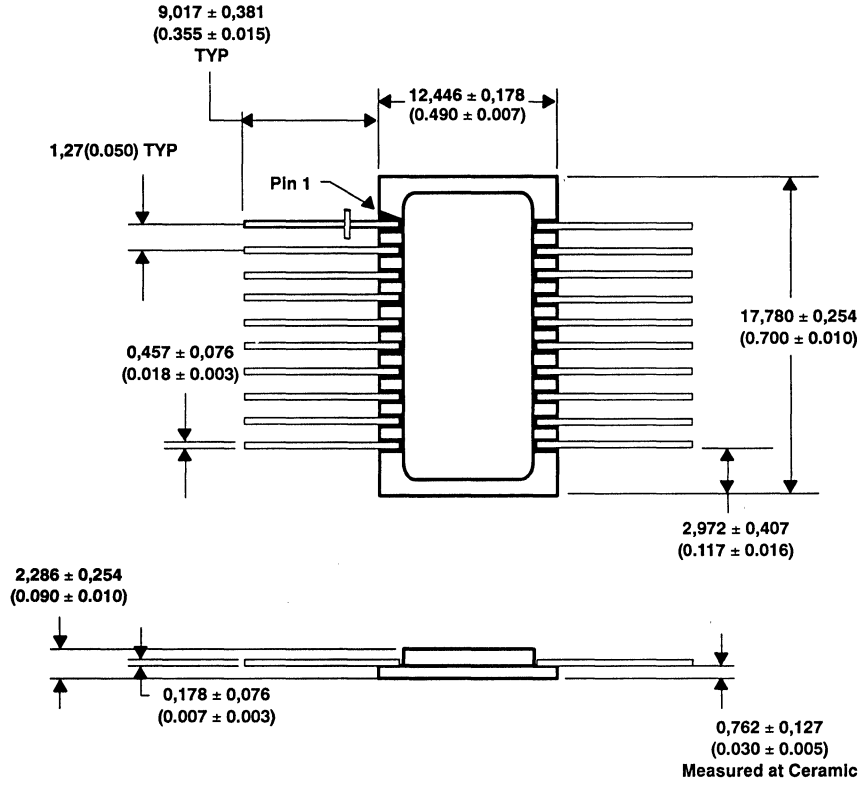
20-Lead Ceramic Flatpack (HR Suffix)



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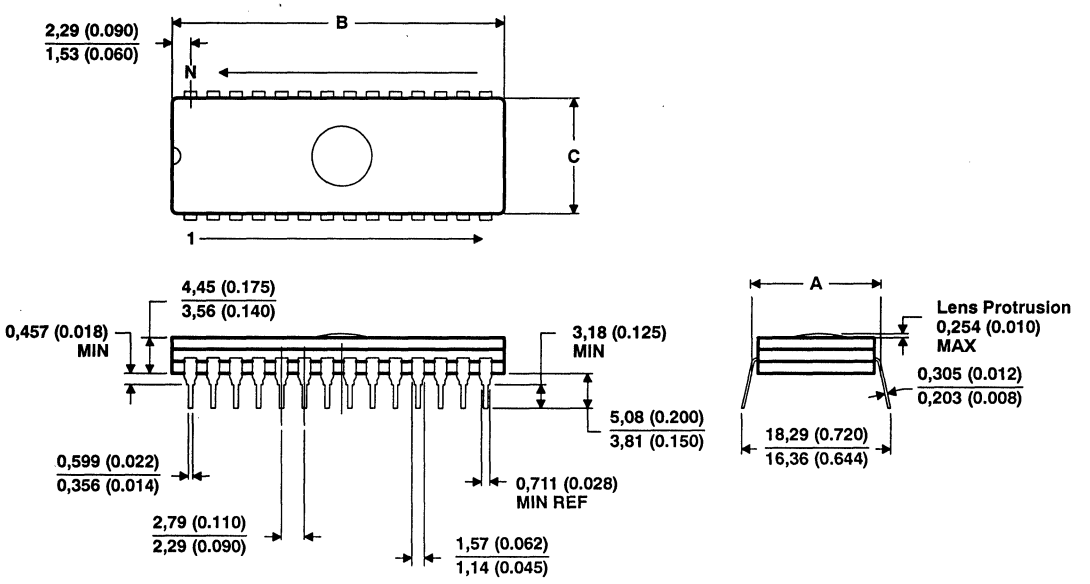
28-Lead Ceramic Dual-In-Line Package (J Suffix)



DIM \ PIN		24	28	32	40
A	(MAX)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)	15,85 (0.624)
B	(MAX)	32,13 (1.265)	37,21 (1.465)	42,37 (1.668)	52,53 (2.068)
C	(MAX)	14,25 (0.561)	14,25 (0.561)	14,25 (0.561)	14,25 (0.561)

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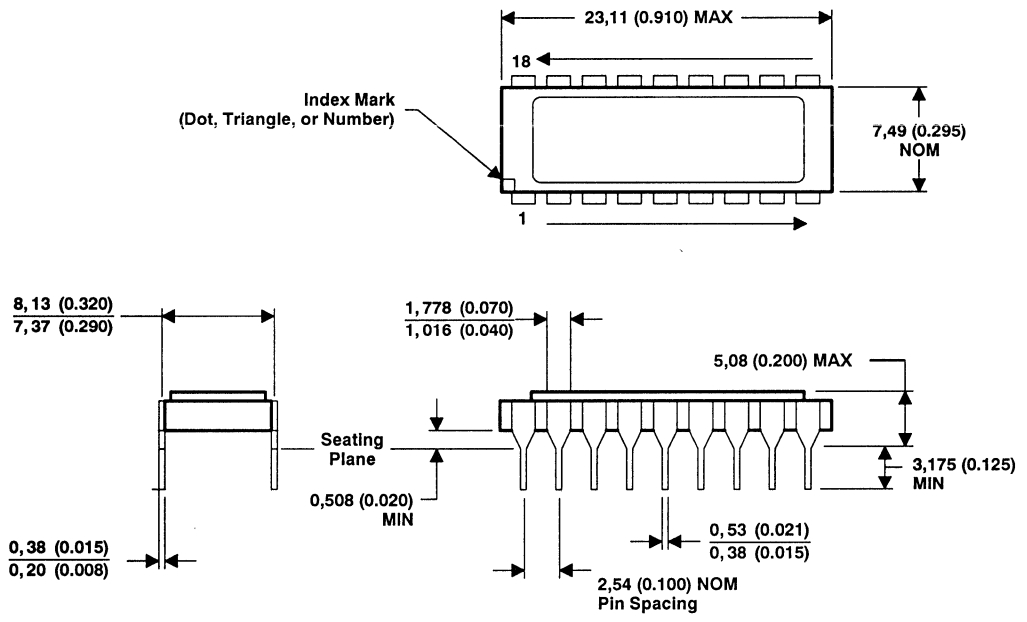
18-Lead Ceramic Sidebrazed Dual-In-Line Package (JD Suffix)



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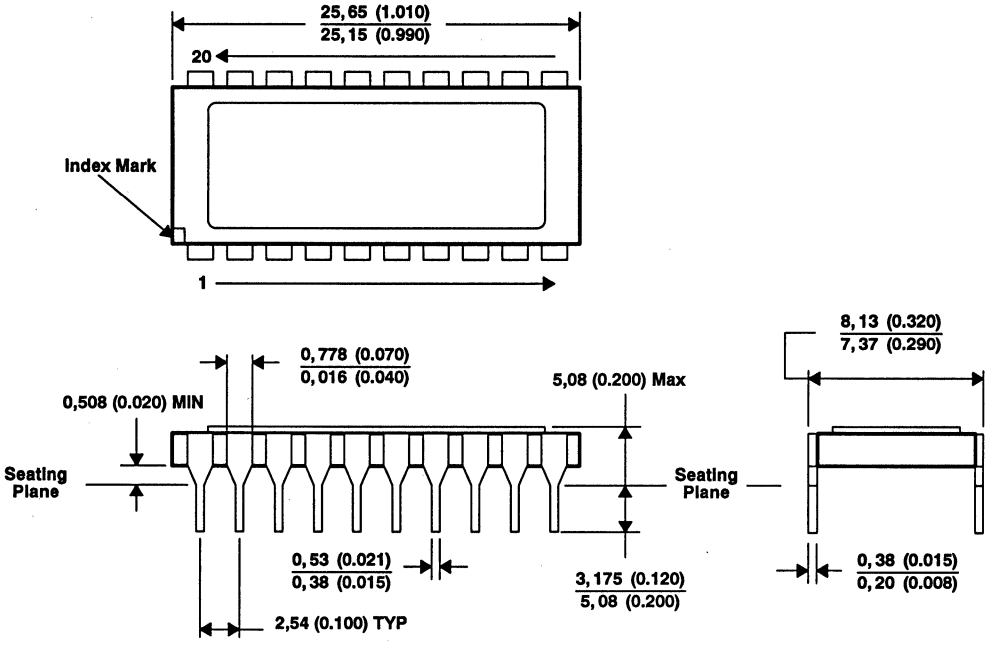
20-Lead Ceramic Sidebrazed 300-Mil Dual-In-Line Package (JDB Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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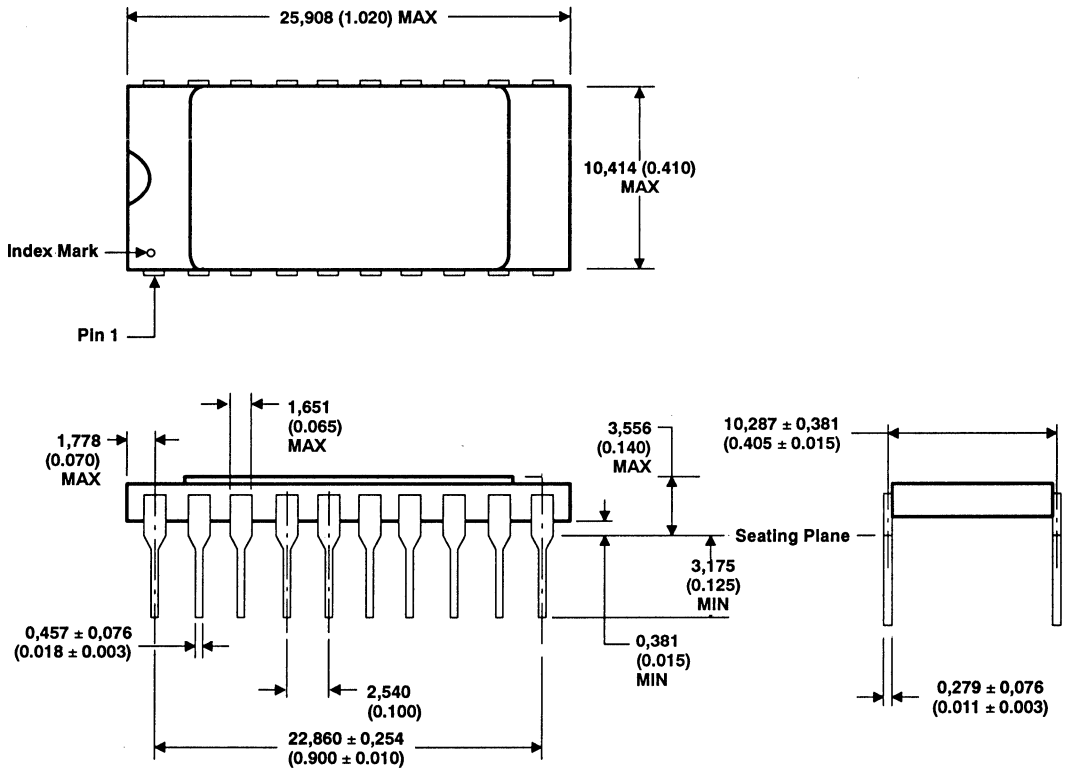
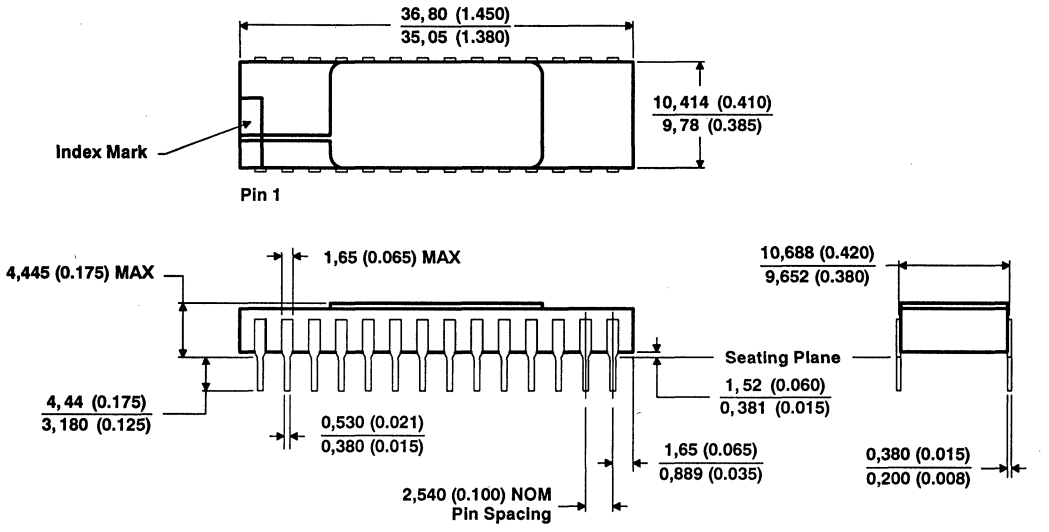
20-Lead Ceramic Sidebrazed 400-Mil Dual-In-Line Package (JD Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

28-Lead Ceramic Sidebrazed Dual-In-Line Package (JD Suffix)



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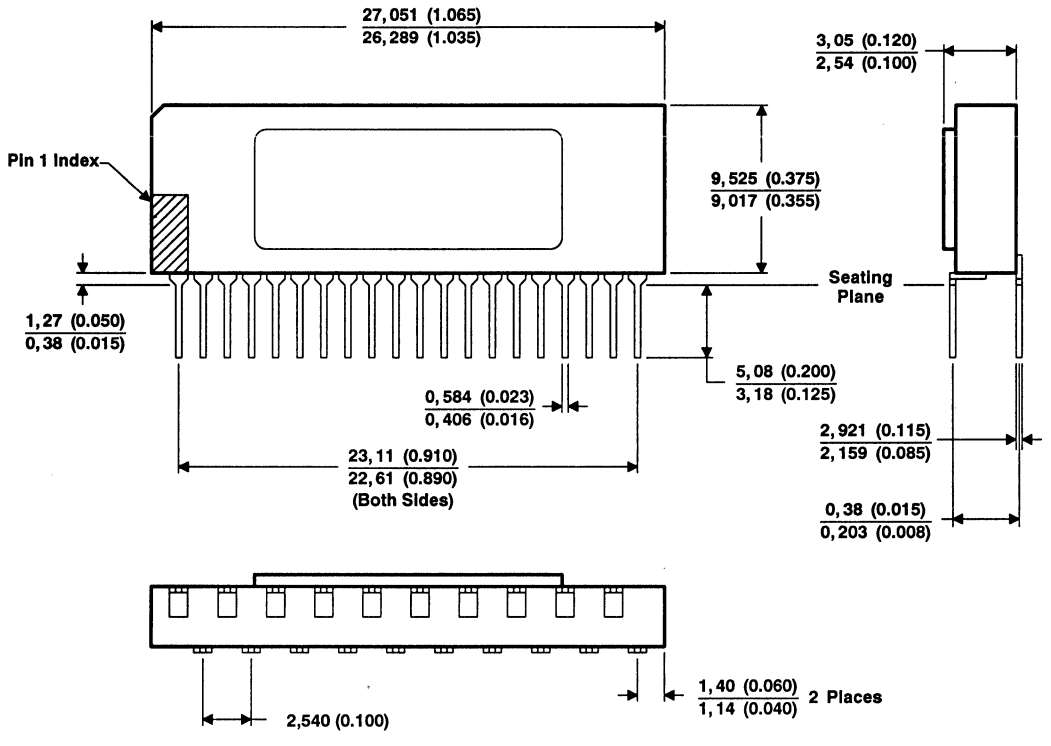
20-Lead Zig-Zag In-line Ceramic Package (ZIP) (SV Suffix)



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