TEXAS INSTRUMENTS

High-Performance FIFO Memories

Standard and Specialty Memories From 1-Bit to 36-Bit Widths

Data Book

September 1994

Advanced System Logic

High-Performance FIFO Memories Data Book

Standard and Specialty Memories From 1-Bit to 36-Bit Widths

PRINTED WITH SOY INK

TEXAS INSTRUMENTS

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INTRODUCTION

First-in, first-out (FIFO) memories from Texas Instruments are valuable data-path elements for eliminating bottlenecks and regulating flow. Data transfers in and out of a FIFO memory are independent of one another and allow the device to be the communication medium between two asynchronous systems. Empty and full status flags that prevent underflow and overflow conditions are standard with all devices, and many have programmable almost-full and almost-empty flags to optimize the control of a particular system.

Each advanced FIFO is constructed with a dual-port SRAM, read and write address incrementing logic, and flag circuitry. Rising-edge-triggered clocks are featured on all TI FIFOs, with self-timed reads and writes on memory that allow a large variance of usable pulse widths. The *strobed* style of FIFO produced by TI writes data to memory on each low-to-high transition of the load-clock (LDCK) input and reads data on each rising edge of the unload-clock (UNCK) input.

TI's *clocked* style FIFO can also receive asynchronous clocks for writing and reading data, but the clock inputs are designed to be continuous, with the rising edge affecting data transfers when separate enable signals are asserted. This characteristic allows a seamless interface between the device and other high-speed buses or microprocessors with similar control. The availability of the free-running clock also provides the means to synchronize the full and empty status flags for use as reliable control signals and reduce the amount of external support logic. Each TI clocked FIFO has the empty flag synchronized to the read clock and the full flag synchronized to the write clock with at least two flip-flop stages. Clocked FIFOs produced in advanced CMOS technology can support clock frequencies up to 67 MHz. The SN74ABT7819, produced in advanced BiCMOS technology, is capable of speeds up to 80 MHz. The SN74ABT7819 is also a bidirectional FIFO, with two independent FIFO memories combined on one chip to buffer data in opposite directions.

Memory organization of the FIFOs ranges in depth from 16 words to 2048 words and data bit widths of 1, 4, 5, 8, 9, 18, 32, and 36. To accommodate the need of reducing the package area as data widths increase, many TI FIFO memories are offered in thin surface-mount packages. The SSOP and TQFP packages, with 25-mil, 0.5-mm, and 0.4-mm lead pitch, respectively, can reduce the FIFO-dedicated board area by greater than 70% over PLCC packages.

Texas Instruments continues to offer leading-edge solutions to customers' needs in both packaging technology and device architecture. This is evidenced by the 120-pin TQFP with 16-mm × 16-mm area used to house the 32- and 36-bit products. With features such as synchronous retransmit, mailbox bypass registers, byte swapping, and bus-width matching, these devices provide a high level of integration in a compact area for applications such as interfacing a digital signal processor (DSP) to a host processor and matching systems with different memory organizations.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i	**Input capacitance** The internal capacitance at an input of the device
C_o	**Output capacitance** The internal capacitance at an output of the device
C_{pd}	**Power dissipation capacitance** Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.
f_{max}	**Maximum clock frequency** The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
I_{CC}	**Supply current** The current into* the V_{CC} supply terminal of an integrated circuit
ΔI_{CC}	**Supply current change** The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}
I_{CEX}	**Output high leakage current** The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5$ V.
$I_{I(hold)}$	**Input hold current** Input current that holds the input at the previous state when the driving device goes to a high-impedance state
I_{IH}	**High-level input current** The current into* an input when a high-level voltage is applied to that input
I_{IL}	**Low-level input current** The current into* an input when a low-level voltage is applied to that input
I_{off}	**Input/output power-off leakage current** The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC} = 0$ V
I_{OH}	**High-level output current** The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
I_{OL}	**Low-level output current** The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

I_{OZ}	**Off-state (high-impedance-state) output current (of a 3-state output)** The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output
t_a	**Access time** The time interval between the application of a specified input pulse and the availability of valid signals at an output
t_c	**Clock cycle time** Clock cycle time is $1/f_{max}$.
t_{dis}	**Disable time (of a 3-state or open-collector output)** The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.
t_{en}	**Enable time (of a 3-state or open-collector output)** The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low) NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.
t_h	**Hold time** The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.
t_{pd}	**Propagation delay time** The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})
t_{PHL}	**Propagation delay time, high-to-low level output** The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level
t_{PHZ}	**Disable time (of a 3-state output) from high level** The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state
t_{PLH}	**Propagation delay time, low-to-high level output** The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

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*Current out of a terminal is given as a negative value.

t_{PLZ}	**Disable time (of a 3-state output) from low level** The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state
t_{PZH}	**Enable time (of a 3-state output) to high level** The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level
t_{PZL}	**Enable time (of a 3-state output) to low level** The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level
t_{su}	**Setup time** The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
t_w	**Pulse duration (width)** The time interval between specified reference points on the leading and trailing edges of the pulse waveform
V_{IH}	**High-level input voltage** An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.
V_{IL}	**Low-level input voltage** An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.
V_{OH}	**High-level output voltage** The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output
V_{OL}	**Low-level output voltage** The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output
V_{IT+}	**Positive-going input threshold level** The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}
V_{IT-}	**Negative-going input threshold level** The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}

definitions

asynchronous FIFO

A first-in, first-out memory that allows asynchronous data reads and writes. The asynchronous FIFO differs from clocked or synchronous FIFOs in the control used to read or write data. Data writes are not edge triggered but initiated by a low level on the write-enable input when the empty flag is high. Likewise, data reads are not edge triggered but initiated by a low-level on the read enables. Flag outputs reflect the instantaneous comparison of the read and write pointers.

clocked FIFO

A first-in, first-out memory that allows data to be written to its array and read from its array at independent rates. The low-to-high transition of a continuous (free-running) write clock stores data in memory when write-enable input signals are asserted. The low-to-high and high-to-low transitions of the input-ready flag (or full flag) output are synchronous to the rising edge of the write clock. The low-to-high transition of a continuous (free-running) read clock reads data from memory when read-enable input signals are asserted. The low-to-high and high-to-low transitions of the output-ready flag (or empty flag) output are synchronous to the rising edge of the read clock.

strobed FIFO

A first-in, first-out memory that allows data to be written to its array and read from its array at independent rates. Data is written on a low-to-high transition on the load-clock (LDCK) input and is read on a low-to-high transition of the unload-clock (UNCK) input. Flag outputs are not synchronized to a particular clock and reflect the comparison of the read and write pointers.

synchronous FIFO

The term *synchronous* refers to a port-control method and does not imply that data writes and reads must be synchronous to one another. Control is the same as for a clocked FIFO wherein data is written by a low-to-high transition of a write clock when write-enable inputs are asserted and data is read by a low-to high transition of a read clock when read enables are asserted. Data writes and reads can be synchronous or asynchronous to one another. The empty flag is synchronized to the read clock, and the full flag is synchronized to the write clock.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⟶ = value/level or resulting value/level is routed to indicated destination
↶ = value/level is re-entered
X = irrelevant (any input, including transitions)
Z = off (high-impedance) state of a 3-state output
a . . . h = the level of steady-state inputs A through H respectively
Q_0 = level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$ = complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n = level of Q before the most recent active transition indicated by ↓ or ↑
⎍ = one high-level pulse
⊔ = one low-level pulse
Toggle = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⊔, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

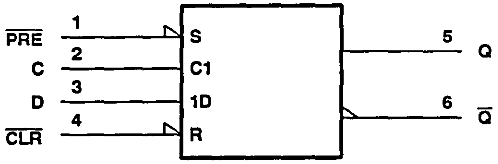
The function table functional tests do not reflect all possible combinations or sequential modes.

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

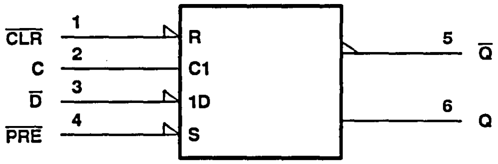
It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

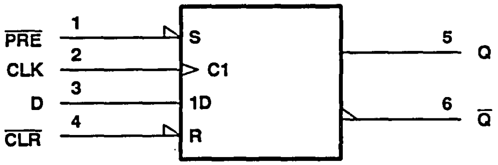
In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



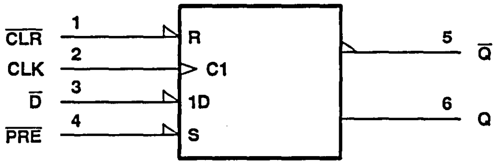
LATCH



LATCH



FLIP-FLOP



FLIP-FLOP

The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

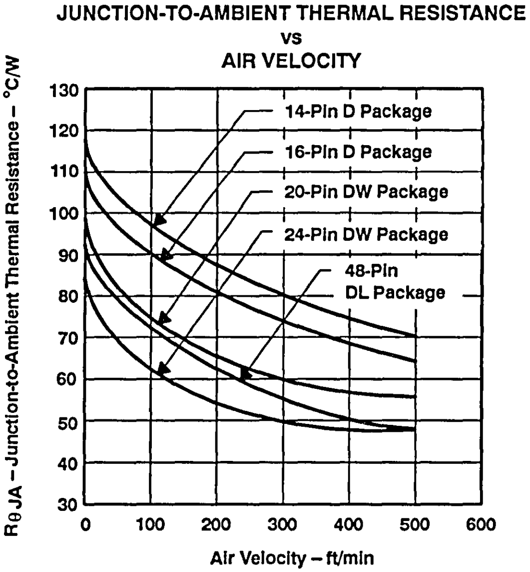


Figure 1

Derating curves for 210-mil shrink small-outline package are shown in Figures 2 through 5.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

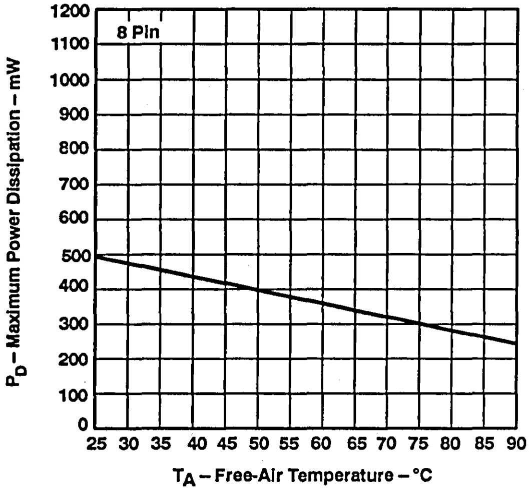


Figure 2

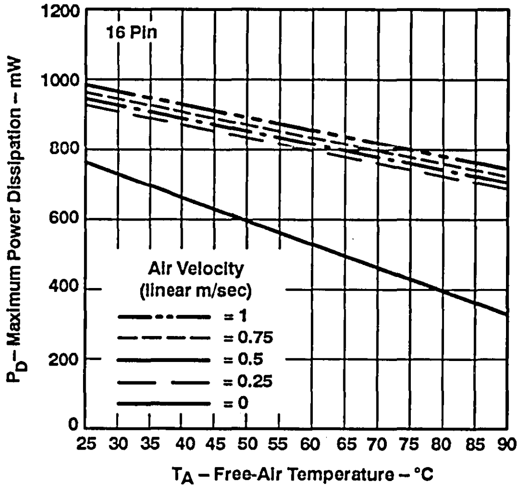


Figure 3

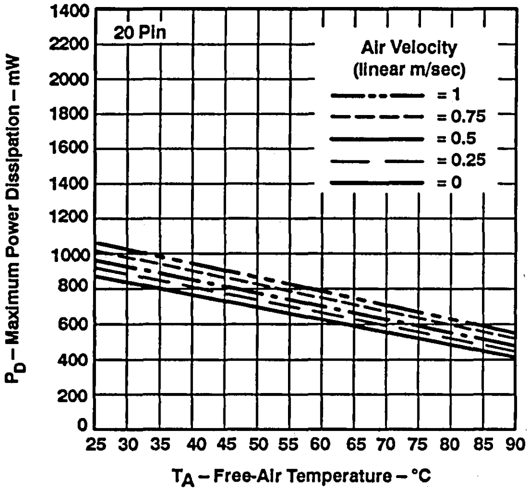


Figure 4

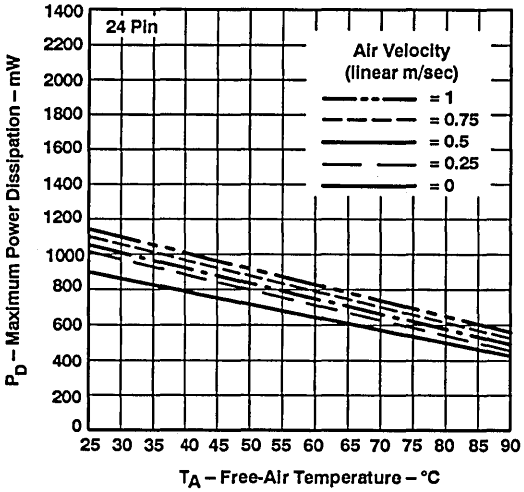


Figure 5

MULTI-Q™ 18-BIT FIFO

Features	Benefits
• Three programmable FIFOs on one device. Depths range from 256 to 4K words.	• Permits user to define each FIFO queue depth for quality of service (QOS)
• Synchronous multiplexer for queue output selections	• Allows user to easily select desired output
• Cell-ready flag for each queue synchronized to read clock	• Indicates minimum of one complete cell available for reads
• Three programmable-cell flags	• Allows user to choose each cell-status indicator
• Programmable-cell size for each queue	• Allows user to define from 10 to 32 18-bit words for cell
• Clocked interface	• Read and write enables synchronized to continuous clock signal
• Separate programming/diagnostic bus	• Allows separate bus for programming required parameters as well as allowing a direct path into each cell for diagnostics
• Input and output start of cell indicator	• Ensures cell alignment for writes and reads
• 0.8-µm CMOS process	• Fast access times combined with low power
• EIAJ standard 100-pin thin quad flat package (TQFP)	• Fine-pitch package option for reduced board space

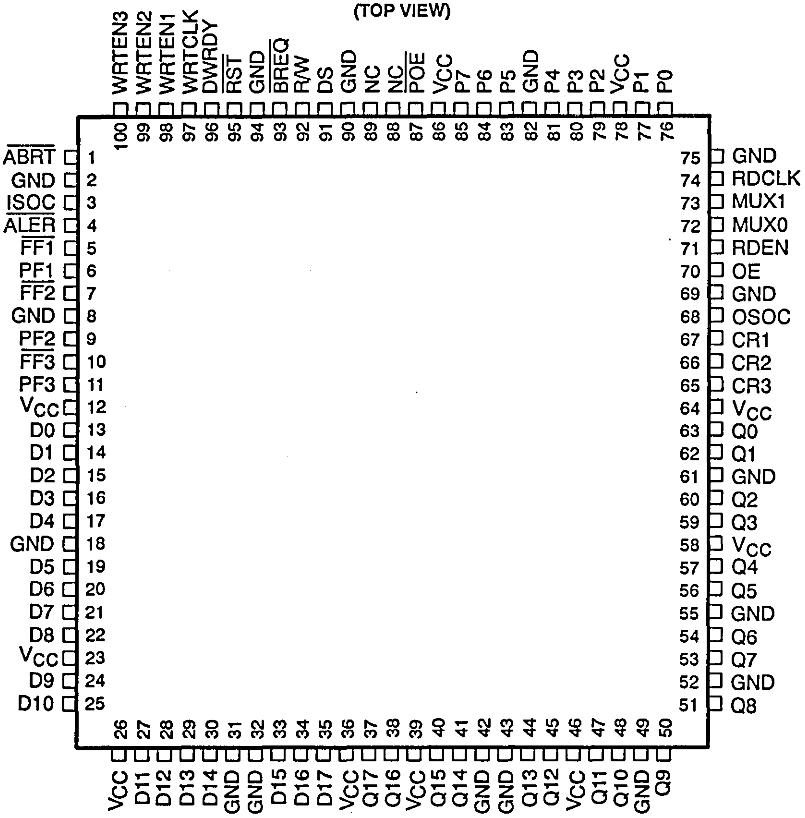
SN74ACT53861
4096 × MULTIPLE-QUEUE (MULTI-Q™) FIRST-IN, FIRST-OUT MEMORY WITH THREE PROGRAMMABLE-DEPTH BUFFERS AND CELL-BASED FLAGS

SCAS443 – JUNE 1994

- **4K × 18 Total Memory Size**
- **Three Programmable-Depth FIFOs on One Device**
- **Memory Allocation of 256 × 18 Blocks**
- **Two Separate Read and Write Clocks That Can Operate Synchronously or Asynchronously**
- **Clocked Interface; Read and Write Enables Synchronize Data Transfers to Continuous Clocks**
- **Programmable Cell Size From 10 to 32 18-Bit Words**
- **Cell-Abort Feature to Discard a Previous Cell Write**
- **Cell-Ready Flag for Each Queue Synchronized to Read Clock**
- **Programmable Flag With Hysteresis for Each Queue Synchronized to Write Clock**
- **Last Word of Cell Flag Synchronized to Read Clock**
- **Input or Output Bus Size of 9 Bits or 18 Bits, Byte Stuff/Destuff Capability**
- **Data Access Times of 11 ns**
- **Synchronous Multiplexer for Queue Output Selection**
- **8-bit Bidirectional Programming Port**
- **Clock Frequencies up to 50 MHz**
- **Produced in 0.8-μm Advanced CMOS Technology**
- **Available in 100-Pin Thin Quad Flat Package (PZ)**

description

PZ PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

MULTI-Q is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

description

The Multi-Q FIFO is a first-in first-out (FIFO) memory with three programmable-length queues and a total memory size of 4096 words of 18 bits each to provide two or three quality of service (QOS) bins for ATM traffic in a single device. The core memory is divided into sixteen 256 x 18 blocks that can be allocated to each queue according to the user's need.

Flags for the queues are designed to indicate the presence or absence of entire cells rather than individual words. The number of 18-bit words that constitutes one cell is programmable by the user and has a default value of 27. A cell ready (CR) flag for a queue is high when at least one complete cell is present in the queue. Each CR flag is synchronized to the read clock (RDCLK). The full flag ($\overline{FF}$) for each queue is synchronized to the write clock (WRTCLK) and indicates when no more cells can be written to the queue. A programmable flag (PF) is provided for each queue, which is synchronized to the WRTCLK. Each PF has two programmable values. PF is low when the number of cells in the queue are greater than or equal to the first limit, and it is set high when the number of cells in the queue are reduced to the second limit. This allows the user to define a hysteresis threshold for the flag if it is needed. No flag is provided to indicate when a queue is completely filled to prevent overflow of a queue.

WRTCLK and RDCLK are designed to be free-running clock inputs to maintain the proper synchronization of the flags. The clocks are synchronized or asynchronous in phase, frequency, or both. Writes to one of the three queues is done by a rising edge of WRTCLK when the queue's write enable (WRTEN) is high. Any write can be done to two or three of the queues simply by asserting two or three of the WRTEN inputs for a WRTCLK rising edge. Data is read from a queue by the rising edge of RDCLK when the queue is selected by the multiplexer (MUX0, MUX1) inputs and the read enable (RDEN) is high. Configuration registers can be programmed to set the input or output port sizes to 9-bits or 18-bits. Big- or little-endian data format can be selected for the buses. When matching 9-bit buses to 18-bit or 36-bit buses with the Multi-Q, byte stuffing can be selected for the data input and byte destuffing can be done on the data output.

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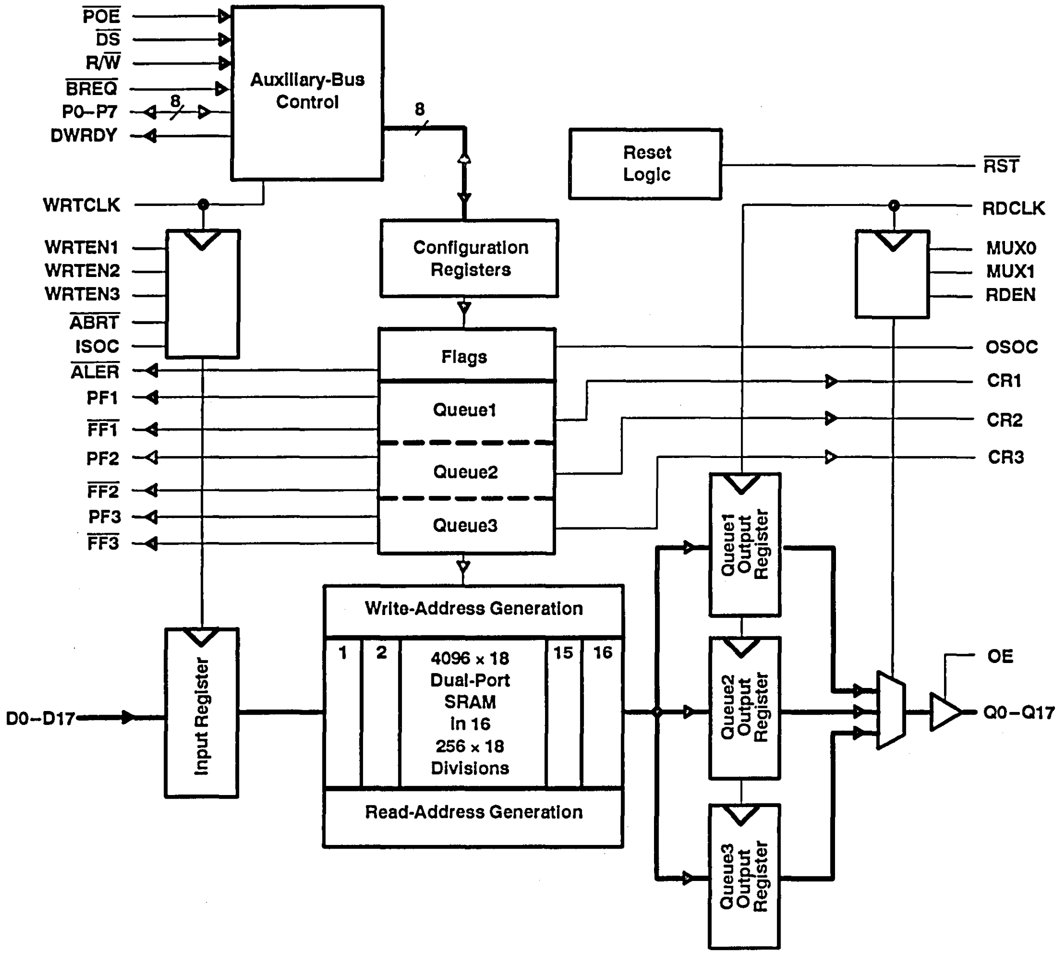
functional block diagram



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Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
$\overline{\text{ALER}}$	O	Align error. $\overline{\text{ALER}}$ maintains cell synchronization at the input. If ISOC and internal start-of-cell status disagree, $\overline{\text{ALER}}$ is low and writes are disabled.
$\overline{\text{BREQ}}$	I	Bus request. When $\overline{\text{BREQ}}$ is low, DWRDY is set high and writes are performed to the configuration registers. When $\overline{\text{BREQ}}$ is high, DWRDY is set high and writes are performed to the 18-bit input port.
$\overline{\text{CR}}$	O	Cell ready flag. $\overline{\text{CR}}$ for each queue is high when at least one complete cell is present in the queue. $\overline{\text{CR}}$ is set low upon the read of the last word or byte in a cell, if no other complete cells are stored in the FIFO.
D0–D17	I	18-bit data input port
$\overline{\text{DS}}$	I	Data strobe. A high-to-low transition of $\overline{\text{DS}}$ latches the data on the 8-bit programming bus to the configuration registers. A low-to-high transition of $\overline{\text{DS}}$ sends the data from configuration registers to the programming bus.
DWRDY	O	Data write ready. DWRDY gives control of data writing to the input bus or the 8-bit programming bus. Data writes to the programming bus are allowed when DWRDY is low and data writes to the synchronous bus are allowed when DWRDY is high.
$\overline{\text{FF}}$	O	Full flag. Full flag for each queue is synchronized to the WRTCLK. When $\overline{\text{FF}}$ is low, no more cells can be written to the FIFO. $\overline{\text{FF}}$ is set high by the second low-to-high transition of WRTCLK after the last byte or word read of a cell in the queue.
ISOC	I	Input start of cell. ISOC must be high for the first word or byte write of a cell and low for all other word or byte writes.
MUX1, MUX0	I	Multiplexer inputs. MUX1 and MUX0 select one of the three queues output registers.
OE	I	Output enable. The data outputs (Q0–Q17) are in the high-impedance state when OE is low.
OSOC	O	Output start of cell. OSOC is high when the first word or byte of cell is present in the output register of the queue. When any other word or byte of a cell or invalid data is present in the output register of Q, OSOC is low.
P0–P7	I/O	8-bit bidirectional programming bus
PF	O	Programmable flag. PF is low when the number of cells in the queue are greater than or equal to write threshold stored in the queue's PFX_W register. PF is set high when the number of cells in the queue are reduced to the read threshold stored in the queue's PFX_R register.
$\overline{\text{POE}}$	I	Program output enable. The programming bus (P0–P7) outputs are active when $\overline{\text{POE}}$ is low and R/$\overline{\text{W}}$ is high.
Q0–Q17	O	18-bit data output port
$\overline{\text{RST}}$	I	FIFO reset. To reset FIFO, four low-to-high transitions of WRTCLK and four low-to-high transition of CLRB must occur while $\overline{\text{RST}}$ is low.
RDCLK	I	Read clock. RDCLK is a continuous clock and is asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from a queue when the queue is selected by the multiplexer (MUX0, MUX1) and RDEN is high.
R/$\overline{\text{W}}$	I	Read/write select. R/$\overline{\text{W}}$ high selects a read operation and low selects a write operation on the 8-bit programming bus.
RDEN	I	Read enable. RDEN high enables a low-to-high transition of the read clock to read data from the queue selected by MUX1 and MUX0.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to one of the 3 queues when WRTEN and $\overline{\text{FF}}$ are high.
WRTEN	I	Write enable. A queue's WRTEN must be high to enable a low-to-high transition of WRTCLK to write data to the queue.

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detailed description

reset

The Multi-Q FIFO is reset by setting the reset ($\overline{RST}$) input low for four WRTCLK and four RDCLK low-to-high transitions. When the device is reset, the cell ready (CR1, CR2, and CR3) flags for each queue are set low, the programmable flags (PF1, PF2, and PF3) are set high, the full flags ($\overline{FF1}$, $\overline{FF2}$, and $\overline{FF3}$) are set high, the align error ($\overline{ALER}$) is set high, and the output start of cell (OSOC) is set low. During a device reset, the default values shown in Table 1 are loaded into the configuration registers.

Table 1. Configuration Registers

REGISTER SYMBOL	REGISTER NAME	NO. OF BITS	DEFAULT VALUE	PROGRAMMABLE RANGE	FUNCTION
PORT	Port Control	5	0	Bit-slice control	Chooses the data input and output bus size and format. Controls output byte destuffing.
QL1	Queue1 Length	5	8	0–16	Defines number of 256 × 18 memory blocks allocated to Queue1
QL2	Queue2 Length	4	6	0–15	Defines number of 256 × 18 memory blocks allocated to Queue2
QL3	Queue3 Length	4	2	0–15	Defines number of 256 × 18 memory blocks allocated to Queue3
CLSZ	Cell Size	6	27	10–32	Defines the number of 18-bit words in one cell
PF1_W	Programmable Flag 1, Write Threshold	9	71	1–409	Defines the number of cells stored in Queue1 to set PF1 low
PF1_R	Programmable Flag 1, Read Threshold	9	70	0–408	Defines the number of cells stored in Queue1 to reset PF1 high
PF2_W	Programmable Flag 2, Write Threshold	9	51	1–383	Defines the number of cells stored in Queue2 to set PF2 low
PF2_R	Programmable Flag 2, Read Threshold	9	50	0–382	Defines the number of cells stored in Queue2 to reset PF2 high
PF3_W	Programmable Flag 3, Write Threshold	8	13	1–383	Defines the number of cells stored in Queue3 to set PF3 low
PF3_R	Programmable Flag 3, Read Threshold	8	12	0–382	Defines the number of cells stored in Queue3 to reset PF3 high

Default Values for the Configuration Registers

Port Control:

A 4-bit register that controls the sizing and word-align functions of the input and output data ports. Figure 1 shows the bit configuration of the port control register. Table 2 lists the register bits, names, and functions.

4	3	2	1	0
OUTSTF	OUTSIZ	INSTF	INBE	INSIZ

Figure 1. Port Control Register

Default Values for the Configuration Registers (continued)

Table 2. Port Control Register Bits

BIT	NAME	VALUE	FUNCTION
0	INSIZ	0 (default value) 1	Enables an 18-bit input data bus Enables a 9-bit input data bus
1	INBE	0 (default value) 1	Enables the placement of D0–D8 data in memory with a little-endian format if INSIZ bit is a 1. Enables the placement of D0–D8 data in memory with a big-endian format (INSIZ bit is a 1).
2	INSTF	0 (default) 1	Sets the end of a cell write to be the last byte write of the last word as defined by the cell size (CLSZ) register if INSIZ bit is a 1. Sets the end of a cell write to be the first byte write of the last word and the byte write is copied to both bytes of the word (INSIZ bit is a 1).
3	OUTSTF	0 (default) 1	Enables 18-bit data output Enables 9-bit data output
4	OUTSTF	0 (default) 1	Allows byte reads to precede normally on all words of a cell, (OUTSIZ bit is a 1). After the first byte of the last word of a cell is read, the last byte of the last word of that cell is ignored and the first byte of the first word of the subsequent cell is read (OUTSIZ bit is a 1).

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Queue Length:

The three queue length registers (QL1, QL2, and QL3) have default values of 8, 6, and 2, respectively. This defines the 18-bit wide Queue1 memory depth as 2048 (8 x 256); Queue2 memory depth as 1536 (6 x 256); and Queue3 memory depth as 512 (2 x 256). The QL1 register has 5 bits and can be programmed to utilize the entire memory of the device for Queue1.

Cell Size:

The cell size register (CLSZ) has a default value of 27. This defines 27 18-bit words as one cell for the cell ready flags and programmable flags.

Programmable Flag Write Threshold:

The default values for the PF1_W, PF2_W, and PF3_W registers are chosen to set the respective programmable flags low when the number of 27-word cells stored in its queue is five cells from filling its buffer.

Programmable Flag Read Threshold:

The default values for the PF1_R, PF2_R, and PF3_R registers are chosen to reset the respective programmable flags high when the number of 27-word cells stored in its queue is reduced by one.

data writes

Data writes are synchronized to the write clock (WRTCLK) and can occur asynchronous to the read clock (RDCLK) while any of the three queues are being read. The data write ready (DWRDY) output must be high to allow a data write from the data inputs (D0–D17) into one or more of the queue memories. When DWRDY is high, the low-to-high transition of WRTCLK stores data (D0–D17) in Queue1 when the WRTEN1 input is high and the $\overline{\text{FF1}}$ output is high, Queue2 when the WRTEN2 input is high and the $\overline{\text{FF2}}$ output is high, and Queue3 when the WRTEN3 input is high and the $\overline{\text{FF3}}$ output is high. Data can be stored in two or three queues simultaneously by asserting two or three WRTEN signals.

The input start of cell (ISOC) input and the align error ($\overline{\text{ALER}}$) output are used to maintain cell synchronization at the input of the device. The ISOC should be high for the first word or byte write of a cell and should be low for all other word or byte writes of the cell. The SN74ACT53861 maintains its own start-of-cell status and compares this to the ISOC on each word or byte write. If a word or byte write is attempted when the ISOC and the internal start-of-cell status disagree, the write is prevented and the $\overline{\text{ALER}}$ output is set low.

data writes (continued)

When all words of a cell are successfully written to one of the queues, the queue's flags are updated. In addition to updating the queue's flags, a completed cell write moves the cell-abort marker to the next memory write location in the queue. After a reset, the cell-abort marker for each queue is positioned at the first memory write location.

If a 9-bit data input is selected by the port control register, data is input to the FIFO through bits D0–D8. If the INBE bit of the PORT register is set to 1, data is stacked into memory big-endian style with the first byte write of a word stored in the D9–D17 byte and the second byte write of a word stored in the D0–D8 byte. If INBE is set to 0, little-endian stacking is enabled with the first byte write of a word stored in the D0–D8 byte and the second byte write of a word stored in the D9–D17 byte.

All data writes since a queue's last cell-abort marker are discarded when the abort ($\overline{\text{ABRT}}$) input is held low and the queue's write enable (WRTEN1, WRTEN2, or WRTEN3) is held high for a low-to-high transition of WRTCLK. The internal write pointer for the queue memory is set to the cell-abort marker for the queue, thereby discarding all data written since the last cell completion. No data write is performed during the abort cycle.

data reads

Data reads are synchronized to the read clock (RDCLK) and can occur asynchronous to the write clock (WRTCLK) while any of the three queues are being written. A data read is done on a queue by the low-to-high transition of RDCLK when the queue is selected by the multiplexer (MUX0, MUX1) inputs (see Table 3), the read enable (RDEN) input is high, and the cell ready flag (CR1, CR2, or CR3) output for the queue is high.

Table 3. Output-Queue Selection by Multiplexer Inputs

MUX1	MUX0	QUEUE OUTPUT
0	0	Queue1
0	1	Queue1
1	0	Queue2
1	1	Queue3

The status of the OUTSIZ bit in the PORT register determines if the output data bus size is 18-bit word or 9-bit byte. If OUTSIZ is 0, each read outputs a new queue word on Q0–Q17. If OUTSIZ is 1, the first read outputs a new queue word on Q0–Q17 and the next read swaps the byte order of Q0–Q8 and Q9–Q17. This pattern is repeated for each subsequent word read.

If the OUTSTF bit in the PORT register is a 1 and the OUTSIZ bit is a 1, the first byte read of the last word of a cell completes the cell read and the next byte read outputs a new word on the data bus, thereby discarding the last byte of each cell. No change in data output flow occurs if OUTSTF is a 0.

The cell ready flag and programmable flag for each queue are updated upon the read of the last word of a cell. The number of words in a cell is defined by the contents of the cell size (CLSZ) configuration register. When the output data bus size is byte and the OUTSTF bit is a 0, the last byte read of the last word of a cell updates the flags. If OUTSTF bit is a 1, the first byte read of the last word of a cell updates the flags.

The output start of cell (OSOC) output is high when the first word or byte of a cell is present in the output register of the queue selected by the MUX1 and MUX0 inputs. When any other word or byte of a cell is present in the output register of the queue selected by the MUX1 and MUX0 outputs, or if the contents of the selected register is invalid, the OSOC is low. OSOC is synchronous to the low-to-high transition of RDCLK.

Switching queues for data output is done synchronous to the low-to-high transition of RDCLK. If the RDEN input and cell ready flag are high at the time the queue output switch occurs, a read is done on the new queue. If the RDEN input is low at the time the queue output switch occurs, the previously read data value held in the new queue's output register is output on Q0–Q17. Queue switching should only be performed on cell boundaries.

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data reads (continued)

OE controls the state of the data outputs (Q0–Q17). When OE is high, Q0–Q17 are active. When OE is low, Q0–Q17 are in the high-impedance state.

cell ready flags

Each queue has a cell ready flag (CR1, CR2, or CR3) that is high when at least one complete cell is stored in the queue. The cell ready flags are synchronized to the low-to-high transition of the RDCLK. After reset, the cell ready flags are set low. The low-to-high transition of a queue's cell ready flag is initiated when a cell write to an empty queue is complete. The queue's cell ready flag is set high by the second RDCLK rising edge after this event. The cell ready flag is set low upon the read of the last word or byte in a cell if no other complete cells are loaded in the queue. Reads from a queue are inhibited while its cell ready flag is low.

full flags

Each queue has a full flag ($\overline{\text{FF1}}$, $\overline{\text{FF2}}$, or $\overline{\text{FF3}}$) that is set high when at least one complete cell space is available in the queue. Upon programming the queue length and the cell size, the SN74ACT53861 calculates the maximum number of complete cells which can be written to a queue. When the number of cells stored in a queue is equal to this maximum value, the queue's full flag is set low. full flags are synchronous to the low-to-high transition of the WRTCLK. When a queue's full flag is low, the full flag is set high by the second WRTCLK low-to-high transition after the last byte or word read of a cell in the queue.

programmable flags

Each queue has one programmable flag (PF1, PF2, or PF3) that is synchronized to the low-to-high transition of the WRTCLK. Two registers per queue define the boundaries of the programmable flags; the *write threshold* register (PF1_W, PF2_W, or PF3_W) and the *read threshold* register (PF1_R, PF2_R, or PF3_R). When the word write that stores the number of complete cells equals the queue's PFx_W register, its programmable flag is set low. The low-to-high transition of the programmable flag is initiated by the read of the last word or byte in a cell. This reduces the number of stored cells equal to the queue's PFx_R value. The programmable flag is set high by the second WRTCLK low-to-high transition after this event.

programming the configuration registers

The configuration registers for the Multi-Q FIFO can be programmed after a device reset and before data is written to one of the queues. The programming port (P0–P7) is used to sequentially write or read the configuration registers.

In order to write to the configuration registers, control of the bus must first be acquired by asserting the bus request ($\overline{\text{BREQ}}$) input low, which in turn sets the data write ready (DWRDY) output low after two rising edges of WRTCLK. The DWRDY output gives data writing control to the synchronous input bus (WRTCLK, WRTEN1–3, D0–D17) or the 8-bit programming bus. Data writes to the programming bus are allowed when DWRDY is low and data writes to the synchronous input bus are allowed when DWRDY is high. Data on P0–P7 is written to the configuration registers on the high-to-low transition of data strobe ($\overline{\text{DS}}$) when DWRDY is low and the read/write (R/$\overline{\text{W}}$) input is low. The configuration registers are written in the sequence shown in Table 4. Ten writes are needed to program the configuration registers. After all ten registers are programmed, further data write attempts to the configuration registers are ignored until the device is reset again. When programming is complete, the $\overline{\text{BREQ}}$ input is set high to set DWRDY high and returns input control to the 18-bit synchronous input port. A list of rules for configuration register programming follows.

Rules for queue length (QL1, QL2, QL3) register values:

1. Zero is the minimum value.
2. Sixteen is the maximum value for QL1. Fifteen is the maximum value for QL2 and QL3.
3. Only QL1 and QL2 can be programmed by the user. QL3 is calculated by the device to use the remaining memory (if any exists).

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programming the configuration registers (continued)

Rules for cell size (CS) register values:

1. Ten is the minimum value.
2. Thirty-two is the maximum value.

Rules for programmable flag write threshold (PF1_W, PF2_W, and PF2_W) register values:

1. One is the minimum value.
2. Value must not exceed number of complete cells that can be stored in the buffer defined by its queue length register and the cell size register.
3. The PF1_W, PF2_W, and PF3_W registers are nine bits each. The most significant eight bits are programmable by the user and the least significant bit is always a 1; therefore, PFx_W values are odd.

Rules for programmable flag read threshold (PF1_R, PF2_R, and PF3_R) register values:

1. Zero is the minimum value.
2. Value must be less than the corresponding programmable flag write threshold register value.
3. The PF1_R, PF2_R, and PF3_R registers are nine bits each. The most significant eight bits are programmable by the user and the least significant bit is always 0; therefore, all PFx_R values are even.

Table 4. Accessing Configuration Registers From the Programming Bus for Data Writes

WRITE ORDER	REGISTER	PROGRMAMMING BUS PORTS	
		MSB	LSB
1	PORT	P4	P0
2	QL1	P4	P0
3	QL2	P3	P0
4	CLSZ	P5	P0
5	PF1_W	P7	P0
6	PF1_R	P7	P0
7	PF2_W	P7	P0
8	PF2_R	P7	P0
9	PF3_W	P7	P0
10	PF3_R	P7	P0

The programming bus (P0–P7) is a bidirectional port whose outputs are active when the program output enable ($\overline{\text{POE}}$) input is low and the read/write (R/$\overline{\text{W}}$) input is high. When the P0–P7 outputs are active, data from the configuration registers are output. The next configuration register in sequence shown in Table 5 is sent to the programming bus outputs on a low-to-high transition of $\overline{\text{DS}}$ when R/$\overline{\text{W}}$ is high. After all ten registers have been read in sequence, a subsequent programming bus read accesses the QL1 register again. Unused bit values for a register appear as logical 0 on the programming bus.

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programming the configuration registers (continued)

Table 5. Accessing Configuration Registers From the Programming Bus for Data Reads

WRITE ORDER	REGISTER	PROGRMAMMING BUS PORTS	
		MSB	LSB
1	PORT	P3	P0
2	QL1	P4	P0
3	QL2	P3	P0
4	CLSZ	P5	P0
5	PF1_W	P7	P0
6	PF1_R	P7	P0
7	PF2_W	P7	P0
8	PF2_R	P7	P0
9	PF3_W	P7	P0
10	PF3_R	P7	P0

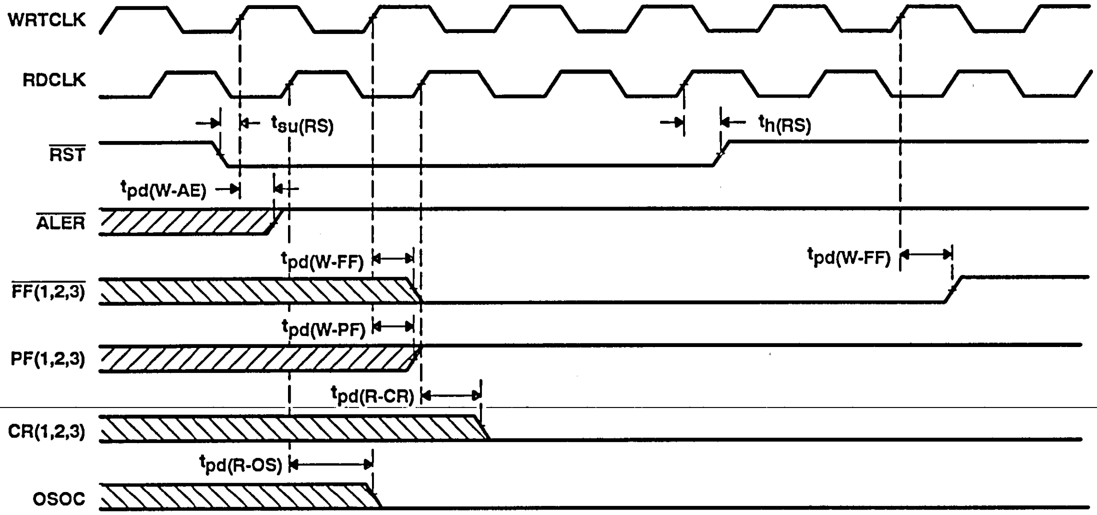

Figure 2. Device Reset

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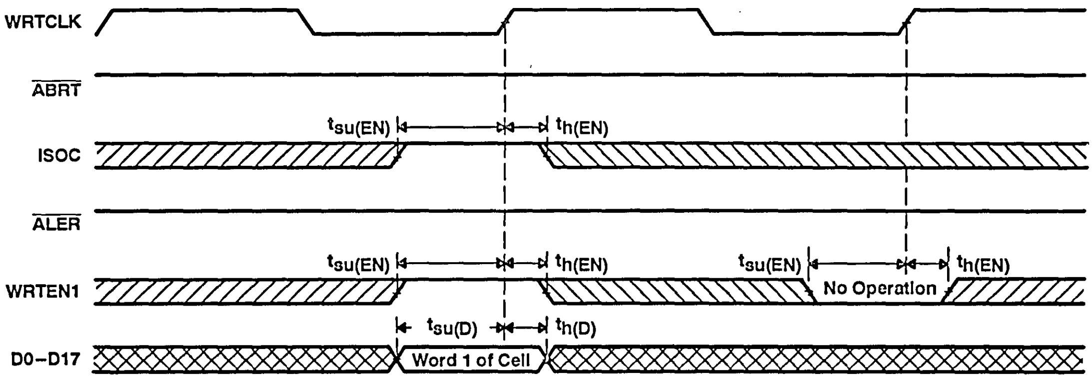
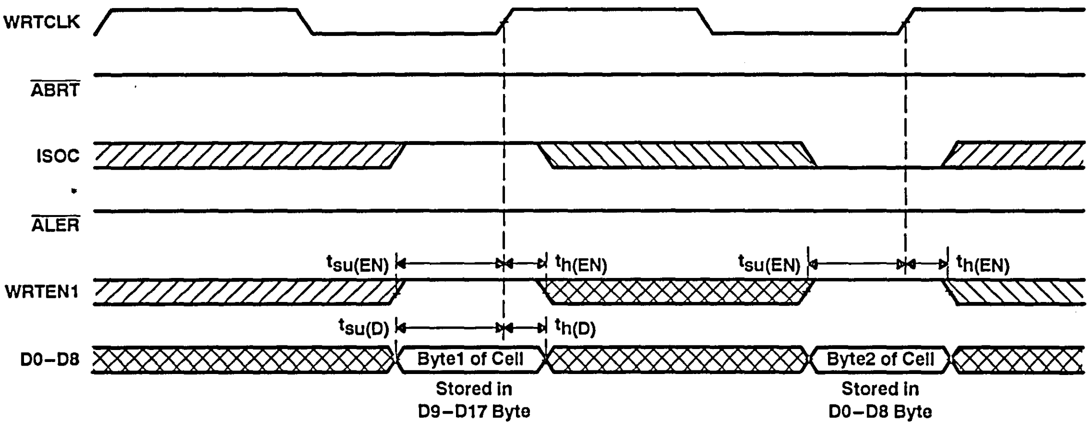


NOTES: A. DWRDY = H
B. Data is loaded to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
C. INSIZ bit of PORT register = 0

Figure 3. Writing Word-Length Data to Queue1



NOTES: A. DWRDY = H
B. Data is loaded to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
C. INSIZ bit of PORT register = 1; INBE bit of PORT register = 1.

Figure 4. Writing Byte Data to Queue1 in Big-Endian Configuration

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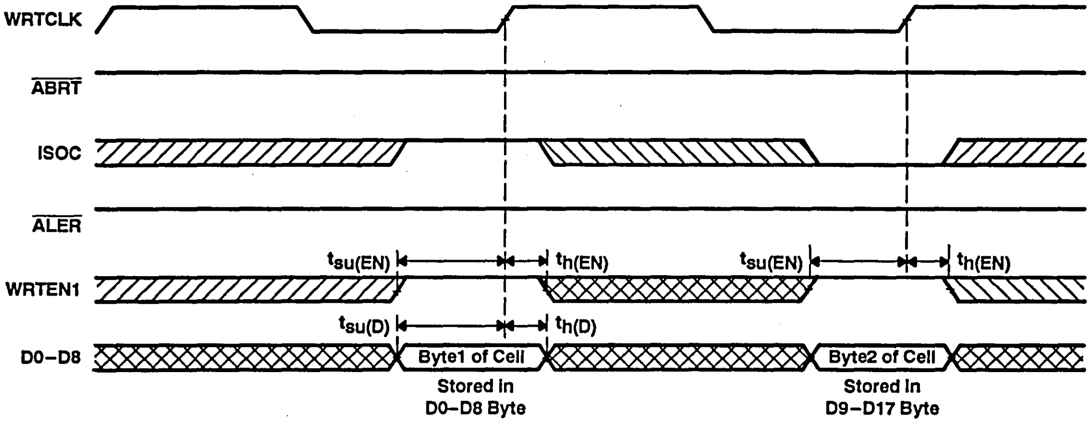
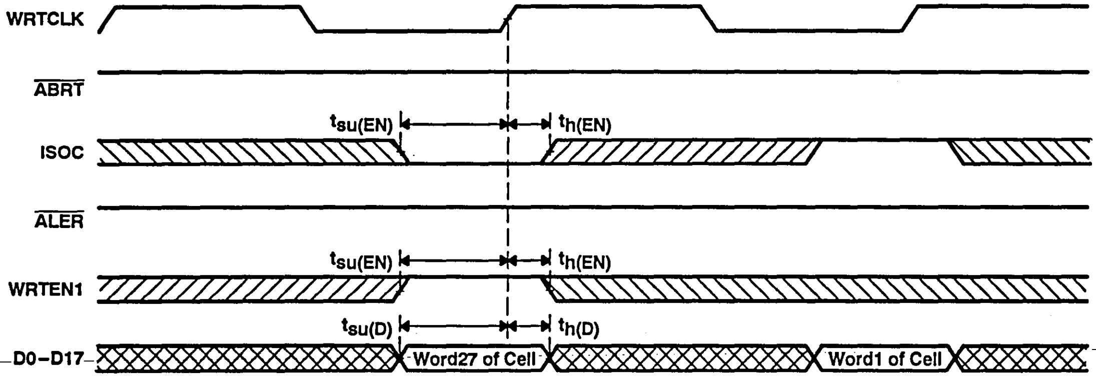


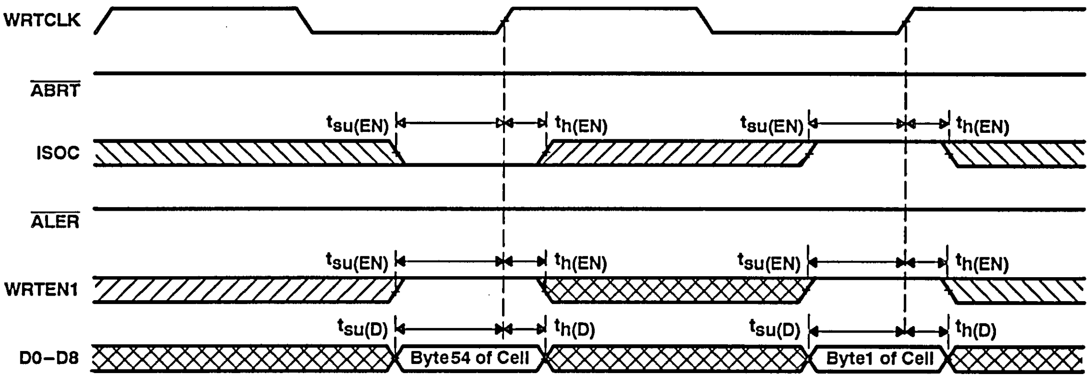
NOTES: A. DWRDY = H
B. Data is loaded to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
C. INSIZ bit of PORT register = 1; INBE bit of PORT register = 0.

Figure 5. Writing Byte Data to Queue1 in Little-Endian Configuration



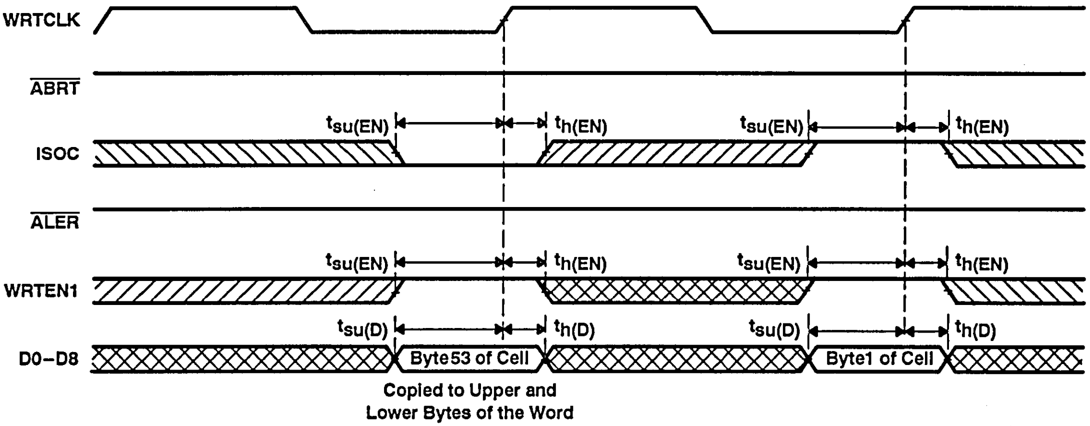
NOTES: A. CLSZ = 27 for the example
B. DWRDY = H
C. A cell is confirmed to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
D. INSIZ bit of PORT register = 0.

Figure 6. Cell-Write Completion With 18-Bit Input



NOTES: A. CLSZ = 27 for the example
B. DWRDY = H
C. A cell is confirmed to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
D. INSIZ bit of PORT register = 1, INSTF bit of PORT register = 0.

Figure 7. Cell-Write-Completion Example With 9-Bit Input and No Byte Stuffing



NOTES: A. CLSZ = 27 for the example
B. DWRDY = H
C. A cell is confirmed to Queue2 or Queue3 in the same manner when the corresponding WRTEN is active.
D. INSIZ bit of PORT register = 1, INSTF bit of PORT register = 1.

Figure 8. Cell-Write-Completion Example With 9-Bit Input and Byte Stuffing

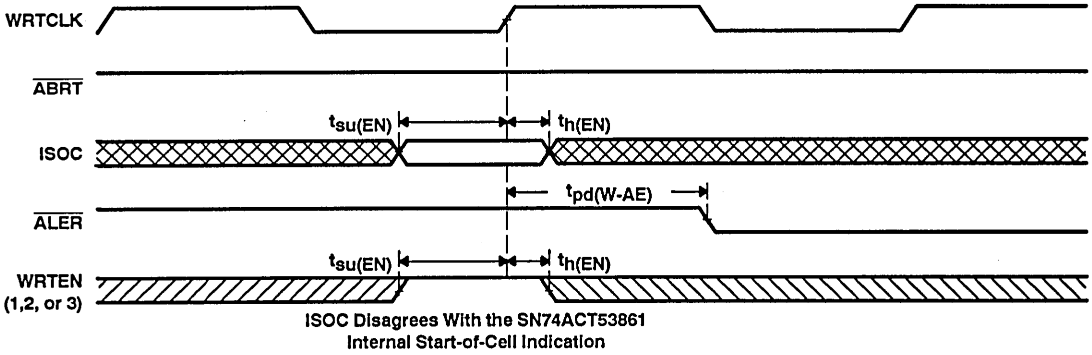
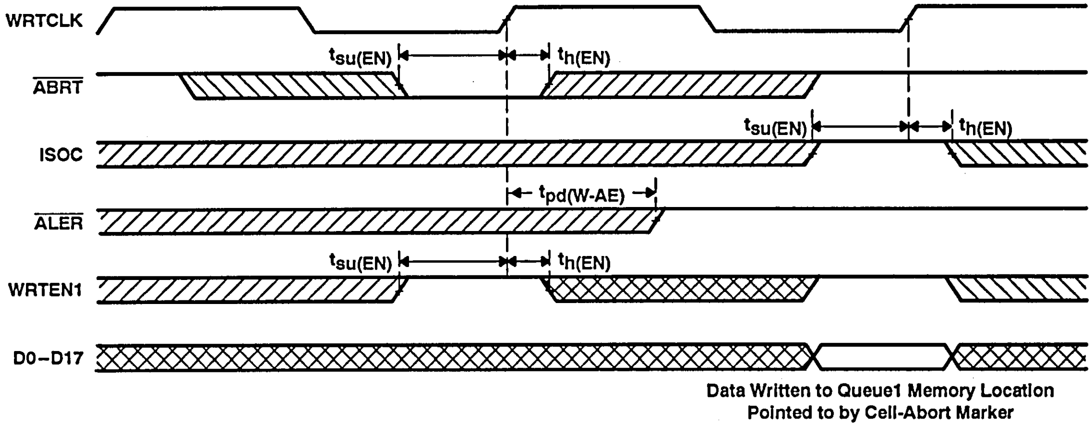


Figure 9. Setting $\overline{ALER}$ When ISOC Is Misaligned



NOTES: A. DWRDY = H
B. Data written since the last confirmation in Queue2 or Queue3 are aborted in the same manner when the corresponding WRTEN is active.

Figure 10. Aborting Data in Queue1 Written Since the Last Cell Completion

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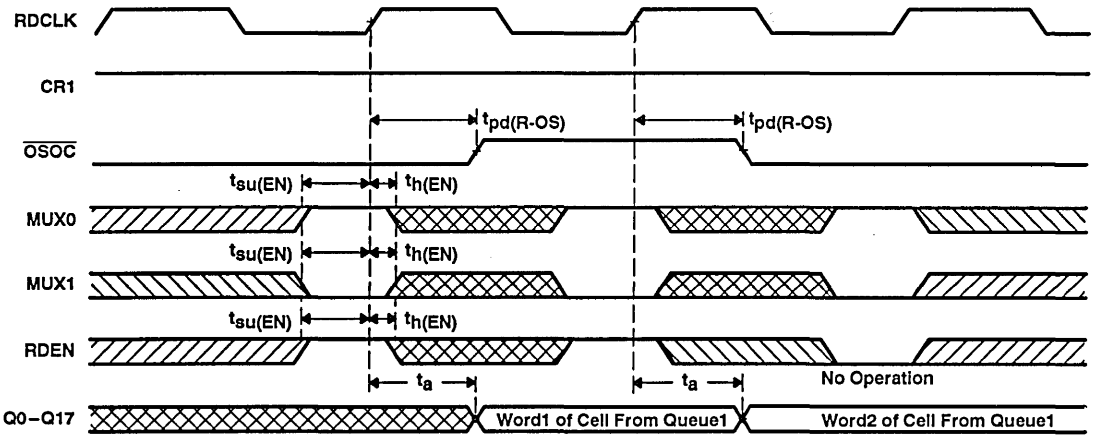
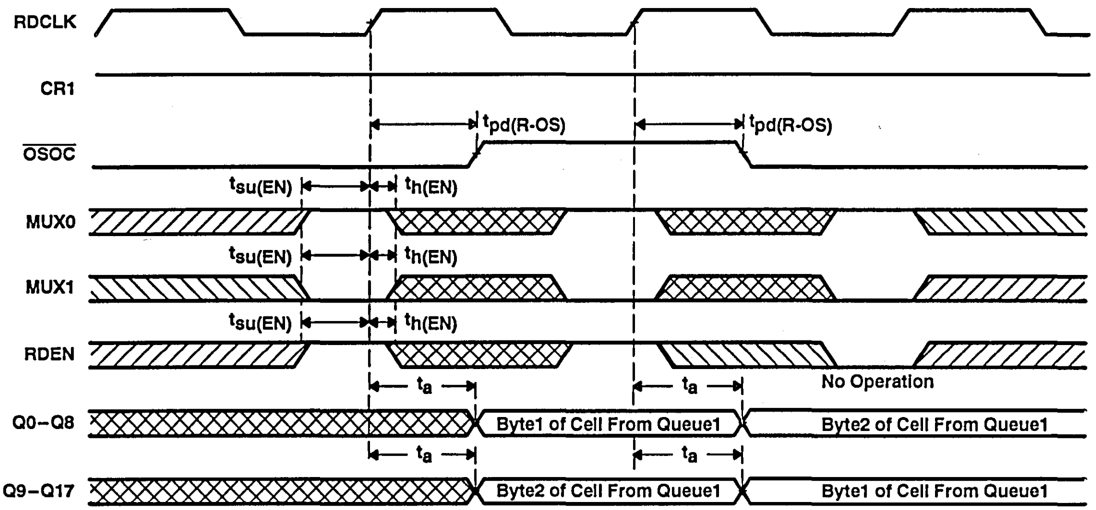


NOTES: A. OE = H
B. Data is read from Queue2 in the same manner when CR2 is high with MUX1 = H and MUX0 = L. Data is read from Queue3 in the same manner when CR3 is high with MUX1 = H and MUX0 = H.
C. OUTSIZ bit of PORT register = 0

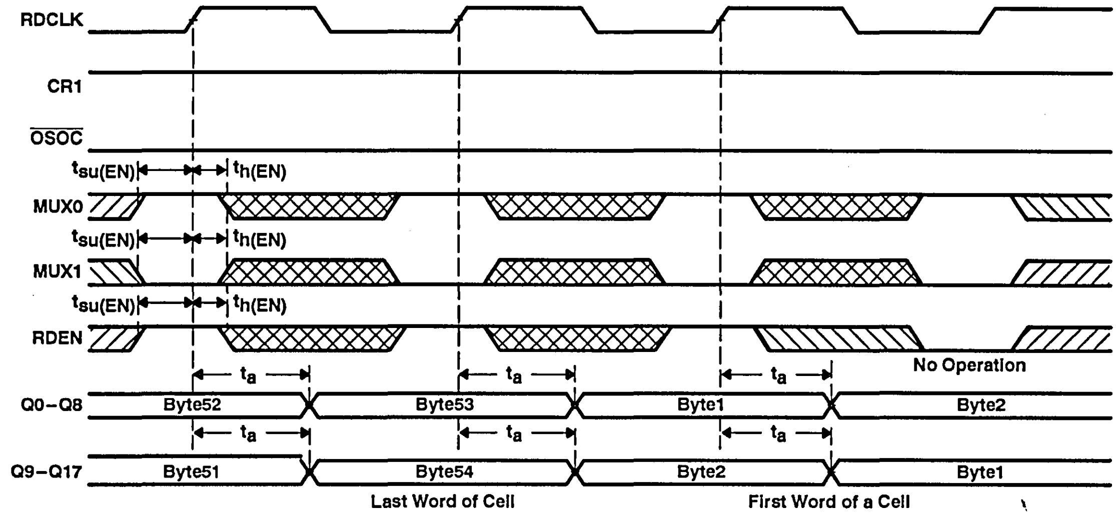
Figure 11. Reading Word-Size Data From Queue1



NOTES: A. OE = H
B. Data is read from Queue2 in the same manner when CR2 is high with MUX1 = H and MUX0 = L. Data is read from Queue3 in the same manner when CR3 is high with MUX1 = H and MUX0 = H.
C. OUTSIZ bit of PORT register = 1

Figure 12. Reading Byte-Size Data From Queue1

PRODUCT PREVIEW



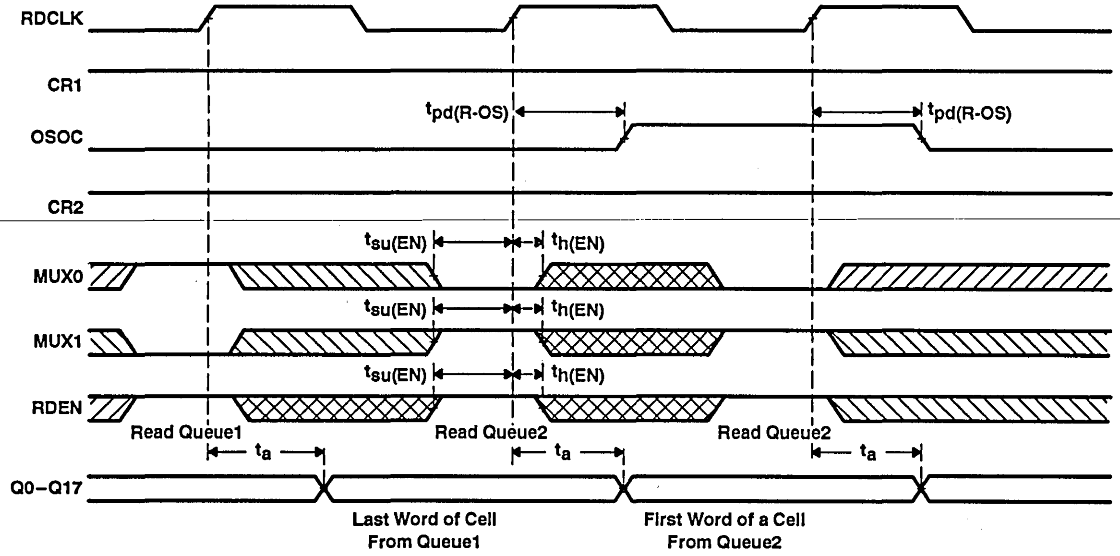
NOTES: D. CLSZ = 27 for the example

E. OE = H

F. Data is read from Queue2 in the same manner when CR2 is high with MUX1 = H and MUX0 = L. Data is read from Queue3 in the same manner when CR3 is high with MUX1 = H and MUX0 = H.

G. OUTSIZ bit of PORT register = 1; OUTSTF bit of PORT register = 1.

Figure 13. Reading Byte-Size Data With Byte Destuffing

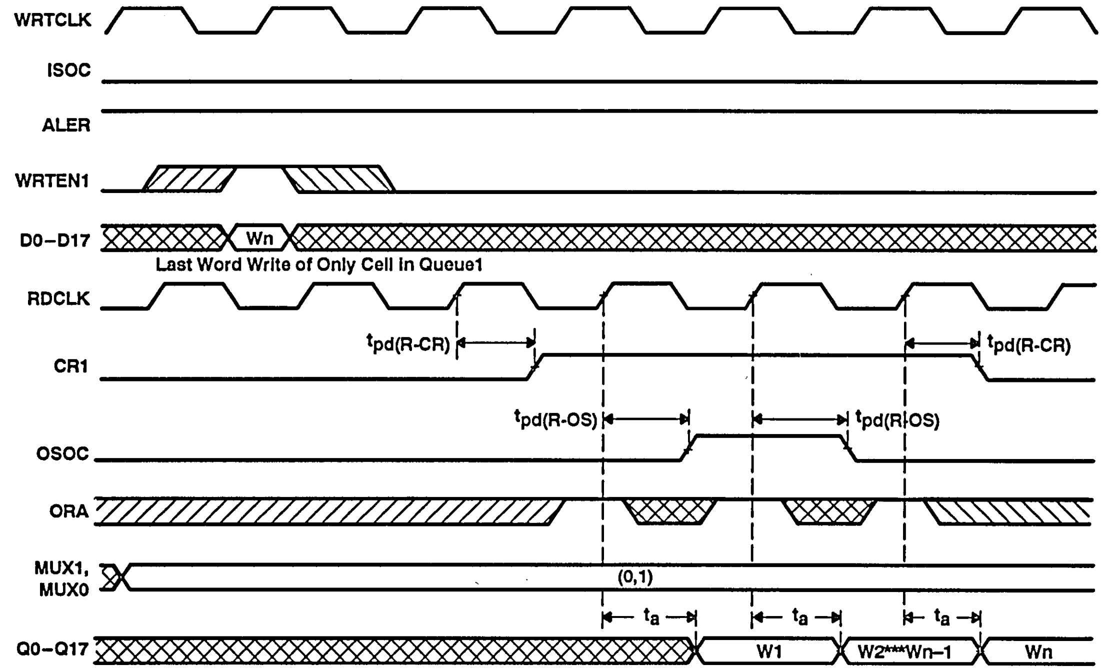


NOTES: A. OE = H

B. If a read from Queue2 is disabled by CR2 low or RDEN low during the cycle the output switch occurs, the previous data held in the Queue2 output register is output.

C. OUTSIZ bit of PORT register = 0

Figure 14. Example of Switching Queues on the Output

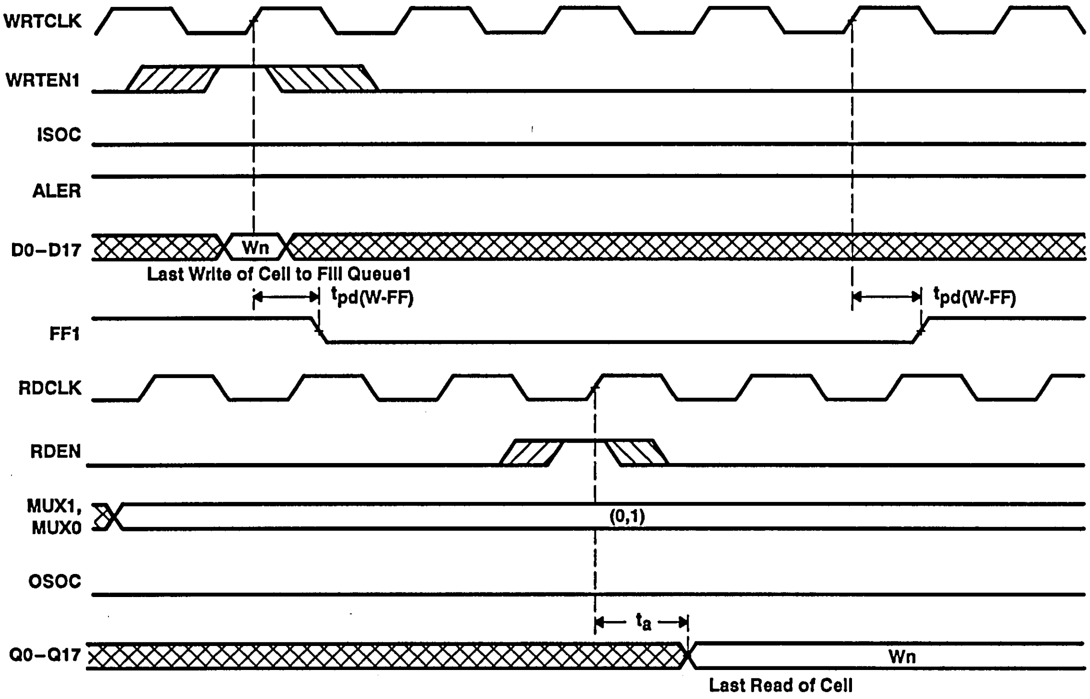


NOTES: D. Outputs enabled (OE = H); word bus size

E. When byte size output bus is used:
- If OUTSTF bit of PORT register = 1, CR1 set low by first byte read of Wn.
- If OUTSTF bit of PORT register = 0, CR1 set low by last byte read of Wn.

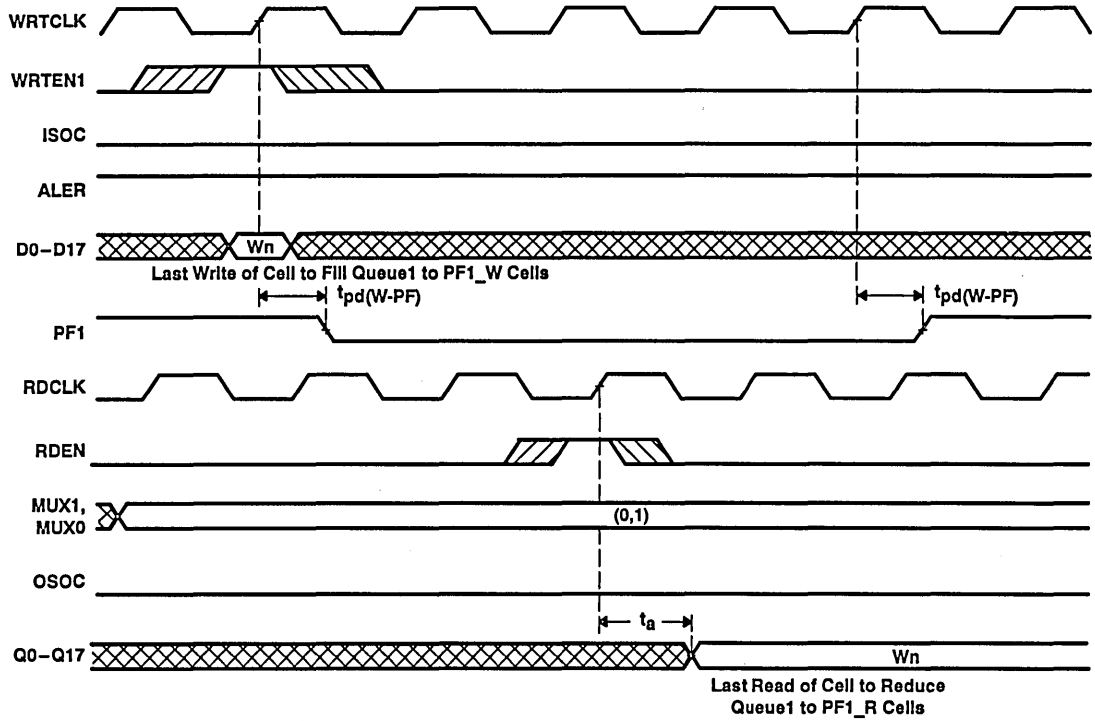
Figure 15. CR1 Timing Example

PRODUCT PREVIEW



NOTES: A. Outputs enabled (OE = H); word bus size
B. When byte size output bus is used:
- If OUTSTF bit of PORT register = 1, FF1 set low by first byte read of Wn.
- If OUTSTF bit of PORT register = 0, FF1 set low by last byte read of Wn.

Figure 16. $\overline{\text{FF1}}$ Timing Example



NOTES: A. Outputs enabled (OE = H); word bus size
B. When byte size output bus is used:
- If OUTSTF bit of PORT register = 1, PF1 set low by first byte read of Wn.
- If OUTSTF bit of PORT register = 0, PF1 set low by last byte read of Wn.

Figure 17. PF1 Timing Example

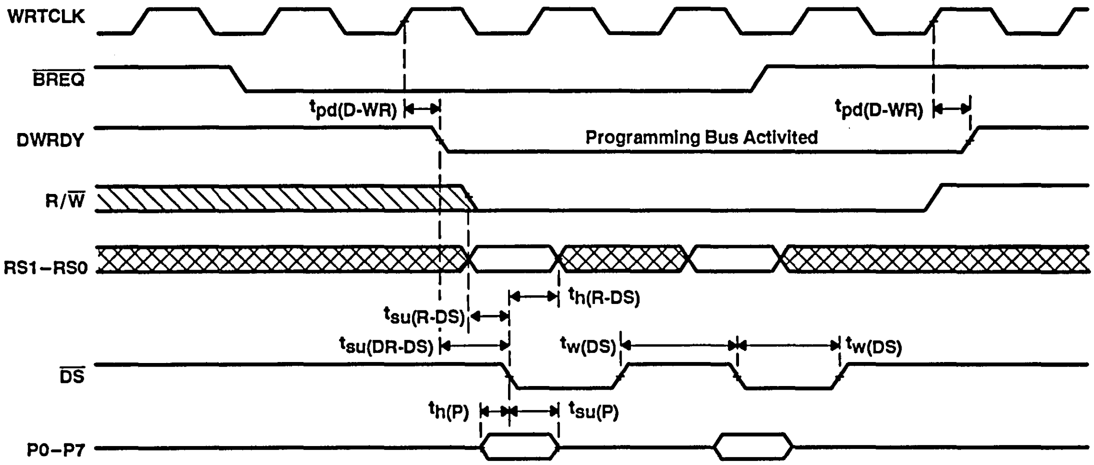


Figure 18. Writing to the Programming Bus

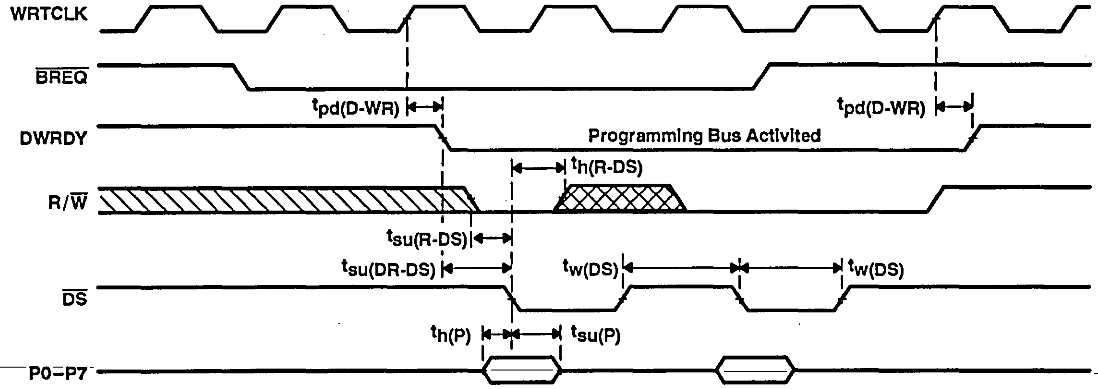


Figure 19. Reading Configuration Registers From the Programming Bus

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0				±5	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0				±5	µA
I_{CC}	V_{CC} = 5.5 V,	$V_I = V_{CC}$ − 0.2 V or 0				400	µA
ΔI_{CC}§	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz			4		pF
C_o	V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 2 through 19)

		MIN	MAX	UNIT
f_{clock}	Clock frequency, WRTCLK or RDCLK		50	MHz
t_c	Clock cycle time, WRTCLK or RDCLK	20		ns
$t_{w(CLKH)}$	Pulse duration, WRTCLK and RDCLK high	7		ns
$t_{w(CLKL)}$	Pulse duration, WRTCLK and RDCLK low	7		ns
$t_{w(DS)}$	Pulse duration, $\overline{\text{DS}}$ high or low	15		ns
$t_{su(D)}$	Setup time, D0–D17 before WRTCLK↑	5		ns
$t_{su(EN)}$	Setup time, ISOC, $\overline{\text{ABRT}}$, WRTEN1, WRTEN2, and WRTEN3 before WRTCLK↑; RDEN, MUX0, and MUX1 before RDCLK↑	5		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RST}}$ low before WRTCLK↑ or RDCLK↑†	7		ns
$t_{su(RS2)}$	Setup time, $\overline{\text{RST}}$ high before first data write	20		ns
$t_{su(R–DS)}$	Setup time, R/$\overline{\text{W}}$ before $\overline{\text{DS}}$↓	8		ns
$t_{su(DR–DS)}$	Setup time, DWRDY before $\overline{\text{DS}}$↓	8		ns
$t_{su(P)}$	Setup time, P0–P7 before $\overline{\text{DS}}$↓	8		ns
$t_{h(D)}$	Hold time, D0–D17 after WRTCLK↑	0		ns
$t_{h(EN)}$	Hold time, ISOC, $\overline{\text{ABRT}}$, WRTEN1, WRTEN2, and WRTEN3 after WRTCLK↑; RDEN, MUX0, and MUX1 after RDCLK↑	0		ns
$t_{h(RS)}$	Hold time, $\overline{\text{RST}}$ low after WRTCLK↑ or RDCLK↑†	7		ns
$t_{h(R–DS)}$	Hold time, R/$\overline{\text{W}}$ after $\overline{\text{DS}}$↓	1		ns
$t_{h(P)}$	Hold time, P0–P7 after $\overline{\text{DS}}$↓	1		ns

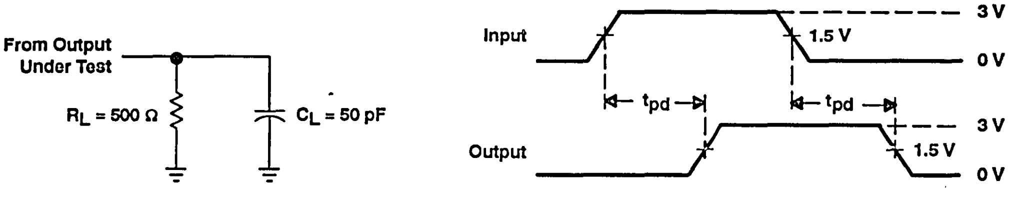
† Requirement to count the clock edge as one of at least four needed to reset a FIFO
‡ Skew time is not a timing constraint for proper device operation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, WRTCLK or RDCLK		50	MHz
t_a	Access time, RDCLK↑ to Q0–Q17		11	ns
$t_{pd(R-CR)}$	Propagation delay time, RDCLK↑ to CR1, CR2, or CR3		10	ns
$t_{pd(R-OS)}$	Propagation delay time, RDCLK↑ to OSOC		10	ns
$t_{pd(W-AE)}$	Propagation delay time, WRTCLK↑ to $\overline{\text{ALER}}$		10	ns
$t_{pd(W-PF)}$	Propagation delay time, WRTCLK↑ to PF1, PF2, or PF3		10	ns
$t_{pd(W-FF)}$	Propagation delay time, WRTCLK↑ to $\overline{\text{FF1}}$, $\overline{\text{FF2}}$, or $\overline{\text{FF3}}$		10	ns
$t_{pd(W-WR)}$	Propagation delay time, WRTCLK↑ to DWRDY		10	ns
$t_{pd(DS–P)}$	Propagation delay time, $\overline{\text{DS}}$↑ to P0–P7		20	ns
$t_{en(Q)}$	Enable time, OE to Q0–Q17 active	1		ns
$t_{dis(Q)}$	Disable time, OE to Q0–Q17 at high impedance		9	ns
$t_{en(P)}$	Enable time, $\overline{\text{POE}}$ and R/$\overline{\text{W}}$ to P0–P7 active	1		ns
$t_{dis(P)}$	Disable time, $\overline{\text{POE}}$ and R/$\overline{\text{W}}$ to P0–P7 at high impedance		9	ns

PRODUCT PREVIEW

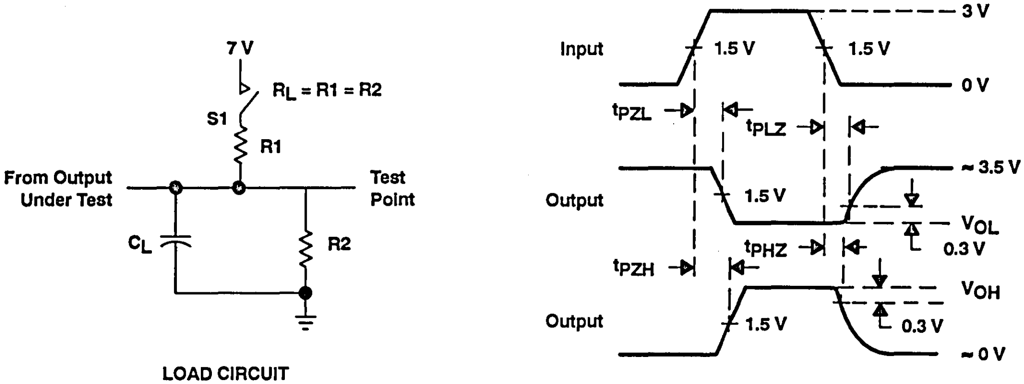
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 9. Standard CMOS Outputs



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 10. 3-State Outputs

PRODUCT PREVIEW

3.3-V LOW-POWERED 18-BIT FIFOS

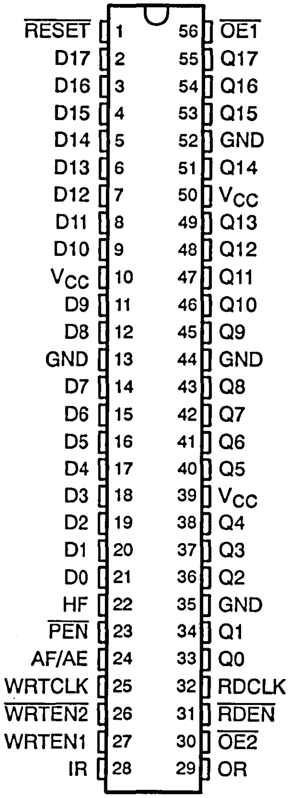
Features	Benefits
• Designed for 3.3-V operations	• Ensures maximum clock speed, access times and low power operations
• Drop in replaceable for the following:	• Allows easy scalability from 5 V to 3.3 V
Clocked 5 V SN74ACT7803 SN74ACT7805 SN74ACT7813	Clocked 3.3 V SN74ALVC7803 SN74ALVC7805 SN74ALVC7813
Strobed 5 V SN74ACT7804 SN74ACT7806 SN74ACT7814	Strobed 3.3 V SN74ALVC7804 SN74ALVC7806 SN74ALVC7814
• Member of Texas Instruments Widebus™ family	• Combined wider data path capability with reduced board space area
• 0.8-µm CMOS process	• Fast access times combined with low power
• TI's advanced clocked interface	• Supports free-running clocks with enables
• Clock frequencies as high as 50 MHz	• Supports high-performance systems
• Fast access time	• Access times as low as 13 ns for improved performance
• High drive capabilities	• −8 mA/16 mA drive capability for high fanout and bus applications
• Depth from 64 to 2K words	• Multiple depths to optimize system applications
• Latched input and output registers	• Allows for fast access times as well as setup and hold times as reduced setup and hold times
• Grey-code flag architecture	• Eliminates race conditions
• First-word fall-through	• Eases system interface requirements
• Programmable AF/AE flag	• Increases design flexibility
• Multistage flag synchronization	• Increases reliability by increasing (MTBF) mean time between failures
• Output edge control (OEC™) circuitry	• Improved reliability
• Distributed V_{CC} and GND	• Improved noise immunity and mutual coupling effects
• JEDEC standard 56-pin SSOP package	• 18-bit product in equal or less space than 9-bit FIFO options

SN74ALVC7803, SN74ALVC7805, SN74ALVC7813
512 × 18, 256 × 18, 64 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORIES

SCAS436 – JUNE 1994

- **Operates at 3-V to 3.6-V V_{CC}**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **Fast Access Times of 13 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **Pin Compatible With SN74ACT7803, SN74ACT7805 and SN74ACT7813**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Lead Spacing**

DL PACKAGE
(TOP VIEW)



description

The SN74ALVC7803, SN74ALVC7805 and SN74ALVC7813 are FIFOs suited for buffering asynchronous data paths at 50-MHz clock rates and 13-ns access times and is designed for 3-V to 3.6-V V_{CC} operation. The 56-pin shrink small-outline (DL) package offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic.

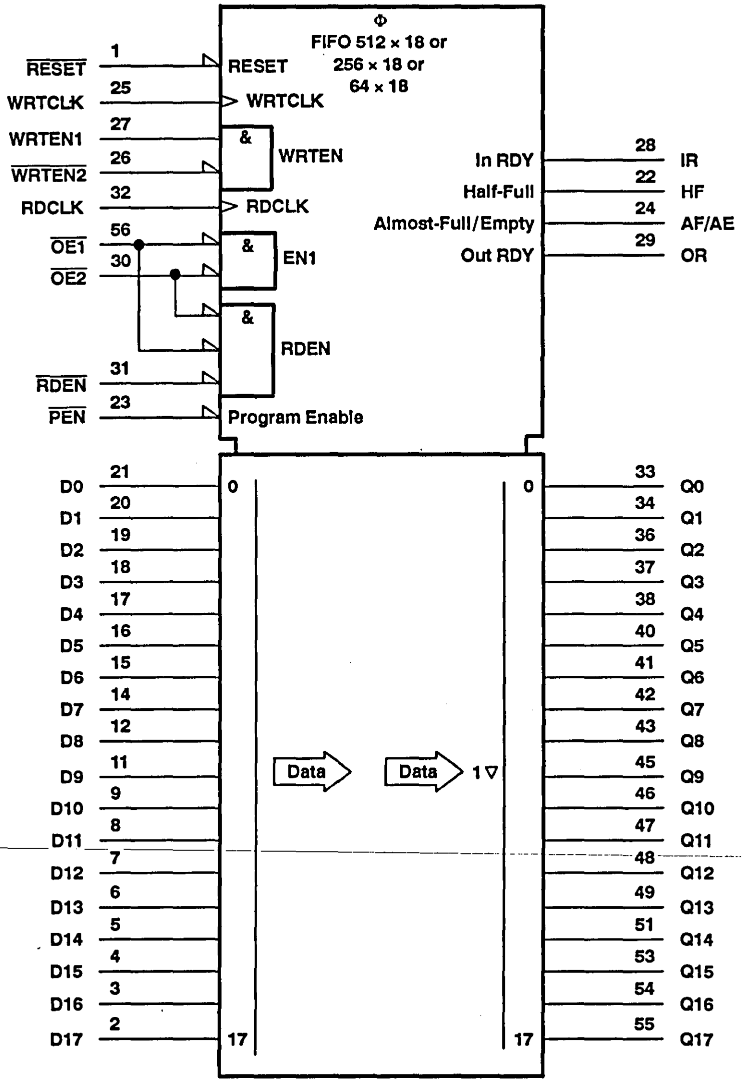
The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

PRODUCT PREVIEW

TEXAS INSTRUMENTS

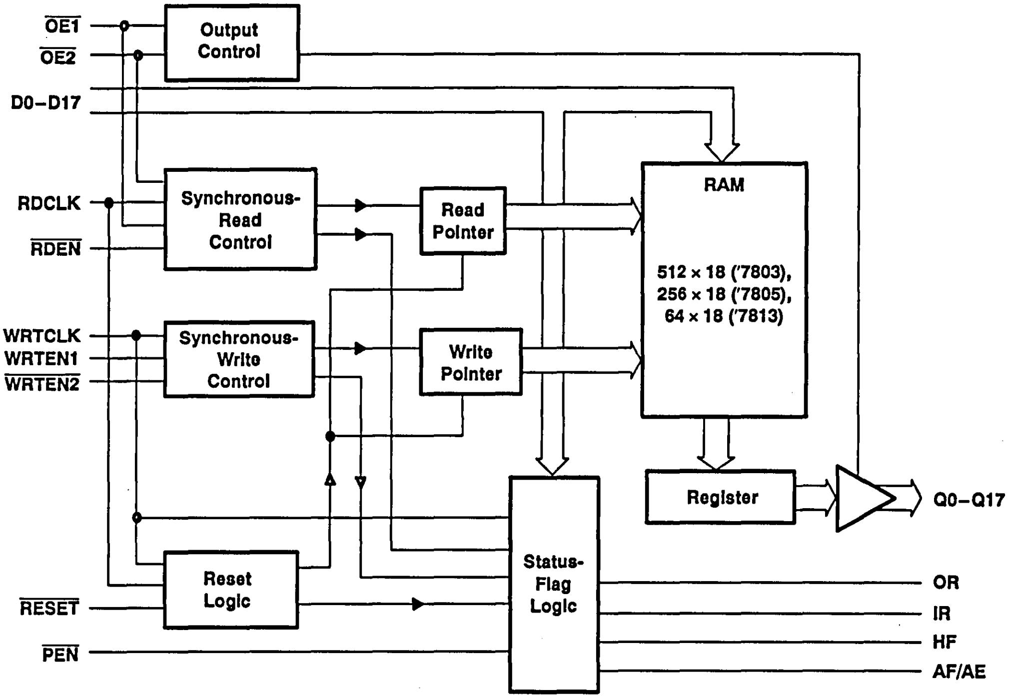
logic symbol[†]



PRODUCT PREVIEW

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for this flag, or the default value of 64 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (512 minus Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
IR	28	O	Input ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	56, 30	I	Output enables. When $\overline{\text{OE1}}$, $\overline{\text{OE2}}$, and $\overline{\text{RDEN}}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{\text{OE1}}$, $\overline{\text{OE2}}$, and $\overline{\text{RDEN}}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
$\overline{\text{RDEN}}$	31	I	Read enable. When $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{\text{WRTEN2}}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{\text{WRTEN2}}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

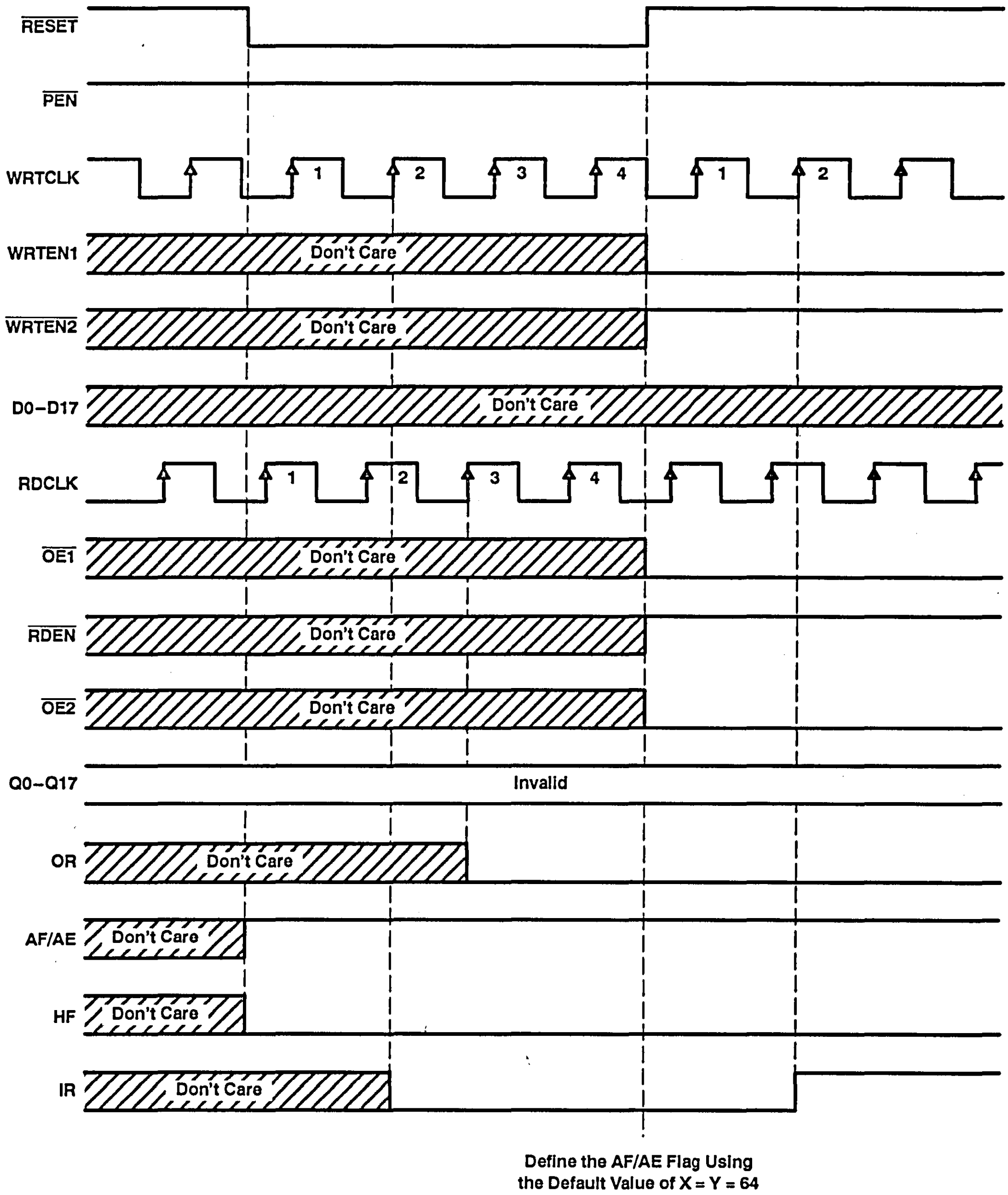
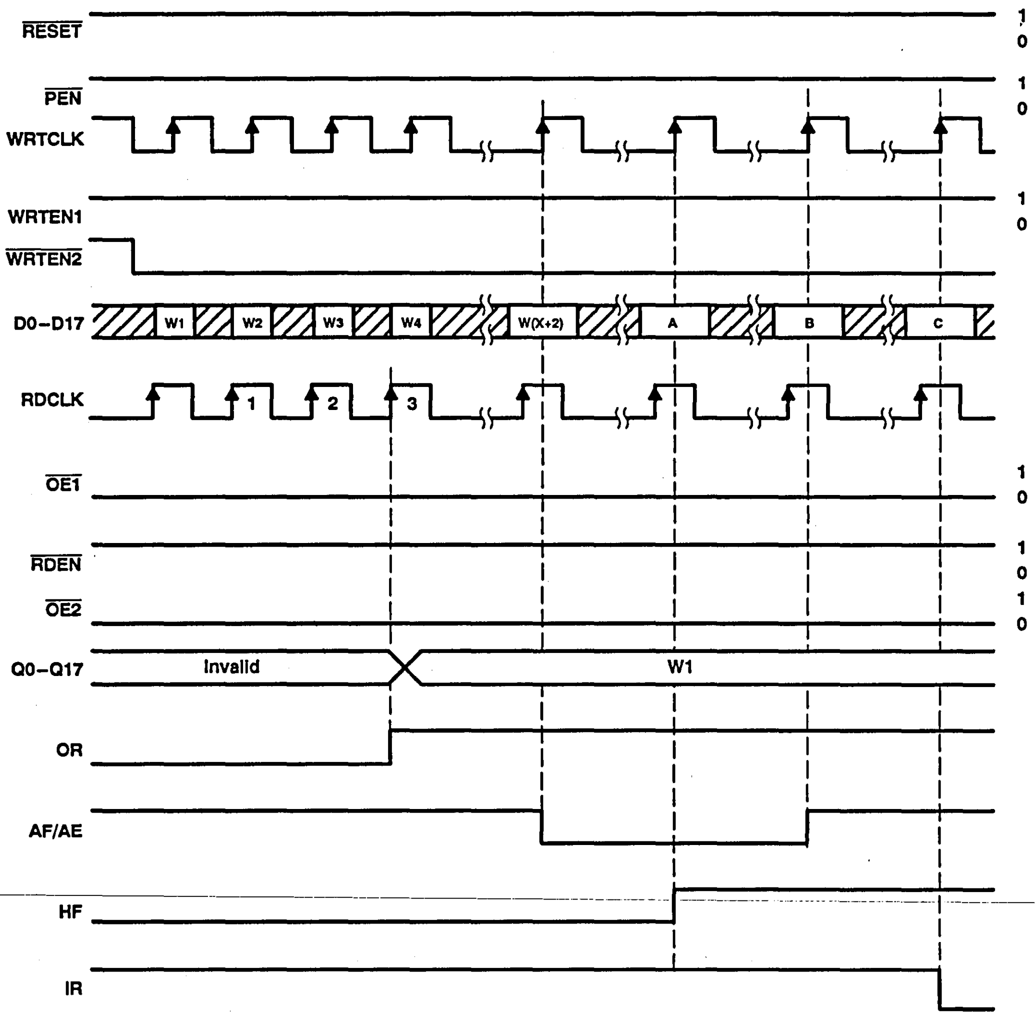


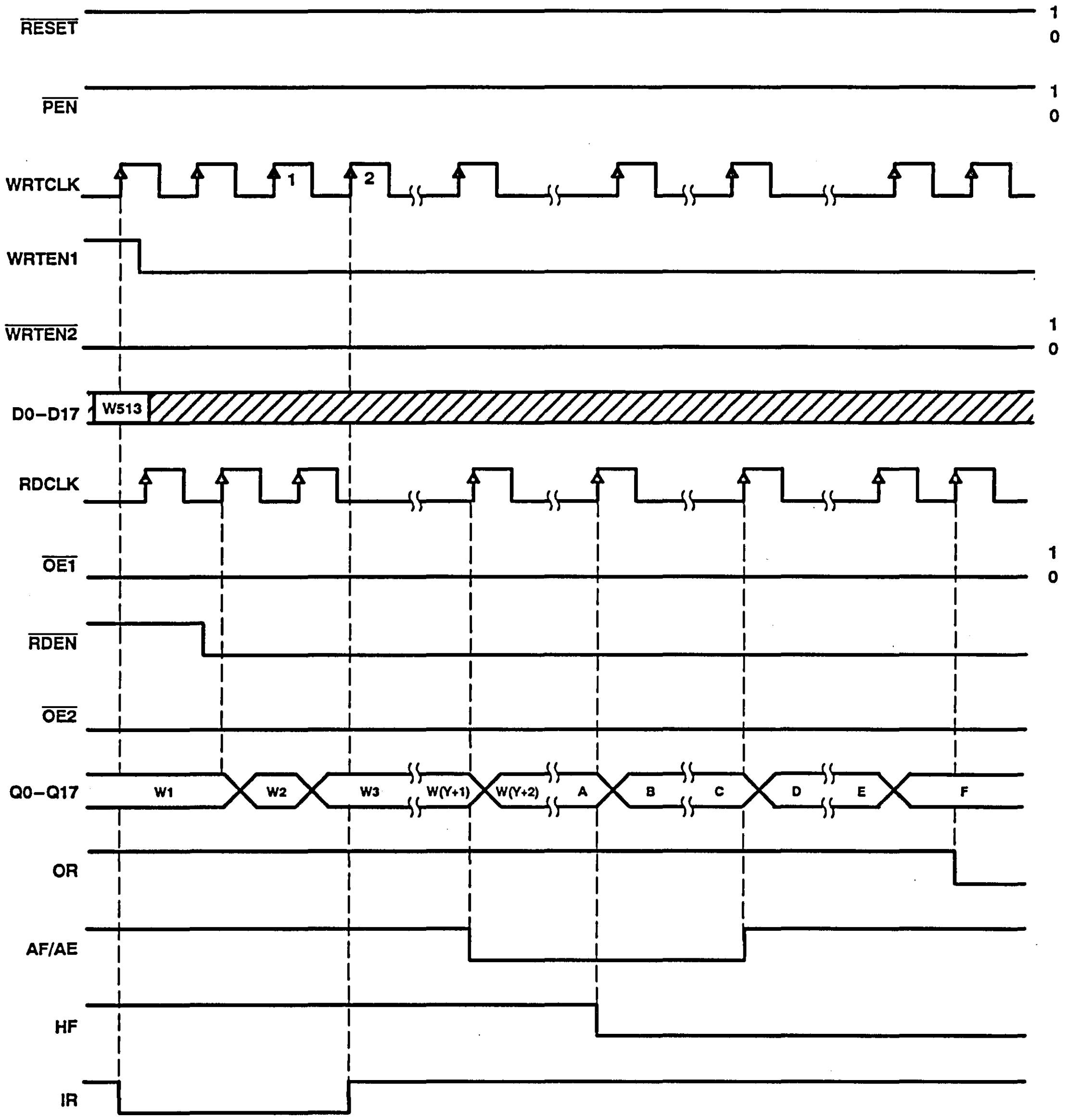
Figure 1. Reset Cycle



DATA WORD NUMBER FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD		
	A/	B	C
SN74ALVC7813	W33	W(65–Y)	W65
SN74ALVC7805	W129	W(257–Y)	W257
SN74ALVC7803	W257	W((513–Y)	W513

Figure 2. FIFO Write



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DATA WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD					
	A	B	C	D	E	F
SN74ALVC7813	W33	W34	W(64–X)	W(65–X)	64	65
SN74ALVC7805	W129	W130	W(256–X)	W(257–X)	W256	W257
SN74ALVC7803	W257	W258	W(512–X)	W(513–X)	W512	W513

Figure 3. FIFO Read

offset values for AF/AE

The almost-full/almost-empty (AF/AE) flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 64 are used. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

Program enable ($\overline{\text{PEN}}$) should be held high throughout the reset cycle. $\overline{\text{PEN}}$ can be brought low only when IR is high. On the following low-to-high transition of WRTCLK, the binary value on D0–D7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D7 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{\text{WRTEN2}}$). A maximum value of 255 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 64, $\overline{\text{PEN}}$ must be held high.

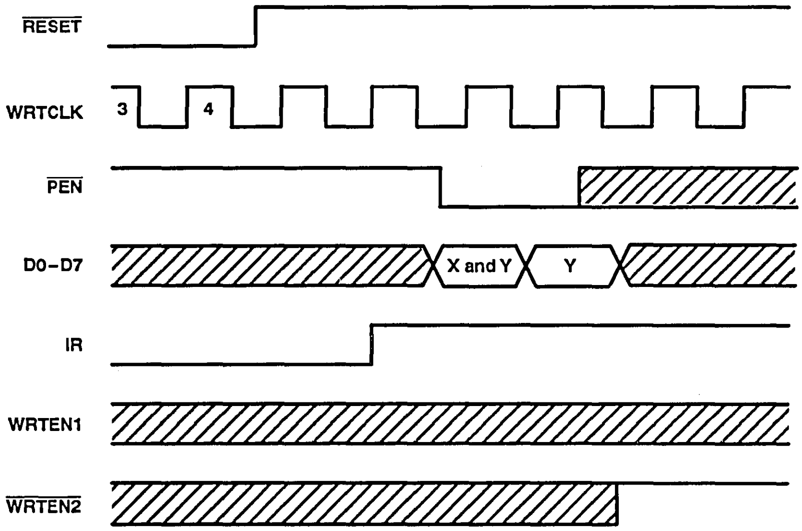


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Voltage applied to a disabled 3-state output	3.6 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions

			'ALVC7803-20 'ALVC7805-20 'ALVC7813-20 V_{CC} = 3.3 V ± 0.3 V		'ALVC7803-25 'ALVC7805-25 'ALVC7813-25 V_{CC} = 3.3 V ± 0.3 V		'ALVC7803-40 'ALVC7805-40 'ALVC7813-40 V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current, Q outputs, Flags	V_{CC} = 3 V		−8		−8		−8	mA
I_{OL}	Low-level output current, Q outputs, Flags	V_{CC} = 3 V		16		16		16	
f_{clock}	Clock frequency			50		40		25	MHz
t_w	Pulse duration	D0−D17 high or low	9		10		14		ns
		WRTCLK high or low	7		8		12		
		RDCLK high or low	7		8		12		
		$\overline{\text{PEN}}$ low	9		9		12		
		WRTEN1 high, $\overline{\text{WRTEN2}}$ low	8		8		12		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$ low	9		9		12		
		$\overline{\text{RDEN}}$ low	8		8		12		
t_{su}	Setup time	D0−D17 before WRTCLK↑	5		5		5		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ before WRTCLK↑	5		5		5		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$ before RDCLK↑	5		6		6		
		$\overline{\text{RDEN}}$ before RDCLK↑	5		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑†	6		6		6		
		$\overline{\text{PEN}}$ before WRTCLK↑	6		6		6		
t_h	Hold time	D0−D17 after WRTCLK↑	0		0		0		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ after WRTCLK↑	0		0		0		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$, $\overline{\text{RDEN}}$ after RDCLK↑	0		0		0		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑†	2		2		2		
		$\overline{\text{PEN}}$ low after WRTCLK↑	2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

† To permit the clock pulse to be utilized for reset purposes

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_{IK} = – 18 mA			–1.2	V
V_{OH}	Flags, Q outputs	V_{CC} = MIN to MAX,	I_{OH} = –100 µA	V_{CC} –0.2			V
		V_{CC} = 3 V,	I_{OH} = –8 mA	2.4			
V_{OL}	Flags, Q outputs	V_{CC} = MIN to MAX,	I_{OL} = 100 µA			0.2	V
	Flags	V_{CC} = 3 V,	I_{OL} = 8 mA			0.4	
	Q outputs	V_{CC} = 3 V,	I_{OL} = 16 mA			0.55	
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±5	µA
I_{OZ}		V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{CC}		V_I = V_{CC} or 0				40	µA
ΔI_{CC}§		V_{CC} = 3.6 V, One input at V_{CC} – 0.6 V	Other inputs at V_{CC} or GND,			500	µA
C_i		V_{CC} = 3.3 V,	V_I = V_{CC} or GND		2.5		pF
C_o		V_{CC} = 3.3 V,	V_O = V_{CC} or GND		3.5		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (OUTPUT)	TO (INPUT)	'ALVC7803-20 'ALVC7805-20 'ALVC7813-20 V_{CC} = 3.3 V ± 0.3 V		'ALVC7803-25 'ALVC7805-25 'ALVC7813-25 V_{CC} = 3.3 V ± 0.3 V		'ALVC7803-40 'ALVC7805-40 'ALVC7813-40 V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	13	4	15	4	20	ns
t_{pd}¶									
t_{pd}	WRTCLK↑	IR	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7	19	7	21	7	23	ns
t_{pd}	RDCLK↑	AF/AE	7	19	7	21	7	23	ns
t_{PLH}	WRTCLK↑	HF	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7	18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	2	11	2	13	2	15	ns
t_{PHL}		HF	2	12	2	14	2	16	
t_{en}	$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	Any Q	2	11	2	11	2	11	ns
t_{dis}			2	11	2	14	2	14	

¶ This parameter is measured with a 50-pF load (see Figure 7).

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 5 MHz	53	pF

APPLICATION INFORMATION

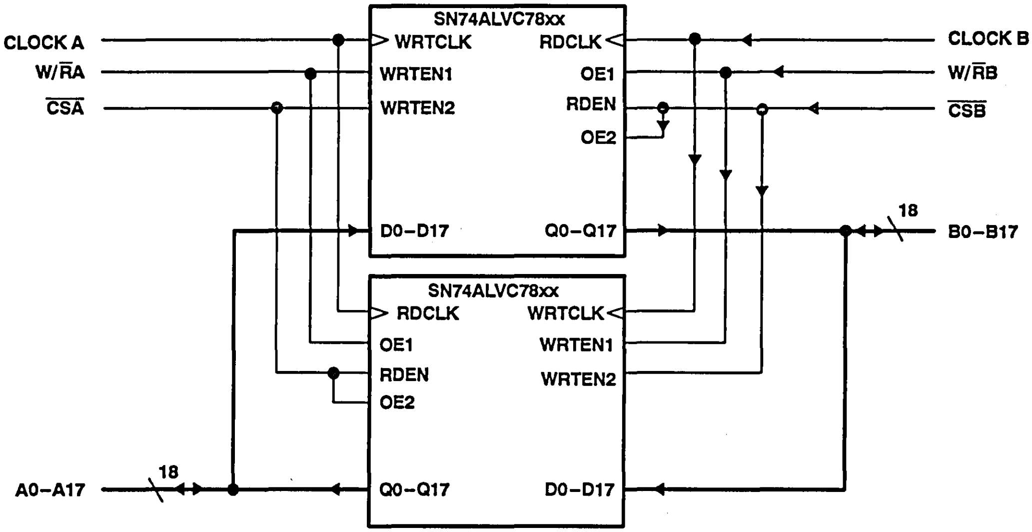


Figure 5. Bidirectional Configuration

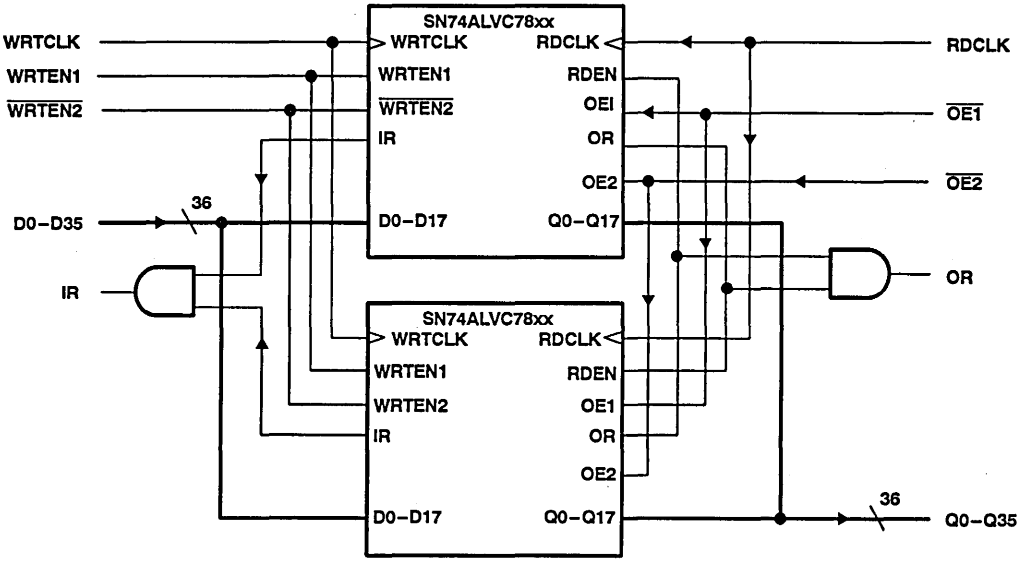


Figure 6. Word-Width Expansion: 512 × 36 Bit , 256 × 36 Bit, and 64 × 36 Bit

PRODUCT PREVIEW

APPLICATION INFORMATION

calculating power dissipation

The maximum power dissipation based on all data outputs changing states on each read can be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

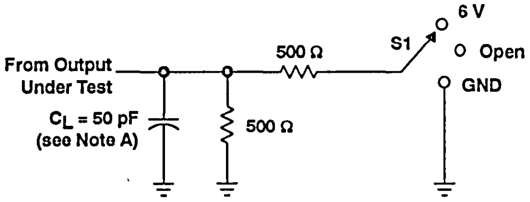
$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times fi) + \Sigma (C_L \times V_{CC}^2 \times fo)$$

where:

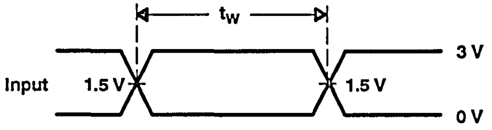
I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

PRODUCT PREVIEW

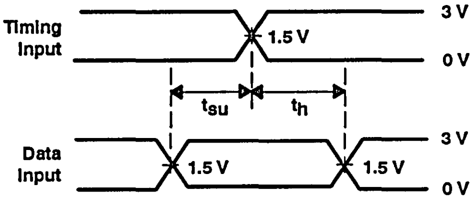
PARAMETER MEASUREMENT INFORMATION



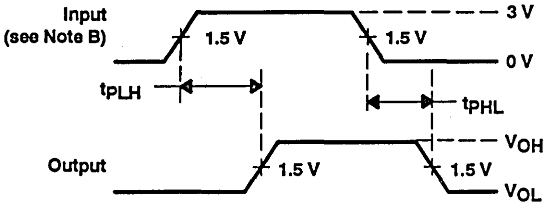
LOAD CIRCUIT FOR OUTPUTS



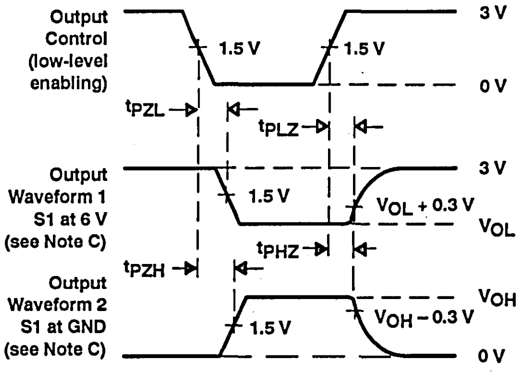
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3-STATE OUTPUTS (ANY Q)

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	GND
	t_{PZL}			6 V
t_{dis}	t_{PHZ}	500 Ω	50 pF	GND
	t_{PLZ}			6 V
t_{pd}	t_{PLH}/t_{PHL}	500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 7. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

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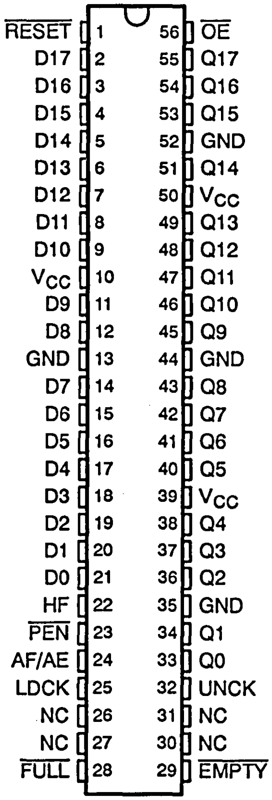
SN74ALVC7804, SN74ALVC7806, SN74ALVC7814
512 × 18, 256 × 18, 64 × 18
FIRST-IN, FIRST-OUT MEMORIES

SCAS437 – JUNE 1994

- Operates at 3-V to 3.6-V V_{CC}
- Load Clock and Unload Clock Can Be Asynchronous or Coincident
- Low-Power Advanced CMOS Technology
- Full, Empty, and Half-Full Flags
- Programmable Almost-Full/Almost-Empty Flag
- Fast Access Times of 18 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates From 0 to 40 MHz
- 3-State Outputs
- Pin Compatible With SN74ACT7804, SN74ACT7806 and SN74ACT7814
- Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing

DL PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALVC7804, SN74ALVC7806, SN74ALVC7814 are 18-bit FIFOs with high speed and fast access times. Data is processed at rates up to 40 MHz with access times of 18 ns in a bit-parallel format. These memories are designed for 3-V to 3.6-V V_{CC} operation.

Data is written into memory on a low-to-high transition of the load clock (LDCK) and is read out on a low-to-high transition of the unload clock (UNCK). The memory is full when the number of words clocked in exceeds the number of words clocked out by 512. When the memory is full, LDCK has no effect on the data residing in memory. When the memory is empty, UNCK has no effect.

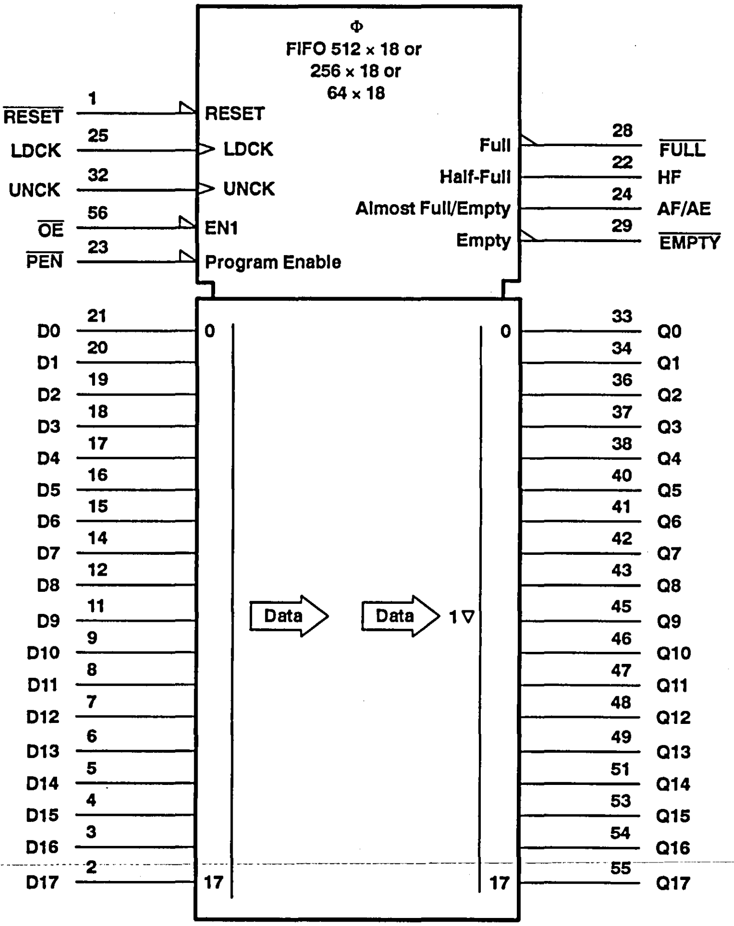
Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 256 or more words and is low when it contains 255 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words. The AF/AE flag is low when the FIFO contains between (X plus 1) and (511 minus Y) words.

A low level on the reset ($\overline{\text{RESET}}$) resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The data outputs are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) is high.

PRODUCT PREVIEW

TEXAS INSTRUMENTS

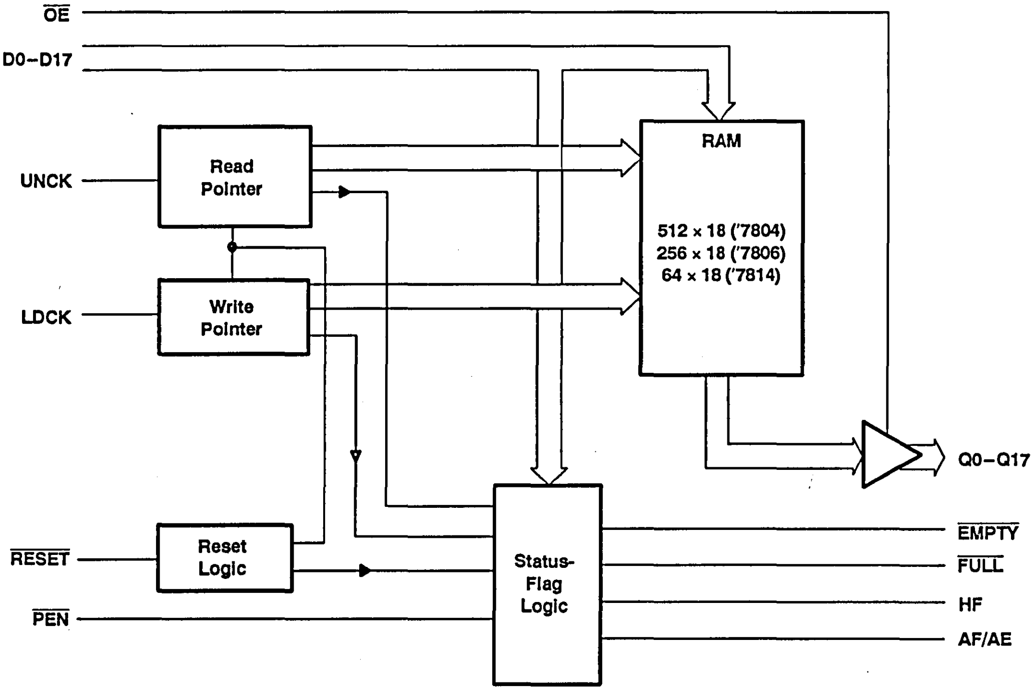
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

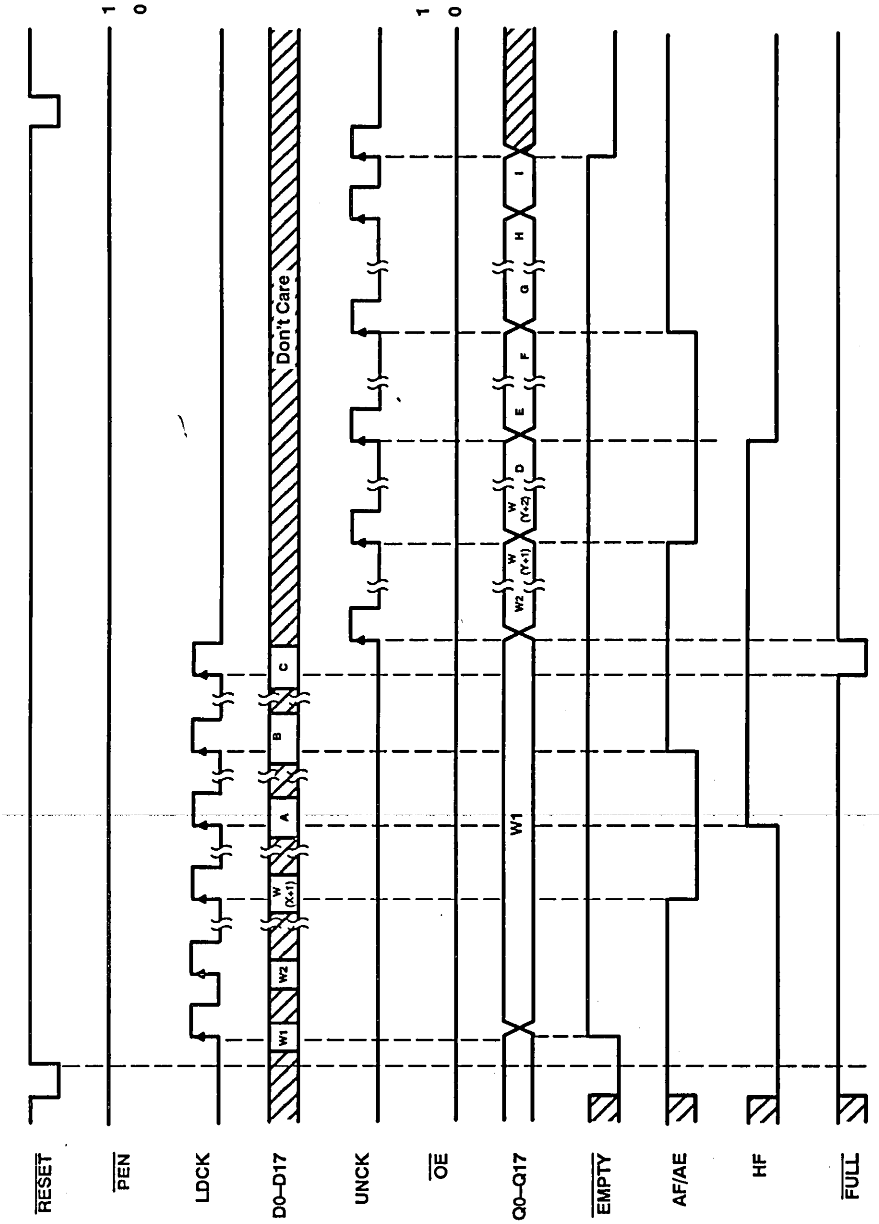
functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AF/AE	24	O	Almost full/almost empty flag. Depth offset values can be programmed for this flag, or the default value of 64 can be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (512 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

PRODUCT PREVIEW



Define the AF/AE Flag
Using the Default Value of X and Y

Figure 1. Write, Read, and Flag Timing Reference

DATA WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD								
	A	B	C	D	E	F	G	H	I
SN74ALVC7814	W32	W(64–Y)	W64	W33	W34	W(64–X)	W(65–X)	W64	W64
SN74ALVC7806	W128	W(256–Y)	W256	W129	W130	W(256–X)	W(257–X)	W255	W256
SN74ALVC7804	W256	W(512–Y)	W512	W257	W258	W(512–X)	W(513–X)	W511	W512

offset values for AF/AE

The almost-full/almost-empty (AF/AE) flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK will reprogram Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 64, $\overline{\text{PEN}}$ must be held high.

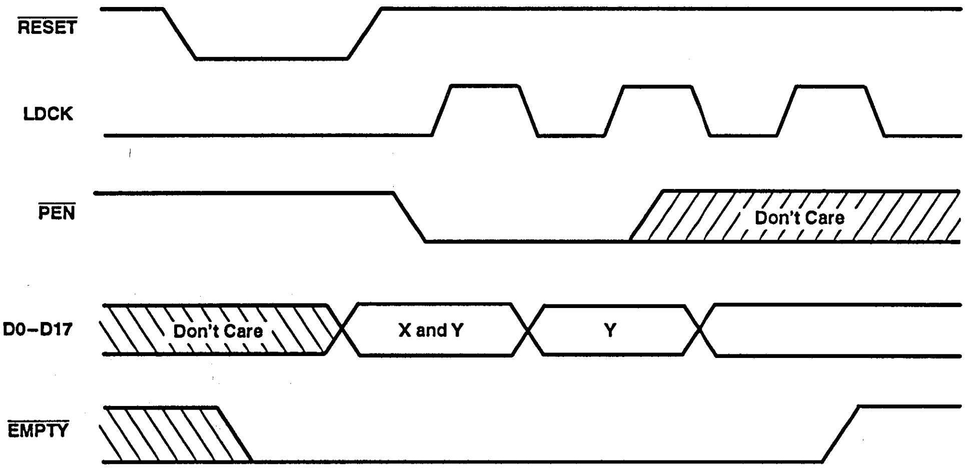


Figure 2. Programming X and Y Separately

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Voltage applied to a disabled 3-state output .... 3.6 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions

			'ALVC7804-25 'ALVC7806-25 'ALVC7814-25 V_{CC} = 3.3 V ± 0.3 V		'ALVC7804-40 'ALVC7806-40 'ALVC7814-40 V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I			0	V_{CC}	0	V_{CC}	V
V_O			0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current, Q outputs, Flags	V_{CC} = 3 V		–8		–8	mA
I_{OL}	Low-level output current, Q outputs, Flags	V_{CC} = 3 V		16		16	mA
f_{clock}	Clock frequency			40		25	MHz
t_w	Pulse duration	D0–D17 high or low	8		12		ns
		LDCK high or low	8		12		
		UNCK high or low	8		12		
		$\overline{\text{PEN}}$ low	8		12		
		$\overline{\text{RESET}}$ low	10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		ns
		LDCK inactive before $\overline{\text{RESET}}$ high	6		6		
		$\overline{\text{PEN}}$ before LDCK↑	5		5		
t_h	Hold time	D0–D17 after LDCK↑	0		0		ns
		$\overline{\text{PEN}}$ high after LDCK low	0		0		
		$\overline{\text{PEN}}$ low after LDCK↑	3		3		
		LDCK inactive after $\overline{\text{RESET}}$ high	6		6		
T_A	Operating free-air temperature		0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{OH}	Flags, Q outputs	V_{CC} = MIN to MAX,	I_{OH} = – 100 µA	V_{CC}−0.2			V
		V_{CC} = 3 V,	I_{OH} = – 8 mA	2.4			
V_{OL}	Flags, Q outputs	V_{CC} = MIN to MAX,	I_{OL} = 100 µA			0.2	V
	Flags	V_{CC} = 3 V,	I_{OL} = 8 mA			0.4	
	Q outputs	V_{CC} = 3 V,	I_{OL} = 16 mA			0.55	
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±5	µA
I_{OZ}		V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{CC}		V_{CC} = 3.6 V,	V_I = V_{CC} or GND and I_O = 0			40	µA
ΔI_{CC}§		V_{CC} = 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC}−0.6 V,			500	µA
C_i		V_{CC} = 3.3 V,	V_I = V_{CC} or GND		2.5		pF
C_o		V_{CC} = 3.3 V,	V_O = V_{CC} or GND		3.5		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ALVC7804-25 'ALVC7806-25 'ALVC7814-25 V_{CC} = 3.3 V ± 0.3 V		'ALVC7804-40 'ALVC7806-40 'ALVC7814-40 V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		40		25		MHz
t_{pd}	LDCK↑	Any Q	9	22	9	24	ns
t_{pd}	UNCK↑		6	18	6	20	
t_{pd}¶	UNCK↑						
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	6	17	6	19	ns
t_{PHL}	UNCK↑		6	17	6	19	
t_{PHL}	$\overline{\text{RESET}}$ low		4	18	4	20	
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6	17	6	19	ns
t_{PLH}	UNCK↑		6	17	6	19	
t_{PLH}	$\overline{\text{RESET}}$ low		4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7	20	7	22	ns
t_{pd}	UNCK↑		7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low		2	12	2	14	
t_{PLH}	LDCK↑	HF	5	20	5	22	ns
t_{PHL}	UNCK↑		7	20	7	22	
t_{PHL}	$\overline{\text{RESET}}$ low		3	14	3	16	
t_{en}	$\overline{\text{OE}}$	Any Q	2	10	2	11	ns
t_{dis}			2	11	2	12	

¶ This parameter tested with a 50-pF load (see Figure 4).

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

APPLICATION INFORMATION

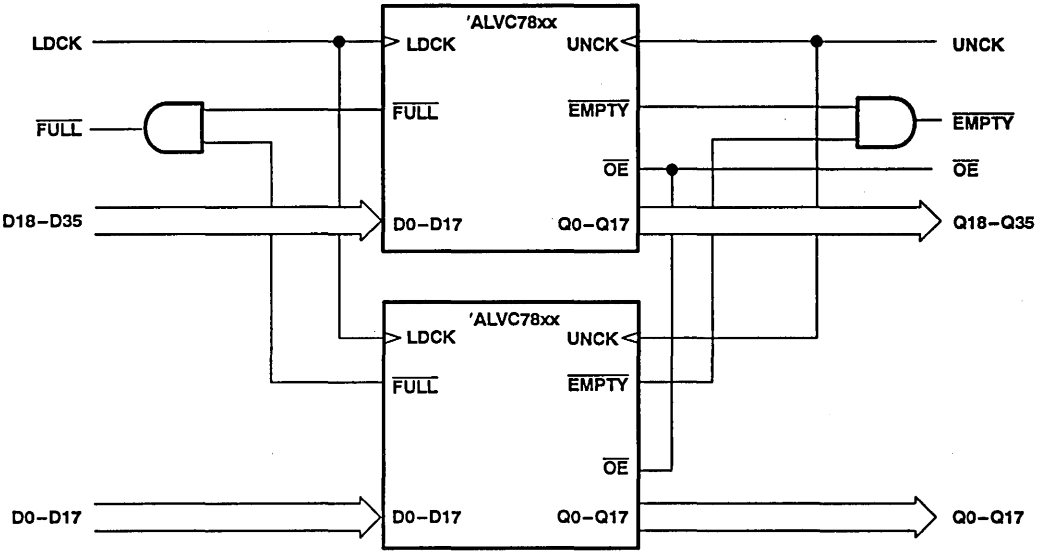


Figure 3. Word-Width Expansion: 512 × 36 Bit, 256 × 36 Bit, and 64 × 36 Bit

calculating power dissipation

The maximum power dissipation based on all data outputs changing states on each read can be calculated using:

$$P_t = V_{CC} \times [I_{CCF} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_L \times V_{CC}{}^2 \times fo)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

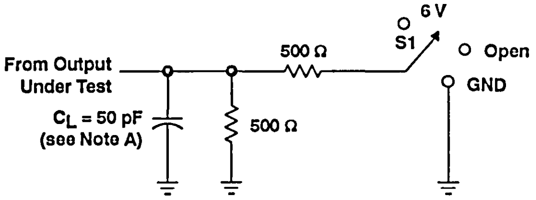
$$P_t = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_{pd} \times V_{CC}{}^2 \times fi) + \Sigma\,(C_L \times V_{CC}{}^2 \times fo)$$

where:

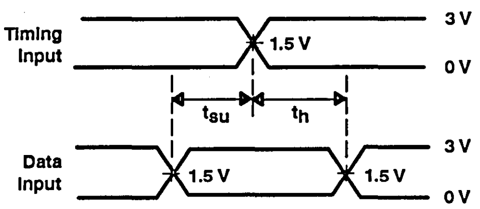
I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

PRODUCT PREVIEW

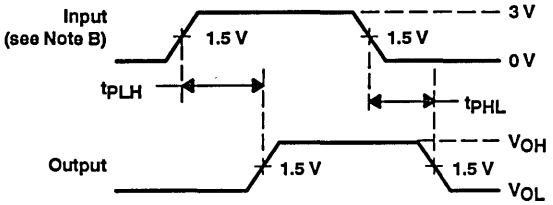
PARAMETER MEASUREMENT INFORMATION



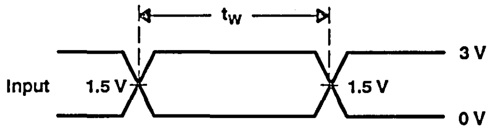
LOAD CIRCUIT FOR OUTPUTS



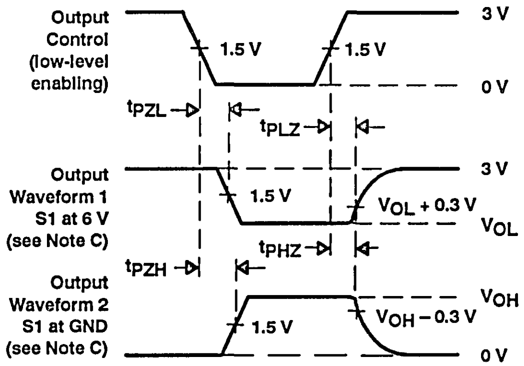
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PRODUCT PREVIEW

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3-STATE OUTPUTS (ANY Q)

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	GND
	t_{PZL}			6 V
t_{dis}	t_{PHZ}	500 Ω	50 pF	GND
	t_{PLZ}			6 V
t_{pd}	t_{PLH}/t_{PHL}	500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 4. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

TELECOM SINGLE-BIT FIFOS

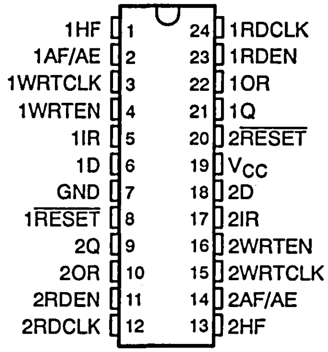
Features	Benefits
0.8-μm CMOS process	High-performance, low-power process
Dual independent FIFOs	Allows either a transmit and receive configuration, two transmits, or two receive operations
Separate inputs, outputs, resets and enables	Greater design flexibility
Synchronous IR and OR flags	Flag synchronization is done on chip.
TI's advanced clocked interface	Supports free-running clocks with enables
Empty, full, and almost-full/almost-empty flags	Multiple status flags enables greater system control
–40°C/85°C characterization	Industrial temperature range for field applications

SN74ACT2226, SN74ACT2228
DUAL 64 × 1 AND DUAL 256 × 1
CLOCKED FIRST-IN, FIRST-OUT MEMORIES

SCAS219A – JUNE 1992 – REVISED AUGUST 1993

- Dual Independent FIFOs Organized as:
  - 64 Words by 1 Bit Each – SN74ACT2226
  - 256 Words by 1 Bit Each – SN74ACT2228
- Free-Running Read and Write Clocks Can Be Asynchronous or Coincident on Each FIFO
- Input-Ready Flags Synchronized to Write Clocks
- Output-Ready Flags Synchronized to Read Clocks
- Half-Full and Almost-Full/Almost-Empty Flags
- Support Clock Frequencies up to 22 MHz
- Characterized for Operation Over the Industrial Temperature Range (–40°C to 85°C)
- Access Times of 20 ns
- Low-Power Advanced CMOS Technology
- Available in 24-Pin SOIC (DW) Package

DW PACKAGE
(TOP VIEW)



description

The SN74ACT2226 and SN74ACT2228 are dual FIFOs suited for a wide range of serial data buffering applications including elastic stores for frequencies up to T2 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2226) or 256 × 1 (SN74ACT2228) and has control signals and status flags for independent operation. Output flags per FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

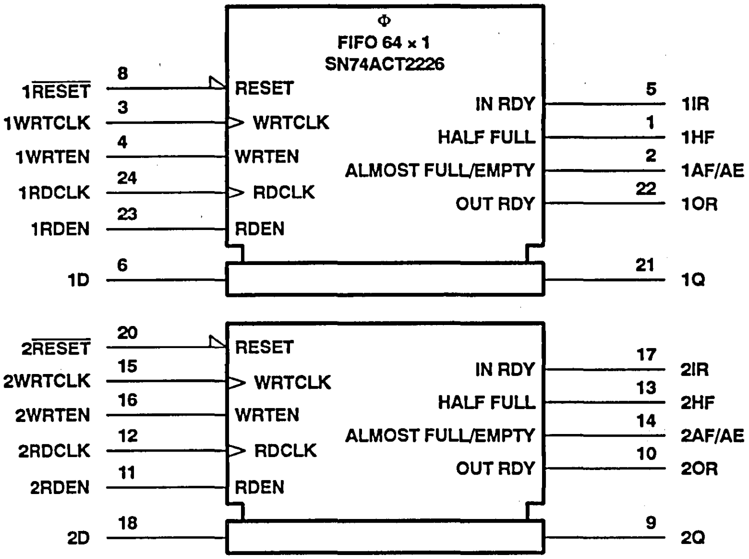
Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write-enable (1WRTEN or 2WRTEN) input and input-ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read-clock (1RDCLK or 2RDCLK) input when the read-enable (1RDEN or 2RDEN) input and output-ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO can be asynchronous to one another.

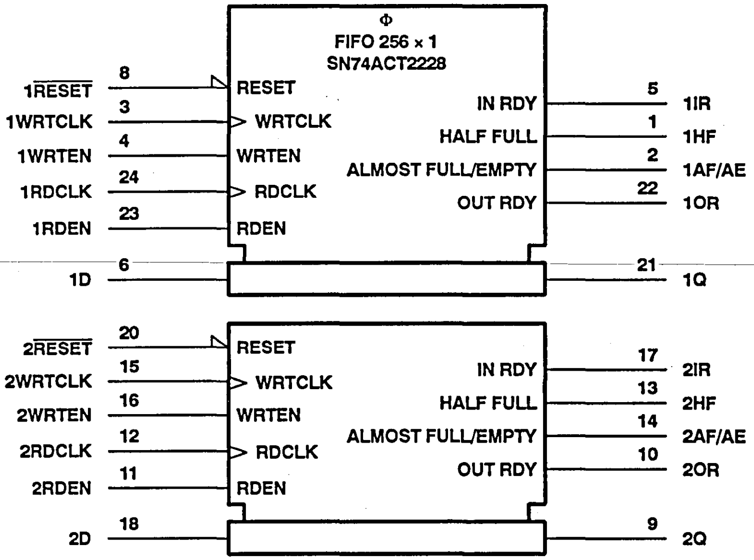
Each input-ready flag (1IR or 2IR) is synchronized by two flip-flop stages to its write clock (1WRTCLK or 2WRTCLK), and each output-ready flag (1OR or 2OR) is synchronized by three flip-flop stages to its read clock (1RDCLK or 2RDCLK). This multistage synchronization ensures reliable flag-output states when data is written and read asynchronously.

A half-full flag (1HF or 2HF) is high when the number of bits stored in its FIFO is greater than or equal to half the depth of the FIFO. An almost-full/almost-empty flag (1AF/AE or 2AF/AE) is high when eight or less bits are stored in its FIFO and when eight or fewer empty locations are left in the FIFO. A bit present on the data output is not stored in the FIFO.

The SN74ACT2226 and SN74ACT2228 are characterized for operation from –40°C to 85°C.

logic symbols†





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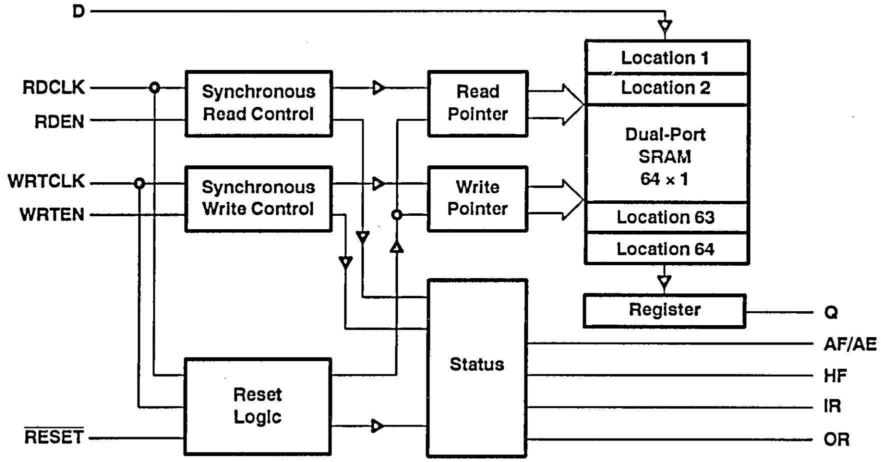
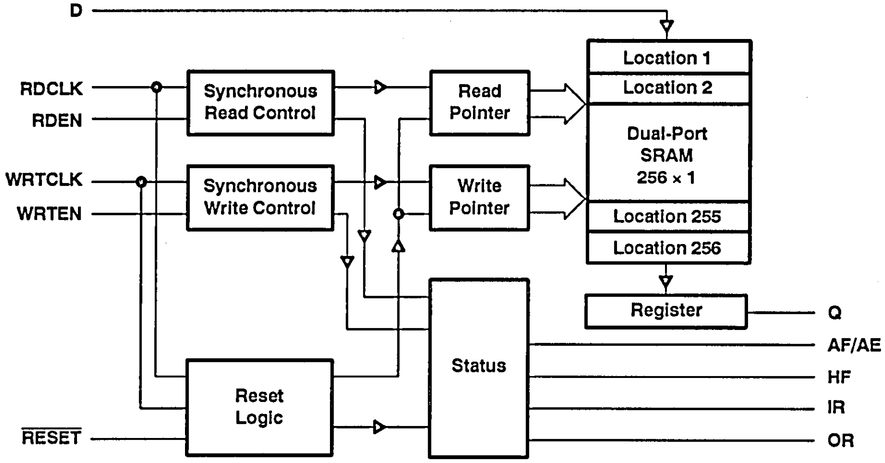
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ACT2226 functional block diagram (each FIFO)



SN74ACT2228 functional block diagram (each FIFO)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
1AF/AE 2AF/AE	2 14	O	Almost-full/almost-empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset.
1D 2D	6 18	I	Data input
GND	7		Ground
1HF 2HF	1 15	O	Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset.
1IR 2IR	5 17	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset.
1OR 2OR	22 10	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
1Q 2Q	21 9	O	Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is asserted high to indicate ready data.
1RDCLK 2RDCLK	24 12	I	Read clock. RDCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK.
1RDEN 2RDEN	23 11	I	Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK.
1$\overline{\text{RESET}}$ 2$\overline{\text{RESET}}$	8 20	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. Before it is used, a FIFO must be reset after power up.
V_{CC}	19		Supply voltage
1WRTCLK 2WRTCLK	3 15	I	Write clock. WRTCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK.
1WRTEN 2WRTEN	4 16	I	Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

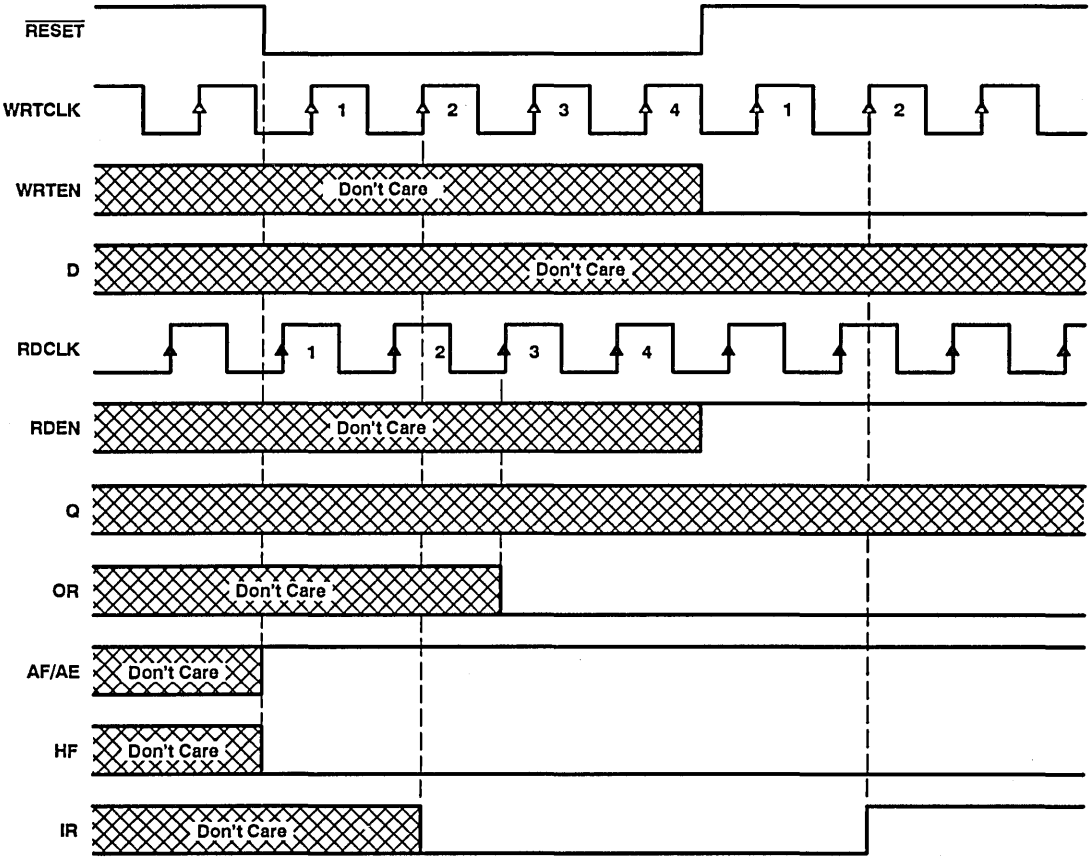
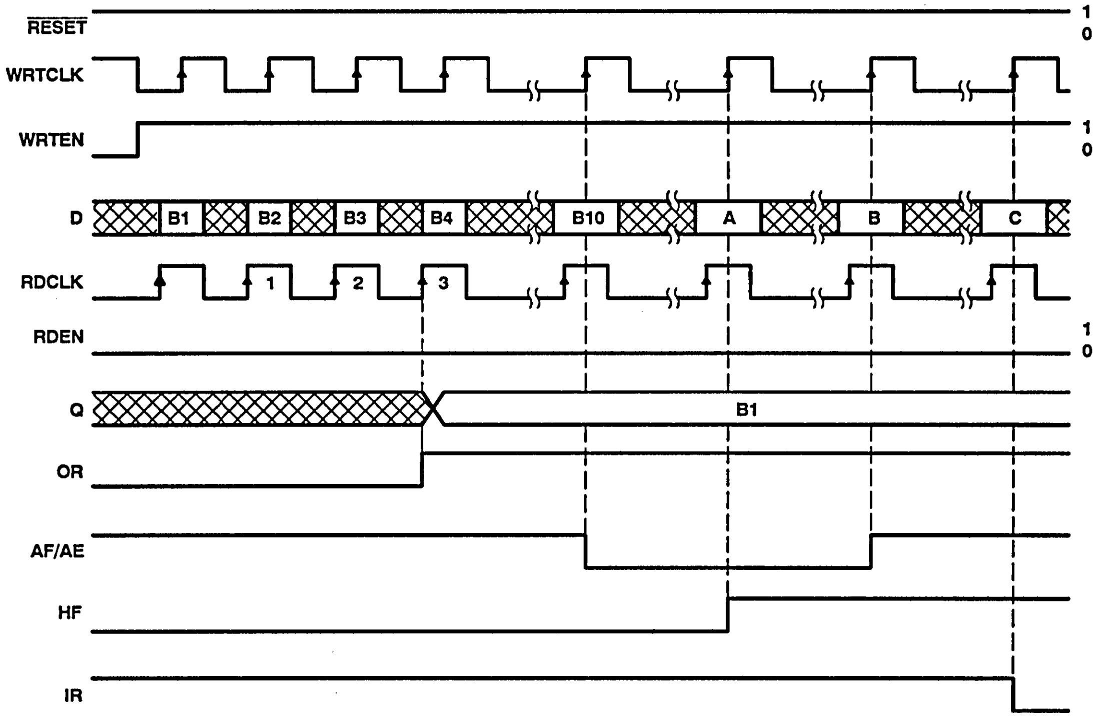


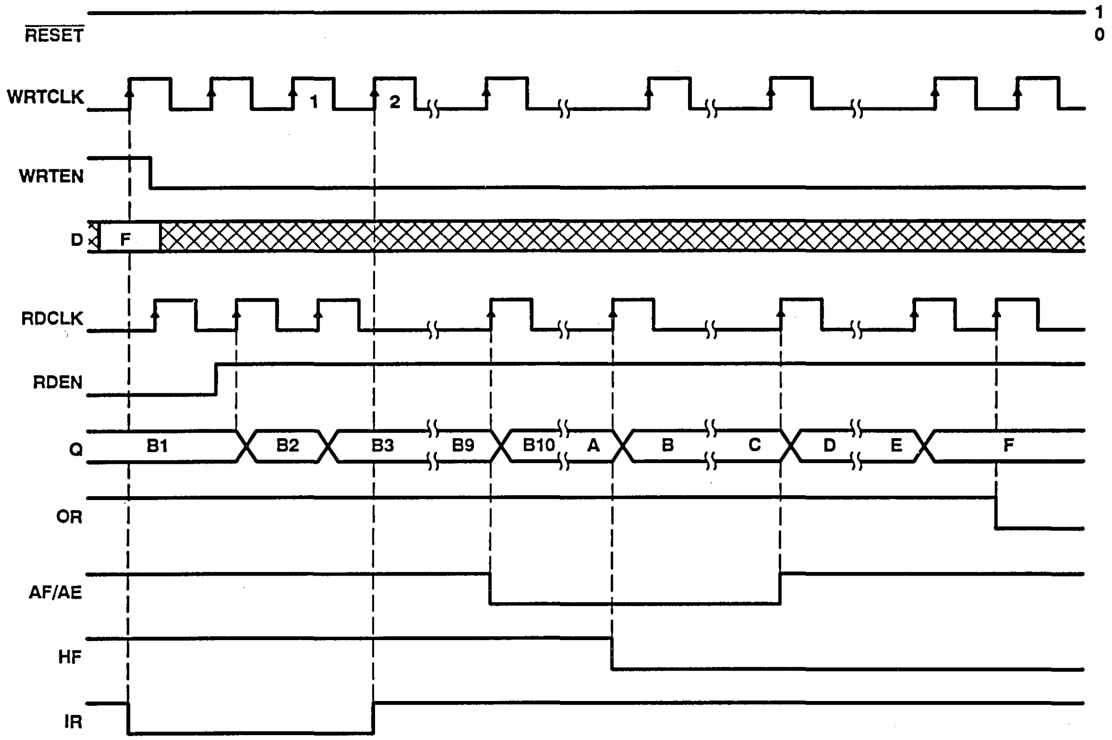
Figure 1. FIFO Reset



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT		
	A	B	C
SN74ACT2226	B33	B57	B65
SN74ACT2228	B129	B249	B257

Figure 2. FIFO Write



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT					
	A	B	C	D	E	F
SN74ACT2226	B33	B34	B56	B57	B64	B65
SN74ACT2228	B129	B130	B248	B249	B256	B257

Figure 3. FIFO Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±200 mA
Operating free-air temperature range, T_A .... −40°C to 85°C
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8	mA
I_{OL}	Low-level output current	Q outputs		16	mA
		Flags		8	
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 through 3)

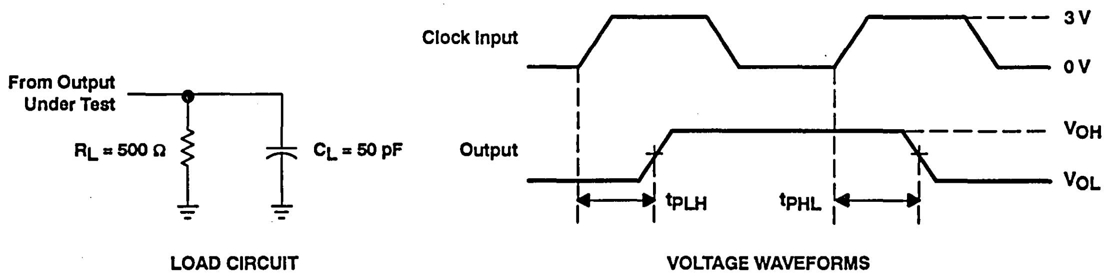
			MIN	MAX	UNIT
f_{clock}	Clock frequency			22	MHz
t_w	Pulse duration	1WRTCLK, 2WRTCLK high or low	15		ns
		1RDCLK, 2RDCLK high or low	15		
t_{su}	Setup time	1D before 1WRTCLK↑ and 2D before 2WRTCLK↑	6		ns
		1WRTEN before 1WRTCLK↑ and 2WRTEN before 2WRTCLK↑	6		
		1RDEN before 1RDCLK↑ and 2RDEN before 2RDCLK↑	6		
		1$\overline{\text{RESET}}$ low before 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low before 2WRTCLK↑§	6		
		1$\overline{\text{RESET}}$ low before 1RDCLK↑ and 2$\overline{\text{RESET}}$ low before 2RDCLK↑§	6		
t_h	Hold time	1D after 1WRTCLK↑ and 2D after 2WRTCLK↑	0		ns
		1WRTEN after 1WRTCLK↑ and 2WRTEN after 2WRTCLK↑	0		
		1RDEN after 1RDCLK↑ and 2RDEN after 2RDCLK↑	0		
		1$\overline{\text{RESET}}$ low after 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low after 2WRTCLK↑§	6		
		1$\overline{\text{RESET}}$ low after 1RDCLK↑ and 2$\overline{\text{RESET}}$ low after 2RDCLK↑§	6		

§ Requirement to count the clock edge as one of at least four needed to reset a FIFO

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK		22		MHz
t_{pd}	1RDCLK↑, 2RDCLK↑	1Q, 2Q	2	20	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1IR, 2IR	1	20	ns
t_{pd}	1RDCLK↑, 2RDCLK↑	1OR, 2OR	1	20	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1AF/AE, 2AF/AE	3	20	ns
	1RDCLK↑, 2RDCLK↑		3	20	
t_{PLH}	1WRTCLK↑, 2WRTCLK↑	1HF, 2HF	2	20	ns
t_{PHL}	1RDCLK↑, 2RDCLK↑		3	20	
t_{PLH}	1$\overline{\text{RESET}}$, 2$\overline{\text{RESET}}$ low	1AF/AE, 2AF/AE	1	20	ns
t_{PHL}		1HF, 2HF	1	20	

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SINGLE FIFO SUPPLY CURRENT
vs
CLOCK FREQUENCY

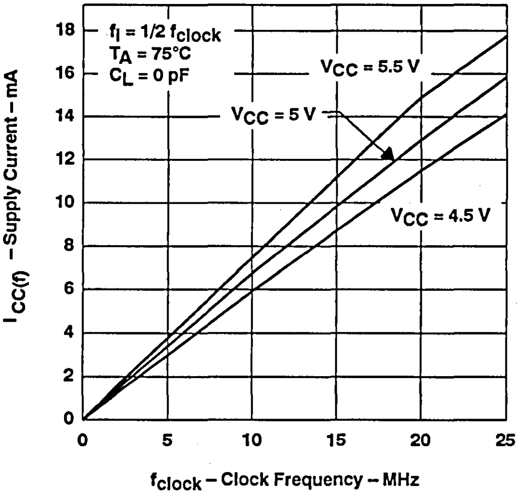


Figure 5

calculating power dissipation

Data for Figure 5 is taken with one FIFO active and one FIFO idle on the device. The active FIFO has both writes and reads enabled with its read clock (RDCLK) and write clock (WRTCLK) operating at the rate specified by f_{clock}. The data input rate and data output rate are half the f_{clock} rate, and the data output is disconnected. A close approximation to the total device power can be found by using Figure 5, determining the capacitive load on the data output and determining the number of SN74ACT2226/2228 inputs driven by TTL high levels.

With $I_{CC(f)}$ taken from Figure 5, the maximum power dissipation (P_T) of one FIFO on the SN74ACT2226 or SN74ACT2228 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + (C_L \times V_{CC}^2 \times f_o)$$

where:

N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

APPLICATION INFORMATION

An example of concentrating two independent serial data signals into a single composite data signal with the use of an SN74ACT2226 or SN74ACT2228 device is shown in Figure 6. The input data to the FIFOs share the same average (mean) frequency, and the mean frequency of the SYS_CLOCK is greater than or equal to the sum of the individual mean input rates. A single-bit FIFO is needed for each additional input data signal that is time-division multiplexed into the composite signal.

The FIFO memories provide a buffer to absorb clock jitter generated by the transmission systems of incoming signals and synchronize the phase-independent inputs to one another. FIFO half-full (HF) flags are used to signal the multiplexer to start fetching data from the buffers. The state of the flags can also be used to indicate when a FIFO read should be suppressed to regulate the output flow (pulse-stuffing control). The FIFO almost-full/almost-empty flags (AF/AE) can be used in place of the half-full flags to reduce transmission delay.

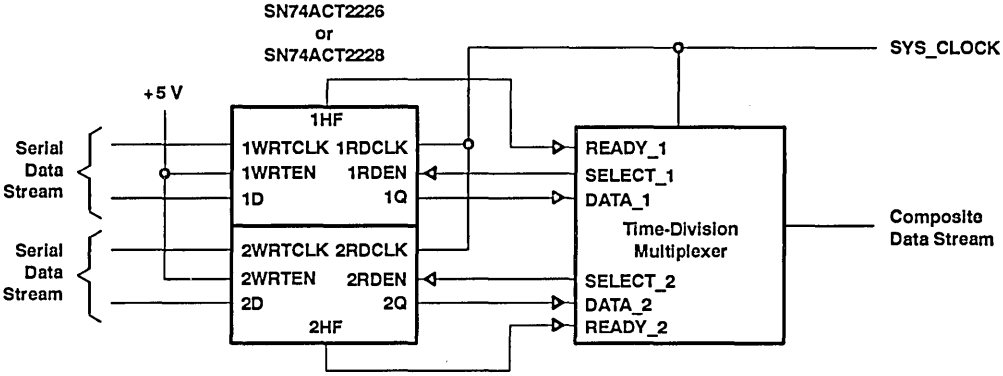


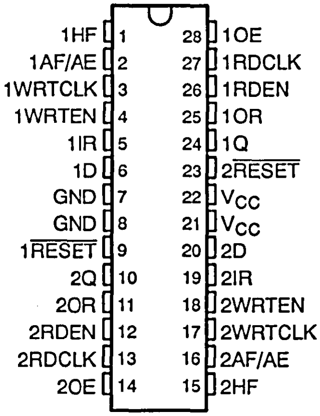
Figure 6. Time-Division Multiplexing Using the SN74ACT2226 or SN74ACT2228

SN74ACT2227, SN74ACT2229
DUAL 64 × 1 AND DUAL 256 × 1
FIRST-IN, FIRST-OUT MEMORIES

SCAS220A – JUNE 1992 – REVISED AUGUST 1993

- **Dual Independent FIFOs Organized as:**
  - **64 Words by 1 Bit Each – SN74ACT2227**
  - **256 Words by 1 Bit Each – SN74ACT2229**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident on Each FIFO**
- **Input-Ready Flags Synchronized to Write Clocks**
- **Output-Ready Flags Synchronized to Read Clocks**
- **Half-Full and Almost-Full/Almost-Empty Flags**
- **Characterized for Operation Over the Industrial Temperature Range (–40°C to 85°C)**
- **Support Clock Frequencies up to 60 MHz**
- **Access Times of 9 ns**
- **3-State Data Outputs**
- **Low-Power Advanced CMOS Technology**
- **Available in 28-Pin SOIC (DW) Package**

DW PACKAGE
(TOP VIEW)



description

The SN74ACT2227 and SN74ACT2229 are dual FIFOs suited for a wide range of serial data buffering applications including elastic stores for frequencies up to OC-1 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2227) or 256 × 1 (SN74ACT2229) and has control signals and status flags for independent operation. Output flags per FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write-enable (1WRTEN or 2WRTEN) input and input-ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read-clock (1RDCLK or 2RDCLK) input when the read-enable (1RDEN or 2RDEN) input and output-ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO can be asynchronous to one another. A FIFO data output (1Q or 2Q) is in the high-impedance state when its output-enable (1OE or 2OE) input is low.

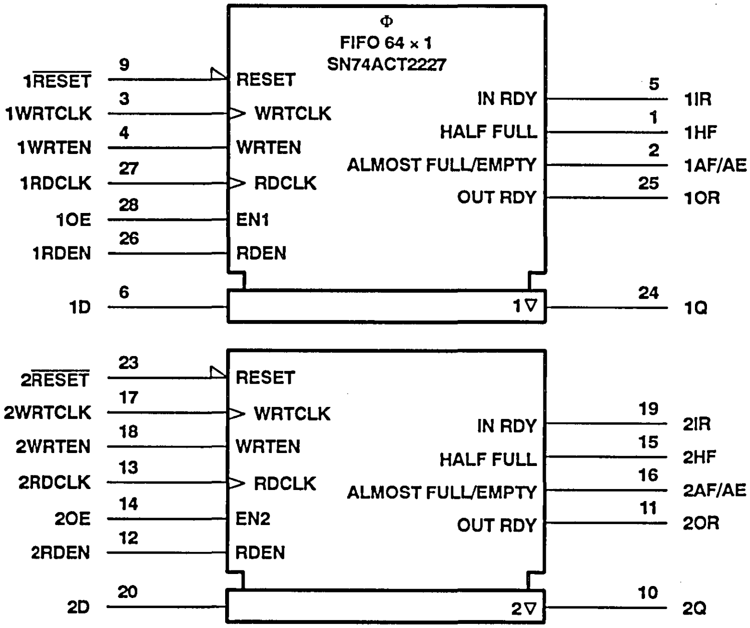
Each input-ready flag (1IR or 2IR) is synchronized by two flip-flop stages to its write clock (1WRTCLK or 2WRTCLK), and each output-ready flag (1OR or 2OR) is synchronized by three flip-flop stages to its read clock (1RDCLK or 2RDCLK). This multistage synchronization ensures reliable flag-output states when data is written and read asynchronously.

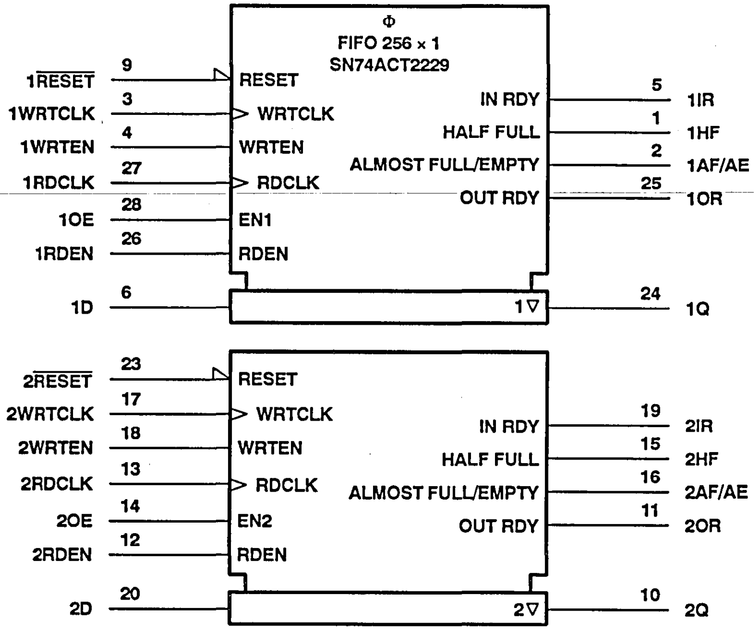
A half-full flag (1HF or 2HF) is high when the number of bits stored in its FIFO is greater than or equal to half the depth of the FIFO. An almost-full/almost-empty flag (1AF/AE or 2AF/AE) is high when eight or less bits are stored in its FIFO and when eight or fewer empty locations are left in the FIFO. A bit present on the data output is not stored in the FIFO.

The SN74ACT2227 and SN74ACT2229 are characterized for operation from –40°C to 85°C.

TEXAS INSTRUMENTS

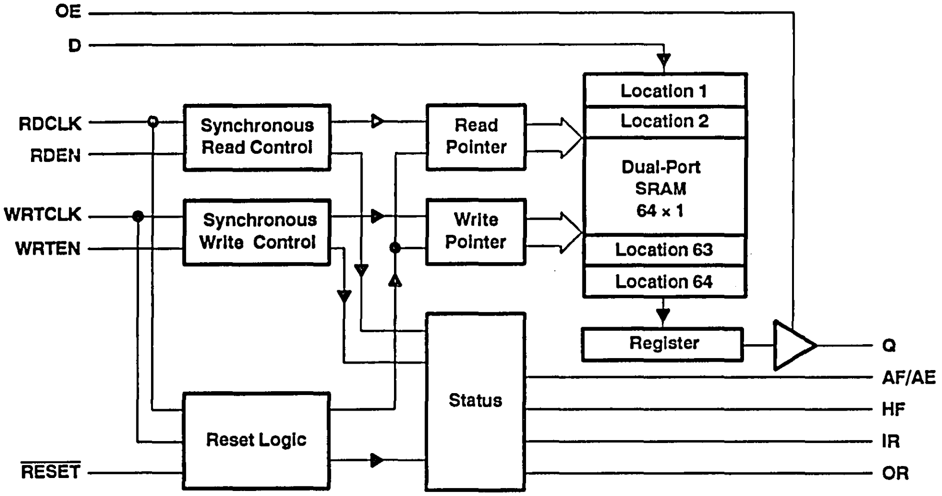
logic symbols†



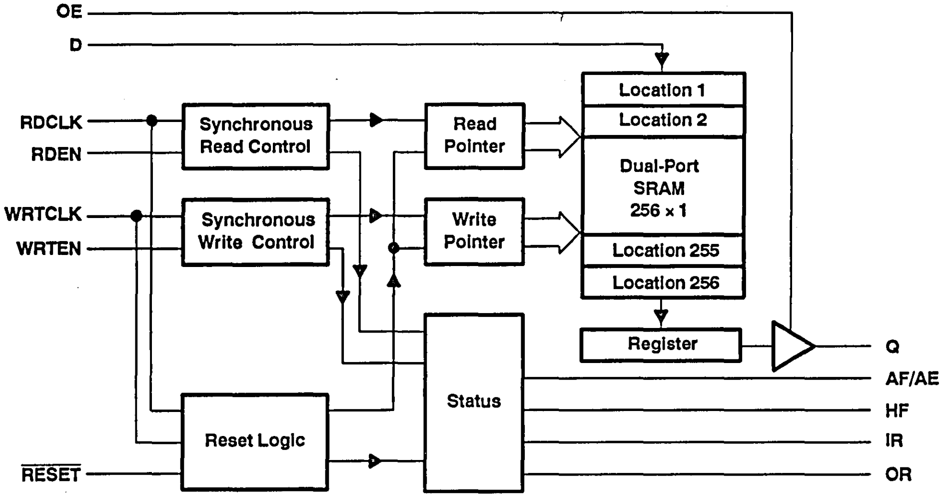


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ACT2227 functional block diagram (each FIFO)



SN74ACT2229 functional block diagram (each FIFO)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1AF/AE 2AF/AE	2 16	O	Almost-full/almost-empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset.
1D 2D	6 20	I	Data input
GND	7, 8		Ground
1HF 2HF	1 15	O	Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset.
1IR 2IR	5 19	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset.
1OE 2OE	28 14	I	Output enable. The data output of a FIFO is active when OE is high and in the high-impedance state when OE is low.
1OR 2OR	25 11	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
1Q 2Q	24 10	O	Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is asserted high to indicate ready data.
1RDCLK 2RDCLK	27 13	I	Read clock. RDCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK.
1RDEN 2RDEN	26 12	I	Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK.
1$\overline{\text{RESET}}$ 2$\overline{\text{RESET}}$	9 23	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. Before it is used, a FIFO must be reset after power up.
V_{CC}	21, 22		Supply voltage
1WRTCLK 2WRTCLK	3 17	I	Write clock. WRTCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK.
1WRTEN 2WRTEN	4 18	I	Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

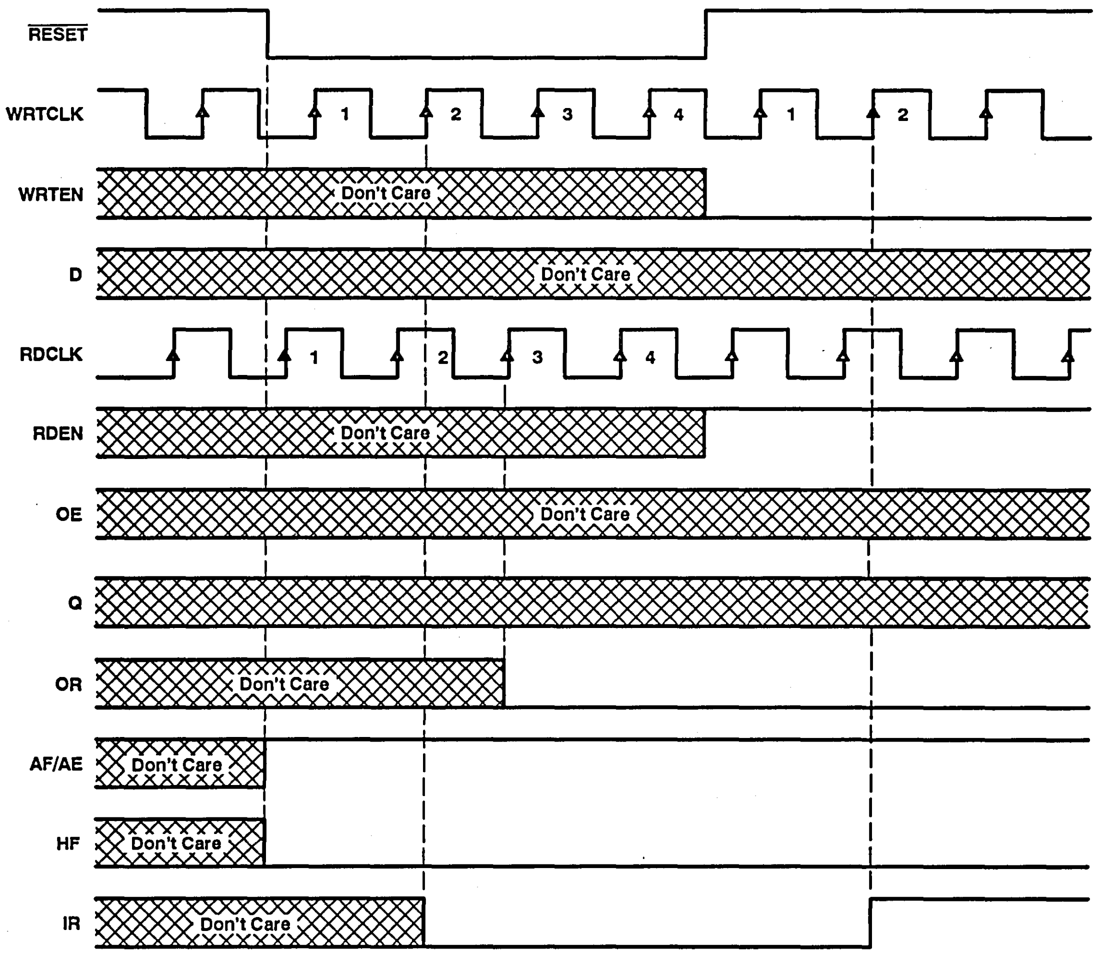
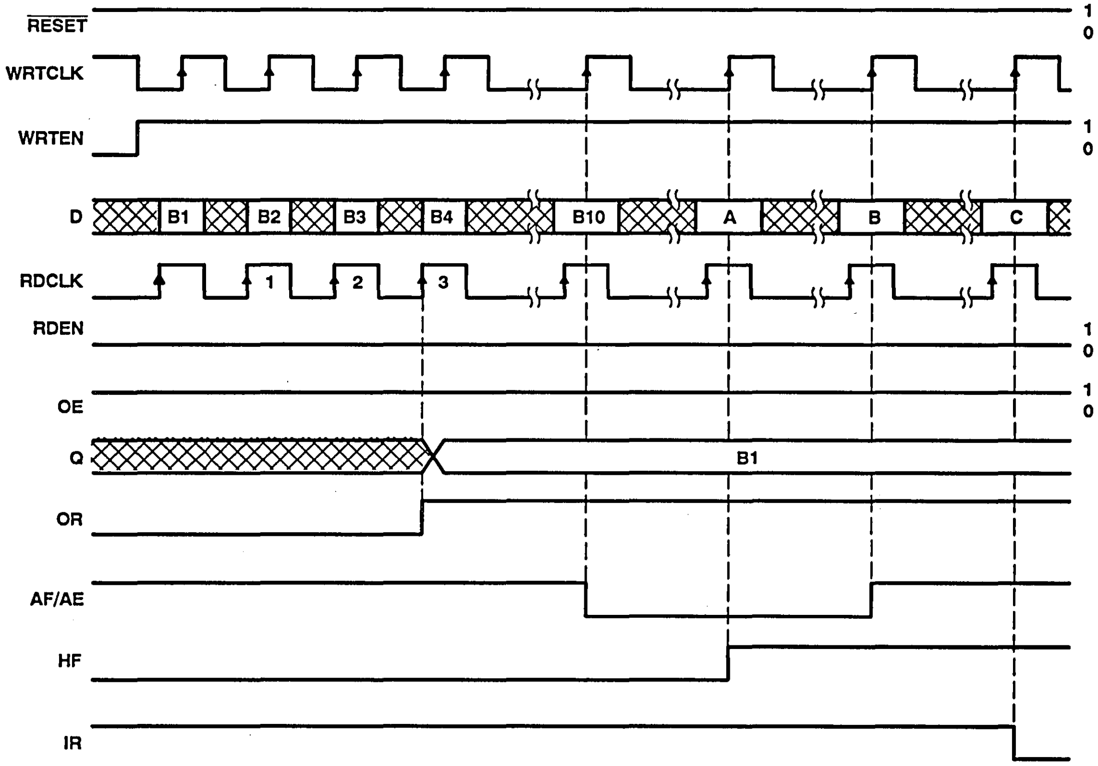


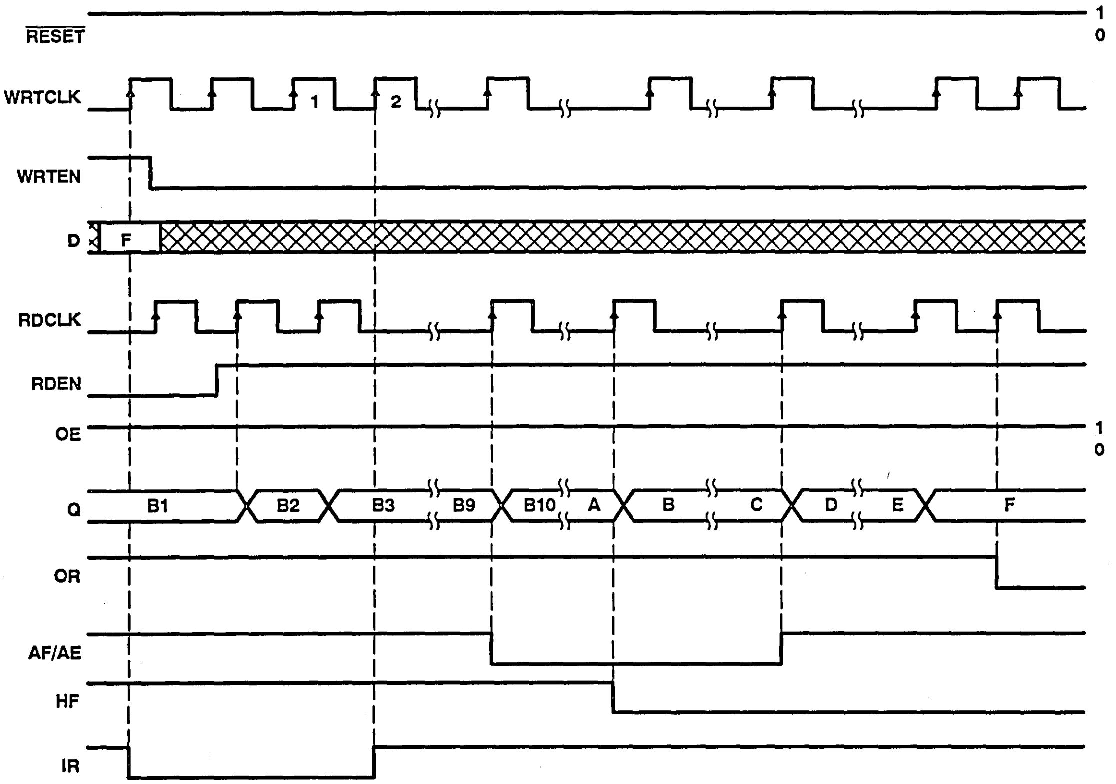
Figure 1. FIFO Reset



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT		
	A	B	C
SN74ACT2227	B33	B57	B65
SN74ACT2229	B129	B249	B257

Figure 2. FIFO Write



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT					
	A	B	C	D	E	F
SN74ACT2227	B33	B34	B56	B57	B64	B65
SN74ACT2229	B129	B130	B248	B249	B256	B257

Figure 3. FIFO Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Voltage applied to a disabled 3-state output	5.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q outputs, Flags		–8	mA
I_{OL}	Low-level output current	Q outputs		16	mA
		Flags		8	
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0				±5	µA
I_{CC}		$V_I = V_{CC}$ – 0.2 V or 0					400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 through 3)

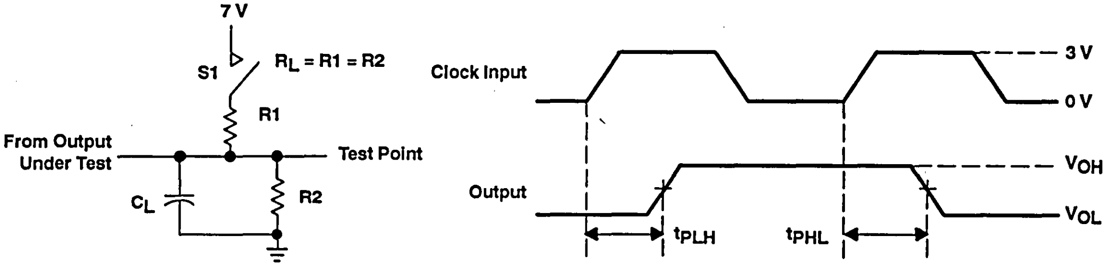
			MIN	MAX	UNIT
f_{clock}	Clock frequency			60	MHz
t_w	Pulse duration	1WRTCLK, 2WRTCLK high or low	5		ns
		1RDCLK, 2RDCLK high or low	5		
t_{su}	Setup time	1D before 1WRTCLK↑ and 2D before 2WRTCLK↑	4.5		ns
		1WRTEN before 1WRTCLK↑ and 2WRTEN before 2WRTCLK↑	4.5		
		1RDEN before 1RDCLK↑ and 2RDEN before 2RDCLK↑	4		
		1$\overline{\text{RESET}}$ low before 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low before 2WRTCLK↑†	6		
		1$\overline{\text{RESET}}$ low before 1RDCLK↑ and 2$\overline{\text{RESET}}$ low before 2RDCLK↑†	6		
t_h	Hold time	1D after 1WRTCLK↑ and 2D after 2WRTCLK↑	0		ns
		1WRTEN after 1WRTCLK↑ and 2WRTEN after 2WRTCLK↑	0		
		1RDEN after 1RDCLK↑ and 2RDEN after 2RDCLK↑	0		
		1$\overline{\text{RESET}}$ low after 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low after 2WRTCLK↑†	6		
		1$\overline{\text{RESET}}$ low after 1RDCLK↑ and 2$\overline{\text{RESET}}$ low after 2RDCLK↑†	6		

† Requirement to count the clock edge as one of at least four needed to reset a FIFO

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

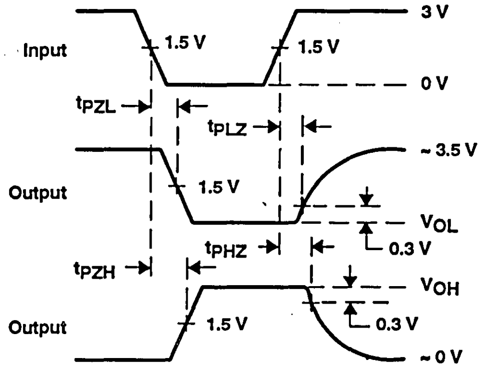
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK		60		MHz
t_{pd}	1RDCLK↑, 2RDCLK↑	1Q, 2Q	2	9	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1IR, 2IR	1	8	ns
t_{pd}	1RDCLK↑, 2RDCLK↑	1OR, 2OR	1	8	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1AF/AE, 2AF/AE	3	14	ns
	1RDCLK↑, 2RDCLK↑		3	14	
t_{PLH}	1WRTCLK↑, 2WRTCLK↑	1HF, 2HF	2	12	ns
t_{PHL}	1RDCLK↑, 2RDCLK↑		3	14	
t_{PLH}	1$\overline{\text{RESET}}$, 2$\overline{\text{RESET}}$ low	1AF/AE, 2AF/AE	1	17	ns
t_{PHL}		1HF, 2HF	1	18	
t_{en}	1OE, 2OE	1Q, 2Q	0	8	ns
t_{dis}			0	8	

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

**SINGLE FIFO SUPPLY CURRENT
vs
CLOCK FREQUENCY**

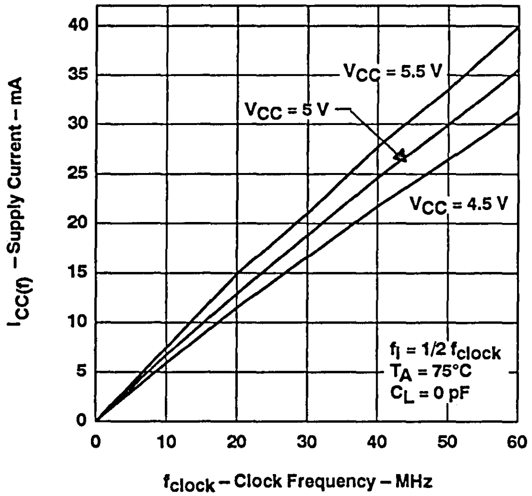


Figure 5

calculating power dissipation

Data for Figure 5 is taken with one FIFO active and one FIFO idle on the device. The active FIFO has both writes and reads enabled with its read clock (RDCLK) and write clock (WRTCLK) operating at the rate specified by f_{clock}. The data input rate and data output rate are half the f_{clock} rate, and the data output is disconnected. A close approximation to the total device power can be found by Figure 5, determining the capacitive load on the data output, and determining the number of SN74ACT2227/2229 inputs driven by TTL high levels.

With $I_{CC(f)}$ taken from Figure 5, the maximum power dissipation (P_T) of one FIFO on the SN74ACT2227 or SN74ACT2229 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + (C_L \times V_{CC}^2 \times f_o)$$

where:

N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

APPLICATION INFORMATION

An example of concentrating two independent serial data signals into a single composite data signal with the use of an SN74ACT2227 or SN74ACT2229 device is shown in Figure 6. The input data to the FIFOs share the same average (mean) frequency, and the mean frequency of the SYS_CLOCK is greater than or equal to the sum of the individual mean input rates. A single-bit FIFO is needed for each additional input data signal that is time-division multiplexed into the composite signal.

The FIFO memories provide a buffer to absorb clock jitter generated by the transmission systems of incoming signals and synchronize the phase-independent inputs to one another. FIFO half-full (HF) flags are used to signal the multiplexer to start fetching data from the buffers. The state of the flags can also be used to indicate when a FIFO read should be suppressed to regulate the output flow (pulse-stuffing control). The FIFO almost-full/almost-empty flags (AF/AE) can be used in place of the half-full flags to reduce transmission delay.

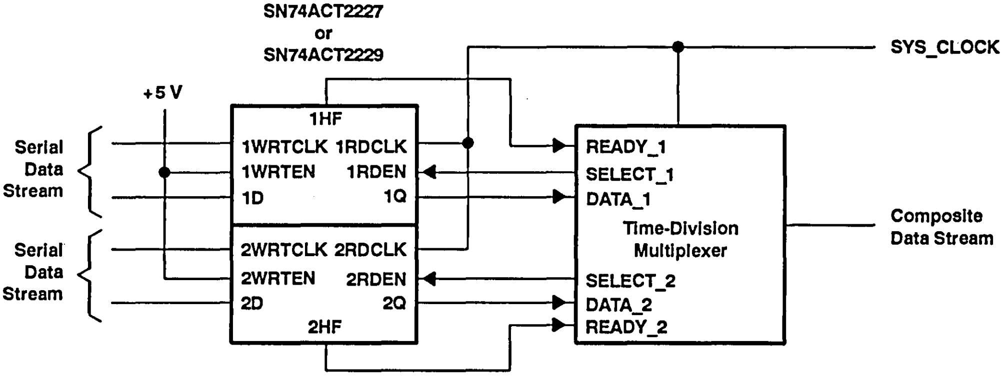


Figure 6. Time-Division Multiplexing Using the SN74ACT2227 or SN74ACT2229

DSP 36-BIT CLOCKED FIFOS

Features	Benefits
• 36-bit FIFO interface	• Single-chip implementation for high levels of intergration
• Bidirectional 32-bit and 36-bit options	• Two dual-port SRAMs allow true bidirectional capability.
• Depths from 256 to 2K words	• Multiple depths to optimize system storage applications
• Mailbox-register bypass	• Quick access to priority information
• Microprocessor-control circuitry	• Interface matches most processors and DSP bus-cycle timing and communications
• Synchronous retransmit option	• Permits user-defined retransmission point
• Multiple default values for separate AF and AE flags	• Easy alternatives for flag settings
• Parallel and serial flag programming options	• Choice of status-flag programming modes
• EIAJ standard 120-pin thin quad flat package (TQFP)	• 67% less board space than equivalent 132-pin PQFPs; over 66% less board space than four 9-bit 32-pin PLCC equivalents
• TI has established alternate source options	• Standardization that comes from a common second source

The following table lists military FIFO Widebus+™ devices currently targeted for market introduction. Customers interested in learning more about TI's plans for these devices should contact military Advanced System Logic marketing at (915) 561-7289.

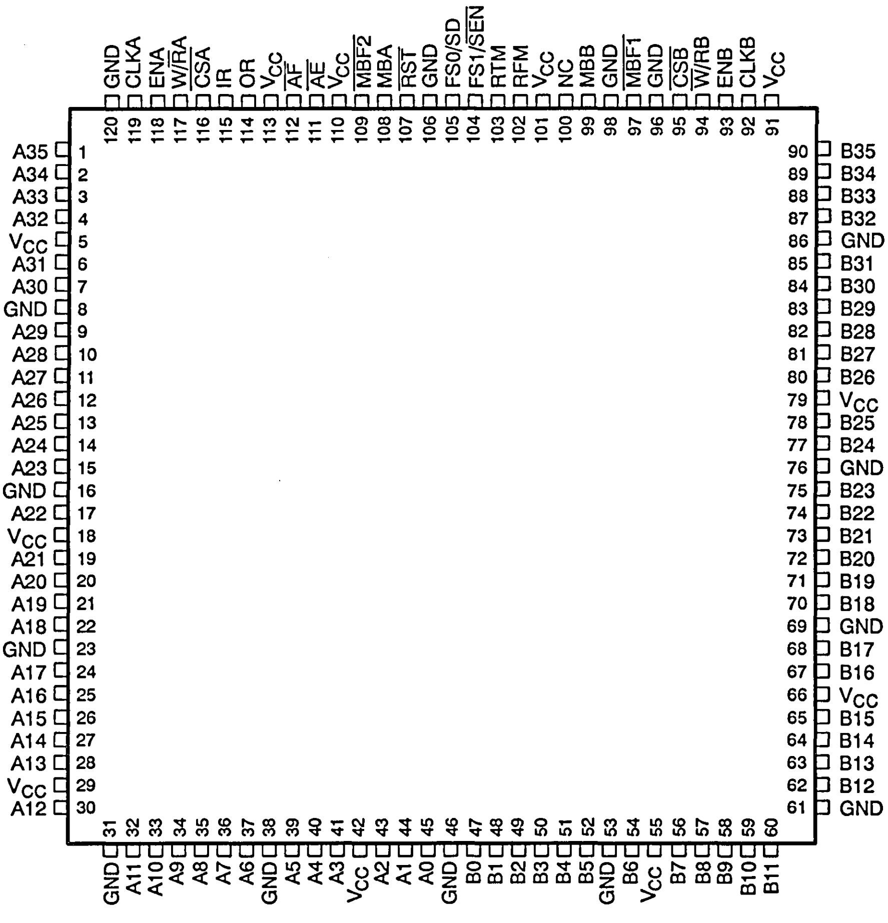
DEVICE	PACKAGE	DESCRIPTION
SNJ54ACT3641-XX	120 CQFP	1K × 36-Bit Unidirectional Clocked FIFO

SN74ACT3631
512 × 36 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS246B – AUGUST 1993 – REVISED JUNE 1994

- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Clocked FIFO Buffering Data From Port A to Port B
- Synchronous Read Retransmit Capability
- Mailbox Register in Each Direction
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- Input-Ready (IR) and Almost-Full ($\overline{AF}$) Flags Synchronized by CLKA
- Output-Ready (OR) and Almost-Empty ($\overline{AE}$) Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Pin-to-Pin Compatible With the SN74ACT3641, and SN74ACT3651
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)

PCB PACKAGE
(TOP VIEW)



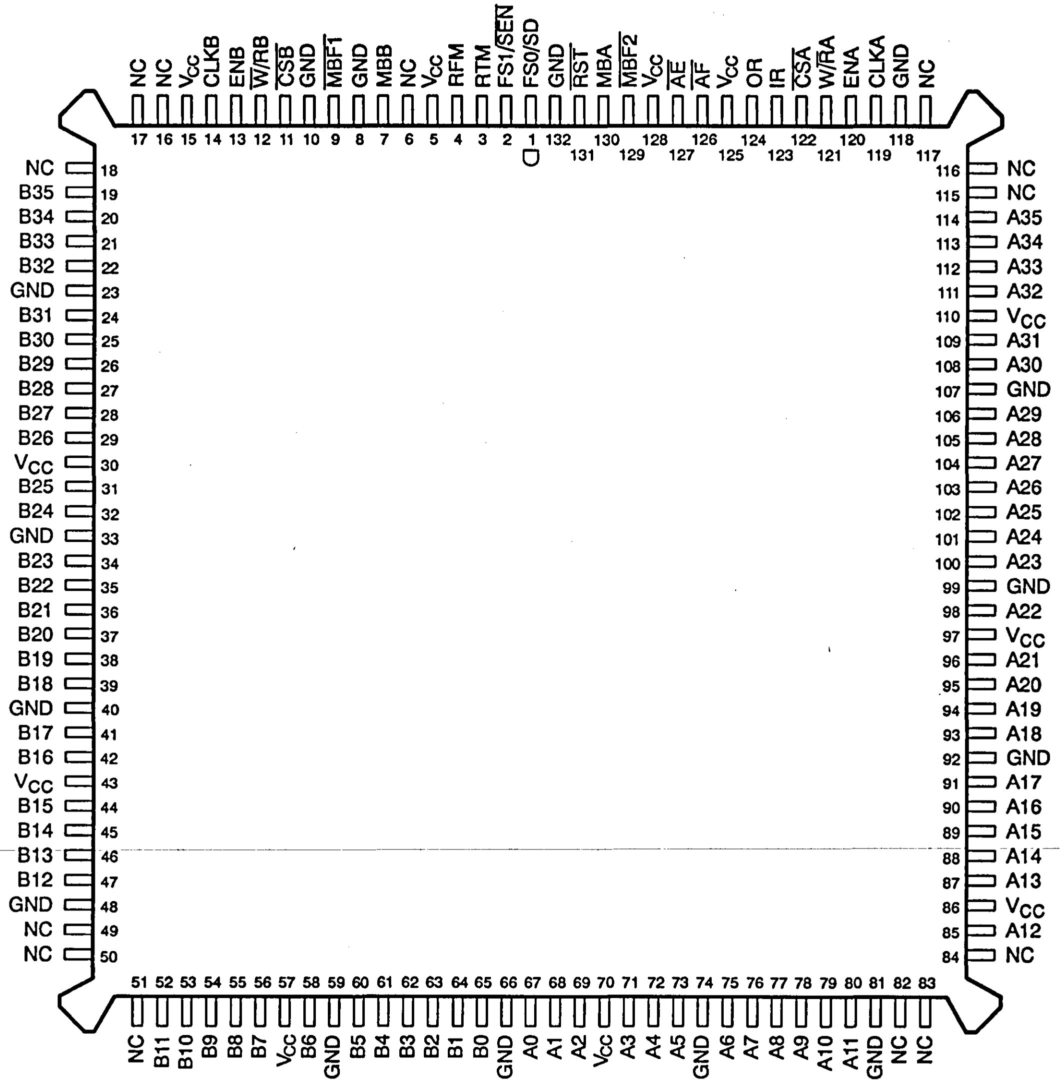
NC – No internal connection

PRODUCT PREVIEW

TEXAS INSTRUMENTS

PRODUCT PREVIEW

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

description

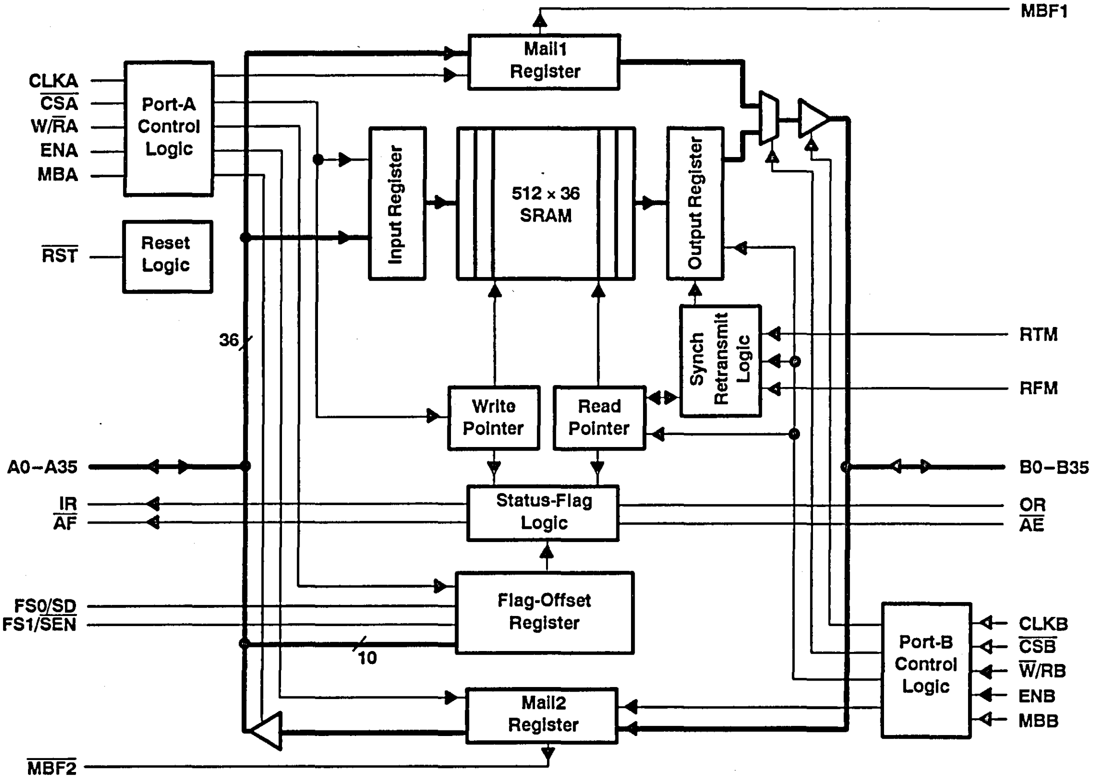
The SN74ACT3631 is a high-speed, low-power, CMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. The 512 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths. Expansion is also possible in word depth.

The SN74ACT3631 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

The input-ready (IR) flag and almost-full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The output-ready (OR) flag and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the almost-full and almost-empty flags of the FIFO can be programmed from port A or through a serial input.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AE}}$	O	Almost-empty flag. Programmable flag synchronized to CLKB. $\overline{\text{AE}}$ is low when the number of words in the FIFO is less than or equal to the value in the almost-empty offset register (X).
$\overline{\text{AF}}$	O	Almost-full flag. Programmable flag synchronized to CLKA. $\overline{\text{AF}}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the almost-full offset register (Y).
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IR and $\overline{\text{AF}}$ are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. OR and $\overline{\text{AE}}$ are synchronous to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1/$\overline{\text{SEN}}$, FS0/SD	I	Flag offset select 1/serial enable, flag offset select 0/serial data. FS1/$\overline{\text{SEN}}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During a device reset, FS1/$\overline{\text{SEN}}$ and FS0/SD select the flag offset programming method. Three offset register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load When serial load is selected for flag offset register programming, FS1/$\overline{\text{SEN}}$ is used as an enable synchronous to the low-to-high transition of CLKA. When FS1/$\overline{\text{SEN}}$ is low, a rising edge on CLKA loads the bit present on FS0/SD into the X and Y offset registers. The number of bit writes required to program the offset register is 18. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of CLKA. When IR is low, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set low during reset and is set high after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high by a reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is set high by a reset.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of CLKB. When OR is low, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is high. OR is forced low during the reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
RFM	I	Read from mark. When the FIFO is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of FS0 and FS1 for $\overline{\text{AF}}$ and $\overline{\text{AE}}$ offset selection.
RTM	I	Retransmit mode. When RTM is high and valid data is present in the FIFO output register (OR is high), a low-to-high transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, taking the FIFO out of retransmit mode.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
W/$\overline{RA}$	I	Port-A write/read select. A high on W/$\overline{RA}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high.
$\overline{W}$/RB	I	Port-B write/read select. A low on $\overline{W}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low.

detailed description

reset

The SN74ACT3631 is reset by taking the reset ($\overline{RST}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the input-ready (IR) flag low, the output-ready (OR) flag high, the almost-empty ($\overline{AE}$) flag low, and the almost-full ($\overline{AF}$) flag high. Resetting the device also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. After a FIFO is reset, its input-ready flag is set high after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

almost-empty flag and almost-full flag offset programming

Two registers in the SN74ACT3631 are used to hold the offset values for the almost-empty and almost-full flags. The almost-empty ($\overline{AE}$) flag offset register is labeled X, and the almost-full ($\overline{AF}$) flag offset register is labeled Y. The offset registers can be loaded with a value in three ways: one of two preset values are loaded into the offset registers, parallel load from port A, or serial load. The offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a low-to-high transition on the $\overline{RST}$ input (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{RST}$	X AND Y REGISTERS†
H	H	↑	Serial load
H	L	↑	64
L	H	↑	8
L	L	↑	Parallel load from port A

† X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.

preset values

If a preset value of 8 or 64 is chosen by the FS1 and FS0 inputs at the time of a $\overline{RST}$ low-to-high transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set high after two low-to-high transitions on CLKA.

parallel load from port A

To program the X and Y registers from port A, the device is reset with FS0 and FS1 low during the low-to-high transition of $\overline{RST}$. After this reset is complete, the IR flag is set high after two low-to-high transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the offset registers in the order Y, X. Each offset register of the SN74ACT3631 uses port-A inputs (A8–A0). The highest number input is used as the most significant bit of the binary number in each case. Each register value can be programmed from 1 to 508. After both offset registers are programmed from port A, subsequent FIFO writes store data in the SRAM.

PRODUCT PREVIEW

serial load

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/SEN high during the low-to-high transition of RST. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each low-to-high transition of CLKA that the FS1/SEN input is low. Eighteen-bit writes are needed to complete the programming. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the X register. Each register value can be programmed from 1 to 508.

When the option to program the offset registers serially is chosen, the input-ready (IR) flag remains low until all register bits are written. The IR flag is set high by the low-to-high transition of CLKA after the last bit is loaded to allow normal FIFO operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select (CSA) and the port-A write/read select (W/RA). The A0–A35 outputs are in the high-impedance state when either CSA or W/RA is high. The A0–A35 outputs are active when both CSA and W/RA are low.

Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when CSA and the port-A mailbox select (MBA) are low, W/RA, the port-A enable (ENA), and the input-ready (IR) flag are high (see Table 2). Writes to the FIFO are independent of any concurrent FIFO reads.

Table 2. Port-A Enable Function Table

CSA	W/RA	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set MBF2 high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select (W/RB) is the inverse of the port-A write/read select (W/RA). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select (CSB) and the port-B write/read select (W/RB). The B0–B35 outputs are in the high-impedance state when either CSB is high or W/RB is low. The B0–B35 outputs are active when CSB is low and W/RB is high.

Data is read from the FIFO to its output register on a low-to-high transition of CLKB when CSB and the port-B mailbox select (MBB) are low, W/RB, the port-B enable (ENB), and the output-ready (OR) flag are high (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	None
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO output register	None
L	H	H	L	↑	Active, FIFO output register	FIFO read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup- and hold-time window of the cycle.

When the output-ready (OR) flag is low, the next data word is sent to the FIFO output register automatically by the CLKB low-to-high transition that sets the output-ready flag high. When OR is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B chip select ($\overline{CSB}$), write/read select ($\overline{W}$/RB), enable (ENB), and mailbox select (MBB).

synchronized FIFO flags

Each SN74ACT3631 FIFO flag is synchronized to its port clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). OR and $\overline{AE}$ are synchronized to CLKB. IR and $\overline{AF}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN FIFO†‡	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	OR	$\overline{AE}$	$\overline{AF}$	IR
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [512 – (Y + 1)]	H	H	H	H
(512 – Y) to 511	H	H	L	H
512	H	H	L	L

† X is the almost-empty offset for $\overline{AE}$. Y is the almost-full offset for $\overline{AF}$.
‡ When a word is present in the FIFO output register, its previous memory location is free.

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output-ready flag (OR)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of CLKB occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time $t_{sk(1)}$ or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

input-ready flag (IR)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). When the input-ready flag is high, a memory location is free in the SRAM to write new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA; therefore, an input-ready flag is low if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets the input-ready flag high, and data can be written in the following cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time $t_{sk(1)}$ or greater after the read. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

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almost-empty flag ($\overline{AE}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-empty flag is low when the FIFO contains X or less words and is high when the FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of CLKB have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 8).

almost-full flag ($\overline{AF}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-full flag is low when the number of words in the FIFO is greater than or equal to (512 – Y). The almost-full flag is high when the number of words in the FIFO is less than or equal to [512 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKA are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [512 – (Y + 1)] or less words remains low if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [512 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of words in memory to [512 – (Y + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the read that reduces the number of words in memory to [512 – (Y + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 9).

synchronous retransmit

The synchronous retransmit feature of the SN74ACT3631 allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent on-going FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a low-to-high transition on CLKB when the retransmit mode (RTM) input is high and OR is high. This rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a low-to-high transition occurs while RTM is low.

When two or more reads have been done past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be low during the CLKB rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{\text{AE}}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{\text{AF}}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{\text{AF}}$ is set low by the write that stores (512 – Y) words after the first retransmit word. The IR flag is set low by the 512th write after the first retransmit word.

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synchronous retransmit (continued)

When the FIFO is in retransmit mode and RFM is high, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflects the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{\text{AE}}$ high (see Figure 11). The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{\text{AF}}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{\text{AF}}$ should cause one or both flags to transition high, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time $t_{sk(1)}$ or greater after the rising CLKB edge (see Figure 12). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{\text{AF}}$ if it occurs at time $t_{sk(2)}$ or greater after the rising CLKB edge (see Figure 14).

mailbox registers

Two 36-bit bypass registers are on the SN74ACT3631/3651 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

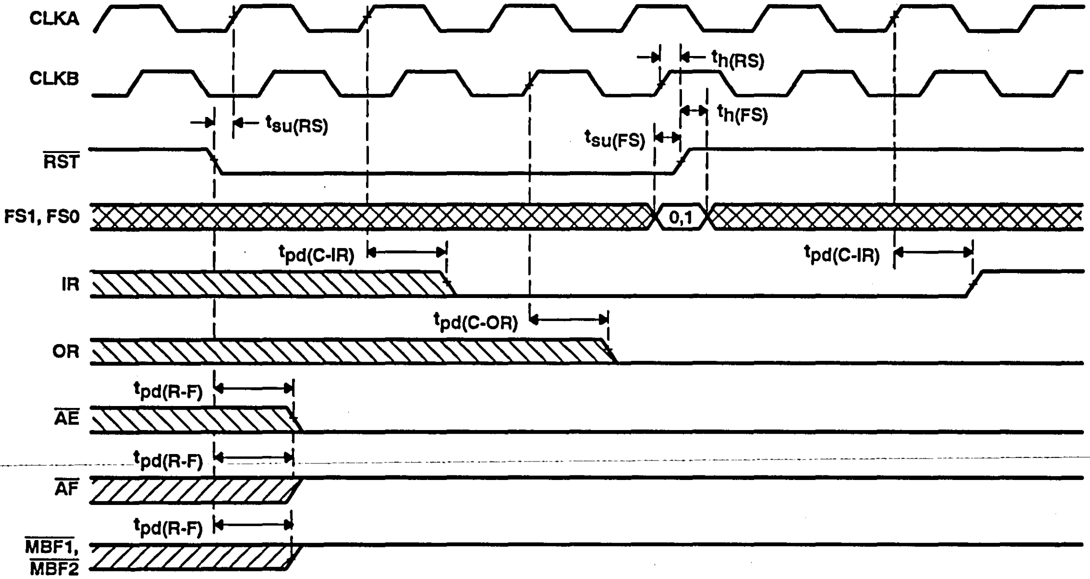

Figure 1. FIFO Reset Loading X and Y With a Preset Value of Eight

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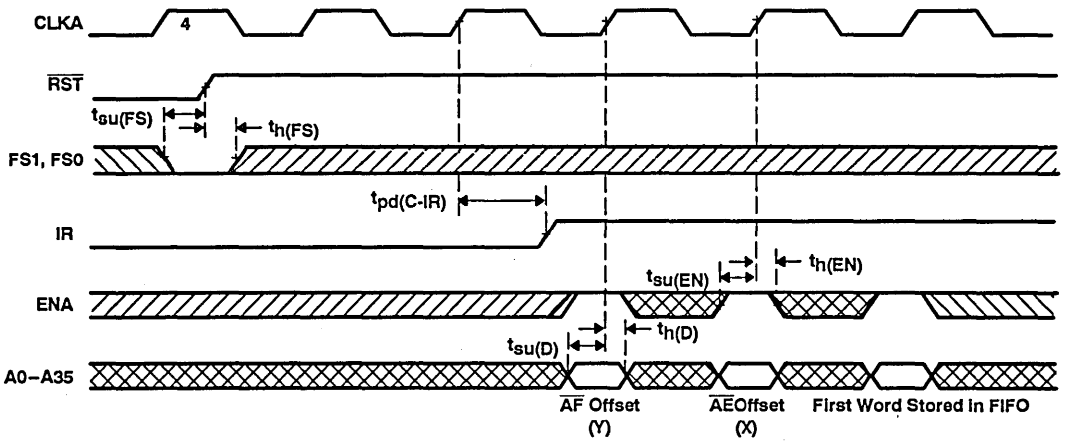
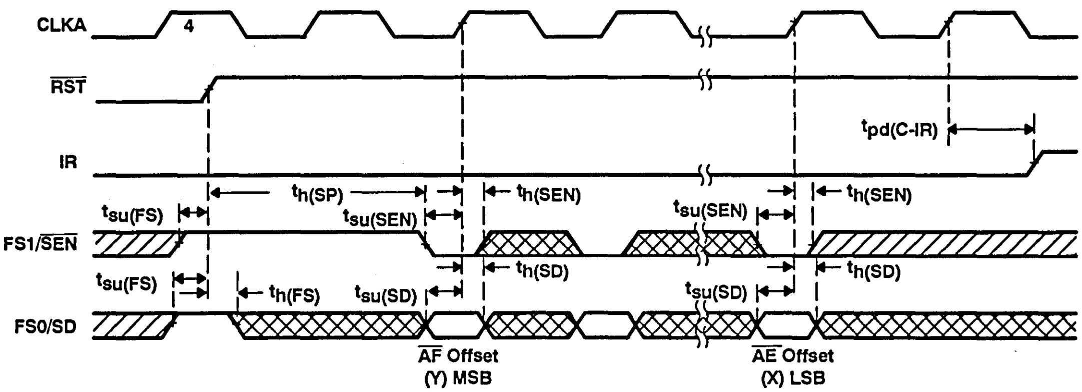


NOTE: CSA = L, W/RA = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values From Port A



NOTE: It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set high.

Figure 3. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values Serially

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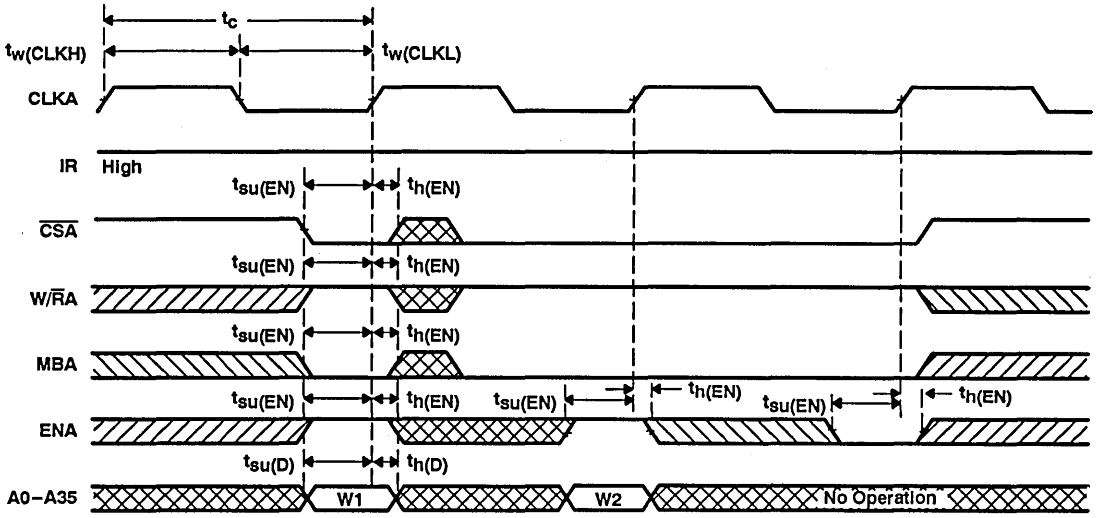


Figure 4. FIFO Write-Cycle Timing

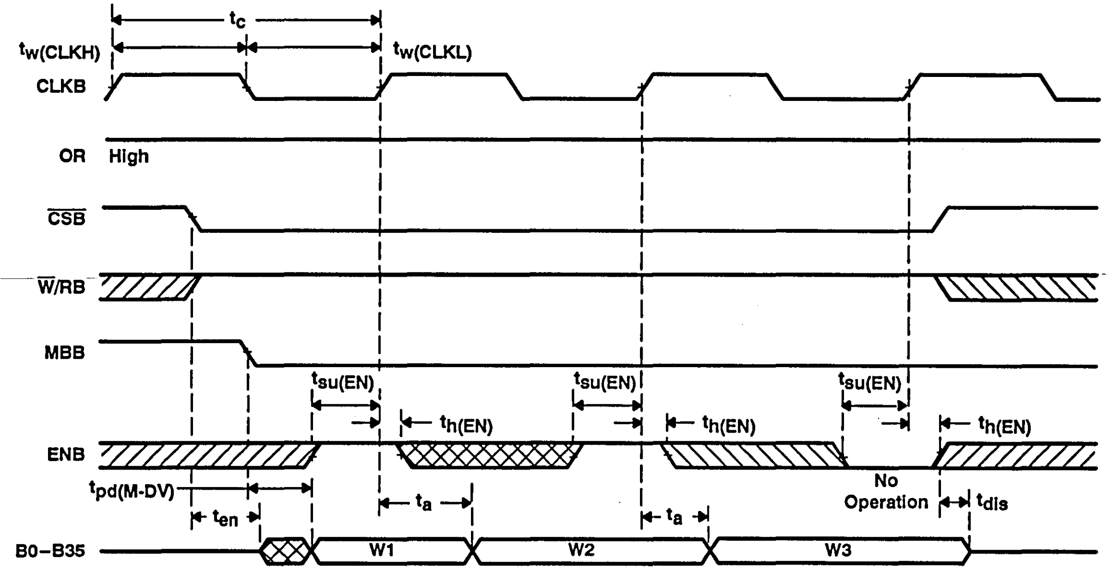
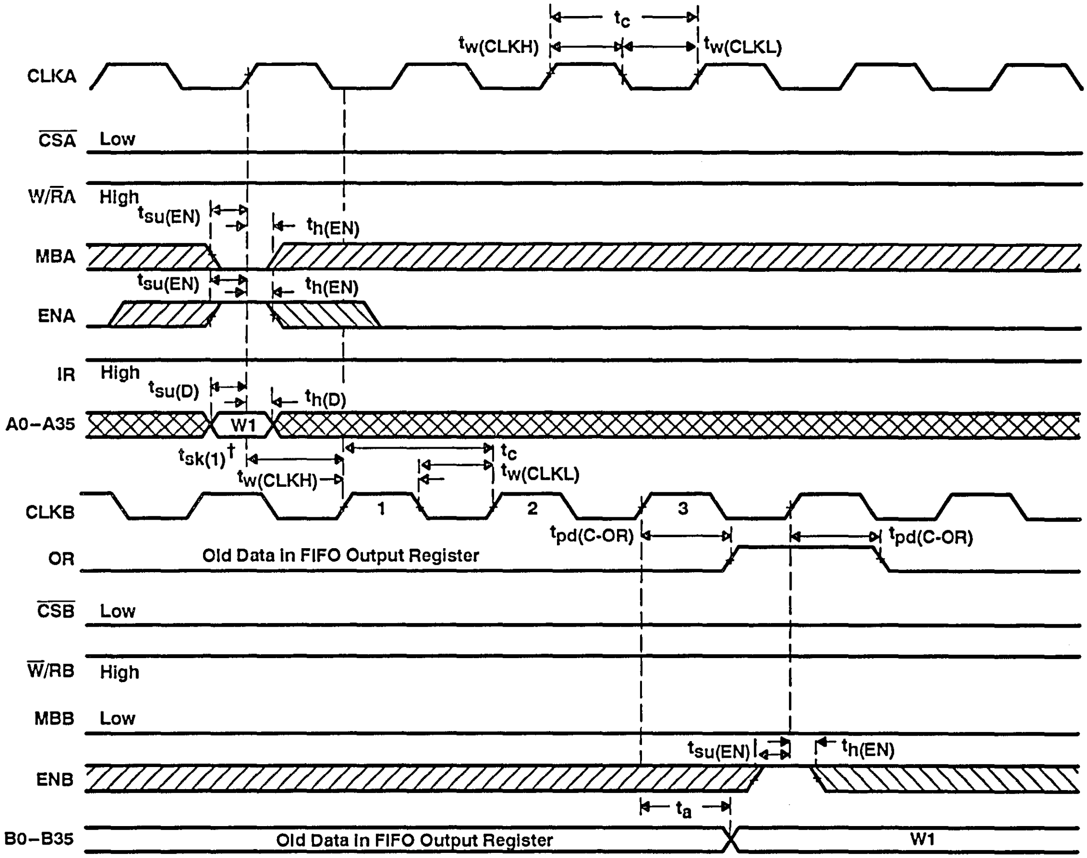
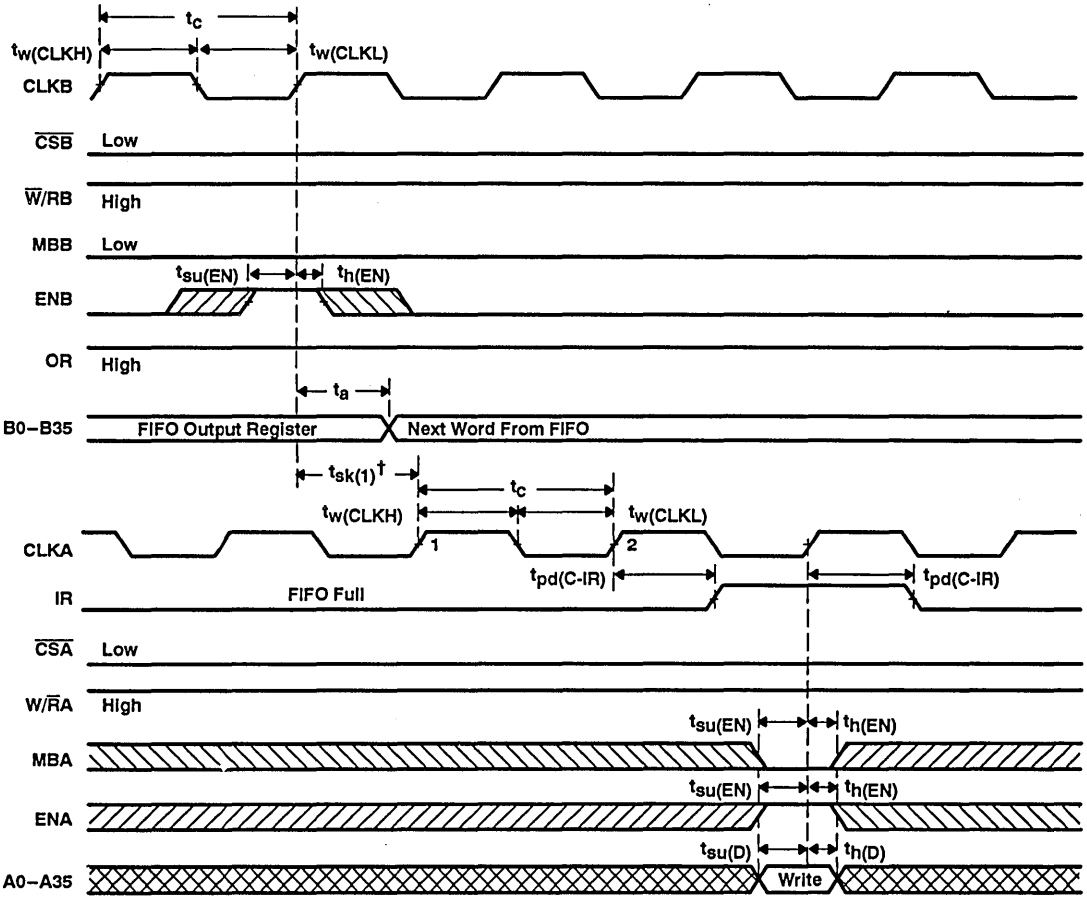


Figure 5. FIFO Read-Cycle Timing



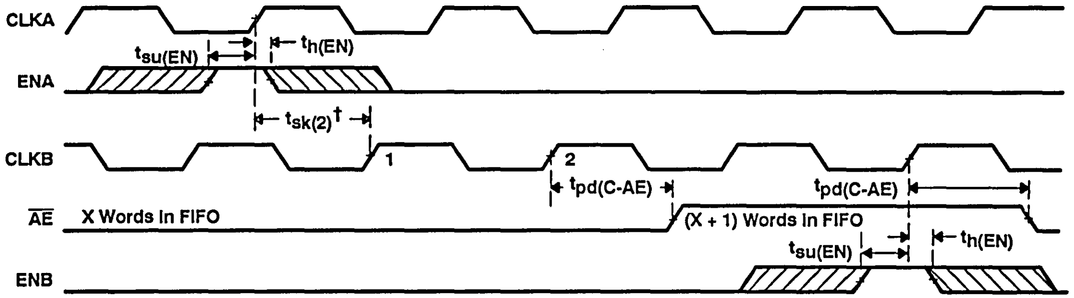
† $t_{sk(1)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition high and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(1)}$, then the transition of OR high and the first word load to the output register can occur one CLKB cycle later than shown.

Figure 6. OR-Flag Timing and First Data Word Fallthrough When the FIFO Is Empty



[†] $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, then IR can transition high one CLKA cycle later than shown.

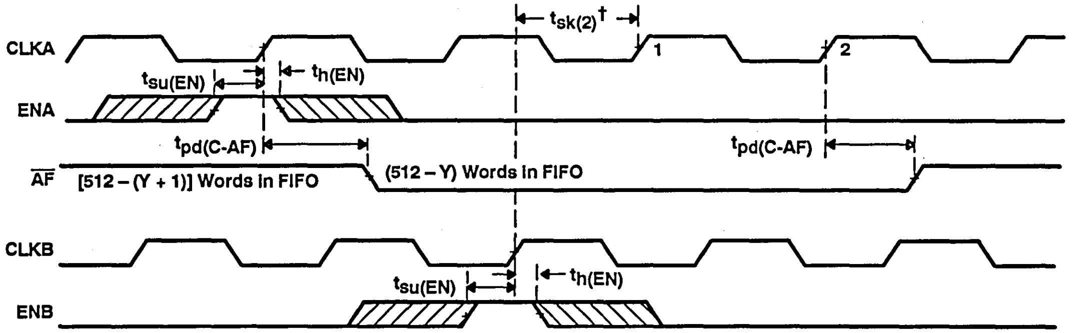
Figure 7. IR-Flag Timing and First Available Write When the FIFO Is Full



NOTE: FIFO write ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = H, MBA = L), FIFO read ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = H, MBB = L)

† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{\text{AE}}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(2)}$, then $\overline{\text{AE}}$ can transition high one CLKB cycle later than shown.

Figure 8. Timing for $\overline{\text{AE}}$ When FIFO Is Almost Empty



NOTE: FIFO write ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = H, MBA = L), FIFO read ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = H, MBB = L)

† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{\text{AF}}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, then $\overline{\text{AF}}$ can transition high one CLKA cycle later than shown.

Figure 9. Timing for $\overline{\text{AF}}$ When FIFO Is Almost Full

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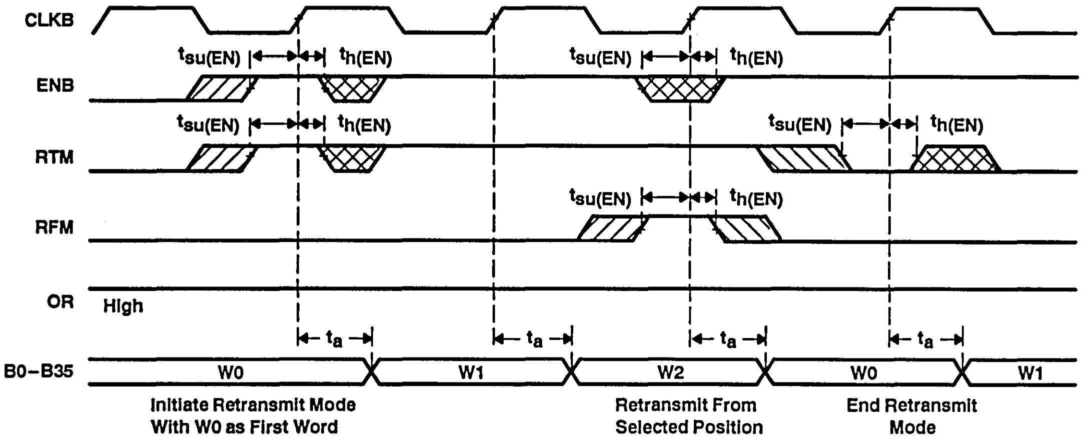
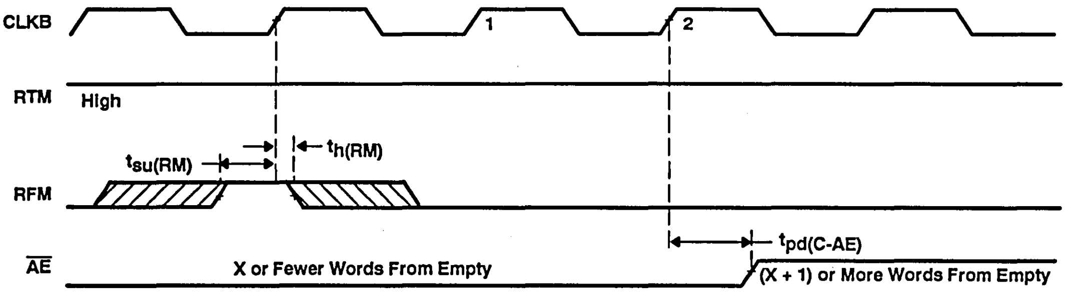


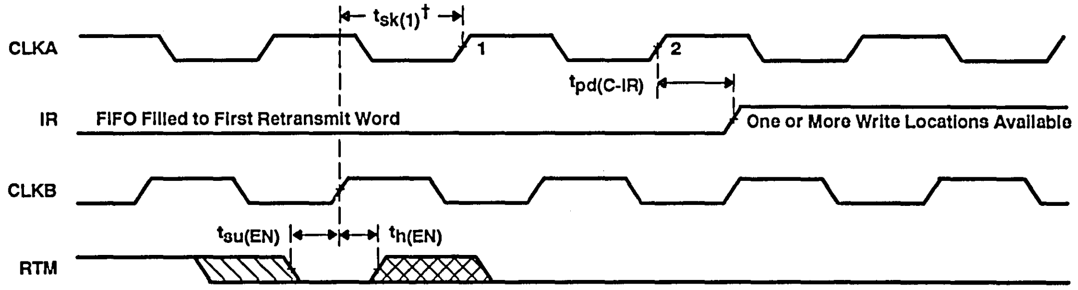
NOTE: $\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

Figure 10. Retransmit Timing Showing Minimum Retransmit Length



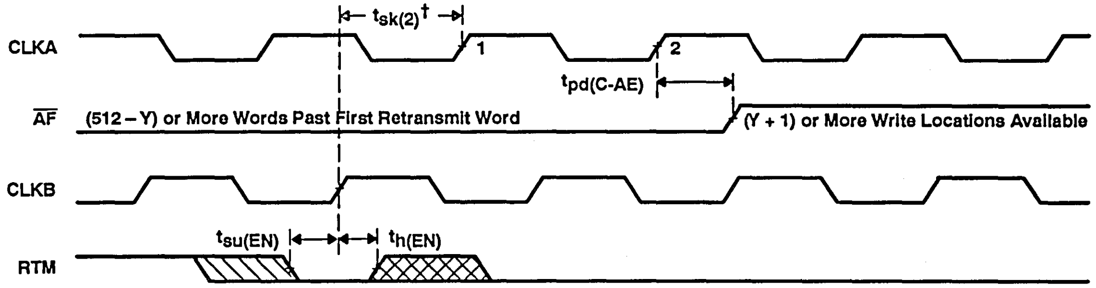
NOTE: X is the value loaded in the almost-empty flag offset register.

Figure 11. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X



† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, then IR can transition high one CLKA cycle later than shown.

Figure 12. IR Timing From the End of Retransmit Mode When One or More Write Locations Are Available



NOTE: Y is the value loaded in the almost-full flag offset register.

† $t_{sk(2)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, then $\overline{AF}$ can transition high one CLKA cycle later than shown.

Figure 13. $\overline{AF}$ Timing From the End of Retransmit Mode When (Y + 1) or More Write Locations Are Available

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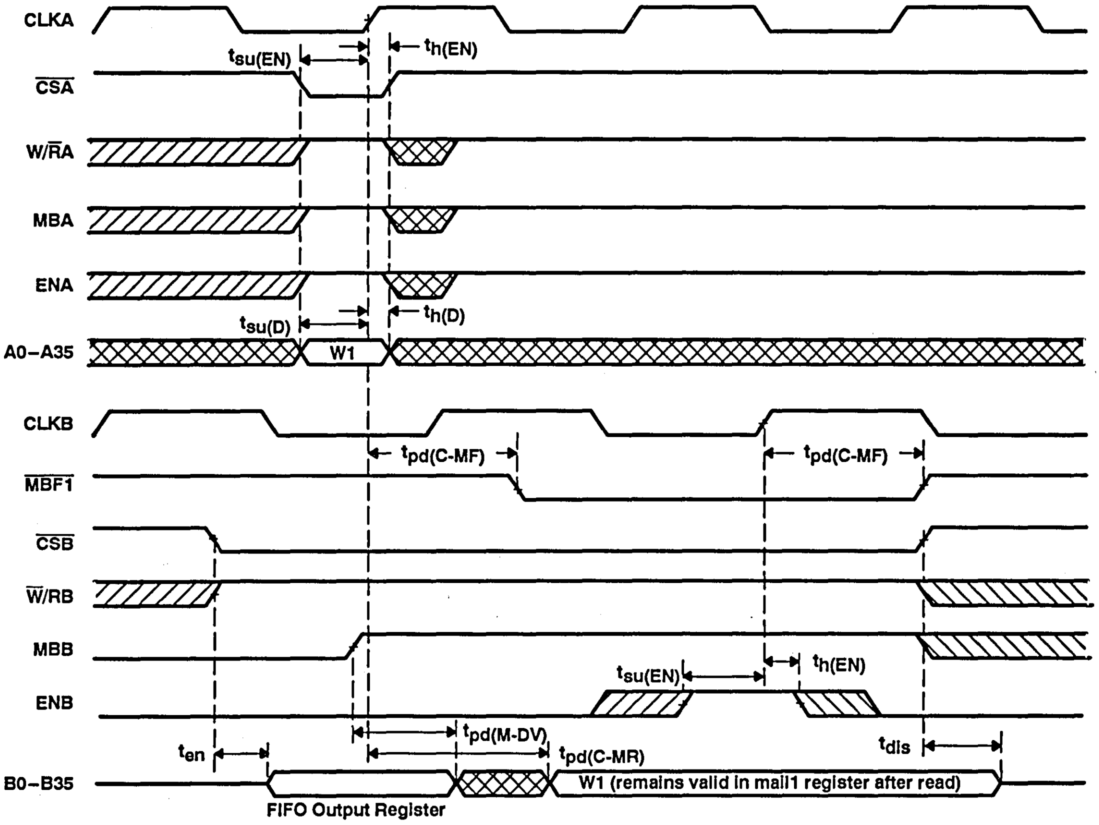

Figure 14. Timing for Mail1 Register and $\overline{MBF1}$ Flag

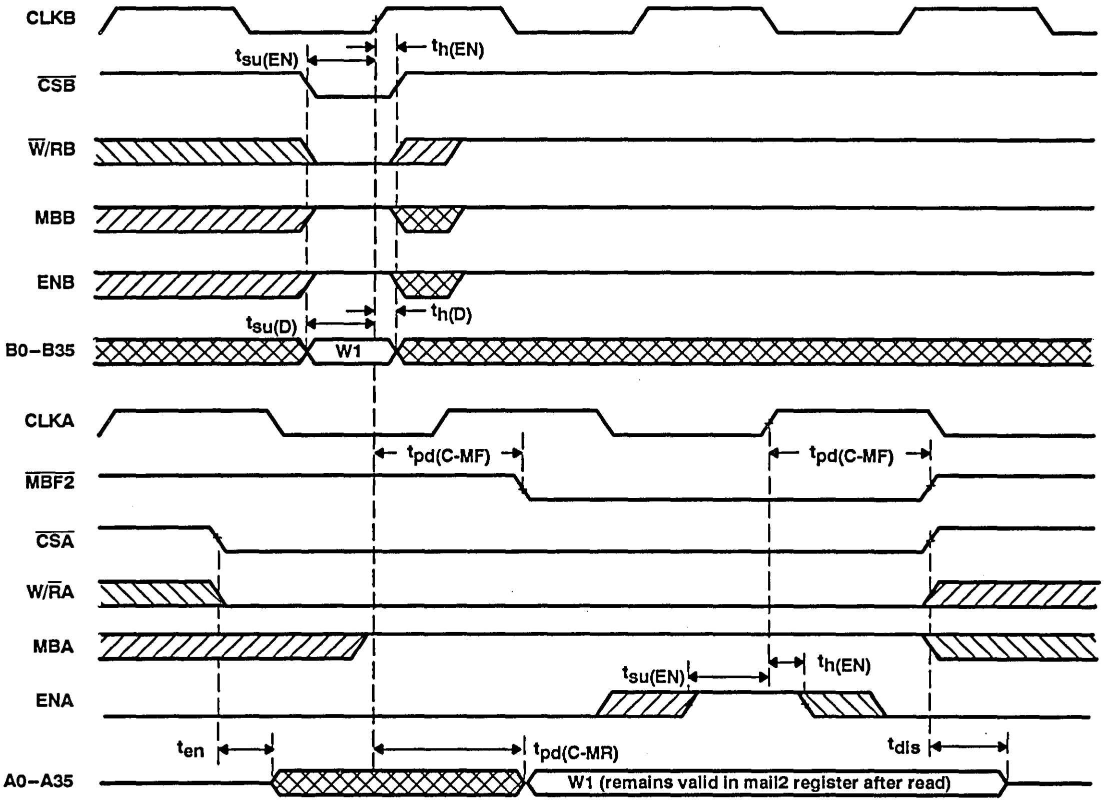

Figure 15. Timing for Mail2 Register and $\overline{MBF2}$ Flag

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings can be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0					±5	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0					±5	µA
I_{CC}	V_{CC} = 5.5 V,	$V_I = V_{CC}$ − 0.2 V or 0					400	µA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{CSA} = V_{IH}$	A0–A35		0		mA
			$\overline{CSB} = V_{IH}$	B0–B35		0		
			$\overline{CSA} = V_{IL}$	A0–A35			1	
			$\overline{CSB} = V_{IL}$	B0–B35			1	
			All other inputs				1	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 15)

		'ACT3631-15		'ACT3631-20		'ACT3631-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, MBB, RTM, and RFM before CLKB↑	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑[†]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{su(SD)}$[‡]	Setup time, FS0/SD before CLKA↑	4		5		6		ns
$t_{su(SEN)}$[‡]	Setup time, FS1/$\overline{SEN}$ before CLKA↑	4		5		6		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑[†]	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	2		3		3		ns
$t_{h(SP)}$[‡]	Hold time, FS1/$\overline{SEN}$ high after $\overline{RST}$ high	15		20		30		ns
$t_{h(SD)}$[‡]	Hold time, FS0/SD after CLKA↑	0		0		0		ns
$t_{h(SEN)}$[‡]	Hold time, FS1/$\overline{SEN}$ after CLKA↑	0		0		0		ns
$t_{sk(1)}$[§]	Skew time, between CLKA↑ and CLKB↑ for OR and IR	6		8		10		ns
$t_{sk(2)}$[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12		16		20		ns

[†] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[‡] Only applies when serial load method is used to program flag offset registers

[§] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 15)

PARAMETER		'ACT3631-15		'ACT3631-20		'ACT3631-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKB↑ to B0–B35		11		13		15	ns
$t_{pd(C-IR)}$	Propagation delay time, CLKA↑ to IR		11		13		15	ns
$t_{pd(C-OR)}$	Propagation delay time, CLKB↑ to OR		11		13		15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$		11		13		15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$		11		13		15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high		11		13		15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡		11		13		15	ns
$t_{pd(M-DV)}$	Propagation delay time, MBB to B0–B35 valid		9		11		13	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ low to $\overline{AE}$ low and $\overline{AF}$ high		15		20		30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active		10		12		14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance		10		12		14	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

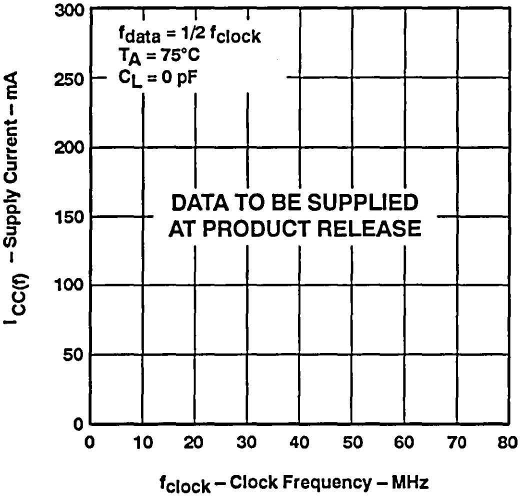


Figure 16

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 16, the maximum power dissipation (P_T) of the SN74ACT3631/3651 can be calculated by:

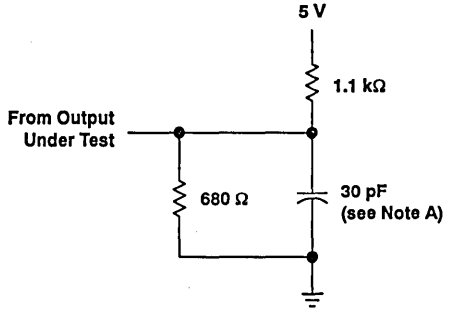
$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

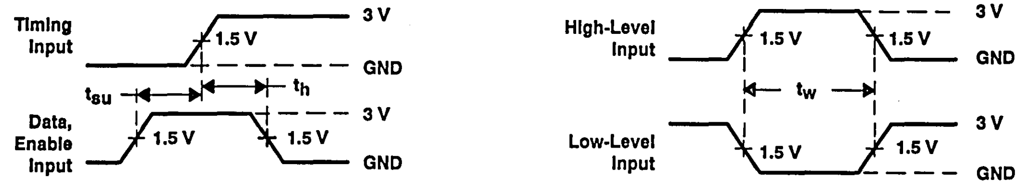
N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

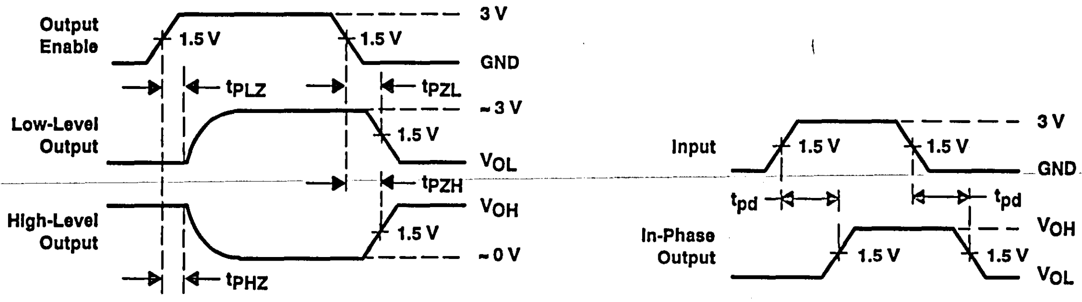


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 17. Load Circuit and Voltage Waveforms

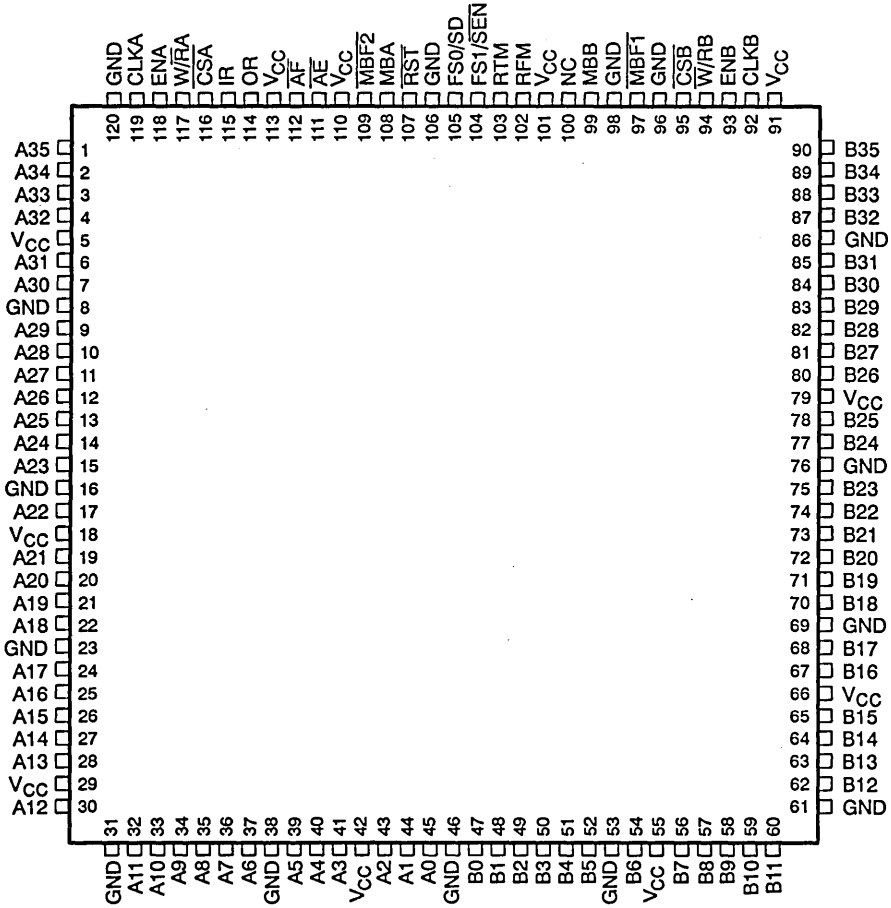
PRODUCT PREVIEW

SN74ACT3641
1024 × 36
CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS338A – JANUARY 1994 – REVISED JUNE 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Clocked FIFO Buffering Data From Port A to Port B**
- **Memory Size: 1024 × 36**
- **Synchronous Read Retransmit Capability**
- **Mailbox Register in Each Direction**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **Input-Ready (IR) and Almost-Full ($\overline{\text{AF}}$) Flags Synchronized by CLKA**
- **Output-Ready (OR) and Almost-Empty ($\overline{\text{AE}}$) Flags Synchronized by CLKB**
- **Low-Power 0.8-Micron Advanced CMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 11 ns**
- **Pin-to-Pin Compatible With the SN74ACT3631, and SN74ACT3651**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)**

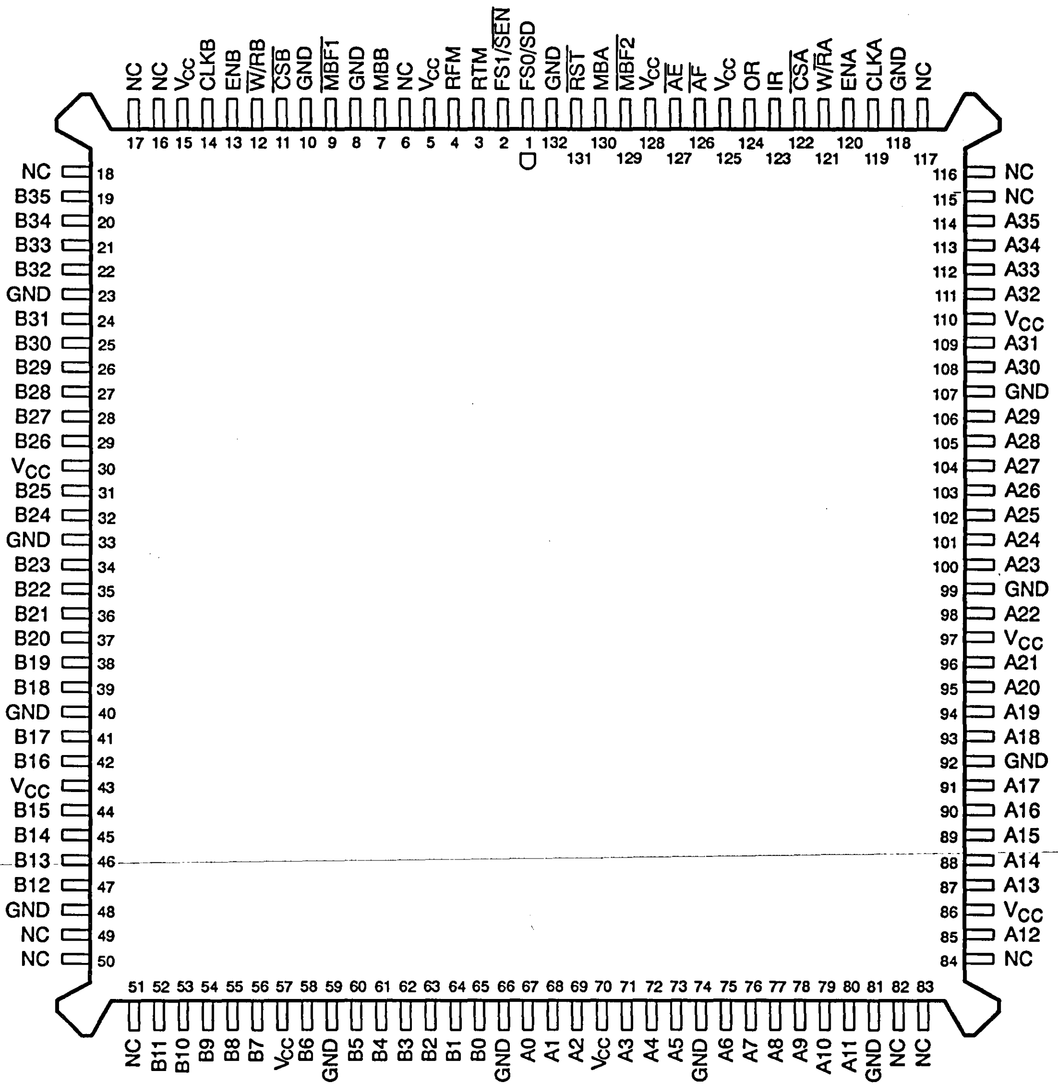
PCB PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

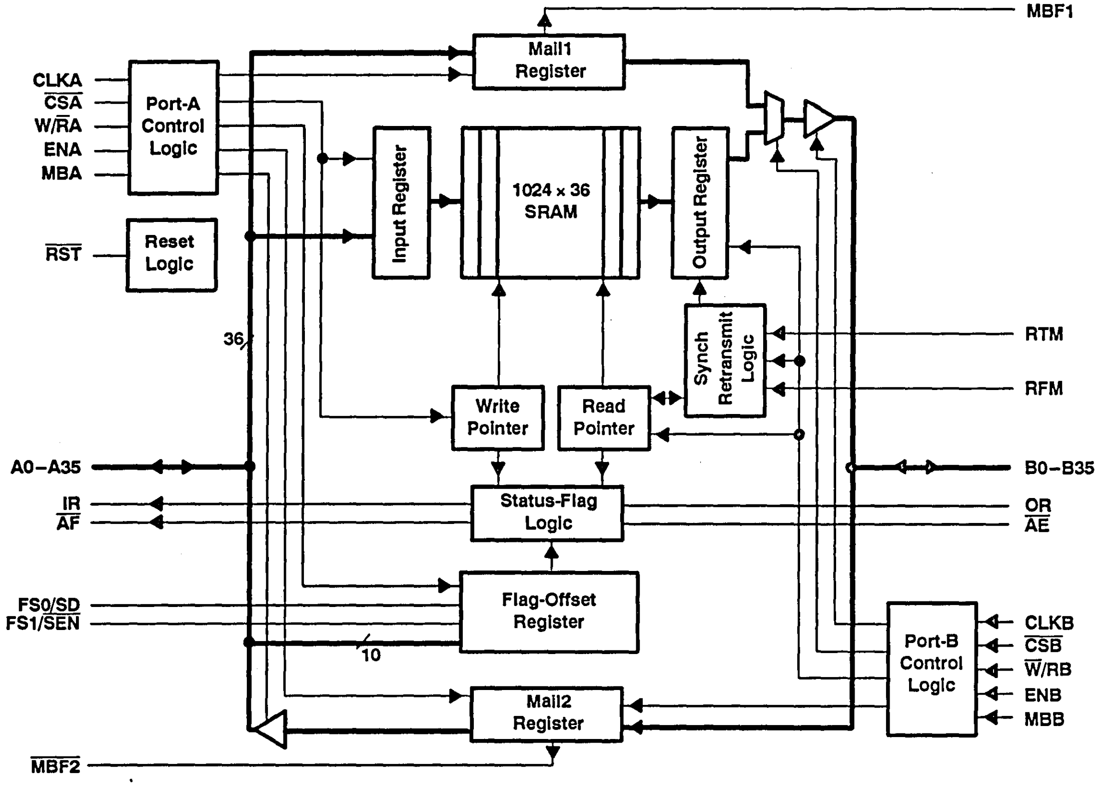
description

The SN74ACT3641 is a high-speed, low-power, CMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. The 1024 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths. Expansion is also possible in word depth.

The SN74ACT3641 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

The input-ready (IR) flag and almost-full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The output-ready (OR) flag and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the almost-full and almost-empty flags of the FIFO can be programmed from port A or through a serial input.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AE}}$	O	Almost-empty flag. Programmable flag synchronized to CLKB. $\overline{\text{AE}}$ is low when the number of words in the FIFO is less than or equal to the value in the almost-empty offset register (X).
$\overline{\text{AF}}$	O	Almost-full flag. Programmable flag synchronized to CLKA. $\overline{\text{AF}}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the almost-full offset register (Y).
B0–B35	I/O	Port-B data. 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IR and $\overline{\text{AF}}$ are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. OR and $\overline{\text{AE}}$ are synchronous to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1/$\overline{\text{SEN}}$, FS0/SD	I	Flag offset select 1/serial enable, flag offset select 0/serial data. FS1/$\overline{\text{SEN}}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During a device reset, FS1/$\overline{\text{SEN}}$ and FS0/SD select the flag offset programming method. Three offset register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{\text{SEN}}$ is used as an enable synchronous to the low-to-high transition of CLKA. When FS1/$\overline{\text{SEN}}$ is low, a rising edge on CLKA loads the bit present on FS0/SD into the X and Y offset registers. The number of bit writes required to program the offset registers is 20. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of CLKA. When IR is low, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set low during reset and is set high after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high by a reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is set high by a reset.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of CLKB. When OR is low, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is high. OR is forced low during the reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
RFM	I	Read from mark. When the FIFO is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of FS0 and FS1 for $\overline{\text{AF}}$ and $\overline{\text{AE}}$ offset selection.
RTM	I	Retransmit mode. When RTM is high and valid data is present in the FIFO output register (OR is high), a low-to-high transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, taking the FIFO out of retransmit mode.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
W/$\overline{\text{RA}}$	I	Port-A write/read select. A high on W/$\overline{\text{RA}}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
$\overline{\text{W}}$/RB	I	Port-B write/read select. A low on $\overline{\text{W}}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{\text{W}}$/RB is low.

detailed description

reset

The SN74ACT3641 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the input-ready (IR) flag low, the output-ready (OR) flag low, the almost-empty ($\overline{\text{AE}}$) flag low, and the almost-full ($\overline{\text{AF}}$) flag high. Resetting the device also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a FIFO is reset, its input-ready flag is set high after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

almost-empty flag and almost-full flag offset programming

Two registers in the SN74ACT3641 are used to hold the offset values for the almost-empty and almost-full flags. The almost-empty ($\overline{\text{AE}}$) flag offset register is labeled X, and the almost-full ($\overline{\text{AF}}$) flag offset register is labeled Y. The offset registers can be loaded with a value in three ways: one of two preset values are loaded into the offset registers, parallel load from port A, or serial load. The offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a low-to-high transition on the $\overline{\text{RST}}$ input (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	X AND Y REGISTERS†
H	H	↑	Serial load
H	L	↑	64
L	H	↑	8
L	L	↑	Parallel load from port A

† X register holds the offset for $\overline{\text{AE}}$; Y register holds the offset for $\overline{\text{AF}}$.

preset values

If a preset value of 8 or 64 is chosen by the FS1 and FS0 inputs at the time of a $\overline{\text{RST}}$ low-to-high transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set high after two low-to-high transitions on CLKA.

parallel load from port A

To program the X and Y registers from port A, the device is reset with FS0 and FS1 low during the low-to-high transition of $\overline{\text{RST}}$. After this reset is complete, the IR flag is set high after two low-to-high transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the offset registers in the order Y, X. Each offset register of the SN74ACT3641 uses port-A inputs (A9–A0). Data input A9 is used as the most significant bit of the binary number. Each register value can be programmed from 1 to 1020. After both offset registers are programmed from port A, subsequent FIFO writes store data in the SRAM.

serial load

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/SEN high during the low-to-high transition of RST. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each low-to-high transition of CLKA that the FS1/SEN input is low. 20-bit writes are needed to complete the programming for the SN74ACT3641. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the the X register. Each register value can be programmed from 1 to 1020.

When the option to program the offset registers serially is chosen, the input-ready (IR) flag remains low until all 20 bits are written. The IR flag is set high by the low-to-high transition of CLKA after the last bit is loaded to allow normal FIFO operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select (CSA) and the port-A write/read select (W/RA). The A0–A35 outputs are in the high-impedance state when either CSA or W/RA is high. The A0–A35 outputs are active when both CSA and W/RA are low.

Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when CSA and the port-A mailbox select (MBA) are low, W/RA, the port-A enable (ENA), and the input-ready (IR) flag are high (see Table 2). Writes to the FIFO are independent of any concurrent FIFO reads.

Table 2. Port-A Enable Function Table

CSA	W/RA	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set MBF2 high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select (W/RB) is the inverse of the port-A write/read select (W/RA). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select (CSB) and the port-B write/read select (W/RB). The B0–B35 outputs are in the high-impedance state when either CSB is high or W/RB is low. The B0–B35 outputs are active when CSB is low and W/RB is high.

Data is read from the FIFO to its output register on a low-to-high transition of CLKB when CSB and the port-B mailbox select (MBB) are low, W/RB, the port-B enable (ENB), and the output-ready (OR) flag are high (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	$\text{W}/\overline{\text{RB}}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	None
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO output register	None
L	H	H	L	↑	Active, FIFO output register	FIFO read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup- and hold-time window of the cycle.

When the output-ready (OR) flag is low, the next data word is sent to the FIFO output register automatically by the CLKB low-to-high transition that sets the output-ready flag high. When OR is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B chip select ($\overline{\text{CSB}}$), write/read select ($\text{W}/\overline{\text{RB}}$), enable (ENB), and mailbox select (MBB).

synchronized FIFO flags

Each SN74ACT3641 FIFO flag is synchronized to its port clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B*)*. OR and $\overline{\text{AE}}$ are synchronized to CLKB. IR and $\overline{\text{AF}}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN FIFO†‡	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	OR	$\overline{\text{AE}}$	$\overline{\text{AF}}$	IR
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [1024 – (Y + 1)]	H	H	H	H
(1024 – Y) to 1023	H	H	L	H
1024	H	H	L	L

† X is the almost-empty offset for $\overline{\text{AE}}$. Y is the almost-full offset for $\overline{\text{AF}}$.

‡ When a word is present in the FIFO output register, its previous memory location is free.

output-ready flag (OR)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of CLKB occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time $t_{sk(1)}$ or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

input-ready flag (IR)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). When the input-ready flag is high, a memory location is free in the SRAM to write new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA; therefore, an input-ready flag is low if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets the input-ready flag high, and data can be written in the following cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time $t_{sk(1)}$ or greater after the read. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

almost-empty flag ($\overline{AE}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-empty flag is low when the FIFO contains X or less words and is high when the FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of CLKB have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 8).

almost-full flag ($\overline{AF}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-full flag is low when the number of words in the FIFO is greater than or equal to (1024 – Y). The almost-full flag is high when the number of words in the FIFO is less than or equal to [1024 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKA are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [1024 – (Y + 1)] or less words remains low if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [1024 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of words in memory to [1024 – (Y + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the read that reduces the number of words in memory to [1024 – (Y + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 9).

synchronous retransmit

The synchronous retransmit feature of the SN74ACT3641 allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent on-going FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a low-to-high transition on CLKB when the retransmit mode (RTM) input is high and OR is high. This rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a low-to-high transition occurs while RTM is low.

When two or more reads have been done past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be low during the CLKB rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{AE}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{AF}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{AF}$ is set low by the write that stores (1024 – Y) words after the first retransmit word. The IR flag is set low by the 1024th write after the first retransmit word.

When the FIFO is in retransmit mode and RFM is high, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflects the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{AE}$ high (see Figure 11). The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{AF}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{AF}$ should cause one or both flags to transition high, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time $t_{sk(1)}$ or greater after the rising CLKB edge (see Figure 12). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{AF}$ if it occurs at time $t_{sk(2)}$ or greater after the rising CLKB edge (see Figure 14).

mailbox registers

Two 36-bit bypass registers are on the SN74ACT3641 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port A write is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{\text{MBF1}}$ or $\overline{\text{MBF2}}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag ($\overline{\text{MBF1}}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB with MBB high. The mail2 register flag ($\overline{\text{MBF2}}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

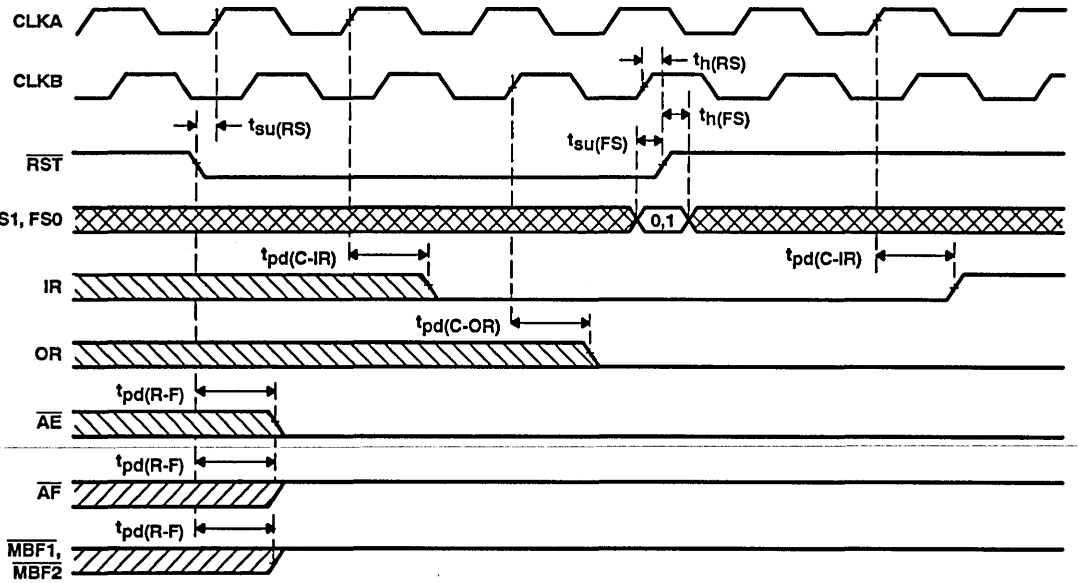
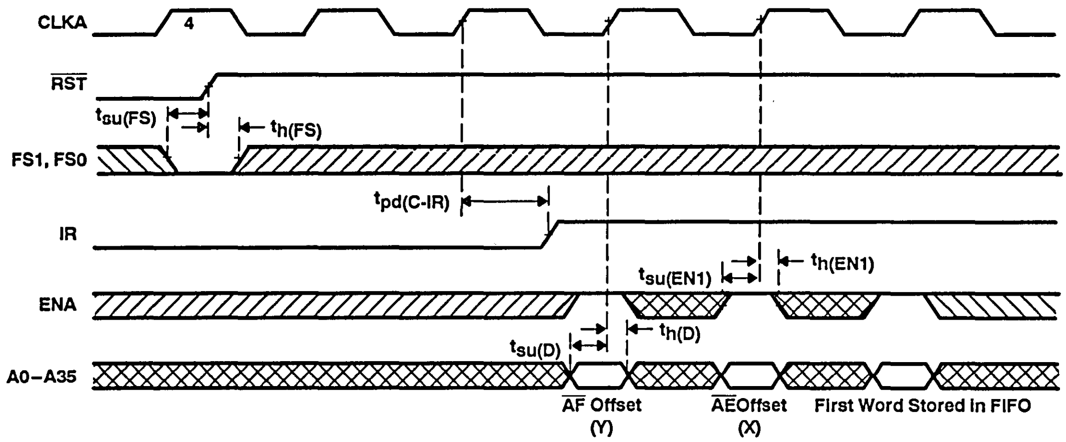
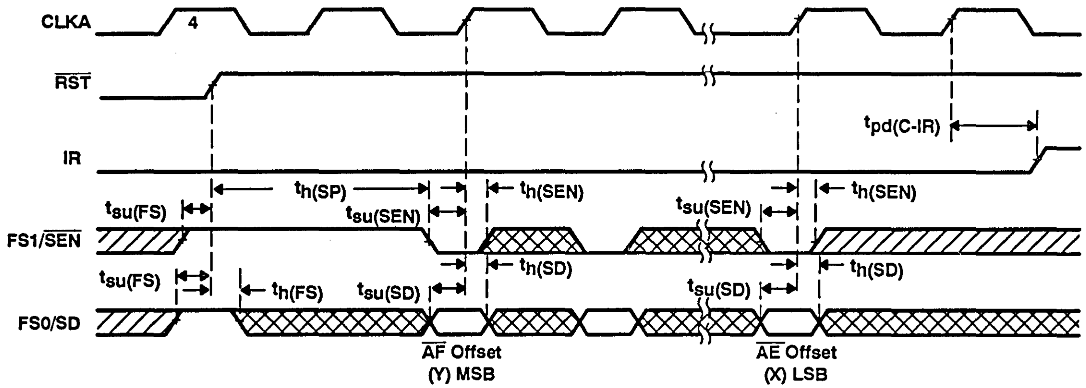


Figure 1. FIFO Reset Loading X and Y With a Preset Value of Eight



NOTE: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values From Port A



NOTE: It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set high.

Figure 3. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values Serially

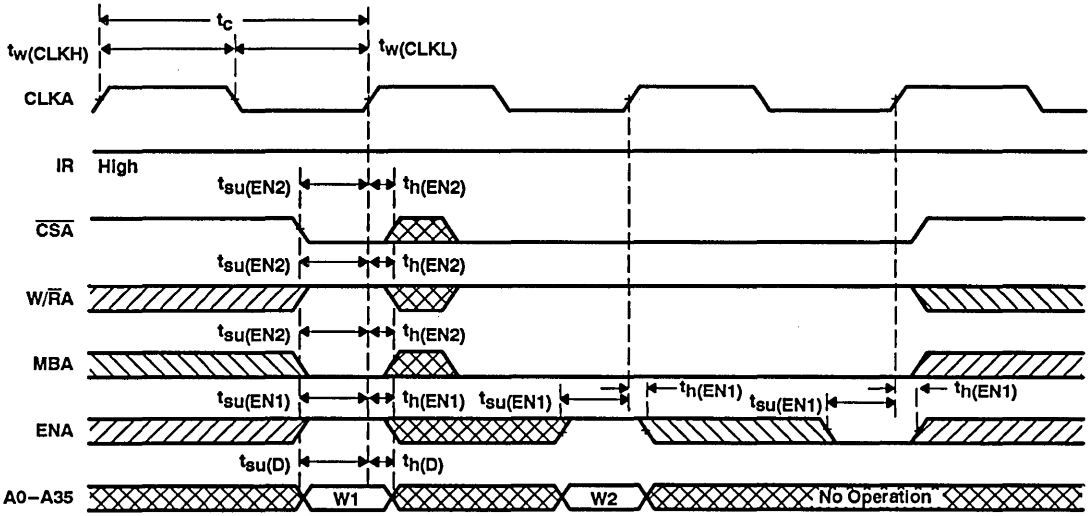


Figure 4. FIFO Write-Cycle Timing

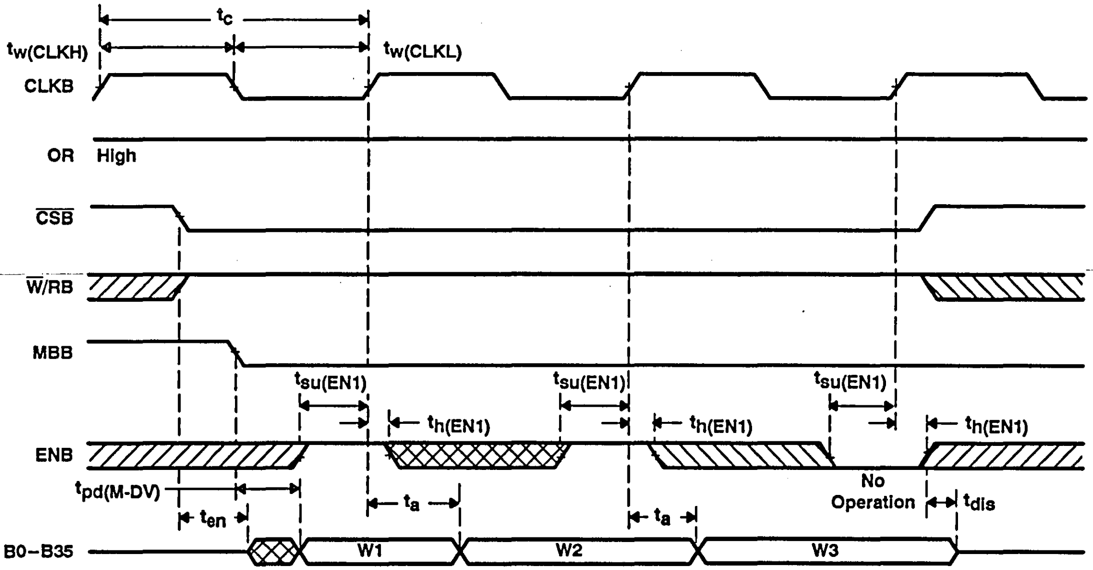
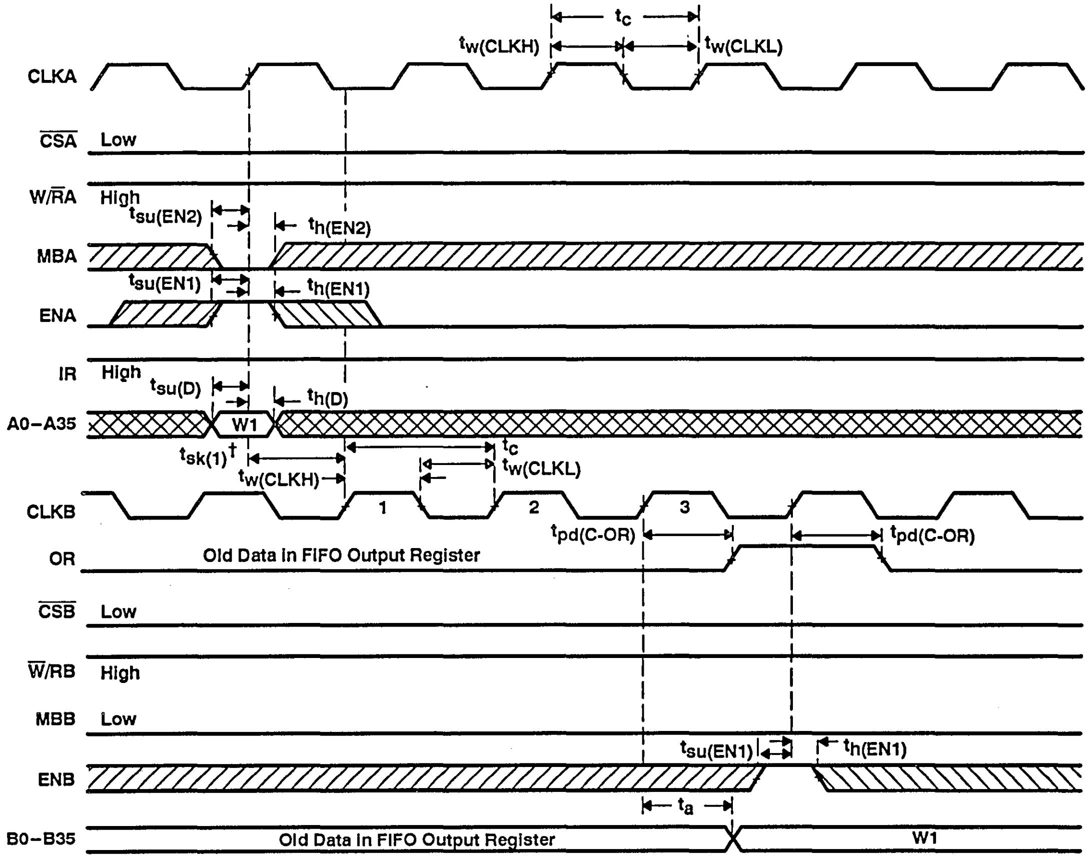
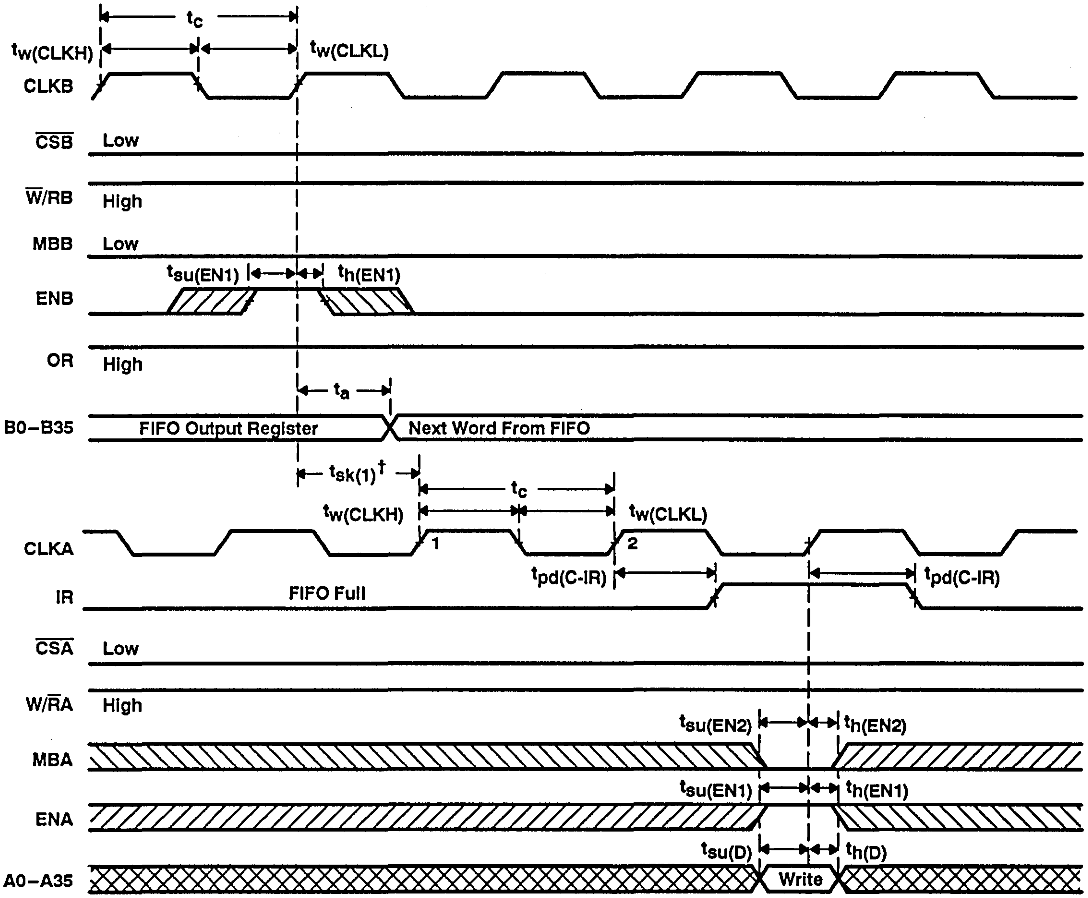


Figure 5. FIFO Read-Cycle Timing



† $t_{sk(1)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition high and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(1)}$, then the transition of OR high and the first word load to the output register can occur one CLKB cycle later than shown.

Figure 6. OR-Flag Timing and First Data Word Fallthrough When the FIFO Is Empty



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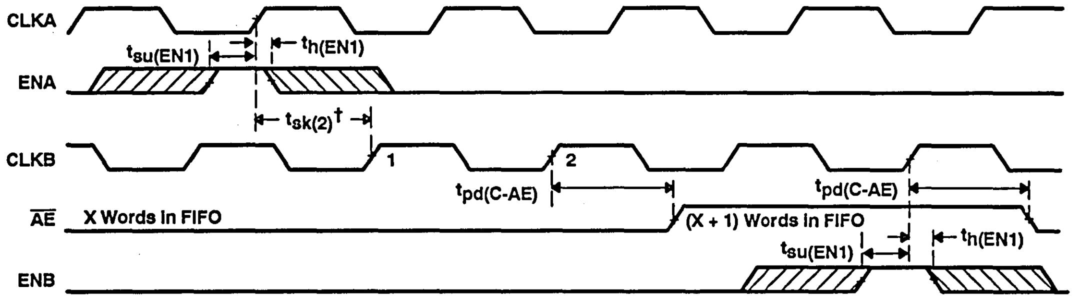
† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, then IR can transition high one CLKA cycle later than shown.

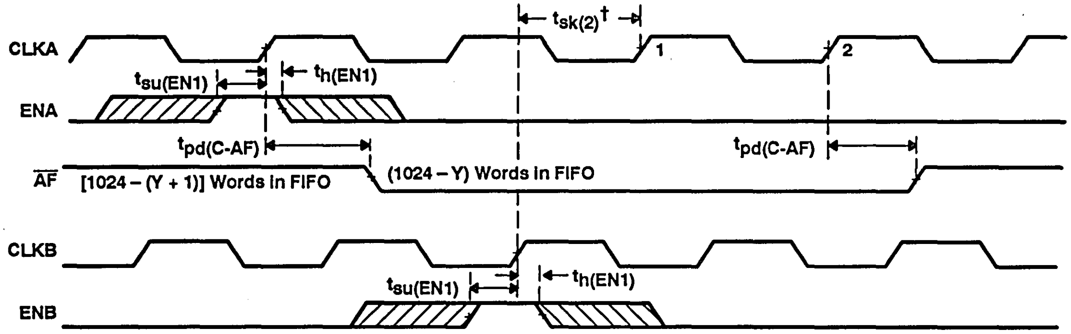
Figure 7. IR-Flag Timing and First Available Write When the FIFO Is Full



NOTE: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(2)}$, then $\overline{AE}$ can transition high one CLKB cycle later than shown.

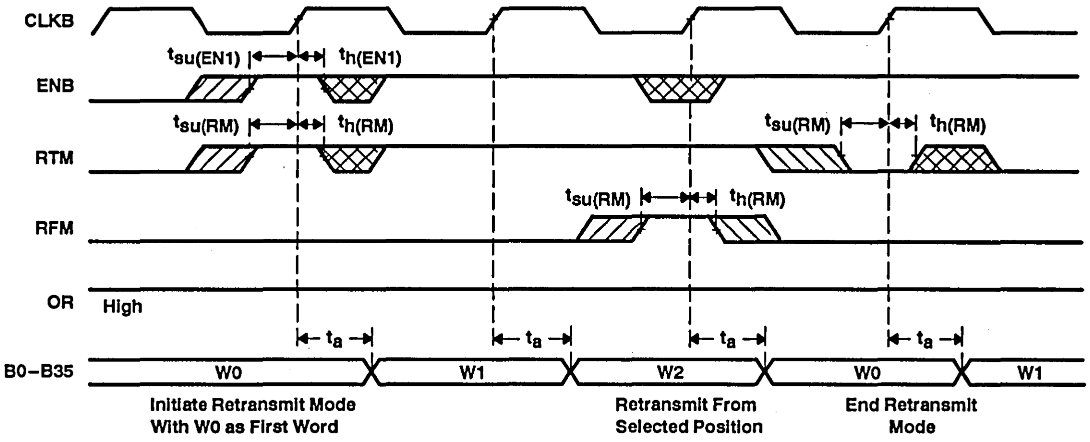
Figure 8. Timing for $\overline{AE}$ When FIFO Is Almost Empty



NOTE: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

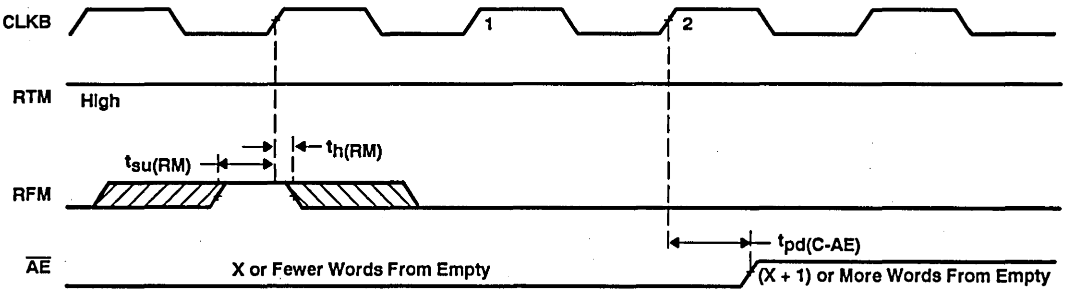
† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, then $\overline{AF}$ can transition high one CLKA cycle later than shown.

Figure 9. Timing for $\overline{AF}$ When FIFO Is Almost Full



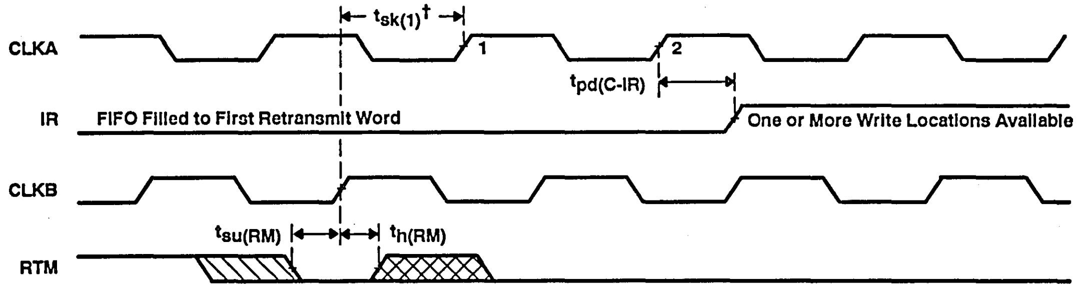
NOTE: $\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

Figure 10. Retransmit Timing Showing Minimum Retransmit Length



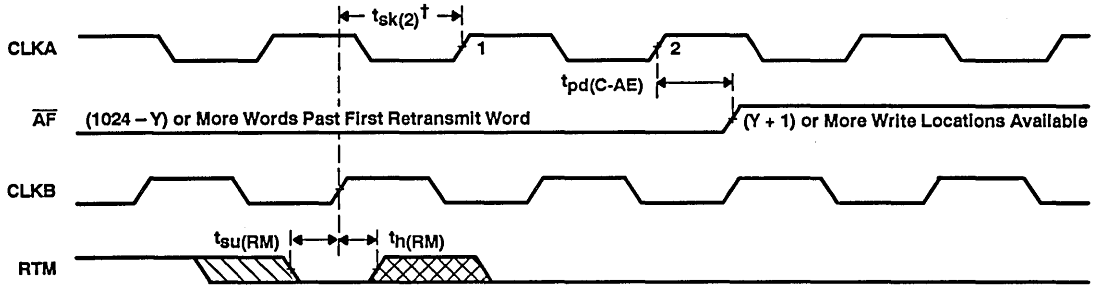
NOTE: X is the value loaded in the almost-empty flag offset register.

Figure 11. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X



† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, then IR can transition high one CLKA cycle later than shown.

Figure 12. IR Timing From the End of Retransmit Mode When One or More Write Locations Are Available



NOTE: Y is the value loaded in the almost-full flag offset register.

† $t_{sk(2)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, then $\overline{AF}$ can transition high one CLKA cycle later than shown.

Figure 13. $\overline{AF}$ Timing From the End of Retransmit Mode When (Y + 1) or More Write Locations Are Available

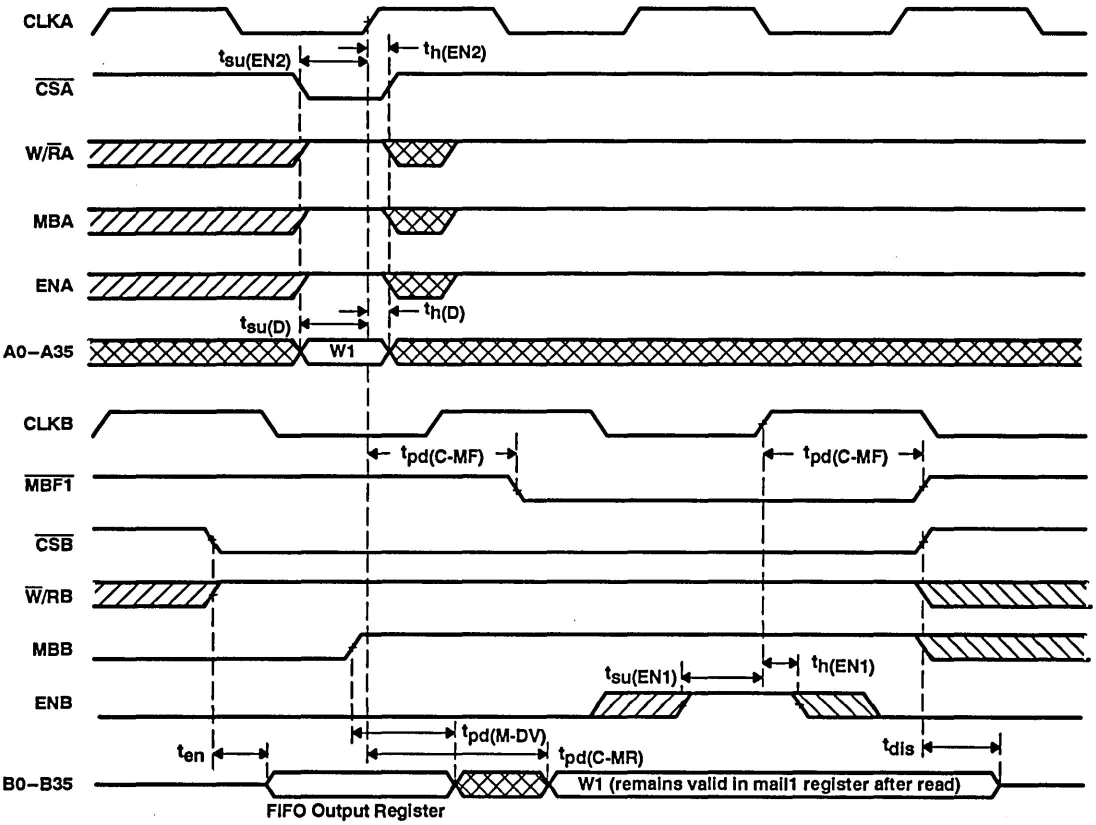


Figure 14. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

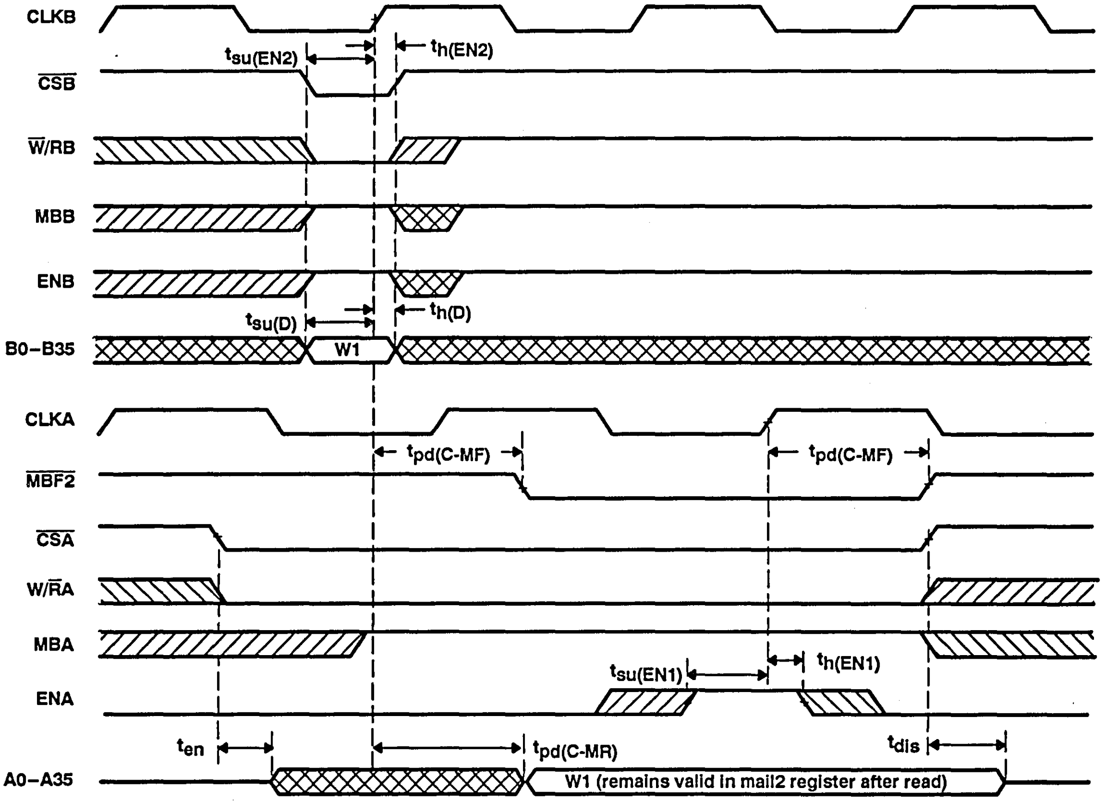


Figure 15. Timing for Mail2 Register and $\overline{MBF2}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

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† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0					±5	μA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0					±5	μA
I_{CC}	V_{CC} = 5.5 V,	$V_I = V_{CC} - 0.2$ V or 0					400	μA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{CSA} = V_{IH}$	A0–A35		0		mA
			$\overline{CSB} = V_{IH}$	B0–B35		0		
			$\overline{CSA} = V_{IL}$	A0–A35			1	
			$\overline{CSB} = V_{IL}$	B0–B35			1	
			All other inputs				1	
C_i	$V_I = 0$,	f = 1 MHz				4		pF
C_o	$V_O = 0$,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 15)

		'ACT3641-15		'ACT3641-20		'ACT3641-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	5		6		7		ns
$t_{su(EN1)}$	Setup time, ENA to CLKA↑; ENB to CLKB↑	5		6		7		ns
$t_{su(EN2)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, and MBA to CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, and MBB to CLKB↑	7		7.5		8		ns
$t_{su(RM)}$	Setup time, RTM and RFM to CLKB↑	6		6.5		7		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑†	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	9		10		11		ns
$t_{su(SD)}$‡	Setup time, FS0/SD before CLKA↑	5		6		7		ns
$t_{su(SEN)}$‡	Setup time, FS1/$\overline{SEN}$ before CLKA↑	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN1)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	0		0		0		ns
$t_{h(EN2)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RM)}$	Hold time, RTM and RFM after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑ †	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	0		0		0		ns
$t_{h(SP)}$‡	Hold time, FS1/$\overline{SEN}$ high after $\overline{RST}$ high	0		0		0		ns
$t_{h(SD)}$‡	Hold time, FS0/SD after CLKA↑	0		0		0		ns
$t_{h(SEN)}$‡	Hold time, FS1/$\overline{SEN}$ after CLKA↑	0		0		0		ns
$t_{sk(1)}$§	Skew time, between CLKA↑ and CLKB↑ for OR and IR	9		11		13		ns
$t_{sk(2)}$§	Skew time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12		16		20		ns

† Requirement to count the clock edge as one of at least four needed to reset a FIFO

‡ Only applies when serial load method is used to program flag offset registers

§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 15)

PARAMETER		'ACT3641-15		'ACT3641-20		'ACT3641-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKB↑ to B0–B35	3	11	3	13	3	15	ns
$t_{pd(C\text{-}IR)}$	Propagation delay time, CLKA↑ to IR	1	8	1	10	1	12	ns
$t_{pd(C\text{-}OR)}$	Propagation delay time, CLKB↑ to OR	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKB↑ to $\overline{\text{AE}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\text{AF}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\text{MBF1}}$ low or $\overline{\text{MBF2}}$ high and CLKB↑ to $\overline{\text{MBF2}}$ low or $\overline{\text{MBF1}}$ high	0	8	0	10	0	12	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	13.5	3	15	3	17	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBB to B0–B35 valid	3	13	3	15	3	17	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\text{RST}}$ low to $\overline{\text{AE}}$ low and $\overline{\text{AF}}$ high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ low to A0–A35 active and $\overline{\text{CSB}}$ low and $\overline{\text{W}}$/RB high to B0–B35 active	2	12	2	13	2	14	ns
t_{dis}	Disable time, $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ high to A0–A35 at high impedance and $\overline{\text{CSB}}$ high or $\overline{\text{W}}$/RB low to B0–B35 at high impedance	1	8	1	10	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

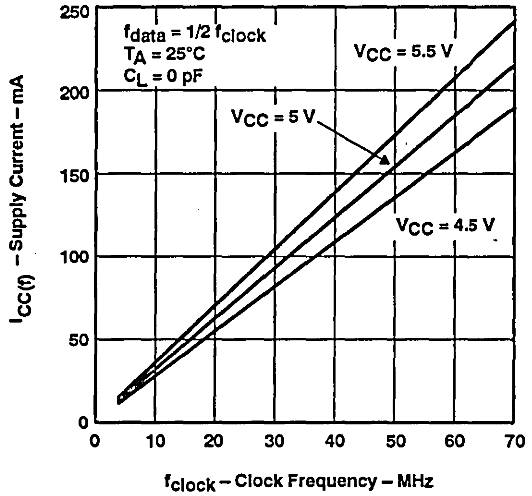


Figure 16

calculating power dissipation

The $I_{CC(f)}$ current in Figure 16 was taken while simultaneously reading and writing the FIFO on the SN74ACT3641 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs are disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel and the number of SN74ACT3641 inputs driven by TTL high levels are known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 16, the maximum power dissipation (P_T) of the SN74ACT3641 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

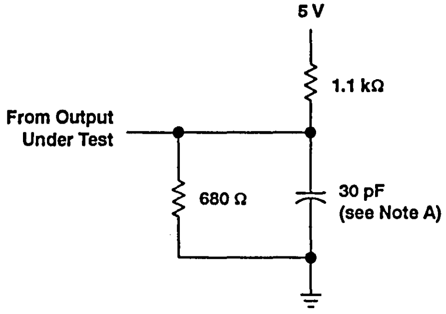
where:

N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

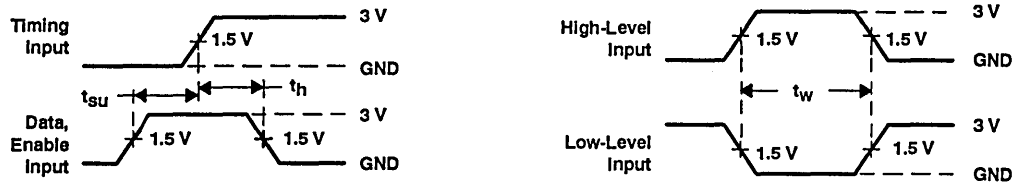
When no reads or writes are occurring on the SN74ACT3632, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.209\ mA/MHz$$

PARAMETER MEASUREMENT INFORMATION

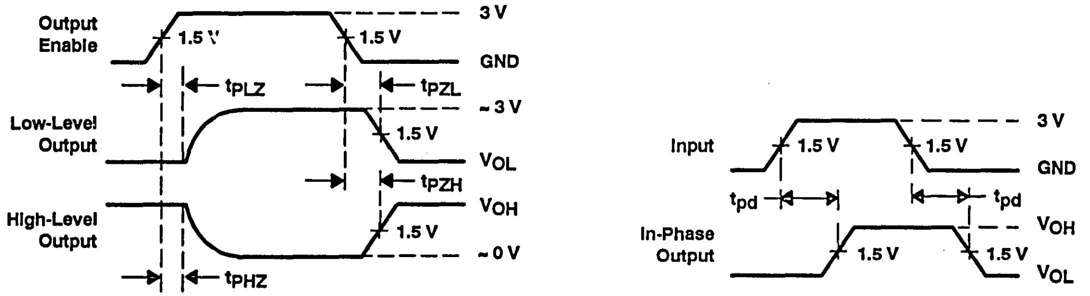


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 17. Load Circuit and Voltage Waveforms

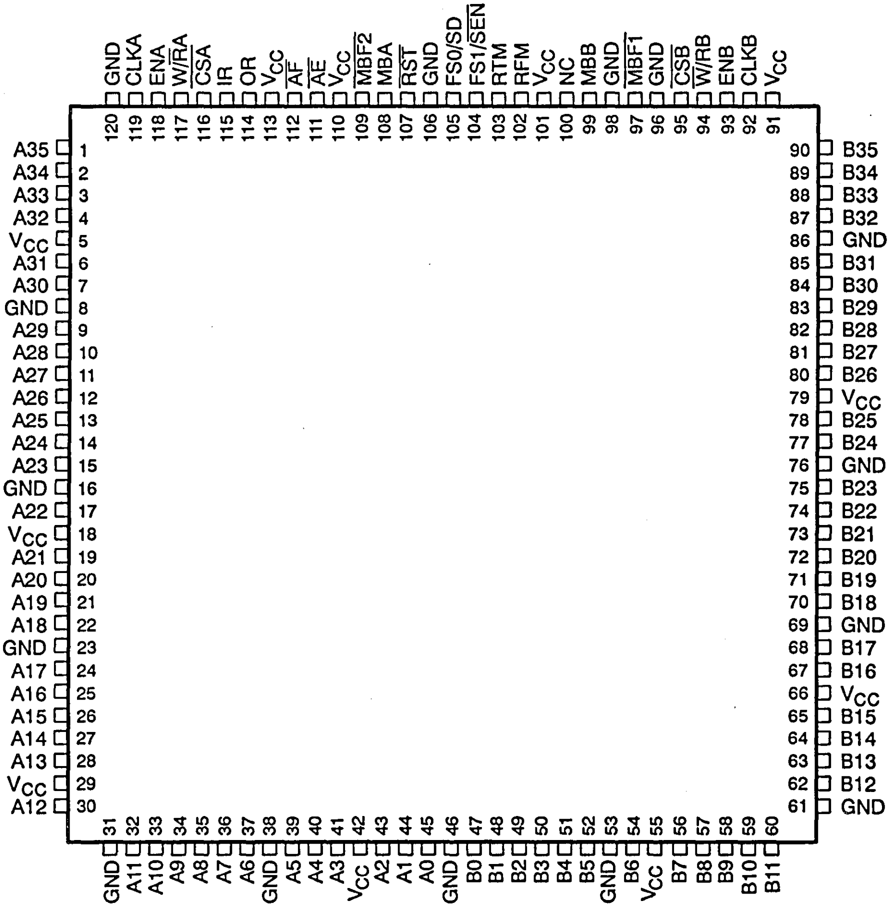
SN74ACT3651
2048 × 36 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS439 – JUNE 1994

- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Clocked FIFO Buffering Data From Port A to Port B
- Synchronous Read Retransmit Capability
- Mailbox Register in Each Direction
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- Input-Ready (IR) and Almost-Full ($\overline{AF}$) Flags Synchronized by CLKA
- Output-Ready (OR) and Almost-Empty ($\overline{AE}$) Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Pin-to-Pin Compatible With the SN74ACT3631 and SN74ACT3641
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)

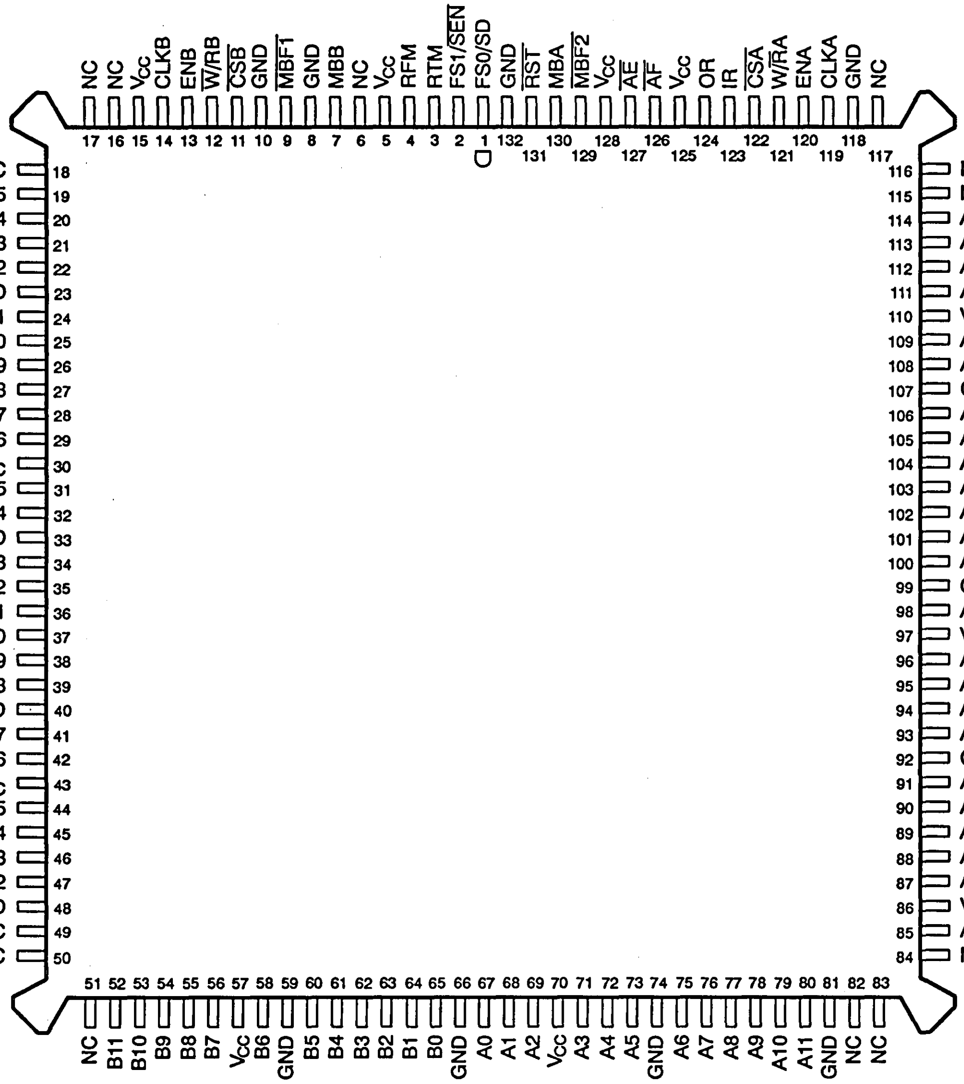
PRODUCT PREVIEW

PCB PACKAGE
(TOP VIEW)



NC – No internal connection

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection

† Uses Yamaichi socket IC51-1324-828

PRODUCT PREVIEW

description

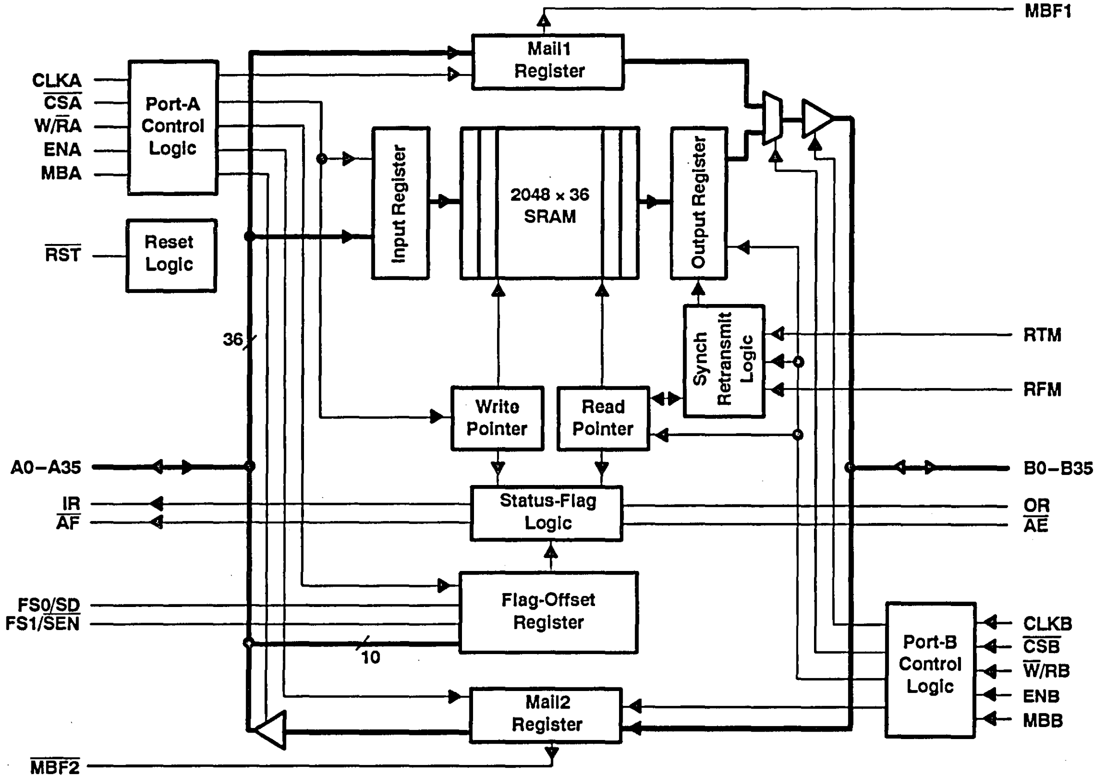
The SN74ACT3651 is a high-speed, low-power, CMOS clocked FIFO memory. It support clock frequencies up to 67 MHz and has read access times as fast as 12 ns. The 2048 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths. Expansion is also possible in word depth.

The SN74ACT3651 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

The input-ready (IR) flag and almost-full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The output-ready (OR) flag and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the almost-full and almost-empty flags of the FIFO can be programmed from port A or through a serial input.

PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AE}}$	O	Almost-empty flag. Programmable flag synchronized to CLKB. $\overline{\text{AE}}$ is low when the number of words in the FIFO is less than or equal to the value in the almost-empty offset register (X).
$\overline{\text{AF}}$	O	Almost-full flag. Programmable flag synchronized to CLKA. $\overline{\text{AF}}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the almost-full offset register (Y).
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IR and $\overline{\text{AF}}$ are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. OR and $\overline{\text{AE}}$ are synchronous to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1/$\overline{\text{SEN}}$, FS0/SD	I	Flag offset select 1/serial enable, flag offset select 0/serial data. FS1/$\overline{\text{SEN}}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During a device reset, FS1/$\overline{\text{SEN}}$ and FS0/SD select the flag offset programming method. Three offset register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{\text{SEN}}$ is used as an enable synchronous to the low-to-high transition of CLKA. When FS1/$\overline{\text{SEN}}$ is low, a rising edge on CLKA loads the bit present on FS0/SD into the X and Y offset registers. The number of bit writes required to program the offset registers is 22. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of CLKA. When IR is low, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set low during reset and is set high after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high by a reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is set high by a reset.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of CLKB. When OR is low, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is high. OR is forced low during the reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
RFM	I	Read from mark. When the FIFO is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of FS0 and FS1 for $\overline{\text{AF}}$ and $\overline{\text{AE}}$ offset selection.
RTM	I	Retransmit mode. When RTM is high and valid data is present in the FIFO output register (OR is high), a low-to-high transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, taking the FIFO out of retransmit mode.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
W/$\overline{\text{RA}}$	I	Port-A write/read select. A high on W/$\overline{\text{RA}}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
$\overline{\text{W}}$/RB	I	Port-B write/read select. A low on $\overline{\text{W}}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{\text{W}}$/RB is low.

detailed description

reset

The SN74ACT3651 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the input-ready (IR) flag low, the output-ready (OR) flag high, the almost-empty ($\overline{\text{AE}}$) flag low, and the almost-full ($\overline{\text{AF}}$) flag high. Resetting the device also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a FIFO is reset, its input-ready flag is set high after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

almost-empty flag and almost-full flag offset programming

Two registers in the SN74ACT3651 are used to hold the offset values for the almost-empty and almost-full flags. The almost-empty ($\overline{\text{AE}}$) flag offset register is labeled X, and the almost-full ($\overline{\text{AF}}$) flag offset register is labeled Y. The offset registers can be loaded with a value in three ways: one of two preset values are loaded into the offset registers, parallel load from port A, or serial load. The offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a low-to-high transition on the $\overline{\text{RST}}$ input (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	X AND Y REGISTERS†
H	H	↑	Serial load
H	L	↑	64
L	H	↑	8
L	L	↑	Parallel load from port A

† X register holds the offset for $\overline{\text{AE}}$; Y register holds the offset for $\overline{\text{AF}}$.

preset values

If a preset value of 8 or 64 is chosen by the FS1 and FS0 inputs at the time of a $\overline{\text{RST}}$ low-to-high transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set high after two low-to-high transitions on CLKA.

parallel load from port A

To program the X and Y registers from port A, the device is reset with FS0 and FS1 low during the low-to-high transition of $\overline{\text{RST}}$. After this reset is complete, the IR flag is set high after two low-to-high transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the offset registers in the order Y, X. Each offset register of the SN74ACT3651 uses port-A inputs (A10–A0). The highest number input is used as the most significant bit of the binary number in each case. Each register value can be programmed from 1 to 2044. After both offset registers are programmed from port A, subsequent FIFO writes store data in the SRAM.

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serial load

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/SEN high during the low-to-high transition of RST. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each low-to-high transition of CLKA that the FS1/SEN input is low. Eighteen- or 22-bit writes are needed to complete the programming for the SN74ACT3631 or SN74ACT3651, respectively. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the X register. Each register value can be programmed from 1 to 2044.

When the option to program the offset registers serially is chosen, the input-ready (IR) flag remains low until all register bits are written. The IR flag is set high by the low-to-high transition of CLKA after the last bit is loaded to allow normal FIFO operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select (CSA) and the port-A write/read select (W/RA). The A0–A35 outputs are in the high-impedance state when either CSA or W/RA is high. The A0–A35 outputs are active when both CSA and W/RA are low.

Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when CSA and the port-A mailbox select (MBA) are low, W/RA, the port-A enable (ENA), and the input-ready (IR) flag are high (see Table 2). Writes to the FIFO are independent of any concurrent FIFO reads.

Table 2. Port-A Enable Function Table

CSA	W/RA	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set MBF2 high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select (W/RB) is the inverse of the port-A write/read select (W/RA). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select (CSB) and the port-B write/read select (W/RB). The B0–B35 outputs are in the high-impedance state when either CSB is high or W/RB is low. The B0–B35 outputs are active when CSB is low and W/RB is high.

Data is read from the FIFO to its output register on a low-to-high transition of CLKB when CSB and the port-B mailbox select (MBB) are low, W/RB, the port-B enable (ENB), and the output-ready (OR) flag are high (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes.

Table 3. Port-B Enable Function Table

$\overline{\mathrm{CSB}}$	$\mathrm{W}/\overline{\mathrm{RB}}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	None
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO output register	None
L	H	H	L	↑	Active, FIFO output register	FIFO read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\mathrm{MBF1}}$ high)

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup- and hold-time window of the cycle.

When the output-ready (OR) flag is low, the next data word is sent to the FIFO output register automatically by the CLKB low-to-high transition that sets the output-ready flag high. When OR is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B chip select ($\overline{\mathrm{CSB}}$), write/read select ($\mathrm{W}/\overline{\mathrm{RB}}$), enable (ENB), and mailbox select (MBB).

synchronized FIFO flags

Each SN74ACT3651 FIFO flag is synchronized to its port clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). OR and $\overline{\mathrm{AE}}$ are synchronized to CLKB. IR and $\overline{\mathrm{AF}}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN FIFO[†‡]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	OR	$\overline{\mathrm{AE}}$	$\overline{\mathrm{AF}}$	IR
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [2048 – (Y + 1)]	H	H	H	H
(2048 – Y) to 2047	H	H	L	H
2048	H	H	L	L

[†] X is the almost-empty offset for $\overline{\mathrm{AE}}$. Y is the almost-full offset for $\overline{\mathrm{AF}}$.

[‡] When a word is present in the FIFO output register, its previous memory location is free.

output-ready flag (OR)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of CLKB occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time $t_{sk(1)}$ or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

input-ready flag (IR)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). When the input-ready flag is high, a memory location is free in the SRAM to write new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA; therefore, an input-ready flag is low if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets the input-ready flag high, and data can be written in the following cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time $t_{sk(1)}$ or greater after the read. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

almost-empty flag ($\overline{AE}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-empty flag is low when the FIFO contains X or less words and is high when the FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of CLKB have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 8).

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almost-full flag ($\overline{\text{AF}}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-full flag is low when the number of words in the FIFO is greater than or equal to 2048 – Y). The almost-full flag is high when the number of words in the FIFO is less than or equal to [2048 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKA are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [2048 – (Y + 1)] or less words remains low if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [2048 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of words in memory to [2048 – (Y + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the read that reduces the number of words in memory to [2048 – (Y + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 9).

synchronous retransmit

The synchronous retransmit feature of the SN74ACT3651 allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent on-going FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a low-to-high transition on CLKB when the retransmit mode (RTM) input is high and OR is high. This rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a low-to-high transition occurs while RTM is low.

When two or more reads have been done past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be low during the CLKB rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{\text{AE}}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{\text{AF}}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{\text{AF}}$ is set low by the write that stores (2048 – Y) words after the first retransmit word. The IR flag is set low by the 2048th write after the first retransmit word.

When the FIFO is in retransmit mode and RFM is high, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflects the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{\text{AE}}$ high (see Figure 11). The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{\text{AF}}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{\text{AF}}$ should cause one or both flags to transition high, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time $t_{sk(1)}$ or greater after the rising CLKB edge (see Figure 12). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{\text{AF}}$ if it occurs at time $t_{sk(2)}$ or greater after the rising CLKB edge (see Figure 14).

mailbox registers

Two 36-bit bypass registers are on the SN74ACT3631/3651 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{\text{MBF1}}$ or $\overline{\text{MBF2}}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag ($\overline{\text{MBF1}}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB with MBB high. The mail2 register flag ($\overline{\text{MBF2}}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

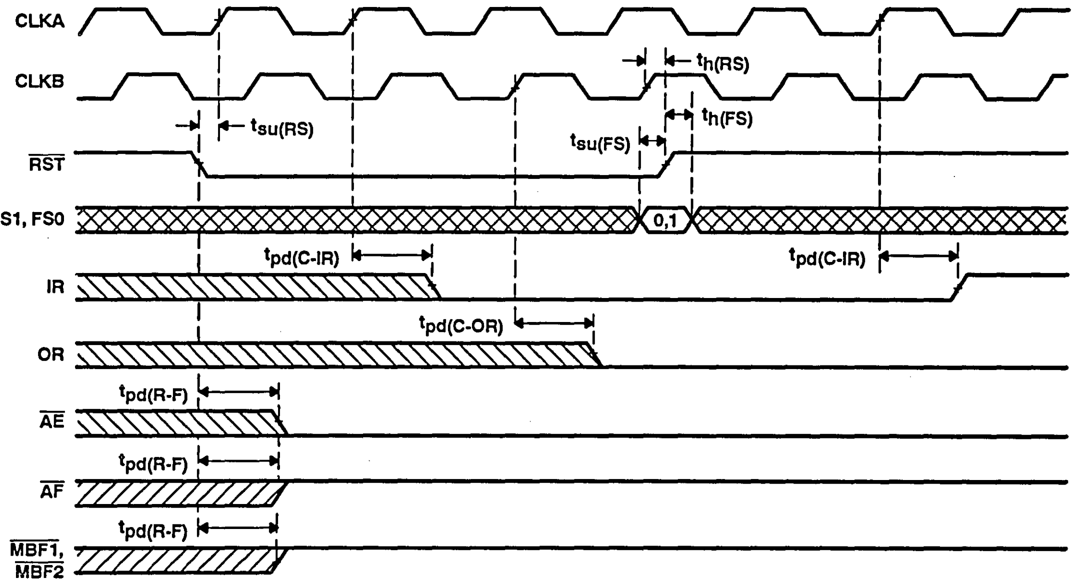

Figure 1. FIFO Reset Loading X and Y With a Preset Value of Eight

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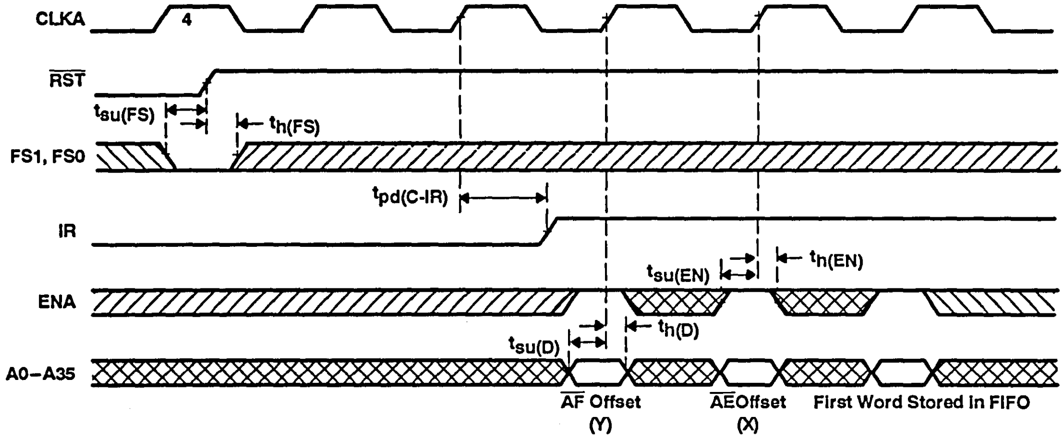
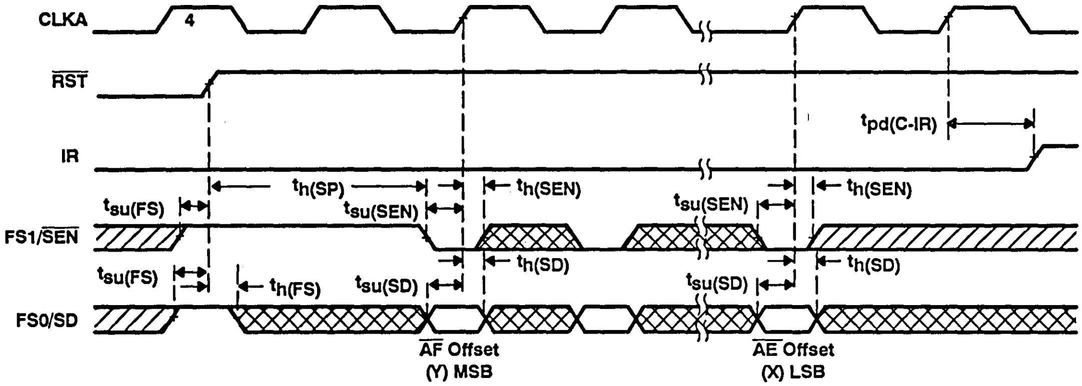


NOTE: CSA = L, W/RA = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values From Port A



NOTE: It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set high.

Figure 3. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values Serially

PRODUCT PREVIEW

PRODUCT PREVIEW

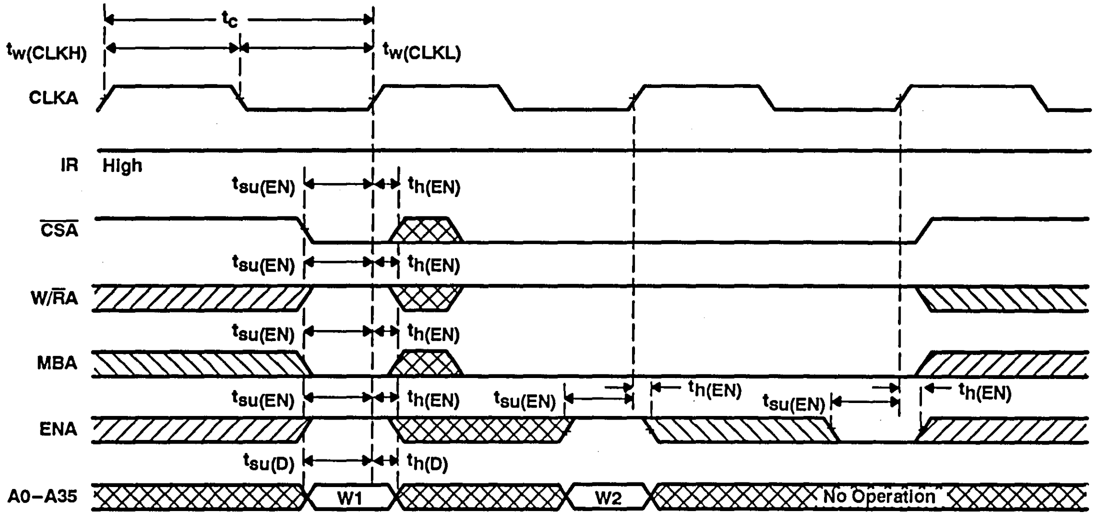


Figure 4. FIFO Write-Cycle Timing

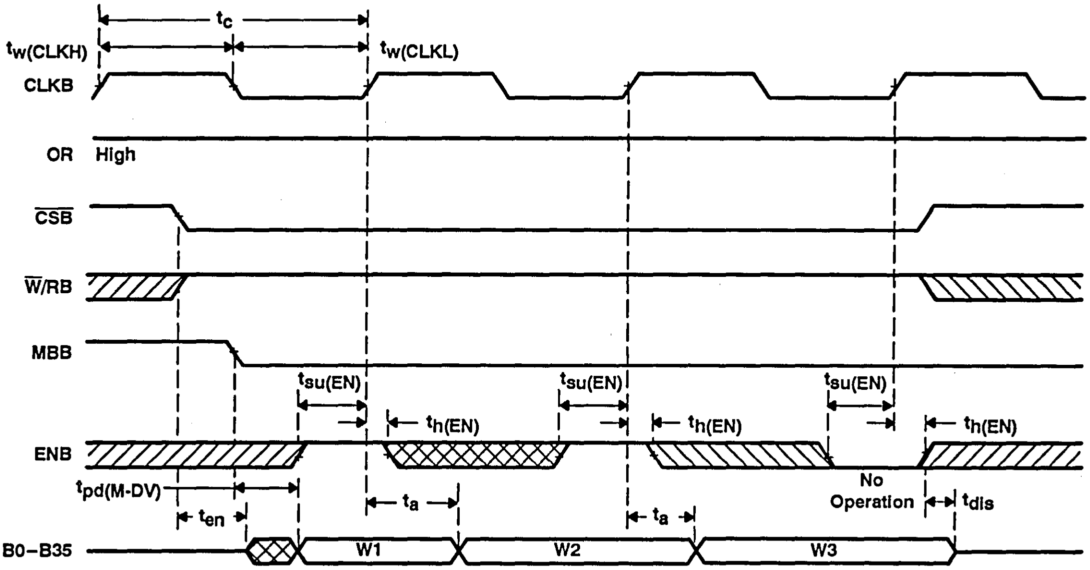
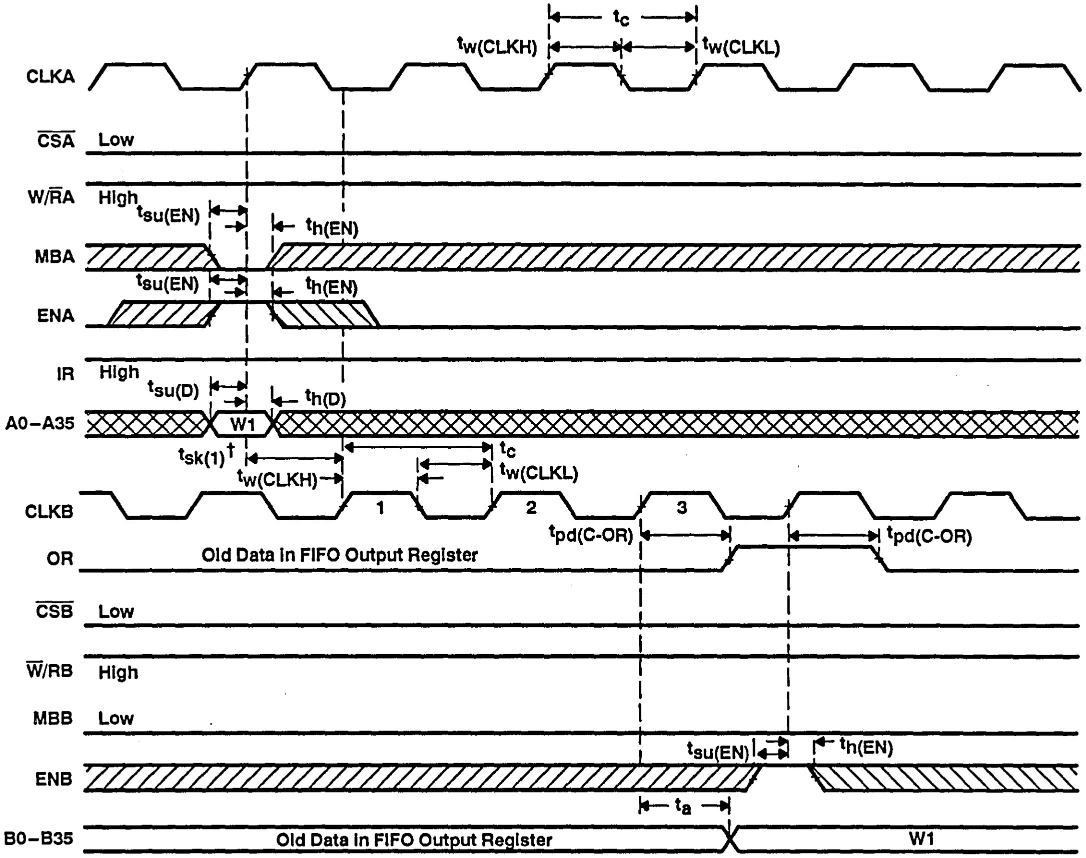
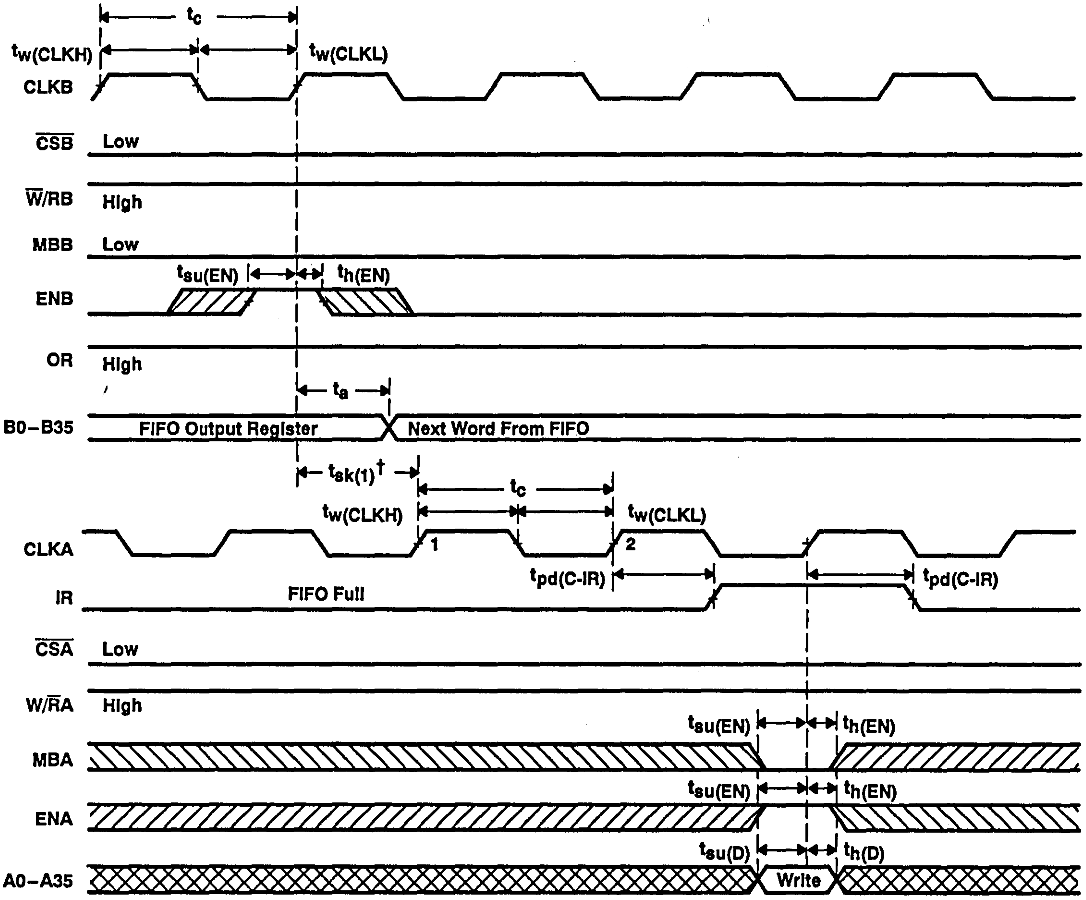


Figure 5. FIFO Read-Cycle Timing



† $t_{sk(1)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition high and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(1)}$, then the transition of OR high and the first word load to the output register can occur one CLKB cycle later than shown.

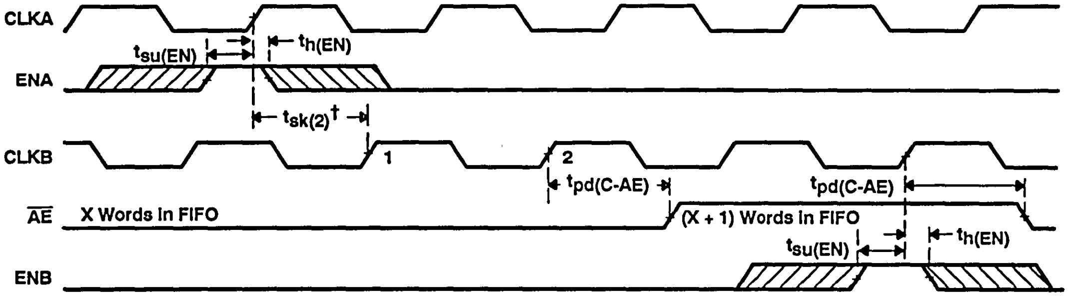
Figure 6. OR-Flag Timing and First Data Word Fallthrough When the FIFO Is Empty



† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, then IR can transition high one CLKA cycle later than shown.

Figure 7. IR-Flag Timing and First Available Write When the FIFO Is Full

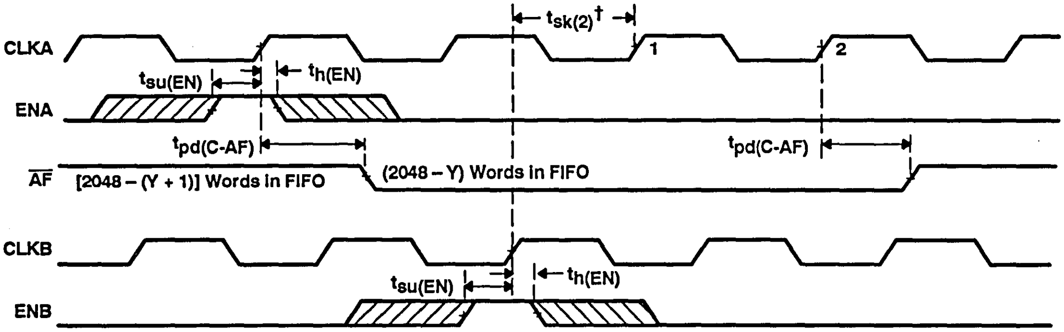
PRODUCT PREVIEW



NOTE: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(2)}$, then $\overline{AE}$ can transition high one CLKB cycle later than shown.

Figure 8. Timing for $\overline{AE}$ When FIFO Is Almost Empty



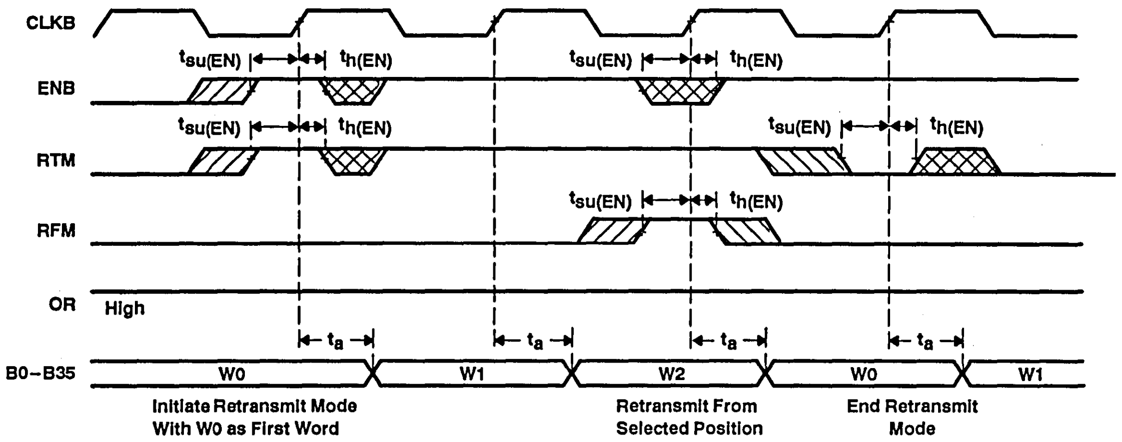
NOTE: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, then $\overline{AF}$ can transition high one CLKA cycle later than shown.

Figure 9. Timing for $\overline{AF}$ When FIFO Is Almost Full

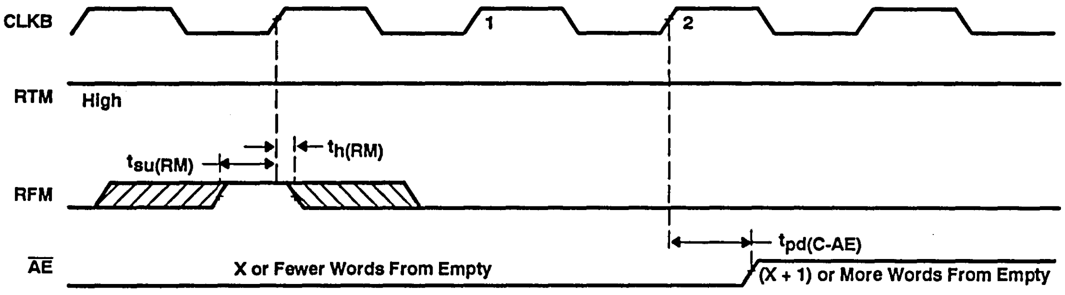
PRODUCT PREVIEW

PRODUCT PREVIEW



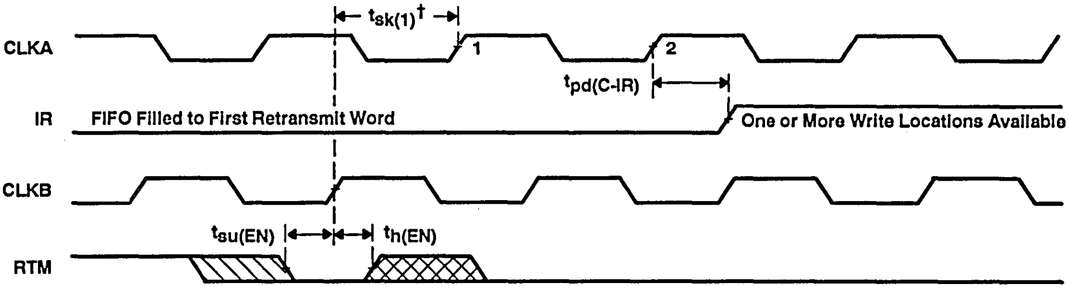
NOTE: $\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

Figure 10. Retransmit Timing Showing Minimum Retransmit Length



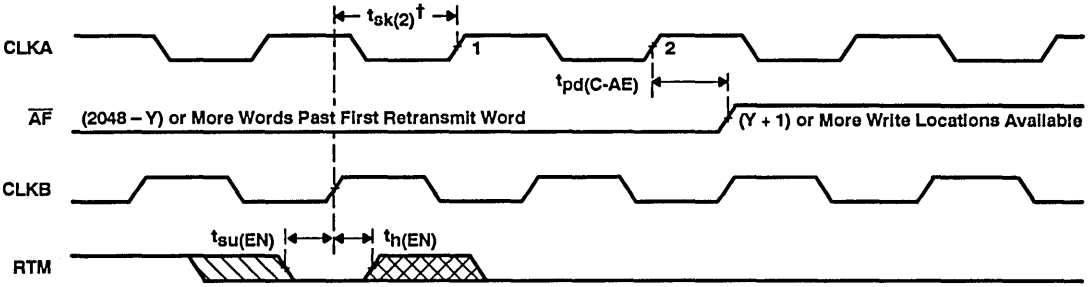
NOTE: X is the value loaded in the almost-empty flag offset register.

Figure 11. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X



† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, then IR can transition high one CLKA cycle later than shown.

Figure 12. IR Timing From the End of Retransmit Mode When One or More Write Locations Are Available



NOTE: Y is the value loaded in the almost-full flag offset register.

† $t_{sk(2)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, then $\overline{AF}$ can transition high one CLKA cycle later than shown.

Figure 13. $\overline{AF}$ Timing From the End of Retransmit Mode When (Y + 1) or More Write Locations Are Available

PRODUCT PREVIEW

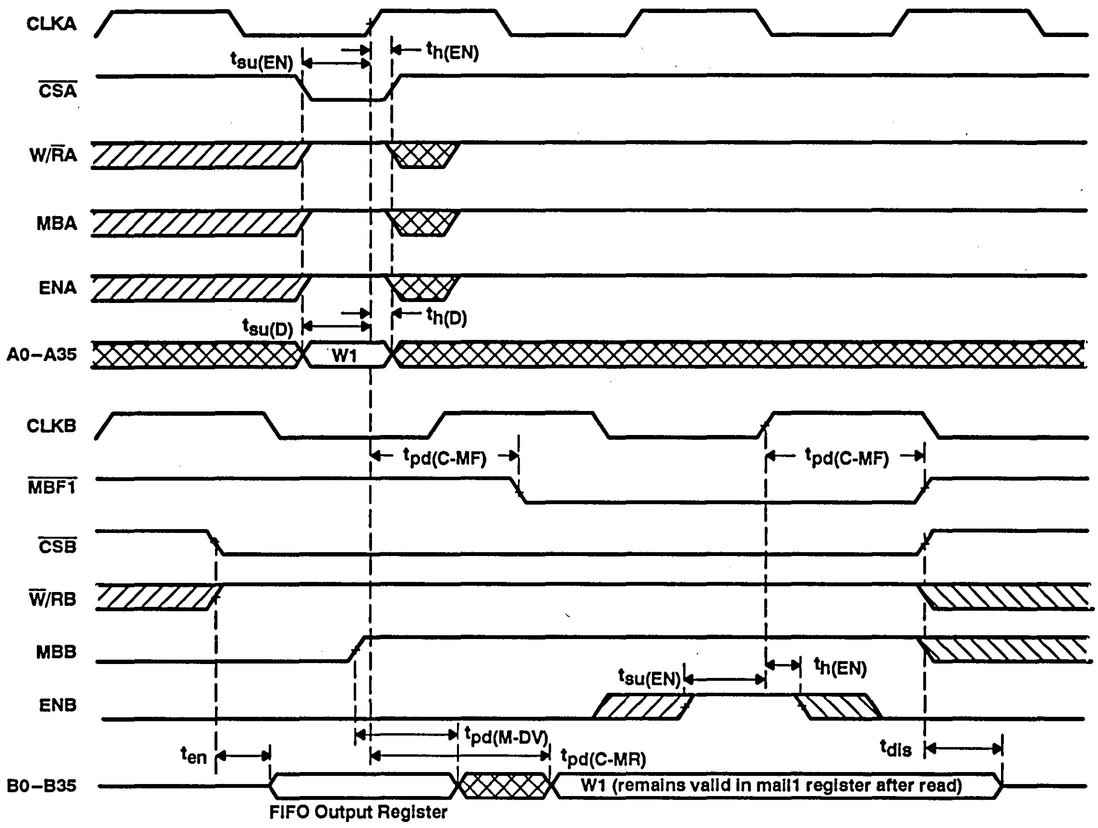


Figure 14. Timing for Mail1 Register and $\overline{MBF1}$ Flag

PRODUCT PREVIEW

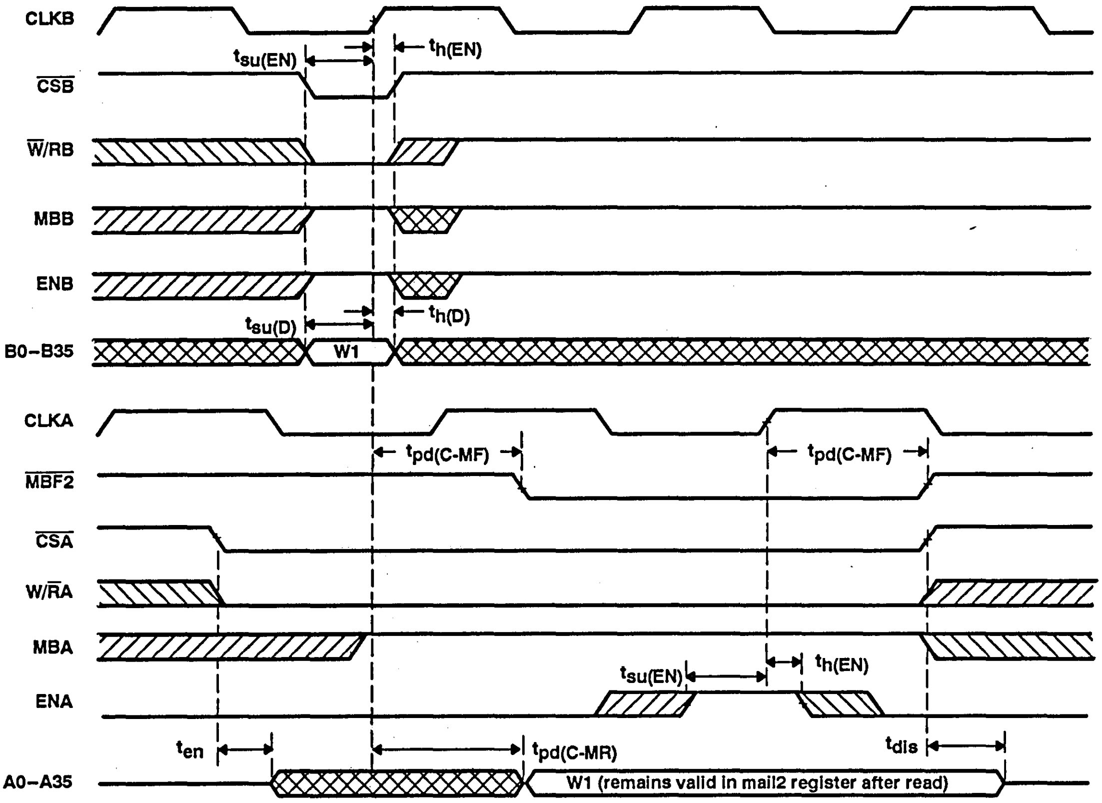


Figure 15. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±5	µA
I_{CC}	V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{\text{CSA}} = V_{IH}$	A0–A35		0		mA
			$\overline{\text{CSB}} = V_{IH}$	B0–B35		0		
			$\overline{\text{CSA}} = V_{IL}$	A0–A35			1	
			$\overline{\text{CSB}} = V_{IL}$	B0–B35			1	
			All other inputs				1	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 15)

		'ACT3651-15		'ACT3651-20		'ACT3651-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, MBB, RTM, and RFM before CLKB↑	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑[†]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{su(SD)}$[‡]	Setup time, FS0/SD before CLKA↑	4		5		6		ns
$t_{su(SEN)}$[‡]	Setup time, FS1/$\overline{SEN}$ before CLKA↑	4		5		6		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑[†]	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	2		3		3		ns
$t_{h(SP)}$[‡]	Hold time, FS1/$\overline{SEN}$ high after $\overline{RST}$ high	15		20		30		ns
$t_{h(SD)}$[‡]	Hold time, FS0/SD after CLKA↑	0		0		0		ns
$t_{h(SEN)}$[‡]	Hold time, FS1/$\overline{SEN}$ after CLKA↑	0		0		0		ns
$t_{sk(1)}$[§]	Skew time, between CLKA↑ and CLKB↑ for OR and IR	6		8		10		ns
$t_{sk(2)}$[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12		16		20		ns

[†] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[‡] Only applies when serial load method used to program flag offset registers

[§] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 30$ pF (see Figures 1 through 15)

PARAMETER		'ACT3651-15		'ACT3651-20		'ACT3651-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKB↑ to B0–B35		11		13		15	ns
$t_{pd(C-IR)}$	Propagation delay time, CLKA↑ to IR		11		13		15	ns
$t_{pd(C-OR)}$	Propagation delay time, CLKB↑ to OR		11		13		15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$		11		13		15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$		11		13		15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high		11		13		15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡		11		13		15	ns
$t_{pd(M-DV)}$	Propagation delay time, MBB to B0–B35 valid		9		11		13	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ low to $\overline{AE}$ low and $\overline{AF}$ high		15		20		30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active		10		12		14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance		10		12		14	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

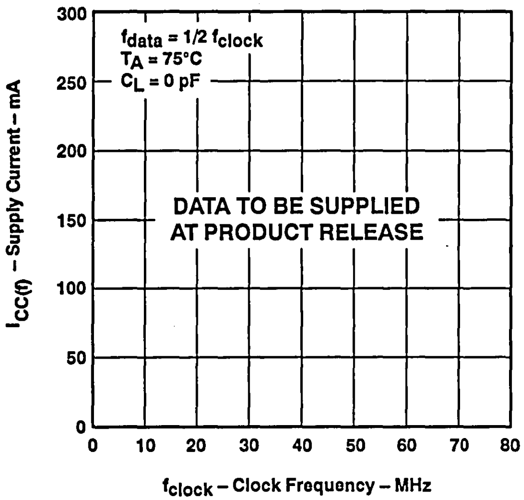


Figure 16

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 16, the maximum power dissipation (P_T) of the SN74ACT3631/3651 can be calculated by:

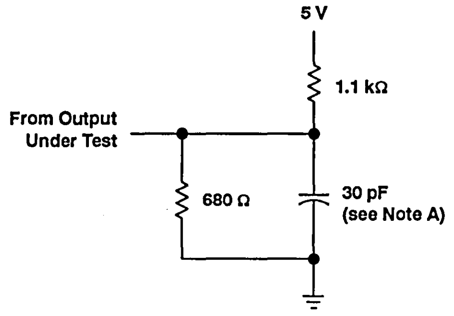
$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

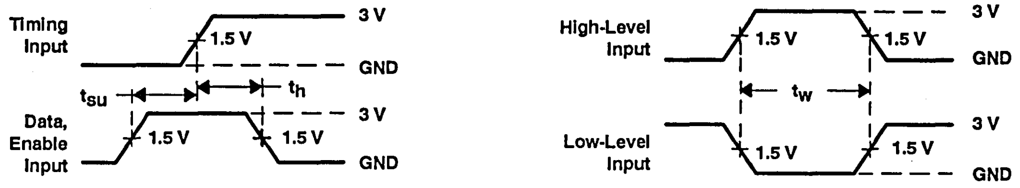
N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

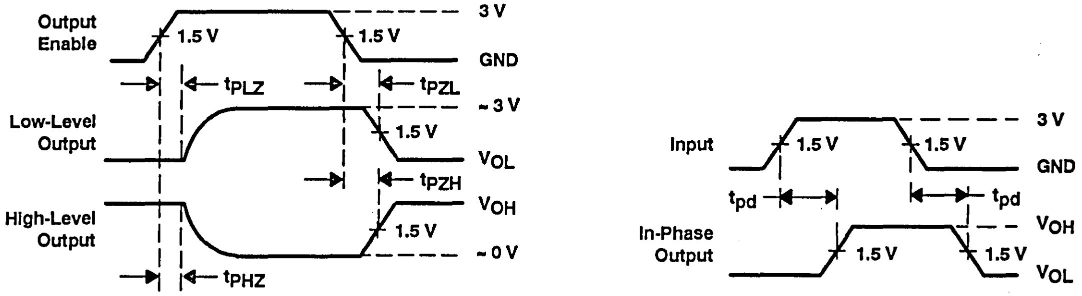


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

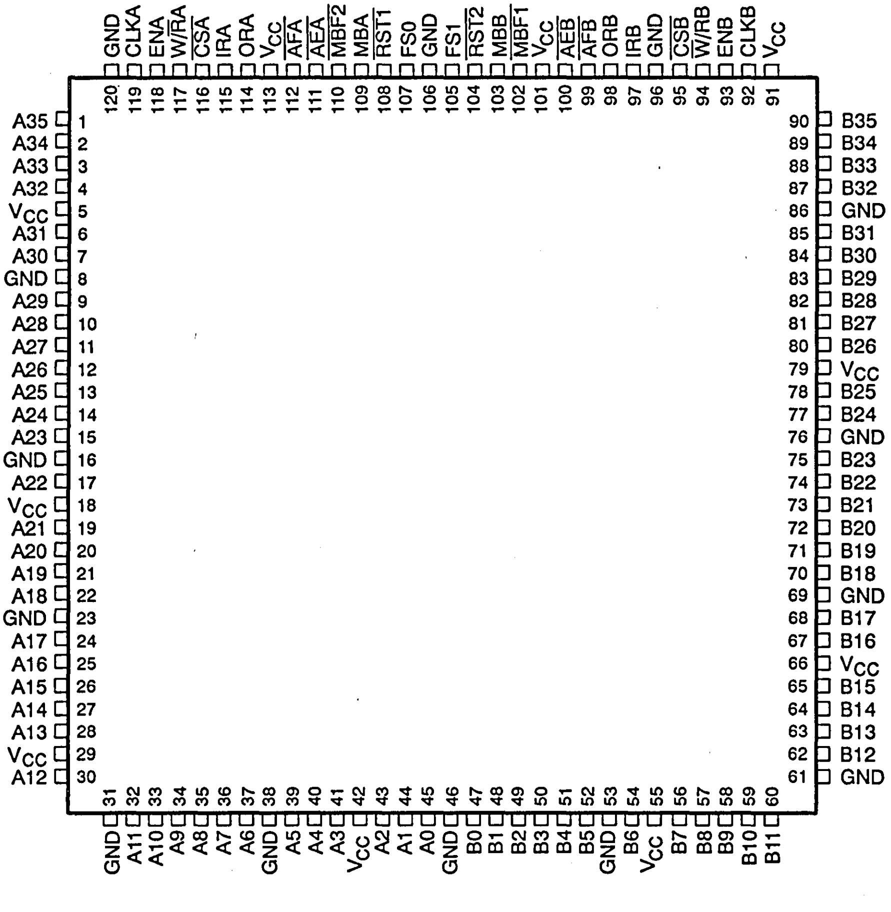
Figure 17. Load Circuit and Voltage Waveforms

SN74ACT3622
256 × 36 × 2
CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS247A – AUGUST 1993 – REVISED JUNE 1994

- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Two Independent Clocked FIFOs Buffering Data in Opposite Directions
- Mailbox Bypass Register for Each FIFO
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ Flags Synchronized by CLKA
- IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Pin-to-Pin Compatible With the SN74ACT3632 and SN74ACT3642
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)

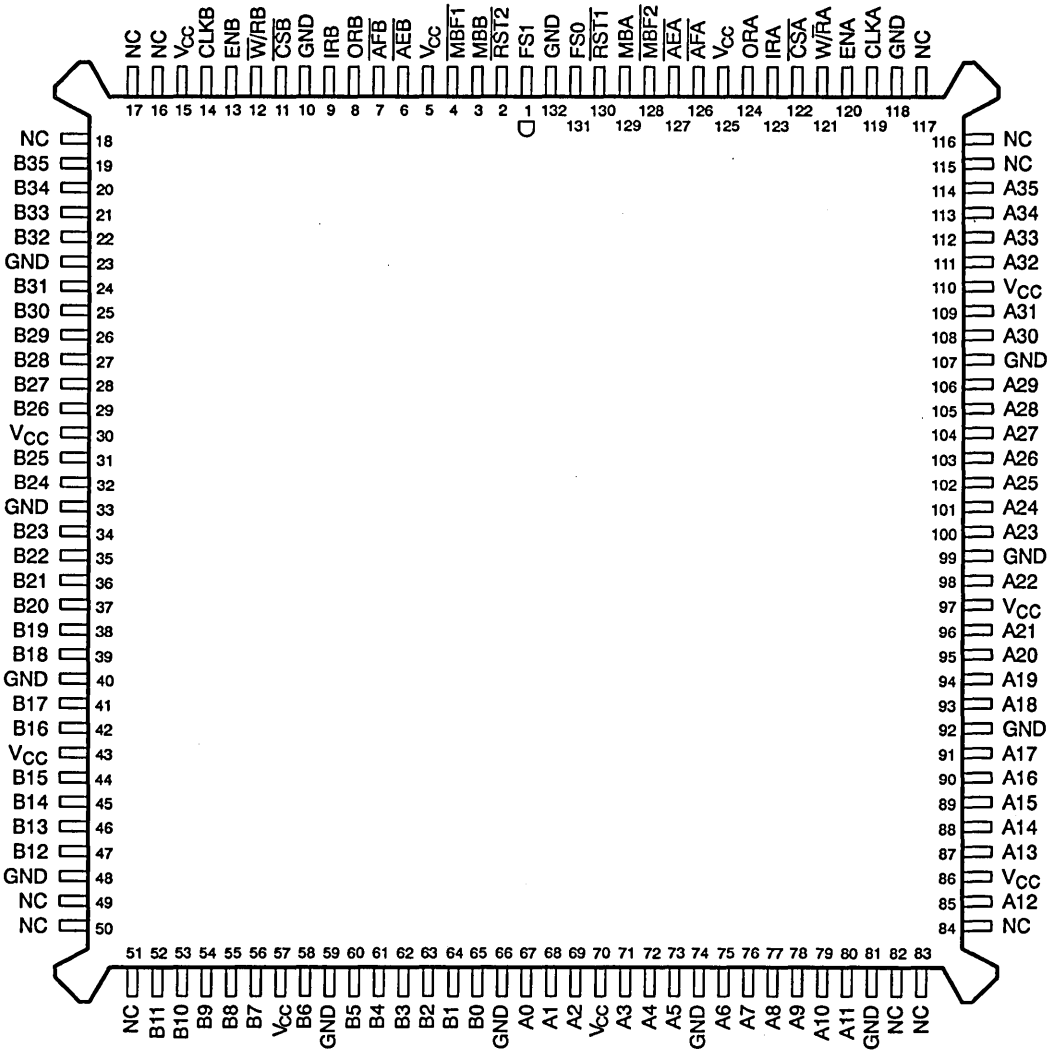
PCB PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

PRODUCT PREVIEW

description

The SN74ACT3622 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz with read access times of 11 ns. Two independent 1024 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths.

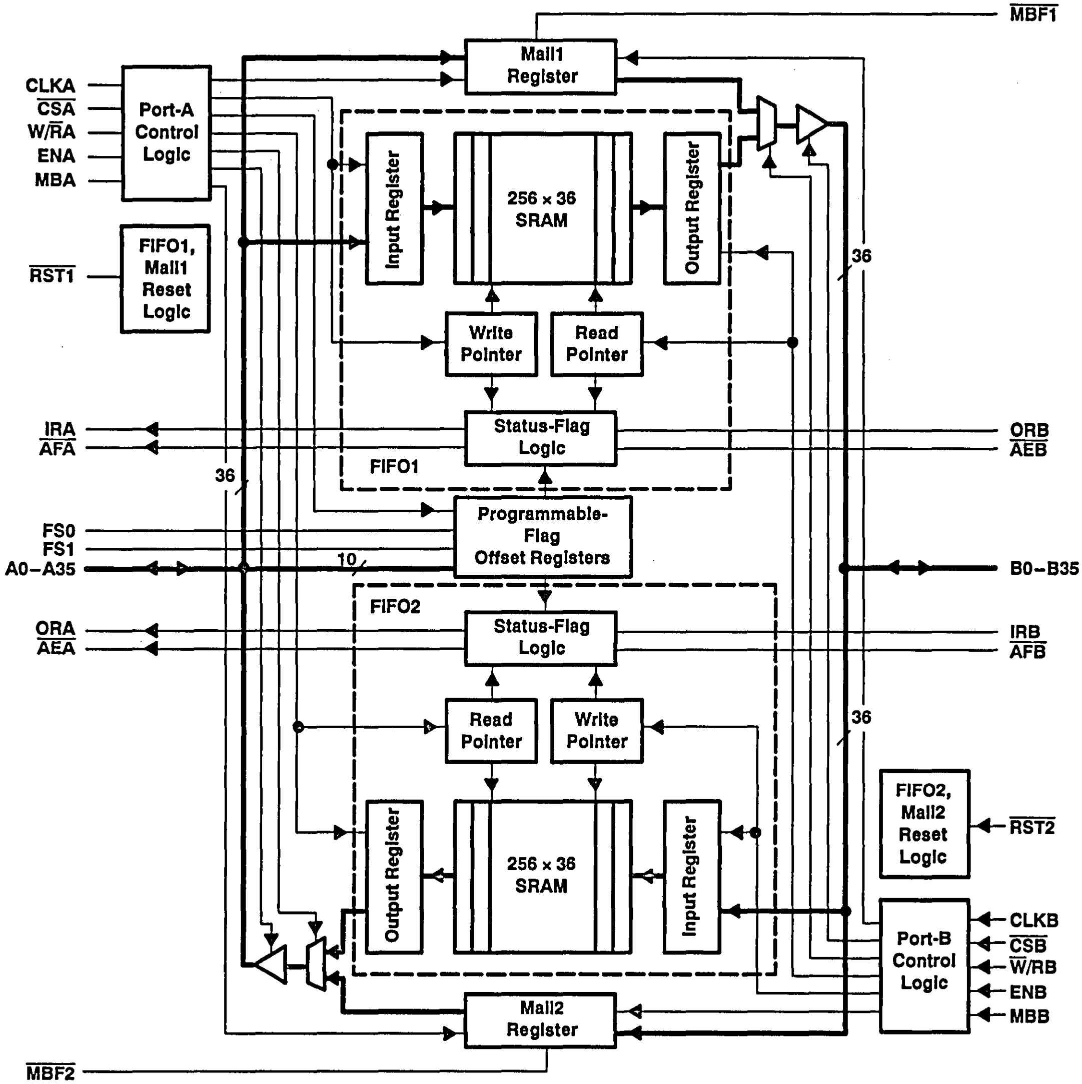
The SN74ACT3622 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input-ready (IRA, IRB) flag and almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output-ready (ORA, ORB) flag and almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the almost-full and almost-empty flags of the FIFO can be programmed from port A.

The SN74ACT3622 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AEA}}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{\text{AEA}}$ is low when the number of words in FIFO2 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{\text{AEB}}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\text{AEB}}$ is low when the number of words in FIFO1 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{\text{AFA}}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\text{AFA}}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{\text{AFB}}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{\text{AFB}}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the almost-full B offset register, Y2.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{\text{AFA}}$, and $\overline{\text{AEA}}$ are all synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{\text{AFB}}$, and $\overline{\text{AEB}}$ are synchronized to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag offset selects. The low-to-high transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO almost-full and almost-empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFOs.
IRA	O (port A)	Input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O (port B)	Input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output-register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output-register data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by a low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\text{MBF1}}$ is low. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high when FIFO1 is reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by a low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\text{MBF2}}$ is low. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is also set high when FIFO2 is reset.
ORA	O (port A)	Output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

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Terminal Functions (continued)

TERMINAL NAME	I/O	DESCRIPTION
ORB	O (port B)	Output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{\text{RST1}}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST1}}$ is low. The low-to-high transition of $\overline{\text{RST1}}$ latches the status of FS0 and FS1 for $\overline{\text{AFA}}$ and $\overline{\text{AEB}}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{\text{RST2}}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST2}}$ is low. The low-to-high transition of $\overline{\text{RST2}}$ latches the status of FS0 and FS1 for $\overline{\text{AFB}}$ and $\overline{\text{AEA}}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{\text{RA}}$	I	Port-A write/read select. A high on W/$\overline{\text{RA}}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
$\overline{\text{W}}$/RB	I	Port-B write/read select. A low on $\overline{\text{W}}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{\text{W}}$/RB is low.

detailed description

reset

The FIFO memories of the SN74ACT3622 are reset separately by taking their reset ($\overline{\text{RST1}}$, $\overline{\text{RST2}}$) inputs low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready flag (IRA, IRB) low, the output-ready flag (ORA, ORB) low, the almost-empty flag ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) low, and the almost-full flag ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) high. Resetting a FIFO also forces the mailbox flag ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) of the parallel mailbox register high. After a FIFO is reset, its input-ready flag is set high after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A low-to-high transition on a FIFO reset ($\overline{\text{RST1}}$, $\overline{\text{RST2}}$) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method (see *almost-empty and almost-full flag offset programming*).

almost-empty flag and almost-full flag offset programming

Four registers in the SN74ACT3622 are used to hold the offset values for the almost-empty and almost-full flags. The port-B almost-empty flag ($\overline{\text{AEB}}$) offset register is labeled X1 and the port-A almost-empty flag ($\overline{\text{AEA}}$) offset register is labeled X2. The port-A almost-full flag ($\overline{\text{AFA}}$) offset register is labeled Y1 and the port-B almost-full flag ($\overline{\text{AFB}}$) offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST1}}$	$\overline{\text{RST2}}$	X1 AND Y1 REGISTERS†	X2 AND Y2 REGISTERS‡
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

† X1 register holds the offset for $\overline{\text{AEB}}$; Y1 register holds the offset for $\overline{\text{AFA}}$.
‡ X2 register holds the offset for $\overline{\text{AEA}}$; Y2 register holds the offset for $\overline{\text{AFB}}$.

almost-empty flag and almost-full flag offset programming (continued)

To load a FIFO almost-empty flag and almost-full flag offset registers with one of the three preset values listed in Table 1, at least one of the flag-select inputs must be high during the low-to-high transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be high when FIFO1 reset ($\overline{\text{RST1}}$) returns high. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{\text{RST2}}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. Each offset register uses port-A inputs (A7–A0). The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 252. After all the offset registers are programmed from port A, the port-B input-ready flag (IRB) is set high and both FIFOs begin normal operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{RA}}$). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are low.

Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is high, ENA is high, MBA is low, and IRA is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is low, ENA is high, MBA is low, and ORA is high (see Table 2). FIFO reads and writes on port A are independent of any concurrent port-B operation.

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{RA}}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{\text{W}}$/RB) is the inverse of the port-A write/read select (W/$\overline{\text{RA}}$). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select ($\overline{\text{W}}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ is high or $\overline{\text{W}}$/RB is low. The B0–B35 outputs are active when $\overline{\text{CSB}}$ is low and $\overline{\text{W}}$/RB is high.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is low, ENB is high, MBB is low, and IRB is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is high, ENB is high, MBB is low, and ORB is high (see Table 3). FIFO reads and writes on port B are independent of any concurrent port-A operation.

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FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	W/$\overline{\text{RB}}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

The setup and hold time constraints to the port clocks for the port chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select may change states during the setup and hold time window of the cycle.

When a FIFO output-ready flag is low, the next data word is sent to the FIFO output register automatically by the low-to-high transition of the port clock that sets the output-ready flag high. When the output-ready flag is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port's chip select, write/read select, enable, and mailbox select.

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). ORA, $\overline{\text{AEA}}$, IRA, and $\overline{\text{AFA}}$ are synchronized to CLKA. ORB, $\overline{\text{AEB}}$, IRB, and $\overline{\text{AFB}}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1[†‡]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	ORB	$\overline{\text{AEB}}$	$\overline{\text{AFA}}$	IRA
0	L	L	H	H
1 to X1	H	L	H	H
(X1 + 1) to [256 – (Y1 + 1)]	H	H	H	H
(256 – Y1) to 255	H	H	L	H
256	H	H	L	L

[†] X1 is the almost-empty offset for FIFO1 used by $\overline{\text{AEB}}$. Y1 is the almost-full offset for FIFO1 used by $\overline{\text{AFA}}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.

[‡] When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

synchronized FIFO flags (continued)

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2†‡	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORA	$\overline{AEA}$	$\overline{AFB}$	IRB
0	L	L	H	H
1 to X2	H	L	H	H
(X2 + 1) to [256 – (Y2 + 1)]	H	H	H	H
(256 – Y2) to 255	H	H	L	H
256	H	H	L	L

† X2 is the almost-empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the almost-full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

output-ready flags (ORA, ORB)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the output-ready flag synchronizing clock; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of the synchronizing clock occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on an output-ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

input-ready flags (IRA, IRB)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the input-ready flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the input-ready flag synchronizing clock; therefore, an input-ready flag is low if less than two cycles of the input-ready flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the input-ready flag synchronizing clock after the read sets the input-ready flag high.

A low-to-high transition on an input-ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-empty flag is low when its FIFO contains X or less words and is high when its FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for its almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-full flag is low when the number of words in its FIFO is greater than or equal to (256 – Y). An almost-full flag is high when the number of words in its FIFO is less than or equal to [256 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for its almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [256 – (Y + 1)] or less words remains low if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [256 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [256 – (Y + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [256 – (Y + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port mailbox select input is low and from the mail register when the port-mailbox select input is high. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

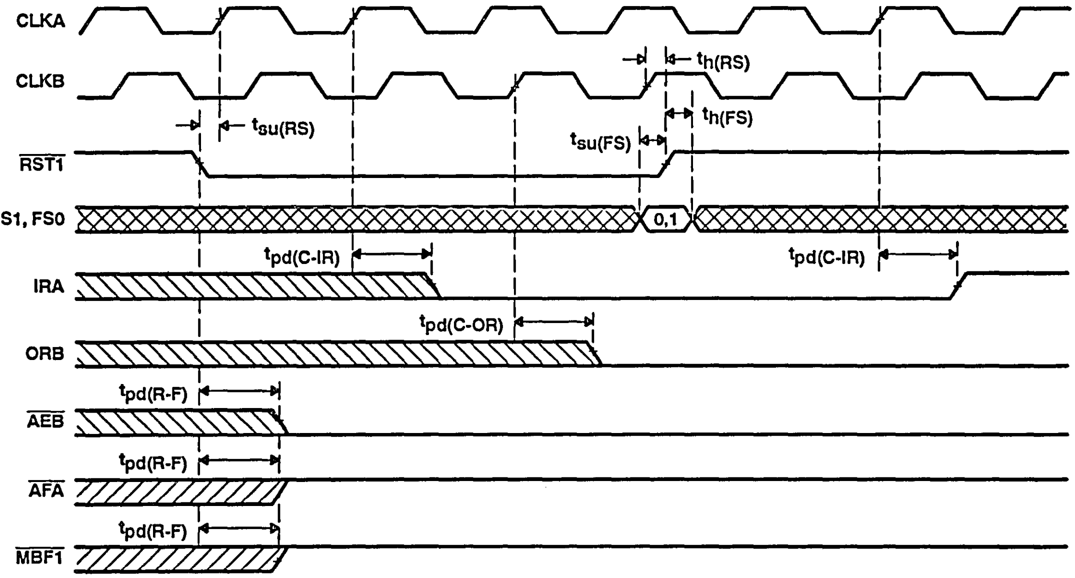
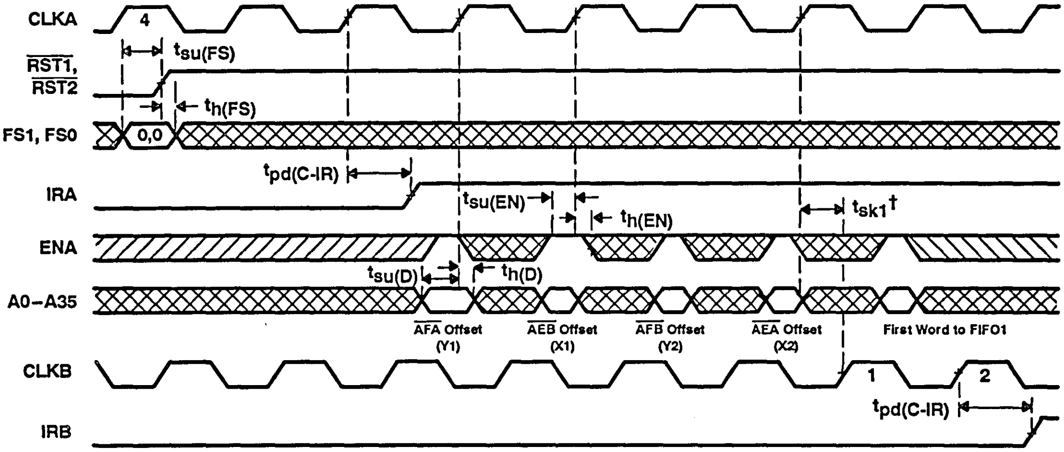


Figure 1. FIFO1 Reset Loading X1 and Y1 With a Preset Value of Eight†

† FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



† t_{sk1} is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition high in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{sk1}, then IRB may transition high one cycle later than shown.

NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values After Reset

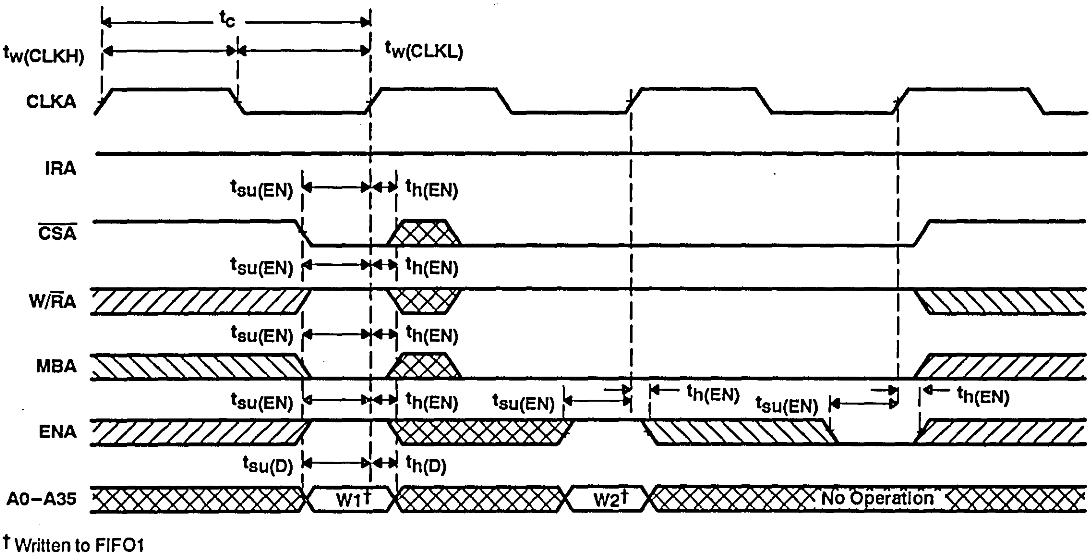


Figure 3. Port-A Write Cycle Timing for FIFO1

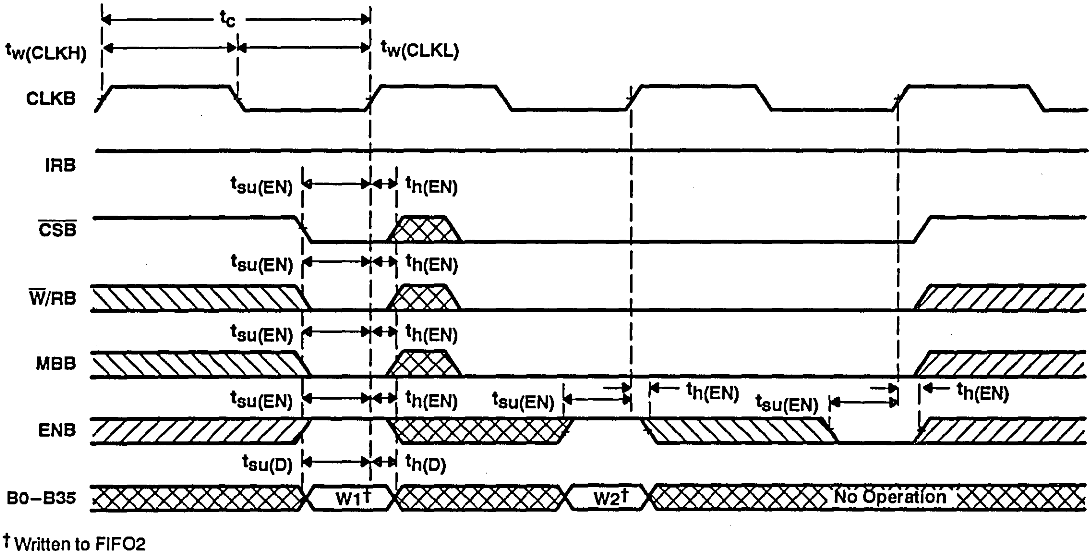


Figure 4. Port-B Write Cycle Timing for FIFO2

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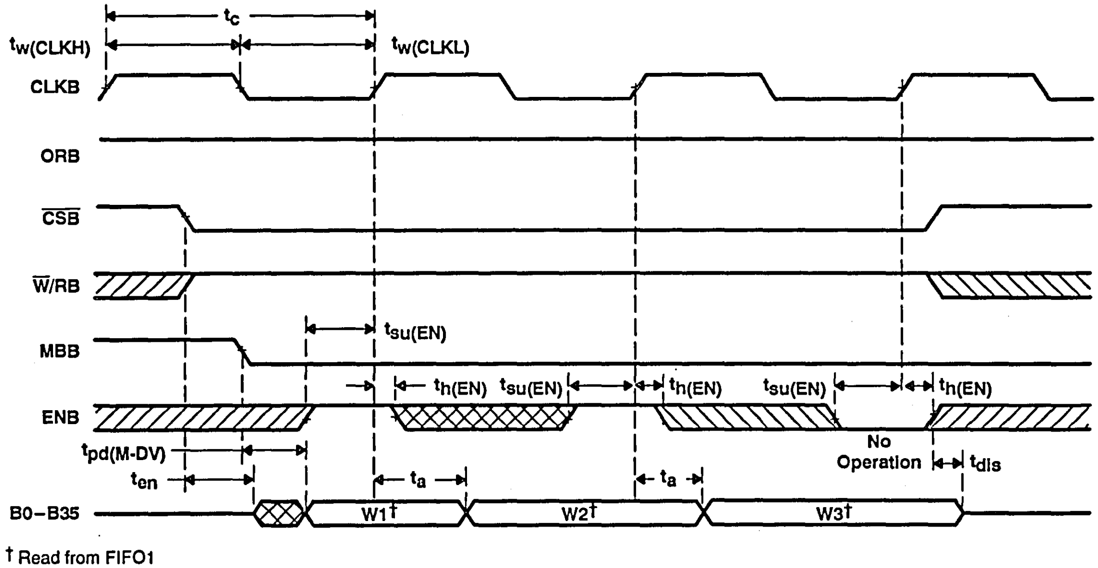
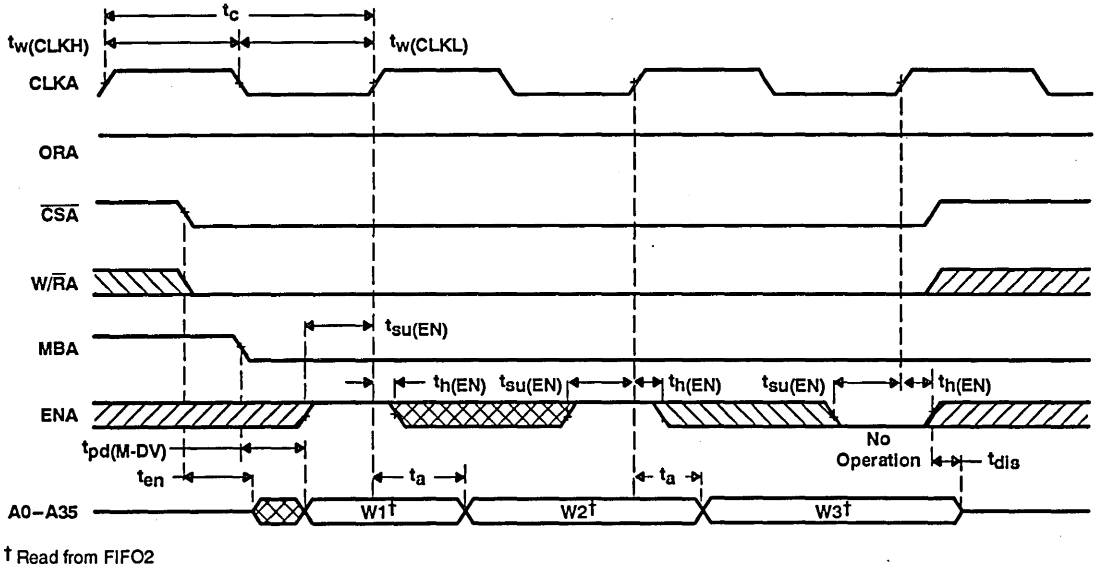


† Read from FIFO1

Figure 5. Port-B Read Cycle Timing for FIFO1



† Read from FIFO2

Figure 6. Port-A Read Cycle Timing for FIFO2

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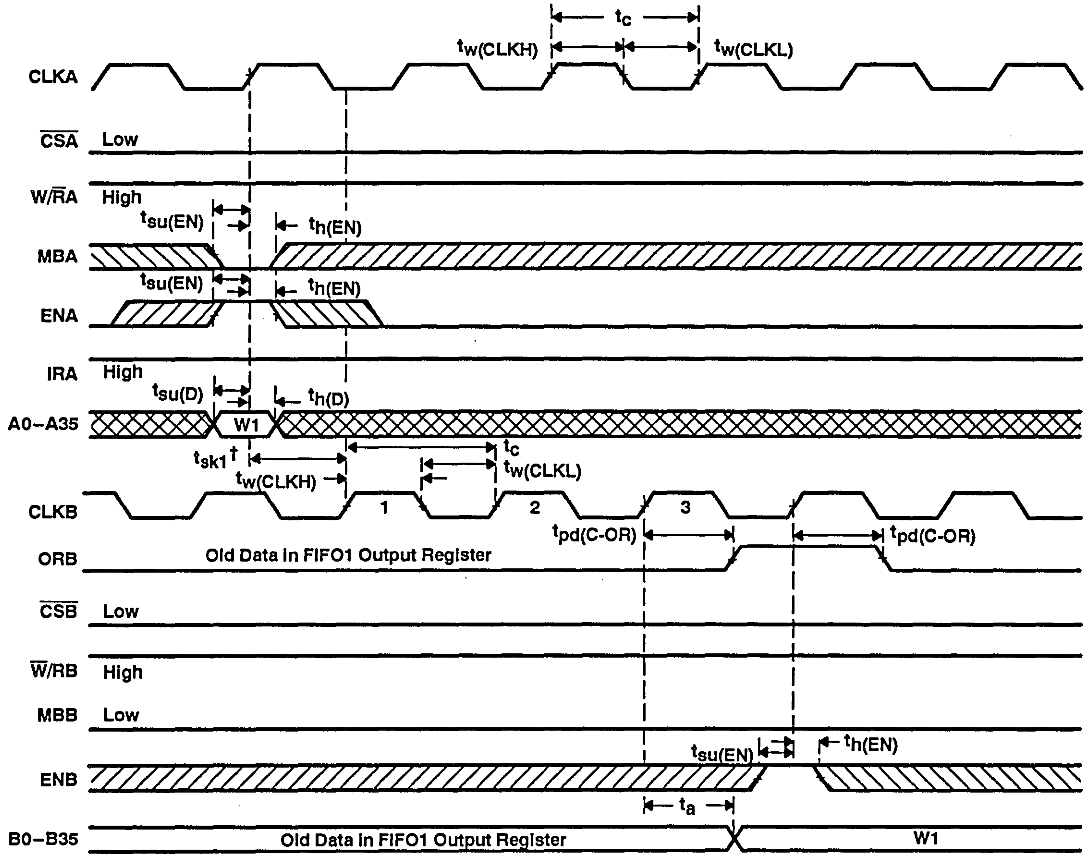
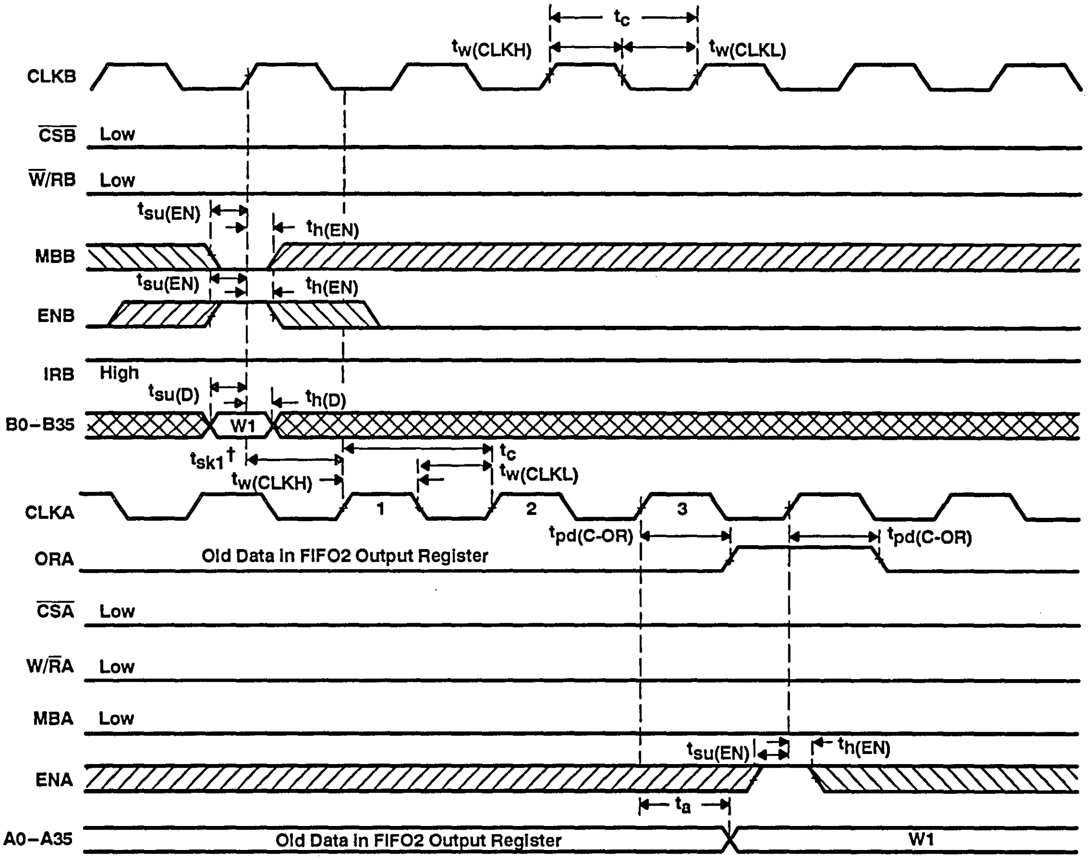


† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 7. ORB-Flag Timing and First Data Word Fallthrough When FIFO1 Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 8. ORA-Flag Timing and First Data Word Fallthrough When FIFO2 Is Empty

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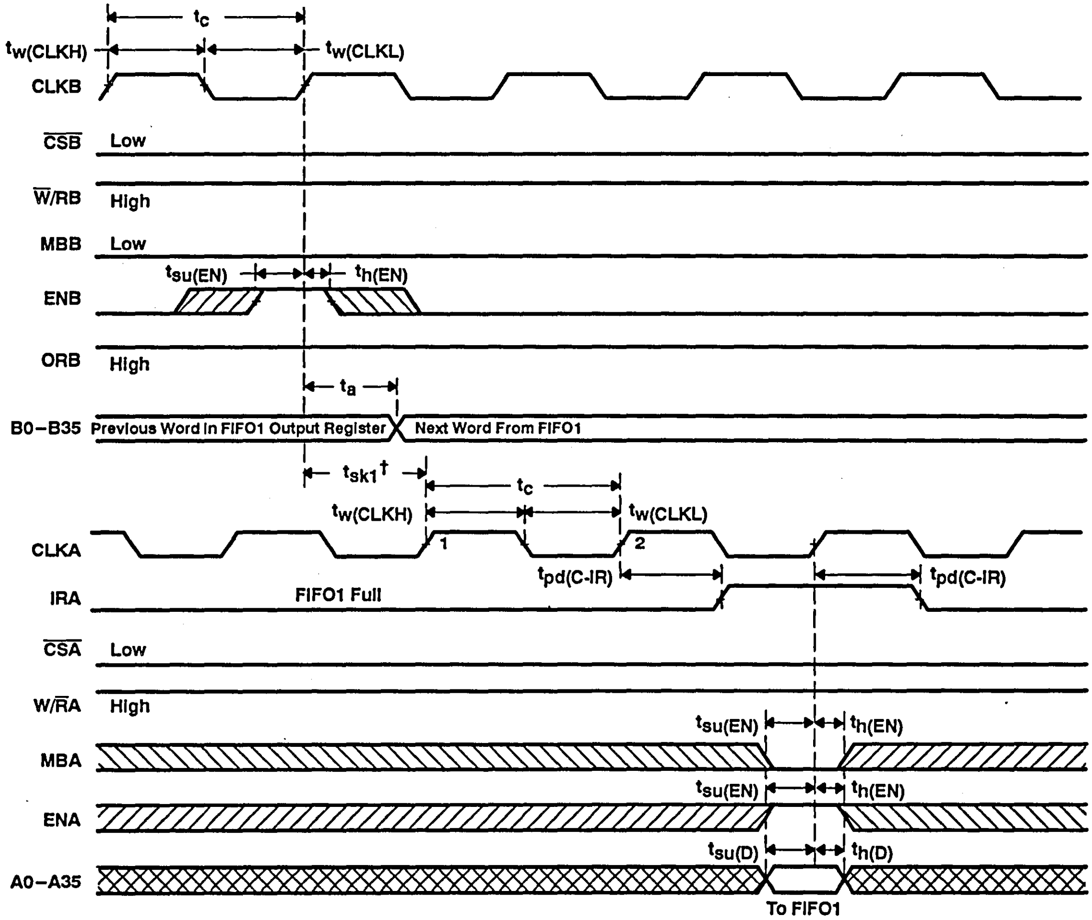
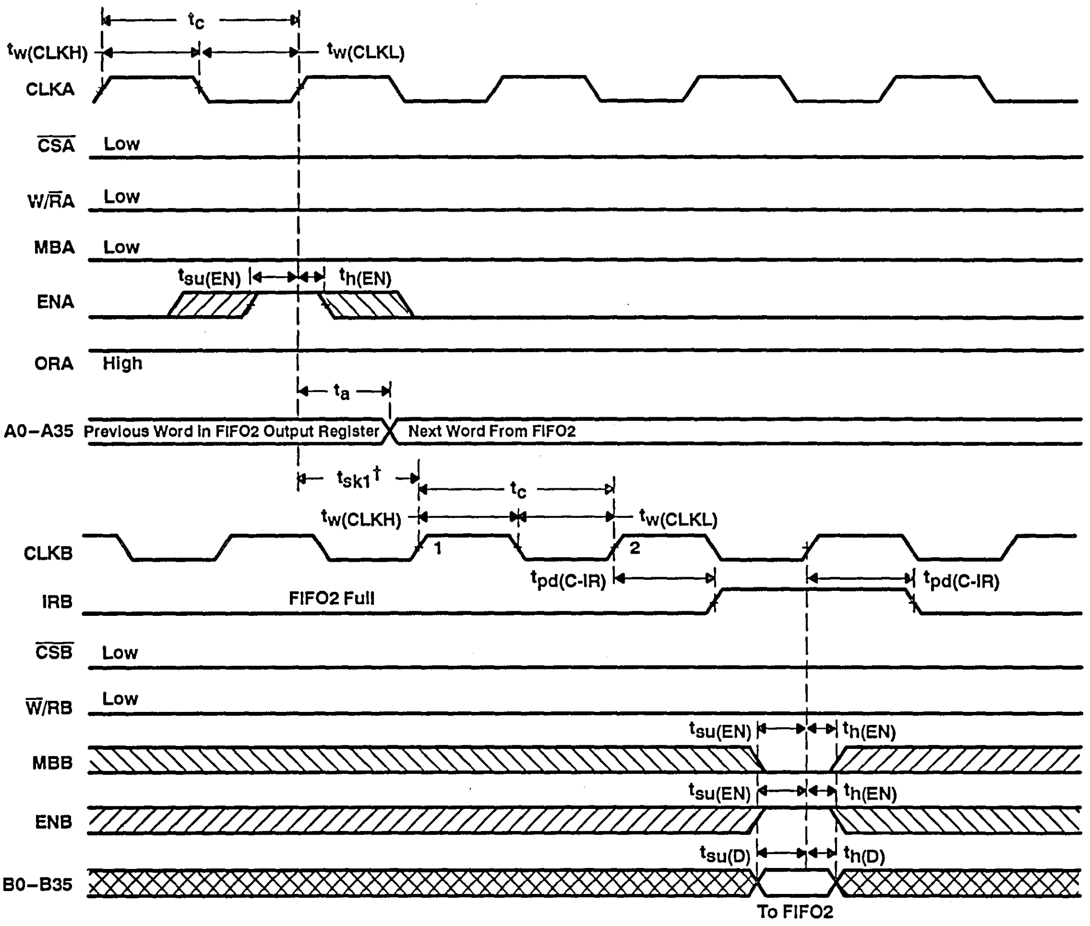


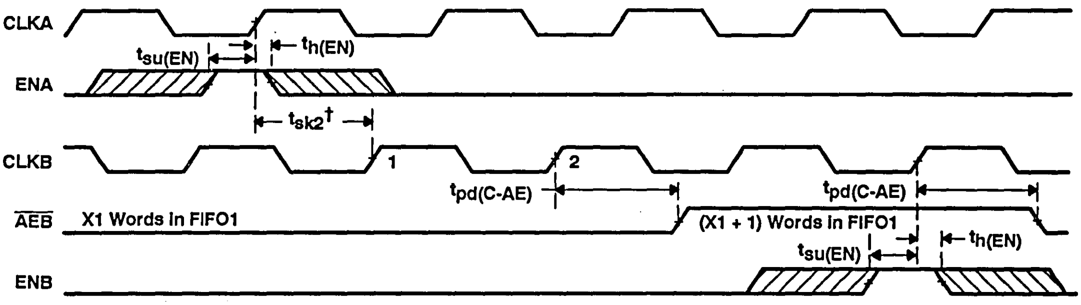
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then IRA may transition high one CLKA cycle later than shown.

Figure 9. IRA-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then IRB may transition high one CLKB cycle later than shown.

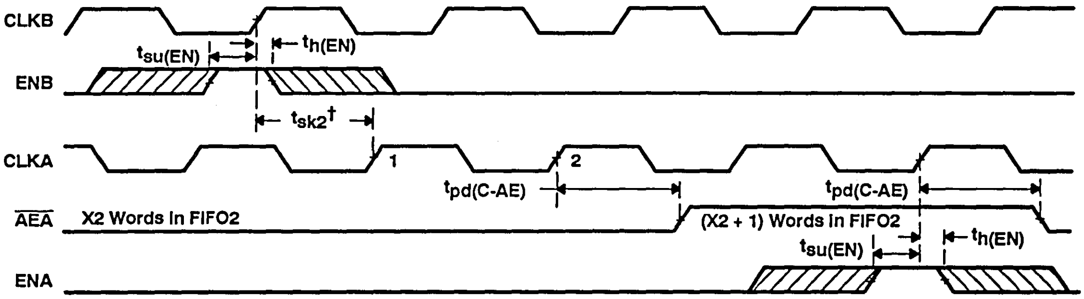
Figure 10. IRB-Flag Timing and First Available Write When FIFO2 Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

Figure 11. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty

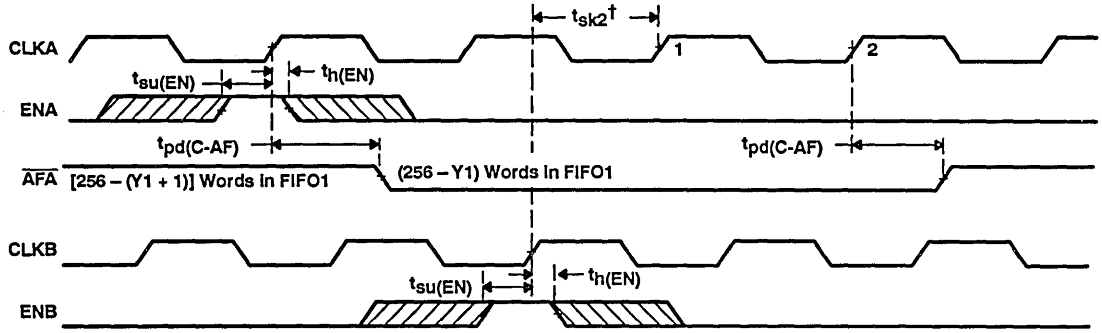


† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB = L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 12. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty

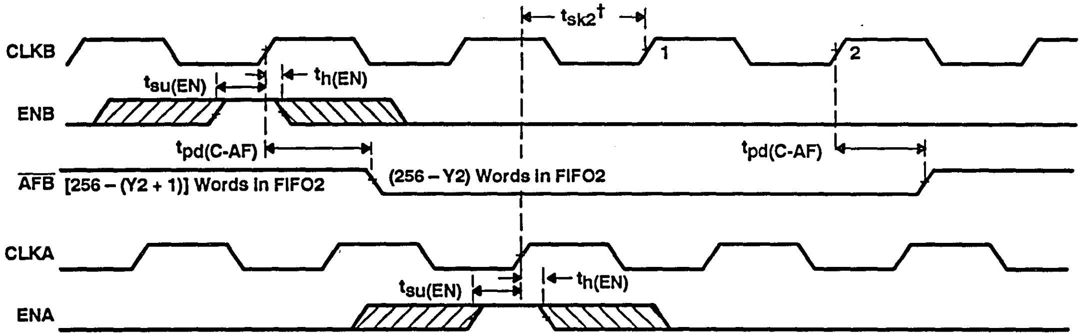
PRODUCT PREVIEW



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{\text{AFA}}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{\text{AFA}}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = H, MBA = L), FIFO1 read ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

Figure 13. Timing for $\overline{\text{AFA}}$ When FIFO1 Is Almost Full



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{\text{AFB}}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{\text{AFB}}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB= L, MBB = L), FIFO2 read ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 14. Timing for $\overline{\text{AFB}}$ When FIFO2 Is Almost Full

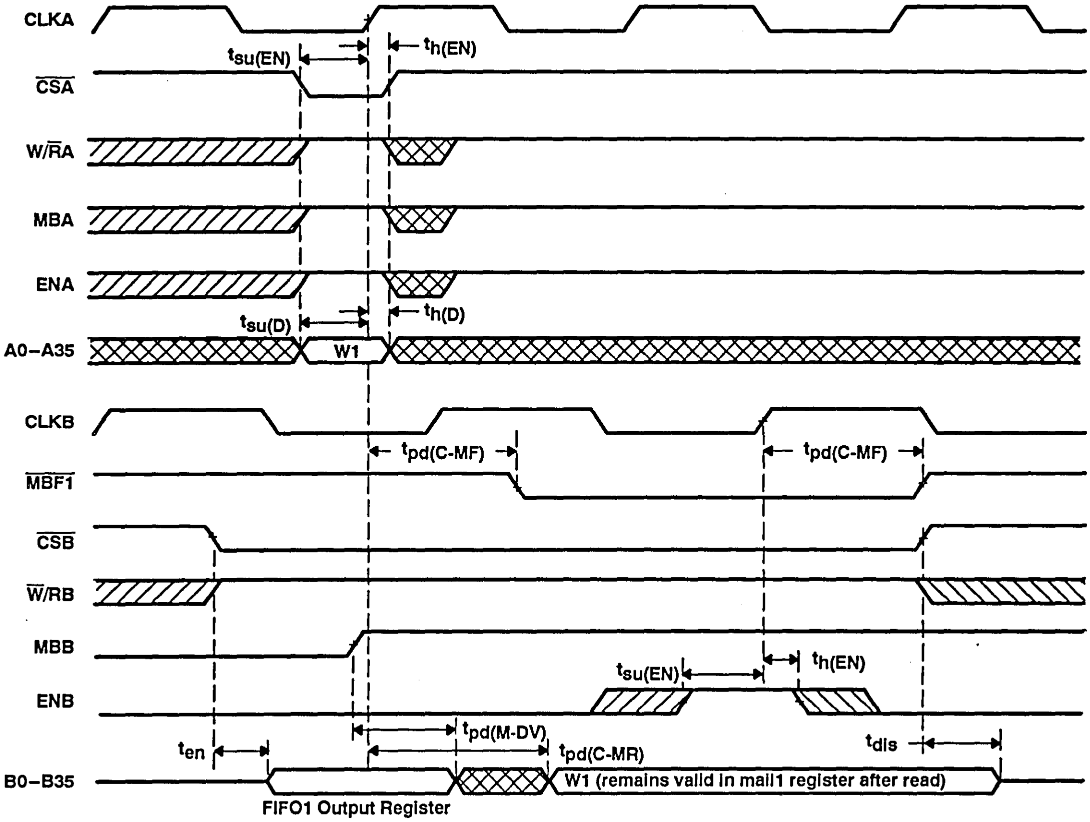


Figure 15. Timing for Mail1 Register and $\overline{MBF1}$ Flag

PRODUCT PREVIEW

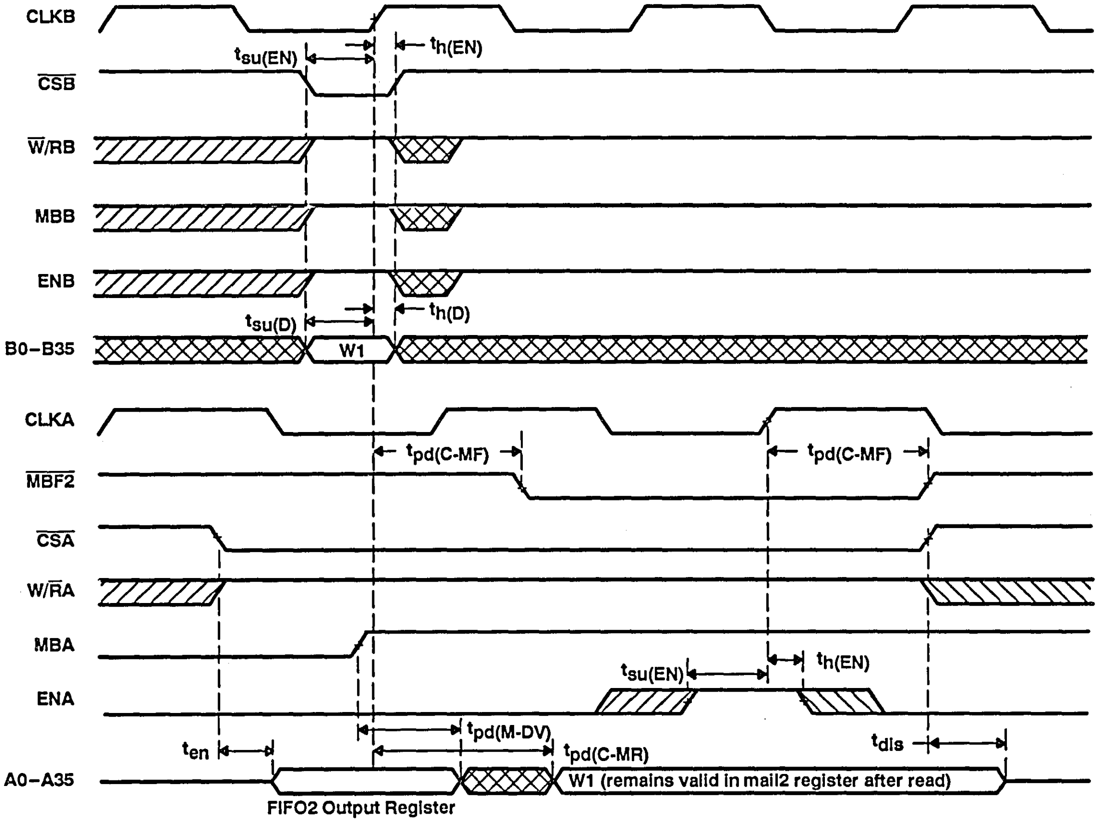


Figure 16. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP[†]	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±5	μA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±5	μA
I_{CC}	V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0					400	μA
ΔI_{CC}[‡]	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{\text{CSA}}$ = V_{IH}	A0–A35		0		mA
			$\overline{\text{CSB}}$ = V_{IH}	B0–B35		0		
			$\overline{\text{CSA}}$ = V_{IL}	A0–A35			1	
			$\overline{\text{CSB}}$ = V_{IL}	B0–B35			1	
			All other inputs				1	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 16)

		'ACT3622-15		'ACT3622-20		'ACT3622-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		10		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		10		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, ENA, and MBA before CLKA↑; $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, ENB, and MBB before CLKB↑	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RST1}}$ or $\overline{\text{RST2}}$ low before CLKA↑ or CLKB↑[§]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN)}$	Hold time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, ENA, and MBA after CLKA↑; $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{\text{RST1}}$ or $\overline{\text{RST2}}$ low after CLKA↑ or CLKB↑[§]	4		4		5		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ high	2		3		3		ns
t_{sk1}[¶]	Skew time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	6		8		10		ns
t_{sk2}[¶]	Skew time, between CLKA↑ and CLKB↑ for $\overline{\text{AEA}}$, $\overline{\text{AEB}}$, $\overline{\text{AFA}}$, and $\overline{\text{AFB}}$	12		16		20		ns

[§] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[¶] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 16)

PARAMETER		'ACT3622-15		'ACT3622-20		'ACT3622-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35		11		13		15	ns
$t_{pd(C\text{-}IR)}$	Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB		11		13		15	ns
$t_{pd(C\text{-}OR)}$	Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB		11		13		15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{\text{AEA}}$ and CLKB↑ to $\overline{\text{AEB}}$		11		13		15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\text{AFA}}$ and CLKB↑ to $\overline{\text{AFB}}$		11		13		15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\text{MBF1}}$ low or $\overline{\text{MBF2}}$ high and CLKB↑ to $\overline{\text{MBF2}}$ low or $\overline{\text{MBF1}}$ high		11		13		15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡		11		13		15	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid		9		11		13	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\text{RST1}}$ low to $\overline{\text{AEB}}$ low, $\overline{\text{AFA}}$ high, and $\overline{\text{MBF1}}$ high, and $\overline{\text{RST2}}$ low to $\overline{\text{AEA}}$ low, $\overline{\text{AFB}}$ high, and $\overline{\text{MBF2}}$ high		15		20		30	ns
t_{en}	Enable time, $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ low to A0–A35 active and $\overline{\text{CSB}}$ low and $\overline{\text{W}}$/RB high to B0–B35 active		10		12		14	ns
t_{dis}	Disable time, $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ high to A0–A35 at high impedance and $\overline{\text{CSB}}$ high or $\overline{\text{W}}$/RB low to B0–B35 at high impedance		10		12		14	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs CLOCK FREQUENCY

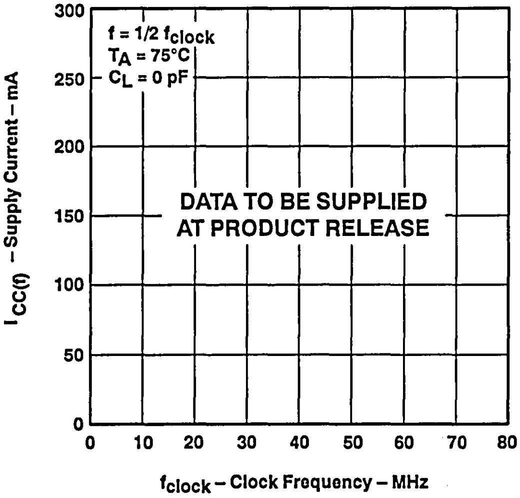


Figure 17

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 17, the maximum power dissipation (P_T) of the SN74ACT3622 can be calculated by:

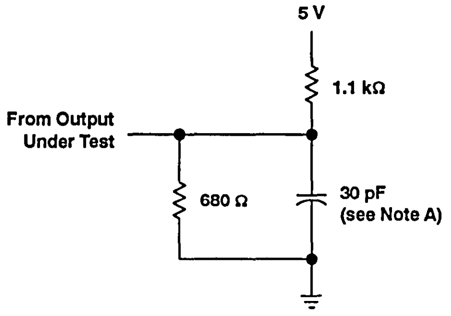
$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

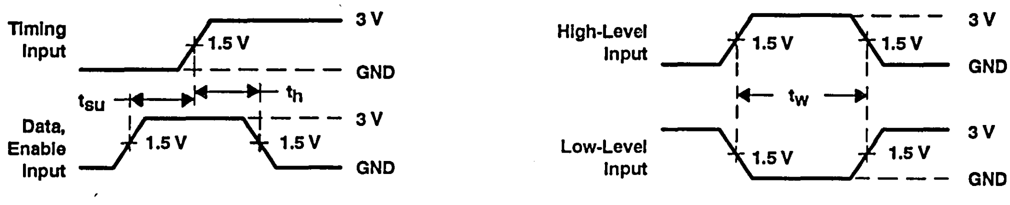
N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

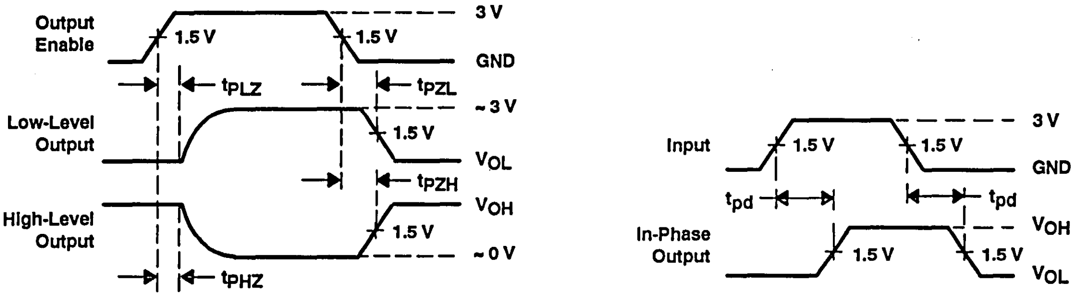


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

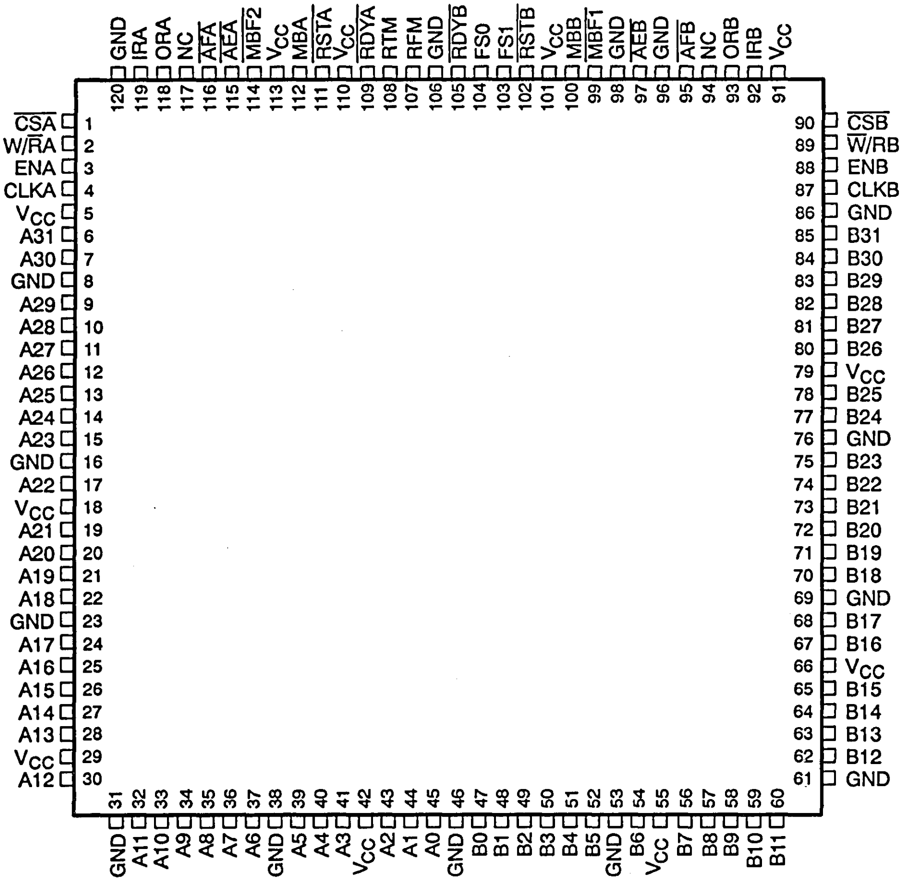
Figure 18. Load Circuit and Voltage Waveforms

SN74ACT3638
512 × 32 × 2 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS228B – JUNE 1992 – REVISED JUNE 1994

- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Two Independent 512 × 32 Clocked FIFOs Buffering Data in Opposite Directions
- Read Retransmit Capability From FIFO on Port B
- Mailbox Bypass Register for Each FIFO
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA
- IRB, ORB, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Quad Flat Package (PQ)

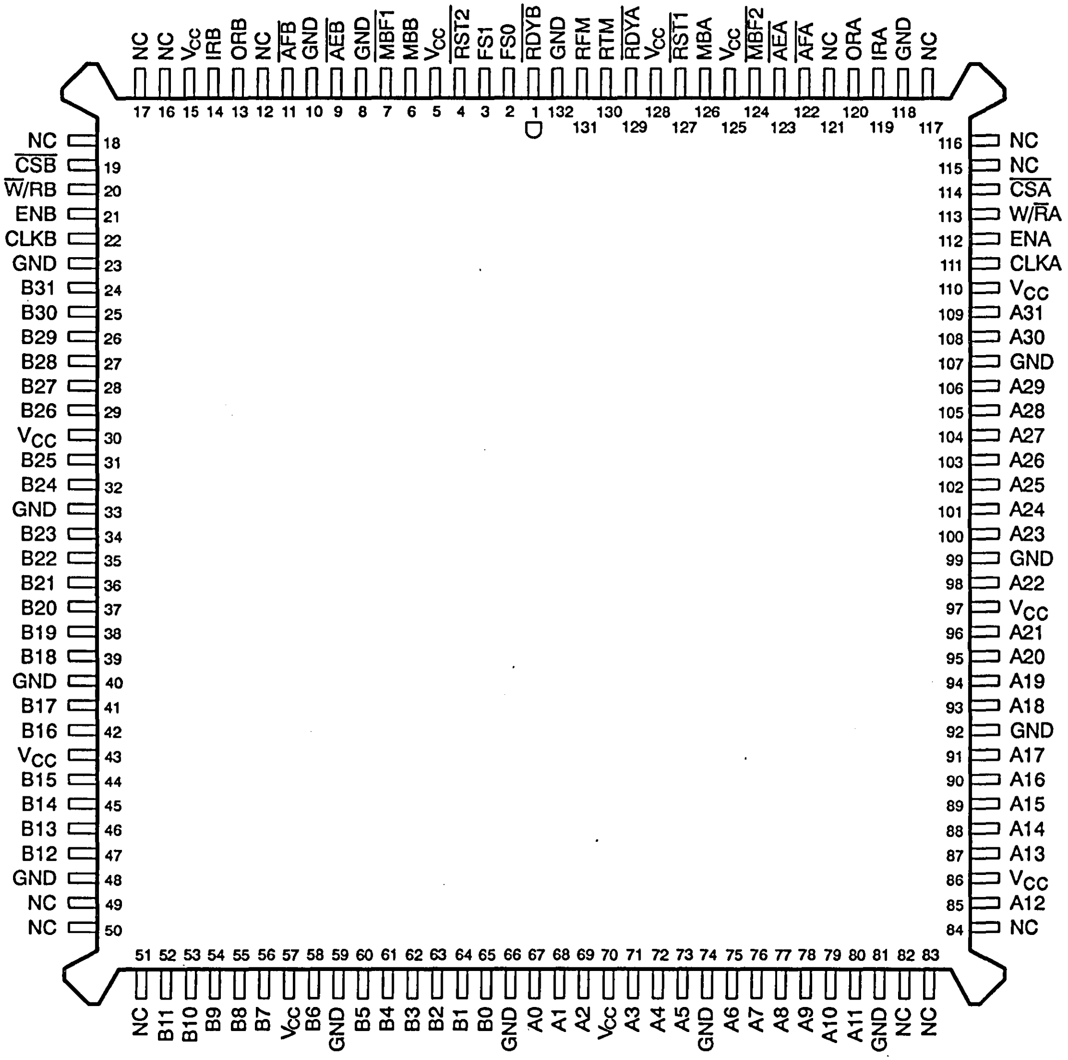
PCB PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

description

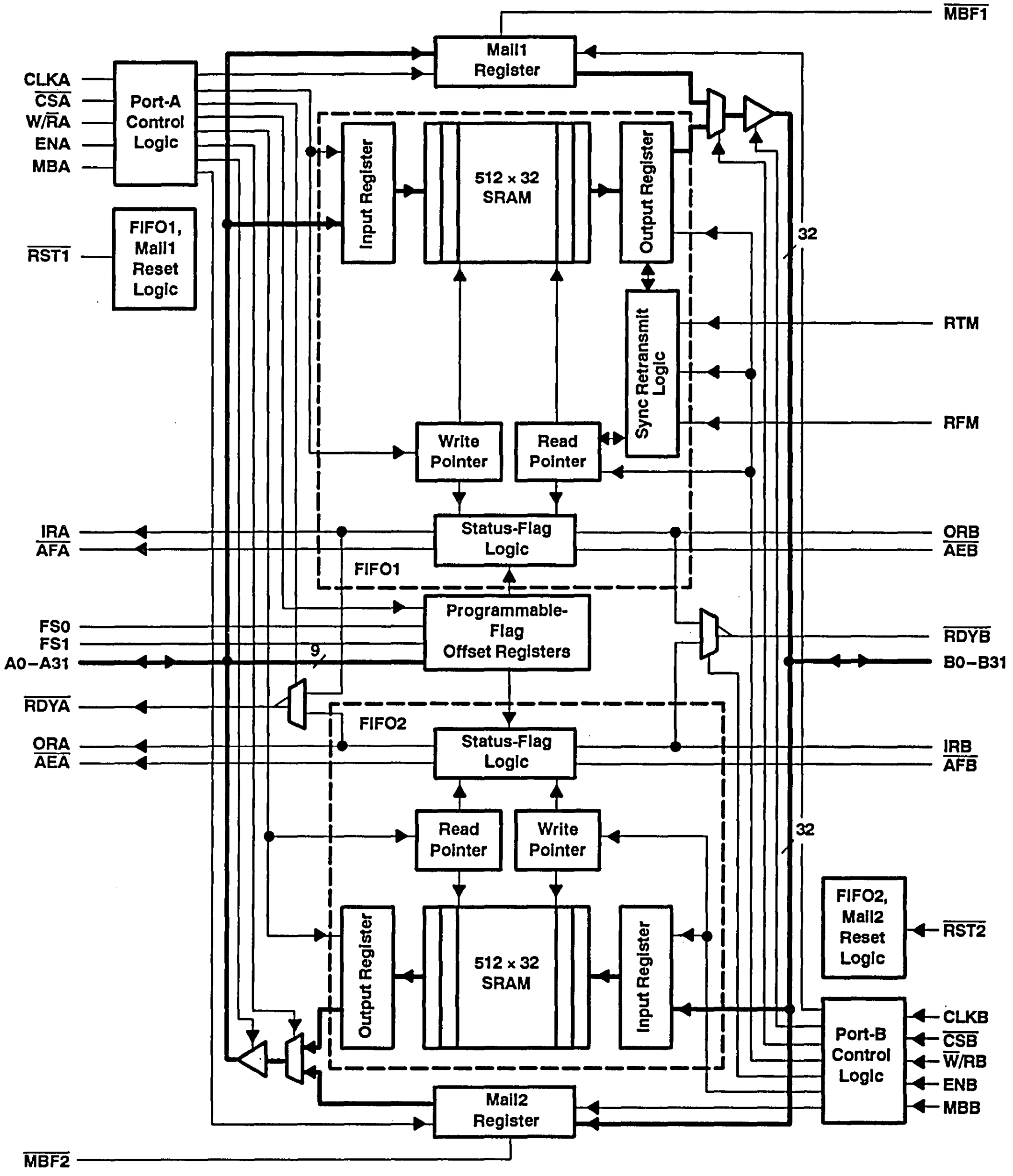
The SN74ACT3638 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 11 ns. Two independent 512 × 32 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. The FIFO memory buffering data from port A to port B has retransmit capability, which allows previously read data to be accessed again. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 32-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths.

The SN74ACT3638 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input-ready (IRA, IRB) flags and almost-full ($\overline{AFA}$, $\overline{AFB}$) flags of the SN74ACT3638 are two-stage synchronized to the port clock that writes data to its array. The output-ready (ORA, ORB) flags and almost-empty ($\overline{AEA}$, $\overline{AEB}$) flags of the SN74ACT3638 are two-stage synchronized to the port clock that reads data from its array. Offsets for the almost-full and almost-empty flags of both FIFOs can be programmed from port A.

The SN74ACT3638 is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A31	I/O	Port-A data. The 32-bit bidirectional data port for side A.
$\overline{\text{AEA}}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{\text{AEA}}$ is low when the number of words in FIFO2 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{\text{AEB}}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\text{AEB}}$ is low when the number of words in FIFO1 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{\text{AFA}}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\text{AFA}}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{\text{AFB}}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{\text{AFB}}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the almost full B offset register, Y2.
B0–B31	I/O	Port-B data. The 32-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{\text{AFA}}$, and $\overline{\text{AEA}}$ are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{\text{AFB}}$, and $\overline{\text{AEB}}$ are synchronous to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A31 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B31 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag-offset selects. The low-to-high transition of a FIFO reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO almost-full and almost-empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFOs.
IRA	O (port A)	Port-A input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. When FIFO1 is in retransmit mode, IRA indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O (port B)	Port-B input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A31 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output-register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B31 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output-register data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\text{MBF1}}$ is low. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high when FIFO1 is reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\text{MBF2}}$ is low. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is set high when FIFO2 is reset.
ORA	O (port A)	Port-A output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
ORB	O (port B)	Port-B output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
RDYA	O (port A)	Port-A ready. A high on W/RA selects the inverted state of IRA for output on RDYA, and a low on W/RA selects the inverted state of ORA for output on RDYA.
RDYB	O (port B)	Port-B ready. A low on W/RB selects the inverted state of IRB for output on RDYB, and a high on W/RB selects the inverted state of ORB for output on RDYB.
RFM	I	FIFO1 read from mark. When FIFO1 is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the FIFO1 read pointer to the retransmit location and output the first retransmit data.
RST1	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while RST1 is low. The low-to-high transition of RST1 latches the status of FS0 and FS1 for AFA and AEB offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
RST2	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while RST2 is low. The low-to-high transition of RST2 latches the status of FS0 and FS1 for AFB and AEA offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
RTM	I	FIFO1 retransmit mode. When RTM is high and valid data is present on the output of FIFO1, a low-to-high transition of CLKB selects the data for the beginning of a FIFO1 retransmit. The selected position remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, which takes FIFO out of retransmit mode.
W/RA	I	Port-A write/read select. A high on W/RA selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A31 outputs are in the high-impedance state when W/RA is high.
W/RB	I	Port-B write/read select. A low on W/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B31 outputs are in the high-impedance state when W/RB is low.

detailed description

reset

The FIFO memories of the SN74ACT3638 are reset separately by taking their reset (RST1, RST2) inputs low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready flag (IRA, IRB) low, the output-ready flag (ORA, ORB) low, the almost-empty flag (AEA, AEB) low, and the almost-full flag (AFA, AFB) high. Resetting a FIFO also forces the mailbox flag (MBF1, MBF2) of the parallel mailbox register high. After a FIFO is reset, its input-ready flag is set high after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A low-to-high transition on a FIFO reset (RST1, RST2) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method (see almost-empty and almost-full flag offset programming).

almost-empty flag and almost-full flag offset programming

Four registers in the SN74ACT3638 are used to hold the offset values for the almost-empty and almost-full flags. The port-B almost-empty flag (AEB) offset register is labeled X1, and the port-A almost-empty flag (AEA) offset register is labeled X2. The port-A almost-full flag (AFA) offset register is labeled Y1, and the port-B almost-full flag (AFB) offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

almost-empty flag and almost-full flag offset programming (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 AND Y1 REGISTERS†	X2 AND Y2 REGISTERS‡
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

† X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.

‡ X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

To load the almost-empty flag and almost-full flag offset registers of a FIFO with one of the three preset values listed in Table 1, at least one of the flag-select inputs must be high during the low-to-high transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be high when FIFO1 reset ($\overline{RST1}$) returns high. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{RST2}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. Each offset register uses port-A (A8–A0) inputs, with A8 as the most-significant bit. Each register value can be programmed from 1 to 508. After all the offset registers are programmed from port A, the port-B input-ready flag (IRB) is set high and both FIFOs begin normal operation.

FIFO write/read operation

The state of the port-A data (A0–A31) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A31 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A31 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low.

Data is loaded into FIFO1 from the A0–A31 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and IRA is high. Data is read from FIFO2 to the A0–A31 outputs by a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, ENA is high, MBA is low, and ORA is high (see Table 2). FIFO reads and writes on port A are independent of any concurrent port-B operation.

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A31 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

FIFO write/read operation (continued)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{\text{W}}$/RB) is the inverse of the port-A write/read select (W/$\overline{\text{RA}}$). The state of the port-B data (B0–B31) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select ($\overline{\text{W}}$/RB). The B0–B31 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ is high or $\overline{\text{W}}$/RB is low. The B0–B31 outputs are active when $\overline{\text{CSB}}$ is low and $\overline{\text{W}}$/RB is high.

Data is loaded into FIFO2 from the B0–B31 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is low, ENB is high, MBB is low, and IRB is high. Data is read from FIFO1 to the B0–B31 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is high, ENB is high, MBB is low, and ORB is high (see Table 3). FIFO reads and writes on port B are independent of any concurrent port-A operation.

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	$\overline{\text{W}}$/RB	ENB	MBB	CLKB	B0–B31 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

The setup and hold-time constraints to the port clocks for the port chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select can change states during the setup and hold time window of the cycle.

When a FIFO output-ready flag is low, the next data word is sent to the FIFO output register automatically by the low-to-high transition of the port clock that sets the output-ready flag high. When the output-ready flag is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port chip select, write/read select, enable, and mailbox select.

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). ORA, $\overline{\text{AEA}}$, IRA, and $\overline{\text{AFA}}$ are synchronized to CLKA. ORB, $\overline{\text{AEB}}$, IRB, and $\overline{\text{AFB}}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

synchronized FIFO flags (continued)

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1[†][‡]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	ORB	$\overline{\text{AEB}}$	$\overline{\text{AFA}}$	IRA
0	L	L	H	H
1 to X1	H	L	H	H
(X1 + 1) to [512 – (Y1 + 1)]	H	H	H	H
(512 – Y1) to 511	H	H	L	H
512	H	H	L	L

[†] X1 is the almost-empty offset for FIFO1 used by $\overline{\text{AEB}}$. Y1 is the almost-full offset for FIFO1 used by $\overline{\text{AFA}}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.

[‡] When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2[‡][§]	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORA	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	IRB
0	L	L	H	H
1 to X2	H	L	H	H
(X2 + 1) to [512 – (Y2 +1)]	H	H	H	H
(512 – Y2) to 511	H	H	L	H
512	H	H	L	L

[‡] When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

[§] X2 is the almost-empty offset for FIFO2 used by $\overline{\text{AEA}}$. Y2 is the almost-full offset for FIFO2 used by $\overline{\text{AFB}}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

output-ready flags (ORA, ORB)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the output-ready flag synchronizing clock; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of the synchronizing clock occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on an output-ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

input-ready flags (IRA, IRB)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the input-ready flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the input-ready flag synchronizing clock; therefore, an input-ready flag is low if less than two cycles of the input-ready flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the input-ready flag synchronizing clock after the read sets the input-ready flag high.

A low-to-high transition on an input-ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

ready flags ($\overline{RDYA}$, $\overline{RDYB}$)

A ready flag is provided on each port to show if the transmitting or receiving FIFO chosen by the port write/read select is available for data transfer. The port-A ready flag ($\overline{RDYA}$) outputs the complement of the IRA flag when W/$\overline{RA}$ is high and the complement of the ORA flag when W/$\overline{RA}$ is low. The port-B ready flag ($\overline{RDYB}$) outputs the complement of the IRB flag when $\overline{W}$/RB is low the the complement of the ORB flag when $\overline{W}$/RB is high (see Figures 11 and 12).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). A FIFO is almost empty when it contains X or less words in memory and is no longer almost empty when it contains (X + 1) or more words. Note that a data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for its almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). A FIFO is almost full when it contains (512 – Y) or more words in memory and is not almost full when it contains [512 – (Y + 1)] or less words. A data word present in the FIFO output register has been read from memory.

almost-full flags ($\overline{AFA}$, $\overline{AFB}$) (continued)

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for its almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [512 – (Y + 1)] or less words remains low if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [512 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [512 – (Y + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [512 – (Y + 1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle (see Figures 15 and 16).

synchronous retransmit

The synchronous retransmit feature of the SN74ACT3638 allows FIFO1 data to be read repeatedly starting at a user-selected position. FIFO1 is first put into retransmit mode to select a beginning word and prevent on-going FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. FIFO1 can be taken out of retransmit mode at any time and allow normal operation.

FIFO1 is put in retransmit mode by a low-to-high transition on CLKB when the retransmit-mode (RTM) input is high and ORB is high. This rising CLKB edge marks the data present in the FIFO1 output register as the first retransmit data. FIFO1 remains in retransmit mode until a low-to-high transition occurs while RTM is low.

When two or more reads have been completed past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO1 output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while FIFO1 is in retransmit mode. RFM should not be high during the CLKB rising edge that takes the FIFO1 out of retransmit mode.

When FIFO1 is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO1 output register and used by the ORB and $\overline{AEB}$ flags. The shadow read pointer stores the SRAM location at the time FIFO1 is put into retransmit mode and does not change until FIFO1 is taken out of retransmit mode. The shadow read pointer is used by the IRA and $\overline{AFA}$ flags. Data writes can proceed while FIFO1 is in retransmit mode, $\overline{AFA}$ is set low by the write that stores (512 – Y1) words after the first retransmit word, and IR is set low by the 512th write after the first retransmit word.

When FIFO1 is in retransmit mode and RFM is high, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the ORB flag reflects the new level of fill immediately. If the retransmit changes the FIFO1 status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{AEB}$ high (see Figure 18). The rising CLKB edge that takes FIFO1 out of retransmit mode shifts the read pointer used by the IRA and $\overline{AFA}$ flags from the shadow to the current read pointer. If the change of read pointer used by IRA and $\overline{AFA}$ should cause one or both flags to transition high, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after FIFO1 is taken out of retransmit mode is the first synchronizing cycle of IRA if it occurs at time t_{sk1} or greater after the rising CLKB edge (see Figure 19). A rising CLKA edge after FIFO1 is taken out of retransmit mode is the first synchronizing cycle of $\overline{AFA}$ if it occurs at time t_{sk2} or greater after the rising CLKB edge (see Figure 20).

mailbox registers

Each FIFO has a 32-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A31 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. A low-to-high transition on CLKB writes B0–B31 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

mailbox registers (continued)

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port mailbox select input is low and from the mail register when the port-mailbox select input is high. The mail1 register flag ($\overline{\text{MBF1}}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB and with MBB high. The mail2 register flag ($\overline{\text{MBF2}}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA and with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

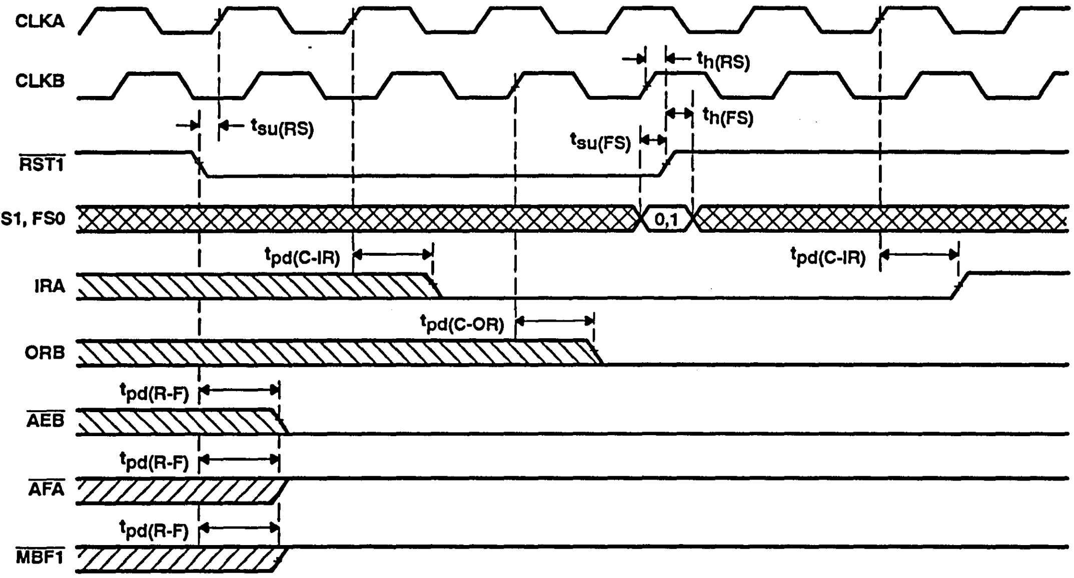
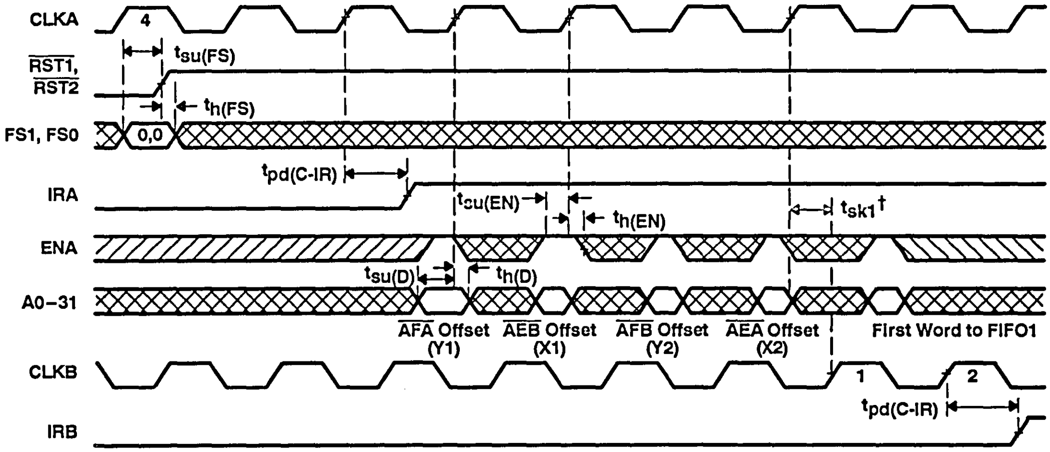


Figure 1. FIFO1 Reset Loading X1 and Y1 With a Preset Value of Eight†

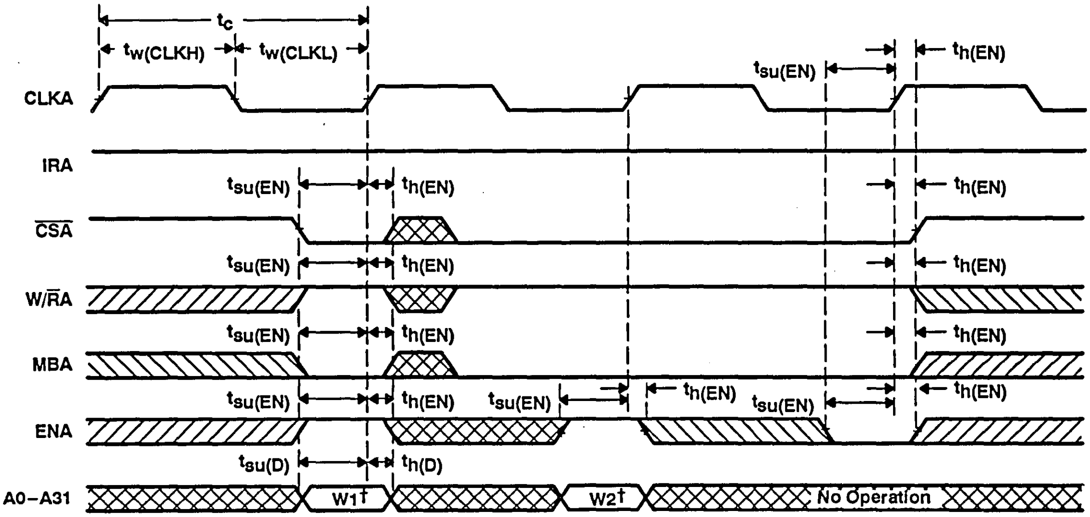
† FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



† t_{sk1} is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition high in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{sk1}, then IRB may transition high one cycle later than shown.

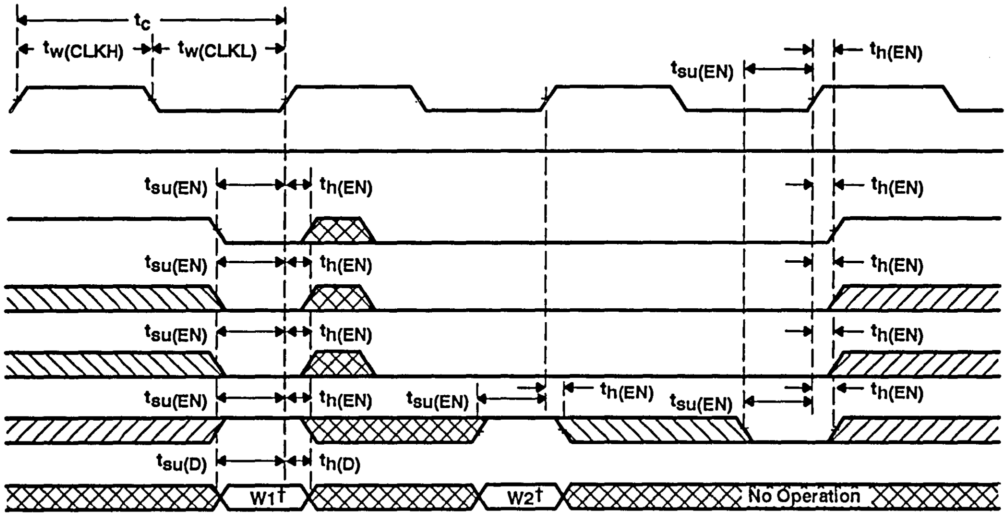
NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values After Reset



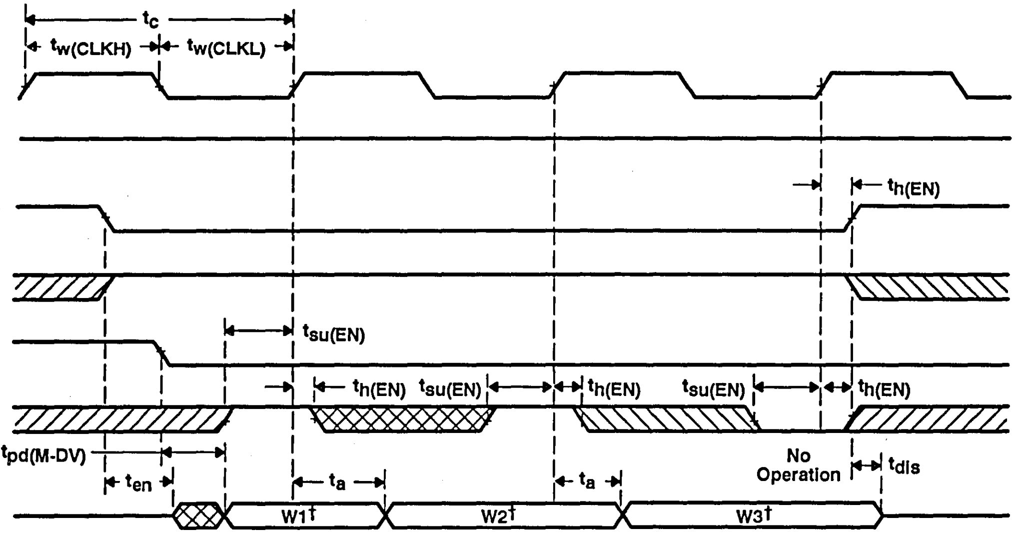
† Written to FIFO1

Figure 3. Port-A Write Cycle Timing for FIFO1



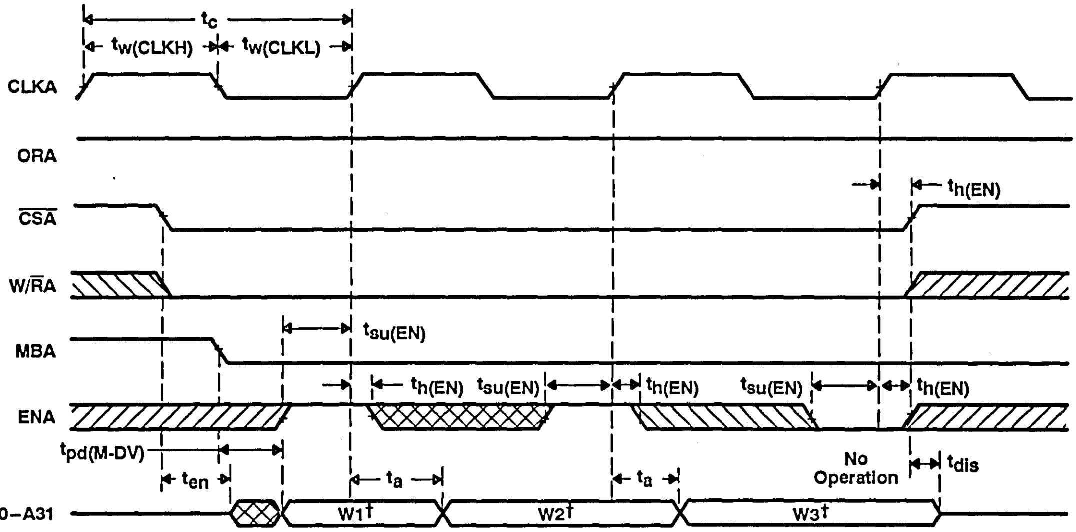
† Written to FIFO2

Figure 4. Port-B Write Cycle Timing for FIFO2



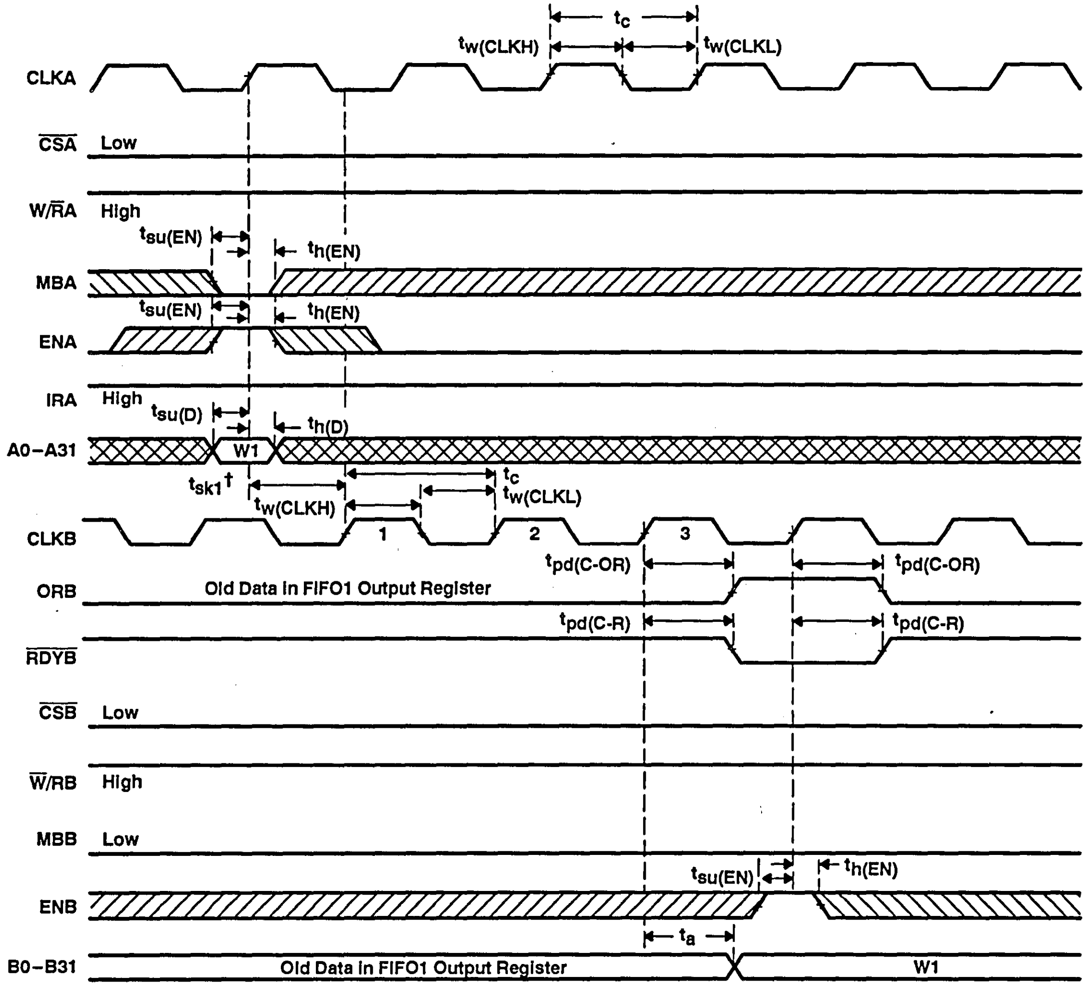
† Read from FIFO1

Figure 5. Port-B Read Cycle Timing for FIFO1



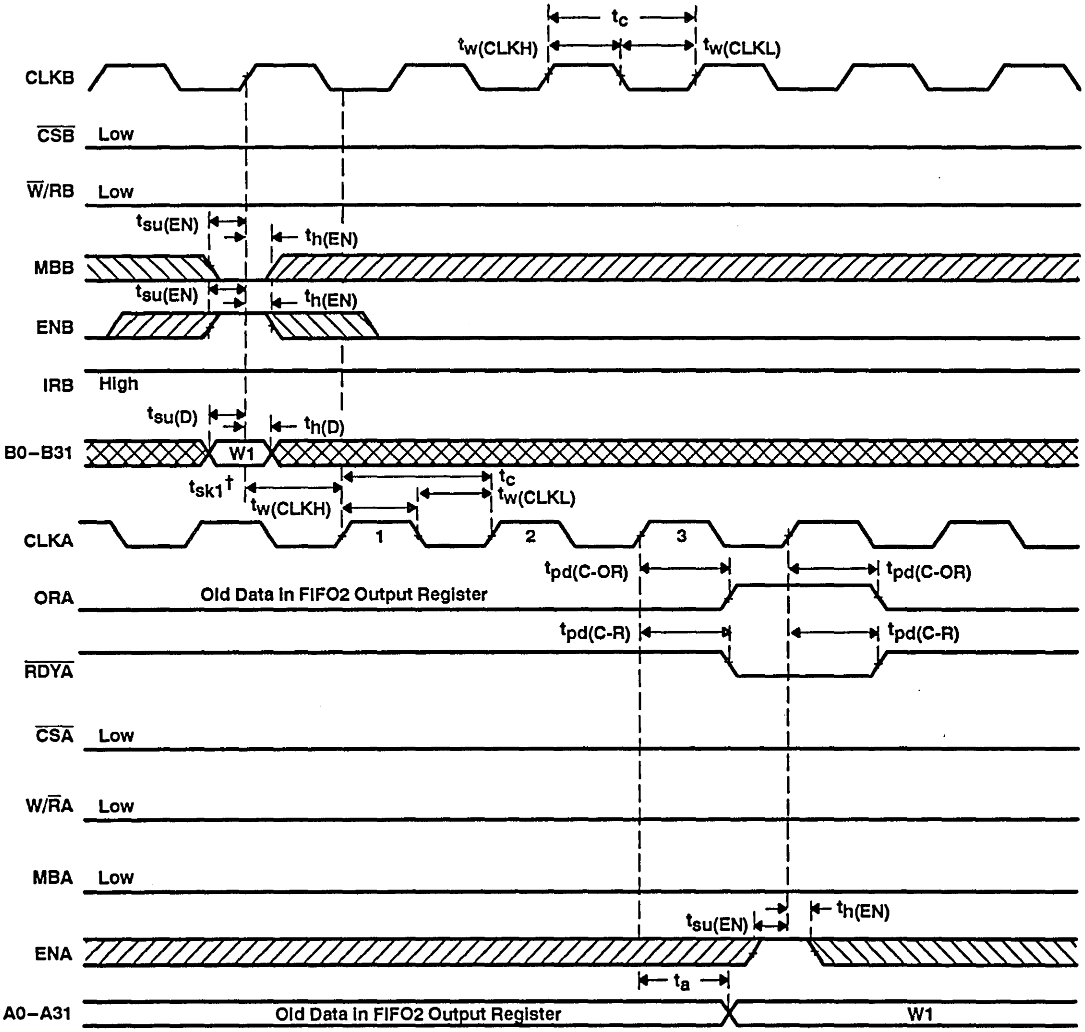
† Read from FIFO2

Figure 6. Port-A Read Cycle Timing for FIFO2



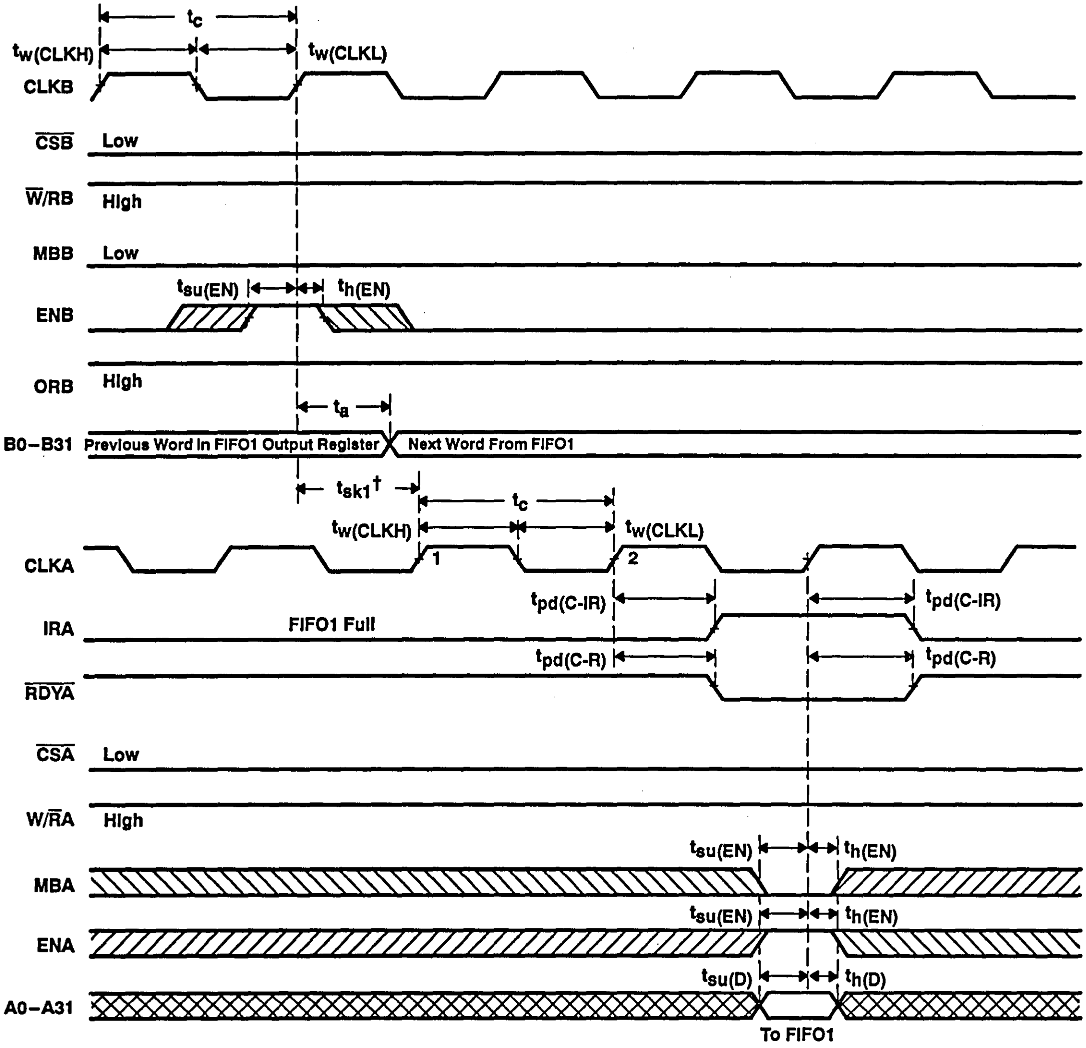
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 7. ORB-Flag Timing and First-Data-Word Fallthrough When FIFO1 Is Empty



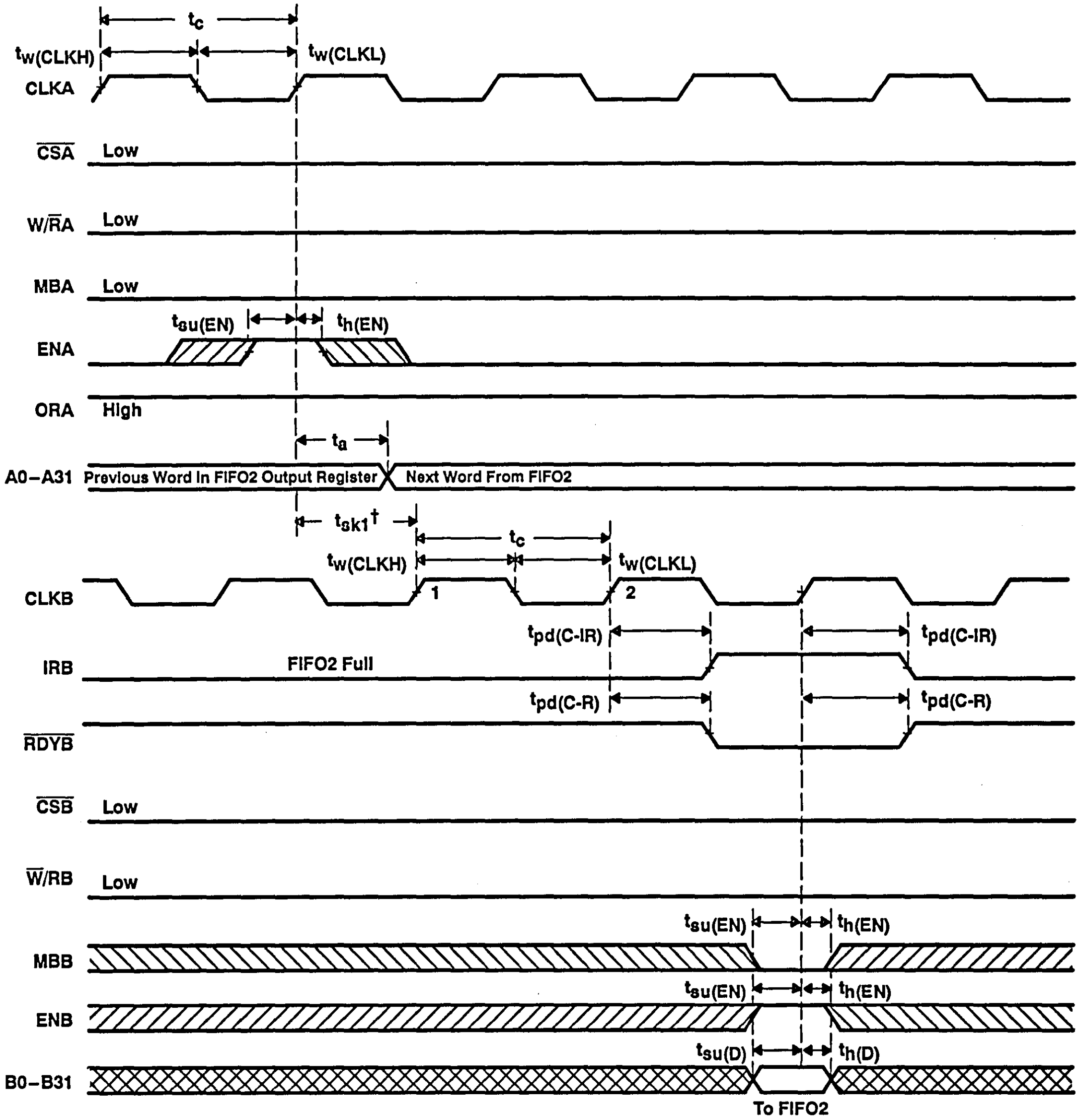
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 8. ORA-Flag Timing and First-Data-Word Fallthrough When FIFO2 Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then IRA may transition high one CLKA cycle later than shown.

Figure 9. IRA-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then IRB may transition high one CLKB cycle later than shown.

Figure 10. IRB-Flag Timing and First Available Write When FIFO2 Is Full

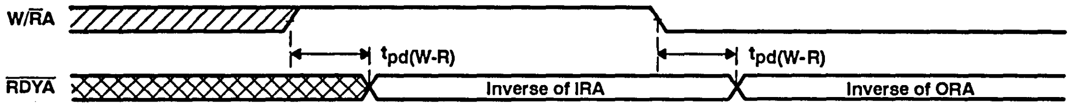


Figure 11. W/$\overline{RA}$ to $\overline{RDYA}$ Timing

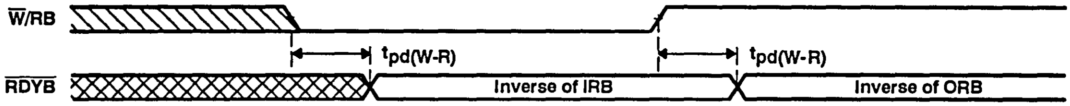
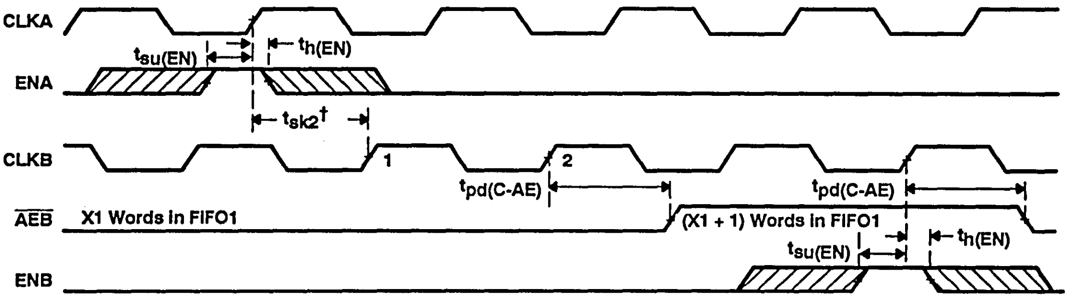


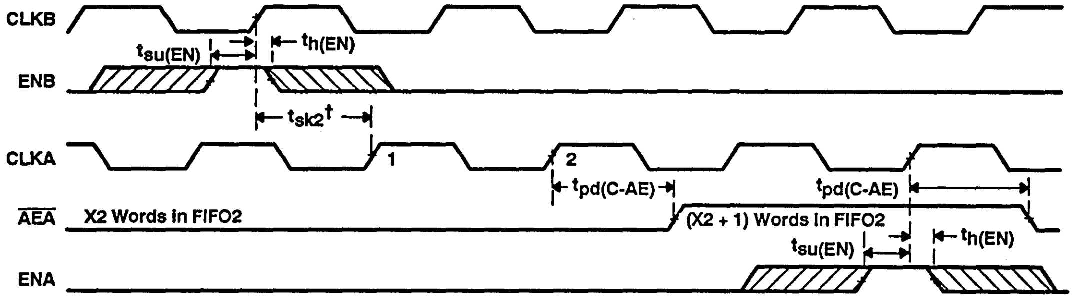
Figure 12. $\overline{W}$/RB to $\overline{RDYB}$ Timing



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

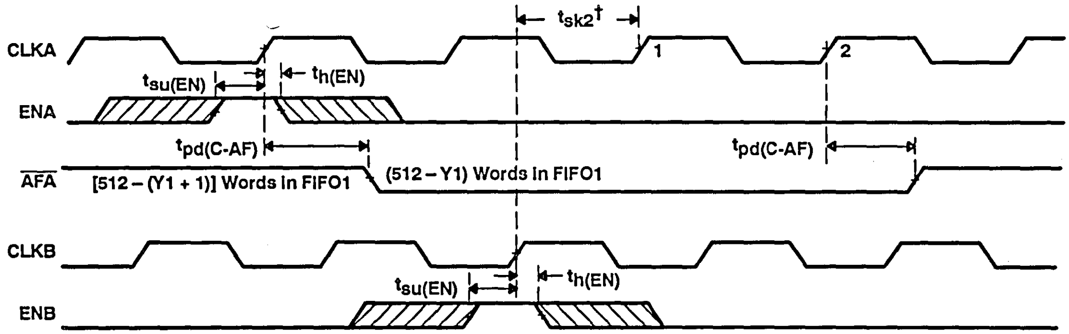
Figure 13. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB = L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

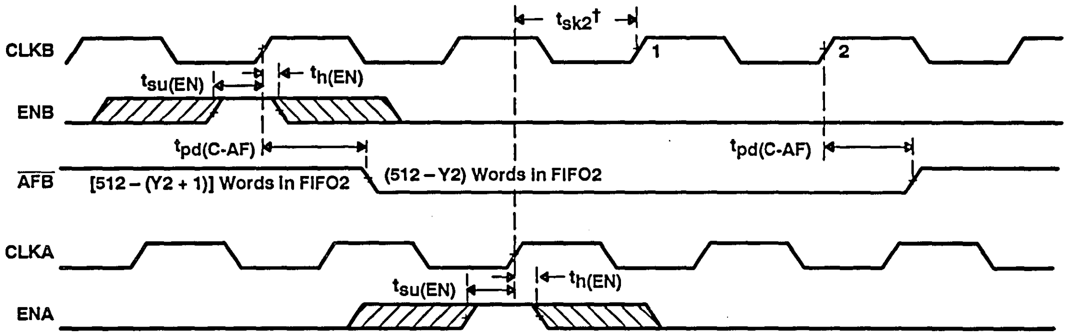
Figure 14. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

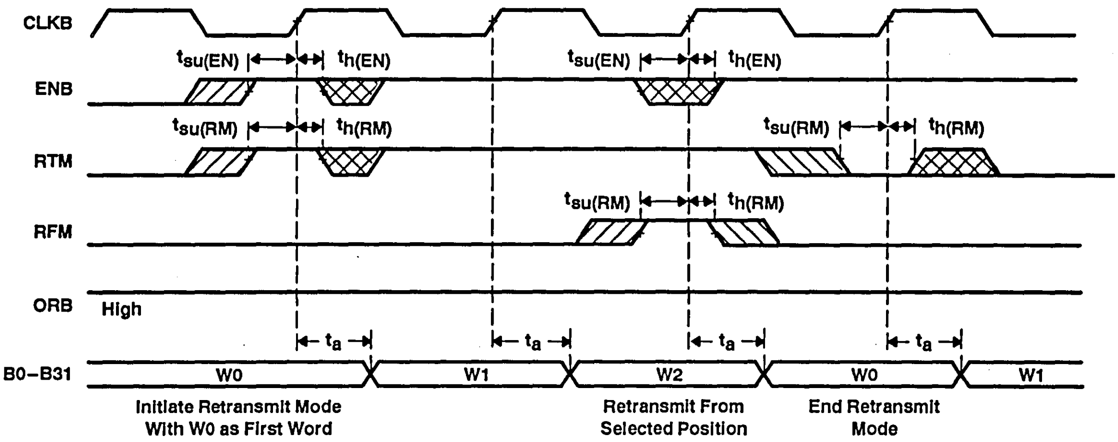
Figure 15. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.

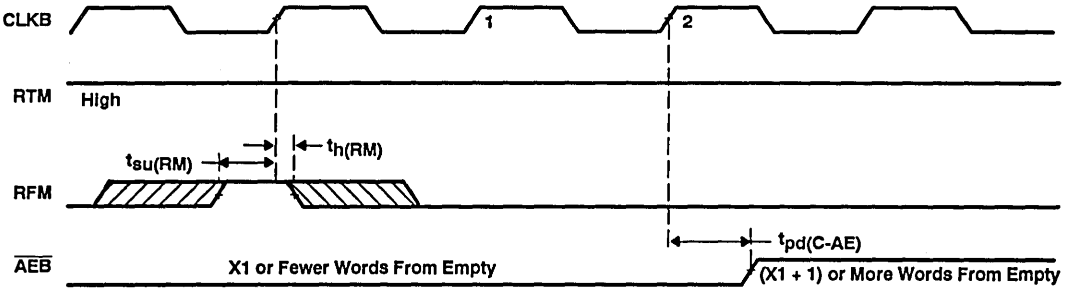
NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB= L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 16. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full



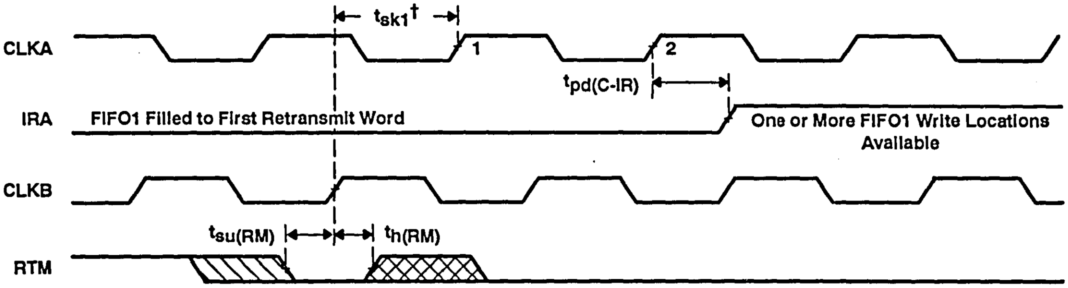
NOTE A: $\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO1 output register.

Figure 17. FIFO1 Retransmit Timing Showing Minimum Retransmit Length



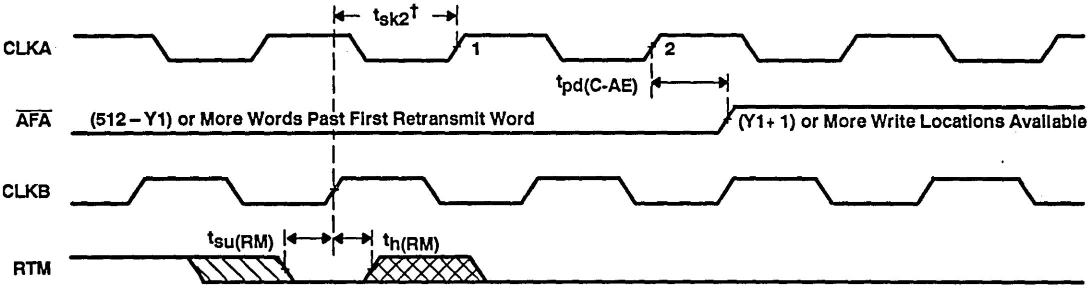
NOTE A: X1 is the value loaded in the $\overline{AEB}$ offset register.

Figure 18. $\overline{AEB}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X1



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then IRA may transition high one CLKA cycle later than shown.

Figure 19. IRA Timing From the End of Retransmit Mode When One or More FIFO1 Write Locations Are Available



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKA cycle later than shown.
NOTE A: Y is the value loaded in the almost-full flag offset register.

Figure 20. $\overline{AFA}$ Timing From the End of Retransmit Mode When (Y1 + 1) or More FIFO1 Write Locations Are Available

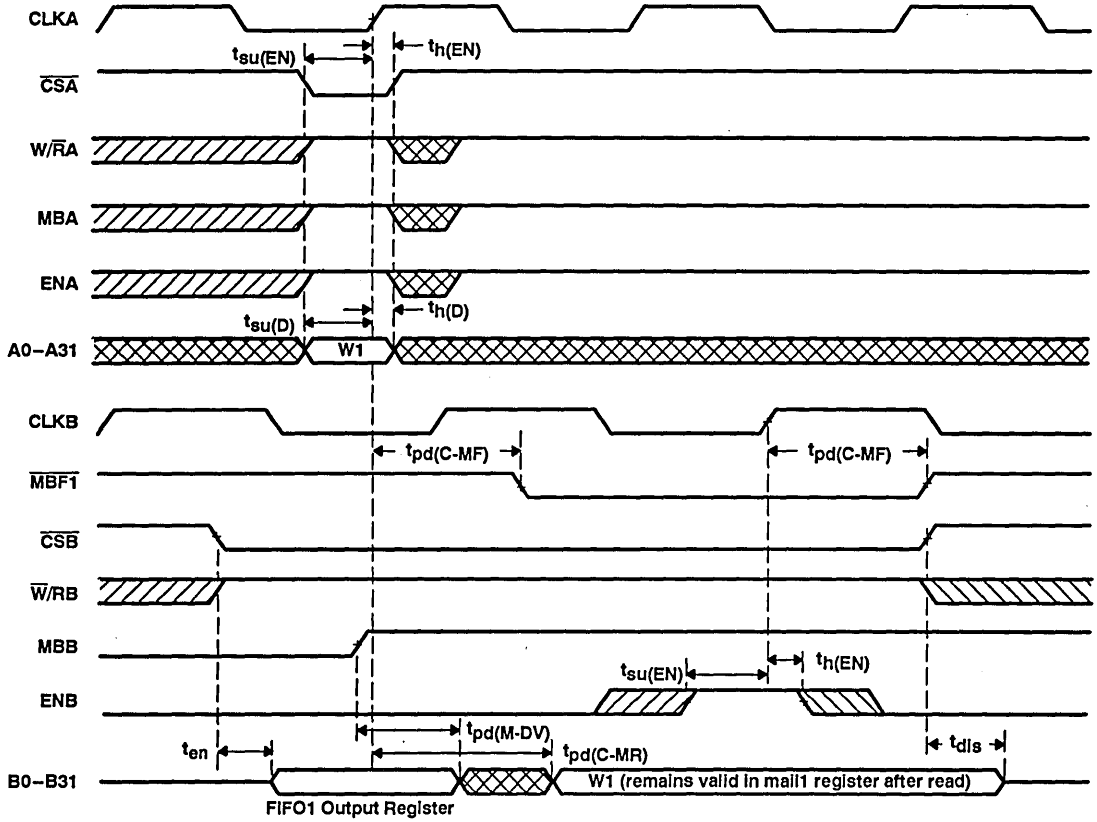


Figure 21. Timing for Mail1 Register and $\overline{MBF1}$ Flag

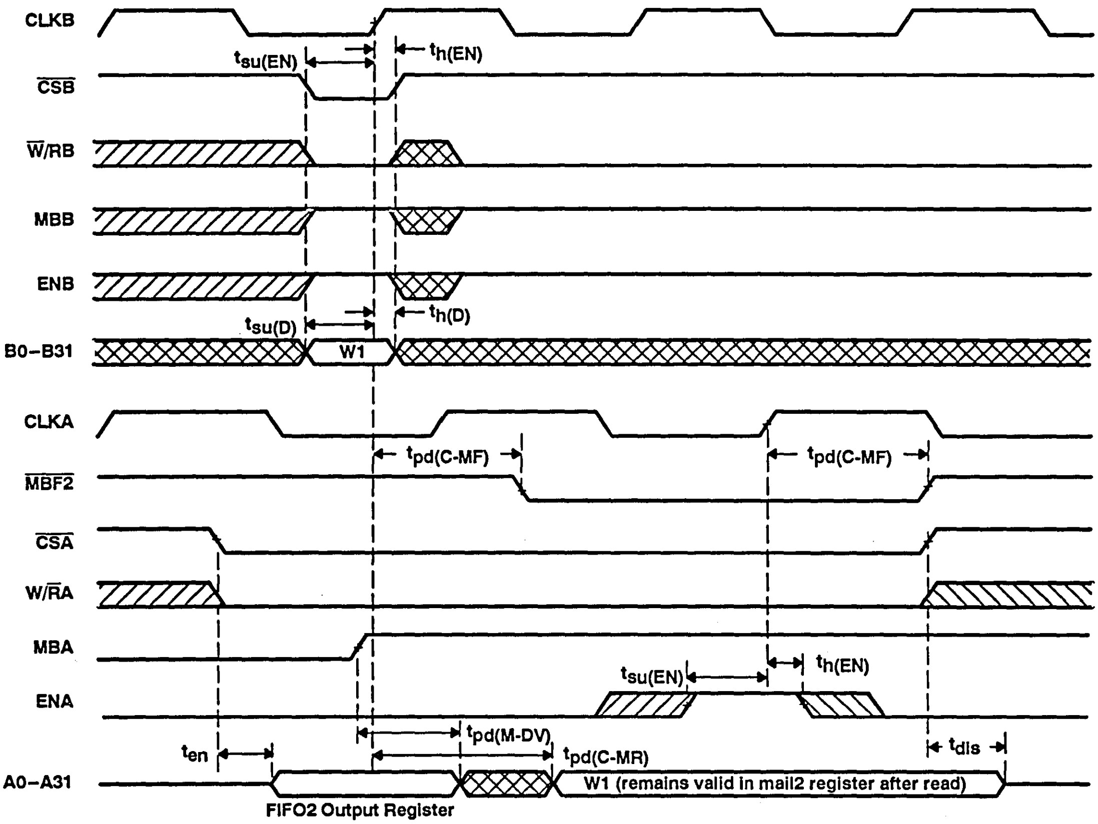


Figure 22. Timing for Mail2 Register and $\overline{MBF2}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0					±5	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0					±5	µA
I_{CC}	V_{CC} = 5.5 V,	$V_I = V_{CC} - 0.2$ V or 0					400	µA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{\text{CSA}} = V_{IH}$	A0–A31		0		mA
			$\overline{\text{CSB}} = V_{IH}$	B0–B31		0		
			$\overline{\text{CSA}} = V_{IL}$	A0–A31			1	
			$\overline{\text{CSB}} = V_{IL}$	B0–B31			1	
			All other inputs				1	
C_i	$V_I = 0$,	f = 1 MHz				4		pF
C_o	$V_O = 0$,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 22)

		'ACT3638-15		'ACT3638-20		'ACT3638-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		10		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		10		ns
$t_{su(D)}$	Setup time, A0–A31 before CLKA↑ and B0–B31 before CLKB↑	4.5		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, ENA, and MBA before CLKA↑; $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, ENB, and MBB before CLKB↑	5		6		7		ns
$t_{su(RM)}$	Setup time, RTM and RFM before CLKB↑	6		6.5		7		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RST1}}$ or $\overline{\text{RST2}}$ low before CLKA↑ or CLKB↑[†]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ high	7		8		9		ns
$t_{h(D)}$	Hold time, A0–A31 after CLKA↑ and B0–B31 after CLKB↑	0		0		0		ns
$t_{h(EN)}$	Hold time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, ENA, and MBA after CLKA↑; $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RM)}$	Hold time, RTM and RFM after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{\text{RST1}}$ or $\overline{\text{RST2}}$ low after CLKA↑ or CLKB↑[†]	4		4		5		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ high	2		3		3		ns
t_{sk1}[‡]	Skew time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	8		9		11		ns
t_{sk2}[‡]	Skew time, between CLKA↑ and CLKB↑ for $\overline{\text{AEA}}$, $\overline{\text{AEB}}$, $\overline{\text{AFA}}$, and $\overline{\text{AFB}}$	12		16		20		ns

[†] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[‡] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 22)

PARAMETER		'ACT3638-15		'ACT3638-20		'ACT3638-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKA↑ to A0–A31 and CLKB↑ to B0–B31	3	11	3	13	3	15	ns
$t_{pd(C\text{-}IR)}$	Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB	1	8	1	10	1	12	ns
$t_{pd(C\text{-}OR)}$	Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB	1	8	1	10	1	12	ns
$t_{pd(C\text{-}R)}$	Propagation delay time, CLKA↑ to $\overline{\text{RDYA}}$ and CLKB↑ to $\overline{\text{RDYB}}$	1	8	1	10	1	12	ns
$t_{pd(W\text{-}R)}$	Propagation delay time, W/$\overline{\text{RA}}$ to $\overline{\text{RDYA}}$ and $\overline{\text{W}}$/RB to $\overline{\text{RDYB}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{\text{AEA}}$ and CLKB↑ to $\overline{\text{AEB}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\text{AFA}}$ and CLKB↑ to $\overline{\text{AFB}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\text{MBF1}}$ low or $\overline{\text{MBF2}}$ high and CLKB↑ to $\overline{\text{MBF2}}$ low or $\overline{\text{MBF1}}$ high	0	8	0	10	0	12	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B31† and CLKB↑ to A0–A31‡	3	13.5	3	15	3	17	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A31 valid and MBB to B0–B31 valid	3	13	3	15	3	17	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\text{RST1}}$ low to $\overline{\text{AEB}}$ low, $\overline{\text{AFA}}$ high, and $\overline{\text{MBF1}}$ high, and $\overline{\text{RST2}}$ low to $\overline{\text{AEA}}$ low, $\overline{\text{AFB}}$ high, and $\overline{\text{MBF2}}$ high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ low to A0–A31 active and $\overline{\text{CSB}}$ low and $\overline{\text{W}}$/RB high to B0–B31 active	2	12	2	13	2	14	ns
t_{dis}	Disable time, $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ high to A0–A31 at high impedance and $\overline{\text{CSB}}$ high or $\overline{\text{W}}$/RB low to B0–B31 at high impedance	1	13	1	14	1	15	ns

† Writing data to the mail1 register when the B0–B31 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A31 outputs are active and MBA is high.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

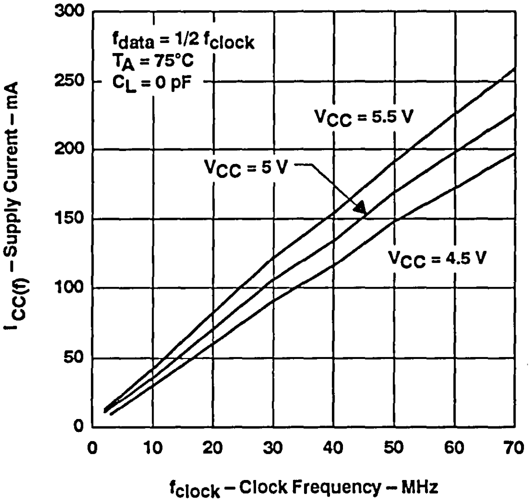


Figure 23

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 23 was taken while simultaneously reading and writing a FIFO on the SN74ACT3638 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel and the number of SN74ACT3638 inputs driven by TTL high levels are known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 23, the maximum power dissipation (P_T) of the SN74ACT3638 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

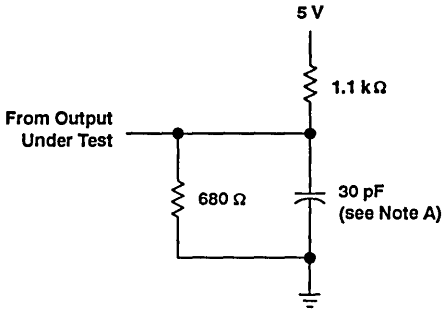
where:

N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

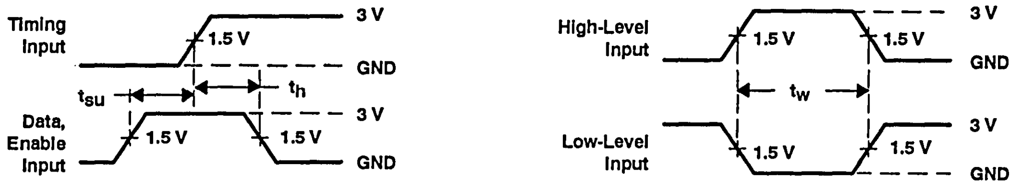
When no reads or writes are occurring on the SN74ACT3638, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.184 \text{ mA/MHz}$$

PARAMETER MEASUREMENT INFORMATION

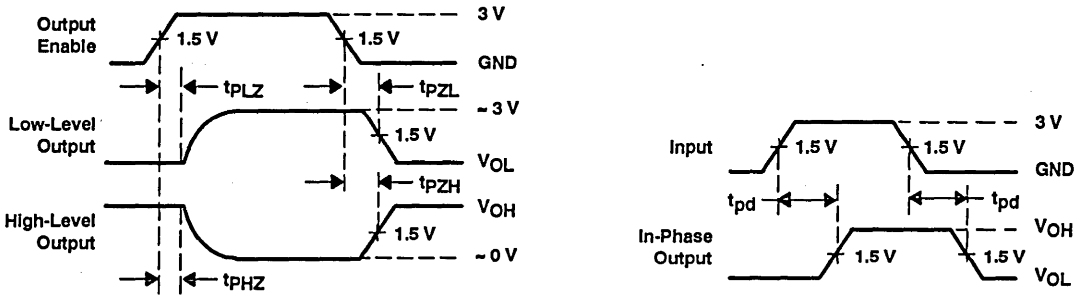


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

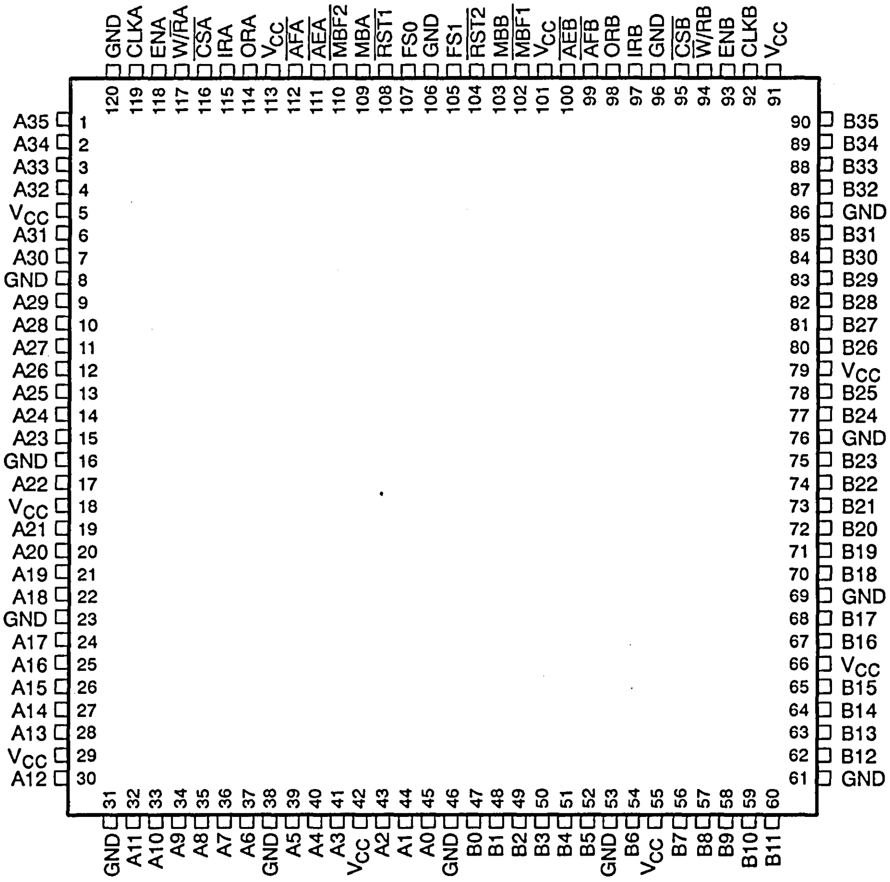
Figure 24. Load Circuit and Voltage Waveforms

SN74ACT3632
512 × 36 × 2 CLOCKED FIRST-IN, FIRST-OUT MEMORY

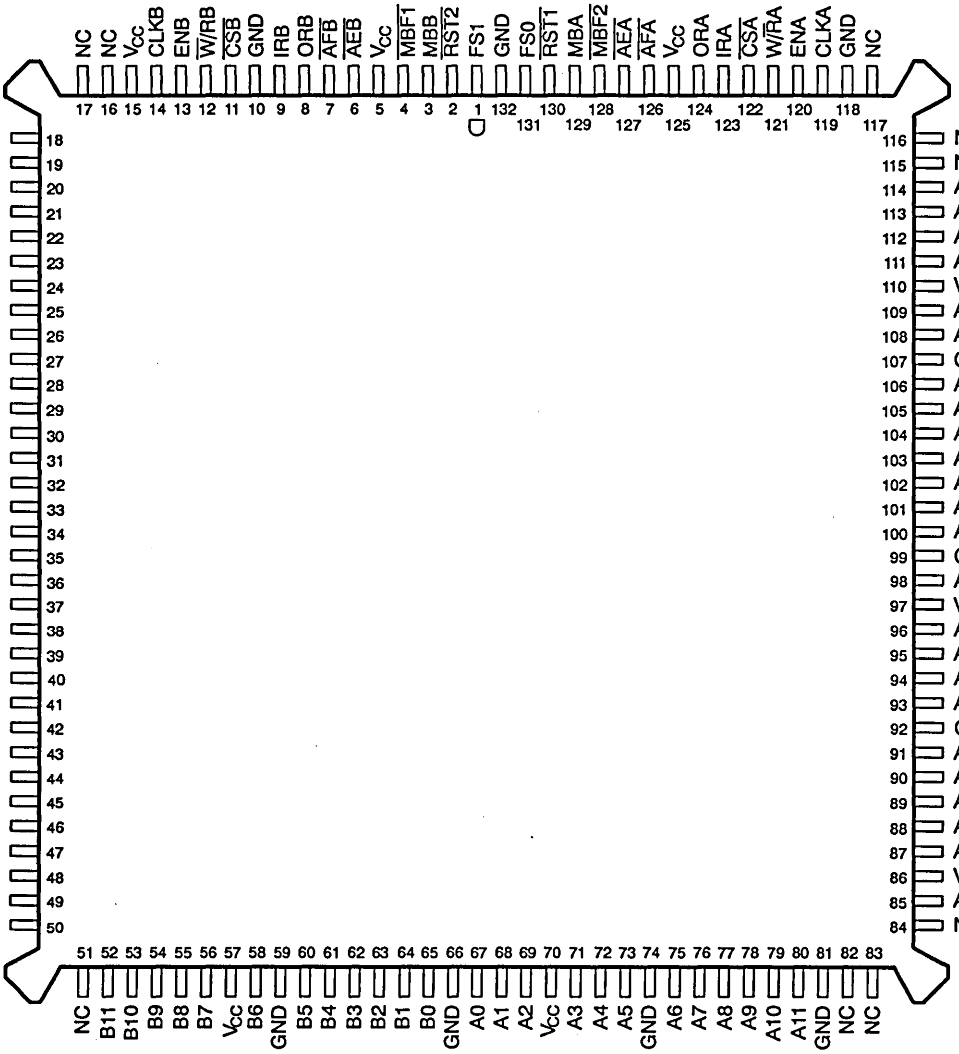
SCAS224A – JUNE 1992 – REVISED AUGUST 1993

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent 512 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **IRA, ORA, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **IRB, ORB, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Low-Power 0.8-Micron Advanced CMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 11 ns**
- **Pin-to-Pin Compatible With the SN74ACT3622 and SN74ACT3642**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)**

PCB PACKAGE
(TOP VIEW)



PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

description

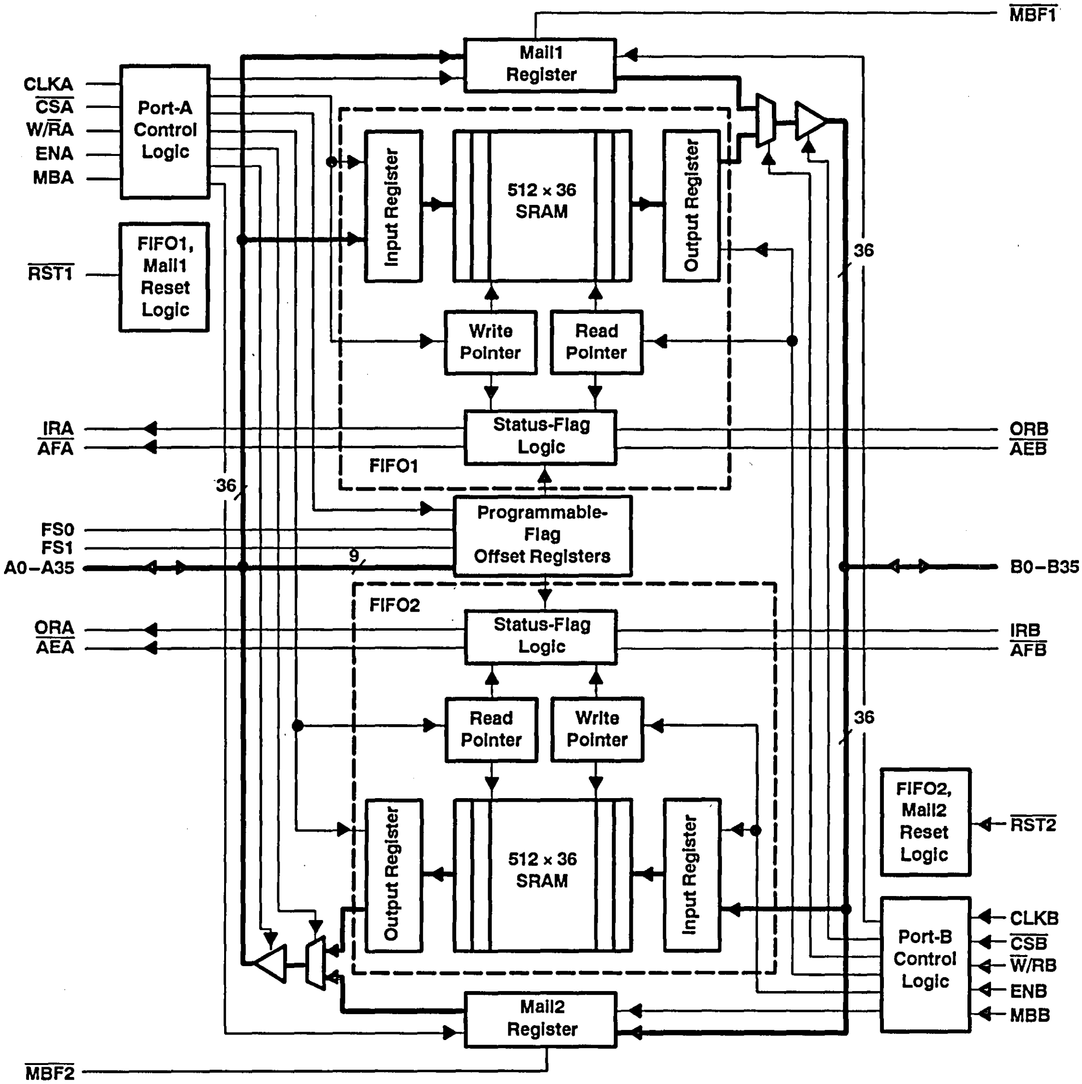
The SN74ACT3632 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 11 ns. Two independent 512 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words are stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths.

The SN74ACT3632 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input-ready (IRA, IRB) flag and almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output-ready (ORA, ORB) flag and almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the almost-full and almost-empty flags of both FIFOs can be programmed from port A.

The SN74ACT3632 is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AEA}}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{\text{AEA}}$ is low when the number of words in FIFO2 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{\text{AEB}}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\text{AEB}}$ is low when the number of words in FIFO1 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{\text{AFA}}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\text{AFA}}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{\text{AFB}}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{\text{AFB}}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the almost-full B offset register, Y2.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{\text{AFA}}$, and $\overline{\text{AEA}}$ are all synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{\text{AFB}}$, and $\overline{\text{AEB}}$ are synchronized to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag offset selects. The low-to-high transition of a FIFO reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO almost-full and almost-empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFOs.
IRA	O (port A)	Input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O (port B)	Input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output-register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output-register data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\text{MBF1}}$ is low. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high when FIFO1 is reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\text{MBF2}}$ is low. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is also set high when FIFO2 is reset.
ORA	O (port A)	Output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
ORB	O (port B)	Output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{\text{RST1}}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST1}}$ is low. The low-to-high transition of $\overline{\text{RST1}}$ latches the status of FS0 and FS1 for $\overline{\text{AFA}}$ and $\overline{\text{AEB}}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{\text{RST2}}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST2}}$ is low. The low-to-high transition of $\overline{\text{RST2}}$ latches the status of FS0 and FS1 for $\overline{\text{AFB}}$ and $\overline{\text{AEA}}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{\text{RA}}$	I	Port-A write/read select. A high on W/$\overline{\text{RA}}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
$\overline{\text{W}}$/RB	I	Port-B write/read select. A low on $\overline{\text{W}}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{\text{W}}$/RB is low.

detailed description

reset

The FIFO memories of the SN74ACT3632 are reset separately by taking their reset ($\overline{\text{RST1}}$, $\overline{\text{RST2}}$) inputs low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready flag (IRA, IRB) low, the output-ready flag (ORA, ORB) low, the almost-empty flag ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) low, and the almost-full flag ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) high. Resetting a FIFO also forces the mailbox flag ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) of the parallel mailbox register high. After a FIFO is reset, its input-ready flag is set high after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A low-to-high transition on a FIFO reset ($\overline{\text{RST1}}$, $\overline{\text{RST2}}$) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method (see *almost-empty and almost-full flag offset programming*).

almost-empty flag and almost-full flag offset programming

Four registers in the SN74ACT3632 are used to hold the offset values for the almost-empty and almost-full flags. The port-B almost-empty flag ($\overline{\text{AEB}}$) offset register is labeled X1 and the port-A almost-empty flag ($\overline{\text{AEA}}$) offset register is labeled X2. The port-A almost-full flag ($\overline{\text{AFA}}$) offset register is labeled Y1 and the port-B almost-full flag ($\overline{\text{AFB}}$) offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST1}}$	$\overline{\text{RST2}}$	X1 AND Y1 REGISTERS†	X2 AND Y2 REGISTERS‡
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

† X1 register holds the offset for $\overline{\text{AEB}}$; Y1 register holds the offset for $\overline{\text{AFA}}$.

‡ X2 register holds the offset for $\overline{\text{AEA}}$; Y2 register holds the offset for $\overline{\text{AFB}}$.

almost-empty flag and almost-full flag offset programming (continued)

To load the almost-empty flag and almost-full flag offset registers of a FIFO with one of the three preset values listed in Table 1, at least one of the flag-select inputs must be high during the low-to-high transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be high when FIFO1 reset ($\overline{\text{RST1}}$) returns high. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{\text{RST2}}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. Each offset register uses port-A (A8–A0) inputs, with A8 as the most significant bit. Each register value can be programmed from 1 to 508. After all the offset registers are programmed from port A, the port-B input-ready flag (IRB) is set high and both FIFOs begin normal operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{RA}}$). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are low.

Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is high, ENA is high, MBA is low, and IRA is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is low, ENA is high, MBA is low, and ORA is high (see Table 2). FIFO reads and writes on port A are independent of any concurrent port-B operation.

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{RA}}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{\text{W}}$/RB) is the inverse of the port-A write/read select (W/$\overline{\text{RA}}$). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select ($\overline{\text{W}}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ is high or $\overline{\text{W}}$/RB is low. The B0–B35 outputs are active when $\overline{\text{CSB}}$ is low and $\overline{\text{W}}$/RB is high.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is low, ENB is high, MBB is low, and IRB is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is high, ENB is high, MBB is low, and ORB is high (see Table 3). FIFO reads and writes on port B are independent of any concurrent port-A operation.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{\mathrm{CSB}}$	$\mathrm{W}/\overline{\mathrm{RB}}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\mathrm{MBF1}}$ high)

The setup and hold time constraints to the port clocks for the port chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select may change states during the setup and hold time window of the cycle.

When a FIFO output-ready flag is low, the next data word is sent to the FIFO output register automatically by the low-to-high transition of the port clock that sets the output-ready flag high. When the output-ready flag is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port's chip select, write/read select, enable, and mailbox select.

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). ORA, $\overline{\mathrm{AEA}}$, IRA, and $\overline{\mathrm{AFA}}$ are synchronized to CLKA. ORB, $\overline{\mathrm{AEB}}$, IRB, and $\overline{\mathrm{AFB}}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1†‡	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	ORB	$\overline{\mathrm{AEB}}$	$\overline{\mathrm{AFA}}$	IRA
0	L	L	H	H
1 to X1	H	L	H	H
(X1 + 1) to [512 – (Y1 + 1)]	H	H	H	H
(512 – Y1) to 511	H	H	L	H
512	H	H	L	L

† X1 is the almost-empty offset for FIFO1 used by $\overline{\mathrm{AEB}}$. Y1 is the almost-full offset for FIFO1 used by $\overline{\mathrm{AFA}}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.

‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

synchronized FIFO flags (continued)

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2†‡	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORA	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	IRB
0	L	L	H	H
1 to X2	H	L	H	H
(X2 + 1) to [512 – (Y2 + 1)]	H	H	H	H
(512 – Y2) to 511	H	H	L	H
512	H	H	L	L

† X2 is the almost-empty offset for FIFO2 used by $\overline{\text{AEA}}$. Y2 is the almost-full offset for FIFO2 used by $\overline{\text{AFB}}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

output-ready flags (ORA, ORB)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the output-ready flag synchronizing clock; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of the synchronizing clock occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on an output-ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

input-ready flags (IRA, IRB)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the input-ready flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the input-ready flag synchronizing clock; therefore, an input-ready flag is low if less than two cycles of the input-ready flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the input-ready flag synchronizing clock after the read sets the input-ready flag high.

A low-to-high transition on an input-ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-empty flag is low when its FIFO contains X or less words and is high when its FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for its almost-empty flag to reflect the new level of fill. Therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-full flag is low when its FIFO contains (512 – Y) or more words and is high when its FIFO contains [512 – (Y + 1)] or less words. A data word is present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [512 – (Y + 1)] or less words remains low if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [512 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [512 – (Y + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [512 – (Y + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port mailbox select input is low and from the mail register when the port-mailbox select input is high. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

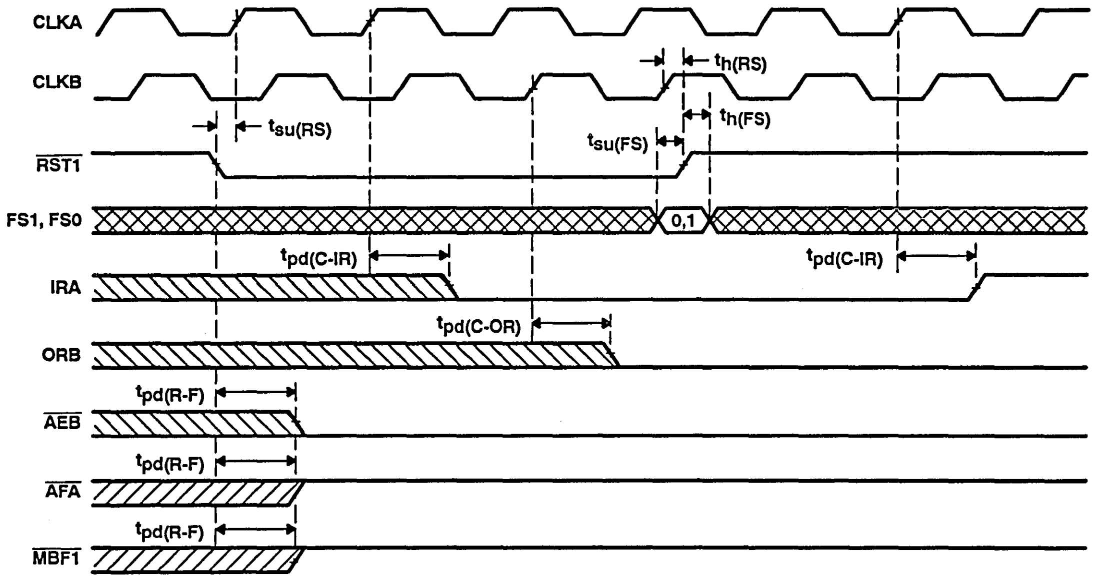
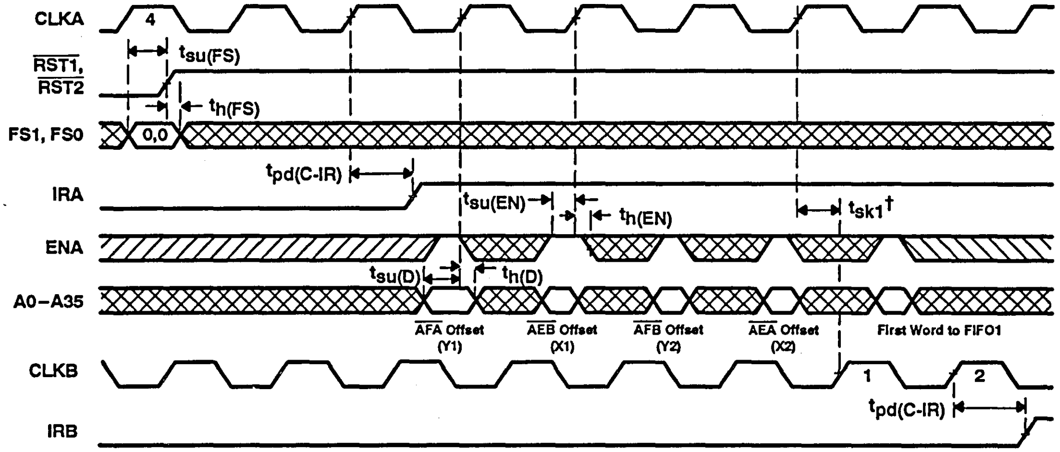


Figure 1. FIFO1 Reset Loading X1 and Y1 With a Preset Value of Eight†

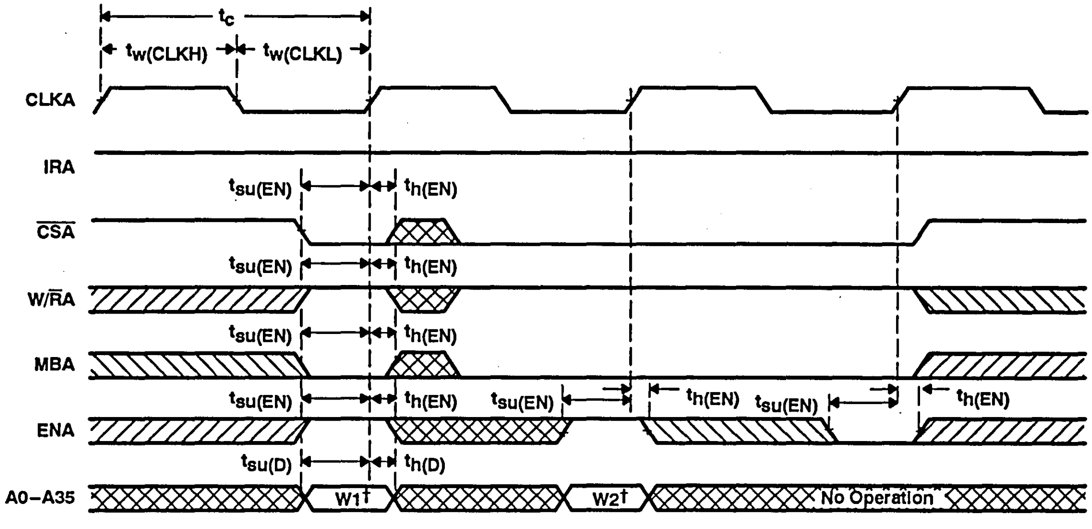
† FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



† t_{sk1} is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition high in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{sk1}, then IRB may transition high one cycle later than shown.

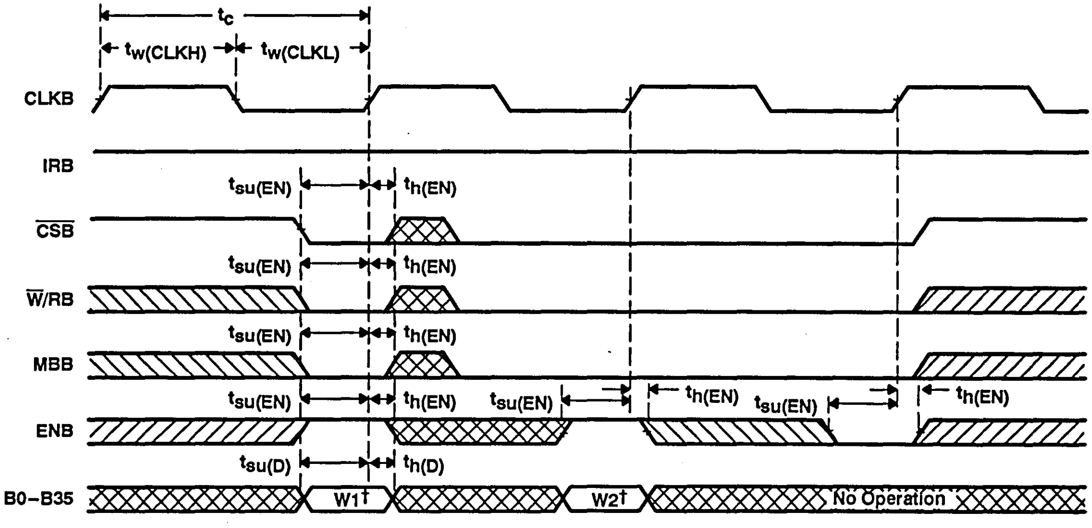
NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values After Reset



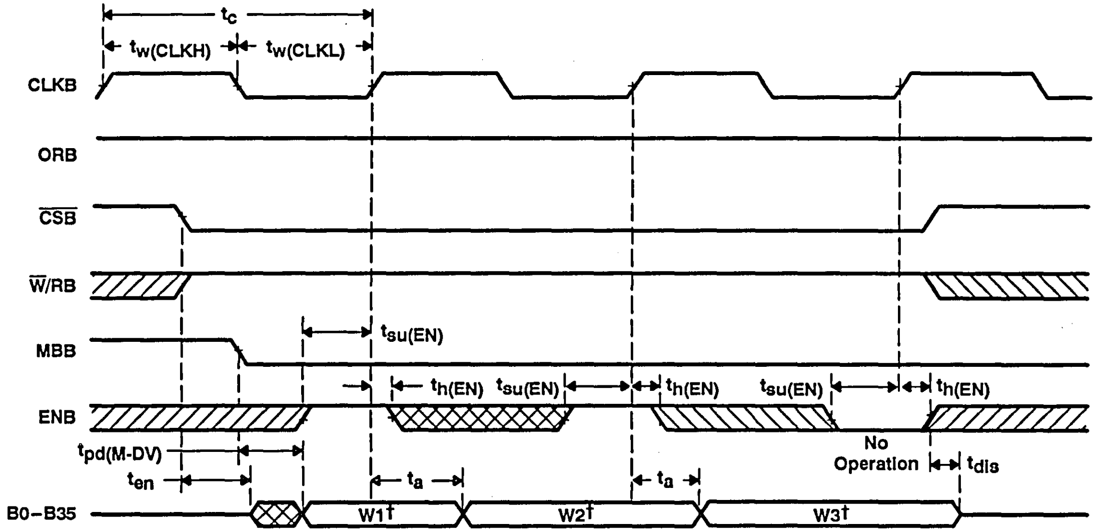
† Written to FIFO1

Figure 3. Port-A Write Cycle Timing for FIFO1



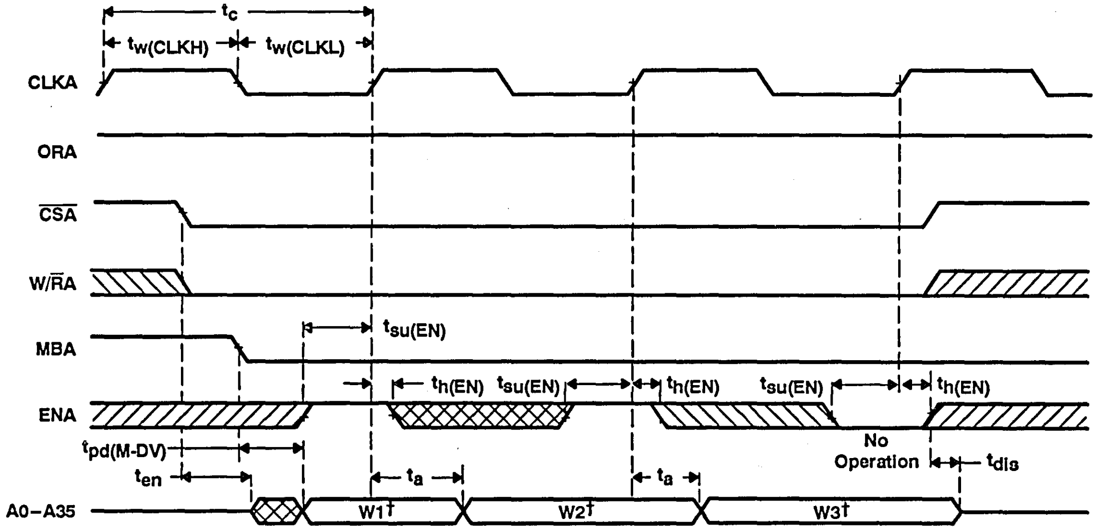
† Written to FIFO2

Figure 4. Port-B Write Cycle Timing for FIFO2



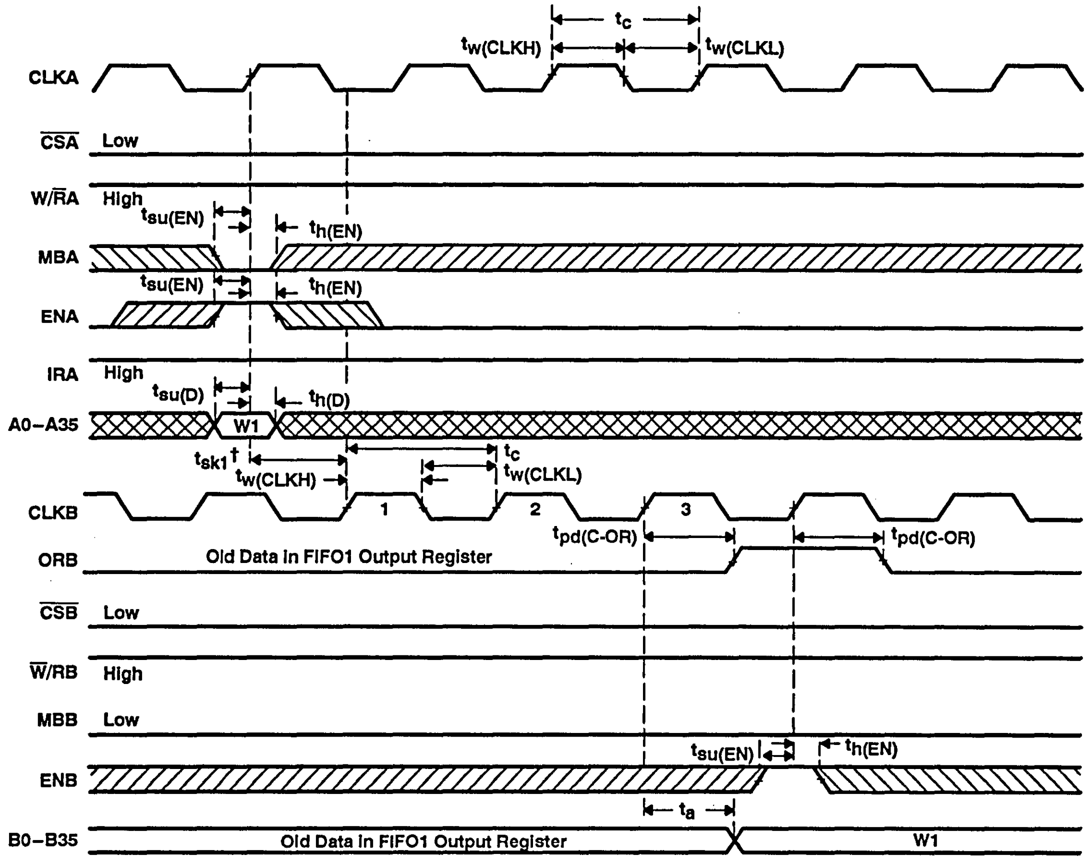
† Read from FIFO1

Figure 5. Port-B Read Cycle Timing for FIFO1



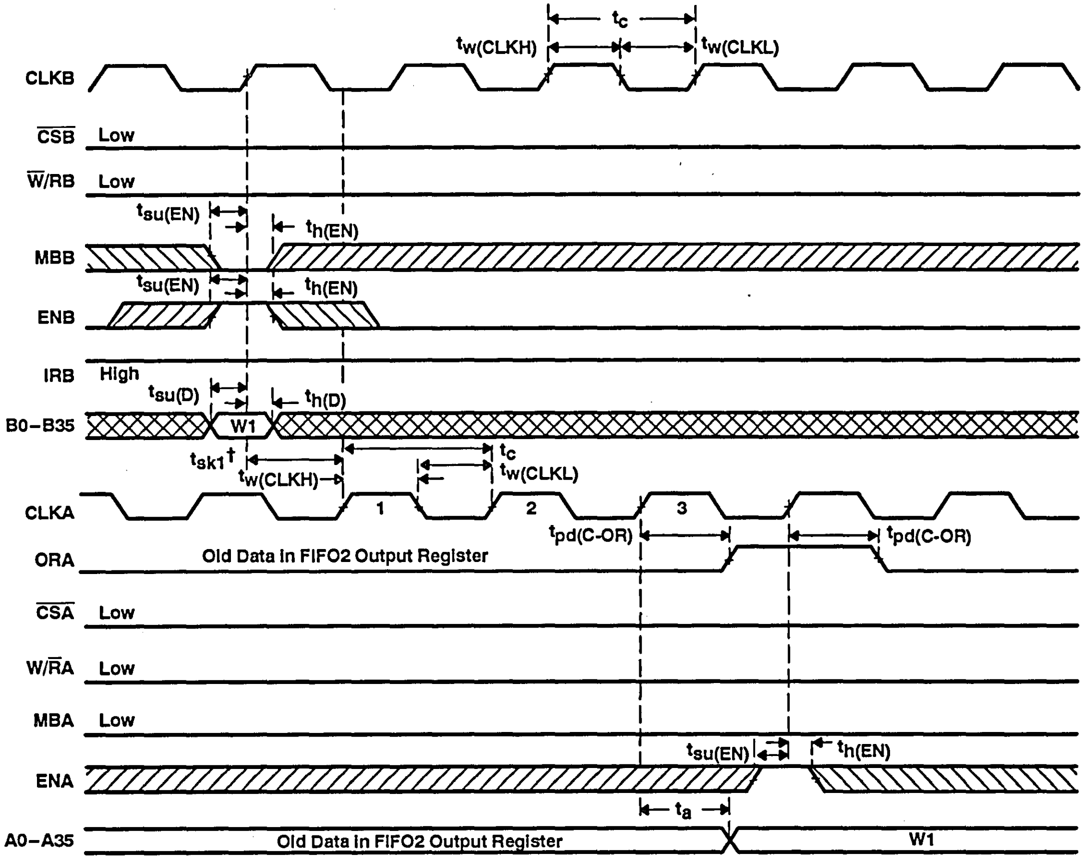
† Read from FIFO2

Figure 6. Port-A Read Cycle Timing for FIFO2



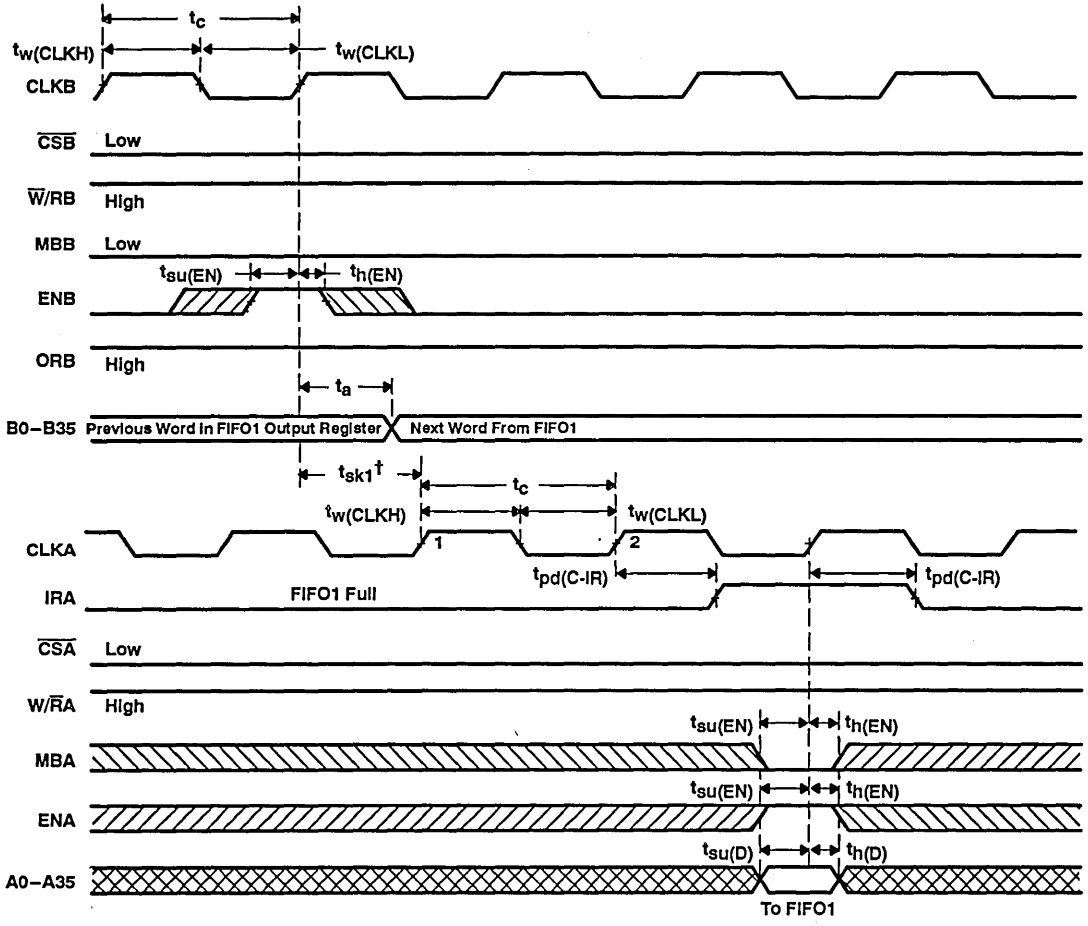
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 7. ORB-Flag Timing and First Data Word Fallthrough When FIFO1 Is Empty



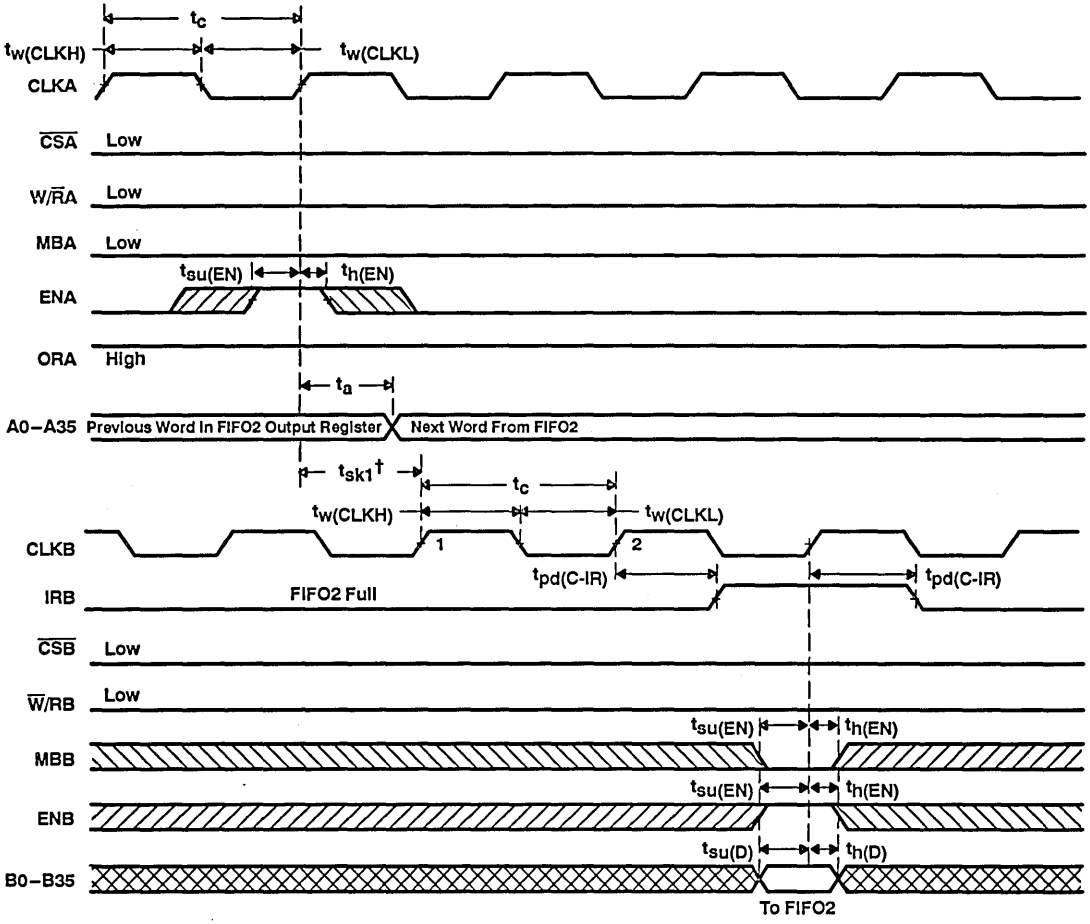
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 8. ORA-Flag Timing and First-Data-Word Fallthrough When FIFO2 Is Empty



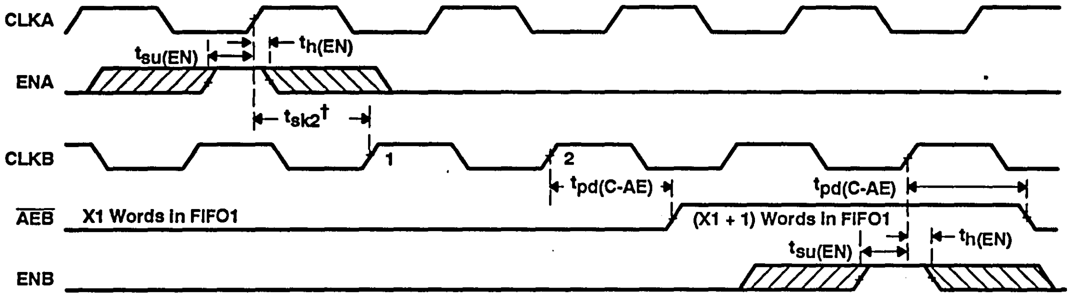
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then IRA may transition high one CLKA cycle later than shown.

Figure 9. IRA-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then IRB may transition high one CLKB cycle later than shown.

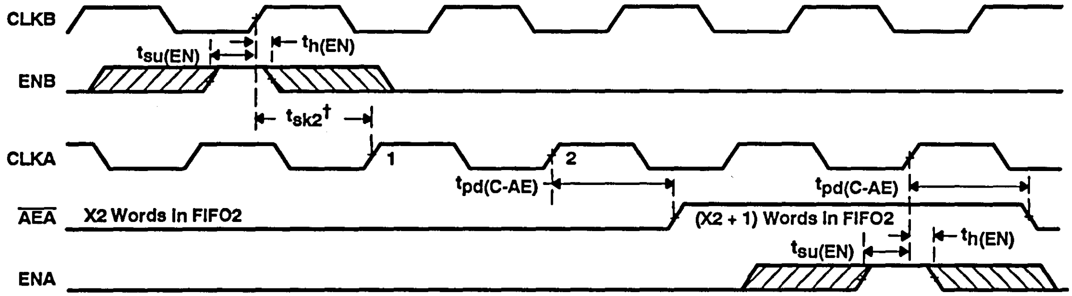
Figure 10. IRB-Flag Timing and First Available Write When FIFO2 Is Full



[†] t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{\text{AEB}}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{\text{AEB}}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = H, MBA = L), FIFO1 read ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

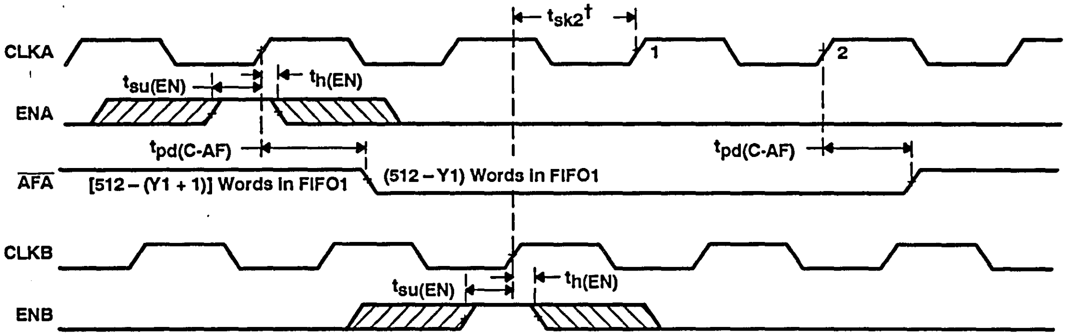
Figure 11. Timing for $\overline{\text{AEB}}$ When FIFO1 Is Almost Empty



[†] t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{\text{AEA}}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{\text{AEA}}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = L, MBB = L), FIFO2 read ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

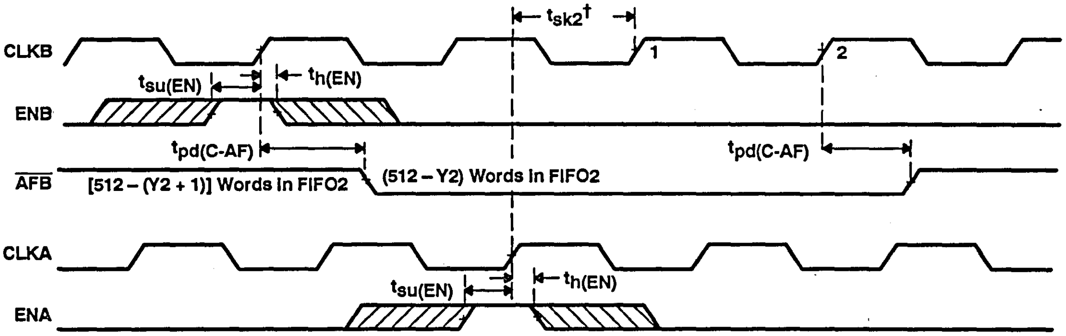
Figure 12. Timing for $\overline{\text{AEA}}$ When FIFO2 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

Figure 13. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB= L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 14. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full

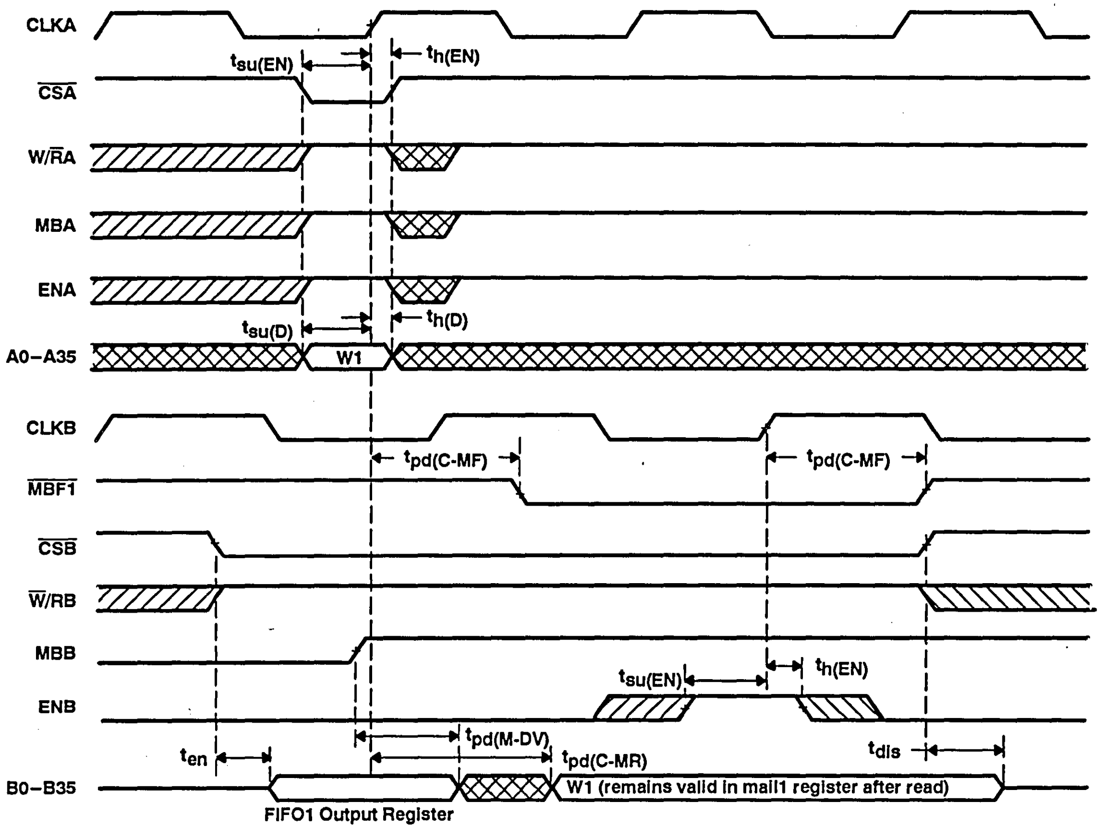


Figure 15. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

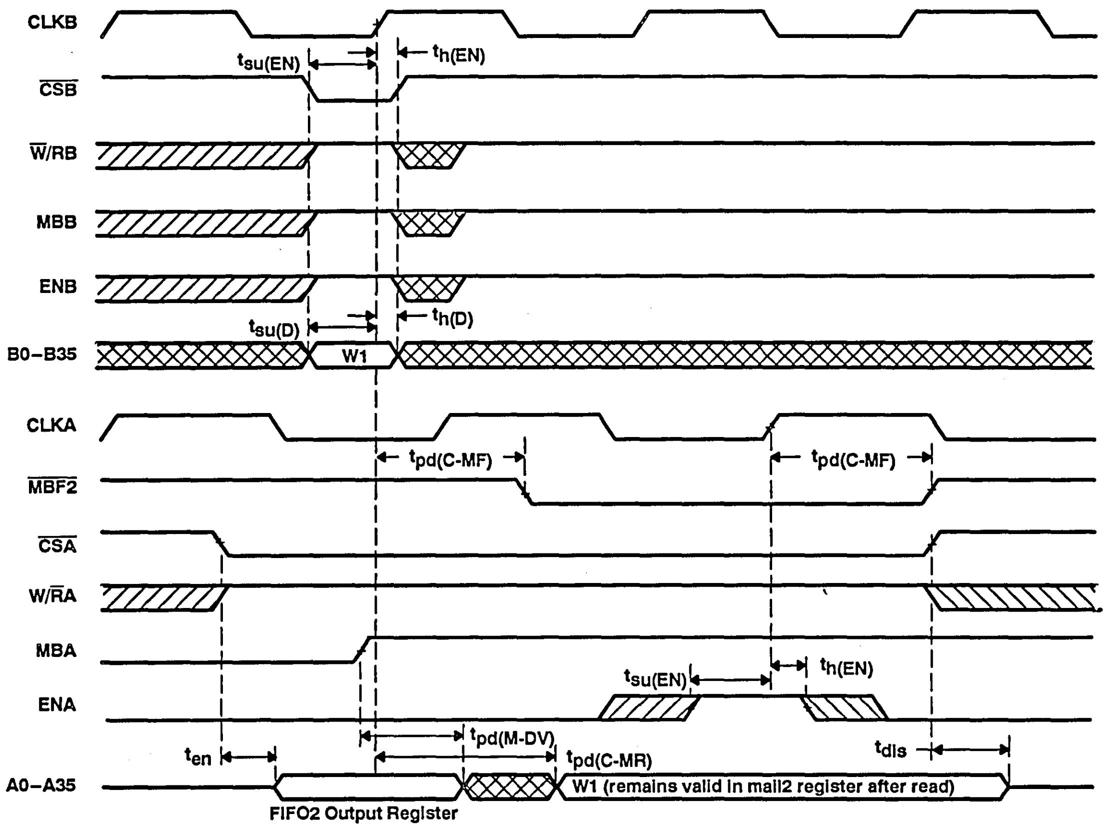


Figure 16. Timing for Mail2 Register and $\overline{MBF2}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0					±5	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0					±5	µA
I_{CC}	V_{CC} = 5.5 V,	$V_I = V_{CC}$ – 0.2 V or 0					400	µA
ΔI_{CC}‡	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{CSA} = V_{IH}$	A0–A35		0		mA
			$\overline{CSB} = V_{IH}$	B0–B35		0		
			$\overline{CSA} = V_{IL}$	A0–A35			1	
			$\overline{CSB} = V_{IL}$	B0–B35			1	
			All other inputs				1	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 16)

		'ACT3632-15		'ACT3632-20		'ACT3632-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		10		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		10		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB before CLKB↑	4.5		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST1}$ or $\overline{RST2}$ low before CLKA↑ or CLKB↑§	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ high	7.5		8.5		9.5		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	1		1		1		ns
$t_{h(RS)}$	Hold time, $\overline{RST1}$ or $\overline{RST2}$ low after CLKA↑ or CLKB↑§	4		4		5		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ high	2		3		3		ns
t_{sk1}¶	Skew time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	7.5		9		11		ns
t_{sk2}¶	Skew time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12		16		20		ns

§ Requirement to count the clock edge as one of at least four needed to reset a FIFO
¶ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 16)

PARAMETER		'ACT3632-15		'ACT3632-20		'ACT3632-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	3	11	3	13	3	15	ns
$t_{pd(C\text{-}IR)}$	Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB	2	8	2	10	2	12	ns
$t_{pd(C\text{-}OR)}$	Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{AEA}}$ and CLKB↑ to $\overline{\mathrm{AEB}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{AFA}}$ and CLKB↑ to $\overline{\mathrm{AFB}}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{MBF1}}$ low or $\overline{\mathrm{MBF2}}$ high and CLKB↑ to $\overline{\mathrm{MBF2}}$ low or $\overline{\mathrm{MBF1}}$ high	0	8	0	10	0	12	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	13.5	3	15	3	17	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid	3	11	3	13	3	15	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\mathrm{RST1}}$ low to $\overline{\mathrm{AEB}}$ low, $\overline{\mathrm{AFA}}$ high, and $\overline{\mathrm{MBF1}}$ high, and $\overline{\mathrm{RST2}}$ low to $\overline{\mathrm{AEA}}$ low, $\overline{\mathrm{AFB}}$ high, and $\overline{\mathrm{MBF2}}$ high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{\mathrm{CSA}}$ and W/$\overline{\mathrm{RA}}$ low to A0–A35 active and $\overline{\mathrm{CSB}}$ low and $\overline{\mathrm{W}}$/RB high to B0–B35 active	2	12	2	13	2	14	ns
t_{dis}	Disable time, $\overline{\mathrm{CSA}}$ or W/$\overline{\mathrm{RA}}$ high to A0–A35 at high impedance and $\overline{\mathrm{CSB}}$ high or $\overline{\mathrm{W}}$/RB low to B0–B35 at high impedance	1	8	1	12	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

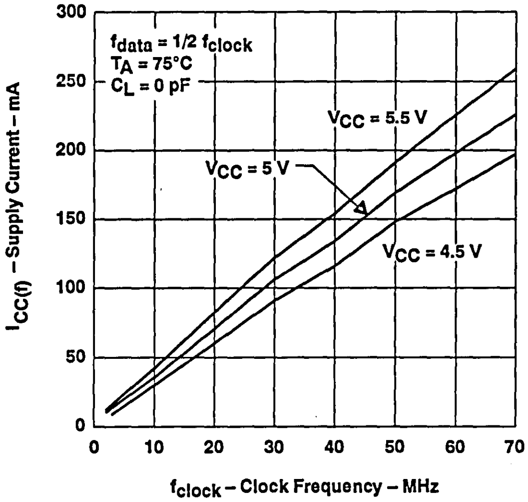


Figure 17

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 17 was taken while simultaneously reading and writing a FIFO on the SN74ACT3632 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel and the number of SN74ACT3632 inputs driven by TTL high levels are known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 17, the maximum power dissipation (P_T) of the SN74ACT3632 can be calculated by:

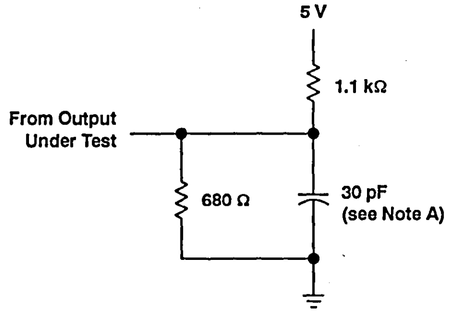
$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:
N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

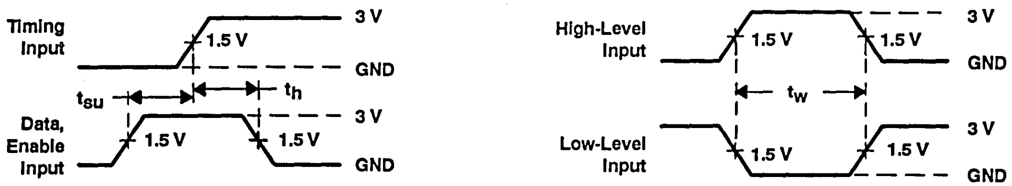
When no reads or writes are occurring on the SN74ACT3632, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.184 \text{ mA/MHz}$$

PARAMETER MEASUREMENT INFORMATION

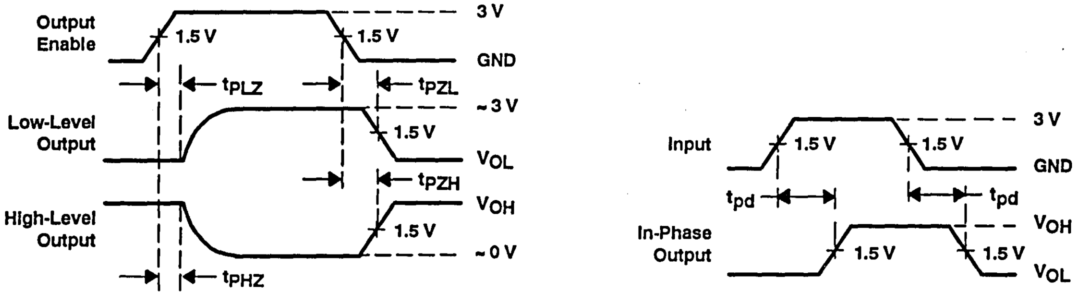


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

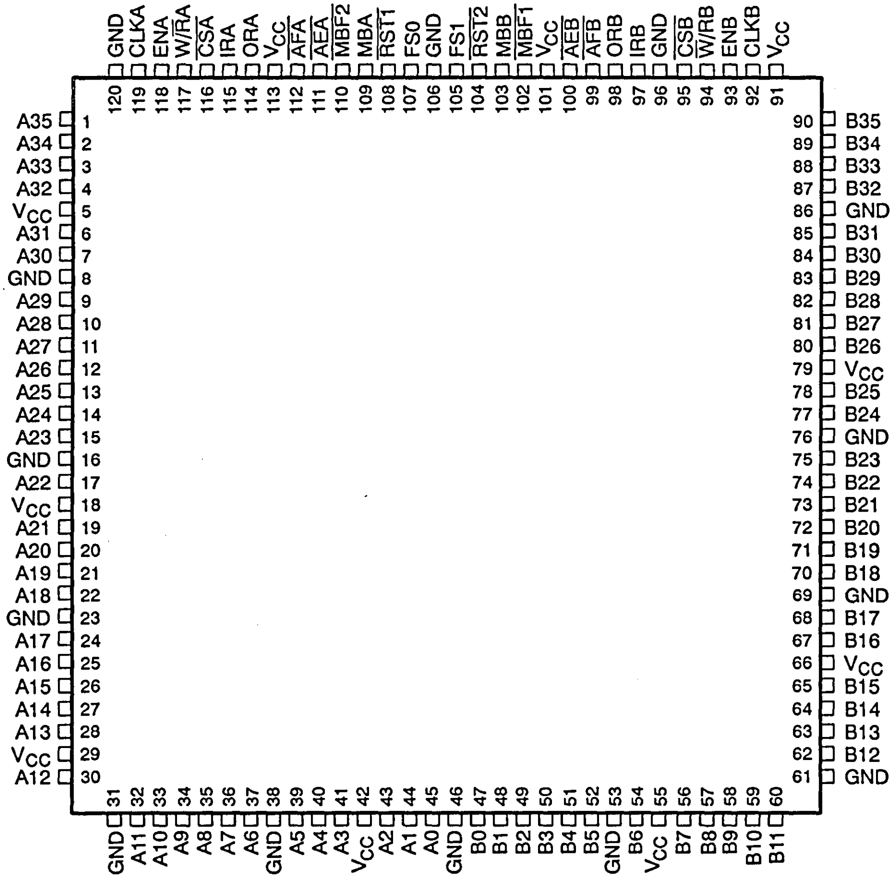
Figure 18. Load Circuit and Voltage Waveforms

SN74ACT3642
1024 × 36 × 2
CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS440 – JUNE 1994

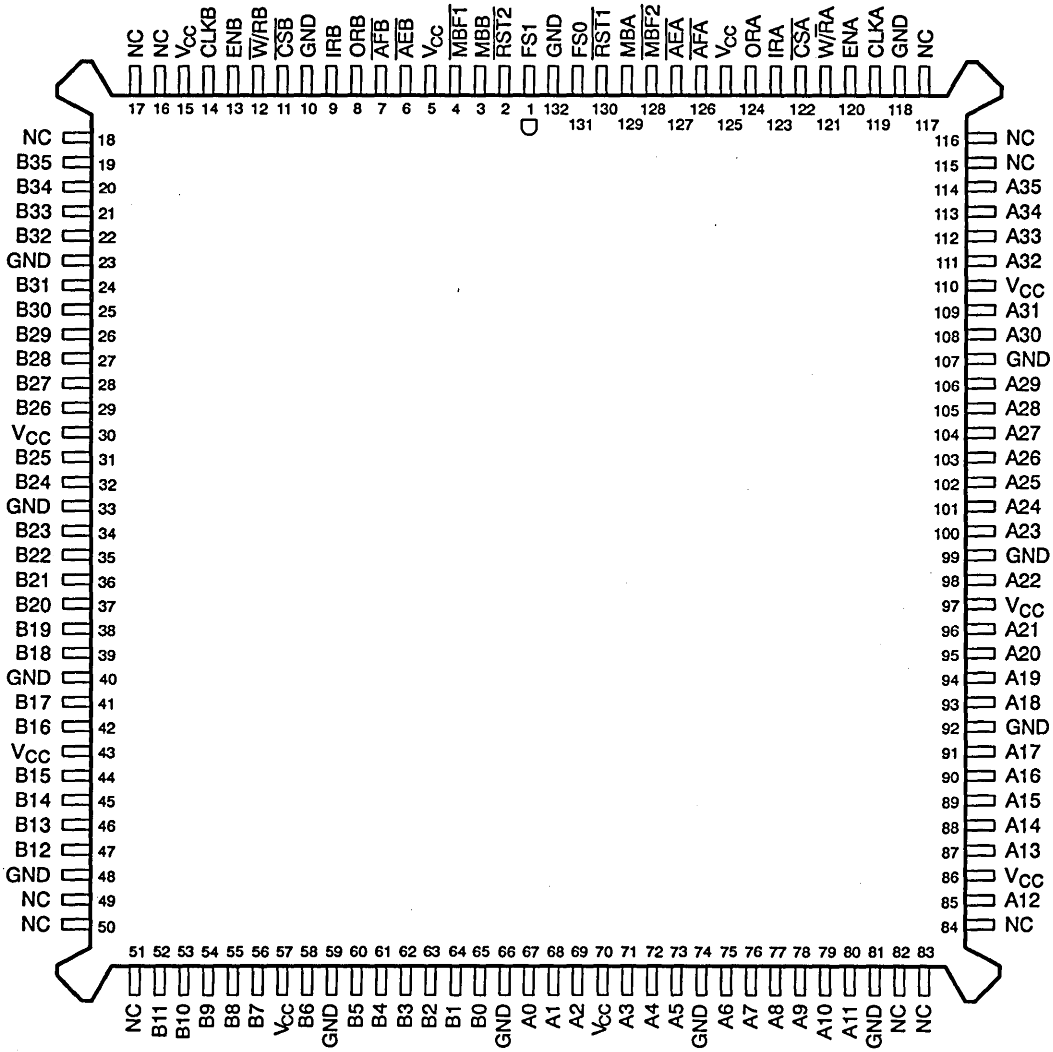
- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Two Independent Clocked FIFOs Buffering Data in Opposite Directions
- Mailbox Bypass Register for Each FIFO
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA
- IRB, ORB, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Pin-to-Pin Compatible With the SN74ACT3622 and SN74ACT3632
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)

PCB PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

PRODUCT PREVIEW

description

The SN74ACT3642 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz with read access times as fast as 11 ns. The two independent 1024 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFO via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths.

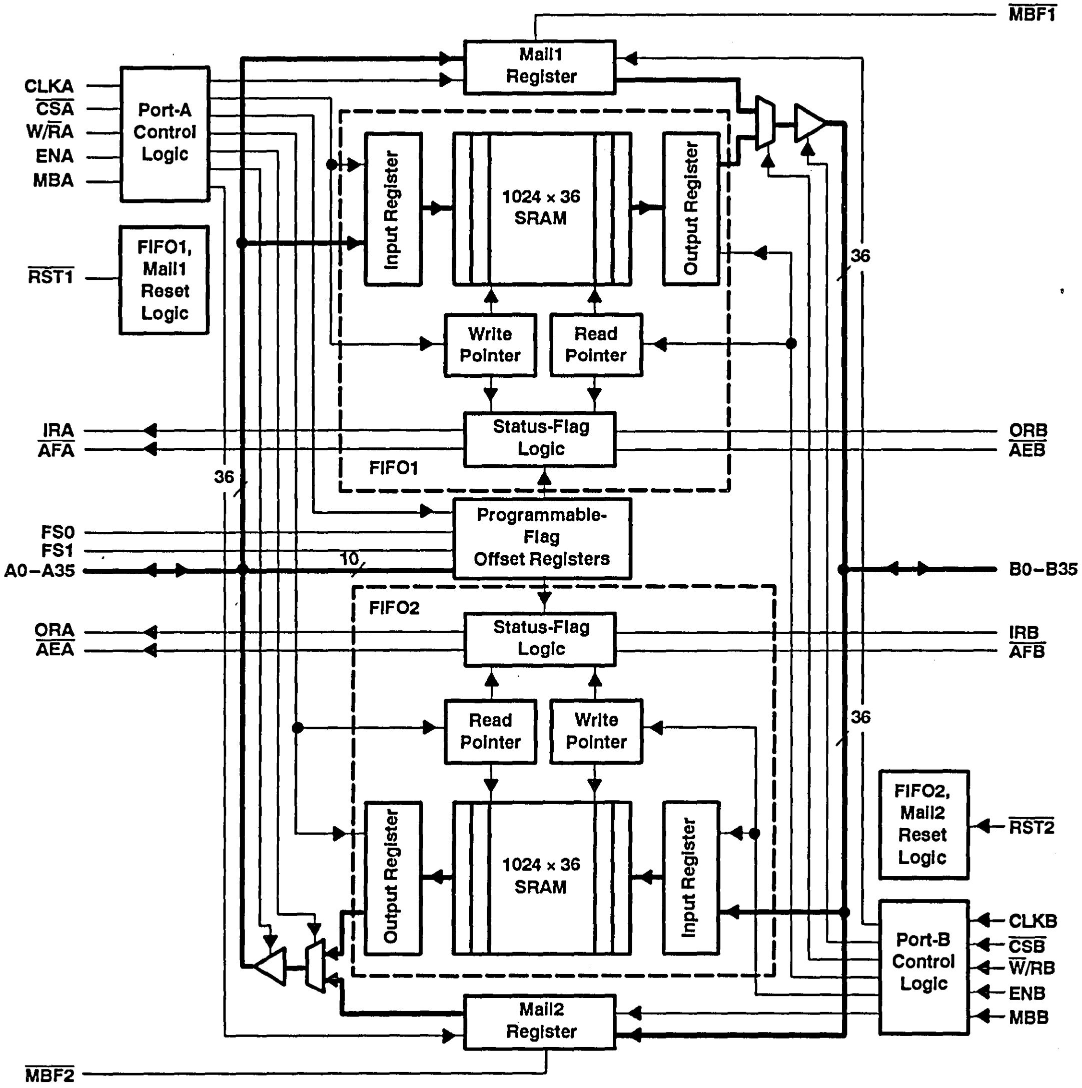
The SN74ACT3642 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input-ready (IRA, IRB) flag and almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output-ready (ORA, ORB) flag and almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the almost-full and almost-empty flags of the FIFO can be programmed from port A.

The SN74ACT3642 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AEA}}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{\text{AEA}}$ is low when the number of words in FIFO2 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{\text{AEB}}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\text{AEB}}$ is low when the number of words in FIFO1 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{\text{AFA}}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\text{AFA}}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{\text{AFB}}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{\text{AFB}}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the almost-full B offset register, Y2.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{\text{AFA}}$, and $\overline{\text{AEA}}$ are all synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{\text{AFB}}$, and $\overline{\text{AEB}}$ are synchronized to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag offset selects. The low-to-high transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO almost-full and almost-empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFOs.
IRA	O (port A)	Input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O (port B)	Input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output-register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output-register data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\text{MBF1}}$ is low. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high when FIFO1 is reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\text{MBF2}}$ is low. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is also set high when FIFO2 is reset.
ORA	O (port A)	Output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

PRODUCT PREVIEW

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
ORB	O (port B)	Output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{\mathrm{RST1}}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\mathrm{RST1}}$ is low. The low-to-high transition of $\overline{\mathrm{RST1}}$ latches the status of FS0 and FS1 for $\overline{\mathrm{AFA}}$ and $\overline{\mathrm{AEB}}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{\mathrm{RST2}}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\mathrm{RST2}}$ is low. The low-to-high transition of $\overline{\mathrm{RST2}}$ latches the status of FS0 and FS1 for $\overline{\mathrm{AFB}}$ and $\overline{\mathrm{AEA}}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{\mathrm{RA}}$	I	Port-A write/read select. A high on W/$\overline{\mathrm{RA}}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\mathrm{RA}}$ is high.
$\overline{\mathrm{W}}$/RB	I	Port-B write/read select. A low on $\overline{\mathrm{W}}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{\mathrm{W}}$/RB is low.

detailed description

reset

The FIFO memories of the SN74ACT3642 are reset separately by taking their reset ($\overline{\mathrm{RST1}}$, $\overline{\mathrm{RST2}}$) inputs low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready flag (IRA, IRB) low, the output-ready flag (ORA, ORB) low, the almost-empty flag ($\overline{\mathrm{AEA}}$, $\overline{\mathrm{AEB}}$) low, and the almost-full flag ($\overline{\mathrm{AFA}}$, $\overline{\mathrm{AFB}}$) high. Resetting a FIFO also forces the mailbox flag ($\overline{\mathrm{MBF1}}$, $\overline{\mathrm{MBF2}}$) of the parallel mailbox register high. After a FIFO is reset, its input-ready flag is set high after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A low-to-high transition on a FIFO reset ($\overline{\mathrm{RST1}}$, $\overline{\mathrm{RST2}}$) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method (see *almost-empty and almost-full flag offset programming*).

almost-empty flag and almost-full flag offset programming

Four registers in the SN74ACT3642 are used to hold the offset values for the almost-empty and almost-full flags. The port-B almost-empty flag ($\overline{\mathrm{AEB}}$) offset register is labeled X1 and the port-A almost-empty flag ($\overline{\mathrm{AEA}}$) offset register is labeled X2. The port-A almost-full flag ($\overline{\mathrm{AFA}}$) offset register is labeled Y1 and the port-B almost-full flag ($\overline{\mathrm{AFB}}$) offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{\mathrm{RST1}}$	$\overline{\mathrm{RST2}}$	X1 AND Y1 REGISTERS†	X2 AND Y2 REGISTERS‡
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

† X1 register holds the offset for $\overline{\mathrm{AEB}}$; Y1 register holds the offset for $\overline{\mathrm{AFA}}$.
‡ X2 register holds the offset for $\overline{\mathrm{AEA}}$; Y2 register holds the offset for $\overline{\mathrm{AFB}}$.

almost-empty flag and almost-full flag offset programming (continued)

To load a FIFO almost-empty flag and almost-full flag offset registers with one of the three preset values listed in Table 1, at least one of the flag-select inputs must be high during the low-to-high transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be high when FIFO1 reset ($\overline{\text{RST1}}$) returns high. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{\text{RST2}}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. Each offset register uses port-A inputs (A9–A0). The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 1020. After all the offset registers are programmed from port A, the port-B input-ready flag (IRB) is set high and both FIFOs begin normal operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{RA}}$). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are low.

Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is high, ENA is high, MBA is low, and IRA is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is low, ENA is high, MBA is low, and ORA is high (see Table 2). FIFO reads and writes on port A are independent of any concurrent port-B operation.

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{RA}}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{\text{W}}$/RB) is the inverse of the port-A write/read select (W/$\overline{\text{RA}}$). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select ($\overline{\text{W}}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ is high or $\overline{\text{W}}$/RB is low. The B0–B35 outputs are active when $\overline{\text{CSB}}$ is low and $\overline{\text{W}}$/RB is high.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is low, ENB is high, MBB is low, and IRB is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, $\overline{\text{W}}$/RB is high, ENB is high, MBB is low, and ORB is high (see Table 3). FIFO reads and writes on port B are independent of any concurrent port-A operation.

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FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{CSB}$	$W/\overline{RB}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup and hold time constraints to the port clocks for the port chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select may change states during the setup and hold time window of the cycle.

When a FIFO output-ready flag is low, the next data word is sent to the FIFO output register automatically by the low-to-high transition of the port clock that sets the output-ready flag high. When the output-ready flag is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port's chip select, write/read select, enable, and mailbox select.

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). ORA, $\overline{AEA}$, IRA, and $\overline{AFA}$ are synchronized to CLKA. ORB, $\overline{AEB}$, IRB, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1[†‡]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	ORB	$\overline{AEB}$	$\overline{AFA}$	IRA
0	L	L	H	H
1 to X1	H	L	H	H
(X1 + 1) to [1024 – (Y1 + 1)]	H	H	H	H
(1024 – Y1) to 1023	H	H	L	H
1024	H	H	L	L

[†] X1 is the almost-empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the almost-full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.

[‡] When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

synchronized FIFO flags (continued)

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2[†][‡]	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORA	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	IRB
0	L	L	H	H
1 to X2	H	L	H	H
(X2 + 1) to [1024 – (Y2 + 1)]	H	H	H	H
(1024 – Y2) to 1023	H	H	L	H
1024	H	H	L	L

[†] X2 is the almost-empty offset for FIFO2 used by $\overline{\text{AEA}}$. Y2 is the almost-full offset for FIFO2 used by $\overline{\text{AFB}}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

[‡] When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

output-ready flags (ORA, ORB)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the output-ready flag synchronizing clock; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of the synchronizing clock occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on an output-ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

input-ready flags (IRA, IRB)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the input-ready flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the input-ready flag synchronizing clock; therefore, an input-ready flag is low if less than two cycles of the input-ready flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the input-ready flag synchronizing clock after the read sets the input-ready flag high.

A low-to-high transition on an input-ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-empty flag is low when its FIFO contains X or less words and is high when its FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for its almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-full flag is low when the number of words in its FIFO is greater than or equal to (1024 – Y) for the SN74ACT3622 or (1024 – Y) for the SN74ACT3642. An almost-full flag is high when the number of words in its FIFO is less than or equal to [1024 – (Y + 1)] for the SN74ACT3622 or [1024 – (Y + 1)] for the SN74ACT3642. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for its almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [1024 – (Y + 1)] or less words remains low if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [1024 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [1024 – (Y + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [1024 – (Y + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port mailbox select input is low and from the mail register when the port-mailbox select input is high. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

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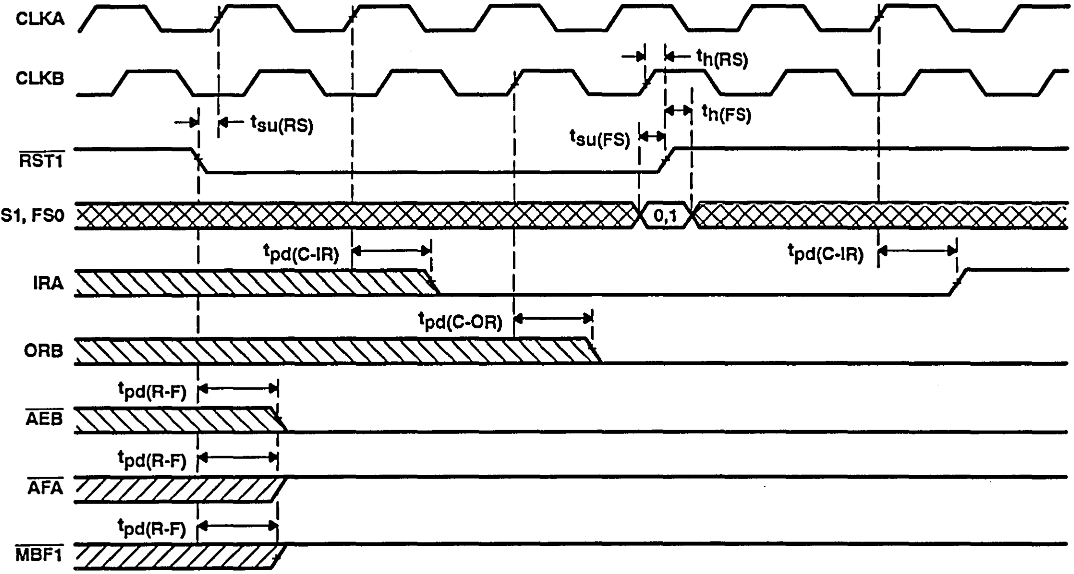
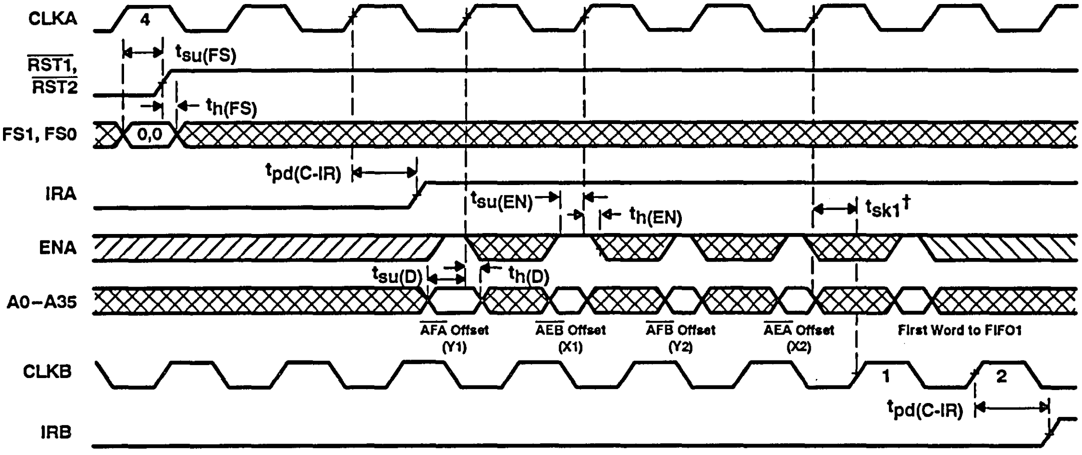


Figure 1. FIFO1 Reset Loading X1 and Y1 With a Preset Value of Eight†

† FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



† t_{sk1} is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition high in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{sk1}, then IRB may transition high one cycle later than shown.

NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values After Reset

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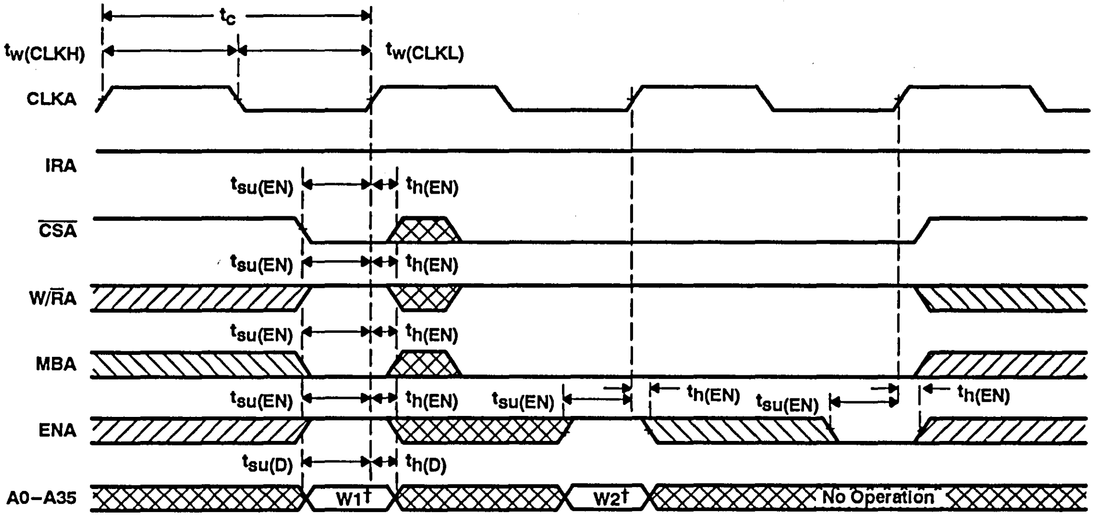
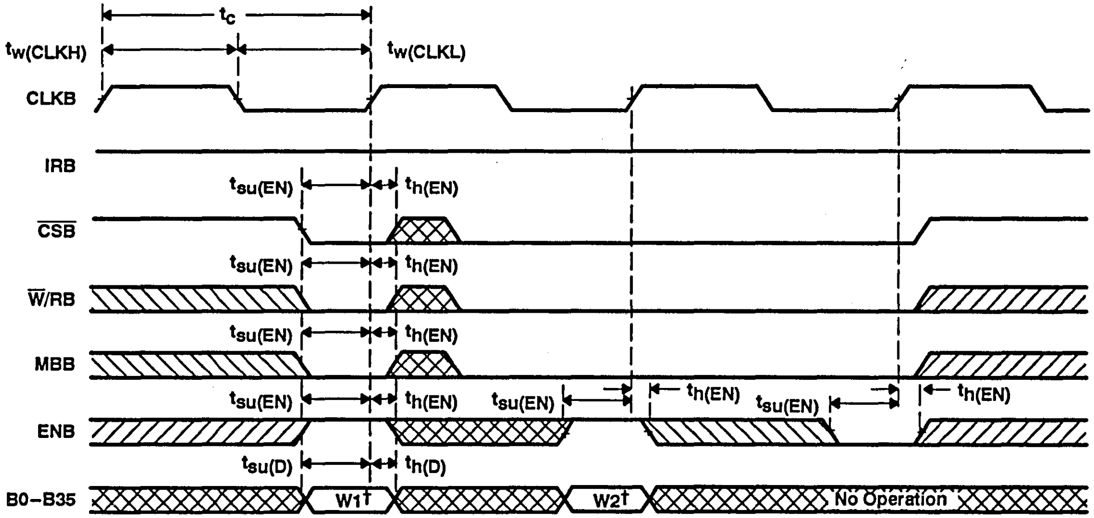


† Written to FIFO1

Figure 3. Port-A Write Cycle Timing for FIFO1



† Written to FIFO2

Figure 4. Port-B Write Cycle Timing for FIFO2

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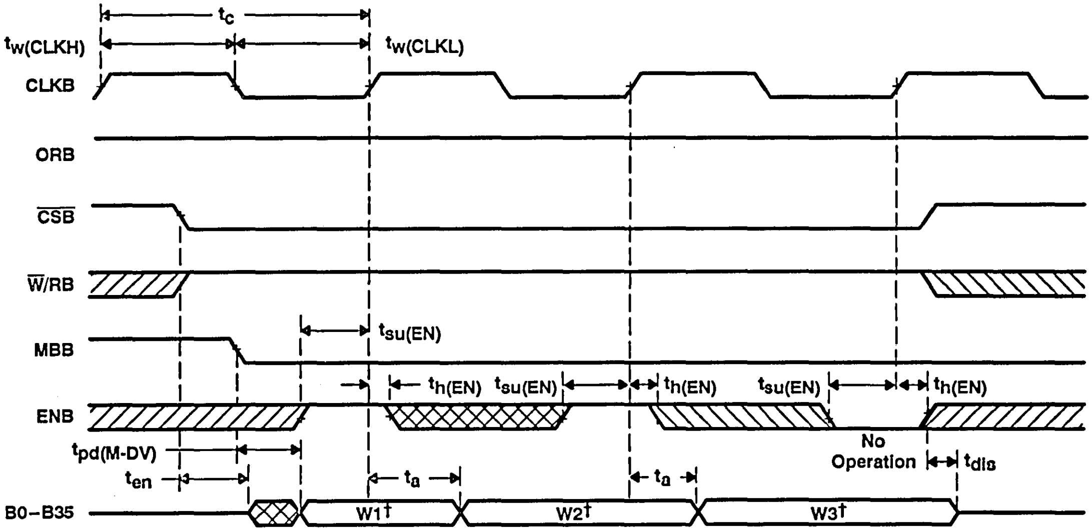
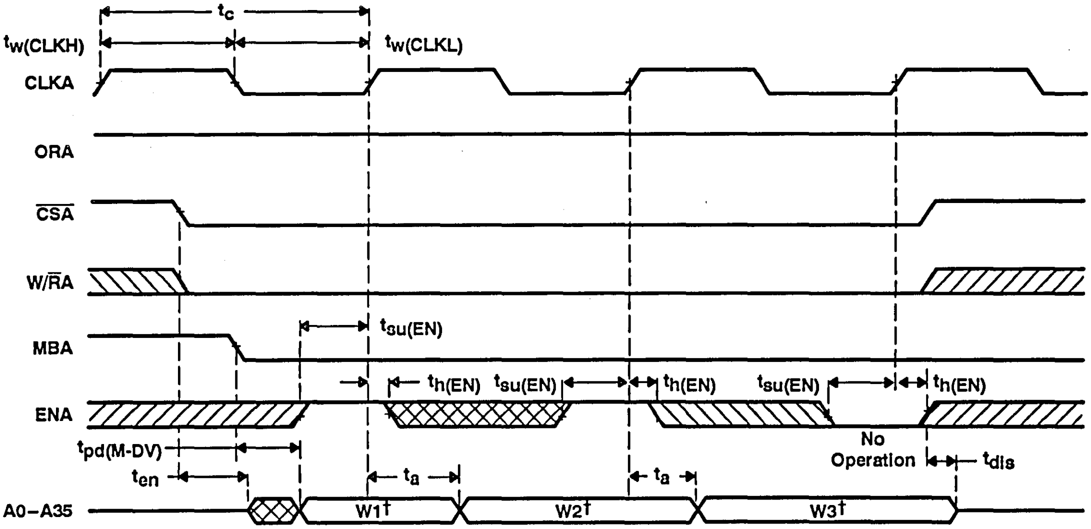


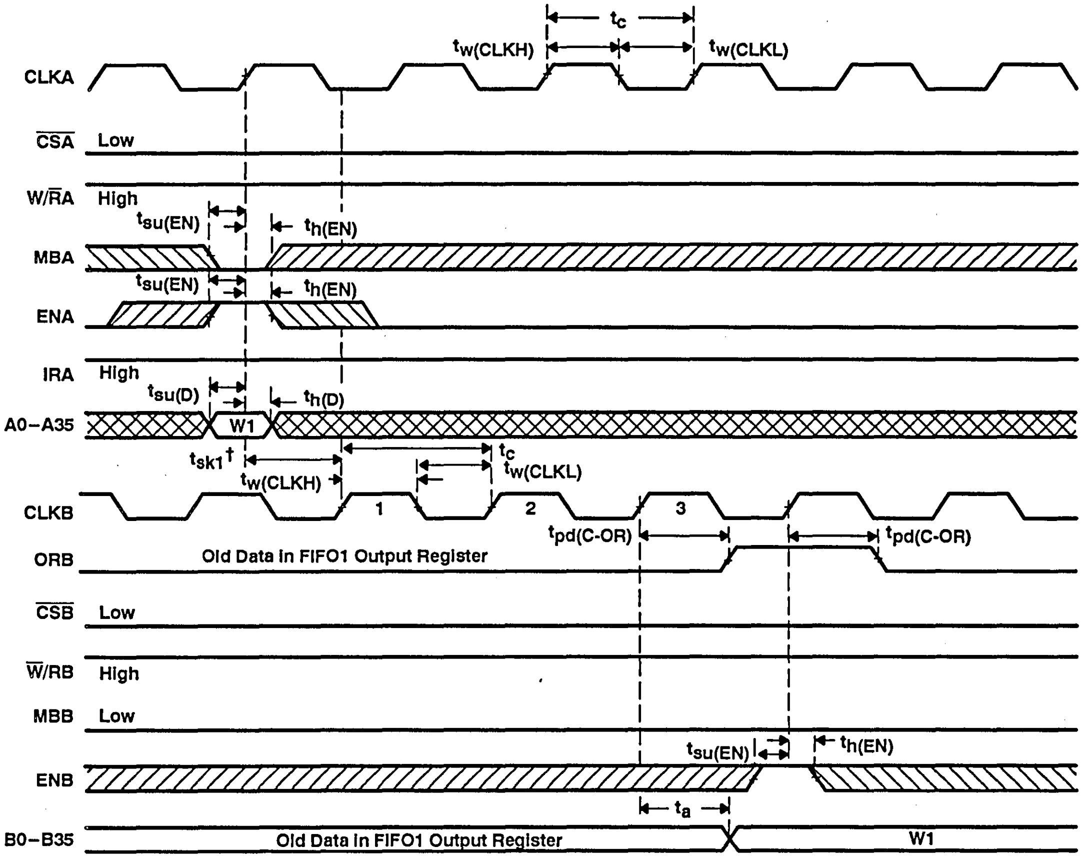
† Read from FIFO1

Figure 5. Port-B Read Cycle Timing for FIFO1



† Read from FIFO2

Figure 6. Port-A Read Cycle Timing for FIFO2



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 7. ORB-Flag Timing and First Data Word Fallthrough When FIFO1 Is Empty

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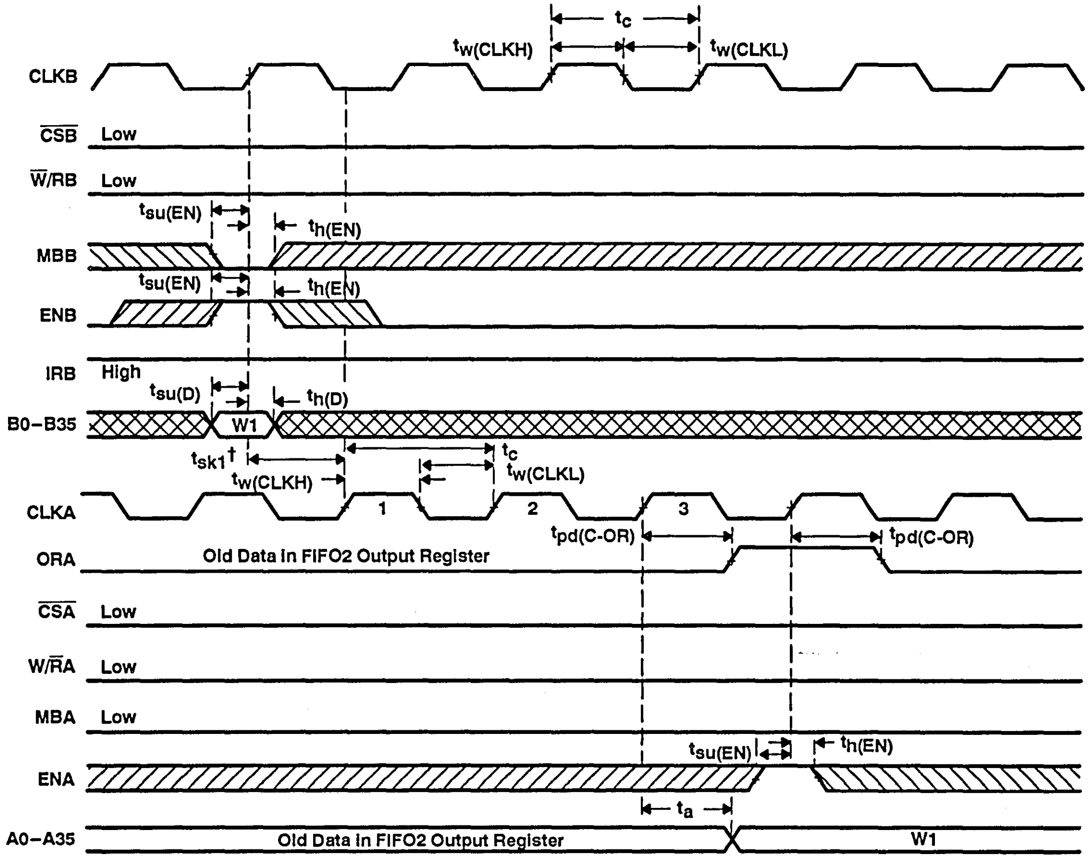

† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 8. ORA-Flag Timing and First Data Word Fallthrough When FIFO2 Is Empty

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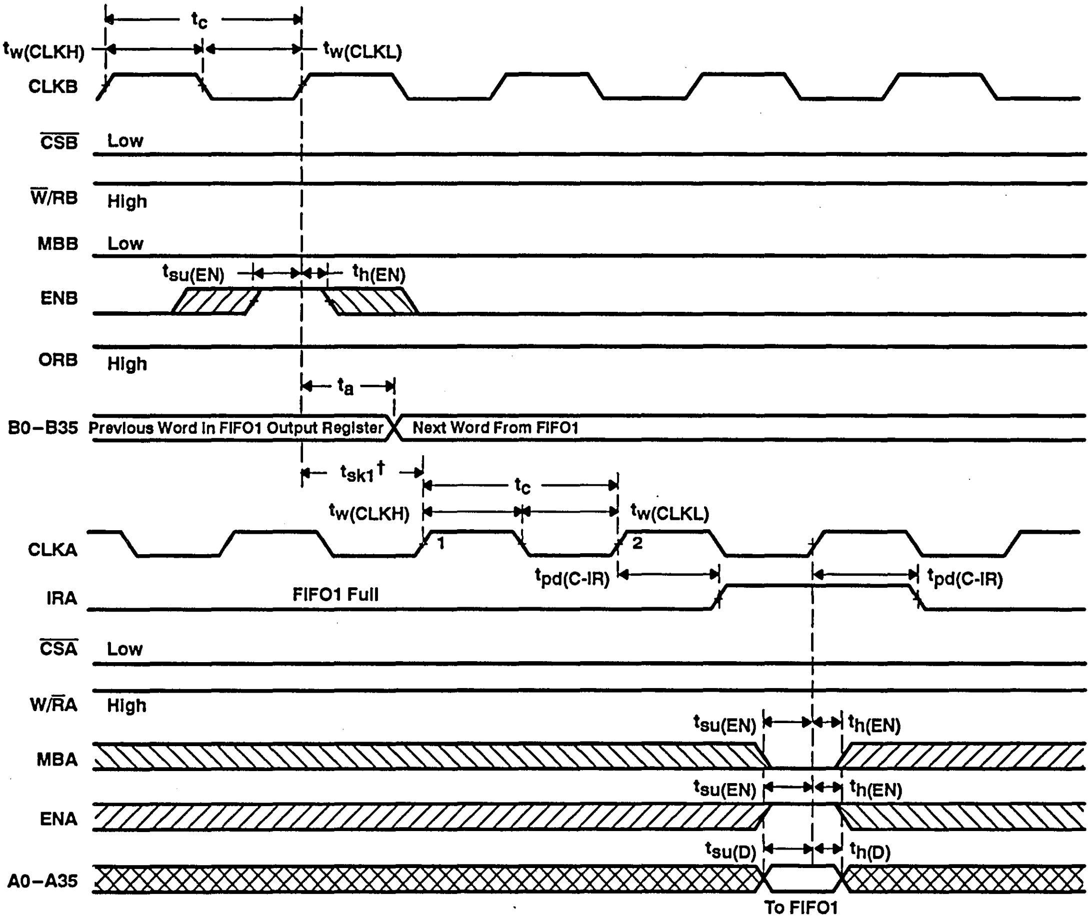
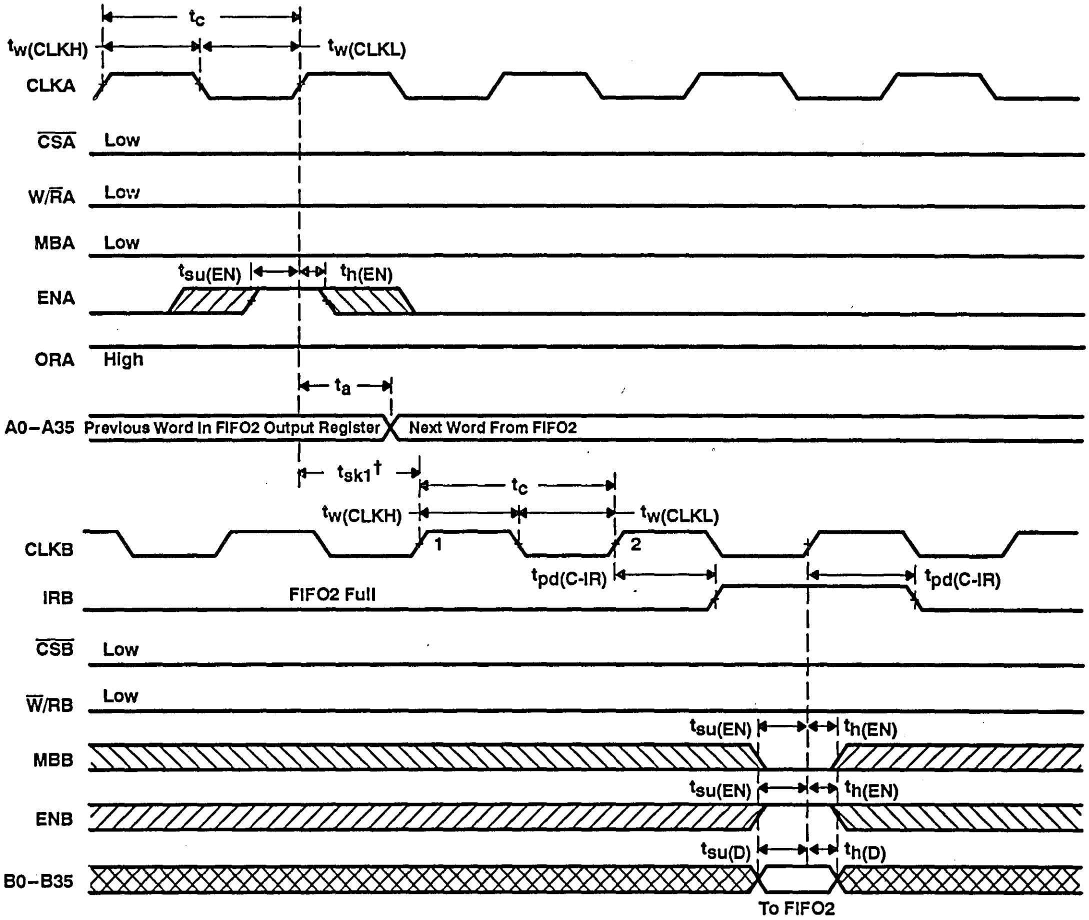


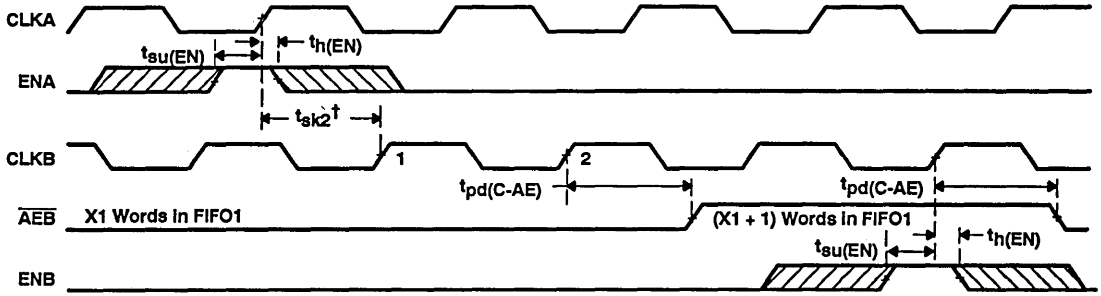
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then IRA may transition high one CLKA cycle later than shown.

Figure 9. IRA-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then IRB may transition high one CLKB cycle later than shown.

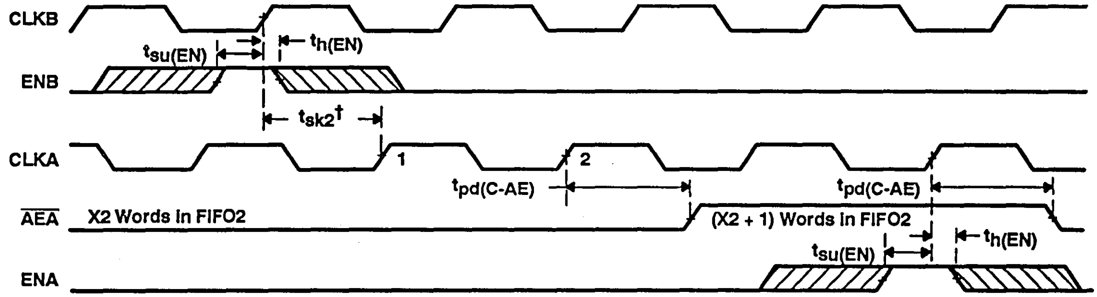
Figure 10. IRB-Flag Timing and First Available Write When FIFO2 Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{\text{AEB}}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{\text{AEB}}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = H, MBA = L), FIFO1 read ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

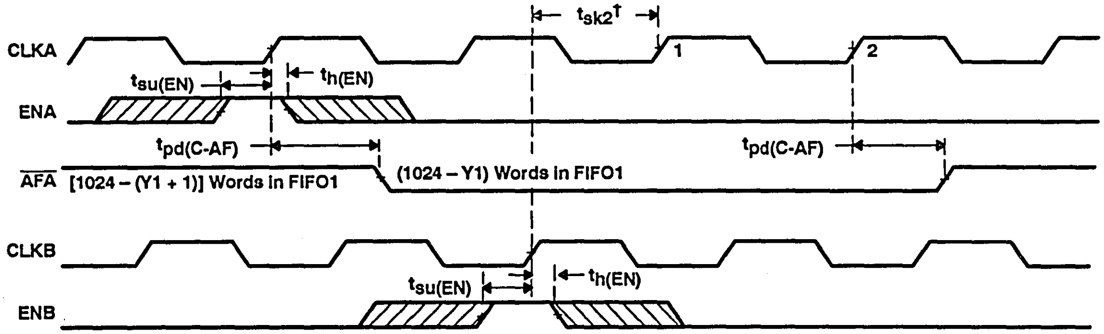
Figure 11. Timing for $\overline{\text{AEB}}$ When FIFO1 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{\text{AEA}}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{\text{AEA}}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{\text{CSB}}$ = L, $\overline{\text{W}}$/RB = L, MBB = L), FIFO2 read ($\overline{\text{CSA}}$ = L, W/$\overline{\text{RA}}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

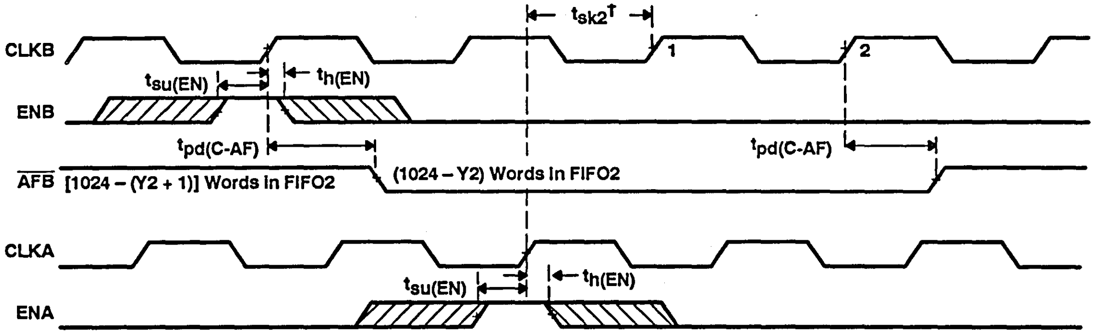
Figure 12. Timing for $\overline{\text{AEA}}$ When FIFO2 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

Figure 13. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB= L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 14. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full

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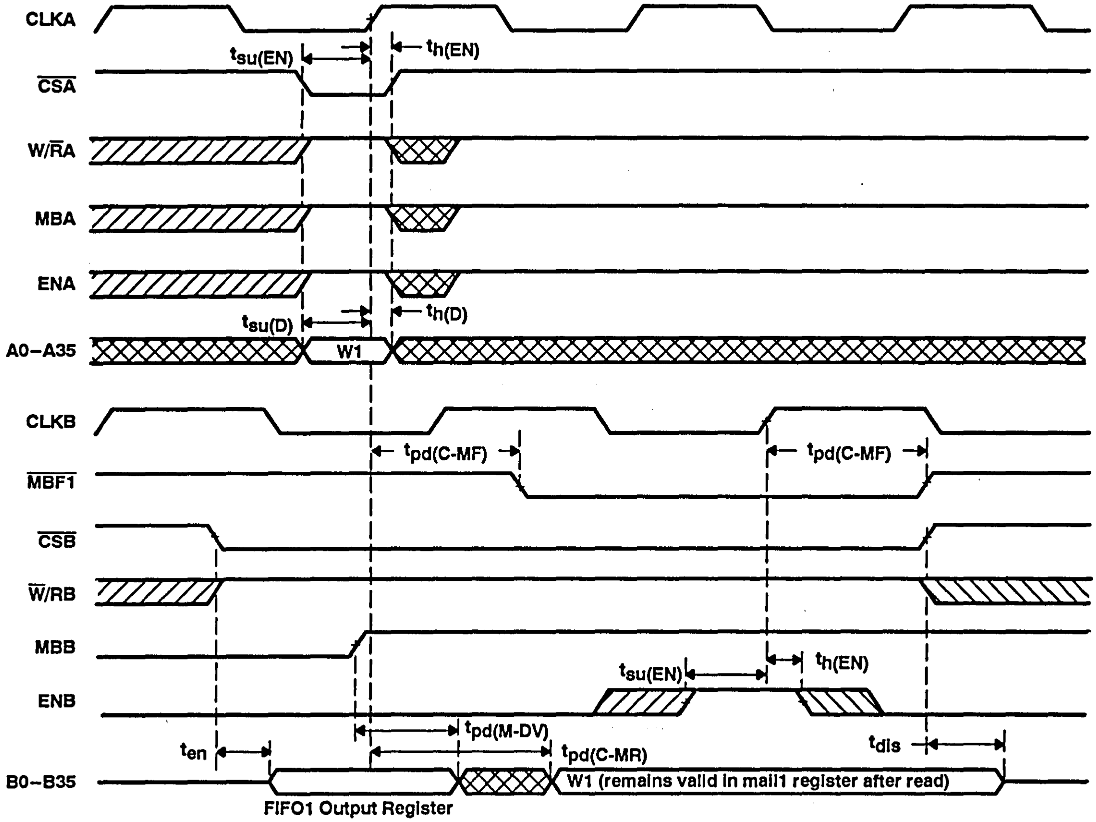

Figure 15. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

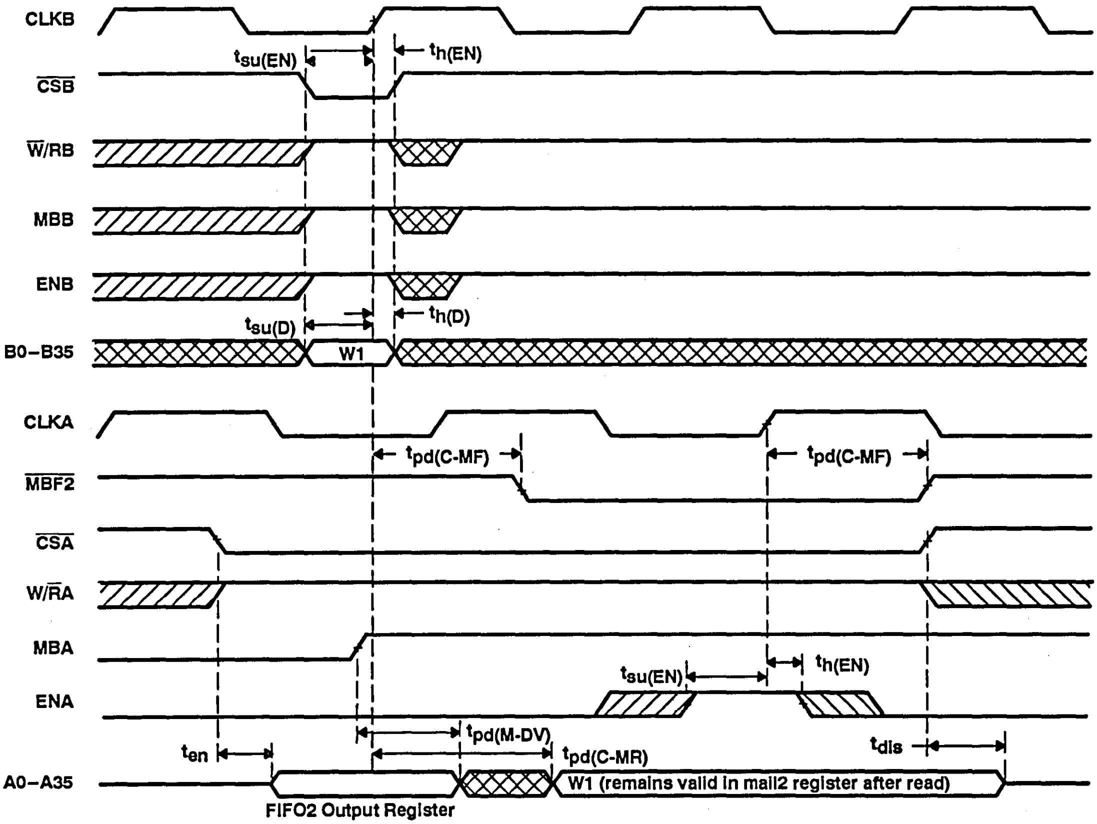

Figure 16. Timing for Mail2 Register and $\overline{MBF2}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±5	μA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±5	μA
I_{CC}	V_{CC} = 5.5 V,	V_I = V_{CC} − 0.2 V or 0					400	μA
ΔI_{CC}‡	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{CSA}$ = V_{IH}	A0–A35		0		mA
			$\overline{CSB}$ = V_{IH}	B0–B35		0		
			$\overline{CSA}$ = V_{IL}	A0–A35			1	
			$\overline{CSB}$ = V_{IL}	B0–B35			1	
			All other inputs				1	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 16)

		'ACT3642-15		'ACT3642-20		'ACT3642-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		10		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		10		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB before CLKB↑	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST1}$ or $\overline{RST2}$ low before CLKA↑ or CLKB↑§	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST1}$ or $\overline{RST2}$ low after CLKA↑ or CLKB↑§	4		4		5		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ high	2		3		3		ns
t_{sk1}¶	Skew time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	6		8		10		ns
t_{sk2}¶	Skew time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12		16		20		ns

§ Requirement to count the clock edge as one of at least four needed to reset a FIFO

¶ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 16)

PARAMETER		'ACT3642-15		'ACT3642-20		'ACT3642-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35		11		13		15	ns
$t_{pd(C\text{-}IR)}$	Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB		11		13		15	ns
$t_{pd(C\text{-}OR)}$	Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB		11		13		15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{\text{AEA}}$ and CLKB↑ to $\overline{\text{AEB}}$		11		13		15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\text{AFA}}$ and CLKB↑ to $\overline{\text{AFB}}$		11		13		15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\text{MBF1}}$ low or $\overline{\text{MBF2}}$ high and CLKB↑ to $\overline{\text{MBF2}}$ low or $\overline{\text{MBF1}}$ high		11		13		15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35[†] and CLKB↑ to A0–A35[‡]		11		13		15	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid		9		11		13	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\text{RST1}}$ low to $\overline{\text{AEB}}$ low, $\overline{\text{AFA}}$ high, and $\overline{\text{MBF1}}$ high, and $\overline{\text{RST2}}$ low to $\overline{\text{AEA}}$ low, $\overline{\text{AFB}}$ high, and $\overline{\text{MBF2}}$ high		15		20		30	ns
t_{en}	Enable time, $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ low to A0–A35 active and $\overline{\text{CSB}}$ low and $\overline{\text{W}}$/RB high to B0–B35 active		10		12		14	ns
t_{dis}	Disable time, $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ high to A0–A35 at high impedance and $\overline{\text{CSB}}$ high or $\overline{\text{W}}$/RB low to B0–B35 at high impedance		10		12		14	ns

[†] Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
[‡] Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

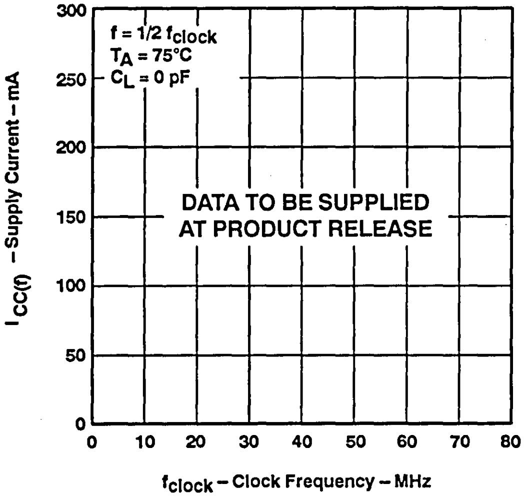

Figure 17

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 17, the maximum power dissipation (P_T) of the SN74ACT3622/3642 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

N = number of inputs driven by TTL levels
ΔI_{CC} = increase in power supply current for each input at a TTL high level
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_L = output capacitive load
f_o = switching frequency of an output

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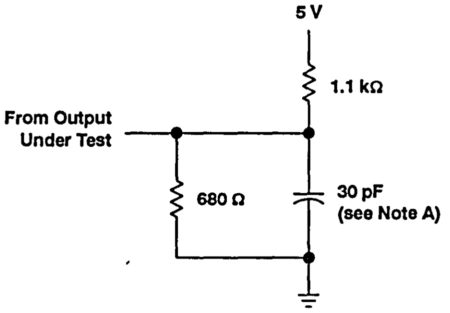
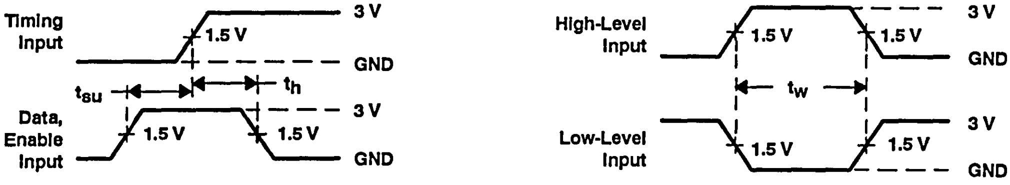
PARAMETER MEASUREMENT INFORMATION

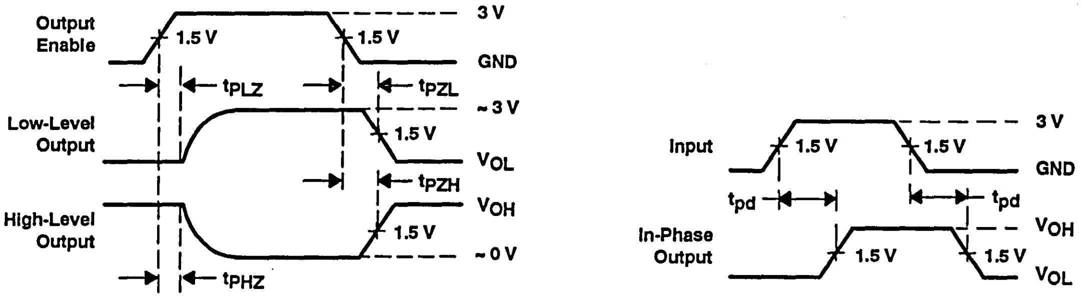


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 18. Load Circuit and Voltage Waveforms

INTERNETWORKING 36-BIT CLOCKED FIFOS

Features	Benefits
36-bit FIFO interface	Single-chip implementation for high levels of integration
Bidirectional option	Two dual-port SRAMs allows true bidirectional capability
Mailbox-register bypass	Quick access to priority information
Microprocessor-control circuitry	Interface matches most processors and DSP bus cycle timing and communications
Separate programmable AF and AE flags as well as multiple default values for separate AF and AE flags	Easy alternatives for flag settings
Byte swapping/bus matching	Allows for smooth interface between multiple processors or buses
Parity generation and check	Ensures valid data
TI has established alternate source options	67% less board space than equivalent 132-pin PQFPs; over 66% less board space than four 9-bit, 32-pin PLCC equivalents

SN74ABT3613
64 × 36 CLOCKED FIRST-IN, FIRST-OUT MEMORY WITH BUS MATCHING AND BYTE SWAPPING

SCBS128C – JULY 1992 – REVISED MARCH 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **64 × 36 FIFO Buffering Data From Port A to Port B**
- **Mailbox Bypass Registers in Each Direction**
- **Dynamic Port-B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte-Order Swapping on Port B**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{FF}$ and $\overline{AF}$ Flags Synchronized by CLKA**
- **$\overline{EF}$ and $\overline{AE}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Quad Flat Package (PQ)**

description

The SN74ABT3613 is a high-speed, low-power BiCMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. A 64 × 36 dual-port SRAM FIFO on board the chip buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B can be output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus-size selection. Communication between each port can bypass the FIFO via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port.

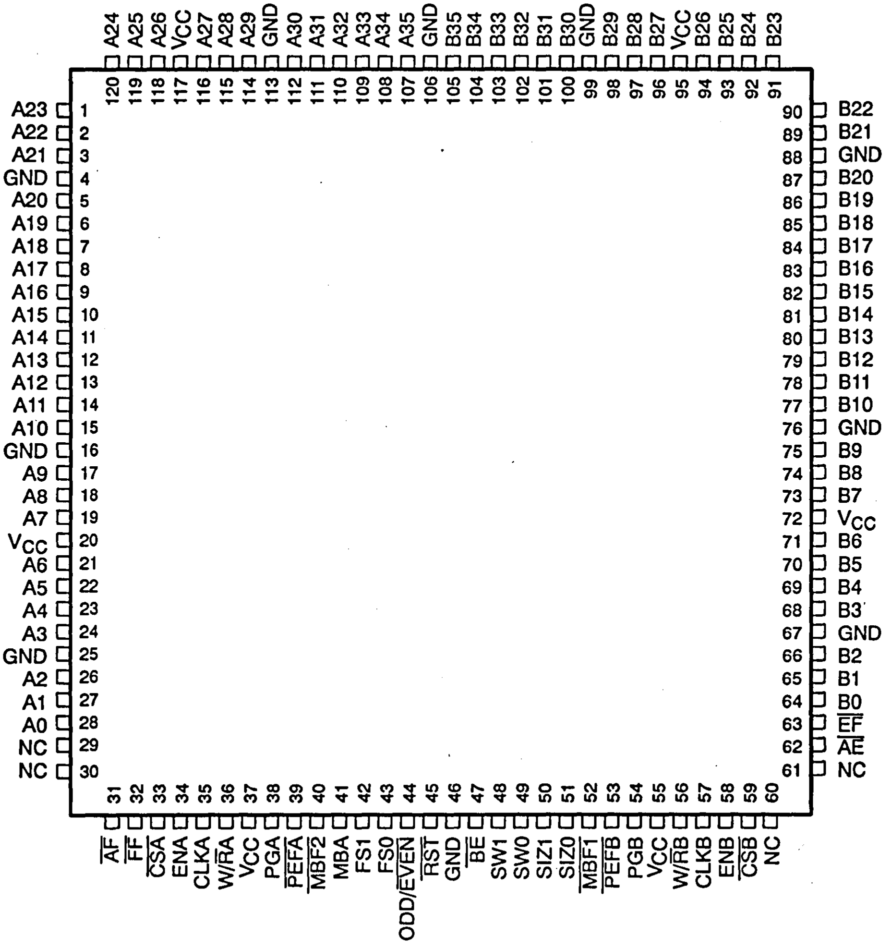
The SN74ABT3613 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses controlled by a synchronous interface.

The full flag and almost-full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost-empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

The SN74ABT3613 is characterized for operation from 0°C to 70°C.

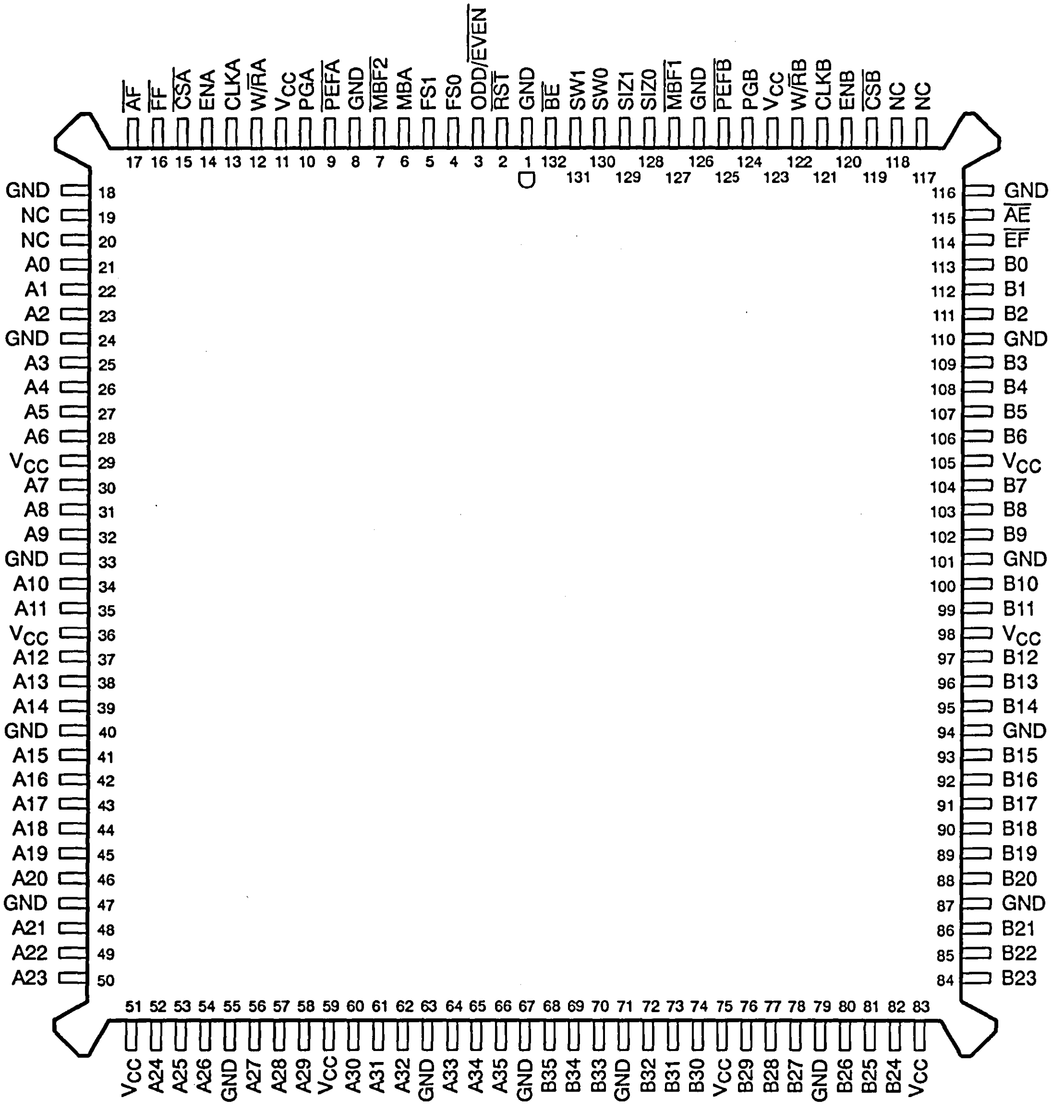
TEXAS INSTRUMENTS

PCB PACKAGE
(TOP VIEW)



NC – No internal connection

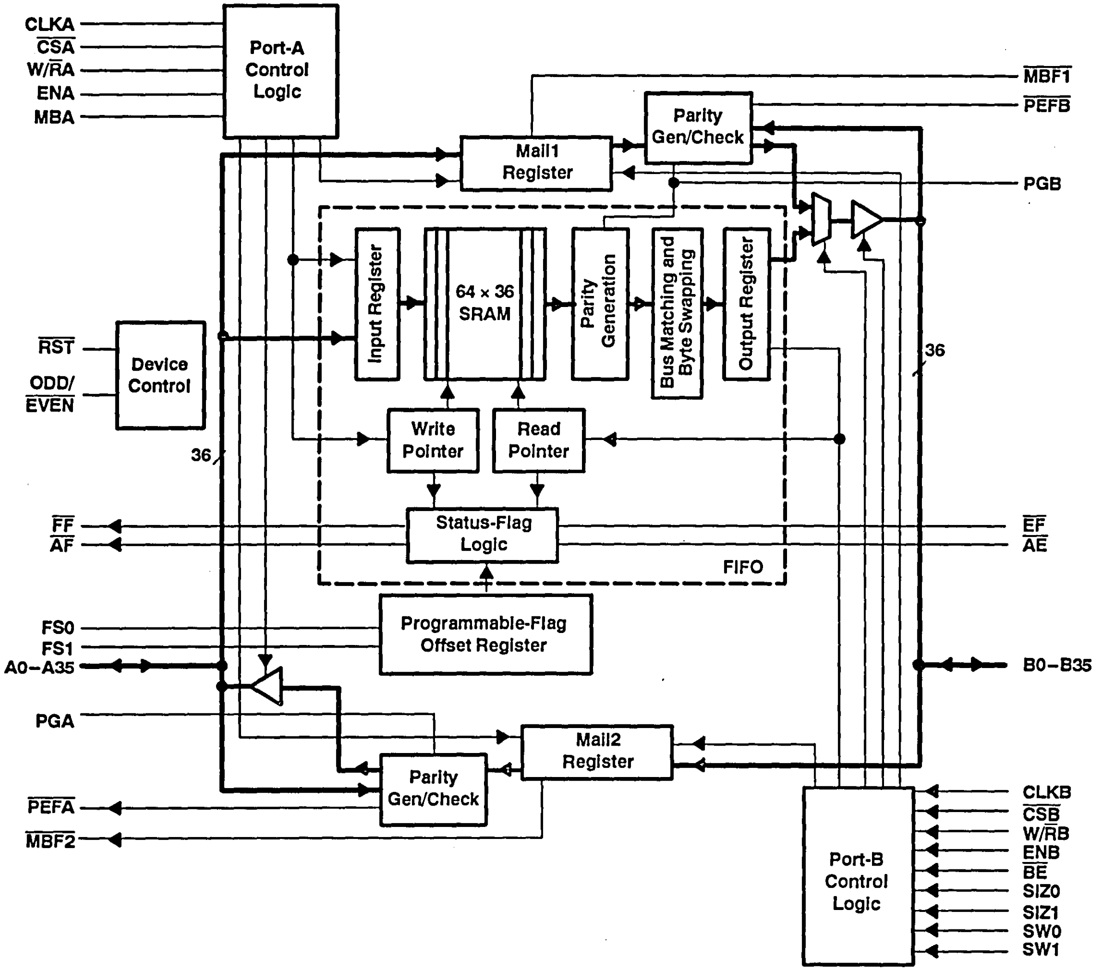
PQ PACKAGE†
(TOP VIEW)



NC – No internal connection

† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\mathrm{AE}}$	O (port B)	Almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\mathrm{AE}}$ is low when the number of 36-bit words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{\mathrm{AF}}$	O (port A)	Almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\mathrm{AF}}$ is low when the number of 36-bit empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
$\overline{\mathrm{BE}}$	I	Big-endian select. Selects the bytes on port B used during byte or word FIFO reads. A low on $\overline{\mathrm{BE}}$ selects the most significant bytes on B0–B35 for use, and a high selects the least significant bytes.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{\mathrm{FF}}$ and $\overline{\mathrm{AF}}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{\mathrm{EF}}$ and $\overline{\mathrm{AE}}$ are synchronized to the low-to-high transition of CLKB.
$\overline{\mathrm{CSA}}$	I	Port-A chip select. $\overline{\mathrm{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\mathrm{CSA}}$ is high.
$\overline{\mathrm{CSB}}$	I	Port-B chip select. $\overline{\mathrm{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\mathrm{CSB}}$ is high.
$\overline{\mathrm{EF}}$	O (port B)	Empty flag. $\overline{\mathrm{EF}}$ is synchronized to the low-to-high transition of CLKB. When $\overline{\mathrm{EF}}$ is low, the FIFO is empty and reads from its memory are disabled. Data can be read from the FIFO to the output register when $\overline{\mathrm{EF}}$ is high. $\overline{\mathrm{EF}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{\mathrm{FF}}$	O (port A)	Full flag. $\overline{\mathrm{FF}}$ is synchronized to the low-to-high transition of CLKA. When $\overline{\mathrm{FF}}$ is low, the FIFO is full and writes to its memory are disabled. $\overline{\mathrm{FF}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{\mathrm{RST}}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and almost-full flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, mail2 register data is output.
$\overline{\mathrm{MBF1}}$	O	Mail1 register flag. $\overline{\mathrm{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\mathrm{MBF1}}$ is low. $\overline{\mathrm{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and both SIZ1 and SIZ0 are high. $\overline{\mathrm{MBF1}}$ is set high when the device is reset.
$\overline{\mathrm{MBF2}}$	O	Mail2 register flag. $\overline{\mathrm{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\mathrm{MBF2}}$ is low. $\overline{\mathrm{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\mathrm{MBF2}}$ is set high when the device is reset.
ODD/ $\overline{\mathrm{EVEN}}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{\mathrm{EVEN}}$ is high, and even parity is checked when ODD/$\overline{\mathrm{EVEN}}$ is low. ODD/$\overline{\mathrm{EVEN}}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{\mathrm{PEFA}}$	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{\mathrm{PEFA}}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35 with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{\mathrm{EVEN}}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA; therefore, if a mail2 read with parity generation is set up by having $\overline{\mathrm{CSA}}$ low, ENA high, W/$\overline{\mathrm{RA}}$ low, MBA high, and PGA high, the $\overline{\mathrm{PEFA}}$ flag is forced high regardless of the state of the A0–A35 inputs.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
$\overline{\text{PEFB}}$	O (port B)	Port-B parity error flag. When any valid byte applied to terminals B0–B35 fails parity, $\overline{\text{PEFB}}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35 with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB; therefore, if a mail1 read with parity generation is set up by having $\overline{\text{CSB}}$ low, ENB high, W/$\overline{\text{RB}}$ low, SIZ1 and SIZ0 high, and PGB high, the $\overline{\text{PEFB}}$ flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from the mail2 register when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. This sets the $\overline{\text{AF}}$, $\overline{\text{MBF1}}$, and $\overline{\text{MBF2}}$ flags high and the $\overline{\text{EF}}$, $\overline{\text{AE}}$, and $\overline{\text{FF}}$ flags low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
SIZ0, SIZ1	I (port B)	Port-B bus size selects. The low-to-high transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{\text{BE}}$, and the following low-to-high transition of CLKB implements the latched states as a port-B bus size. Port-B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox registers for a port-B 36-bit write or read.
SW0, SW1	I (port B)	Port-B byte swap selects. At the beginning of each long word FIFO read, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{\text{RA}}$	I	Port-A write/read select. W/$\overline{\text{RA}}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
W/$\overline{\text{RB}}$	I	Port-B write/read select. W/$\overline{\text{RB}}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{\text{RB}}$ is high.

detailed description

reset

The SN74ABT3613 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flag ($\overline{\text{FF}}$) low, the empty flag ($\overline{\text{EF}}$) low, the almost-empty flag ($\overline{\text{AE}}$) low, and the almost-full flag ($\overline{\text{AF}}$) high. A reset also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a reset, $\overline{\text{FF}}$ is set high after two low-to-high transitions of CLKA. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the $\overline{\text{RST}}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{R}}$A). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{R}}$A is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{R}}$A are low. Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is high, ENA is high, MBA is low, and $\overline{\text{FFA}}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{R}}$A	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select (W/$\overline{\text{R}}$B). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ or W/$\overline{\text{R}}$B is high. The B0–B35 outputs are active when both $\overline{\text{CSB}}$ and W/$\overline{\text{R}}$B are low. Data is read from the FIFO to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is low, ENB is high, $\overline{\text{EFB}}$ is high, and either SIZ0 or SIZ1 is low (see Table 3).

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	W/$\overline{\text{R}}$B	ENB	SIZ1, SIZ0	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both low	↑	In high-impedance state	None
L	H	H	Both high	↑	In high-impedance state	Mail2 write
L	L	L	One, both low	X	Active, FIFO output register	None
L	L	H	One, both low	↑	Active, FIFO output register	FIFO read
L	L	L	Both high	X	Active, mail1 register	None
L	L	H	Both high	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) and write/read selects (W/$\overline{\text{R}}$A, W/$\overline{\text{R}}$B) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup and hold time window of the cycle.

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of each port flag to the level of FIFO fill.

Table 4. FIFO Flag Operation

NUMBER OF 36-BIT WORDS IN THE FIFO[†]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

[†] X is the value in the almost-empty flag and almost-full flag offset register.

empty flag ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored. When reading the FIFO with a byte or word size on port B, $\overline{EF}$ is set low when the fourth byte or second word of the last long word is read.

The FIFO read pointer is incremented each time a new word is clocked to the output register. The state machine that controls the empty flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles. An empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 9).

full flag ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from the FIFO, the previous memory location is ready to be written in a minimum of three CLKA cycles. A full flag is low if less than two CLKA cycles have elapsed since the next memory write location has been read. The second low-to-high transition on the full-flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 10).

almost-empty flag ($\overline{\text{AE}}$)

The FIFO almost-empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset). An almost-empty flag is low when the FIFO contains X or less long words in memory and is high when the FIFO contains (X + 1) or more long words.

Two low-to-high transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more long words remains low if two CLKB cycles have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) long words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 11).

almost-full flag ($\overline{\text{AF}}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). An almost-full flag is low when the FIFO contains (64 – X) or more long words in memory and is high when the FIFO contains [64 – (X + 1)] or less long words.

Two low-to-high transitions of CLKA are required after a FIFO read for the almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two CLKA cycles have not elapsed since the read that reduced the number of long words in memory to [64 – (X + 1)]. An almost-full flag is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of long words in memory to [64 – (X + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of long words in memory to [64 – (X + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 12).

mailbox registers

Two 36-bit bypass registers (mail1, mail2) are on board the SN74ABT3613 to pass command and control information between port A and port B without putting it in queue. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA, and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by ($\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, and ENB) and both SIZ0 and SIZ1 are high. Writing data to a mail register sets the corresponding flag ($\overline{\text{MBF1}}$ or $\overline{\text{MBF2}}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

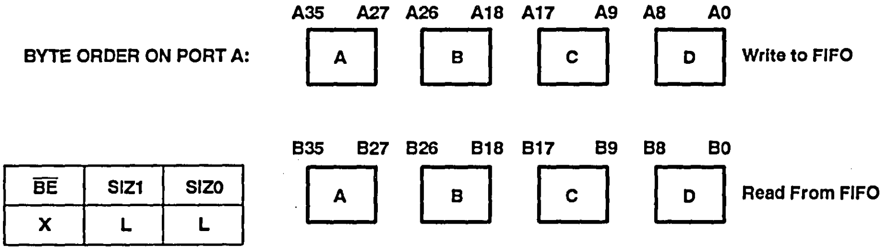
When the port-B data outputs (B0–B35) are active, the data on the bus comes from the FIFO output register when either one or both SIZ1 and SIZ0 are low and from the mail1 register when both SIZ1 and SIZ0 are high. The mail1 register flag ($\overline{\text{MBF1}}$) is set high by a rising CLKB edge when a port-B read is selected by $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, and ENB, and both SIZ1 and SIZ0 are high. The mail2 register flag ($\overline{\text{MBF2}}$) is set high by a rising CLKA edge when a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA and MBA is high. The data in the mail register remains intact after it is read and changes only when new data is written to the register.

dynamic bus sizing

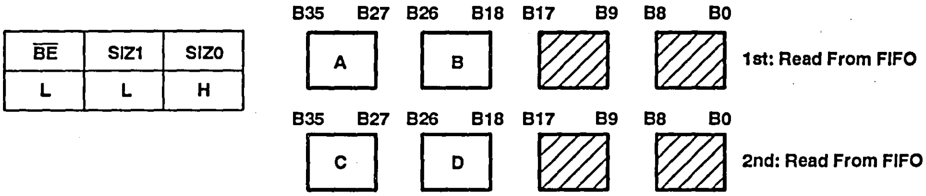
The port-B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from the FIFO. Word- and byte-size bus selections can utilize the most significant bytes of the bus (big endian) or least significant bytes of the bus (little endian). Port-B bus-size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port-B bus size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{\mathrm{BE}}$) input are stored on each CLKB low-to-high transition. The stored port-B bus-size selection is implemented by the next rising edge on CLKB according to Figure 1.

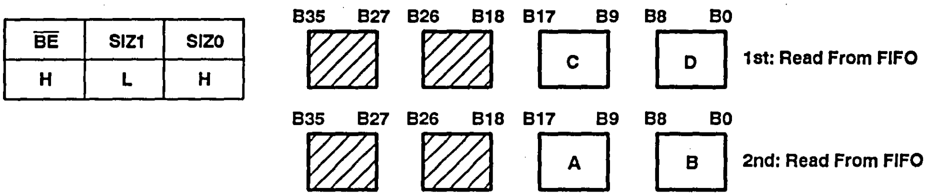
Only 36-bit long-word data is written to or read from the FIFO memory on the SN74ABT3613. Bus-matching operations are done after data is read from the FIFO RAM. Port-B bus sizing does not apply to mail register operations.



(a) LONG-WORD SIZE



(b) WORD SIZE – BIG ENDIAN

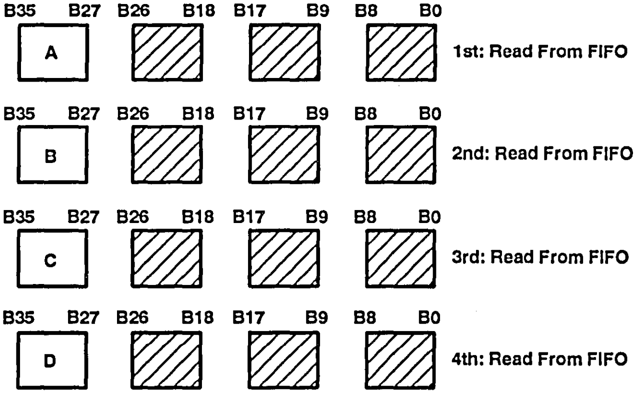


(c) WORD SIZE – LITTLE ENDIAN

Figure 1. Dynamic Bus Sizing

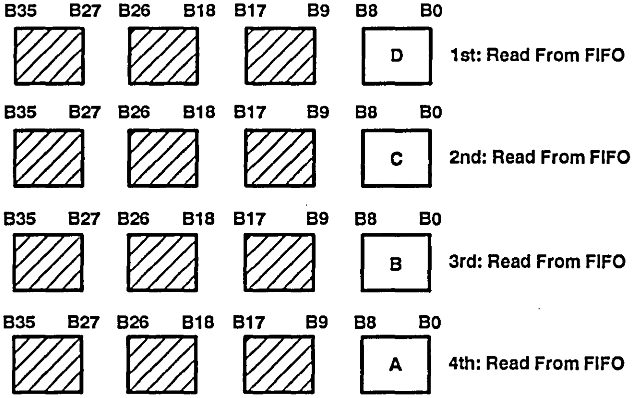
dynamic bus sizing (continued)

$\overline{BE}$	SIZ1	SIZ0
L	H	L



(d) BYTE SIZE – BIG ENDIAN

$\overline{BE}$	SIZ1	SIZ0
H	H	L



(e) BYTE SIZE – LITTLE ENDIAN

Figure 1. Dynamic Bus Sizing (continued)

bus-matching FIFO reads

Data is read from the FIFO RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long word immediately shifts to the FIFO output register upon a read. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO output register with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO reads with the same bus-size implementation output the rest of the long word to the FIFO output register in the order shown by Figure 1.

Each FIFO read with a new bus-size implementation automatically unloads data from the FIFO RAM to its output register and auxiliary registers. Implementing a new port-B bus size and performing a FIFO read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread data in these registers.

When reading data from FIFO in byte or word format, the unused B0–B35 outputs remain inactive but static, with the unused FIFO output register bits holding the last data value to decrease power consumption.

port-B mail register access

In addition to selecting port-B bus sizes for FIFO reads, the port-B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are high, the mail1 register is accessed for a port-B long-word read and the mail2 register is accessed for a port-B long-word write. The mail register is accessed immediately and any bus-sizing operation that can be underway is unaffected by the the mail-register access. After the mail-register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 2 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port-B bus size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{\text{BE}}$_Q.

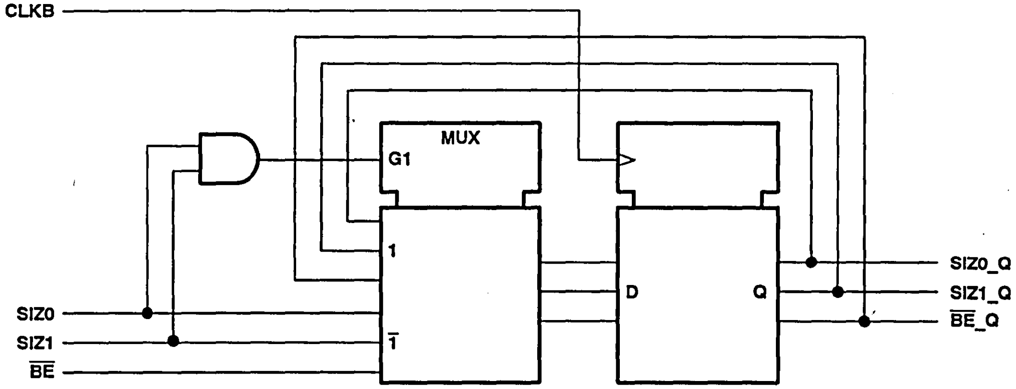


Figure 2. Logic Diagram for SIZ0, SIZ1, and $\overline{\text{BE}}$ Register

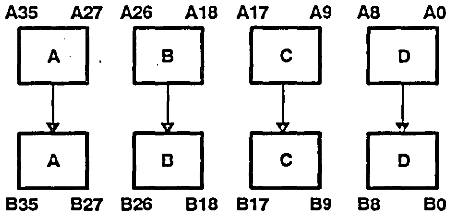
byte swapping

The byte-order arrangement of data read from the FIFO can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail-register data. Four modes of byte-order swapping (including no swap) can be done with any data port-size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port-B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from the FIFO. The byte order chosen on the first byte or first word of a new long word read from the FIFO is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent reads. Figure 3 is an example of the byte-order swapping available for long word reads. Performing a byte swap and bus size simultaneously for a FIFO read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1.

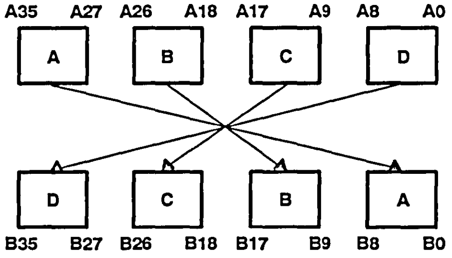
byte swapping (continued)

SW1	SW0
L	L



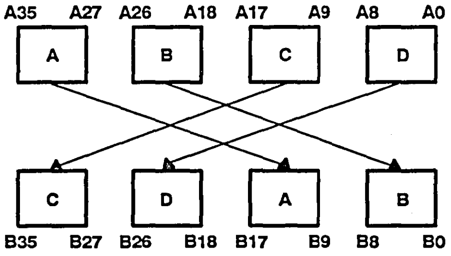
(a) NO SWAP

SW1	SW0
L	H



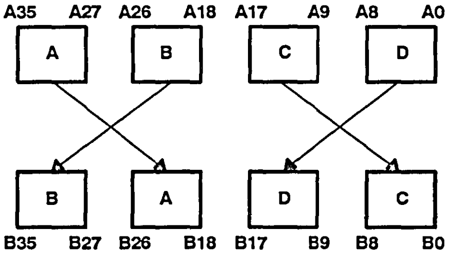
(b) BYTE SWAP

SW1	SW0
H	L



(c) WORD SWAP

SW1	SW0
H	H



(d) BYTE-WORD SWAP

Figure 3. Byte Swapping for FIFO Reads (Long-Word Size Example)

parity checking

The port-A data inputs (A0–A35) and port-B data inputs (B0–B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port-A data bus is reported by a low level on the port-A parity error flag ($\overline{\mathrm{PEFA}}$). A parity failure on one or more bytes of the port-B data inputs that are valid for the bus-size implementation is reported by a low level on the port-B parity error flag ($\overline{\mathrm{PEFB}}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\mathrm{EVEN}}$) select input. A parity error on one or more valid bytes of a port is reported by a low level on the corresponding port-parity-error flag ($\overline{\mathrm{PEFA}}$, $\overline{\mathrm{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, and its valid bytes are those used in a port-B bus-size implementation. When odd/even parity is selected, a port-parity-error flag ($\overline{\mathrm{PEFA}}$, $\overline{\mathrm{PEFB}}$) is low if any valid byte on the port has an odd/even number of low levels applied to the bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\mathrm{CSA}}$ low, ENA high, W/$\overline{\mathrm{RA}}$ low, MBA high, and PGA high, the port-A parity error flag ($\overline{\mathrm{PEFA}}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\mathrm{CSB}}$ low, ENB high, W/$\overline{\mathrm{RB}}$ low, both SIZ0 and SIZ1 high, and PGB high, the port-B parity error flag ($\overline{\mathrm{PEFB}}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3613 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35 with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\mathrm{EVEN}}$ select. The generated parity bits are substituted for the levels origninally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. The port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{\mathrm{EVEN}}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{\mathrm{EVEN}}$ select have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{\mathrm{CSA}}$, $\overline{\mathrm{CSB}}$) is low, enable (ENA, ENB) is high, and write/read select (W/$\overline{\mathrm{RA}}$, W/$\overline{\mathrm{RB}}$) input is low, the mail register is selected (MBA is high for port A; both SIZ0 and SIZ1 are high for port B), and port parity generate select (PGA, PGB) is high. Generating parity for mail-register data does not change the contents of the register.

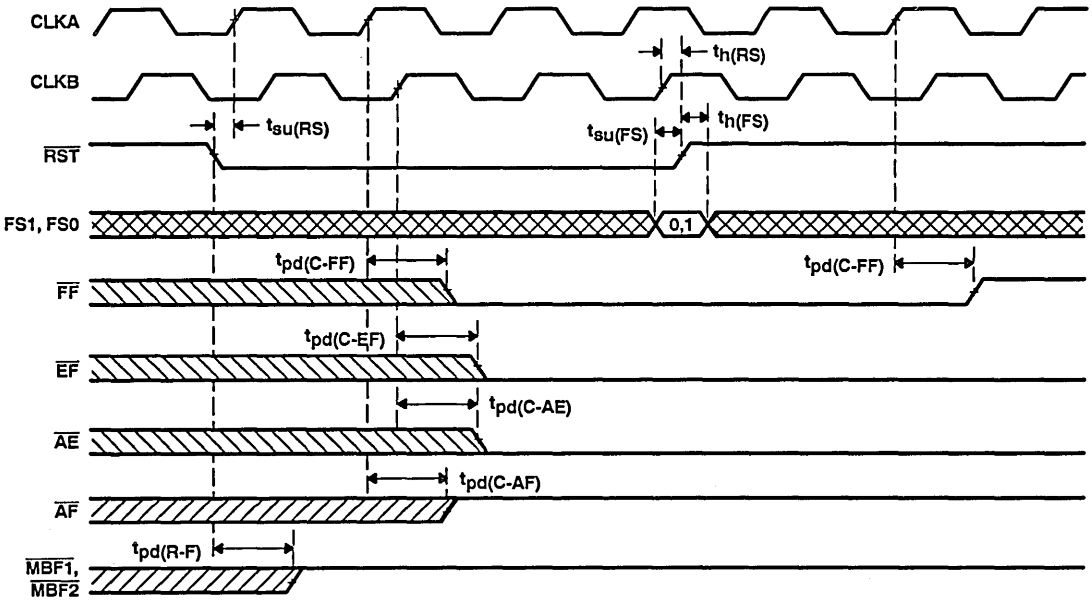
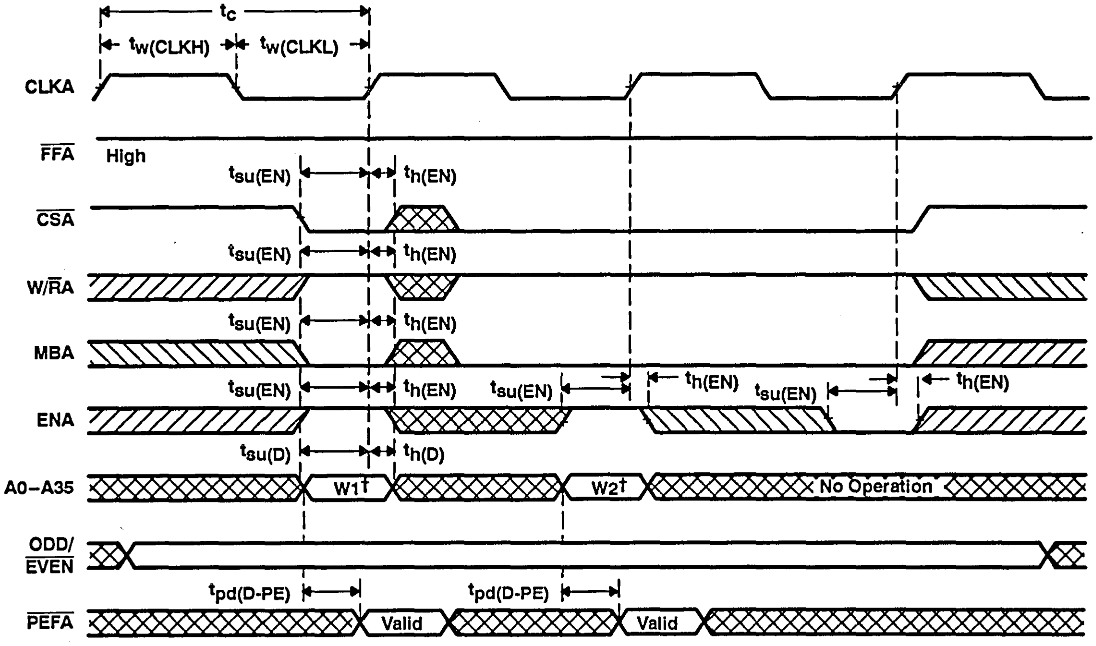
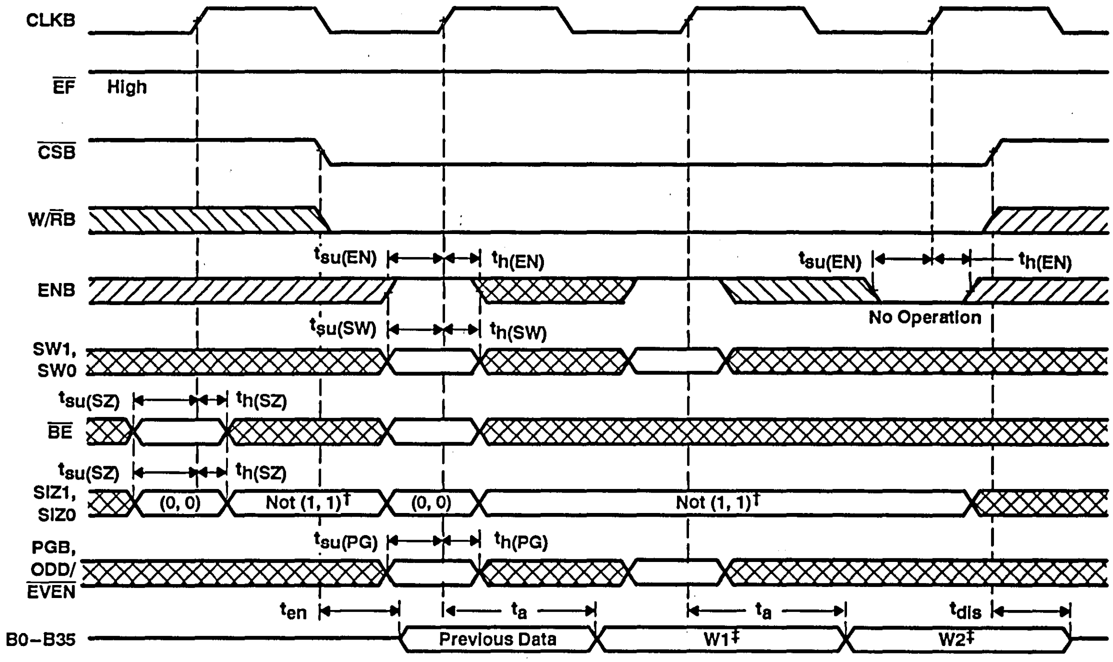


Figure 4. Device Reset Loading the X Register With the Value of Eight



† Written to the FIFO

Figure 5. FIFO-Write-Cycle Timing

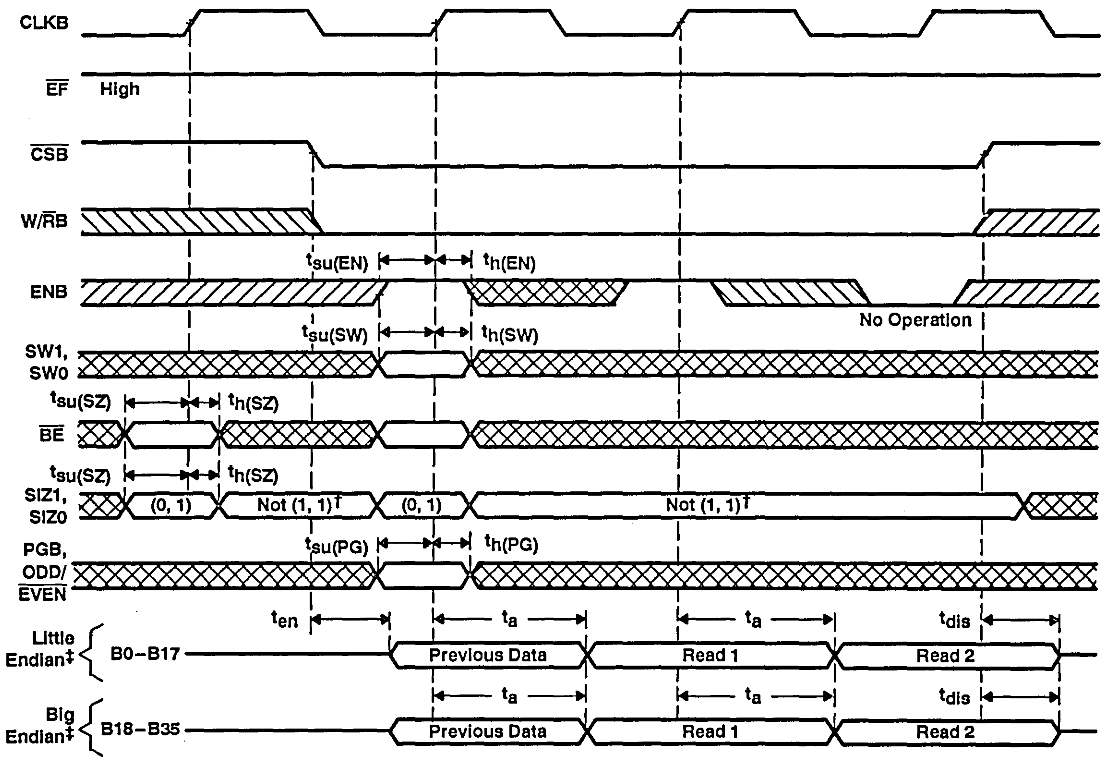


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Data read from the FIFO

DATA SWAP TABLE FOR FIFO LONG-WORD READS

FIFO DATA WRITE				SWAP MODE		FIFO DATA READ			
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 6. FIFO Long-Word Read-Cycle Timing

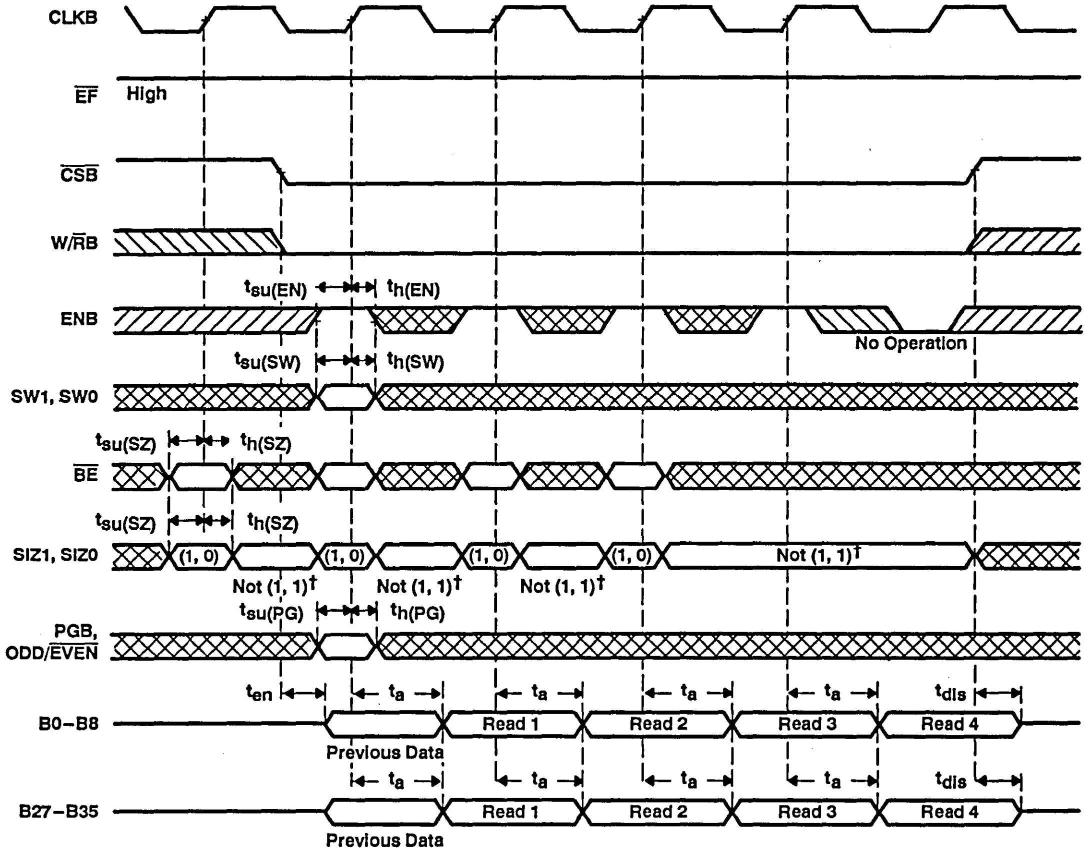


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Unused word B0–B17 or B18–B35 holds last FIFO output register data for word-size reads.

DATA SWAP TABLE FOR FIFO-WORD READS

FIFO-DATA WRITE				SWAP MODE		READ NO.	FIFO-DATA READ			
							BIG ENDIAN		LITTLE ENDIAN	
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	1	A	B	C	D
						2	C	D	A	B
A	B	C	D	L	H	1	D	C	B	A
						2	B	A	D	C
A	B	C	D	H	L	1	C	D	A	B
						2	A	B	C	D
A	B	C	D	H	H	1	B	A	D	C
						2	D	C	B	A

Figure 7. FIFO-Word Read-Cycle Timing



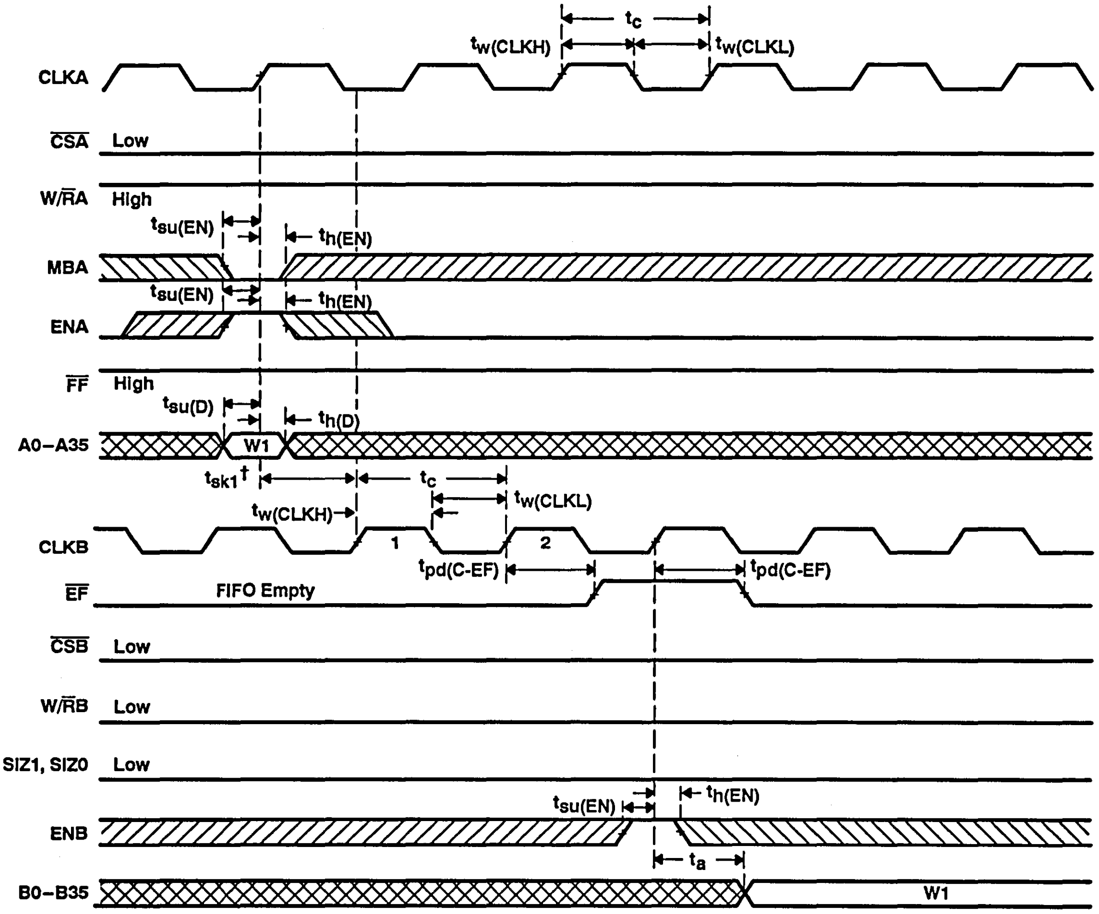
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
NOTE: Unused bytes hold last FIFO output register data for byte-size reads.

Figure 8. FIFO-Byte Read-Cycle Timing

DATA SWAP TABLE FOR FIFO-BYTE READS

FIFO-DATA WRITE				SWAP MODE		READ NO.	FIFO-DATA READ	
							BIG ENDIAN	LITTLE ENDIAN
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B8–B0
A	B	C	D	L	L	1	A	D
						2	B	C
						3	C	B
						4	D	A
A	B	C	D	L	H	1	D	A
						2	C	B
						3	B	C
						4	A	D
A	B	C	D	H	L	1	C	B
						2	D	A
						3	A	D
						4	B	C
A	B	C	D	H	H	1	B	C
						2	A	D
						3	D	A
						4	C	B

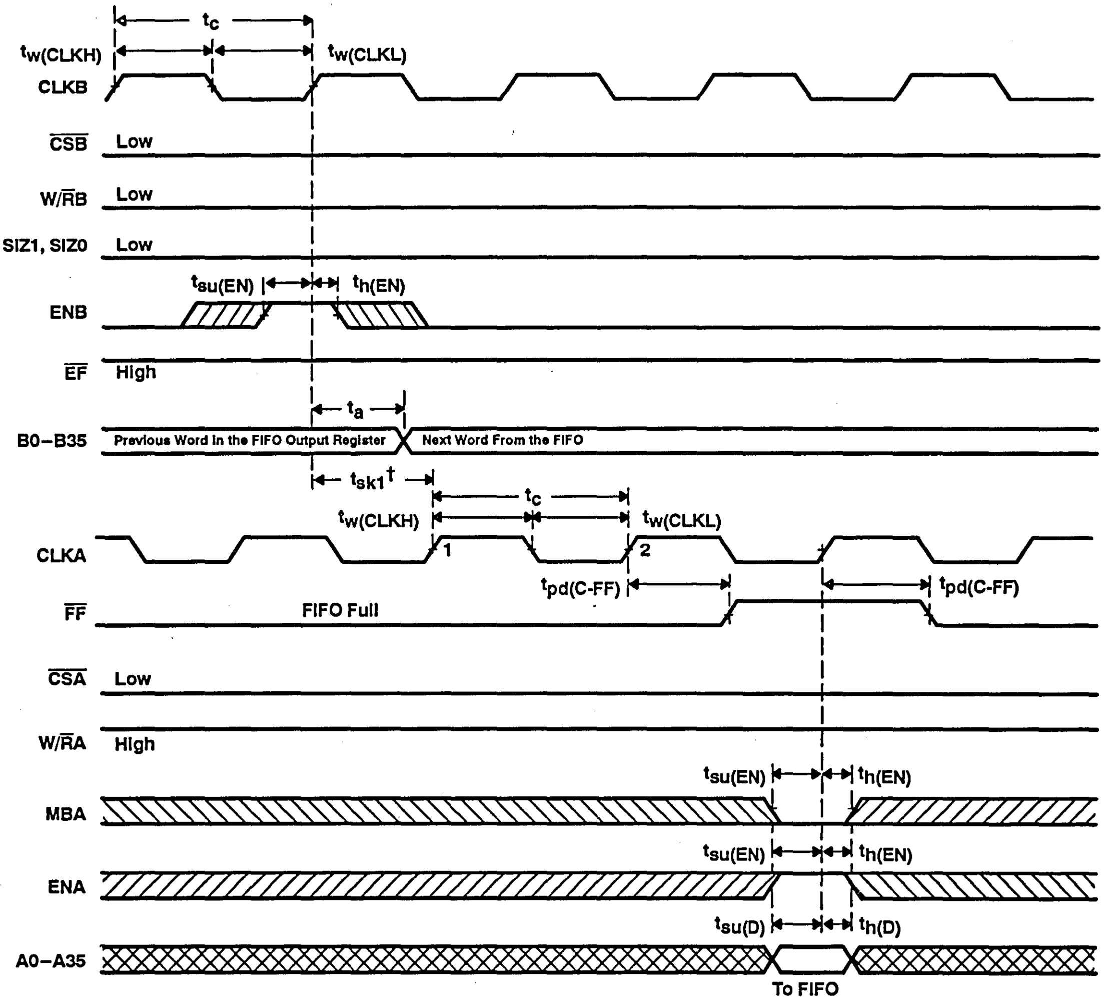
Figure 8. FIFO-Byte Read-Cycle Timing (continued)



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of $\overline{EF}$ high may occur one CLKB cycle later than shown.

NOTE A: Port-B size of long word is selected for the FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{EF}$ is set low by the last word or byte read from the FIFO, respectively.

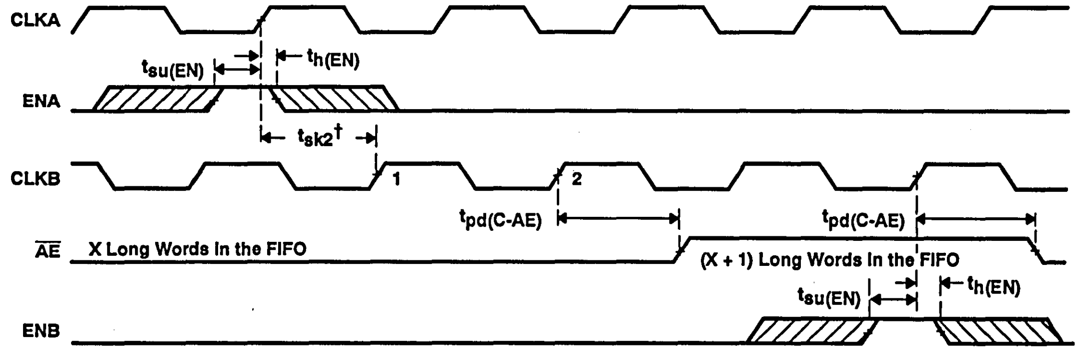
Figure 9. $\overline{EF}$-Flag Timing and First Data Read When the FIFO Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then $\overline{FF}$ may transition high one CLKA cycle later than shown.

NOTE A: Port-B size of long word is selected for the FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced from the rising CLKB edge that reads the first word or byte of the long word, respectively.

Figure 10. $\overline{FF}$-Flag Timing and First Available Write When the FIFO Is Full

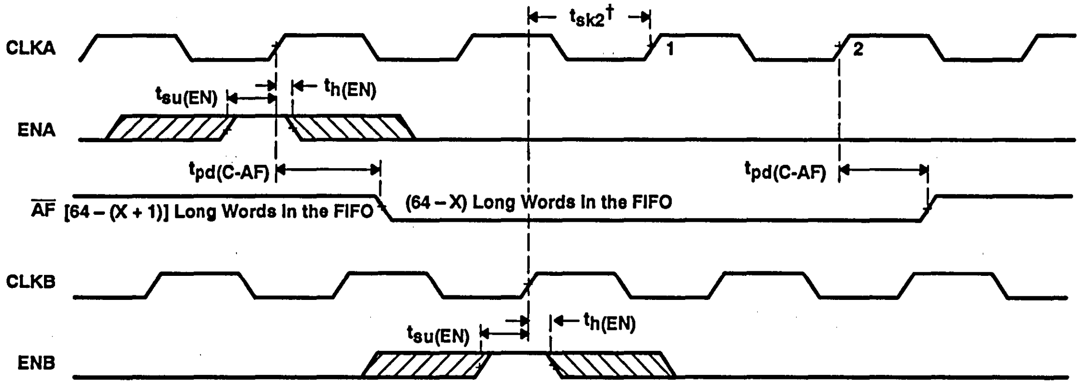


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AE}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L)

B. Port-B size of long word is selected for FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced to the first word or byte read of the long word, respectively.

Figure 11. Timing for $\overline{AE}$ When the FIFO Is Almost Empty

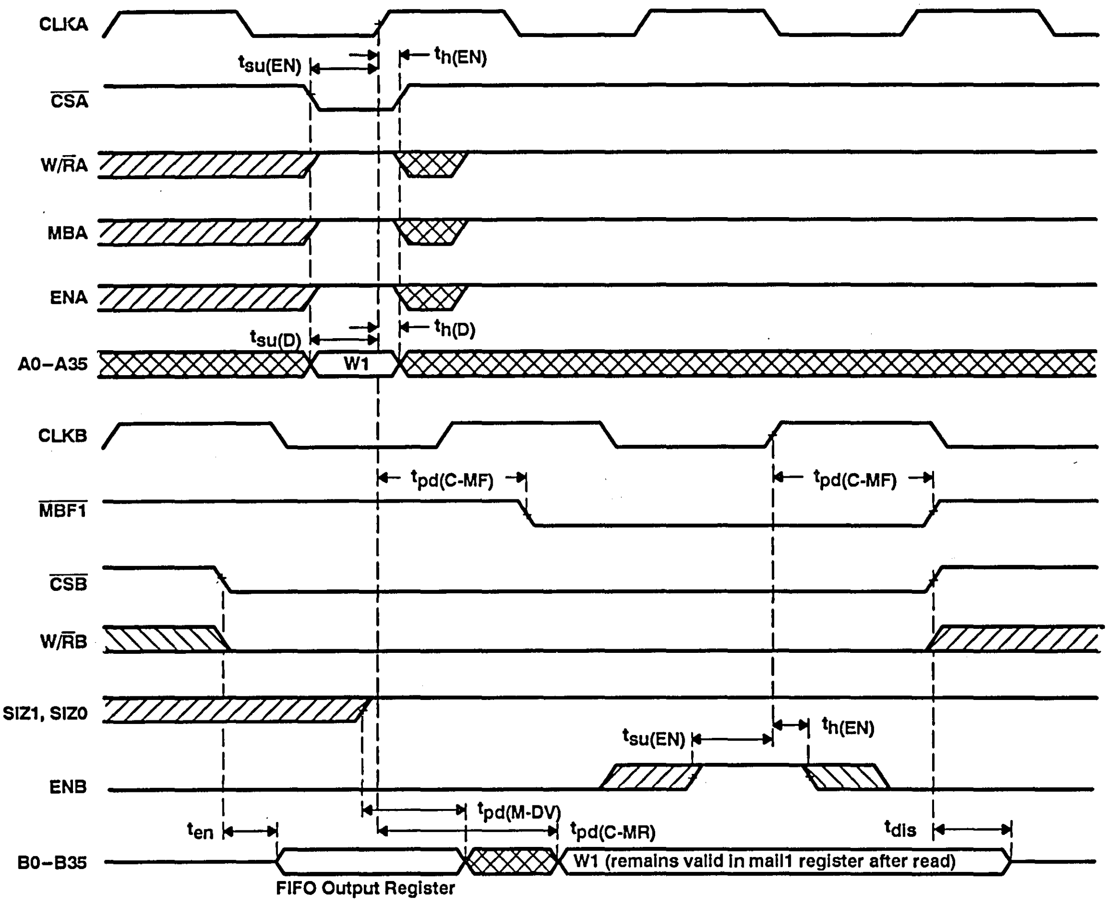


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AF}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L)

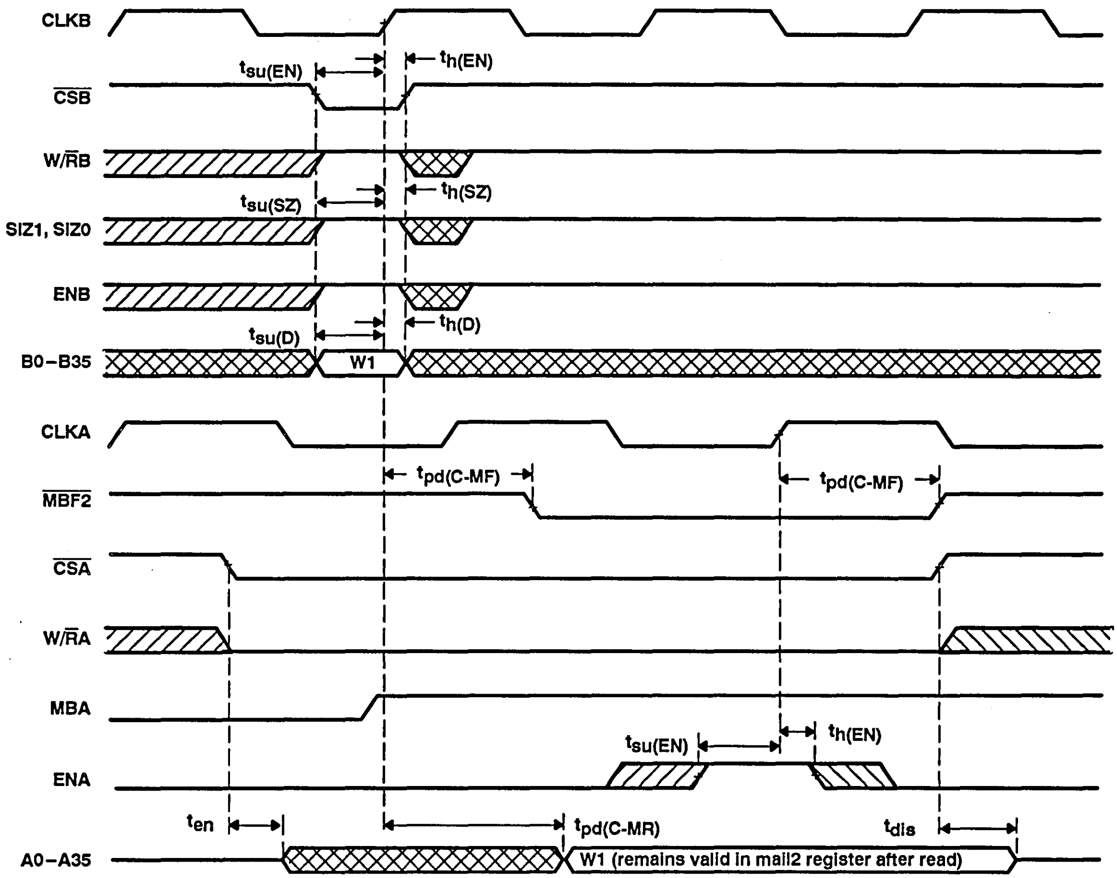
B. Port-B size of long word is selected for FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the first word or byte read of the long word, respectively.

Figure 12. Timing for $\overline{AF}$ When the FIFO Is Almost Full



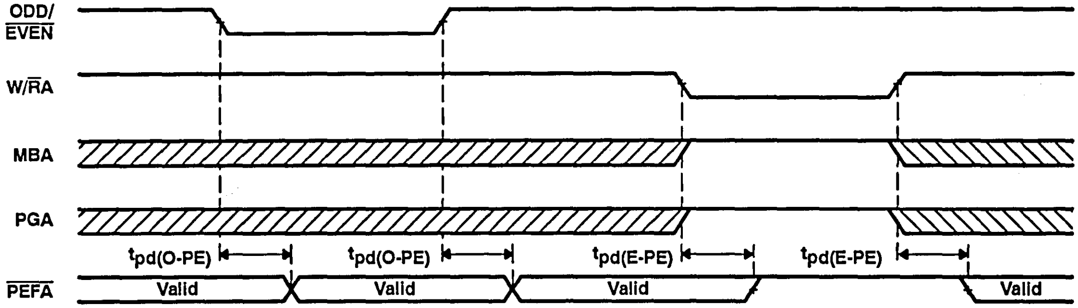
NOTE A: Port-B parity generation off (PGB = L)

Figure 13. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



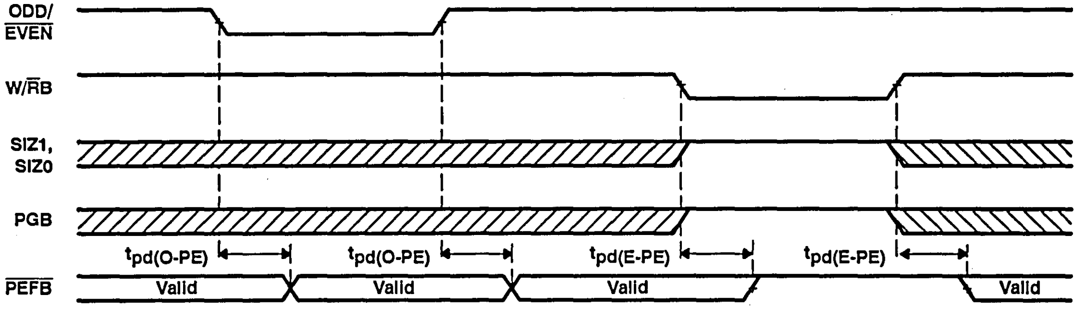
NOTE A: Port-A parity generation off (PGA = L)

Figure 14. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag



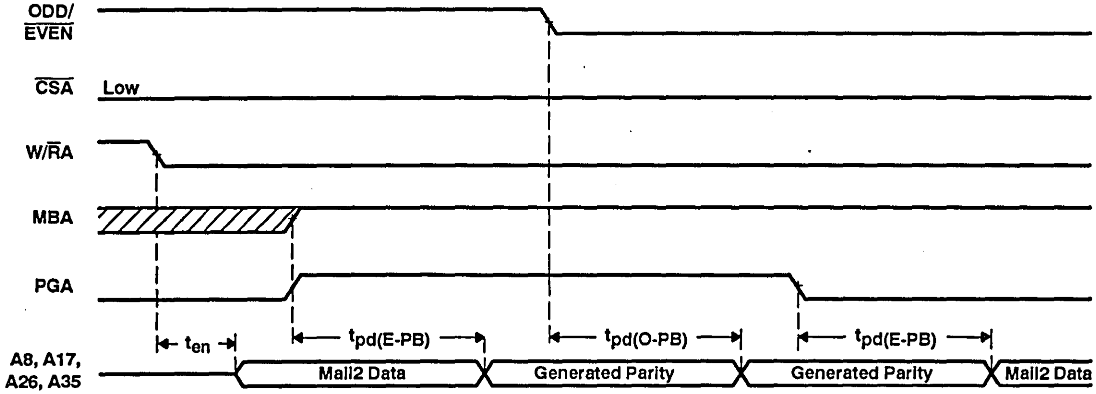
NOTE A: $\overline{CSA}$ = L and ENA = H

Figure 15. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



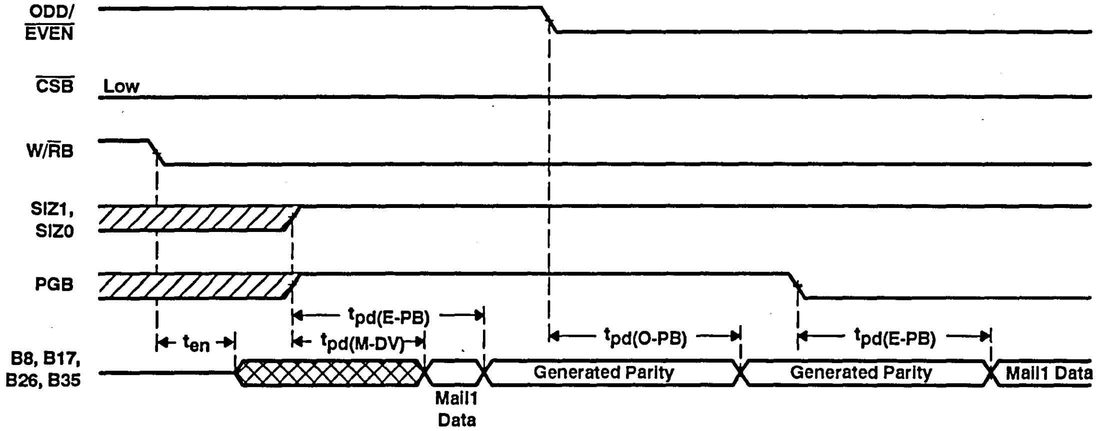
NOTE A: $\overline{CSB}$ = L and ENB = H

Figure 16. ODD/$\overline{EVEN}$, W/$\overline{RB}$, SIZ1, SIZ0, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA = H

Figure 17. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB = H

Figure 18. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±500 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -4$ mA		2.4			V
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 8$ mA				0.5	V
I_I	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or 0				±50	µA
I_{OZ}	$V_{CC} = 5.5$ V, $V_O = V_{CC}$ or 0				±50	µA
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$ mA, $V_I = V_{CC}$ or GND	Outputs high			60	mA
		Outputs low			130	
		Outputs disabled			60	
C_i	$V_I = 0$, f = 1 MHz			4		pF
C_o	$V_O = 0$, f = 1 MHz			8		pF

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 4 through 18)

		'ABT3613-15		'ABT3613-20		'ABT3613-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{\mathrm{CSA}}$, W/$\overline{\mathrm{RA}}$, ENA, and MBA before CLKA↑; $\overline{\mathrm{CSB}}$, W/$\overline{\mathrm{RB}}$, and ENB before CLKB↑	5		5		6		ns
$t_{su(SZ)}$	Setup time, SIZ0, SIZ1, and $\overline{\mathrm{BE}}$ before CLKB↑	4		5		6		ns
$t_{su(SW)}$	Setup time, SW0 and SW1 before CLKB↑	5		7		8		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{\mathrm{EVEN}}$ and PGB before CLKB↑[†]	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{\mathrm{RST}}$ low before CLKA↑ or CLKB↑[‡]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{\mathrm{RST}}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{\mathrm{CSA}}$, W/$\overline{\mathrm{RA}}$, ENA, and MBA after CLKA↑; $\overline{\mathrm{CSB}}$, W/$\overline{\mathrm{RB}}$, and ENB after CLKB↑	1		1		1		ns
$t_{h(SZ)}$	Hold time, SIZ0, SIZ1, and $\overline{\mathrm{BE}}$ after CLKB↑	2		2		2		ns
$t_{h(SW)}$	Hold time, SW0 and SW1 after CLKB↑	0		0		0		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{\mathrm{EVEN}}$ and PGB after CLKB↑[†]	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{\mathrm{RST}}$ low after CLKA↑ or CLKB↑[‡]	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{\mathrm{RST}}$ high	4		4		4		ns
t_{sk1}[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{\mathrm{EF}}$ and $\overline{\mathrm{FF}}$	8		8		10		ns
t_{sk2}[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{\mathrm{AE}}$ and $\overline{\mathrm{AF}}$	9		16		20		ns

[†] Only applies for a clock edge that does a FIFO read

[‡] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[§] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 4 through 18)

PARAMETER		'ABT3613-15		'ABT3613-20		'ABT3613-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C\text{-}FF)}$	Propagation delay time, CLKA↑ to $\overline{\text{FF}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}EF)}$	Propagation delay time, CLKB↑ to $\overline{\text{EF}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKB↑ to $\overline{\text{AE}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\text{AF}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\text{MBF1}}$ low or $\overline{\text{MBF2}}$ high and CLKB↑ to $\overline{\text{MBF2}}$ low or $\overline{\text{MBF1}}$ high	1	9	1	12	1	15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35[†] and CLKB↑ to A0–A35[‡]	3	11	3	12	3	15	ns
$t_{pd(C\text{-}PE)}$[§]	Propagation delay time, CLKB↑ to $\overline{\text{PEFB}}$	2	11	2	12	2	13	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, SIZ1, SIZ0 to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D\text{-}PE)}$	Propagation delay time, A0-A35 valid to $\overline{\text{PEFA}}$ valid; B0–B35 valid to $\overline{\text{PEFB}}$ valid	3	10	3	11	3	13	ns
$t_{pd(O\text{-}PE)}$	Propagation delay time, ODD/$\overline{\text{EVEN}}$ to $\overline{\text{PEFA}}$ and $\overline{\text{PEFB}}$	3	11	3	12	3	14	ns
$t_{pd(O\text{-}PB)}$[¶]	Propagation delay time, ODD/$\overline{\text{EVEN}}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
$t_{pd(E\text{-}PE)}$	Propagation delay time $\overline{\text{CSA}}$, ENA, W/$\overline{\text{RA}}$, MBA, or PGA to $\overline{\text{PEFA}}$; $\overline{\text{CSB}}$, ENB, W/$\overline{\text{RB}}$, SIZ1, SIZ0, or PGB to $\overline{\text{PEFB}}$	1	11	1	12	1	14	ns
$t_{pd(E\text{-}PB)}$[¶]	Propagation delay time, $\overline{\text{CSA}}$, ENA, W/$\overline{\text{RA}}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{\text{CSB}}$, ENB, W/$\overline{\text{RB}}$, SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\text{RST}}$ to $\overline{\text{AE}}$, $\overline{\text{EF}}$ low and $\overline{\text{AF}}$, $\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$ high.	1	15	1	20	1	25	ns
t_{en}	Enable time, $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ low to A0–A35 active and $\overline{\text{CSB}}$ low and W/$\overline{\text{RB}}$ high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ high to A0–A35 at high impedance and $\overline{\text{CSB}}$ high or W/$\overline{\text{RB}}$ low to B0–B35 at high impedance	1	8	1	9	1	11	ns

[†] Writing data to the mail1 register when the B0–B35 outputs are active and SIZ1 and SIZ0 are high.
[‡] Writing data to the mail2 register when the A0–A35 outputs are active.
[§] Only applies when a new port-B bus size is implemented by the rising CLKB edge.
[¶] Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

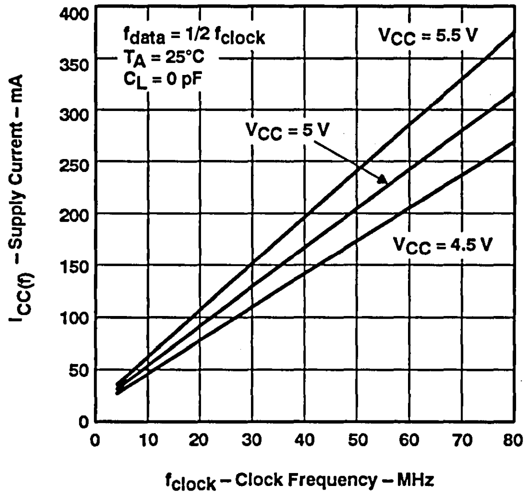


Figure 19

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 19 was taken while simultaneously reading and writing the FIFO on the SN74ACT3613 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 19, the maximum power dissipation (P_T) of the SN74ABT3613 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma[C_L \times (V_{OH} - V_{OL})^2 \times f_o]$$

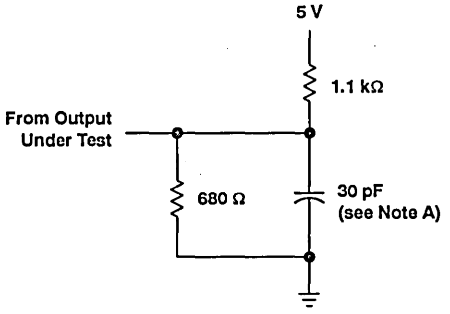
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = output high-level voltage
V_{OL} = output low-level voltage

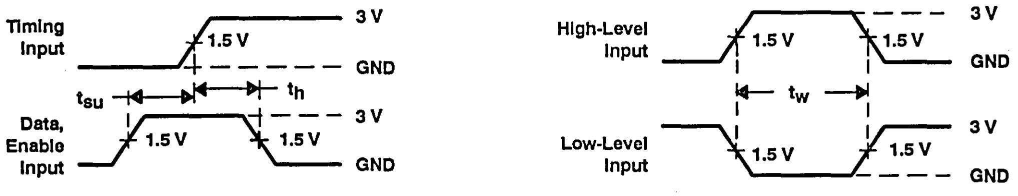
When no reads or writes are occurring on the SN74ABT3613, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

PARAMETER MEASUREMENT INFORMATION

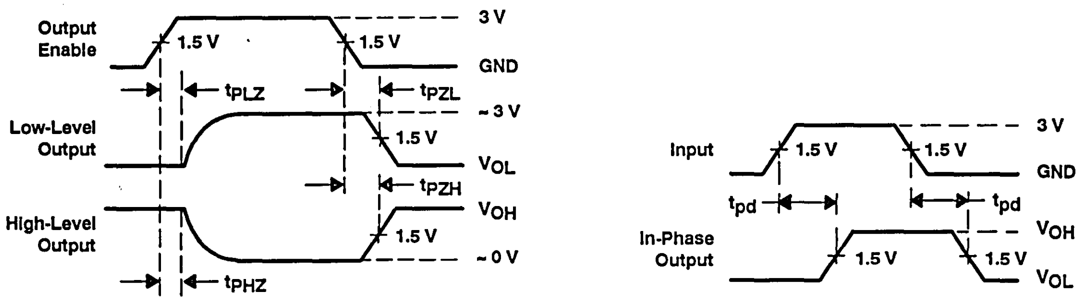


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 20. Load Circuit and Voltage Waveforms

SN74ABT3614
64 × 36 × 2 CLOCKED FIRST-IN, FIRST-OUT MEMORY WITH BUS MATCHING AND BYTE SWAPPING

SCBS126C – JUNE 1992 – REVISED JANUARY 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Dynamic Port-B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte-Order Swapping on Port B**
- **Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Quad Flat Package (PQ)**

description

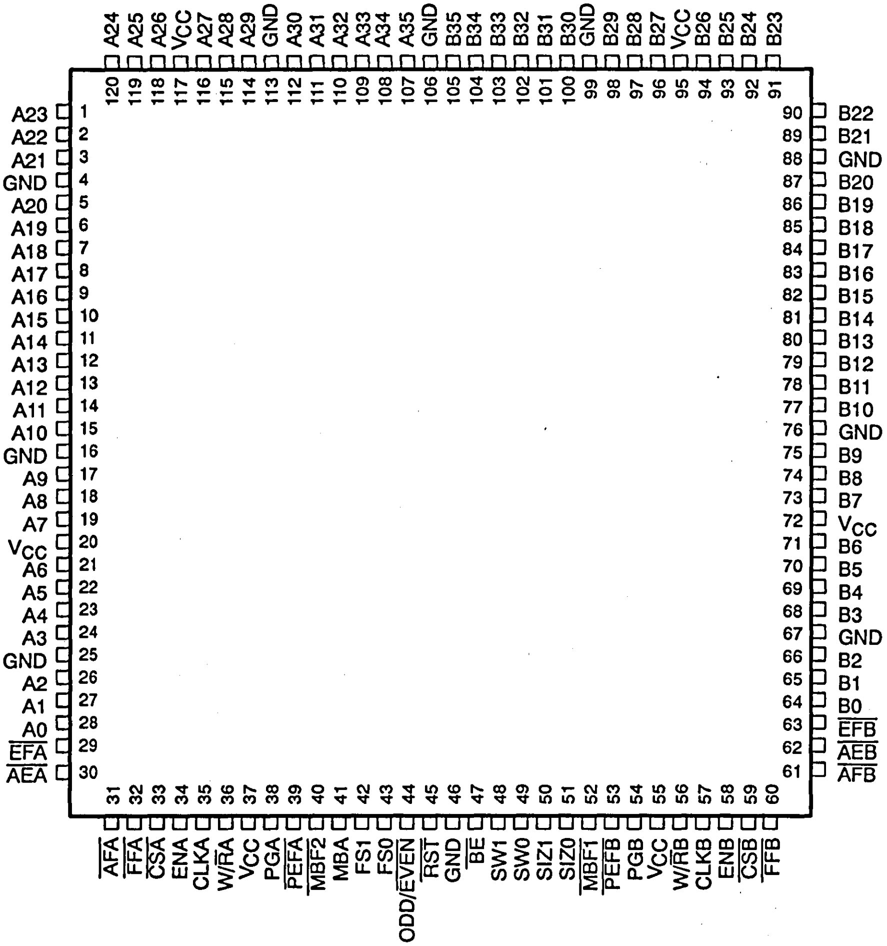
The SN74ABT3614 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. Two independent 64 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B can be input and output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus size selection. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port.

The SN74ABT3614 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

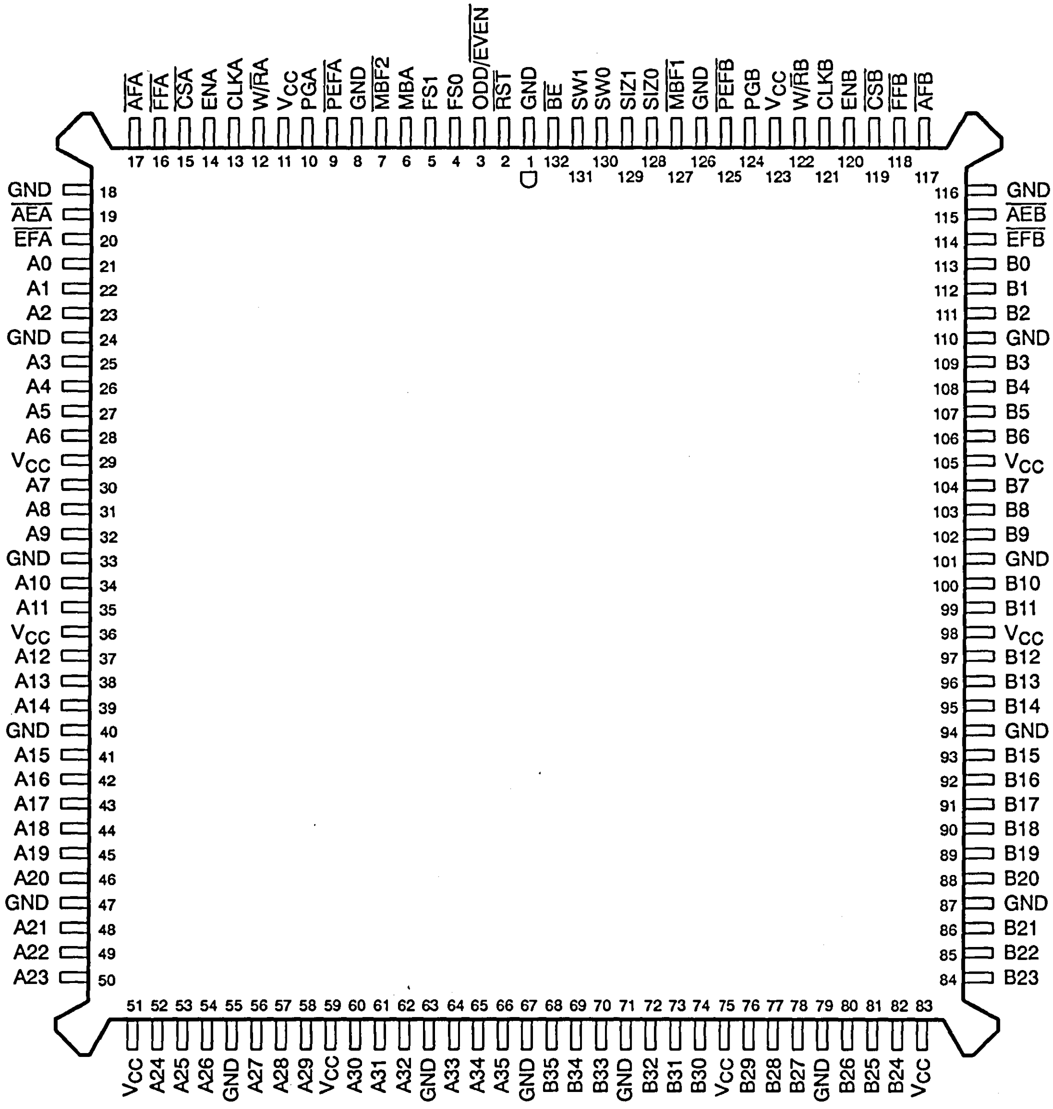
The full flag and almost-full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost-empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

The SN74ABT3614 is characterized for operation from 0°C to 70°C.

**PCB PACKAGE
(TOP VIEW)**

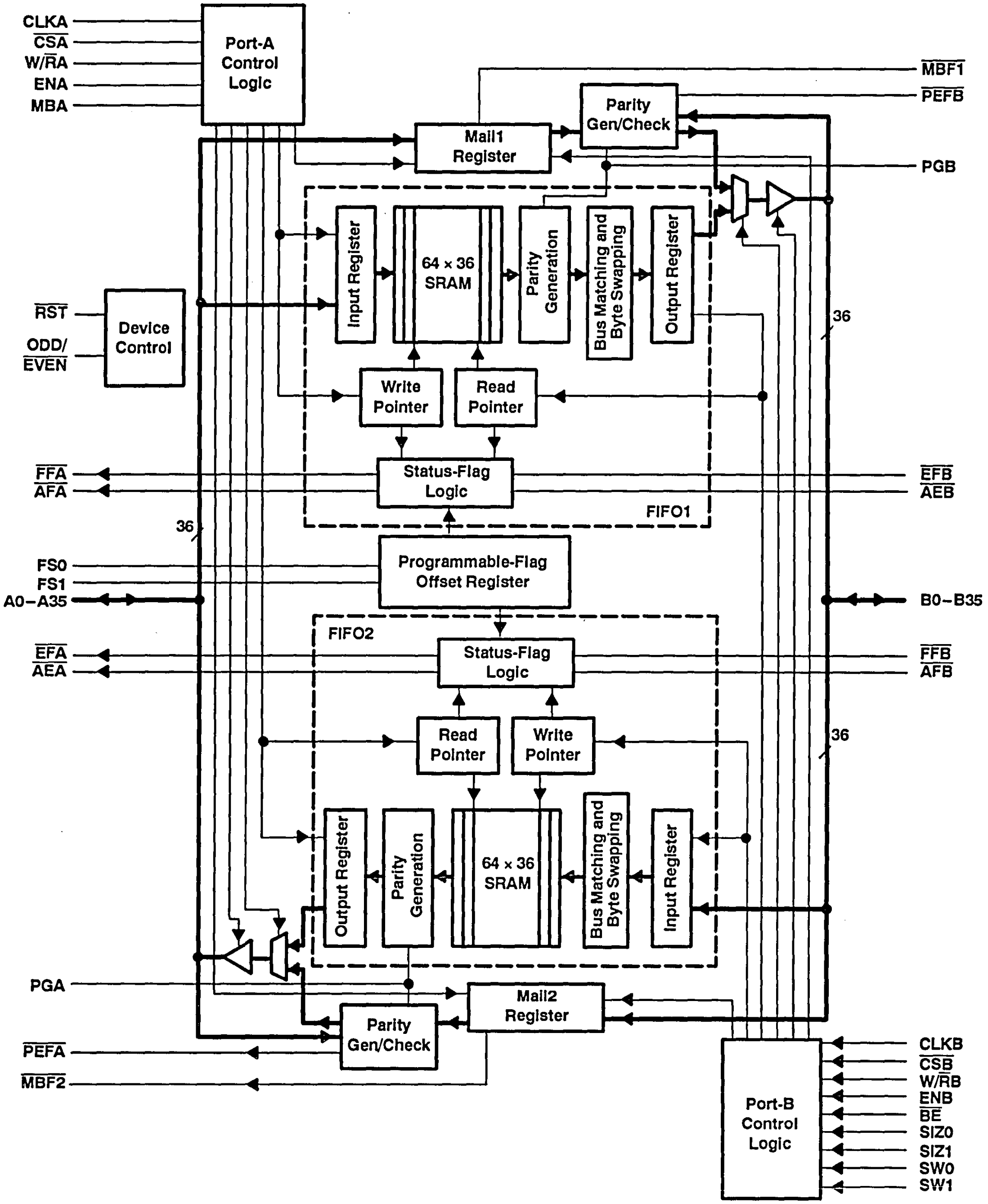


PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AEA}}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{\text{AEA}}$ is low when the number of 36-bit words in FIFO2 is less than or equal to the value in the offset register, X.
$\overline{\text{AEB}}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\text{AEB}}$ is low when the number of 36-bit words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{\text{AFA}}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\text{AFA}}$ is low when the number of 36-bit empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{\text{AFB}}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{\text{AFB}}$ is low when the number of 36-bit empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
$\overline{\text{BE}}$	I	Big-endian select. Selects the bytes on port B used during byte or word data transfer. A low on $\overline{\text{BE}}$ selects the most significant bytes on B0–B35 for use, and a high selects the least significant bytes.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AFA}}$, and $\overline{\text{AEA}}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AFB}}$, and $\overline{\text{AEB}}$ are synchronized to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
$\overline{\text{EFA}}$	O (port A)	Port-A empty flag. $\overline{\text{EFA}}$ is synchronized to the low-to-high transition of CLKA. When $\overline{\text{EFA}}$ is low, FIFO2 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{\text{EFA}}$ is high. $\overline{\text{EFA}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{\text{EFB}}$	O (port B)	Port-B empty flag. $\overline{\text{EFB}}$ is synchronized to the low-to-high transition of CLKB. When $\overline{\text{EFB}}$ is low, FIFO1 is empty and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{\text{EFB}}$ is high. $\overline{\text{EFB}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{\text{FFA}}$	O (port A)	Port-A full flag. $\overline{\text{FFA}}$ is synchronized to the low-to-high transition of CLKA. When $\overline{\text{FFA}}$ is low, FIFO1 is full and writes to its memory are disabled. $\overline{\text{FFA}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
$\overline{\text{FFB}}$	O (port B)	Port-B full flag. $\overline{\text{FFB}}$ is synchronized to the low-to-high transition of CLKB. When $\overline{\text{FFB}}$ is low, FIFO2 is full and writes to its memory are disabled. $\overline{\text{FFB}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{\text{RST}}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and almost-full flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output register data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\text{MBF1}}$ is low. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and both SIZ1 and SIZ0 are high. $\overline{\text{MBF1}}$ is set high when the device is reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\text{MBF2}}$ is low. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is set high when the device is reset.

Terminal Functions (continued)

PIN NAME	I/O	DESCRIPTION
ODD/EVEN	I	Odd/even parity select. Odd parity is checked on each port when ODD/EVEN is high, and even parity is checked when ODD/EVEN is low. ODD/EVEN also selects the type of parity generated for each port if parity generation is enabled for a read operation.
PEFA	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, PEFA is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/EVEN input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/RA low, MBA high, and PGA high, the PEFA flag is forced high regardless of the state of the A0–A35 inputs.
PEFB	O (port B)	Port-B parity error flag. When any valid byte applied to terminals B0–B35 fails parity, PEFB is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/EVEN input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/RB low, SIZ1 and SIZ0 high, and PGB high, the PEFB flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
RST	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while RST is low. This sets the AFA, AFB, MBF1, and MBF2 flags high and the EFA, EFB, AEA, AEB, FFA, and FFB flags low. The low-to-high transition of RST latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
SIZ0, SIZ1	I (port B)	Port-B bus size selects. The low-to-high transition of CLKB latches the states of SIZ0, SIZ1, and BE, and the following low-to-high transition of CLKB implements the latched states as a port-B bus size. Port-B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox registers for a port-B 36-bit write or read.
SW0, SW1	I (port B)	Port-B byte swap selects. At the beginning of each long word transfer, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/RA	I	Port-A write/read select. W/RA high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/RA is high.
W/RB	I	Port-B write/read select. W/RB high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/RB is high.

detailed description

reset

The SN74ABT3614 is reset by taking the reset (RST) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags (FFA, FFB) low, the empty flags (EFA, EFB) low, the almost-empty flags (AEA, AEB) low, and the almost-full flags (AFA, AFB) high. A reset also forces the mailbox flags (MBF1, MBF2) high. After a reset, FFA is set high after two low-to-high transitions of CLKA and FFB is set high after two low-to-high transitions of CLKB. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the RST input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

reset (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{RA}}$). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are low. Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is high, ENA is high, MBA is low, and $\overline{\text{FFA}}$ is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is low, ENA is high, MBA is low, and $\overline{\text{EFA}}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{RA}}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select (W/$\overline{\text{RB}}$). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ or W/$\overline{\text{RB}}$ is high. The B0–B35 outputs are active when both $\overline{\text{CSB}}$ and W/$\overline{\text{RB}}$ are low. Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{RB}}$ is high, ENB is high, $\overline{\text{FFB}}$ is high, and either SIZ0 or SIZ1 is low. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{RB}}$ is low, ENB is high, $\overline{\text{EFB}}$ is high, and either SIZ0 or SIZ1 is low (see Table 3).

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) and write/read selects (W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup and hold time window of the cycle.

FIFO writer/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{\mathrm{CSB}}$	W/$\overline{\mathrm{RB}}$	ENB	SIZ1, SIZ0	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both low	↑	In high-impedance state	FIFO2 write
L	H	H	Both high	↑	In high-impedance state	Mail2 write
L	L	L	One, both low	X	Active, FIFO1 output register	None
L	L	H	One, both low	↑	Active, FIFO1 output register	FIFO1 read
L	L	L	Both high	X	Active, mail1 register	None
L	L	H	Both high	↑	Active, mail1 register	Mail1 read (set $\overline{\mathrm{MBF1}}$ high)

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{\mathrm{EFA}}$, $\overline{\mathrm{AEA}}$, $\overline{\mathrm{FFA}}$, and $\overline{\mathrm{AFA}}$ are synchronized to CLKA. $\overline{\mathrm{EFB}}$, $\overline{\mathrm{AEB}}$, $\overline{\mathrm{FFB}}$, and $\overline{\mathrm{AFB}}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF 36-BIT WORDS IN FIFO1†	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{\mathrm{EFB}}$	$\overline{\mathrm{AEB}}$	$\overline{\mathrm{AFA}}$	$\overline{\mathrm{FFA}}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

Table 5. FIFO2 Flag Operation

NUMBER OF 36-BIT WORDS IN FIFO2†	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	$\overline{\mathrm{EFA}}$	$\overline{\mathrm{AEA}}$	$\overline{\mathrm{AFB}}$	$\overline{\mathrm{FFB}}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flags ($\overline{EFA}$, $\overline{EFB}$)

The empty flag of a FIFO is synchronized to the port clock that reads data from its array. When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored. When reading FIFO1 with a byte or word size on port B, $\overline{EFB}$ is set low when the fourth byte or second word of the last long word is read.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 13 and 14).

full flags ($\overline{FFA}$, $\overline{FFB}$)

The full flag of a FIFO is synchronized to the port clock that writes data to its array. When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock. Therefore, a full flag is low if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the full flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 15 and 16).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). An almost-empty flag is low when the FIFO contains X or less long words in memory and is high when the FIFO contains (X + 1) or more long words.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more long words remains low if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) long words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 17 and 18).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). An almost-full flag is low when the FIFO contains (64 – X) or more long words in memory and is high when the FIFO contains [64 – (X + 1)] or less long words.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for the almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of long words in memory to [64 – (X + 1)]. An almost-full flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO read that reduces the number of long words in memory to [64 – (X + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of long words in memory to [64 – (X + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 19 and 20).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA, and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and both SIZ0 and SIZ1 are high. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When the port-A data outputs (A0–A35) are active, the data on the bus comes from the FIFO2 output register when MBA is low and from the mail2 register when MBA is high. When the port-B data outputs (B0–B35) are active, the data on the bus comes from the FIFO1 output register when either one or both SIZ1 and SIZ0 are low and from the mail2 register when both SIZ1 and SIZ0 are high. The mail1 register flag ($\overline{MBF1}$) is set high by a rising CLKB edge when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and both SIZ1 and SIZ0 are high. The mail2 register flag ($\overline{MBF2}$) is set high by a rising CLKA edge when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is high. The data in the mail register remains intact after it is read and changes only when new data is written to the register.

dynamic bus sizing

The port-B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from FIFO1 or written to FIFO2. Word- and byte-size bus selections can utilize the most significant bytes of the bus (big endian) or least significant bytes of the bus (little endian). Port-B bus size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port-B bus size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{BE}$) input are stored on each CLKB low-to-high transition. The stored port-B bus size selection is implemented by the next rising edge on CLKB according to Figure 1.

Only 36-bit long-word data is written to or read from the two FIFO memories on the SN74ABT3614. Bus-matching operations are done after data is read from the FIFO1 RAM and before data is written to the FIFO2 RAM. Port-B bus sizing does not apply to mail register operations.

dynamic bus sizing (continued)

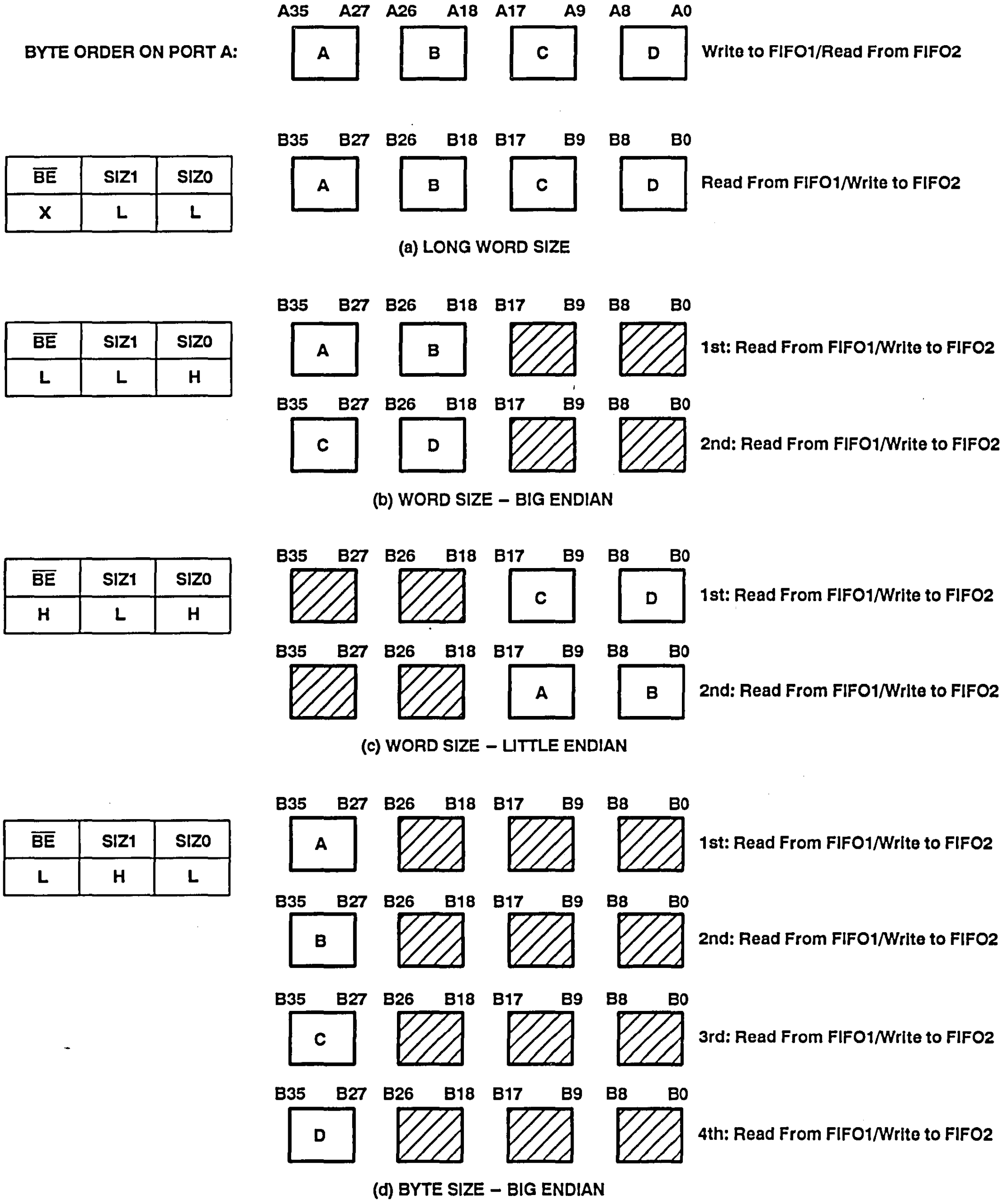
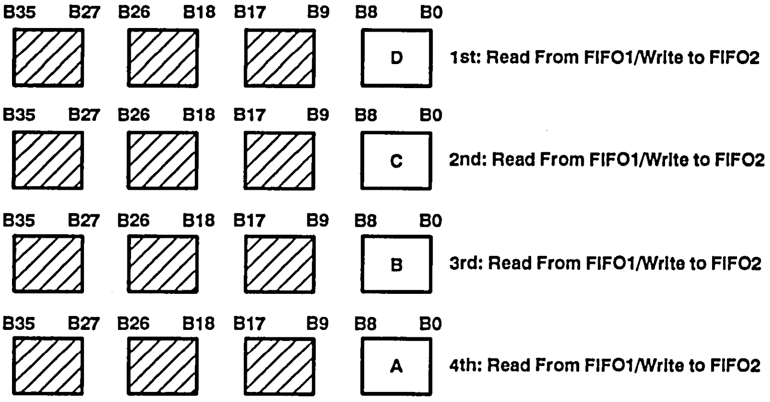


Figure 1. Dynamic Bus Sizing

dynamic bus sizing (continued)

$\overline{BE}$	SIZ1	SIZ0
H	H	L



(e) BYTE SIZE – LITTLE ENDIAN

Figure 1. Dynamic Bus Sizing (continued)

bus-matching FIFO1 reads

Data is read from the FIFO1 RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long word immediately shifts to the FIFO1 output register. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO1 output register with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads with the same bus-size implementation output the rest of the long word to the FIFO1 output register in the order shown by Figure 1.

Each FIFO1 read with a new bus-size implementation automatically unloads data from the FIFO1 RAM to its output register and auxiliary registers. Therefore, implementing a new port-B bus size and performing a FIFO1 read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread long-word data.

When reading data from FIFO1 in byte or word format, the unused B0–B35 outputs remain inactive but static with the unused FIFO1 output register bits holding the last data value to decrease power consumption.

bus-matching FIFO2 writes

Data is written to the FIFO2 RAM in 36-bit long-word increments. FIFO2 writes, with a long-word bus size, immediately store each long word in FIFO2 RAM. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKB rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in FIFO2 RAM. The bytes are arranged in the manner shown in Figure 1.

Each FIFO2 write with a new bus-size implementation resets the state machine that controls the data flow from the auxiliary registers to the FIFO2 RAM. Therefore, implementing a new bus size and performing a FIFO2 write before bytes or words stored in the auxiliary registers have been loaded to FIFO2 RAM results in a loss of data.

port-B mail register access

In addition to selecting port-B bus sizes for FIFO reads and writes, the port-B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are high, the mail1 register is accessed for a port-B long-word read and the mail2 register is accessed for a port-B long-word write. The mail register is accessed immediately and any bus-sizing operation that can be underway is unaffected by the the mail register access. After the mail register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 2 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port-B bus size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{\text{BE}}$_Q.

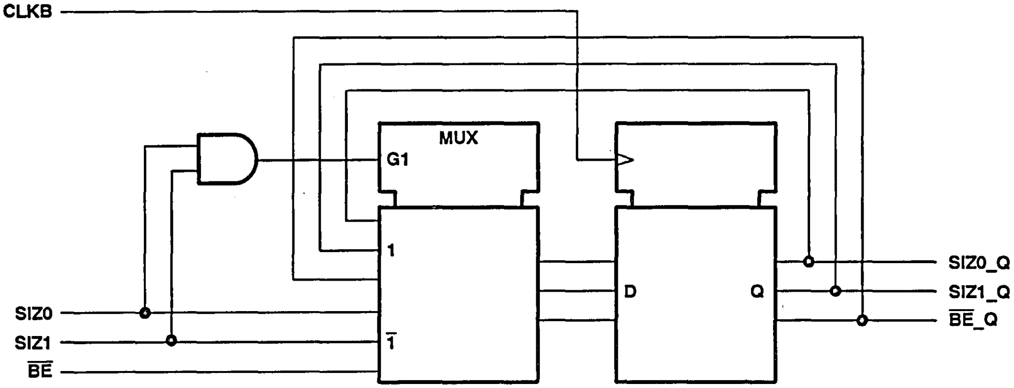


Figure 2. Logic Diagram for SIZ0, SIZ1, and $\overline{\text{BE}}$ Register

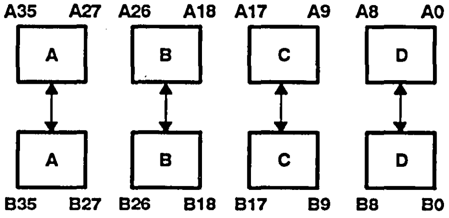
byte swapping

The byte-order arrangement of data read from FIFO1 or data written to FIFO2 can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail register data. Four modes of byte-order swapping (including no swap) can be done with any data port size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port-B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from FIFO1 or writes a new long word to FIFO2. The byte order chosen on the first byte or first word of a new long word read from FIFO1 or written to FIFO2 is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent writes or reads. Figure 3 is an example of the byte-order swapping available for long words. Performing a byte swap and bus size simultaneously for a FIFO1 read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1. Simultaneous bus-sizing and byte-swapping operations for FIFO2 writes, first loads the data according to Figure 1, then swaps the bytes as shown in Figure 3 when the long word is loaded to FIFO2 RAM.

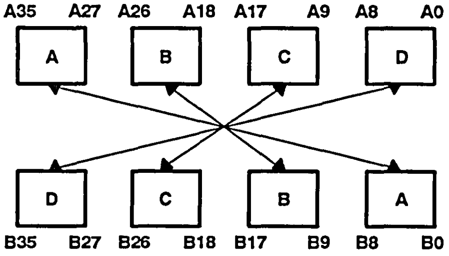
byte swapping (continued)

SW1	SW0
L	L



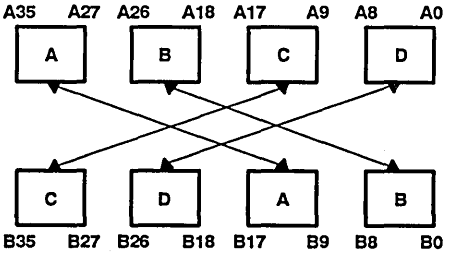
(a) NO SWAP

SW1	SW0
L	H



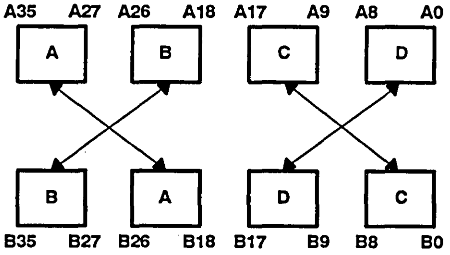
(b) BYTE SWAP

SW1	SW0
H	L



(c) WORD SWAP

SW1	SW0
H	H



(d) BYTE-WORD SWAP

Figure 3. Byte Swapping (Long-Word Size Example)

parity checking

The port-A data inputs (A0–A35) and port-B data inputs (B0–B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port-A data bus is reported by a low level on the port-A parity error flag ($\overline{\text{PEFA}}$). A parity failure on one or more bytes of the port-B data inputs that are valid for the bus-size implementation is reported by a low level on the port-B parity error flag ($\overline{\text{PEFB}}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\text{EVEN}}$) select input. A parity error on one or more valid bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, and its valid bytes are those used in a port-B bus-size implementation. When odd/even parity is selected, a port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) is low if any valid byte on the port has an odd/even number of low levels applied to the bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\text{CSA}}$ low, ENA high, W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the port-A parity error flag ($\overline{\text{PEFA}}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\text{CSB}}$ low, ENB high, and W/$\overline{\text{RB}}$ low, both SIZ0 and SIZ1 high, and PGB high, the port-B parity error flag ($\overline{\text{PEFB}}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3614 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\text{EVEN}}$ select. The generated parity bits are substituted for the levels origninally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{\text{EVEN}}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{\text{EVEN}}$ have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) is low, enable (ENA, EMB) is high, write/read select (W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) input is low, the mail register is selected (MBA is high for port A; both SIZ0 and SIZ1 are high for port B), and port parity generate select (PGA, PGB) is high. Generating parity for mail register data does not change the contents of the register.

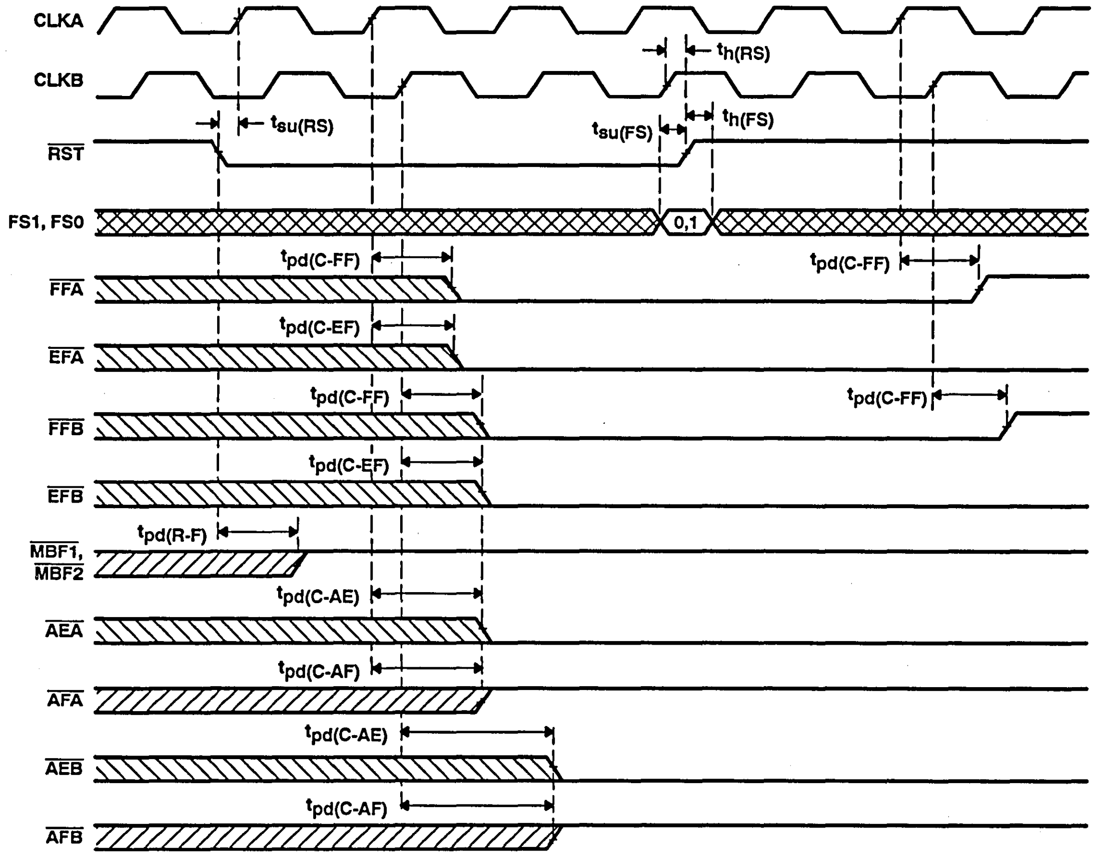
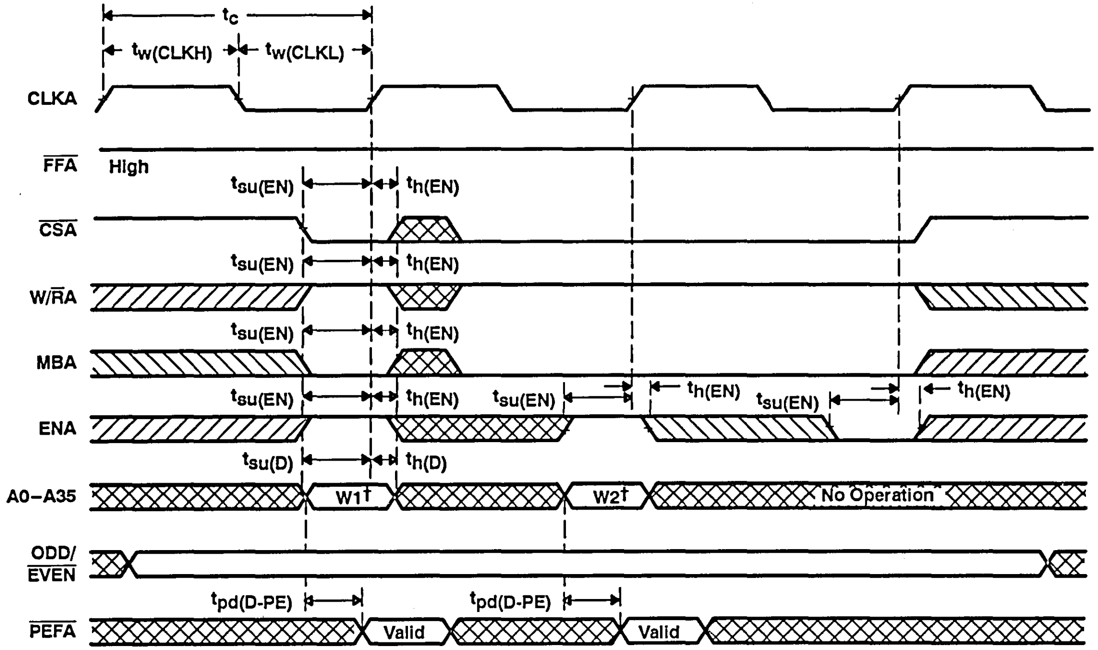
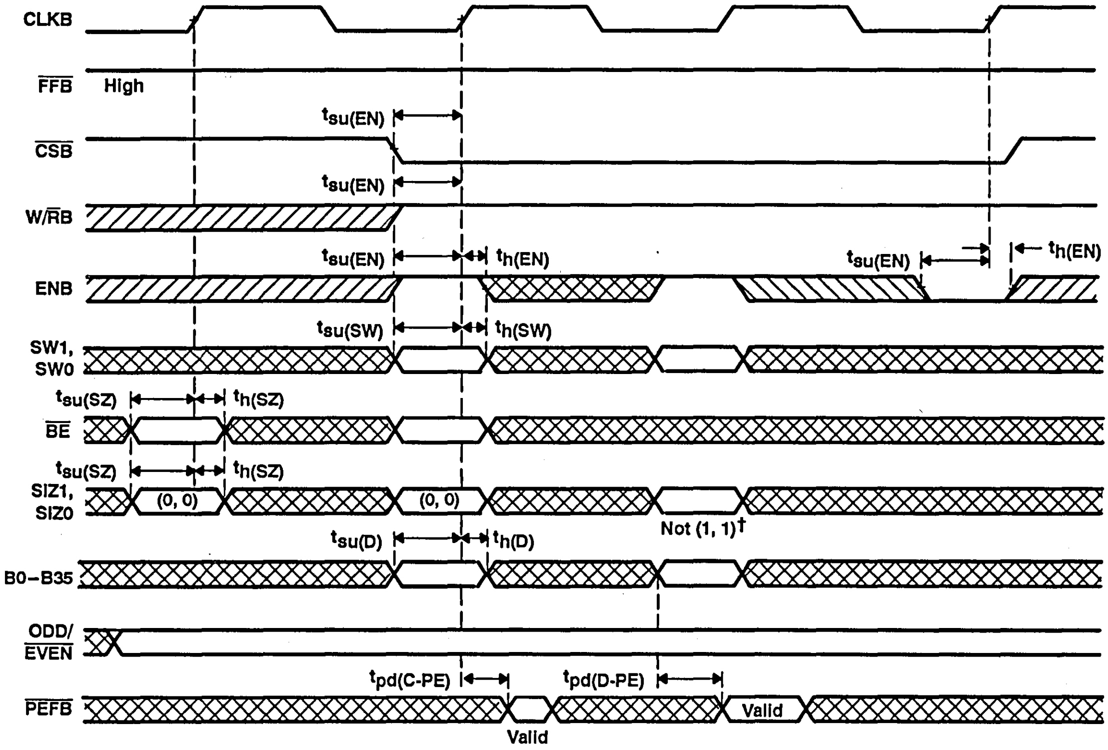


Figure 4. Device Reset Loading the X Register With the Value of Eight



† Written to FIFO1

Figure 5. Port-A Write Cycle Timing for FIFO1

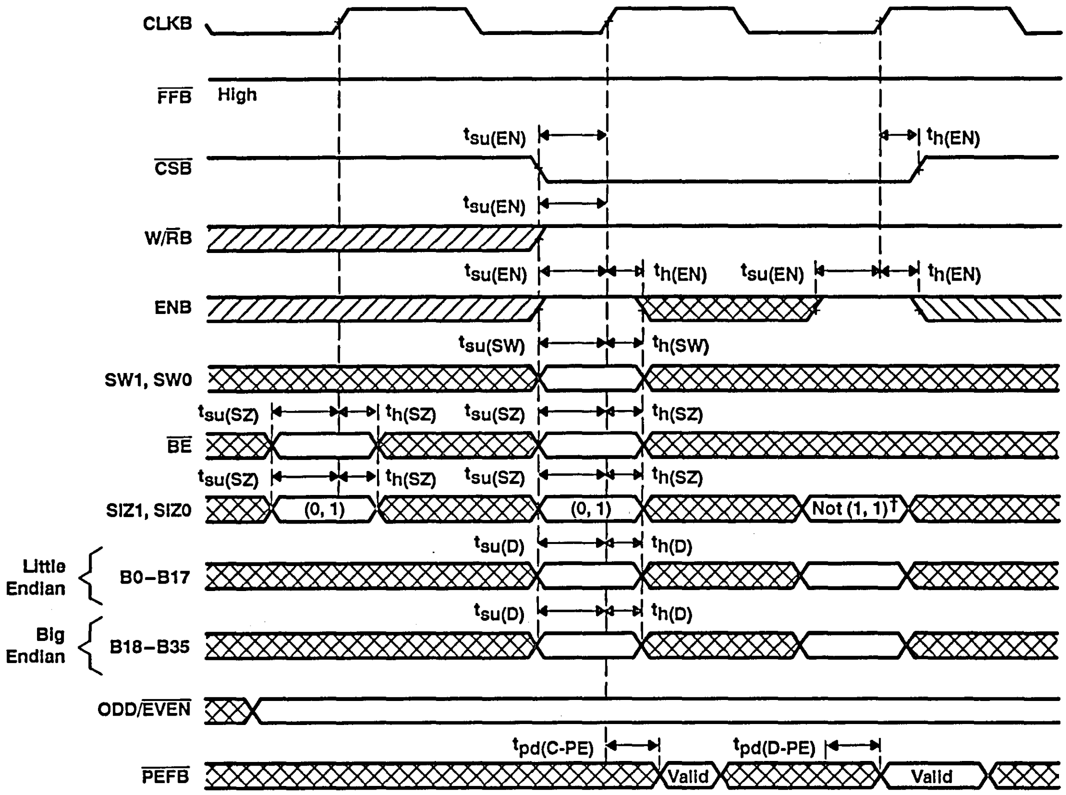


† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

DATA SWAP TABLE FOR LONG-WORD WRITES TO FIFO2

SWAP MODE		DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0	A35–A27	A26–A18	A17–A9	A8–A0
L	L	A	B	C	D	A	B	C	D
L	H	D	C	B	A	A	B	C	D
H	L	C	D	A	B	A	B	C	D
H	H	B	A	D	C	A	B	C	D

Figure 6. Port-B Long-Word Write Cycle Timing for FIFO2



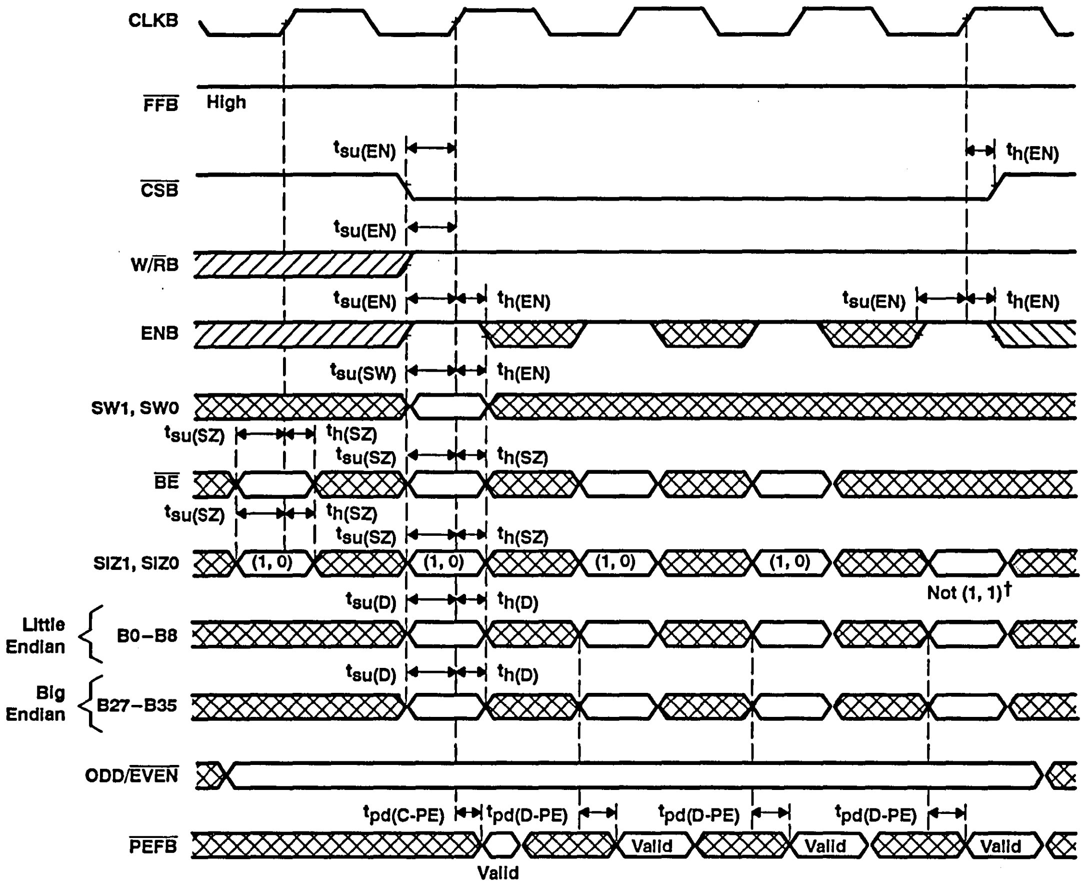
† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

NOTE A: PEFB indicates parity error for the following bytes: B35–B27 and B26–B18 for big-endian bus, and B17–B9 and B8–B0 for little-endian bus.

DATA SWAP TABLE FOR WORD WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
			BIG ENDIAN		LITTLE ENDIAN					
SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0	A35–A27	A26–A18	A17–A9	A8–A0
L	L	1 2	A C	B D	C A	D B	A	B	C	D
L	H	1 2	D B	C A	B D	A C	A	B	C	D
H	L	1 2	C A	D B	A C	B D	A	B	C	D
H	H	1 2	B D	A C	D B	C A	A	B	C	D

Figure 7. Port-B Word Write Cycle Timing for FIFO2



† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

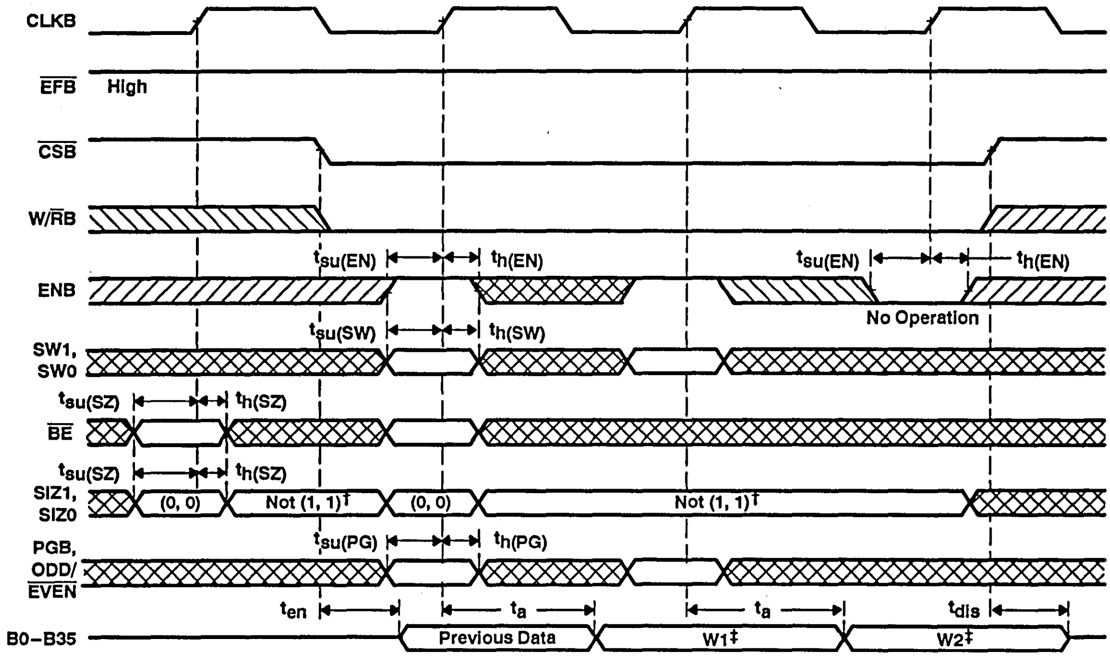
NOTE A: PEFB indicates parity error for the following bytes: B35–B27 for big-endian bus and B17–B9 for little-endian bus.

Figure 8. Port-B Byte Write Cycle Timing for FIFO2

DATA SWAP TABLE FOR BYTE WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
			BIG ENDIAN	LITTLE ENDIAN				
SW1	SW0		B35–B27	B8–B0	A35–A27	A26–A18	A17–A9	A8–A0
L	L	1	A	D	A	B	C	D
		2	B	C				
		3	C	B				
		4	D	A				
L	H	1	D	A	A	B	C	D
		2	C	B				
		3	B	C				
		4	A	D				
H	L	1	C	B	A	B	C	D
		2	D	A				
		3	A	D				
		4	B	C				
H	H	1	B	C	A	B	C	D
		2	A	D				
		3	D	A				
		4	C	B				

Figure 8. Port-B Byte Write Cycle Timing for FIFO2 (continued)

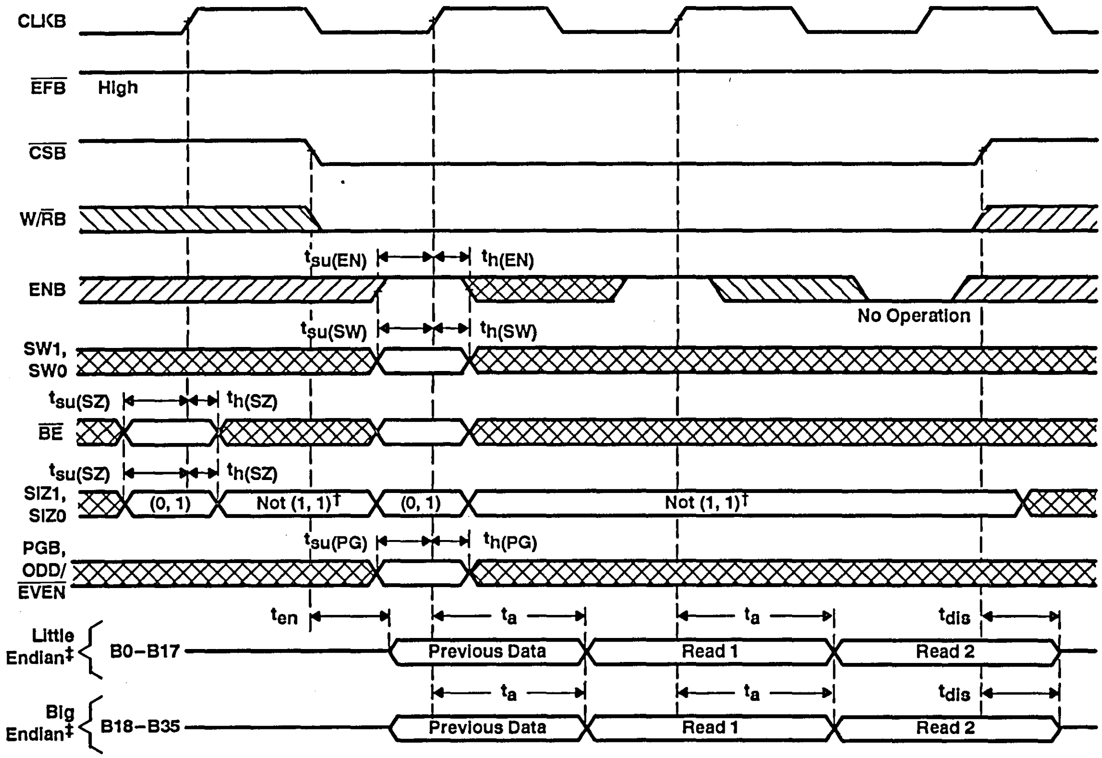


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Data read from FIFO1.

DATA SWAP TABLE FOR LONG-WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		DATA READ FROM FIFO1			
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 9. Port-B Long-Word Read Cycle Timing for FIFO1

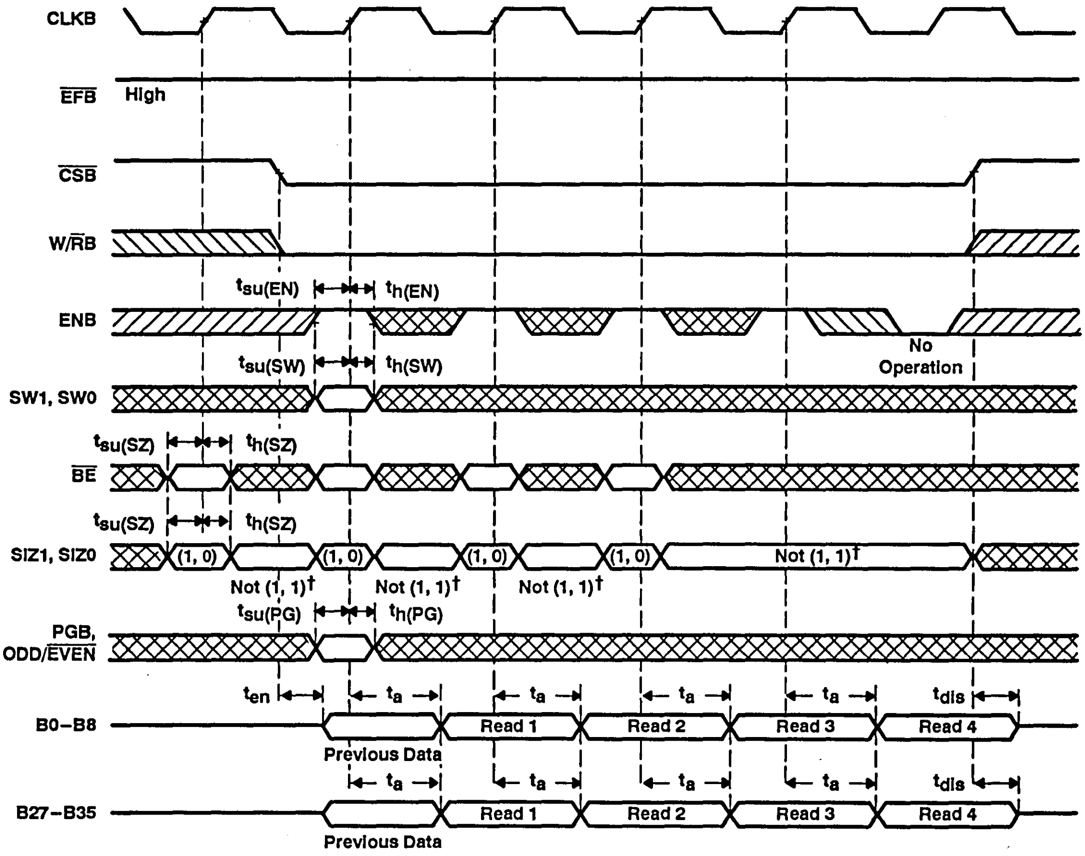


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Unused word B0–B17 or B18–B35 holds last FIFO1 output register data for word-size reads.

DATA SWAP TABLE FOR WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1			
							BIG ENDIAN		LITTLE ENDIAN	
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	1	A	B	C	D
						2	C	D	A	B
A	B	C	D	L	H	1	D	C	B	A
						2	B	A	D	C
A	B	C	D	H	L	1	C	D	A	B
						2	A	B	C	D
A	B	C	D	H	H	1	B	A	D	C
						2	D	C	B	A

Figure 10. Port-B Word Read Cycle Timing for FIFO1



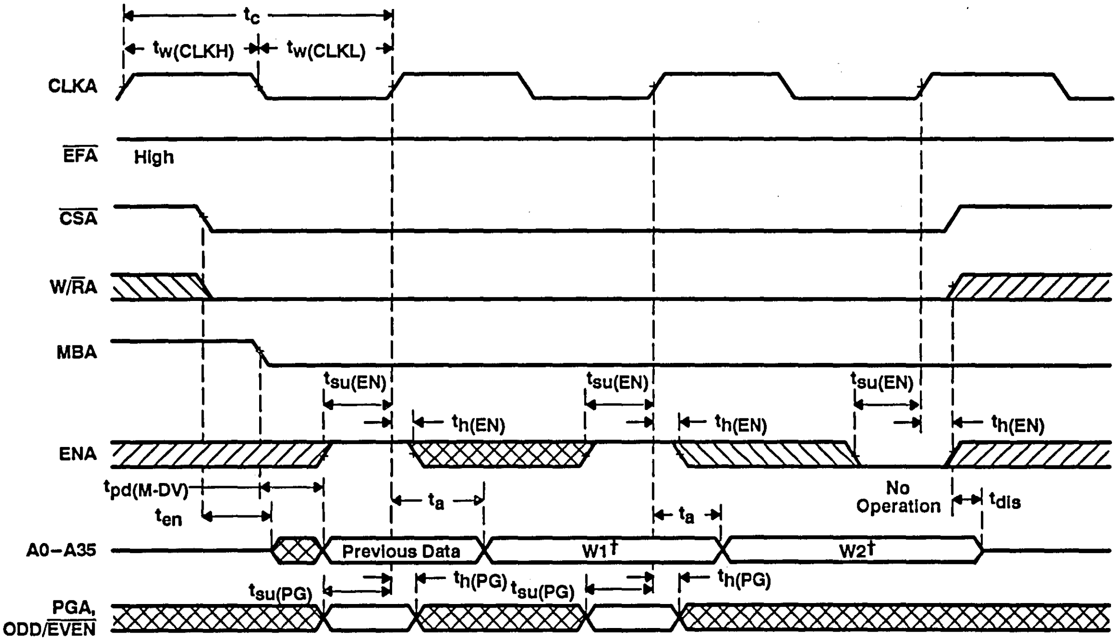
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
NOTE A: Unused bytes hold last FIFO1 output register data for byte-size reads.

Figure 11. Port-B Byte Read Cycle Timing for FIFO1

DATA SWAP TABLE FOR BYTE READS FROM FIFO1

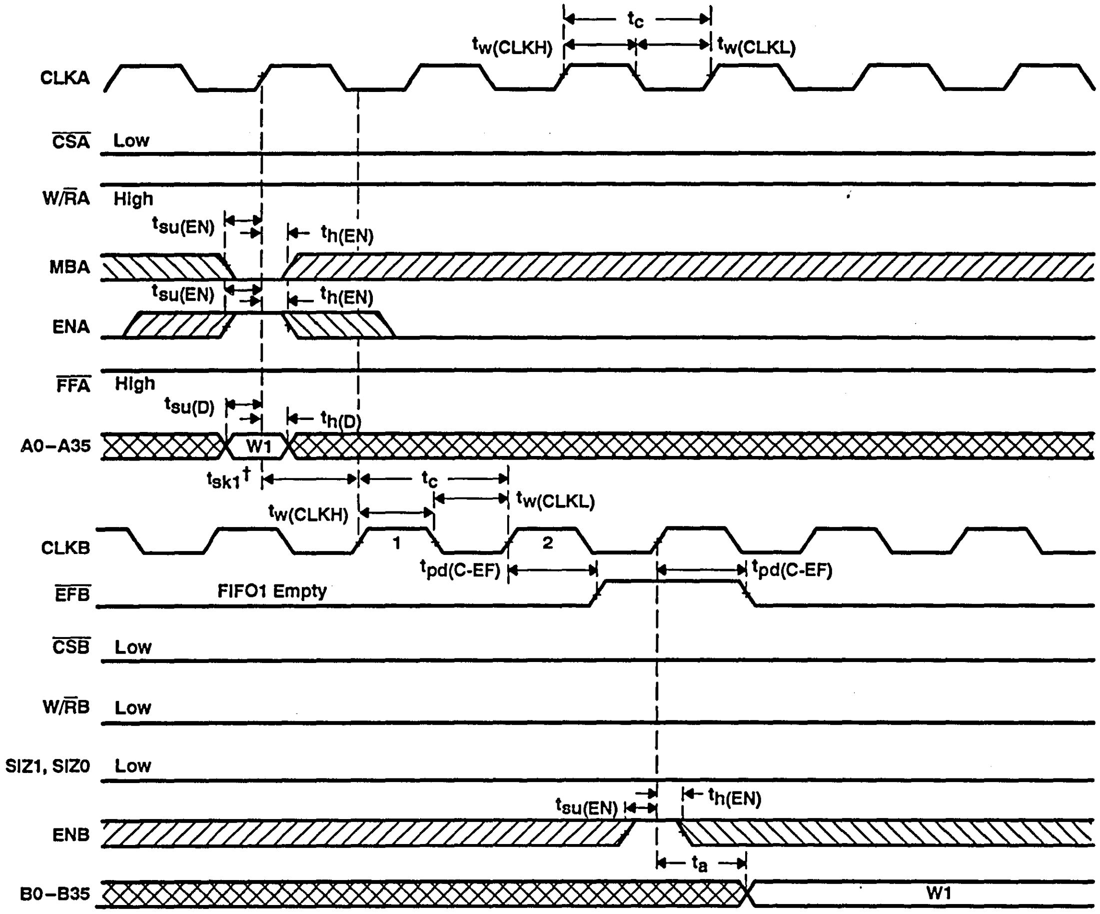
DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1	
							BIG ENDIAN	LITTLE ENDIAN
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B8–B0
A	B	C	D	L	L	1	A	D
						2	B	C
						3	C	B
						4	D	A
A	B	C	D	L	H	1	D	A
						2	C	B
						3	B	C
						4	A	D
A	B	C	D	H	L	1	C	B
						2	D	A
						3	A	D
						4	B	C
A	B	C	D	H	H	1	B	C
						2	A	D
						3	D	A
						4	C	B

Figure 11. Port-B Byte Read Cycle Timing for FIFO1 (continued)



† Read from FIFO2

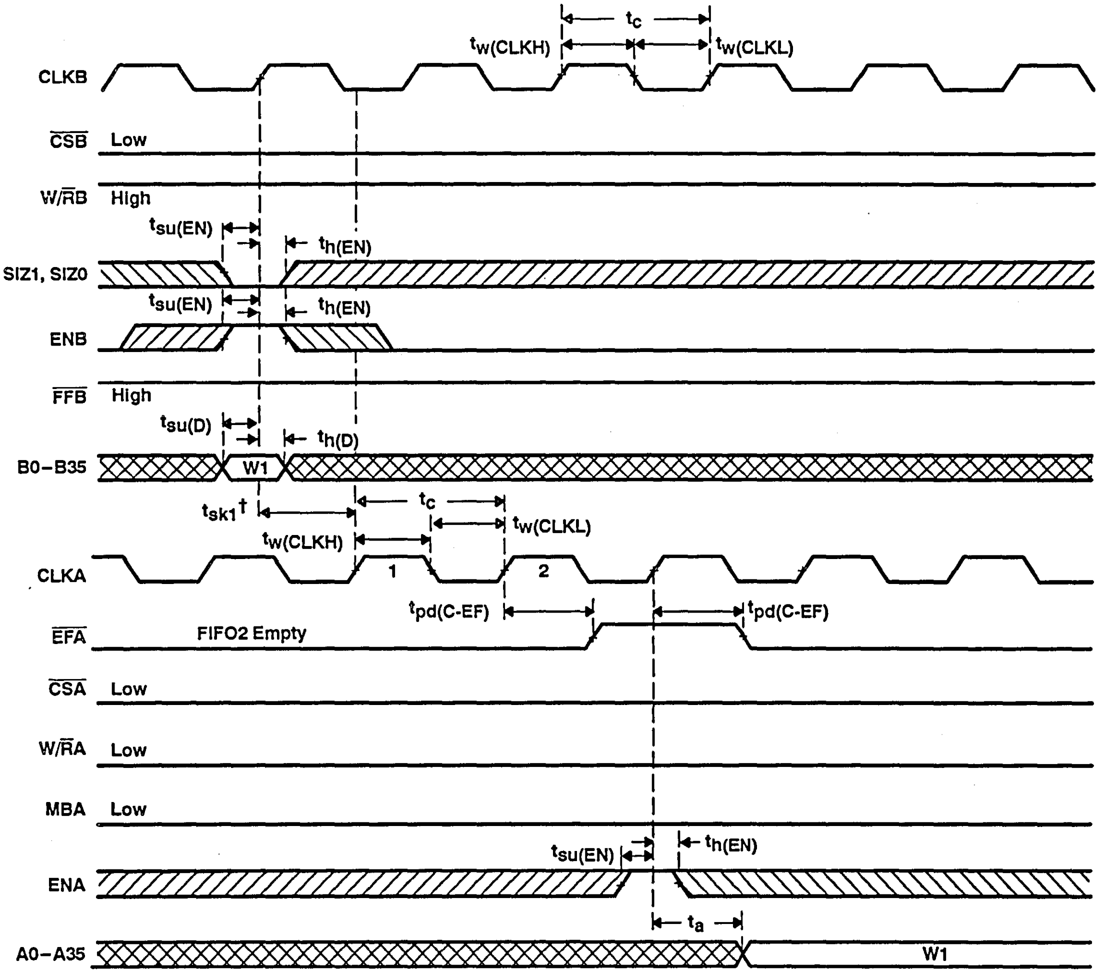
Figure 12. Port-A Read Cycle Timing for FIFO2



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of $\overline{EFB}$ high may occur one CLKB cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{EFB}$ is set low by the last word or byte read from FIFO1, respectively.

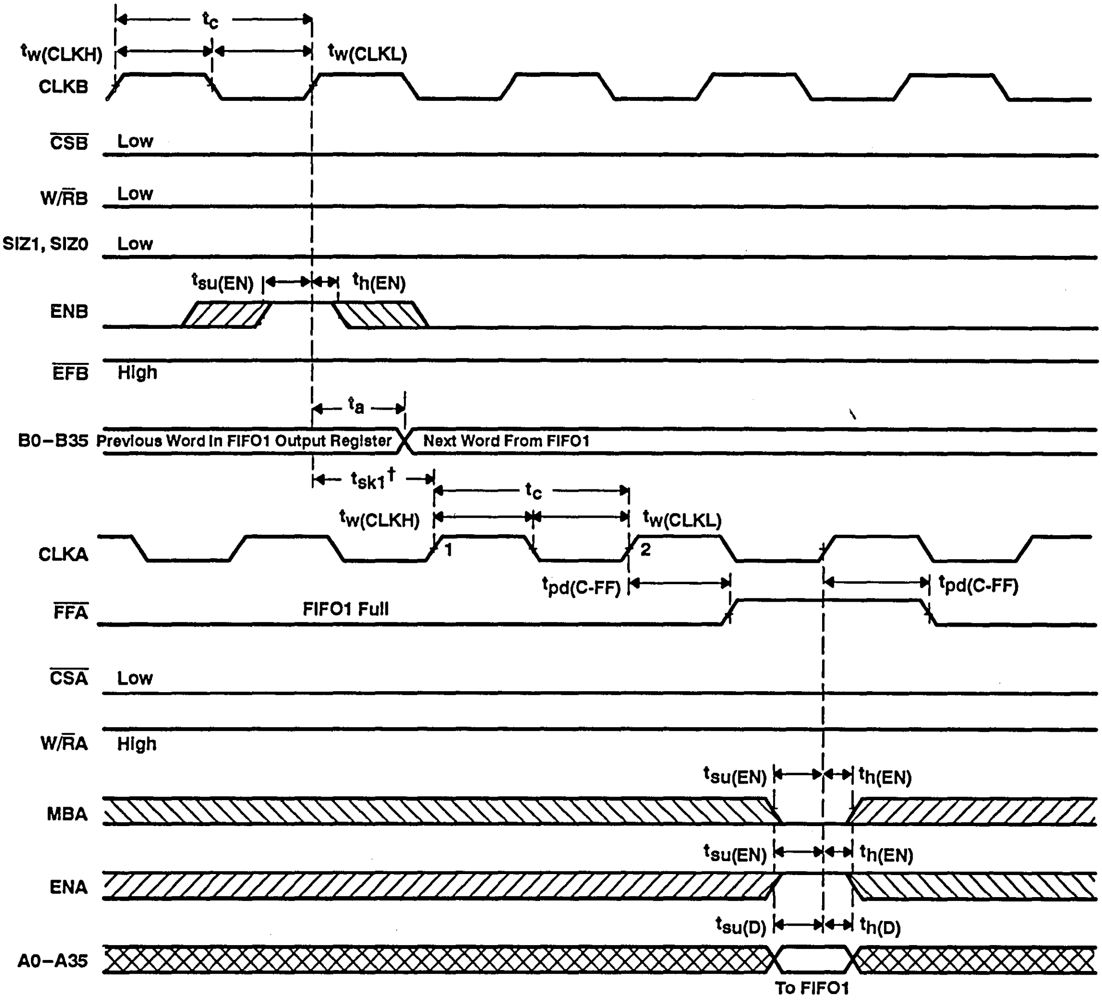
Figure 13. $\overline{EFB}$-Flag Timing and First Data Read When FIFO1 Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of $\overline{EFA}$ high may occur one CLKA cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

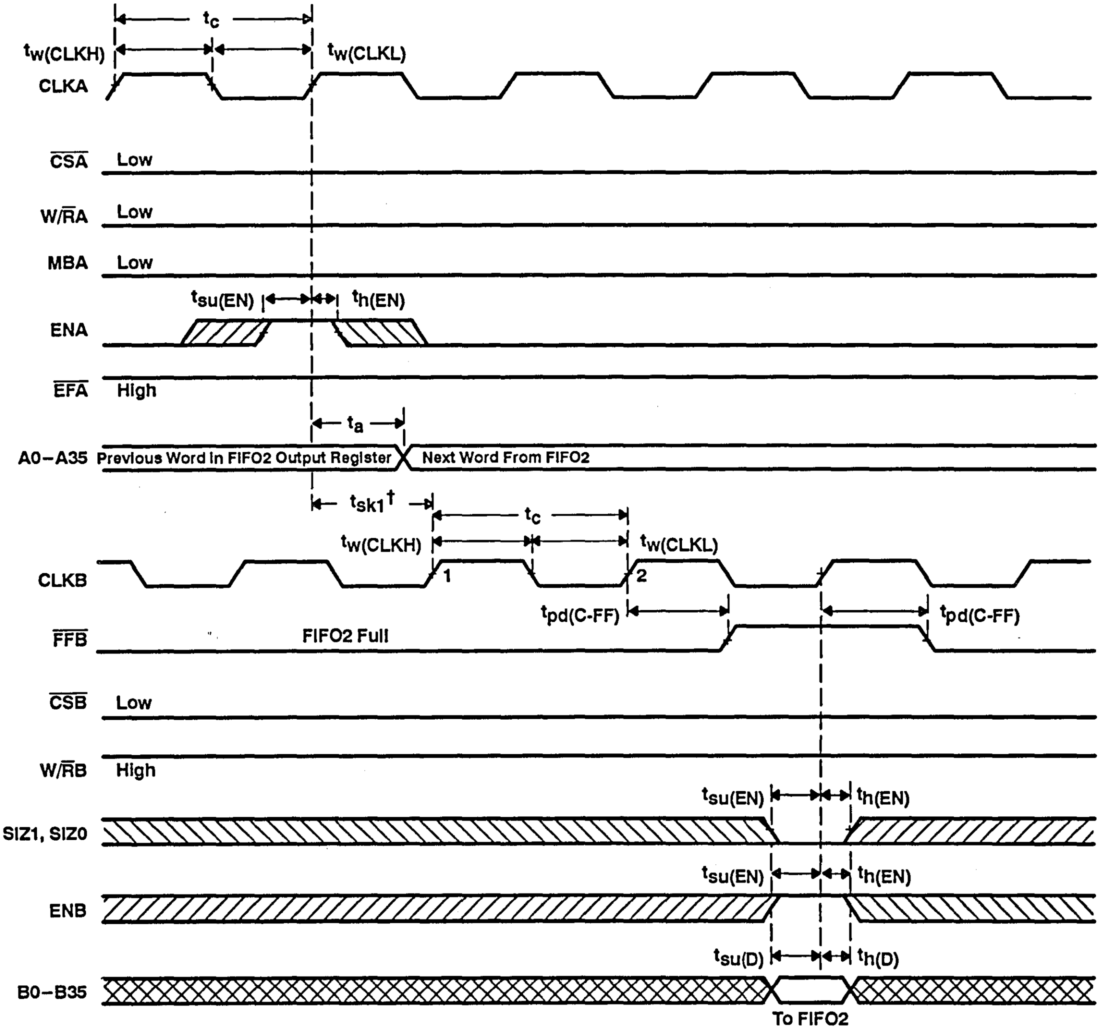
Figure 14. $\overline{EFA}$-Flag Timing and First Data Read When FIFO2 Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then $\overline{FFA}$ may transition high one CLKA cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced from the rising

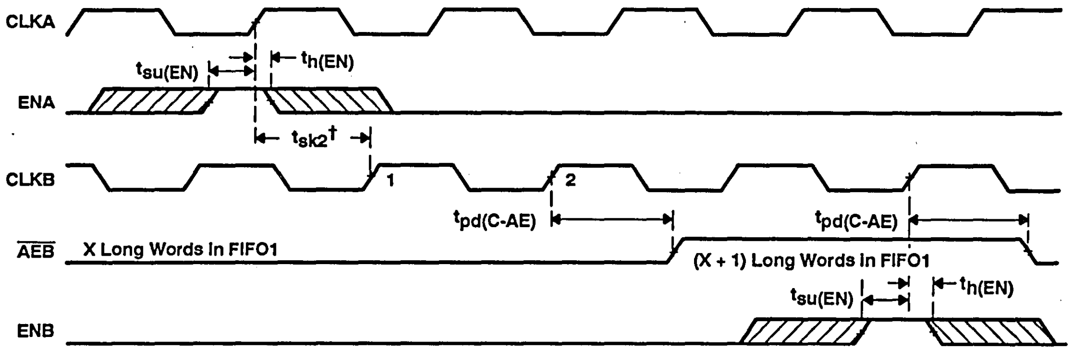
Figure 15. $\overline{FFA}$-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then $\overline{FFB}$ may transition high one CLKB cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{FFB}$ is set low by the last word or byte write of the long word, respectively.

Figure 16. $\overline{\text{FFB}}$-Flag Timing and First Available Write When FIFO2 Is Full

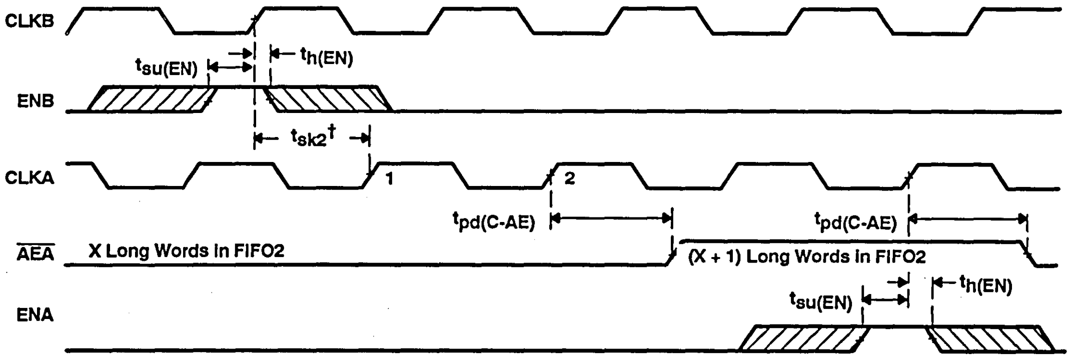


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

B. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AEB}$ is set low by the first word or byte read of the long word, respectively.

Figure 17. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty

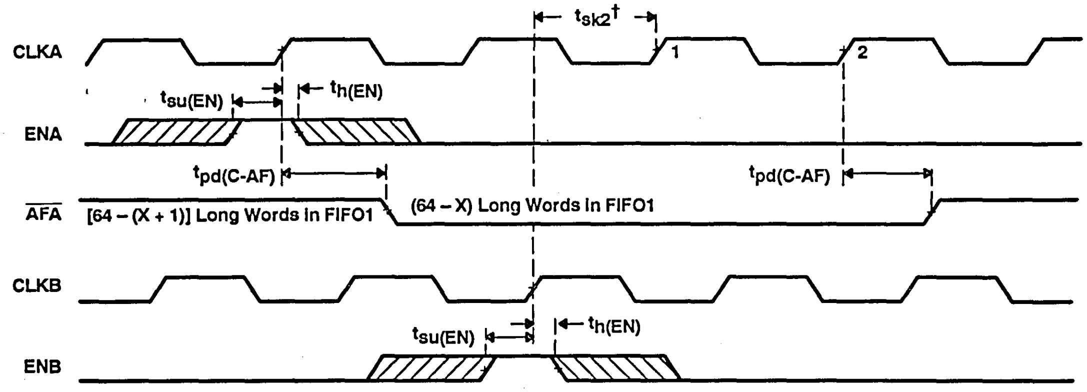


† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

B. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 18. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty

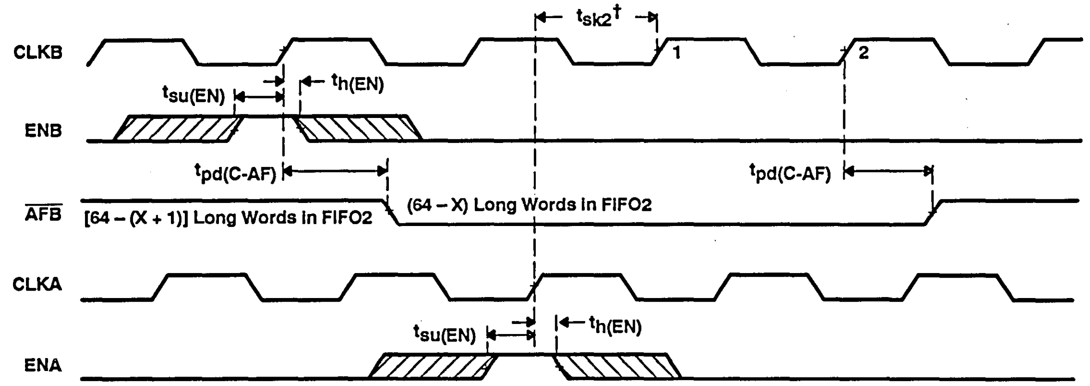


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

B. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the first word or byte read of the long word, respectively.

Figure 19. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full

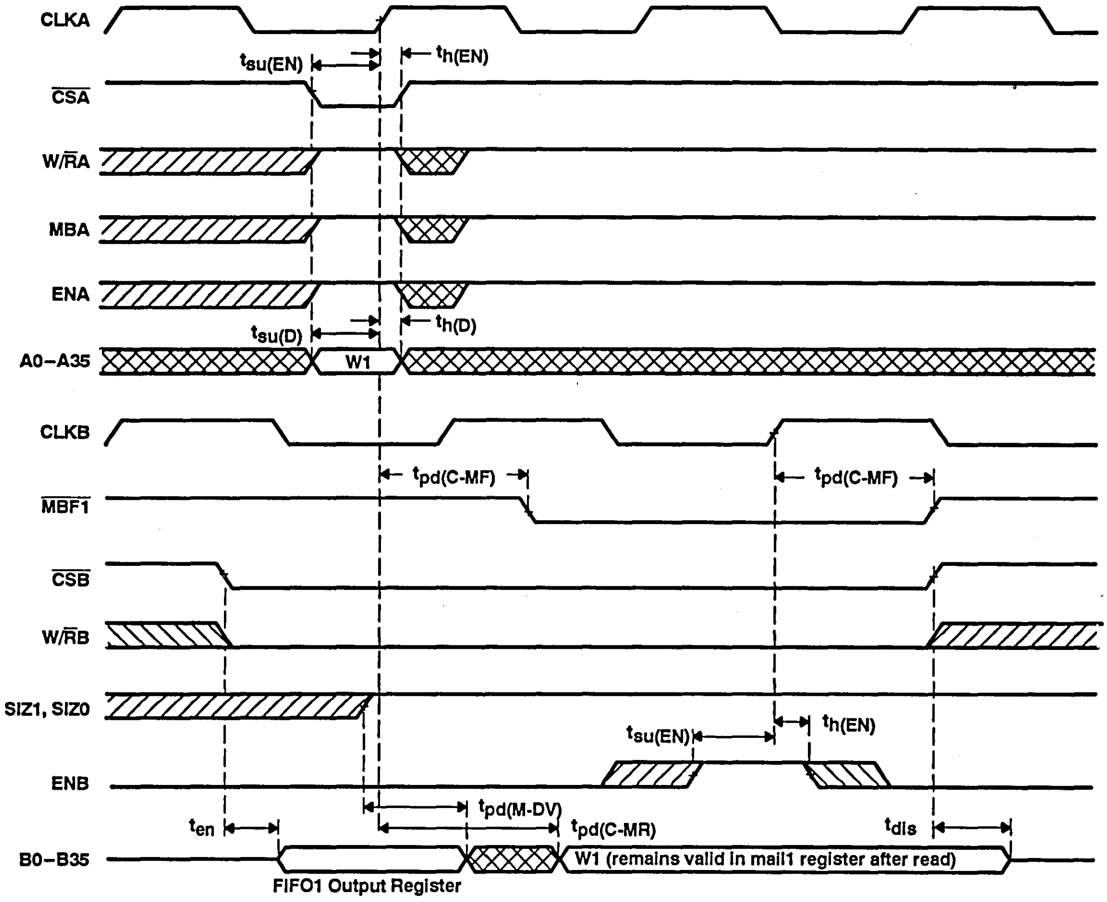


† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$= H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

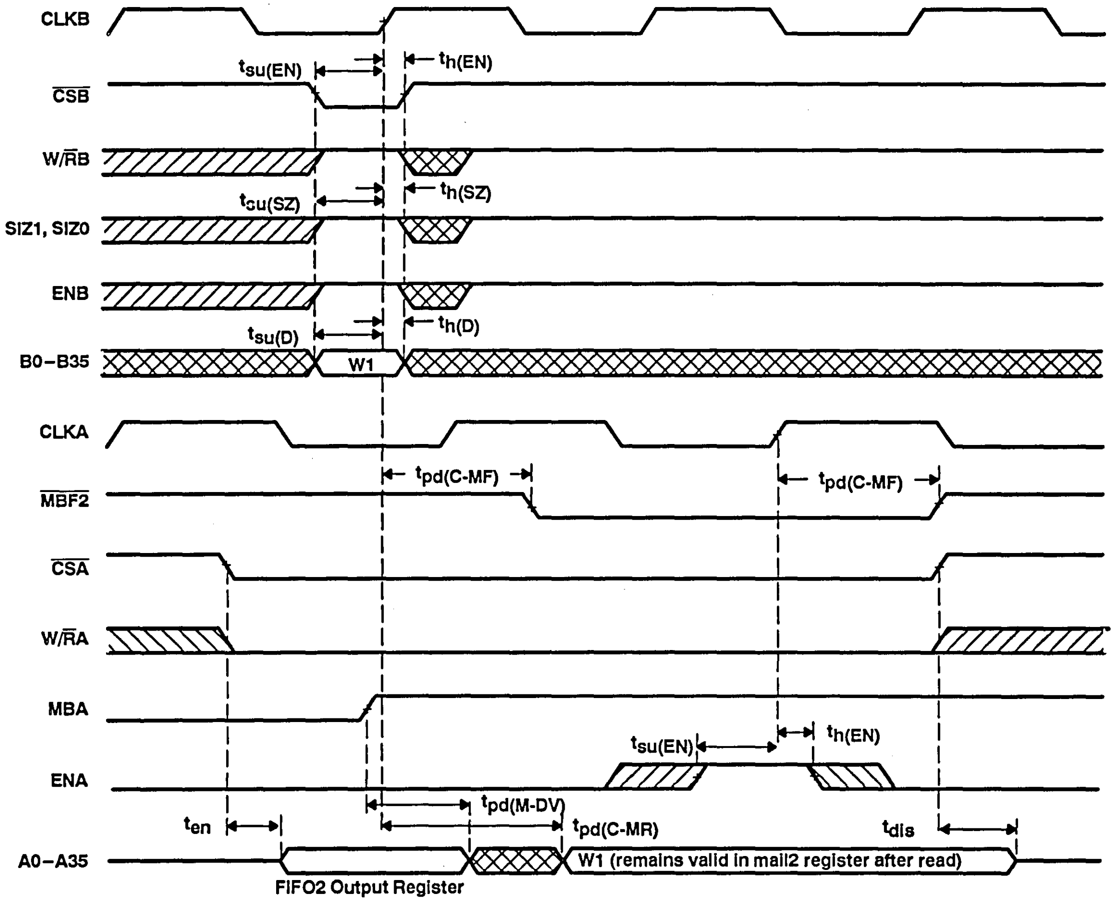
B. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AFB}$ is set low by the last word or byte write of the long word, respectively.

Figure 20. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full



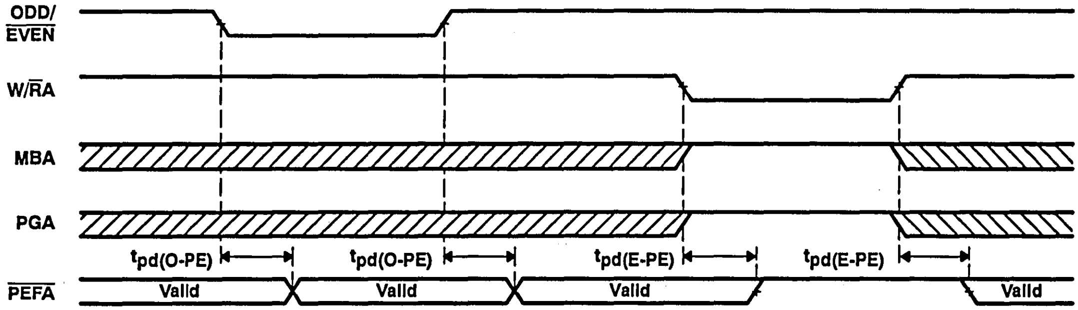
NOTE A: Port-B parity generation off (PGB = L)

Figure 21. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



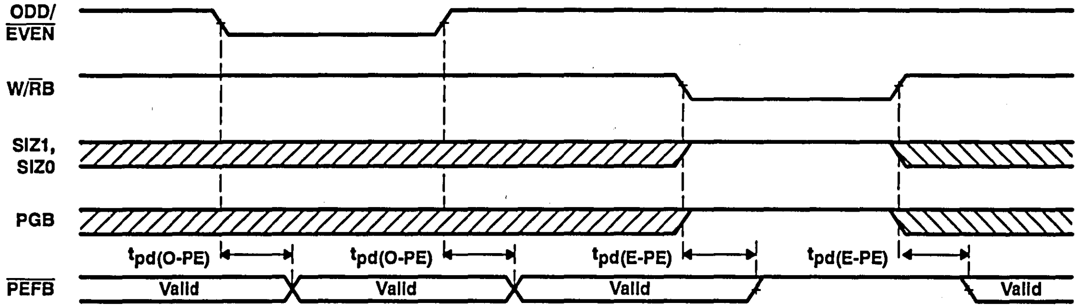
NOTE A: Port-A parity generation off (PGA = L)

Figure 22. Timing for Mail2 Register and $\overline{MBF2}$ Flag



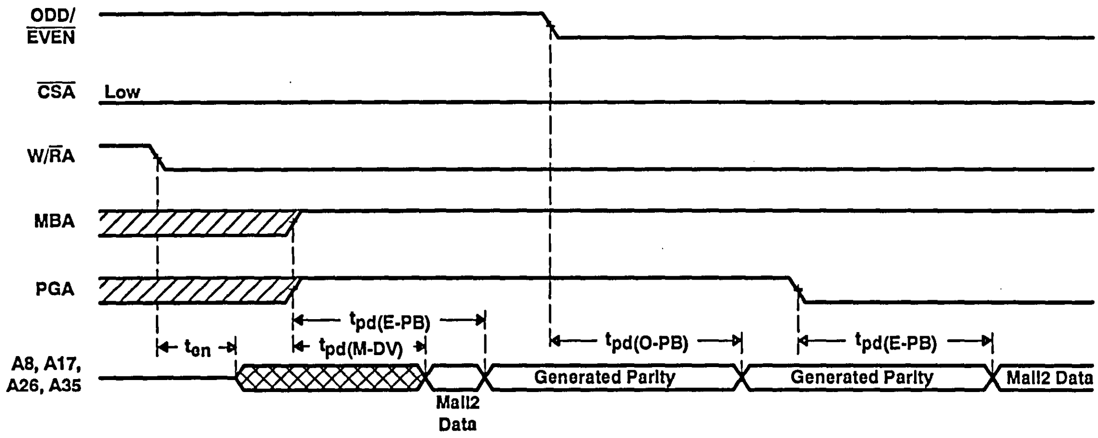
NOTE A: ENA is high and $\overline{\text{CSA}}$ is low.

Figure 23. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RA}}$, MBA, and PGA to $\overline{\text{PEFA}}$ Timing



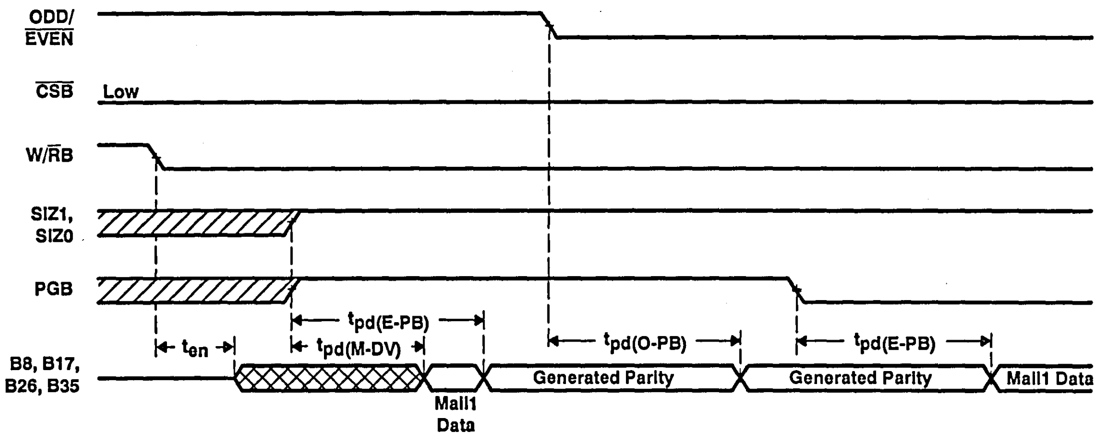
NOTE A: ENB is high and $\overline{\text{CSB}}$ is low.

Figure 24. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RB}}$, SIZ1, SIZ0, and PGB to $\overline{\text{PEFB}}$ Timing



NOTE A: ENA is high.

Figure 25. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB is high.

Figure 26. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±500 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −4 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA				0.5	V
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or 0				±50	µA
I_{OZ}	V_{CC} = 5.5 V, V_O = V_{CC} or 0				±50	µA
I_{CC}	V_{CC} = 5.5 V, I_O = 0 mA, V_I = V_{CC} or GND	Outputs high			30	mA
		Outputs low			130	
		Outputs disabled			30	
C_i	V_I = 0, f = 1 MHz			4		pF
C_o	V_O = 0, f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 4 through 26)

		'ABT3614-15		'ABT3614-20		'ABT3614-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB before CLKB↑	5		5		6		ns
$t_{su(SZ)}$	Setup time, SIZ0, SIZ1, and $\overline{BE}$ before CLKB↑	4		5		6		ns
$t_{su(SW)}$	Setup time, SW0 and SW1 before CLKB↑	5		7		8		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑[†]	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑[‡]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	1		1		1		ns
$t_{h(SZ)}$	Hold time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2		2		2		ns
$t_{h(SW)}$	Hold time, SW0 and SW1 after CLKB↑	0		0		0		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑[†]	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑[‡]	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8		8		10		ns
t_{sk2}[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9		16		20		ns

[†] Only applies for a clock edge that does a FIFO read

[‡] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[§] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 4 through 26)

PARAMETER		'ABT3614-15		'ABT3614-20		'ABT3614-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C\text{-}FF)}$	Propagation delay time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}EF)}$	Propagation delay time, CLKA↑ to $\overline{EFA}$ and CLKB↑ to $\overline{EFB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35[†] and CLKB↑ to A0–A35[‡]	3	11	3	13	3	15	ns
$t_{pd(C\text{-}PE)}$[§]	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	11	2	12	2	13	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and SIZ1, SIZ0 to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D\text{-}PE)}$	Propagation delay time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
$t_{pd(O\text{-}PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O\text{-}PB)}$[¶]	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
$t_{pd(E\text{-}PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
$t_{pd(E\text{-}PB)}$[¶]	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{RST}$ to ($\overline{MBF1}$, $\overline{MBF2}$) high.	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and W/$\overline{RB}$ high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or W/$\overline{RB}$ low to B0–B35 at high impedance	1	8	1	9	1	11	ns

[†] Writing data to the mail1 register when the B0–B35 outputs are active and SIZ1, SIZ0 are high.
[‡] Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
[§] Only applies when a new port-B bus size is implemented by the rising CLKB edge.
[¶] Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

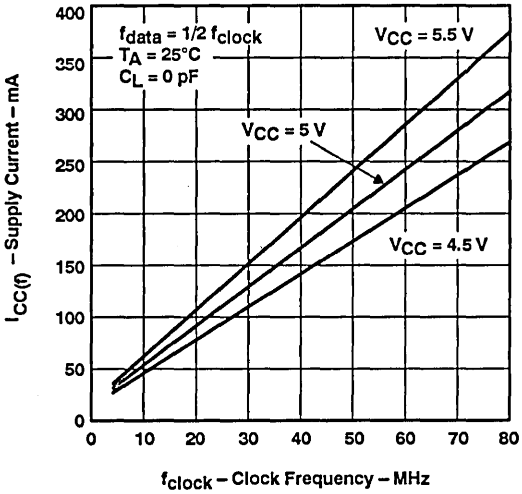


Figure 27

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 28 was taken while simultaneously reading and writing the FIFO on the SN74ACT3614 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 28, the maximum power dissipation (P_T) of the SN74ABT3614 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH}^2 \times f_o)$$

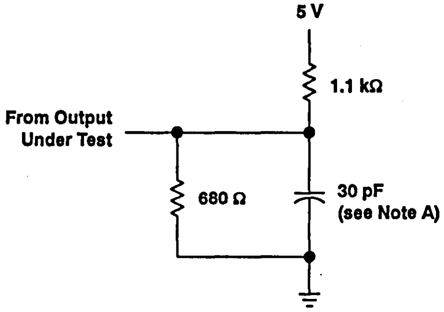
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = output high-level voltage

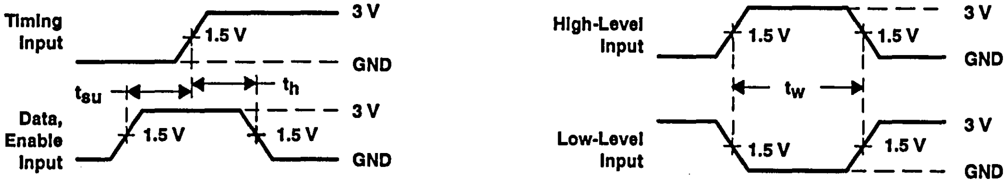
When no reads or writes are occurring on the SN74ABT3614, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.290 \text{ mA/MHz}$$

PARAMETER MEASUREMENT INFORMATION

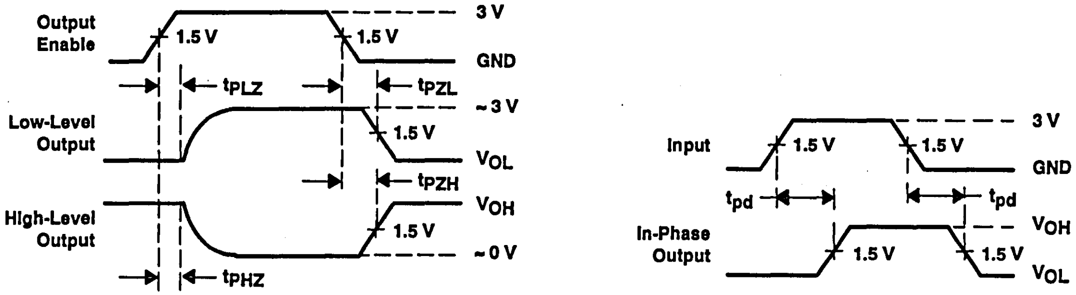


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 28. Load Circuit and Voltage Waveforms

H-B (HIGH-BANDWIDTH) COMPUTING 36-BIT CLOCKED FIFOS

Features	**Benefits**
36-bit FIFO interface	Single-chip implementation for high levels of integration
Bidirectional option	Two dual-port SRAMS allows true bidirectional capability
Mailbox-register bypass	Quick access to priority information
Microprocessor-control circuitry	Interface matches most processors and DSP bus cycle timing and communications
Multiple default values for separate AF and AE flags	Easy alternatives for flag settings
Parity generation and check	Ensures valid data
EIAJ standard 120-pin thin quad flat packs (TQFP)	67% less board space than equivalent 132-pin PQFPs; over 66% less board space than four 9-bit 32-pin PLCC equivalents
TI has established an alternate source	Standardization that comes from a common second source

SN74ABT3611
64 × 36 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCBS127C – JULY 1992 – REVISED APRIL 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **64 × 36 Clocked FIFO Buffering Data From Port A to Port B**
- **Mailbox Bypass Register In Each Direction**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **Full Flag ($\overline{FF}$) and Almost-Full Flag ($\overline{AF}$) Synchronized by CLKA**
- **Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available In Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)**

description

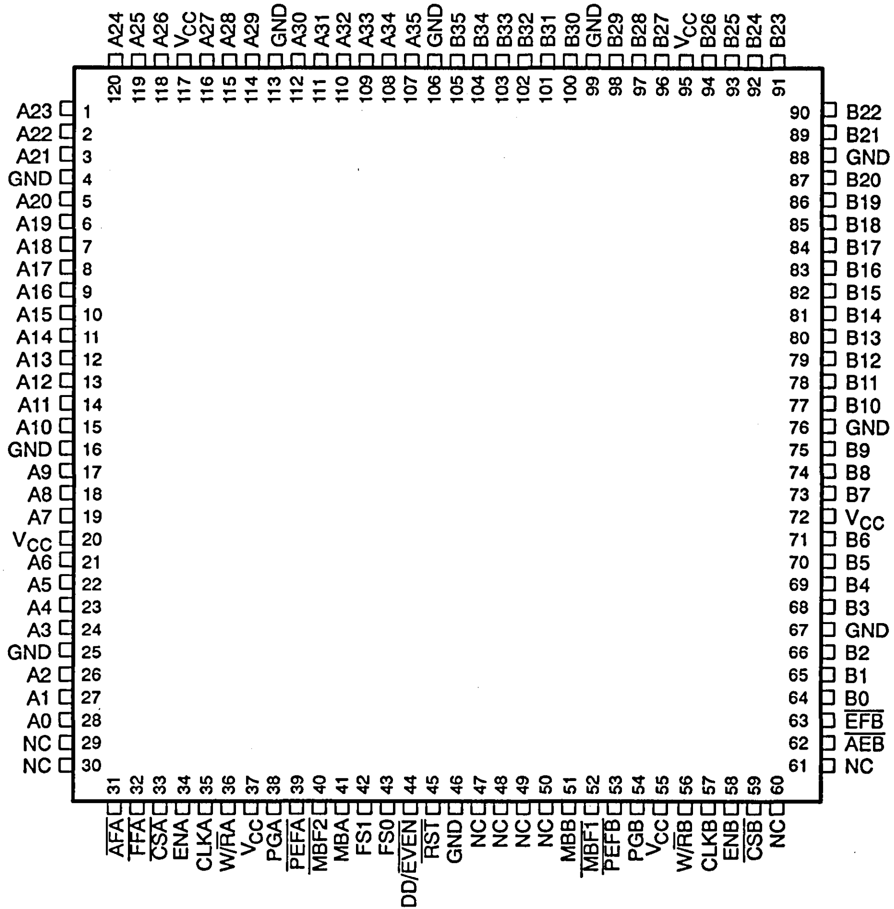
The SN74ABT3611 is a high-speed, low-power BiCMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. A 64 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words are stored in memory. Communication between each port can take place through two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

The SN74ABT3611 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{FF}$) and almost-full flag ($\overline{AF}$) of the FIFO are two-stage synchronized to the port clock that writes data to its array (CLKA). The empty flag ($\overline{EF}$) and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock that reads data from array (CLKB).

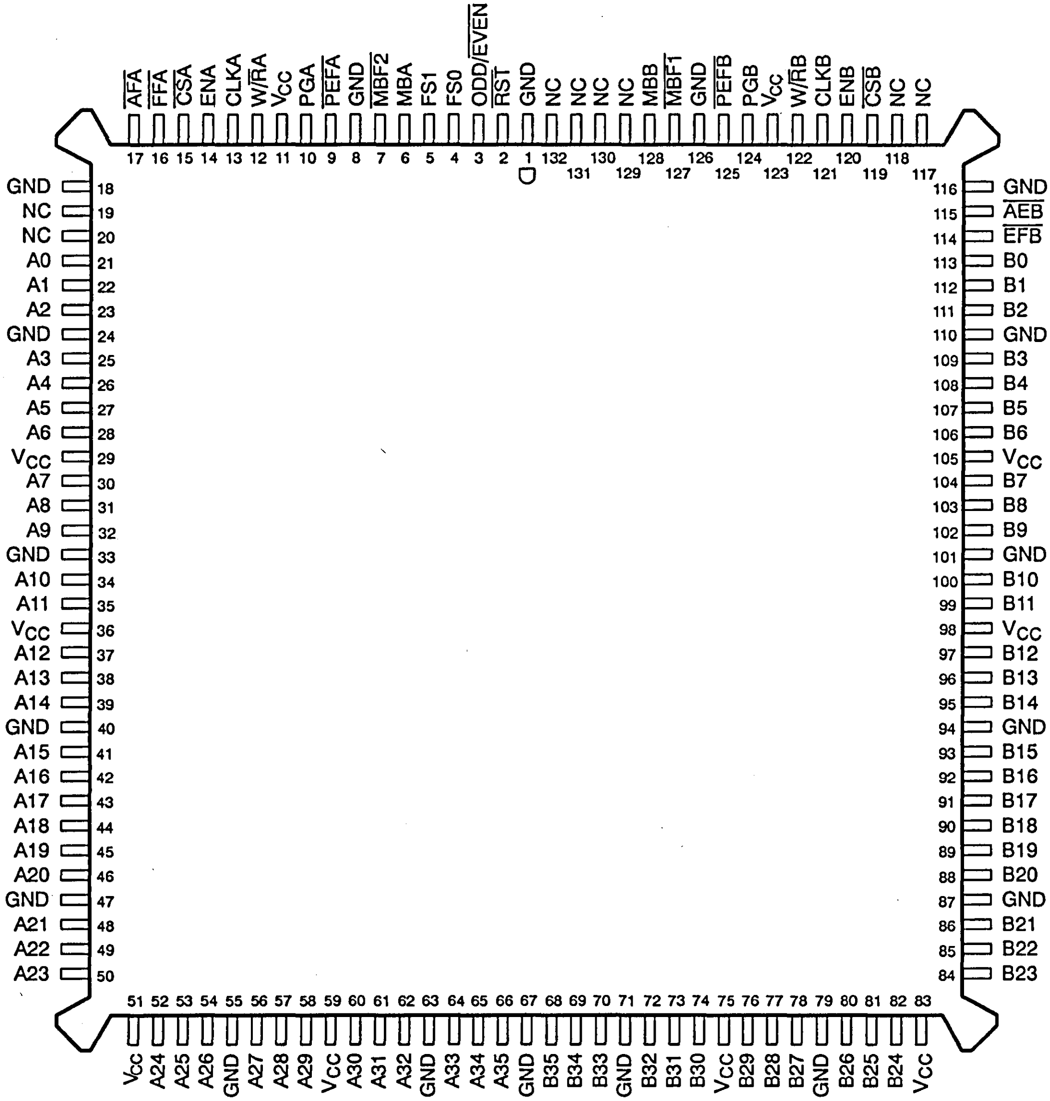
The SN74ABT3611 is characterized for operation from 0°C to 70°C.

**PCB PACKAGE
(TOP VIEW)**



NC – No internal connection

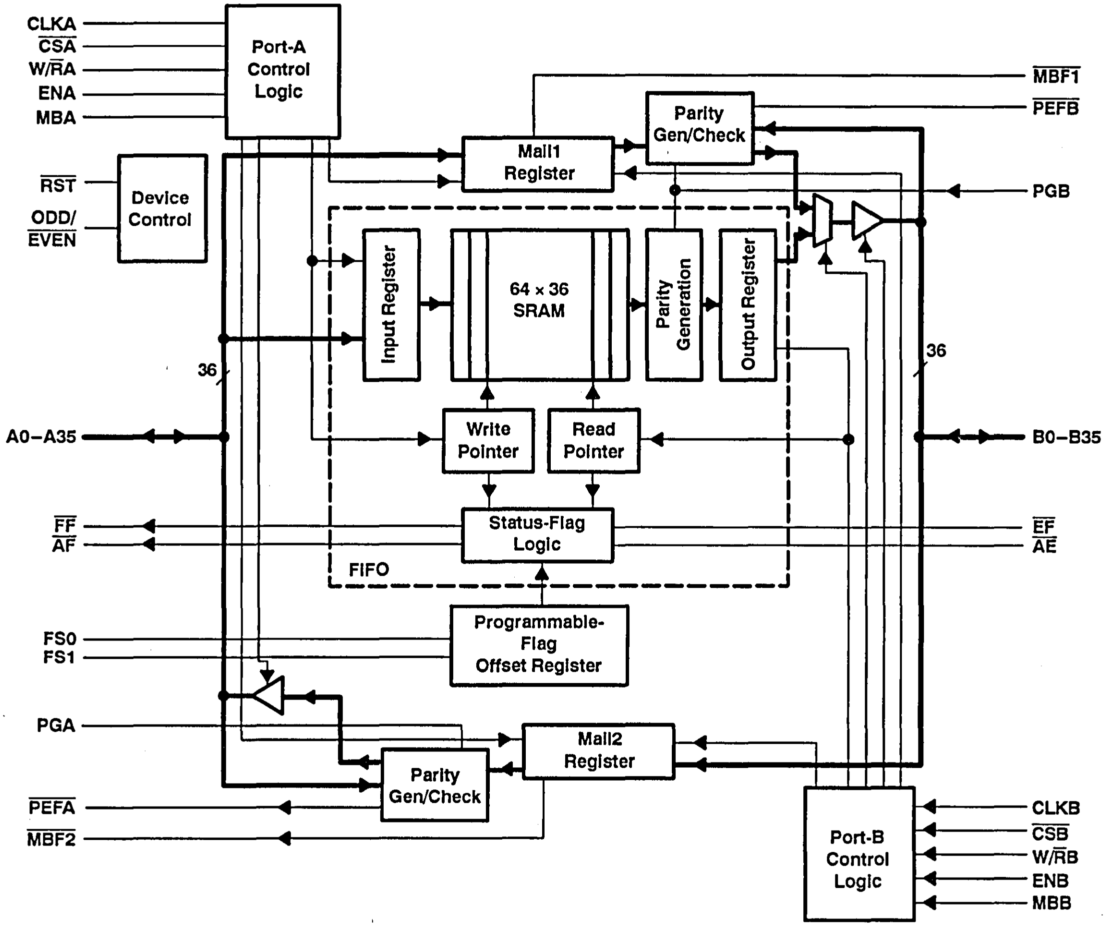
PQ PACKAGE†
(TOP VIEW)



NC – No internal connection

† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{\text{AE}}$	O	Almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{\text{AE}}$ is low when the number of words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{\text{AF}}$	O	Almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{\text{AF}}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{\text{FF}}$ and $\overline{\text{AF}}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. $\overline{\text{EF}}$ and $\overline{\text{AE}}$ are synchronized to the low-to-high transition of CLKB.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
$\overline{\text{EF}}$	O	Empty flag. $\overline{\text{EF}}$ is synchronized to the low-to-high transition of CLKB. When $\overline{\text{EF}}$ is low, the FIFO is empty and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{\text{EF}}$ is high. $\overline{\text{EF}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{\text{FF}}$	O	Full flag. $\overline{\text{FF}}$ is synchronized to the low-to-high transition of CLKA. When $\overline{\text{FF}}$ is low, the FIFO is full and writes to its memory are disabled. $\overline{\text{FF}}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
FS1, FS0	I	Flag-offset selects. The low-to-high transition of $\overline{\text{RST}}$ latches the values of FS0 and FS1, which loads one of four preset values into the almost-full and almost-empty offset register (X).
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects the FIFO output register data for output.
$\overline{\text{MBF1}}$	O	Mail1 register flag. $\overline{\text{MBF1}}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{\text{MBF1}}$ is low. $\overline{\text{MBF1}}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{\text{MBF1}}$ is set high when the device is reset.
$\overline{\text{MBF2}}$	O	Mail2 register flag. $\overline{\text{MBF2}}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{\text{MBF2}}$ is low. $\overline{\text{MBF2}}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{\text{MBF2}}$ is set high when the device is reset.
ODD/ $\overline{\text{EVEN}}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{\text{EVEN}}$ is high, and even parity is checked when ODD/$\overline{\text{EVEN}}$ is low. ODD/$\overline{\text{EVEN}}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{\text{PEFA}}$	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{\text{PEFA}}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having $\overline{\text{CSA}}$ low, ENA high, W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the $\overline{\text{PEFA}}$ flag is forced high regardless of the state of the A0 –A35 inputs.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
$\overline{\text{PEFB}}$	O (port B)	Port-B parity error flag. When any byte applied to terminals B0–B35 fails parity, $\overline{\text{PEFB}}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having $\overline{\text{CSB}}$ low, ENB high, W/$\overline{\text{RB}}$ low, MBB high, and PGB high, the $\overline{\text{PEFB}}$ flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for mail2 register reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. This sets the $\overline{\text{AF}}$, $\overline{\text{MBF1}}$, and $\overline{\text{MBF2}}$ flags high and the $\overline{\text{EF}}$, $\overline{\text{AE}}$, and $\overline{\text{FF}}$ flags low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of the FS1 and FS0 inputs to select almost-full and almost-empty flag offset.
W/$\overline{\text{RA}}$	I	Port-A write/read select. W/$\overline{\text{RA}}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
W/$\overline{\text{RB}}$	I	Port-B write/read select. W/$\overline{\text{RB}}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{\text{RB}}$ is high.

detailed description

reset

The SN74ABT3611 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the full flag ($\overline{\text{FF}}$) low, the empty flag ($\overline{\text{EF}}$) low, the almost-empty flag ($\overline{\text{AE}}$) low, and the almost-full flag ($\overline{\text{AF}}$) high. A reset also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a reset, $\overline{\text{FF}}$ is set high after two low-to-high transitions of CLKA. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the $\overline{\text{RST}}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{RA}}$). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are low. Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is high, ENA is high, MBA is low, and $\overline{\text{FF}}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{RA}}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The port-B control signals are identical to those of port A. The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select (W/$\overline{\text{RB}}$). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ or W/$\overline{\text{RB}}$ is high. The B0–B35 outputs are active when both $\overline{\text{CSB}}$ and W/$\overline{\text{RB}}$ are low. Data is read from the FIFO to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{RB}}$ is low, ENB is high, MBB is high, and $\overline{\text{EF}}$ is high (see Table 3).

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	W/$\overline{\text{RB}}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	None
L	H	H	H	↑	In high-impedance state	Mail2 write
L	L	L	L	X	Active, FIFO output register	None
L	L	H	L	↑	Active, FIFO output register	FIFO read
L	L	L	H	X	Active, mail1 register	None
L	L	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

The setup and hold-time constraints to the port clocks for the port chip selects ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) and write/read selects (W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select can change states during the setup and hold-time window of the cycle.

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of the flags to the FIFO.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN THE FIFO	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flag ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 4).

full flag ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When the full flag is high, an SRAM location is free to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write pointer is incremented. The state machine that controls the full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three port-A clock cycles. A full flag is low if less than two CLKA cycles have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 5).

almost-empty flag (AE)

The FIFO almost-empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the almost-empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). The almost-empty flag is low when the FIFO contains X or less words in memory and is high when the FIFO contains (X + 1) or more words.

Two low-to-high transitions on the port-B clock (CLKB) are required after a FIFO write for the almost-empty flag to reflect the new level of fill. The almost-empty flag of a FIFO containing (X + 1) or more words remains low if two CLKB cycles have not elapsed since the write that filled the memory to the (X + 1) level. The almost-empty flag is set high by the second CLKB low-to-high transition after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition on CLKB begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

almost-full flag (AF)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). The almost-full flag is low when the FIFO contains (64 – X) or more words in memory and is high when the FIFO contains [64 – (X + 1)] or less words.

Two low-to-high transitions on the port-A clock (CLKA) are required after a FIFO read for the almost-full flag to reflect the new level of fill. The almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two CLKA cycles have not elapsed since the read that reduced the number of words in memory to [64 – (X + 1)]. The almost-full flag is set high by the second CLKA low-to-high transition after the FIFO read that reduces the number of words in memory to [64 – (X + 1)]. A low-to-high transition on CLKA begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [64 – (X + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

mailbox registers

Two 36-bit bypass registers are on the SN74ABT3611 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by(CSA, W/RA, and ENA) with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by (CSB, W/RB, and ENB) with MBB high. Writing data to a mail register sets its corresponding flag (MBF1 or MBF2) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag (MBF1) is set high by a low-to-high transition on CLKB when a port-B read is selected by (CSB, W/RB, and ENB) with MBB high. The mail2 register flag (MBF2) is set high by a low-to-high transition on CLKA when a port-A read is selected by (CSA, W/RA, and ENA) with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

parity checking

The port-A (A0–A35) inputs and port-B (B0–B35) inputs each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a low level on the port parity error flag (PEFA, PEFB). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

parity checking (continued)

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\mathrm{EVEN}}$) select input. A parity error on one or more bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{\mathrm{PEFA}}$, $\overline{\mathrm{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, and port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35. When odd/even parity is selected, a port parity error flag ($\overline{\mathrm{PEFA}}$, $\overline{\mathrm{PEFB}}$) is low if any byte on the port has an odd/even number of low levels applied to its bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\mathrm{CSA}}$ low, ENA high, W/$\overline{\mathrm{RA}}$ low, MBA high, and PGA high, the port-A parity error flag ($\overline{\mathrm{PEFA}}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\mathrm{CSB}}$ low, ENB high, W/$\overline{\mathrm{RB}}$ low, MBB high, and PGB high, the port-B parity error flag ($\overline{\mathrm{PEFB}}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3611 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\mathrm{EVEN}}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-B parity generate select (PGB) and ODD/$\overline{\mathrm{EVEN}}$ have setup and hold-time constraints to the port-B clock (CLKB) for a rising edge of CLKB used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port write/read select (W/$\overline{\mathrm{RA}}$, W/$\overline{\mathrm{RB}}$) input is low, the port mail select (MBA, MBB) input is high, chip select ($\overline{\mathrm{CSA}}$, $\overline{\mathrm{CSB}}$) is low, enable (ENA, ENB) is high, and port parity generate select (PGA, PGB) is high. Generating parity for mail register data does not change the contents of the register.

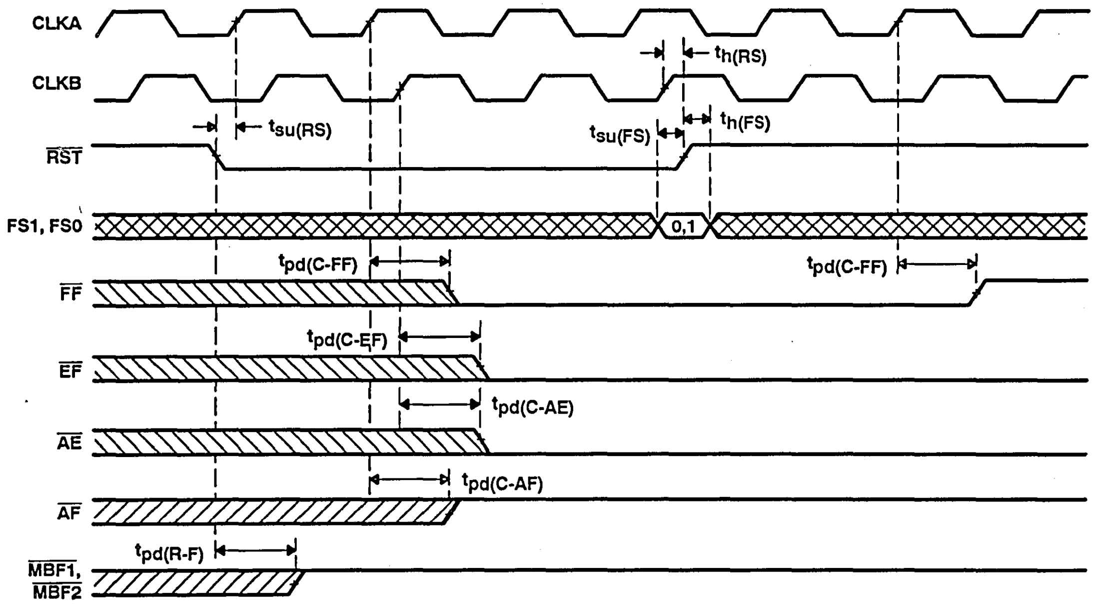


Figure 1. Device Reset Loading the X Register With the Value of Eight

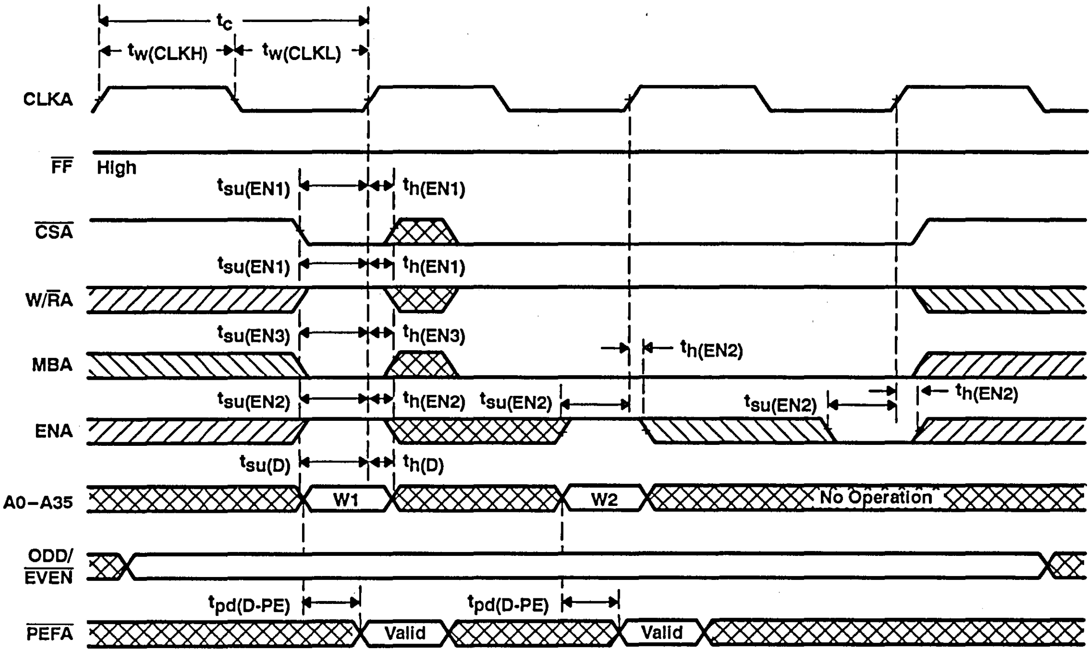


Figure 2. FIFO1-Write-Cycle Timing

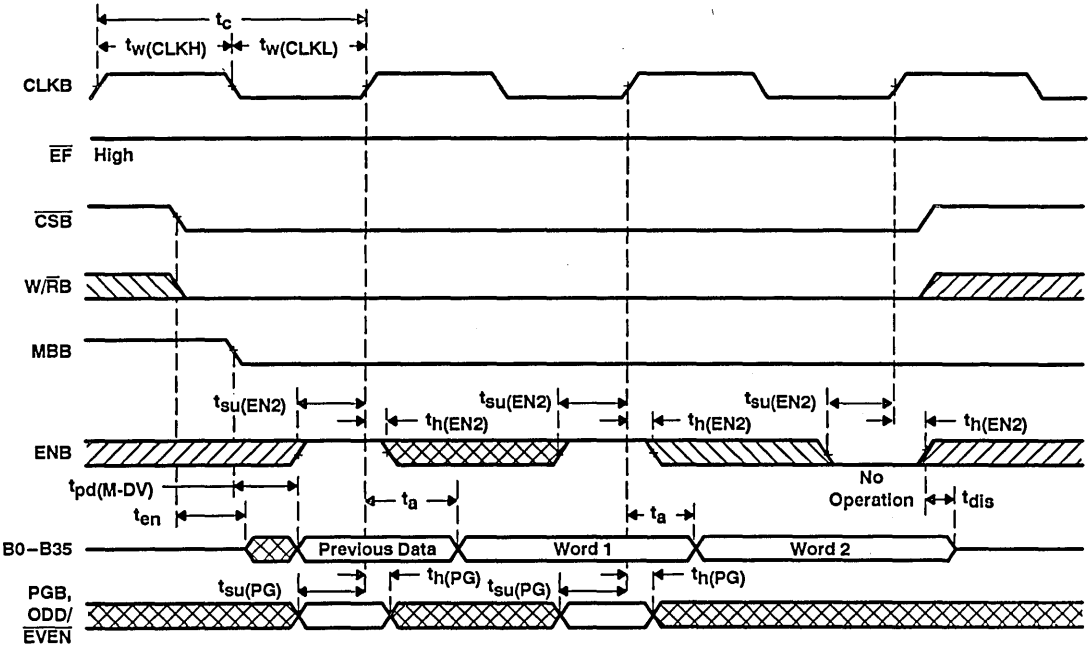
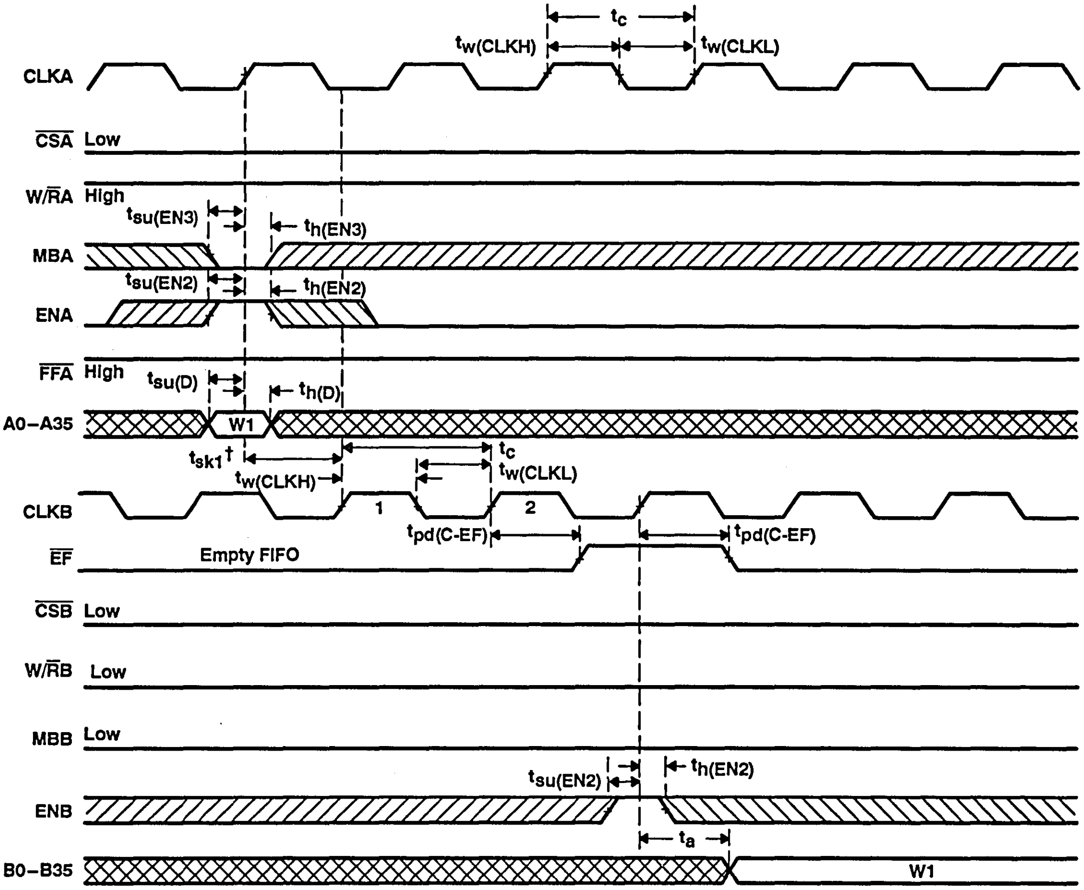
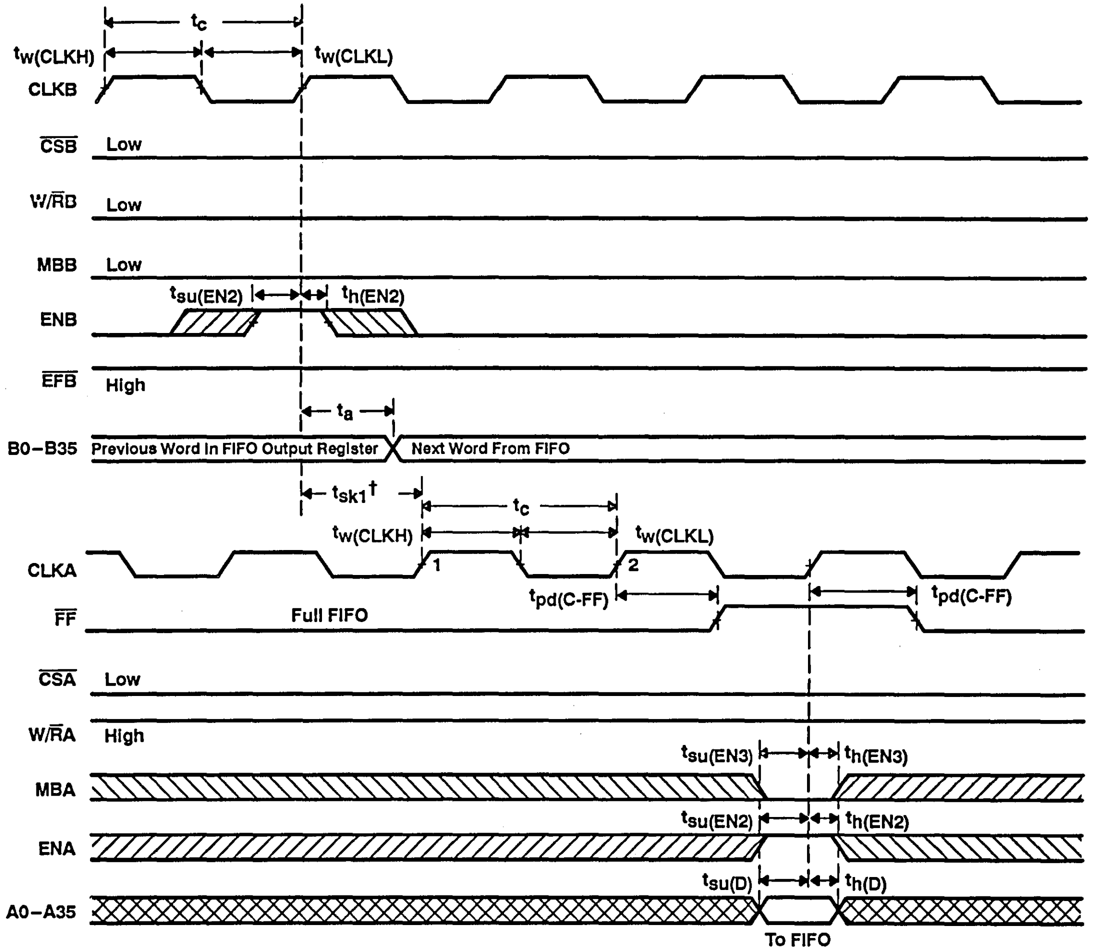


Figure 3. FIFO-Read-Cycle Timing



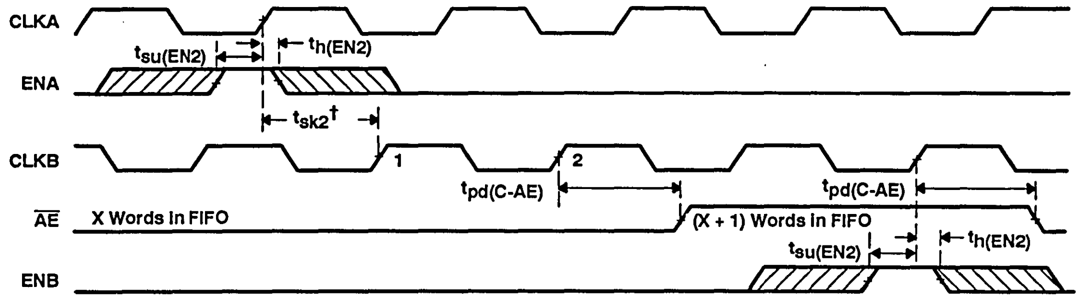
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of $\overline{EF}$ high may occur one CLKB cycle later than shown.

Figure 4. $\overline{EF}$-Flag Timing and First Data Read When the FIFO Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then $\overline{FF}$ may transition high one CLKA cycle later than shown.

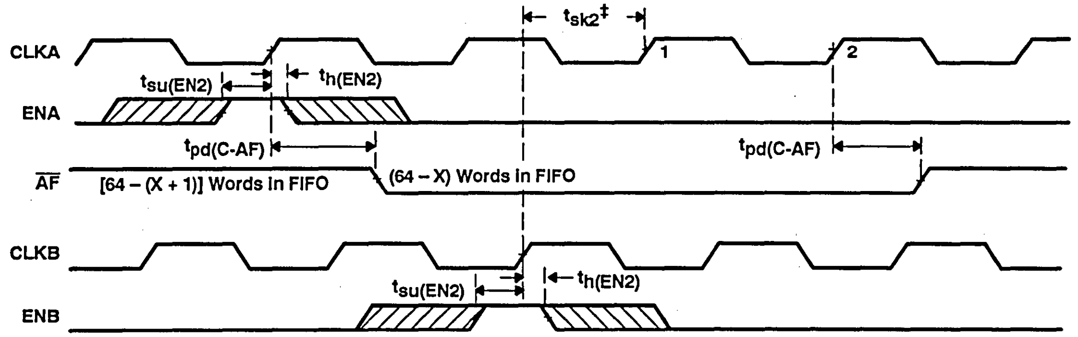
Figure 5. $\overline{FF}$-Flag Timing and First Available Write When the FIFO Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AE}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

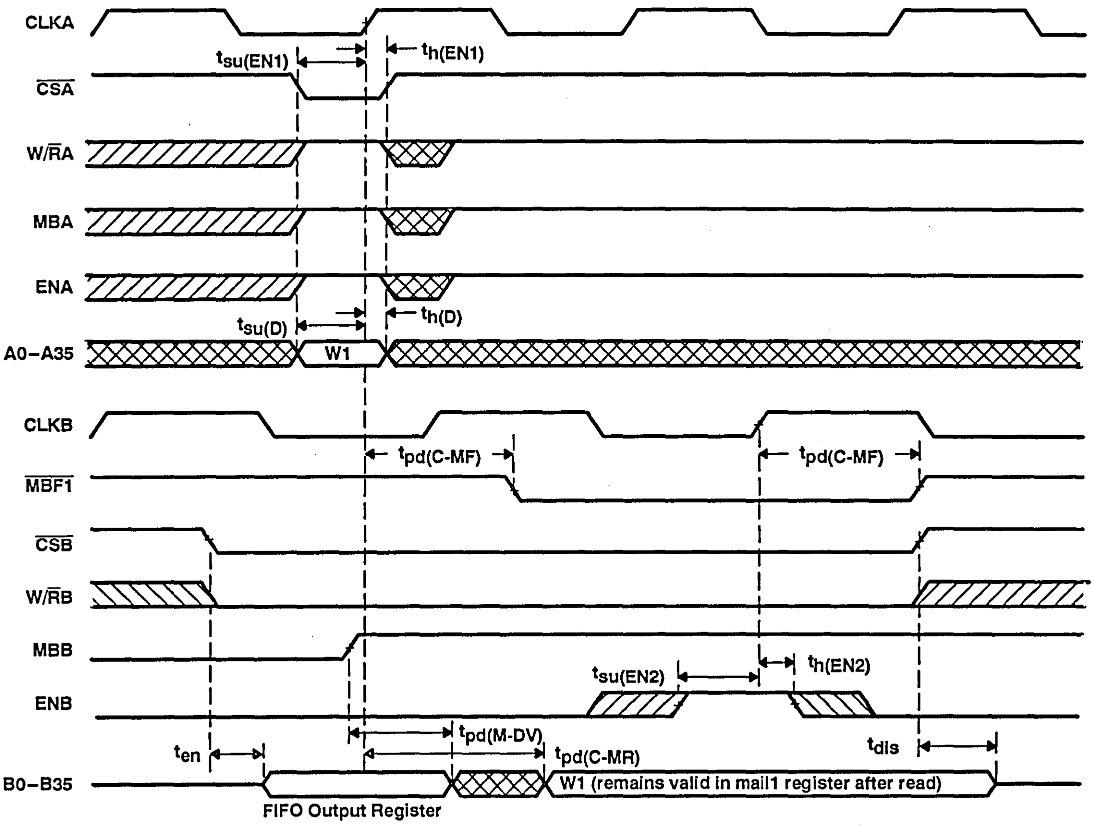
Figure 6. Timing for $\overline{AE}$ When the FIFO Is Almost Empty



‡ t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AF}$ may transition high one CLKB cycle later than shown.

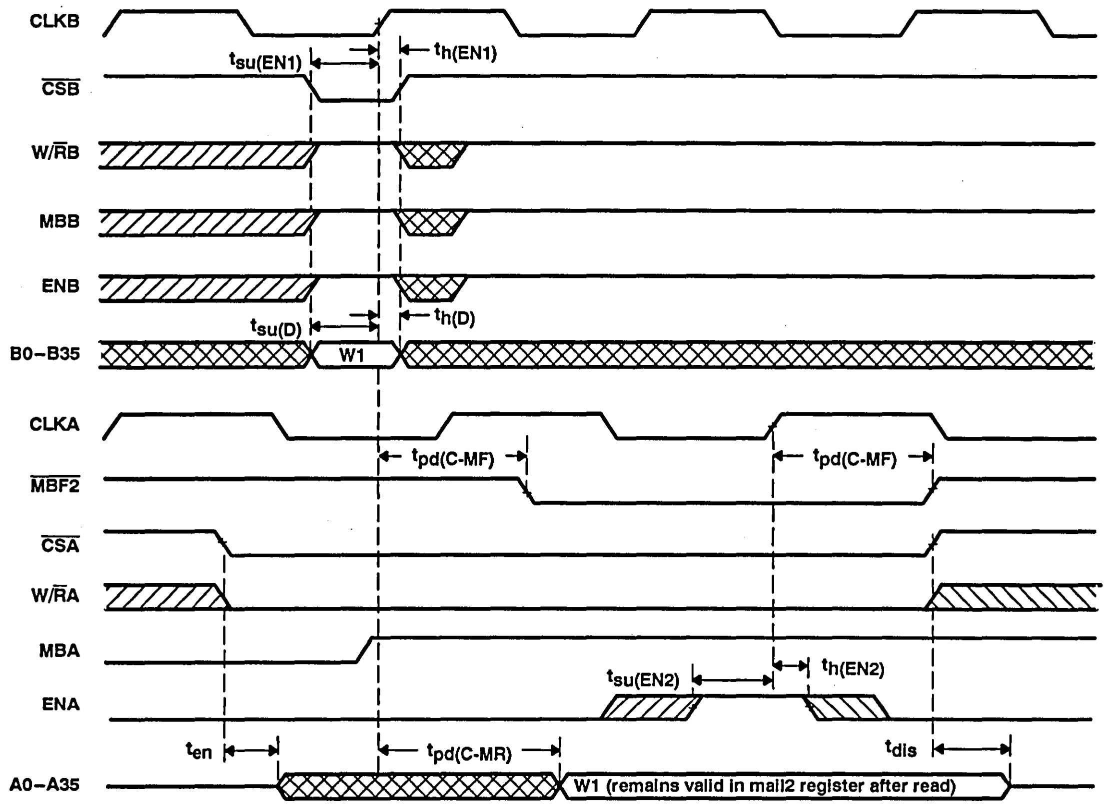
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 7. Timing for $\overline{AF}$ When the FIFO Is Almost Full



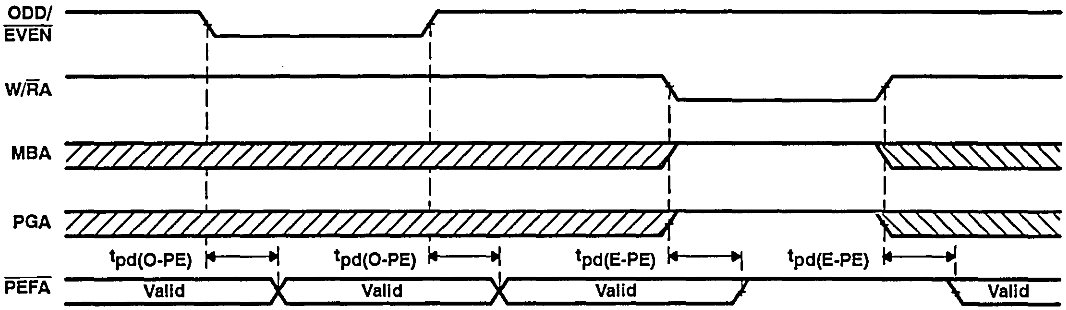
NOTE A: Port-B parity generation off (PGB = L)

Figure 8. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



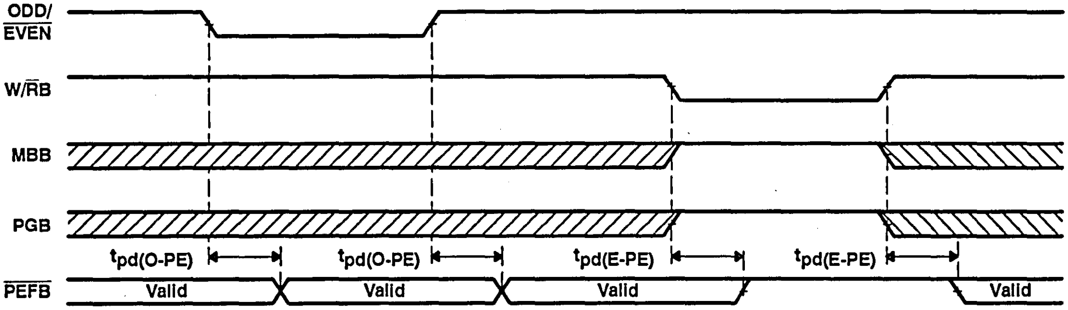
NOTE A: Port-A parity generation off (PGA = L)

Figure 9. Timing for Mail2 Register and $\overline{\mathrm{MBF2}}$ Flag



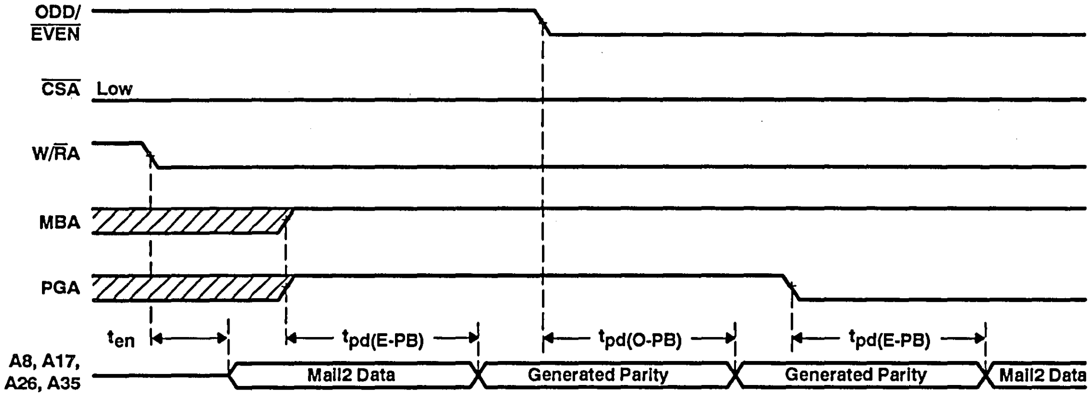
NOTE A: $\overline{CSA}$ = L and ENA = H

Figure 10. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



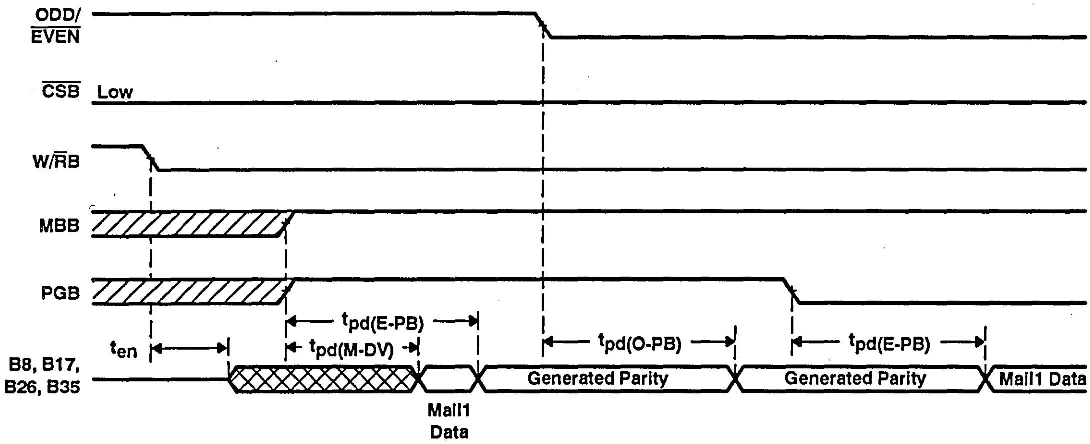
NOTE A: $\overline{CSB}$ = L and ENB = H

Figure 11. ODD/$\overline{EVEN}$, W/$\overline{RB}$, MBB, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA = H

Figure 12. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB = H

Figure 13. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 500 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					± 50	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					± 50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	V_I = V_{CC} or GND	Outputs high			60	mA
				Outputs low			130	
				Outputs disabled			60	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 13)

		'ABT3611-15		'ABT3611-20		'ABT3611-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		MHz
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN1)}$	Setup time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$ before CLKA↑; $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, before CLKB↑	6		6		7		ns
$t_{su(EN2)}$	Setup time, ENA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(EN3)}$	Setup time, MBA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{\text{EVEN}}$ and PGB before CLKB↑[†]	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RST}}$ low before CLKA↑ or CLKB↑[‡]	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{\text{RST}}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN1)}$	Hold time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$ after CLKA↑; $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$ after CLKB↑	1		1		1		ns
$t_{h(EN2)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	1		1		1		ns
$t_{h(EN3)}$	Hold time, MBA after CLKA↑; MBB after CLKB↑	1		1		1		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{\text{EVEN}}$ and PGB after CLKB↑[†]	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{\text{RST}}$ low after CLKA↑ or CLKB↑[‡]	6		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{\text{RST}}$ high	4		4		4		ns
t_{sk1}[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{\text{EFA}}$, $\overline{\text{EFB}}$, $\overline{\text{FFA}}$, and $\overline{\text{FFB}}$	8		8		10		ns
t_{sk2}[§]	Skew time, between CLKA↑ and CLKB↑ for $\overline{\text{AEA}}$, $\overline{\text{AEB}}$, $\overline{\text{AFA}}$, and $\overline{\text{AFB}}$	9		16		20		ns

[†] Only applies for a rising edge of CLKB that does a FIFO read

[‡] Requirement to count the clock edge as one of at least four needed to reset a FIFO

[§] Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 13)

PARAMETER		'ABT3611-15		'ABT3611-20		'ABT3611-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C-FF)}$	Propagation delay time, CLKA↑ to $\overline{FF}$	2	10	2	12	2	15	ns
$t_{pd(C-EF)}$	Propagation delay time, CLKB↑ to $\overline{EF}$	2	10	2	12	2	15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$	2	10	2	12	2	15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$	2	10	2	12	2	15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35[†] and CLKB↑ to A0–A35[‡]	3	12	3	14	3	16	ns
$t_{pd(M-DV)}$	Propagation delay time, MBB to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D-PE)}$	Propagation delay time, A0–A35 valid to $\overline{PEFA}$ valid; B0–B35 valid to $\overline{PEFB}$ valid	3	12	3	13	3	14	ns
$t_{pd(O-PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O-PB)}$[§]	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
$t_{pd(E-PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to $\overline{PEFB}$	1	12	1	13	1	15	ns
$t_{pd(E-PB)}$[§]	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to parity bits (B8, B17, B26, B35)	3	14	3	15	3	16	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ to $\overline{AE}$ low and ($\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$) high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	9	1	10	1	11	ns

[†] Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
[‡] Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
[§] Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

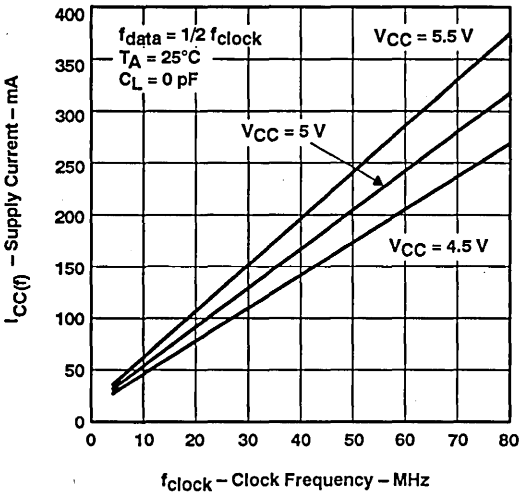


Figure 14

calculating power dissipation

The $I_{CC(f)}$ data for the graph was taken while simultaneously reading and writing the FIFO on the SN74ACT3613 with CLKA and CLKB operating at frequency f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 14, the maximum power dissipation (P_T) of the SN74ABT3613 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum(C_L \times (V_{OH} - V_{OL})^2 \times f_o)$$

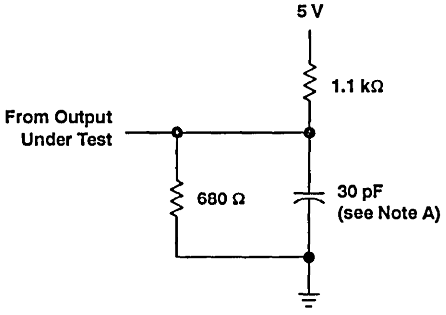
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = output high-level voltage
V_{OL} = outut low-level voltage

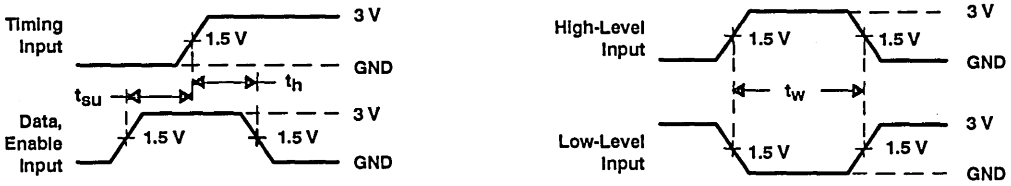
When no reads or writes are occurring on the SN74ABT3613, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.290 \text{ mA/MHz}$$

PARAMETER MEASUREMENT INFORMATION

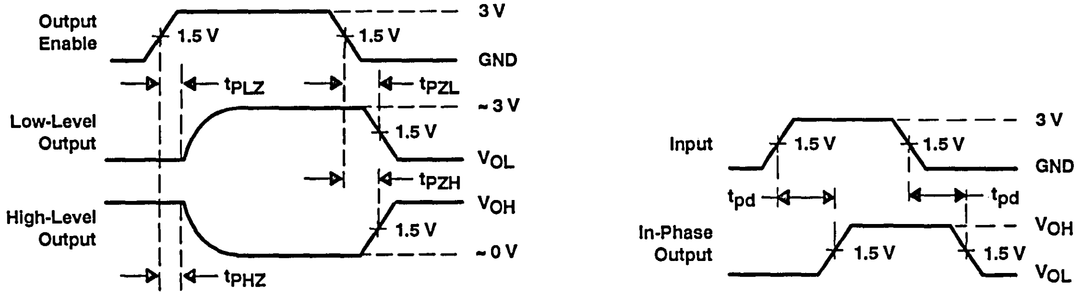


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 15. Load Circuit and Voltage Waveforms

SN74ABT3612
64 × 36 × 2 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCBS129D – JULY 1992 – REVISED JANUARY 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)**

description

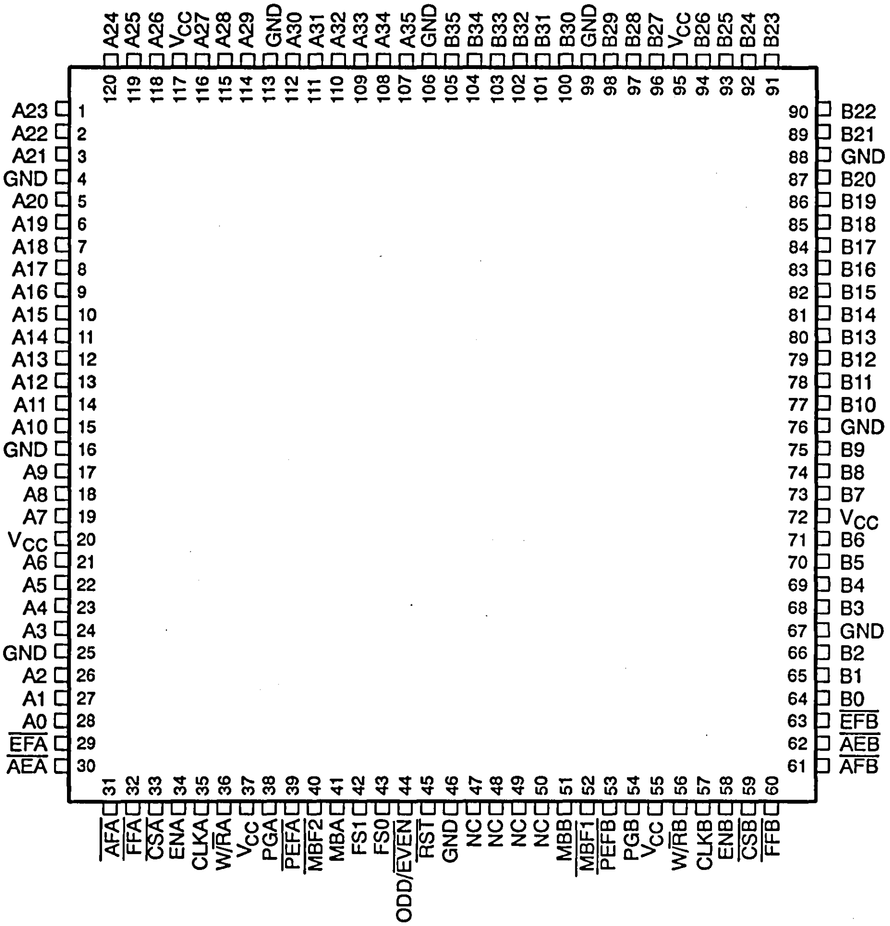
The SN74ABT3612 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. Two independent 64 x 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost-full and almost-empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

The SN74ABT3612 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{\text{FFA}}$, $\overline{\text{FFB}}$) and almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag ($\overline{\text{EFA}}$, $\overline{\text{EFB}}$) and almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

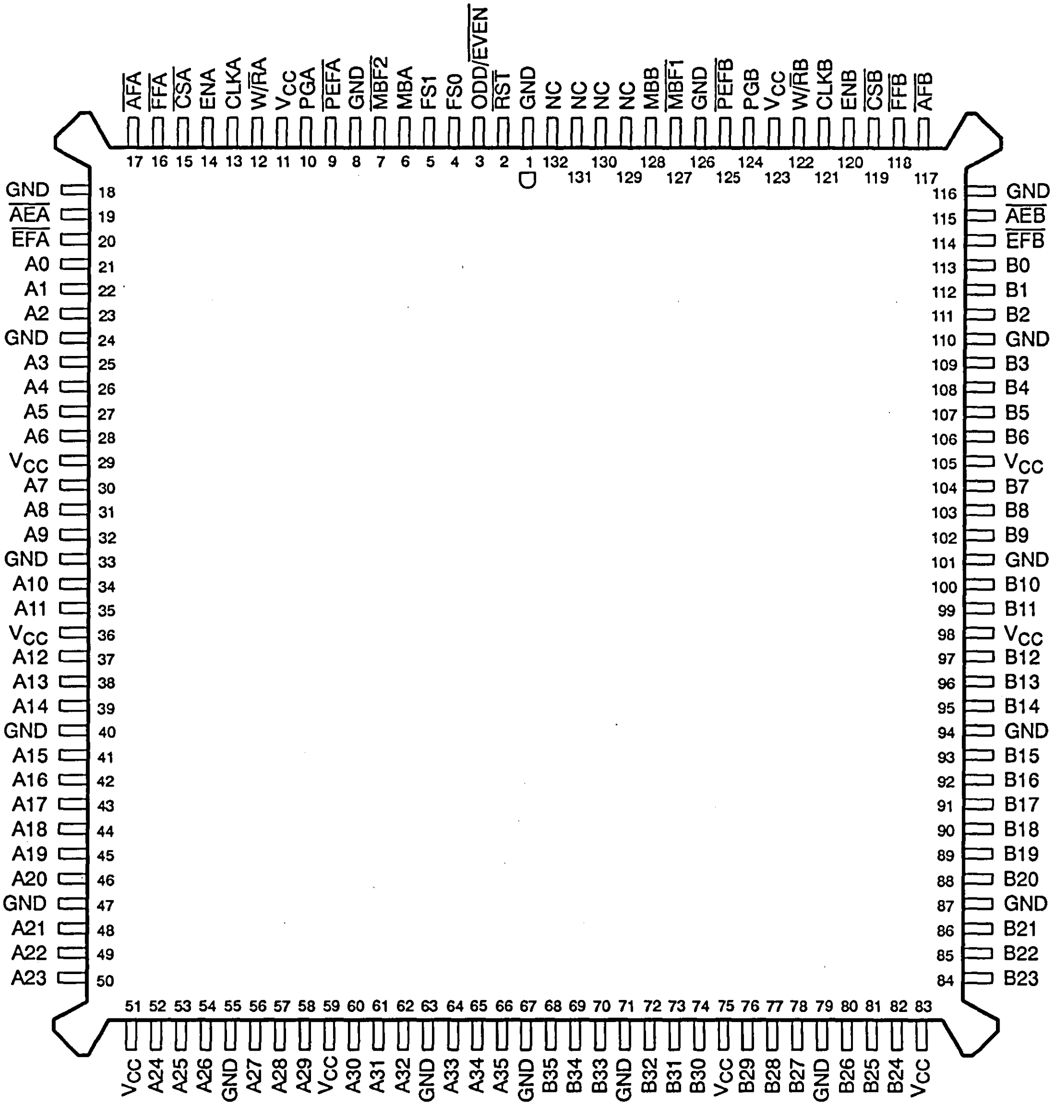
The SN74ABT3612 is characterized for operation from 0°C to 70°C.

PCB PACKAGE
(TOP VIEW)



NC – No internal connection

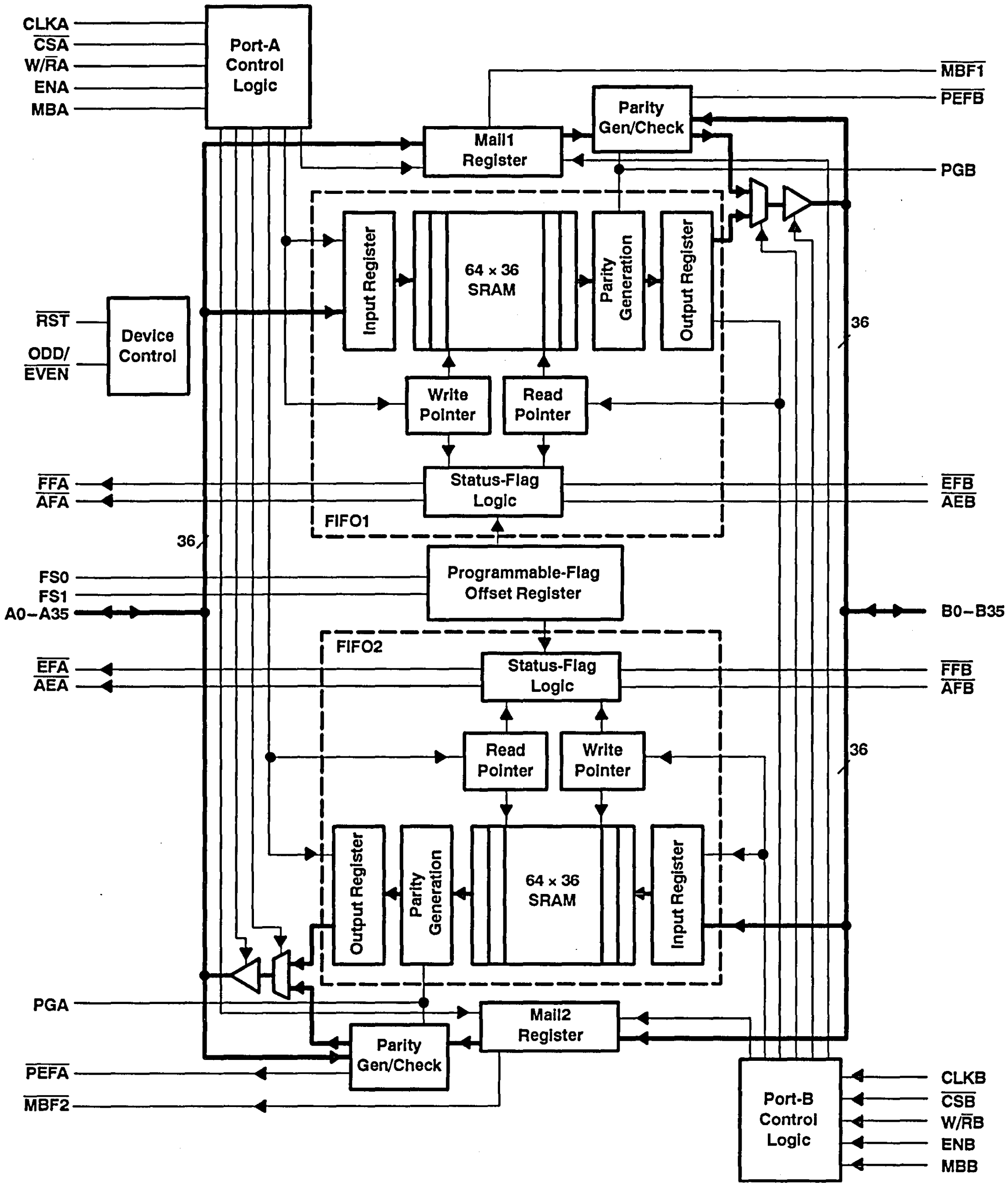
PQ PACKAGE†
(TOP VIEW)



NC – No internal connection

† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AEA}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{AEA}$ is low when the number of words in FIFO2 is less than or equal to the value in the offset register, X.
$\overline{AEB}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{AEB}$ is low when the number of words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{AFA}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFB}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{AFB}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EFA}$	O (port A)	Port-A empty flag. $\overline{EFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{EFA}$ is low, FIFO2 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is high. $\overline{EFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	O (port B)	Port-B empty flag. $\overline{EFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EFB}$ is low, FIFO1 is empty and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is high. $\overline{EFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FFA}$	O (port A)	Port-A full flag. $\overline{FFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FFA}$ is low, FIFO1 is full and writes to its memory are disabled. $\overline{FFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
$\overline{FFB}$	O (port B)	Port-B full flag. $\overline{FFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{FFB}$ is low, FIFO2 is full and writes to its memory are disabled. $\overline{FFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and almost-full flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when the device is reset.

Terminal Functions (continued)

PIN NAME	I/O	DESCRIPTION
MBF2	O	Mail2 register flag. MBF2 is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while MBF2 is low. MBF2 is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. MBF2 is set high when the device is reset.
ODD/ EVEN	I	Odd/even parity select. Odd parity is checked on each port when ODD/EVEN is high, and even parity is checked when ODD/EVEN is low. ODD/EVEN also selects the type of parity generated for each port if parity generation is enabled for a read operation.
PEFA	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, PEFA is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/EVEN input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/RA low, MBA high, and PGA high, the PEFA flag is forced high regardless of the state of the A0–A35 inputs.
PEFB	O (port B)	Port-B parity error flag. When any byte applied to terminals B0–B35 fails parity, PEFB is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/EVEN input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/RB low, MBB high, and PGB high, the PEFB flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
RST	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while RST is low. This sets the AFA, AFB, MBF1, and MBF2 flags high and the EFA, EFB, AEA, AEB, FFA, and FFB flags low. The low-to-high transition of RST latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
W/RA	I	Port-A write/read select. W/RA high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/RA is high.
W/RB	I	Port-B write/read select. W/RB high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/RB is high.

detailed description

reset

The SN74ABT3612 is reset by taking the reset (RST) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags (FFA, FFB) low, the empty flags (EFA, EFB) low, the almost-empty flags (AEA, AEB) low, and the almost-full flags (AFA, AFB) high. A reset also forces the mailbox flags (MBF1, MBF2) high. After a reset, FFA is set high after two low-to-high transitions of CLKA and FFB is set high after two low-to-high transitions of CLKB. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the RST input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

reset (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{\text{RST}}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{\text{CSA}}$) and the port-A write/read select (W/$\overline{\text{R}}$A). The A0–A35 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{R}}$A is high. The A0–A35 outputs are active when both $\overline{\text{CSA}}$ and W/$\overline{\text{R}}$A are low. Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is high, ENA is high, MBA is low, and $\overline{\text{FFA}}$ is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is low, ENA is high, MBA is low, and $\overline{\text{EFA}}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{\text{CSA}}$	W/$\overline{\text{R}}$A	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{\text{MBF2}}$ high)

The port-B control signals are identical to those of port A. The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{\text{CSB}}$) and the port-B write/read select (W/$\overline{\text{R}}$B). The B0–B35 outputs are in the high-impedance state when either $\overline{\text{CSB}}$ or W/$\overline{\text{R}}$B is high. The B0–B35 outputs are active when both $\overline{\text{CSB}}$ and W/$\overline{\text{R}}$B are low.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is high, ENB is high, MBB is low, and $\overline{\text{FFB}}$ is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is low, ENB is high, MBB is high, and $\overline{\text{EFB}}$ is high (see Table 3).

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) and write/read selects (W/$\overline{\text{R}}$A, W/$\overline{\text{R}}$B) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select may change states during the setup and hold time window of the cycle.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{\text{CSB}}$	W/$\overline{\text{RB}}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO2 write
L	H	H	H	↑	In high-impedance state	Mail2 write
L	L	L	L	X	Active, FIFO1 output register	None
L	L	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	L	L	H	X	Active, mail1 register	None
L	L	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{\text{MBF1}}$ high)

synchronized FIFO flags

Each FIFO is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{\text{EFA}}$, $\overline{\text{AEA}}$, $\overline{\text{FFA}}$, and $\overline{\text{AFA}}$ are synchronized to CLKA. $\overline{\text{EFB}}$, $\overline{\text{AEB}}$, $\overline{\text{FFB}}$, and $\overline{\text{AFB}}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1†	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{\text{EFB}}$	$\overline{\text{AEB}}$	$\overline{\text{AFA}}$	$\overline{\text{FFA}}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2†	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	$\overline{\text{EFA}}$	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	$\overline{\text{FFB}}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flags ($\overline{\mathrm{EFA}}$, $\overline{\mathrm{EFB}}$)

The empty flag of a FIFO is synchronized to the port clock that reads data from its array. When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 6 and 7).

full flags ($\overline{\mathrm{FFA}}$, $\overline{\mathrm{FFB}}$)

The full flag of a FIFO is synchronized to the port clock that writes data to its array. When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls the full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock; therefore, a full flag is low if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the full flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 8 and 9).

almost-empty flags ($\overline{\mathrm{AEA}}$, $\overline{\mathrm{AEB}}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset). An almost-empty flag is low when the FIFO contains X or less words in memory and is high when the FIFO contains (X + 1) or more words.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset). An almost-full flag is low when the FIFO contains (64 – X) or more words in memory and is high when the FIFO contains [64 – (X + 1)] or less words.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for the almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of words in memory to [64 – (X + 1)]. An almost-full flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO read that reduces the number of words in memory to [64 – (X + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [64 – (X + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, and ENB and MBB is high. Writing data to a mail register sets the corresponding flag ($\overline{\text{MBF1}}$ or $\overline{\text{MBF2}}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When a port's data outputs are active, the data on the bus comes from the FIFO output register when the port mailbox-select input (MBA, MBB) is low and from the mail register when the port mailbox-select input is high. The mail1 register flag ($\overline{\text{MBF1}}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$, and ENB and MBB is high. The mail2 register flag ($\overline{\text{MBF2}}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA and MBA is high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

parity checking

The port-A inputs (A0–A35) and port-B inputs (B0–B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a low level on the port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\text{EVEN}}$) select input. A parity error on one or more bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. When odd/even parity is selected, a port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) is low if any byte on the port has an odd/even number of low levels applied to the bits.

parity checking (continued)

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with W/$\overline{RA}$ low, $\overline{CSA}$ low, ENA high, MBA high, and PGA high, the port-A parity error flag ($\overline{PEFA}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with W/$\overline{RB}$ low, $\overline{CSB}$ low, ENB high, MBB high, and PGB high, the port-B parity error flag ($\overline{PEFB}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3612 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port write/read select (W/$\overline{RA}$, W/$\overline{RB}$) input is low, the port mail select (MBA, MBB) input is high, chip select ($\overline{CSA}$, $\overline{CSB}$) is low, enable (ENA, ENB) is high, and port parity generate select (PGA, PGB) is high. Generating parity for mail register data does not change the contents of the register.

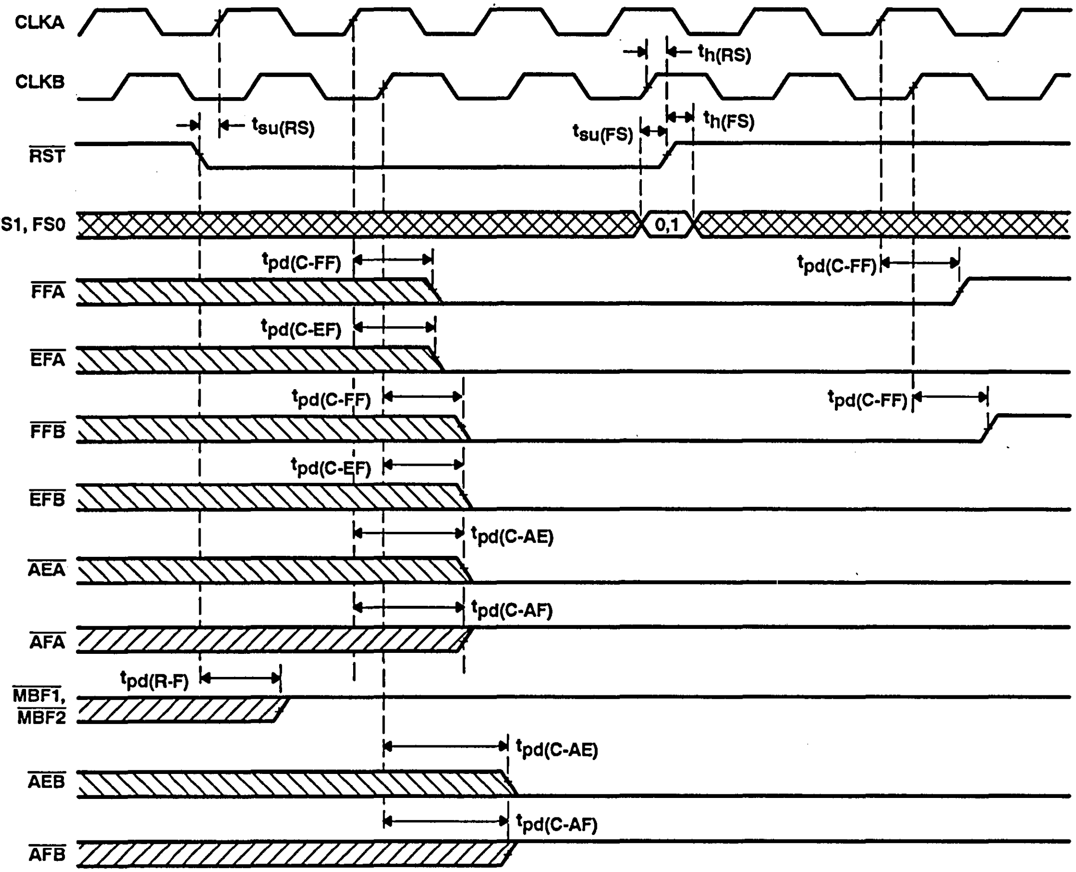
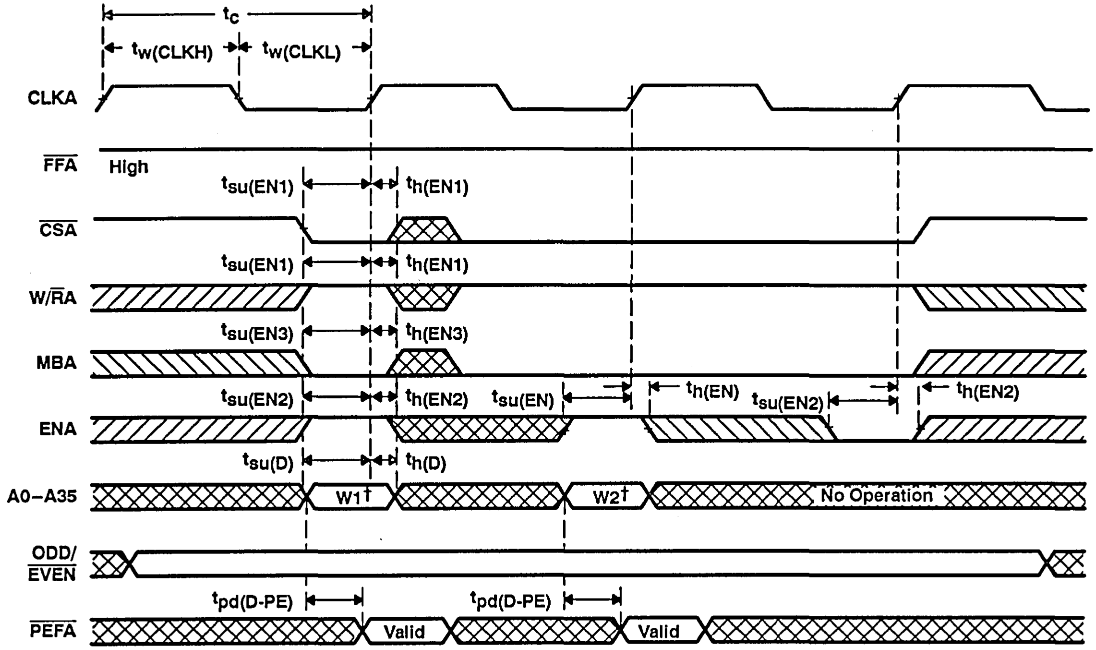
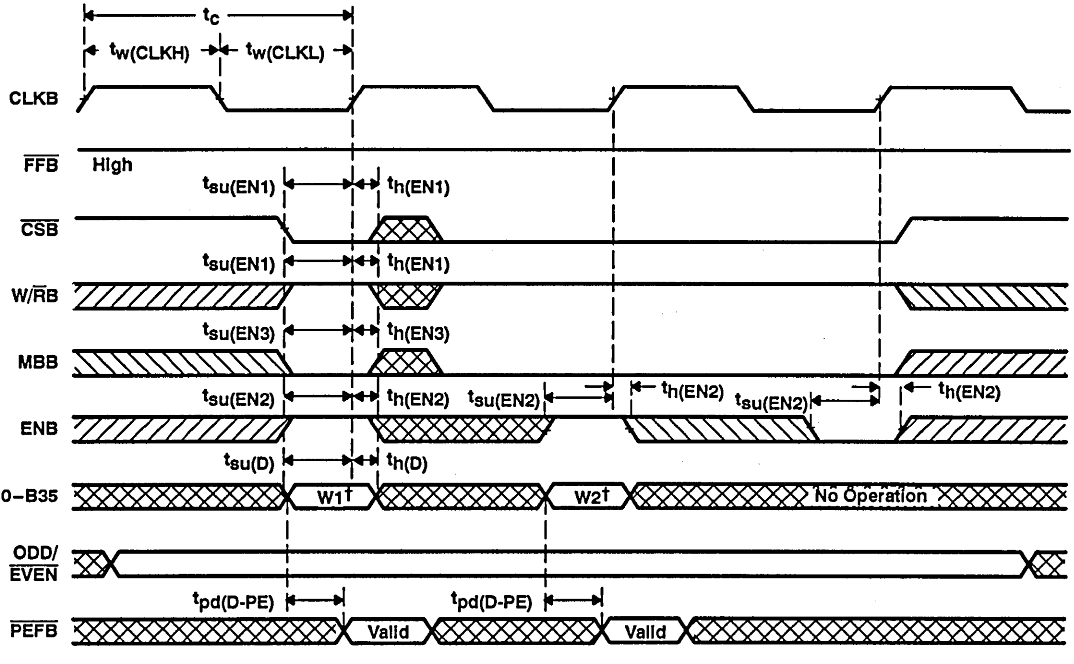


Figure 1. Device Reset Loading the X Register With the Value of Eight



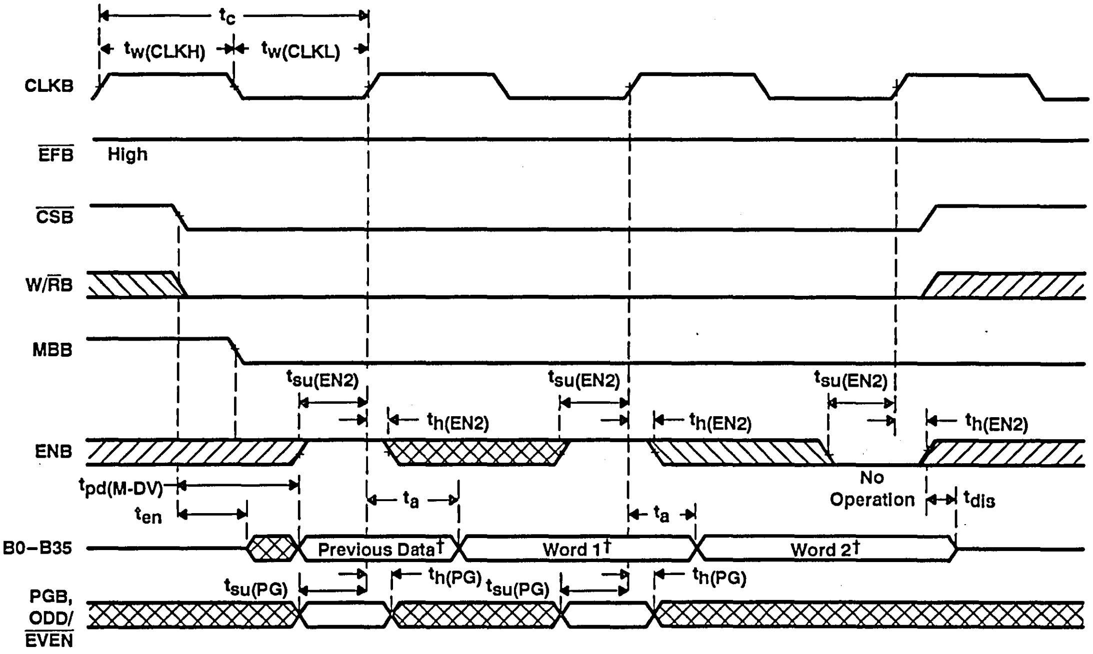
† Written to FIFO1

Figure 2. Port-A Write Cycle Timing for FIFO1



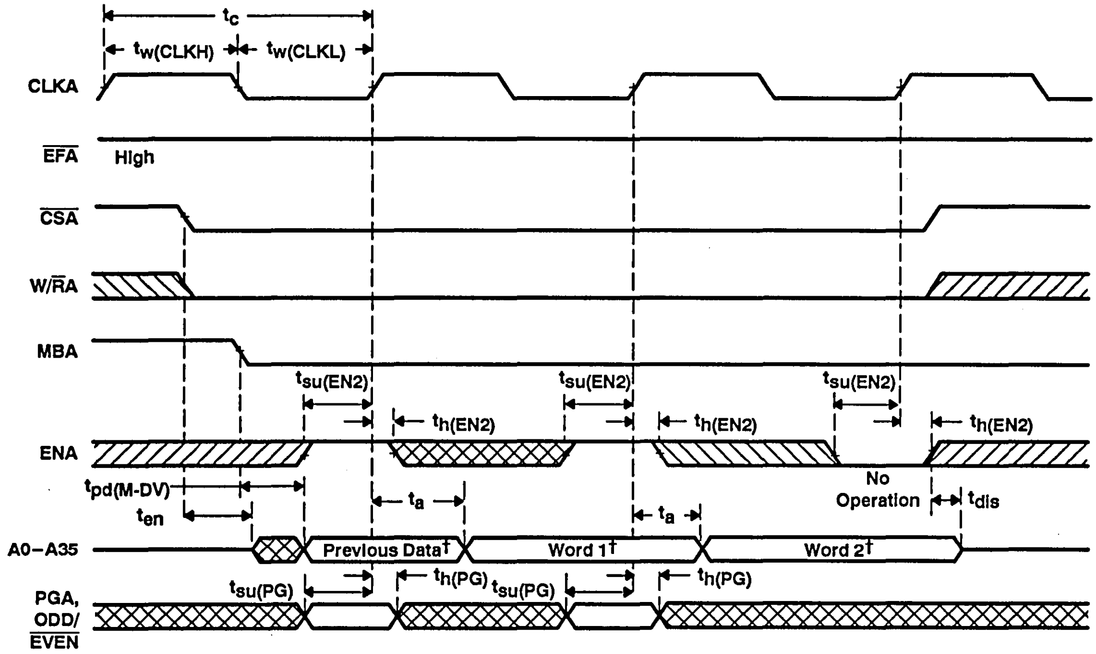
† Written to FIFO2

Figure 3. Port-B Write Cycle Timing for FIFO2



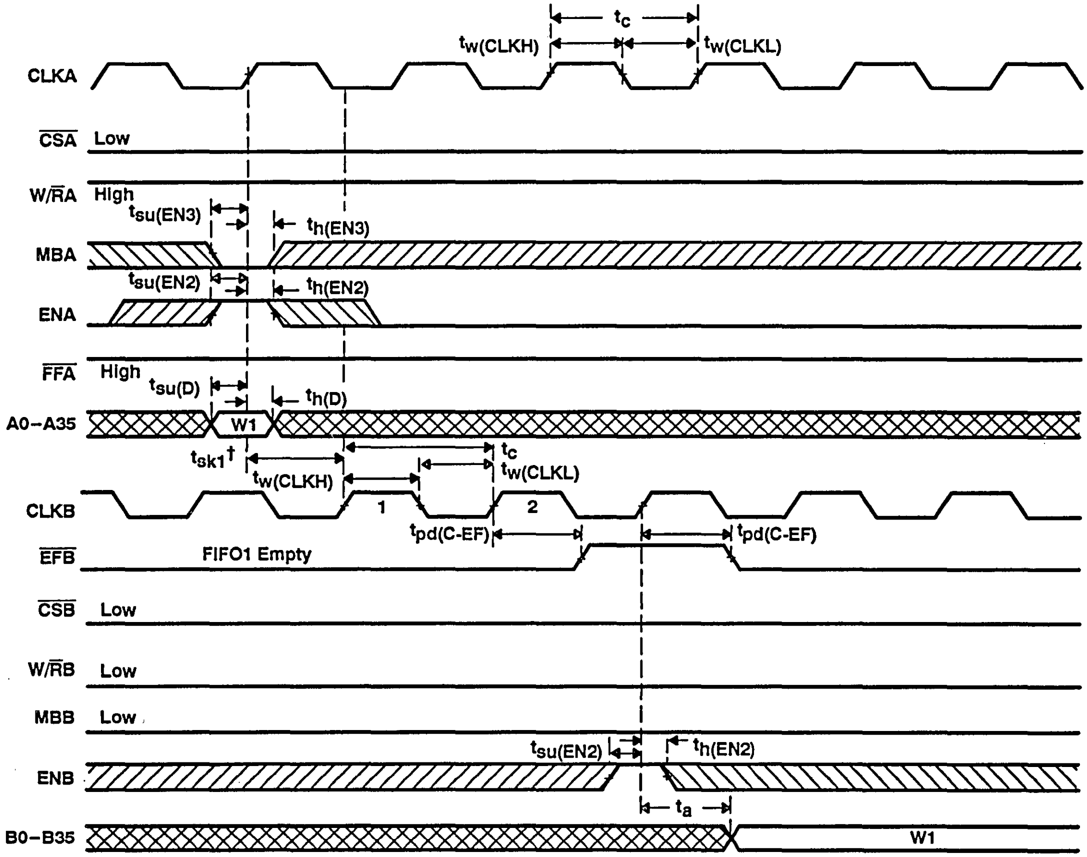
† Read from FIFO1

Figure 4. Port-B Read Cycle Timing for FIFO1



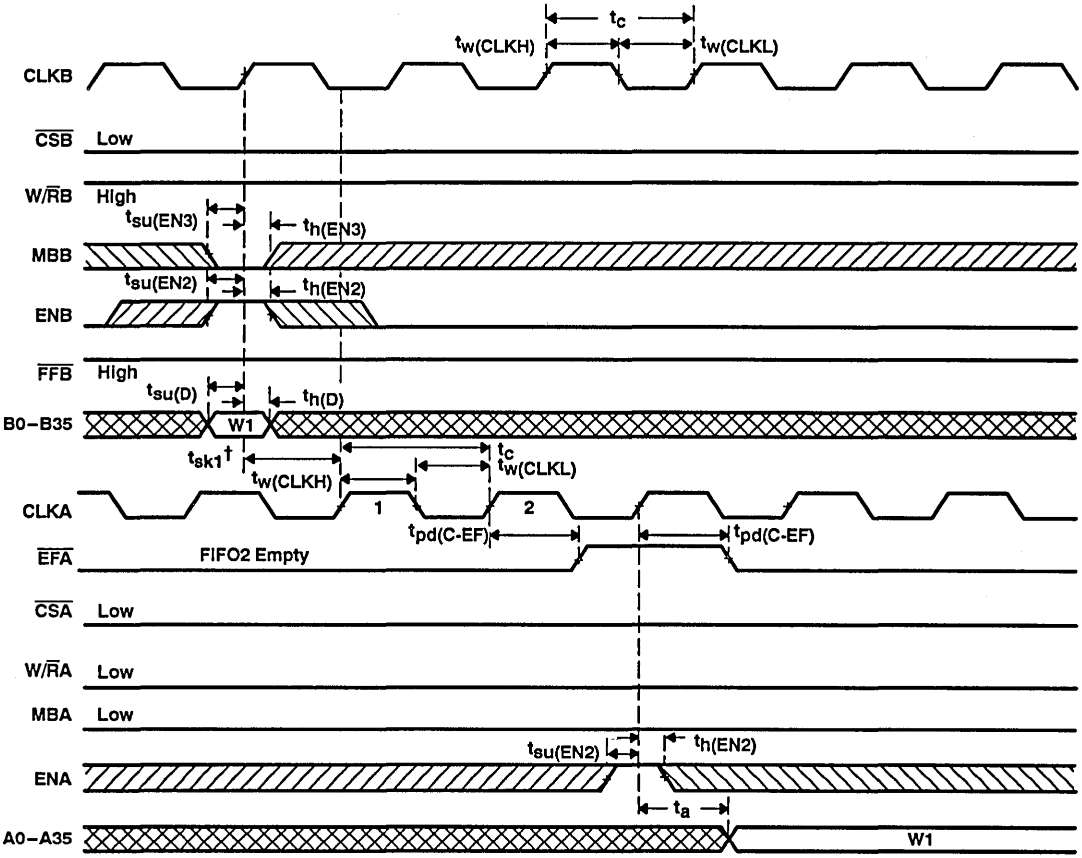
† Read from FIFO2

Figure 5. Port-A Read Cycle Timing for FIFO2



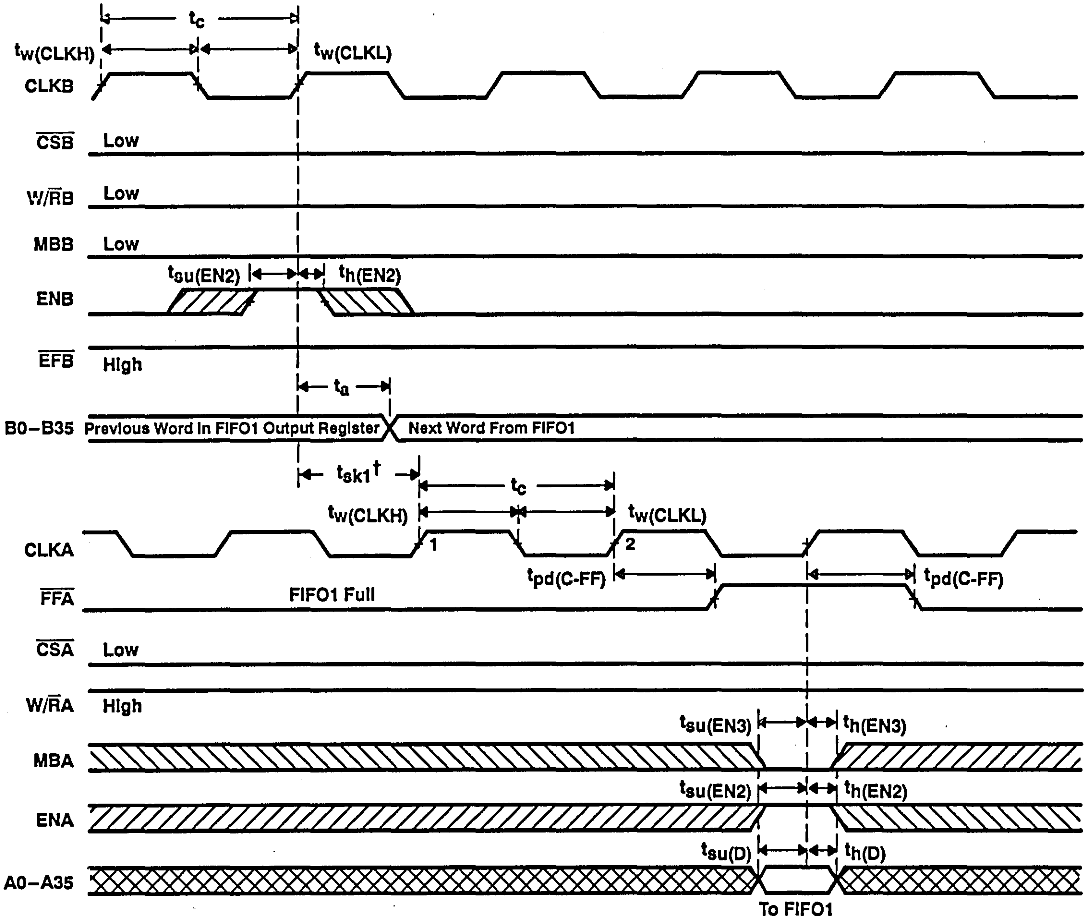
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of $\overline{EFB}$ high may occur one CLKB cycle later than shown.

Figure 6. $\overline{EFB}$-Flag Timing and First Data Read When FIFO1 Is Empty



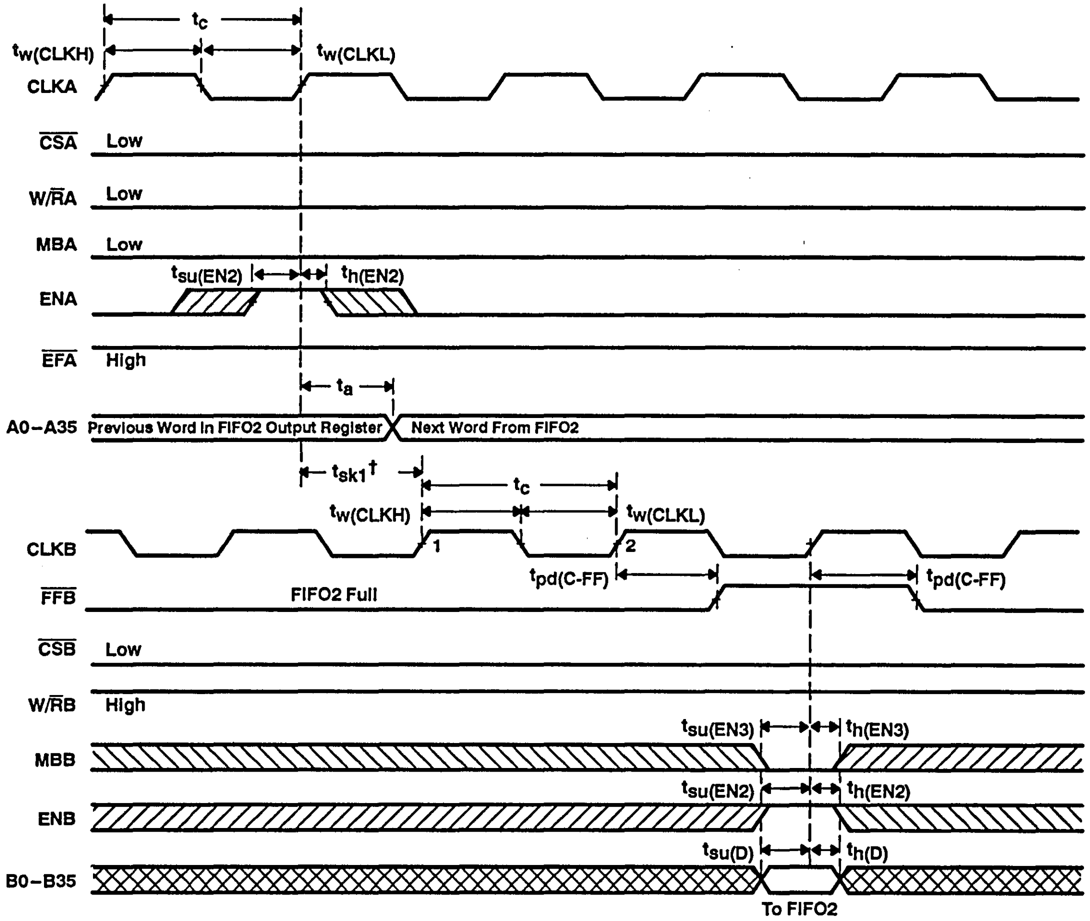
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then the transition of $\overline{EFA}$ high may occur one CLKA cycle later than shown.

Figure 7. $\overline{EFA}$-Flag Timing and First Data Read When FIFO2 Is Empty



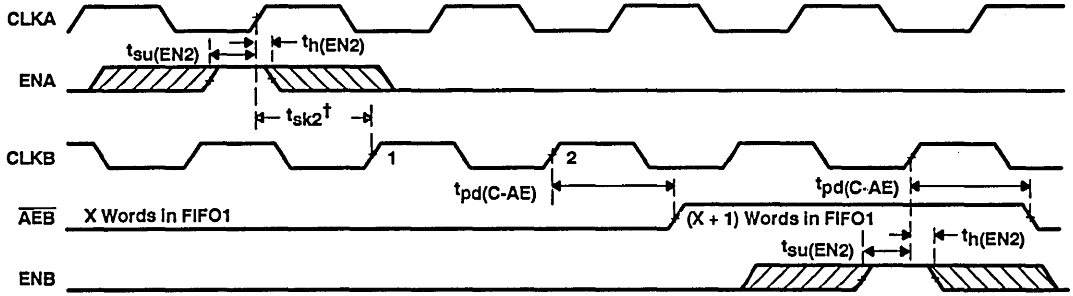
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, then $\overline{FFA}$ may transition high one CLKA cycle later than shown.

Figure 8. $\overline{FFA}$-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then $\overline{FFB}$ may transition high one CLKB cycle later than shown.

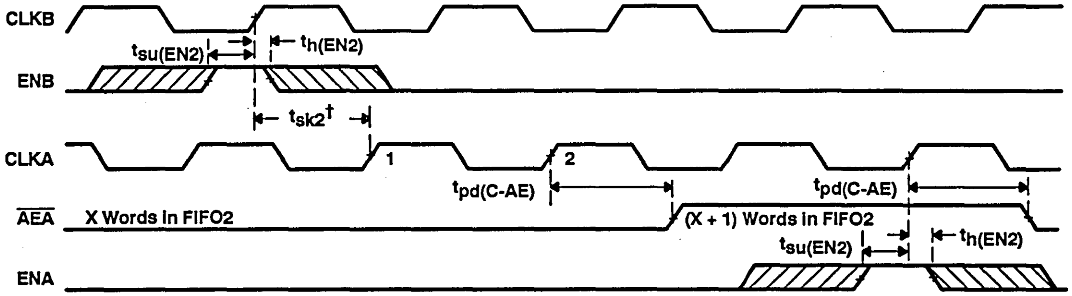
Figure 9. $\overline{FFB}$-Flag Timing and First Available Write When FIFO2 Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

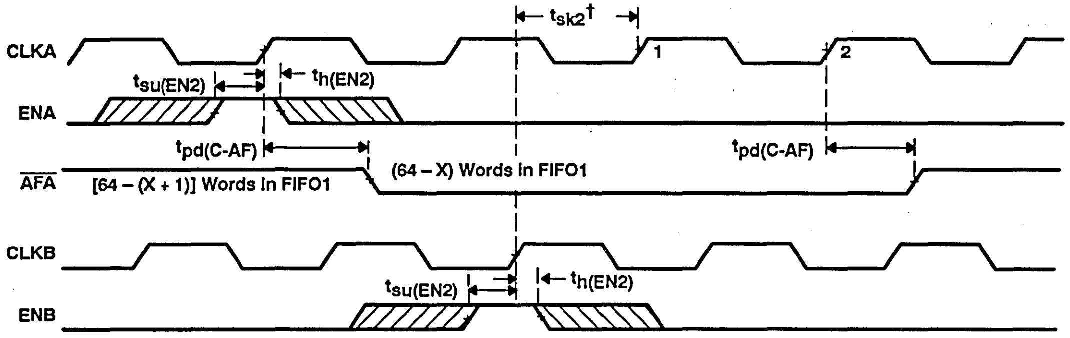
Figure 10. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

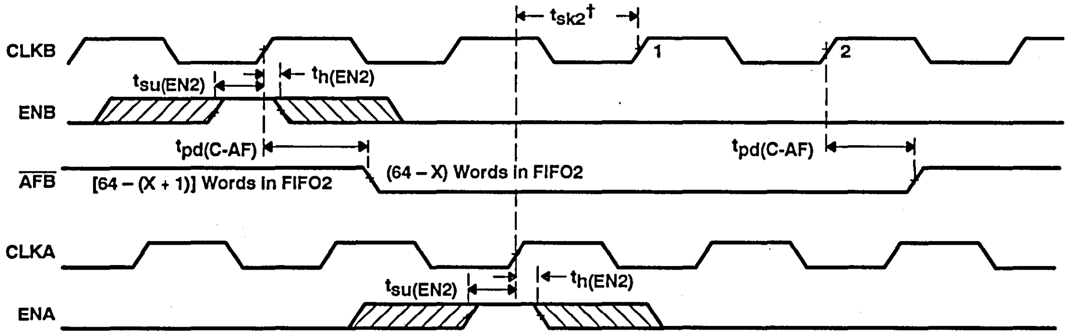
Figure 11. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

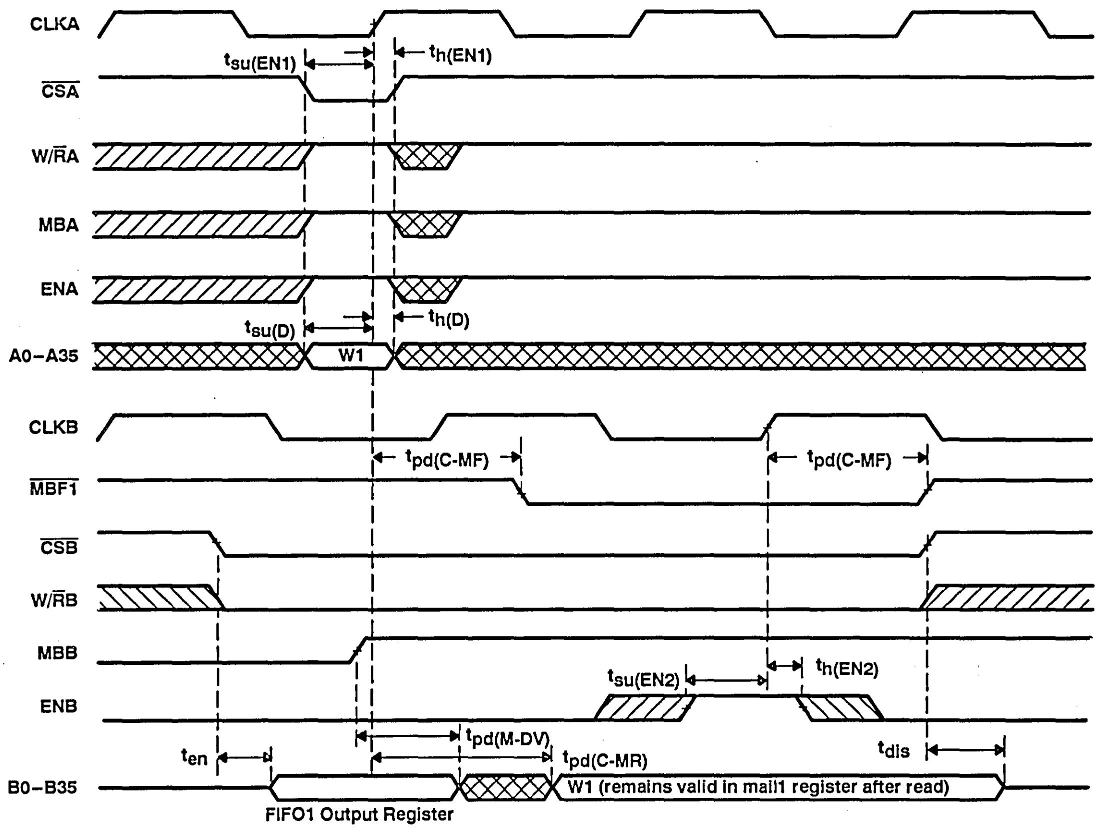
Figure 12. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.

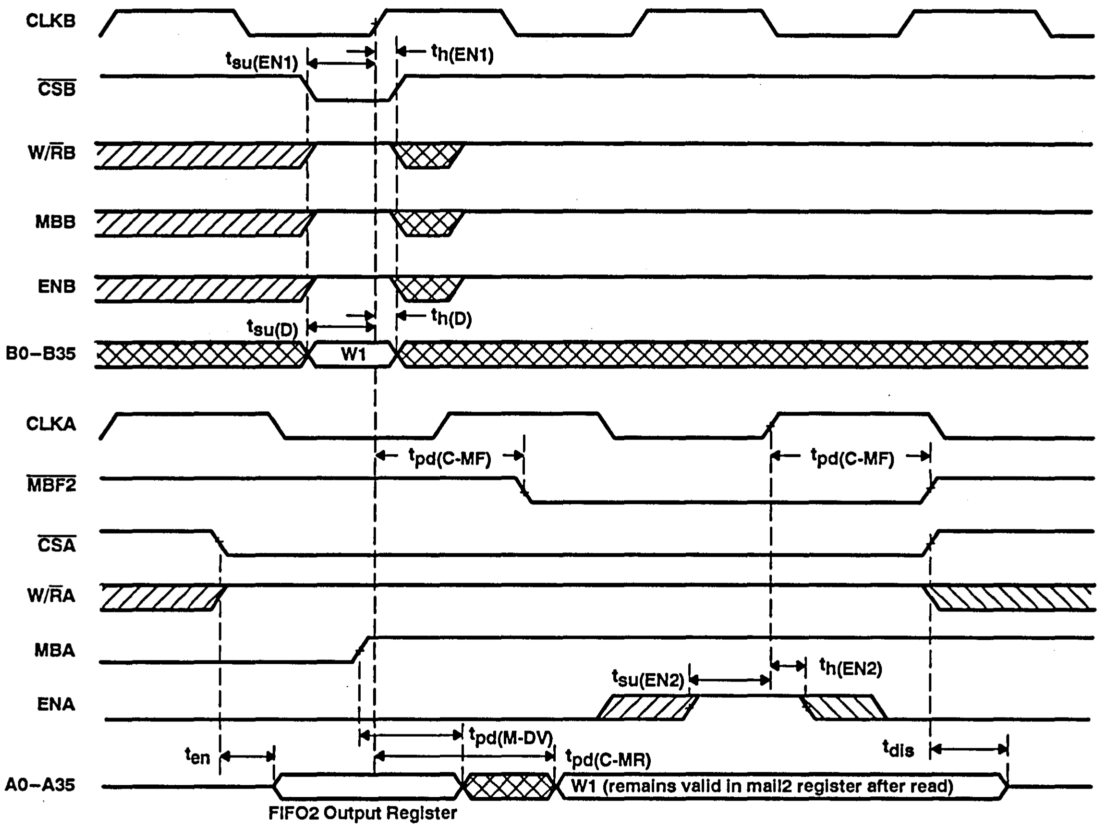
NOTE A: FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$= H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

Figure 13. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full



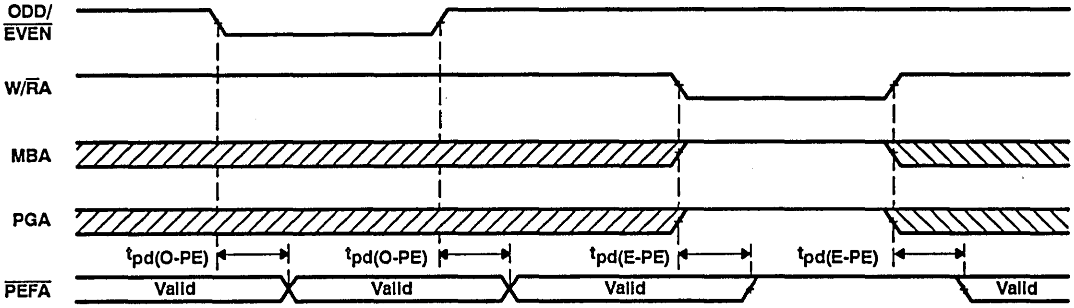
NOTE A: Port-B parity generation off (PGB = L)

Figure 14. Timing for Mail1 Register and $\overline{MBF1}$ Flag



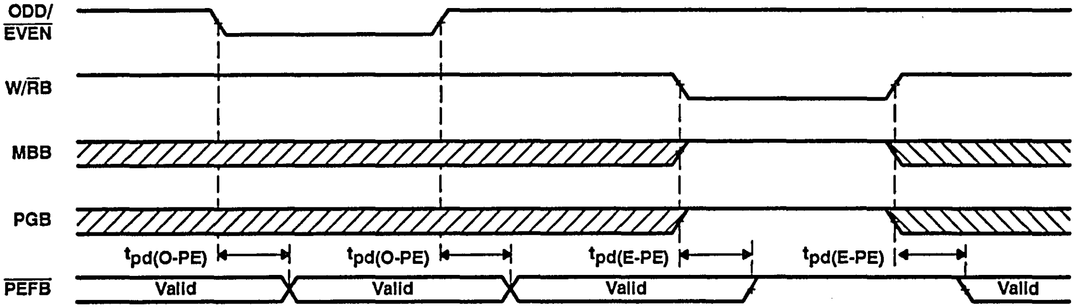
NOTE A: Port-A parity generation off (PGA = L)

Figure 15. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag



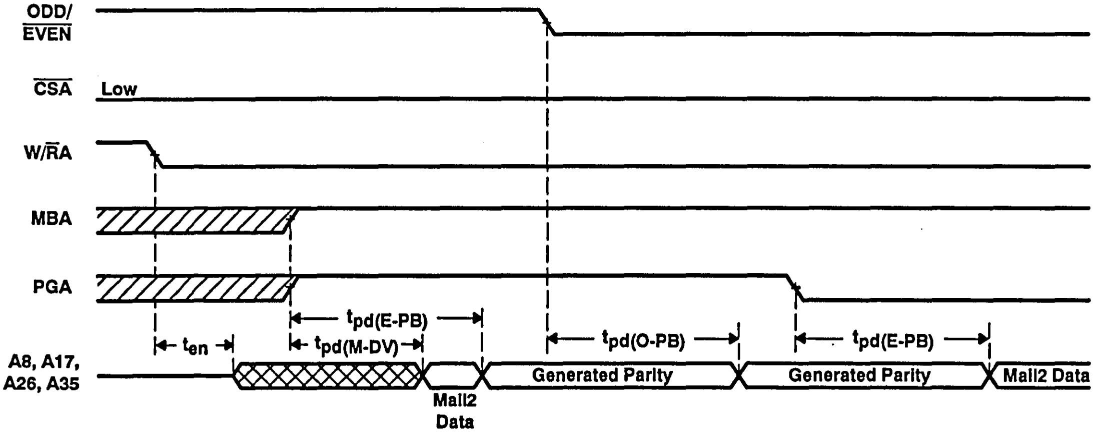
NOTE A: ENA is high and $\overline{\text{CSA}}$ is low.

Figure 16. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RA}}$, MBA, and PGA to $\overline{\text{PEFA}}$ Timing



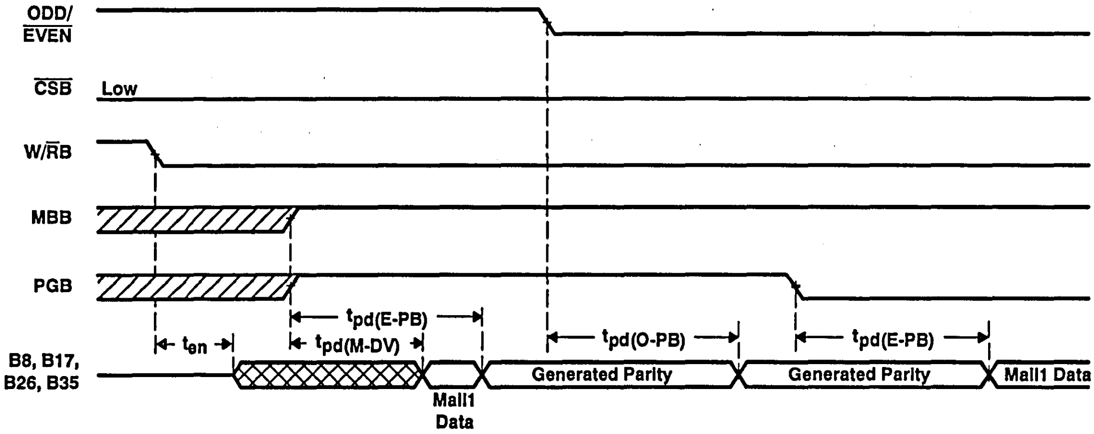
NOTE A: ENB is high and $\overline{\text{CSB}}$ is low.

Figure 17. ODD/$\overline{\text{EVEN}}$, W/$\overline{\text{RB}}$, MBB, and PGB to $\overline{\text{PEFB}}$ Timing



NOTE A: ENA is high.

Figure 18. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB is high.

Figure 19. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±500 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±50	μA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±50	μA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	V_I = V_{CC} or GND	Outputs high			60	mA
				Outputs low			130	mA
				Outputs disabled			60	mA
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 19)

		'ABT3612-15		'ABT3612-20		'ABT3612-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN1)}$	Setup time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$ before CLKA↑; $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$ before CLKB↑	6		6		7		ns
$t_{su(EN2)}$	Setup time, ENA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(EN3)}$	Setup time, MBA before CLKA↑; MBB before CLKB↑	4		5		6		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{\text{EVEN}}$ and PGA before CLKA↑; ODD/$\overline{\text{EVEN}}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{\text{RST}}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{\text{RST}}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	2.5		2.5		2.5		ns
$t_{h(EN1)}$	Hold time, $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$ after CLKA↑; $\overline{\text{CSB}}$, W/$\overline{\text{RB}}$ after CLKB↑	2		2		2		ns
$t_{h(EN2)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	2.5		2.5		2.5		ns
$t_{h(EN3)}$	Hold time, MBA after CLKA↑; MBB after CLKB↑	1		1		1		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{\text{EVEN}}$ and PGA after CLKA↑; ODD/$\overline{\text{EVEN}}$ and PGB after CLKB↑†	1		1		1		ns
$t_{h(RS)}$	Hold time, $\overline{\text{RST}}$ low after CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{\text{RST}}$ high	4		4		4		ns
t_{sk1}§	Skew time, between CLKA↑ and CLKB↑ for $\overline{\text{EFA}}$, $\overline{\text{EFB}}$, $\overline{\text{FFA}}$, and $\overline{\text{FFB}}$	8		8		10		ns
t_{sk2}§	Skew time, between CLKA↑ and CLKB↑ for $\overline{\text{AEA}}$, $\overline{\text{AEB}}$, $\overline{\text{AFA}}$, and $\overline{\text{AFB}}$	9		16		20		ns

† Only applies for a clock edge that does a FIFO read

‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO

§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 19)

PARAMETER		'ABT3612-15		'ABT3612-20		'ABT3612-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C\text{-}FF)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{FFA}}$ and CLKB↑ to $\overline{\mathrm{FFB}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}EF)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{EFA}}$ and CLKB↑ to $\overline{\mathrm{EFB}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{AEA}}$ and CLKB↑ to $\overline{\mathrm{AEB}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{AFA}}$ and CLKB↑ to $\overline{\mathrm{AFB}}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{\mathrm{MBF1}}$ low or $\overline{\mathrm{MBF2}}$ high and CLKB↑ to $\overline{\mathrm{MBF2}}$ low or $\overline{\mathrm{MBF1}}$ high	1	9	1	12	1	15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35[†] and CLKB↑ to A0–A35[‡]	3	11	3	13	3	15	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D\text{-}PE)}$	Propagation delay time, A0-A35 valid to $\overline{\mathrm{PEFA}}$ valid; B0-B35 valid to $\overline{\mathrm{PEFB}}$ valid	3	10	3	11	3	13	ns
$t_{pd(O\text{-}PE)}$	Propagation delay time, ODD/$\overline{\mathrm{EVEN}}$ to $\overline{\mathrm{PEFA}}$ and $\overline{\mathrm{PEFB}}$	3	11	3	12	3	14	ns
$t_{pd(O\text{-}PB)}$[§]	Propagation delay time, ODD/$\overline{\mathrm{EVEN}}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
$t_{pd(E\text{-}PE)}$	Propagation delay time, W/$\overline{\mathrm{RA}}$, $\overline{\mathrm{CSA}}$, ENA, MBA, or PGA to $\overline{\mathrm{PEFA}}$; W/$\overline{\mathrm{RB}}$, $\overline{\mathrm{CSB}}$, ENB, MBB, or PGB to $\overline{\mathrm{PEFB}}$	1	11	1	12	1	14	ns
$t_{pd(E\text{-}PB)}$[§]	Propagation delay time, W/$\overline{\mathrm{RA}}$, $\overline{\mathrm{CSA}}$, ENA, MBA, or PGA to parity bits (A8, A17, A26, A35); W/$\overline{\mathrm{RB}}$, $\overline{\mathrm{CSB}}$, ENB, MBB, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\mathrm{RST}}$ to ($\overline{\mathrm{AEA}}$, $\overline{\mathrm{AEB}}$) low and ($\overline{\mathrm{AFA}}$, $\overline{\mathrm{AFB}}$, $\overline{\mathrm{MBF1}}$, $\overline{\mathrm{MBF2}}$) high.	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{\mathrm{CSA}}$ and W/$\overline{\mathrm{RA}}$ low to A0–A35 active and $\overline{\mathrm{CSB}}$ low and $\overline{\mathrm{W}}$/RB high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{\mathrm{CSA}}$ or W/$\overline{\mathrm{RA}}$ high to A0–A35 at high impedance and $\overline{\mathrm{CSB}}$ high or $\overline{\mathrm{W}}$/RB low to B0–B35 at high impedance	1	8	1	9	1	11	ns

[†] Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
[‡] Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
[§] Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs CLOCK FREQUENCY

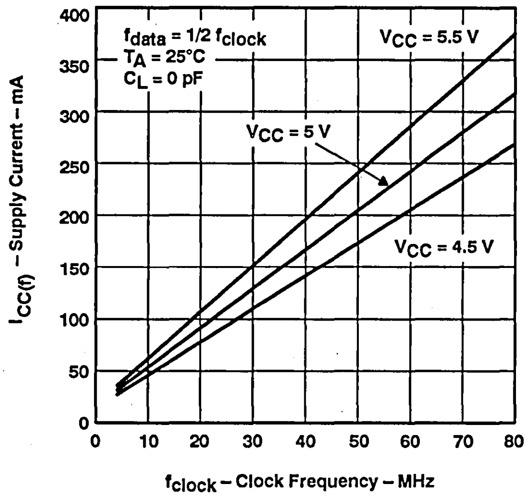


Figure 20

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 20 was taken while simultaneously reading and writing the FIFO on the SN74ACT3612 with CLKA and CLKB set to f_{clock}.All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 28, the maximum dynamic power dissipation (P_D) of the SN74ABT3614 can be calculated by:

$$P_D = V_{CC} \times I_{CC(f)} + \sum(C_L \times V_{CC} \times (V_{OH} - V_{OL}) \times f_o)$$

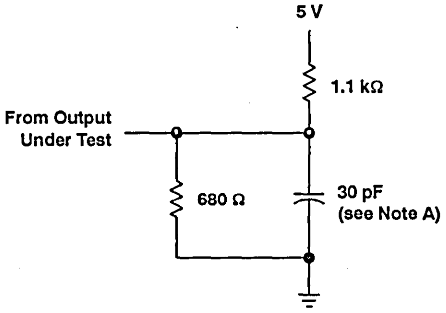
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = output high-level voltage
V_{OL} = output low-level voltage

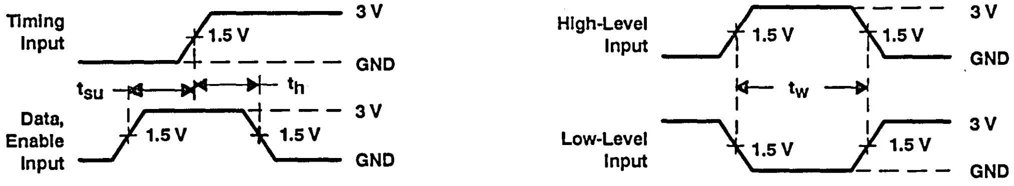
When no reads or writes are occurring on the SN74ABT3612, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.290 \text{ mA/MHz}$$

PARAMETER MEASUREMENT INFORMATION

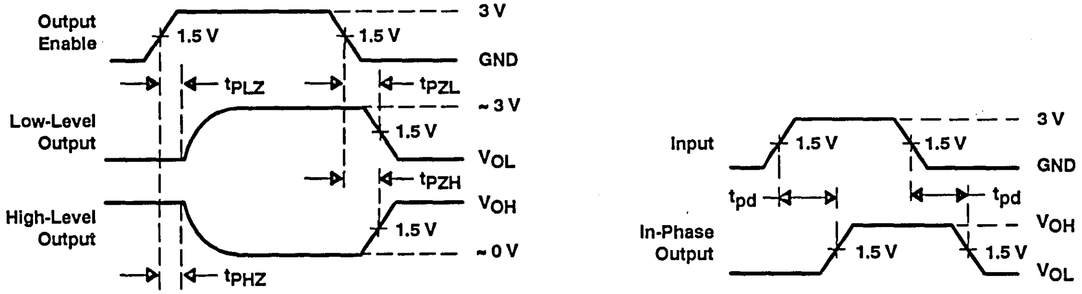


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 21. Load Circuit and Voltage Waveforms

18-BIT CLOCKED FIFOS

Features	Benefits
Member of Texas Instruments Widebus™ family	Combines wider data-path capability with reduced board space area
Advanced BiCMOS process	Fast access time for improved system cycle time and performance
0.8-µm CMOS process	Fast access times combined with low power
TI's advanced clocked interface	Supports free-running clocks with enables
Support clock rates up to 80 MHZ	Supports high-performance systems
Fast access times	Access times as low as 9 ns for improved performance
High drive capabilites	Drive capability as high as –12 mA to 24 mA for high fanout and bus applications
Depths from 64 to 4K words	Multiple depths to optimize system applications
Latched input and output registers	Allows for fast access times and reduced setup and hold times
Grey-code flag architecture	Eliminates race conditions
First-word fallthrough	Eases system interface requirements
Programmable AF/AE flag	Increases design flexibility
Multistage flag synchronization	Increases reliability by increasing MTBF (mean time between failures)
Output edge control (OEC™) circuitry	Improved reliability
Distributed V_{CC} and GND	Improved noise immunity and mutual coupling effects
Fine-pitch package options	Significantly reduces critical board space
EIAJ 80-pin TQFP packages	Board-space savings of up to 70% over 68-pin PLCC option

The following table lists military FIFO Widebus™ devices currently targeted for market introduction. Customers interested in learning more about TI's plans for these devices should contact military Advanced System Logic marketing at (915) 561-7289.

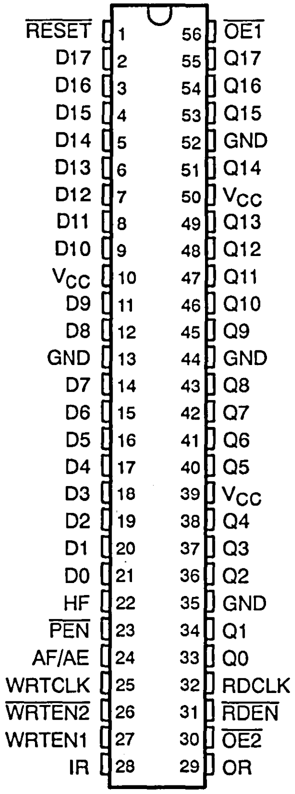
DEVICE	PACKAGE	DESCRIPTION
SNJ54ACT7811-XX	68 CQFP, 68 PGA	1K × 18-Bit Unidirectional Clocked FIFO
SNJ54ABT7819-XX	68 CQFP, 68 PGA	512 × 18-Bit Bidirectional Clocked FIFO

SN74ACT7813
64 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS199 – JANUARY 1991 – REVISED APRIL 1992

- Member of the Texas Instruments Widebus ™ Family
- Free-Running Read and Write Clocks Can Be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Input-Ready Flag Synchronized to Write Clock
- Output-Ready Flag Synchronized to Read Clock
- 64 Words by 18 Bits
- Low-Power Advanced CMOS Technology
- Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag
- Bidirectional Configuration and Width Expansion Without Additional Logic
- Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates From 0 to 67 MHz
- Pin Compatible With SN74ACT7803 and SN74ACT7805
- Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing

DL PACKAGE
(TOP VIEW)



description

The SN74ACT7813 is a 64-word × 18-bit FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins along with TI's patented output edge control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7813 is characterized for operation from 0°C to 70°C.

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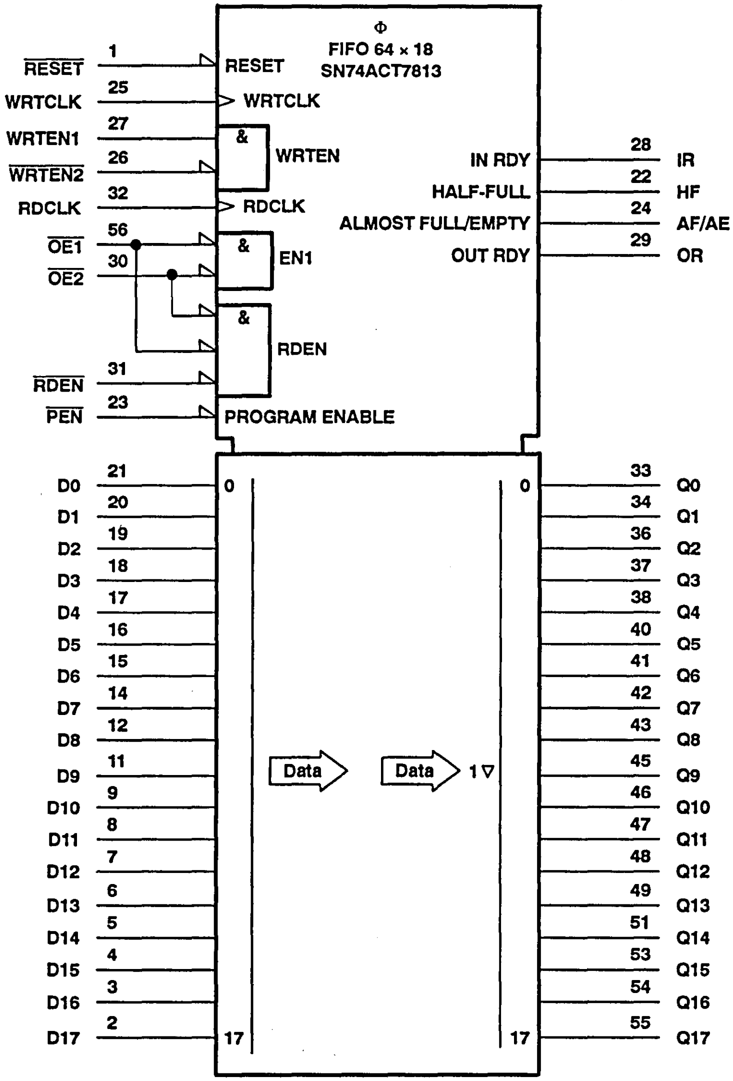
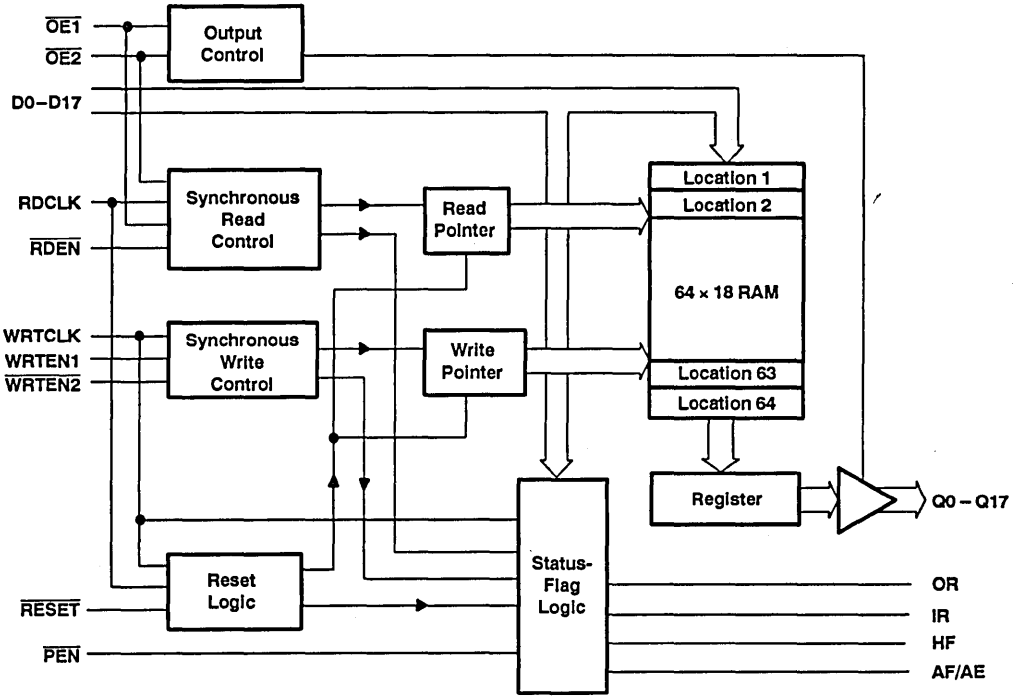
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 8 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{\mathrm{OE1}}$, $\overline{\mathrm{OE2}}$	56, 30	I	Output enables. When $\overline{\mathrm{OE1}}$, $\overline{\mathrm{OE2}}$, and $\overline{\mathrm{RDEN}}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{\mathrm{OE1}}$ or $\overline{\mathrm{OE2}}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\mathrm{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{\mathrm{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{\mathrm{OE1}}$, $\overline{\mathrm{OE2}}$, and $\overline{\mathrm{RDEN}}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
$\overline{\mathrm{RDEN}}$	31	I	Read enable. When $\overline{\mathrm{RDEN}}$, $\overline{\mathrm{OE1}}$, and $\overline{\mathrm{OE2}}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\mathrm{RESET}}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\mathrm{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{\mathrm{WRTEN2}}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{\mathrm{WRTEN2}}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{\mathrm{WRTEN2}}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

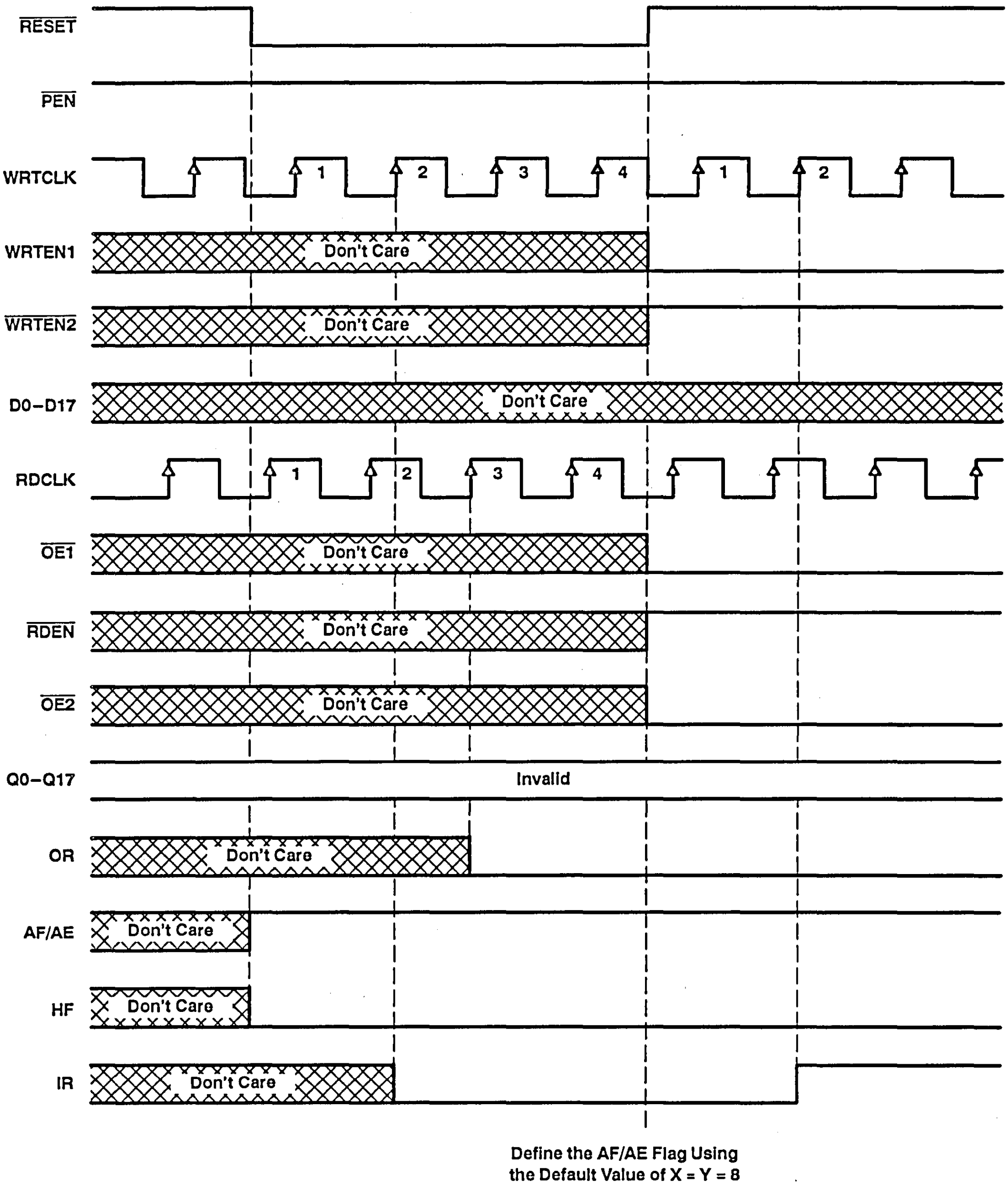


Figure 1. Reset Cycle

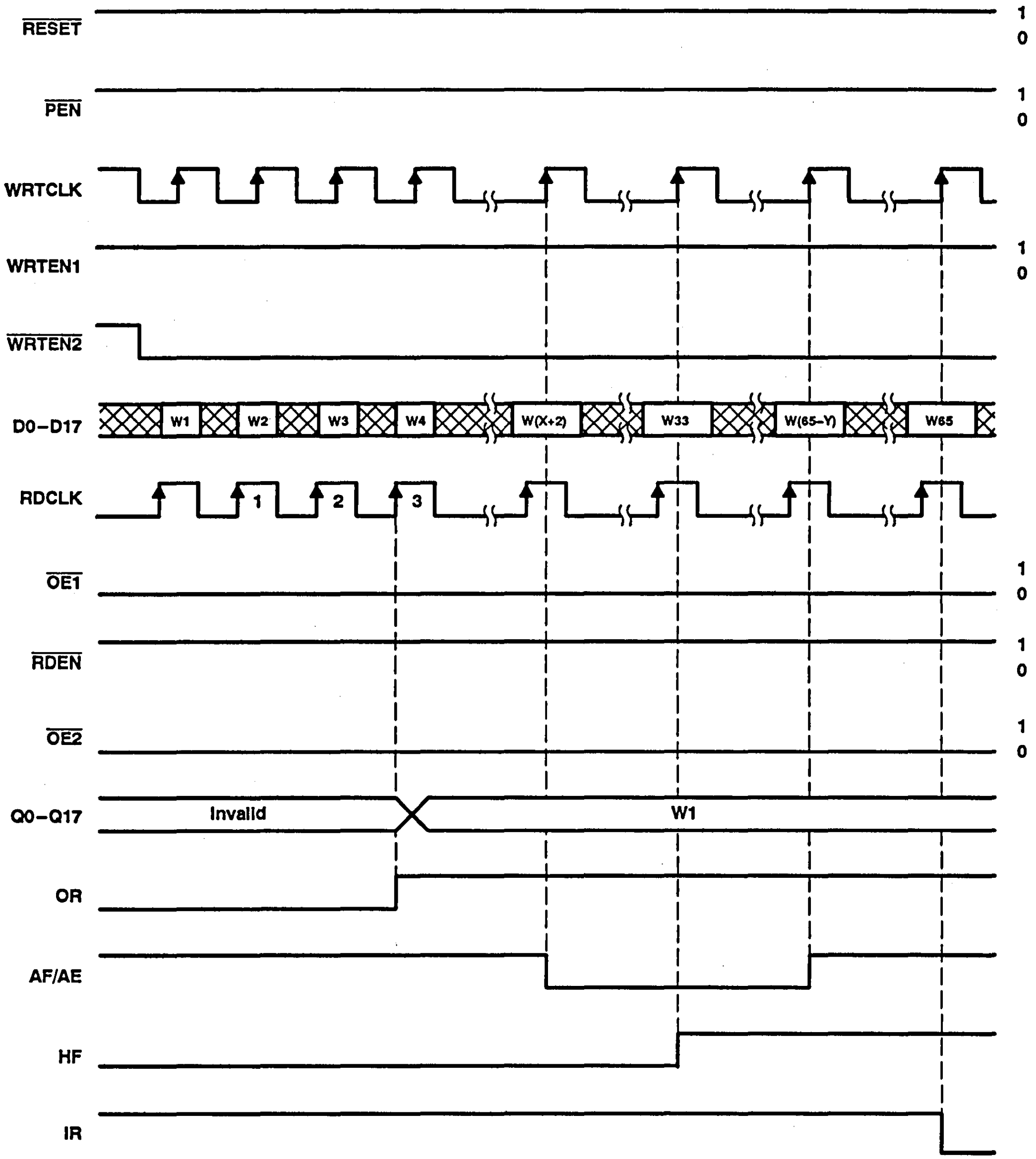


Figure 2. Write

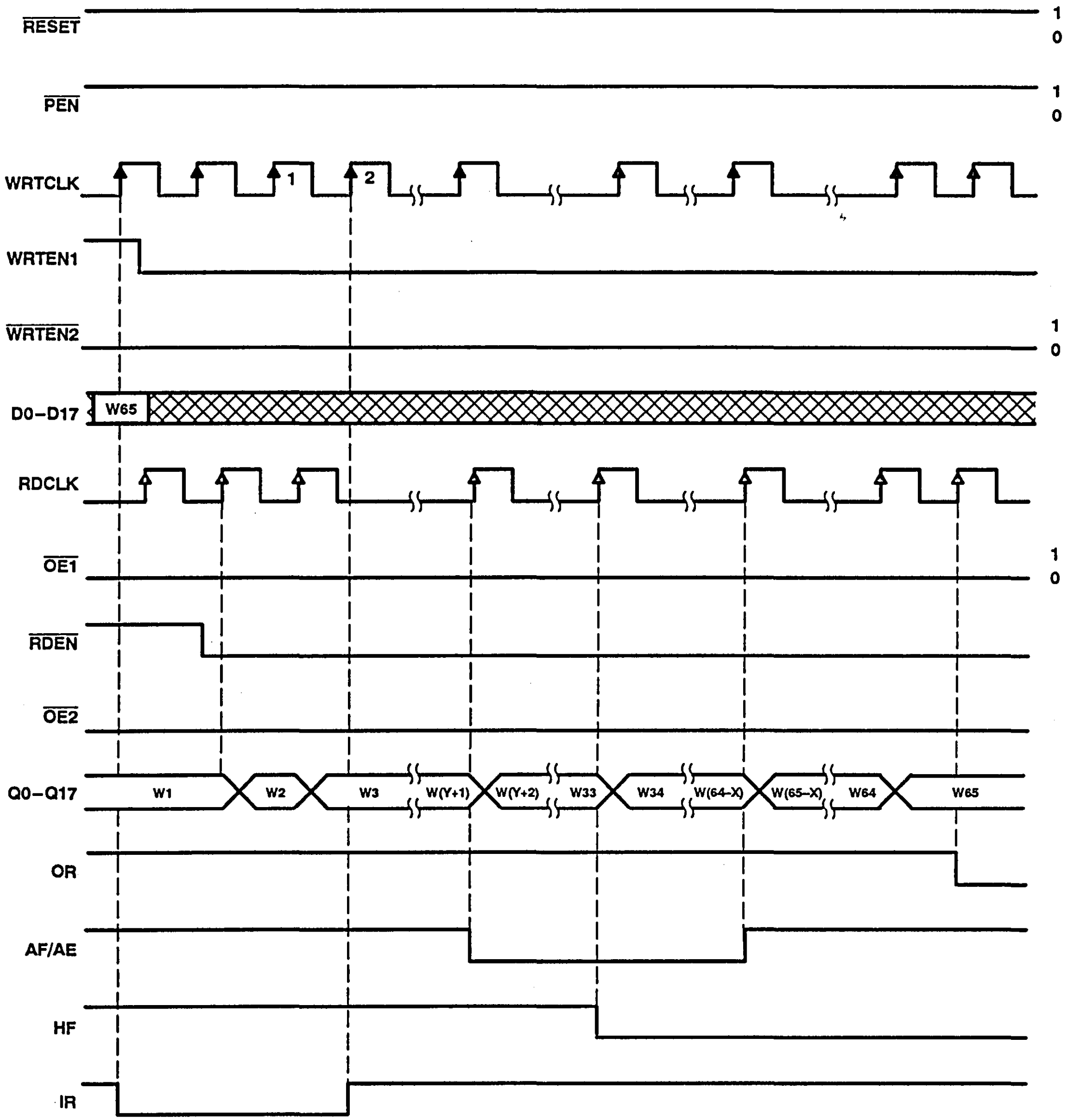


Figure 3. Read

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 8 are used. The AF/AE flag is high when the FIFO contains X or less words or (64 – Y) or more words.

Program enable ($\overline{\text{PEN}}$) should be held high throughout the reset cycle. $\overline{\text{PEN}}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D4 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D4 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{\text{WRTEN2}}$). A maximum value of 31 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 8, $\overline{\text{PEN}}$ must be held high.

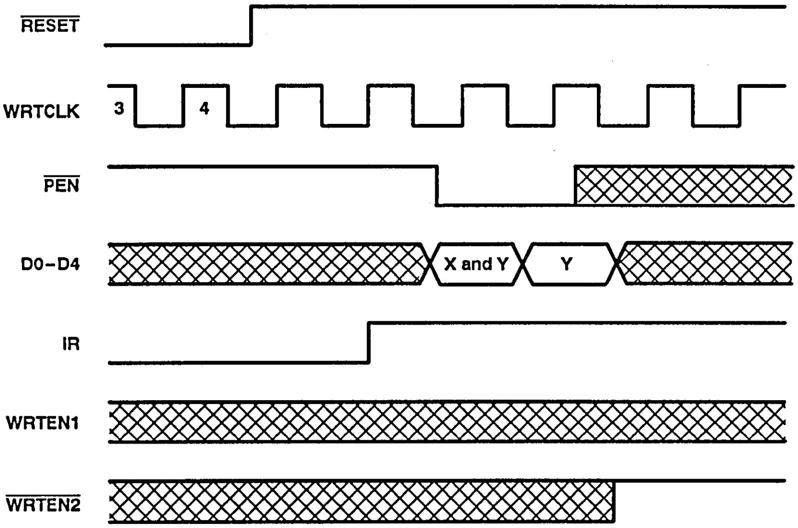


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

---

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7813-15		'ACT7813-20		'ACT7813-25		'ACT7813-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		–8		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{\text{PEN}}$ low	8		9		9		12		
t_{su}	Setup time	D0–D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ before WRTCLK↑	4		5		5		5		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$ before RDCLK↑	5		5		6		6		
		$\overline{\text{RDEN}}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑[†]	5		6		6		6		
		$\overline{\text{PEN}}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ after WRTCLK↑	0		0		0		0		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$, $\overline{\text{RDEN}}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑[†]	2		2		2		2		
		$\overline{\text{PEN}}$ high after WRTCLK↓	0		0		0		0		
		$\overline{\text{PEN}}$ low after WRTCLK↑	2		2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

[†] To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7813-15			'ACT7813-20		'ACT7813-25		'ACT7813-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§				8.5								
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
	RDCLK↑		7		17	7	19	7	21	7	23	
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7		15.5	7	18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}		HF	2		10	2	12	2	14	2	16	
t_{en}	$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}			2		9.5	2	11	2	14	2	14	

§ This parameter is measured with a 30-pF load (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

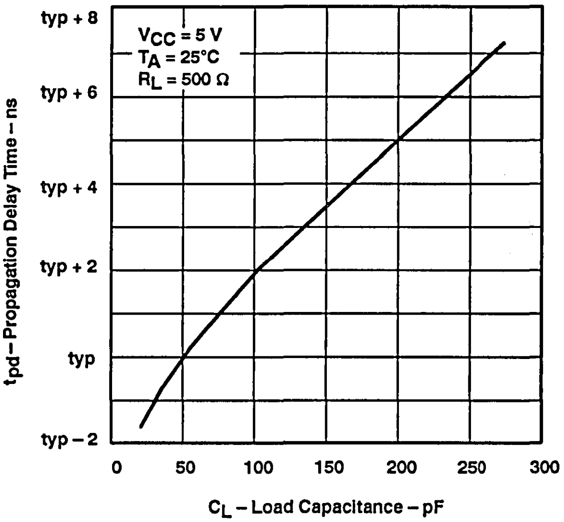


Figure 5

SUPPLY CURRENT vs CLOCK FREQUENCY

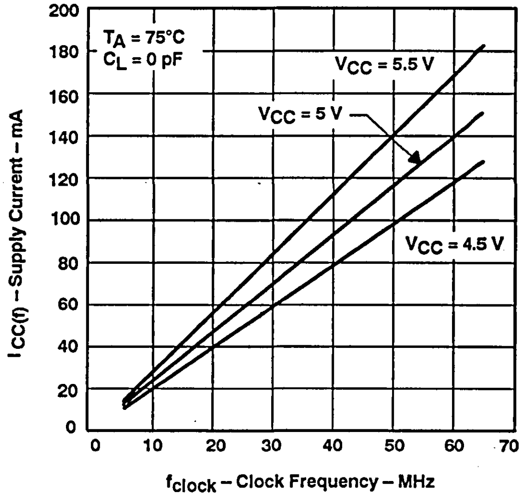


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

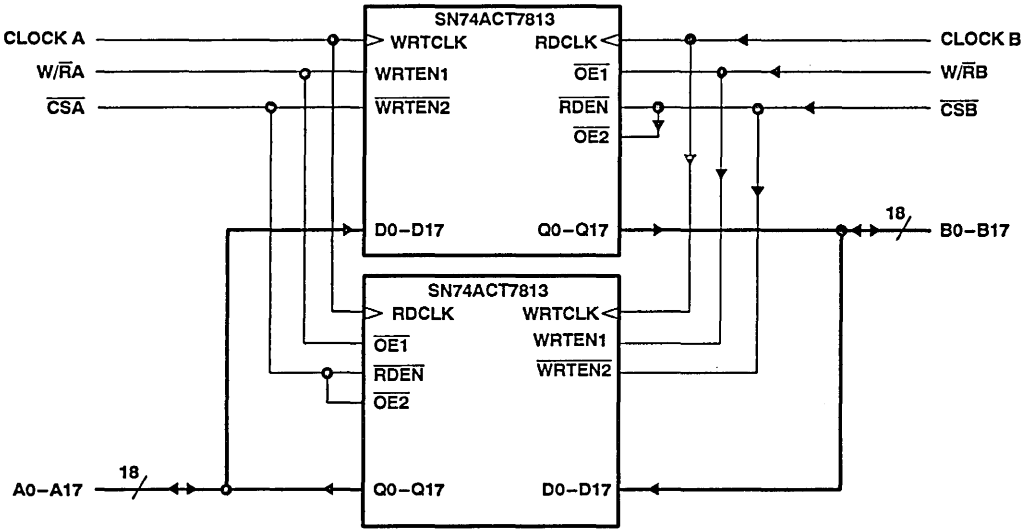


Figure 7. Bidirectional Configuration

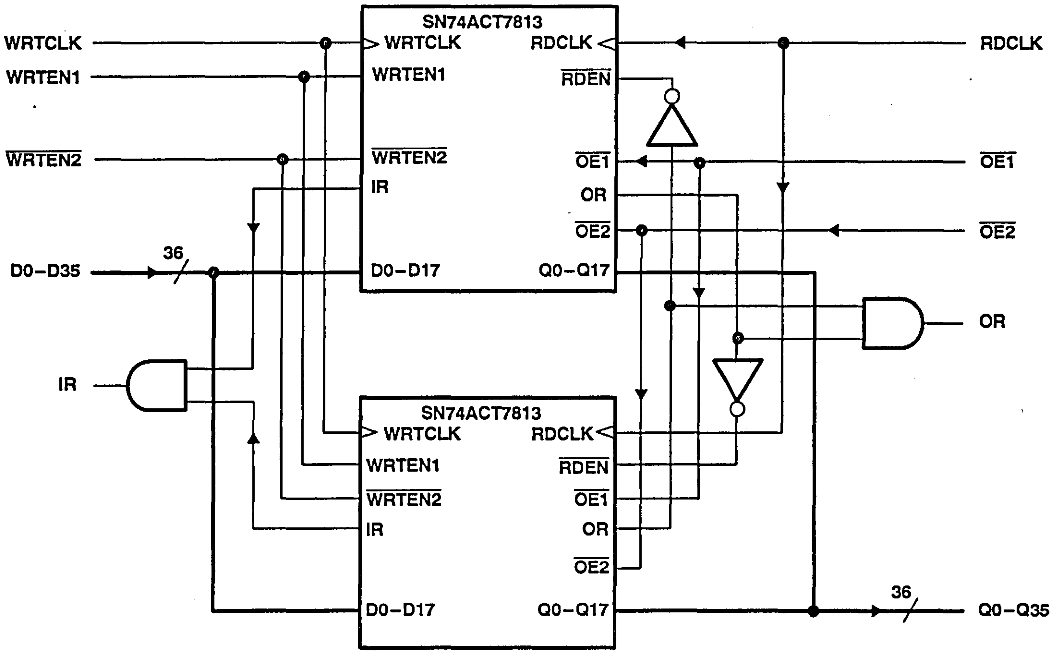


Figure 8. Word-Width Expansion: 64 × 36 Bits

PARAMETER MEASUREMENT INFORMATION

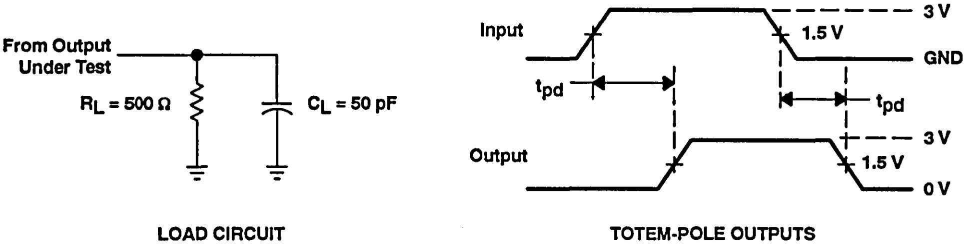
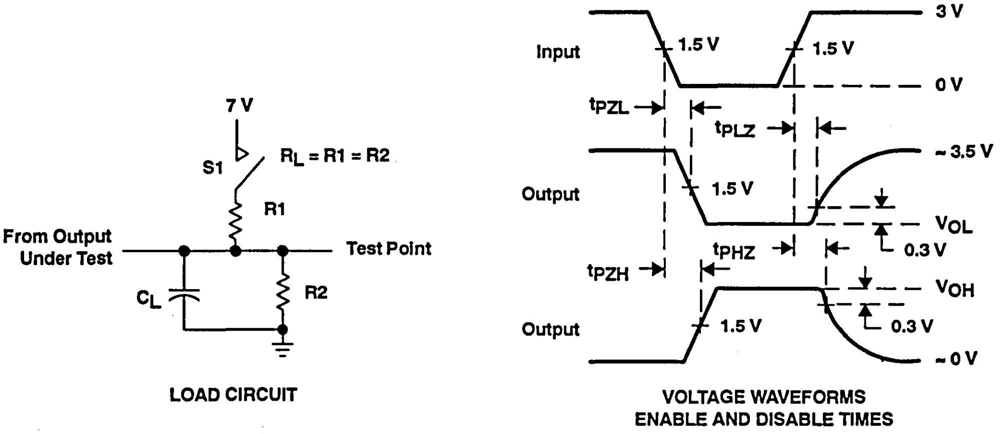


Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

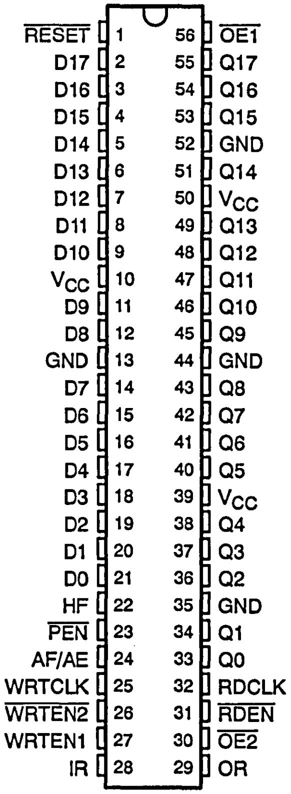
Figure 10. 3-State Outputs (Any Q)

SN74ACT7805
256 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS201 – MARCH 1991 – REVISED APRIL 1992

- **Member of the Texas Instruments Widebus™ Family**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **256 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7803 and SN74ACT7813**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

The SN74ACT7805 is a 256-word × 18-bit clocked FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins along with TI's patented Output Edge Control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

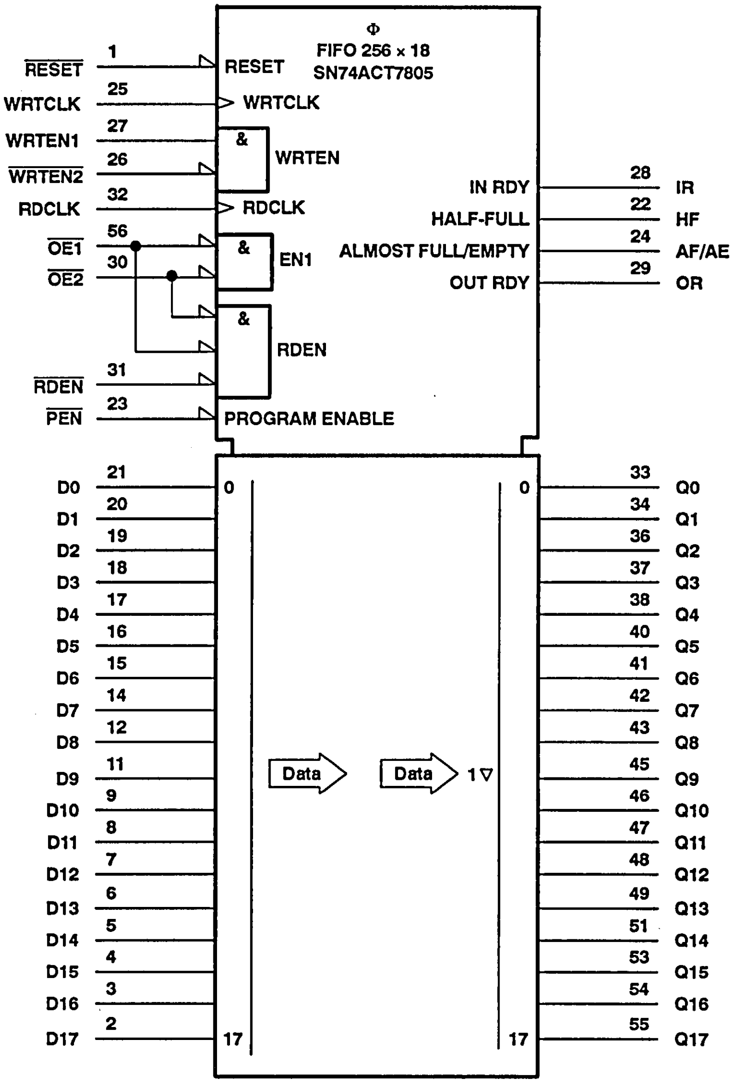
The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7805 is characterized for operation from 0°C to 70°C.

Widebus and OEC are trademarks of Texas Instruments Incorporated.

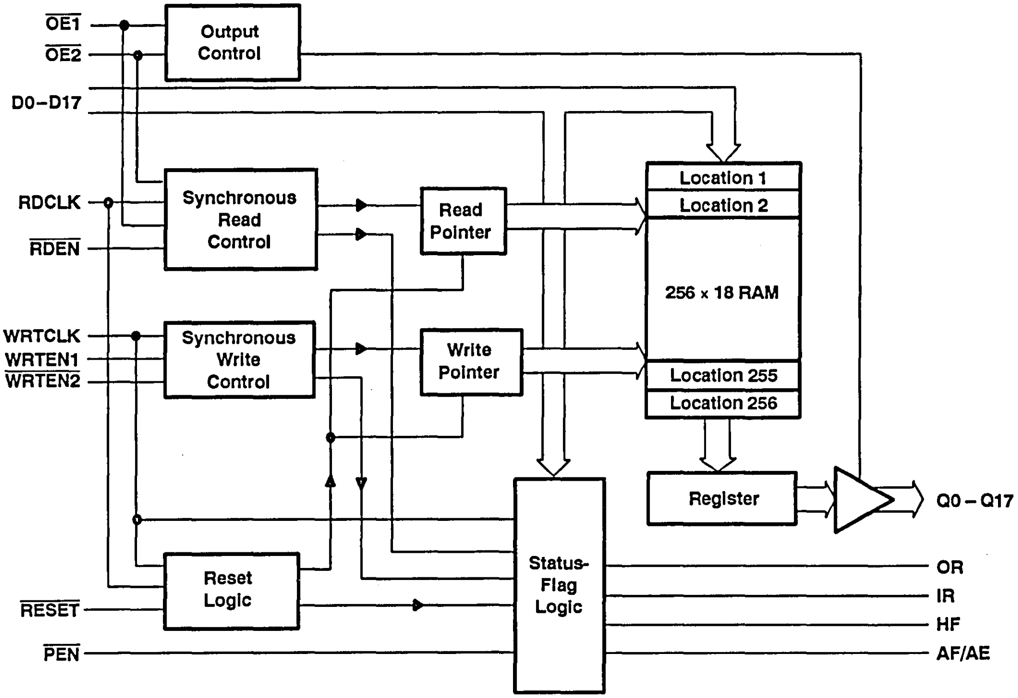
TEXAS INSTRUMENTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 32 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (256 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{\mathrm{OE1}}$, $\overline{\mathrm{OE2}}$	56, 30	I	Output enables. When $\overline{\mathrm{OE1}}$, $\overline{\mathrm{OE2}}$, and $\overline{\mathrm{RDEN}}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{\mathrm{OE1}}$ or $\overline{\mathrm{OE2}}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\mathrm{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when $\overline{\mathrm{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{\mathrm{OE1}}$, $\overline{\mathrm{OE2}}$, and $\overline{\mathrm{RDEN}}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
$\overline{\mathrm{RDEN}}$	31	I	Read enable. When $\overline{\mathrm{RDEN}}$, $\overline{\mathrm{OE1}}$, and $\overline{\mathrm{OE2}}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\mathrm{RESET}}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\mathrm{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{\mathrm{WRTEN2}}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{\mathrm{WRTEN2}}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{\mathrm{WRTEN2}}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

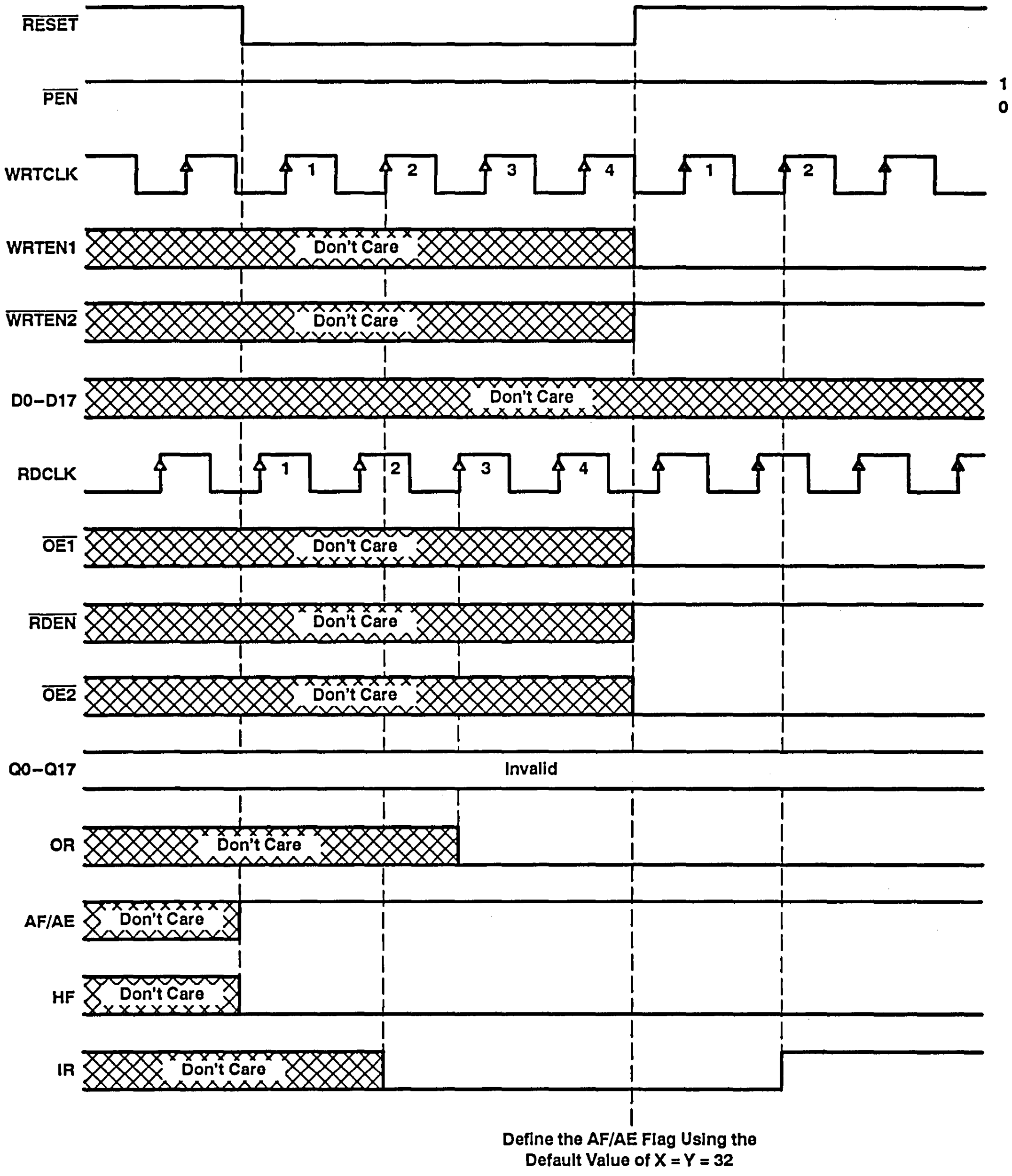


Figure 1. Reset Cycle

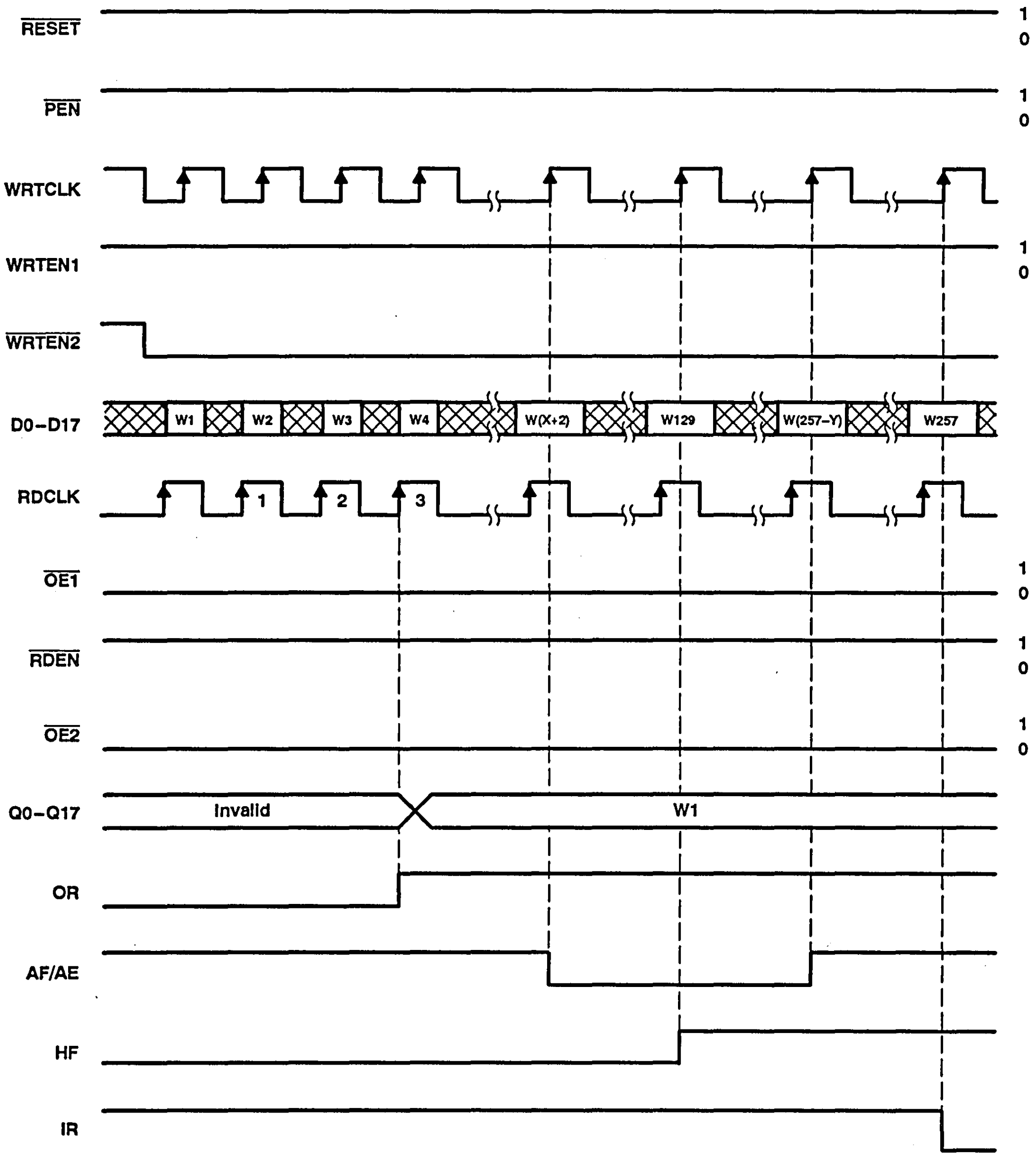


Figure 2. Write

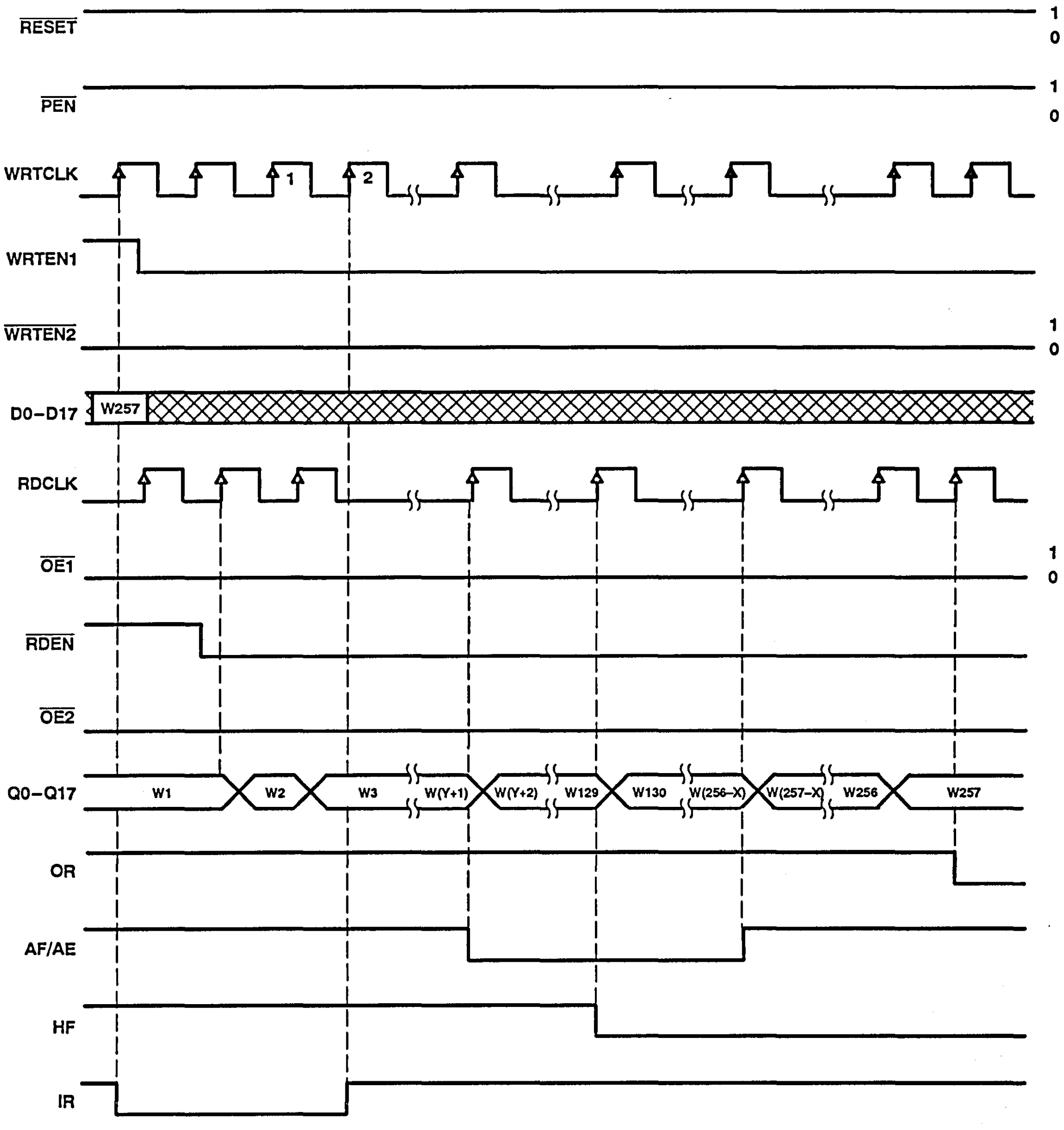


Figure 3. Read

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 32 are used. The AF/AE flag is high when the FIFO contains X or less words or (256 – Y) or more words.

Program enable ($\overline{\text{PEN}}$) should be held high throughout the reset cycle. $\overline{\text{PEN}}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D6 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{\text{WRTEN2}}$). A maximum value of 127 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 32, $\overline{\text{PEN}}$ must be held high.

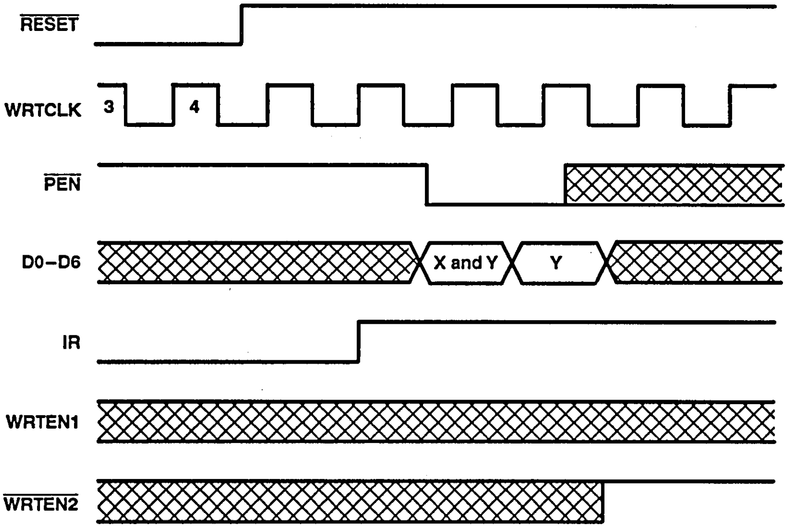


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7805-15		'ACT7805-20		'ACT7805-25		'ACT7805-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{\text{PEN}}$ low	8		9		9		12		
t_{su}	Setup time	D0−D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ before WRTCLK↑	4		5		5		5		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$ before RDCLK↑	5		5		6		6		
		$\overline{\text{RDEN}}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑ †	5		6		6		6		
		$\overline{\text{PEN}}$ before WRTCLK↑	5		6		6		6		
		Define AF/AE: $\overline{\text{PEN}}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0−D17) after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ after WRTCLK↑	0		0		0		0		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$, $\overline{\text{RDEN}}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑ †	2		2		2		2		
		Define AF/AE: $\overline{\text{PEN}}$ after WRTCLK↑	2		2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

† To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V, I_{OH} = – 8 mA	2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V, I_{OL} = 8 mA			0.5	V
	Q outputs	V_{CC} = 4.5 V, I_{OL} = 16 mA			0.5	
I_I		V_{CC} = 5.5 V, V_I = V_{CC} or 0			±5	µA
I_{OZ}		V_{CC} = 5.5 V, V_O = V_{CC} or 0			±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0			400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0, f = 1 MHz		4		pF
C_o		V_O = 0, f = 1 MHz		8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7805-15			'ACT7805-20		'ACT7805-25		'ACT7805-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§				8.5								
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
	RDCLK↑		7		17	7	19	7	21	7	23	
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7		15.5	7	18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}		HF	2		10	2	12	2	14	2	16	
t_{en}	$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}			2		9.5	2	11	2	14	2	14	

§ This parameter is measured with a 30-pF load (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

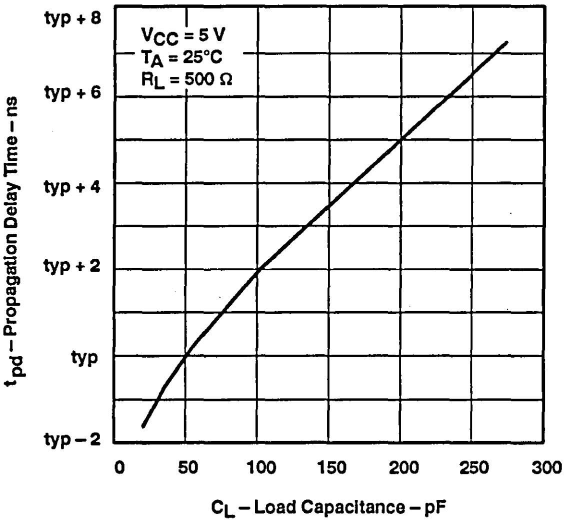


Figure 5

SUPPLY CURRENT
vs
CLOCK FREQUENCY

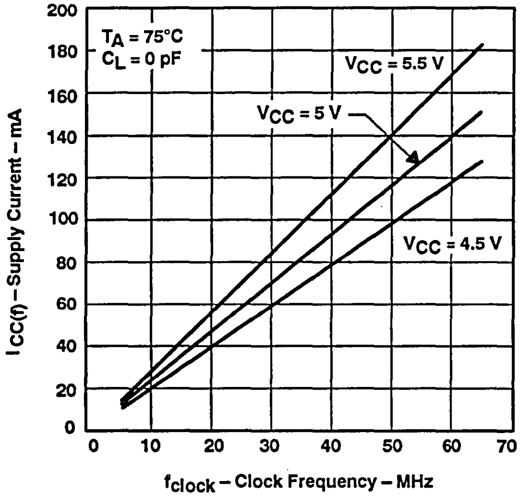


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

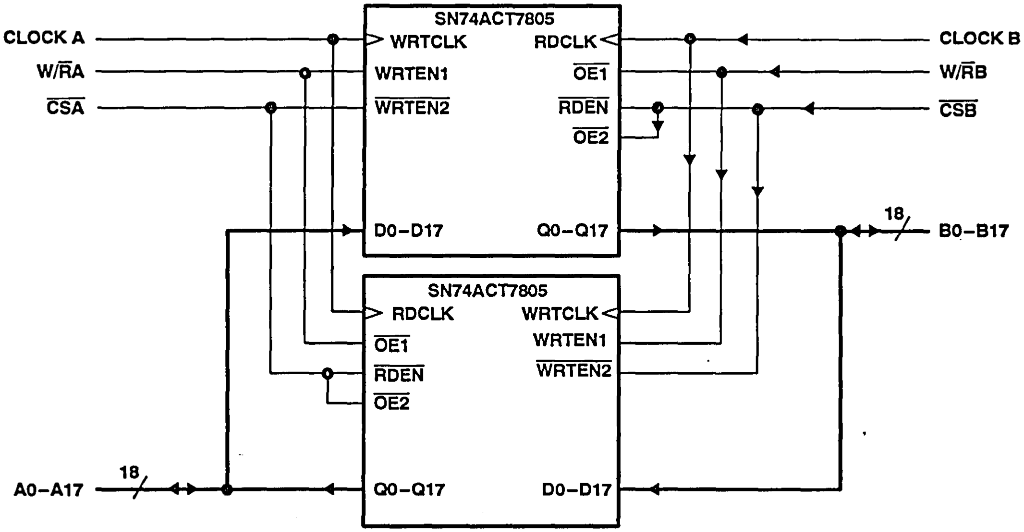


Figure 7. Bidirectional Configuration

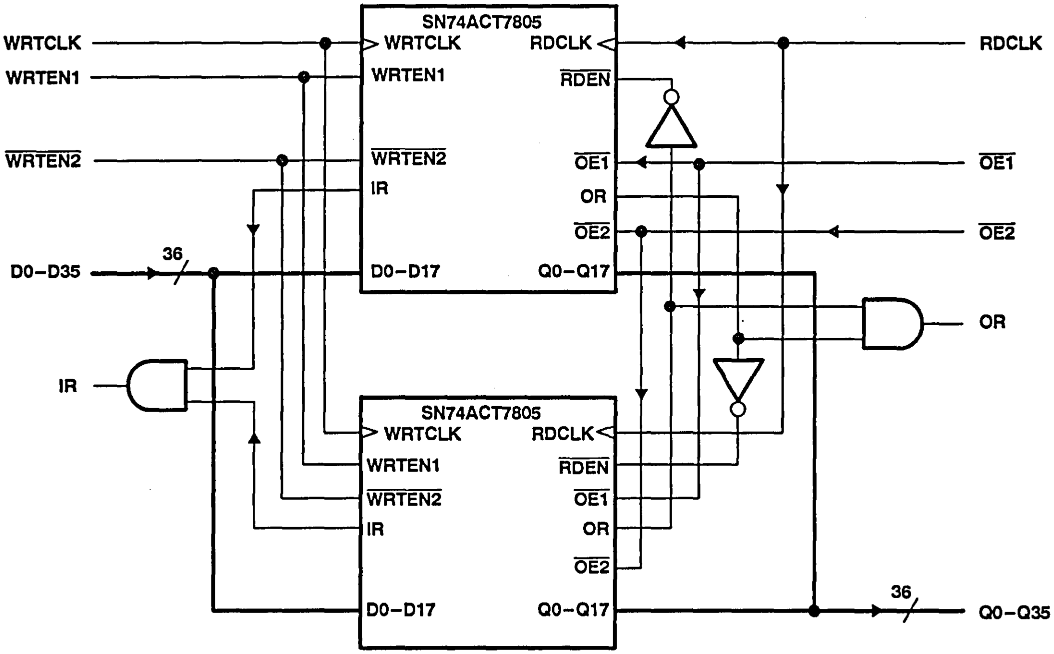
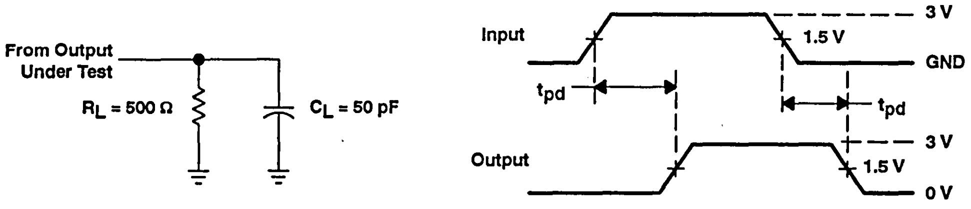


Figure 8. Word-Width Expansion: 256 × 36 Bits

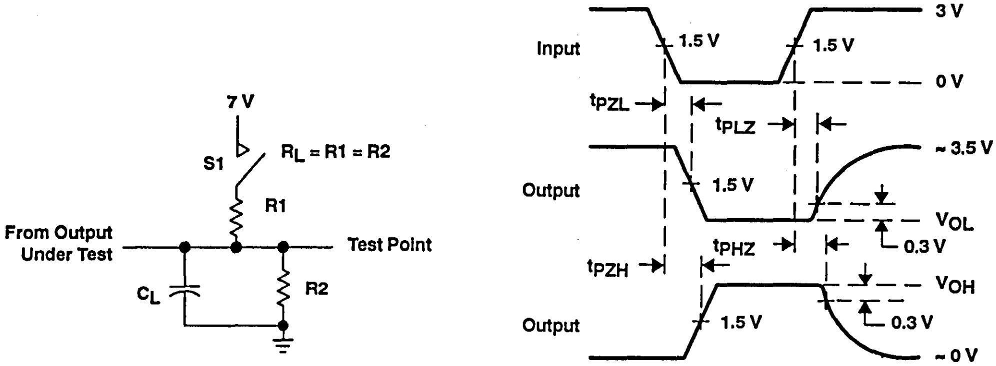
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

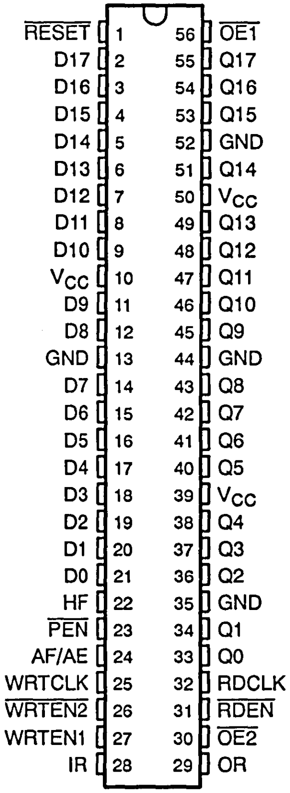
Figure 10. 3-State Outputs (Any Q)

SN74ACT7803
512 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS191 – MARCH 1991 – REVISED MARCH 1992

- **Member of the Texas Instruments Widebus ™ Family**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **512 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7805 and SN74ACT7813**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

The SN74ACT7803 is a 512-word × 18-bit FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins along with TI's patented output edge control (OEC™) circuit dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ levels. The OR flag indicates that valid data is present on the output buffer.

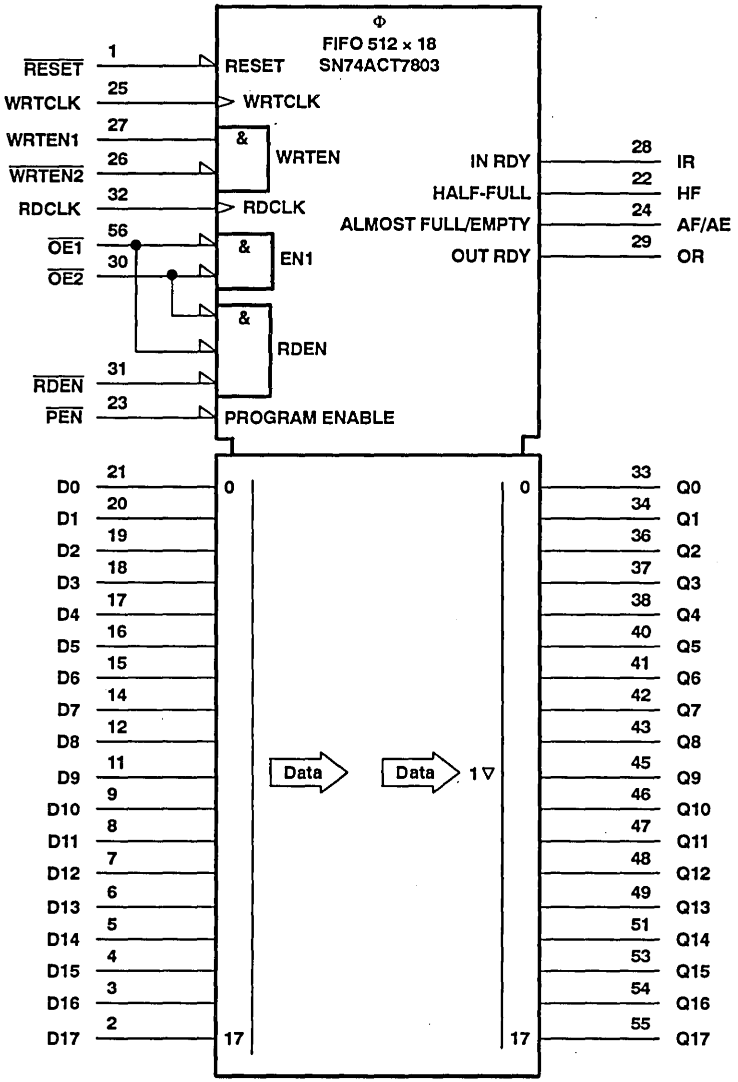
The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{RESET}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7803 is characterized for operation from 0°C to 70°C.

Widebus and OEC are trademarks of Texas Instruments Incorporated.

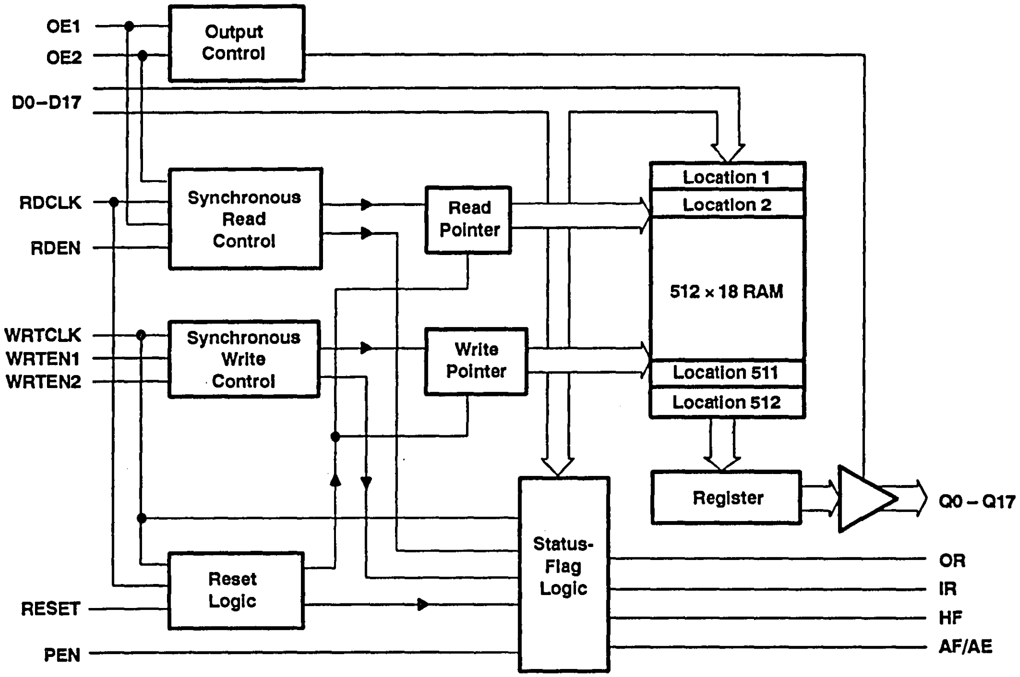
TEXAS
INSTRUMENTS

logic symbol†



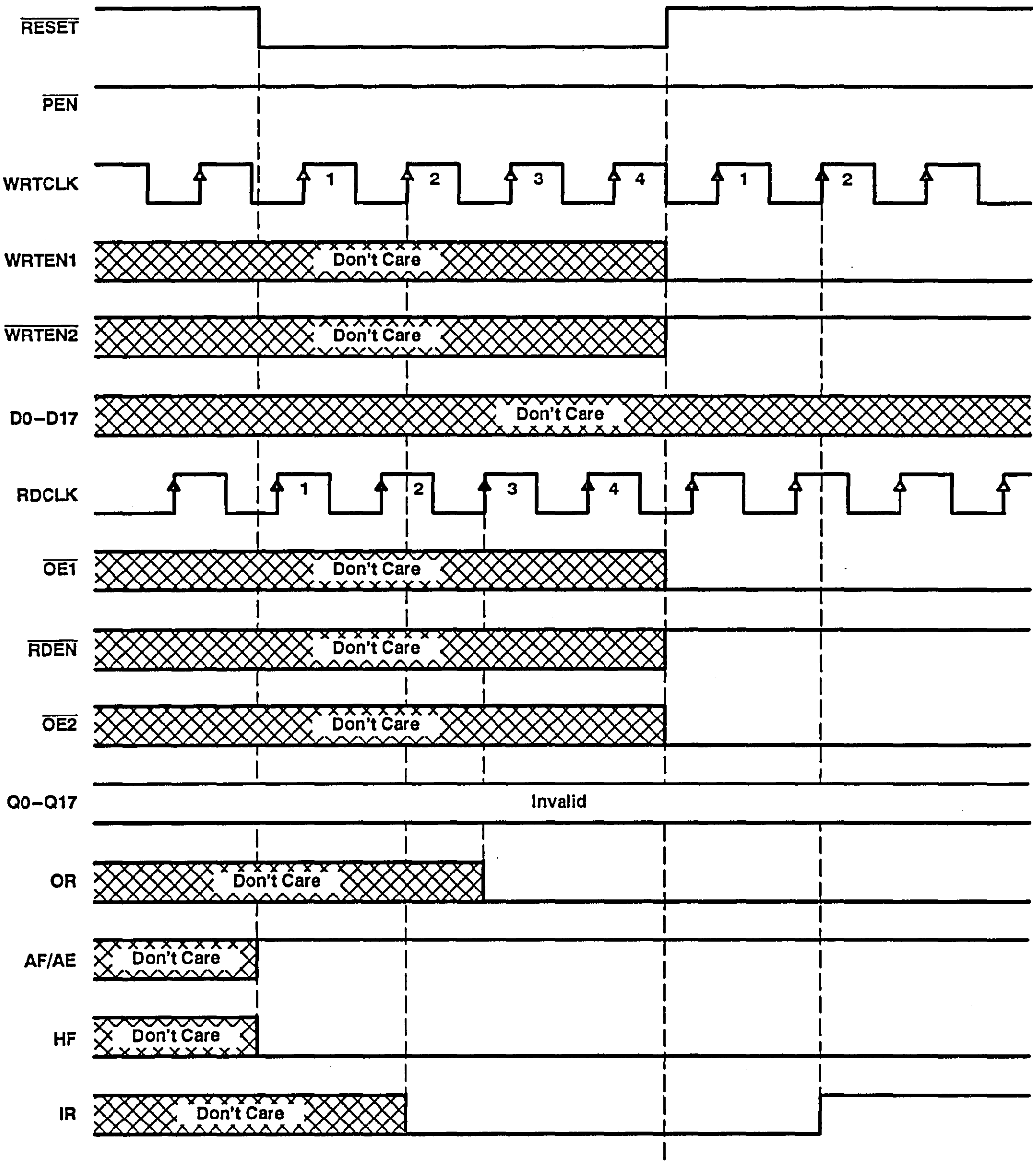
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 64 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (512 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	56, 30	I	Output enables. When $\overline{\text{OE1}}$, $\overline{\text{OE2}}$, and $\overline{\text{RDEN}}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{\text{OE1}}$, $\overline{\text{OE2}}$, and $\overline{\text{RDEN}}$ are low and OR is high. OR is synchronous to the low-to-high transition of RDCLK.
$\overline{\text{RDEN}}$	31	I	Read enable. When $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{\text{WRTEN2}}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{\text{WRTEN2}}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.



Define the AF/AE Flag Using the
Default Value of X = Y = 64

Figure 1. Reset Cycle

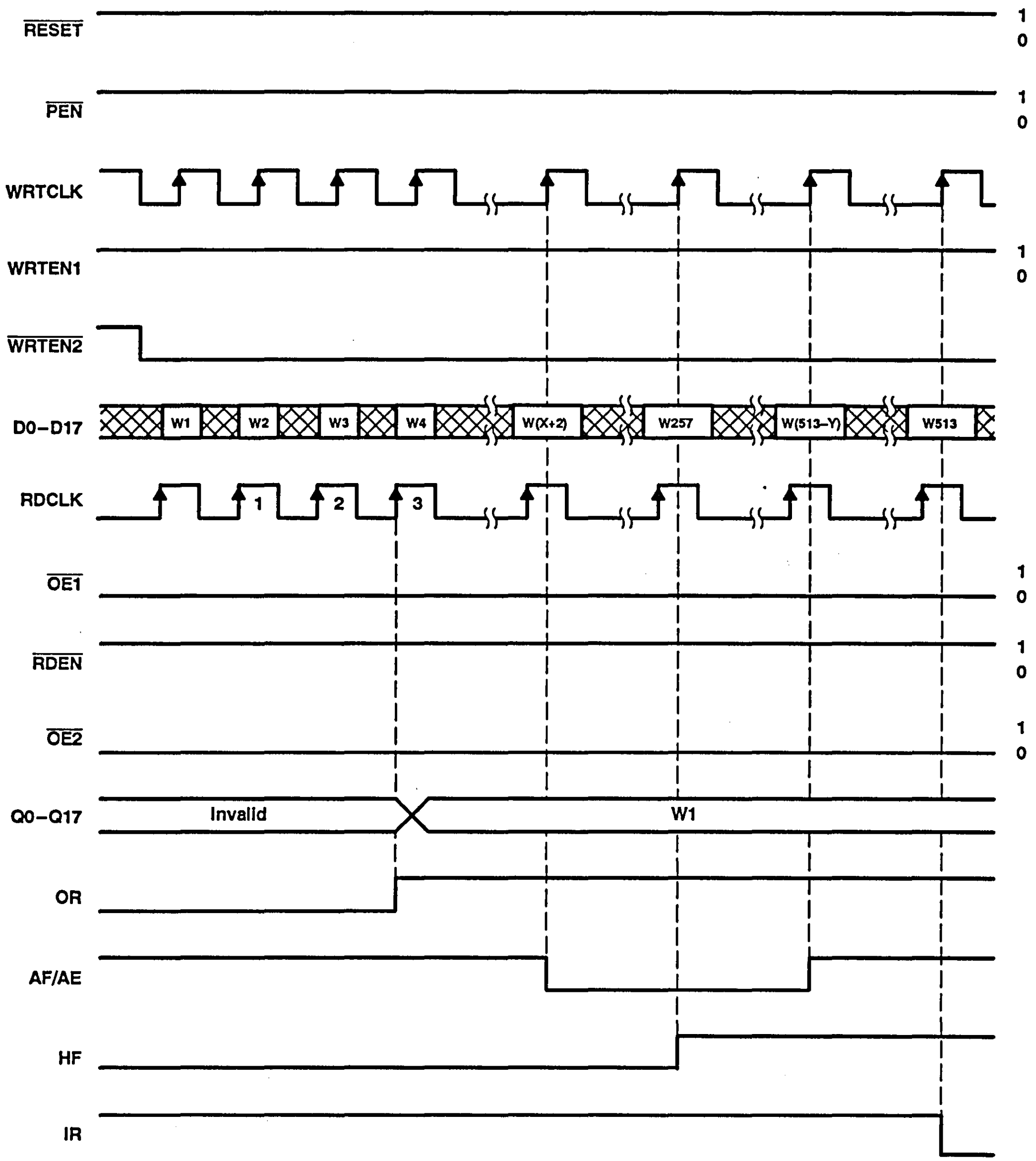


Figure 2. Write

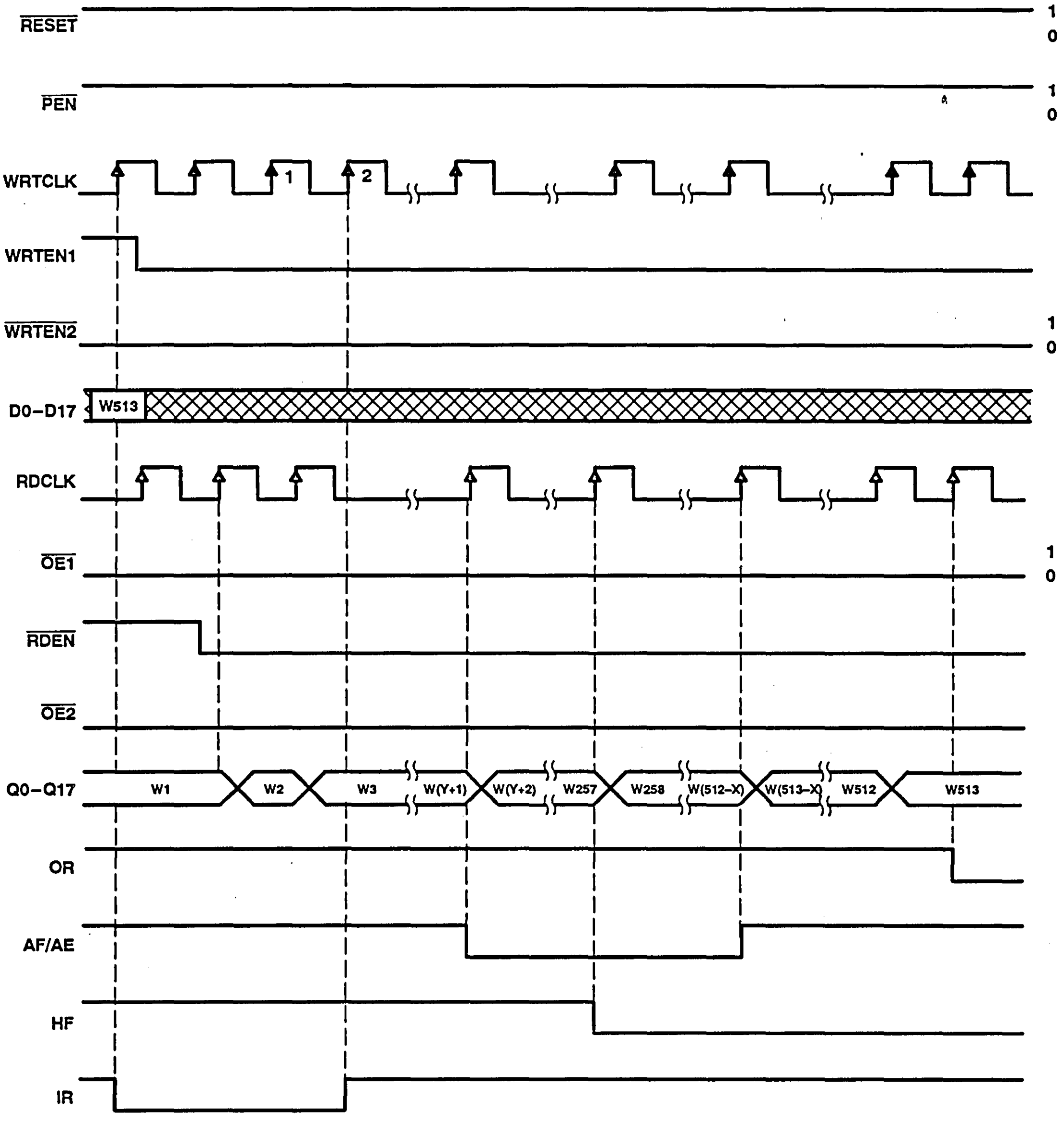


Figure 3. Read

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 64 are used. The AF/AE flag is high when the FIFO contains X or less words or (512 – Y) or more words.

Program enable (PEN) should be held high throughout the reset cycle. PEN can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding PEN low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D7 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, WRTEN2). A maximum value of 255 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 64, PEN must be held high.

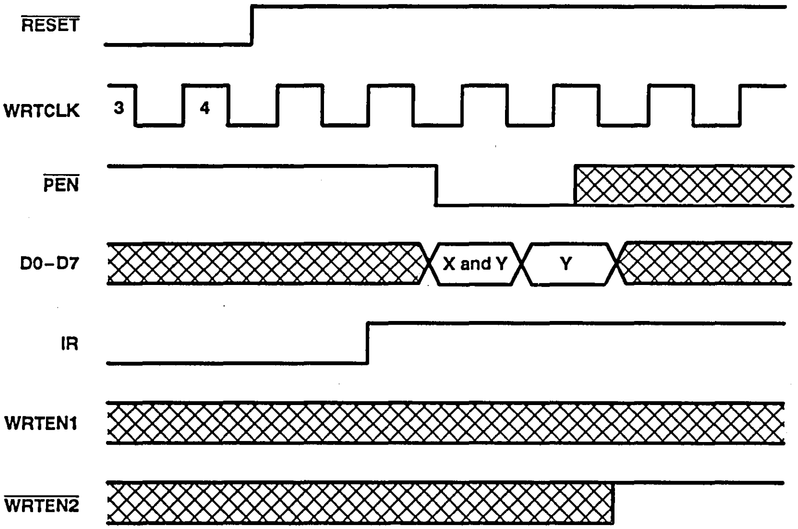


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7803-15		'ACT7803-20		'ACT7803-25		'ACT7803-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{\text{PEN}}$ low	8		9		9		12		
t_{su}	Setup time	D0−D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ before WRTCLK↑	4		5		5		5		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$ before RDCLK↑	5		5		6		6		
		$\overline{\text{RDEN}}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑ †	5		6		6		6		
		$\overline{\text{PEN}}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0−D17 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{\text{WRTEN2}}$ after WRTCLK↑	0		0		0		0		
		$\overline{\text{OE1}}$, $\overline{\text{OE2}}$, $\overline{\text{RDEN}}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑ †	2		2		2		2		
		$\overline{\text{PEN}}$ high after WRTCLK↓	0		0		0		0		
		$\overline{\text{PEN}}$ low after WRTCLK↑	2		2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

† To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	μA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	μA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7803-15			'ACT7803-20		'ACT7803-25		'ACT7803-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§				8.5								
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
t_{pd}	RDCLK↑	AF/AE	7		17	7	19	7	21	7	23	ns
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7		15.5	7	18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}		HF	2		10	2	12	2	14	2	16	
t_{en}	$\overline{\text{OE1}}$, $\overline{\text{OE2}}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}			2		9.5	2	11	2	14	2	14	

§ This parameter is measured with a 30-pF load (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

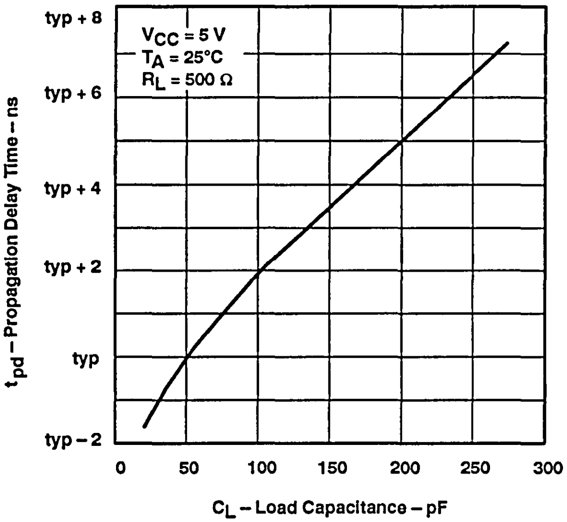


Figure 5

SUPPLY CURRENT
vs
CLOCK FREQUENCY

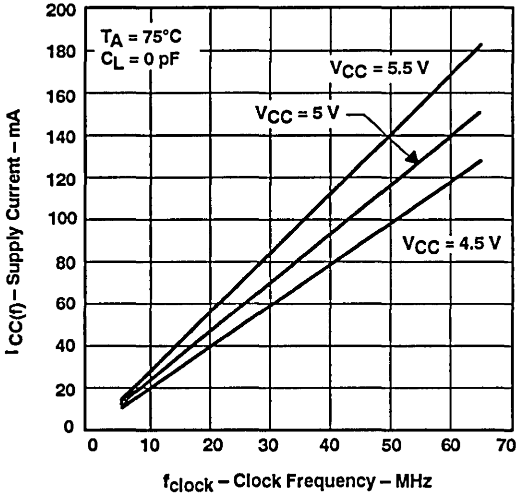


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

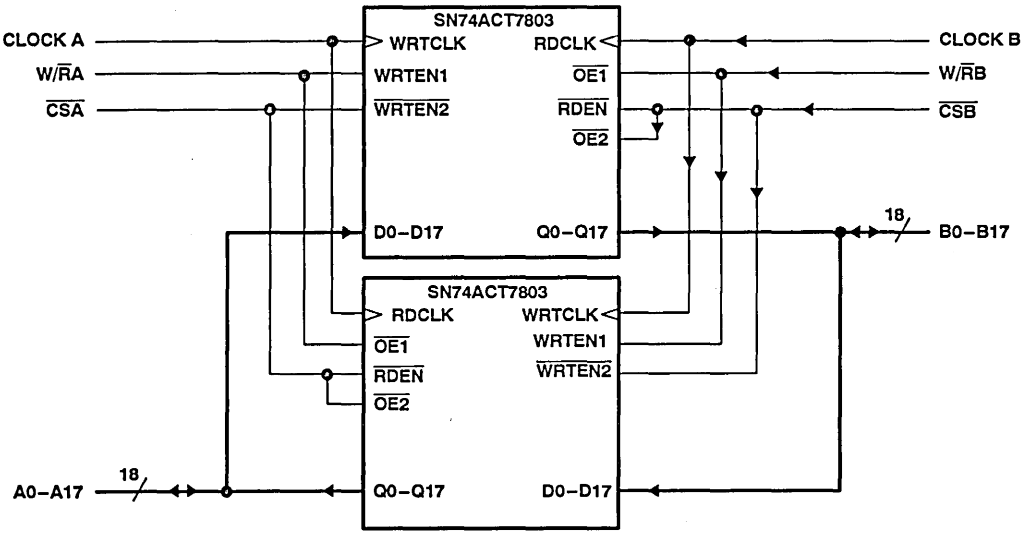


Figure 7. Bidirectional Configuration

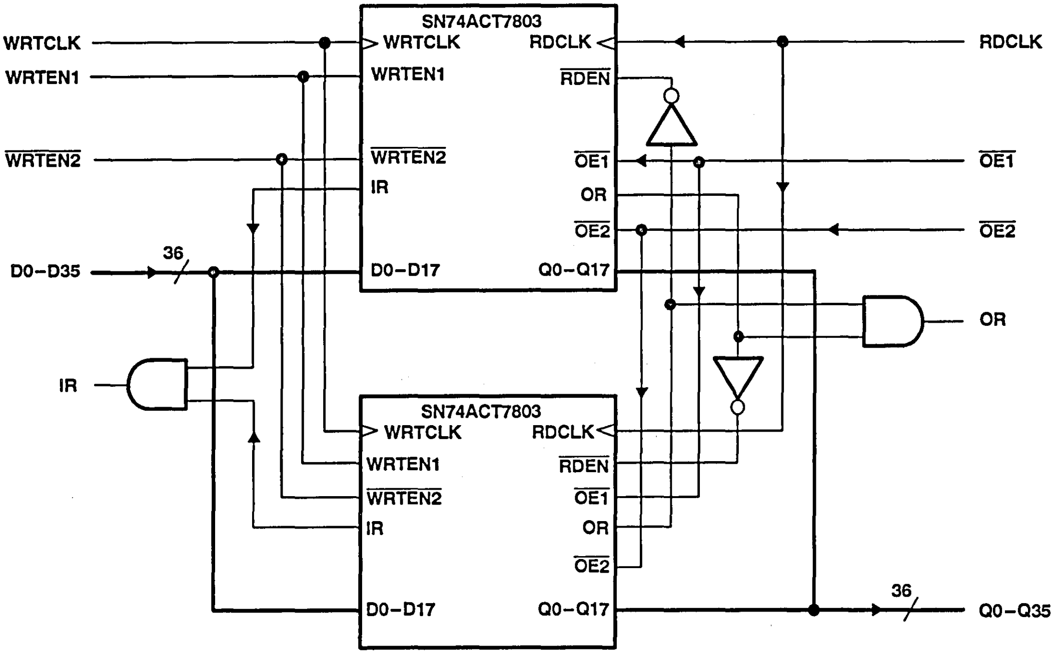


Figure 8. Word-Width Expansion: 512 × 36 Bits

PARAMETER MEASUREMENT INFORMATION

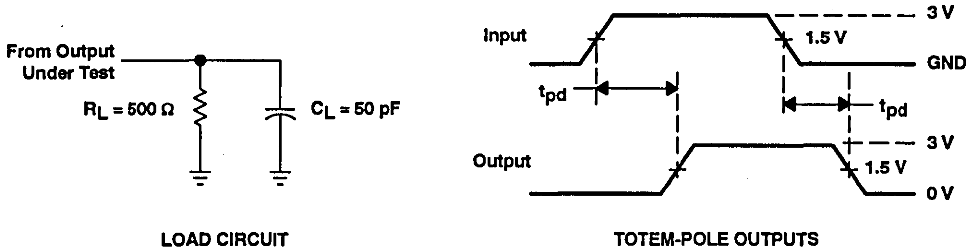
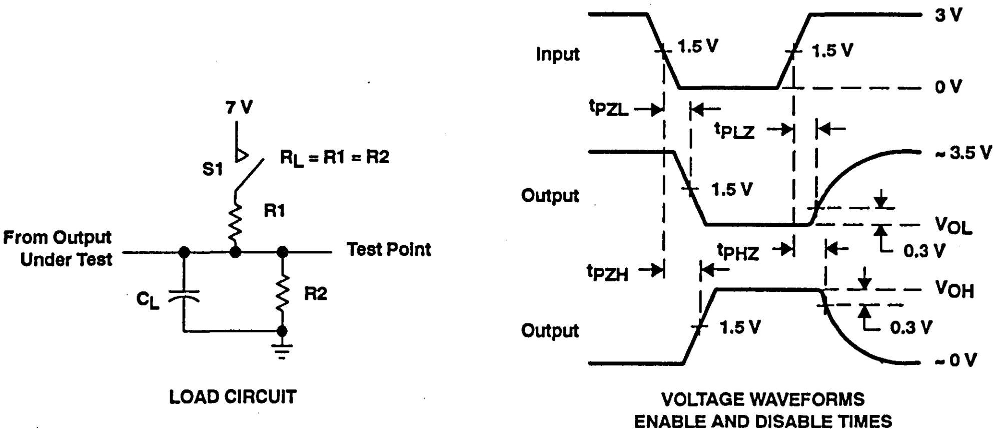


Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

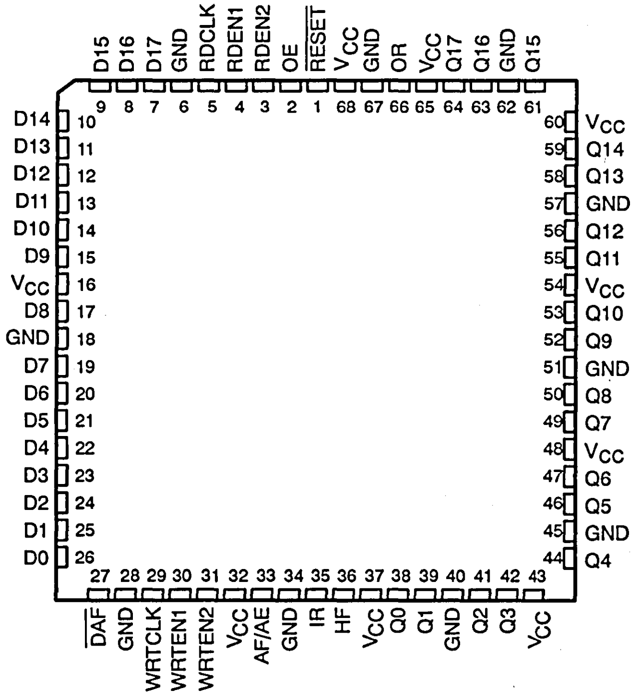
Figure 10. 3-State Outputs (Any Q)

SN74ACT7811
1024 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

SCAS151A – JANUARY 1991 – REVISED FEBRUARY 1992

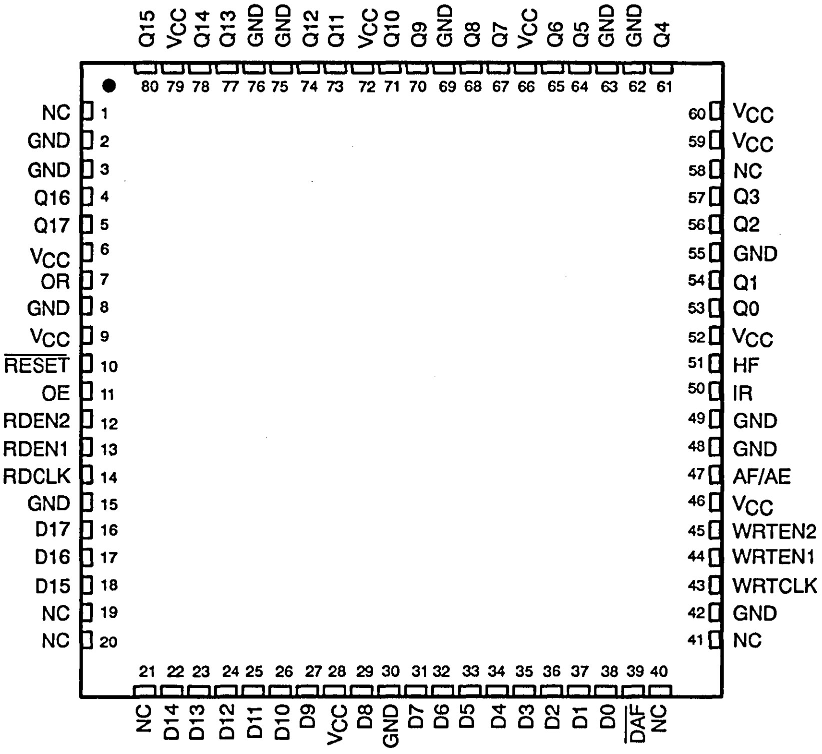
- **Member of the Texas Instruments Widebus™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **1024 Words × 18 Bits**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7882, and SN74ACT7884**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 15 ns With a 50-pF Load**
- **High Output Drive for Direct Bus Interface**
- **Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Thin Quad Flat Packages (PN)**

FN PACKAGE
(TOP VIEW)



Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



NC – No internal connection

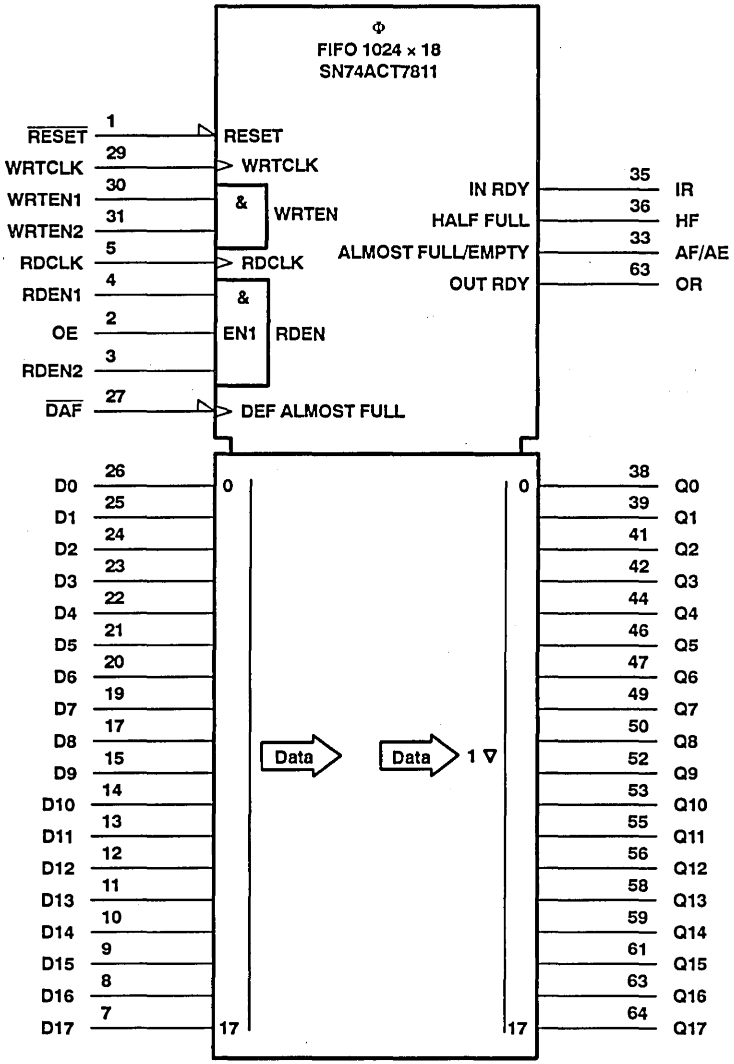
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7811 is a 1024- × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.

The SN74ACT7811 is characterized for operation from 0°C to 70°C.

logic symbol†



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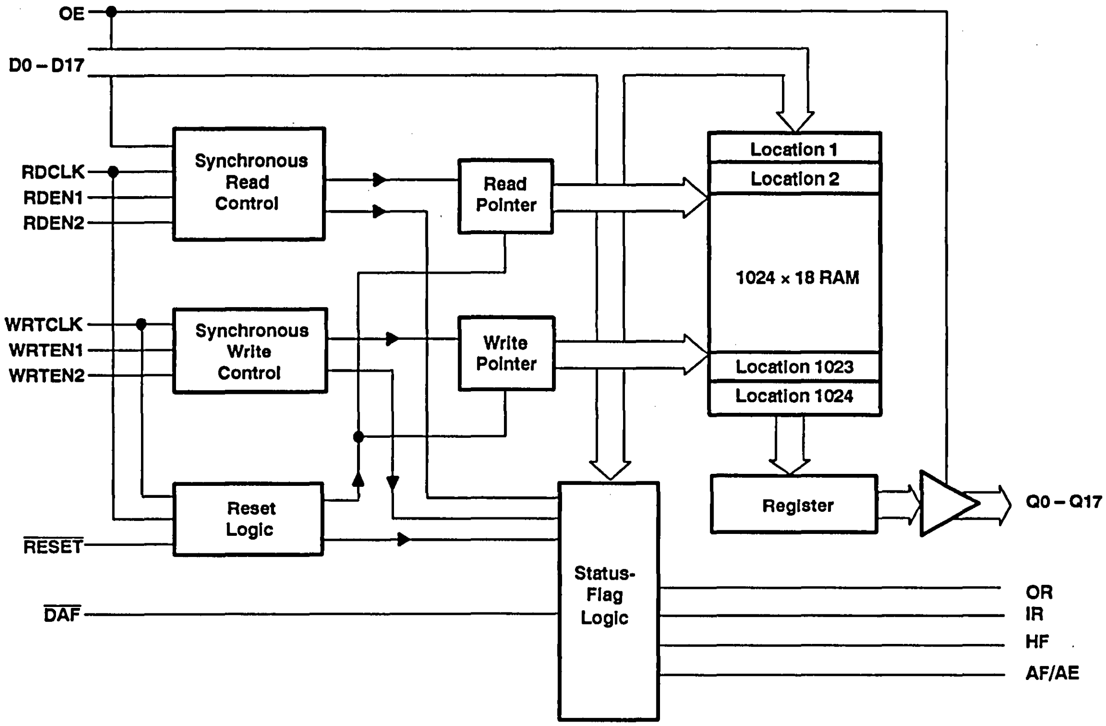
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram

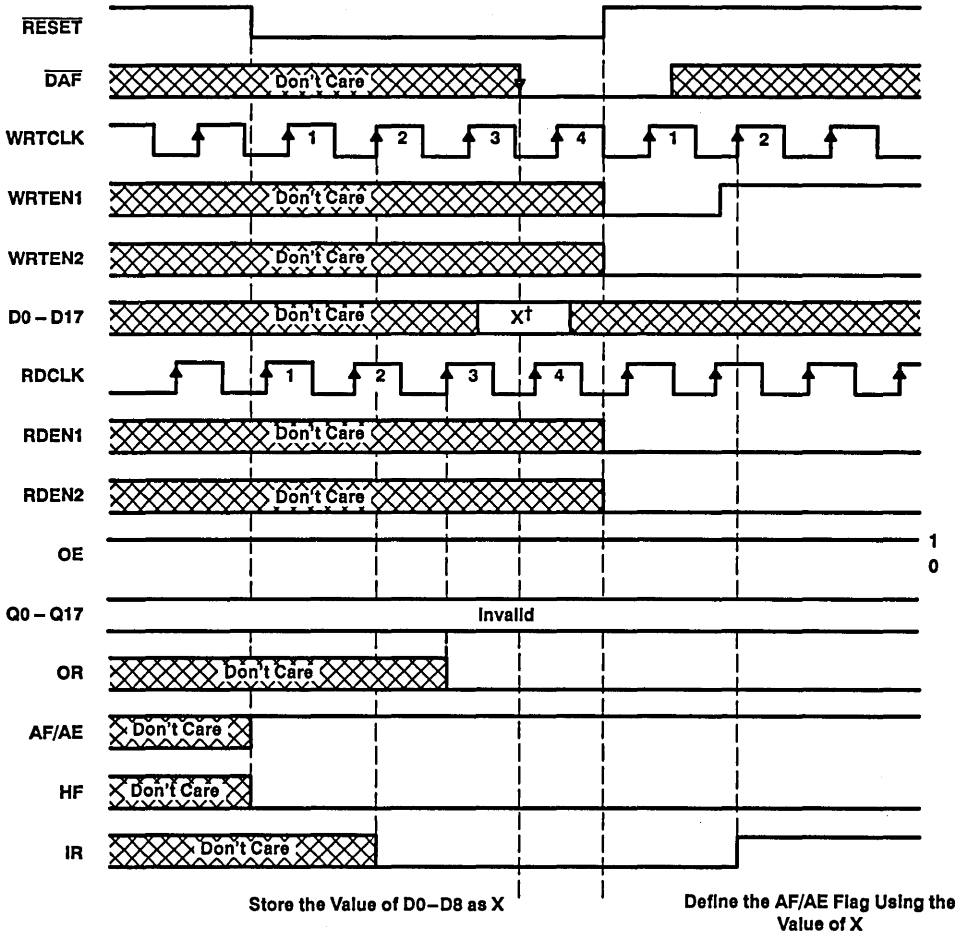


Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. The AR/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset, or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or less words or (1025 – X) or more words. AF/AE is low when the FIFO contains between (X + 2) and (1024 - X) words. Programming procedure for AF/AE – The almost-full/almost-empty flag is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: User-defined X Step 1: Take $\overline{\text{DAF}}$ from high to low. Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. Default X To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	27	I	Define-almost-full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0 – D8 also carry the almost-full/almost-empty offset value (X) on a high-to-low transition of the $\overline{\text{DAF}}$.
HF	36	O	Half-full flag. HF is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.
IR	35	O	Input-ready-flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The data-out (Q0–Q17) outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	63	O	Output ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and the OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE, and RDEN1 and RDEN2 control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and OR, HF, and IR are low and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines the AF/AE status flag using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enables. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).



† X is the binary value of D0–D8 only.

Figure 1. Reset Cycle: Define AF/AE Using the Value of X

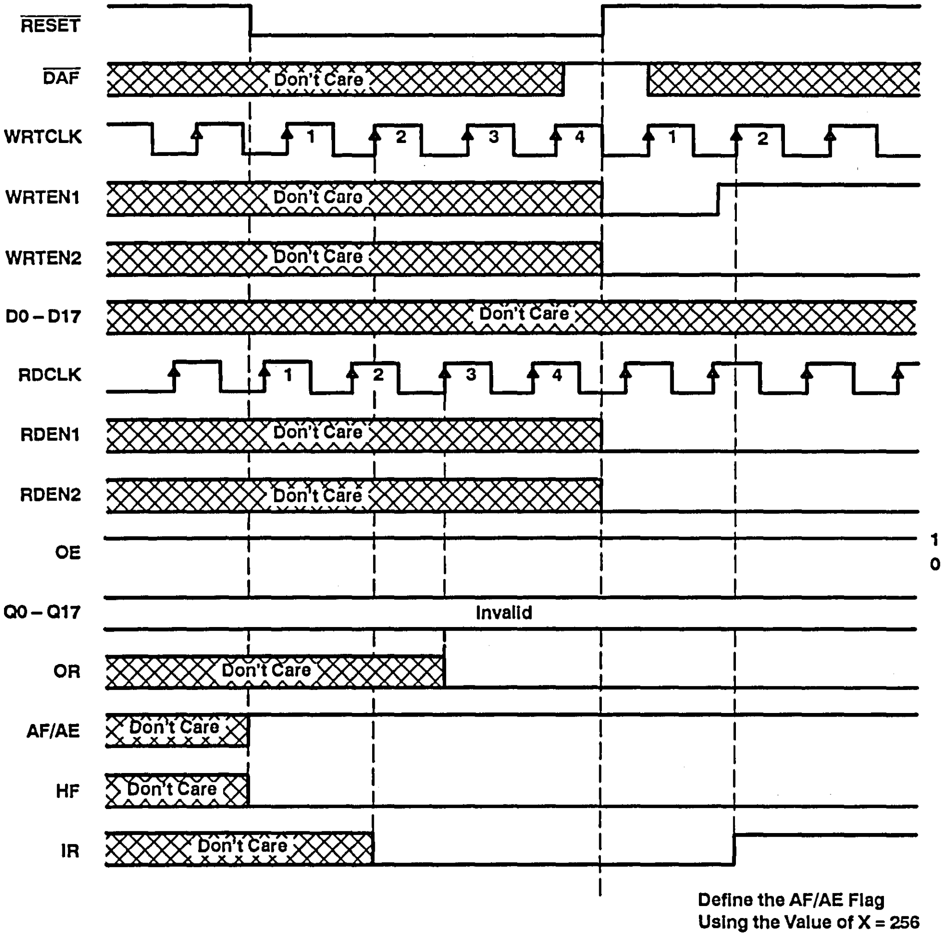


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

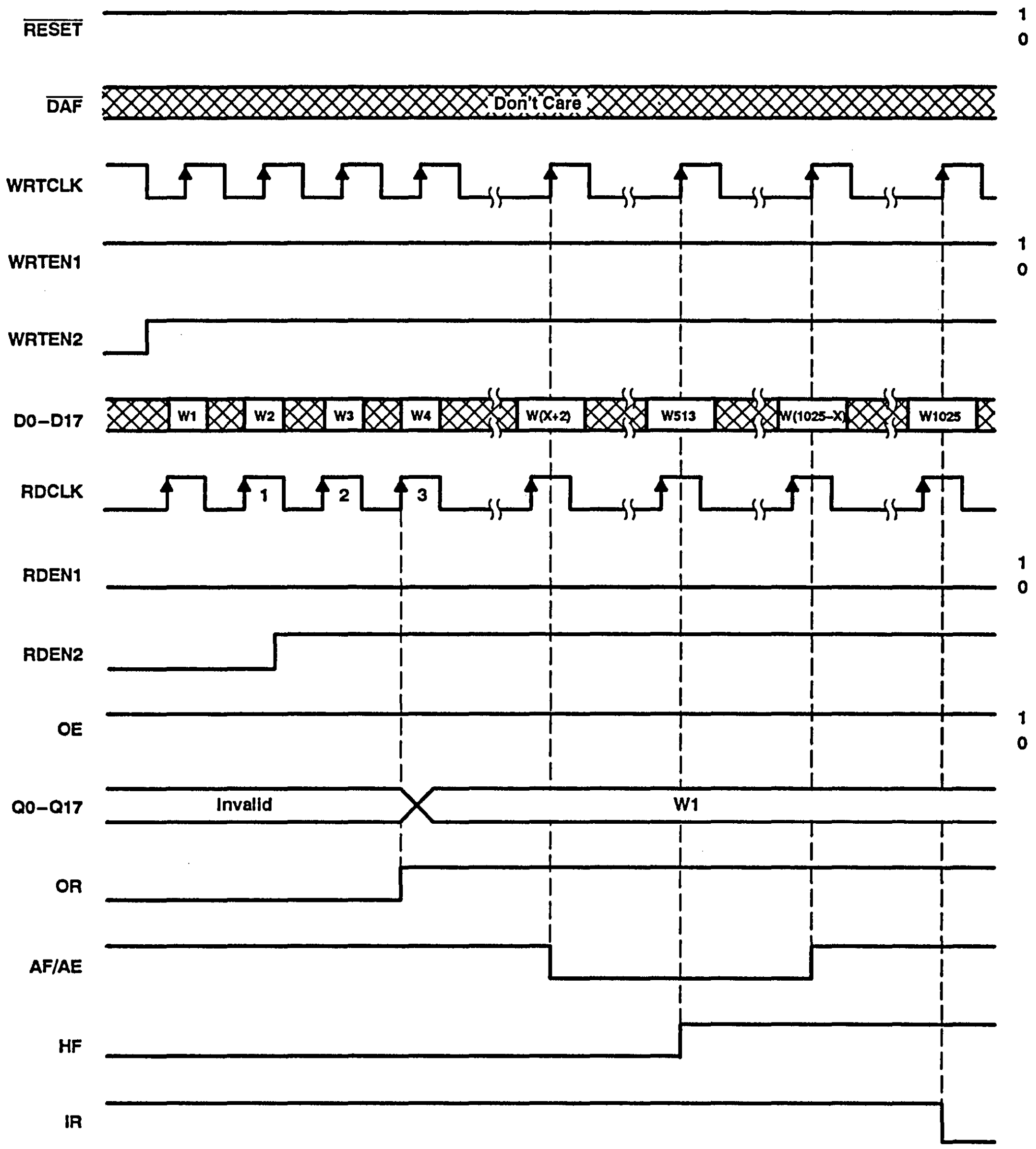


Figure 3. Write

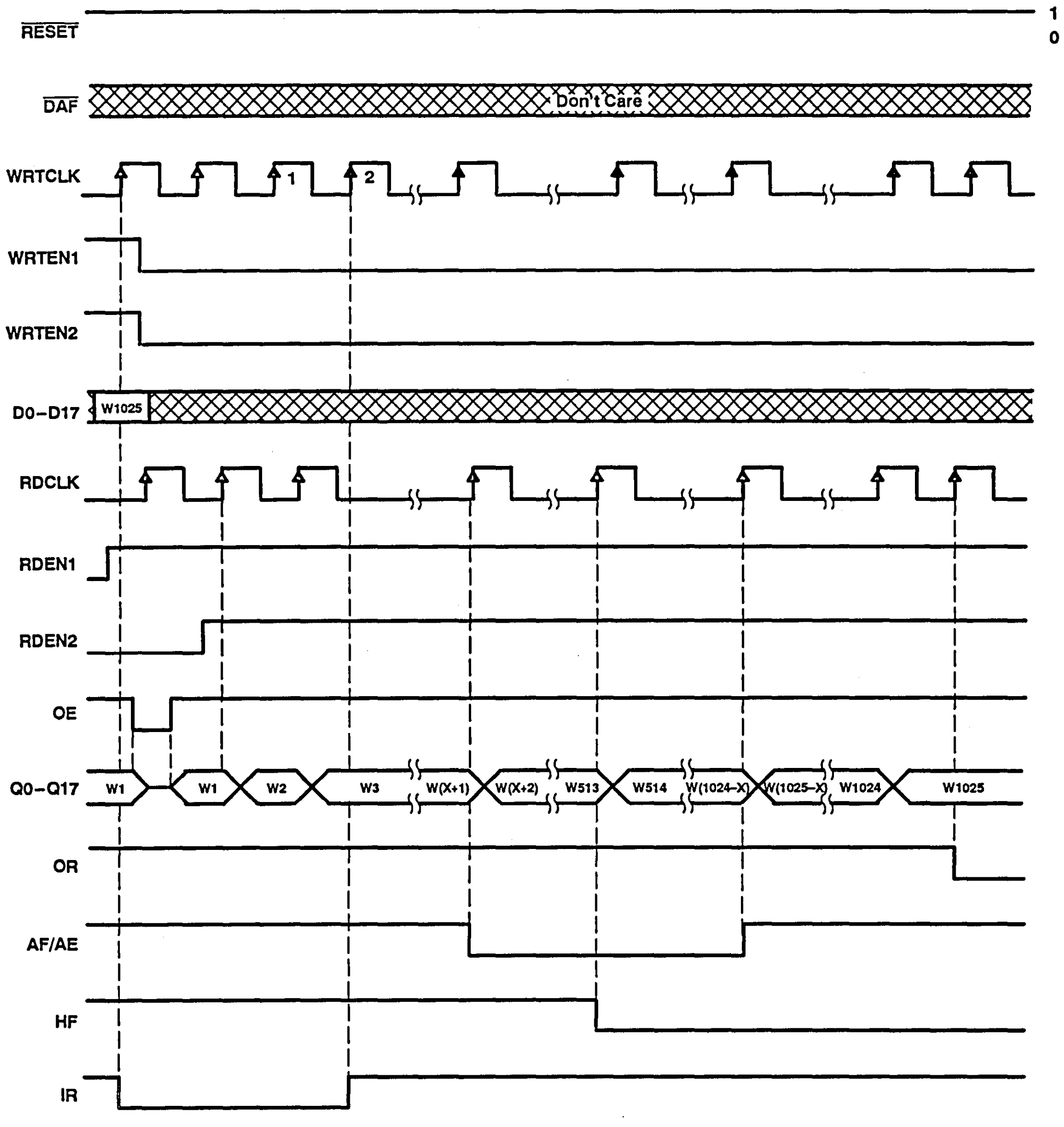


Figure 4. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range, T_A .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP[‡]	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0 V			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0 V			±5	µA
I_{CC}[§]	V_I = V_{CC} – 0.2 V or 0 V				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0 V, f = 1 MHz			4		pF
C_o	V_O = 0 V, f = 1 MHz			8		pF

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] I_{CC} tested with outputs open.

timing requirements (see Figures 1 through 8)

			'ACT7811-15		'ACT7811-18		'ACT7811-20		'ACT7811-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		40		35		28.5		16.7		MHz
t_w	Pulse duration	Data In (D0–D17) high or low	10		12		14		20		ns
		WRTCLK high	7		8.5		10		17		
		WRTCLK low	10		11		14		23		
		RDCLK high	7		8.5		10		17		
		RDCLK low	10		11		14		23		
		$\overline{\text{DAF}}$ high	10		10		10		10		
		WRTEN1, WRTEN2 high or low	10		10		10		10		
		OE, RDEN1, RDEN2 high or low	10		10		10		10		
t_{su}	Setup time	D0–D17 before WRTCLK↑	5		5		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	5		5		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	5		5		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK and RDCLK↑	7		7		7		7		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	5		5		5		5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	7		7		7		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	5		5		5		5		
t_h	Hold time	D0–D17 after WRTCLK↑	1		1		1		1		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	1		1		1		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	1		1		1		1		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK and RDCLK↑	0		0		0		0		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	1		1		1		1		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	1		1		1		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C									UNIT
			'ACT7811-15			'ACT7811-18		'ACT7811-20		'ACT7811-25		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		40			35		28.5		16.7		MHz
t_{pd}	RDCLK↑	Any Q	4	12	15	4	18	4	20	4	25	ns
t_{pd}†				10.5								
t_{pd}	WRTCLK↑	IR	2		10	2	12	2	14	2	16	ns
t_{pd}	RDCLK↑	OR	2		10	2	12	2	14	2	16	ns
t_{pd}	WRTCLK↑	AF/AE	6		20	6	22	6	24	6	26	ns
	RDCLK↑		6		20	6	22	6	24	6	26	
t_{PLH}	WRTCLK↑	HF	6		19	6	21	6	23	6	25	ns
t_{PHL}	RDCLK↑		6		19	6	21	6	23	6	25	
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	3		19	3	21	3	23	3	25	ns
t_{PHL}		HF	4		21	4	23	4	25	4	27	
t_{en}	OE	Any Q	2		11	2	11	2	11	2	11	ns
t_{dis}			2		14	2	14	2	14	2	14	

† This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

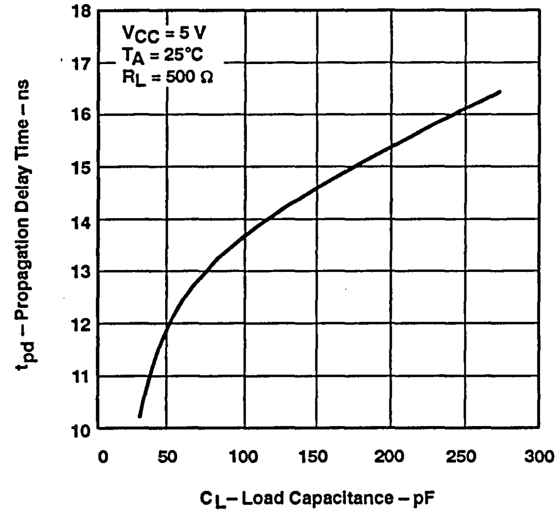


Figure 5

TYPICAL CHARACTERISTICS

TYPICAL POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

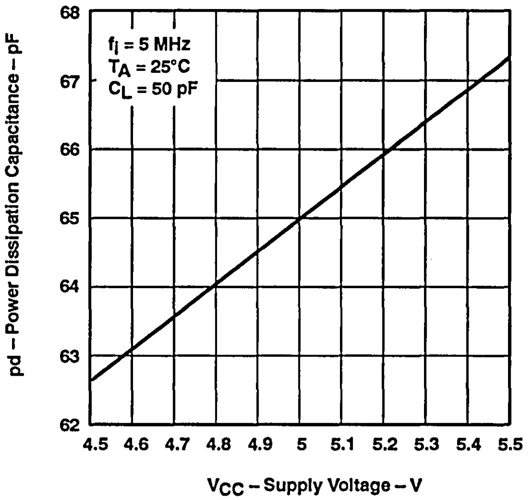


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7811 can be calculated by:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

expanding the SN74ACT7811

The SN74ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

> After the first data word is loaded into the FIFO, the word is unloaded, and the output-ready flag output (OR) goes high after (N × 3) read clock (RDCLK) cycles, where N is the number of devices used in depth expansion.
>
> After the FIFO is filled, the input-ready flag output (IR) goes low, the first word is unloaded, and the IR flag output is driven high after (N × 2) write clock cycles, where N is the number of devices used in depth expansion.

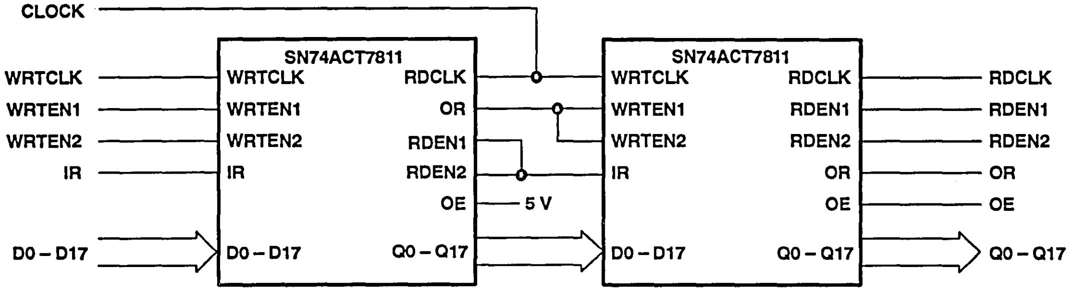


Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2

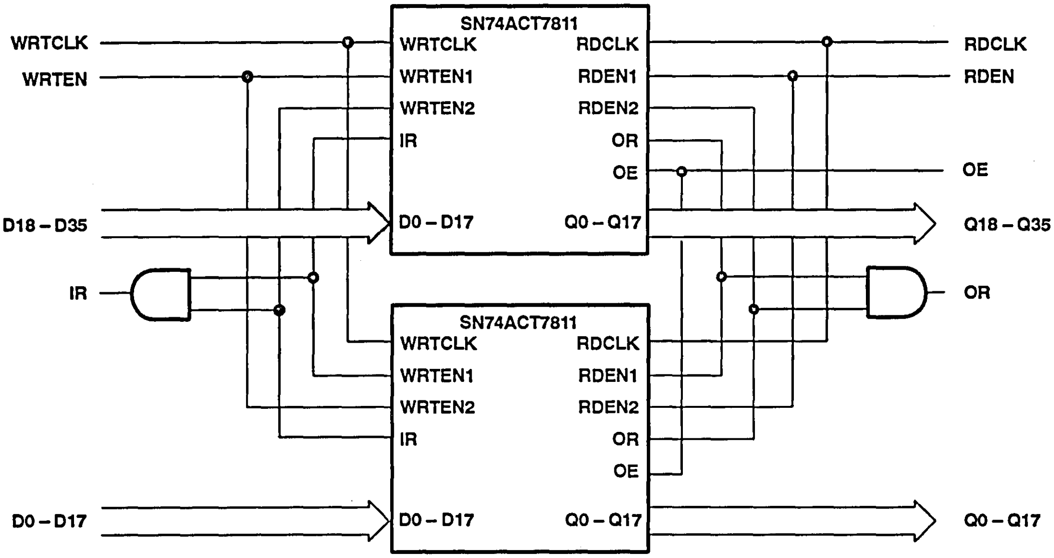
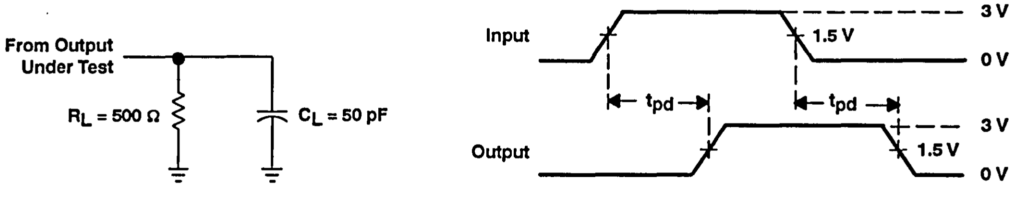


Figure 8. Word-Width Expansion: 1024 Words × 36 Bits

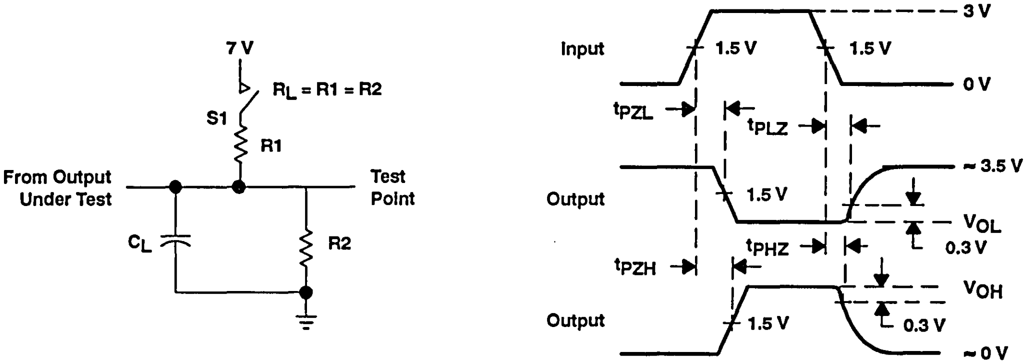
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 9. Standard CMOS Outputs



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

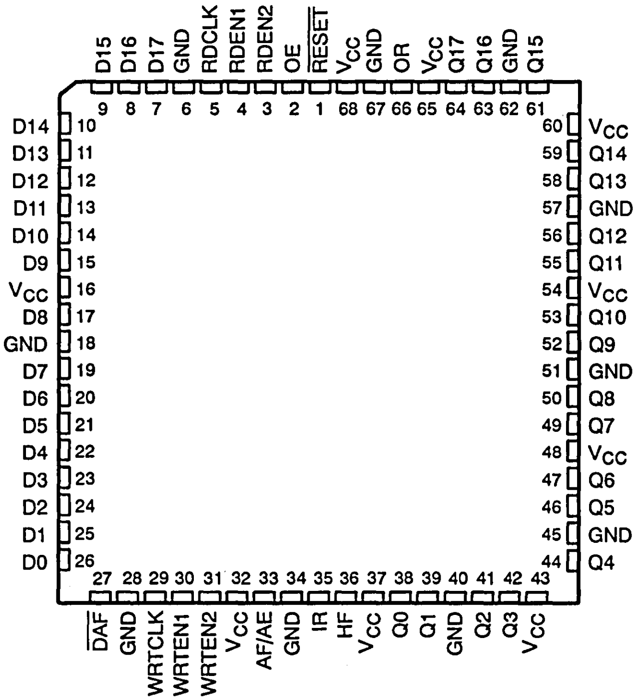
Figure 10. 3-State Outputs (Any Q)

SN74ACT7881
1024 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS227A – FEBRUARY 1993 – REVISED JUNE 1994

- Member of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost-Full/Almost-Empty Flag
- Pin-to-Pin Compatible With SN74ACT7882, SN74ACT7884, and SN74ACT7811
- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 11 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat (PN) Packages

FN PACKAGE
(TOP VIEW)



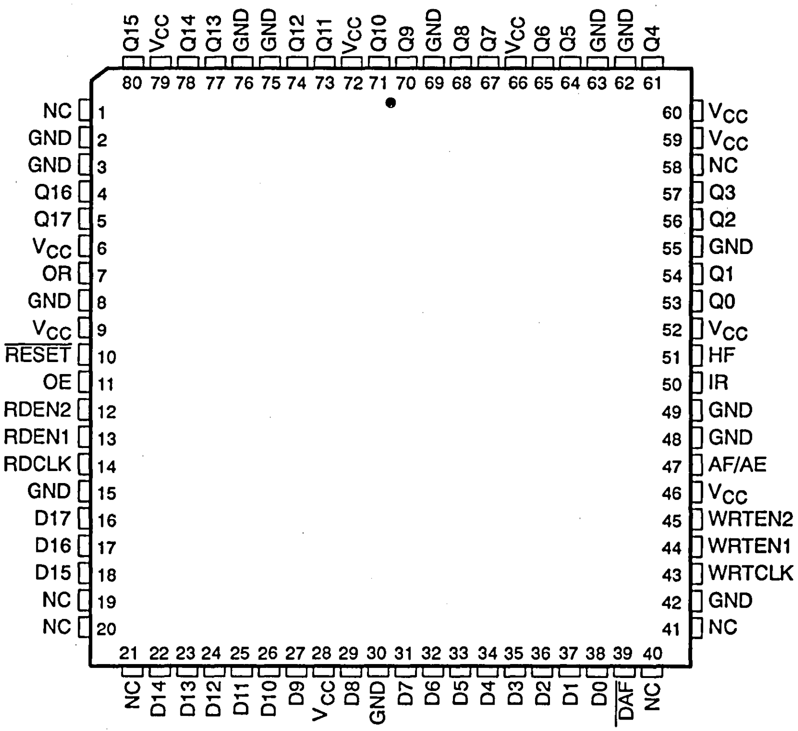
PRODUCT PREVIEW

Widebus is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

PRODUCT PREVIEW

PN PACKAGE
(TOP VIEW)



NC – No internal connection

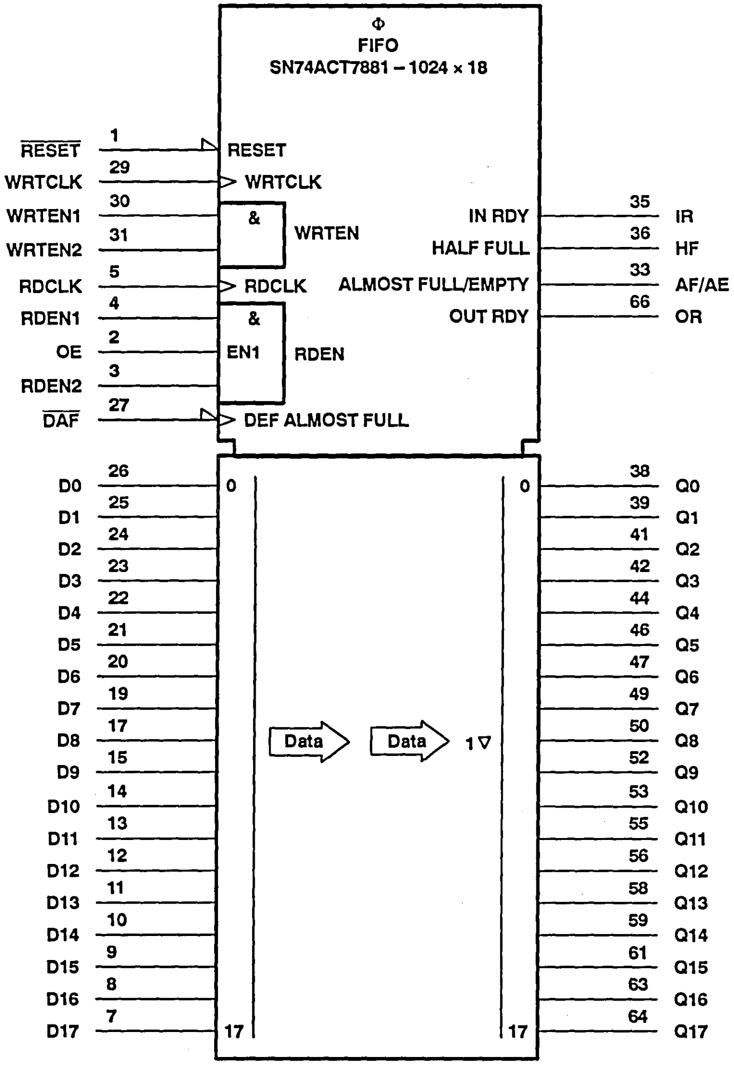
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7881 is organized as 1024 × 18 bits. The SN74ACT7881 processes data at rates up to 67 MHz and access times of 11 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7881 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

The SN74ACT7881 is characterized for operation from 0°C to 70°C.

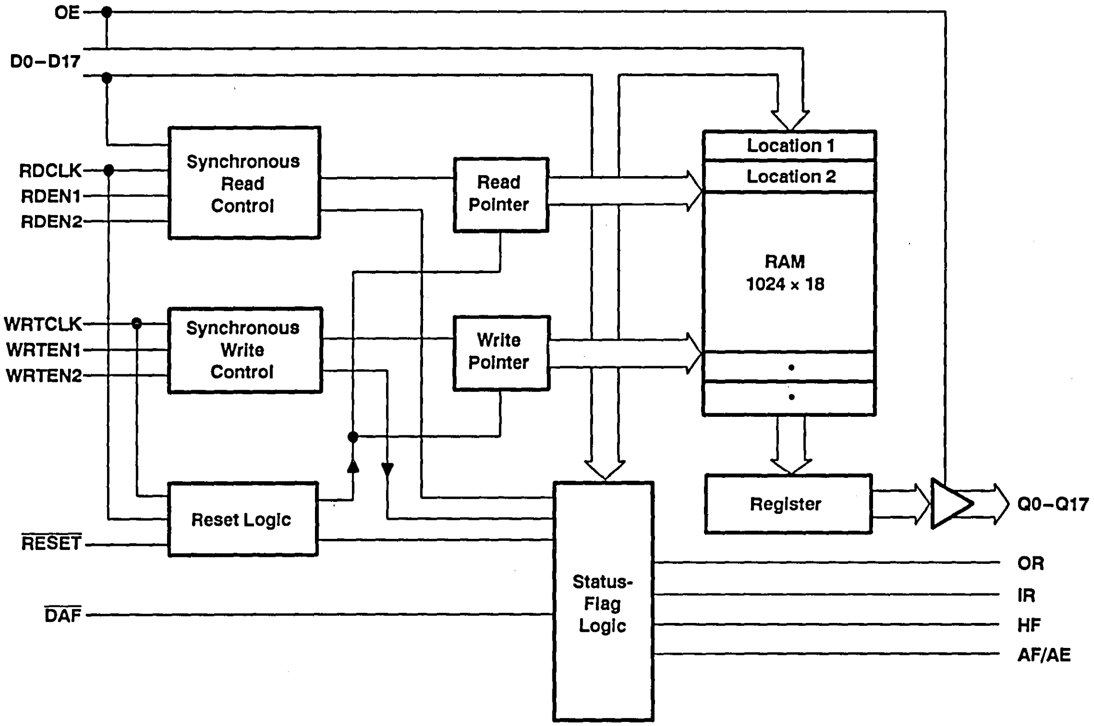
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

PRODUCT PREVIEW

functional block diagram



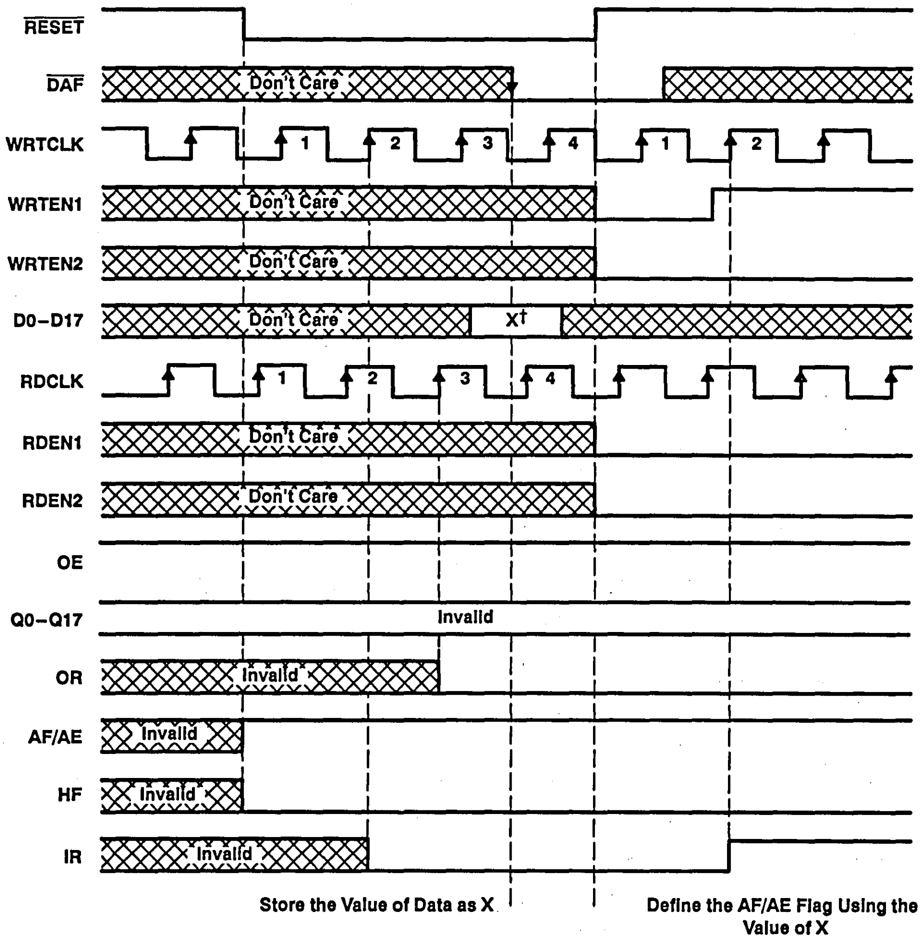
PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the number of words in memory is less than or equal to X. AF/AE is also high when the number of words in memory is greater than or equal to (1024 – X). Programming procedure for AF/AE is programmed during each reset cycle. The almost-full/almost empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: <u>User-defined X</u> Step 1: Take $\overline{\text{DAF}}$ from high to low. The low-to-high transition of $\overline{\text{DAF}}$ input stores the binary value on the data inputs as X. The following bits are used, listed from most significant bit to least significant bit (D8 – D0). Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. <u>Default X</u> To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	27	I	Define-almost-full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the almost-full/almost-empty (AF/AE) flag using X.
D0 – D17	26 – 19, 17, 15 – 7	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition on $\overline{\text{DAF}}$ captures data for the almost-empty/almost-full offset (X) from D8 – D0.
HF	36	O	Half-full flag. HF is high when the FIFO contains 512 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The Q0 – Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0 – Q17	38 – 39, 41 – 42, 44, 46 – 47, 49 – 50, 52 – 53, 55 – 56, 58 – 59, 61, 63 – 64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0 – Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on the low-to-high transition at RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to the RDCLK signal.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, IR are low, AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).



† X is the binary value on D8–D0.

Figure 1. Reset Cycle: Define AF/AE Using a Programmed Value of X

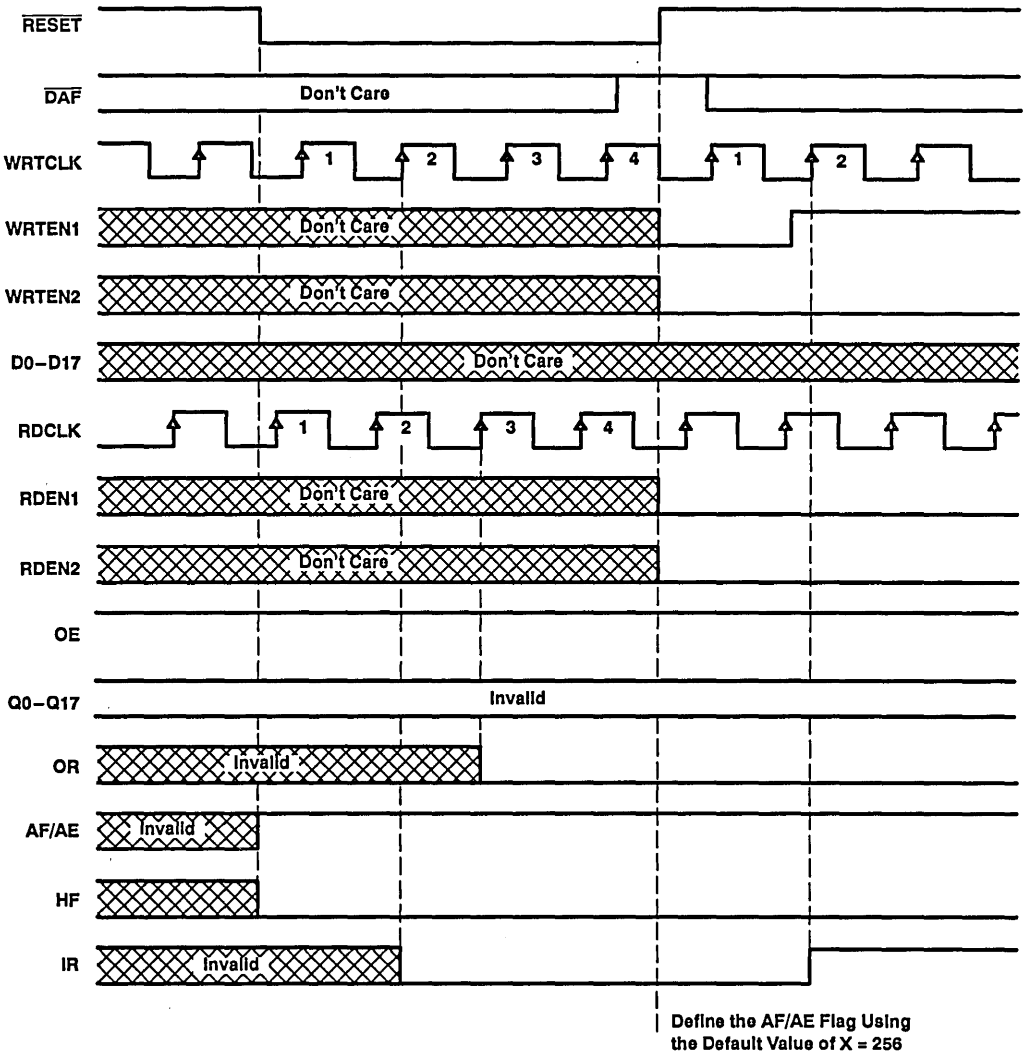
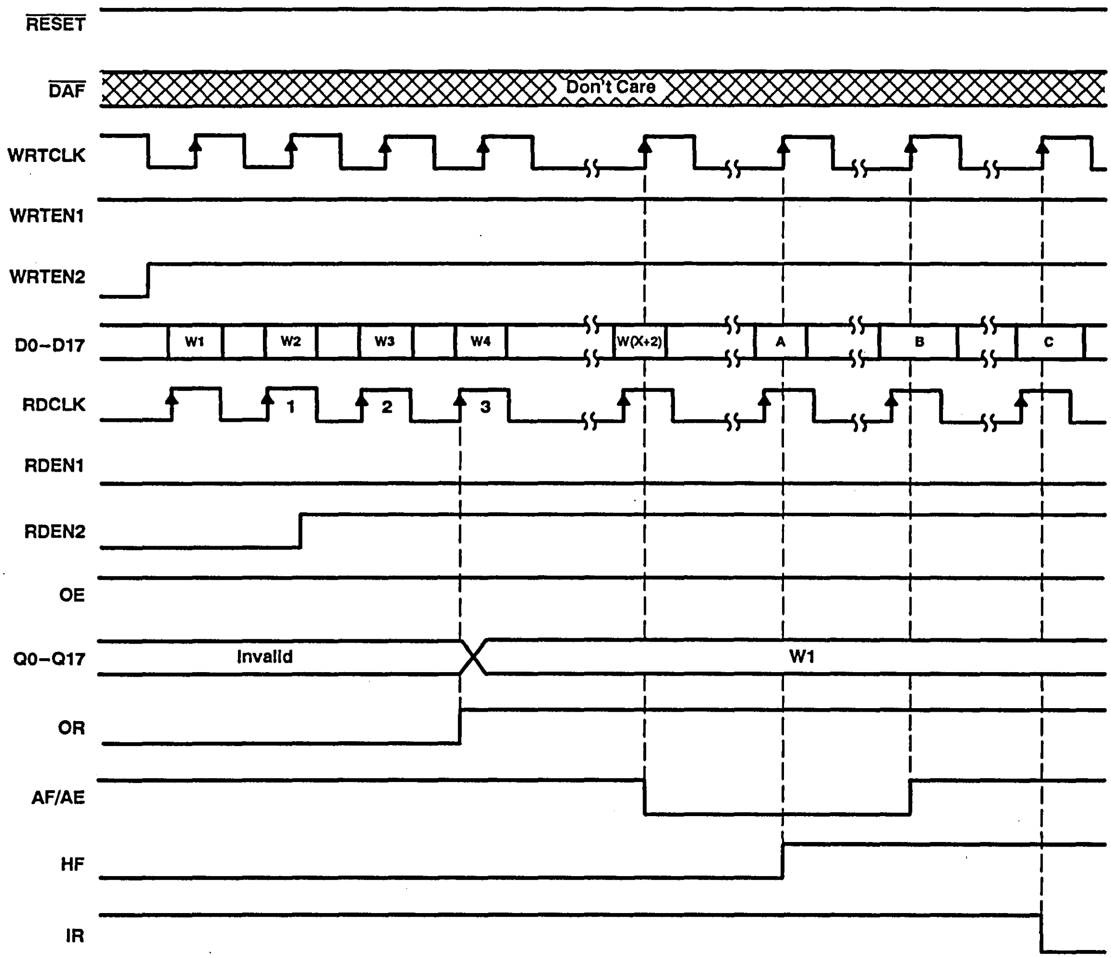


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

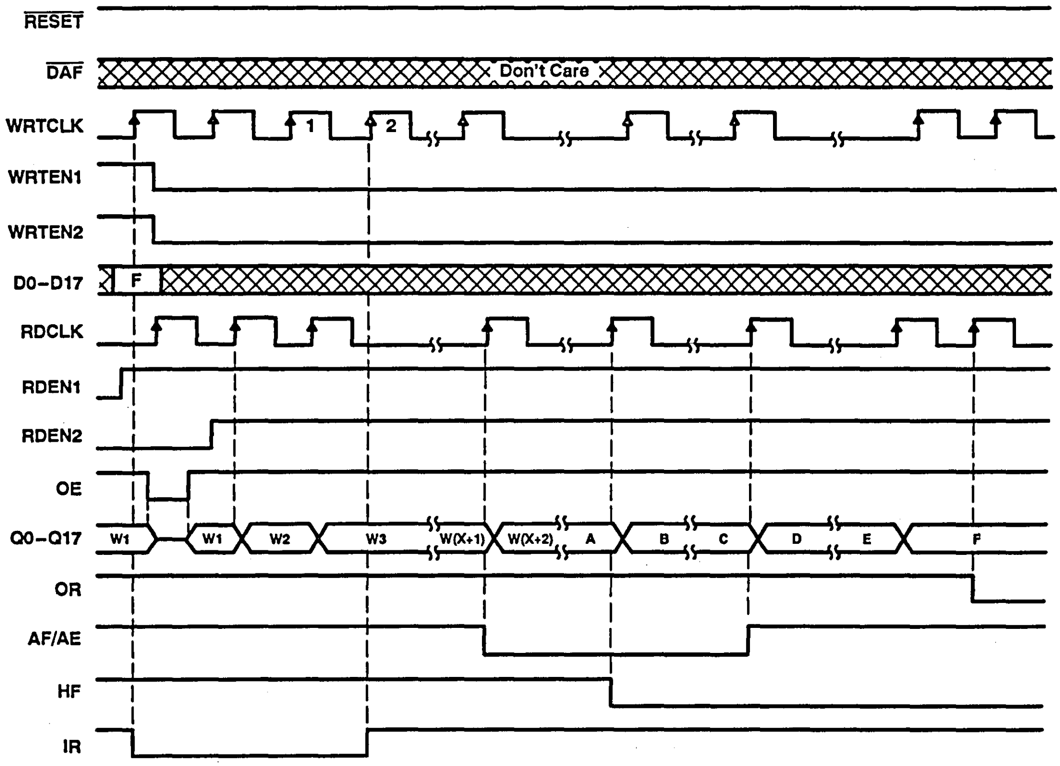


PRODUCT PREVIEW

DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	B	C
W513	W(1025 – X)	W1025

Figure 3. Write



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	B	C	D	E	F
W513	W514	W(1024 – X)	W(1025 – X)	W1024	W1025

Figure 4. Read

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP[‡]	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	μA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	μA
I_{CC}[§]	V_I = V_{CC} − 0.2 V or 0				400	μA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_o	V_O = 0,	f = 1 MHz		8		pF

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] I_{CC} tested with outputs open.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 4)

			'ACT7881-15		'ACT7881-20		'ACT7881-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		33.4		MHz
t_w	Pulse duration	WRTCLK high	6		7		8.5		ns
		WRTCLK low	6		7		11		
		RDCLK high	6		7		8.5		
		RDCLK low	6		7		11		
		$\overline{\text{DAF}}$ high	6		7		10		
t_{su}	Setup time	D0–D17 before WRTCLK↑	4		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	4		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	4		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑†	5		6		7		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	4		5		5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	5		6		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	4		5		5		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		0		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	0		0		1		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑†	0		0		0		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	0		0		1		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	0		0		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7881-15		'ACT7881-20		'ACT7881-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67		50		33.4		MHz
t_{pd}	RDCLK↑	Any Q	4	11	4	13	4	18	ns
t_{pd}‡									
t_{pd}	WRTCLK↑	IR	2	9	2	9.5	2	12	ns
t_{pd}	RDCLK↑	OR	2	9	2	9.5	2	12	
t_{pd}	WRTCLK↑	AF/AE	6	17	6	19	6	22	ns
	RDCLK↑		6	17	6	19	6	22	
t_{PLH}	WRTCLK↑	HF	6	15	6	17	6	21	ns
t_{PHL}	RDCLK↑		6	15	6	17	6	21	
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	3	16	3	17	3	21	ns
t_{PHL}		HF	4	18	4	19	4	23	
t_{en}	OE	Any Q	2	11	2	11	2	11	ns
t_{dis}			2	14	2	14	2	14	

‡ This parameter is measured with C_L = 30 pF (see Figure 5).

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

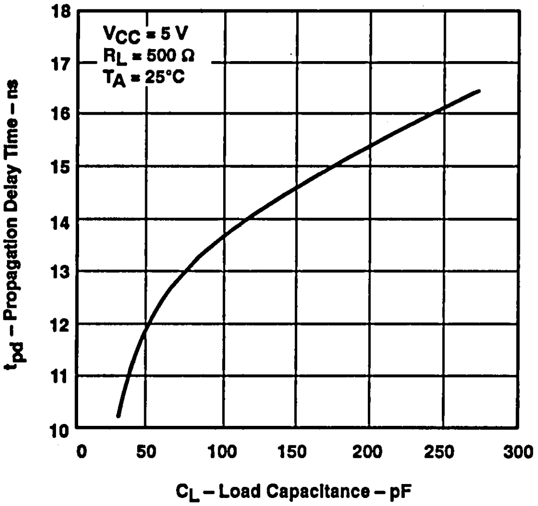


Figure 5

TYPICAL CHARACTERISTICS

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

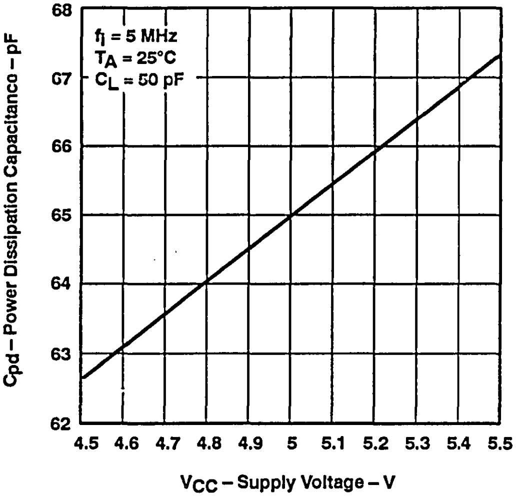


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7881 can be calculated using:

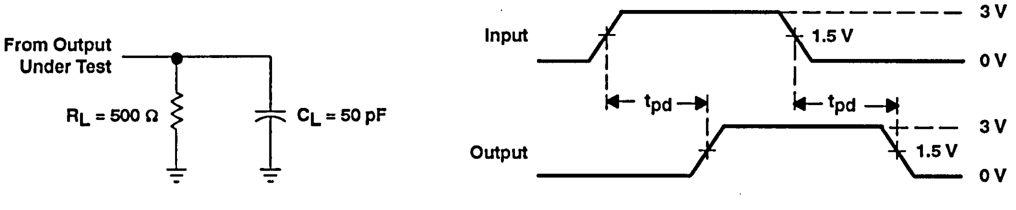
$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \sum(C_{pd} \times V_{CC}^2 \times f_i) + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

PRODUCT PREVIEW

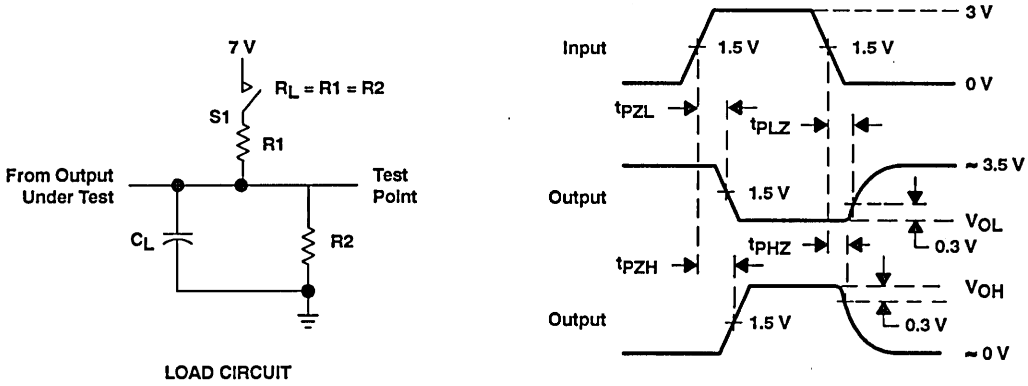
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 7. Standard CMOS Outputs



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 8. 3-State Outputs (Any Q)

APPLICATION INFORMATION

expanding the SN74ACT7881

The SN74ACT7881 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 9 shows two SN74ACT7881 devices configured for depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready flag (OR) of the previous device and the input-ready flag (IR) of the next device maintain data flow to the last device in the chain whenever space is available.

Figure10 is an example of two SN74ACT7881 devices in word-width expansion. Width expansion is accomplished by simply connecting all common control signals between the devices and creating composite input-ready (IR) and output-ready (OR) signals. The almost-full/almost-empty flag (AF/AE) and half-full flag (HF) can be sampled from any one device. Depth expansion and width expansion can be used together.

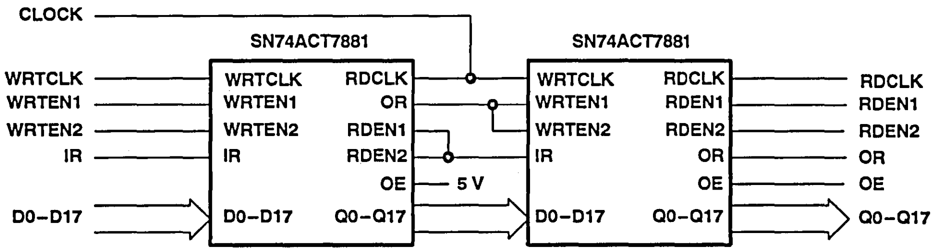


Figure 9. Word-Depth Expansion: 2048/4096/8192 Words × 18 Bits, N = 2

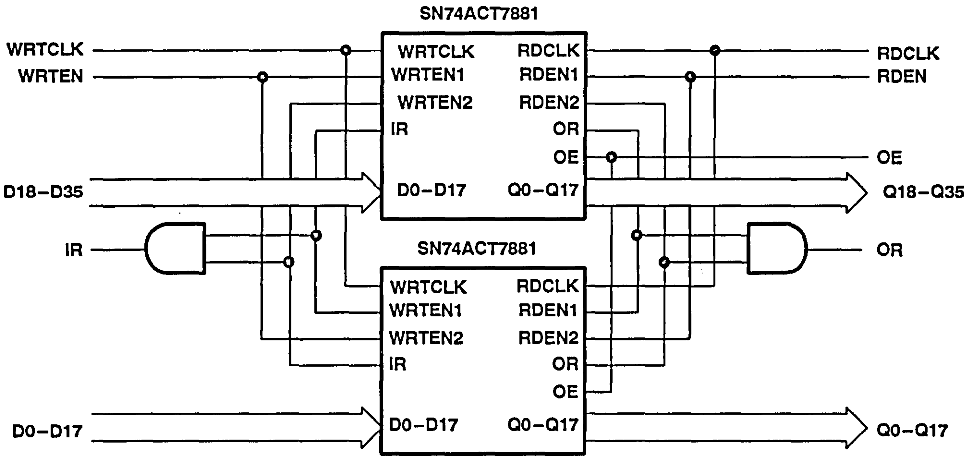


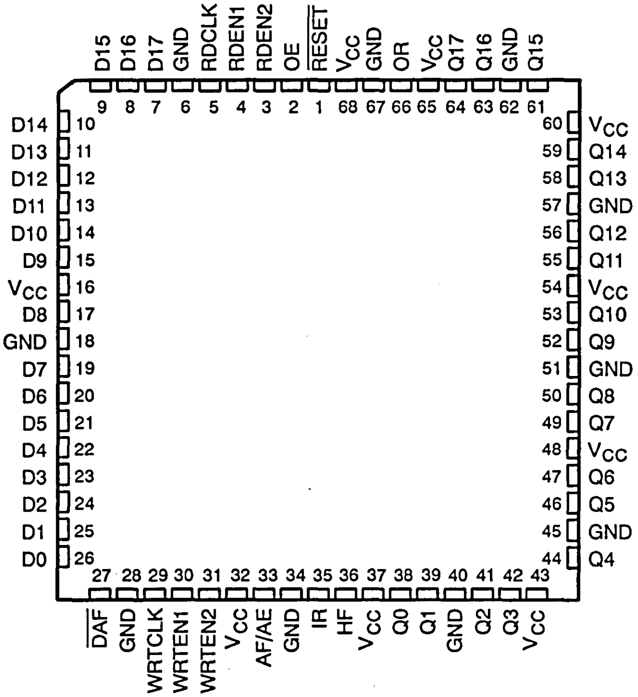
Figure 10. Word-Depth Expansion: 1024 Words × 36 Bits

SN74ACT7882
2048 × 18 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS445 – JUNE 1994

- **Member of the Texas Instruments Widebus™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **Read and Write Operations Can Be Synchronized to Independent System Clocks**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7884, and SN74ACT7811**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 11 ns With a 50-pF Load**
- **High Output Drive for Direct Bus Interface**
- **Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat (PN) Packages**

FN PACKAGE
(TOP VIEW)

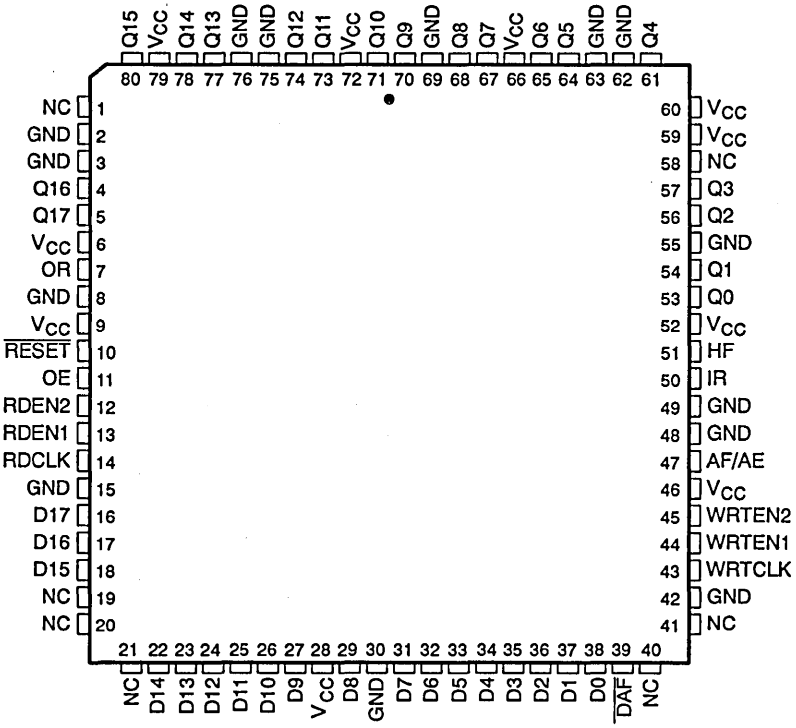


PRODUCT PREVIEW

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

PN PACKAGE
(TOP VIEW)



NC – No internal connection

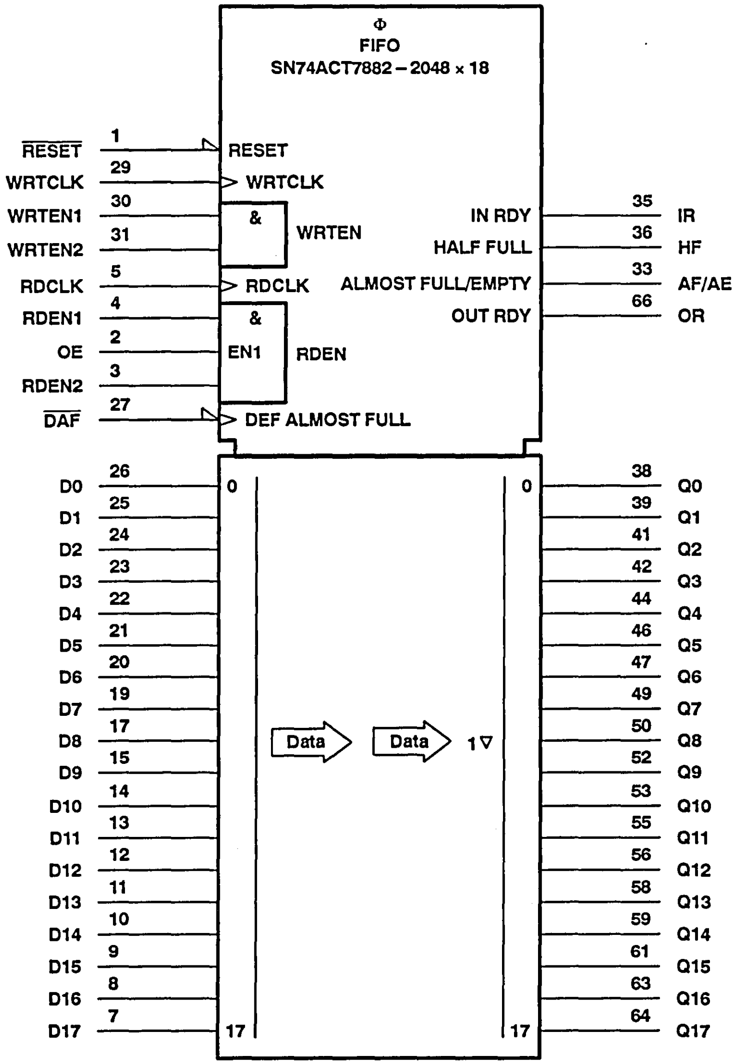
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7882 is organized as 2048 × 18 bits. The SN74ACT7882 processes data at rates up to 67 MHz and access times of 11 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7882 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

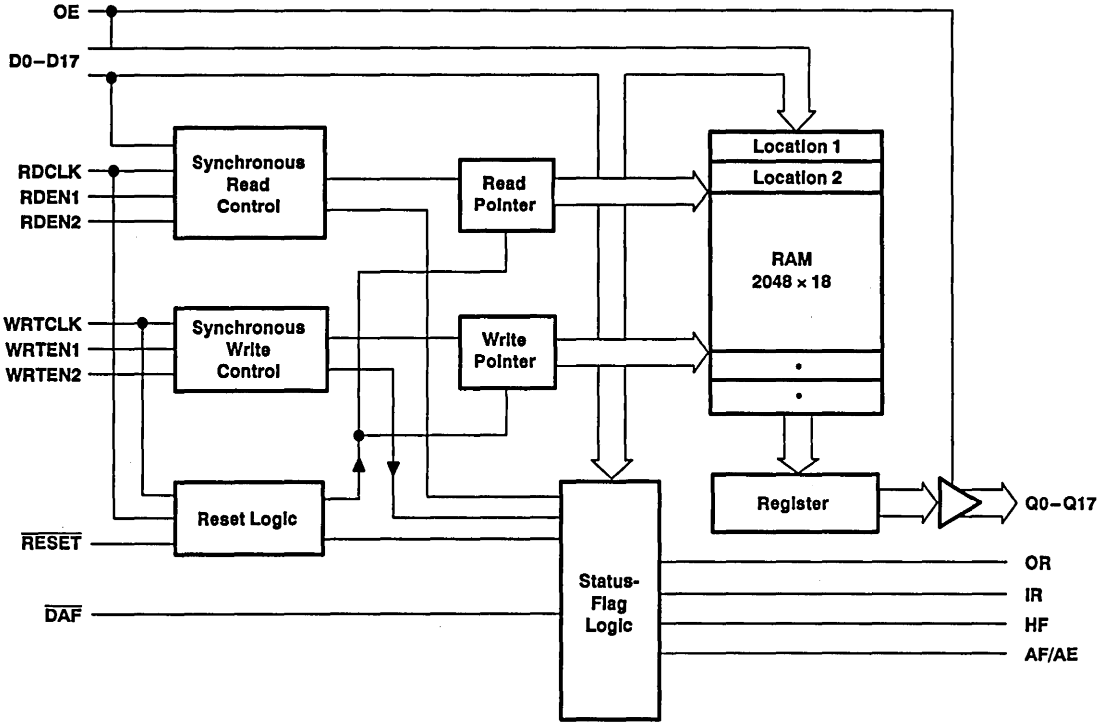
The SN74ACT7882 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



PRODUCT PREVIEW

Terminal Functions

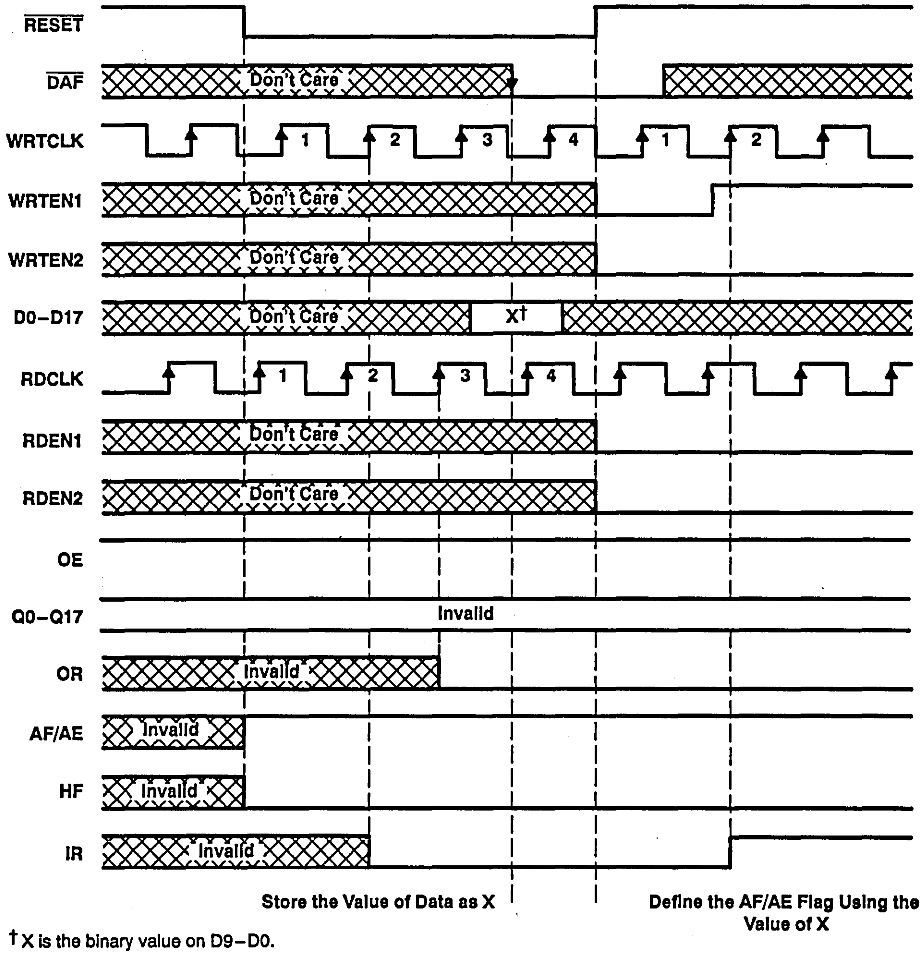
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the number of words in memory is less than or equal to X. AF/AE is also high when the number of words in memory is greater than or equal to (2048 – X). Programming procedure for AF/AE is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: <u>User-defined X</u> Step 1: Take $\overline{\text{DAF}}$ from high to low. The low-to-high transition of $\overline{\text{DAF}}$ input stores the binary value on the data inputs as X. The following bits are used, listed from most significant bit to least significant bit D9–D0. Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. <u>Default X</u> To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	27	I	Define-almost-full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the almost-full/almost-empty (AF/AE) flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition on $\overline{\text{DAF}}$ captures data for the almost-empty/almost-full offset (X) from D9–D0.
HF	36	O	Half-full flag. HF is high when the FIFO contains 1024 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The Q0–Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data out. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on the low-to-high transition at RDCLK if OR, OE, and RDEN1 and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low, and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines the AF/AE flag using the default value of X = 256.

PRODUCT PREVIEW

PRODUCT PREVIEW

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).



† X is the binary value on D9–D0.

Figure 1. Reset Cycle: Define AF/AE Using a Programmed Value of X

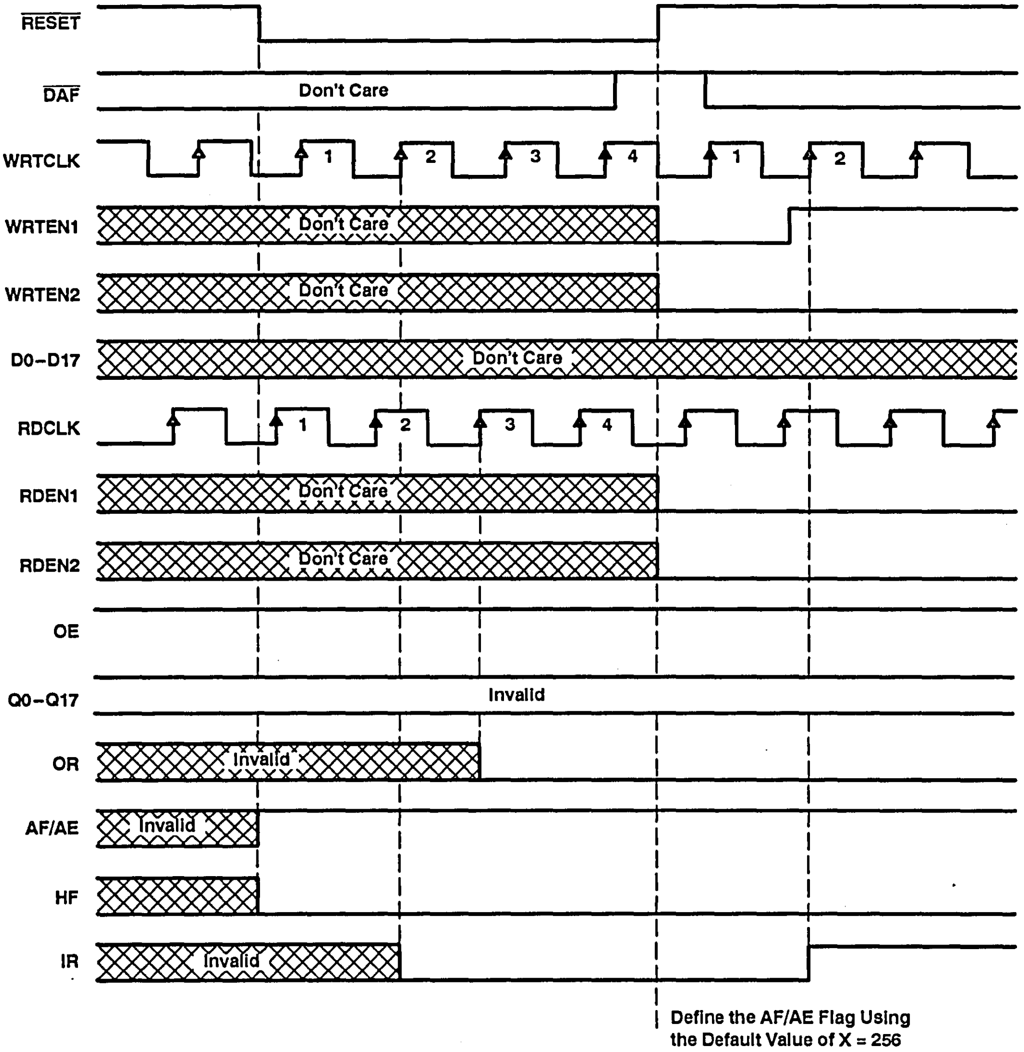
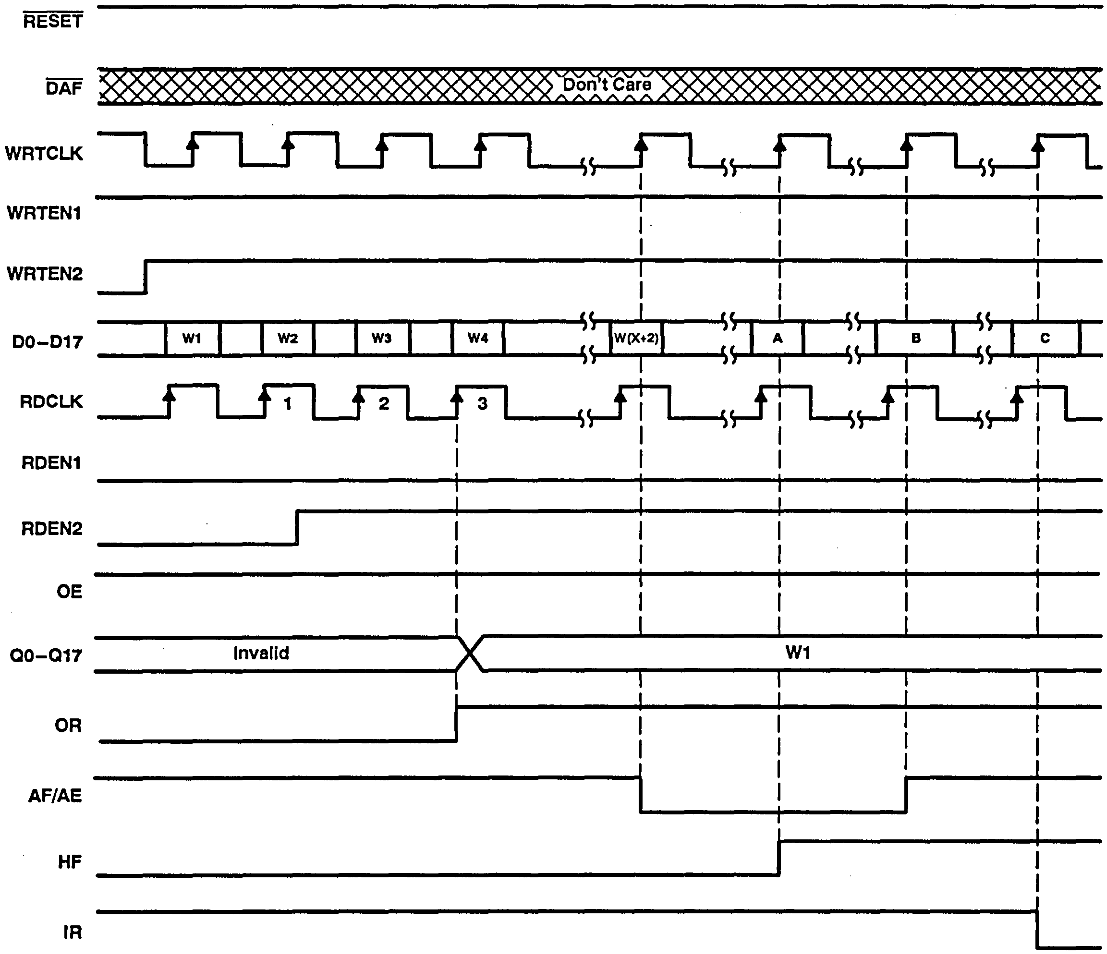


Figure 2. Reset Cycle: Define AF/AE Using the Default Value

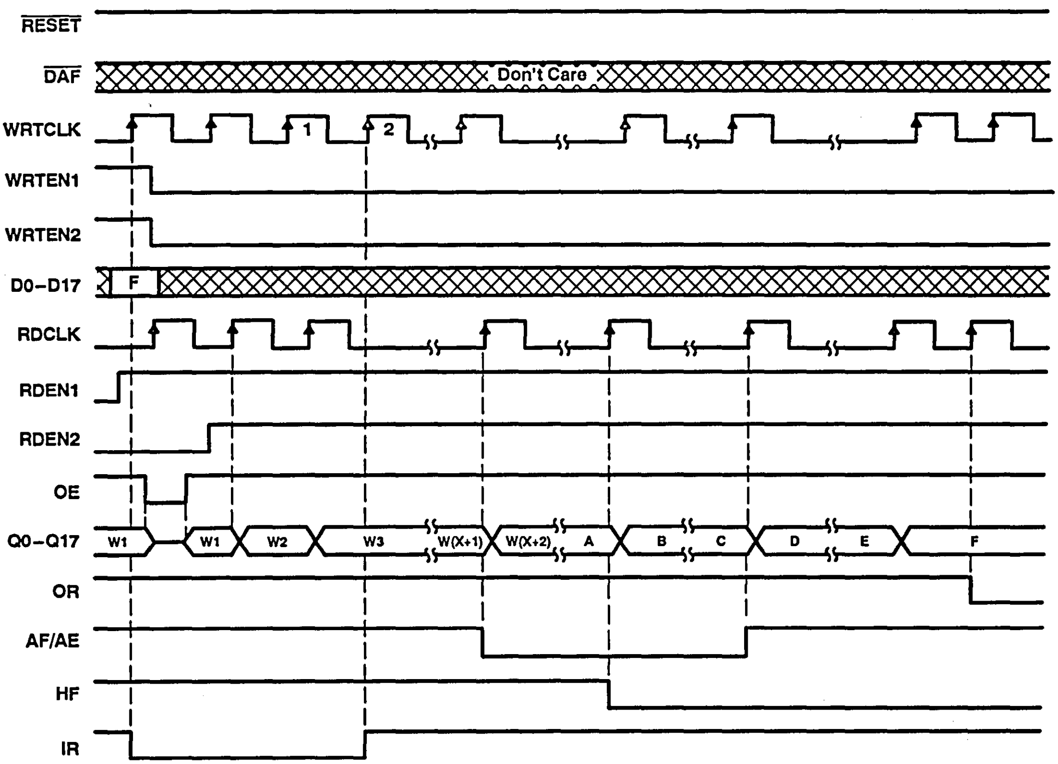
PRODUCT PREVIEW



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	B	C
W1025	W(2049 – X)	W2049

Figure 3. Write



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	B	C	D	E	F
W1025	W1030	W(2048 – X)	W(2049 – X)	W2048	W2049

Figure 4. Read

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range[†]

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP[‡]	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	µA
I_{CC}[§]	V_I = V_{CC} – 0.2 V or 0				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_o	V_O = 0,	f = 1 MHz		8		pF

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] I_{CC} tested with outputs open.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 4)

			'ACT7882-15		'ACT7882-20		'ACT7882-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		33.4		MHz
t_w	Pulse duration	WRTCLK high	6		7		8.5		ns
		WRTCLK low	6		7		11		
		RDCLK high	6		7		8.5		
		RDCLK low	6		7		11		
		$\overline{\text{DAF}}$ high	6		7		10		
t_{su}	Setup time	Data in (D0–D17) before WRTCLK↑	4		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	4		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	4		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑†	5		6		7		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	4		5		5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	5		6		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	4		5		5		
t_h	Hold time	Data in (D0–D17) after WRTCLK↑	0		0		0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		0		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	0		0		1		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑†	0		0		0		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	0		0		1		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	0		0		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7882-15		'ACT7882-20		'ACT7882-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67		50		33.4		MHz
t_{pd}	RDCLK↑	Any Q	4	11	4	13	4	18	ns
t_{pd}‡									
t_{pd}	WRTCLK↑	IR	2	9	2	9.5	2	12	ns
t_{pd}	RDCLK↑	OR	2	9	2	9.5	2	12	
t_{pd}	WRTCLK↑	AF/AE	6	17	6	19	6	22	ns
	RDCLK↑		6	17	6	19	6	22	
t_{PLH}	WRTCLK↑	HF	6	15	6	17	6	21	ns
t_{PHL}	RDCLK↑		6	15	6	17	6	21	
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	3	16	3	17	3	21	ns
t_{PHL}		HF	4	18	4	19	4	23	
t_{en}	OE	Any Q	2	11	2	11	2	11	ns
t_{dis}			2	14	2	14	2	14	

‡ This parameter is measured with C_L = 30 pF (see Figure 5).

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

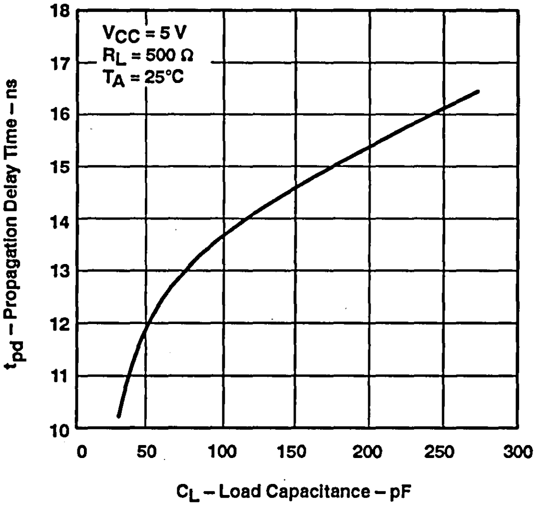


Figure 5

TYPICAL CHARACTERISTICS

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

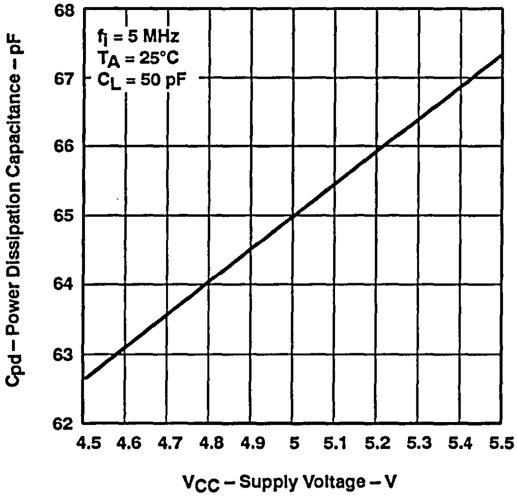


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7882 can be calculated using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \sum(C_{pd} \times V_{CC}^2 \times f_i) + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

PARAMETER MEASUREMENT INFORMATION

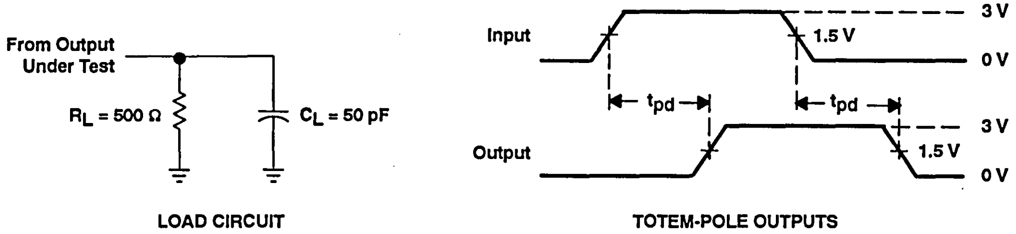
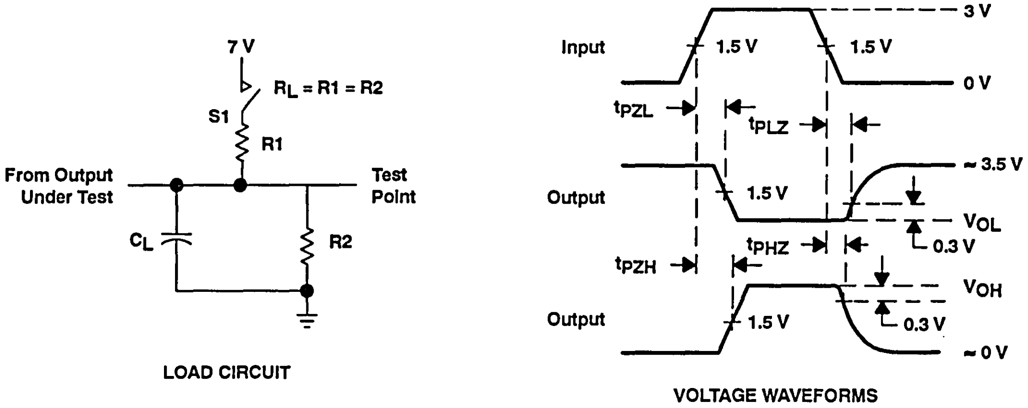


Figure 7. Standard CMOS Outputs



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 8. 3-State Outputs (Any Q)

PRODUCT PREVIEW

APPLICATION INFORMATION

expanding the SN74ACT7882

The SN74ACT7882 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 9 shows two SN74ACT7882 devices configured for depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready flag (OR) of the previous device and the input-ready flag (IR) of the next device maintain data flow to the last device in the chain whenever space is available.

Figure 10 is an example of two SN74ACT7882 devices in word-width expansion. Width expansion is accomplished by simply connecting all common control signals between the devices and creating composite input-ready (IR) and output-ready (OR) signals. The almost-full/almost-empty flag (AF/AE) and half-full flag (HF) can be sampled from any one device. Depth expansion and width expansion can be used together.

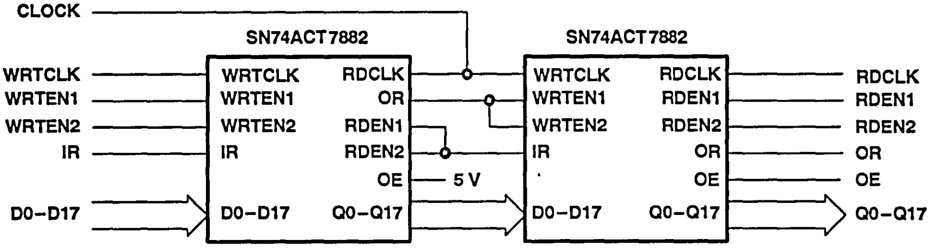


Figure 9. Word-Depth Expansion: 2048/4096/8192 Words × 18 Bits, N = 2

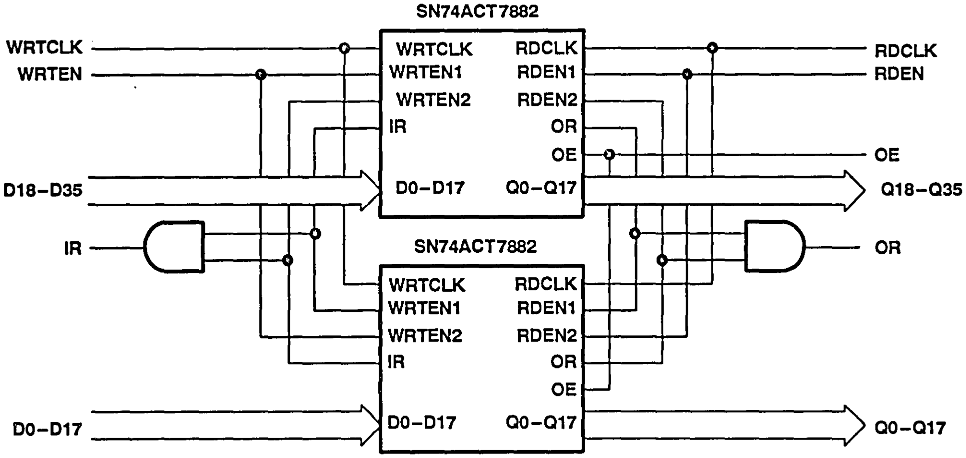


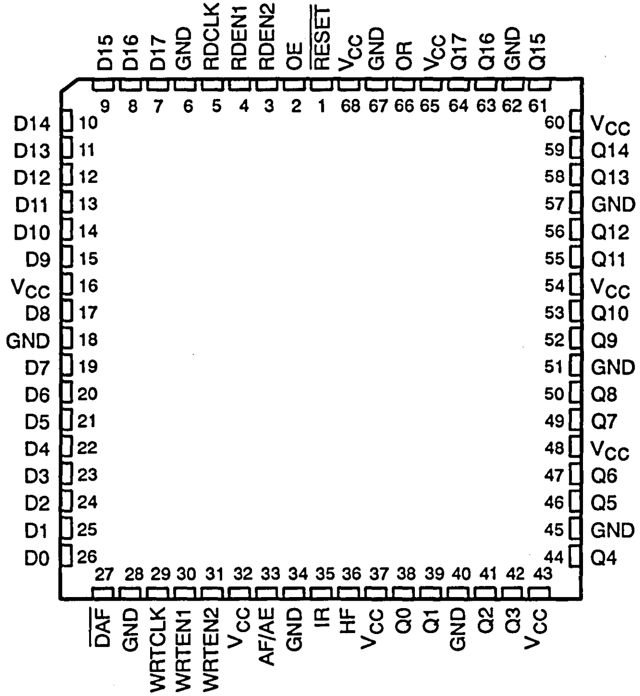
Figure 10. Word-Depth Expansion: 2048 Words × 36 Bits

PRODUCT PREVIEW

SCAS444 – JUNE 1994

- Members of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost-Full/Almost-Empty Flag
- Pin-to-Pin Compatible With SN74ACT7881, SN74ACT7882, and SN74ACT7811
- Input-Ready, Output-Ready, and Half-Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 11 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat (PN) Packages

FN PACKAGE
(TOP VIEW)

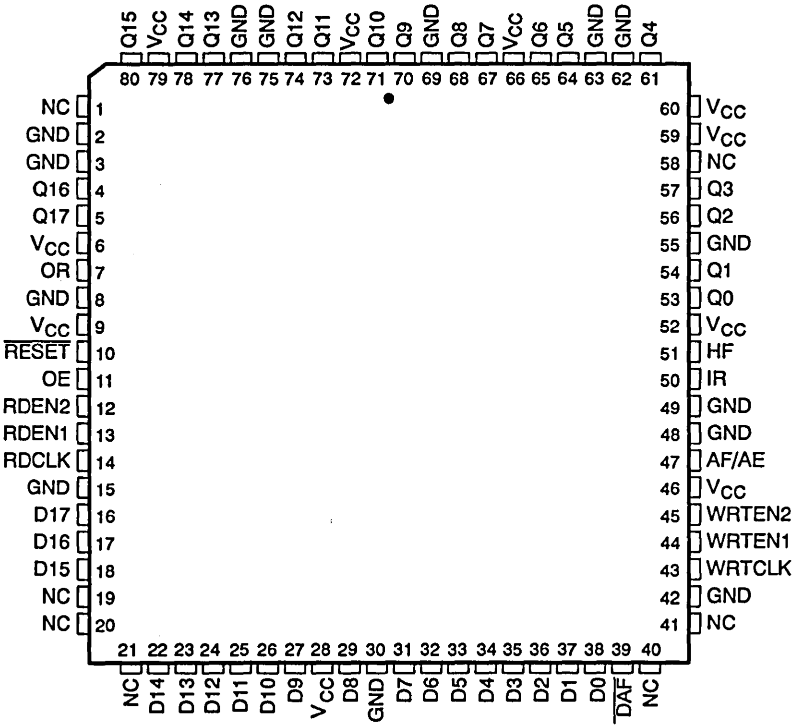


PRODUCT PREVIEW

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

PN PACKAGE
(TOP VIEW)



NC – No internal connection

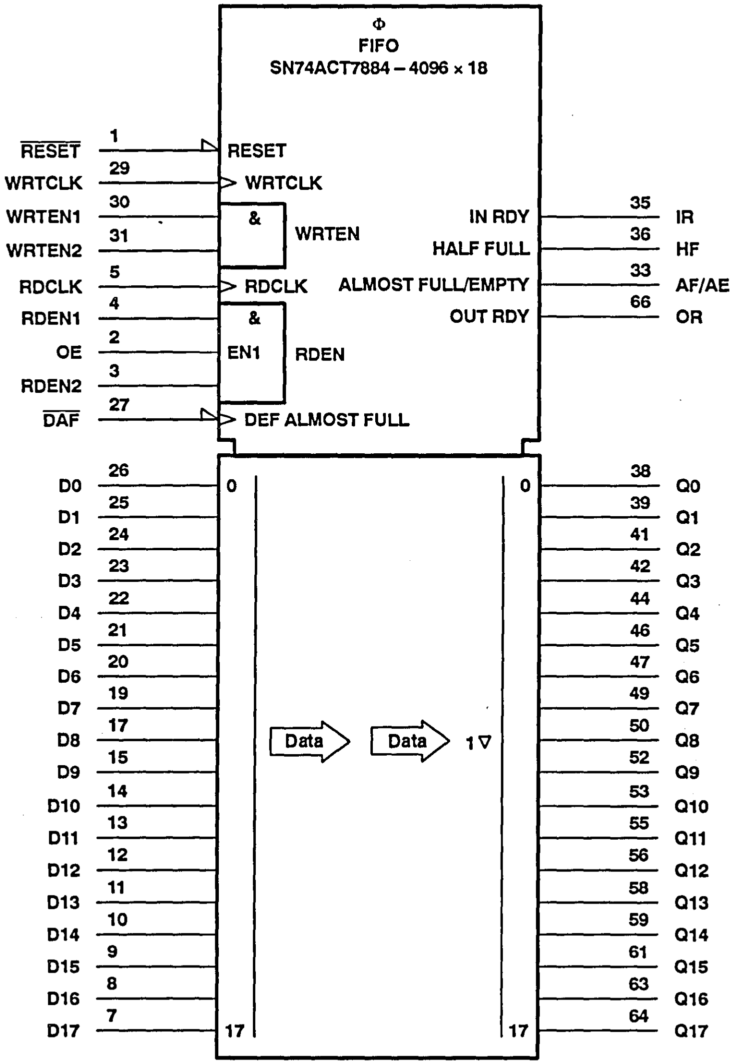
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7884 is organized as 4096 × 18 bits. The SN74ACT7884 processes data at rates up to 67 MHz and access times of 11 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7884 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

The SN74ACT7884 is characterized for operation from 0°C to 70°C.

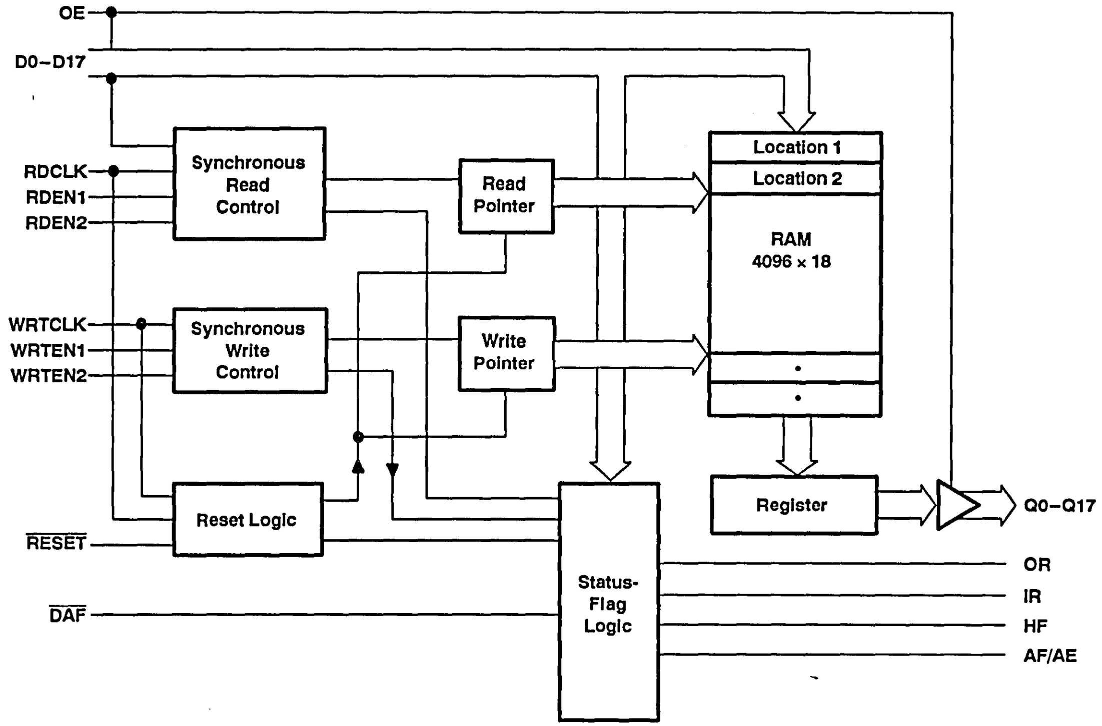
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

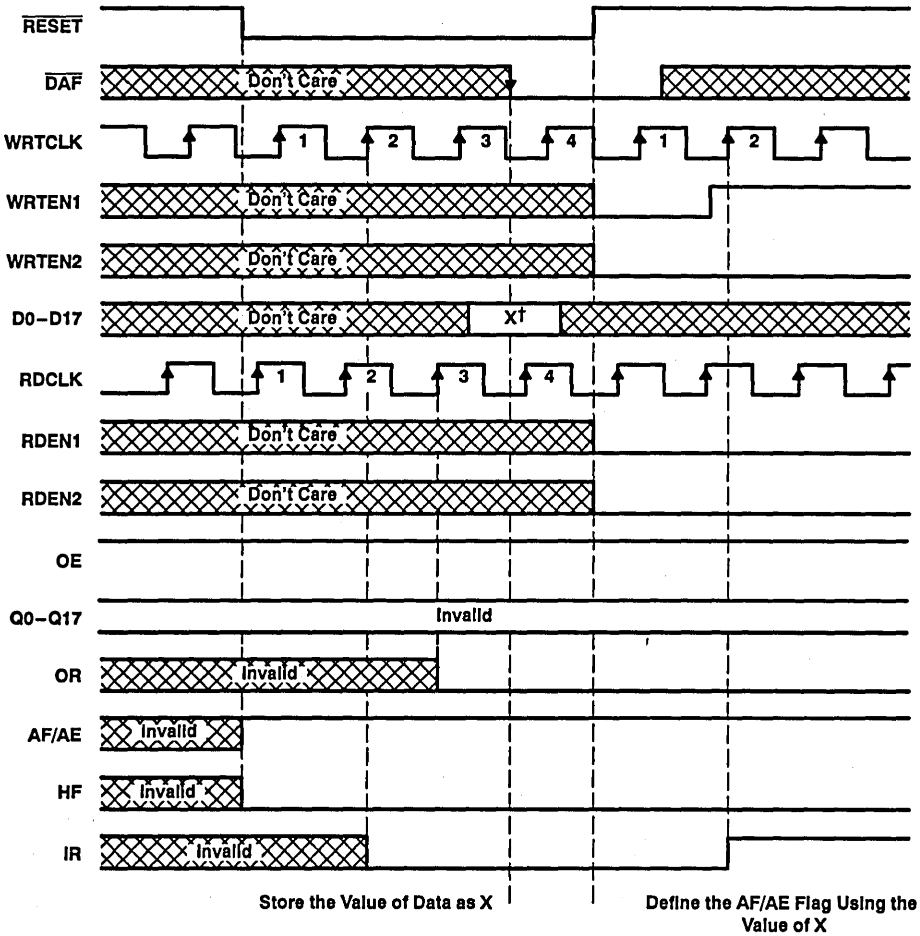
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the number of words in memory is less than or equal to X. AF/AE is also high when the number of words in memory is greater than or equal to (4096 – X). Programming procedure for AF/AE is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: User-defined X Step 1: Take $\overline{\text{DAF}}$ from high to low. The low-to-high transition of $\overline{\text{DAF}}$ stores the binary value on the data inputs as X. The following bits are used, listed from most significant bit to least significant bit D10–D0. Step 2: If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low. Step 3: With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low. Default X To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.
$\overline{\text{DAF}}$	27	I	Define-almost-full. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{\text{DAF}}$ held low, a low pulse on $\overline{\text{RESET}}$ defines the almost-full/almost-empty (AF/AE) flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition on $\overline{\text{DAF}}$ captures data for the almost-empty/almost-full offset (X) from D10–D0.
HF	36	O	Half-full flag. HF is high when the FIFO contains 2048 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{\text{RESET}}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The Q0–Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data out. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on the low-to-high transition at RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{\text{RESET}}$	1	I	Reset. A reset is accomplished by taking $\overline{\text{RESET}}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low, and AF/AE is high. The FIFO must be reset upon power up. With $\overline{\text{DAF}}$ at a low level, a low pulse on $\overline{\text{RESET}}$ defines AF/AE using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{\text{DAF}}$ at a high level, a low-level pulse on $\overline{\text{RESET}}$ defines AF/AE using the default value of X = 256.

PRODUCT PREVIEW

Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).



† X is the binary value on D10–D0.

Figure 1. Reset Cycle: Define AF/AE Using a Programmed Value of X

PRODUCT PREVIEW

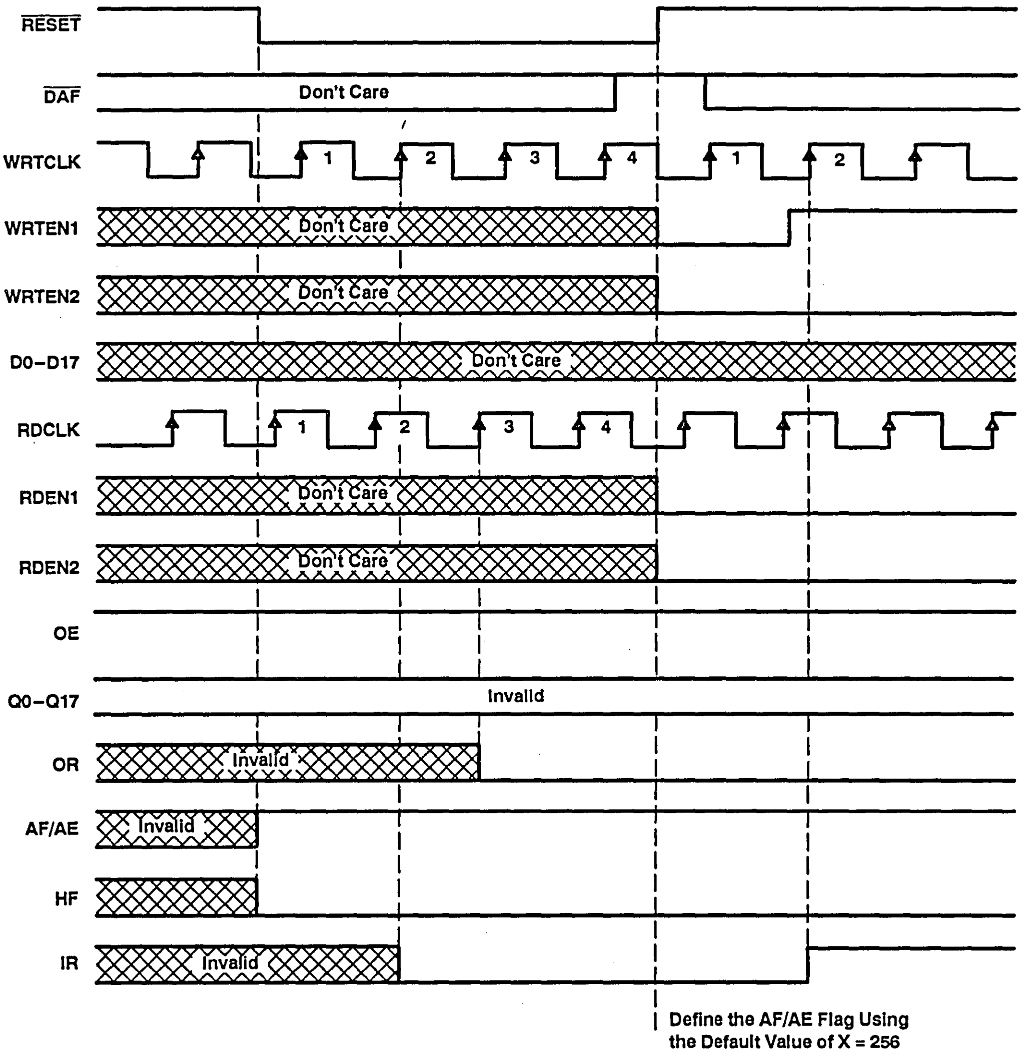
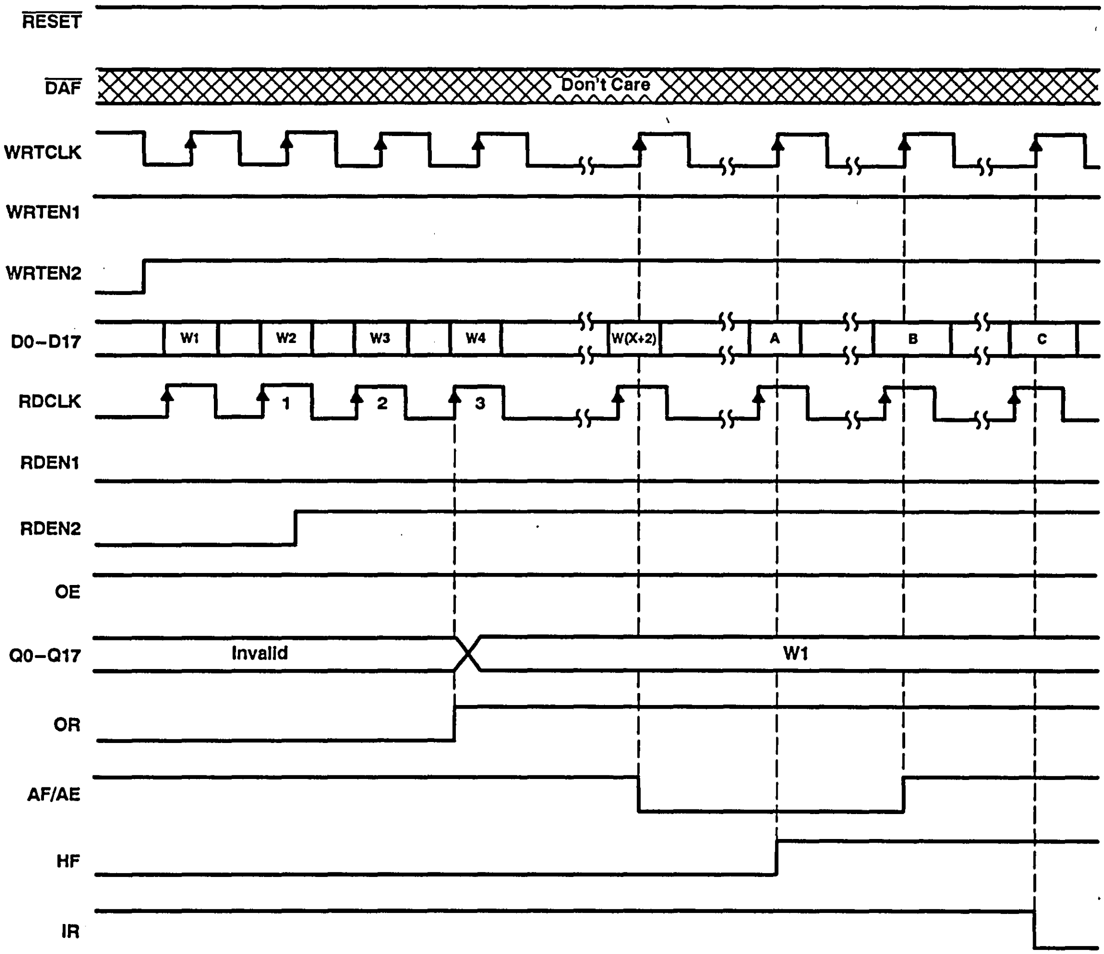


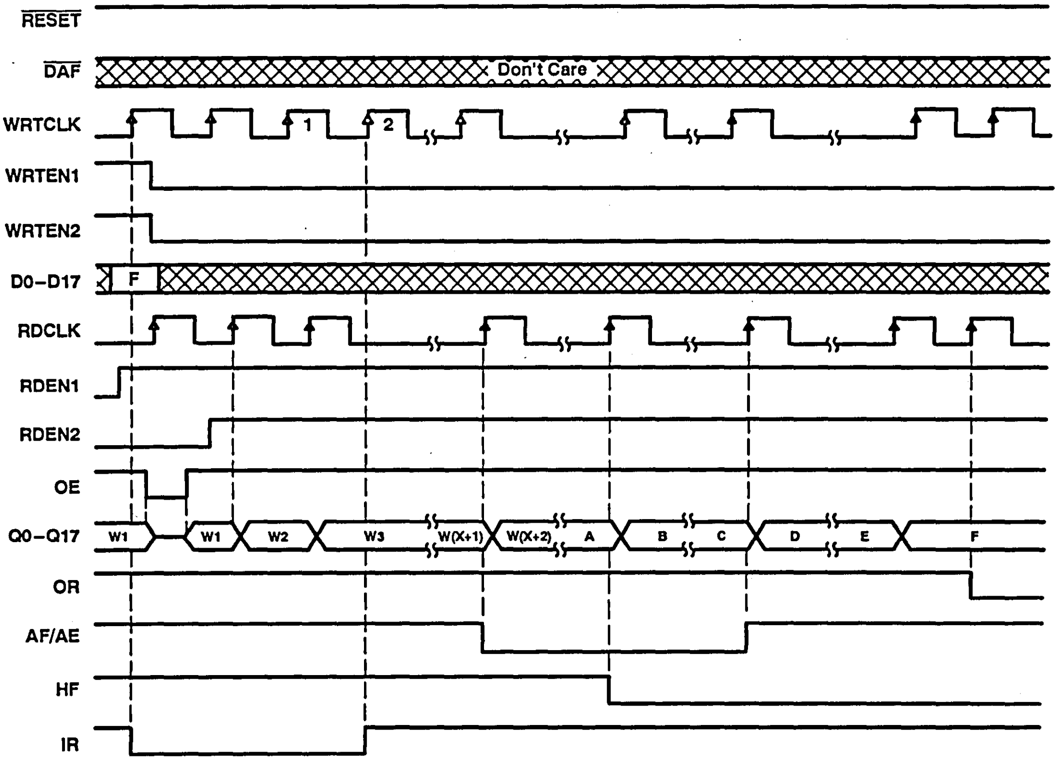
Figure 2. Reset Cycle: Define AF/AE Using the Default Value



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	B	C
W2049	W(4097 – X)	W4097

Figure 3. Write



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	B	C	D	E	F
W2049	W2050	W(4096 – X)	W(4097 – X)	W4096	W4097

Figure 4. Read

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	µA
I_{CC}§	V_I = V_{CC} – 0.2 V or 0				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_o	V_O = 0,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} tested with outputs open.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 4)

			'ACT7884-15		'ACT7884-20		'ACT7884-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		33.4		MHz
t_w	Pulse duration	WRTCLK high	6		7		8.5		ns
		WRTCLK low	6		7		11		
		RDCLK high	6		7		8.5		
		RDCLK low	6		7		11		
		$\overline{\text{DAF}}$ high	6		7		10		
t_{su}	Setup time	Data in (D0–D17) before WRTCLK↑	4		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	4		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	4		5		5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑†	5		6		7		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	4		5		5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	5		6		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	4		5		5		
t_h	Hold time	Data in (D0–D17) after WRTCLK↑	0		0		0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		0		1		
		OE, RDEN1, RDEN2 high after RDCLK↑	0		0		1		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑†	0		0		0		
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	0		0		1		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	0		0		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7884-15		'ACT7884-20		'ACT7884-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67		50		33.4		MHz
t_{pd}	RDCLK↑	Any Q	4	11	4	13	4	18	ns
t_{pd}‡									
t_{pd}	WRTCLK↑	IR	2	9	2	9.5	2	12	ns
t_{pd}	RDCLK↑	OR	2	9	2	9.5	2	12	
t_{pd}	WRTCLK↑	AF/AE	6	17	6	19	6	22	ns
	RDCLK↑		6	17	6	19	6	22	
t_{PLH}	WRTCLK↑	HF	6	15	6	17	6	21	ns
t_{PHL}	RDCLK↑		6	15	6	17	6	21	
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	3	16	3	17	3	21	ns
t_{PHL}		HF	4	18	4	19	4	23	
t_{en}	OE	Any Q	2	11	2	11	2	11	ns
t_{dis}			2	14	2	14	2	14	

‡ This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF,	f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

PRODUCT PREVIEW

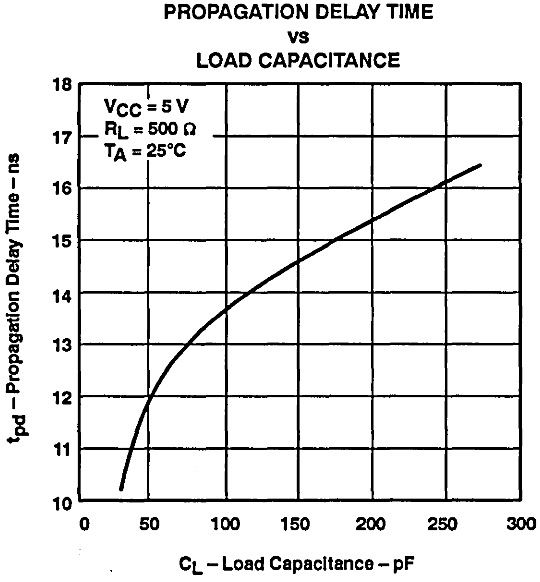


Figure 5

TYPICAL CHARACTERISTICS

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

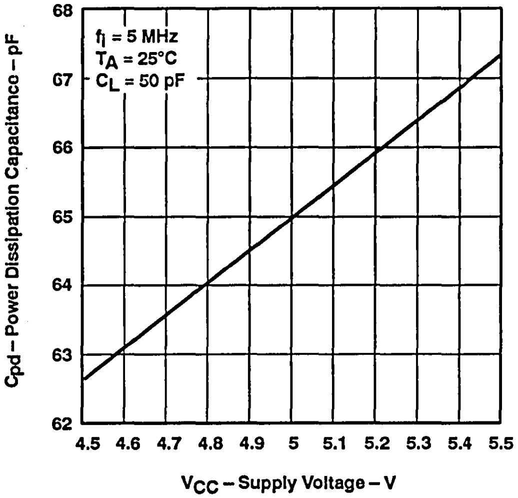


Figure 6

calculating power dissipation

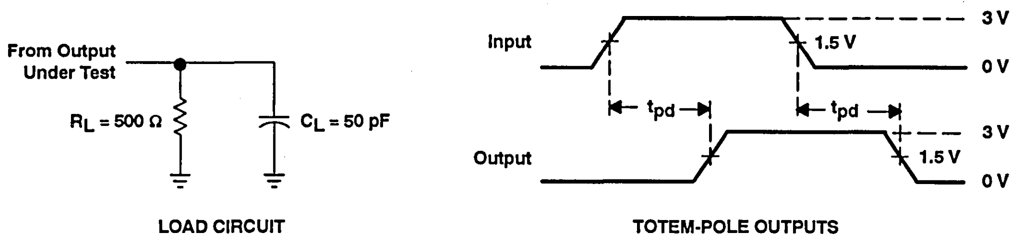
The maximum power dissipation (P_T) of the SN74ACT7884 can be calculated using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \sum(C_{pd} \times V_{CC}^2 \times f_i) + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

PARAMETER MEASUREMENT INFORMATION

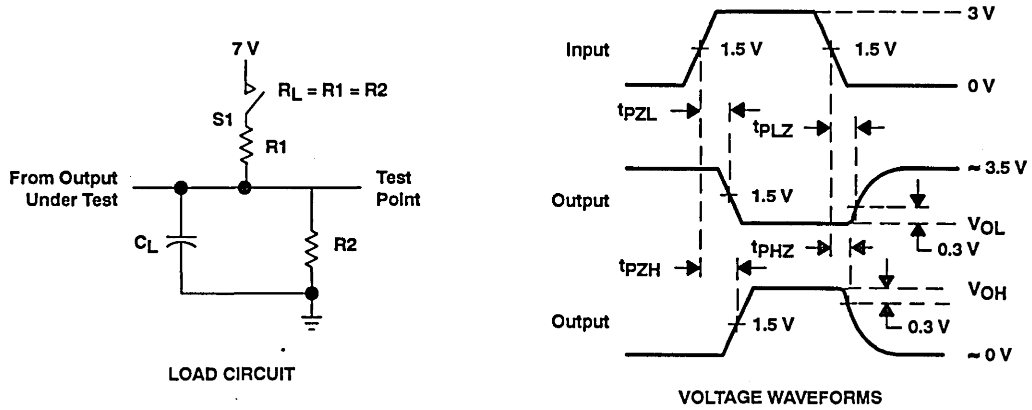


LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 7. Standard CMOS Outputs

PRODUCT PREVIEW



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 8. 3-State Outputs (Any Q)

APPLICATION INFORMATION

expanding the SN74ACT7884

The SN74ACT7884 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 9 shows two SN74ACT7884 devices configured for depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready flag (OR) of the previous device and the input-ready flag (IR) of the next device maintain data flow to the last device in the chain whenever space is available.

Figure 10 is an example of two SN74ACT7884 devices in word-width expansion. Width expansion is accomplished by simply connecting all common control signals between the devices and creating composite input-ready (IR) and output-ready (OR) signals. The almost-full/almost-empty flag (AF/AE) and half-full flag (HF) can be sampled from any one device. Depth expansion and width expansion can be used together.

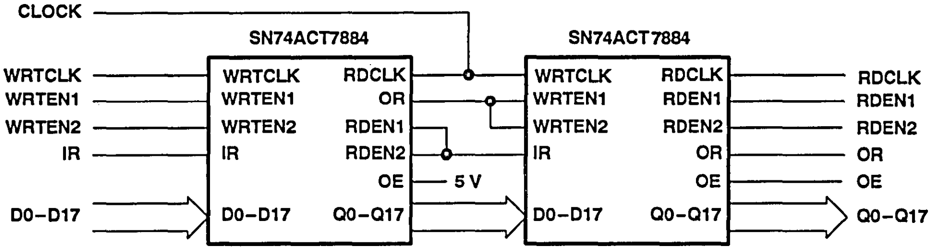


Figure 9. Word-Depth Expansion: 2048/4096/8192 Words × 18 Bits, N = 2

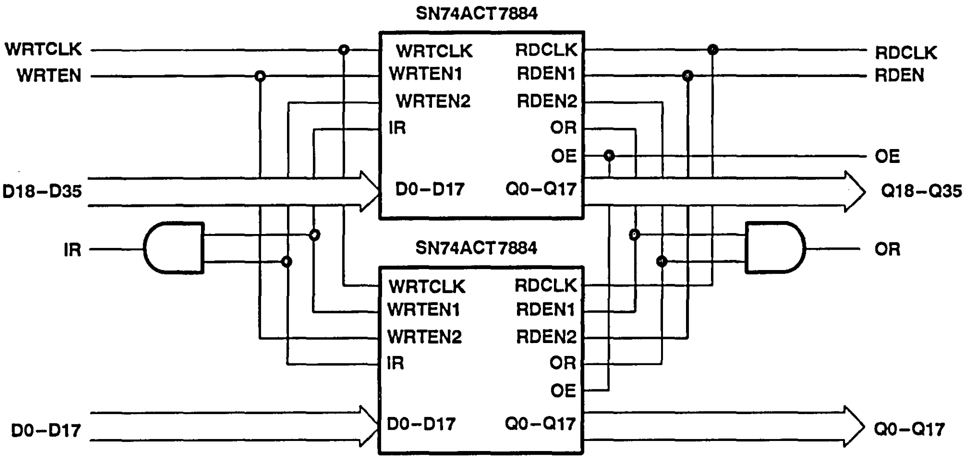


Figure 10. Word-Depth Expansion: 4096 Words × 36 Bits

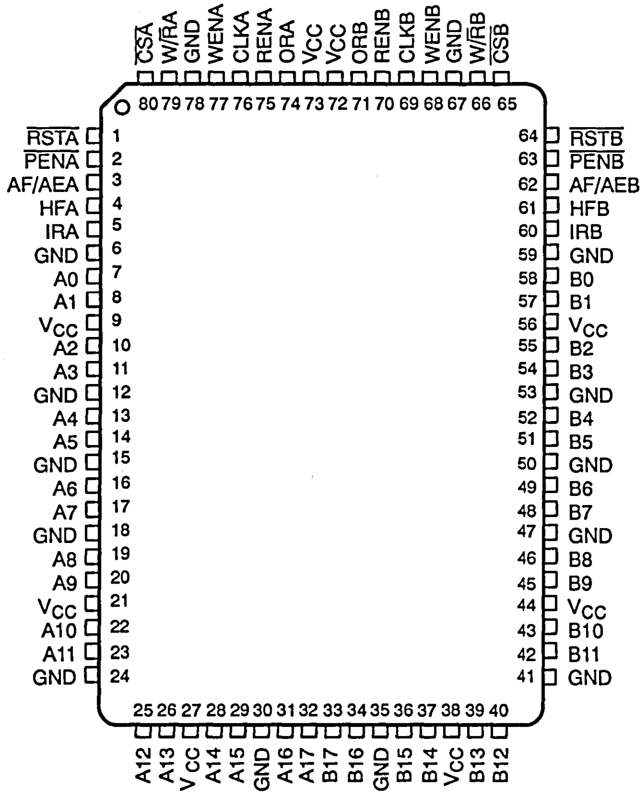
PRODUCT PREVIEW

SN74ABT7819
512 × 18 × 2 CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCBS125B – JULY 1992 – REVISED AUGUST 1994

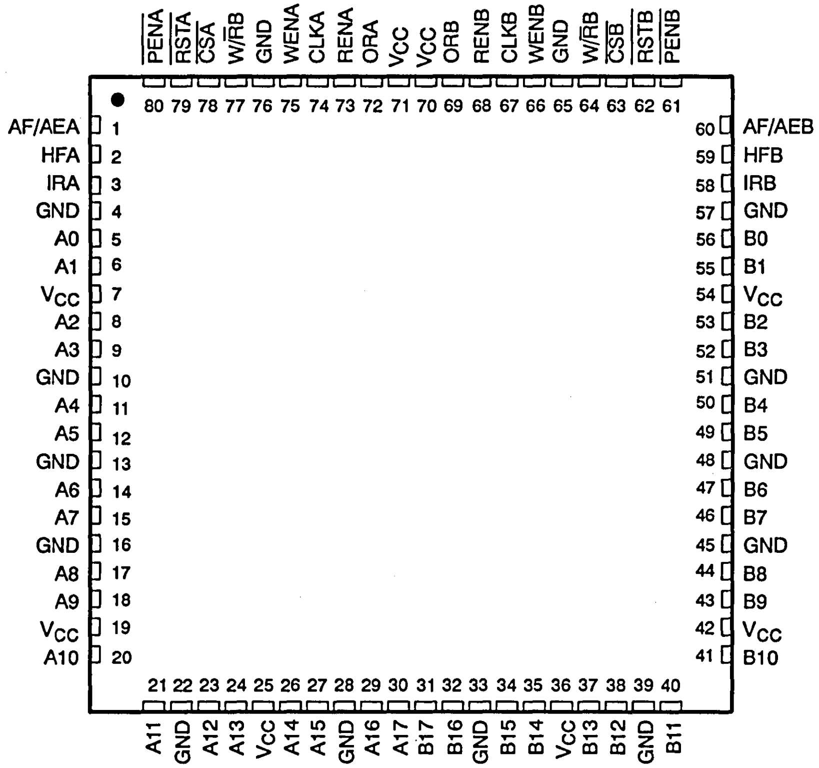
- **Member of the Texas Instruments Widebus ™ Family**
- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Two Separate 512 × 18 Clocked FIFOs Buffering Data in Opposite Directions**
- **IRA and ORA Synchronized to CLKA**
- **IRB and ORB Synchronized to CLKB**
- **Microprocessor Interface Control Logic**
- **Programmable Almost-Full/Almost-Empty Flags**
- **Fast Access Times of 9 ns With a 50-pF Load and Simultaneous Switching Data Outputs**
- **Data Rates up to 80 MHz**
- **Advanced BiCMOS Technology**
- **Available in 80-Pin Quad Flat Packages (PH) and Space-Saving 80-Pin Thin Quad Flat Packages (PN)**

PH PACKAGE
(TOP VIEW)



Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be read from its array in the same order it is written. The SN74ABT7819 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. Two independent 512 × 18 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions, a half-full flag, and a programmable almost-full/almost-empty flag.

The SN74ABT7819 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The state of the A0–A17 outputs is controlled by $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$. When both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are low, the outputs are active. The A0–A17 outputs are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is high. Data is written to FIFOA–B from port A on the low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is high, WENA is high, and the IRA flag is high. Data is read from FIFOB–A to the A0–A17 outputs on the low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is low, RENA is high, and the ORA flag is high.

description (continued)

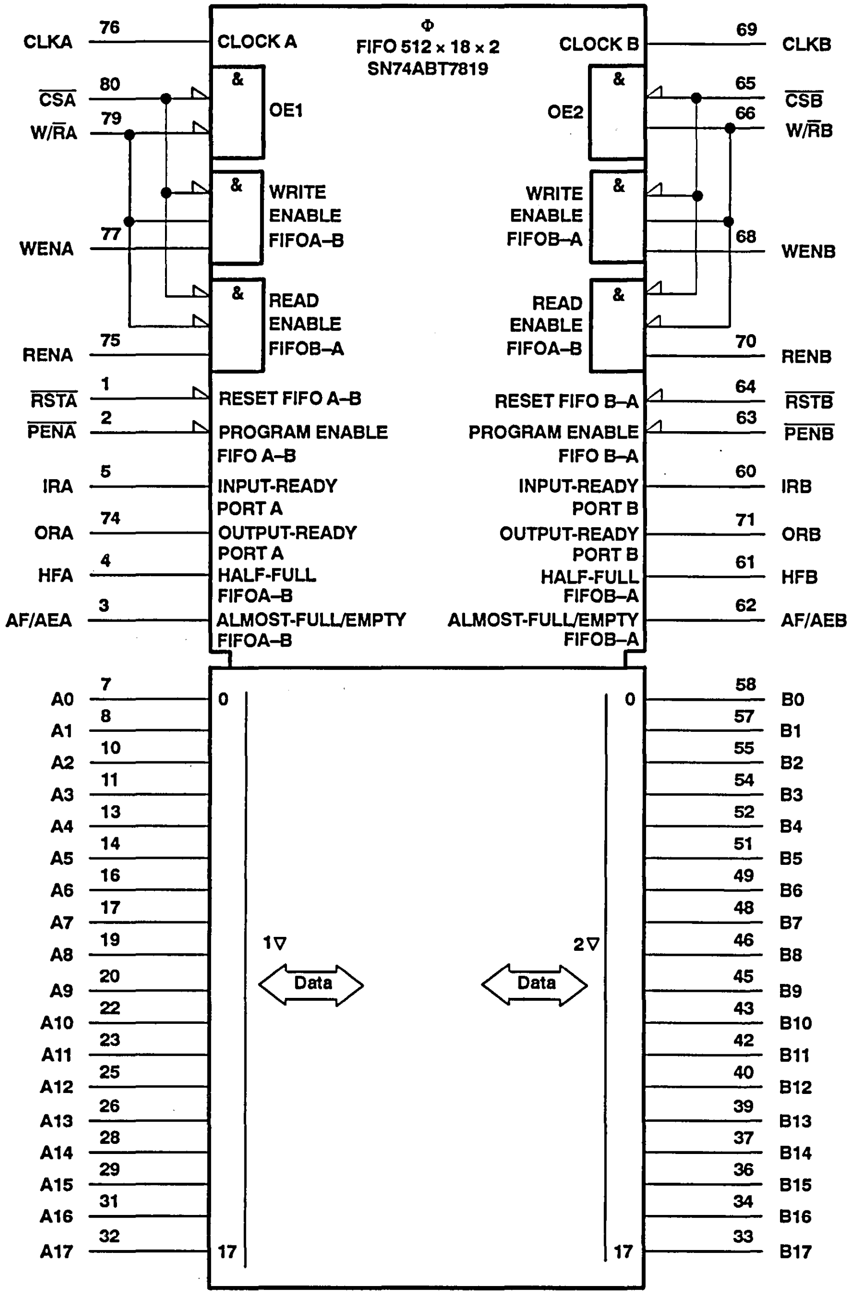
The state of the B0–B17 outputs is controlled by $\overline{\mathrm{CSB}}$ and W/$\overline{\mathrm{R}}$B. When both $\overline{\mathrm{CSB}}$ and W/$\overline{\mathrm{R}}$B are low, the outputs are active. The B0–B17 outputs are in the high-impedance state when either $\overline{\mathrm{CSB}}$ or W/$\overline{\mathrm{R}}$B is high. Data is written to FIFOB–A from port B on the low-to-high transition of CLKB when $\overline{\mathrm{CSB}}$ is low, W/$\overline{\mathrm{R}}$B is high, WENB is high, and the IRB flag is high. Data is read from FIFOA–B to the B0–B17 outputs on the low-to-high transition of CLKB when $\overline{\mathrm{CSB}}$ is low, W/$\overline{\mathrm{R}}$B is low, RENB is high, and the ORB flag is high.

The setup and hold-time constraints for the chip selects ($\overline{\mathrm{CSA}}$, $\overline{\mathrm{CSB}}$) and write/read selects (W/$\overline{\mathrm{R}}$A, W/$\overline{\mathrm{R}}$B) are for enabling write and read operations on memory and are not related to the high-impedance control of the data outputs. If a port's read enable (RENA or RENB) and write enable (WENA or WENB) are set low during a clock cycle, the chip select and write/read select can switch at any time during the cycle to change the state of the data outputs.

The input-ready and output-ready flags of a FIFO are two-stage synchronized to the port clocks for use as reliable control signals. CLKA synchronizes the status of the input-ready flag of FIFOA–B (IRA) and the output-ready flag of FIFOB–A (ORA). CLKB synchronizes the status of the input-ready flag of FIFOB–A (IRB) and the output-ready flag of FIFOA–B (ORB). When the input-ready flag of a port is low, the FIFO receiving input from the port is full and writes are disabled to its array. When the output-ready flag of a port is low, the FIFO that outputs data to the port is empty and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO output register at the same time its output-ready flag is asserted (high). When the memory is read empty and the output-ready flag is forced low, the last valid data remains on the FIFO outputs until the output-ready flag is asserted (high) again. In this way, a high on the output-ready flag indicates new data is present on the FIFO outputs.

The SN74ABT7819 is characterized for operation from 0°C to 70°C.

logic symbol†



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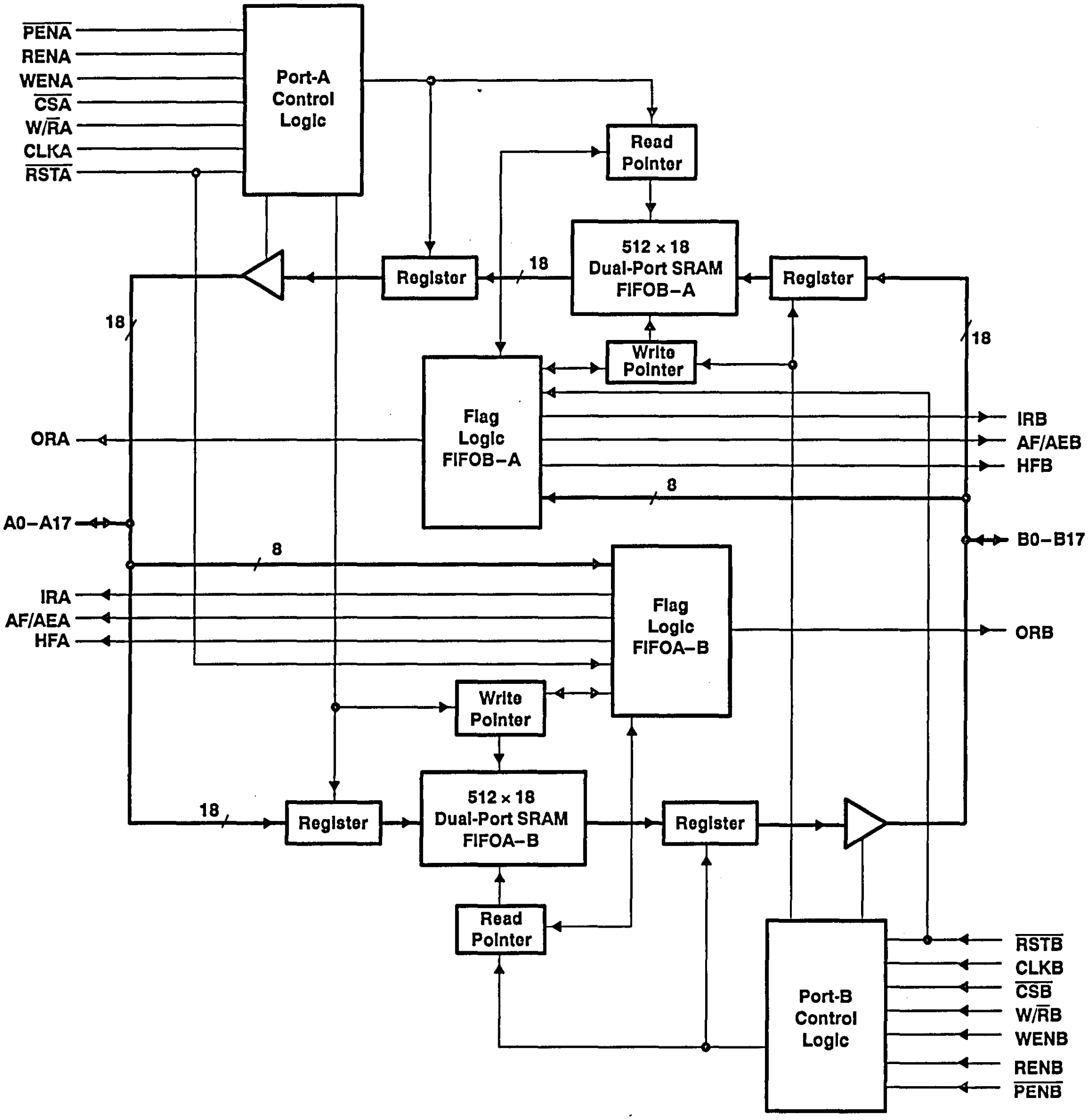
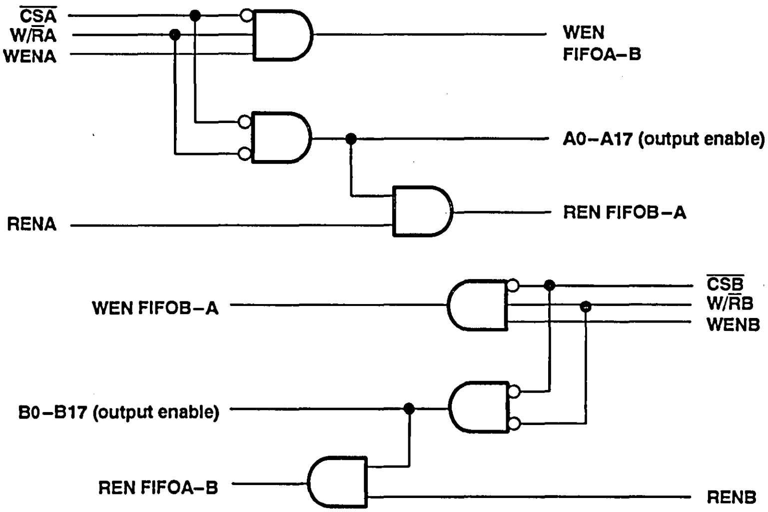
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the PH package.

functional block diagram



enable logic diagram (positive logic)



FUNCTION TABLES

SELECT INPUTS					A0–A17	PORT-A OPERATION
CLKA	$\overline{CSA}$	W/$\overline{RA}$	WENA	RENA		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write A0–A17 to FIFOA–B
↑	L	L	X	H	Active	Read FIFOB–A to A0–A17

SELECT INPUTS					B0–B17	PORT-B OPERATION
CLKB	$\overline{CSB}$	W/$\overline{RB}$	WENB	RENB		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write B0 –B17 to FIFOB–A
↑	L	L	X	H	Active	Read FIFOA–B to B0–B17

Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFOA–B almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEA or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when X or less words or (512 – Y) or more words are stored in FIFOA–B. AF/AEA is forced high when FIFOA–B is reset.
AF/AEB	O	FIFOB–A almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEB or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when X or less words or (512 – Y) or more words are stored in FIFOB–A. AF/AEB is forced high when FIFOB–A is reset.
B0–B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A to its low-to-high transition and can be asynchronous or coincident to CLKB.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B to its low-to-high transition and can be asynchronous or coincident to CLKA.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to either write data from A0–A17 to FIFOA–B or read data from FIFOB–A to A0–A17. The A0–A17 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to either write data from B0–B17 to FIFOB–A or read data from FIFOA–B to B0–B17. The B0–B17 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
HFA	O	FIFOA–B half-full flag. HFA is high when FIFOA–B contains 256 or more words and is low when FIFOA–B contains 255 or less words. HFA is set low after FIFOA–B is reset.
HFB	O	FIFOB–A half-full flag. HFB is high when FIFOB–A contains 256 or more words and is low when FIFOB–A contains 255 or less words. HFB is set low after FIFOB–A is reset.
IRA	O	Port-A input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFOA–B is full and writes to its array are disabled. IRA is set low during a FIFOA–B reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O	Port-B input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFOB–A is full and writes to its array are disabled. IRB is set low during a FIFOB–A reset and is set high on the second low-to-high transition of CLKB after reset.
ORA	O	Port-A output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFOB–A is empty and reads from its array are disabled. The last valid word remains on the FIFOB–A outputs when ORA is low. Ready data is present for the A0–A17 outputs when ORA is high. ORA is set low during a FIFOB–A reset and goes high on the third low-to-high transition of CLKA after the first word is loaded to an empty FIFOB–A.
ORB	O	Port-B output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFOA–B is empty and reads from its array are disabled. The last valid word remains on the FIFOA–B outputs when ORB is low. Ready data is present for the B0–B17 outputs when ORB is high. ORB is set low during a FIFOA–B reset and goes high on the third low-to-high transition of CLKB after the first word is loaded to an empty FIFOA–B.
$\overline{\text{PENA}}$	I	AF/AEA program enable. After FIFOA–B is reset and before a word is written to its array, the binary value on A0–A7 is latched as an AF/AEA offset when $\overline{\text{PENA}}$ is low and CLKA is high.
$\overline{\text{PENB}}$	I	AF/AEB program enable. After FIFOB–A is reset and before a word is written to its array, the binary value on B0–B7 is latched as an AF/AEB offset when $\overline{\text{PENB}}$ is low and CLKB is high.
RENA	I	Port-A read enable. A high level on RENA enables data to be read from FIFOB–A on the low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{RA}}$ is low, and ORA is high.
RENB	I	Port-B read enable. A high level on RENB enables data to be read from FIFOA–B on the low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{RB}}$ is low, and ORB is high.
$\overline{\text{RSTA}}$	I	FIFOA–B reset. To reset FIFOA–B, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RSTA}}$ is low. This sets HFA low, IRA low, ORB low, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFOB–A reset. To reset FIFOB–A, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RSTB}}$ is low. This sets HFB low, IRB low, ORA low, and AF/AEB high.
WENA	I	Port-A write enable. A high level on WENA enables data on A0–A17 to be written into FIFOA–B on the low-to-high transition of CLKA when W/$\overline{\text{RA}}$ is high, $\overline{\text{CSA}}$ is low, and IRA is high.

Terminal Functions (continued)

PIN NAME	I/O	DESCRIPTION
WENB	I	Port-B write enable. A high level on WENB enables data on B0–B17 to be written into FIFOB–A on the low-to-high transition of CLKB when W/$\overline{\text{R}}$B is high, $\overline{\text{CSB}}$ is low, and IRB is high.
W/$\overline{\text{R}}$A	I	Port-A write/$\overline{\text{read}}$ select. A high on W/$\overline{\text{R}}$A enables A0–A17 data to be written to FIFOA–B on a low-to-high transition of CLKA when WENA is high, $\overline{\text{CSA}}$ is low, and IRA is high. A low on W/$\overline{\text{R}}$A enables data to be read from FIFOB–A on a low-to-high transition of CLKA when RENA is high, $\overline{\text{CSA}}$ is low, and ORA is high. The A0–A17 outputs are in the high-impedance state when W/$\overline{\text{R}}$A is high.
W/$\overline{\text{R}}$B	I	Port-B write/read select. A high on W/$\overline{\text{R}}$B enables B0–B17 data to be written to FIFOB–A on a low-to-high transition of CLKB when WENB is high, $\overline{\text{CSB}}$ is low, and IRB is high. A low on W/$\overline{\text{R}}$B enables data to be read from FIFOA–B on a low-to-high transition of CLKB when RENB is high, $\overline{\text{CSB}}$ is low, and ORB is high. The B0–B17 outputs are in the high-impedance state when W/$\overline{\text{R}}$B is high.

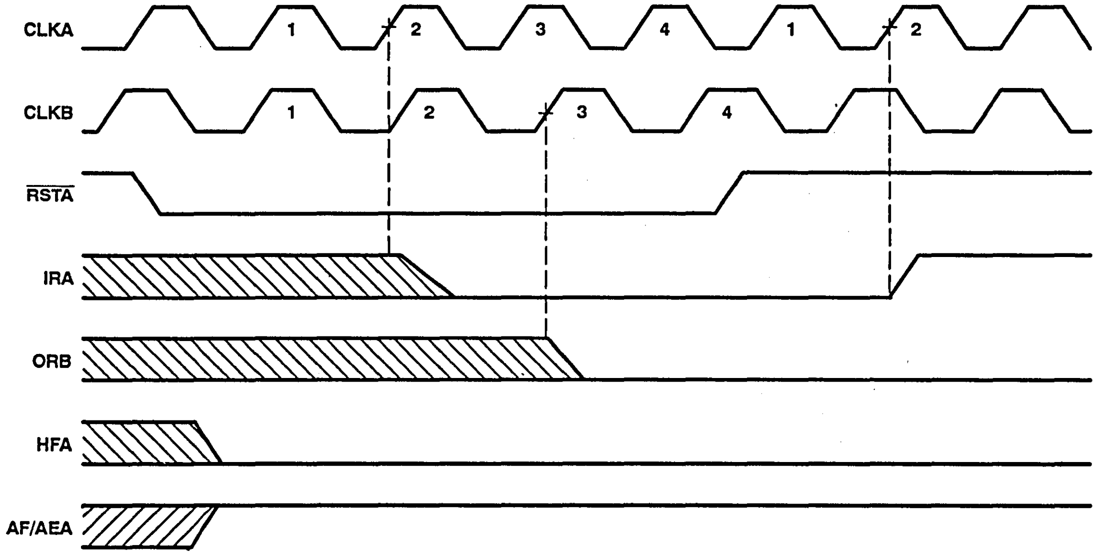


Figure 1. Reset Cycle for FIFOA–B†

† FIFOB–A is reset in the same manner.

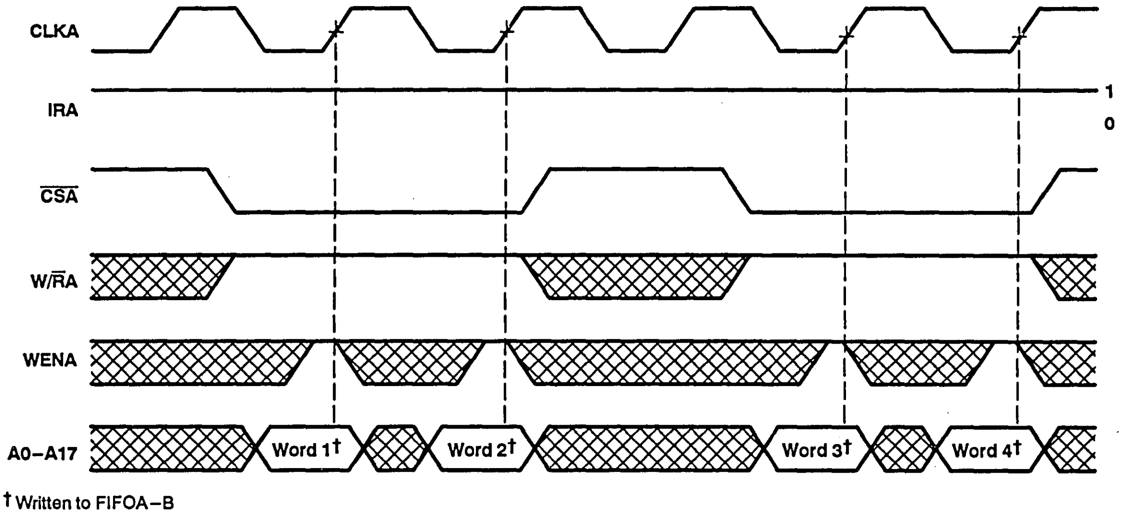


Figure 2. Write Timing – Port A

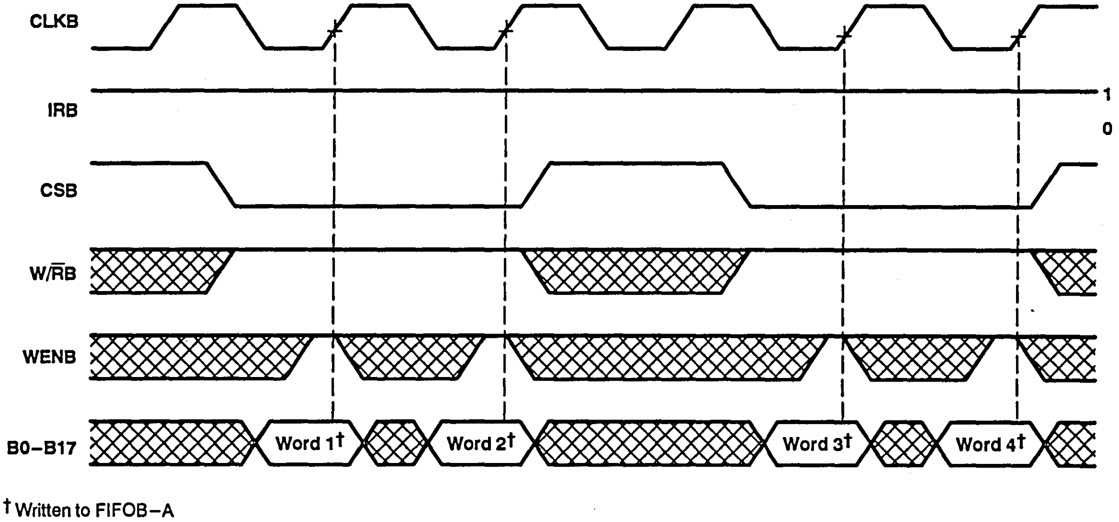


Figure 3. Write Timing – Port B

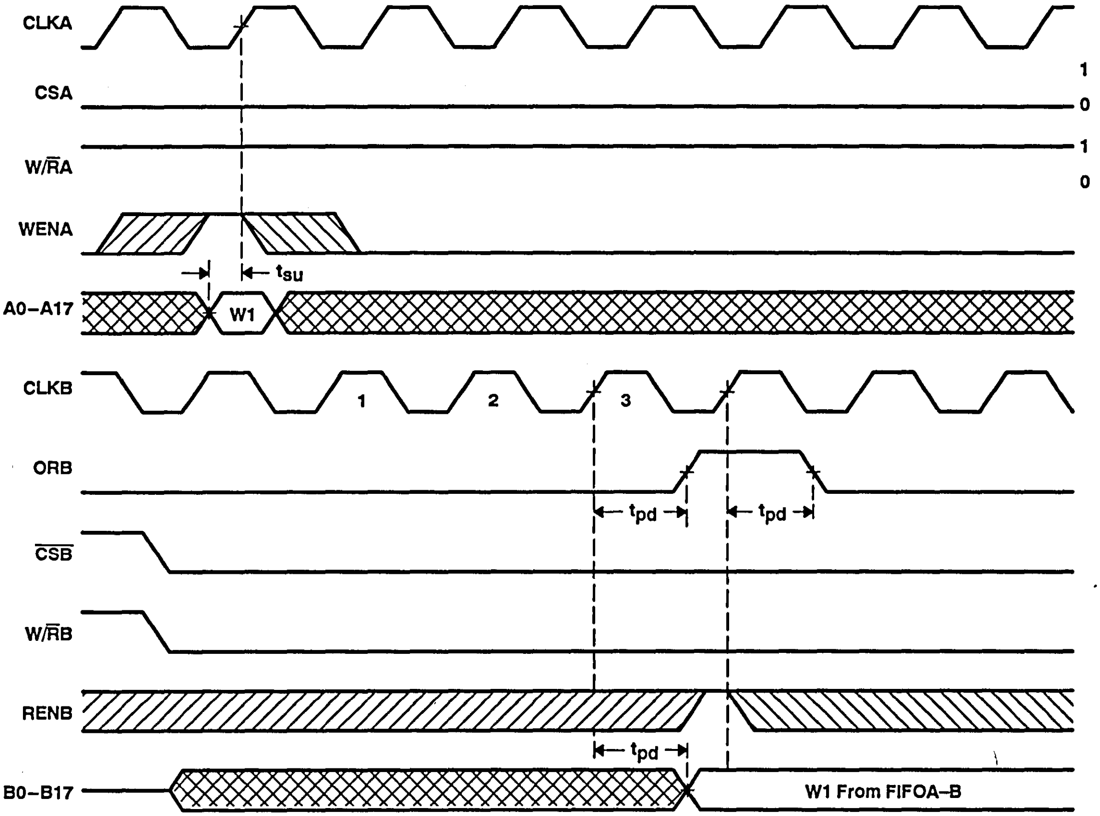


Figure 4. ORB-Flag Timing and First Data Word Fallthrough When FIFOA–B Is Empty†

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† Operation of FIFOB–A is identical to that of FIFOA–B.

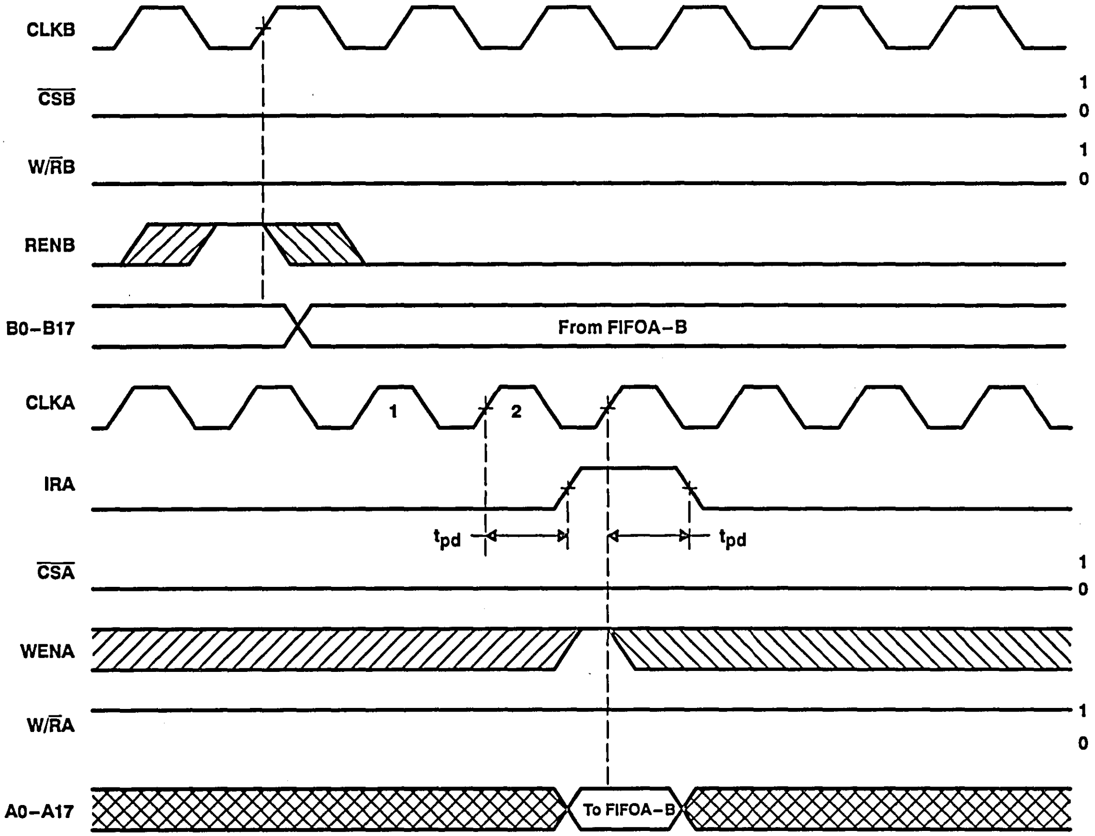

Figure 5. Write-Cycle and IRA-Flag Timing When FIFOA–B Is Full†

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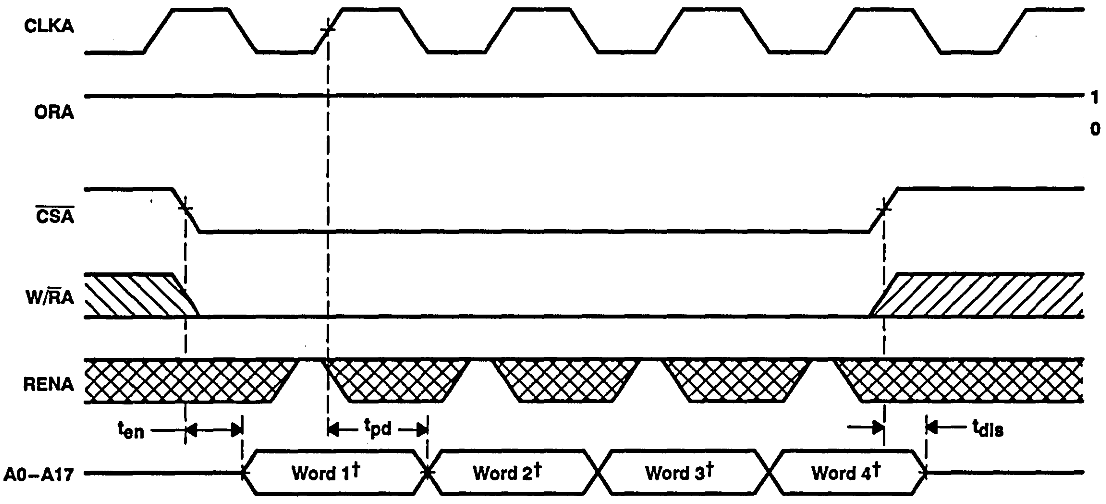
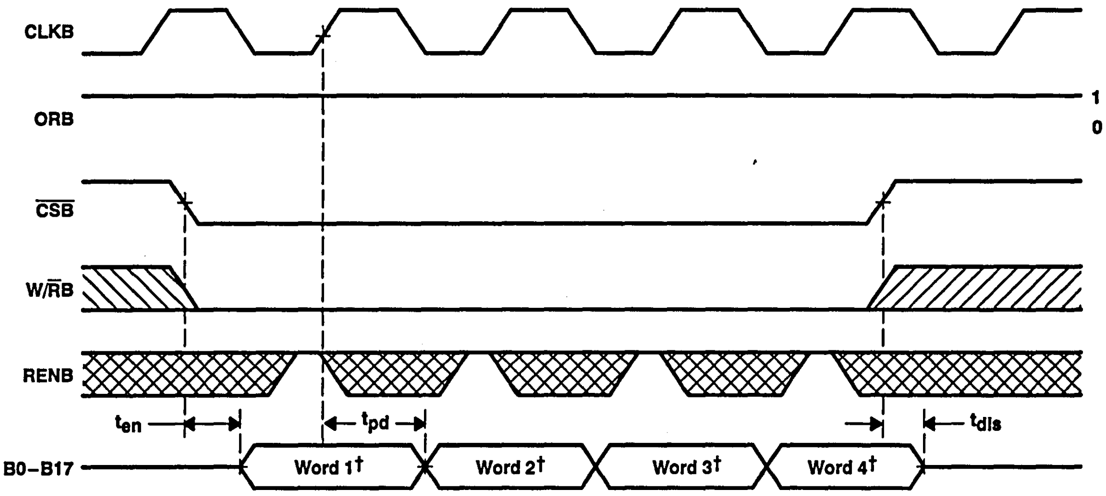
† Operation of FIFOB–A is identical to that of FIFOA–B.



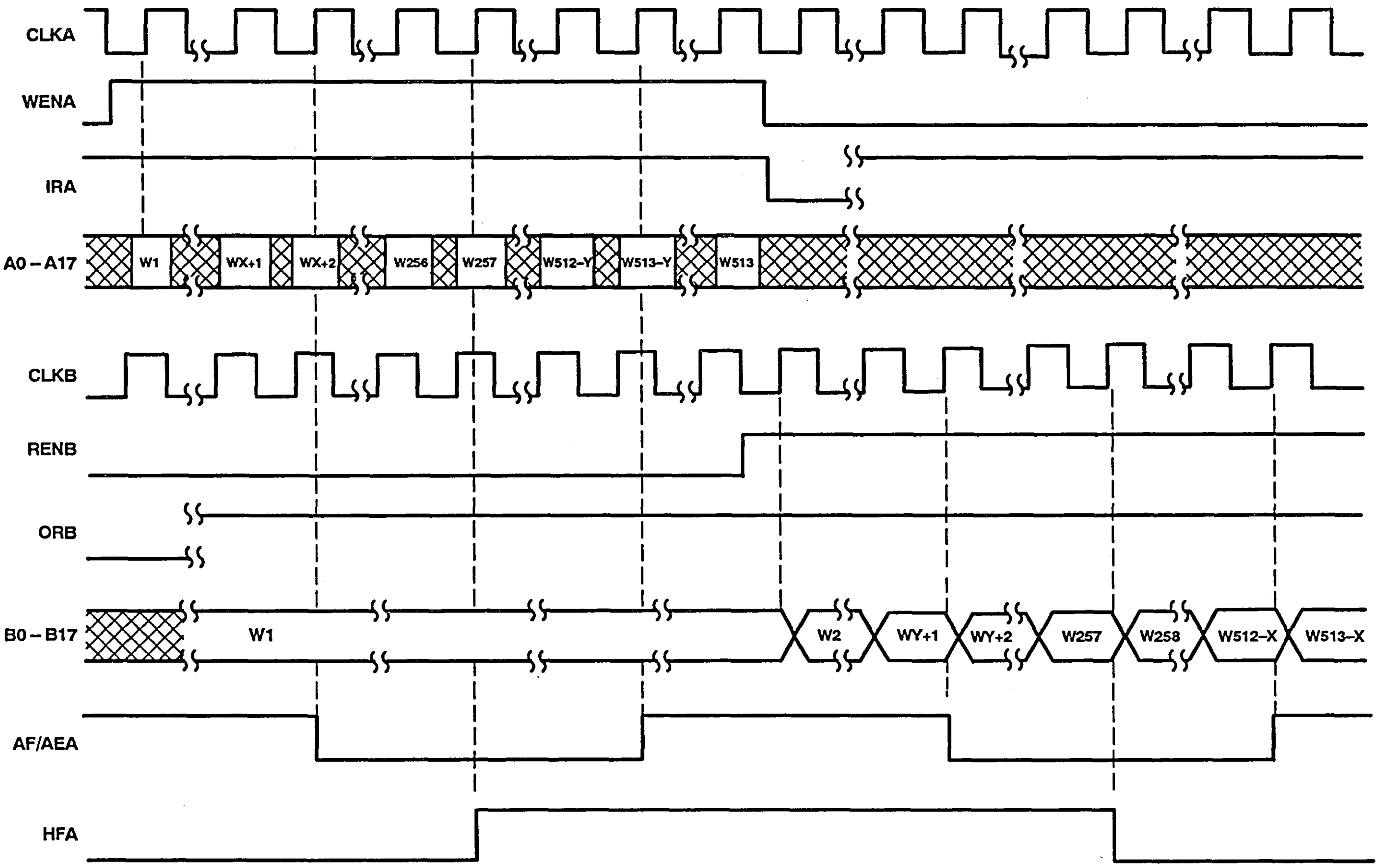
† Read from FIFOB–A

Figure 6. Read Timing – Port A



† Read from FIFOA–B

Figure 7. Read Timing – Port B



NOTES: $\overline{\text{CSA}}$, $\overline{\text{CSB}}$ = 0, W/$\overline{\text{RA}}$ = 1, W/$\overline{\text{RB}}$ = 0
X is the almost-empty offset and Y is the almost-full offset for AF/AEA.
HFB and AF/AEB function in the same manner for FIFO B–A.

Figure 8. FIFOA–B (HFA, AF/AEA) Asynchronous Flag Timing

offset values for AF/AE

The almost-full/almost-empty flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed from the input of the FIFO after it is reset and before a word is written to its memory. An AF/AE flag is high when its FIFO contains X or less words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ is brought low after FIFOA–B is reset and only when CLKA is low. On the following low-to-high transition of CLKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of CLKA reprograms Y to the binary value on A0–A7 at the time of the second CLKA low-to-high transition.

During the first two CLKA cycles used for offset programming, $\overline{\text{PENA}}$ can be brought high only when CLKA is low. $\overline{\text{PENA}}$ can be brought high at any time after the second CLKA pulse used for offset programming returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 9). To use the default values of X = Y = 128, $\overline{\text{PENA}}$ must be tied high. No data is stored in FIFOA–B while the AF/AEA offsets are programmed. The AF/AEB flag is programmed in the same manner with $\overline{\text{PENB}}$ enabling CLKB to program the offset values taken from B0–B7.

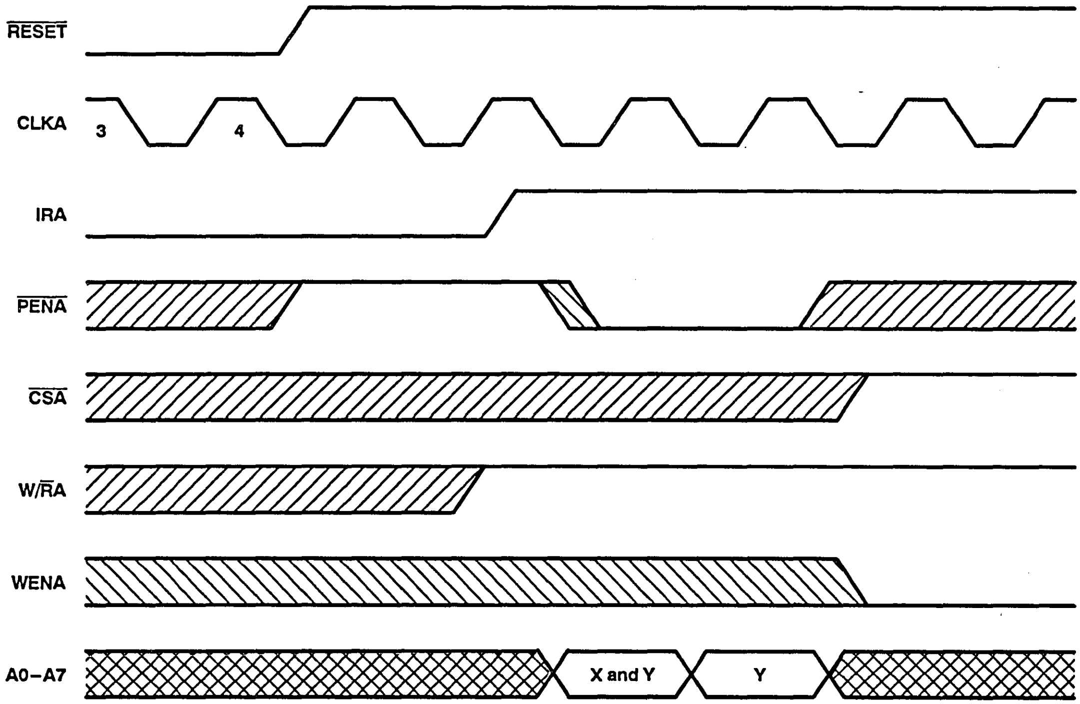


Figure 9. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O	48 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−12	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			V
		V_{CC} = 5 V, I_{OH} = −3 mA		3			
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 24 mA			0.5		V
I_I		V_{CC} = 5.5 V, V_I = V_{CC} or GND				±1	µA
I_{OZH}§		V_{CC} = 5.5 V, V_O = 2.7 V				50	µA
I_{OZL}§		V_{CC} = 5.5 V, V_O = 0.5 V				−50	µA
I_O¶		V_{CC} = 5.5 V, V_O = 2.5 V		−40	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			15	mA
			Outputs low			95	
			Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V			6		pF
C_o	Flags	V_O = 2.5 V or 0.5 V			4		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 8)

			'ABT7819-12		'ABT7819-15		'ABT7819-20		'ABT7819-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			80		67		50		33.3	MHz
t_w	Pulse duration	CLKA, CLKB high or low	4.5		6		8		11		ns
t_{su}	Setup time	A0–A17 before CLKA↑ and B0–B17 before CLKB↑	3		4		5		5		ns
		$\overline{\text{CSA}}$ before CLKA↑ and $\overline{\text{CSB}}$ before CLKB↑	6		6		7		7		
		W/$\overline{\text{RA}}$ before CLKA↑ and W/$\overline{\text{RB}}$ before CLKB↑	6		6		7		7		
		WENA before CLKA↑ and WENB before CLKB↑	4		4		5		5		
		RENA before CLKA↑ and RENB before CLKB↑	5		5		5		6		
		$\overline{\text{PENA}}$ before CLKA↑ and $\overline{\text{PENB}}$ before CLKB↑	3		4		5		5		
		$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low before first CLKA↑ and CLKB↑ †	3		4		5		5		
t_h	Hold time	A0–A17 after CLKA↑ and B0–B17 after CLKB↑	0		0		0		0		ns
		$\overline{\text{CSA}}$ after CLKA↑ and $\overline{\text{CSB}}$ after CLKB↑	0		0		0		0		
		W/$\overline{\text{RA}}$ after CLKA↑ and W/$\overline{\text{RB}}$ after CLKB↑	0		0		0		0		
		WENA after CLKA↑ and WENB after CLKB↑	0		0		0		0		
		RENA after CLKA↑ and RENB after CLKB↑	0		0		0		0		
		PENA after CLKA low and PENB after CLKB low	2		2		2		2		
		$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low after fourth CLKA↑ and CLKB↑ †	3		3		4		4		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figures 10 and 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ABT7819-12			'ABT7819-15		'ABT7819-20		'ABT7819-30		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKA or CLKB		80			67		50		33.3		MHz
t_{pd}	CLKA↑	A0–A17	4	7	9	4	10	4	12	4	14	ns
	CLKB↑	B0–B17	4	7	9	4	10	4	12	4	14	
t_{pd}‡	CLKA↑	A0–A17		6								ns
	CLKB↑	B0–B17		6								
t_{pd}	CLKA↑	IRA	4		9	4	10	4	12	4	14	ns
	CLKB↑	IRB	4		9	4	10	4	12	4	14	
t_{pd}	CLKA↑	ORA	3.5		9	3.5	10	3.5	12	3.5	14	ns
	CLKB↑	ORB	3.5		9	3.5	10	3.5	12	3.5	14	
t_{pd}	CLKA↑	AF/AEA	8		17	8	17	8	18	8	20	ns
	CLKB↑		8		17	8	17	8	18	8	20	
t_{PLH}	$\overline{\text{RSTA}}$	AF/AEA	4		12	4	14	4	15	4	16	ns
t_{pd}	CLKA↑	AF/AEB	8		17	8	17	8	18	8	20	ns
	CLKB↑		8		17	8	17	8	18	8	20	
t_{PLH}	$\overline{\text{RSTB}}$	AF/AEB	4		12	4	14	4	15	4	16	ns
	CLKA↑	HFA	8		17	8	17	8	18	8	20	
t_{PHL}	CLKB↑	HFA	8		17	8	17	8	18	8	20	ns
	$\overline{\text{RSTA}}$		4		12	4	14	4	15	4	16	
t_{PHL}	CLKA↑	HFB	8		17	8	17	8	18	8	20	ns
t_{PLH}	CLKB↑	HFB	8		17	8	17	8	18	8	20	ns
t_{PHL}	$\overline{\text{RSTB}}$		4		12	4	14	4	15	4	16	
t_{en}	$\overline{\text{CSA}}$	A0–A17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{\text{RA}}$		2.5		8	2.5	9	2.5	10	2.5	11	
t_{en}	$\overline{\text{CSB}}$	B0–B17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{\text{RB}}$		2.5		8	2.5	9	2.5	10	2.5	11	
t_{dis}	$\overline{\text{CSA}}$	A0–A17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{\text{RA}}$		2.5		8	2.5	9	2.5	10	2.5	11	
t_{dis}	$\overline{\text{CSB}}$	B0–B17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{\text{RB}}$		2.5		8	2.5	9	2.5	10	2.5	11	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ This parameter is measured with a 30-pF load (see Figure 10).

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

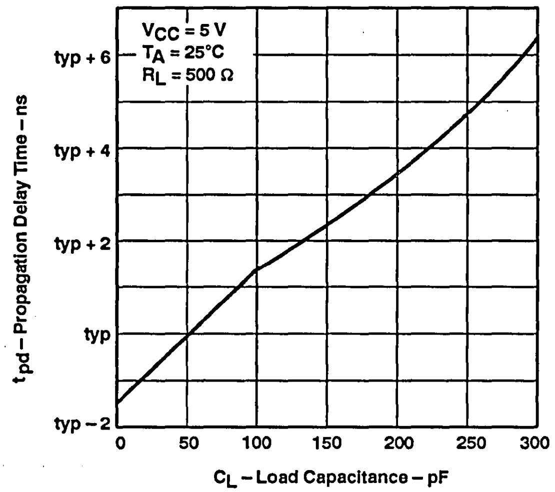


Figure 10

SUPPLY CURRENT vs CLOCK FREQUENCY

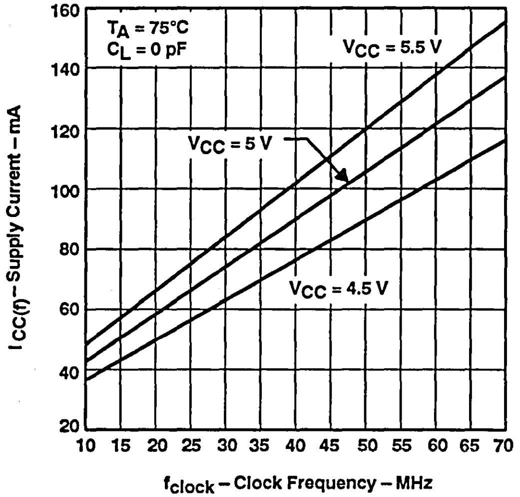


Figure 11

TYPICAL CHARACTERISTICS

calculating power dissipation

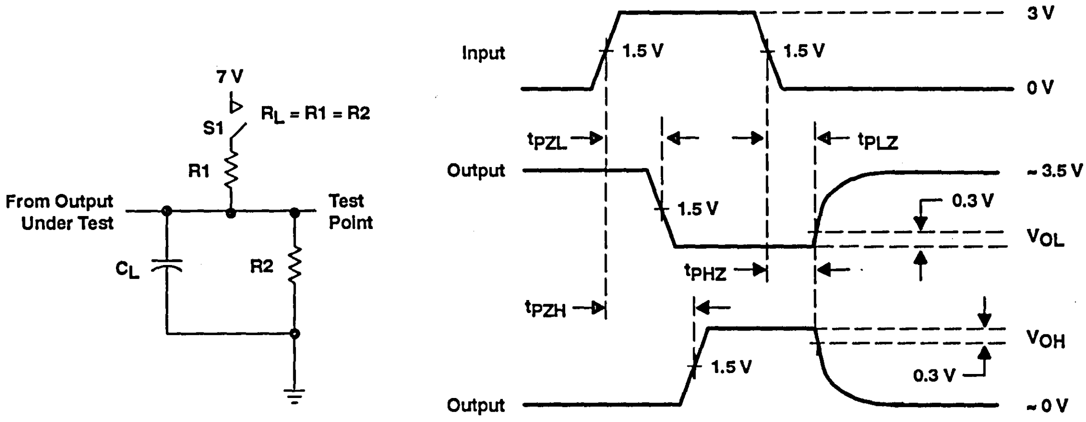
With $I_{CC(f)}$ taken from Figure 11, the maximum power dissipation (P_T) based on all outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH}^2 \times f_o)$$

where:

$I_{CC(f)}$ = maximum I_{CC} per clock frequency
C_L = output capacitive load
f_o = data output frequency
V_{OH} = typical output high level

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 12. Load Circuit and Voltage Waveforms

18-BIT STROBED FIFOS

Features	Benefits
Member of Texas Instruments Widebus™ family	Combines wider data-path capability with reduced package area
Advanced BiCMOS process	Fast access time for improved system cycle time and performance
0.8-µm CMOS process	Fast access times combined with low power
Supports clock rates up to 67 MHZ	Supports high-performance systems
Fast access times	Access times as low as 12 ns for improved performance
High drive capabilities	Drive capability as high as –12 mA to 24 mA for high fanout and bus applications
Depth from 16 to 2K words	Allows greater system optimization
Load/unload clock rising edge triggered	Reduces timing and pulse-shaping requirements
Asynchronous load/unload clock	Independent read and write capabilities
Grey-code flag architecture	Eliminates race conditions
Output edge control (OEC™) circuitry	Improved reliability
Distributed V_{CC} and GND	Improved noise immunity and mutual coupling effects
Fine-pitch package options	Significantly reduces critical board space
Available in EIAJ 80-pin TQFP packages	Board-space savings of up to 70% over 68-pin PLCC option

The following table lists military FIFO Widebus™ devices currently targeted for market introduction. Customers interested in learning more about TI's plans for these devices should contact military Advanced System Logic marketing at (915) 561-7289.

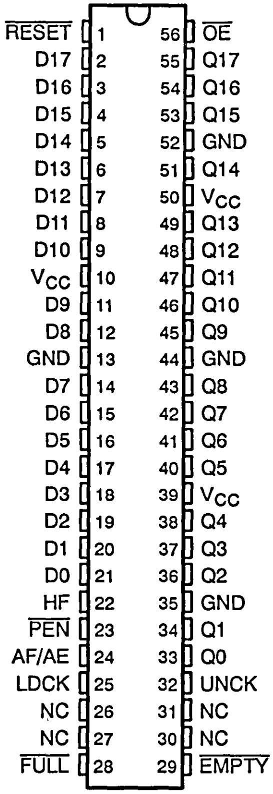
DEVICE	PACKAGE	DESCRIPTION
SNJ54ABT7820-XX	68 CQFP, 68 PGA	512 × 18-Bit Bidirectional Strobed FIFO

SN74ACT7814
64 × 18 FIRST-IN, FIRST-OUT MEMORY

SCAS209 – APRIL 1992

- **Member of the Texas Instruments Widebus ™ Family**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7804 and SN74ACT7806**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7814 is a 64-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 64. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 32 or more words and is low when it contains 31 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (64 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (63 – Y) words.

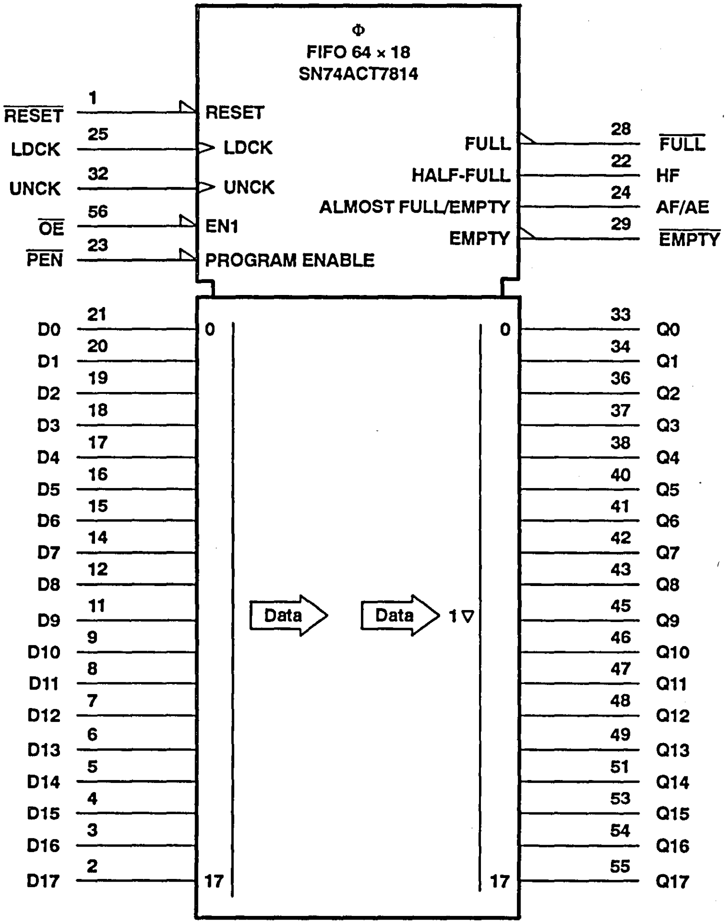
A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

The SN74ACT7814 is characterized for operation from 0°C to 70°C.

Widebus is a trademark of Texas Instruments Incorporated.

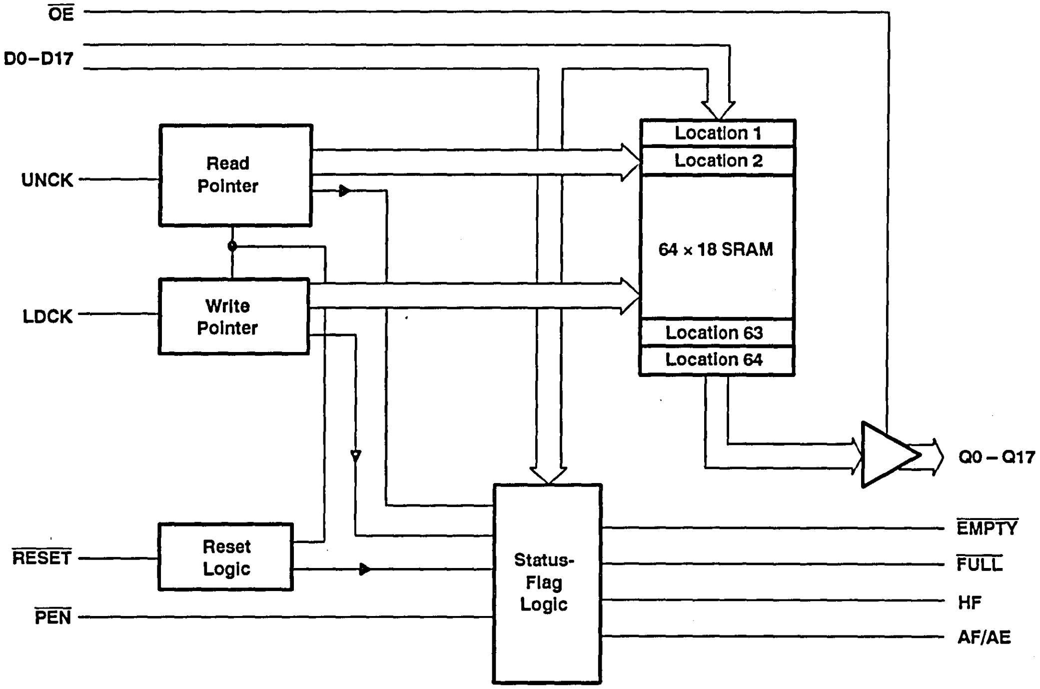
TEXAS
INSTRUMENTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 8 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
EMPTY	29	O	Empty flag. EMPTY is high when the FIFO memory is not empty; EMPTY is low when the FIFO memory is empty or upon assertion of RESET.
FULL	28	O	Full flag. FULL is high when the FIFO memory is not full or upon assertion of RESET; FULL is low when the FIFO memory is full.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when FULL is high.
OE	56	I	Output enable. When OE is high, the data outputs are in the high-impedance state.
PEN	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when PEN is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
RESET	1	I	Reset. A low level on this input resets the FIFO and drives FULL high and HF and EMPTY low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when EMPTY is high.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag will be high when the FIFO contains X or less words or (64 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D4 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D4 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 31 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 8, $\overline{\text{PEN}}$ must be held high.

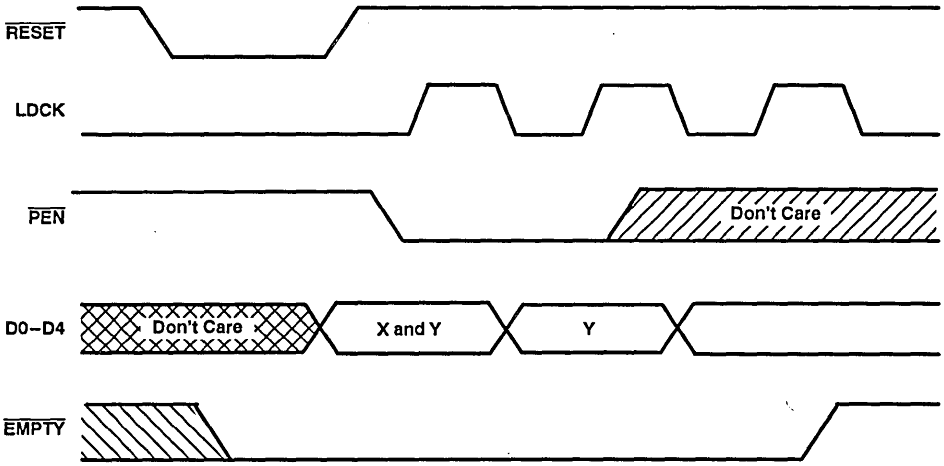
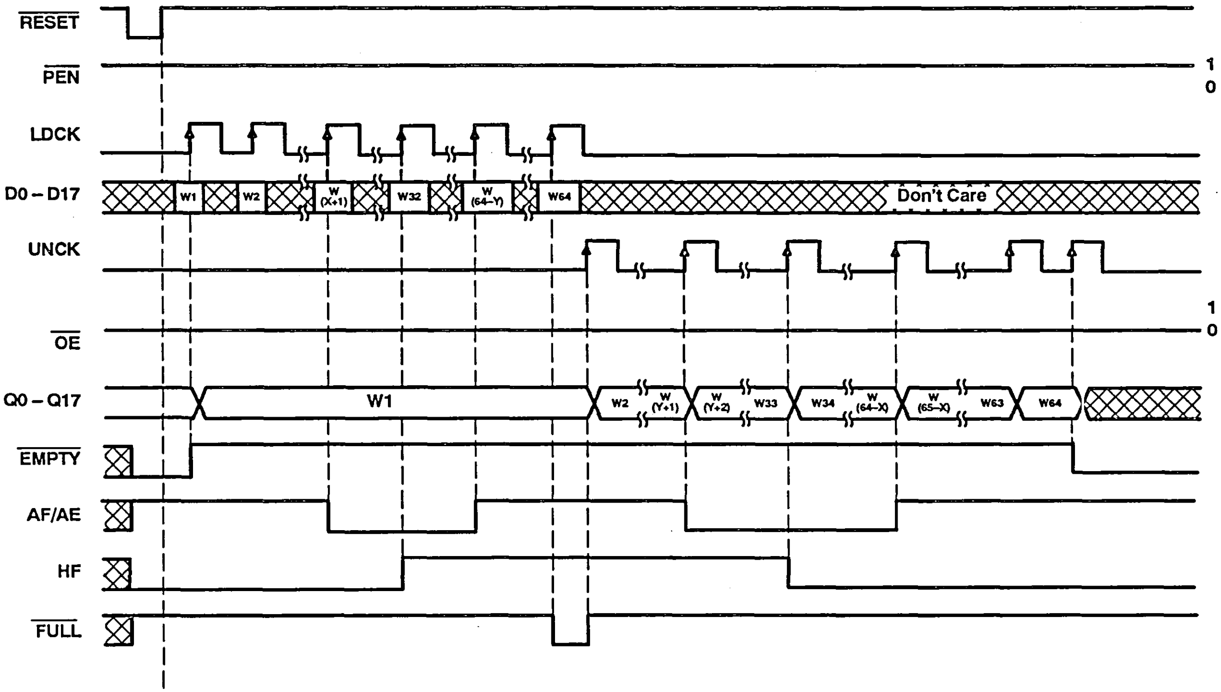


Figure 1. Programming X and Y Separately



Define the AF/AE Flag Using
the Default Value of X and Y

Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7814-20		'ACT7814-25		'ACT7814-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16	mA
		Flags		8		8		8	
f_{clock}	Clock frequency			50		40		25	MHz
t_w	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		$\overline{\text{PEN}}$ low	7		8		12		
		$\overline{\text{RESET}}$ low	10		10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		$\overline{\text{PEN}}$ before LDCK↑	5		5		5		
		LDCK inactive before $\overline{\text{RESET}}$ high	5		6		6		
t_h	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after $\overline{\text{RESET}}$ high	5		6		6		
		$\overline{\text{PEN}}$ low after LDCK↑	3		3		3		
		$\overline{\text{PEN}}$ high after LDCK↓	0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 5 and 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7814-20			'ACT7814-25		'ACT7814-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		25		MHz
t_{pd}	LDCK↑	Any Q	9		20	9	22	9	24	ns
	UNCK↑		6	11.5	15	6	18	6	20	
t_{pd}‡	UNCK↑			10.5						
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
t_{PHL}	UNCK↑		6		15	6	17	6	19	
	$\overline{\text{RESET}}$ low		4		16	4	18	4	20	
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6		15	6	17	6	19	ns
t_{PLH}	UNCK↑		6		15	6	17	6	19	
	$\overline{\text{RESET}}$ low		4		18	4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7		18	7	20	7	22	ns
	UNCK↑		7		18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low		2		10	2	12	2	14	
t_{PLH}	LDCK↑	HF	5		18	5	20	5	22	ns
t_{PHL}	UNCK↑		7		18	7	20	7	22	
	$\overline{\text{RESET}}$ low		3		12	3	14	3	16	
t_{en}	$\overline{\text{OE}}$	Any Q	2		9	2	10	2	11	ns
t_{dis}			2		10	2	11	2	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured at C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

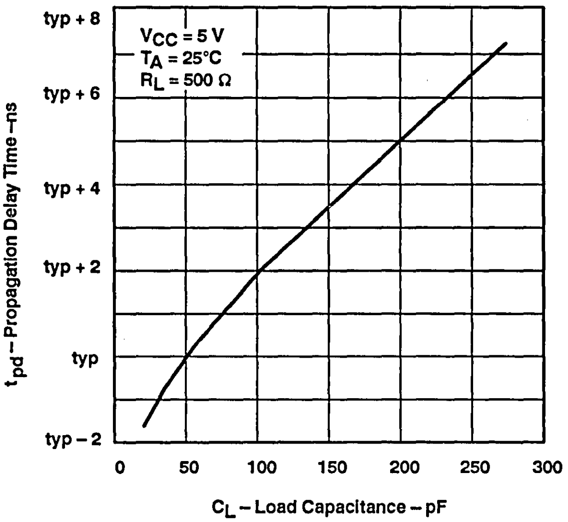


Figure 3

SUPPLY CURRENT vs CLOCK FREQUENCY

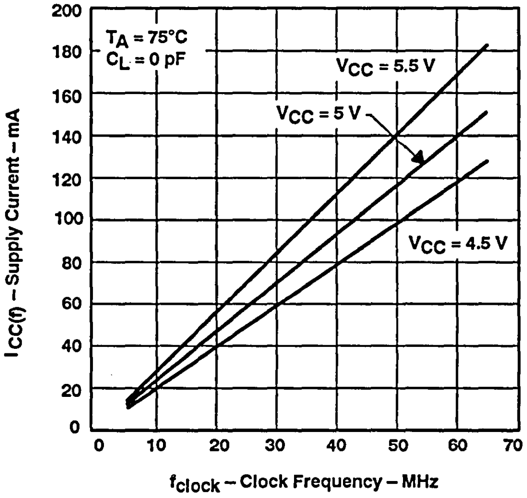


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

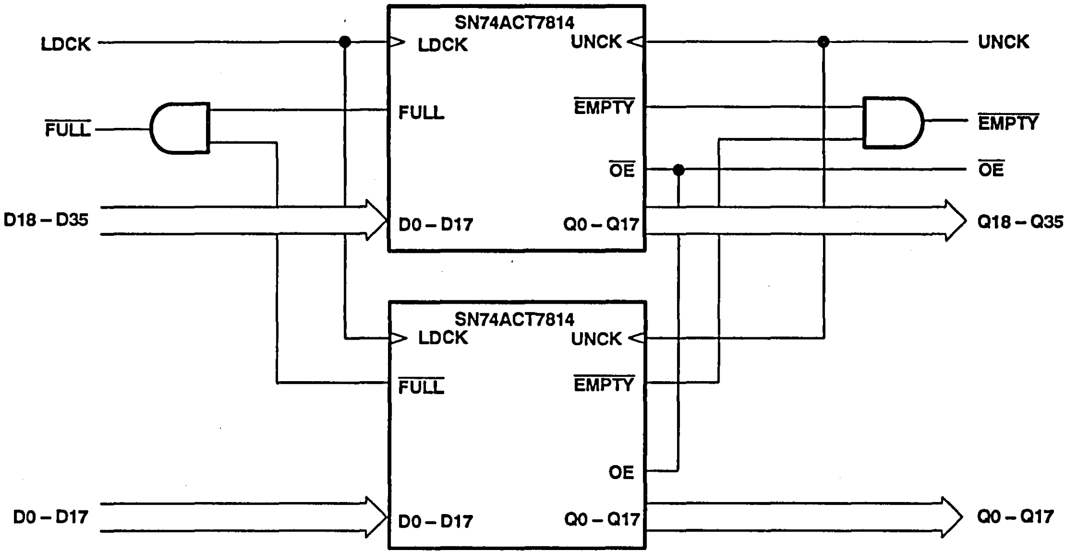
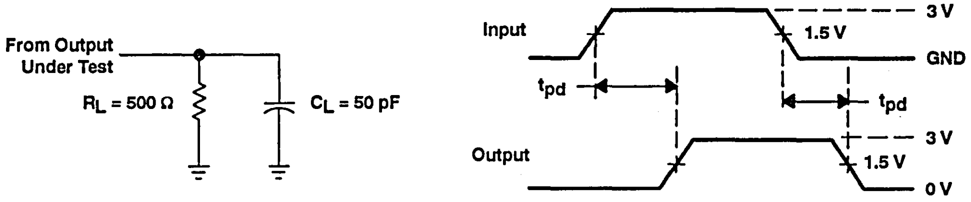


Figure 5. Word-Width Expansion: 64 Words by 36 Bits

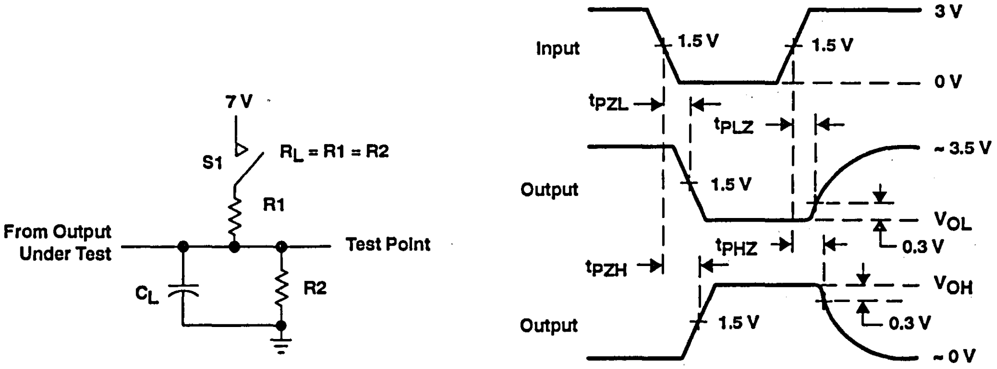
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 6. Standard CMOS Outputs ($\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, HF, AF/AE)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

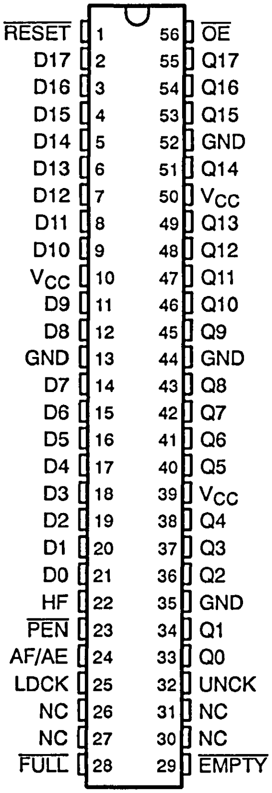
Figure 7. 3-State Outputs (Any Q)

SN74ACT7806
256 × 18 FIRST-IN, FIRST-OUT MEMORY

SCAS436 – APRIL 1992

- **Member of the Texas Instruments Widebus ™ Family**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **256 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7804 and SN74ACT7814**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7806 is a 256-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 256. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

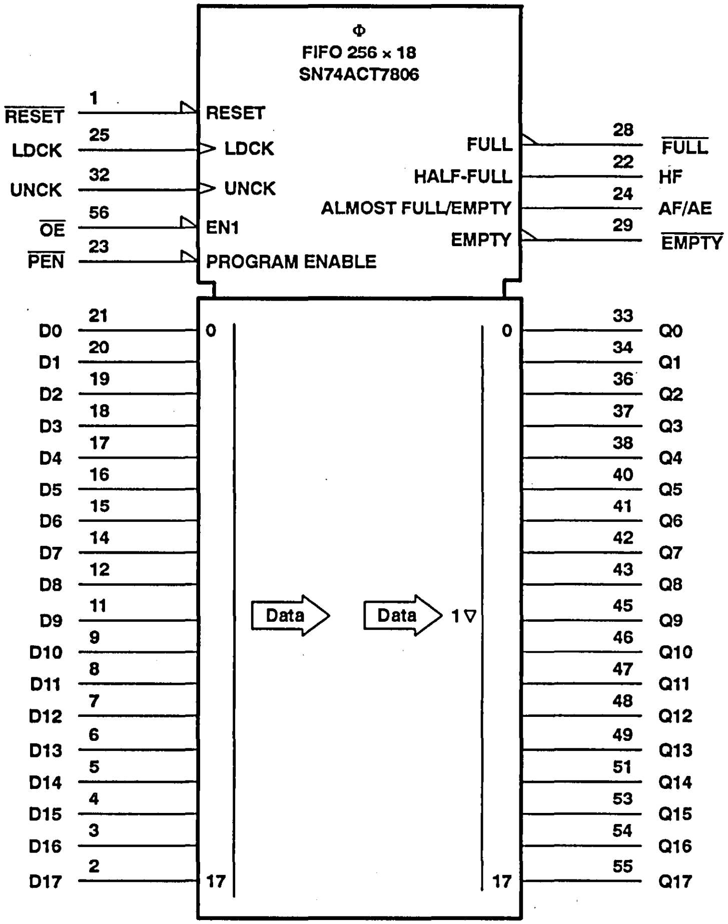
Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 128 or more words and is low when it contains 127 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (256 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (255 – Y) words.

A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

The SN74ACT7806 is characterized for operation from 0°C to 70°C.

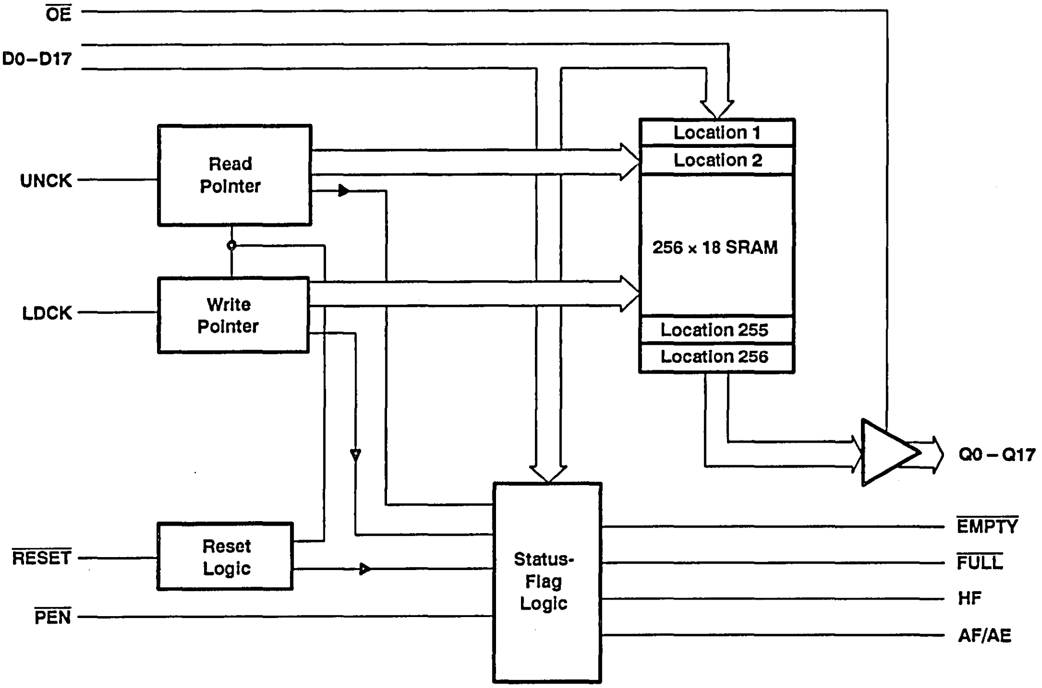
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 32 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (256 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
EMPTY	29	O	Empty flag. EMPTY is high when the FIFO memory is not empty; EMPTY is low when the FIFO memory is empty or upon assertion of RESET.
FULL	28	O	Full flag. FULL is high when the FIFO memory is not full or upon assertion of RESET; FULL is low when the FIFO memory is full.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when FULL is high.
OE	56	I	Output enable. When OE is high, the data outputs are in the high-impedance state.
PEN	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when PEN is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
RESET	1	I	Reset. A low level on this input resets the FIFO and drives FULL high and HF and EMPTY low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when EMPTY is high.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits, the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag will be high when the FIFO contains X or less words or (256 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D6 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 127 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 32, $\overline{\text{PEN}}$ must be held high.

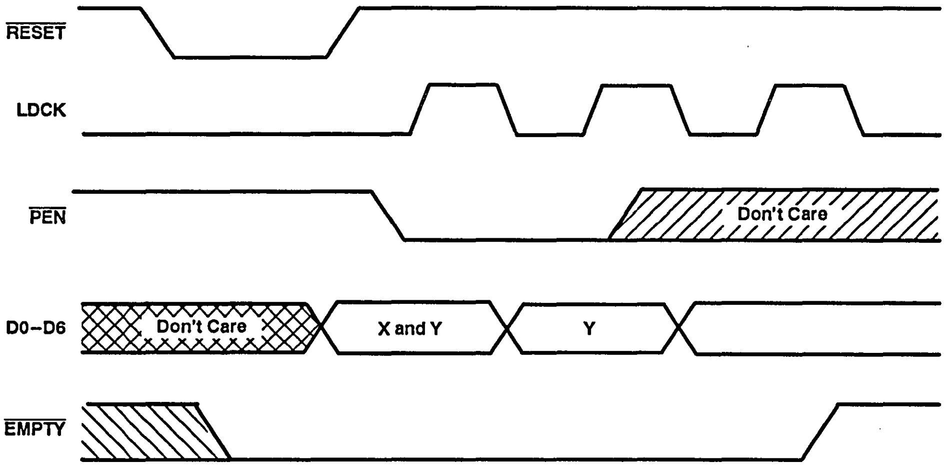
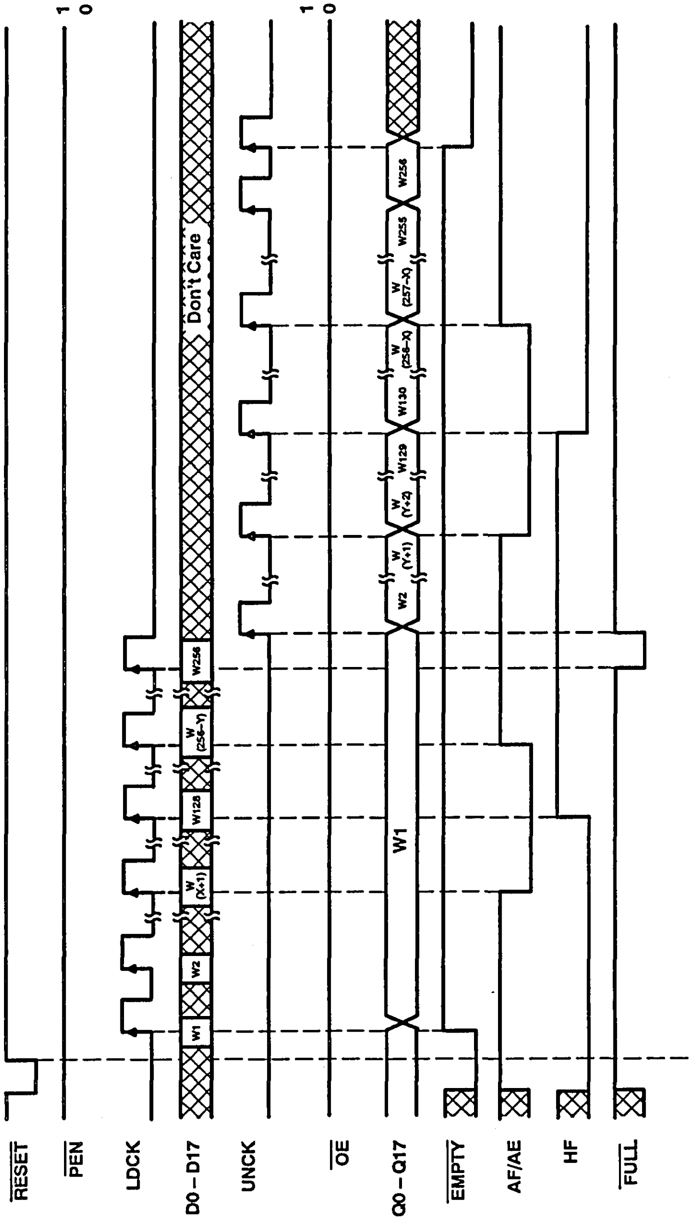


Figure 1. Programming X and Y Separately



Define the AF/AE Flag Using
the Default Value of X and Y

Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7806-20		'ACT7806-25		'ACT7806-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16	mA
		Flags		8		8		8	
f_{clock}	Clock frequency			50		40		25	MHz
t_w	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		$\overline{\text{PEN}}$ low	7		8		12		
		$\overline{\text{RESET}}$ low	10		10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		$\overline{\text{PEN}}$ before LDCK↑	5		5		5		
		LDCK inactive before $\overline{\text{RESET}}$ high	5		6		6		
t_h	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after $\overline{\text{RESET}}$ high	5		6		6		
		$\overline{\text{PEN}}$ low after LDCK↑	3		3		3		
		$\overline{\text{PEN}}$ high after LDCK↓	0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 5 and 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7806-20			'ACT7806-25		'ACT7806-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		25		MHz
t_{pd}	LDCK↑	Any Q	9		20	9	22	9	24	ns
	UNCK↑		6	11.5	15	6	18	6	20	
t_{pd}‡	UNCK↑			10.5						
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
t_{PHL}	UNCK↑		6		15	6	17	6	19	
	$\overline{\text{RESET}}$ low		4		16	4	18	4	20	
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6		15	6	17	6	19	ns
t_{PLH}	UNCK↑		6		15	6	17	6	19	
	$\overline{\text{RESET}}$ low		4		18	4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7		18	7	20	7	22	ns
	UNCK↑		7		18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low		2		10	2	12	2	14	
t_{PLH}	LDCK↑	HF	5		18	5	20	5	22	ns
t_{PHL}	UNCK↑		7		18	7	20	7	22	
	$\overline{\text{RESET}}$ low		3		12	3	14	3	16	
t_{en}	$\overline{\text{OE}}$	Any Q	2		9	2	10	2	11	ns
t_{dis}			2		10	2	11	2	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured at C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

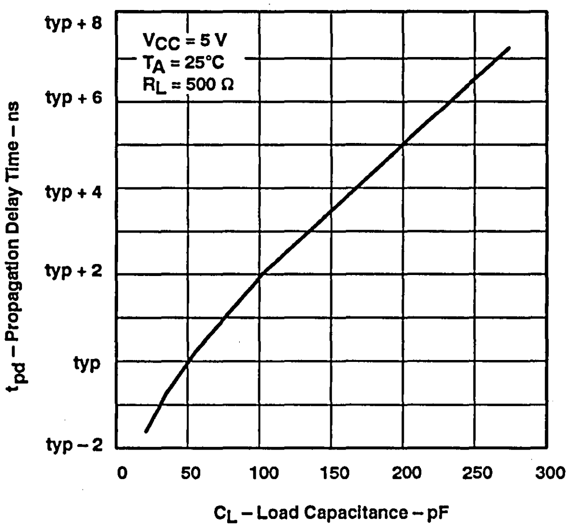


Figure 3

SUPPLY CURRENT
vs
CLOCK FREQUENCY

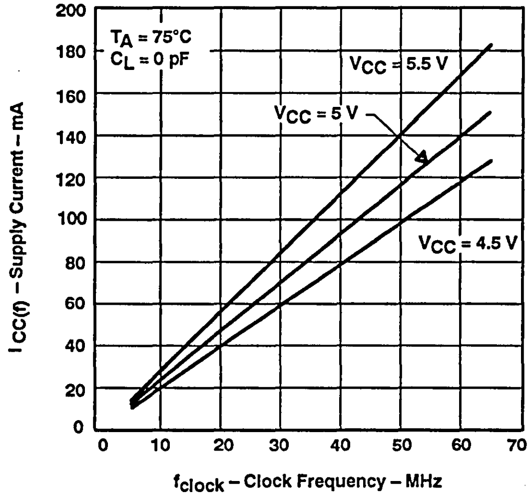


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

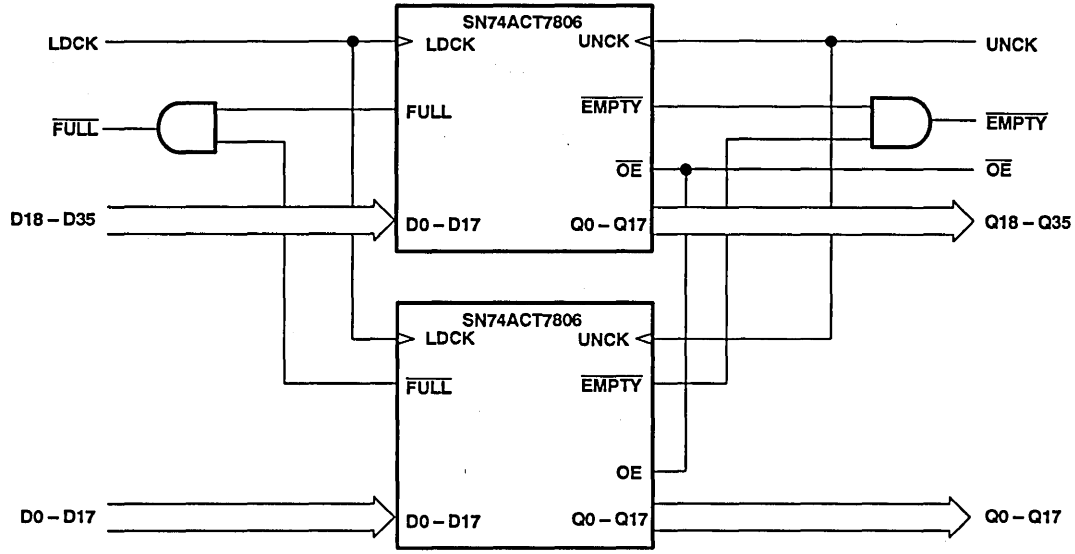
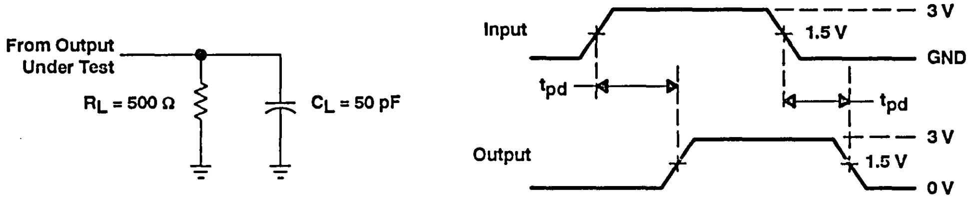


Figure 5. Word-Width Expansion: 256 Words by 36 Bits

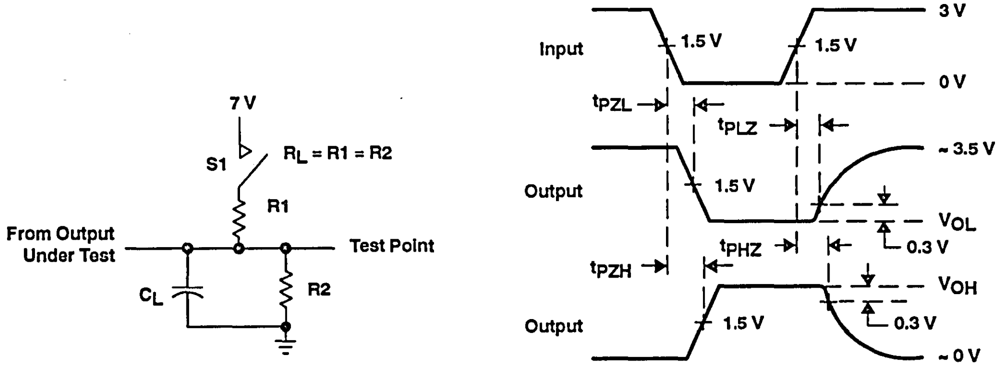
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 6. Standard CMOS Outputs ($\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, HF, AF/AE)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

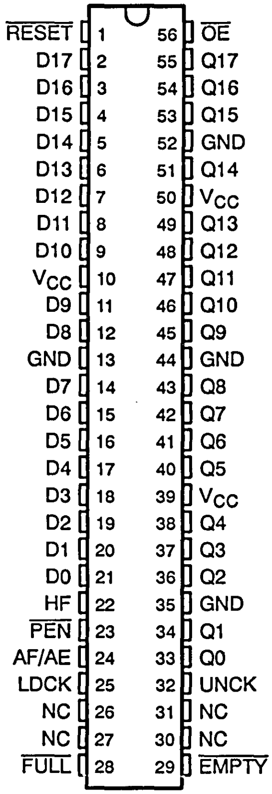
PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 7. 3-State Outputs (Any Q)

- **Member of the Texas Instruments Widebus™ Family**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **512 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7806 and SN74ACT7814**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7804 is a 512-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 512. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 256 or more words and is low when it contains 255 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (512 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (511 – Y) words.

A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

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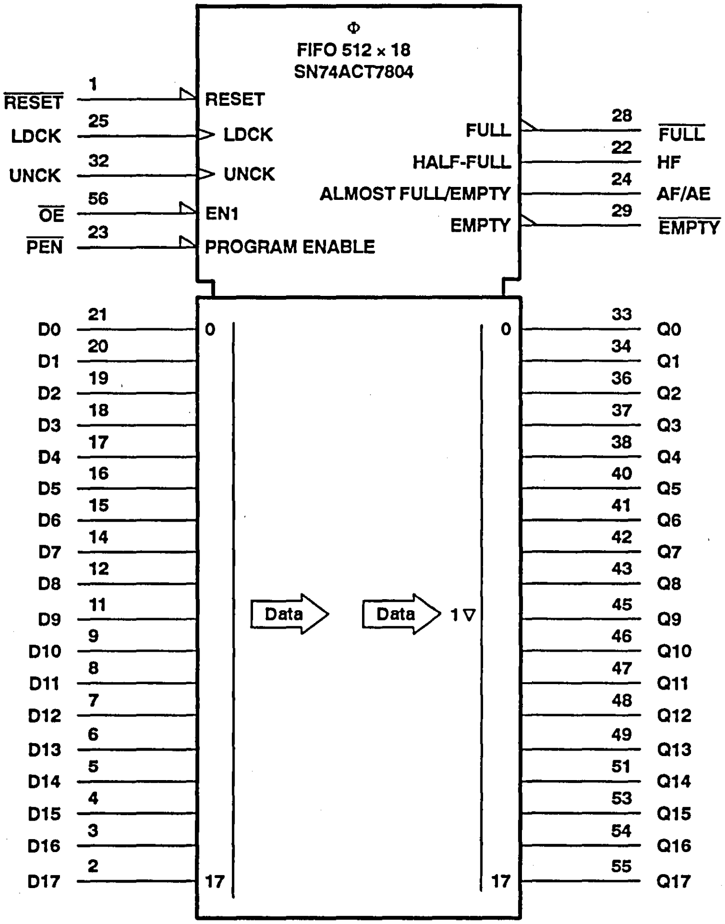
TEXAS INSTRUMENTS

description (continued)

The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) input is high.

The SN74ACT7804 is characterized for operation from 0°C to 70°C.

logic symbol†



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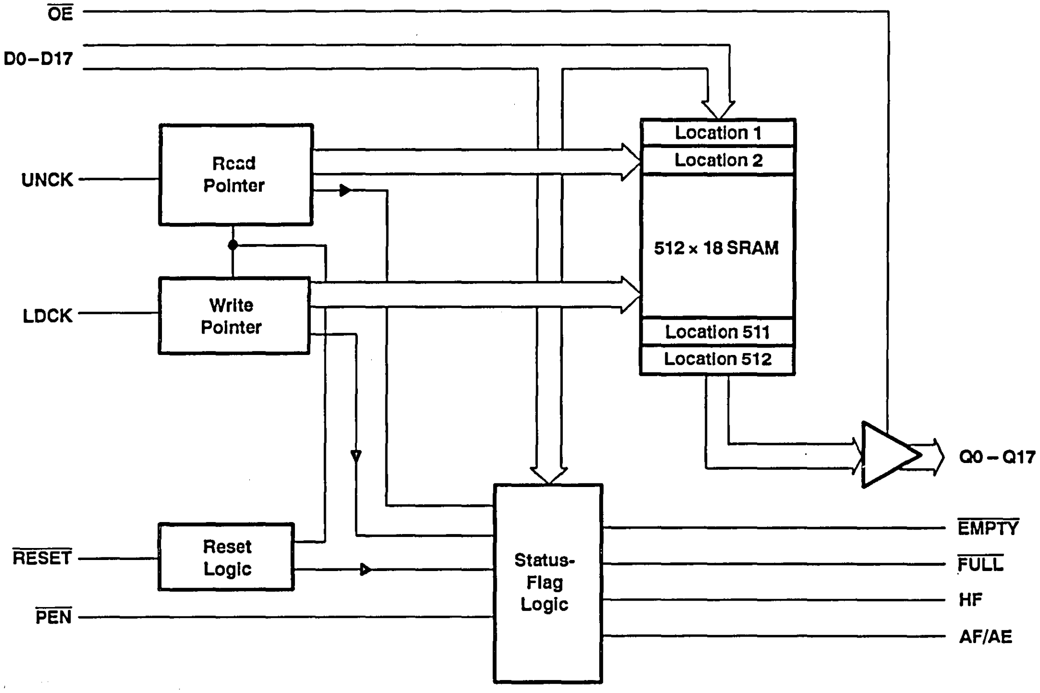
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 64 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (512 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	18-bit data input port
EMPTY	29	O	Empty flag. EMPTY is low when the FIFO is empty. A FIFO reset also causes EMPTY to go low.
FULL	28	O	Full flag. FULL is low when the FIFO is full. A FIFO reset causes FULL to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when FULL is high.
OE	56	I	Output enable. When OE is high, the data outputs are in the high-impedance state.
PEN	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when PEN is low and LDCK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
RESET	1	I	Reset. A low level on this input resets the FIFO and drives AF/AE and FULL high and HF and EMPTY low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when EMPTY is high.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or less words or (512 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0 – D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0 – D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 255 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 64, $\overline{\text{PEN}}$ must be held high.

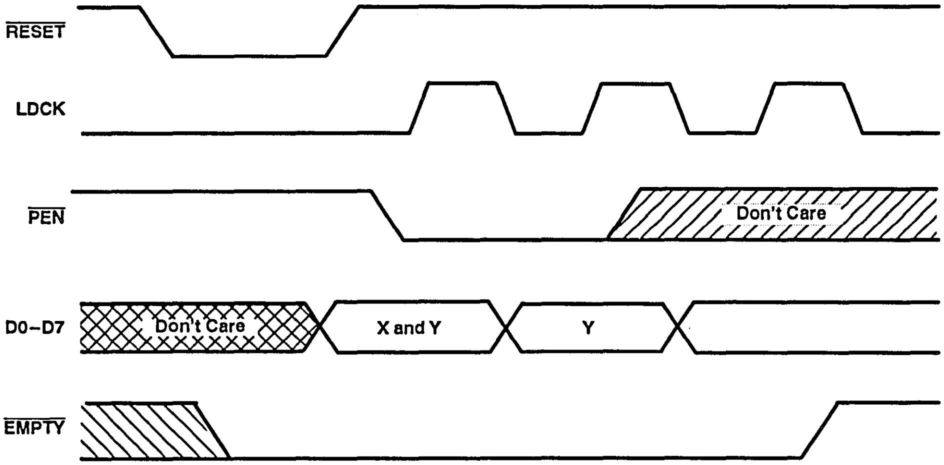
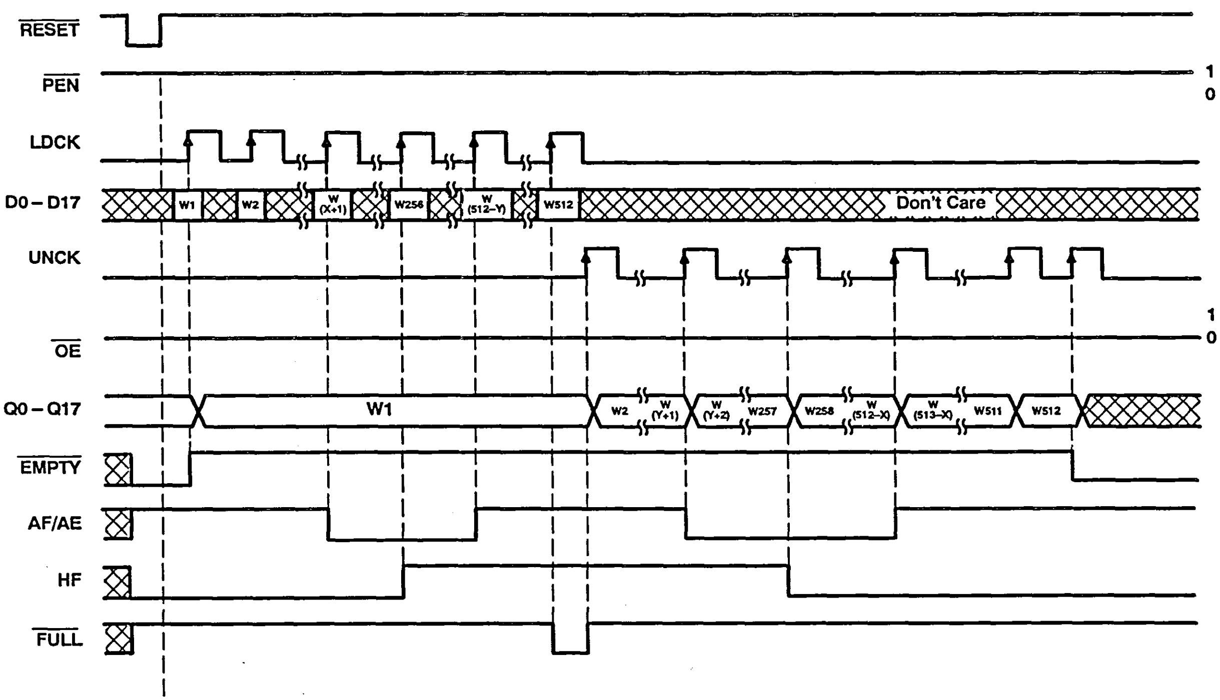


Figure 1. Programming X and Y Separately



Define the AF/AE Flag Using the Default Value of X and Y

Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7804-20		'ACT7804-25		'ACT7804-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16	mA
		Flags		8		8		8	
f_{clock}	Clock frequency			50		40		25	MHz
t_w	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		$\overline{\text{PEN}}$ low	7		8		12		
		$\overline{\text{RESET}}$ low	10		10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		$\overline{\text{PEN}}$ before LDCK↑	5		5		5		
		LDCK inactive before $\overline{\text{RESET}}$ high	5		6		6		
t_h	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after $\overline{\text{RESET}}$ high	5		6		6		
		$\overline{\text{PEN}}$ low after LDCK↑	3		3		3		
		$\overline{\text{PEN}}$ high after LDCK↓	0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 5 and 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7804-20			'ACT7804-25		'ACT7804-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		25		MHz
t_{pd}	LDCK↑	Any Q	9		20	9	22	9	24	ns
t_{pd}	UNCK↑		6	11.5	15	6	18	6	20	
t_{pd}‡	UNCK↑			10.5						
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	6		15	6	17	6	19	ns
t_{PHL}	UNCK↑		6		15	6	17	6	19	
t_{PHL}	$\overline{\text{RESET}}$ low		4		16	4	18	4	20	
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6		15	6	17	6	19	ns
t_{PLH}	UNCK↑		6		15	6	17	6	19	
t_{PLH}	$\overline{\text{RESET}}$ low		4		18	4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7		18	7	20	7	22	ns
t_{pd}	UNCK↑		7		18	7	20	7	22	
t_{PLH}	$\overline{\text{RESET}}$ low		2		10	2	12	2	14	
t_{PLH}	LDCK↑	HF	5		18	5	20	5	22	ns
t_{PHL}	UNCK↑		7		18	7	20	7	22	
t_{PHL}	$\overline{\text{RESET}}$ low		3		12	3	14	3	16	
t_{en}	$\overline{\text{OE}}$	Any Q	2		9	2	10	2	11	ns
t_{dis}			2		10	2	11	2	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This parameter is measured at C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

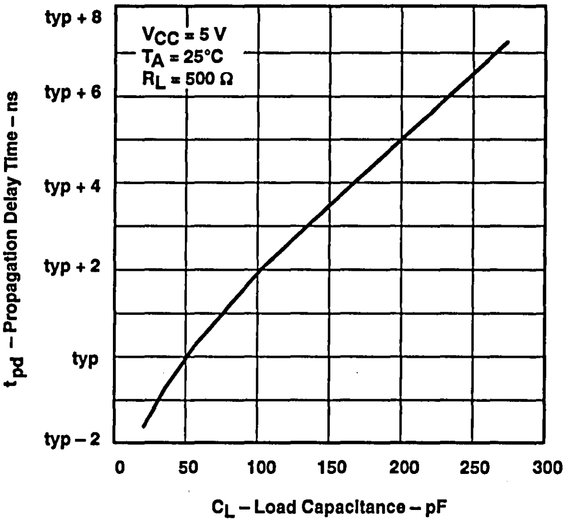


Figure 3

SUPPLY CURRENT
vs
CLOCK FREQUENCY

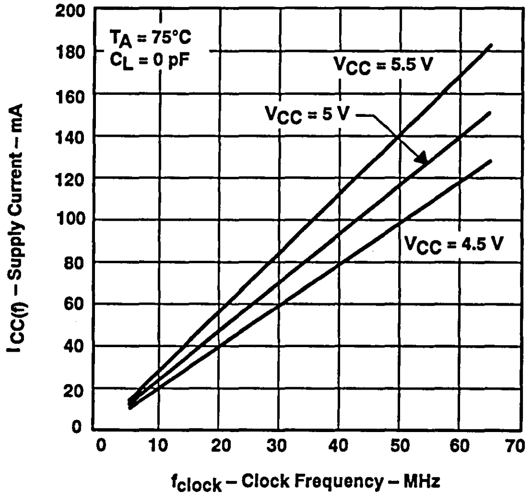


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

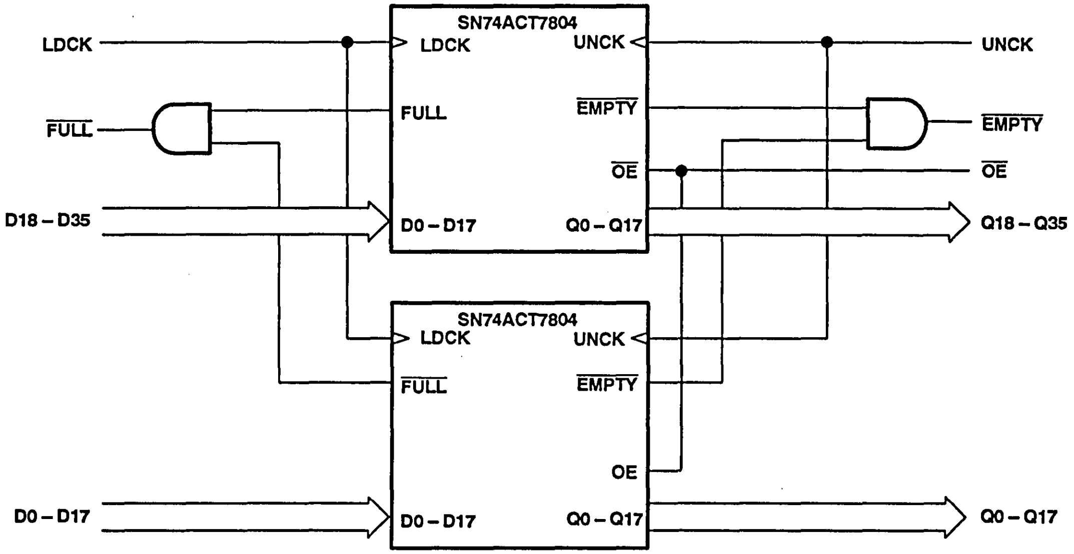
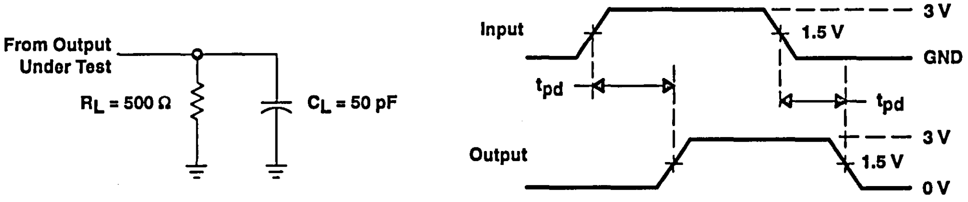


Figure 5. Word-Width Expansion: 512 Words by 36 Bits

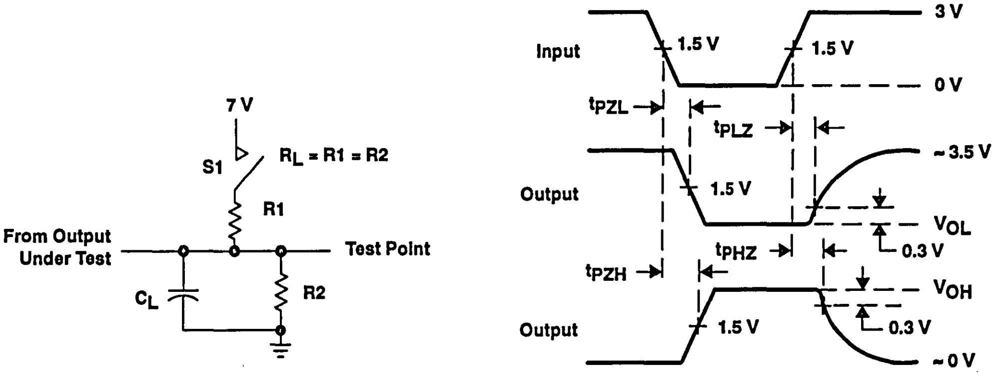
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 6. Standard CMOS Outputs ($\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, HF, AF/AE)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

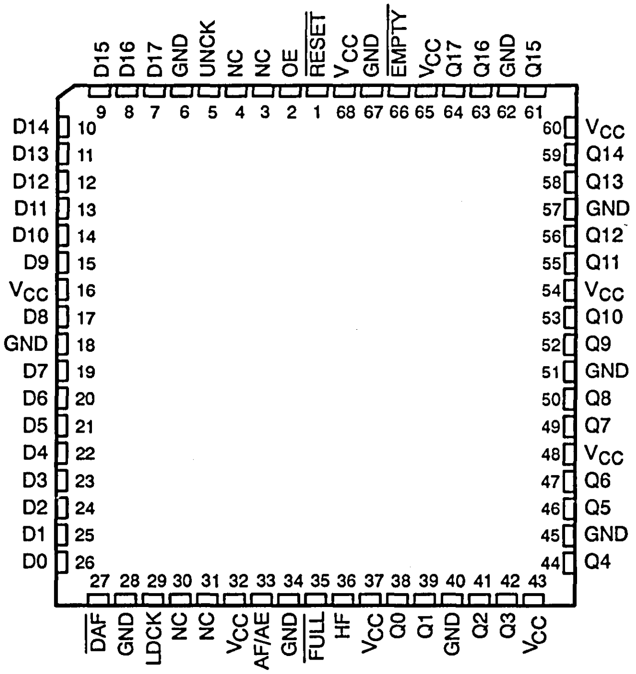
Figure 7. 3-State Outputs (Any Q)

SN74ACT7802
1024 × 18 FIRST-IN, FIRST-OUT MEMORY

SCAS187A – AUGUST 1990 – REVISED AUGUST 1993

- Load and Unload Clocks Can Be Asynchronous or Coincident
- Low-Power Advanced CMOS Technology
- 1024 Words × 18 Bits
- Programmable Almost-Full/Almost-Empty Flag
- Empty, Full, and Half-Full Flags
- Fast Access Times of 30 ns With a 50-pF Load
- Fall-Through Time . . . 20 ns Typical
- Data Rates From 0 to 40 MHz
- High-Output Drive for Direct Bus Interface
- 3-State Outputs
- Available in 68-Pin PLCC (FN) Packages or 80-Pin Thin Quad Flat (PN) Packages

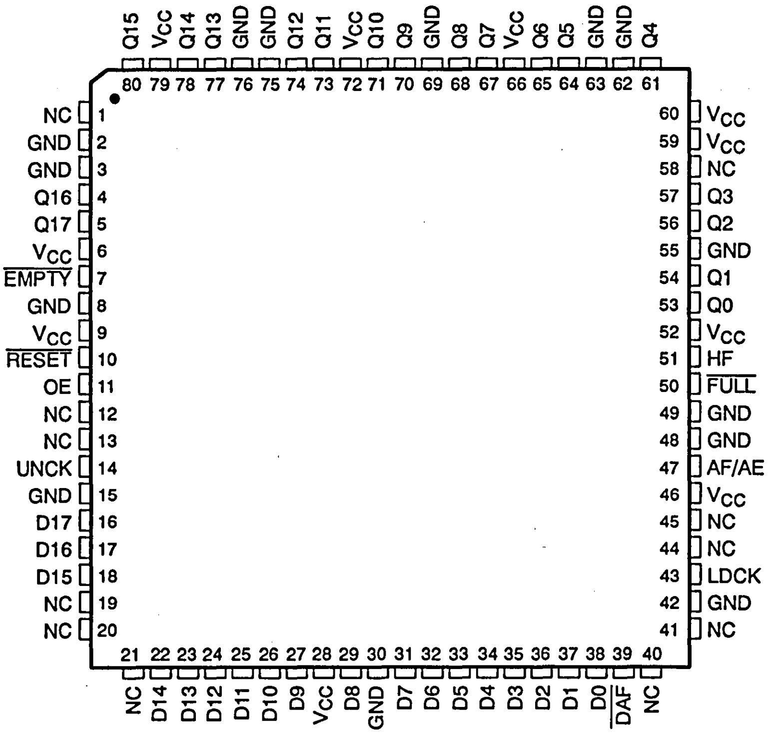
FN PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS

PN PACKAGE
(TOP VIEW)



NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7802 is a 1024-word by 18-bit FIFO for high-speed applications. It processes data in a bit-parallel format at rates up to 40 MHz and access times of 30 ns.

Data is written into the FIFO memory on a low-to-high transition on the load-clock (LDCK) input and is read out on a low-to-high transition on the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, LDCK has no effect on the data in the memory; when the memory is empty, UNCK has no effect.

A low level on the reset ($\overline{\text{RESET}}$) input resets the FIFO internal clock stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The Q outputs are noninverting and are in the high-impedance state when the output-enable (OE) input is low.

When writing to the FIFO after a reset pulse or when the FIFO is empty, the first active transition on LDCK drives $\overline{\text{EMPTY}}$ high and causes the first word written to the FIFO to appear on the Q outputs. Therefore, an active transition on UNCK is not required to read the first word written to the FIFO. Each subsequent read from the FIFO requires an active transition on UNCK.

The SN74ACT7802 can be cascaded in the word-width direction but not in the word-depth direction.

The SN74ACT7802 is characterized for operation from 0°C to 70°C.

offset value values for AF/AE

The FIFO memory status is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full; the $\overline{\text{EMPTY}}$ output is low when the memory is empty. The HF output is high when the memory contains 512 or more words and low when it contains less than 512 words. The level of the AF/AE flag is determined by both the number of words in the FIFO and a user-definable offset X. AF/AE is high when the FIFO is almost full or almost empty, i.e., when it contains X or less words or (1024 – X) or more words. The almost-full/almost-empty offset value is either user-defined or the default value of 256; it is programmed during each reset cycle as follows:

user-defined X:

Take $\overline{\text{DAF}}$ from high to low.

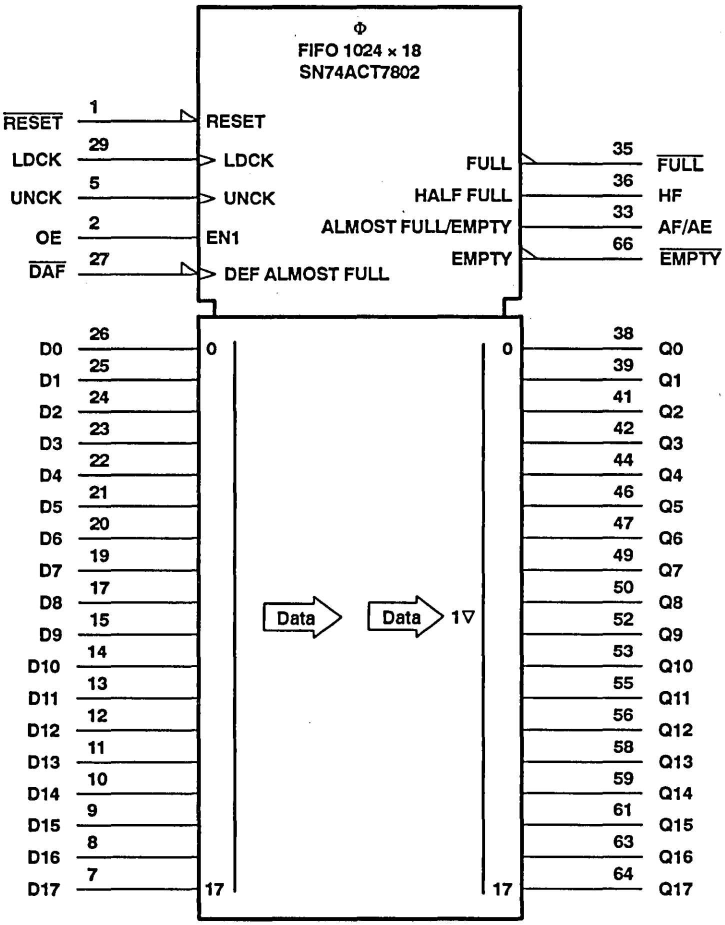
If $\overline{\text{RESET}}$ is not already low, take $\overline{\text{RESET}}$ low.

With $\overline{\text{DAF}}$ held low, take $\overline{\text{RESET}}$ high. This defines the AF/AE flag using X.

default X:

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

logic symbol†



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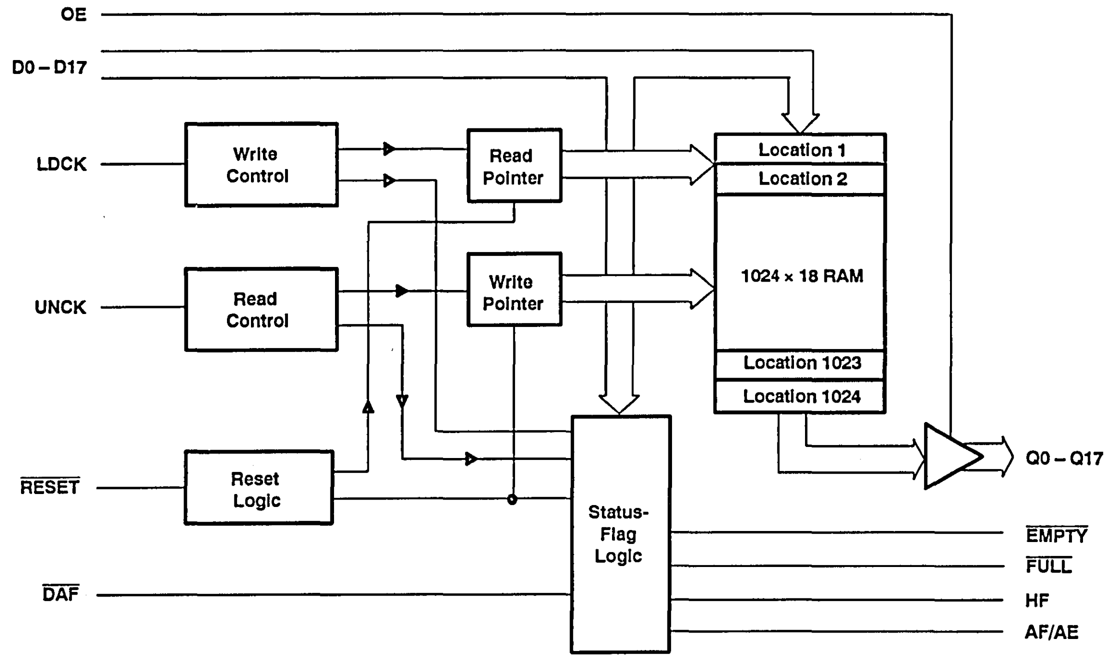
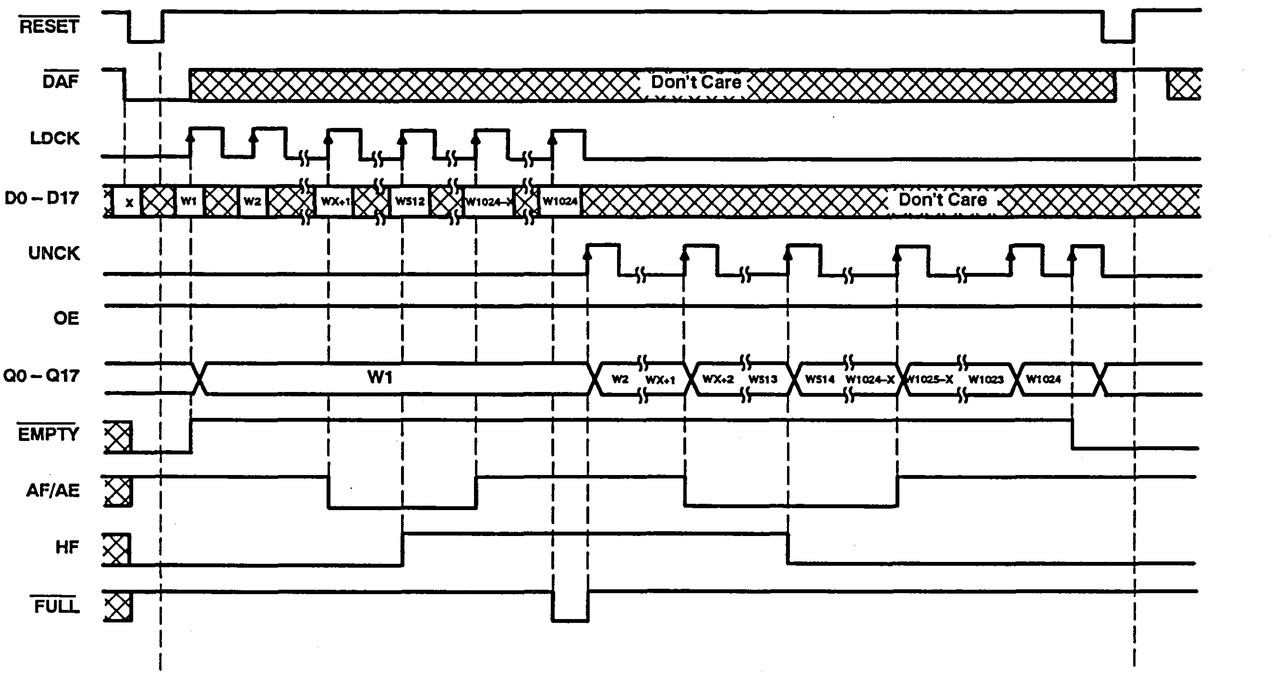
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AF/AE	33	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 256 can be used for the almost-empty almost-full offset (X). AF/AE is high when memory contains X or less words or (1024 – X) or more words. AF/AE is high after reset.
$\overline{\text{DAF}}$	27	I	Define almost full flag. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With DAF held low, a low pulse on RESET defines AF/AE using X.
D0–D17	26, 19, 17, 15–7	I	18-bit data input port
$\overline{\text{EMPTY}}$	66	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	35	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	36	O	Half-full flag. HF is high when the FIFO memory contains 512 or more words. HF is low after reset.
LDCK	29	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
OE	2	I	Output enable. When OE is low, the data outputs are in the high-impedance state.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	5	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.



Define the AF/AE Offset Value (X)
Using the Data on D0 – D8

Define the AF/AE Offset Value (X)
Using the Default Value of 256

Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7802-25		'ACT7802-40		'ACT7802-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current			−8		−8		−8	mA
I_{OL}	Low-level output current			16		16		16	mA
f_{clock}	Clock frequency		40		25		16.7		MHz
t_w	Pulse duration	LDCK high or low	10		14		20		ns
		UNCK high or low	10		14		20		
		$\overline{\text{DAF}}$ high	10		10		10		
		$\overline{\text{RESET}}$ low	20		25		25		
t_{su}	Setup time	D0–D7 before LDCK↑	4		5		5		ns
		$\overline{\text{RESET}}$ inactive (high) before LDCK↑	5		5		5		
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$↓	5		5		5		
		Define AF/AE: $\overline{\text{DAF}}$↓ before $\overline{\text{RESET}}$↑	7		7		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ high before $\overline{\text{RESET}}$↑	5		5		5		
t_h	Hold time	D0–D7 after LDCK↑	1		2		2		ns
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$↓	0		0		0		
		Define AF/AE: $\overline{\text{DAF}}$ low after $\overline{\text{RESET}}$↑	0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ high after $\overline{\text{RESET}}$↑	0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}‡	V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}‡	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz			4		pF
C_o	V_O = 0,	f = 1 MHz			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7802-25			'ACT7802-40		'ACT7802-60		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		40			25		16.7		MHz
t_{pd}	LDCK↑	Any Q	8	20	30	8	35	8	45	ns
t_{pd}	UNCK↑	Any Q	12		30	12	35	12	45	ns
t_{pd}§	UNCK↑	Any Q		21						ns
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	4		18	4	20	4	22	ns
t_{PHL}	UNCK↑		2		18	2	20	2	22	
t_{PHL}	$\overline{\text{RESET}}$↓	$\overline{\text{EMPTY}}$	2		18	2	20	2	22	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	4		18	4	20	4	22	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$	4		17	4	19	4	21	ns
	$\overline{\text{RESET}}$↓		2		17	2	19	2	21	
t_{pd}	LDCK↑	AF/AE	2		20	2	22	2	24	ns
	UNCK↑		2		20	2	22	2	24	
t_{PLH}	$\overline{\text{RESET}}$↓	AF/AE	2		17	2	19	2	21	ns
t_{PLH}	LDCK↑	HF	2		18	2	20	2	22	ns
t_{PHL}	UNCK↑	HF	2		18	2	20	2	22	ns
	$\overline{\text{RESET}}$↓		2		17	2	19	2	21	
t_{en}	OE	Any Q	2		12	2	14	2	16	ns
t_{dis}	OE	Any Q	2		14	2	16	2	18	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I_{CC} tested with outputs open
§ This parameter is measured with C_L = 30 pF (see Figure 1).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitancer per channel	CL = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

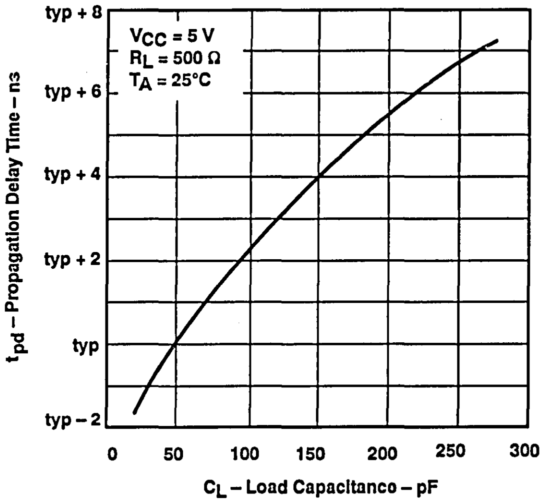


Figure 1

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

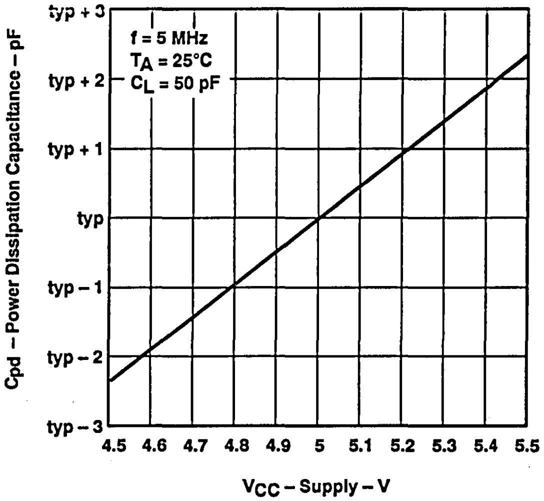


Figure 2

TYPICAL CHARACTERISTICS

calculating power dissipation

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

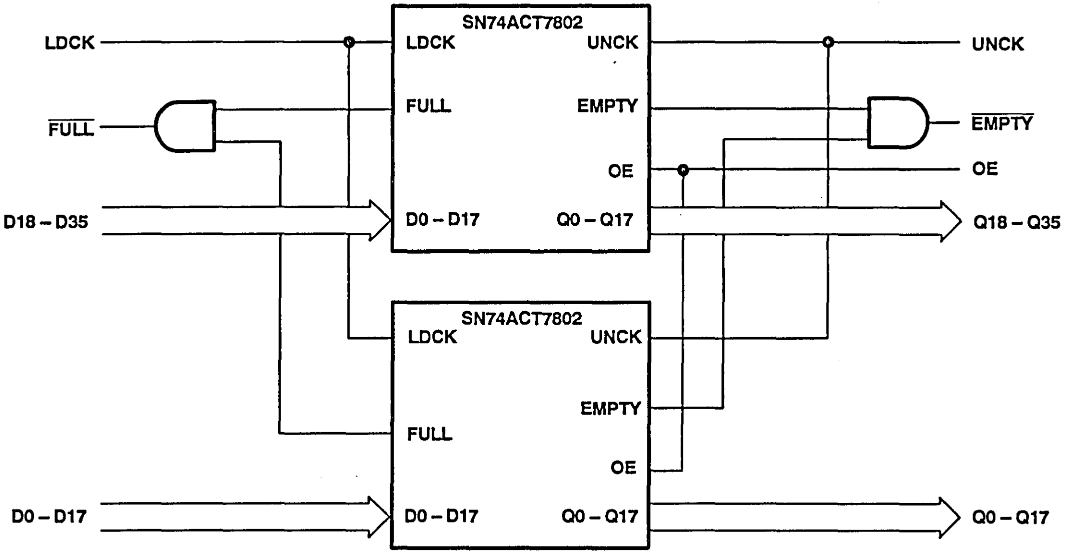
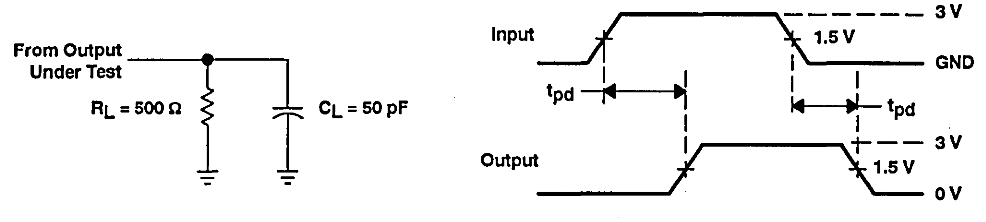


Figure 3. Word-Width Expansion: 1024 Word by 36 Bit

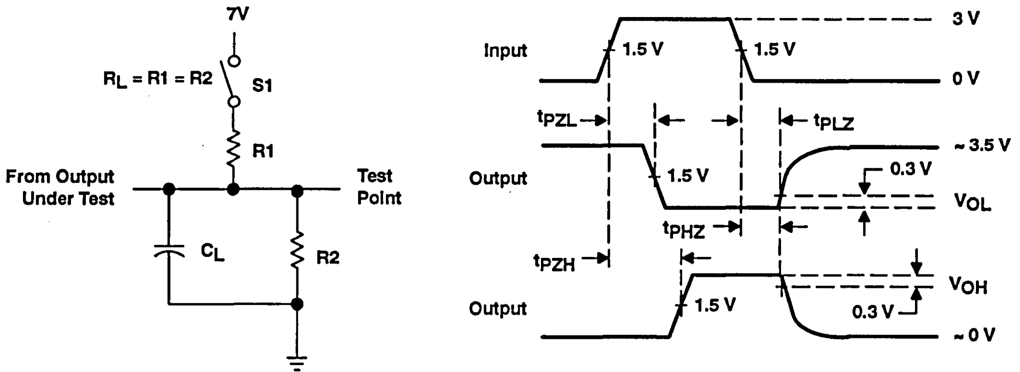
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 4. Standard CMOS Outputs ($\overline{\text{FULL}}$, AF/AE, $\overline{\text{EMPTY}}$)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

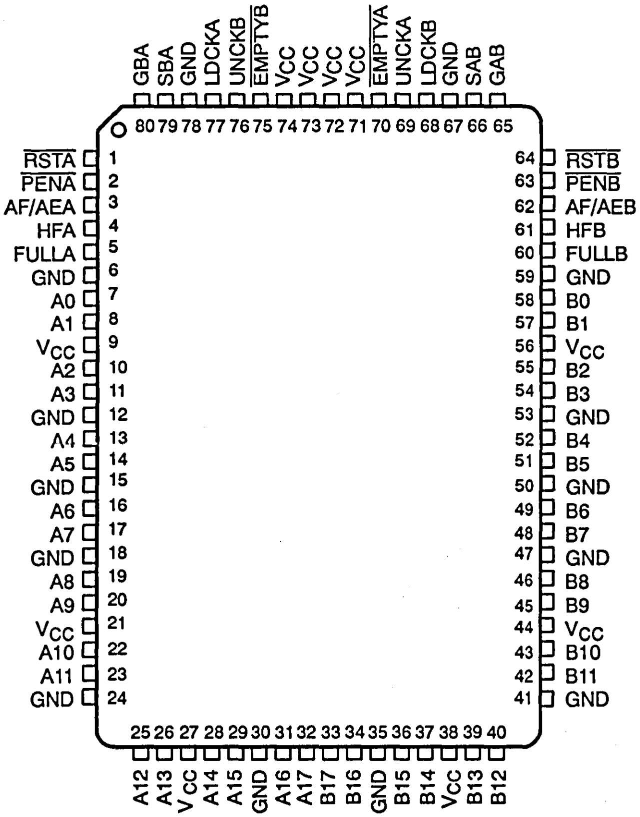
Figure 5. 3-State Outputs (Any Q)

SN74ABT7820
512 × 18 × 2 FIRST-IN, FIRST-OUT MEMORY

SCAS206A – AUGUST 1991 – REVISED AUGUST 1992

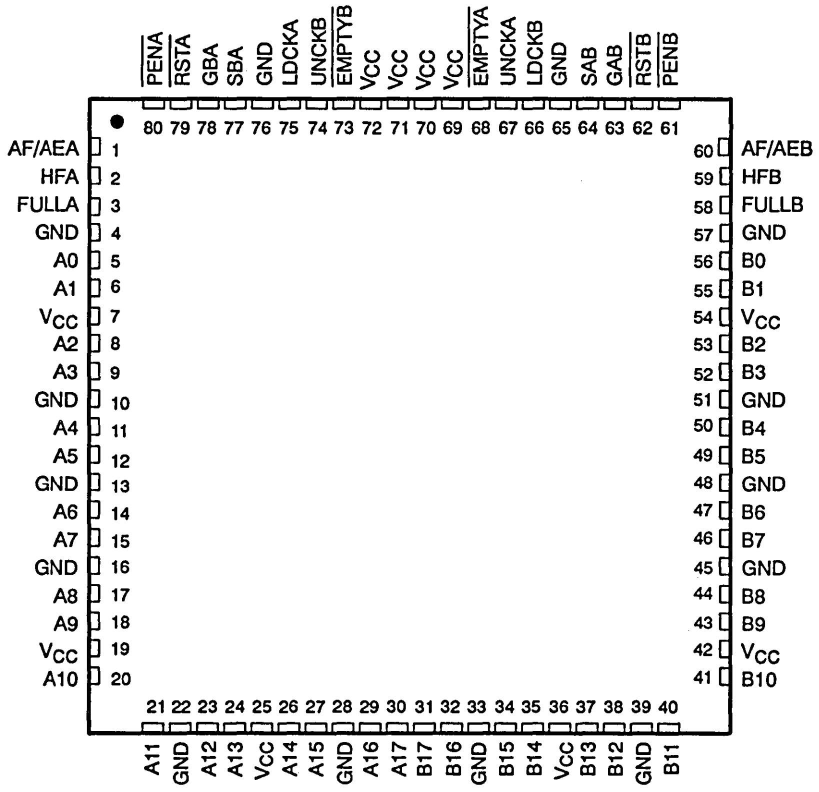
- Member of the Texas Instruments Widebus ™ Family
- Independent Asynchronous Inputs and Outputs
- Produced in Advanced BiCMOS Technology
- Two Separate 512 × 18 FIFOs Buffering Data in Opposite Directions
- Programmable Almost-Full/Almost-Empty Flags
- Empty, Full, and Half-Full Flags
- Fast Access Times of 12 ns With a 50-pF Load and Simultaneous Switching Data Outputs
- Supports Clock Rates up to 67 MHz
- Available in 80-Pin Quad Flat Packages (PH) and Space-Saving 80-Pin Thin Quad Flat Packages (PN)

PH PACKAGE
(TOP VIEW)



Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ABT7820 is arranged as two 512 by 18-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 67 MHz with access times of 12 ns in a bit-parallel format.

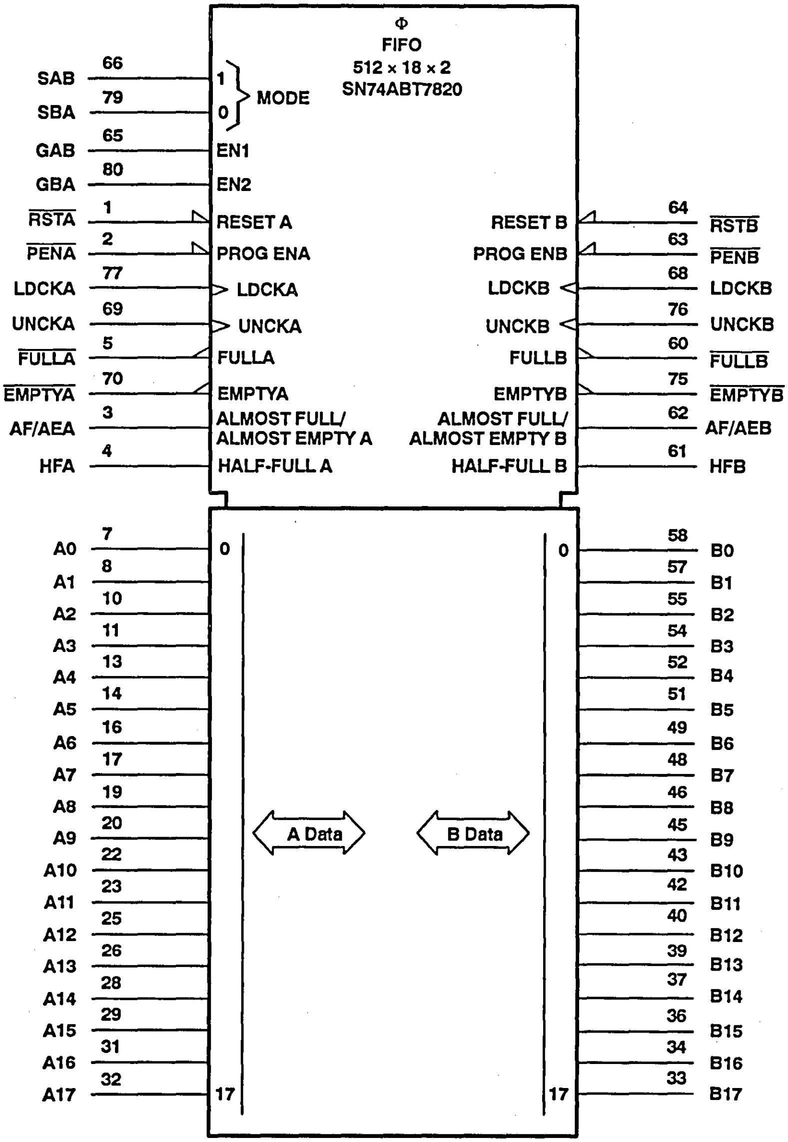
The SN74ABT7820 consists of bus transceiver circuits, two 512 × 18 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable inputs GAB and GBA control the transceiver functions. The SAB and SBA control inputs select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the eight fundamental bus-management functions that can be performed with the SN74ABT7820.

The SN74ABT7820 is characterized for operation from 0°C to 70°C.

Terminal Functions

TERMINAL	I/O	DESCRIPTION
A0–A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFO A almost-full/almost-empty flag. Depth offset values can be programmed for AF/AEA or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when FIFO A contains X or less words or (512 – Y) or more words. AF/AEA is set high after FIFO A is reset.
AF/AEB	O	FIFO B almost-full/almost-empty flag. Depth offset values can be programmed for AF/AEB or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when FIFO B contains X or less words or (512 – Y) or more words. AF/AEB is set high after FIFO B is reset.
B0–B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
$\overline{\text{EMPTYA}}$	O	FIFO A empty flag. $\overline{\text{EMPTYA}}$ is low when FIFO A is empty and high when FIFO A is not empty. $\overline{\text{EMPTYA}}$ is set low after FIFO A is reset.
$\overline{\text{EMPTYB}}$	O	FIFO B empty flag. $\overline{\text{EMPTYB}}$ is low when FIFO B is empty and high when FIFO B is not empty. $\overline{\text{EMPTYB}}$ is set low after FIFO B is reset.
$\overline{\text{FULLA}}$	O	FIFO A full flag. $\overline{\text{FULLA}}$ is low when FIFO A is full and high when FIFO A is not full. $\overline{\text{FULLA}}$ is set high after FIFO A is reset.
$\overline{\text{FULLB}}$	O	FIFO B full flag. $\overline{\text{FULLB}}$ is low when FIFO B is full and high when FIFO B is not full. $\overline{\text{FULLB}}$ is set high after FIFO B is reset.
GAB	I	Port-B output enable. B0–B17 outputs are active when GAB is high and in the high-impedance state when GAB is low.
GBA	I	Port-A output enable. A0–A17 outputs are active when GBA is high and in the high-impedance state when GBA is low.
HFA	O	FIFO A half-full flag. HFA is high when FIFO A contains 256 or more words and is low when FIFO A contains 255 or less words. HFA is set low after FIFO A is reset.
HFB	O	FIFO B half-full flag. HFB is high when FIFO B contains 256 or more words and is low when FIFO B contains 255 or less words. HFB is set low after FIFO B is reset.
LDCKA	I	FIFO A load clock. Data is written into FIFO A on a low-to-high transition of LDCKA when $\overline{\text{FULLA}}$ is high. The first word written into an empty FIFO A is sent directly to the FIFO A data outputs.
LDCKB	I	FIFO B load clock. Data is written into FIFO B on a low-to-high transition of LDCKB when $\overline{\text{FULLB}}$ is high. The first word written into an empty FIFO B is sent directly to the FIFO B data outputs.
$\overline{\text{PENA}}$	I	FIFO A program enable. After reset and before a word is written into FIFO A, the binary value on A0–A7 is latched as an AF/AEA offset value when $\overline{\text{PENA}}$ is low and LDCKA is high.
$\overline{\text{PENB}}$	I	FIFO B program enable. After reset and before a word is written into FIFO B, the binary value on B0–B7 is latched as an AF/AEB offset value when $\overline{\text{PENB}}$ is low and LDCKB is high.
$\overline{\text{RSTA}}$	I	FIFO A reset. A low level on $\overline{\text{RSTA}}$ resets FIFO A forcing $\overline{\text{EMPTYA}}$ low, HFA low, $\overline{\text{FULLA}}$ high, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFO B reset. A low level on $\overline{\text{RSTB}}$ resets FIFO B forcing $\overline{\text{EMPTYB}}$ low, HFB low, $\overline{\text{FULLB}}$ high, and AF/AEB high.
SAB	I	Port-B read select. SAB selects the source of B0–B17 read data. A low level selects real-time data from A0–A17. A high level selects the FIFO A output.
SBA	I	Port-A read select. SBA selects the source of A0–A17 read data. A low level selects real-time data from B0 – B17. A high level selects the FIFO B output.
UNCKA	I	FIFO A unload clock. Data is read from FIFO A on a low-to-high transition of UNCKA when $\overline{\text{EMPTYA}}$ is high.
UNCKB	I	FIFO B unload clock. Data is read from FIFO B on a low-to-high transition of UNCKB when $\overline{\text{EMPTYB}}$ is high.

logic symbol†



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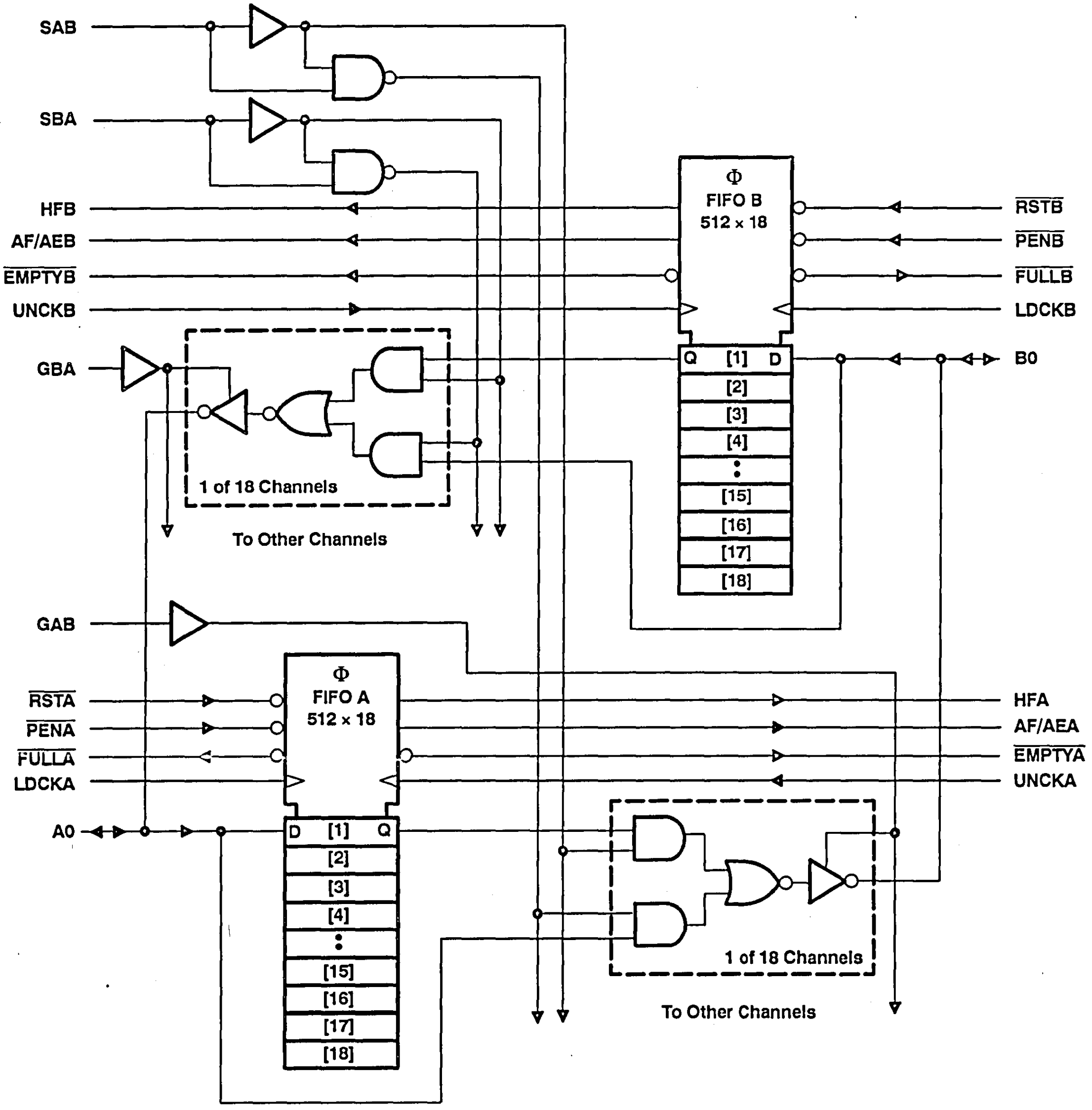
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



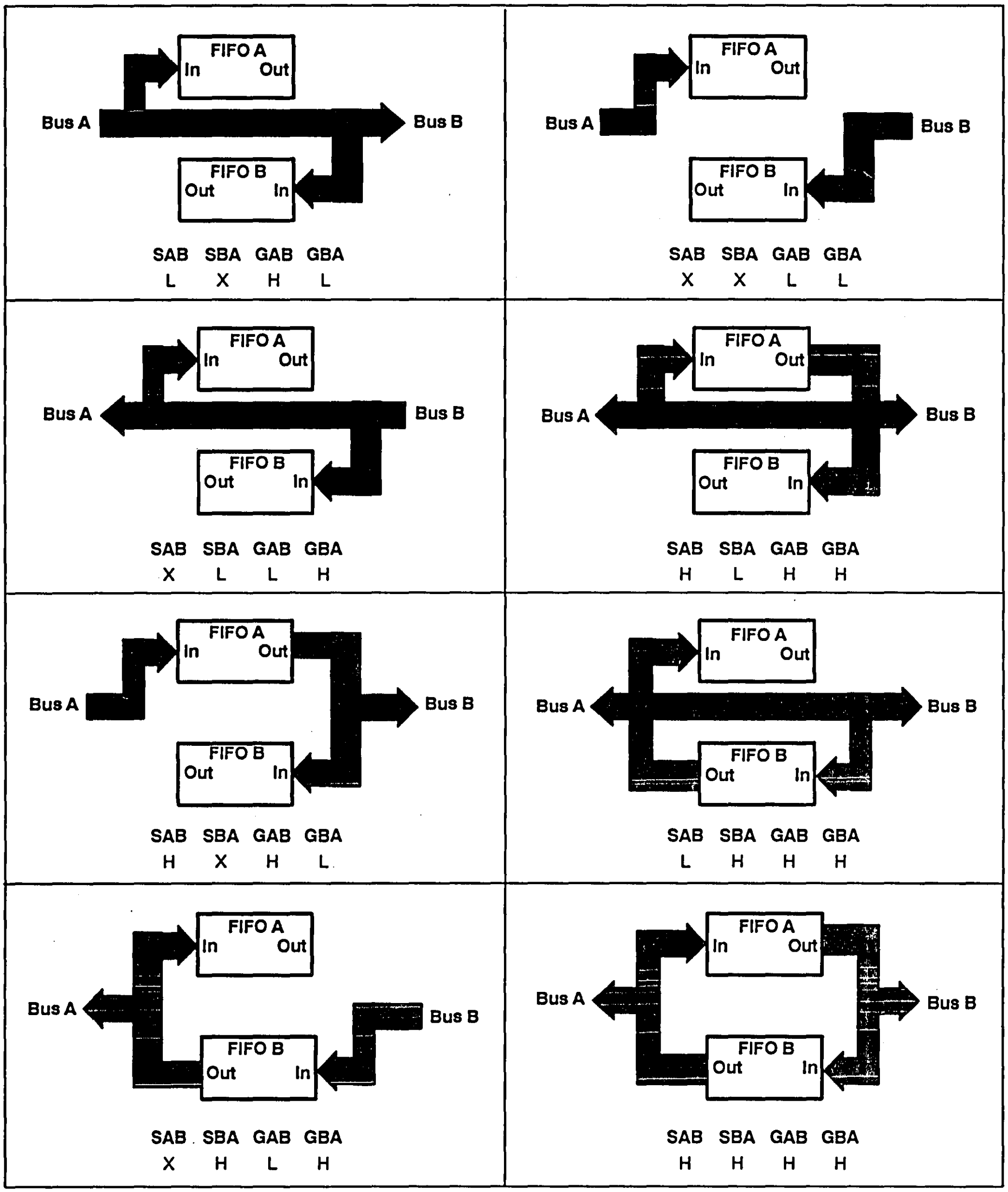


Figure 1. Bus-Management Functions

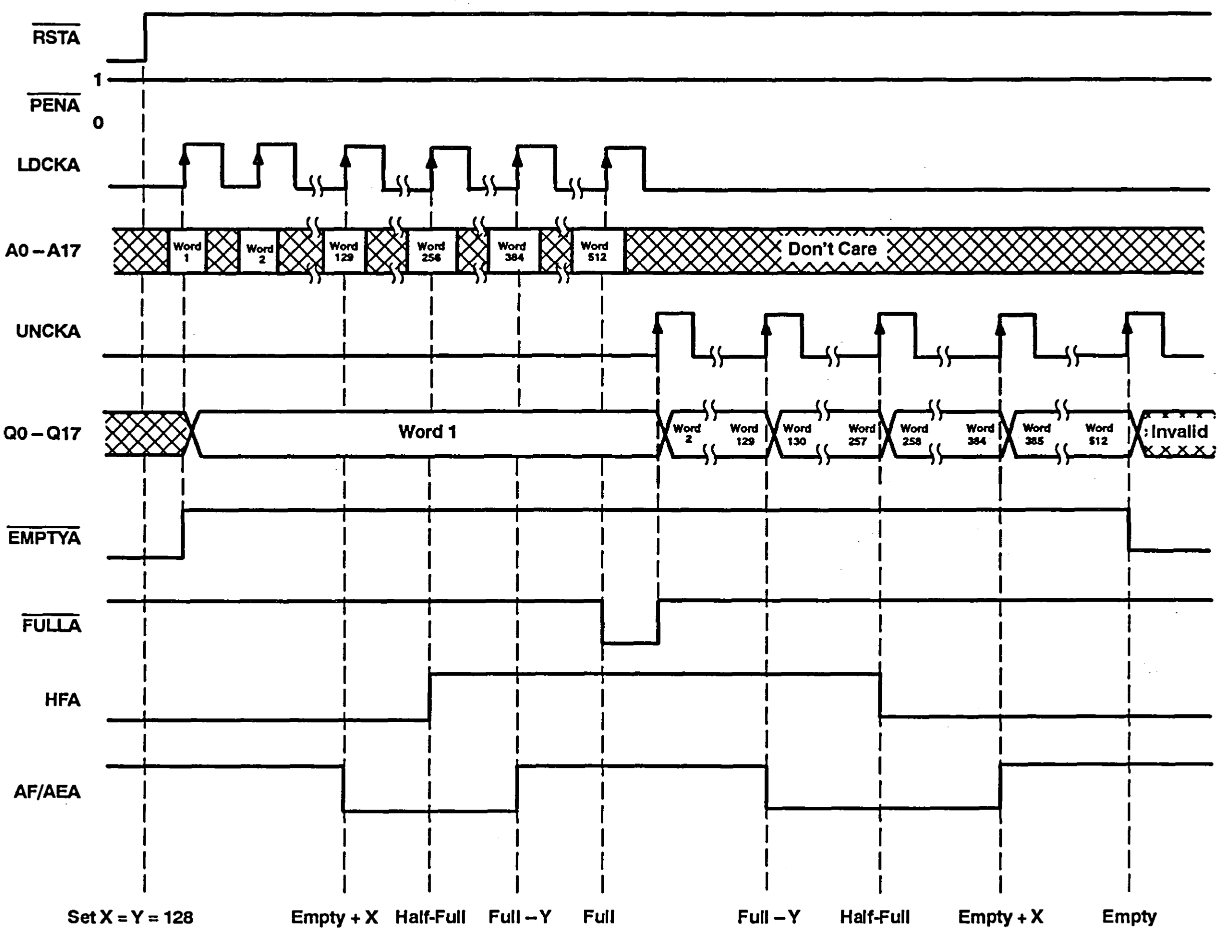
SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SBA	SAB	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
H	L	FIFO B to A bus	Real-time A to B bus
L	H	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
GBA	GAB	A BUS	B BUS
L	L	Isolation/input to A bus	Isolation/input to B bus
H	L	A bus enabled	Isolation/input to B bus
L	H	Isolation/input to A bus	B bus enabled
H	H	A bus enabled	B bus enabled

timing diagram for FIFO A†



† SAB = GAB = H, GBA = L

Operation of FIFO B is identical to that of FIFO A

offset values for AF/AE

The almost-full/almost-empty flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). The offsets of a flag can be programmed from the input of its FIFO after it is reset and before any data is written to its memory. An AF/AE flag is high when its FIFO contains X or less words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ can be brought low after FIFO A is reset and only when LDCKA is low. On the following low-to-high transition of LDCKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of LDCKA reprograms Y to the binary value on A0–A7 at the time of the second LDCKA low-to-high transition.

$\overline{\text{PENA}}$ can be brought back high only when LDCKA is low during the first two LDCKA cycles. $\overline{\text{PENA}}$ can be brought high at any time after the second LDCKA pulse returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 128 for AF/AEA, $\overline{\text{PENA}}$ must be tied high. No data is stored in the FIFO when its AF/AE offsets are programmed. The AF/AEB flag is programmed in the same manner. $\overline{\text{PENB}}$ enables LDCKB to program the AF/AEB offset values taken from B0–B7.

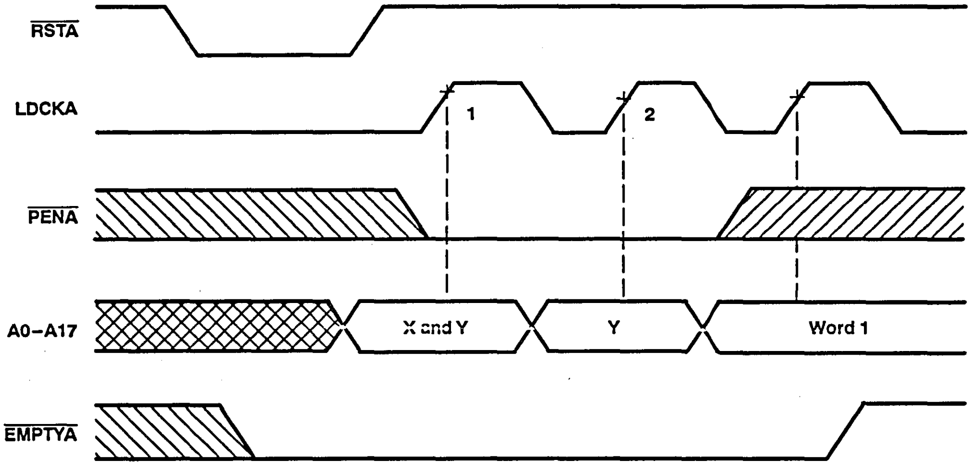


Figure 2. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O .... 48 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	4.5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−12	mA
I_{OL}	Low-level output current			24	mA
Δt/Δv	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA		2.5			V
		V_{CC} = 5 V, I_{OH} = −3 mA		3			
		V_{CC} = 4.5 V, I_{OH} = −12 mA		2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 24 mA				0.55	V
I_I		V_{CC} = 5.5 V, V_I = V_{CC} or GND				±5	μA
I_{OZH}§		V_{CC} = 5.5 V, V_O = 2.7 V				50	μA
I_{OZL}§		V_{CC} = 5.5 V, V_O = 0.5 V				−50	μA
I_O¶		V_{CC} = 5.5 V, V_O = 2.5 V		−40	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			15	mA
			Outputs low			95	
			Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V			6		pF
C_o	Flags	V_O = 2.5 V or 0.5 V			4		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			'ABT7820-15		'ABT7820-20		'ABT7820-25		'ABT7820-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		40		33		MHz
t_w	Pulse duration	LDCKA, LDCKB high	4		6		9		11		ns
		LDCKA, LDCKB low	4		6		9		11		
		UNCKA, UNCKB high	4		6		9		11		
		UNCKA, UNCKB low	4		6		9		11		
		$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$ low	6		8		10		12		
t_{su}	Setup time	A0–A17 before LDCKA↑ and B0–B17 before LDCKB↑	3		4		4		4		ns
		$\overline{\text{PENA}}$ before LDCKA↑ and $\overline{\text{PENB}}$ before LDCKB↑	5		5		5		5		
		LDCKA inactive before $\overline{\text{RSTA}}$ high and LDCKB inactive before $\overline{\text{RSTB}}$ high	3		3		4		4		
t_h	Hold time	A0–A17 after LDCKA↑ and B0–B17 after LDCKB↑	0		0		0		0		ns
		$\overline{\text{PENA}}$ after LDCKA low and $\overline{\text{PENB}}$ after LDCKB low	2		2		2		2		
		LDCKA inactive after $\overline{\text{RSTA}}$ high and LDCKB inactive after $\overline{\text{RSTB}}$ high	3		3		4		4		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7820-15			'ACT7820-20		'ACT7820-25		'ACT7820-30		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK, UNCK				67		50		40		33.3	MHz
t_{pd}	LDCKA↑, LDCKB↑	B/A	4		14	4	15	4	18	4	20	ns
	UNCKA↑, UNCKB↑		4	9	12	4	13.5	4	15	4	17	
t_{pd}‡	UNCKA↑, UNCKB↑	B/A		8								ns
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	4		14	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑		4		13	4	14	4	16	4	18	
t_{PHL}	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	6		16	6	16	6	18	6	20	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	6		13	6	14	6	16	6	18	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	6		15	6	15	6	17	6	19	ns
	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low		8		20	8	20	8	22	8	22	
t_{pd}	LDCKA↑, LDCKB↑	AF/AEA, AF/AEB	8		16	8	17	8	18	8	20	ns
	UNCKA↑, UNCKB↑		8		16	8	17	8	18	8	20	
t_{PLH}	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low	AF/AEA, AF/AEB	2		12	2	14	2	16	2	18	ns
t_{PLH}	LDCKA↑, LDCKB↑	HFA, HFB	8		15	8	15	8	17	8	19	ns
t_{PHL}	UNCKA, UNCKB	HFA, HFB	8		15	8	15	8	17	8	19	ns
	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low		2		12	2	14	2	16	2	18	
t_{pd}	SAB/SBA§	B/A	2		10	2	11	2	12	2	14	ns
	A/B		2		9	2	10	2	11	2	13	
t_{en}	GBA/GAB	A/B	2		6.5	2	8	2	10	2	12	ns
t_{dis}	GBA/GAB	A/B	2		11	2	12	2	13	2	14	ns

† All typical values are at 5 V, T_A = 25°C.
‡ This parameter is measured with a 30-pF load (see Figure 3).
§ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

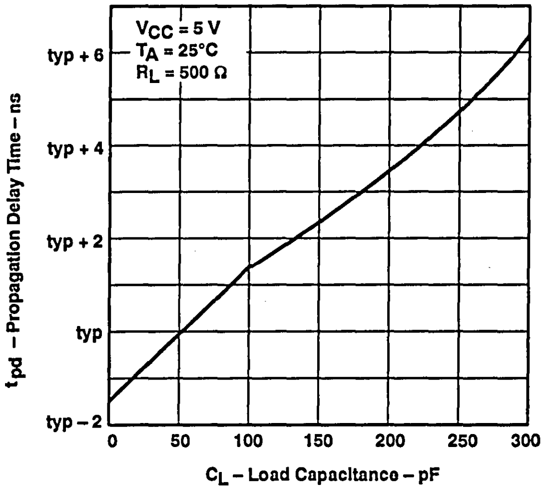


Figure 3

SUPPLY CURRENT vs CLOCK FREQUENCY

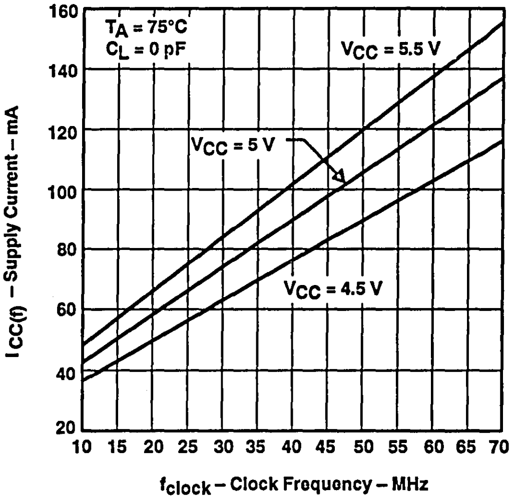


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

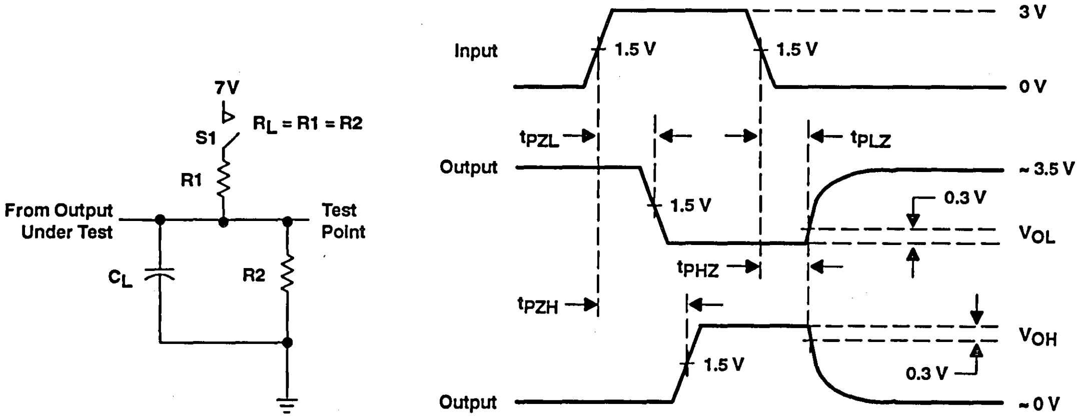
With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

$I_{CC(f)}$ = maximum I_{CC} per clock frequency
C_L = output capacitive load
f_o = data output frequency

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 5. Load Circuit and Voltage Waveforms

9-BIT CLOCKED/STROBED FIFOS

Features	Benefits
• 0.8-µm CMOS process	• Fast access times combined with low power
• Supports clock rates up to 67 MHZ	• Supports high-performance systems
• Fast access times	• Access times as low as 12 ns for improved performance
• High drive capabilities	• –8-mA to 16-mA drive capability for high-fanout and bus applications
• Depths from 32 to 2K words	• Allows greater system optimization
• Output edge control (OEC™) circuitry coupled with distributed V_{CC} and GND	• Improved noise immunity and mutual coupling effects
• Available in JEDEC reduced-height 64-pin TQFP, PCMCIA Type I compliant	• Board-space savings of up to 23% over 32-pin PLCC option

SN74ACT7807
2048 × 9 CLOCKED FIRST-IN, FIRST-OUT MEMORY

- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 12 ns With a 50-pF Load**
- **Data Rates From 0 to 67 MHz**
- **3-State Outputs**
- **Available in 44-Pin PLCC (FN), Space-Saving 64-Pin Thin Quad Flat Packages (PM), or Reduced-Height 64-Pin Thin Quad Flat Packages (PAG)**

description

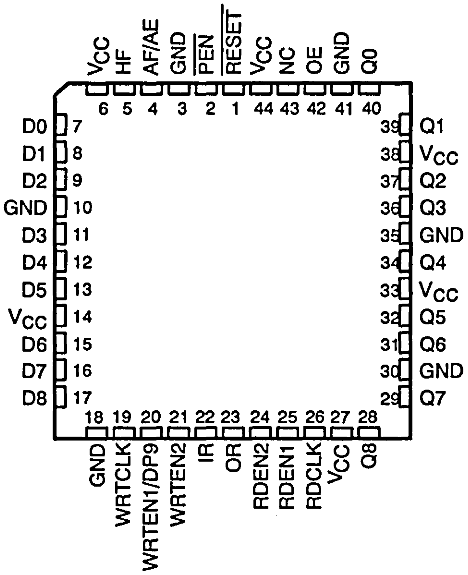
The SN74ACT7807 is a 2048-word by 9-bit FIFO with high speed and fast access times. It processes data at rates up to 67 MHz and access times of 12 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The write clock (WRTCLK) and read clock (RDCLK) inputs should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when the write-enable (WRTEN1/DP9, WRTEN2) inputs are high and the input-ready (IR) flag output is high. Data is read from memory on the rising edge of RDCLK when the read-enable (RDEN1, RDEN2) and output-enable (OE) inputs are high and the output-ready (OR) flag output is high. The first word written to memory is clocked through to the output buffer regardless of the levels on RDEN1, RDEN2, and OE. The OR flag indicates that valid data is present on the output buffer.

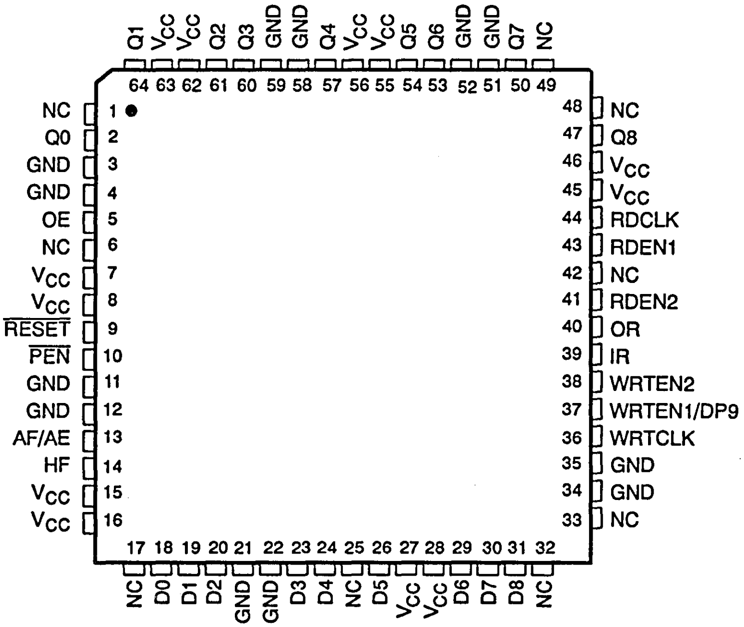
The FIFO can be reset asynchronous to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK cycles occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7807 is characterized for operation from 0°C to 70°C.

FN PACKAGE
(TOP VIEW)

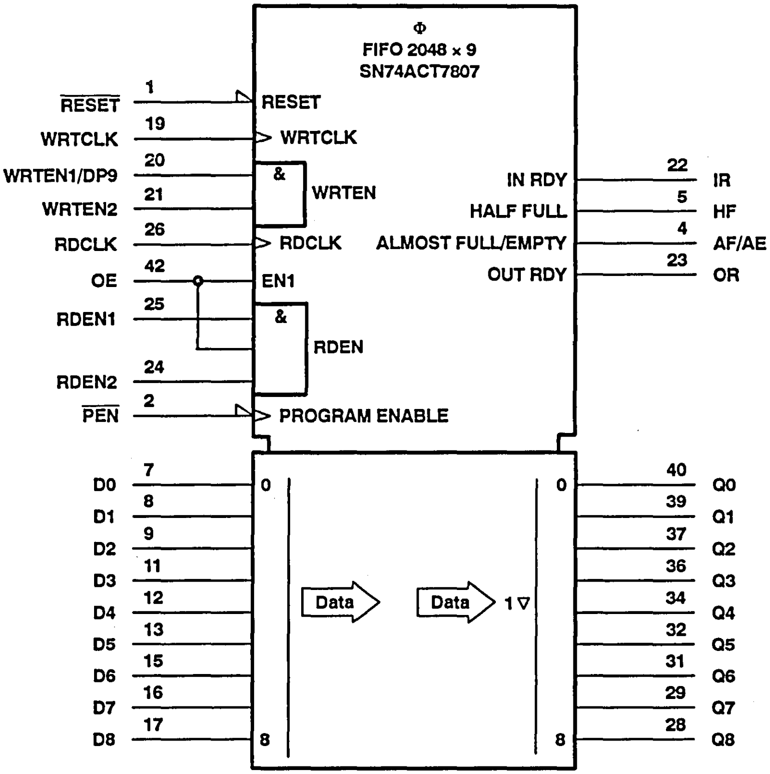


PAG OR PM PACKAGE
(TOP VIEW)



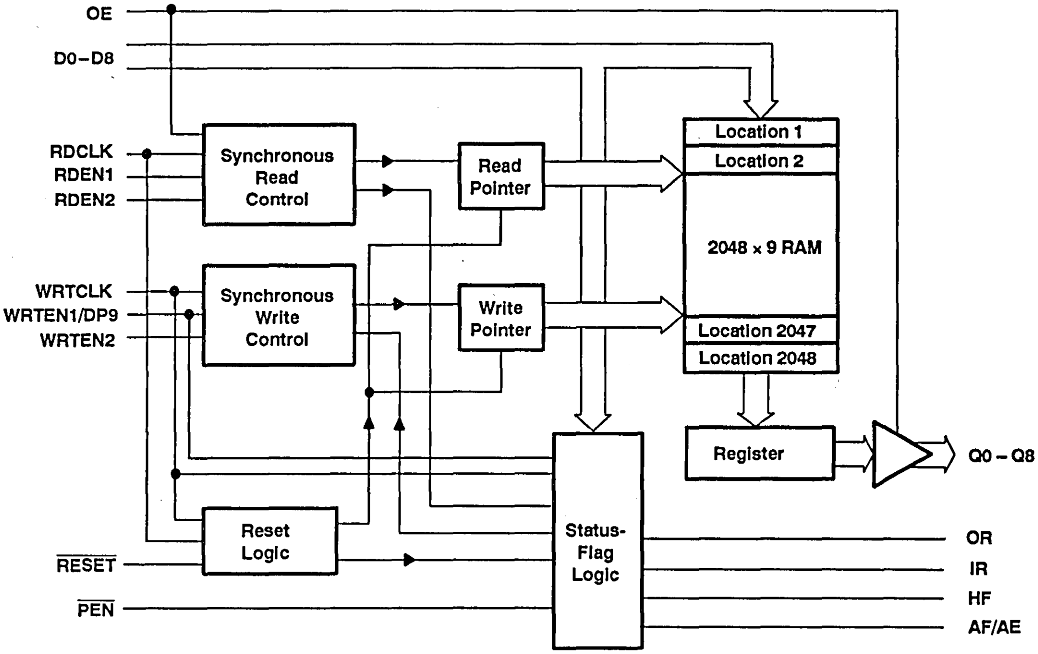
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (2048 – Y) or more words. AF/AE is high after reset.
D0–D8	I	Nine-bit data input port
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
OE	I	Output enable. When OE, RDEN1, RDEN2 and OR are high, data is read from the FIFO on a low-to-high transition of RDCLK. When OE is low, reads are disabled and the data outputs are in the high-impedance state.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q8	O	Nine-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q8 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q8.
RDCLK	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when RDEN1, RDEN2, OE, and OR are high. OR is synchronous to the low-to-high transition or RDCLK.
RDEN1, RDEN2	I	Read enables. When RDEN1, RDEN2, OE, and OR are high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN1/DP9, WRTEN2, and IR are high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1/DP9	I	Write enable/data pin 9. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. When programming an AF/AE offset value, WRTEN1/DP9 is used as the most significant data bit.
WRTEN2	I	Write enable. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or less words or (2048 – Y) or more words.

Program enable ($\overline{\text{PEN}}$) should be held high throughout the reset cycle. $\overline{\text{PEN}}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D8 and WRTEN1/DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D8 and WRTEN1/DP9 at the time of the second WRTCLK low-to-high transition. While the offsets are programmed, data is not written to the FIFO memory regardless of the state of the write enables (WRTEN1/DP9, WRTEN2). A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256, $\overline{\text{PEN}}$ must be held high.

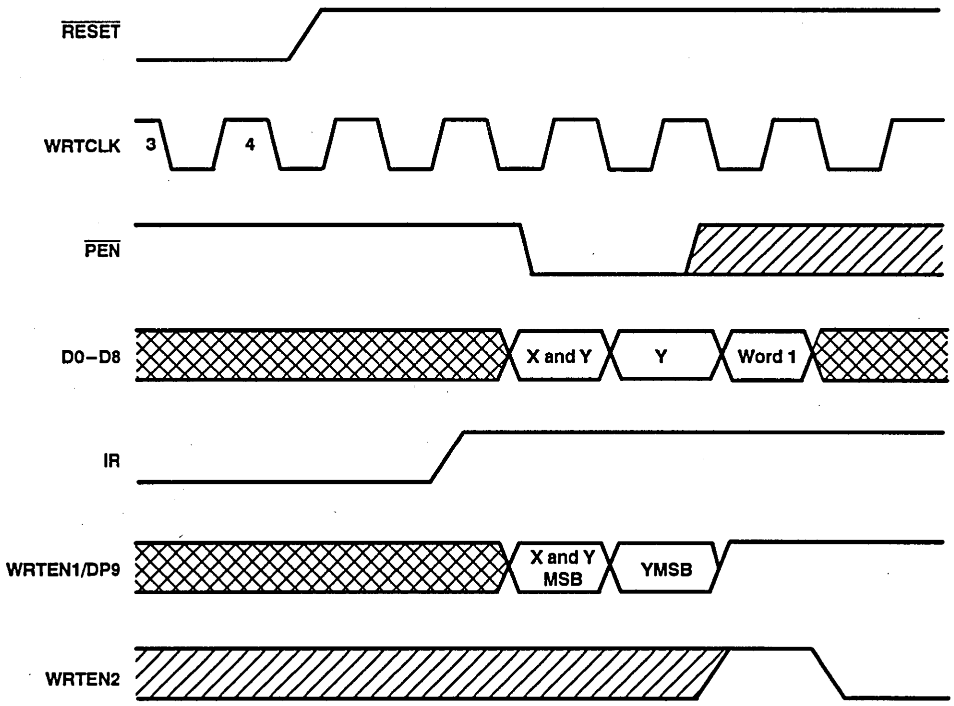


Figure 1. Programming X and Y Separately

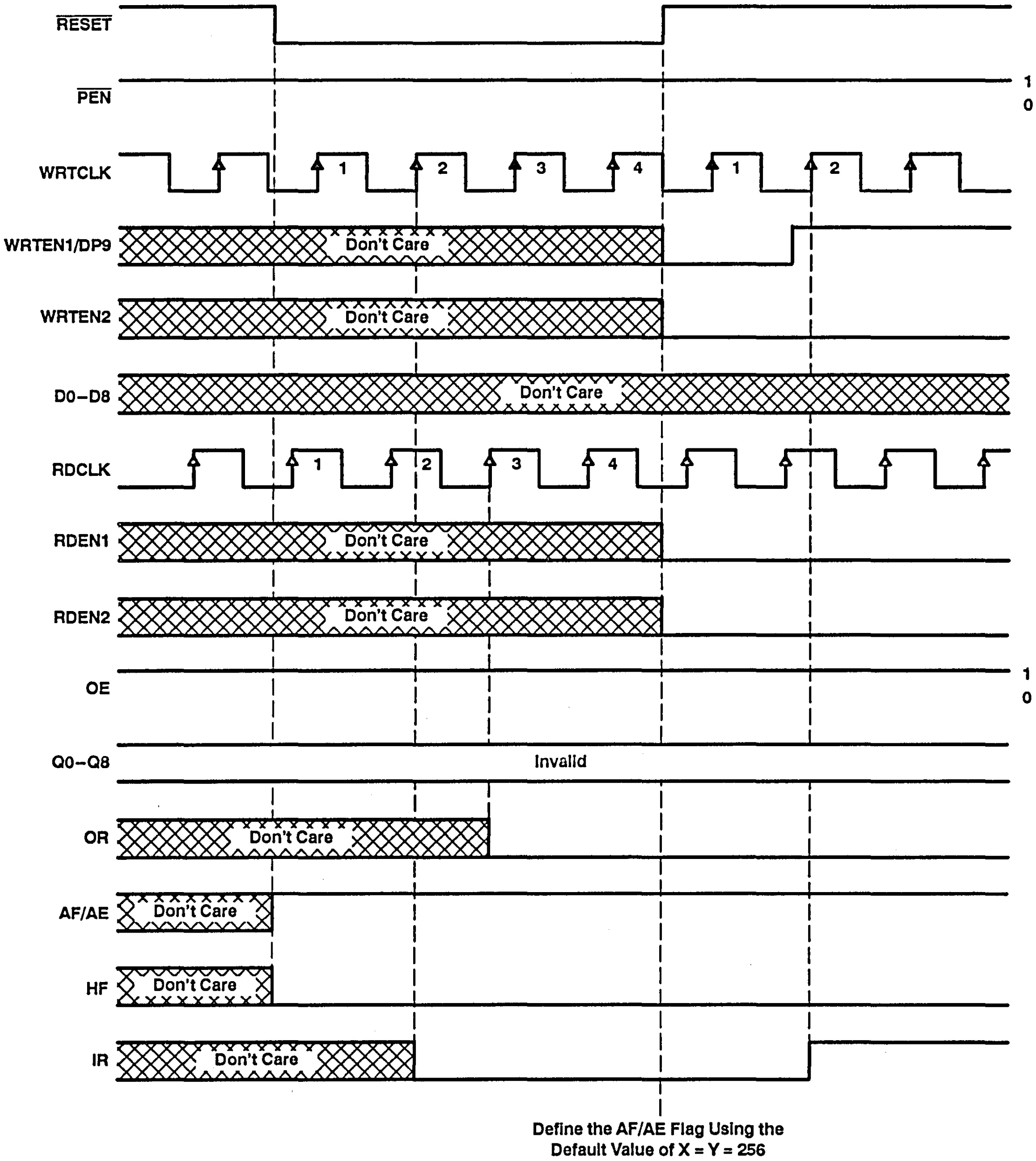


Figure 2. Reset Cycle

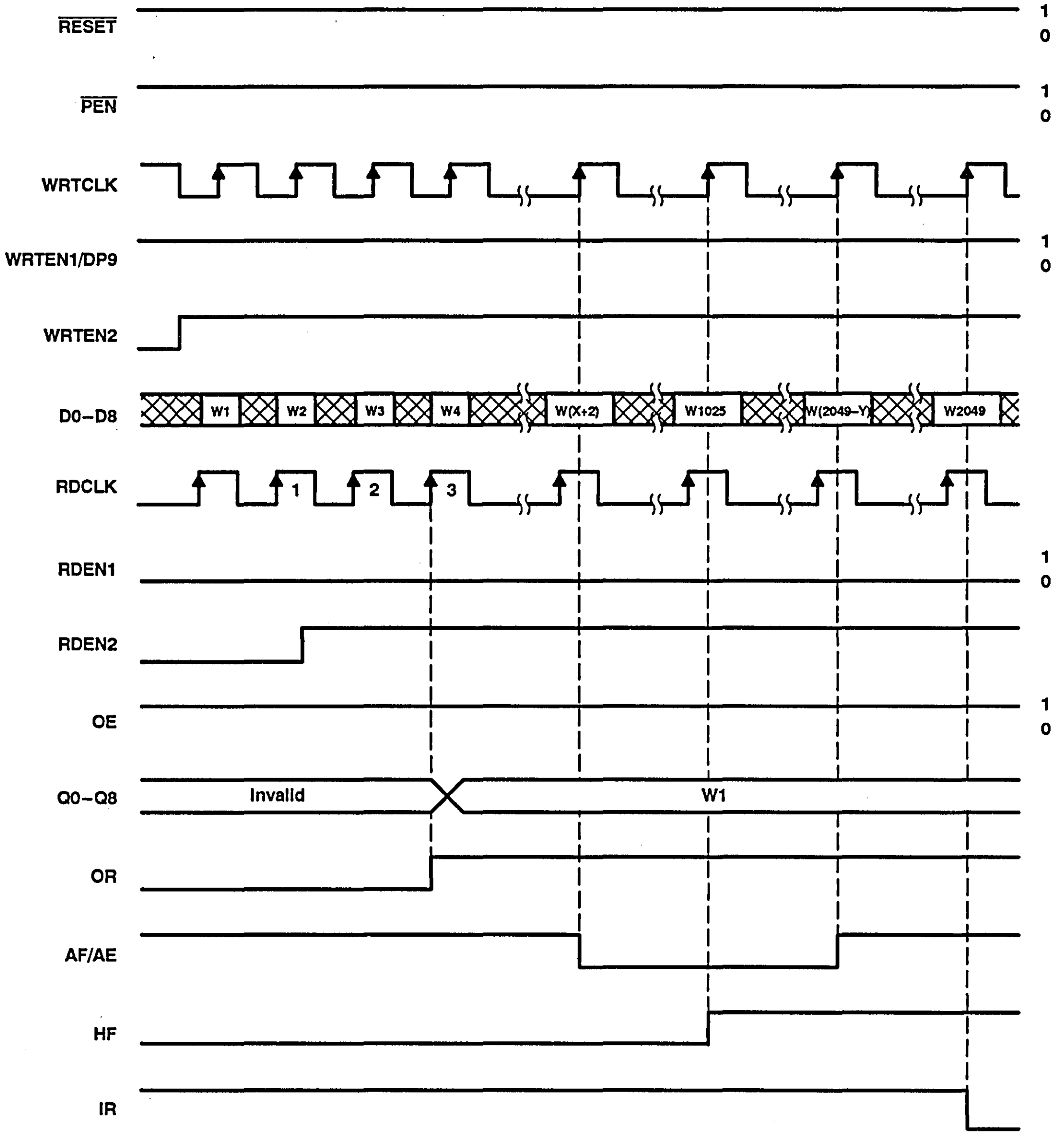


Figure 3. Write

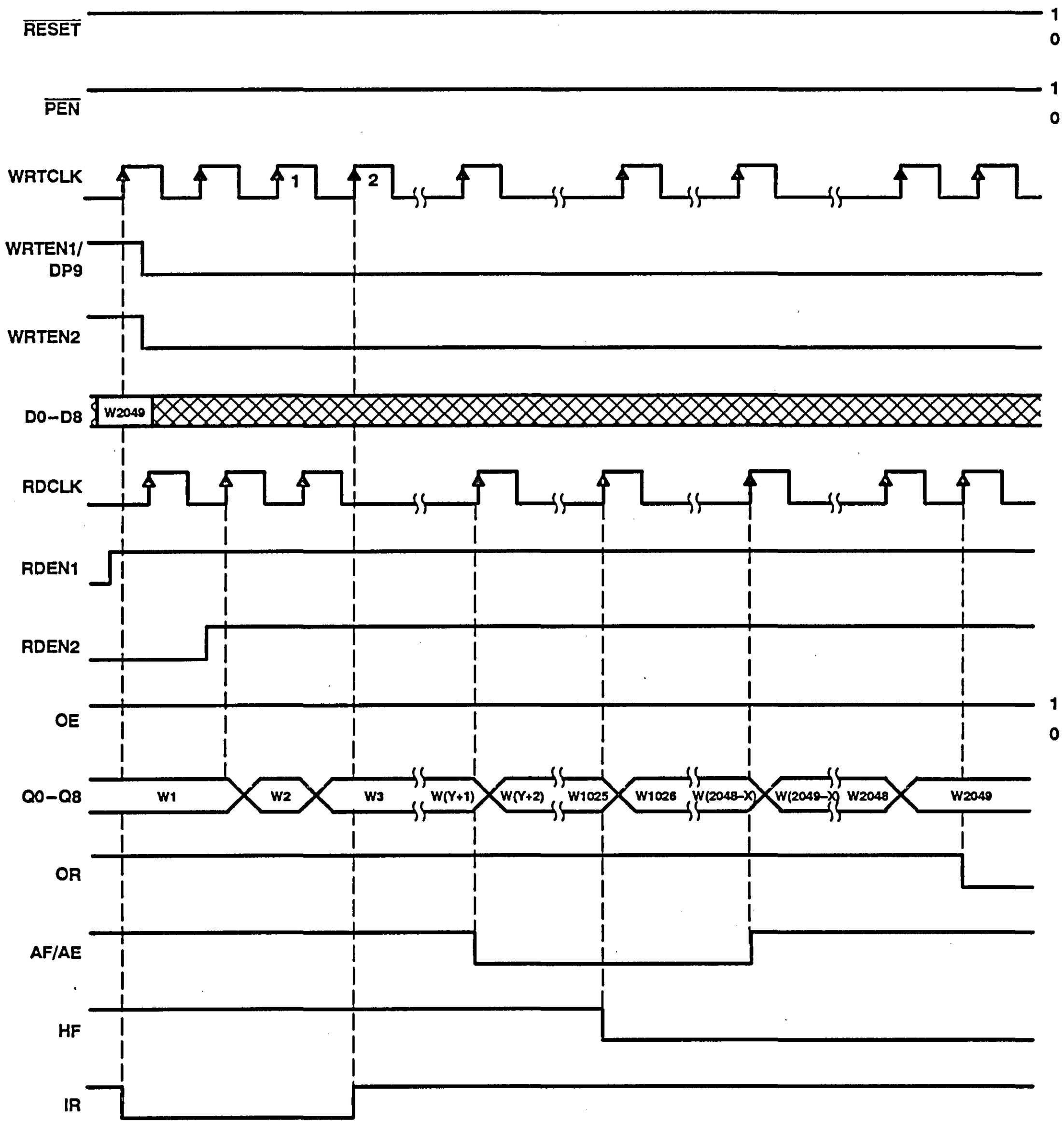


Figure 4. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7807-15		'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		–8		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		8		9		13		ns
		RDCLK high or low	6		8		9		13		
		$\overline{\text{PEN}}$ low	6		9		9		13		
t_{su}	Setup time	D0–D8 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, WRTEN2 before WRTCLK↑	4		5		5		5		
		OE, RDEN1, RDEN2 before RDCLK↑	5		6		6		6.5		
		Reset: $\overline{\text{RESET}}$ low before first WRTCLK↑ and RDCLK↑[‡]	7		8		8		8		
		$\overline{\text{PEN}}$ before WRTCLK↑	4		5		5		5		
t_h	Hold time	D0–D8 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, WRTEN2 after WRTCLK↑	0		0		0		0		
		OE, RDEN1, RDEN2 after RDCLK↑	0		0		0		0		
		Reset: $\overline{\text{RESET}}$ low after fourth WRTCLK↑ and RDCLK↑[‡]	5		5		5		5		
		$\overline{\text{PEN}}$ high after WRTCLK↓	0		0		0		0		
		$\overline{\text{PEN}}$ low after WRTCLK↑	3		3		3		3		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

[‡] To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	μA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	μA
ΔI_{CC}[‡]	WRTEN1/DP9	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2	mA
	Other inputs						1	
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7807-15			'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	TYP[†]	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	3	9	12	3	13	3	18	3	25	ns
t_{pd}[§]				8								
t_{pd}	WRTCLK↑	IR	1		9	1	12	1	14	1	16	ns
t_{pd}	RDCLK↑	OR	1		9	2	12	2	14	2	16	ns
t_{pd}	WRTCLK↑	AF/AE	2		16	2	20	2	25	2	30	ns
	RDCLK↑		2		17	2	20	2	25	2	30	
t_{PLH}	WRTCLK↑	HF	2		19	2	21	2	23	2	25	ns
t_{PHL}	RDCLK↑		2		16	2	18	2	20	2	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	1		12	1	18	1	22	1	24	ns
t_{PHL}		HF	2		12	2	18	2	22	2	24	
t_{en}	OE	Any Q	2		10	2	13	2	15	2	18	ns
t_{dis}			1		11	1	13	1	15	1	18	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[‡] This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.
[§] This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	91	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

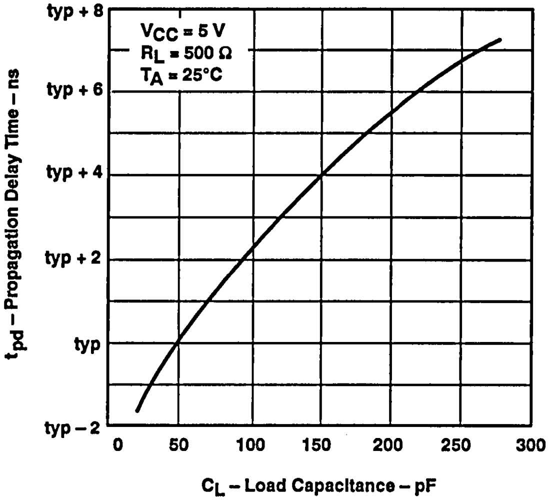


Figure 5

ACTIVE I_{CC} vs FREQUENCY

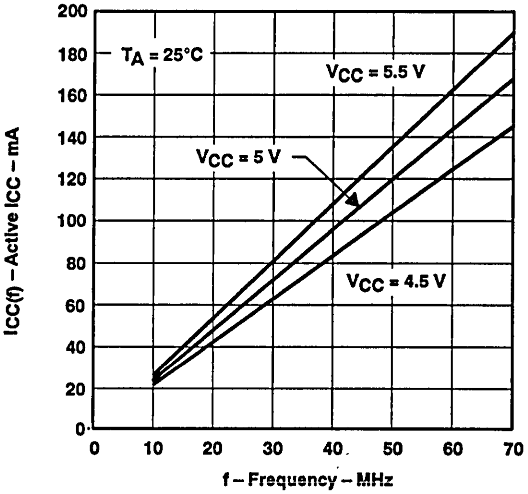


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) of the SN74ACT7807 can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

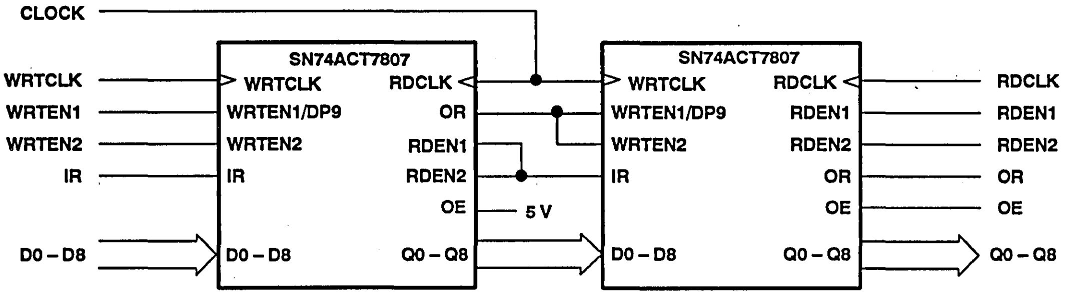


Figure 7. Word-Depth Expansion: 4096 Words by 9 Bits

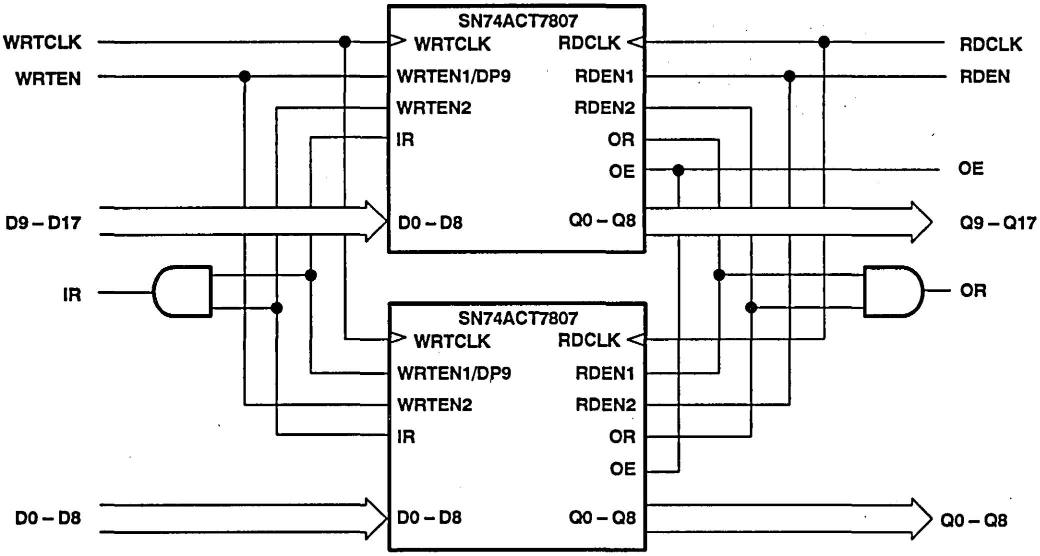
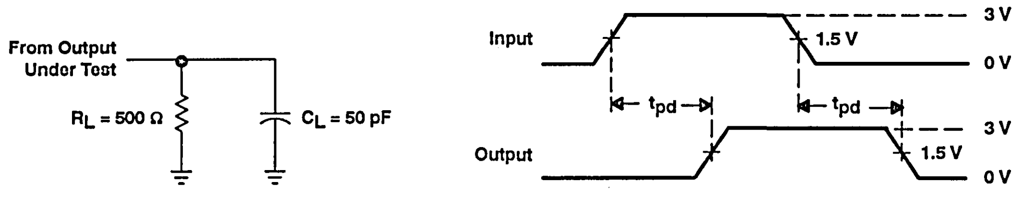


Figure 8. Word-Width Expansion: 2048 Words by 18 Bits

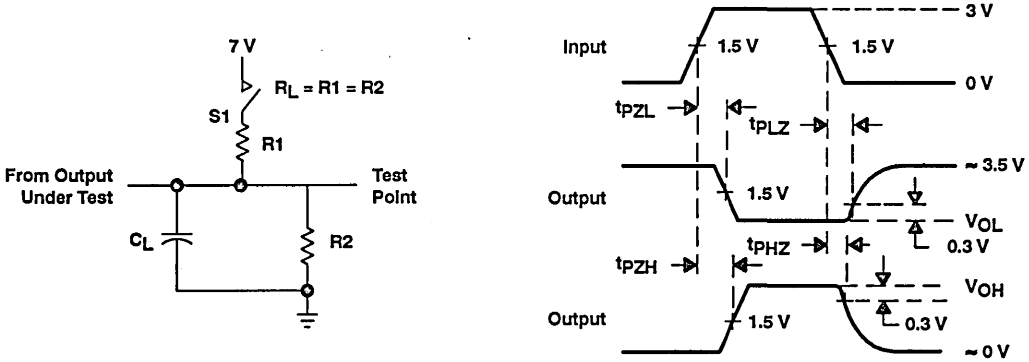
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 10. 3-State Outputs (Any Q)

SN74ACT7808
2048 × 9 FIRST-IN, FIRST-OUT MEMORY

SCAS205A – FEBRUARY 1991 – REVISED AUGUST 1994

- **Load Clocks and Unload Clocks Can Be Asynchronous or Coincident**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Fast Access Times of 15 ns With a 50-pF Load**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Expansion Logic for Depth Cascading**
- **Empty, Full, and Half-Full Flags**
- **Fall-Through Time of 20 ns Typ**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Available in 44-Pin PLCC (FN), Space-Saving 64-Pin Thin Quad Flat Packages (PM), or Reduced-Height 64-Pin Quad Flat Packages (PAG)**

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7808 is a 2048-word by 9-bit FIFO designed for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 2048. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 1024 or more words and is low when it contains 1023 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset can be used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (2048 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (2047 – Y) words.

A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

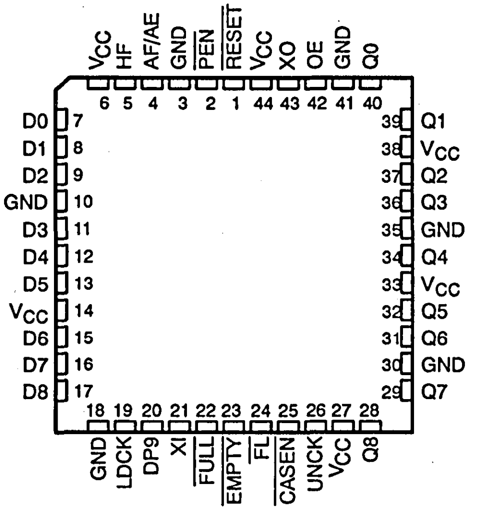
The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable (OE) input is low. OE does not affect the output flags.

Cascading is easily accomplished in the word-width and word-depth directions. When not using the FIFO in depth expansion, cascade enable ($\overline{\text{CASEN}}$) must be tied high.

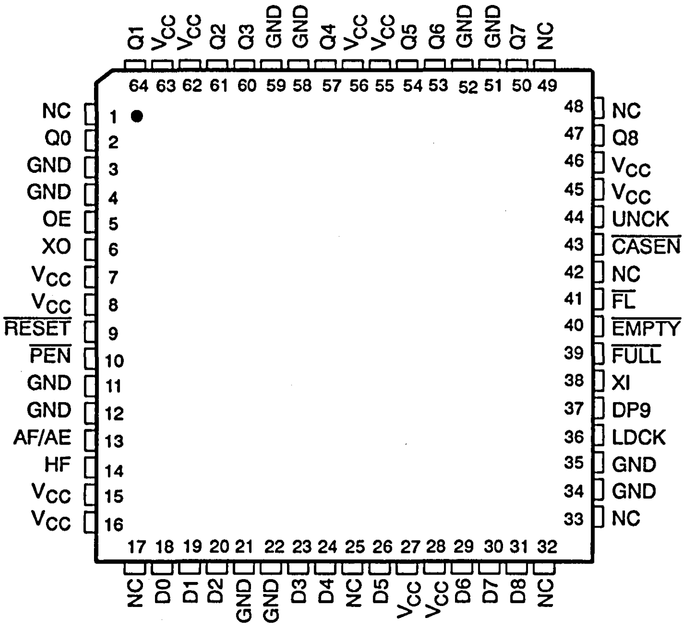
The SN74ACT7808 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS

**FN PACKAGE
(TOP VIEW)**

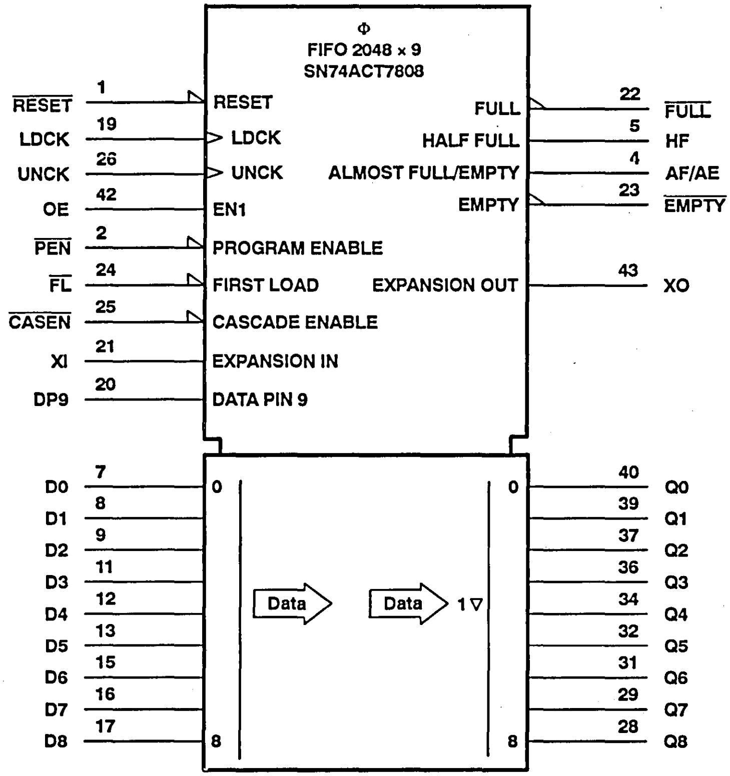


**PAG OR PM PACKAGE
(TOP VIEW)**



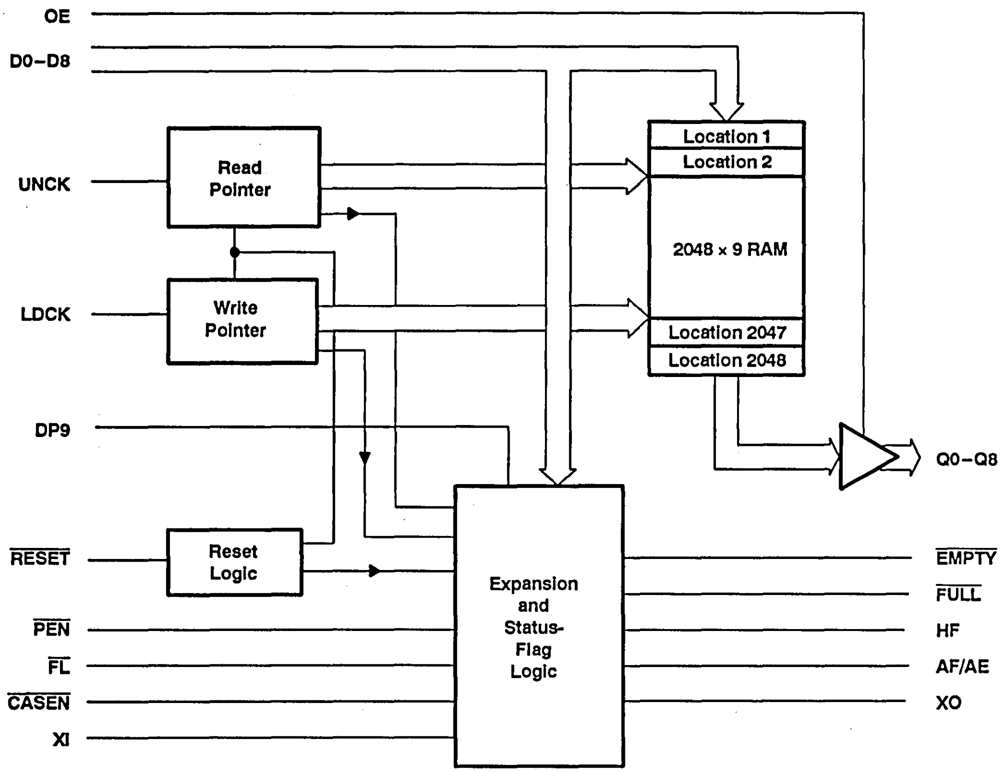
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for this AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (2048 – Y) or more words. AF/AE is high after reset.
$\overline{\text{CASEN}}$†	I	Cascade enable. When multiple SN74ACT7808 devices are depth cascaded, every device must have $\overline{\text{CASEN}}$ tied low. $\overline{\text{CASEN}}$ must be tied high when a device is not used in depth expansion.
D0–D8	I	Nine-bit data input port
DP9	I	DP9 is used as the most significant bit when programming the AF/AE offset values.
$\overline{\text{EMPTY}}$	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FL}}$†	I	When multiple SN74ACT7808 devices are depth cascaded, the first device in the chain must have its $\overline{\text{FL}}$ input tied low and all other devices must have their $\overline{\text{FL}}$ inputs tied high.
$\overline{\text{FULL}}$	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
LDCK	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
OE	I	Output enable. When OE is low, D0–D8 are in the high-impedance state.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and LDCK is high.
Q0–Q8	O	Nine-bit data output port
$\overline{\text{RESET}}$	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives $\overline{\text{FULL}}$ and AF/AE high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.
XI†	I	Expansion input (XI) and expansion output (XO). When multiple SN74ACT7808 devices are depth cascaded, the XO of one device must be connected to the XI of the next device in the chain. The XO of the last device in the chain is connected to the XI of the first device in the chain.
XO†	O	

† See Figures 4 and 5 for application information on FIFO word-width and word-depth expansions, respectively.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or less words or (2048 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D8 and DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D8 and DP9 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256, $\overline{\text{PEN}}$ must be held high.

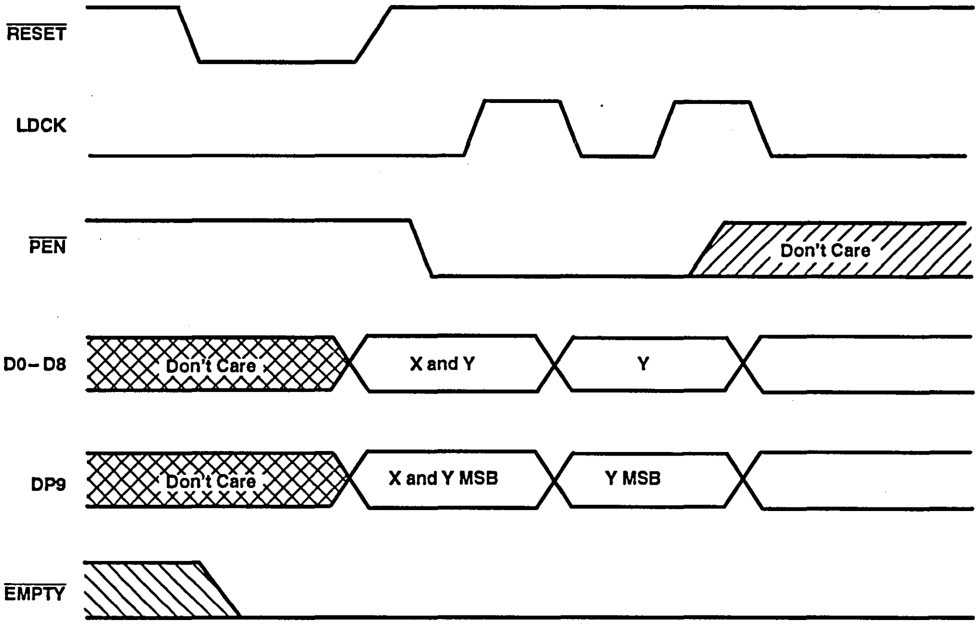
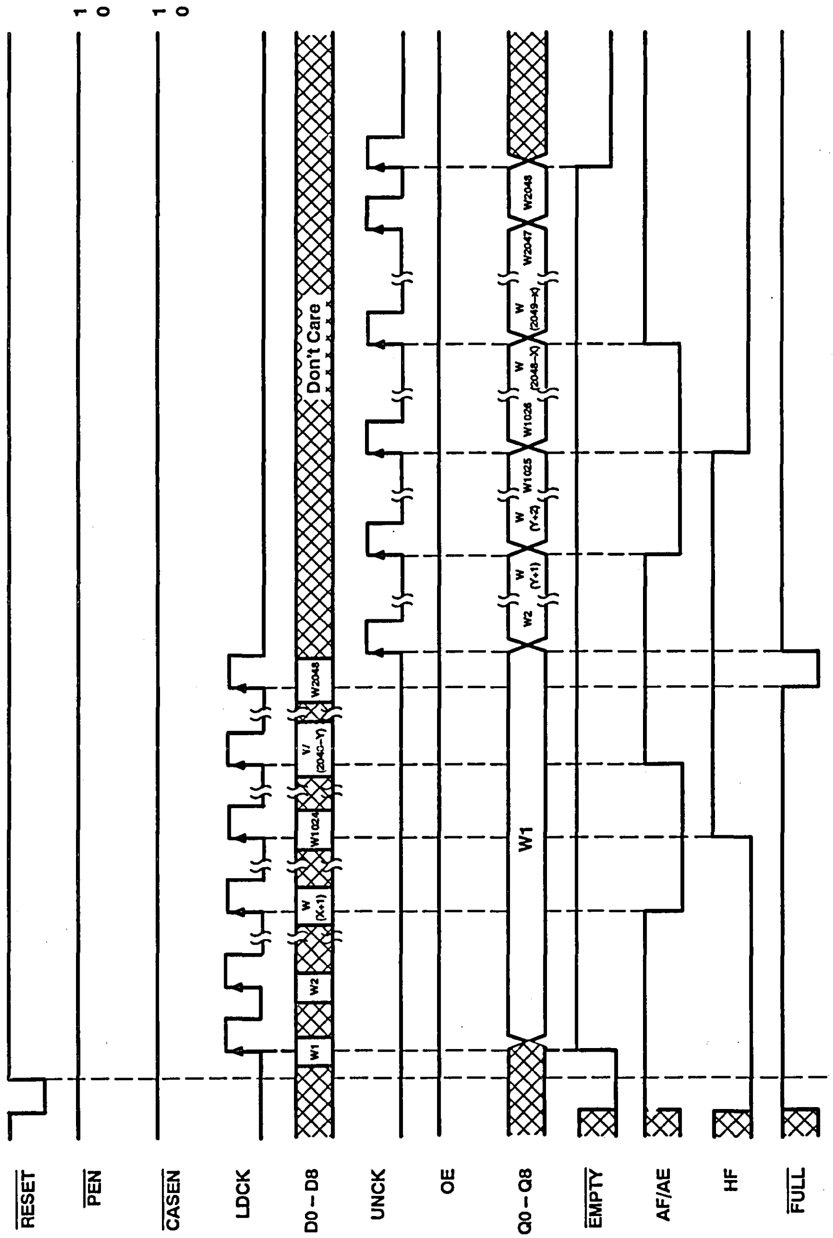


Figure 1. Programming X and Y Separately



Define the AF/AE Flag Using the Default Value or X and Y

Figure 2. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7808-20		'ACT7808-25		'ACT7808-30		'ACT7808-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	XI	3.85		3.85		3.85		3.85		V
		Other inputs	2		2		2		2		
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current			–8		–8		–8		–8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			50		40		33.3		25	MHz
t_w	Pulse duration	LDCK high or low	8		9		11		13		ns
		UNCK high or low	8		9		11		13		
		$\overline{\text{PEN}}$ low	9		9		11		13		
		$\overline{\text{RESET}}$ low	10		13		16		19		
t_{su}	Setup time	D0– D8, DP9 before LDCK↑	5		5		5		5		ns
		LDCK inactive before $\overline{\text{RESET}}$ high	5		5		5		5		
		$\overline{\text{PEN}}$ before LDCK↑	5		5		5		5		
t_h	Hold time	D0–D8, DP9 after LDCK↑	0		0		0		0		ns
		LDCK inactive after $\overline{\text{RESET}}$ high	5		5		5		5		
		$\overline{\text{PEN}}$ low after LDCK↑	4		4		4		4		
		$\overline{\text{PEN}}$ high after LDCK low	0		0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	μA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	μA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7808-20			'ACT7808-25		'ACT7808-30		'ACT7808-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		33.3		25		MHz
t_{pd}	LDCK↑	Any Q	5		20	5	22	5	25	5	28	ns
	UNCK↑		4.5	11	15	4.5	18	4.5	20	4.5	22	
t_{pd}§				10								
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	4		15	4	17	4	19	4	21	ns
t_{PHL}	UNCK↑		2		15	2	17	2	19	2	21	
	$\overline{\text{RESET}}$ low		2		16	2	18	2	20	2	22	
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	4		15	4	17	4	19	4	21	ns
t_{PLH}	UNCK↑		4		14	4	16	4	18	4	20	
	$\overline{\text{RESET}}$ low		2		18	2	20	2	22	2	24	
t_{pd}	LDCK↑	AF/AE	2		16	2	18	2	20	2	22	ns
	UNCK↑		2		16	2	18	2	20	2	22	
t_{PLH}	$\overline{\text{RESET}}$ low		0		10	0	12	0	14	0	16	
t_{PLH}	LDCK↑	HF	2		19	2	21	2	23	2	25	ns
t_{PHL}	UNCK↑		2		16	2	18	2	20	2	22	
	$\overline{\text{RESET}}$ low		2		12	2	14	2	16	2	18	
t_{PLH}	UNCK↑	XO	2		11	2	13	2	15	2	17	ns
t_{PHL}	LDCK↑		2		11	2	13	2	15	2	17	
t_{en}	OE	Any Q	1		10	1	12	1	14	1	16	ns
t_{dis}			1		9	1	11	1	13	1	15	
t_{en}	XI high	Any Q	3		13	3	15	3	17	3	19	ns
t_{dis}	XO high				4		4		4		4	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input, excluding XI, that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

§ This parameter is measured with C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	91	pF

TYPICAL CHARACTERISTICS

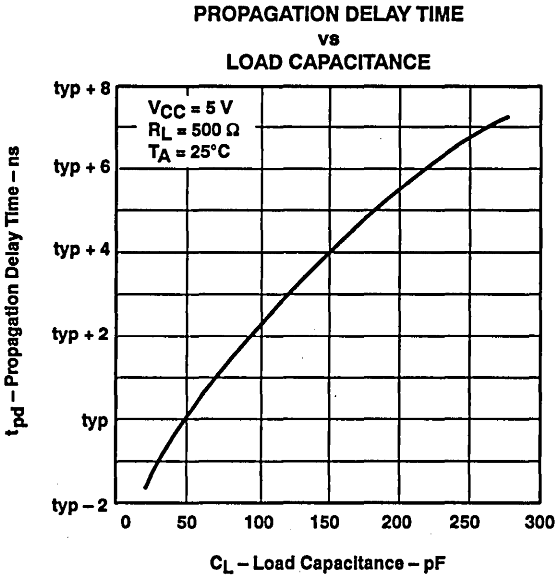


Figure 3

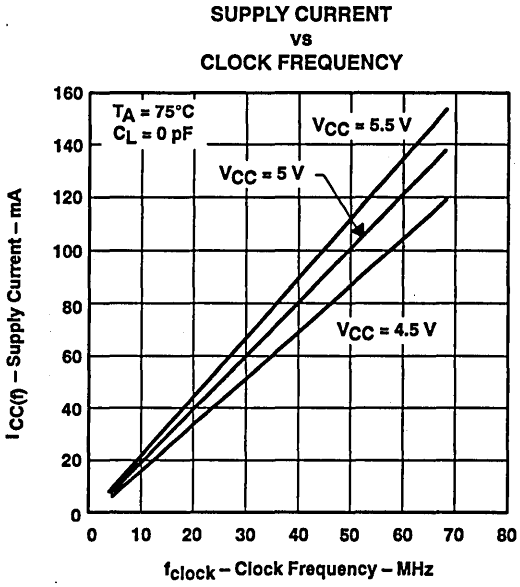


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) of the SN74ACT7808 can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

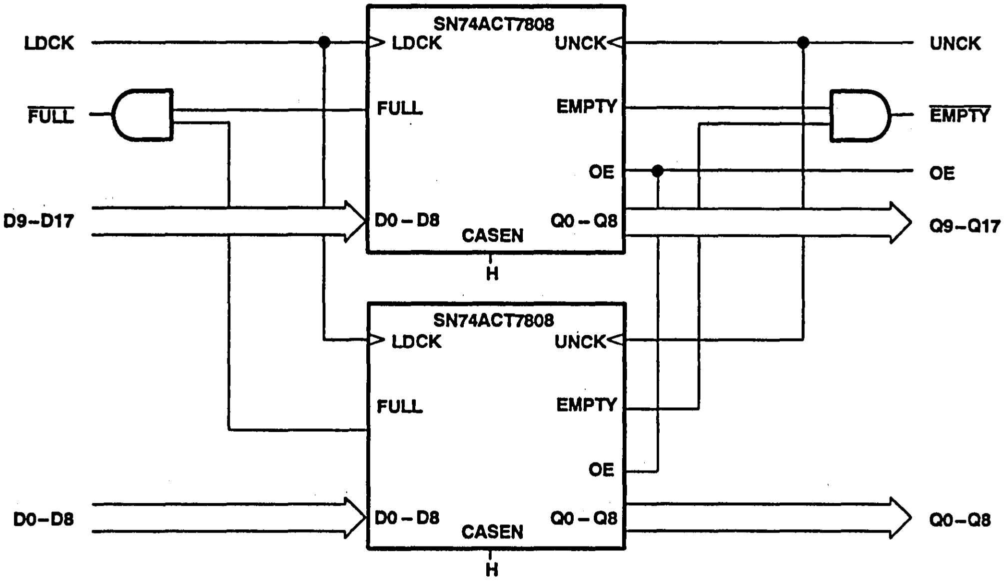


Figure 5. Word-Width Expansion: 2048 Words by 18 Bits

depth cascading (see Figure 6)

The SN74ACT7808 provides expansion logic necessary for cascading an unlimited number of the FIFOs in depth. $\overline{\text{CASEN}}$ must be low on all FIFOs used in depth expansion. $\overline{\text{FL}}$ must be tied low on the first FIFO in the chain; all others must have $\overline{\text{FL}}$ tied high. The expansion-out (XO) output of a FIFO must be tied to the expansion-in (XI) input of the next FIFO in the chain. The XO output of the last FIFO is tied to the XI input of the first FIFO to complete the loop. Data buses are common to each FIFO in the chain. A composite $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ signal must be generated to indicate boundary conditions.

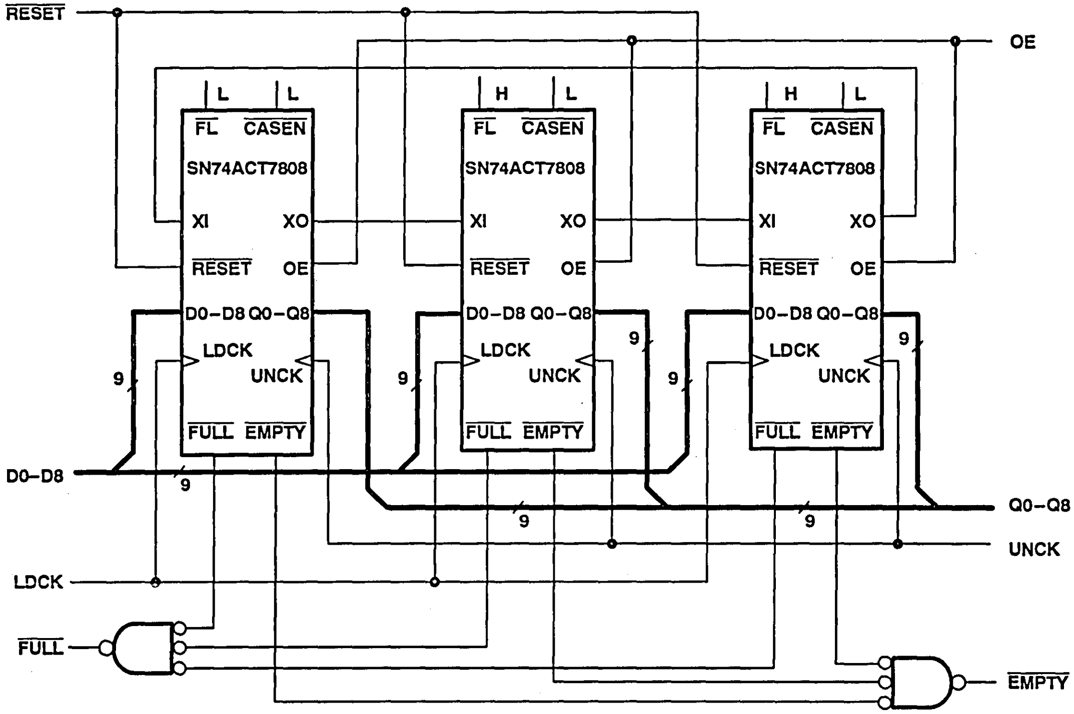
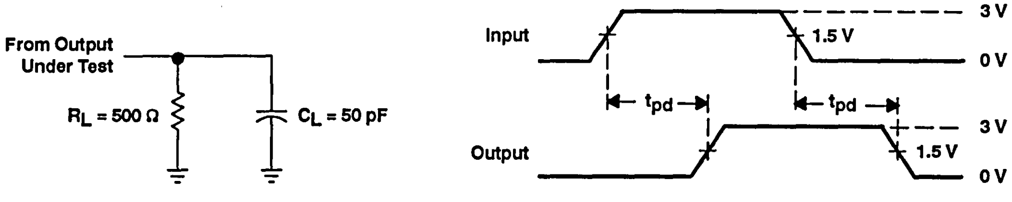


Figure 6. Depth Cascading to Form a 6K × 9 FIFO

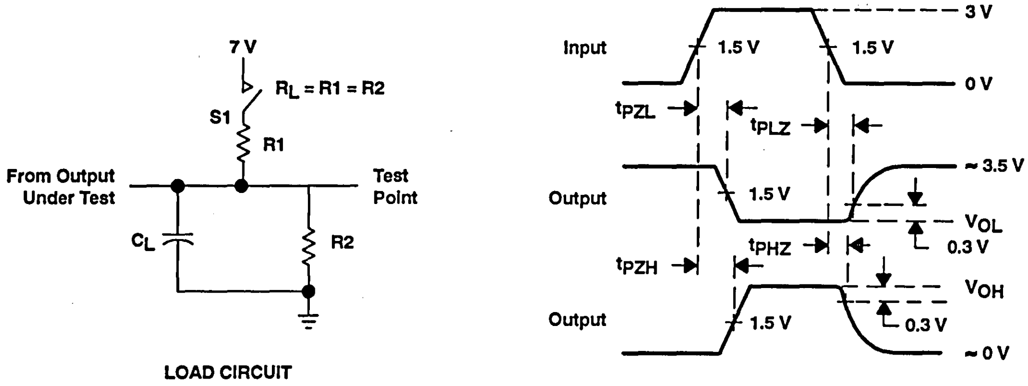
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 7. Standard CMOS Outputs (XO, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, AF/AE, HF)



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

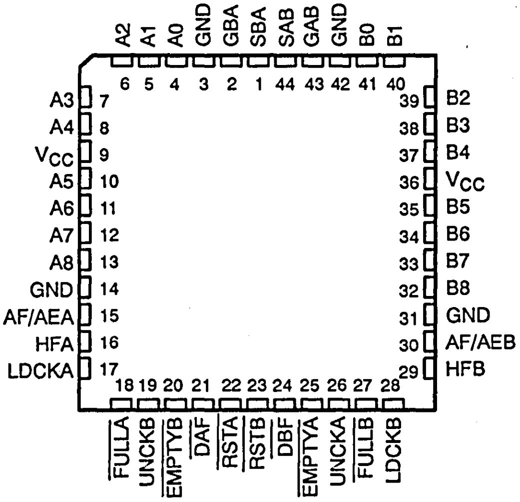
Figure 8. 3-State Outputs (Any Q)

SN74ACT2235
1024 × 9 × 2 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

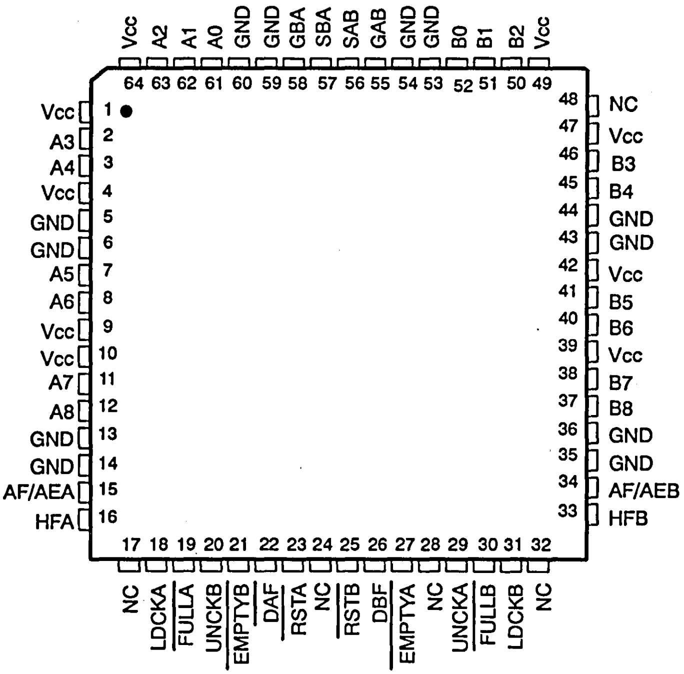
SCAS148B – DECEMBER 1990 – REVISED AUGUST 1994

- **Independent Asynchronous Inputs and Outputs**
- **Low-Power Advanced CMOS Technology**
- **Bidirectional**
- **1024 Words by 9 Bits Each**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Empty, Full, and Half-Full Flags**
- **Access Times of 25 ns With a 50-pF Load**
- **Data Rates From 0 to 50 MHz**
- **Fall-Through Times of 22 ns Max**
- **High Output Drive for Direct Bus Interface**
- **Available in 44-Pin PLCC (FN), Space-Saving 64-Pin Thin Quad Flat Packages (PM), or Reduced-Height 64-Pin Thin Quad Flat Packages (PAG)**

FN PACKAGE
(TOP VIEW)



PAG OR PM PACKAGE
(TOP VIEW)



NC – No internal connection

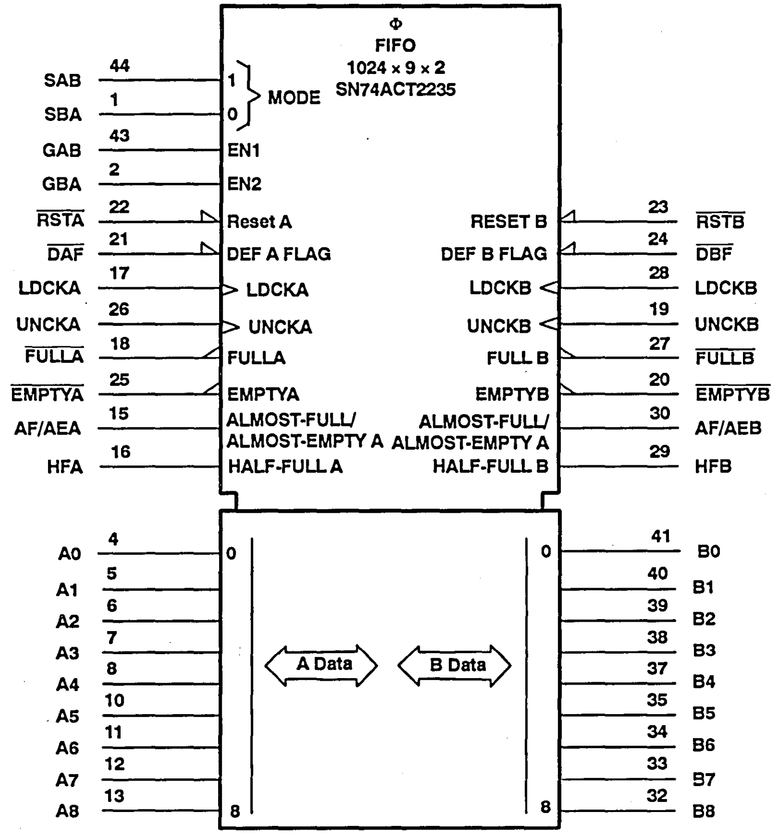
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT2235 is arranged as two 1024 by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 50 MHz with access times of 25 ns in a bit-parallel format.

The SN74ACT2235 consists of bus-transceiver circuits, two 1024 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable GAB and GBA inputs are provided to control the transceiver functions. The SAB and SBA control inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 shows the eight fundamental bus-management functions that can be performed with the SN74ACT2235.

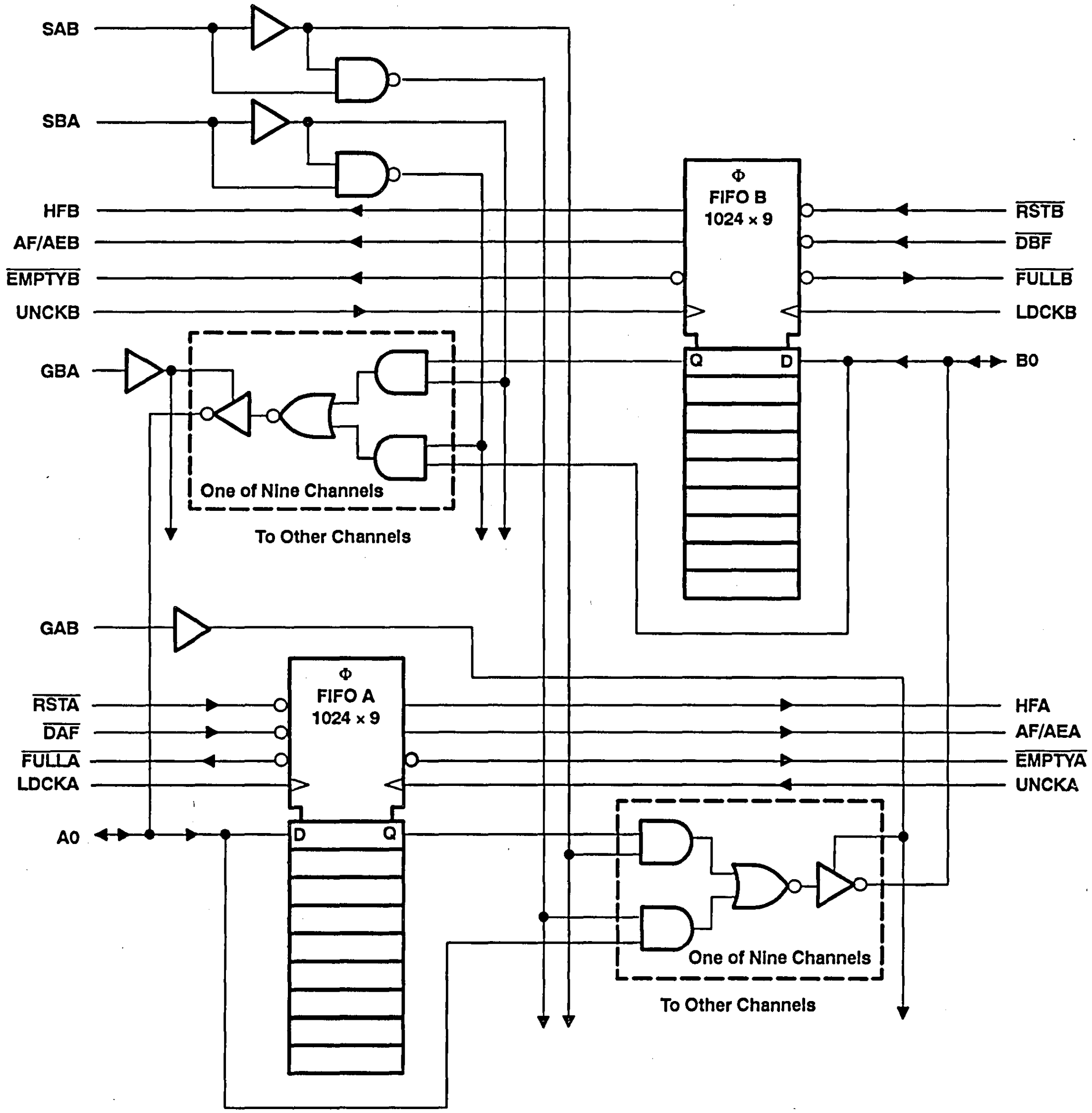
The SN74ACT2235 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

logic diagram (positive logic)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AF/AEA, AF/AEB	15, 30	O	Almost full/almost empty flags. The almost-full/almost-empty A flag (AF/AEA) is defined by the almost-full/almost-empty offset value for FIFO A (X). AF/AEA is high when FIFO A contains X or less words or 1024–X words. AF/AEA is low when FIFO A contains between X + 1 or 1023 – X words. The operation of the almost-full/almost-empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.
A0–A8	4–8, 10–13	I/O	A data inputs and outputs
B0–B8	32–35, 37–41	I/O	B data inputs and outputs
$\overline{\text{DAF}}$, $\overline{\text{DBF}}$	21, 24	I	Define-flag inputs. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value on A0–A8 as the almost-full/almost-empty offset value for FIFO A (X). The high-to-low transition of $\overline{\text{DBF}}$ stores the binary value of B0–B8 as the almost-full/almost-empty offset value for FIFO B (Y).
$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	20, 25	O	Empty flags. $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ are low when their corresponding memories are empty and high when they are not empty.
$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	18, 27	O	Full flags. FULLA and FULLB are low when their corresponding memories are full and high when they are not full.
HFA, HFB	16, 29	O	Half-full flags. HFA and HFB are high when their corresponding memories contain 512 or more words and low when they contain 511 or less words.
LOCKA, LOCKB	17, 28	I	Lead clocks. Data on A0–A8 is written into FIFO A on a low-to-high transition of LDCKA. Data on B0–B8 is written into FIFO B on a low-to-high transition of LDCKB. When the FIFOs are full, load clock signals have no effect on the data residing in memory.
GAB, GBA	2, 43	I	Output enables. GAB, GBA control the transceiver functions. When GBA is low, A0–A8 are in the high-impedance state. When GAB is low, B0–B8 are in the high-impedance state.
$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$	22, 23	I	Resets. A reset is accomplished in each direction by taking $\overline{\text{RSTA}}$ and $\overline{\text{RSTB}}$ low. This sets $\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$, $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, and AF/AEB high. Both FIFOs must be reset upon power up.
SAB, SBA	1, 44	I	Select-control inputs. SAB and SBA select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown in Figure 1.
$\overline{\text{UNCKA}}$, $\overline{\text{UNCKB}}$	19, 26	I	Unload clocks. Data in FIFO A is read to B0–B8 on a low-to-high transition of UNCKB. Data in FIFO B is read to A0–A8 on a low-to-high transition of UNCKB. When the FIFOs are empty, unload clock signals have no effect on data residing in memory.

programming procedure for AF/AEA

The almost-full/almost-empty flags (AF/AEA, AF/AEB) are programmed during each reset cycle. The almost-full/almost-empty offset value FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

user-defined X

Take $\overline{\text{DAF}}$ from high to low. This stores A0 thru A8 as X.
If $\overline{\text{RSTA}}$ is not already low, take $\overline{\text{RSTA}}$ high.
With $\overline{\text{DAF}}$ held low, take $\overline{\text{RSTA}}$ high. This defines AF/AEA using X.
To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.

default X

To redefine AF/AE using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

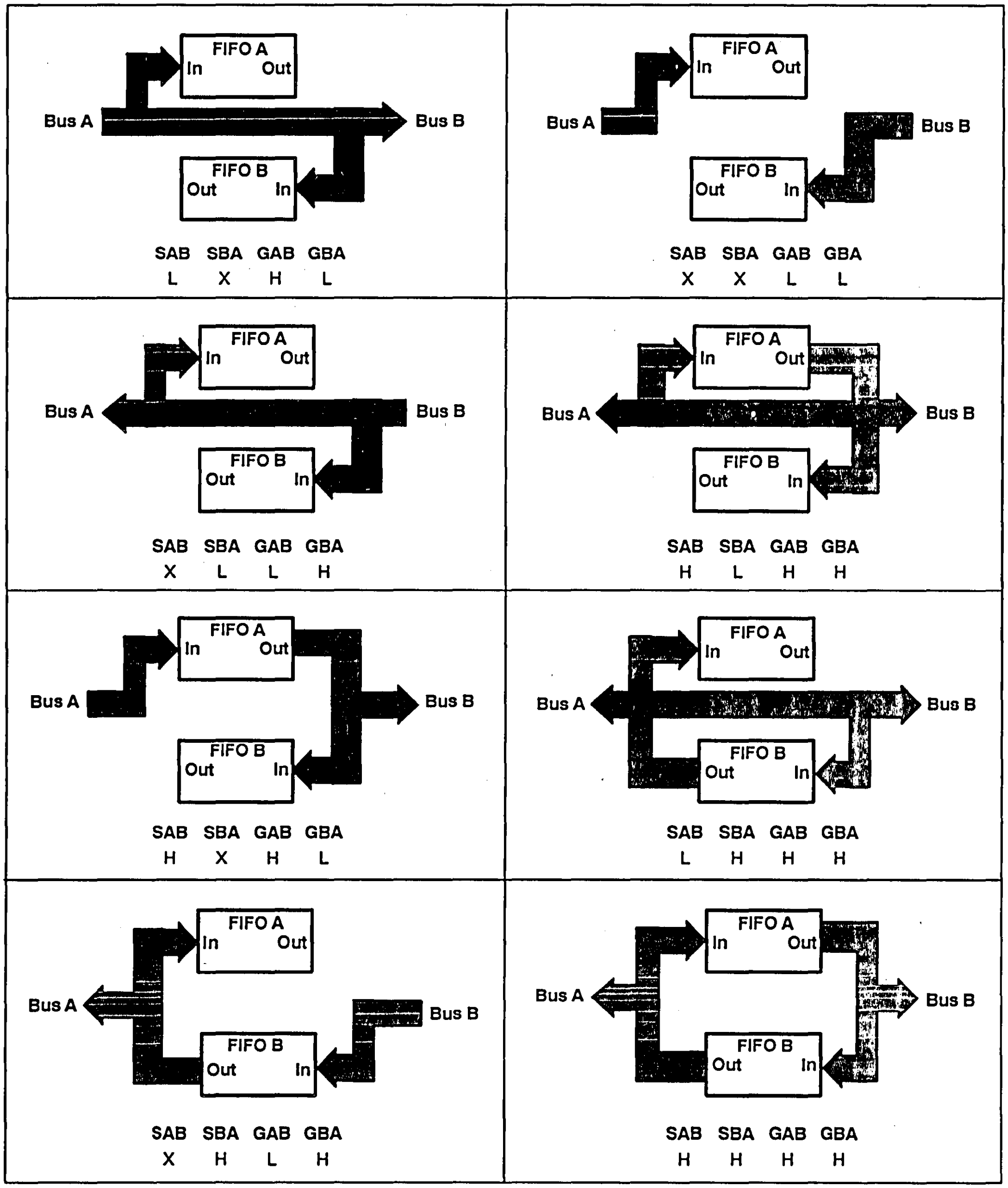
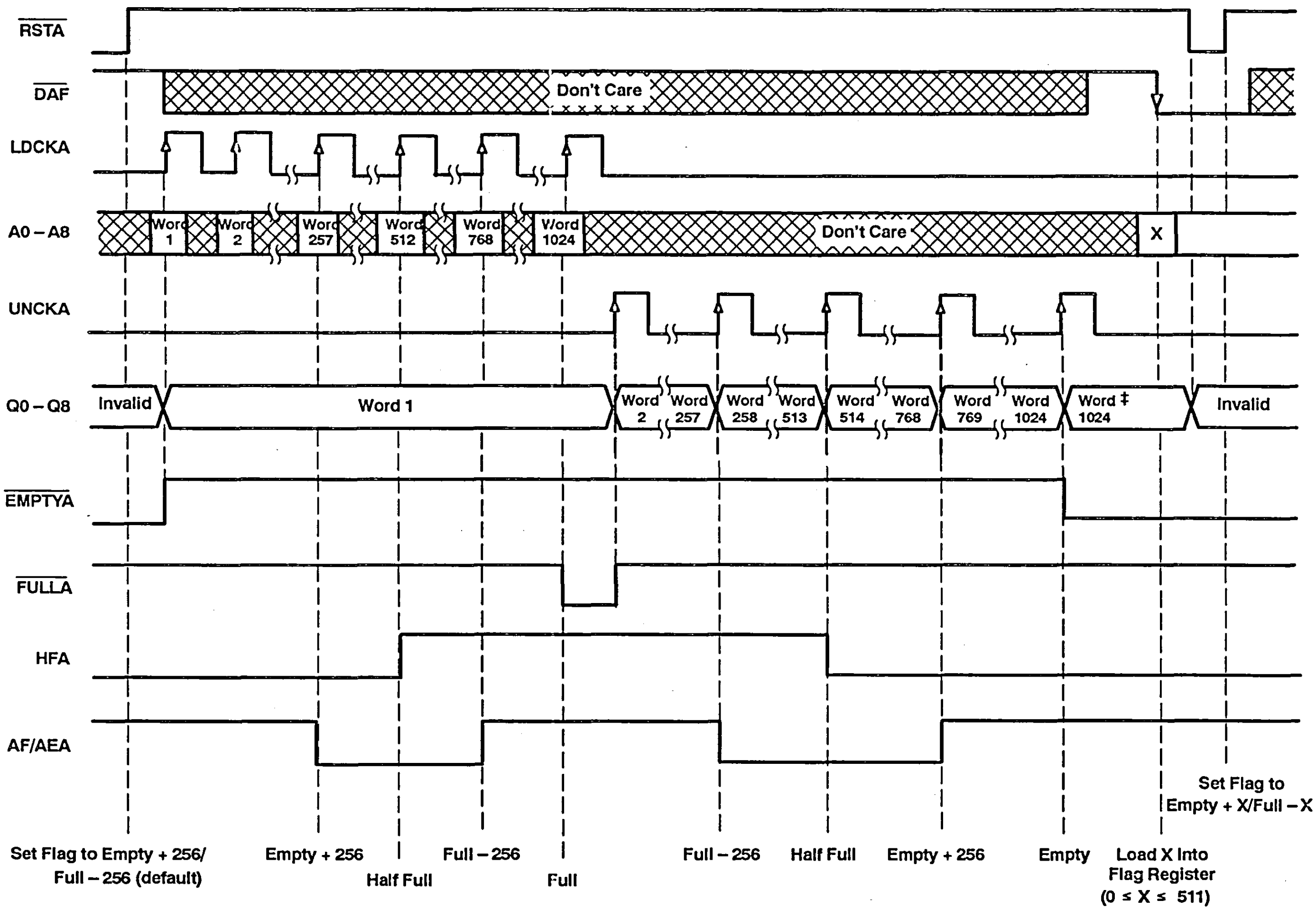


Figure 1. Bus-Management Functions

timing diagram for FIFO A†



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† Operation of FIFO B is identical to that of FIFO A.

‡ Last valid data stays on outputs when FIFO goes empty due to a read.

SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SAB	SBA	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
L	H	FIFO B to A bus	Real-time A to B bus
H	L	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
GAB	GBA	A BUS	B BUS
H	H	A bus enabled	B bus enabled
L	H	A bus enabled	Isolation/input to B bus
H	L	Isolation/input to A bus	B bus enabled
L	L	Isolation/input to A bus	Isolation/input to B bus

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage: Control inputs .... 7 V
I/O ports .... 5.5 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Maximum junction temperature .... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT2235-20		'ACT2235-30		'ACT2235-40		'ACT2235-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	A or B ports		−8		−8		−8		−8	mA
		Status flags		−8		−8		−8		−8	
I_{OL}	Low-level output current	A or B ports		16		16		16		16	mA
		Status flags		8		8		8		8	
f_{clock}	Clock frequency	LDCKA or LDCKB		50		33		25		16.7	MHz
		UNCKA or UNCKB		50		33		25		16.7	
t_w	Pulse duration	$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low	20		20		25		25		ns
		LDCKA or LDCKB low	8		10		14		20		
		LDCKA or LDCKB high	8		10		14		20		
		UNCKA or UNCKB low	8		10		14		20		
		UNCKA or UNCKB high	8		10		14		20		
		$\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high	10		10		10		10		
t_{su}	Setup time	Data before LDCKA or LDCKB↑	4		4		5		5		ns
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	5		5		5		5		
		Define AF/AE: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓ before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	7		7		7		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	5		5		5		5		
		$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inactive (high) before LDCKA or LDCKB↑	5		5		5		5		
t_h	Hold time	Data after LDCKA or LDCKB↑	1		1		2		2		ns
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	0		0		0		0		
		Define AF/AE: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ low after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0		0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0		0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	I/O ports	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	μA
I_{CC}‡		V_I = V_{CC} – 0.2 V or 0				10	400	μA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I_{CC} tested with outputs open.
§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT2235-20			'ACT2235-30		'ACT2235-40		'ACT2235-60		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK		50			33		25		16.7		MHz
	UNCK		50			33		25		16.7		
t_{pd}	LDCK↑, LDCKB↑	B or A	8		22	8	22	8	24	8	26	ns
t_{pd}	UNCKA↑, UNCKB↑	B or A	12	17	25	12	25	12	35	12	45	ns
t_{PLH}	LDCK↑, LDCKB↑	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	4		15	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	2		17	2	17	2	19	2	21	ns
t_{PHL}	$\overline{\text{RSTA}}$↓, $\overline{\text{RSTB}}$↓	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	2		18	2	18	2	20	2	22	ns
t_{PHL}	LDCK↑, LDCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	4		15	4	15	4	17	4	19	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	4		15	4	15	4	17	4	19	ns
t_{PLH}	$\overline{\text{RSTA}}$↓, $\overline{\text{RSTB}}$↓	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	2		15	2	15	2	17	2	19	ns
t_{PLH}	$\overline{\text{RSTA}}$↓, $\overline{\text{RSTB}}$↓	AF/AEA, AF/AEB	2		15	2	15	2	17	2	19	ns
t_{PLH}	LDCK↑, LDCKB↑	HFA, HFB	2		15	2	15	2	17	2	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	HFA, HFB	4		18	4	18	4	20	4	22	ns
t_{PHL}	$\overline{\text{RSTA}}$↓, $\overline{\text{RSTB}}$↓	HFA, HFB	1		15	1	15	1	17	1	19	ns
t_{pd}	SAB or SBA¶	B or A	1		11	1	11	1	12	1	14	ns
t_{pd}	A or B	B or A	1		11	1	11	1	12	1	14	ns
t_{pd}	LDCK↑, LDCKB↑	AF/AEA, AF/AEB	2		18	2	18	2	20	2	22	ns
t_{pd}	UNCKA↑, UNCKB↑	AF/AEA, AF/AEB	2		18	2	18	2	20	2	22	ns
t_{en}	GBA or GAB	A or B	2		11	2	11	2	13	2	15	ns
t_{dis}	GBA or GAB	A or B	1		9	1	9	1	11	1	13	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	Outputs enabled	C_L = 50 pF, f = 5 MHz	71	pF
		Outputs disabled		57	

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

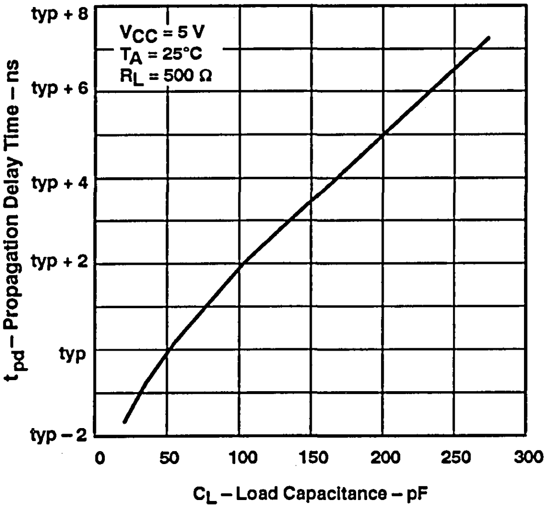


Figure 2

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

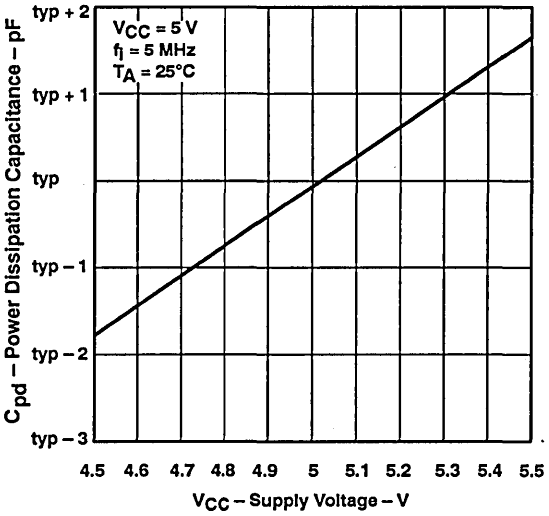


Figure 3

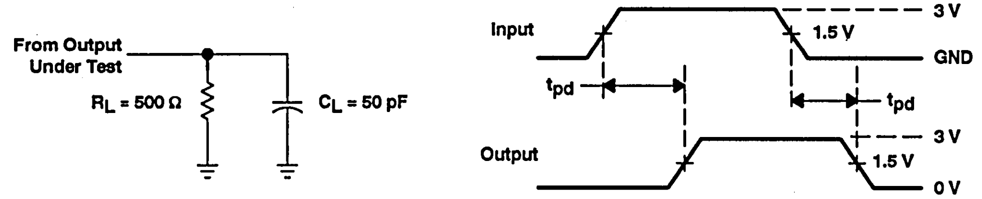
calculating power dissipation

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

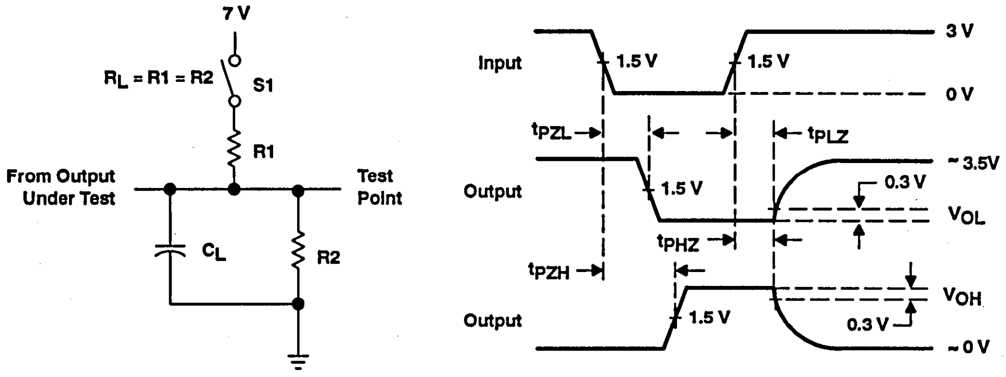
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 4. Standard CMOS Outputs ($\overline{\text{FULL}}$, AF/AE, $\overline{\text{EMPTY}}$)



LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		–	50 pF	Open

† Includes probe and test-fixture capacitance

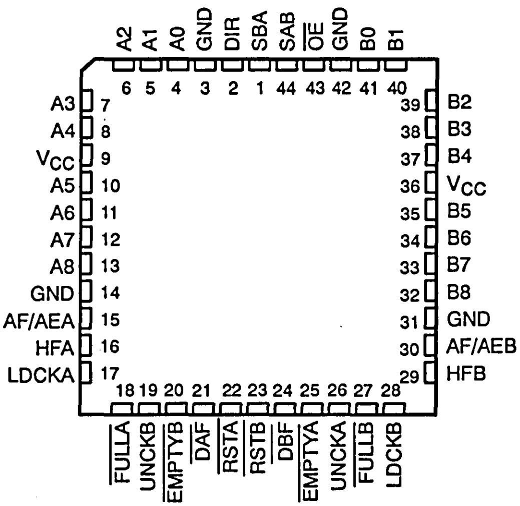
Figure 5. 3-State Outputs (A0–A8, B0–B8)

SN74ACT2236
1024 × 9 × 2 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

SCAS149 – APRIL 1990 – REVISED DECEMBER 1990

- **Independent Asynchronous Inputs and Outputs**
- **Low-Power Advanced CMOS Technology**
- **Bidirectional**
- **1024 Words by 9 Bits Each**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Empty, Full, and Half-Full Flags**
- **Access Times of 25 ns With a 50-pF Load**
- **Data Rates From 0 to 50 MHz**
- **Fall-Through Times of 23 ns Max**
- **High Output Drive for Direct Bus Interface**
- **3-State Outputs**

FN PACKAGE
(TOP VIEW)



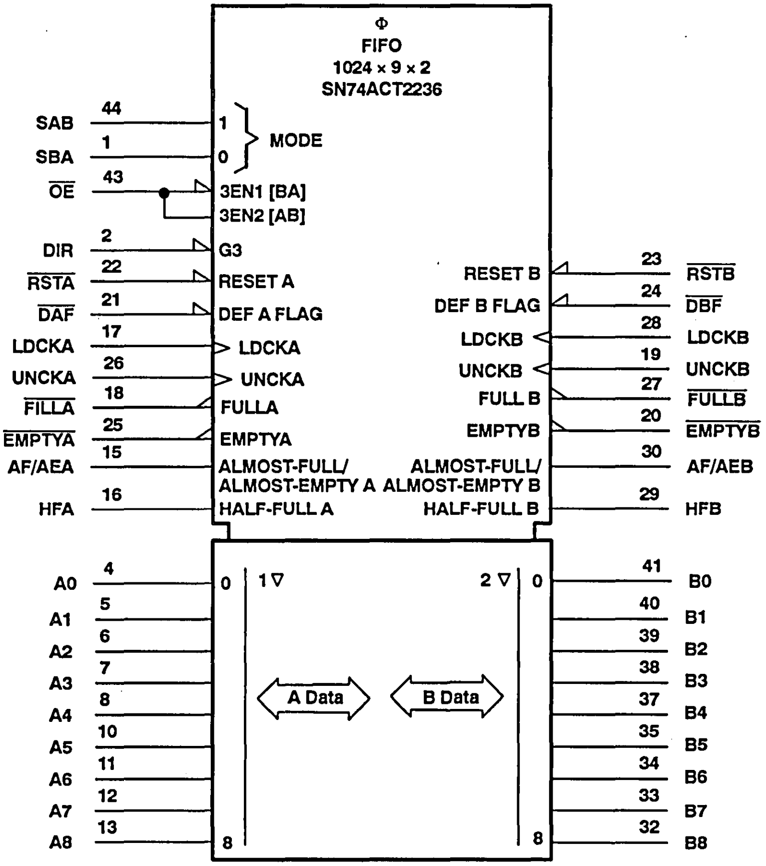
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT2236 is arranged as two 1024 by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 50 MHz with access times of 25 ns in a bit-parallel format.

The SN74ACT2236 consists of bus-transceiver circuits, two 1024 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable $\overline{\text{OE}}$ and DIR inputs are provided to control the transceiver functions. The SAB and SBA control inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 shows the five fundamental bus-management functions that can be performed with the SN74ACT2236.

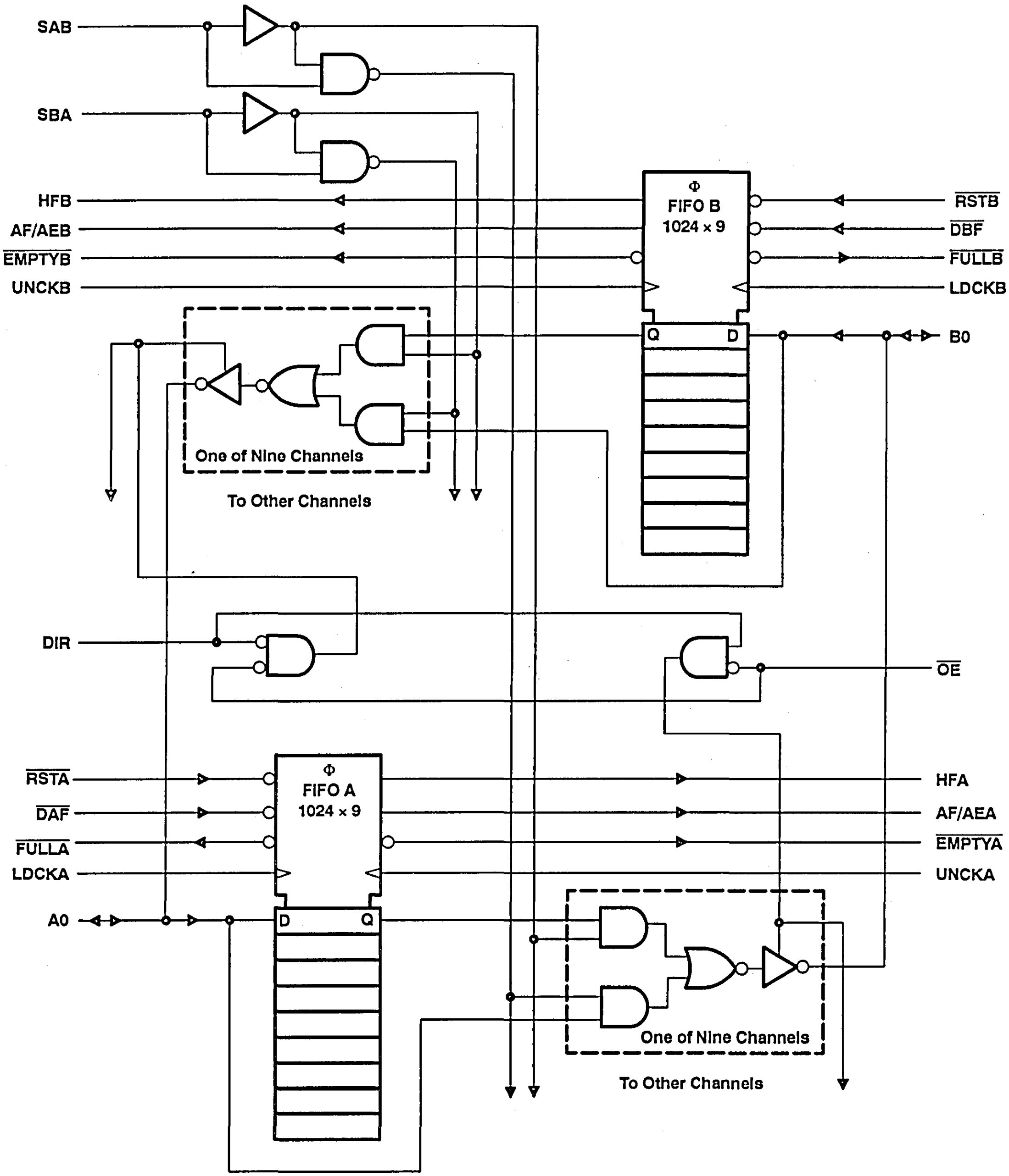
The SN74ACT2236 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AEA, AF/AEB	15, 30	O	Almost full/almost empty flags. The almost-full/almost-empty A flag (AF/AEA) is defined by the almost-full/almost-empty offset value for FIFO A (X). AF/AEA is high when FIFO A contains X or less words or 1024–X words. AF/AEA is low when FIFO A contains between X + 1 or 1023 – X words. The operation of the almost-full/almost-empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.
A0–A8	4–8, 10–13	I/O	A data inputs and outputs
B0–B8	32–35, 37–41	I/O	B data inputs and outputs
$\overline{\text{DAF}}$, $\overline{\text{DBF}}$	21, 24	I	Define-flag inputs. The high-to-low transition of $\overline{\text{DAF}}$ stores the binary value on A0–A8 as the almost-full/almost-empty offset value for FIFO A (X). The high-to-low transition of $\overline{\text{DBF}}$ stores the binary value of B0–B8 as the almost-full/almost-empty offset value for FIFO B (Y).
$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	20, 25	O	Empty flags. $\overline{\text{EMPTYA}}$ and $\overline{\text{EMPTYB}}$ are low when their corresponding memories are empty and high when they are not empty.
$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	18, 27	O	Full flags. FULLA and FULLB are low when their corresponding memories are full and high when they are not full.
HFA, HFB	16, 29	O	Half-full flags. HFA and HFB are high when their corresponding memories contain 512 or more words, and low when they contain 511 or less words.
LOCKA, LOCKB	17, 28	I	Lead clocks. Data on A0–A8 is written into FIFO A on a low-to-high transition of LDCKA. Data on B0–B8 is written into FIFO B on a low-to-high transition of LDCKB. When the FIFOs are full, load clock signals have no effect on the data residing in memory.
DIR, $\overline{\text{OE}}$	2, 43	I	Enable inputs. DIR and $\overline{\text{OE}}$ control the transceiver functions. When OE is high, both A0–A8 and B0–B8 are in the high-impedance state and can be used as inputs. With $\overline{\text{OE}}$ low and DIR high, the A bus is in the high-impedance state and B bus is active. When both $\overline{\text{OE}}$ and DIR are low, the A bus is active and the B bus is in the high-impedance state.
$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$	22, 23	I	Resets. A reset is accomplished in each direction by taking $\overline{\text{RSTA}}$ and $\overline{\text{RSTB}}$ low. This sets $\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$, $\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$, and AF/AEB high. Both FIFOs must be reset upon power up.
SAB, SBA	1, 44	I	Select-control inputs. SAB and SBA select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown in Figure 1.
$\overline{\text{UNCKA}}$, $\overline{\text{UNCKB}}$	19, 26	I	Unload clocks. Data in FIFO A is read to B0–B8 on a low-to-high transition of UNCKB. Data in FIFO B is read to A0–A8 on a low-to-high transition of UNCKB. When the FIFOs are empty, unload clock signals have no effect on data residing in memory.

programming procedure for AF/AEA

The almost-full/almost-empty flags (AF/AEA, AF/AEB) are programmed during each reset cycle. The almost-full/almost-empty offset value FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

user-defined X

Take $\overline{\text{DAF}}$ from high to low. This stores A0 thru A8 as X.
If $\overline{\text{RSTA}}$ is not already low, take $\overline{\text{RSTA}}$ high.
With $\overline{\text{DAF}}$ held low, take $\overline{\text{RSTA}}$ high. This defines the AF/AEA flag using X.
To retain the current offset for the next reset, keep $\overline{\text{DAF}}$ low.

default X

To redefine the AF/AE flag using the default value of X = 256, hold $\overline{\text{DAF}}$ high during the reset cycle.

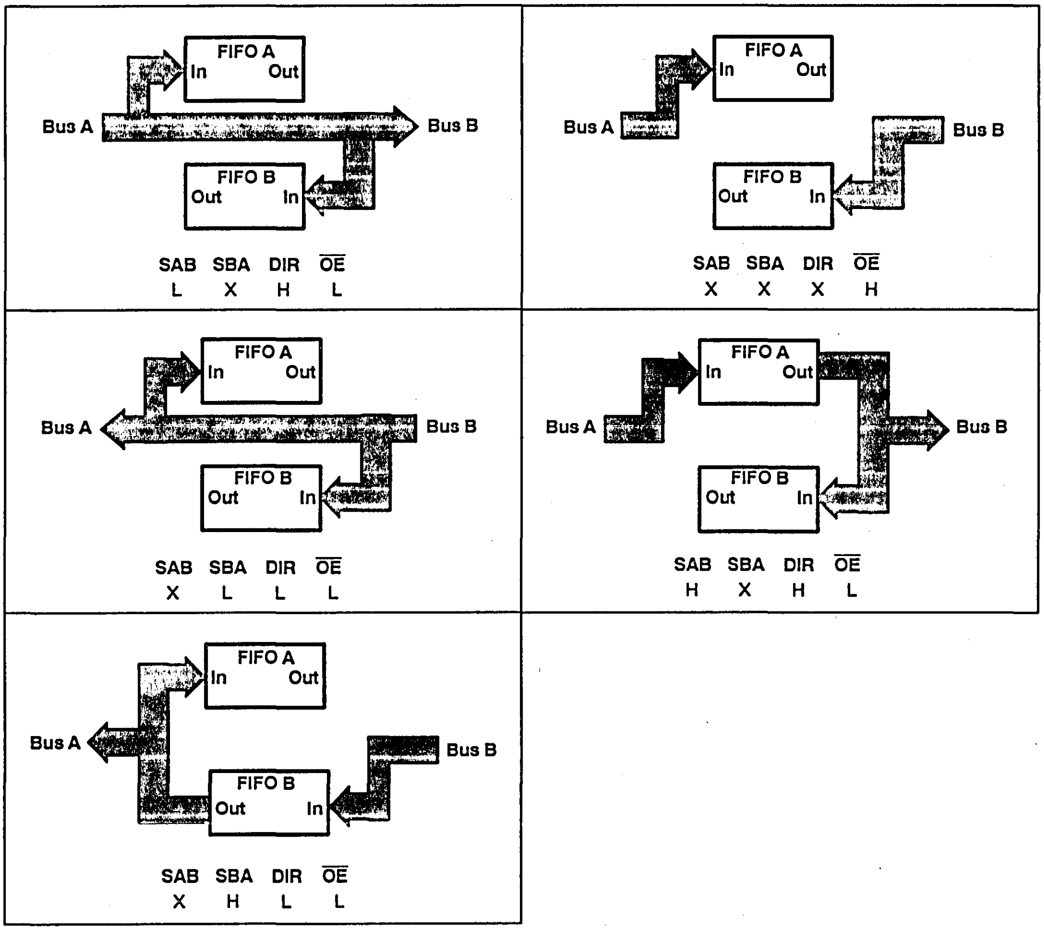
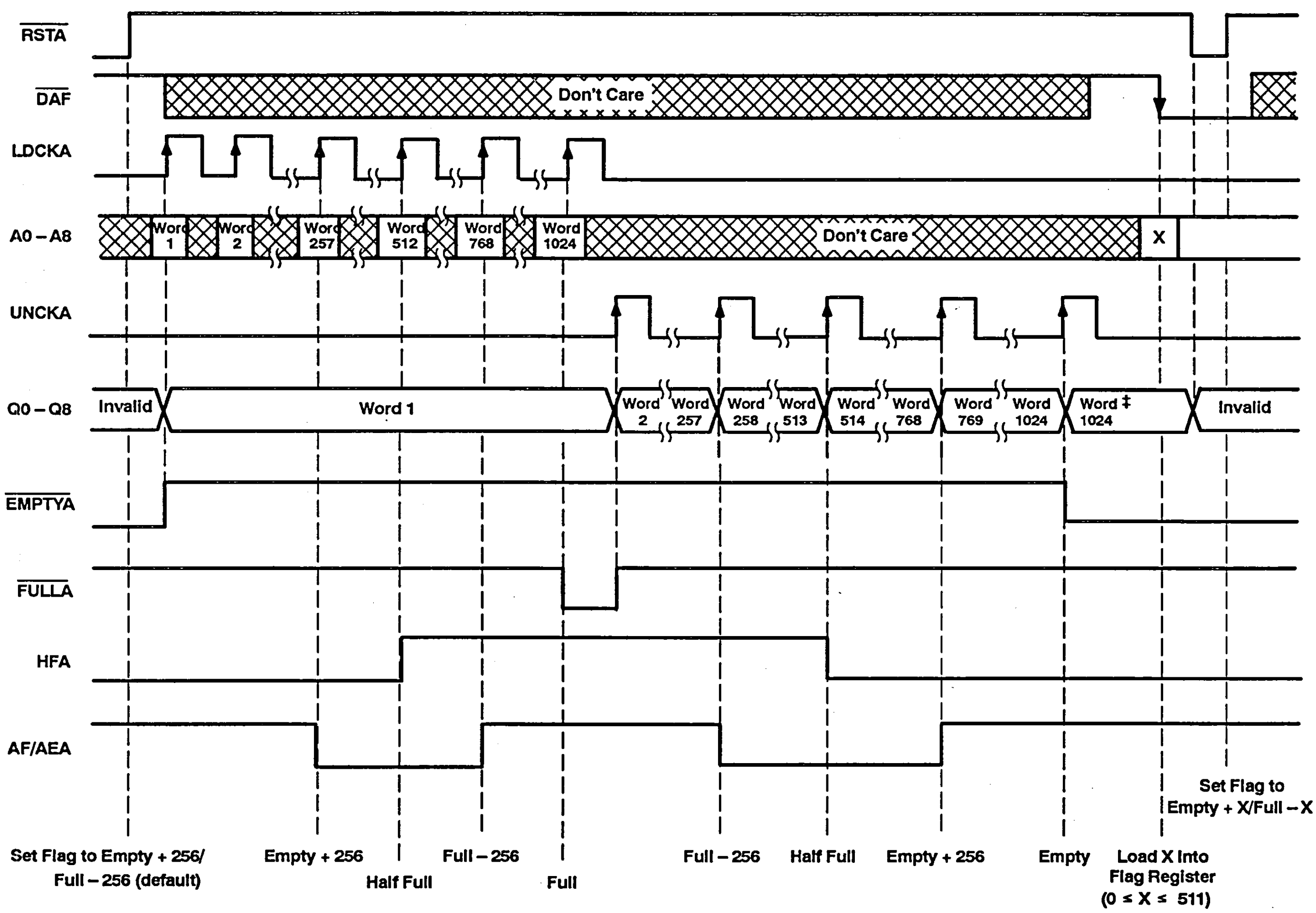


Figure 1. Bus-Management Functions

timing diagram for FIFO A†



† Operation of FIFO B is identical to that of FIFO A.
‡ Last valid data stays on outputs when FIFO goes empty due to a read.

SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SAB	SBA	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
L	H	FIFO B to A bus	Real-time A to B bus
H	L	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
DIR	$\overline{OE}$	A BUS	B BUS
X	H	Input	Input
L	L	Output	Input
H	L	Input	Output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Maximum junction temperature	150°C

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† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT2236-20		'ACT2236-30		'ACT2236-40		'ACT2236-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	A or B ports		−8		−8		−8		−8	mA
		Status flags		−8		−8		−8		−8	
I_{OL}	Low-level output current	A or B ports		16		16		16		16	mA
		Status flags		8		8		8		8	
f_{clock}	Clock frequency	LDCKA or LDCKB		50		33		25		16.7	MHz
		UNCKA or UNCKB		50		33		25		16.7	
t_w	Pulse duration	$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low	20		20		25		25		ns
		LDCKA or LDCKB low	8		10		14		20		
		LDCKA or LDCKB high	8		10		14		20		
		UNCKA or UNCKB low	8		10		14		20		
		UNCKA or UNCKB high	8		10		14		20		
		$\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high	10		10		10		10		
t_{su}	Setup time	Data before LDCKA or LDCKB↑	4		4		5		5		ns
		Define AF/AE: D0–D8 before $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	5		5		5		5		
		Define AF/AE: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓ before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	7		7		7		7		
		Define AF/AE (default): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	5		5		5		5		
		$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ inactive (high) before LDCKA or LDCKB↑	5		5		5		5		
t_h	Hold time	Data after LDCKA or LDCKB↑	1		1		2		2		ns
		Define AF/AE: D0–D8 after $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	0		0		0		0		
		Define AF/AE: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ low after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0		0		0		0		
		Define AF/AE (default): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0		0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	I/O ports	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}‡		V_I = V_{CC} – 0.2 V or 0				10	400	µA
ΔI_{CC}§	DIR, $\overline{OE}$	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2	mA
	Other inputs						1	
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I_{CC} tested with outputs open.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT2236-20			'ACT2236-30		'ACT2236-40		'ACT2236-60		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK		50			33		25		16.7		MHz
	UNCK		50			33		25		16.7		
t_{pd}	LDCK↑, LDCKB↑	B or A	8		23	8	23	8	25	8	27	ns
t_{pd}	UNCKA↑, UNCKB↑	B or A	10	17	25	10	25	10	35	10	45	ns
t_{PLH}	LDCK↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	4		15	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	2		17	2	17	2	19	2	21	ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{EMPTYA}$, $\overline{EMPTYB}$	2		18	2	18	2	20	2	22	ns
t_{PHL}	LDCK↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	4		15	4	15	4	17	4	19	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	4		15	4	15	4	17	4	19	ns
t_{PLH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	$\overline{FULLA}$, $\overline{FULLB}$	2		15	2	15	2	17	2	19	ns
t_{PLH}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	AF/AEA, AF/AEB	2		15	2	15	2	17	2	19	ns
t_{PLH}	LDCK↑, LDCKB↑	HFA, HFB	2		15	2	15	2	17	2	19	ns
t_{PHL}	UNCKA↑, UNCKB↑	HFA, HFB	4		19	4	19	4	21	4	23	ns
t_{PHL}	$\overline{RSTA}$↓, $\overline{RSTB}$↓	HFA, HFB	1		15	1	15	1	17	1	19	ns
t_{pd}	SAB or SBA¶	B or A	1		11	1	11	1	13	1	15	ns
t_{pd}	A or B	B or A	1		11	1	11	1	13	1	15	ns
t_{pd}	LDCK↑, LDCKB↑	AF/AEA, AF/AEB	2		19	2	19	2	21	2	23	ns
t_{pd}	UNCKA↑, UNCKB↑	AF/AEA, AF/AEB	2		19	2	19	2	23	2	23	ns
t_{en}	DIR, $\overline{OE}$	A or B	2		12	2	12	2	14	2	16	ns
t_{dis}	DIR, $\overline{OE}$	A or B	1		10	1	10	1	12	1	14	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	Outputs enabled	C_L = 50 pF, f = 5 MHz	71	pF
		Outputs disabled		57	

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

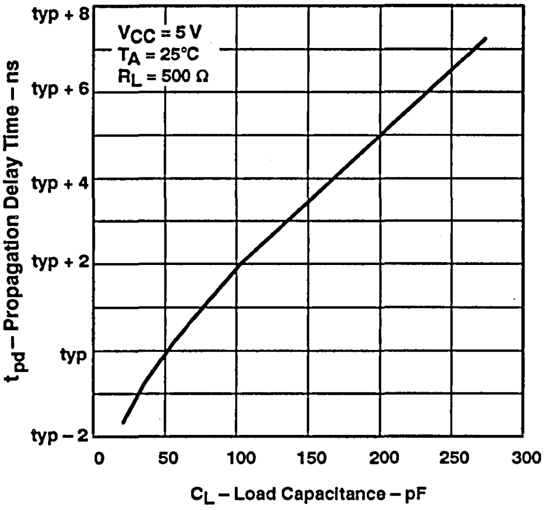


Figure 2

POWER DISSIPATION CAPACITANCE
vs
SUPPLY VOLTAGE

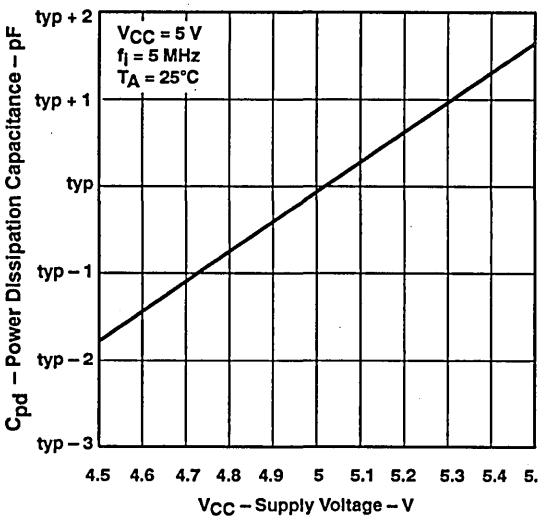


Figure 3

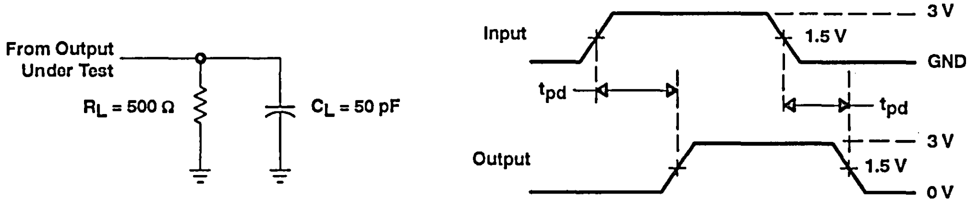
calculating power dissipation

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

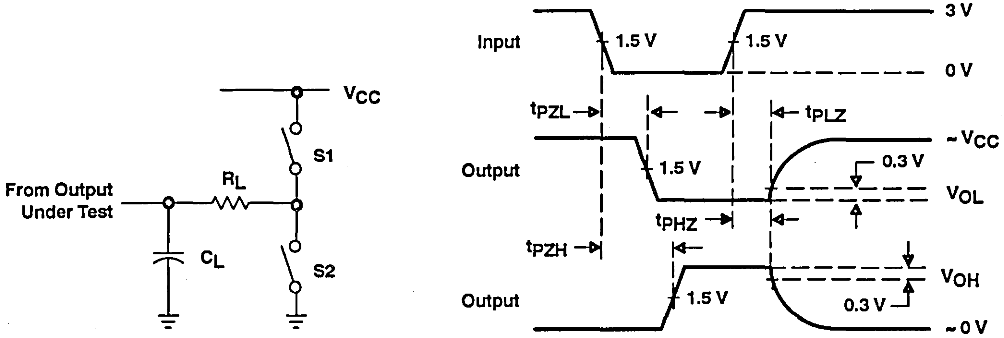
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 4. Standard CMOS Outputs (All Flags)



LOAD CIRCUIT

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R_L	C_L†	S1	S2
t_{en}	t_{PZH}	500 Ω	50 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		–	50 pF	Open	Open

† Includes probe and test-fixture capacitance

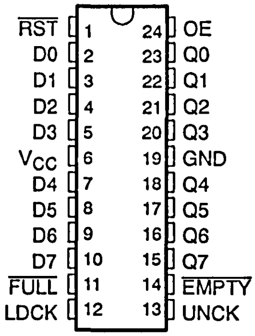
Figure 5. 3-State Outputs (A0–A8, B0–B8)

SN74ALS2232A
64 × 8 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

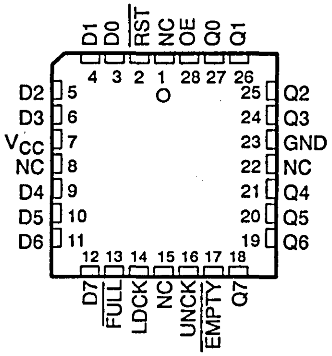
SCAS248 – FEBRUARY 1988 – REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 8 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 512-bit memory uses advanced low-power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock (LDCK) input and is read out on a low-to-high transition of the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the the memory is empty, UNCK signals have no effect.

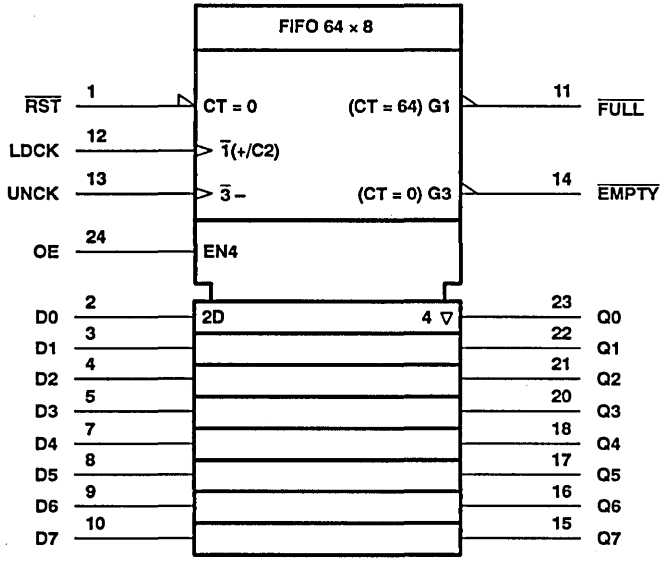
Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable (OE) input is low. The OE input does not effect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232A is characterized for operation from 0°C to 70°C.

IMPACT-X is a trademark of Texas Instruments Incorporated.

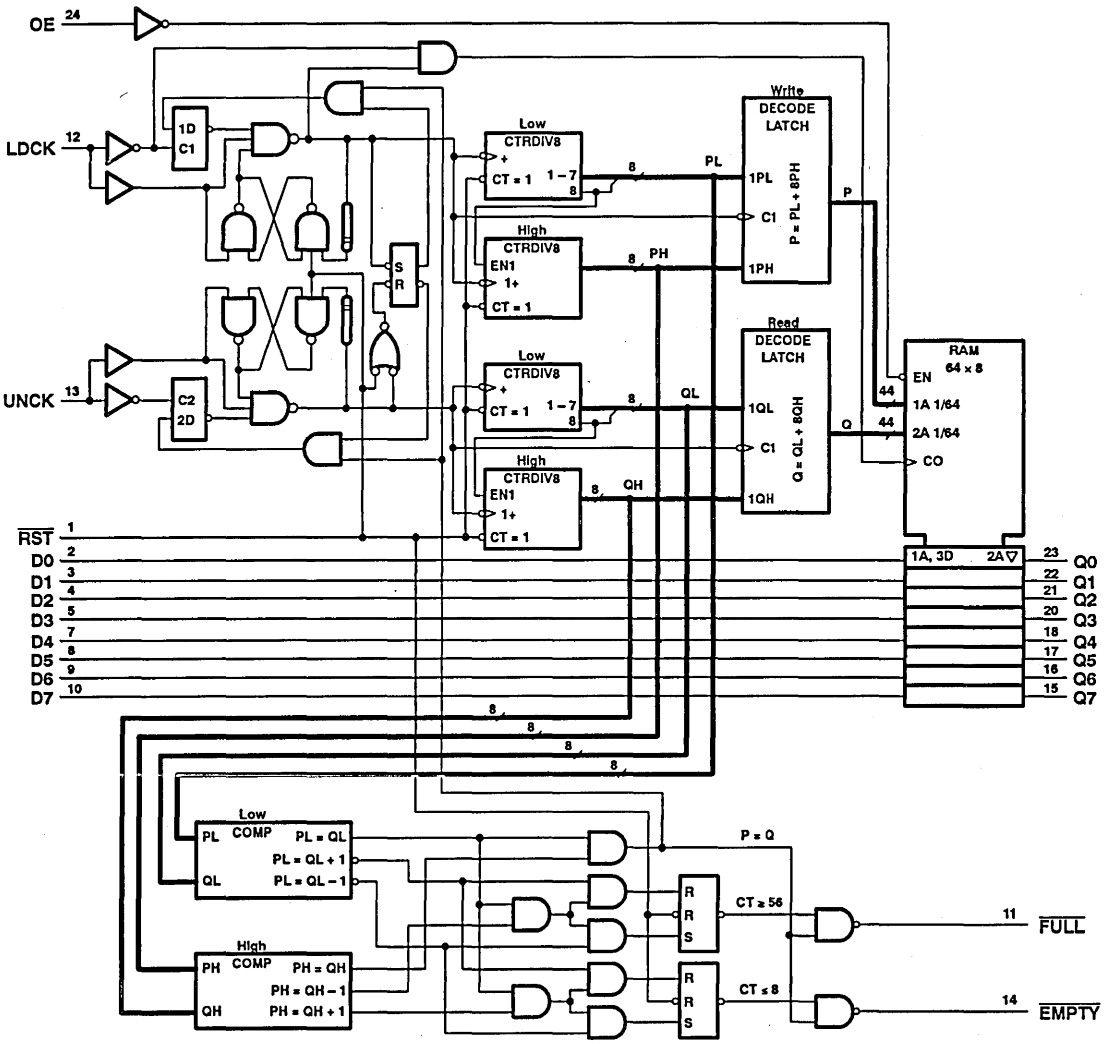
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

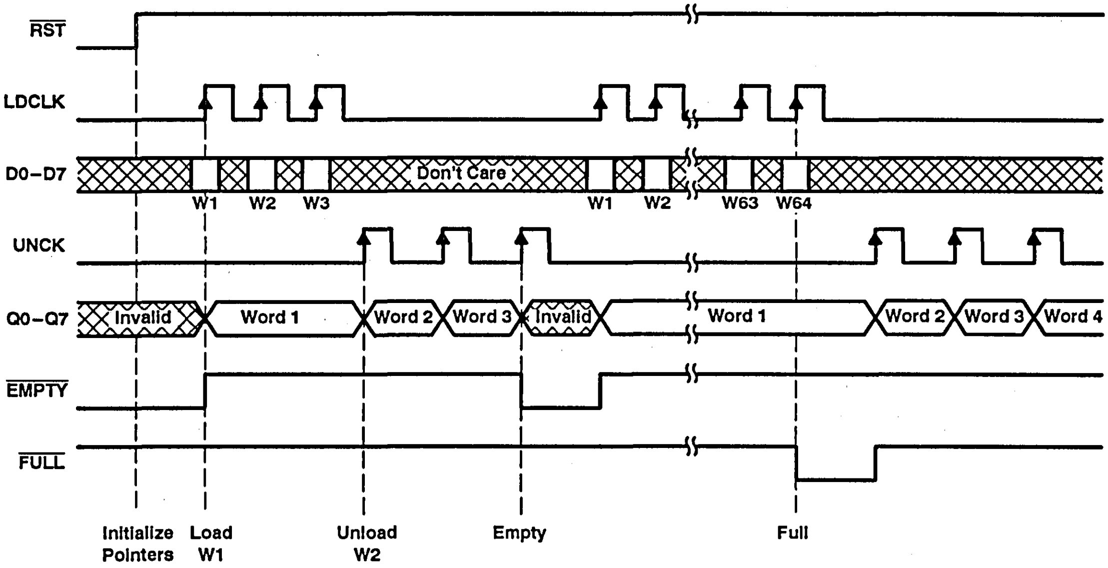
Pin numbers shown are for the NT package.

logic diagram (positive logic)



Pin numbers shown are for the NT package.

timinig diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{\text{RST}}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{\text{RST}}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
	$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$	V_{CC} = MIN to MAX,	I_{OH} = 0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	CLKs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Others					−0.1	
I_O§	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	270	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

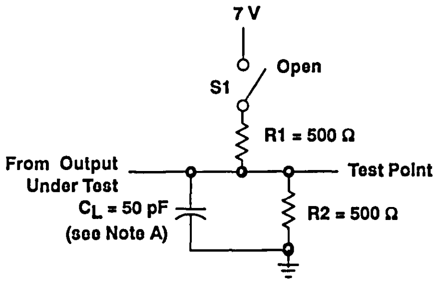
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MAX	TYP	MAX	MIN	MAX	
f_{max}	LDCK, UNCK					40		MHz
t_{pd}	LDCK↑	Any Q		18	26		30	ns
	UNCK↑			18	24		27	
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$		12	16		18	ns
t_{PHL}	UNCK↑			12	17		20	
t_{PHL}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY}}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$		10	15		18	ns
	$\overline{\text{RST}}$↓			13	19		23	
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

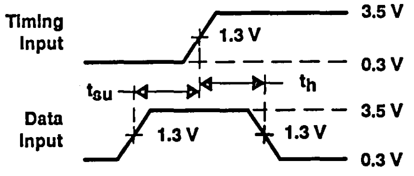
PARAMETER MEASUREMENT INFORMATION



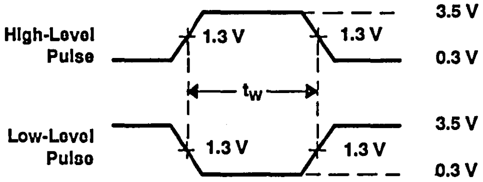
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

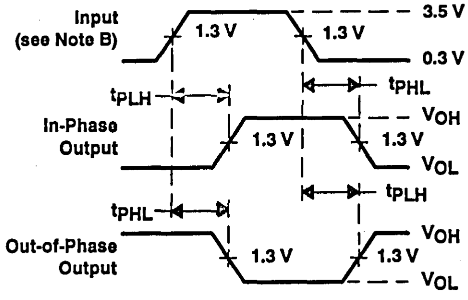
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



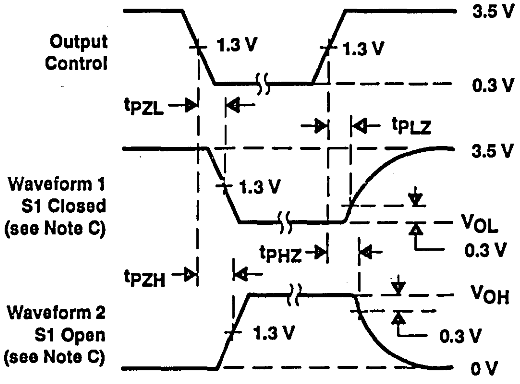
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

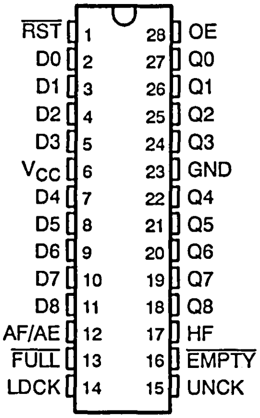
Figure 1. Load Circuit and Voltage Waveforms

SN74ALS2233A
64 × 9 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

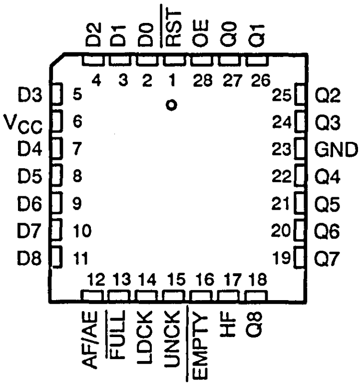
SCAS249 – FEBRUARY 1988 – REVISED MARCH 1990

- **Independent Asynchronous Inputs and Outputs**
- **64 Words by 9 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 20 ns Typical**
- **3-State Outputs**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 576-bit memory uses advanced low-power Schottky IMPACT-X ™ technology and features high speed and fast fall-through times. It is organized as 64 words by 9 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock (LDCK) input and is read out on a low-to-high transition of the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the the memory is empty, UNCK signals have no effect.

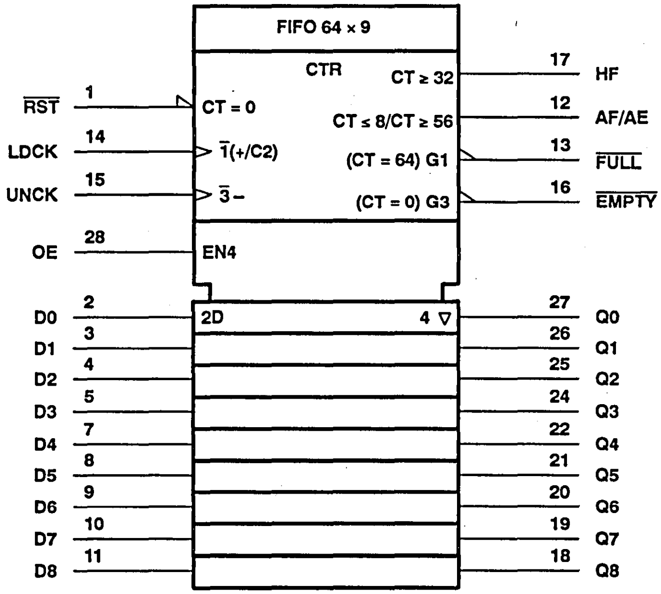
Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, almost-full/almost-empty (AF/AE), and half-full (HF) output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty, and high when it is not empty. The AF/AE flag is high when the FIFO contains eight or less words or 56 or more words. The AF/AE flag is low when the FIFO contains between nine and 55 words. The HF flag is high when the FIFO contains 32 or more words and is low when the FIFO contains 31 words or less.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and $\overline{\text{FULL}}$ high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable (OE) input is low. The OE input does not effect either the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2233A is characterized for operation from 0°C to 70°C.

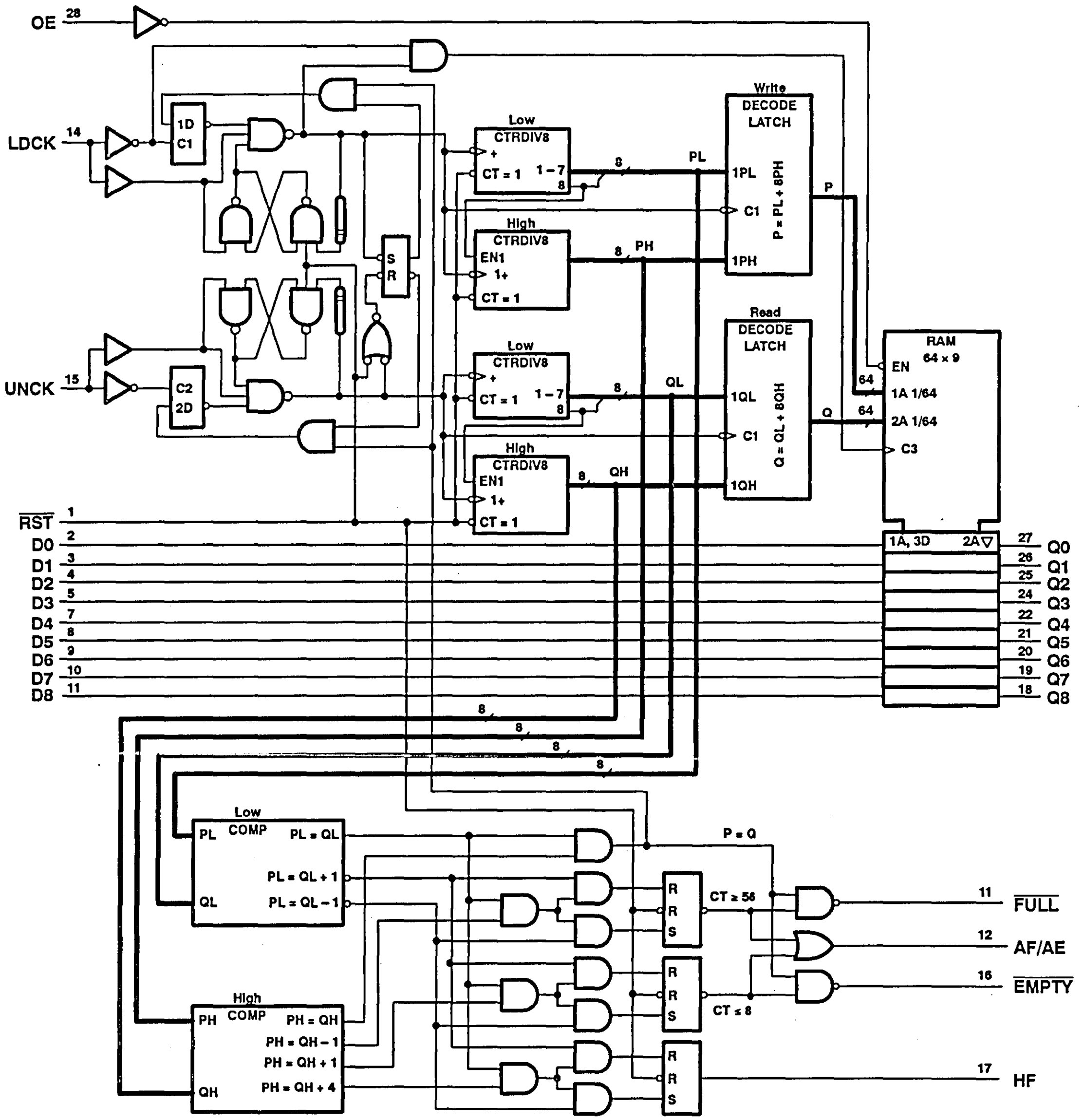
IMPACT-X is a trademark of Texas Instruments Incorporated.

logic symbol†

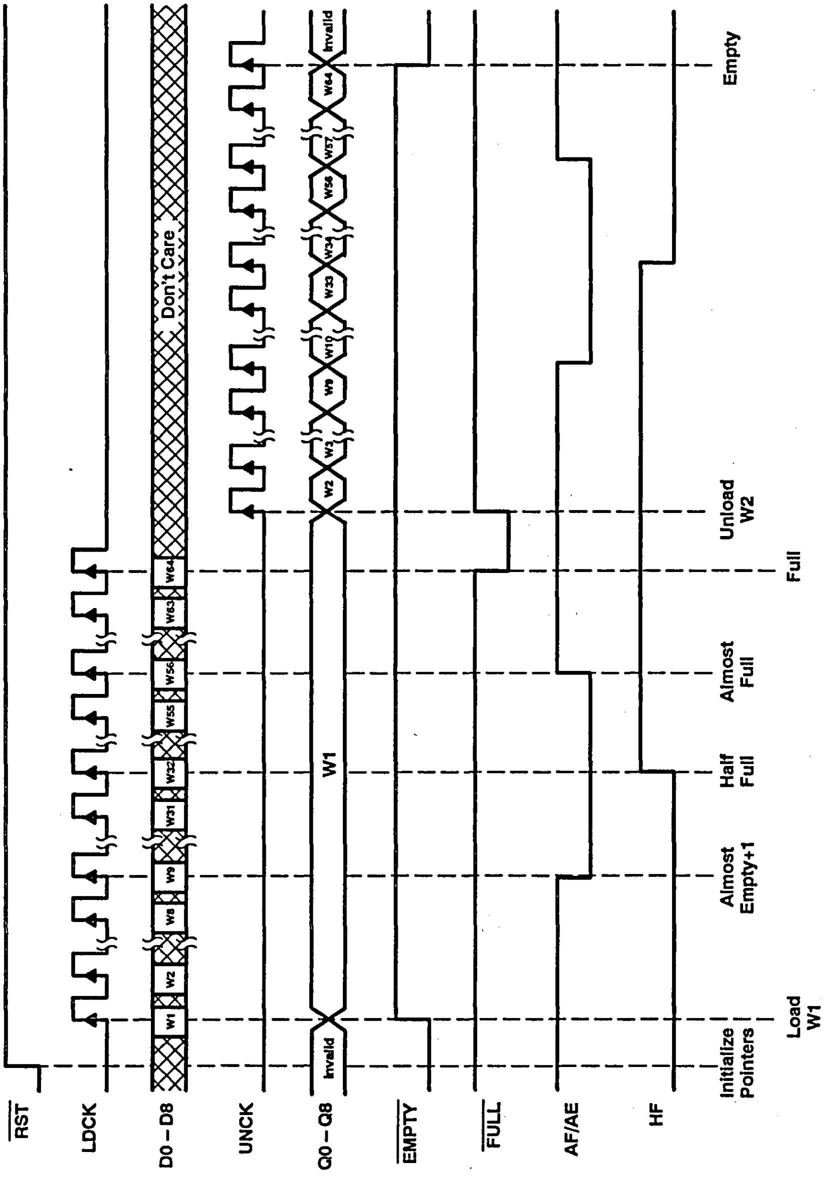


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		Flag outputs			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Flag outputs			8	
f_{clock}	Clock frequency	LDCK, UNCK	0		40	MHz
t_w	Pulse duration	$\overline{RST}$ low	25			ns
		LDCK low	13			
		LDCK high	12			
		UNCK low	13			
		UNCK high	12			
t_{su1}	Setup time, data before LDCK↑		5			ns
t_{su2}	Setup time, $\overline{RST}$ high (inactive) before LDCK↑		5			ns
t_h	Hold time, data after LDCK↑		5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
	Flag outputs	V_{CC} = MIN to MAX,	I_{OH} = 0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	Flag outputs	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	CLKs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Others					−0.1	
I_O§	Q outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−130	mA
	Flag outputs			−20		−112	
I_{CC}		V_{CC} = 5.5 V			175	290	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

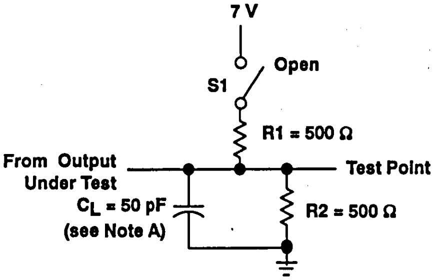
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK, UNCK					40		MHz
t_{pd}	LDCK↑	Any Q		18	26		30	ns
	UNCK↑			18	24		27	
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$		12	16		18	ns
t_{PHL}	UNCK↑			12	17		20	
t_{PHL}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY}}$		12	17		20	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$		16	21		22	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$		10	15		18	ns
	$\overline{\text{RST}}$↓			13	19		23	
t_{PLH}	LDCK↑	AF/AE		22	27		30	ns
t_{PHL}				19	25		28	
t_{PLH}	UNCK↑	AF/AE		22	27		30	ns
t_{PHL}				17	23		26	
t_{PLH}	$\overline{\text{RST}}$↓	AF/AE		12	16		18	ns
t_{PLH}	LDCK↑	HF		22	27		30	ns
t_{PHL}	$\overline{\text{RST}}$↓			28	32		35	
t_{PHL}	UNCK↑	HF		16	22		25	ns
t_{en}	OE↑	Q		11	15		17	ns
t_{dis}	OE↓	Q		11	17		19	ns

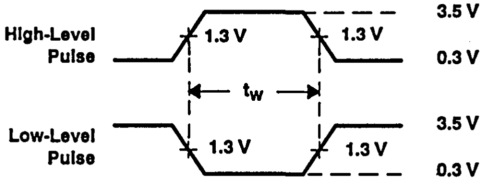
PARAMETER MEASUREMENT INFORMATION



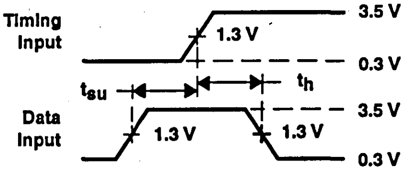
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

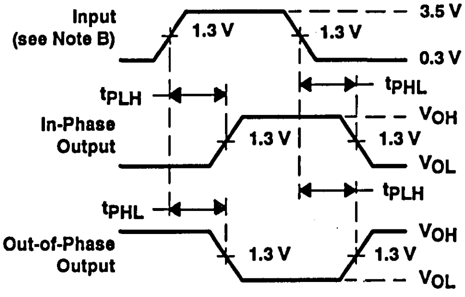
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



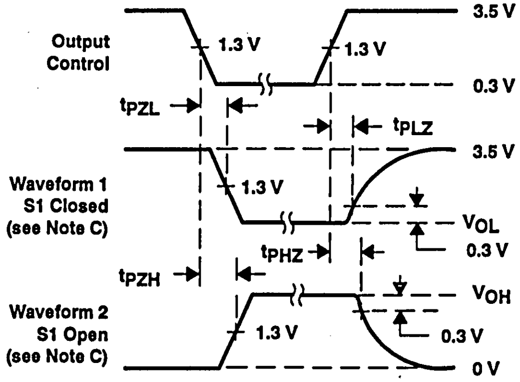
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74ALS2238
32 × 9 × 2 ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

SCAS250 – APRIL 1990

- **Independent Asychronous Inputs and Outputs**
- **Bidirectional**
- **32 Words by 9 Bits**
- **Programmable Depth**
- **Data Rates from 0 to 40 MHz**
- **Fall-Through Time . . . 22 ns Typ**
- **3-State Outputs**

description

This 576-bit memory uses advanced low-power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

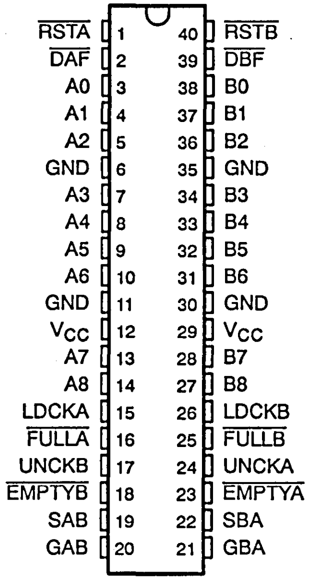
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

The SN74ALS2238 consists of bus-transceiver circuits, two 32 × 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enables GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown in Figure 1.

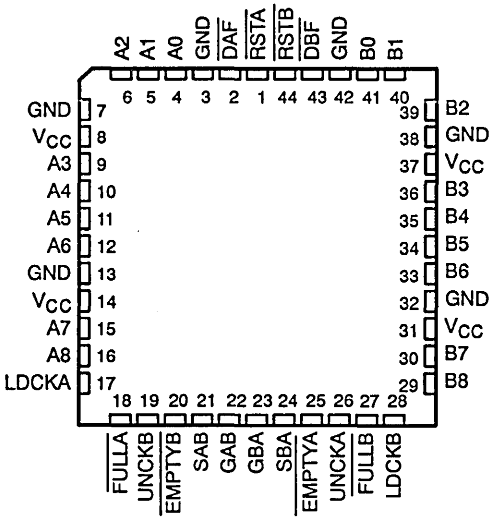
Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock (LDCKA or LDCKB) input and is read out on a low-to-high transition at the unload clock (UNCKA or UNCKB) input. The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.

When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



IMPACT-X is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
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description (continued)

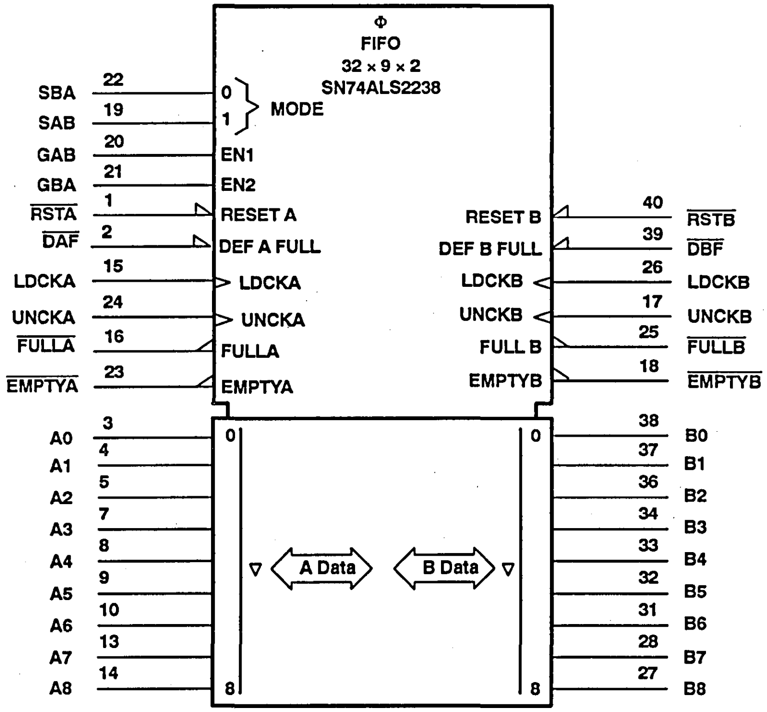
Status of the FIFO memories is monitored by the FULLA, FULLB, EMPTYA, and EMPTYB output flags. The FULLA and FULLB are definable full flags. A high-to-low transition on DAF stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on DBF stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to 32 words deep. The value of X and Y must be defined after power up or the stored value of X and Y will be ambiguous. The FULLA and FULLB outputs are low when their corresponding memories are full and high when the memories are not full.

The EMPTYA and EMPTYB outputs are low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

A low-level pulse on the RSTA or RSTB inputs resets the control pointers on FIFO A or FIFO B and also sets EMPTYA low and FULLA high or EMPTYB low and FULLB high. The outputs are not reset to any specific logic levels. With DAF at a low level, a low-level pulse on RSTA sets FIFO A to a depth of 32 – X, where X is the value stored above. With DAF at a high level, a low level pulse on RSTA sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause EMPTYA or EMPTYB to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2238 is characterized for operation from 0°C to 70°C.

logic symbol†



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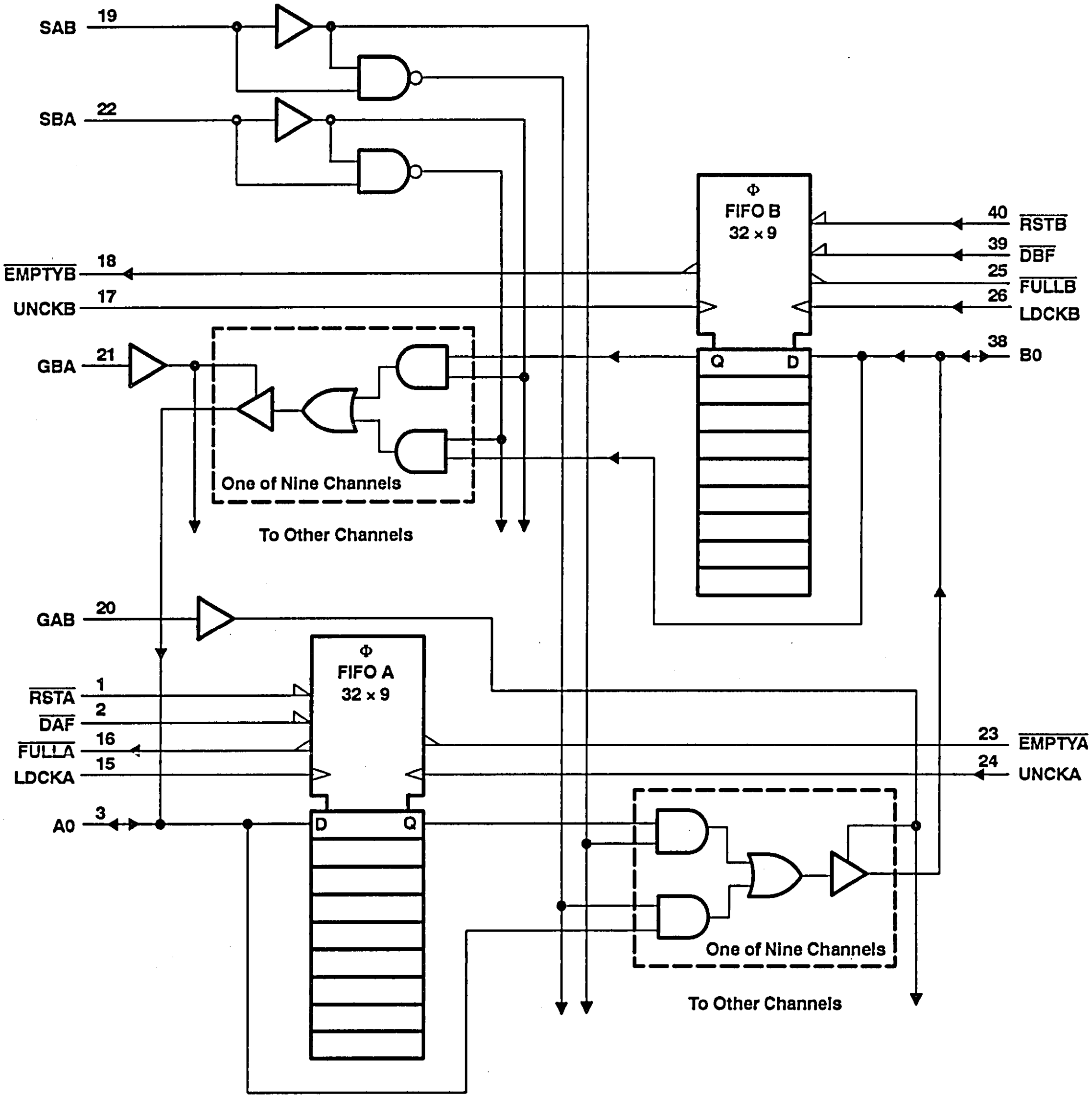
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



Pin numbers shown are for the N package.

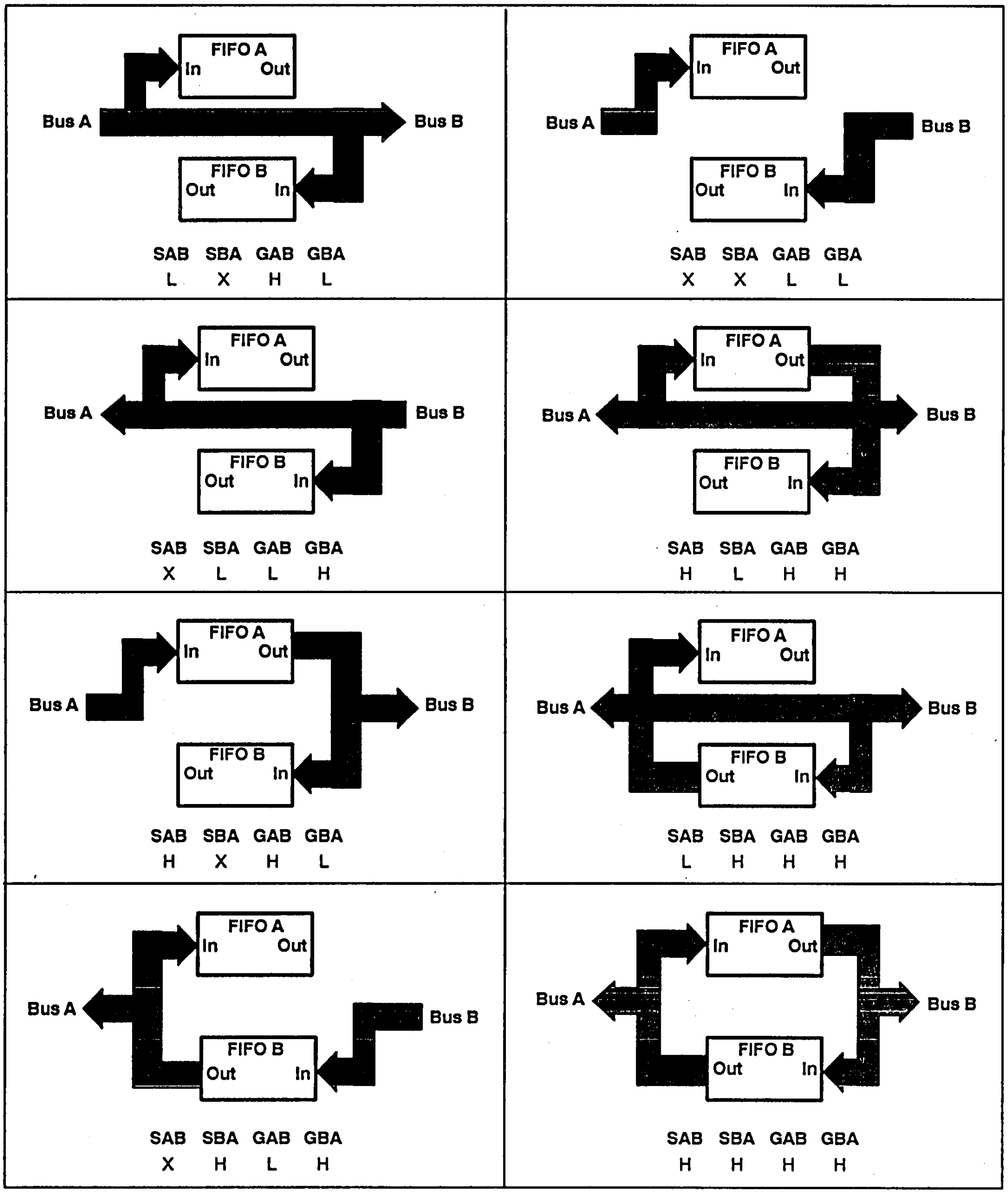
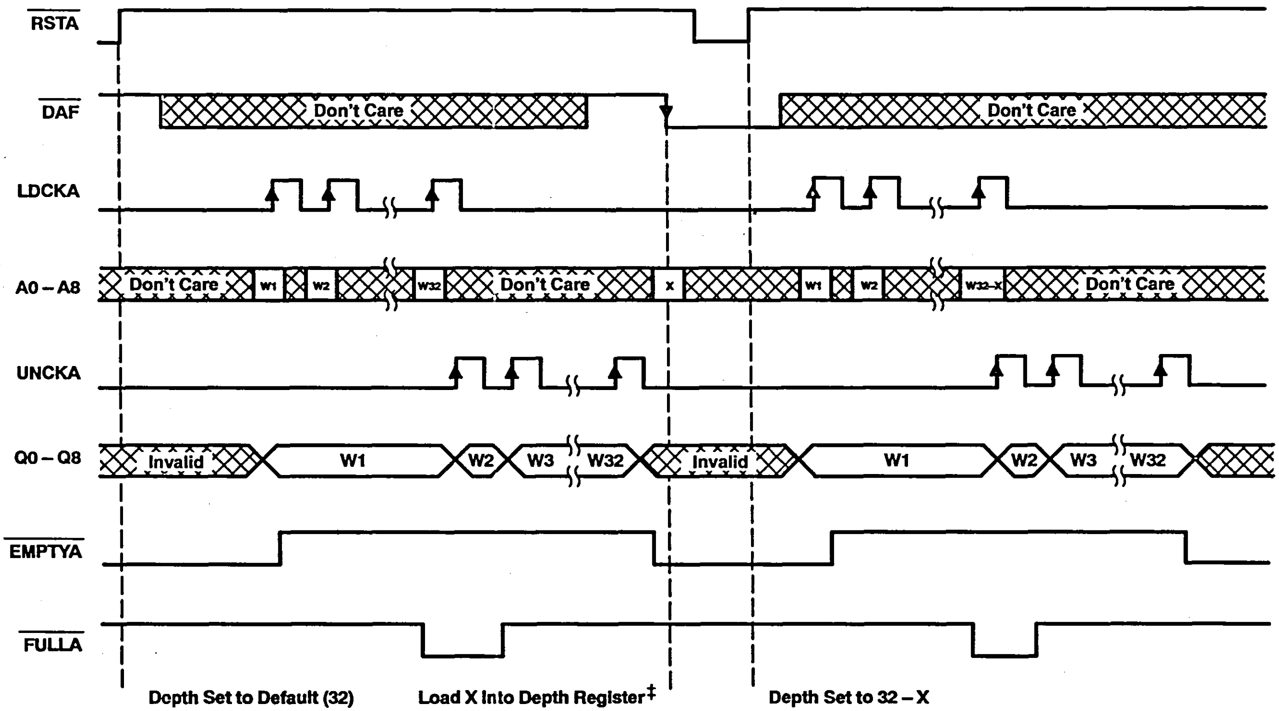


Figure 1. Bus-Management Functions

timing diagram for FIFO A[†]



[†] Operation of FIFO B is identical to that of FIFO A.

[‡] X includes A0 through A4 only. A5 through A8 are ignored.

SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SAB	SBA	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
L	H	FIFO B to A bus	Real-time A to B bus
H	L	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
GAB	GBA	A BUS	B BUS
H	H	A bus enabled	B bus enabled
L	H	A bus enabled	Isolation/input to B bus
H	L	Isolation/input to A bus	B bus enabled
L	L	Isolation/input to A bus	Isolation/input to B bus

programming procedure for depth of FIFO A†

Program:

Step 1. With $\overline{\text{RSTA}}$ at a high level, take $\overline{\text{DAF}}$ from a high level to a low level. The high-to-low transition on $\overline{\text{DAF}}$ stores the binary value of A0–A4 for use as the value of X in defining the depth of FIFO A.

Step 2. With $\overline{\text{DAF}}$ held low, pulse the $\overline{\text{RSTA}}$ signal low. On the low-to-high transition of $\overline{\text{RSTA}}$, FIFO A is set to a depth of 32 – X, where X is the value of A0–A4 stored above.

Step 3. To redefine the depth of FIFO A to 32 words, hold $\overline{\text{DAF}}$ at a high level and pulse the $\overline{\text{RSTA}}$ signal low.

† The programming procedures used to define the depth of FIFO B are the same as the procedure above.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C
Maximum junction temperature	150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	A or B ports			−15	mA
		Status flags			−0.4	
I_{OL}	Low-level output current	A or B ports			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCKA or LDCKB	0		40	MHz
		UNCKA or UNCKB	0		40	
t_w	Pulse duration	$\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low	17			ns
		LDCKA or LDCKB low	12.5			
		LDCKA or LDCKB high	10			
		UNCKA or UNCKB low	12.5			
		UNCKA or UNCKB high	10			
		$\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high	10			
t_{su}	Setup time	Data before LDCKA or LDCKB↑	7			ns
		Define depth: D4–D0 before $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	6			
		Define depth: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓ before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	45			
		Define depth (32): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	32			
		LDCKA or LDCKB (inactive) before $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	5			
t_h	Hold time	Data after LDCKA or LDCKB↑	3			ns
		Define depth: D4–D0 after $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$↓	4			
		Define depth: $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ low after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0			
		Define depth (32): $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ high after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	0			
		LDCKA or LDCKB (inactive) after $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$↑	5			
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the V_{IL}, V_{IH}, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V
	A or B ports	V_{CC} = 4.5 V,	I_{OH} = – 2 mA	V_{CC}–2			
		V_{CC} = 4.5 V,	I_{OH} = – 3 mA	2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = –15 mA	2			
V_{OL}	A or B ports	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_I	$\overline{\text{DAF}}$, $\overline{\text{DBF}}$, $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	A or B ports					0.2	
I_{IH}	$\overline{\text{DAF}}$, $\overline{\text{DBF}}$, $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports‡					40	
I_{IL}	$\overline{\text{DAF}}$, $\overline{\text{DBF}}$, $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2	mA
	A or B ports‡					–0.4	
I_O§	A or B ports‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–130	mA
	Status flags			–15		–100	
I_{CC}		V_{CC} = 5.5 V			190	350	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

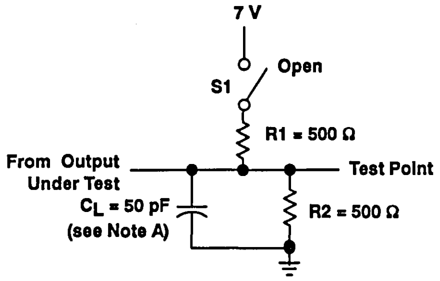
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f_{max}	LDCK, UNCK		40			MHz
t_{pd}	LDCKA↑, LDCKB↑	B, A	7	22	33	ns
	UNCKA↑, UNCKB↑		7	20	29	
t_{PLH}	LDCKA↑, LDCKB↑	EMPTYA, EMPTYB	5	12	22	ns
t_{PHL}	UNCKA↑, UNCKB↑		5	12	22	
t_{PHL}	$\overline{\text{RSTA}}$↓, $\overline{\text{RSTB}}$↓	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	5	12	22	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	5	12	22	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	5	12	23	ns
	$\overline{\text{RSTA}}$↓, $\overline{\text{RSTB}}$↓		6	15	28	
t_{pd}	SAB, SBA‡	B, A	2	11	18	ns
	A/B		2	8	15	
t_{en}	GBA, GAB	A, B	2	6	15	ns
t_{dis}	GBA, GAB	A, B	1	5	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

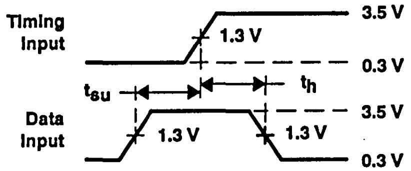
PARAMETER MEASUREMENT INFORMATION



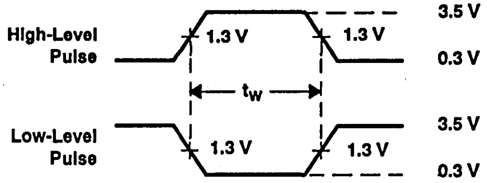
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

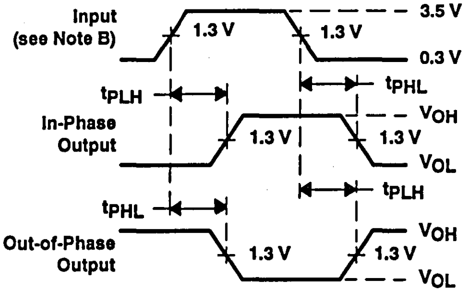
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



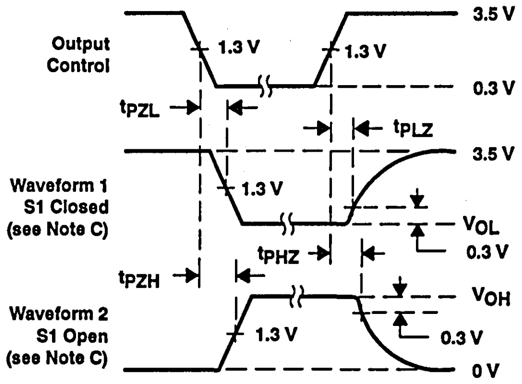
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r \le 2$ ns, $t_f \le 2$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

9-BIT ASYNCHRONOUS FIFOS

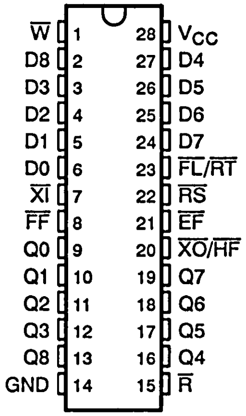
Features	Benefits
Multiple speed sort options	Design flexibility
Depth from 256 to 4K words	Optimize depth for specific application
Fast data access time of 15 ns	Increased system performance
Bit-width and word-depth expandable	Allows interface to larger and deeper data paths
Empty, full, and half-full flags	Multiple status flags to ease design efforts
Compatible to 720x pinout	Drop-in replaceable to existing layouts and designs
TI has established an alternate source	Standardization that comes from a common-product approach

SN74ACT7200L, SN74ACT7201LA, SN74ACT7202LA
256 × 9, 512 × 9, AND 1K × 9
FIRST-IN, FIRST-OUT MEMORIES

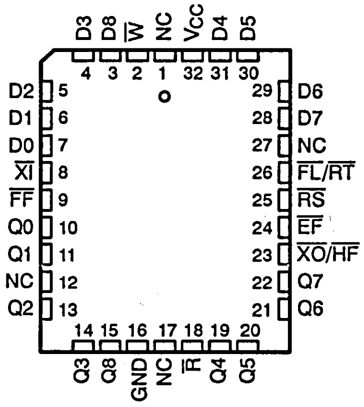
SCAS221 – FEBRUARY 1993 – REVISED JUNE 1993

- **Reads and Writes Can Be Asynchronous or Coincident**
- **Organization:**
  - **– SN74ACT7200L – 256 × 9**
  - **– SN74ACT7201LA – 512 × 9**
  - **– SN74ACT7202LA – 1K × 9**
- **Fast Data Access Times of 15 ns**
- **Read and Write Frequencies up to 40 MHz**
- **Bit-Width and Word-Depth Expansion**
- **Fully Compatible With the IDT7200/7201/7202**
- **Retransmit Capability**
- **Empty, Full, and Half-Full Flags**
- **TTL-Compatible Inputs**
- **Available in 28-Terminal Plastic DIP (NP) and Small-Outline (DV) Packages and 32-Terminal Plastic J-Leaded Chip-Carrier (RJ) Packages**

DV OR NP PACKAGE
(TOP VIEW)



RJ PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and can be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth-expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

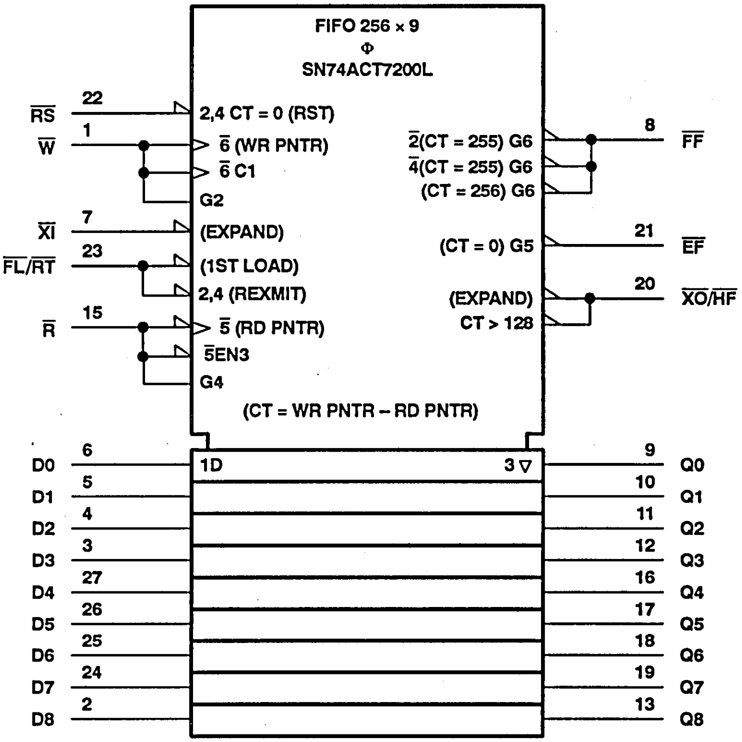
Data is loaded into memory by the write-enable ($\overline{W}$) input and unloaded by the read-enable ($\overline{R}$) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are characterized for operation from 0°C to 70°C.

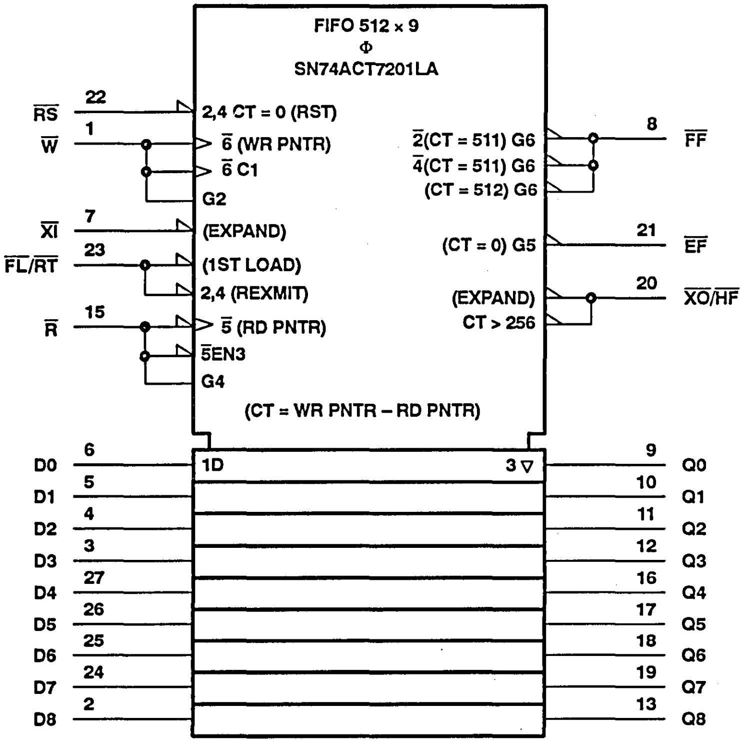
TEXAS INSTRUMENTS

SN74ACT7200L logic symbol†



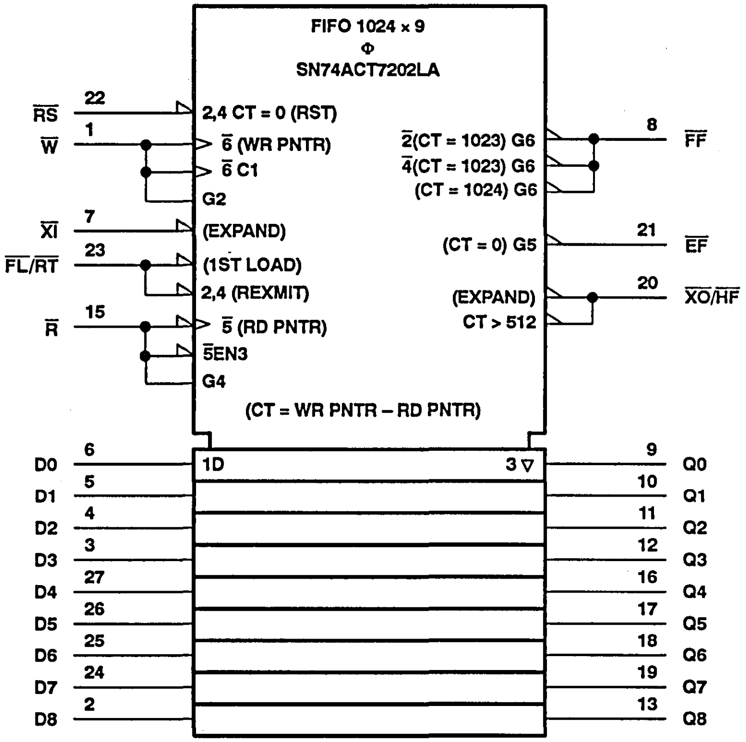
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

SN74ACT7201LA logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

SN74ACT7202LA logic symbol†



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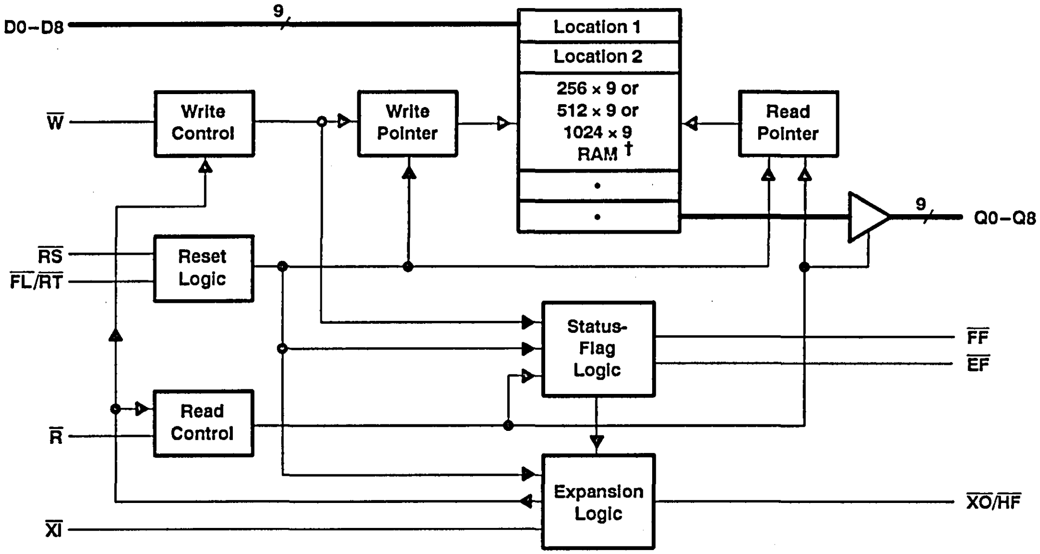
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

functional block diagram



† 256 × 9 for SN74ACT7200L; 512 × 9 for SN74ACT7201LA; 1024 × 9 for SN74ACT7202LA

RESET AND RETRANSMIT FUNCTION TABLE
(single-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
$\overline{\text{RS}}$	$\overline{\text{FL}}/\overline{\text{RT}}$	$\overline{\text{XI}}$	READ POINTER	WRITE POINTER	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{XO}}/\overline{\text{HF}}$	
L	X	L	Location zero	Location zero	L	H	H	Reset device
H	L	L	Location zero	Unchanged	X	X	X	Retransmit
H	H	L	Increment if $\overline{\text{EF}}$ high	Increment if $\overline{\text{FF}}$ high	X	X	X	Read/write

RESET AND FIRST-LOAD FUNCTION TABLE
(multiple-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
$\overline{\text{RS}}$	$\overline{\text{FL}}/\overline{\text{RT}}$	$\overline{\text{XI}}$	READ POINTER	WRITE POINTER	$\overline{\text{EF}}$	$\overline{\text{FF}}$	
L	L	‡	Location zero	Location zero	L	H	Reset first device
L	H	‡	Location zero	Location zero	L	H	Reset all other devices
H	X	‡	X	X	X	X	Read/write

‡ $\overline{\text{XI}}$ is connected to $\overline{\text{XO}}/\overline{\text{HF}}$ of the previous device in the daisy chain (see Figure 15).

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
D0–D8	I	Data inputs
$\overline{\mathrm{EF}}$	O	Empty-flag output. $\overline{\mathrm{EF}}$ is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at Q0–Q8 by holding $\overline{\mathrm{R}}$ low when loading the data word with a low-level pulse on $\overline{\mathrm{W}}$.
$\overline{\mathrm{FF}}$	O	Full-flag output. $\overline{\mathrm{FF}}$ is low when the write pointer is one location less than the read pointer, indicating that the device is full and inhibiting any operation initiated by a write cycle. $\overline{\mathrm{FF}}$ goes low when the number of writes after reset exceeds the number of reads by 256 for the SN74ACT7200L, 512 for the SN74ACT7201LA, and 1024 for the SN74ACT7202LA. When the FIFO is full, a data word can be written automatically into memory by holding $\overline{\mathrm{W}}$ low while reading out another data word with a low-level pulse on $\overline{\mathrm{R}}$.
$\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$	I	First-load/retransmit input. $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth expansion chain. A device is not used in depth expansion when its expansion ($\overline{\mathrm{XI}}$) input is tied to ground. In that case, $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ acts as a retransmit enable. A retransmit operation is initiated when $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. $\overline{\mathrm{R}}$ and $\overline{\mathrm{W}}$ must be at a high logic level during the low-level $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ retransmit pulse. Retransmit should be used only when less than 256/512/1024 writes are performed between resets; otherwise, an attempt to retransmit can cause the loss of unread data. The retransmit function can affect $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ depending on the relative locations of the read and write pointers.
GND		Ground
Q0–Q8	O	Data outputs. Q0–Q8 are in the high-impedance state when $\overline{\mathrm{R}}$ is high or the FIFO is empty.
$\overline{\mathrm{R}}$	I	Read-enable input. A read cycle begins on the falling edge of $\overline{\mathrm{R}}$ if $\overline{\mathrm{EF}}$ is high. This activates Q0–Q8 and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{\mathrm{R}}$ goes high. As the last stored word is read by the falling edge of $\overline{\mathrm{R}}$, $\overline{\mathrm{EF}}$ transitions low but Q0–Q8 remain active until $\overline{\mathrm{R}}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{\mathrm{R}}$.
$\overline{\mathrm{RS}}$	I	Reset input. A reset is performed by taking $\overline{\mathrm{RS}}$ low. This initializes the internal read and write pointers to the first location and sets $\overline{\mathrm{EF}}$ low, $\overline{\mathrm{FF}}$ high, and $\overline{\mathrm{HF}}$ high. Both $\overline{\mathrm{R}}$ and $\overline{\mathrm{W}}$ must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place.
V_{CC}		Supply voltage
$\overline{\mathrm{W}}$	I	Write-enable input. A write cycle begins on the falling edge of $\overline{\mathrm{W}}$ if $\overline{\mathrm{FF}}$ is high. The value on D0–D8 is stored in memory as $\overline{\mathrm{W}}$ returns high. When the FIFO is full, $\overline{\mathrm{FF}}$ is low, inhibiting $\overline{\mathrm{W}}$ from performing any operation on the device.
$\overline{\mathrm{XI}}$	I	Expansion-in input. $\overline{\mathrm{XI}}$ performs two functions. $\overline{\mathrm{XI}}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, $\overline{\mathrm{XI}}$ is connected to the expansion-out ($\overline{\mathrm{XO}}$) output of the previous device in the depth-expansion chain.
$\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$	O	Expansion-out/half-full-flag output. $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ performs two functions. When the device is not used in depth expansion (i.e., when $\overline{\mathrm{XI}}$ is tied to ground), $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on $\overline{\mathrm{W}}$ for the next write operation drives $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ low. $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ remains low until a rising edge of $\overline{\mathrm{R}}$ reduces the number of words stored to exactly half of the total memory. When the device is used in depth expansion, $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ is connected to $\overline{\mathrm{XI}}$ of the next device in the daisy chain. $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Input voltage range (any input), V_I	−0.5 V to 7 V
Continuous output current, I_O	50 mA
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−55°C to 125°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{XI}$	2.6			V
		Other inputs	2			
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.4	V
I_{OZH}	$V_O = V_{CC}$,	$\overline{R} \geq V_{IH}$				±10	μA
I_{OZL}	V_O = 0.4 V,	$\overline{R} \geq V_{IH}$				±10	μA
I_I	V_I = 0 to 5.5 V			−1		1	μA
I_{CC1}[‡]	t_a = 15 and 25 ns					125[¶]	mA
	t_a = 35 and 50 ns				50	80	
I_{CC2}[‡]	t_a = 15 and 25 ns	$\overline{R}$, $\overline{W}$, $\overline{RS}$, and $\overline{FL}/\overline{RT}$ at V_{IH}				15	mA
	t_a = 35 and 50 ns				5	8	
I_{CC3}[‡]	t_a = 15 and 25 ns	$V_I = V_{CC} - 0.2$ V				0.5	mA
	t_a = 35 and 50 ns					0.5	
C_i[§]	V_I = 0,	T_A = 25°C,	f = 1 MHz			8	pF
C_o[§]	V_O = 0,	T_A = 25°C,	f = 1 MHz			8	pF

[‡] I_{CC1} = supply current; I_{CC2} = standby current; I_{CC3} = power-down current. I_{CC} measurements are made with outputs open (only capacitive loading).

[§] This parameter is sampled and not 100% tested.

[¶] Tested at f_{clock} = 20 MHz

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		FIGURE	'ACT7200L-15 'ACT7201LA-15 'ACT7202LA-15		'ACT7200L-25 'ACT7201LA-25 'ACT7202LA-25		'ACT7201LA-35† 'ACT7202LA-35†		'ACT7200L-50 'ACT7201LA-50 'ACT7202LA-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, $\overline{R}$ or $\overline{W}$			40		28.5		22.2		15	MHz
$t_{c(R)}$	Cycle time, read	1(a)	25		35		45		65		ns
$t_{c(W)}$	Cycle time, write	1(b)	25		35		45		65		ns
$t_{c(RS)}$	Cycle time, reset	7	25		35		45		65		ns
$t_{c(RT)}$	Cycle time, retransmit	4	25		35		45		65		ns
$t_{w(RL)}$	Pulse duration, $\overline{R}$ low	1(a)	15		25		35		50		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	1(b)	15		25		35		50		ns
$t_{w(RH)}$	Pulse duration, $\overline{R}$ high	1(a)	10		10		10		15		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	1(b)	10		10		10		15		ns
$t_{w(RT)}$	Pulse duration, $\overline{FL}/\overline{RT}$ low	4	15		25		35		50		ns
$t_{w(RS)}$	Pulse duration, $\overline{RS}$ low	7	15		25		35		50		ns
$t_{w(XIL)}$	Pulse duration, $\overline{XI}$ low	10	15		25		35		50		ns
$t_{w(XIH)}$	Pulse duration, $\overline{XI}$ high	10	10		10		10		10		ns
$t_{su(D)}$	Setup time, data before $\overline{W}$↑	1(b), 6	11		15		18		30		ns
$t_{su(RT)}$	Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{FL}/\overline{RT}$↑‡	4	15		25		35		50		ns
$t_{su(RS)}$	Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{RS}$↑‡	7	15		25		35		50		ns
$t_{su(XI-R)}$	Setup time, $\overline{XI}$ low before $\overline{R}$↓	10	10		10		10		15		ns
$t_{su(XI-W)}$	Setup time, $\overline{XI}$ low before $\overline{W}$↓	10	10		10		10		15		ns
$t_{h(D)}$	Hold time, data after $\overline{W}$↑	1(b), 6	0		0		0		5		ns
$t_{h(E-R)}$	Hold time, $\overline{R}$ low after $\overline{EF}$↑	5, 11	15		25		35		50		ns
$t_{h(F-W)}$	Hold time, $\overline{W}$ low after $\overline{FF}$↑	6, 12	15		25		35		50		ns
$t_{h(RT)}$	Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{FL}/\overline{RT}$↑	4	10		10		10		15		ns
$t_{h(RS)}$	Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{RS}$↑	7	10		10		10		15		ns

† Released in RJ package only

‡ These values are characterized but not currently tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 13)

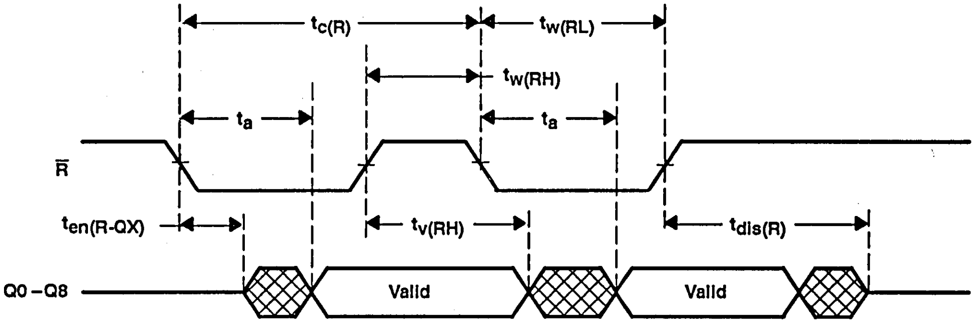
PARAMETER		FIGURE	'ACT7200L-15 'ACT7201LA-15 'ACT7202LA-15		'ACT7200L-25 'ACT7201LA-25 'ACT7202LA-25		'ACT7201LA-35[†] 'ACT7202LA-35[†]		'ACT7200L-50 'ACT7201LA-50 'ACT7202LA-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock frequency, $\overline{\mathrm{R}}$ or $\overline{\mathrm{W}}$		40		28.5		22.2		15		MHz
t_{a}	Access time, $\overline{\mathrm{R}}$↓ or $\overline{\mathrm{EF}}$↑ to data out valid	1(a), 3, 5		15		25		35		50	ns
$t_{v(RH)}$	Valid time, data out valid after $\overline{\mathrm{R}}$↑	1(a)	5		5		5		5		ns
$t_{en(R\text{-}QX)}$	Enable time, $\overline{\mathrm{R}}$↓ to Q outputs at low impedance[‡]	1(a)	5		5		10		10		ns
$t_{en(W\text{-}QX)}$	Enable time, $\overline{\mathrm{W}}$↑ to Q outputs at low impedance[‡§]	5	5		5		5		15		ns
$t_{dis(R)}$	Disable time, $\overline{\mathrm{R}}$↑ to Q outputs at high impedance[‡]	1(a)		15		18		20		30	ns
$t_{w(FH)}$	Pulse duration, $\overline{\mathrm{FF}}$ high in automatic write mode	6		15		25		30		45	ns
$t_{w(EH)}$	Pulse duration, $\overline{\mathrm{EF}}$ high in automatic read mode	5		15		25		30		45	ns
$t_{pd(W\text{-}F)}$	Propagation delay time, $\overline{\mathrm{W}}$↓ to $\overline{\mathrm{FF}}$ low	2		15		25		30		45	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{\mathrm{R}}$↑ to $\overline{\mathrm{FF}}$ high	2, 6, 12		15		25		30		45	ns
$t_{pd(RS\text{-}F)}$	Propagation delay time, $\overline{\mathrm{RS}}$↓ to $\overline{\mathrm{FF}}$ high	7		25		35		45		65	ns
$t_{pd(RS\text{-}HF)}$	Propagation delay time, $\overline{\mathrm{RS}}$↓ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ high	7		25		35		45		65	ns
$t_{pd(W\text{-}E)}$	Propagation delay time, $\overline{\mathrm{W}}$↑ to $\overline{\mathrm{EF}}$ high	3, 5, 11		15		25		30		45	ns
$t_{pd(R\text{-}E)}$	Propagation delay time, $\overline{\mathrm{R}}$↓ to $\overline{\mathrm{EF}}$ low	3		15		25		30		45	ns
$t_{pd(RS\text{-}E)}$	Propagation delay time, $\overline{\mathrm{RS}}$↓ to $\overline{\mathrm{EF}}$ low	7		25		35		45		65	ns
$t_{pd(W\text{-}HF)}$	Propagation delay time, $\overline{\mathrm{W}}$↓ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ low	8		25		35		45		65	ns
$t_{pd(R\text{-}HF)}$	Propagation delay time, $\overline{\mathrm{R}}$↑ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ high	8		25		35		45		65	ns
$t_{pd(R\text{-}XOL)}$	Propagation delay time, $\overline{\mathrm{R}}$↓ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ low	9		15		25		35		50	ns
$t_{pd(W\text{-}XOL)}$	Propagation delay time, $\overline{\mathrm{W}}$↓ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ low	9		15		25		35		50	ns
$t_{pd(R\text{-}XOH)}$	Propagation delay time, $\overline{\mathrm{R}}$↑ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ high	9		15		25		35		50	ns
$t_{pd(W\text{-}XOH)}$	Propagation delay time, $\overline{\mathrm{W}}$↑ to $\overline{\mathrm{XO}}$/$\overline{\mathrm{HF}}$ high	9		15		25		35		50	ns
$t_{pd(RT\text{-}FL)}$	Propagation delay time, $\overline{\mathrm{FL}/\mathrm{RT}}$↓ to $\overline{\mathrm{HF}}$, $\overline{\mathrm{EF}}$, $\overline{\mathrm{FF}}$ valid	4		25		35		45		65	ns

[†] Released in RJ package only

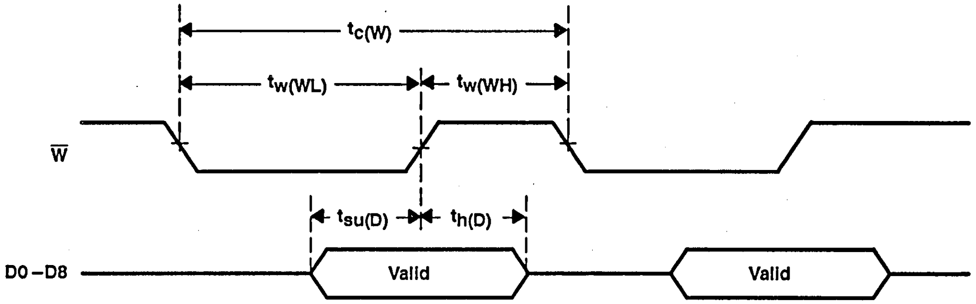
[‡] These values are characterized but not currently tested.

[§] Only applies when data is automatically read (see Figure 5)

PARAMETER MEASUREMENT INFORMATION



(a) READ



(b) WRITE

Figure 1. Asynchronous Waveforms

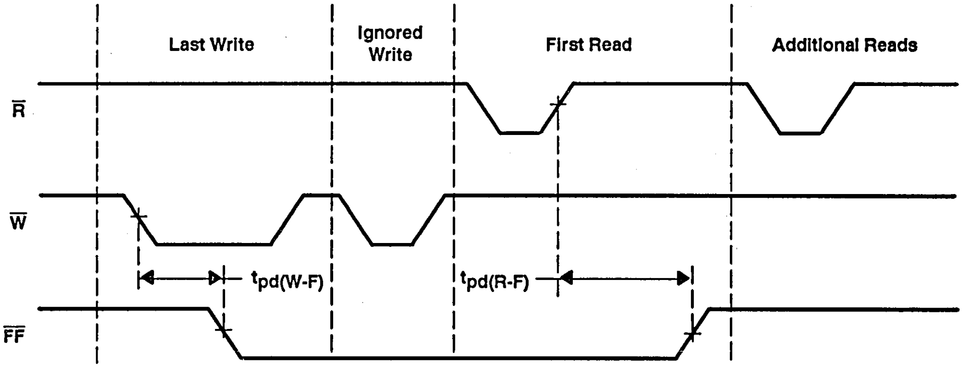


Figure 2. Full-Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

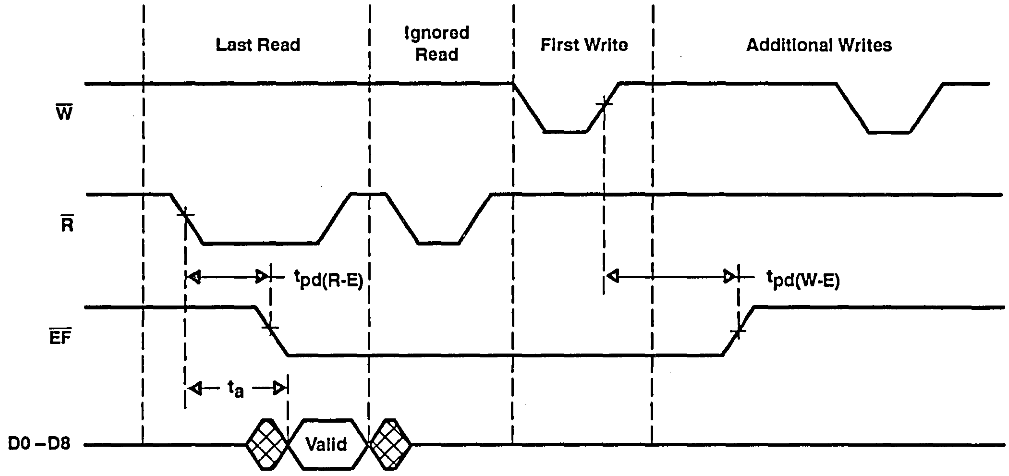
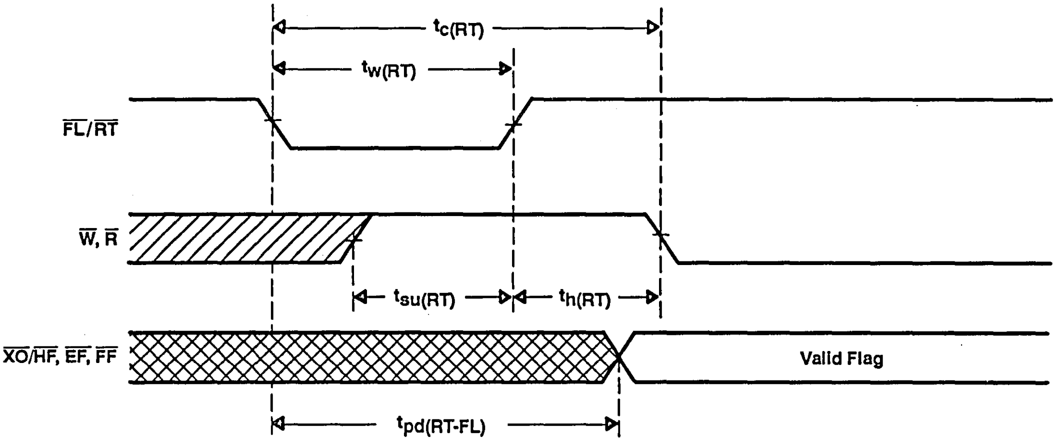


Figure 3. Empty-Flag Waveforms



NOTE A: The $\overline{EF}$, $\overline{FF}$, and $\overline{XO}/\overline{HF}$ status flags is valid after completion of the retransmit cycle.

Figure 4. Retransmit Waveforms

PARAMETER MEASUREMENT INFORMATION

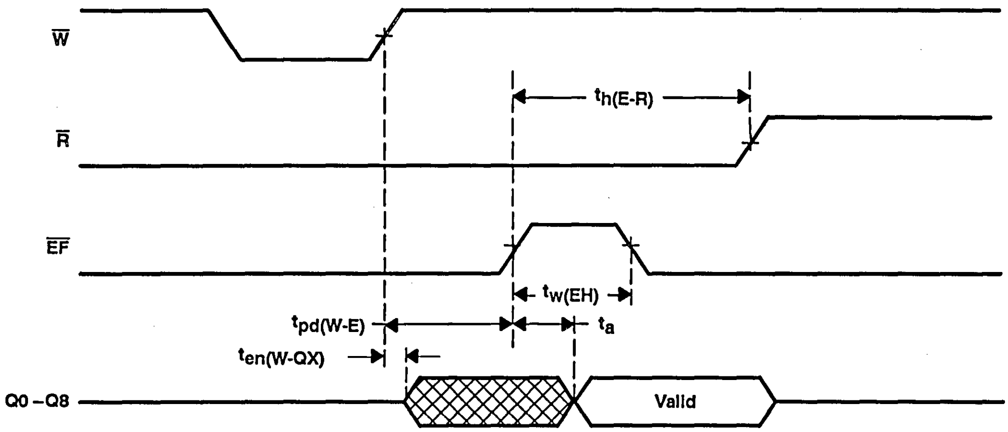


Figure 5. Automatic-Read Waveforms

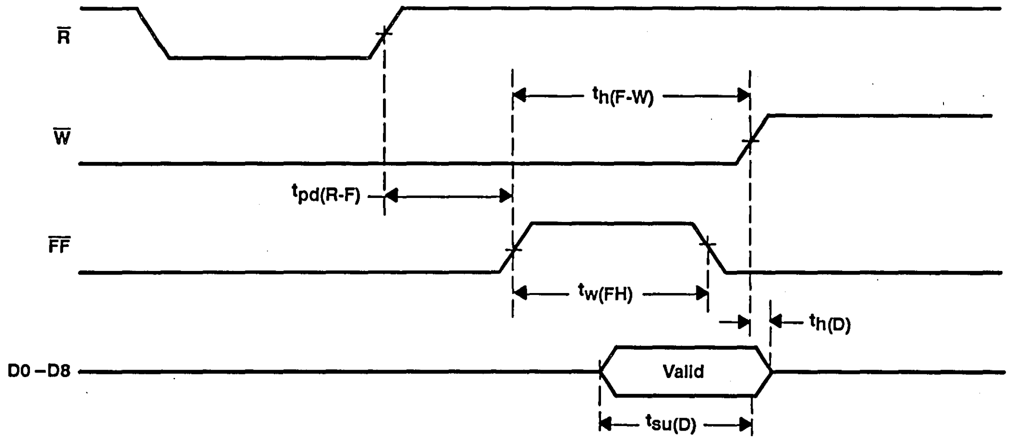


Figure 6. Automatic-Write Waveforms

PARAMETER MEASUREMENT INFORMATION

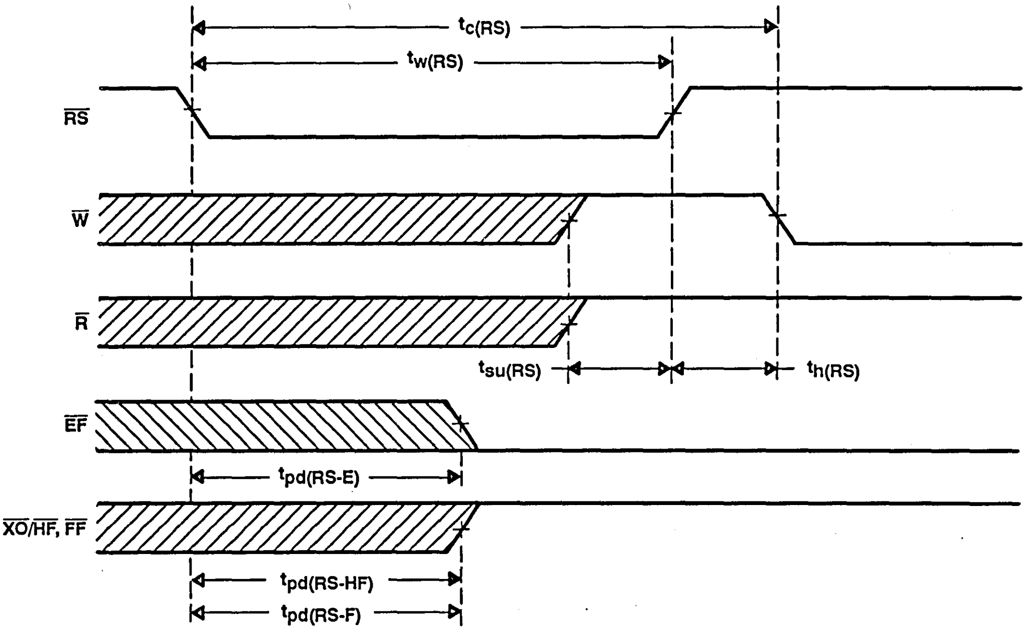


Figure 7. Master Reset Waveforms

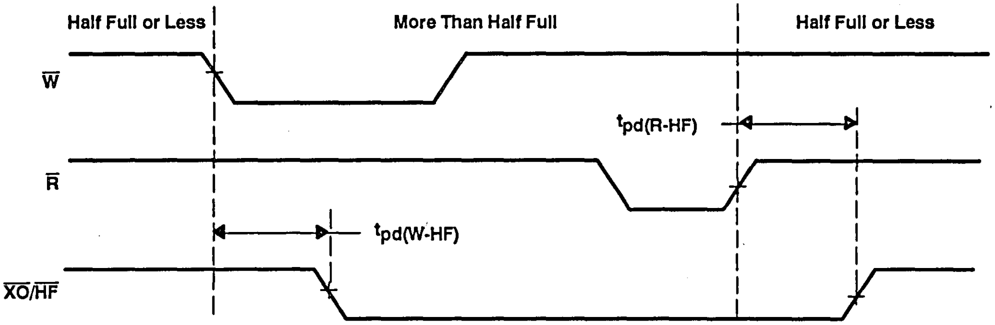


Figure 8. Half-Full Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

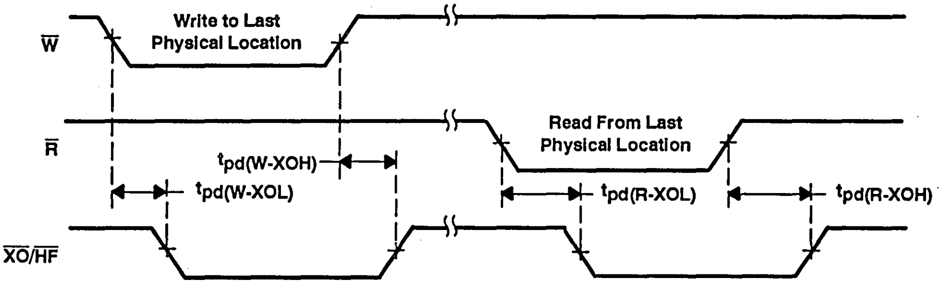


Figure 9. Expansion-Out Waveforms

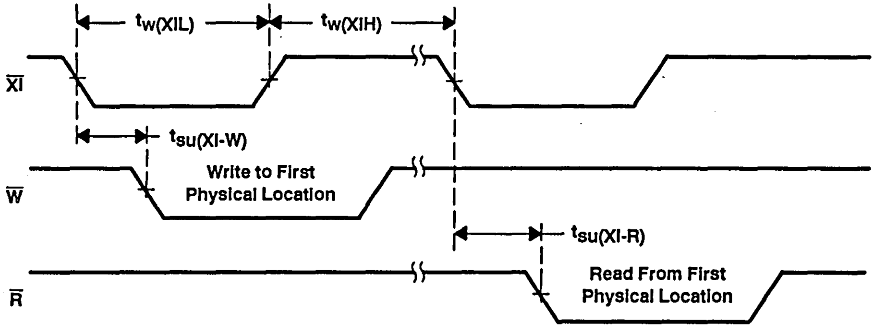


Figure 10. Expansion-In Waveforms

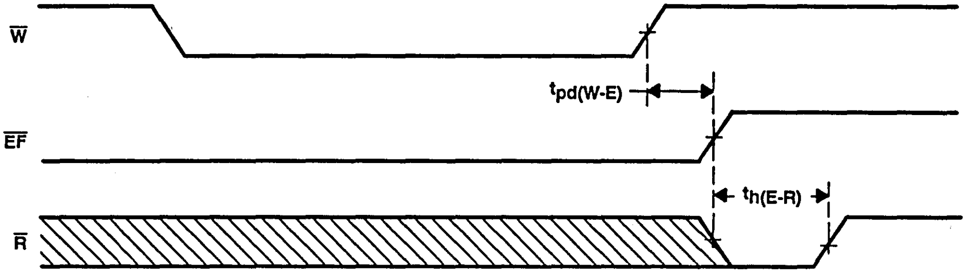


Figure 11. Minimum Timing for an Empty Flag-Coincident Read Pulse

PARAMETER MEASUREMENT INFORMATION

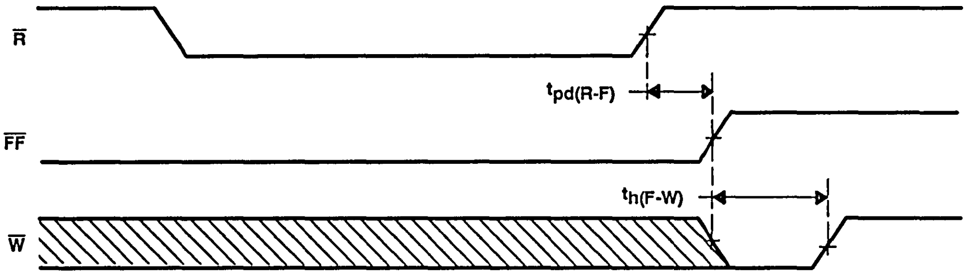
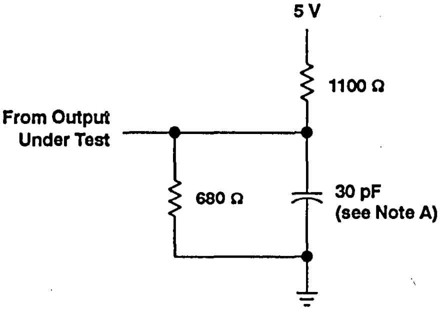
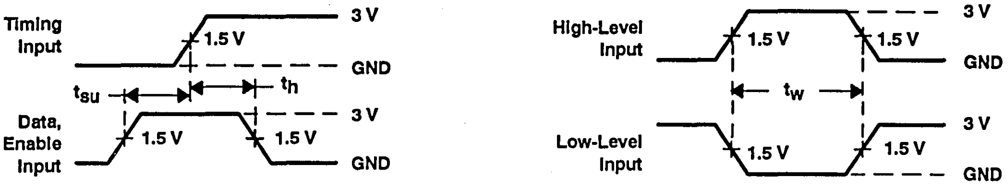


Figure 12. Minimum Timing for a Full Flag-Coincident Write Pulse

PARAMETER MEASUREMENT INFORMATION

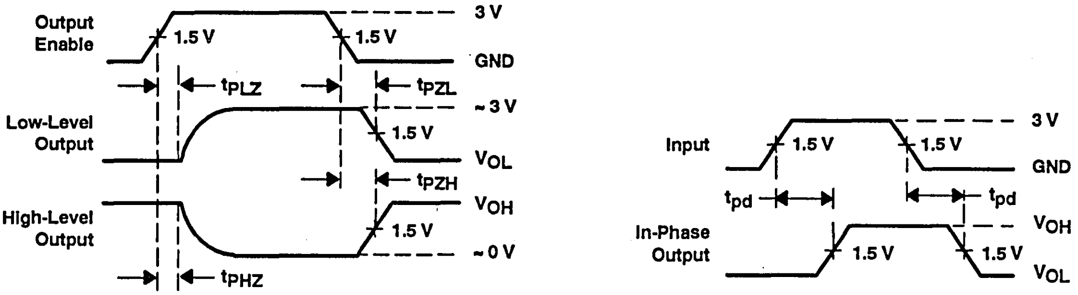


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 13. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 256, 512, or 1024 words of storage. Width expansion and depth expansion can be used together.

width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be monitored from any one device. Figure 14 shows two FIFOs in a width-expansion configuration. Both devices have their expansion-in ($\overline{XI}$) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first-load/retransmit ($\overline{FL}/\overline{RT}$) input to function as a retransmit ($\overline{RT}$) input and the expansion-out/half-full ($\overline{XO}/\overline{HF}$) output to function as a half-full ($\overline{HF}$) flag.

depth expansion

The SN74ACT7200L/7201LA/7202LA is easily expanded in depth. Figure 15 shows the connections used to depth expand three SN74ACT7200L/7201LA/7202LA devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7200L/7201LA/7202LA operates in depth expansion under the following conditions:

1. The first device in the chain is designated by tying $\overline{FL}$ to ground.
2. All other devices must have their $\overline{FL}$ inputs at a high logic level.
3. $\overline{XO}$ of each device must be tied to $\overline{XI}$ of the next device.
4. External logic is needed to generate a composite $\overline{FF}$ and $\overline{EF}$ (all $\overline{FF}$ outputs must be ORed together, and all $\overline{EF}$ outputs must be ORed together).
5. $\overline{RT}$ and $\overline{HF}$ functions are not available in the depth-expanded configuration.

combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by first creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 16).

APPLICATION INFORMATION

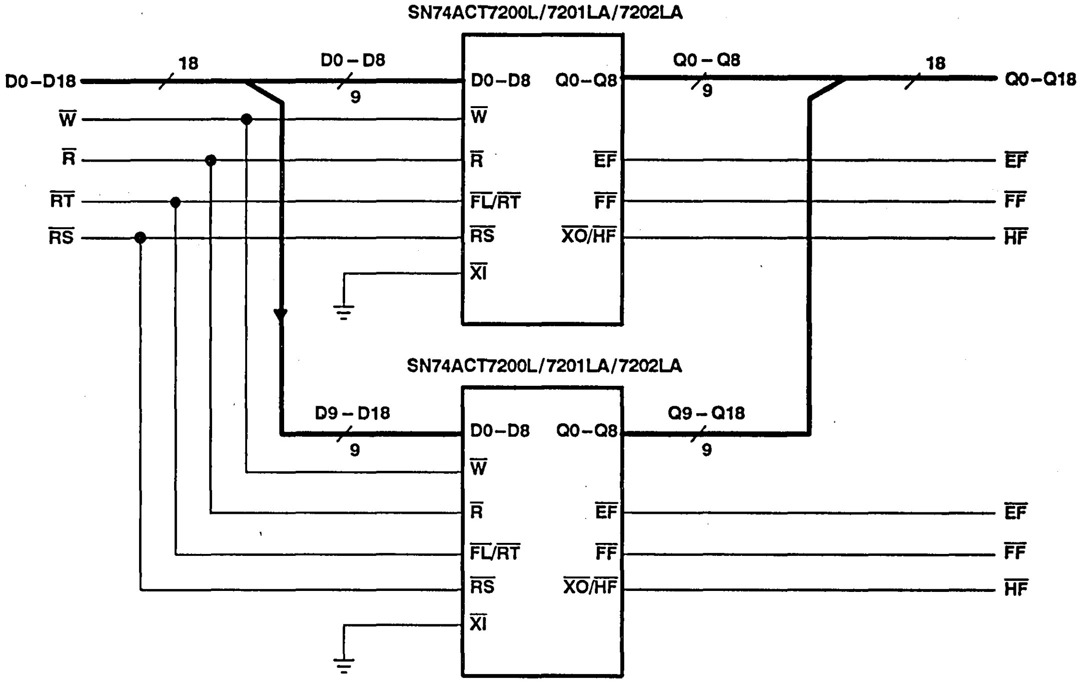


Figure 14. Word-Width Expansion: 256/512/1024 Words × 18 Bits

APPLICATION INFORMATION

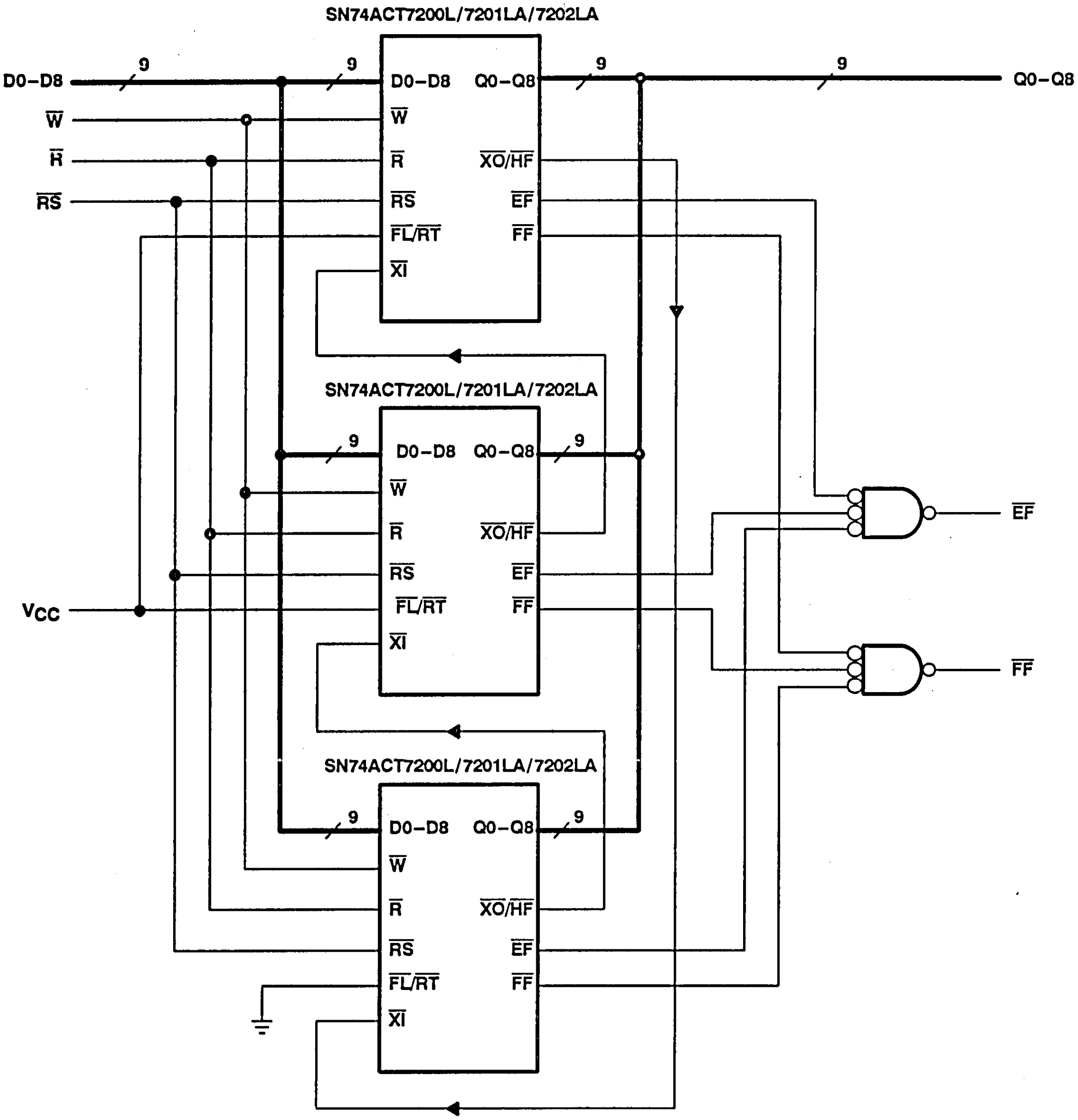


Figure 15. Word-Depth Expansion: 768/1536/3072 Words × 9 Bits

APPLICATION INFORMATION

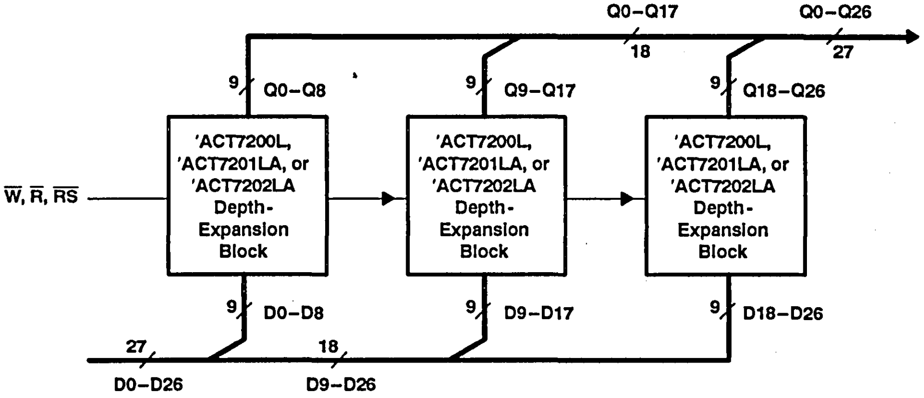


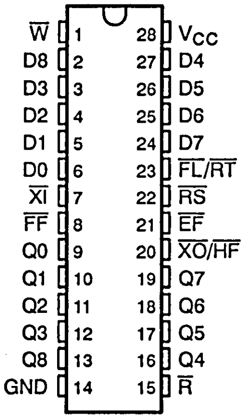
Figure 16. Word-Depth Plus Word-Width Expansion

SN74ACT7203L, SN74ACT7204L
2048 × 9 AND 4096 × 9
FIRST-IN, FIRST-OUT MEMORIES

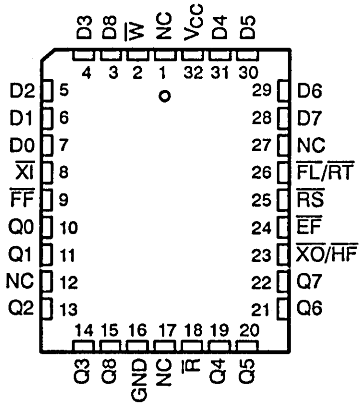
SCAS226 – FEBRUARY 1993 – REVISED JUNE 1993

- **Reads and Writes Can Be Asynchronous or Coincident**
- **Organization:**
  - **SN74ACT7203L – 2048 × 9**
  - **SN74ACT7204L – 4096 × 9**
- **Fast Data Access Times of 15 ns**
- **Read and Write Frequencies up to 40 MHz**
- **Bit-Width and Word-Depth Expansion**
- **Fully Compatible With the IDT7203/7204**
- **Retransmit Capability**
- **Empty, Full, and Half-Full Flags**
- **TTL-Compatible Inputs**
- **Available in 28-Terminal Plastic DIP (NP) and Small-Outline (DV) Packages and 32-Terminal Plastic J-Leaded Chip-Carrier (RJ) Packages**

NP PACKAGE
(TOP VIEW)



RJ PACKAGE
(TOP VIEW)



NC – No internal connection

description

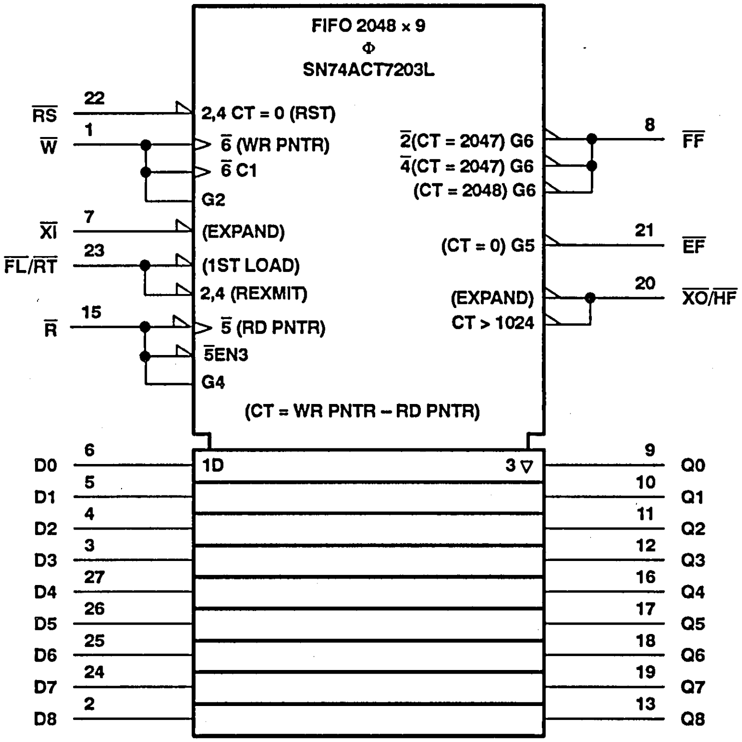
The SN74ACT7203L and SN74ACT7204L are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and can be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth-expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

Data is loaded into memory by the write-enable ($\overline{W}$) input and unloaded by the read-enable ($\overline{R}$) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

The SN74ACT7203L and SN74ACT7204L are characterized for operation from 0°C to 70°C.

SN74ACT7203L logic symbol†



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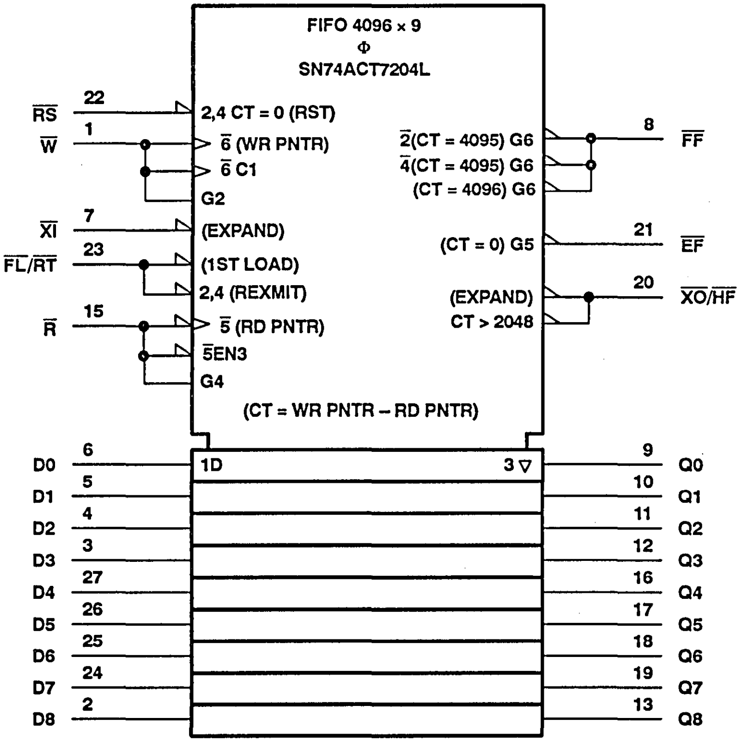
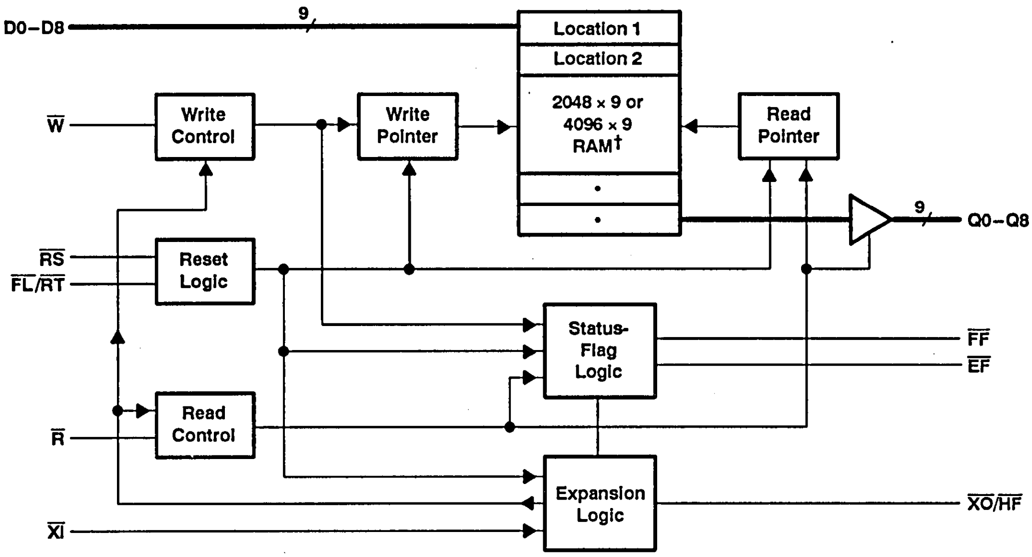
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the NP package.

SN74ACT7204L logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the NP package.

functional block diagram



† 2048 × 9 for SN74ACT7203L; 4096 × 9 for SN74ACT7204L

RESET AND RETRANSMIT FUNCTION TABLE
(single-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
$\overline{\text{RS}}$	$\overline{\text{FL}}/\overline{\text{RT}}$	$\overline{\text{XI}}$	READ POINTER	WRITE POINTER	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{XO}}/\overline{\text{HF}}$	
L	X	L	Location zero	Location zero	L	H	H	Reset device
H	L	L	Location zero	Unchanged	X	X	X	Retransmit
H	H	L	Increment if $\overline{\text{EF}}$ high	Increment if $\overline{\text{FF}}$ high	X	X	X	Read/write

RESET AND FIRST-LOAD FUNCTION TABLE
(multiple-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
$\overline{\text{RS}}$	$\overline{\text{FL}}/\overline{\text{RT}}$	$\overline{\text{XI}}$	READ POINTER	WRITE POINTER	$\overline{\text{EF}}$	$\overline{\text{FF}}$	
L	L	‡	Location zero	Location zero	L	H	Reset first device
L	H	‡	Location zero	Location zero	L	H	Reset all other devices
H	X	‡	X	X	X	X	Read/write

‡ $\overline{\text{XI}}$ is connected to $\overline{\text{XO}}/\overline{\text{HF}}$ of the previous device in the daisy chain (see Figure 15).

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
D0–D8	I	Data inputs
$\overline{\mathrm{EF}}$	O	Empty-flag output. $\overline{\mathrm{EF}}$ is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at Q0–Q8 by holding $\overline{\mathrm{R}}$ low when loading the data word with a low-level pulse on $\overline{\mathrm{W}}$.
$\overline{\mathrm{FF}}$	O	Full-flag output. $\overline{\mathrm{FF}}$ is low when the write pointer is one location less than the read pointer, indicating that the device is full and inhibiting any operation initiated by a write cycle. $\overline{\mathrm{FF}}$ goes low when the number of writes after reset exceeds the number of reads by 2048 for the SN74ACT7203L and 4096 for the SN74ACT7204L. When the FIFO is full, a data word can be written automatically into memory by holding $\overline{\mathrm{W}}$ low while reading out another data word with a low-level pulse on $\overline{\mathrm{R}}$.
$\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$	I	First-load/retransmit input. $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth expansion chain. A device is not used in depth expansion when its expansion-in ($\overline{\mathrm{XI}}$) input is tied to ground. In that case, $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ acts as a retransmit enable. A retransmit operation is initiated when $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. $\overline{\mathrm{R}}$) and $\overline{\mathrm{W}}$ must be at a high logic level during the low-level $\overline{\mathrm{FL}}/\overline{\mathrm{RT}}$ retransmit pulse. Retransmit should be used only when less than 2048/4096 writes are performed between resets; otherwise, an attempt to retransmit can cause the loss of unread data. The retransmit function can affect $\overline{\mathrm{XO}}$/HF depending on the relative locations of the read and write pointers.
GND		Ground
Q0–Q8	O	Data outputs. Q0–Q8 are in the high-impedance state when $\overline{\mathrm{R}}$ is high or the FIFO is empty.
$\overline{\mathrm{R}}$	I	Read-enable input. A read cycle begins on the falling edge of $\overline{\mathrm{R}}$ if $\overline{\mathrm{EF}}$ is high. This activates Q0–Q8 and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{\mathrm{R}}$ goes high. As the last stored word is read by the falling edge of $\overline{\mathrm{R}}$, $\overline{\mathrm{EF}}$ transitions low but Q0–Q8 remain active until $\overline{\mathrm{R}}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{\mathrm{R}}$.
$\overline{\mathrm{RS}}$	I	Reset input. A reset is performed by taking $\overline{\mathrm{RS}}$ low. This initializes the internal read and write pointers to the first location and sets $\overline{\mathrm{EF}}$ low, $\overline{\mathrm{FF}}$ high, and $\overline{\mathrm{HF}}$ high. Both $\overline{\mathrm{R}}$ and $\overline{\mathrm{W}}$ must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place.
V_{CC}		Supply voltage
$\overline{\mathrm{W}}$	I	Write-enable input. A write cycle begins on the falling edge of $\overline{\mathrm{W}}$ if $\overline{\mathrm{FF}}$ is high. The value on D0–D8 is stored in memory as $\overline{\mathrm{W}}$ returns high. When the FIFO is full, $\overline{\mathrm{FF}}$ is low inhibiting $\overline{\mathrm{W}}$ from performing any operation on the device.
$\overline{\mathrm{XI}}$	I	Expansion-in input. $\overline{\mathrm{XI}}$ performs two functions. $\overline{\mathrm{XI}}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, $\overline{\mathrm{XI}}$ is connected to the expansion-out ($\overline{\mathrm{XO}}$) output of the previous device in the depth-expansion chain.
$\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$	O	Expansion-out/half-full-flag output. $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ performs two functions. When the device is not used in depth expansion (i.e., when $\overline{\mathrm{XI}}$ is tied to ground), $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on $\overline{\mathrm{W}}$ for the next write operation drives $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ low. $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ remains low until a rising edge of $\overline{\mathrm{R}}$ reduces the number of words stored to exactly half of the total memory. When the device is used in depth expansion, $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ is connected to $\overline{\mathrm{XI}}$ of the next device in the daisy chain. $\overline{\mathrm{XO}}/\overline{\mathrm{HF}}$ drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Input voltage range (any input), V_I	−0.5 V to 7 V
Continuous output current, I_O	50 mA
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−55°C to 125°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{XI}$	2.6			V
		Other inputs	2			
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 2 mA		2.4		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	V
I_{OZH}	$V_O = V_{CC}$,	$\overline{R} \ge V_{IH}$			±10	µA
I_{OZL}	V_O = 0.4 V,	$\overline{R} \ge V_{IH}$			±10	µA
I_I	V_I = 0 to 5.5 V			−1	1	µA
I_{CC1}[‡]	f_{clock} = 20 MHz				120	mA
I_{CC2}[‡]	$\overline{R}$, $\overline{W}$, $\overline{RS}$, and $\overline{FL}/\overline{RT}$ at V_{IH}				12	mA
I_{CC3}[‡]	$V_I = V_{CC} - 0.2$ V				2	mA
C_i[§]	V_I = 0,	T_A = 25°C,	f = 1 MHz		10	pF
C_o[§]	V_O = 0,	T_A = 25°C,	f = 1 MHz		10	pF

[‡] I_{CC1} = supply current; I_{CC2} = standby current; I_{CC3} = power-down current. I_{CC} measurements are made with outputs open (only capacitive loading).

[§] This parameter is sampled and not 100% tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		FIGURE	'ACT7203L-15 'ACT7204L-15		'ACT7203L-25 'ACT7204L-25		'ACT7203L-50 'ACT7204L-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, $\overline{R}$ or $\overline{W}$			40		28.5		15	MHz
$t_{c(R)}$	Cycle time, read	1(a)	25		35		65		ns
$t_{c(W)}$	Cycle time, write	1(b)	25		35		65		ns
$t_{c(RS)}$	Cycle time, reset	7	25		35		65		ns
$t_{c(RT)}$	Cycle time, retransmit	4	25		35		65		ns
$t_{w(RL)}$	Pulse duration, $\overline{R}$ low	1(a)	15		25		50		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	1(b)	15		25		50		ns
$t_{w(RH)}$	Pulse duration, $\overline{R}$ high	1(a)	10		10		15		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	1(b)	10		10		15		ns
$t_{w(RT)}$	Pulse duration, $\overline{FL}/\overline{RT}$ low	4	15		25		50		ns
$t_{w(RS)}$	Pulse duration, $\overline{RS}$ low	7	15		25		50		ns
$t_{w(XIL)}$	Pulse duration, $\overline{XI}$ low	10	15		25		50		ns
$t_{w(XIH)}$	Pulse duration, $\overline{XI}$ high	10	10		10		10		ns
$t_{su(D)}$	Setup time, data before $\overline{W}$↑	1(b), 6	11		15		30		ns
$t_{su(RT)}$	Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{FL}/\overline{RT}$↑†	4	15		25		50		ns
$t_{su(RS)}$	Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{RS}$↑†	7	15		25		50		ns
$t_{su(XI-R)}$	Setup time, $\overline{XI}$ low before $\overline{R}$↓	10	10		10		15		ns
$t_{su(XI-W)}$	Setup time, $\overline{XI}$ low before $\overline{W}$↓	10	10		10		15		ns
$t_{h(D)}$	Hold time, data after $\overline{W}$↑	1(b), 6	0		0		5		ns
$t_{h(E-R)}$	Hold time, $\overline{R}$ low after $\overline{EF}$↑	5, 11	15		25		50		ns
$t_{h(F-W)}$	Hold time, $\overline{W}$ low after $\overline{FF}$↑	6, 12	15		25		50		ns
$t_{h(RT)}$	Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{FL}/\overline{RT}$↑	4	10		10		15		ns
$t_{h(RS)}$	Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{RS}$↑	7	10		10		15		ns

† These values are characterized but not currently tested.

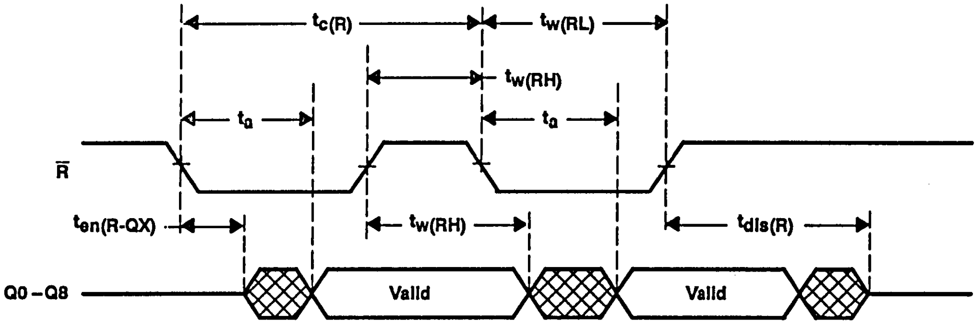
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 13)

PARAMETER		FIGURE	'ACT7203L-15 'ACT7204L-15		'ACT7203L-25 'ACT7204L-25		'ACT7203L-50 'ACT7204L-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock frequency, $\overline{R}$ or $\overline{W}$		40		28.5		15		MHz
t_a	Access time, $\overline{R}$↓ or $\overline{EF}$↑ to data out valid	1(a), 3, 5		15		25		50	ns
$t_{v(RH)}$	Valid time, data out valid after $\overline{R}$↑	1(a)	5		5		5		ns
$t_{en(R-QX)}$	Enable time, $\overline{R}$↓ to Q outputs at low impedance†	1(a)	5		5		10		ns
$t_{en(W-QX)}$	Enable time, $\overline{W}$↑ to Q outputs at low impedance†‡	5	5		5		15		ns
$t_{dis(R)}$	Disable time, $\overline{R}$↑ to Q outputs at high impedance†	1(a)		15		18		30	ns
$t_{w(FH)}$	Pulse duration, $\overline{FF}$ high in automatic-write mode	6		15		25		45	ns
$t_{w(EH)}$	Pulse duration, $\overline{EF}$ high in automatic-read mode	5		15		25		45	ns
$t_{pd(W-F)}$	Propagation delay time, $\overline{W}$↓ to $\overline{FF}$ low	2		15		25		45	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{R}$↑ to $\overline{FF}$ high	2, 6, 12		15		25		45	ns
$t_{pd(RS-F)}$	Propagation delay time, $\overline{RS}$↓ to $\overline{FF}$ high	7		25		35		65	ns
$t_{pd(RS-HF)}$	Propagation delay time, $\overline{RS}$↓ to $\overline{XO}/\overline{HF}$ high	7		25		35		65	ns
$t_{pd(W-E)}$	Propagation delay time, $\overline{W}$↑ to $\overline{EF}$ high	3, 5, 11		15		25		45	ns
$t_{pd(R-E)}$	Propagation delay time, $\overline{R}$↓ to $\overline{EF}$ low	3		15		25		45	ns
$t_{pd(RS-E)}$	Propagation delay time, $\overline{RS}$↓ to $\overline{EF}$ low	7		25		35		65	ns
$t_{pd(W-HF)}$	Propagation delay time, $\overline{W}$↓ to $\overline{XO}/\overline{HF}$ low	8		25		35		65	ns
$t_{pd(R-HF)}$	Propagation delay time, $\overline{R}$↑ to $\overline{XO}/\overline{HF}$ high	8		25		35		65	ns
$t_{pd(R-XOL)}$	Propagation delay time, $\overline{R}$↓ to $\overline{XO}/\overline{HF}$ low	9		15		25		50	ns
$t_{pd(W-XOL)}$	Propagation delay time, $\overline{W}$↓ to $\overline{XO}/\overline{HF}$ low	9		15		25		50	ns
$t_{pd(R-XOH)}$	Propagation delay time, $\overline{R}$↑ to $\overline{XO}/\overline{HF}$ high	9		15		25		50	ns
$t_{pd(W-XOH)}$	Propagation delay time, $\overline{W}$↑ to $\overline{XO}/\overline{HF}$ high	9		15		25		50	ns
$t_{pd(RT-FL)}$	Propagation delay time, $\overline{FL}/\overline{RT}$↓ to $\overline{HF}$, $\overline{EF}$, $\overline{FF}$ valid	4		25		35		65	ns

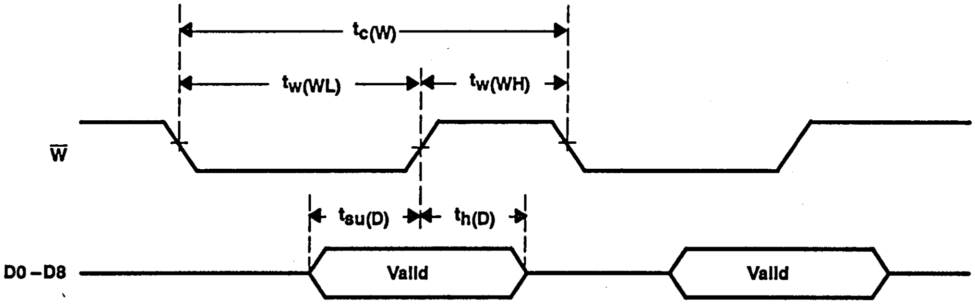
† These values are characterized but not currently tested.

‡ Only applies when data is automatically read (see Figure 5).

PARAMETER MEASUREMENT INFORMATION



(a) READ



(b) WRITE

Figure 1. Asynchronous Waveforms

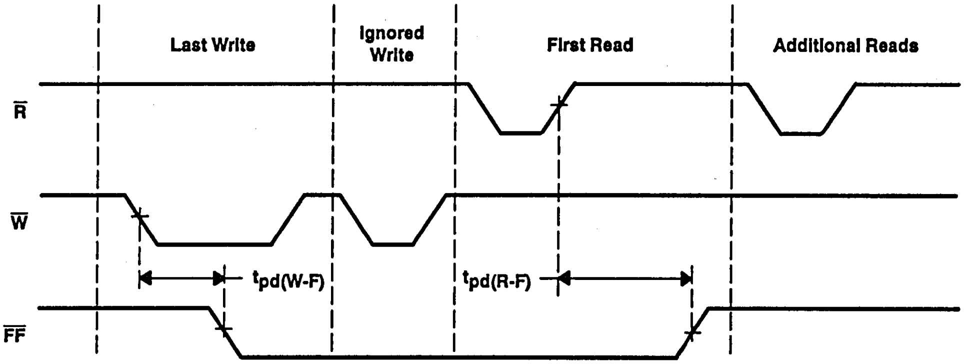


Figure 2. Full-Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

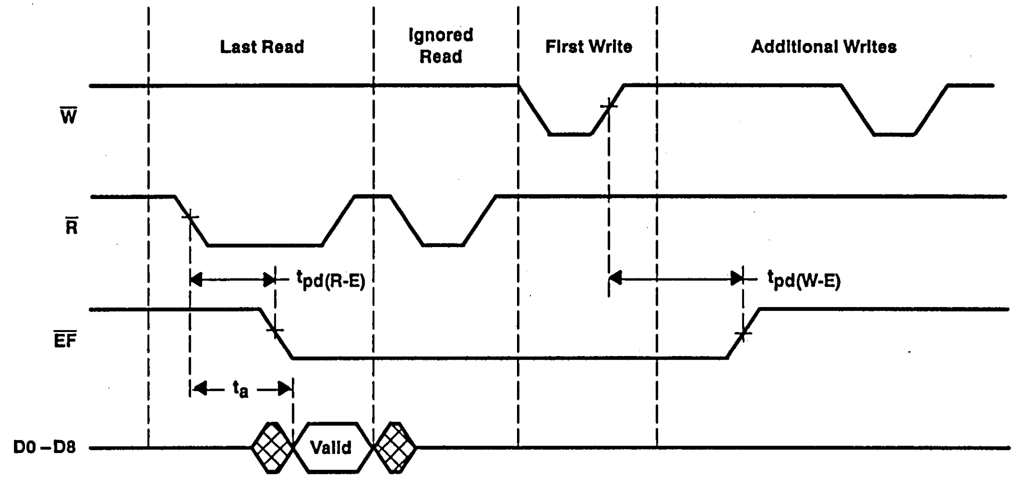
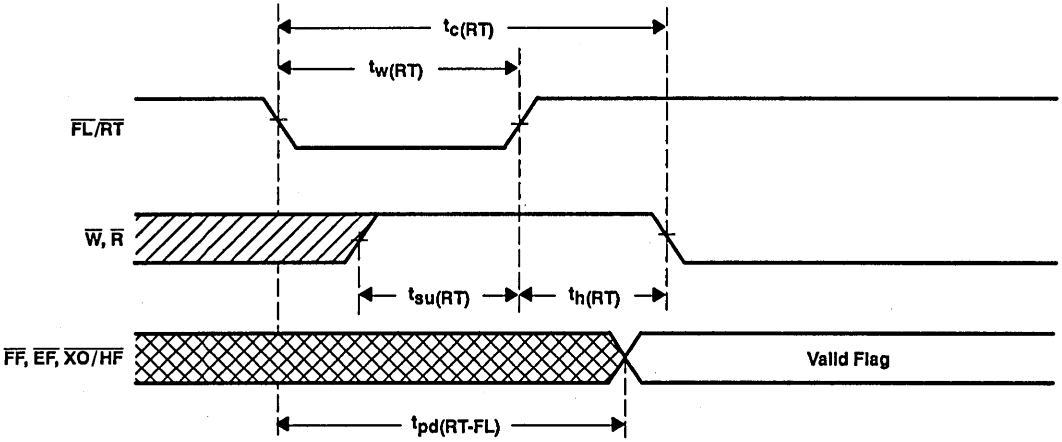


Figure 3. Empty-Flag Waveforms



NOTE A: The EF̄, FF̄, and XO̅/HF̄ status flags is valid after completion of the retransmit cycle.

Figure 4. Retransmit Waveforms

PARAMETER MEASUREMENT INFORMATION

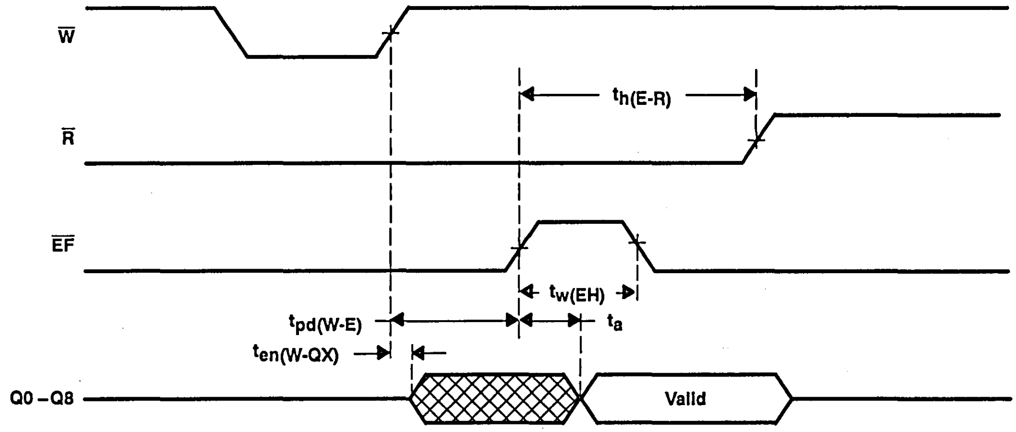


Figure 5. Automatic-Read Waveforms

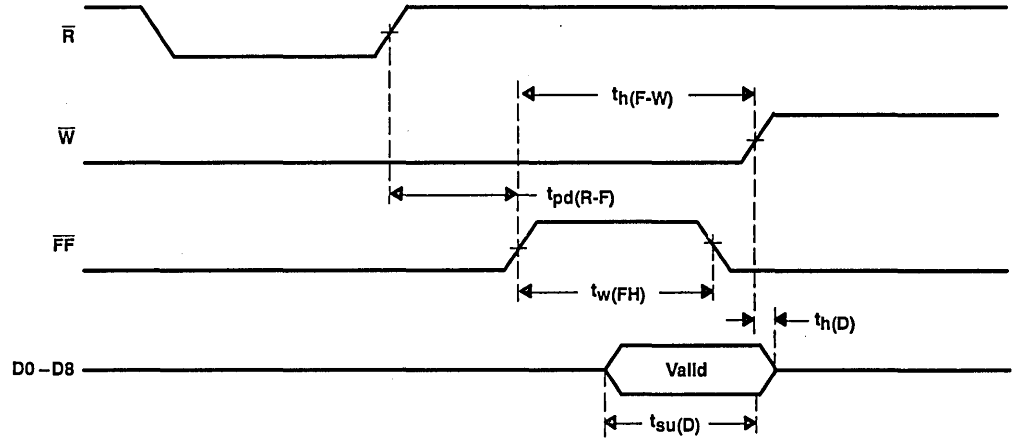


Figure 6. Automatic-Write Waveforms

PARAMETER MEASUREMENT INFORMATION

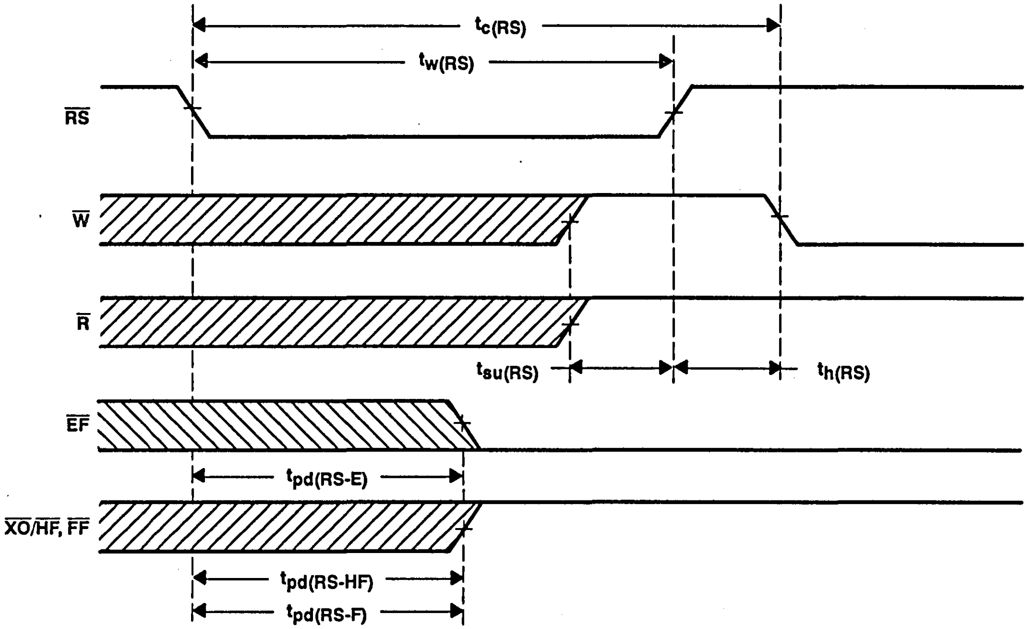


Figure 7. Master-Reset Waveforms

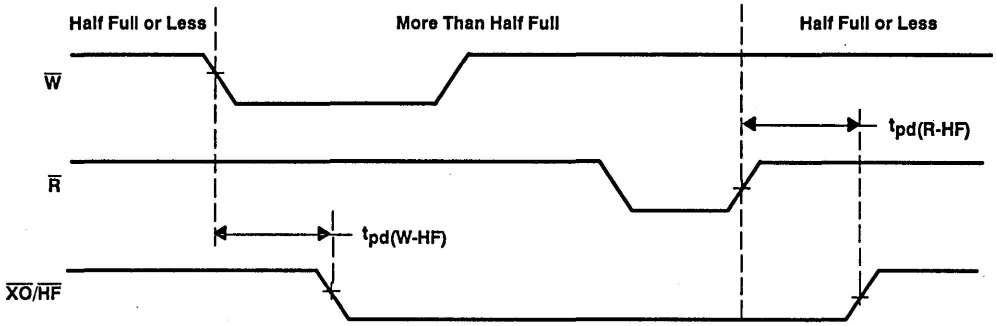


Figure 8. Half-Full Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

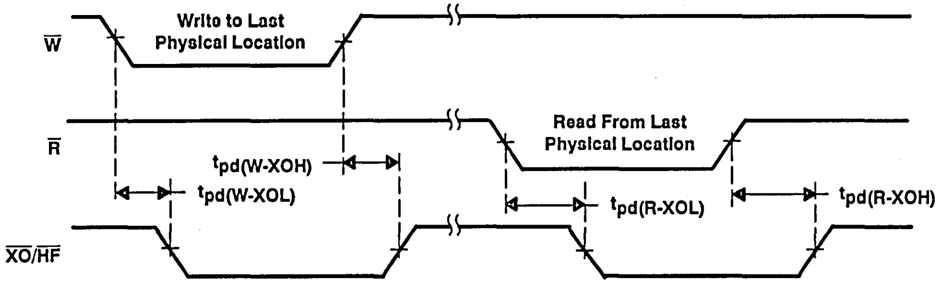


Figure 9. Expansion-Out Waveforms

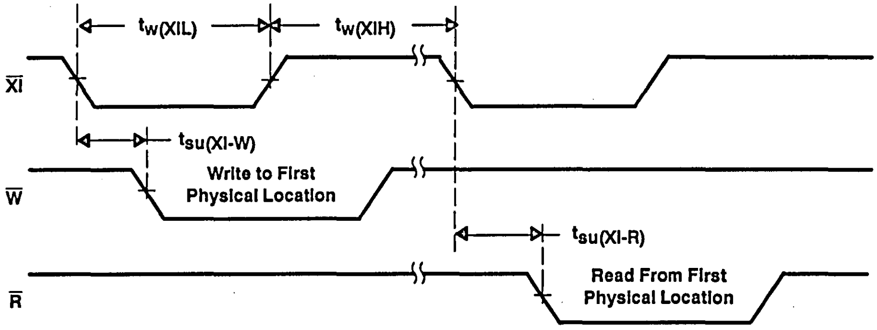


Figure 10. Expansion-In Waveforms

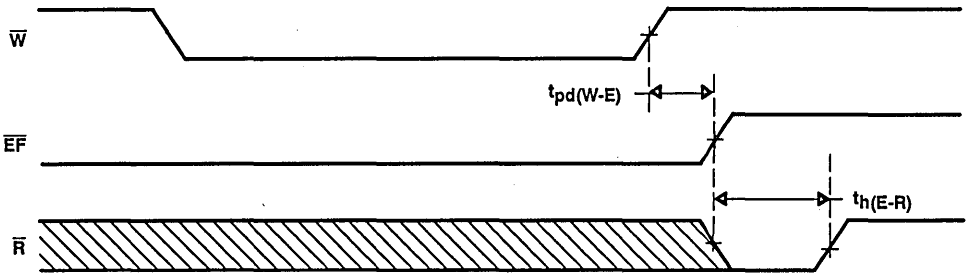


Figure 11. Minimum Timing for an Empty Flag-Coincident Read Pulse

PARAMETER MEASUREMENT INFORMATION

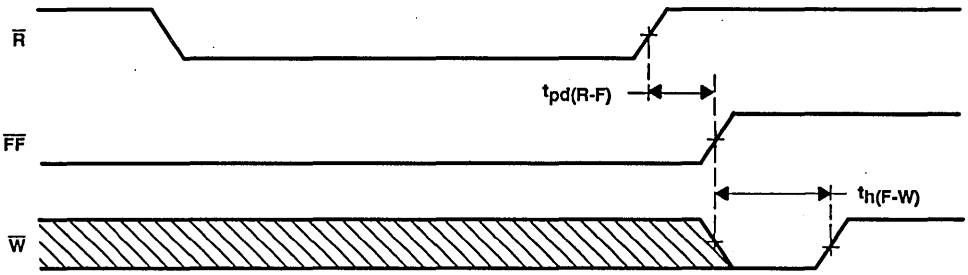
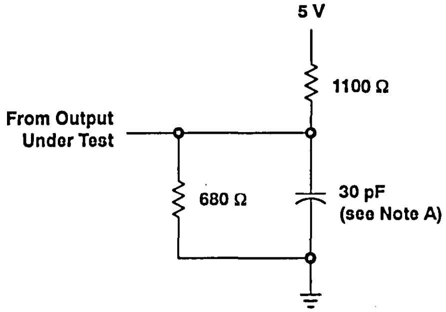
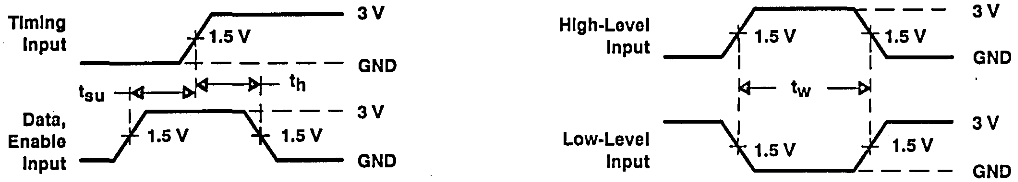


Figure 12. Minimum Timing for a Full Flag-Coincident Write Pulse

PARAMETER MEASUREMENT INFORMATION

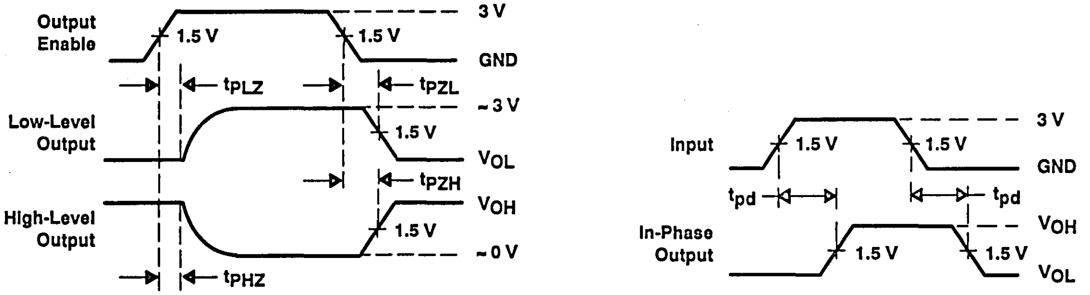


LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 13. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 2048 or 4096 words of storage. Width expansion and depth expansion can be used together.

width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ($\overline{\text{EF}}$, $\overline{\text{FF}}$, and $\overline{\text{HF}}$) can be monitored from any one device. Figure 14 shows two FIFOs in a width-expansion configuration. Both devices have their expansion-in ($\overline{\text{XI}}$) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first-load/retransmit ($\overline{\text{FL}}/\overline{\text{RT}}$) input to function as a retransmit ($\overline{\text{RT}}$) input and the expansion-out/half-full ($\overline{\text{XO}}/\overline{\text{HF}}$) output to function as a half-full ($\overline{\text{HF}}$) flag.

depth expansion

The SN74ACT7203L/7204L is easily expanded in depth. Figure 15 shows the connections used to depth expand three SN74ACT7203L/7204L devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7203L/7204L operates in depth expansion under the following conditions:

1. The first device in the chain is designated by connecting $\overline{\text{FL}}$ to ground.
2. All other devices have their $\overline{\text{FL}}$ inputs at a high logic level.
3. $\overline{\text{XO}}$ of each device must be connected to $\overline{\text{XI}}$ of the next device.
4. External logic is needed to generate a composite $\overline{\text{FF}}$ and $\overline{\text{EF}}$. All $\overline{\text{FF}}$ outputs must be ORed together, and all $\overline{\text{EF}}$ outputs must be ORed together.
5. $\overline{\text{RT}}$ and $\overline{\text{HF}}$ functions are not available in the depth-expanded configuration.

combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 16).

APPLICATION INFORMATION

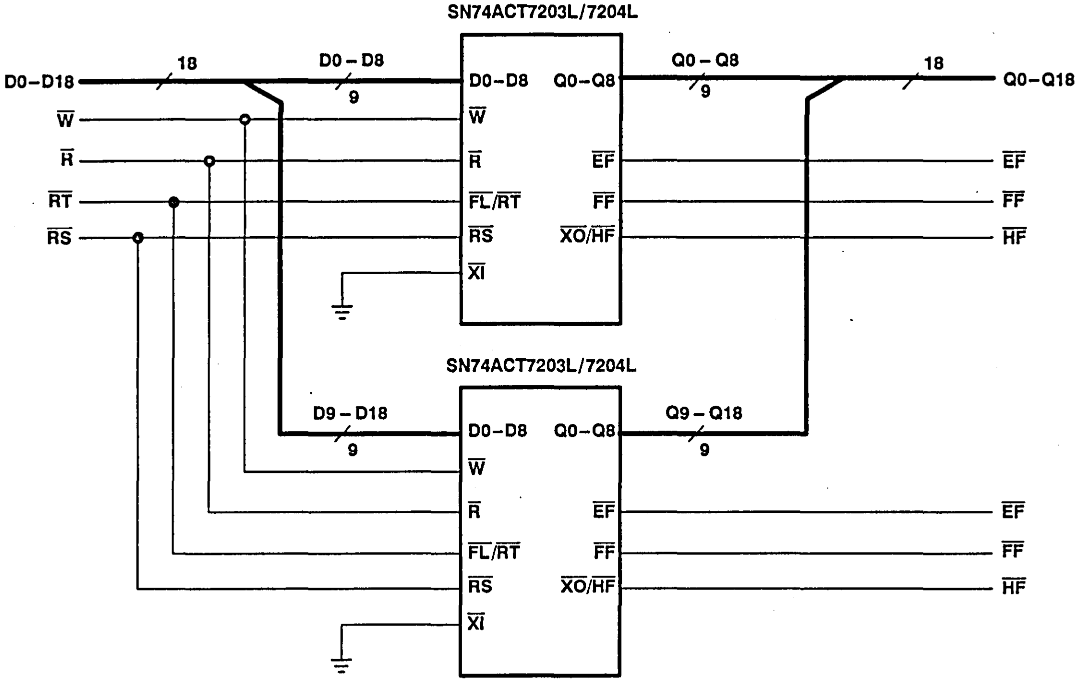


Figure 14. Word-Width Expansion: 2048/4096 Words × 18 Bits

APPLICATION INFORMATION

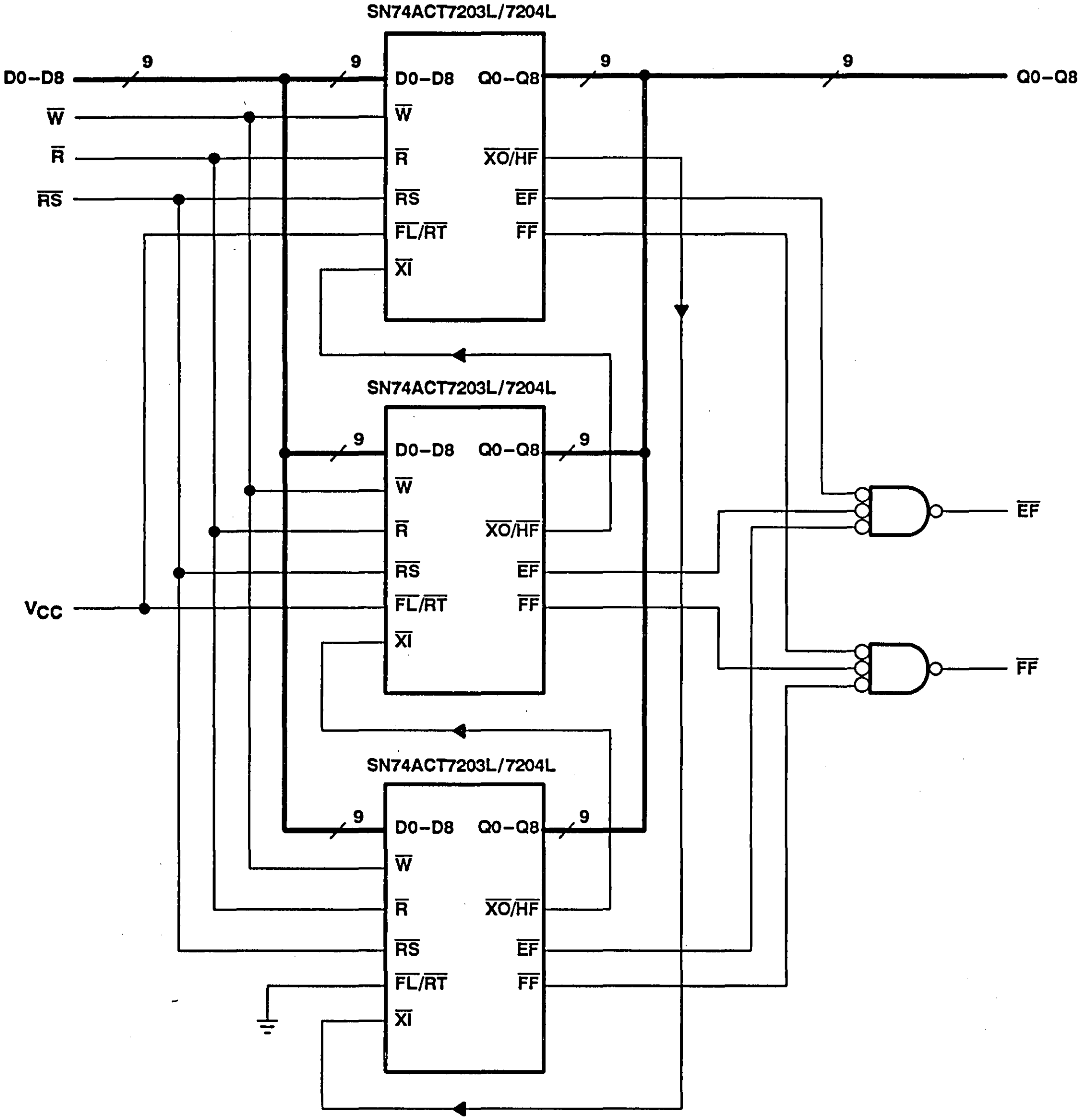


Figure 15. Word-Depth Expansion: 6144/12288 Words × 9 Bits

APPLICATION INFORMATION

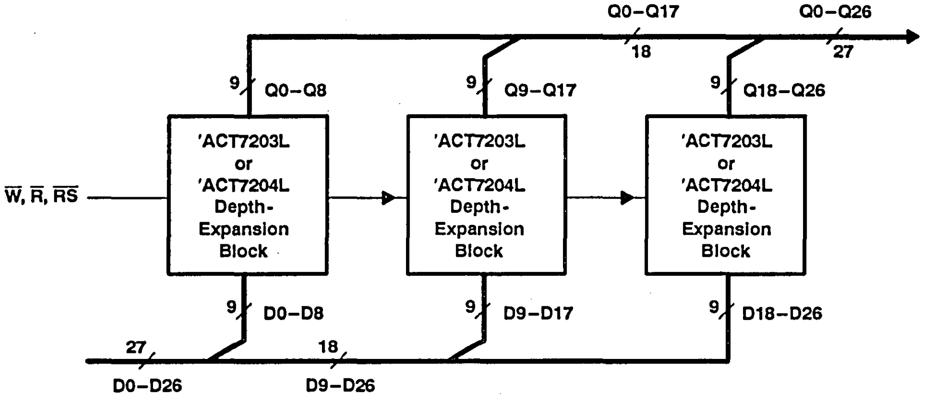


Figure 16. Word-Depth Plus Word-Width Expansion

9-BIT SYNCHRONOUS FIFOS

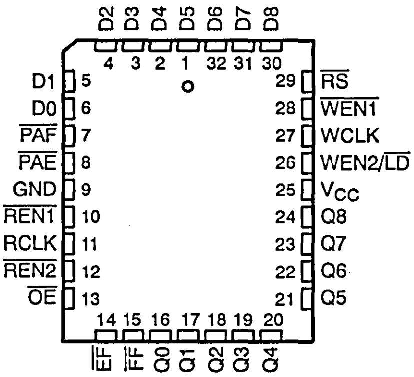
Features	Benefits
Data I/O employs synchronous control architecture	Allows for simultaneous read and write
Multiple speed sort options	Design flexibility
Depth from 512 to 4K words	Optimize depth for specific application
Write and read cycle times of 15 ns	Increased system performance
Bit-width expandable	Allows interface to larger data path architectures
Empty, full, programmable-empty and programmable-full flags	Multiple status flags to ease design efforts
Compatible to 722X1 pinout	Drop-in replaceable to existing layouts and designs
TI has established an alternate source	Standardization that comes from a common-product approach

SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, SN74ACT72241L
512 × 9, 1024 × 9, 2048 × 9, AND 4096 × 9
SYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS222 – FEBRUARY 1993 – REVISED JUNE 1993

- **Read and Write Clocks Can Be Asynchronous or Coincident**
- **Organization:**
  - **SN74ACT72211L – 512 × 9**
  - **SN74ACT72221L – 1024 × 9**
  - **SN74ACT72231L – 2048 × 9**
  - **SN74ACT72241L – 4096 × 9**
- **Write and Read Cycle Times of 15 ns**
- **Bit-Width Expandable**
- **Empty and Full Flags**
- **Programmable Almost-Empty and Almost-Full Flags With Default Offsets of Empty+7 and Full–7, Respectively**
- **TTL-Compatible Inputs**
- **Fully Compatible With the IDT72211/72221/72231/72241**
- **Available in 32-Pin Plastic J-Leaded Chip Carrier (RJ)**

RJ PACKAGE
(TOP VIEW)



description

The SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, and SN74ACT72241L are constructed with CMOS dual-port SRAM and are arranged as 512, 1024, 2048, and 4096 9-bit words, respectively. Internal write and read address counters provide data throughput on a first-in, first-out (FIFO) basis. Full and empty flags prevent memory overflow and underflow, and two programmable flags (almost full and almost empty) are provided.

The SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, and SN74ACT72241L are synchronous FIFOs, which means the data input port and data output port each employ synchronous control. Write-enable ($\overline{\text{WEN1}}$, WEN2/$\overline{\text{LD}}$) signals allow the low-to-high transition of the write clock (WCLK) to store data in memory, and read-enable ($\overline{\text{REN1}}$, $\overline{\text{REN2}}$) signals allow the low-to-high transition of the read clock (RCLK) to read data from memory. WCLK and RCLK are independent of one another and can operate asynchronously or be tied together for single-clock operation.

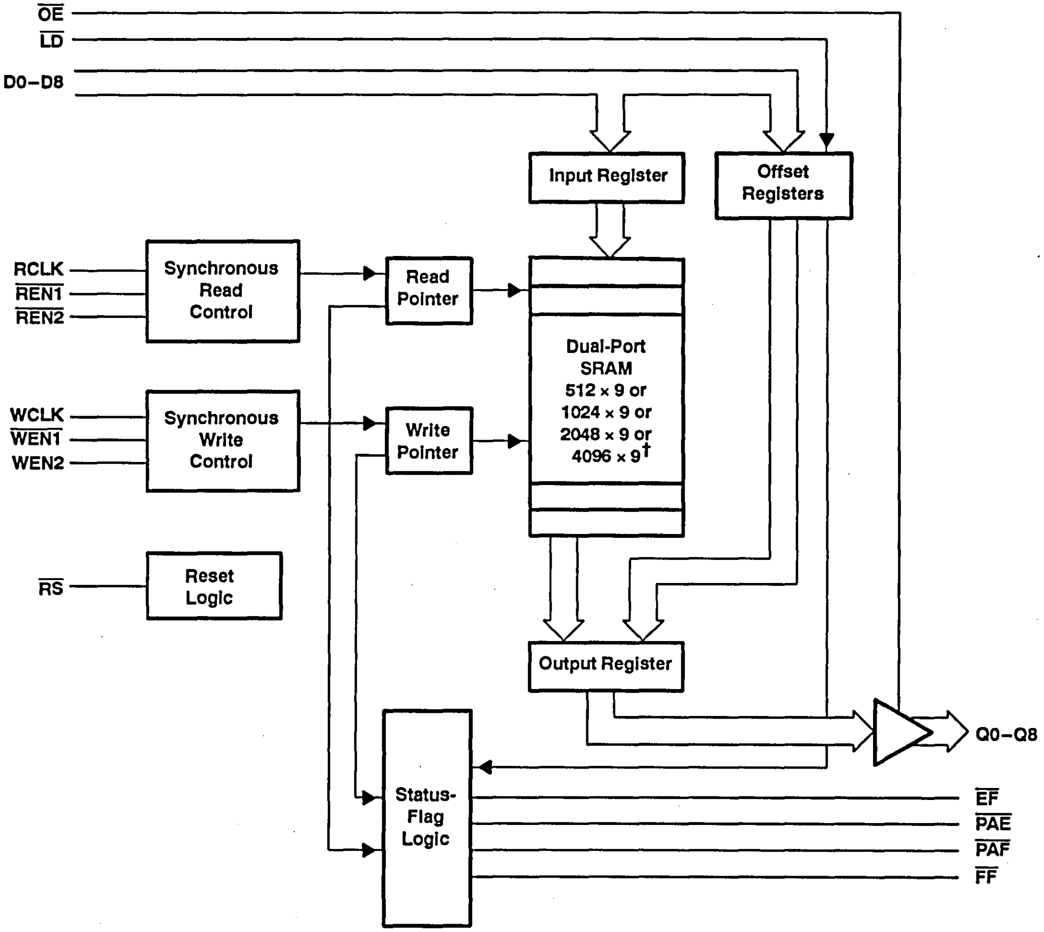
The empty-flag ($\overline{\text{EF}}$) output is synchronized to RCLK and the full-flag ($\overline{\text{FF}}$) output is synchronized to WCLK to indicate absolute boundary conditions. Write operations are prohibited when $\overline{\text{FF}}$ is low, and read operations are prohibited when $\overline{\text{EF}}$ is low. Two programmable flags, programmable almost empty ($\overline{\text{PAE}}$) and programmable almost full ($\overline{\text{PAF}}$), can both be programmed to indicate any measure of memory fill. After reset, $\overline{\text{PAE}}$ defaults to empty+7 and $\overline{\text{PAF}}$ defaults to full–7. Flag-offset programming control is similar to a memory write with the use of the load (WEN2/$\overline{\text{LD}}$) signal.

These devices are suited for providing a data channel between two buses operating at asynchronous or synchronous rates. Applications include use as rate buffers for graphics systems and high-speed queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information.

The SN74ACT72211L, SN74ACT72221L, SN74ACT72231L, and SN74ACT72241L are characterized for operation from 0°C to 70°C.

TEXAS
INSTRUMENTS

functional block diagram



† 512 × 9 for the SN74ACT72211L; 1024 × 9 for the SN74ACT72221L; 2048 × 9 for the SN74ACT72231L; 4096 × 9 for the SN74ACT72241L

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
D0–D8	6–1, 32–30	I	Data inputs
$\overline{\text{EF}}$	14	O	Empty-flag. When memory is empty, $\overline{\text{EF}}$ is low and further data reads are ignored by the device. When $\overline{\text{EF}}$ is high, the memory is not empty and data reads are allowed. $\overline{\text{EF}}$ is synchronized to RCLK by one flip-flop.
$\overline{\text{FF}}$	15	O	Full-flag. When memory is full, $\overline{\text{FF}}$ is low and data writes are inhibited. $\overline{\text{FF}}$ is synchronized to WCLK by one flip-flop.
GND	9		Ground
$\overline{\text{OE}}$	13	I	Output-enable. Q0–Q8 are in the high-impedance state when $\overline{\text{OE}}$ is high. Q0–Q8 are active when $\overline{\text{OE}}$ is low.
$\overline{\text{PAE}}$	8	O	Programmable almost-empty-flag. $\overline{\text{PAE}}$ is low when the FIFO is almost empty based on the value in its offset register. The default value for the register is empty + 7. $\overline{\text{PAE}}$ is synchronized to RCLK by one flip-flop.
$\overline{\text{PAF}}$	7	O	Programmable almost-full-flag. $\overline{\text{PAF}}$ is low when the FIFO is almost full based on the value in its offset register. The default value for the register is full –7. $\overline{\text{PAF}}$ is synchronized to WCLK by one flip-flop.
Q0–Q8	16–24	O	Data outputs
RCLK	11	I	Read-clock. A data read is performed by the low-to-high transition of RCLK when $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are asserted and $\overline{\text{EF}}$ is high.
$\overline{\text{REN1}}$, $\overline{\text{REN2}}$	10, 11	I	Read-enable. Data is read from the FIFO on a low-to-high transition of RCLK when $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are low and $\overline{\text{EF}}$ is high.
$\overline{\text{RS}}$	29	I	Reset. When $\overline{\text{RS}}$ is set low, the read and write pointers are initialized to the first RAM location and the FIFO is empty. $\overline{\text{FF}}$ and $\overline{\text{PAF}}$ are set high, and $\overline{\text{EF}}$ and $\overline{\text{PAE}}$ are set low. Each bit in the data output register is set low by a device reset. The FIFO must be reset after power up before data is written.
V_{CC}			Supply voltage
WCLK	27	I	Write-clock. Data is written by the low-to-high transition of WCLK when $\overline{\text{WEN1}}$ and WEN2/$\overline{\text{LD}}$ are asserted and $\overline{\text{FF}}$ is high.
$\overline{\text{WEN1}}$	28	I	Write-enable 1. $\overline{\text{WEN1}}$ is the only write enable terminal if the device is configured to have programmable flags. Data is written on a low-to-high transition of WCLK when $\overline{\text{WEN1}}$ is low and $\overline{\text{FF}}$ is high. If the FIFO is not configured for programmable flags, data is written on a low-to-high transition of WCLK when $\overline{\text{WEN1}}$ and WEN2 are asserted and $\overline{\text{FF}}$ is high.
WEN2/$\overline{\text{LD}}$	26	I	Write-enable 2/load. This is a dual-purpose input. The FIFO can have either two write enables or programmable flags. To use WEN2/$\overline{\text{LD}}$ as a WEN2, WEN2/$\overline{\text{LD}}$ must be held high at reset. When WEN2 and $\overline{\text{WEN1}}$ are asserted and $\overline{\text{FF}}$ is high, a low-to-high transition of WCLK writes data. To use WEN2/$\overline{\text{LD}}$ as the $\overline{\text{LD}}$ terminal, it must be held low at reset. In this case, $\overline{\text{LD}}$ is asserted low to write or read the programmable offset registers.

detailed description

device reset

A reset is performed by taking the reset ($\overline{\mathrm{RS}}$) input low. This initializes both the write and read pointers to the first memory location. After a reset, the full flag ($\overline{\mathrm{FF}}$) and programmable almost-full flag ($\overline{\mathrm{PAF}}$) are high and the empty flag ($\overline{\mathrm{EF}}$) and programmable almost-empty flag ($\overline{\mathrm{PAE}}$) are low. Each bit in the data output register (Q0–Q8) is set low, and the flag offset registers are loaded with the default offset values. A FIFO must be reset after power up before a write cycle is allowed.

The logic level on the dual-purpose input write enable 2/load (WEN2/$\overline{\mathrm{LD}}$) during reset determines its function. If WEN2/$\overline{\mathrm{LD}}$ is high when $\overline{\mathrm{RS}}$ returns high at the end of the reset cycle, the input is a second write enable (see FIFO writes and reads) and the programmable flags ($\overline{\mathrm{PAF}}$, $\overline{\mathrm{PAE}}$) can only use the default values. If WEN2/$\overline{\mathrm{LD}}$ is low when $\overline{\mathrm{RS}}$ returns high at the end of the reset cycle, the input is the load ($\overline{\mathrm{LD}}$) enable for writing and reading flag offset registers (see flag programming).

FIFO writes and reads

Data is written to memory by a low-to-high transition of write clock (WCLK) when write enable 1 ($\overline{\mathrm{WEN1}}$) is low, WEN2/$\overline{\mathrm{LD}}$ is high, and $\overline{\mathrm{FF}}$ is high. This stores D0–D8 data in the dual-port SRAM and increments the write pointer.

If no reads are performed after reset ($\overline{\mathrm{RS}}$ = V_{IL}), $\overline{\mathrm{FF}}$ is set low upon the completion of 512 writes to the SN74ACT72211, 1024 writes to the SN74ACT72221, 2048 writes to the SN74ACT72231, and 4096 writes to the SN74ACT72241. Attempted write cycles are ignored when $\overline{\mathrm{FF}}$ is low. $\overline{\mathrm{FF}}$ is set high by the first low-to-high transition of WCLK after data is read from a full FIFO. $\overline{\mathrm{FF}}$ and $\overline{\mathrm{PAF}}$ are each synchronized to the low-to-high transition of WCLK by one flip-flop.

If a device is configured to have two write enables (see device reset), data is read by the low-to-high transition of read clock (RCLK) when both read enables ($\overline{\mathrm{REN1}}$, $\overline{\mathrm{REN2}}$) are low and $\overline{\mathrm{EF}}$ is high. WEN2/$\overline{\mathrm{LD}}$ must also be high if the device is configured to have programmable flags. A read from the FIFO puts RAM data on Q0–Q8 and increments the read pointer in the same sequence as the write pointer. New data is not shifted to the output register while either one or both of the read enables are high.

$\overline{\mathrm{EF}}$ and $\overline{\mathrm{PAE}}$ are each synchronized to the low-to-high transition of RCLK by one flip-flop. When the device is empty, the write and read pointers are equal and $\overline{\mathrm{EF}}$ is set low. Attempted read cycles are ignored while $\overline{\mathrm{EF}}$ is set low. $\overline{\mathrm{EF}}$ is set high by the first low-to-high transition of RCLK after data is written to an empty FIFO.

WCLK and RCLK can be asynchronous or coincident to one another. Writing data to FIFO memory is independent of reading data from FIFO memory and vice versa.

flag programming

When WEN2/$\overline{\mathrm{LD}}$ is held low during a device reset ($\overline{\mathrm{RS}}$ = V_{IL}), the input is the load ($\overline{\mathrm{LD}}$) enable for flag offset programming. In this configuration, WEN2/$\overline{\mathrm{LD}}$ can be used to access the four 8-bit offset registers contained in the SN74ACT72211L/-72221L/-72231L/-72241L for writing or reading data.

When the device is configured for programmable flags and both WEN2/$\overline{\mathrm{LD}}$ and $\overline{\mathrm{WEN1}}$ are low, the first low-to-high transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth low-to-high transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{\mathrm{LD}}$ and $\overline{\mathrm{WEN1}}$ are low. The fifth low-to-high transition of WCLK while WEN2/$\overline{\mathrm{LD}}$ and $\overline{\mathrm{WEN1}}$ are low writes data to the empty LSB register again. Figure 1 shows the register sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then, by bringing the WEN2/$\overline{\mathrm{LD}}$ input high, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{\mathrm{LD}}$ is brought low, a write operation stores data in the next offset register in sequence.

flag programming (continued)

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{\text{LD}}$ is low and both $\overline{\text{REN1}}$ and $\overline{\text{REN2}}$ are low. Low-to-high transitions of RCLK read the register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers (see Figure 1 and Table 1).

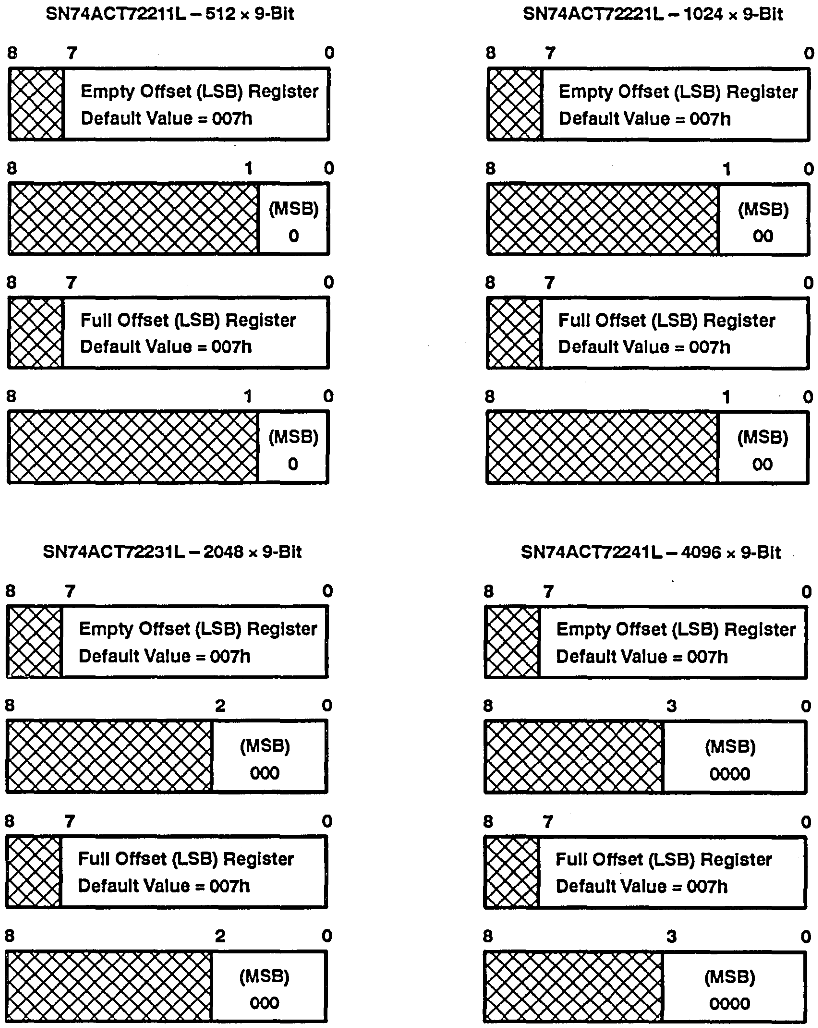


Figure 1. Offset Register Location and Default Values

flag programming (continued)

Table 1. Writing the Offset Registers

$\overline{\mathrm{LD}}$	$\overline{\mathrm{WEN1}}$	WCLK†	SELECTION
0	0	↑	Empty offset (LSB) Empty offset (MSB) Full offset (LSB) Full offset (MSB)
0	1	↑	No operation
1	0	↑	Write into FIFO
1	1	↑	No operation

† The same selection sequence applies to reading from the registers. $\overline{\mathrm{REN1}}$ and $\overline{\mathrm{REN2}}$ are enabled and a read is performed on the low-to-high transition of RCLK.

programmable flag ($\overline{\mathrm{PAE}}$, $\overline{\mathrm{PAF}}$) operation

Whether the flag offset registers are programmed as described in Table 1 or the default values are used, the programmable almost-empty flag ($\overline{\mathrm{PAE}}$) and programmable almost-full flag ($\overline{\mathrm{PAF}}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

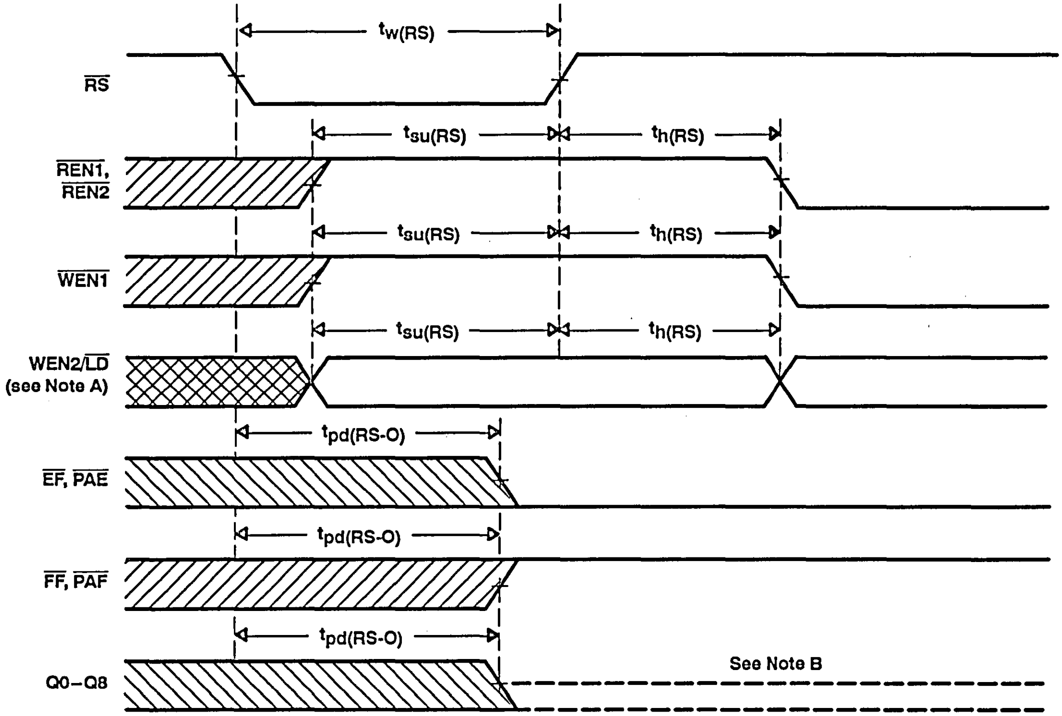
The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as *n* and determines the operation of $\overline{\mathrm{PAE}}$. $\overline{\mathrm{PAE}}$ is synchronized to the low-to-high transition of RCLK by one flip-flop and is low when the FIFO contains n or fewer unread words. $\overline{\mathrm{PAE}}$ is set high by the low-to-high transition of RCLK when the FIFO contains (n + 1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{\mathrm{PAF}}$. $\overline{\mathrm{PAF}}$ is synchronized to the low-to-high transition of WCLK by one flip-flop and is set low when the number of unread words in the FIFO is greater then or equal to (512 – m) for the SN74ACT72211L, (1024 – m) for the SN74ACT72221L, (2048 – m) for the SN74ACT72231L, and (4096 – m) for the SN74ACT72241L. $\overline{\mathrm{PAF}}$ is set high by the low-to-high transition of WCLK when the number of available memory locations is greater than m (see Table 2).

Table 2. Status Flags

NUMBER OF WORDS IN FIFO				OUTPUTS			
SN74ACT72211L	SN74ACT72221L	SN74ACT72231L	SN74ACT72241L	$\overline{\mathrm{FF}}$	$\overline{\mathrm{PAF}}$	$\overline{\mathrm{PAE}}$	$\overline{\mathrm{EF}}$
0	0	0	0	H	H	L	L
1 to n†	1 to n†	1 to n†	1 to n†	H	H	L	H
(n + 1) to [512 – (m + 1)]	(n + 1) to [1024 – (m + 1)]	(n + 1) to [2048 – (m + 1)]	(n + 1) to [4096 – (m + 1)]	H	H	H	H
(512 – m)‡ to 511	(1024 – m)‡ to 1023	(2048 – m)‡ to 2047	(4096 – m)‡ to 4095	H	L	H	H
512	1024	2048	4096	L	L	H	H

† n = empty offset (default value = 7)
‡ m = full offset (default value = 7)

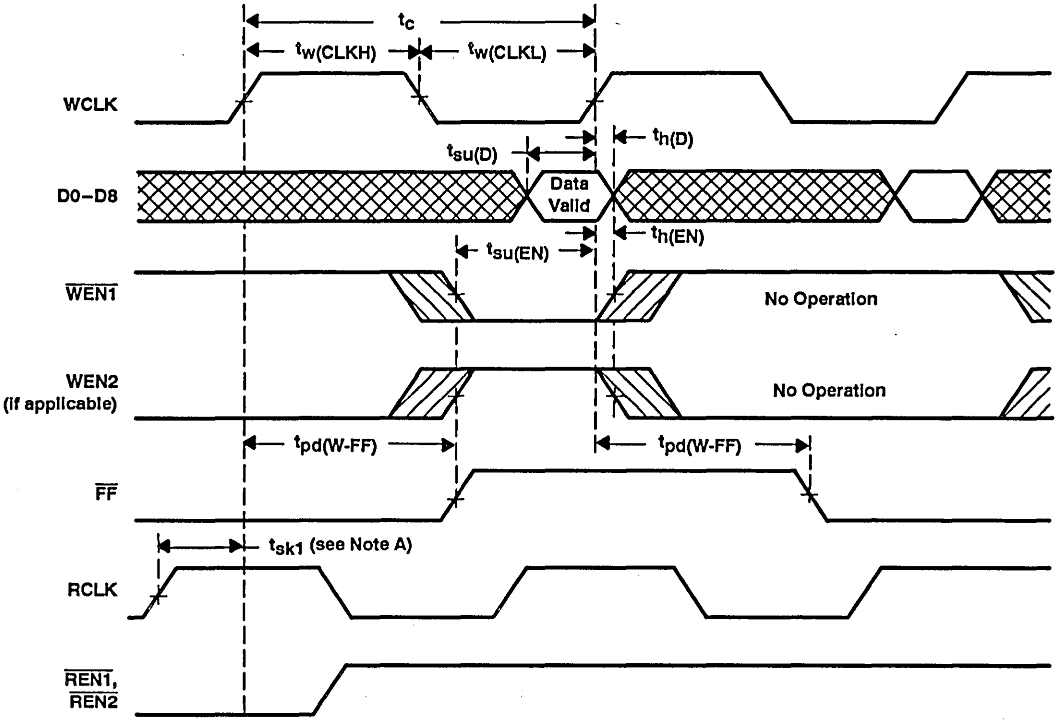


NOTES: A. Holding WEN2/$\overline{LD}$ high during reset makes it act as a second write enable. Holding WEN2/$\overline{LD}$ low during reset makes it act as a load enable for the programmable flag offset registers.

B. After reset, the outputs are low if $\overline{OE}$ is low and at the high-impedance level if $\overline{OE}$ is high.

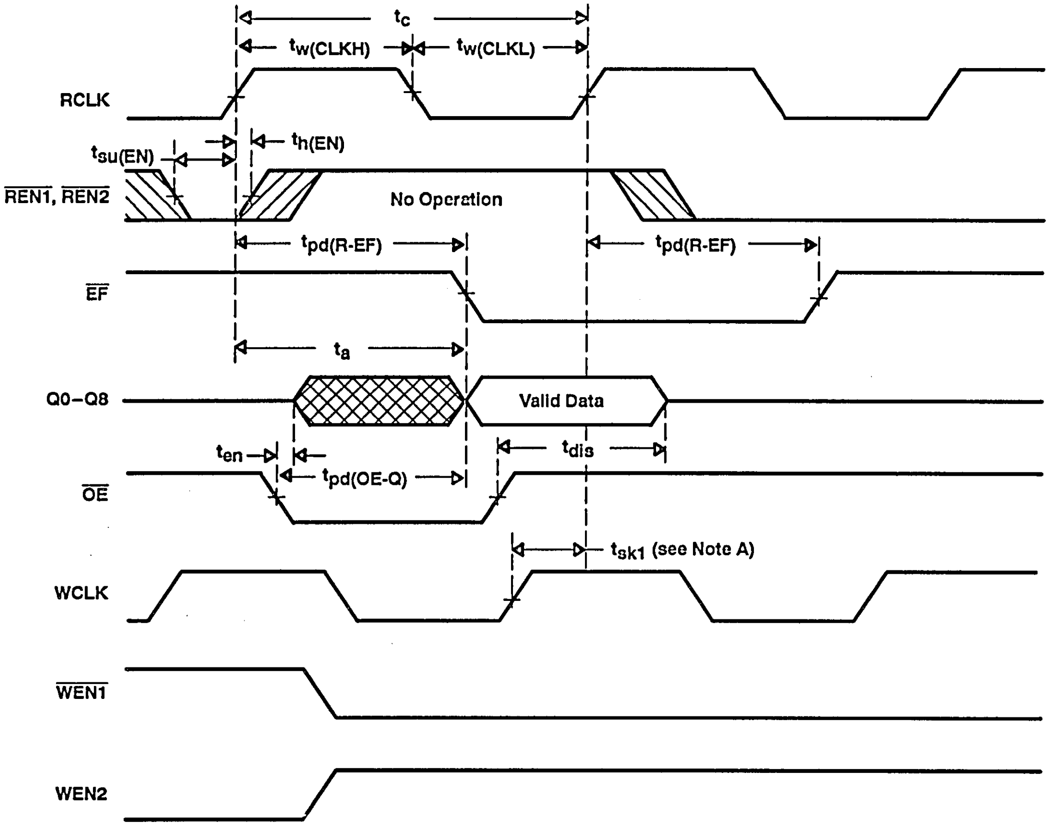
C. The clocks (RCLK, WCLK) can be free running during reset.

Figure 2. Reset Timing



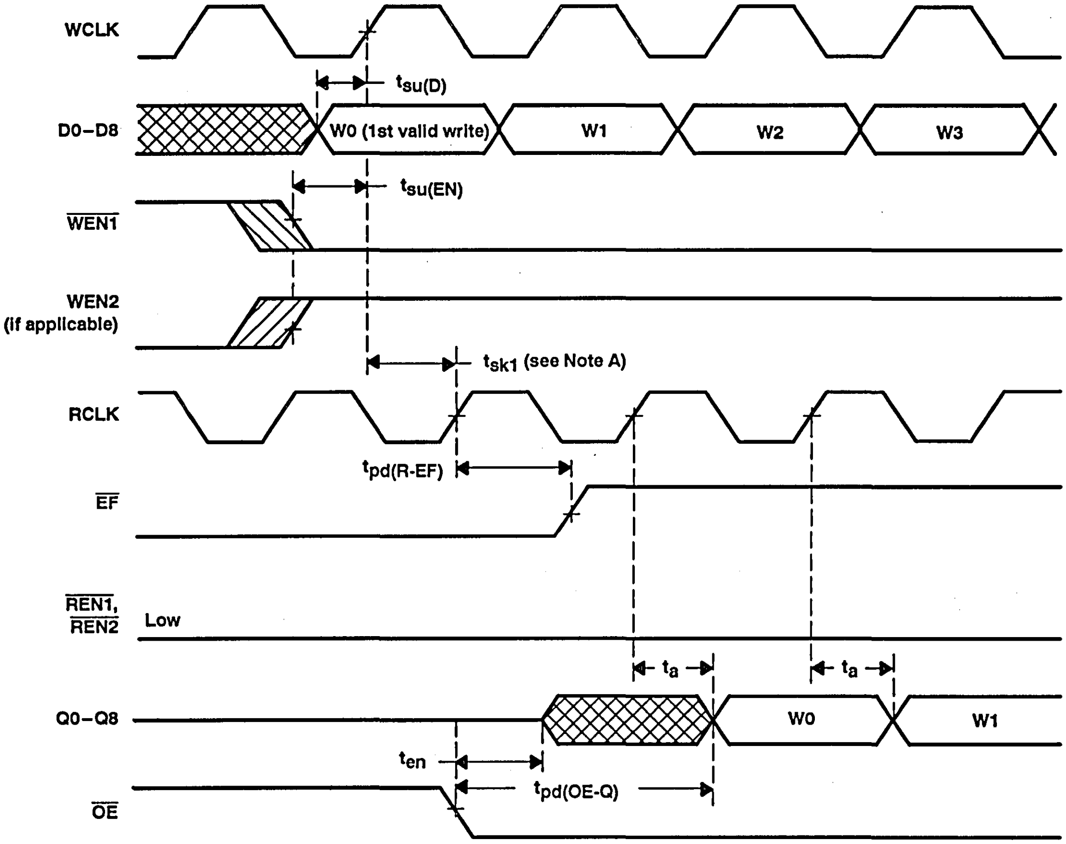
NOTE A: t_{sk1} is the minimum time between a rising RCLK edge and a subsequent rising WCLK edge for $\overline{FF}$ to change logic levels during the current clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than t_{sk1}, then $\overline{FF}$ may not change its logic level until the next WCLK rising edge.

Figure 3. Write-Cycle Timing



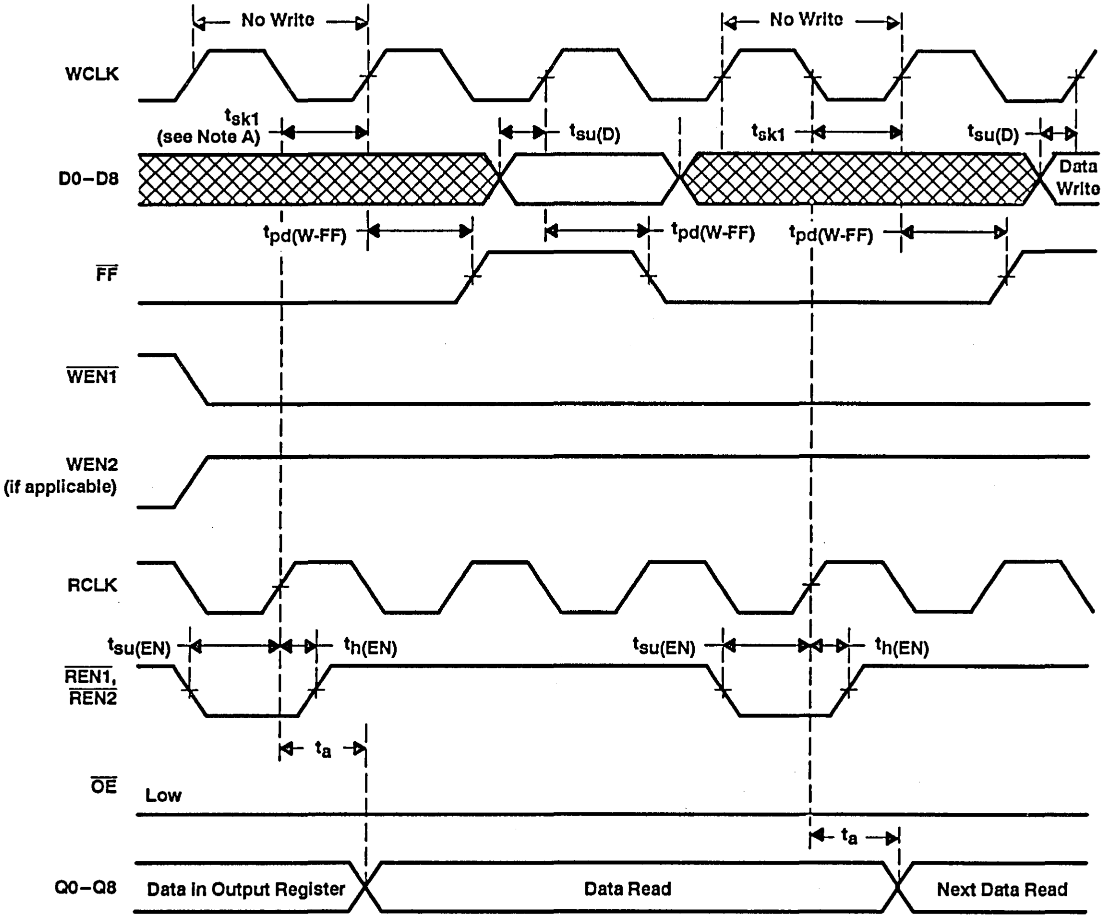
NOTE A: t_{sk1} is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change logic levels during the current clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than t_{sk1}, then $\overline{EF}$ may not change its logic level until the next RCLK rising edge.

Figure 4. Read-Cycle Timing



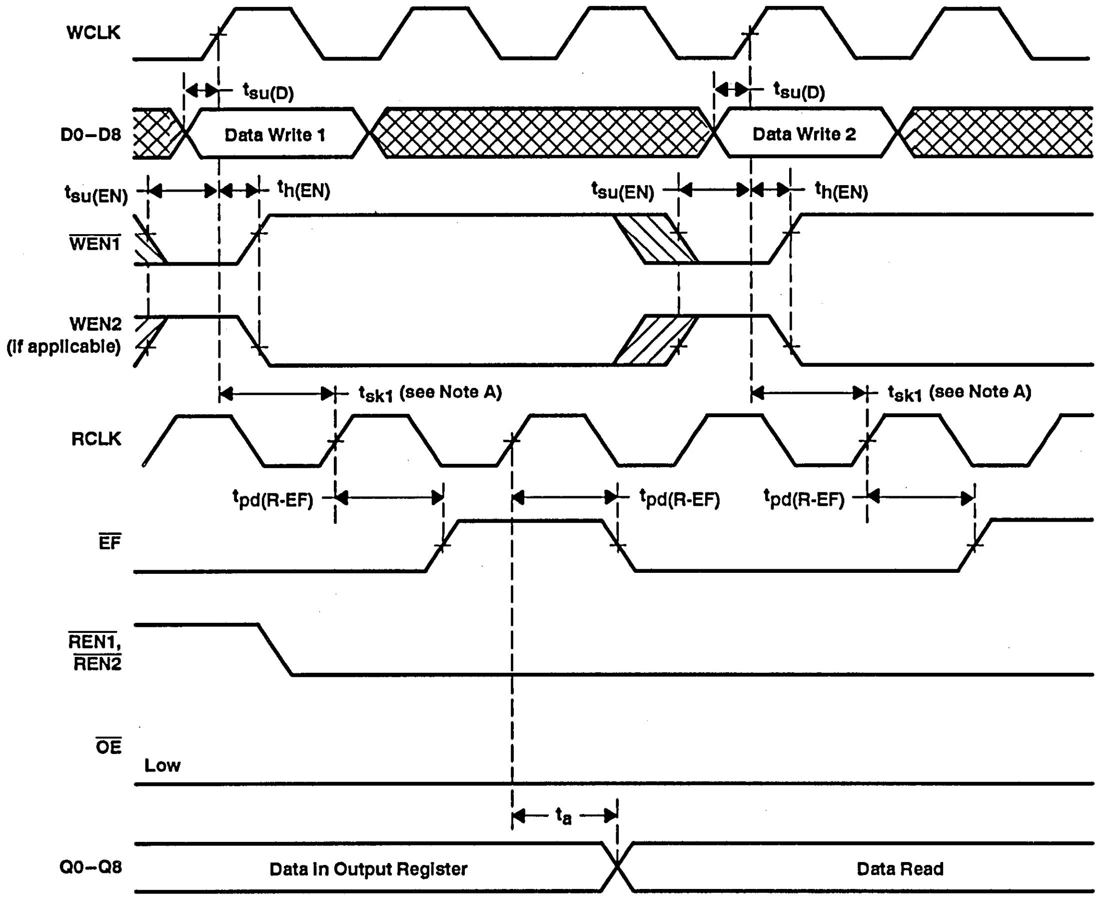
NOTE A: t_{sk1} is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{sk1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 5. First-Data-Word-Latency Timing



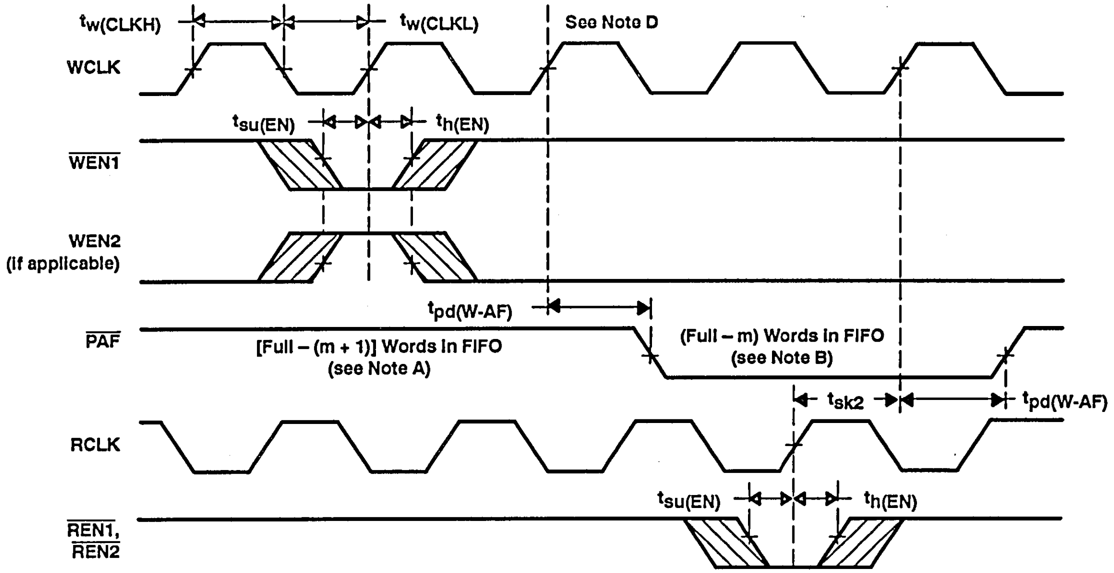
NOTE A: t_{sk1} is the minimum time between a rising RCLK edge and a subsequent rising WCLK edge for $\overline{FF}$ to change logic levels during the current clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than t_{sk1}, then $\overline{FF}$ may not change its logic level until the next WCLK rising edge.

Figure 6. Full-Flag Timing



NOTE A: t_{sk1} is the minimum time between a rising WCLK edge and a subsequent rising RCLK edge for $\overline{EF}$ to change logic levels during the current clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than t_{sk1}, then $\overline{EF}$ may not change its logic level until the next RCLK rising edge.

Figure 7. Empty-Flag Timing



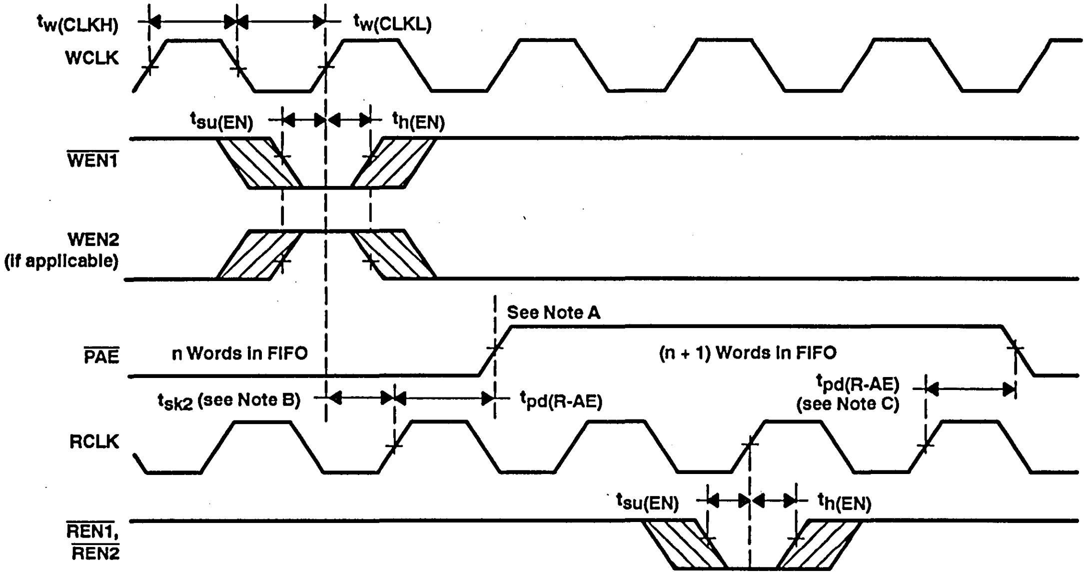
NOTES: A. $\overline{PAF}$ offset = m

B. (512 – m) words for SN74ACT72211L, (1024 – m) words for SN74ACT72221L, (2048 – m) words for SN74ACT72231L, (4096 – m) words for SN74ACT72241L

C. t_{sk2} is the minimum time between a rising RCLK edge and the subsequent rising WCLK edge for $\overline{PAF}$ to change its logic level during that clock cycle. If the time between the rising edge of RCLK and the subsequent rising edge of WCLK is less than t_{sk2}, then $\overline{PAF}$ may not change its logic level until the next WCLK rising edge.

D. If a write is performed on this rising edge of the write clock, there will be [Full – (m – 1)] words in the FIFO when $\overline{PAF}$ goes low.

Figure 8. Programmable Almost-Full Flag Timing



NOTES: A. $\overline{PAE}$ offset = n

B. t_{sk2} is the minimum time between a rising WCLK edge and the subsequent rising RCLK edge for $\overline{PAE}$ to change its logic level during that clock cycle. If the time between the rising edge of WCLK and the subsequent rising edge of RCLK is less than t_{sk2}, then $\overline{PAE}$ may not change its logic level until the next RCLK rising edge.

C. If a write is performed on this rising edge of the write clock, there will be [Empty + (n – 1)] words in the FIFO when $\overline{PAE}$ goes low.

Figure 9. Programmable Almost-Empty Flag Timing

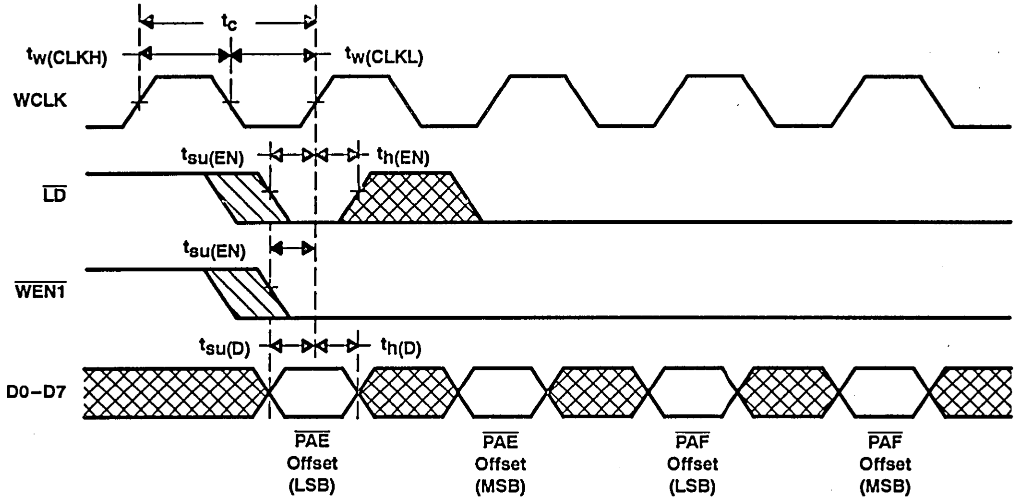


Figure 10. Write-Offset-Registers Timing

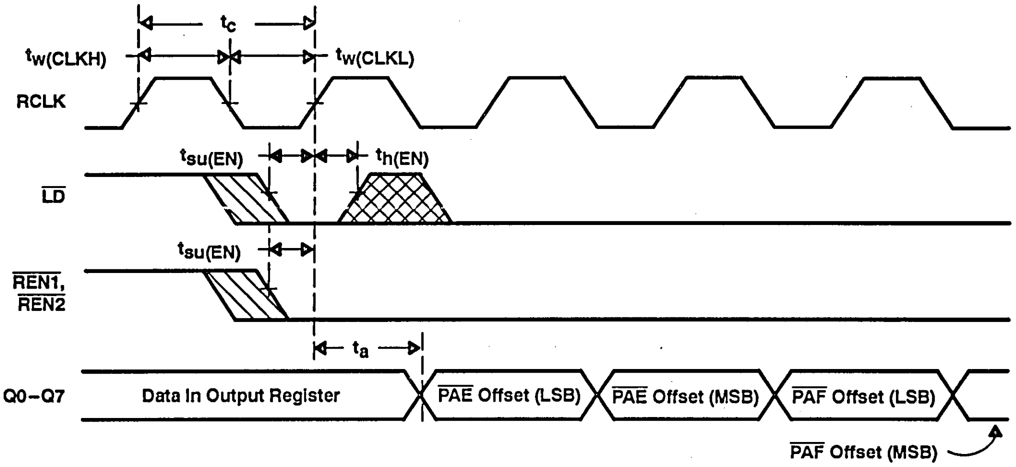


Figure 11. Read-Offset-Registers Timing

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Input voltage range, any input, V_I (see Note 1)	−0.5 V to 7 V
Continuous output current, I_O	±50 mA
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range under bias	−55°C to 125°C
Storage temperature range	−55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = − 2 mA		2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	V
I_I	Input current	V_{CC} = 5.5 V,	V_I = V_{CC} or 0 V			±1	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.5 V,	V_O = V_{CC} or 0 V			±10	µA
C_i‡	Input capacitance	V_I = 0,	f = 1 MHz			10	pF
C_o‡	Output capacitance	V_O = 0,	f = 1 MHz,	$\overline{OE} \geq V_{IH}$		10	pF
I_{CC}¶	Active supply current	f_{clock} = 20 MHz	SN74ACT72211L			140§	mA
			SN74ACT72221L, SN74ACT72231L, SN74ACT72241L			160#	

‡ Specified by design but not tested

§ I_{CC} measurements are made with outputs open (only capacitive loading). Typical $I_{CC} = 65 + (f_{clock} \times 1.1/\text{MHz}) + (f_{clock} \times C_L \times 0.03/\text{MHz-pF})$ mA (C_L = external capacitive load).

¶ The I_{CC} limits are valid for t_c = 15, 20, 25, and 50 ns.

I_{CC} measurements are made with outputs open (only capacitive loading). Typical $I_{CC} = 80 + (f_{clock} \times 2.1/\text{MHz}) + (f_{clock} \times C_L \times 0.03/\text{MHz-pF})$ mA (C_L = external capacitive load).

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 2 through 13)

		'ACT72211L-15 'ACT72221L-15 'ACT72231L-15 'ACT72241L-15		'ACT72211L-20 'ACT72221L-20 'ACT72231L-20 'ACT72241L-20		'ACT72211L-25 'ACT72221L-25 'ACT72231L-25 'ACT72241L-25		'ACT72211L-50 'ACT72221L-50 'ACT72231L-50 'ACT72241L-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, RCLK or WCLK		66.7		50		40		20	MHz
t_c	Clock cycle time, RCLK or WCLK	15[†]		20		25		50		ns
$t_{w(CLKH)}$	Pulse duration, RCLK or WCLK high	6		8		10		20		ns
$t_{w(CLKL)}$	Pulse duration, RCLK or WCLK low	6		8		10		20		ns
$t_{w(RS)}$	Pulse duration, $\overline{\text{RS}}$ low	15		20		25		50		ns
$t_{su(D)}$	Setup time, D0–D8 before RCLK↑	4		5		6		10		ns
$t_{su(EN)}$	Setup time, $\overline{\text{WEN1}}$, WEN2[‡], and $\overline{\text{LD}}$[§] before WCLK↑; $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, and $\overline{\text{LD}}$[§] before RCLK↑	4		5		6		10		ns
$t_{su(RS)}$	Setup time, $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, $\overline{\text{WEN1}}$, and WEN2/$\overline{\text{LD}}$ before $\overline{\text{RS}}$ high	15		20		25		50		ns
$t_{h(D)}$	Hold time, D0–D8 after RCLK↑	1		1		1		2		ns
$t_{h(EN)}$	Hold time, $\overline{\text{WEN1}}$, WEN2[‡], and $\overline{\text{LD}}$[§] after WCLK↑; $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, and $\overline{\text{LD}}$[§] after RCLK↑	1		1		1		2		ns
$t_{h(RS)}$	Hold time, $\overline{\text{REN1}}$, $\overline{\text{REN2}}$, $\overline{\text{WEN1}}$, and WEN2/$\overline{\text{LD}}$ after $\overline{\text{RS}}$ high	15		20		25		50		
t_{sk1}	Skew time between RCLK↑ and WCLK↑ to allow $\overline{\text{EF}}$ or $\overline{\text{FF}}$ to change logic levels during the current clock cycle	6		8		10		15		ns
t_{sk2}	Skew time between RCLK↑ and WCLK↑ to allow $\overline{\text{PAF}}$ or $\overline{\text{PAE}}$ to change logic levels during the current clock cycle	28		35		40		45		ns

[†] Valid for $\overline{\text{PAE}}$ or $\overline{\text{PAF}}$ program values as follows:
≤ 63 bytes from the respective boundary for the SN74ACT72211L;
≤ 511 bytes from the respective boundary for the SN74ACT72221L/-72231L/-72241L;
minimum t_c is 20 ns for program values greater than those indicated above.

[‡] Applicable when the device is configured with two write-enable inputs (WEN2/$\overline{\text{LD}}$ = WEN2).

[§] Applicable when the device is configured to have programmable flags (WEN2/$\overline{\text{LD}}$ = $\overline{\text{LD}}$).

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 2 through 13)

PARAMETER		'ACT72211L-15 'ACT72221L-15 'ACT72231L-15 'ACT72241L-15		'ACT72211L-20 'ACT72221L-20 'ACT72231L-20 'ACT72241L-20		'ACT72211L-25 'ACT72221L-25 'ACT72231L-25 'ACT72241L-25		'ACT72211L-50 'ACT72221L-50 'ACT72231L-50 'ACT72241L-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, RCLK↑ to Q0–Q8 valid	2	10	2	12	3	15	3	25	ns
$t_{pd(OE-Q)}$	Propagation delay time, $\overline{\text{OE}}$ low to Q0–Q8 valid	3	8	3	10	3	13	3	28	ns
$t_{pd(R-EF)}$	Propagation delay time, RCLK↑ to $\overline{\text{EF}}$ low or high		10		12		15		30	ns
$t_{pd(W-FF)}$	Propagation delay time, WCLK↑ to $\overline{\text{FF}}$ low or high		10		12		15		30	ns
$t_{pd(R-AE)}$	Propagation delay time, RCLK↑ to $\overline{\text{PAE}}$ low or high		10		12		15		30	ns
$t_{pd(W-AF)}$	Propagation delay time, WCLK↑ to $\overline{\text{PAF}}$ low or high		10		12		15		30	ns
$t_{pd(RS-O)}$	Propagation delay time, $\overline{\text{RS}}$ low to $\overline{\text{FF}}$ and $\overline{\text{PAF}}$ high and $\overline{\text{EF}}$, $\overline{\text{PAE}}$, and Q0–Q8 low		15		20		25		50	ns
t_{en}	Enable time, $\overline{\text{OE}}$ low to Q0–Q8 at the low-impedance level†	0		0		0		0		ns
t_{dis}	Disable time, $\overline{\text{OE}}$ high to Q0–Q8 at the high-impedance level†	3	8	3	10	3	13	3	28	ns

† These values are characterized but not tested.

APPLICATION INFORMATION

width-expansion configuration

Word width is increased by connecting the corresponding input control signals of multiple devices. Composite empty and full flags should be created by monitoring all devices in width expansion. Almost-full and almost-empty status can be obtained from any one device. Figure 12 shows an 18-bit-wide data path formed by using two SN74ACT72211L/72221L/72231L/72241L devices.

In Figure 12, read enable 2 ($\overline{\text{REN2}}$) is grounded and read enable 1 ($\overline{\text{REN1}}$) acts as the only read control. The write enable 2/load (WEN2/$\overline{\text{LD}}$) input of only one device is set low at reset to configure the device for programmable flags and to have it act as a load control for reading and writing the programmable flag offset registers.

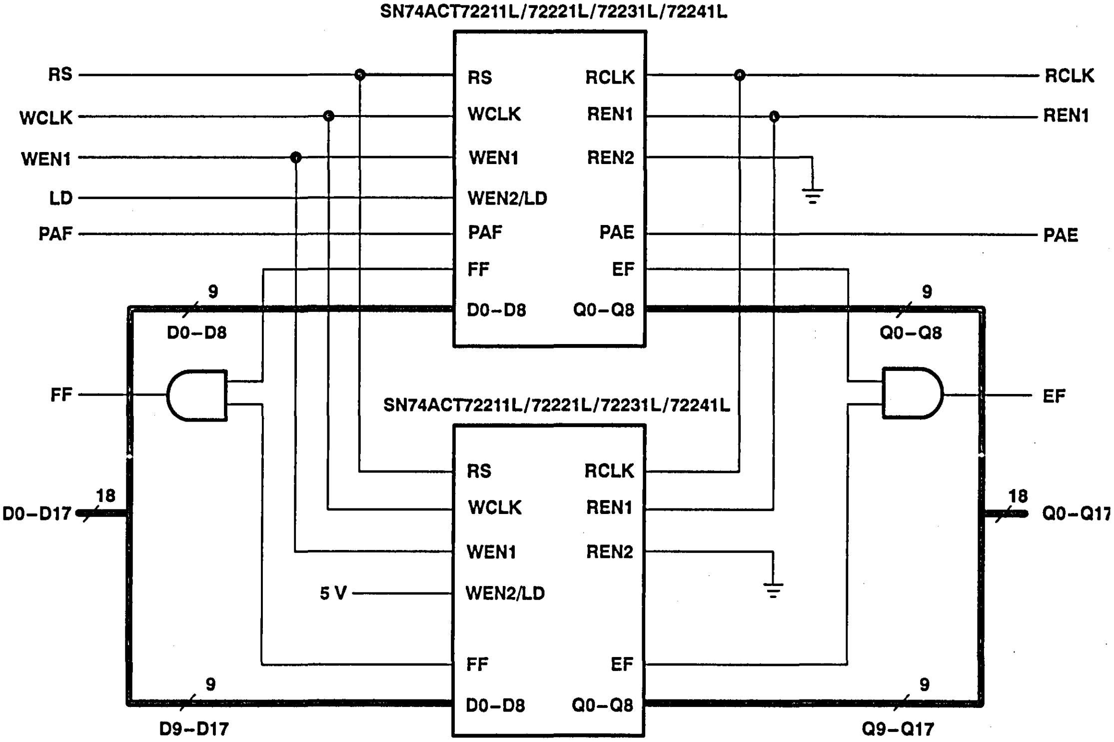
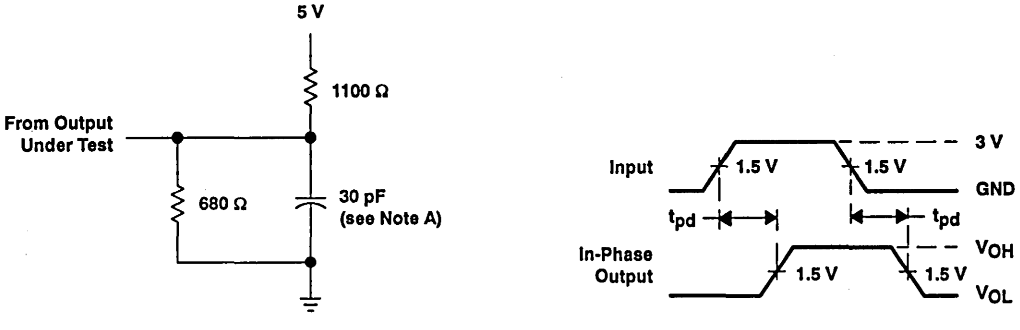


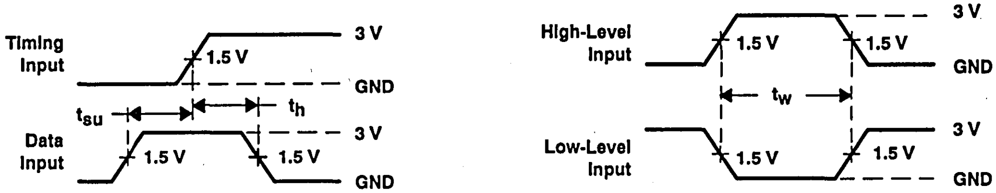
Figure 12. Word-Width Expansion for 512/1024/2048/4096 × 18 FIFO

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTE A: Includes probe and jig capacitance

Figure 13. Load Circuit and Voltage Waveforms

REDUCED-WIDTH FIFOS

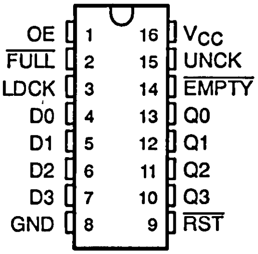
Features	Benefits
Frequencies up to 40 MHZ	Multiple frequencies for greater system-performance flexibility
3-state outputs	Disables output from the data path
Depths available from 16 to 64 words	Shallow depths for elastic store
Package options include SOIC PLCC, and DIP	Multiple package options for high-volume production requirements

SN74ALS232B
16 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

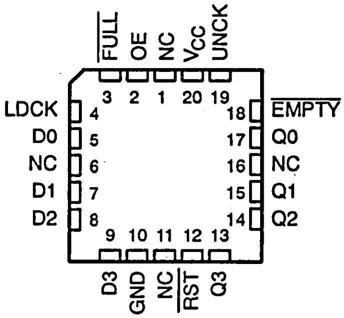
SCAS251 – FEBRUARY 1989 – REVISED SEPTEMBER 1993

- **Independent Asynchronous Inputs and Outputs**
- **16 Words by 4 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 64-bit memory use advanced low-power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 4 bits each.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

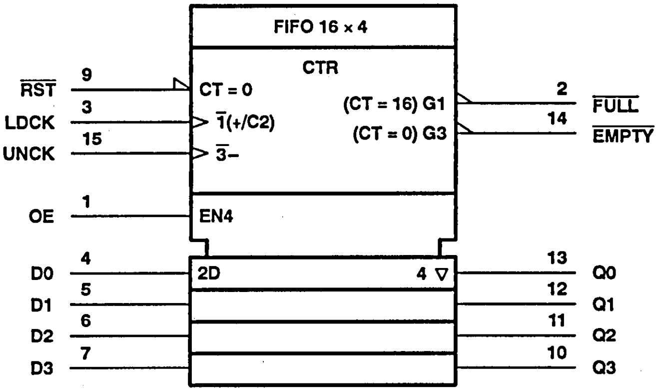
Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack-control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the $\overline{\text{FULL}}$ or $\overline{\text{EMPTY}}$ output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS232B is characterized for operation from 0°C to 70°C.

logic symbol†



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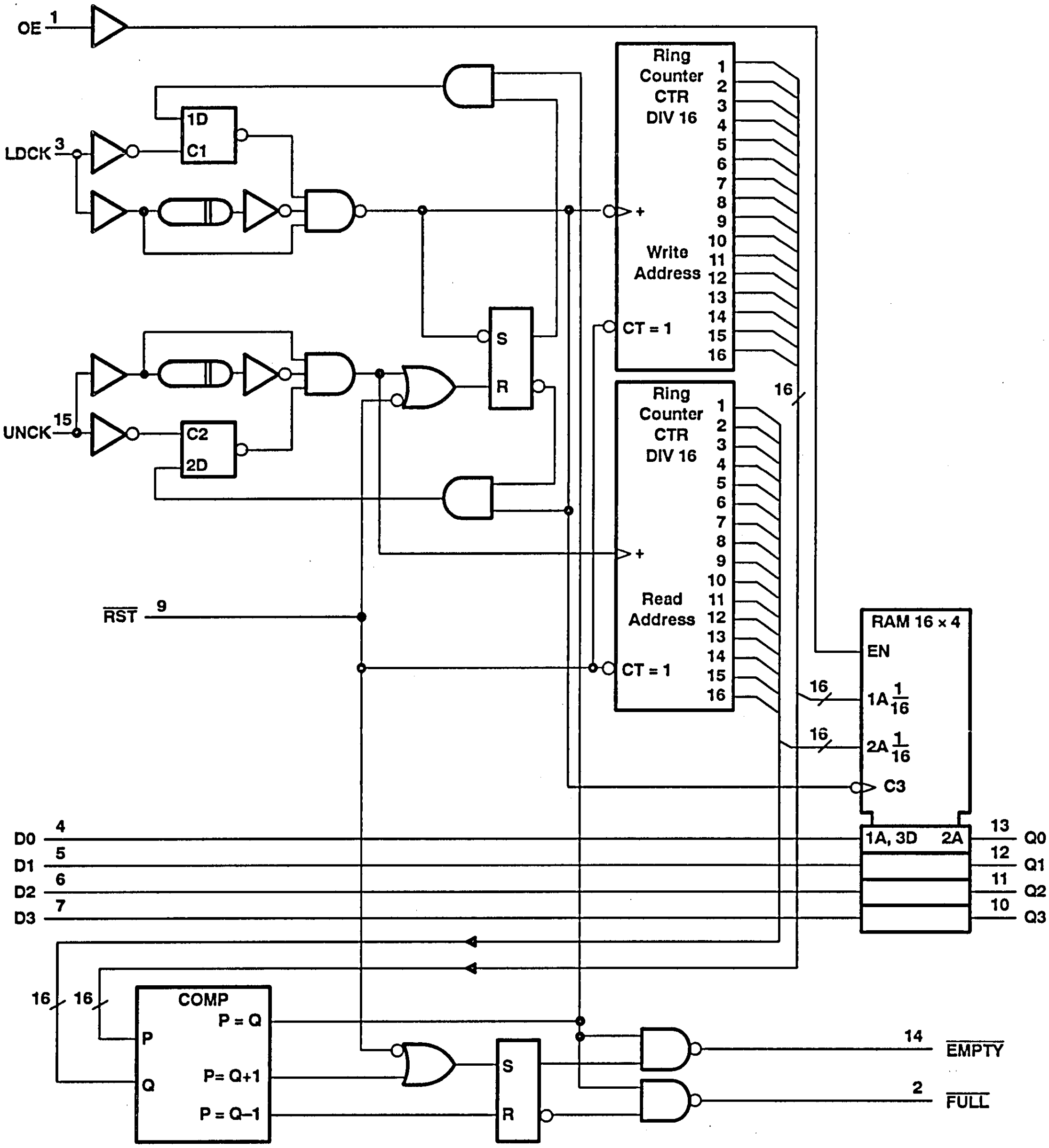
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

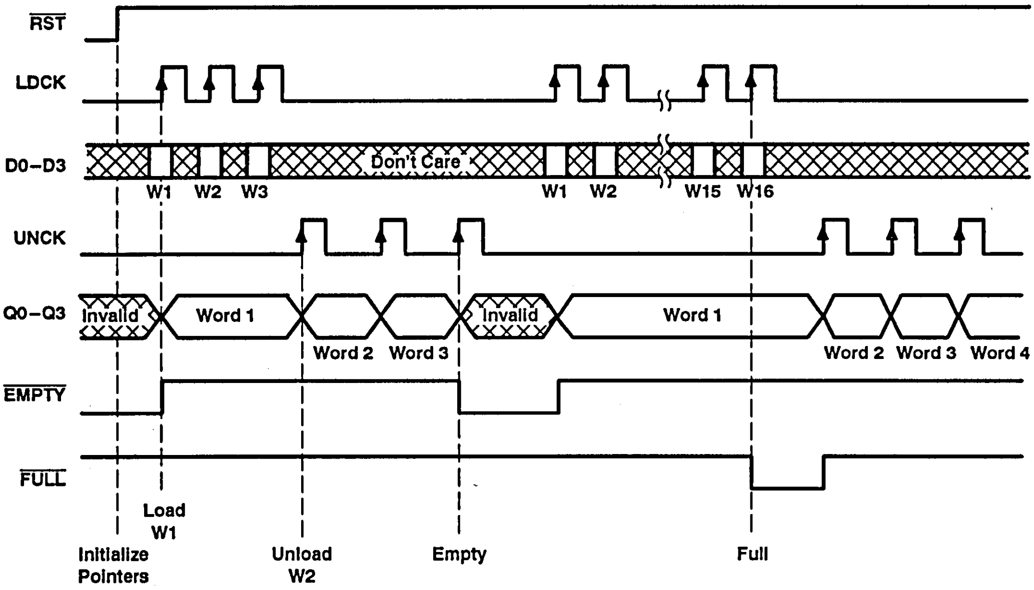
Pin numbers shown are for the DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for the DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−2.6	mA
		$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$			8	
f_{clock}[†]	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{\text{RST}}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		LDCK inactive before $\overline{\text{RST}}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
		LDCK inactive after $\overline{\text{RST}}$↑	5			
T_A	Operating free-air temperature		0		70	°C

[†] The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum V_{IL}, minimum V_{IH}, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
	$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	$\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O[§]		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			80	125	mA

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

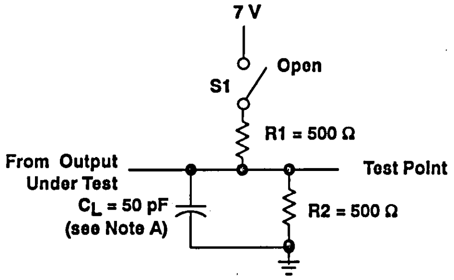
[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	LDCK, UNCK			50		40		MHz
t_{pd}	LDCK↑	Any Q		14	23	6	30	ns
	UNCK↑			15	23	6	30	
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$		13	20	5	25	ns
t_{PHL}	UNCK↑			15	22	6	27	
t_{PHL}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY}}$		15	21	5	26	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$		15	22	6	27	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$		13	20	5	25	ns
	$\overline{\text{RST}}$↓			16	23	7	28	
t_{en}	OE↑	Q		5	12	1	14	ns
t_{dis}	OE↓	Q		5	12	1	16	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

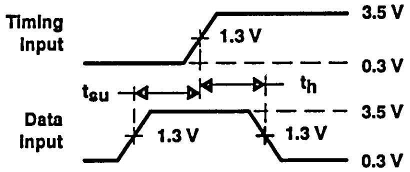
PARAMETER MEASUREMENT INFORMATION



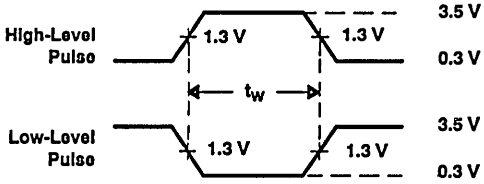
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

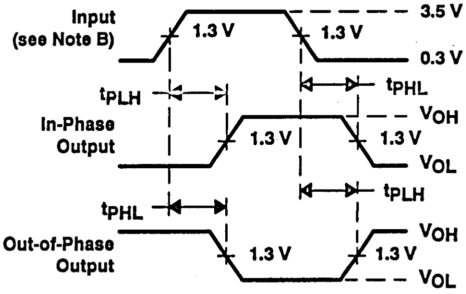
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



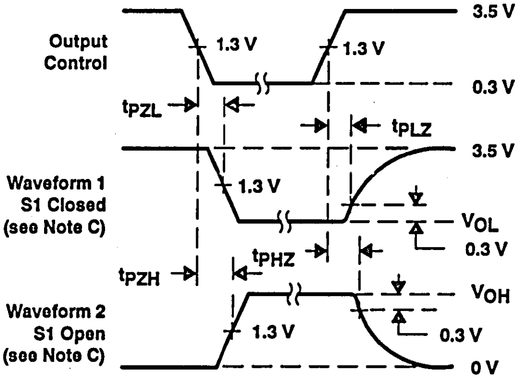
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

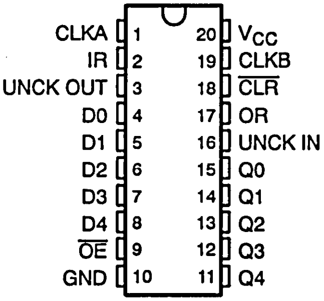
Figure 1. Load Circuit and Voltage Waveforms

SN74S225
16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

SDLS207 – SEPTEMBER 1976 – REVISED SEPTEMBER 1993

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **DC to 10-MHz Data Rate**
- **3-State Outputs**
- **Packaged in Standard Plastic 300-mil DIPs**

N PACKAGE
(TOP VIEW)



description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words by 5 bits. A memory system using the SN74S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The 3-state outputs controlled by a single output-enable ($\overline{OE}$) input make bus connection and multiplexing easy.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from dc to 10 MHz in a bit-parallel format, word by word.

Reading or writing is done independently utilizing separate asynchronous data clocks. Data can be written into the array on the low-to-high transition of either load-clock (CLKA, CLKB) input. Data can be read out of the array on the low-to-high transition of the unload-clock (UNCK IN) input (normally high). Writing data into the FIFO can be accomplished in one of two manners:

1. In applications not requiring a gated clock control, best results will be achieved by applying the clock input to one of the clocks while tying the other clock input high.
2. In applications needing a gated clock, the load clock (gate control) must be high in order for the FIFO to load on the next clock pulse.

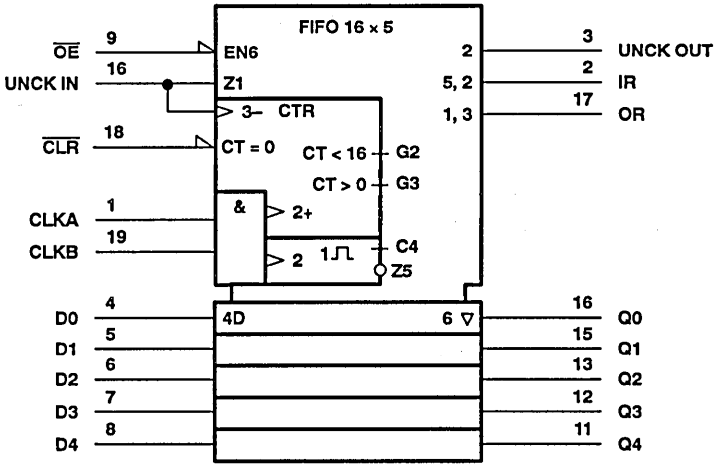
CLKA and CLKB can be used interchangeably for either clock gate control or clock input.

Status of the SN74S225 is provided by three outputs. The input-ready (IR) output monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload-clock (UNCK OUT) output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready (OR), is high when the first word location contains valid data and UNCK IN is high. When UNCK IN goes low, OR will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are 3-state with a common control input ($\overline{OE}$). When $\overline{OE}$ is low, the data outputs are enabled to function as totem-pole outputs. A high logic level forces each data output to a high-impedance state while all other inputs and outputs remain active.The clear ($\overline{CLR}$) input invalidates all data stored in the memory array by clearing the control logic and setting OR to a low logic level on the high-to-low transition of a low-active pulse.

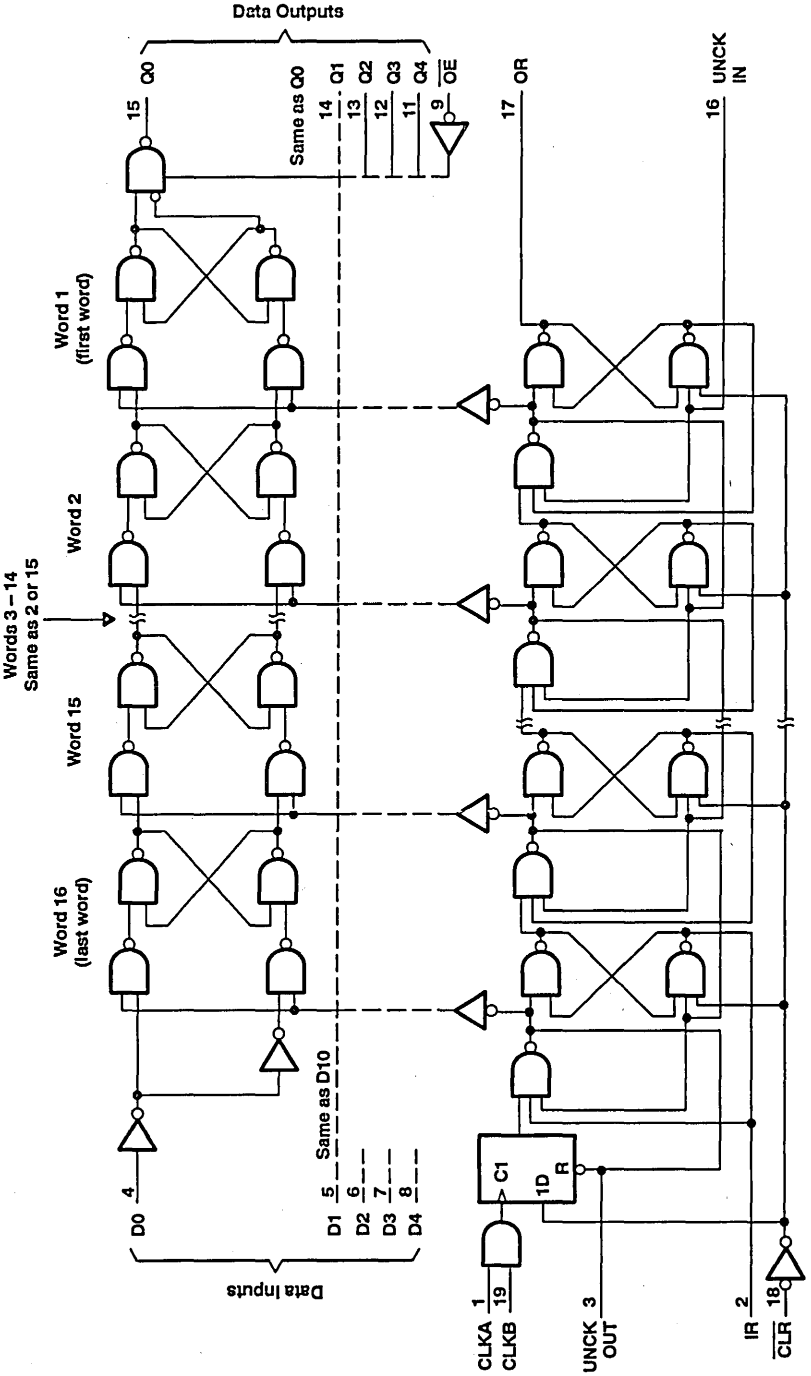
The SN74S225 is characterized for operation from 0°C to 70°C.

logic symbol†

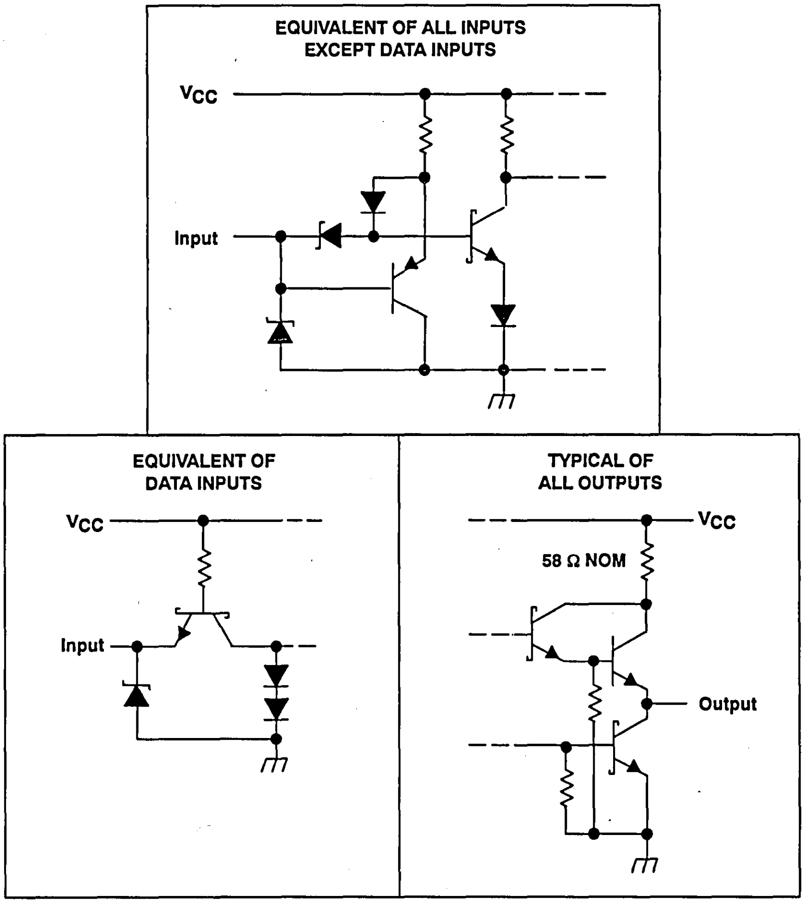


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range, T_A	0°C to 70°
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−6.5	mA
		All other outputs			−3.2	
I_{OL}	Low-level output current	Q outputs			16	mA
		All other outputs			8	
t_w	Pulse duration	CLKA or CLKB high	25			ns
		UNCK IN low	7			
		$\overline{CLR}$ low	40			
t_{su}	Set up time before CLKA↑ or CLKB↑	Data (see Note 2)	−20			ns
		$\overline{CLR}$ inactive	25			
t_h	Hold time after CLKA↑ or CLKB↑		70			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 2: Data must be set up within 20 ns after the load clock positive transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.75 V,	I_{OL} = − 6.5 mA	2.4	2.9		V
	All others	V_{CC} = 4.75 V,	I_{OL} = −3.2 mA	2.4	2.9		
V_{OL}	Q outputs	V_{CC} = 4.75 V,	I_{OL} = 16 mA		0.35	0.5	V
	All others	V_{CC} = 4.75 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.4 V			50	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.5 V			−50	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}	Data	V_{CC} = 5.25 V,	V_I = 2.7 V			40	µA
	All others					25	
I_{IL}	Data	V_{CC} = 5.25 V,	V_I = 0.5 V			−1	mA
	All others					−0.25	
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0	−30		−100	mA
I_{CC}§		V_{CC} = 5.25 V			80	120	mA

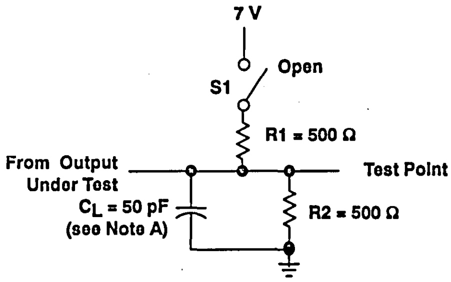
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Duration of the short circuit should not exceed one second.
§ I_{CC} is measured with all inputs grounded and the output open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

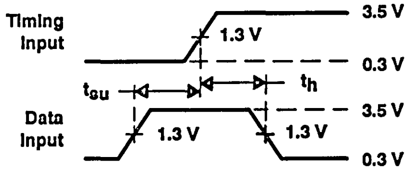
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	CLKA		C_L = 30 pF	10	20		MHz
	CLKB			10	20		
	UNCK IN			10	20		
t_w	UNCK OUT			7	14		ns
t_{dis}	$\overline{\text{OE}}$	Any Q	C_L = 5 pF		10	25	ns
t_{en}	$\overline{\text{OE}}$	Any Q	C_L = 30 pF		25	40	ns
t_{PLH}	UNCK IN	Any Q			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CLKA or CLKB	OR			190	300	ns
t_{PLH}	UNCK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{\text{CLR}}$	OR			35	60	ns
	CLKA or CLKB	UNCK OUT			25	45	
	UNCK IN				270	400	
	CLKA or CLKB	IR			55	75	
t_{PLH}	UNCK IN	IR			255	400	ns
	$\overline{\text{CLR}}$				16	35	
	OR↑	Any Q			10	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

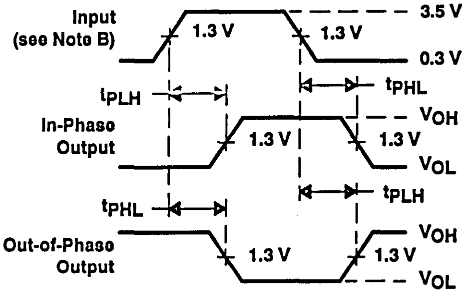
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS



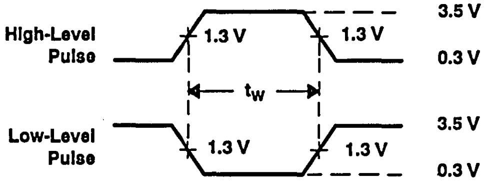
VOLTAGE WAVEFORMS
SET UP AND HOLD TIMES



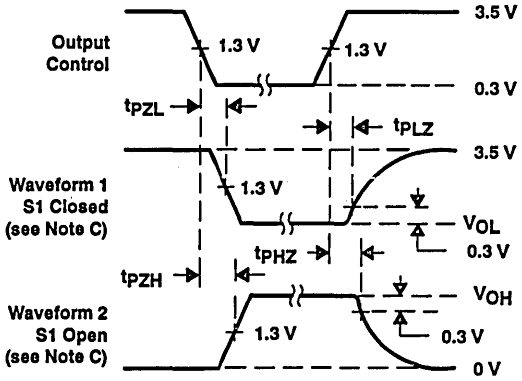
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

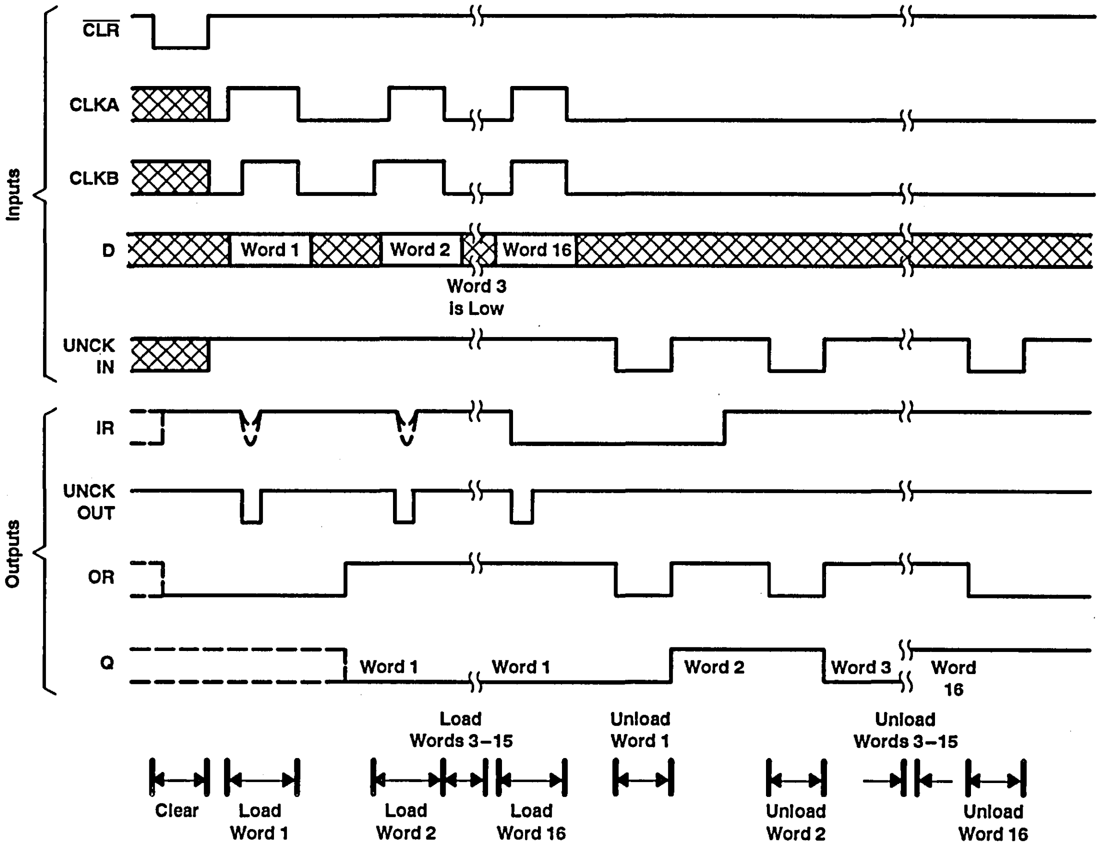


Figure 2. Typical Waveforms for a 16-Word FIFO

APPLICATION INFORMATION

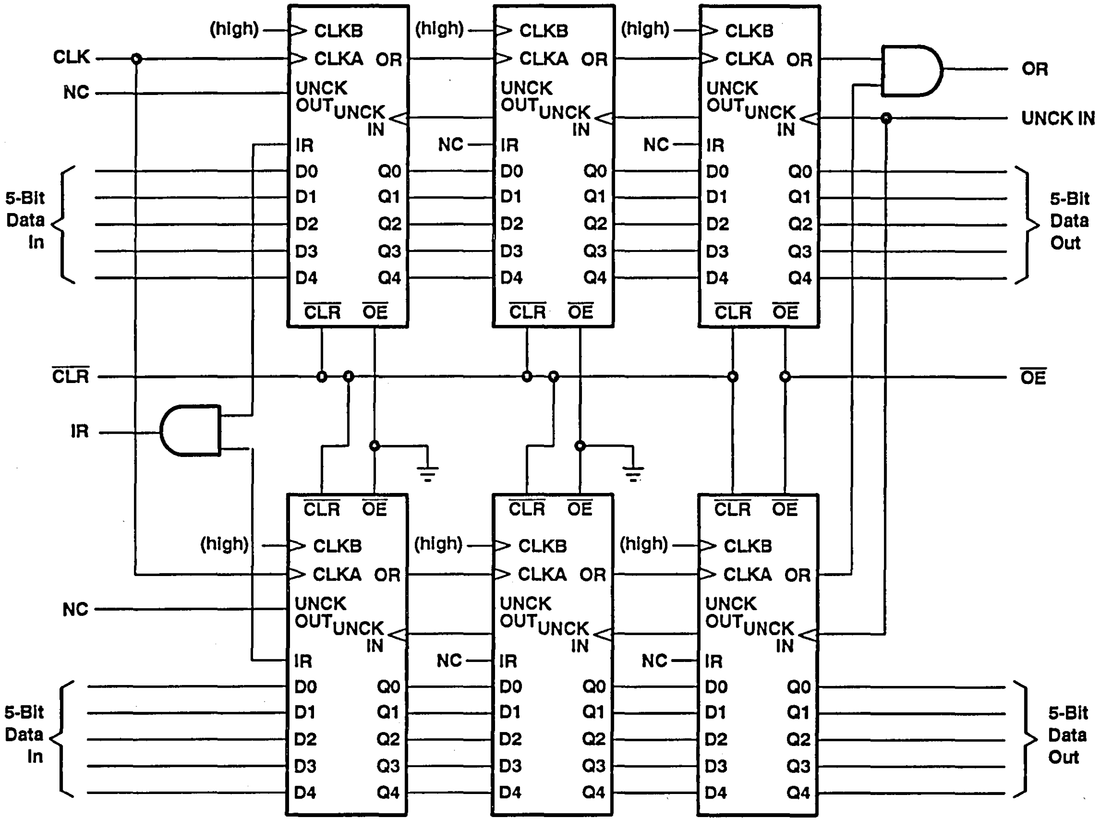


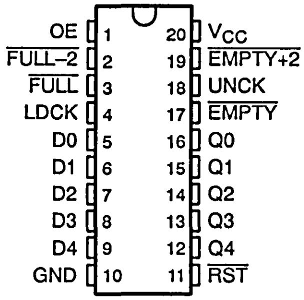
Figure 3. Expanding the SN74S225 FIFO (48 words of 10 bits shown)

SN74ALS229B
16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

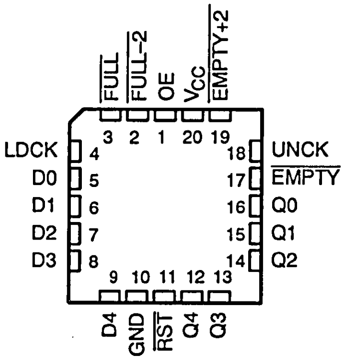
SCAS252 – MARCH 1990 – REVISED JUNE 1992

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 80-bit memory uses advanced low-power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

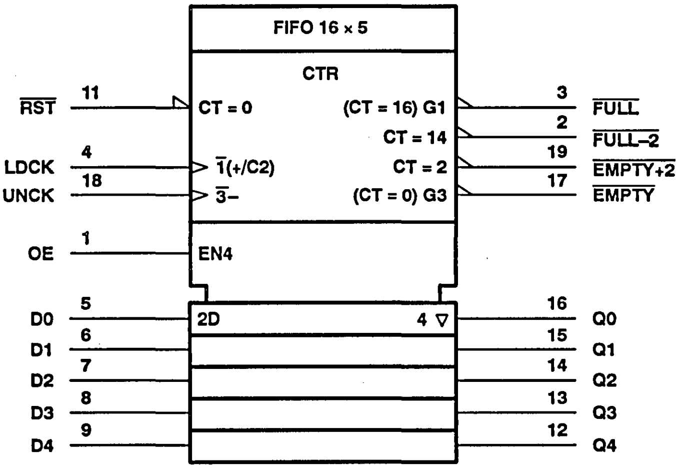
Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{FULL+2}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–2}}$ output is low when the memory contains 14 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+2}}$ output is low when two words remain in memory.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–2}}$, and $\overline{\text{EMPTY+2}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK after either a $\overline{\text{RST}}$ pulse or from an empty condition causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS229B is characterized for operation from 0°C to 70°C.

logic symbol†



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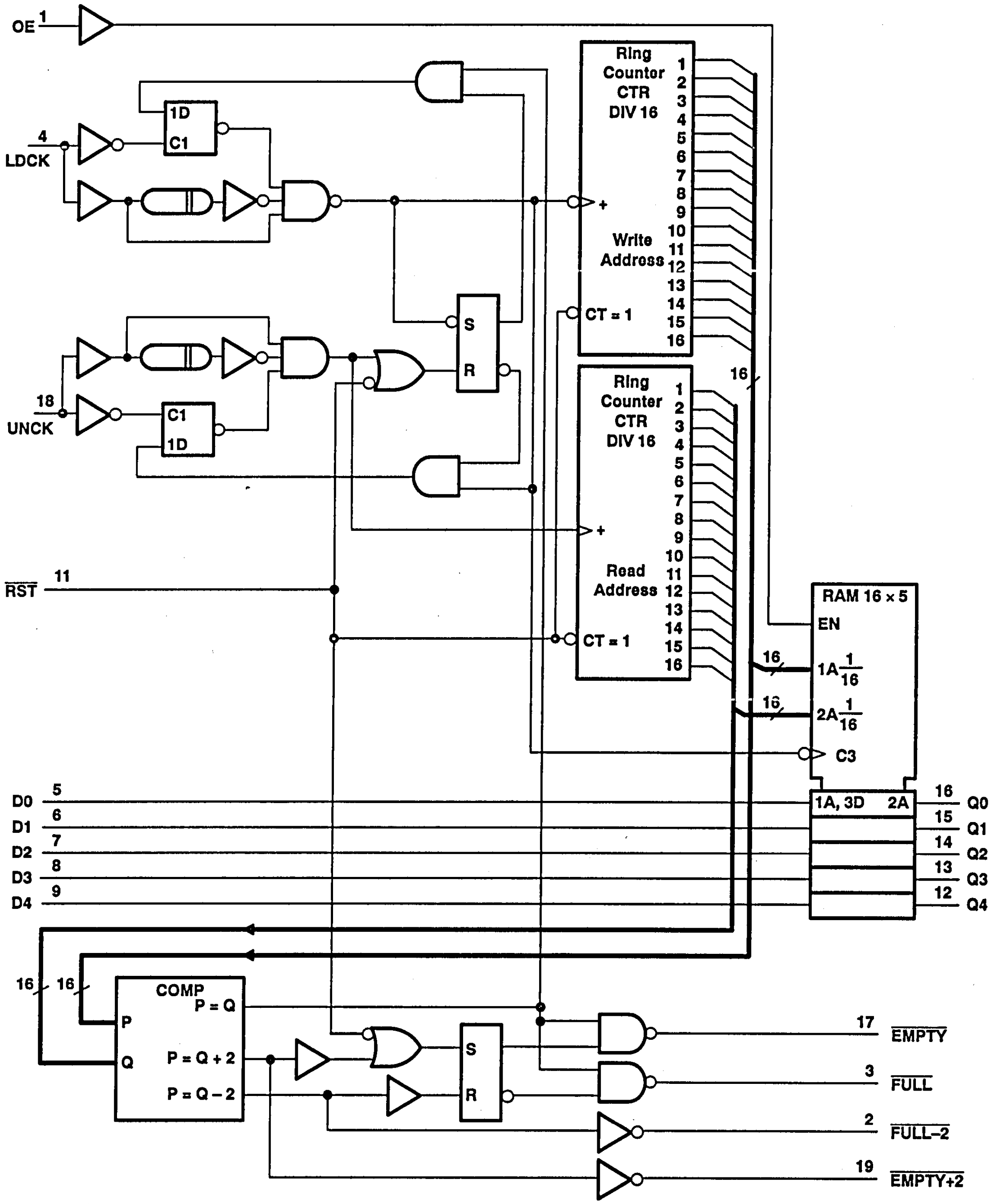
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

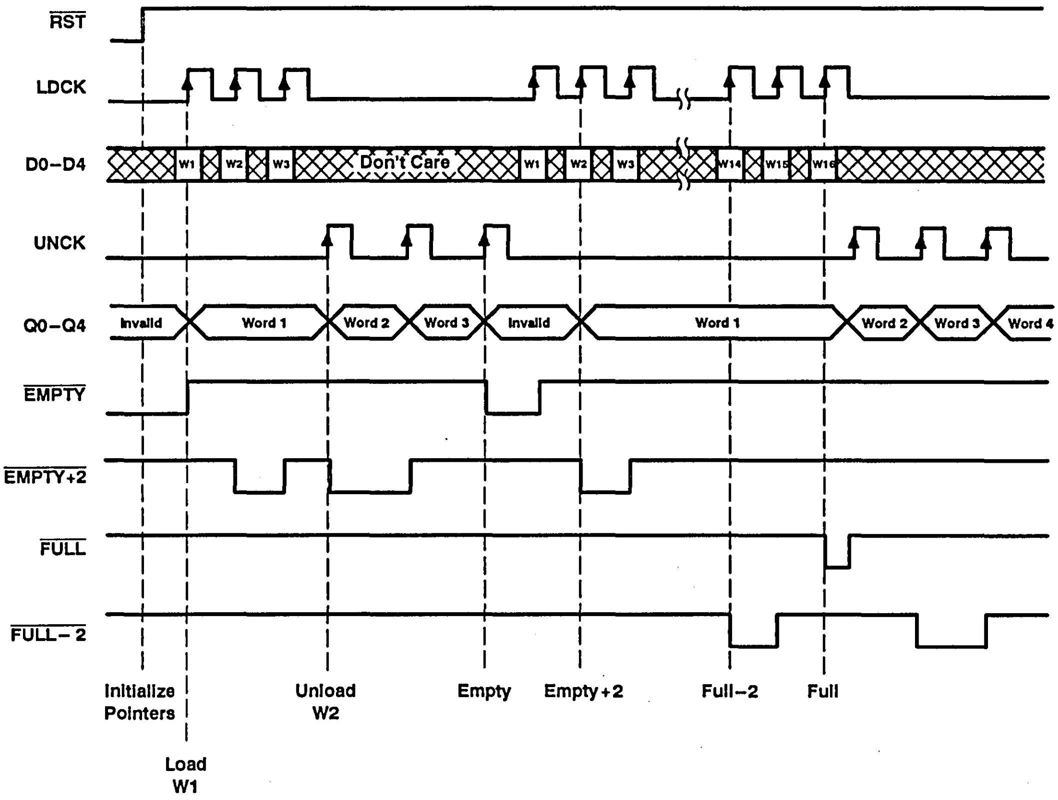
Pin numbers shown are for the DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for the DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−1.6	mA
		Status flags			−0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{\text{RST}}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{\text{RST}}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{\text{RST}}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = −2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OL} = −0.4 mA	V_{CC}−2			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			85	140	mA

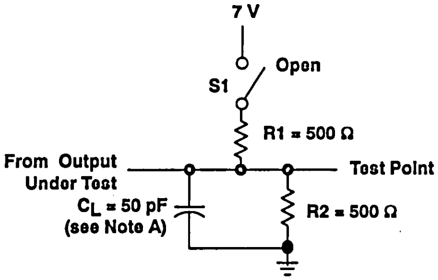
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
f_{max}	LDCK, UNCK		40		MHz
t_{pd}	LDCK↑	Any Q	6	30	ns
	UNCK↑		6	30	
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	5	25	ns
t_{PHL}	UNCK↑		6	27	
t_{PHL}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY}}$	5	26	ns
t_{pd}	LDCK↑	$\overline{\text{EMPTY+2}}$	7	33	ns
	UNCK↑		9	35	
t_{PLH}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY+2}}$	9	33	ns
t_{pd}	LDCK↑	$\overline{\text{FULL–2}}$	7	33	ns
	UNCK↑		9	35	
t_{PLH}	$\overline{\text{RST}}$↓	$\overline{\text{FULL–2}}$	9	33	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$	5	25	ns
	$\overline{\text{RST}}$↓		8	31	
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

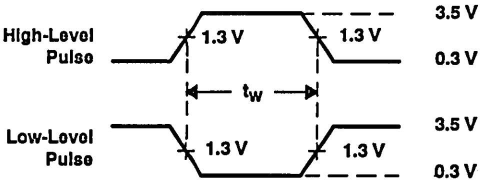
PARAMETER MEASUREMENT INFORMATION



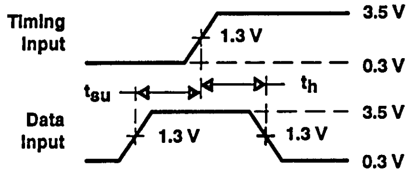
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

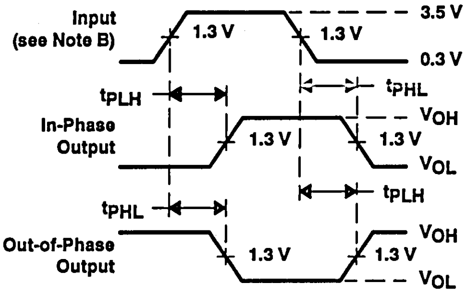
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



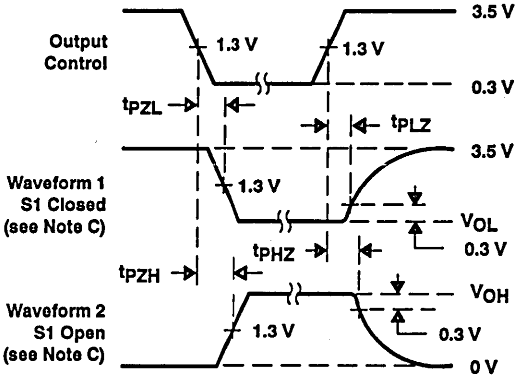
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

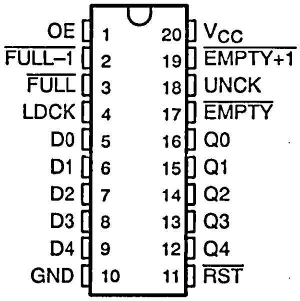
Figure 1. Load Circuit and Voltage Waveforms

SN74ALS233B
16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

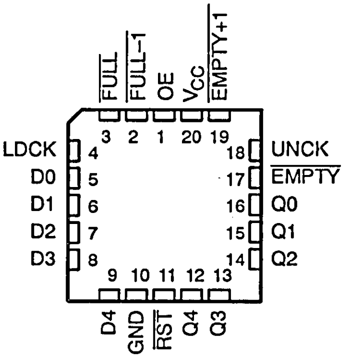
SCAS253 – MARCH 1990 – REVISED JUNE 1992

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **Data Rates From 0 to 40 MHz**
- **Fall-Through Time . . . 14 ns Typ**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

This 80-bit memory uses advanced low-power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

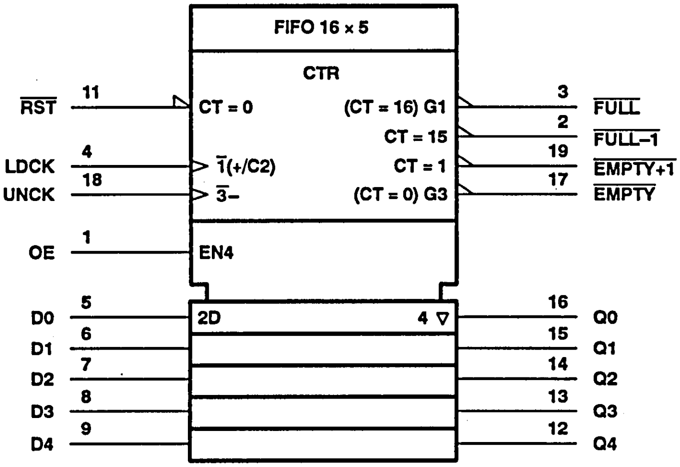
Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{EMPTY+1}}$ output flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when it is not full. The $\overline{\text{FULL–1}}$ output is low when the memory contains 15 data words. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The $\overline{\text{EMPTY+1}}$ output is low when one word remains in memory.

A low level on the reset ($\overline{\text{RST}}$) input resets the internal stack control pointers and also sets $\overline{\text{EMPTY}}$ low and sets $\overline{\text{FULL}}$, $\overline{\text{FULL–1}}$, and $\overline{\text{EMPTY+1}}$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a $\overline{\text{RST}}$ pulse or from an empty condition, causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS233B is characterized for operation from 0°C to 70°C.

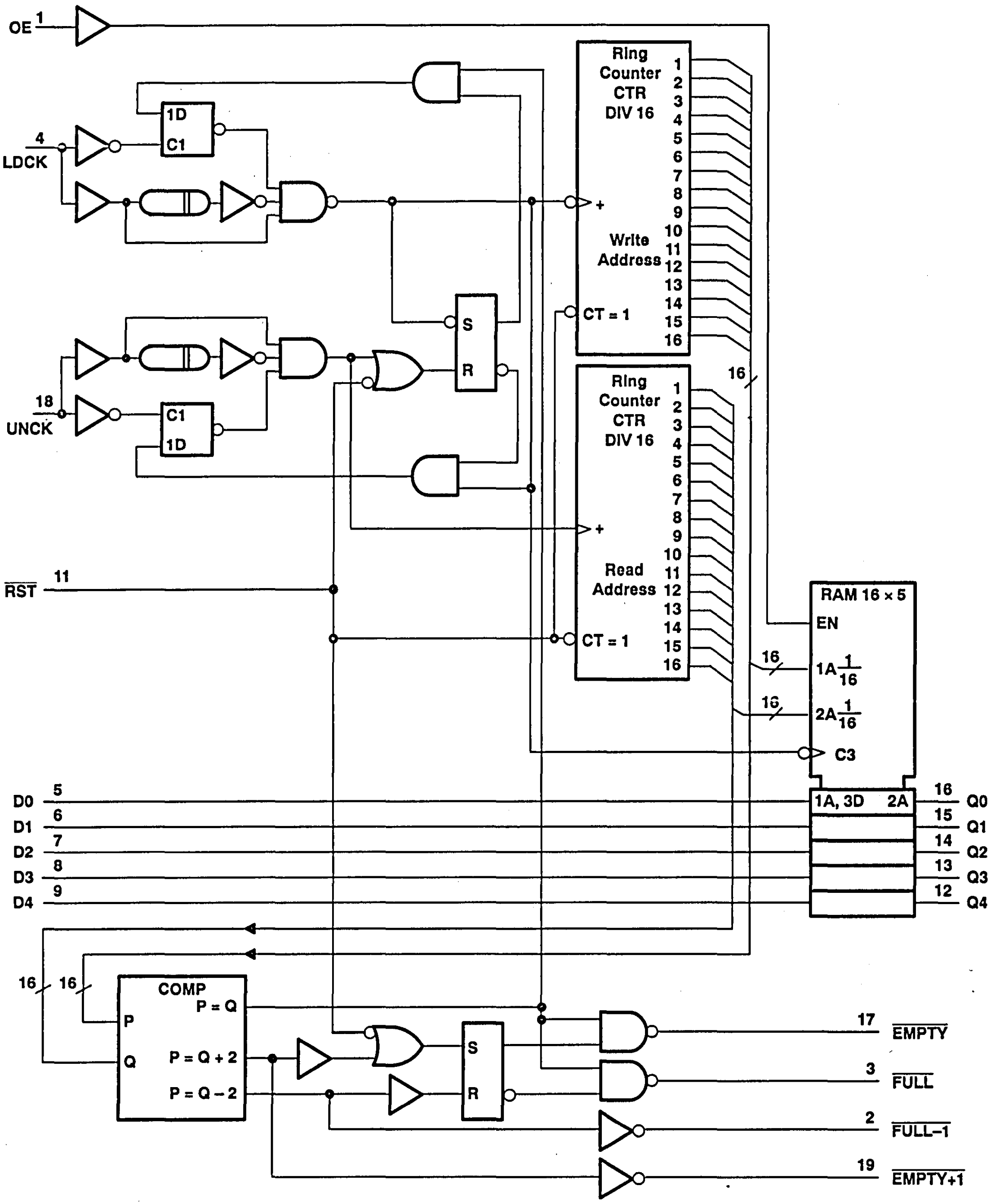
logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

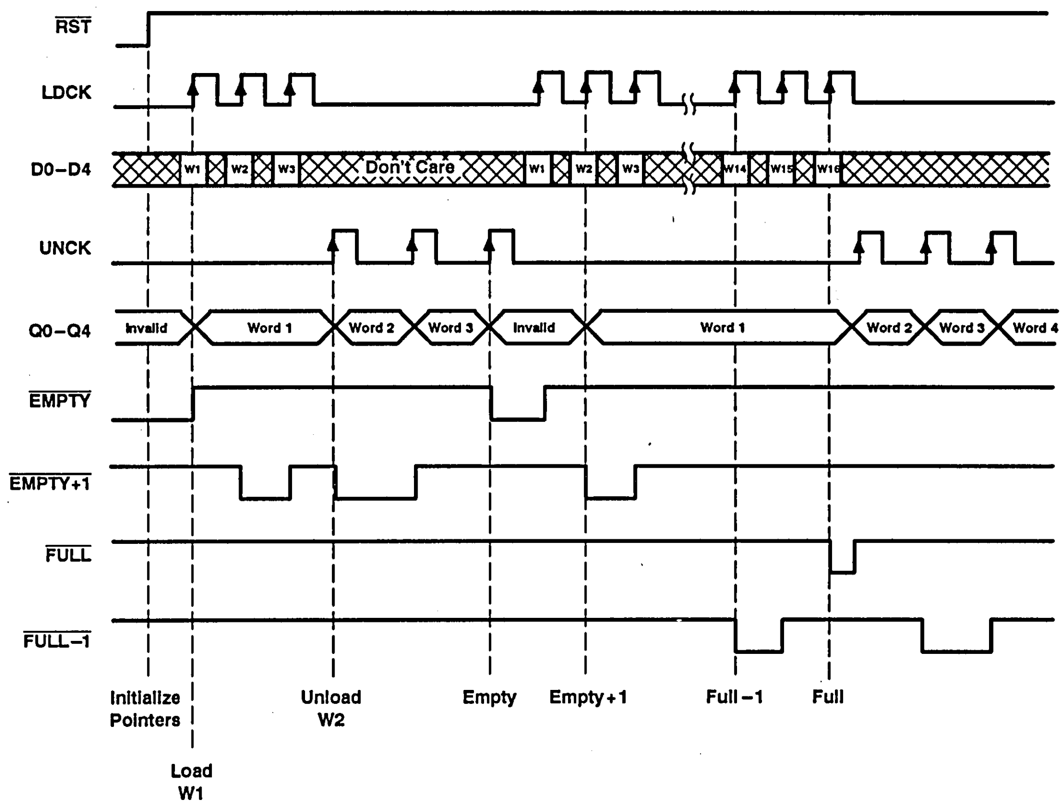
Pin numbers shown are for the DW and N packages.

logic diagram (positive logic)



Pin numbers shown are for the DW and N packages.

timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			–1.6	mA
		Status flags			–0.4	
I_{OL}	Low-level output current	Q outputs			24	mA
		Status flags			8	
f_{clock}	Clock frequency	LDCK	0		40	MHz
		UNCK	0		40	
t_w	Pulse duration	$\overline{RST}$ low	18			ns
		LDCK low	15			
		LDCK high	10			
		UNCK low	15			
		UNCK high	10			
t_{su}	Setup time	Data before LDCK↑	8			ns
		$\overline{RST}$ (inactive) before LDCK↑	5			
		LDCK (inactive) before $\overline{RST}$↑	5			
t_h	Hold time	Data after LDCK↑	5			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

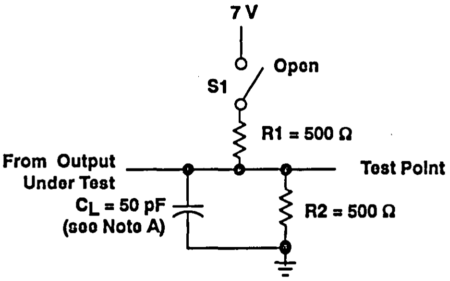
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	Q outputs	V_{CC} = 4.5 V,	I_{OH} = – 2.6 mA	2.4	3.2		V
	Status flags	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			
V_{OL}	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
	Status flags	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V			88	133	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
f_{max}	LDCK, UNCK		40		MHz
t_{pd}	LDCK↑	Any Q	6	32	ns
	UNCK↑		6	30	
t_{PLH}	LDCK↑	$\overline{\text{EMPTY}}$	5	25	ns
t_{PHL}	UNCK↑		6	27	
t_{PHL}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY}}$	5	25	ns
t_{pd}	LDCK↑	$\overline{\text{EMPTY+1}}$	7	34	ns
	UNCK↑		7	34	
t_{PLH}	$\overline{\text{RST}}$↓	$\overline{\text{EMPTY+1}}$	8	31	ns
t_{pd}	LDCK↑	$\overline{\text{FULL−1}}$	9	33	ns
	UNCK↑		8	32	
t_{PLH}	$\overline{\text{RST}}$↓	$\overline{\text{FULL−1}}$	11	32	ns
t_{PHL}	LDCK↑	$\overline{\text{FULL}}$	6	27	ns
t_{PLH}	UNCK↑	$\overline{\text{FULL}}$	5	25	ns
	$\overline{\text{RST}}$↓		9	30	
t_{en}	OE↑	Q	2	15	ns
t_{dis}	OE↓	Q	1	15	ns

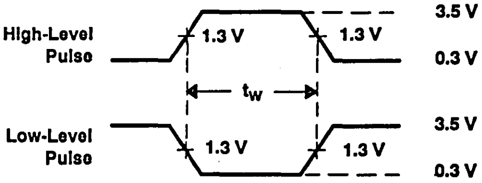
PARAMETER MEASUREMENT INFORMATION



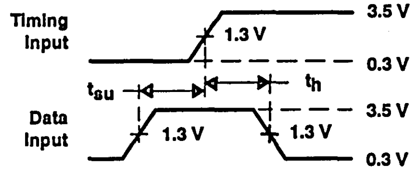
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

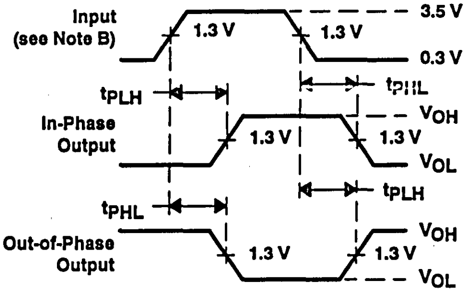
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



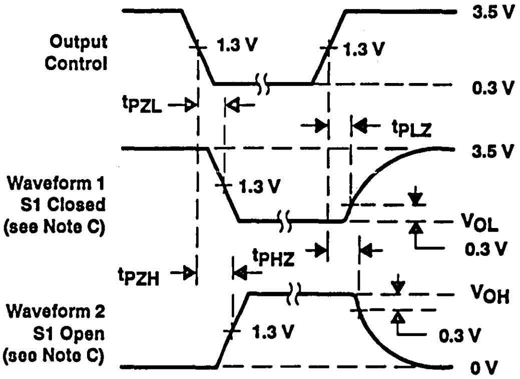
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

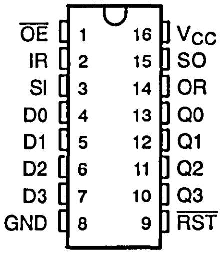
Figure 1. Load Circuit and Voltage Waveforms

SN74ALS234
64 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

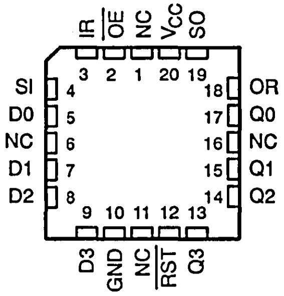
SDAS106B – OCTOBER 1986 – REVISED SEPTEMBER 1993

- Asynchronous Operation
- Organized as 64 Words by 4 Bits
- Data Rates From 0 to 30 MHz
- 3-State Outputs
- Package Options Include Plastic Small-Outline Packages (DW), Plastic J-Leaded Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74ALS234 is a 256-bit memory utilizing advanced low-power Schottky IMPACT™ technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALS234 is designed to process data at rates from 0 to 30 MHz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the shift-in (SI) input. When SI goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional shift-in pulses have no effect. Data is shifted out of memory on the falling edge of the shift-out (SO) input (see Figure 2). When the FIFO is empty, additional SO pulses have no effect. The last data word remains at the outputs until a new word falls through or reset ($\overline{\text{RST}}$) goes low.

Status of the SN74ALS234 FIFO memory is monitored by the output-ready (OR) and input-ready (IR) flags. When OR is high, valid data is available at the outputs. OR is low when SO is high and stays low when the FIFO is empty. IR is high when the inputs are ready to receive more data. IR is low when SI is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when SI goes low. If SO is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding SI high and taking SO low. One propagation delay after SO goes low, IR will go high. If SI is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and SI is high, only a high-level pulse is seen on the IR output (see Figure 4).

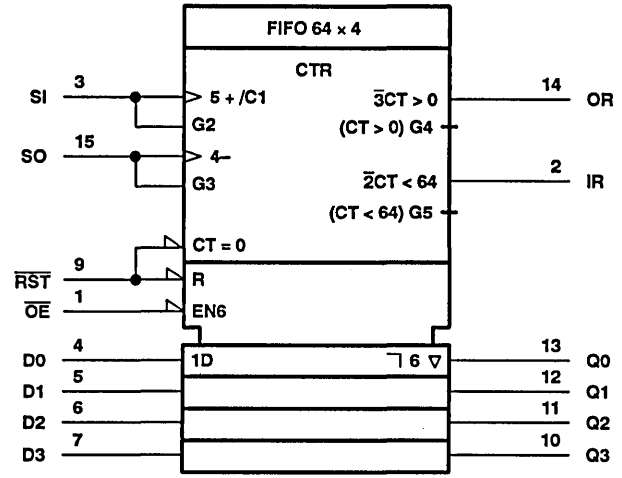
The FIFO must be reset after power up with a low-level pulse on the master reset ($\overline{\text{RST}}$) input. This sets IR high and OR low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If SI is high when $\overline{\text{RST}}$ goes high, the input data is shifted in and IR goes low and remains low until SI goes low. If SI goes low before $\overline{\text{RST}}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable ($\overline{\text{OE}}$) input is high. $\overline{\text{OE}}$ does not affect the IR or OR.

The SN74ALS234 is characterized for operation from 0°C to 70°C.

IMPACT is a trademark of Texas Instruments Incorporated.

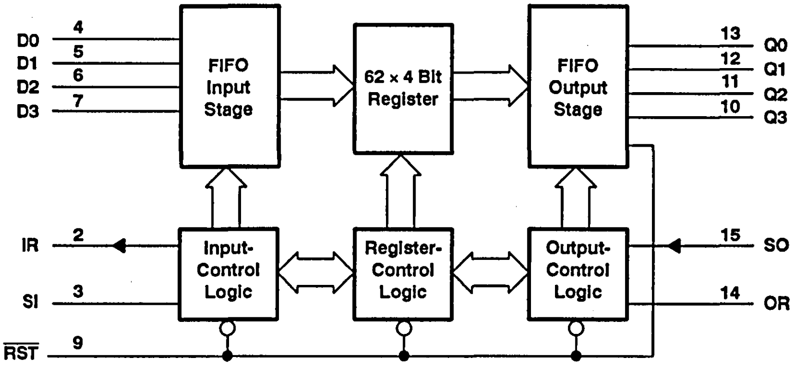
TEXAS INSTRUMENTS

logic symbol†



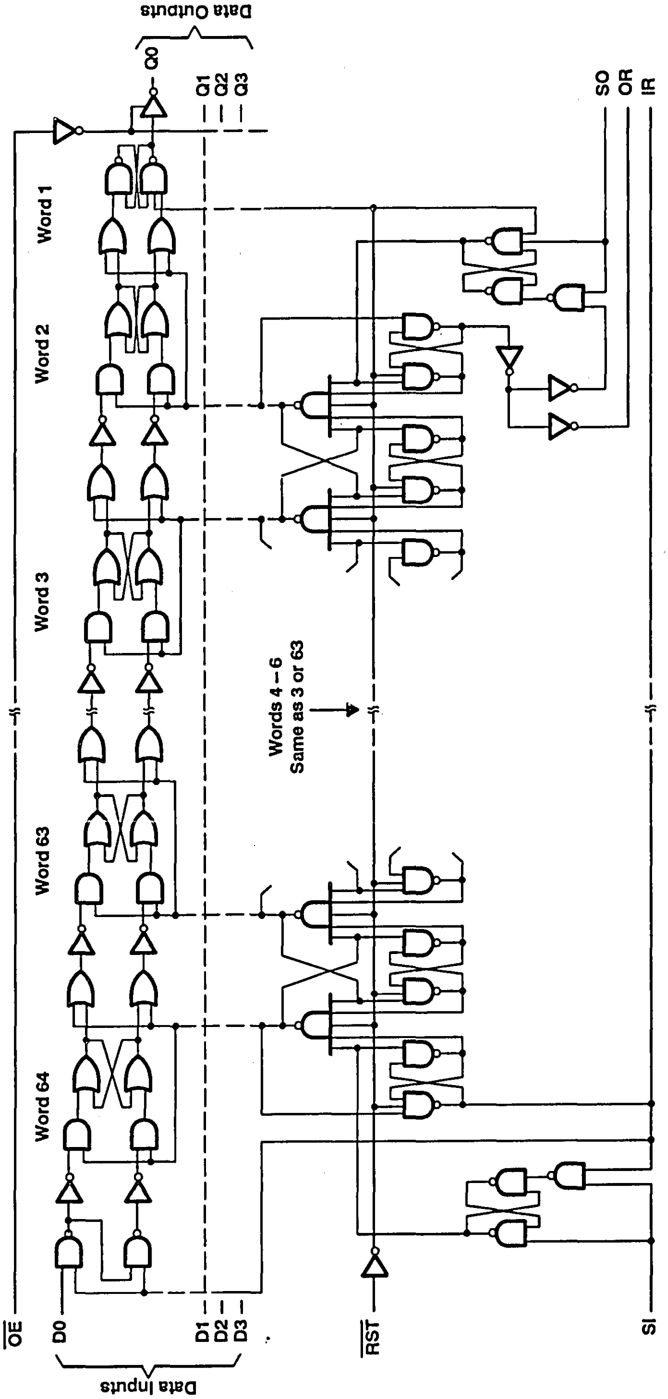
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram

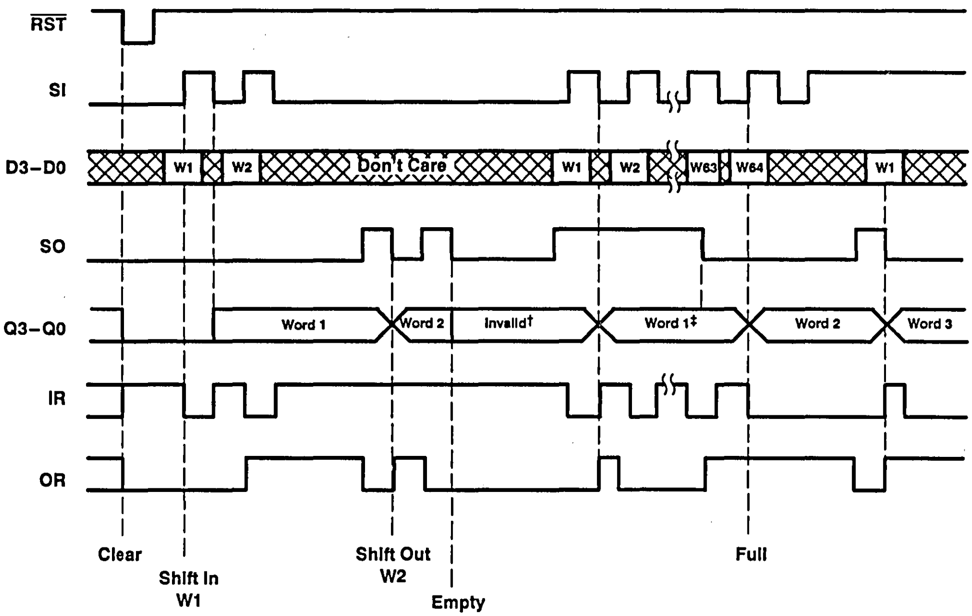


Pin numbers shown are for the DW and N packages.

logic diagram (positive logic)

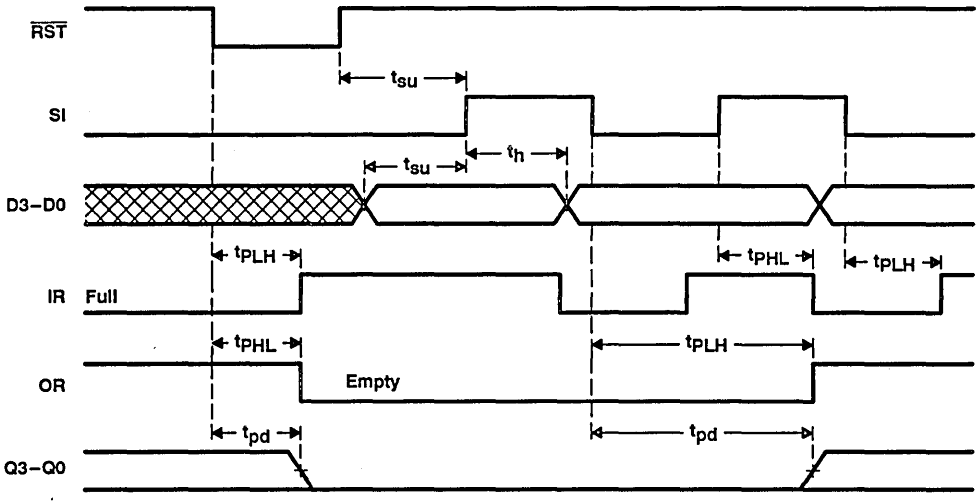


timing diagram



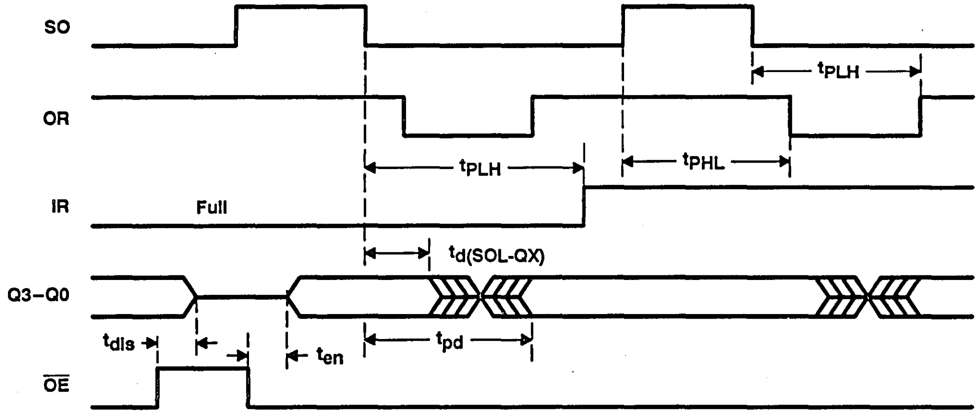
† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{\text{RST}}$ pulse clears the FIFO.

‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the outputs. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SO is taken low.



NOTE: SO is low.

Figure 1. Master Reset and Data-In Waveforms



NOTE: SI is low.

Figure 2. Data-Out Waveforms

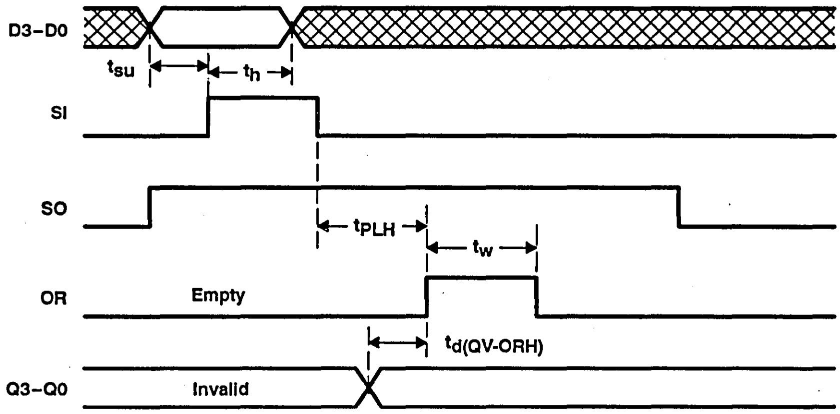


Figure 3. Data Fall-Through Waveforms

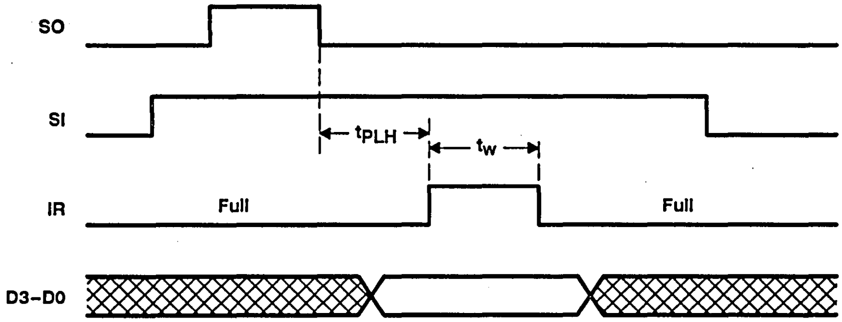


Figure 4. Automatic Data-In Waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current	Q outputs				−2.6	mA
		IR and OR				−0.4	
I_{OL}	Low-level output current	Q outputs				24	mA
		IR and OR				8	
f_{clock}	Clock frequency	SI or SO		0		30	MHz
t_w	Pulse duration	SI or SO	High or low	15			ns
		$\overline{RST}$	Low	15			
t_{su}	Setup time before SI↑	Data		0			ns
		$\overline{RST}$	High (inactive)	15			
t_h	Hold time, data after SI↑			17			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	Any Q	V_{CC} = 4.5 V	I_{OH} = −1 mA				V
			I_{OH} = −2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = −0.4 mA	2.7	3.4		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Low		100	145	mA
			High		97	142	
			Disabled		103	148	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

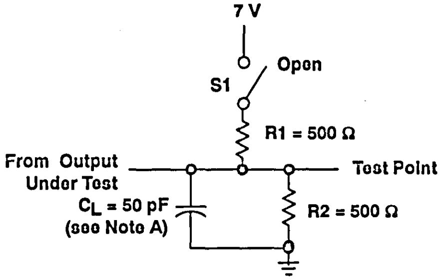
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SI			35		30		MHz
	SO			35		30		
t_w‡	IR high			15		8		ns
t_w§	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR↑			6	9	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SO↓			13		4		ns
t_{pd}	SI↓	Q		600	800	350	1000	ns
t_{PHL}	SI↑	IR		20	26	8	30	ns
t_{PLH}	SI↓			16	21	6	25	
t_{PLH}¶	SI↓	OR		600	800	350	1000	ns
t_{pd}	SO↓	Q		13	17	4	22	ns
t_{PHL}	SO↑	OR		23	27	7	33	ns
t_{PLH}	SO↓			20	24	6	30	
t_{PLH}¶	SO↓	IR		600	800	350	1000	ns
t_{PHL}	RST↓	OR		22	26	10	34	ns
t_{PLH}		IR		17	21	6	27	
t_{PHL}	$\overline{\text{RST}}$↓	Q		14	17	5	19	ns
t_{dis}	$\overline{\text{OE}}$↑	Q		7	13	2	15	ns
t_{en}	$\overline{\text{OE}}$↓	Q		6	12	2	13	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ The IR output pulse occurs when the FIFO is full, SI is high, and SO is pulsed (see Figure 4).
§ The OR output pulse occurs when the FIFO is empty, SO is high, and SI is pulsed (see Figure 3).
¶ Data throughput or fall-through times

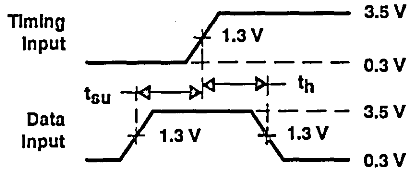
PARAMETER MEASUREMENT INFORMATION



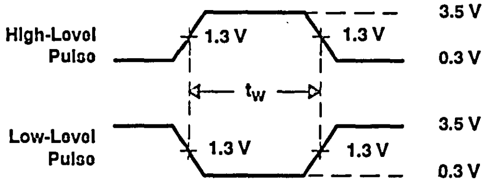
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

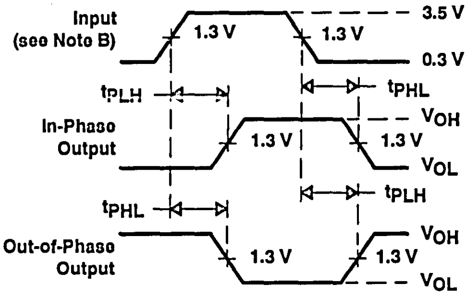
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



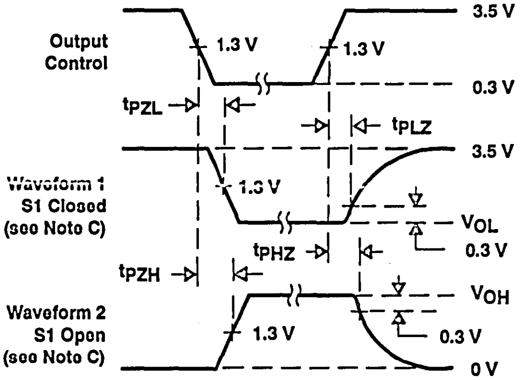
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 5. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

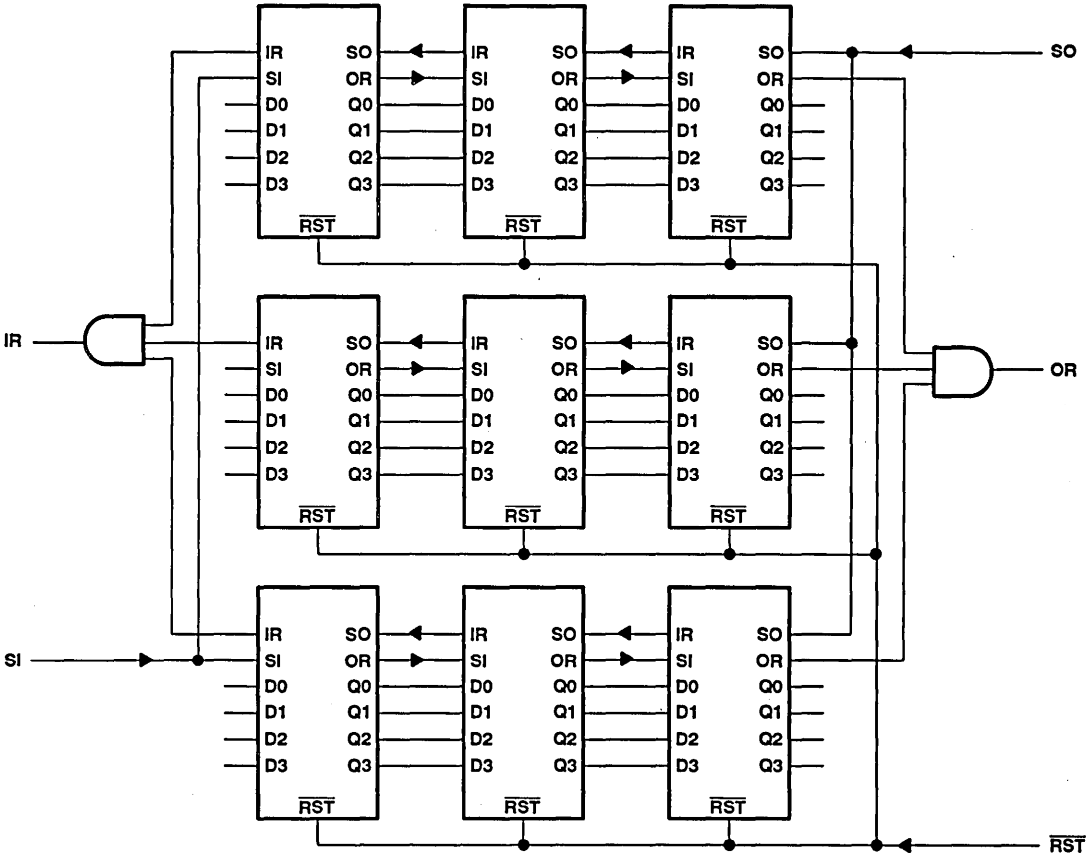


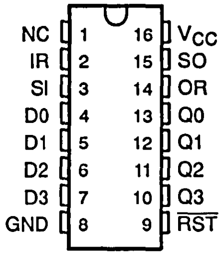
Figure 6. 192-Word by 12-Bit Expansion

SN74ALS236
64 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

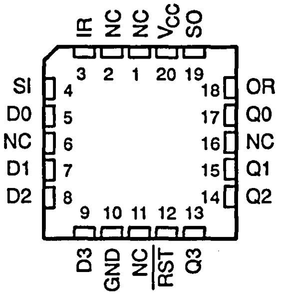
SDAS107A – OCTOBER 1986 – REVISED SEPTEMBER 1993

- **Asynchronous Operation**
- **Organized as 64 Words by 4 Bits**
- **Data Rates From 0 to 30 MHz**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic J-Leaded Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74ALS236 is a 256-bit memory utilizing advanced low-power Schottky IMPACT™ technology. It features high speed with fast fall-through times and is organized as 64 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALS236 is designed to process data at rates from 0 to 30 MHz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the shift-in (SI) input. When SI goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional shift-in pulses have no effect. Data is shifted out of memory on the falling edge of the shift-out (SO) input (see Figure 2). When the FIFO is empty, additional SO pulses have no effect. The last data word remains at the outputs until a new word falls through or reset ($\overline{\text{RST}}$) goes low.

Status of the SN74ALS236 FIFO memory is monitored by the output-ready (OR) and input-ready (IR) flags. When OR is high, valid data is available at the outputs. OR is low when SO is high and stays low when the FIFO is empty. IR is high when the inputs are ready to receive more data. IR is low when SI is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when SI goes low. If SO is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding SI high and taking SO low. One propagation delay after SO goes low, IR will go high. If SI is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and SI is high, only a high-level pulse is seen on the IR output (see Figure 4).

The FIFO must be reset after power up with a low-level pulse on the master reset ($\overline{\text{RST}}$) input. This sets IR high and OR low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If SI is high when $\overline{\text{RST}}$ goes high, the input data is shifted in and IR goes low and remains low until SI goes low. If SI goes low before $\overline{\text{RST}}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

The SN74ALS236 is characterized for operation from 0°C to 70°C.

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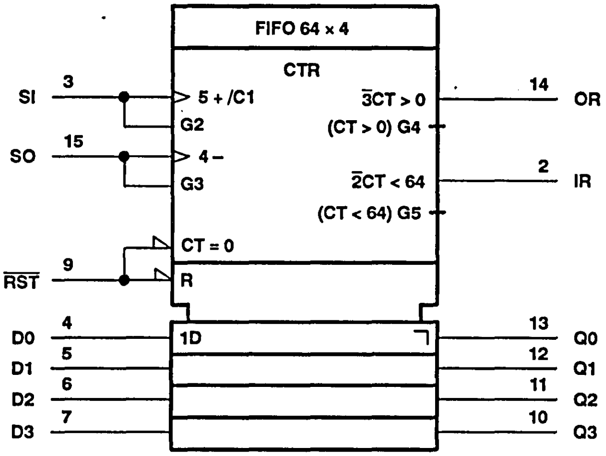
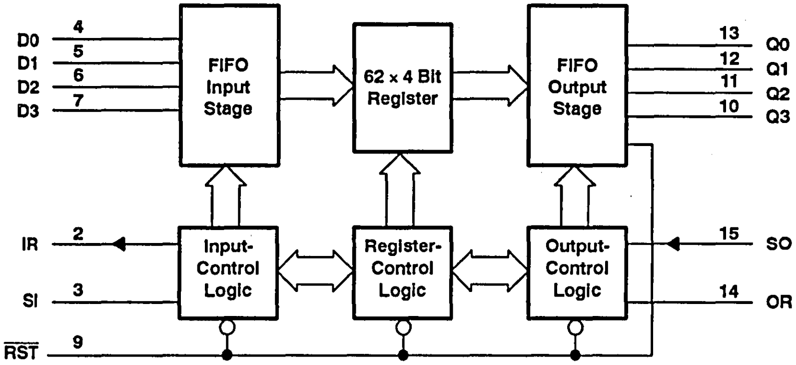
TEXAS INSTRUMENTS

logic symbol†



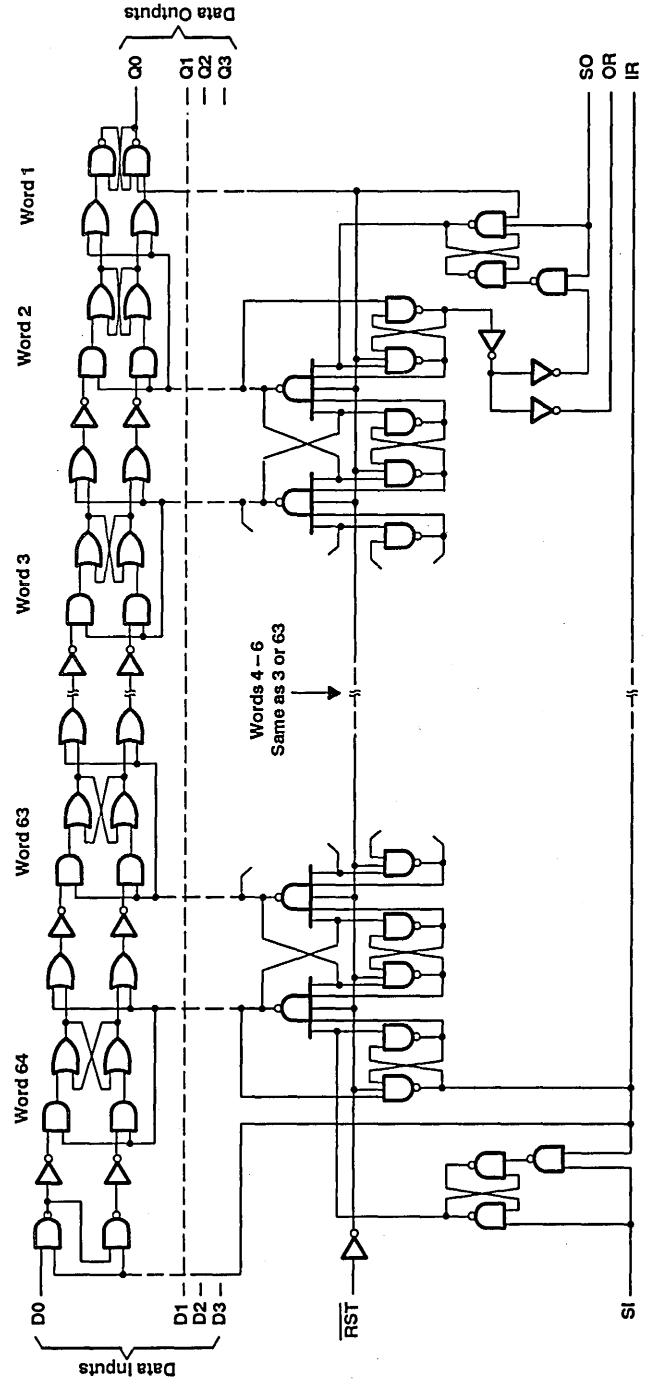
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram

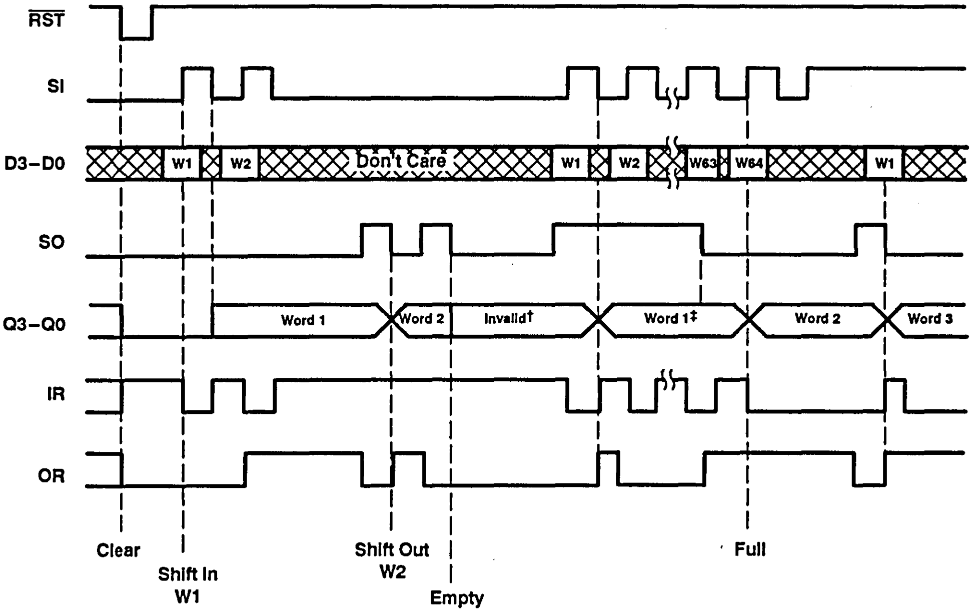


Pin numbers shown are for the DW and N packages.

logic diagram (positive logic)

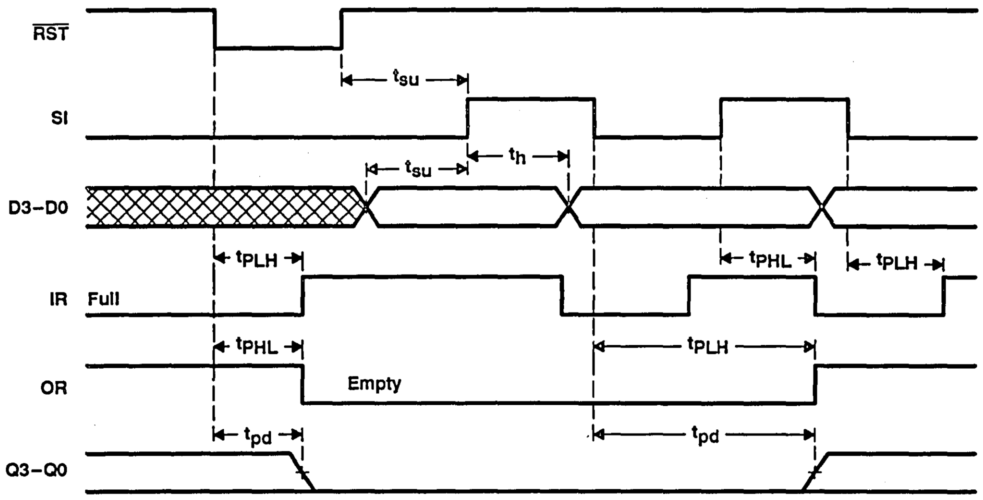


timing diagram



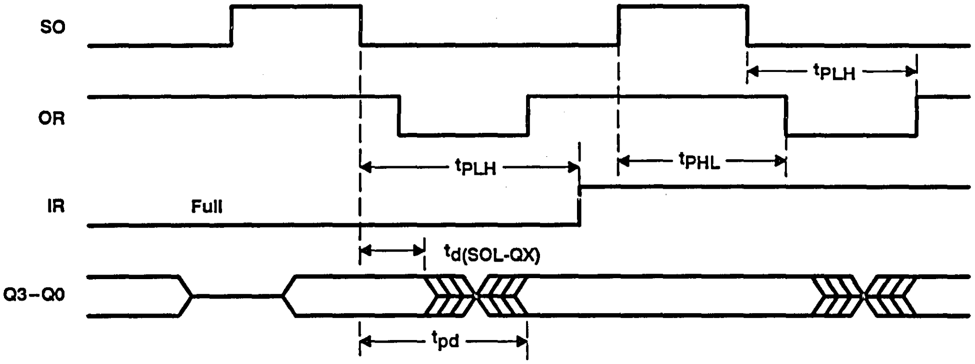
† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{RST}$ pulse clears the FIFO.

‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the outputs. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SO is taken low.



NOTE A: SO is low.

Figure 1. Master Reset and Data-In Waveforms



NOTE A: SI is low.

Figure 2. Data-Out Waveforms

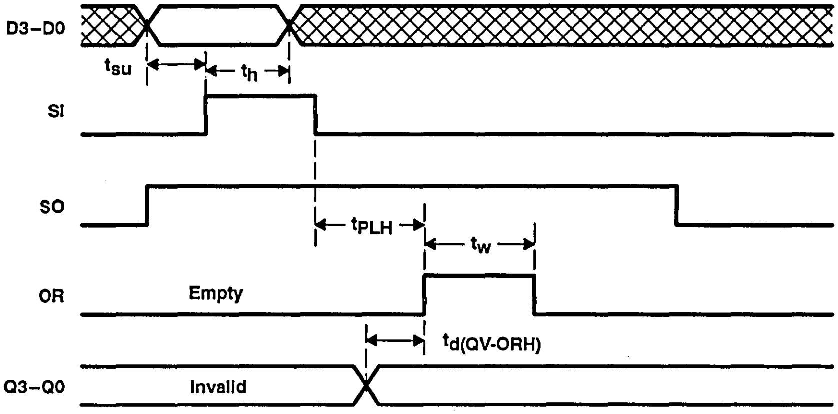


Figure 3. Data Fall-Through Waveforms

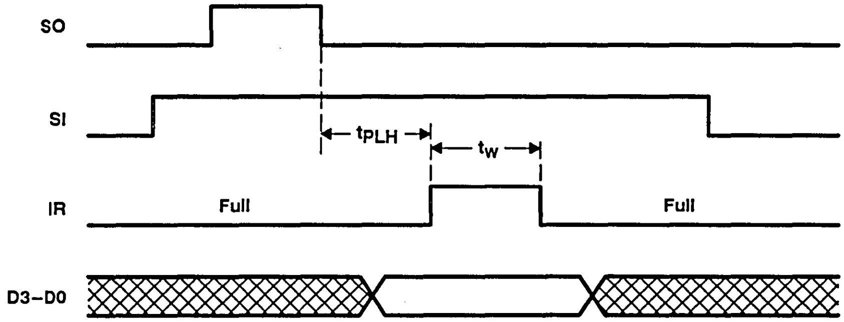


Figure 4. Automatic Data-In Waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A	0°C to 70°
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current	Q outputs				– 2.6	mA
		IR and OR				– 0.4	
I_{OL}	Low-level output current	Q outputs				24	mA
		IR and OR				8	
f_{clock}	Clock frequency	SI or SO		0		30	MHz
t_w	Pulse duration	SI or SO	High or low	15			ns
		$\overline{\text{RST}}$	Low	15			
t_{su}	Setup time before SI↑	Data		0			ns
		$\overline{\text{RST}}$	High (inactive)	15			
t_h	Hold time, data after SI↑			17			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	Any Q	V_{CC} = 4.5 V	I_{OH} = –1 mA				V
			I_{OH} = –2.6 mA	2.4	3.2		
	IR, OR	V_{CC} = 4.5 V,	I_{OH} = –0.4 mA	2.7	3.4		
V_{OL}	Any Q	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	IR, OR	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	
			I_{OL} = 8 mA		0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Low		100	145	mA
			High		97	142	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SI			35		30		MHz
	SO			35		30		
t_w‡	IR high			15		8		ns
t_w§	OR high			19		8		ns
$t_{d(QV\text{-}ORH)}$	Q valid before OR↑			6	9	−5	12	ns
$t_{d(SOL\text{-}QX)}$	Q valid after SO↓			13		4		ns
t_{pd}	SI↓	Q		600	800	350	1000	ns
t_{PHL}	SI↑	IR		20	26	8	30	ns
t_{PLH}	SI↓			16	21	6	25	
t_{PLH}#	SI↓	OR		600	800	350	1000	ns
t_{pd}	SO↓	Q		13	17	4	22	ns
t_{PHL}	SO↑	OR		23	27	7	33	ns
t_{PLH}	SO↓			20	24	6	30	
t_{PLH}#	SO↓	IR		600	800	350	1000	ns
t_{PHL}	RST↓	OR		22	26	10	34	ns
t_{PLH}		IR		17	21	6	27	
t_{PHL}	$\overline{RST}$↓	Q	14	14	17	5	19	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ The IR output pulse occurs when the FIFO is full, SI is high, and SO is pulsed (see Figure 4).
§ The OR output pulse occurs when the FIFO is empty, SO is high, and SI is pulsed (see Figure 3).
¶ Data throughput or fall-through times

APPLICATION INFORMATION

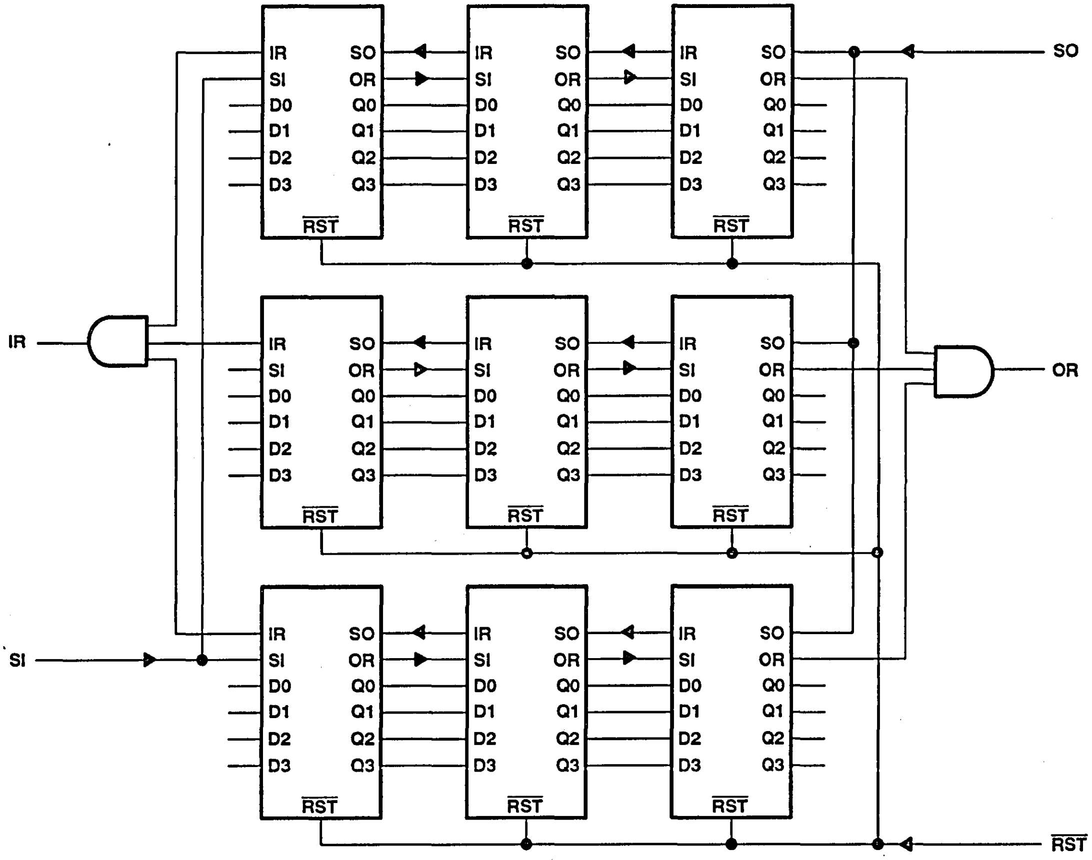
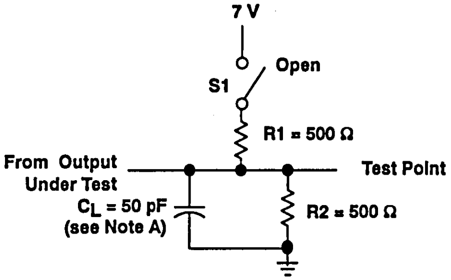


Figure 5. 192-Word by 12-Bit Expansion

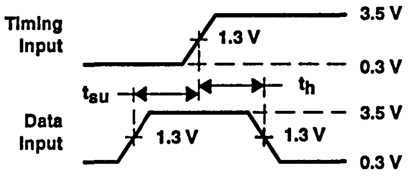
PARAMETER MEASUREMENT INFORMATION



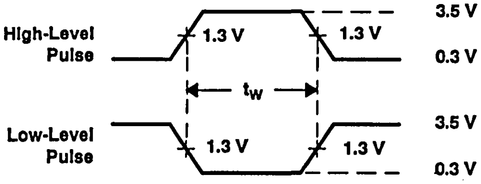
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

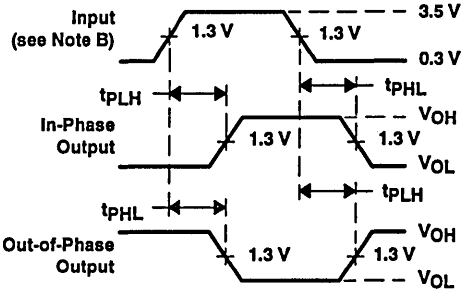
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



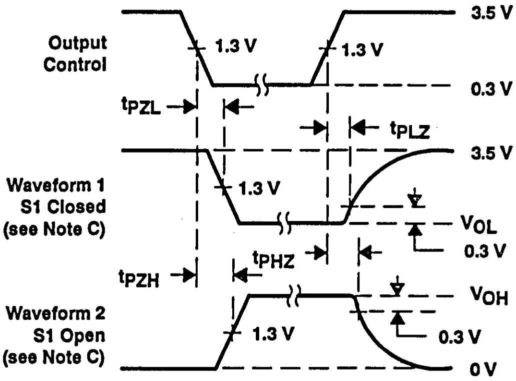
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, $t_r \le 2$ ns, $t_f \le 2$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

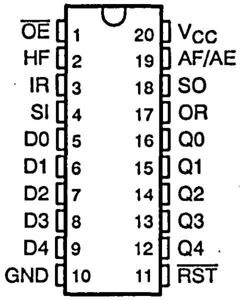
Figure 6. Load Circuit and Voltage Waveforms

SN74ALS235
64 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

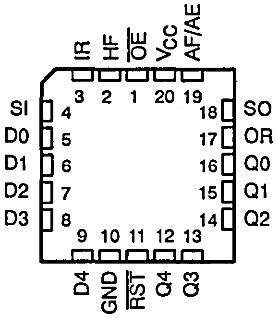
SDAS108A – OCTOBER 1986 – REVISED SEPTEMBER 1993

- **Asynchronous Operation**
- **Organized as 64 Words by 5 Bits**
- **Data Rates From 0 to 25 MHz**
- **3-State Outputs**
- **Package Options Include Plastic Small-Outline Packages (DW), Plastic J-Leaded Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The SN74ALS235 is a 320-bit memory utilizing advanced low-power Schottky IMPACT™ technology. It features high speed with fast fall-through times and is organized as 64 words by 5 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALS235 is designed to process data at rates from 0 to 25 MHz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the shift-in (SI) input. When SI goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional shift-in pulses have no effect. Data is shifted out of memory on the falling edge of the shift-out (SO) input (see Figure 2). When the FIFO is empty, additional SO pulses have no effect. The last data word remains at the outputs until a new word falls through or reset ($\overline{\mathrm{RST}}$) goes low.

Status of the SN74ALS235 FIFO memory is monitored by the output-ready (OR), input-ready (IR), almost-full/almost-empty (AF/AE), and half-full (HF) flags. When OR is high, valid data is available at the outputs. OR is low when SO is high and stays low when the FIFO is empty. IR is high when the inputs are ready to receive more data. IR is low when SI is high and stays low when the FIFO is full. AF/AE is high when the FIFO contains eight or less words (see Figure 5) or 56 or more words (see Figure 6). AF/AE is low when the FIFO contains between nine and 55 words. HF is high when the FIFO contains 32 or more words and is low when the FIFO contains 31 words or less (see Figure 7).

When the FIFO is empty, input data is shifted to the output automatically when SI goes low. If SO is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding SI high and taking SO low. One propagation delay after SO goes low, IR will go high. If SI is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and SI is high, only a high-level pulse is seen on the IR output.

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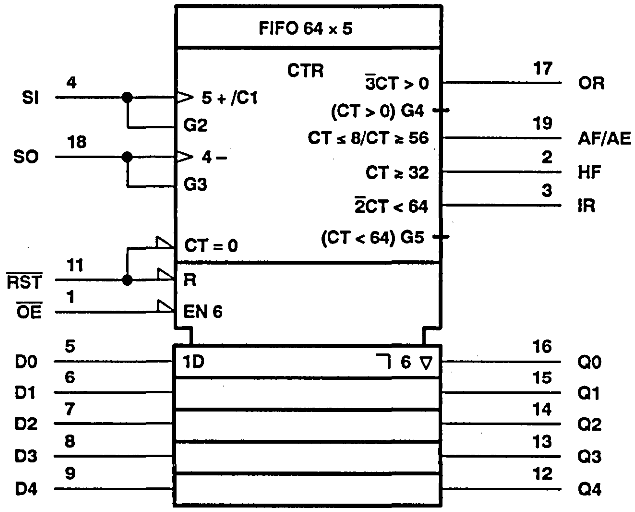
TEXAS INSTRUMENTS

description (continued)

The FIFO must be reset after power up with a low-level pulse on the master reset ($\overline{\text{RST}}$) input. This sets IR high and OR low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If SI is high when $\overline{\text{RST}}$ goes high, the input data is shifted in and IR goes low and remains low until SI goes low. If SI goes low before $\overline{\text{RST}}$ goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable ($\overline{\text{OE}}$) input is high. $\overline{\text{OE}}$ does not affect the status-flag outputs (see Figure 2).

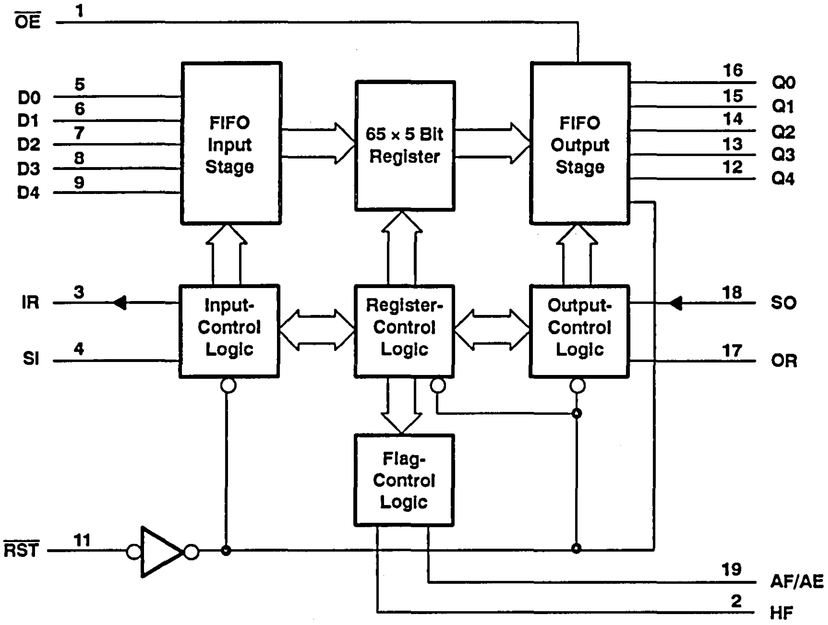
The SN74ALS235 is characterized for operation from 0°C to 70°C.

logic symbol†

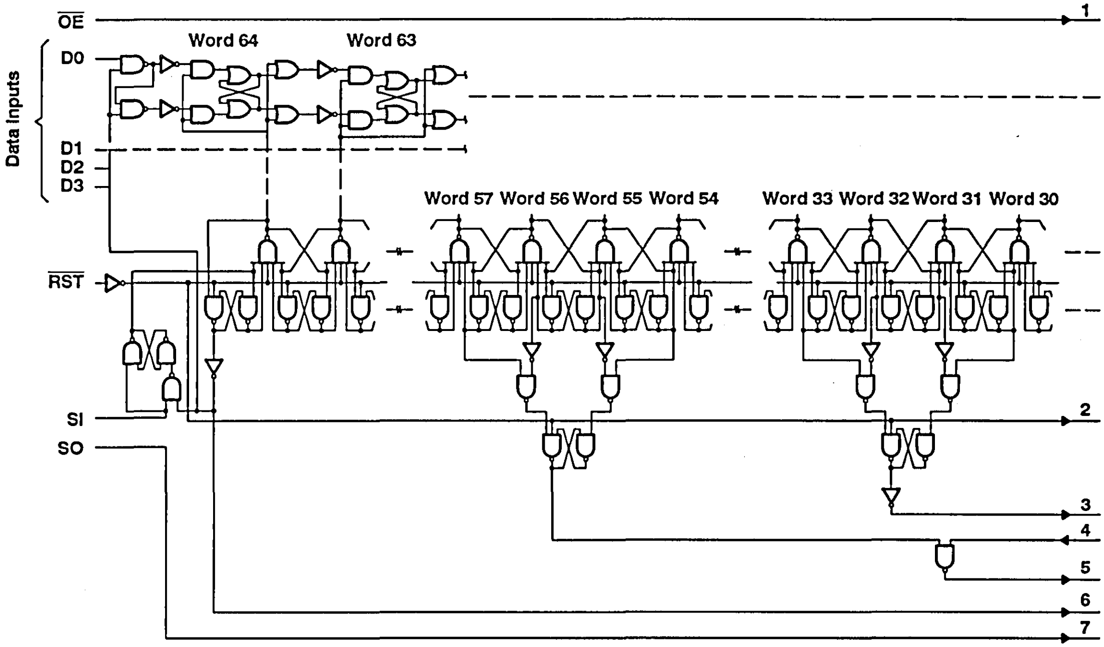


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram



logic diagram (positive logic)



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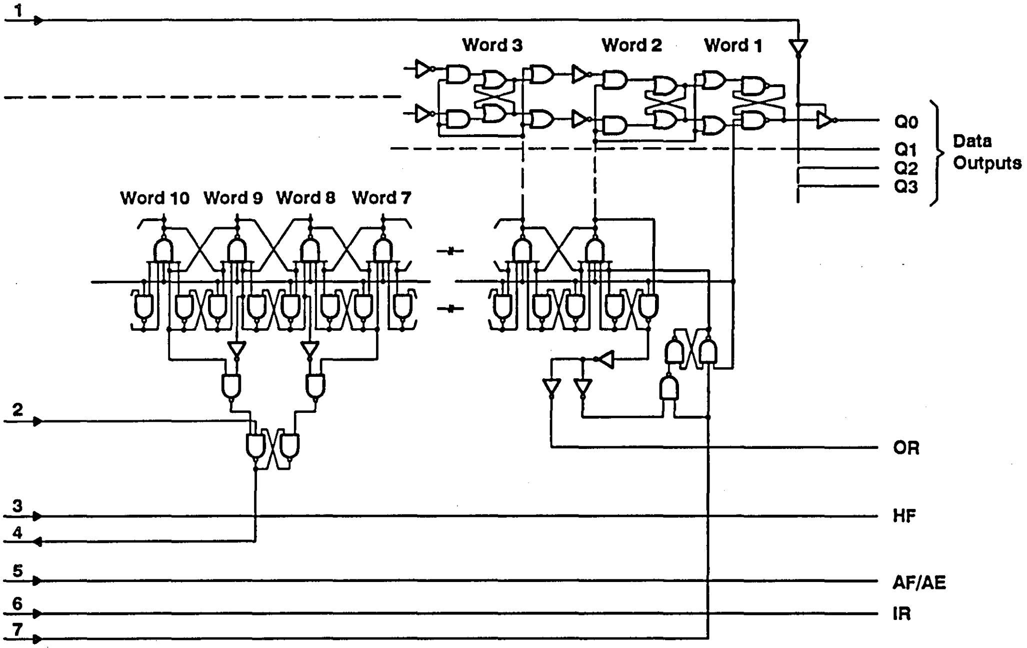
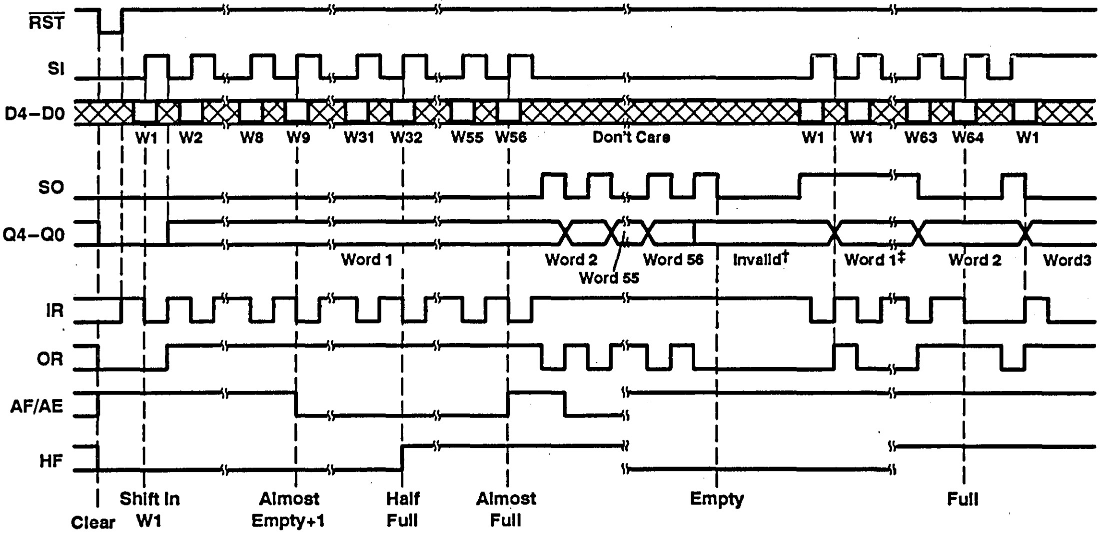
logic diagram (positive logic) (continued)



timing diagram



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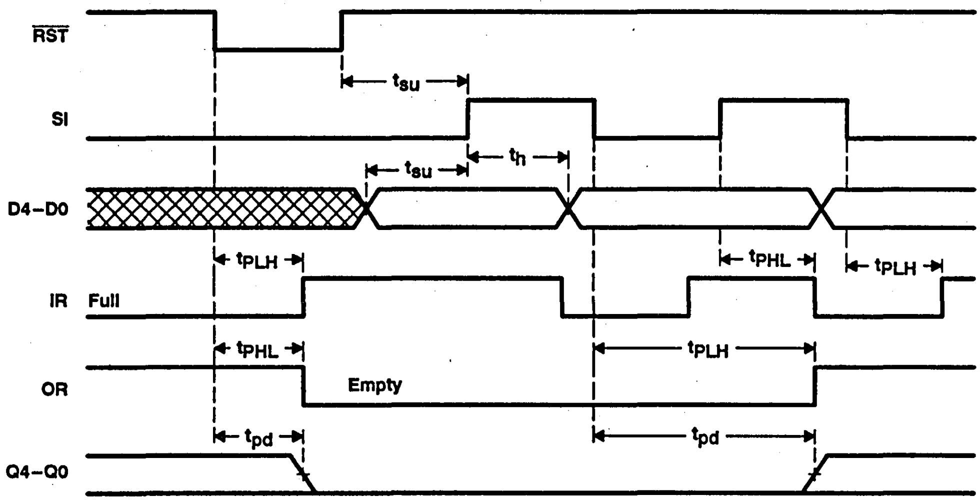
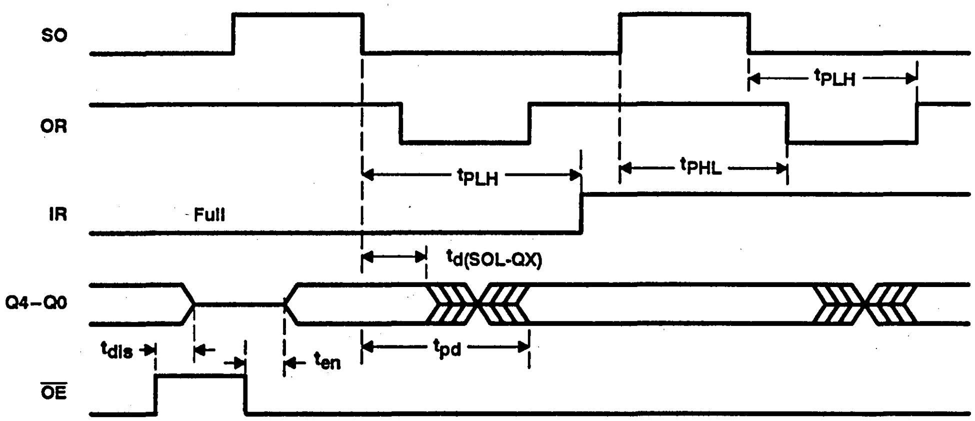
† The last data word shifted out of the FIFO remains at the output until a new word falls through or a $\overline{\text{RST}}$ pulse clears the FIFO.

‡ While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SO is taken low.



NOTE A: SO is low.

Figure 1. Master Reset and Data-In Waveforms



NOTE A: SI is low.

Figure 2. Data-Out Waveforms

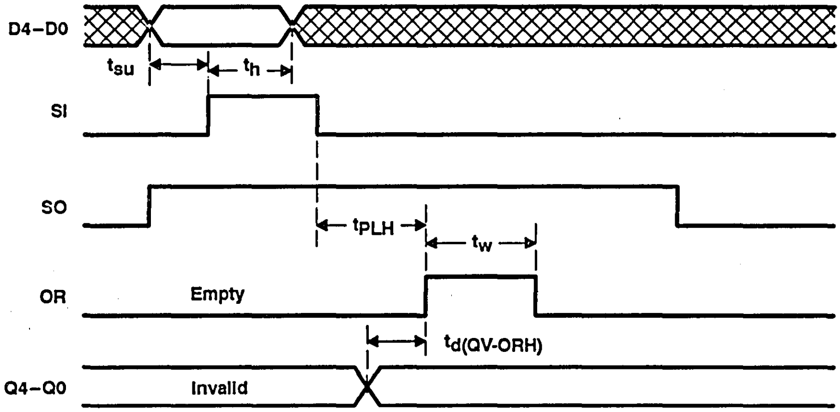


Figure 3. Data Fall-Through Waveforms

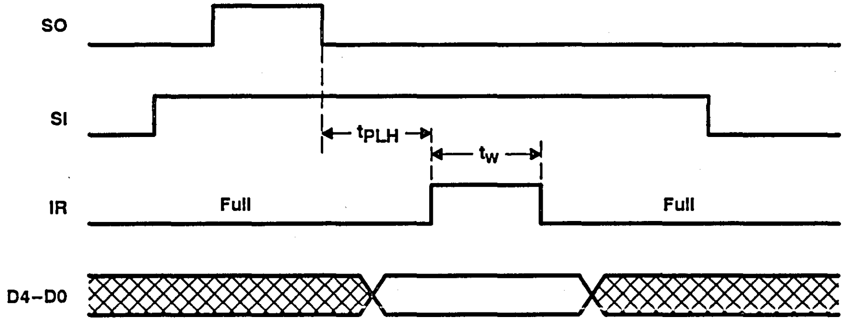


Figure 4. Automatic Data-In Waveforms

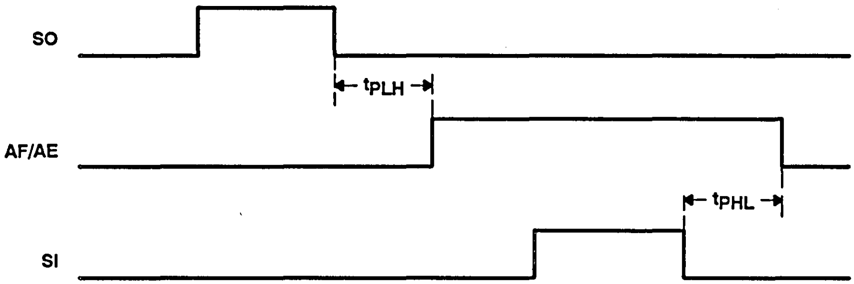


Figure 5. Almost-Empty Waveforms

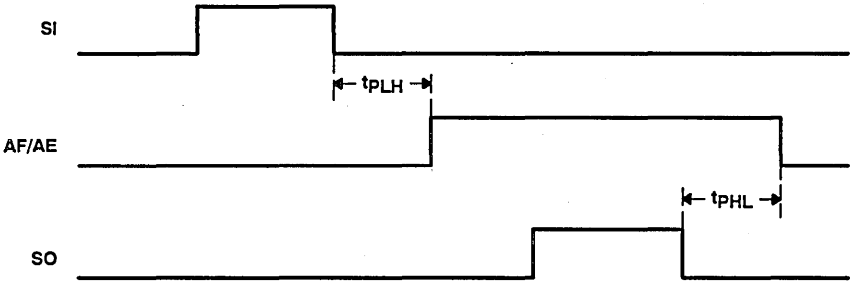


Figure 6. Almost-Full Waveforms

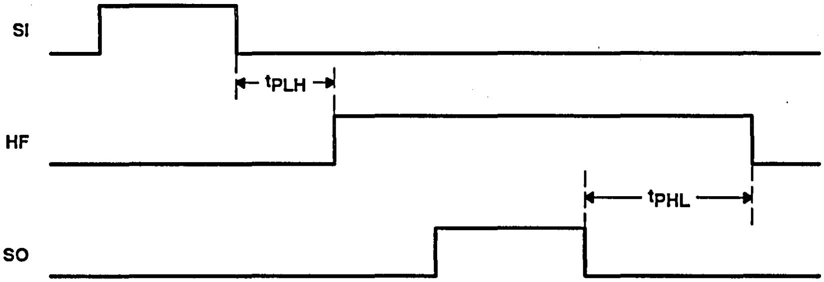


Figure 7. Half-Full Waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current	Q outputs				– 2.6	mA
		Flags				– 0.4	
I_{OL}	Low-level output current	Q outputs				24	mA
		Flags				8	
f_{clock}	Clock frequency	SI or SO		0		25	MHz
t_w	Pulse duration	SI or SO	High or low	15			ns
		$\overline{\text{RST}}$	Low	15			
t_{su}	Setup time before SI↑	Data		0			ns
		$\overline{\text{RST}}$	High (inactive)	15			
t_h	Hold time, data after SI↑			17			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2	V
V_{OH}	Any Q	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA				V
			$I_{OH} = -2.6$ mA	2.4	3.2		
	Flags	$V_{CC} = 4.5$ V,	$I_{OH} = -0.4$ mA	2.7	3.4		
V_{OL}	Any Q	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4	V
			$I_{OL} = 24$ mA		0.35	0.5	
	Flags	$V_{CC} = 4.5$ V	$I_{OL} = 4$ mA		0.25	0.4	
			$I_{OL} = 8$ mA		0.35	0.5	
I_{OZH}		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			20	μA
I_{OZL}		$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			−20	μA
I_I		$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1	mA
I_{IH}		$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20	μA
I_{IL}		$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			−0.1	mA
I_O‡		$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	−30		−112	mA
I_{CC}		$V_{CC} = 5.5$ V	Low		112	165	mA
			High		105	160	
			Disabled		115	170	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}	SI			30		25		MHz
	SO			30		25		
t_w[‡]	IR high			15		8		ns
t_w[§]	OR high			19		8		ns
$t_{d(QV-ORH)}$	Q valid before OR↑			6	9	−5	12	ns
$t_{d(SOL-QX)}$	Q valid after SO↓			13		4		ns
t_{pd}	SI↓	Q		600	800	350	1000	ns
t_{PHL}	SI↑	IR		20	26	8	30	ns
t_{PLH}	SI↓			16	21	6	25	
t_{PLH}[¶]	SI↓	OR		600	800	350	1000	ns
t_{PHL}	SI↓	AF/AE		550	700	290	880	ns
t_{PLH}				85	115	40	150	
t_{PLH}	SI↓	HF		340	410	180	510	ns
t_{pd}	SO↓	Q		13	17	4	22	ns
t_{PHL}	SO↑	OR		23	27	7	33	ns
t_{PLH}	SO↓			20	24	6	30	
t_{PLH}[¶]	SO↓	IR		600	800	350	1000	ns
t_{PHL}	SO↓	AF/AE		550	700	290	880	ns
t_{PLH}				85	115	35	150	
t_{PHL}	SO↓	HF		340	410	170	510	ns
t_{PHL}	$\overline{\text{RST}}$↓	OR		22	26	10	34	ns
t_{PLH}	$\overline{\text{RST}}$↑	IR		12	18	5	22	ns
t_{PHL}	$\overline{\text{RST}}$↓	IR		12	18	5	22	ns
		Q		14	17	5	19	
t_{dis}	$\overline{\text{OE}}$↑	Q		7	13	2	15	ns
t_{en}	$\overline{\text{OE}}$↓	Q		6	12	2	13	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] The IR output pulse occurs when the FIFO is full, SI is high, and SO is pulsed (see Figure 4).

[§] The OR output pulse occurs when the FIFO is empty, SO is high, and SI is pulsed (see Figure 3).

[¶] Data throughput or fall-through times

APPLICATION INFORMATION

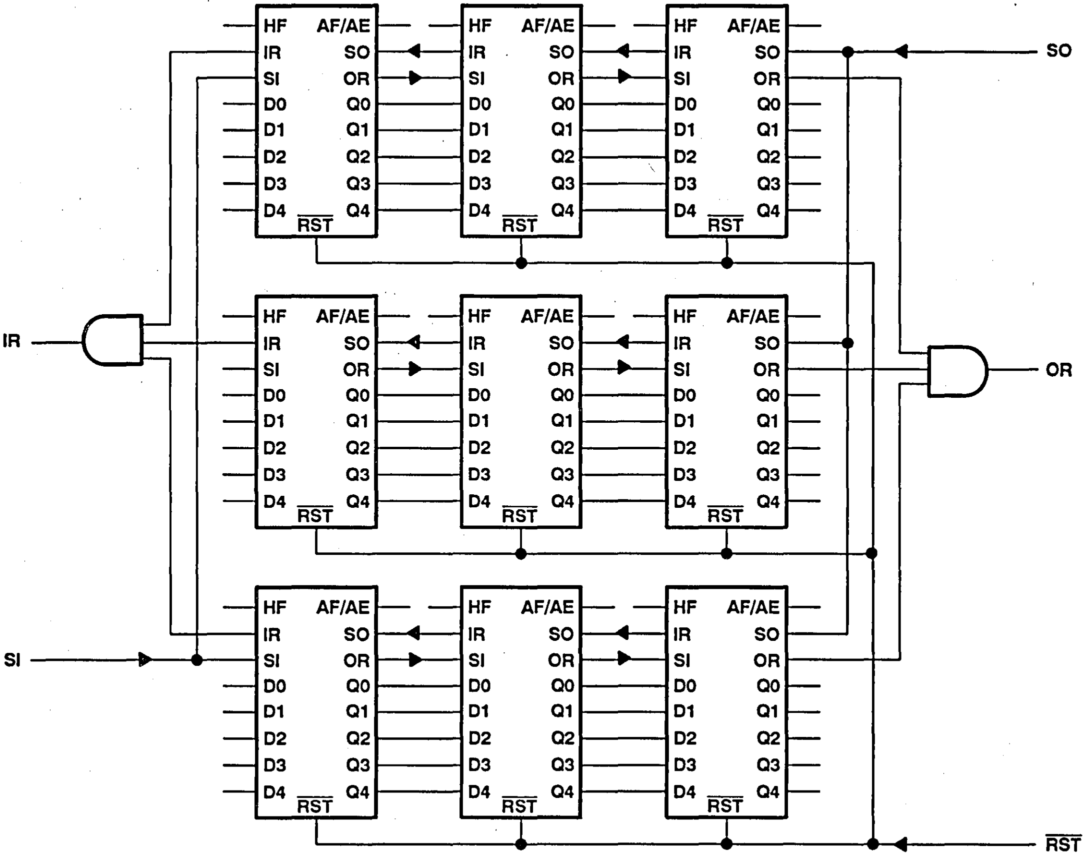
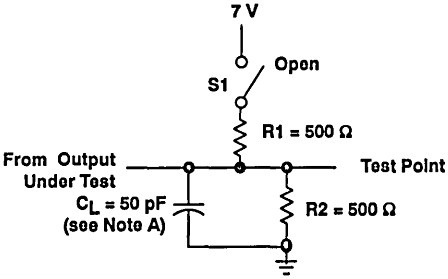


Figure 8. 192-Word by 15-Bit Expansion

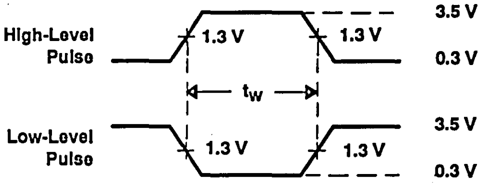
PARAMETER MEASUREMENT INFORMATION



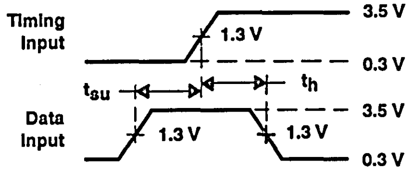
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

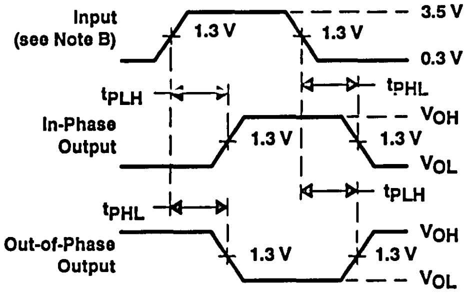
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



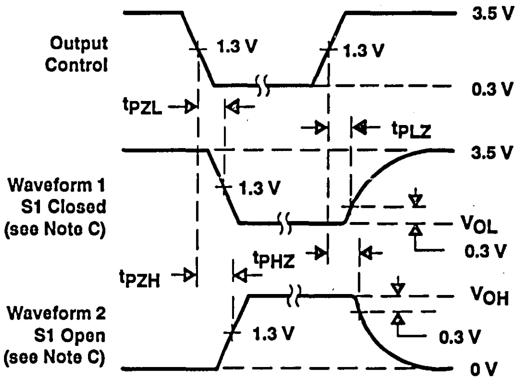
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 9. Load Circuit and Voltage Waveforms

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FIFO Solutions for Increasing Clock Rates and Data Widths

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Introduction

Steady increases in microprocessor operating frequencies and bus widths over recent years have challenged system designers to find FIFO memories that meet their needs. To assist the designer, new FIFOs from Texas Instruments are available with features that complement these microprocessor trends.

Higher data transfer rates have dictated the need for FIFOs to evolve into *clocked* architecture wherein data is moved in and out of the device with synchronous controls. Each synchronous control of the clocked FIFO uses enable signals that synchronize the data exchange to a *free-running* (continuous) clock.

Since the continuous clocks on each port of a clocked FIFO may operate asynchronously to each other, internal status signals indicating when the FIFO is empty or full can change with respect to either clock. To use a status signal for port control, it is synchronized to the port's clock on a clocked FIFO. Synchronization of these signals with flip-flops introduces metastability failures that increase with clock frequency. Texas Instruments uses two-stage flag synchronization to greatly improve reliability.

Higher clock frequencies augment raw speed, but greater bandwidth is also achieved by increasing the data width. Wider data paths can have the associated cost of large board area due to increased package sizes. New compact packages for TI's FIFOs reduce this cost.

Clocked FIFOs

Clocked FIFOs have become popular for relieving bottlenecks in high-speed data traffic. Data transfers for many systems are synchronized to a central clock with read and write enables. These free-running clocks can be input directly to a clocked FIFO with the same enables controlling its data transfer on the low-to-high transition of the clock.

Reducing the number of clocks keeps the interface simple and easy to manage. Extra logic is needed to produce a gated pulse when using a FIFO that accepts a clock only for a data transfer request. The generated clock signal is a derivative of the master clock with a margin of timing uncertainty. At high clock frequencies, this timing uncertainty is not tolerable and costly adjustments are needed.

Additional logic is also conserved by implementing flag synchronization on the clocked FIFO. Tracking is done to generate flags that indicate when the memory is empty or full. In many applications, the input and output to the FIFO are asynchronous and the flag signals must be synchronized for use as control. A read will not be completed on the FIFO if no data is ready, so the $\overline{\text{EMPTY}}$ signal is synchronized to the read clock. This synchronous output-ready flag (OR) is useful for controlling read operations. Likewise, the $\overline{\text{FULL}}$ signal is synchronized to the write clock, producing the input-ready flag (IR).

Flag Synchronization

As previously explained, one of the advantages of the clocked FIFO is the on-board synchronization of the $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ status flags when the input and output are asynchronous. In one method of synchronization, a single flip-flop captures the asynchronous flag's value (see Figure 1). With this method, the rising transition of data can violate the flip-flop's setup time and produce a metastable event (metastability is a malfunction of a flip-flop wherein the latch hangs between high and low states for an indefinite period of time).

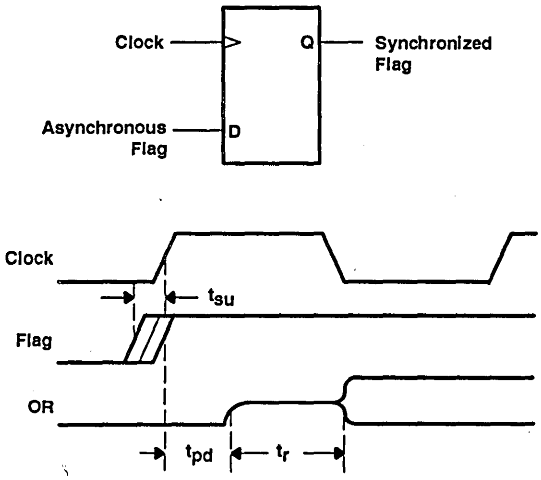


Figure 1. Triggering a Metastable Event With a One-Stage Synchronizer

Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with increased resolve time (t_r). The expected time until the output of a single flip-flop with asynchronous data has a metastable event that lasts t_r or longer is characterized by the following mean time between failures (MTBF) equation:

$$MTBF_1 = \frac{\exp\left(\frac{t_r}{\tau}\right)}{t_o f_c f_d}$$

Where:

t_o = flip-flop constant representing the time window during which changing data invokes a failure
t_r = resolve time allowed in excess of the normal propagation delay
t = flip-flop constant related to the settling time of a metastable event
f_c = clock frequency
f_d = asynchronous data frequency. For OR flag analysis, it is the frequency at which data is written to empty memory. For IR flag analysis, it is the frequency at which data is read from full memory.

The MTBF decreases as clock and data frequency increase and as the time allowed for a metastable event to settle (t_r) decreases.

Metastability failures are a formidable issue for short clock cycle times. Increasing the clock frequency linearly increases the number of metastable events triggered, but the shortened available resolve time exponentially increases the the failure rate. It is impossible to eliminate the possibility of a metastable event under these conditions, but solutions exist to reliably increase the expected time between failures.

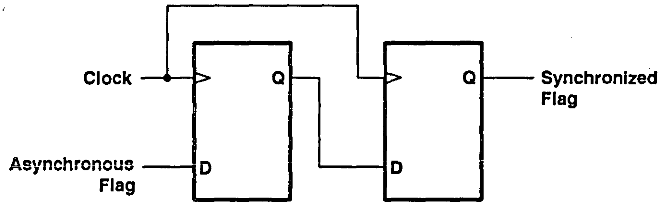


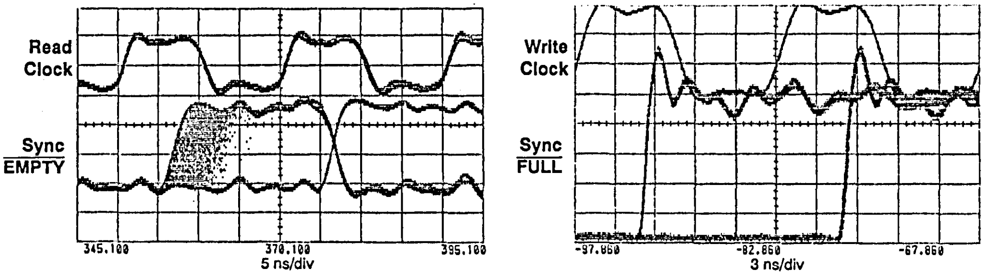
Figure 2. Two-Stage Synchronizer

Texas Instruments increases the metastable MTBF by several orders of magnitude for IR and OR flags by employing two-stage synchronization (see Figure 2). For the output of the second stage to be metastable, the first stage must have a metastable event that lingers until it encroaches upon the setup time of the second stage. Adding another stage to a single flip-flop synchronizer is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. The mean time between failures for a two-stage synchronizer is given by:

$$MTBF_2 = \frac{\exp\left[\dfrac{t_r + \frac{1}{f_c} - t_p}{\tau}\right]}{t_o\, f_c\, f_d}$$

Where:

t_p = propagation delay of the first flip-flop



f_C = 50 MHz, f_d = 5 MHZ, V_{CC} = 5 V

(a) ONE-STAGE SYNCHRONIZATION

f_C = 66.7 MHz, f_d = 6.7 MHz, V_{CC} = 5 V

(b) TWO-STAGE SYNCHRONIZATION

Figure 3. Storage Oscilloscope Plots Taken Over a 15-Hour Duration

Figure 3 compares the two synchronization methods discussed. Both plots were taken at room temperature and nominal V_{CC} while each data transition violated setup time. Figure 3(a) shows the performance of an $\overline{\text{EMPTY}}$ flag synchronizer using only one flip-flop, while Figure 3(b) is the IR flag of an SN74ACT7807 with the write clock operating at maximum frequency.

Compact Packaging

Microprocessor bus widths have continuously doubled every few years to maximize their performance. Bus widths of 32 and 64 bits are common place today, whereas they were almost unheard of a few years ago. The downside to the increased bit count is that each subordinate device in the system must match this width with corresponding increases in board size.

New shrink packages for TI's clocked FIFOs provide a solution to this problem. Multiple-byte data paths can be buffered while covering only a fraction of the area of conventional packages. These new FIFO packages are presently available in 56-, 64-, and 80-pin configurations. Dubbed shrink quad flat package (SQFP), the 64-pin package is used for 9-bit-wide FIFOs, and the 80-pin package is used for 18-bit-wide FIFOs. Both SQFP packages have a lead pitch of 0.5 mm. The 56-pin shrink small-outline package has a 0.025-inch lead pitch and also houses 18-bit-wide FIFOs. A variety of TI's FIFOs are offered in these new packages (see Table 1).

Table 1. FIFOs Available In Space-Efficient Packages

DEVICE	CLOCKED	ORGANIZATION	CLOCK CYCLE TIME (ns)	PACKAGES
SN74ACT2235	No	1K × 9 × 2	20, 30 40, 50	64 SQFP 44 PLCC
SN74ACT7802	No	1K × 18	25, 40, 60	80 SQFP 68 PLCC
SN74ACT7811	Yes	1K × 18	15, 18, 20, 25	80 SQFP 68 PLCC
SN74ACT7803 SN74ACT7805 SN74ACT7813	Yes	512 × 18 256 × 18 64 × 18	15, 20, 25, 40	56 SSOP
SN74ACT7804 SN74ACT7806 SN74ACT7814	No	512 × 18 256 × 18 64 × 18	20, 25, 40	56 SSOP
SN74ACT7807	Yes	2K × 9	15, 20, 25, 40	64 SQFP 44 PLCC
SN74ACT7808	No	2K × 9	20, 25, 30, 40	64 SQFP 44 PLCC

Figure 4 compares the space savings of the new compact packages compared to competitive surface-mount solutions. A four-byte path constructed with four clocked FIFOs in 32-pin PLCC packages consumes 1.16 in^2, while two 56-pin SSOP packages cover only 0.59 in^2.

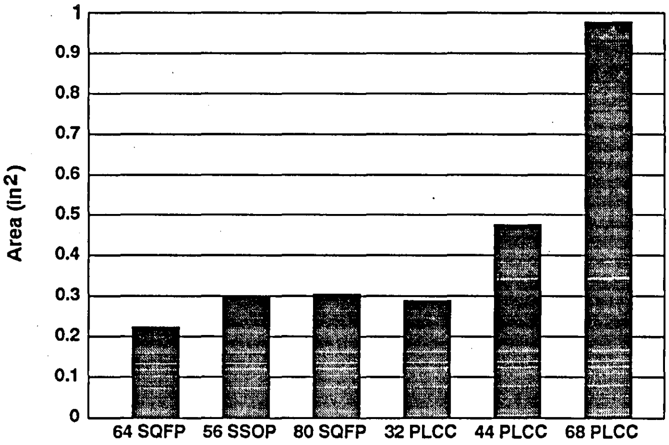


Figure 4. Surface-Mount Package Area Comparison

New Clocked FIFOs

Four new CMOS clocked FIFOs from Texas Instruments offer a variety of memory depths. All four can match applications that require maximum clock frequencies of 67 MHz and access times of 12 ns. Suited for buffering long packets, the 2K × 9 SN74ACT7807 is the deepest of the four and is available in the 44-pin PLCC or 64-pin SQFP. The SN74ACT7803, SN74ACT7805, and SN74ACT7813 are organized as 512 × 18, 256 × 18, and 64 × 18, respectively, and have the same pin arrangement in the 56-pin SSOP. Every TI clocked FIFO is easily expanded in word width, and the SN74ACT7803/05/13 can also be arranged to form a bidirectional FIFO. With the two FIFOs connected as in Figure 5, no extra logic is needed for bidirectional operation.

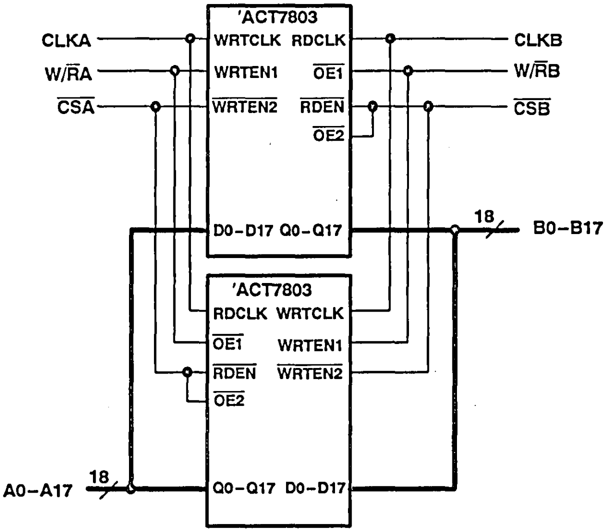


Figure 5. Bidirectional Configuration for the SN74ACT7803

Silicon is currently available for a bidirectional clocked FIFO fabricated in TI's Advanced BiCMOS (ABT) process. The SN74ABT7819 is organized as 512 × 18 × 2 with two internal independent FIFOs. Each port has a continuous free-running clock, a chip select ($\overline{\text{CS}}$), a read/write select ($\overline{\text{R}}$/W), and two separate read and write enables for control. It supports clock frequencies in excess of 80 MHz and a maximum access time below 10 ns. This device is packaged in the 80-pin QFP and 80-pin SQFP.

Conclusion

Several semiconductor manufacturers including Texas Instruments have responded to customer needs by providing clocked FIFOs whose synchronous interfaces conform to the requirements of many high-performance systems. Capitalizing on the available continuous system clocks, this architecture limits the amount of necessary glue logic and the number of timing constraints.

Flag synchronization is important for clocked FIFOs buffering between asynchronous systems. Flip-flop synchronizers used for this task have a metastable failure rate that grows exponentially with clock frequency. Texas Instruments employs two stages of synchronization that improve the flags' reliability significantly.

Finally, providing a FIFO buffer for wide buses has historically consumed large amounts of board area. Designers seeking relief from this problem can find it in the packaging options offered for Texas Instruments FIFOs. Used to house 9- and 18-bit devices, these packages require only about 50% of the space required for conventional surface-mount packages.

Acknowledgement

This application note was authored by Kam Kittrell, Advanced System Logic – Semiconductor Group, Texas Instruments Incorporated.

FIFO Surface-Mount Package Information

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Introduction

Texas Instruments provides seven types of plastic surface-mount packages for CMOS FIFO memory devices. These packages and the data bus width that each package can provide are listed in Table 1.

Table 1. Plastic Surface-Mount FIFO Packages

PACKAGE	NO. OF DATA BITS
44-pin PLCC	9
64-pin SQFP	9
56-pin SSOP	18
68-pin PLCC	18
80-pin SQFP	18
80-pin QFP	18
120-pin SQFP	32 or 36

SSOP = shrink small-outline package
PLCC = plastic leaded chip carrier
SQFP = shrink quad flat package
QFP = quad flat package

This application report discusses several topics concerning the FIFO packages listed in Table 1:

- The thermal resistance, $R_{\Theta JA}$, and the chip junction temperature of the device
- The need for dry packing to maintain safe moisture levels inside the package
- The three methods used by Texas Instruments for shipping FIFOs to customers
- The package dimensions, including two-dimensional drawings that show areas, heights, and lead pitches
- The area comparison of surface-mount packages used for commercial FIFO memories
- The test sockets available for surface-mount FIFO packages

Thermal Resistance

Thermal resistance is defined as the ability of a package to dissipate heat generated by an electronic device and is characterized by $R_{\Theta JA}$. $R_{\Theta JA}$ is the thermal resistance from the integrated circuits chip junction to the free air (ambient). Units for this parameter are in degrees Celsius per watt. Table 2 lists $R_{\Theta JA}$ for SSOP, PLCC, SQFP, and QFP packages under five different air-flow environments: 0, 100, 200, 250, and 500 linear feet/minute. The chip junction temperature (T_J) can be determined using the following equation:

$$T_J = R_{\Theta JA} \times P_T + T_A$$

Where:

T_J = chip junction temperature (°C)
$R_{\Theta JA}$ = thermal resistance, junction to free-air (°C/watt)
P_T = total power dissipation of the device (watts)
T_A = free-air (ambient) temperature in the particular environment in which the device is operating (°C)

Table 2. Thermal Resistance, $R_{\Theta JA}$, for FIFO Packages

PACKAGE	LEAD FRAME	$R_{\Theta JA}$ (°C/W)				
		0 LFPM	100 LFPM	200 LFPM	250 LFPM	500 LFPM
56-pin SSOP	Copper	94.2	82.2	N/A	70	57.8
44-pin PLCC	Copper	65	N/A	N/A	N/A	N/A
68-pin PLCC	Copper	47.2	43.4	N/A	32.7	27.8
64-pin SQFP	Copper	92.5	87.8	N/A	72.9	57.8
80-pin SQFP	Copper	87.8	79.1	N/A	67.3	54.2
120-pin SQFP†	Copper	49.6	44.3	N/A	38.3	28.6
80-pin QFP	Alloy 42	80	67	61	N/A	N/A

† Heat spreader molded inside the package
N/A = not available

$R_{\Theta JA}$ generally increases with decreasing package size; however, this is not true with the 120-pin SQFP package. A heat spreader molded inside the package absorbs a large amount of heat dissipated by the device. As a result, this package provides a relatively low $R_{\Theta JA}$. The 120-pin SQFP is the only package in Table 2 that incorporates a heat spreader.

Package Moisture Sensitivity

When a plastic surface-mount package is exposed to temperatures typical of furnace reflow, IR (infrared) soldering, or wave soldering (215°C or higher), the moisture absorbed by the package turns to steam and expand rapidly. The stress caused by this expanding moisture can result in internal and external cracking of the package that can lead to reliability failures. Possible damage includes the delamination of the plastic from the chip surface and lead frame, damaged bonds, cratering beneath the bonds, and external package cracks.

To prevent potential damage, packages that are susceptible to the effects of moisture expansion undergo a process called dry pack. This dry pack process helps to reduce moisture levels inside the package. The process consists of a 24-hour bake at 125°C followed by sealing of the packages in moisture-barrier bags with desiccant to prevent reabsorption of moisture during the shipping and storage processes. These moisture-barrier bags allow a shelf storage of 12 months from the date of seal. Once the moisture-barrier bag is opened, the devices in it must be handled by one of the following four methods, listed in order of preference:

1. The devices may be mounted within 48 hours in an atmospheric environment of less than 60% relative humidity and less than 30°C.
2. The devices may be stored outside the moisture-barrier bag in a dry atmospheric environment of less than 20% relative humidity until future use.
3. The devices may be resealed in the moisture-barrier bag adding *new* fresh desiccant to the bag. When the bag is opened again, the devices should be used within the 48-hour time limit or resealed again with fresh desiccant.
4. The devices may be resealed in the moisture-barrier bag using the *original* desiccant. This method does not allow the floor life of the devices to be extended. The cumulative exposure time before reflow must not exceed a total of 48 hours.

All plastic surface-mount FIFO devices are tested for moisture sensitivity in accordance with Texas Instruments IPC-SM-786 procedure.

Shipping Methods/Quantities/Dry Pack

Three methods are used by Texas Instruments for shipping FIFOs to customers. These methods are tubes, tape/reel, and trays. The quantities for each of the shipping methods are listed in Table 3. The shipping quantity is defined as the maximum number of packages that can be packed in a single shipping unit (e.g., the maximum number of 56-pin SSOP packages that can be packed in a tube is 20). Whether or not the packages require dry pack before shipping is denoted by a yes or no in the dry-pack column.

Table 3. Shipping Methods and Quantities

PACKAGE	SHIPPING METHOD			DRY PACK
	TUBE†	TAPE/REEL†	TRAYS†	
56-pin SSOP	20	500	N/A	No
44-pin PLCC	27	500	N/A	No
68-pin PLCC	18/19‡	250	N/A	Yes
64-pin SQFP	N/A	N/A	50	Yes
80-pin SQFP	N/A	N/A	50	Yes
120-pin SQFP	N/A	N/A	50/84§	Yes
80-pin SQFP	N/A	N/A	50	Yes

† Texas Instruments reserves the right to change any of the shipping quantities at any time without notice.

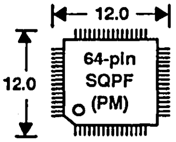
‡ Eighteen packages can be packed in a single tube when pin is used as a tap, or nineteen packages can be packed in a tube when plug is used as a tap.

§ Depending on tray size

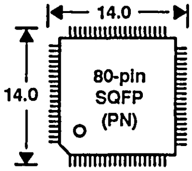
N/A = not applicable

Package Dimensions and Area Comparison

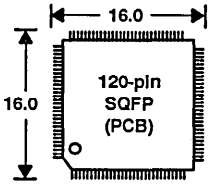
Figure 1 contains two-dimensional drawings of the seven available surface-mount FIFO packages. For detailed mechanical drawings of these packages, please refer to the mechanical drawing section of the 1994 *High-Performance FIFO Memories Data Book* (literature #SCAD003B).



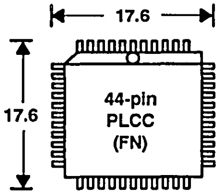
Area: 144.00 mm^2
Height: 1.50 mm
Lead Pitch: 0.5 mm



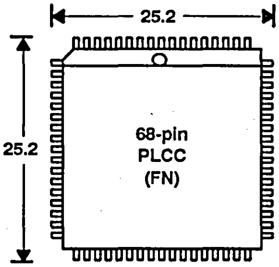
Area: 196.00 mm^2
Height: 1.50 mm
Lead Pitch: 0.5 mm



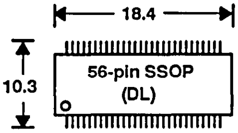
Area: 256.00 mm^2
Height: 1.58 mm
Lead Pitch: 0.4 mm



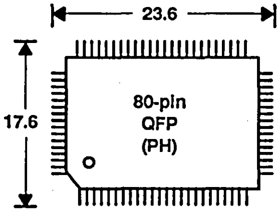
Area: 309.80 mm^2
Height: 4.37 mm
Lead Pitch: 1.27 mm



Area: 635.04 mm^2
Height: 4.37 mm
Lead Pitch: 1.27 mm



Area: 189.50 mm^2
Height: 2.59 mm
Lead Pitch: 0.635 mm



Area: 415.40 mm^2
Height: 2.95 mm
Lead Pitch: 0.8 mm

Figure 1. Package Dimensions

Figure 2 shows the area comparison of surface-mount packages for FIFOs from Texas Instruments and other FIFO vendors.

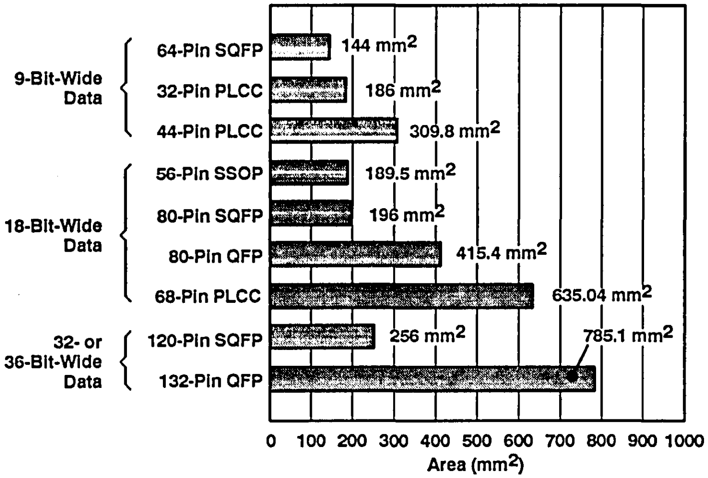


Figure 2. Surface-Mount Package Area Comparison

Test Sockets

For prototype development of a system, it is often an advantage to have sockets for surface-mount products. Test sockets available for use with Texas Instruments FIFO packages are listed in Table 4. Only one manufacturer is listed for each socket type, although other vendors may offer comparable sockets.

Table 4. Table 4. Test Sockets for FIFO Packages

PACKAGE	MANUFACTURER	NUMBER	DESCRIPTION
56-pin SSOP	Yamaichi	IC51-0562-1387	Solder through hole
44-pin PLCC	NEY	6044	Solder through hole
68-pin PLCC	NEY	6068	Solder through hole
64-pin SQFP	Yamaichi	IC51-0644-807	Solder through hole
80-pin SQFP	Yamaichi	IC51-0804-808	Solder through hole
120-pin SQFP	Yamaichi	In development (as of 6/92)	Solder through hole
80-pin QFP	Yamaichi	IC51-0804-394	Solder through hole

Acknowledgement

This application note was authored by Jon E. Lyu, Advanced System Logic – Semiconductor Group, Texas Instruments Incorporated.

FIFO Memories:
Fine-Pitch Surface-Mount Manufacturability

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Introduction

Recent advances in semiconductor processing and packaging have produced highly integrated, fine-pitch devices to satisfy the demand for smaller systems. With the trend towards higher chip complexity occupying less board space, device manufacturers must increase bit density while decreasing package size. To accommodate these requirements, manufacturers have two choices: increase bit density, keeping the number of pins constant while reducing pitch and area, or reduce the package lead pitch, keeping area constant while increasing pin count. Manufacturers of hand-held and laptop computers and data communications and telecommunications equipment require the use of fine-pitch packages to build and maintain a competitive advantage.

Improved Function Density

Texas Instruments (TI) provides five types of fine-pitch plastic surface-mount packages for its FIFO product line (see Table 1). Each of these surface-mount packages has lead-to-lead spacing less than or equal to 0.635 mm (0.025 in.). All of these packages offer designers critical board-space savings that is required for advanced systems. Compared to the commonly used 68-pin plastic leaded chip carrier (PLCC) for 18-bit FIFOs, TI's Widebus™ package in either the 56-pin shrink small-outline package (SSOP) or the 80-pin thin quad flat package (TQFP) reduces board space by 70%. A 67% saving of board space is available with TI's 36-bit FIFO family in the 120-pin TQFP compared to the 132-pin plastic quad flat package (PQFP).

Table 1. Fine-Pitch Packages

	THIN QUAD FLAT PACKAGE (TQFP)				THIN SHRINK SMALL-OUTLINE PACKAGE (SSOP)
Pin count	64	80	120	132	56
Lead pitch (mm)	0.5	0.5	0.4	0.635	0.635
Footprint (mm)	12 x 12	14 x 14	16 x 16	28 x 28	10.35 x 18.42
Board area (mm^2)	144	196	256	784	190.6
Package suffix	PM	PN	PCB	PQ	DL

Manufacturing

Manufacturers are currently employing high-volume board assembly techniques using standard lead pitches of 0.5 mm (20 mils) and greater. However, as lead pitch continues to decrease, questions must be asked of both the manufacturer and the supplier:

1. Are fine-pitch packaging capabilities available?
2. Does production equipment have sufficient accuracy to produce high-volume, high-quality parts?
3. Do the manufacturing personnel have experience in high-volume, high-quality production using fine-pitch packaging?
4. Have the testability issues of fine-pitch packaging been considered?

Standard processing techniques, such as those used with surface-mount rigid lead packages, become difficult with fine-pitch packaging. Manufacturing issues may arise from compromises in screen-printing techniques, solder board/lead coplanarity, placement-accuracy requirements of components, and solder deposition methods (e.g., mass reflowing). All of these factors can result in shorts or opens due to poor placement, too much solder, or not enough solder. These issues will influence the overall yield and reliability of the product.

Equipment for the placement of fine-pitch packaging must feature a highly accurate positioning system. Placement accuracy for fine-pitch packages must increase as lead pitch decreases. Misaligned packages and boards greatly reduce production yields as well as throughput. Systems that feature state-of-the-art machine vision, align and inspect leads,

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and calculate registration with an extremely high degree of accuracy and repeatability, ensure high-production yields. There must also be careful control over the Z-axis pressure when placing these fine-pitch packages to protect the lead coplanarity. Currently, there are systems available with accurate placement as fine as 0.1-mm pitch.

One of the most critical issues facing the manufacturer is the reliability of the footprint design. Constraints include the length and width of the footprint and the amount of solder paste used to produce a good joint. If too much solder is used, the footprint may bridge causing a short (see Table 2). The minute dimensions associated with fine-pitch packages require that the footprint be drawn to the highest level of accuracy in order to ensure consistent reliability. Board assemblers must be able to match the footprint with the same level of accuracy and repeatability.

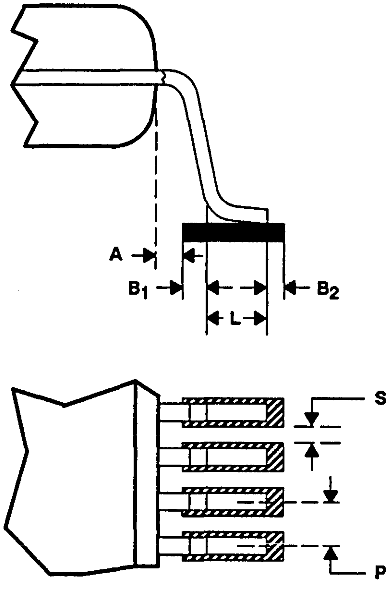
Table 2. Defect Causes and Effects

DEFECT	CONTROL
Solder bridging	Control the solder paste quantity
Open circuits	Control solder-paste thickness and maintain lead coplanarity
Shorts and opens	Control equipment accuracy in the placement of parts

As previously discussed, the key to ensuring high yield is an accurate footprint pattern. Many manufacturers request footprint patterns and dimensions to assist in their board assembly. There are several factors to consider when designing a footprint pattern to ensure reliability:

- Device design – JEDEC or EIAJ Standard
- PWB – foil thickness, number of layers, supplier's capabilities
- Solder paste – type, solder mesh
- Printer – manufacturer, standoff control, squeegee pressure
- Print mask – type (stencil/mesh), tension, bias
- Reflow process – preheat, temperature, dwell, etc.

Figure 1 diagrams the key dimensions for designing an accurate footprint layout.



A = Distance Package Edge to End of Pad
B_1 = Pad Extension Beyond Heel of Foot
B_2 = Pad Extension Beyond Toe of Foot
L = Lead Foot Length
P = Lead Pitch
S = Distance From Center of Pin to Center of Pin

Figure 1. Footprint Diagram

Palladium-Plated Lead Frames

Another area for manufacturers to investigate is metallization or bonding of the leads to the circuit board with solder. There are several widely used localized reflow techniques including hand soldering, hot bar, focused infrared (IR), and laser. With each technique, heat is applied to the leads until the solder melts. When the heat source is removed, the solder cools forming the joint. Each manufacturer must make the choice between precision point-to-point systems (one chip at a time) and the speed of gang bonding (multiple chip bonding). Another area of metallization to consider is preplating of the leads by the device manufacturer. TI has begun to implement palladium (Pd) lead plating on many fine-pitch packages. These efforts began with joint testing of palladium-plated leads with several large computer and telecom customers in 1987. Since then, TI has begun high-volume manufacturing with over five billion Pd-plated devices in the field.

Palladium preplating is essentially a nickel (Ni)-plated lead frame that has a minimum of 3 microinches (0.076 microns) of Pd. The Pd finish protects the Ni from oxidation and eliminates the need for silver spotting. Silver (Ag) spots are used to attach the fine wires from the die to the lead frames. However, the silver can migrate over time to form extraneous electrical contacts that greatly impacts reliability. Many problems associated with fine-pitch manufacturing can be eliminated with palladium preplating:

- Reduces excess solder
- Excellent Pd wetting characteristics
- Reduced handling
- Improved package integrity
- Reduced mechanical damage
- Tarnish resistant
- Compatible with existing assembly processes
- Excellent adhesion to mold compounds

Table 3 shows the results of a solder-joint strength test comparing Pd solder joints to traditional solder joints, the results demonstrate an equal performance between the two techniques. Palladium preplating also exhibits adhesion to most mold compounds that reduces moisture ingress and plastic-to-lead-frame delimitation.

Table 3. Results of Soldered Joint Strength

SAMPLE	HOURS OF HEAT AGING			
	O HR	8 HR	16 HR	24 HR
3 micro inches Pd	5.17 lbf	5.95 lbf	5.85 lbf	4.71 lbf
Solder dip	5.07 lbf	4.51 lbf	5.55 lbf	5.50 lbf

In many cases, the cause for shorts and opens can be attributed to lead coplanarity or the extent to which all leads lie in a single plane. This holds especially true for fine-pitch packaging due to the smaller geometries and delicate leads. Traditional solder-dipped leads tend to have more pin-to-pin alignment problems than the Pd-plated leads. The Pd preplated leads have a more conformal and uniform coating than those that are solder dipped, since the plating is performed prior to the packaging process (see Figure 4). An increase in coplanarity improves overall circuit reliability. The excellent wetting characteristics of Pd improve the wicking effects of solder and form a better solder joint/fillet. The thin Pd coating and minimal handling reduce the chance of coplanarity problems (i.e., shorts and opens) and also produce uniform solder joints with a minimum amount of solder. Table 4 lists TI's fine-pitch packages that implement Pd plating.

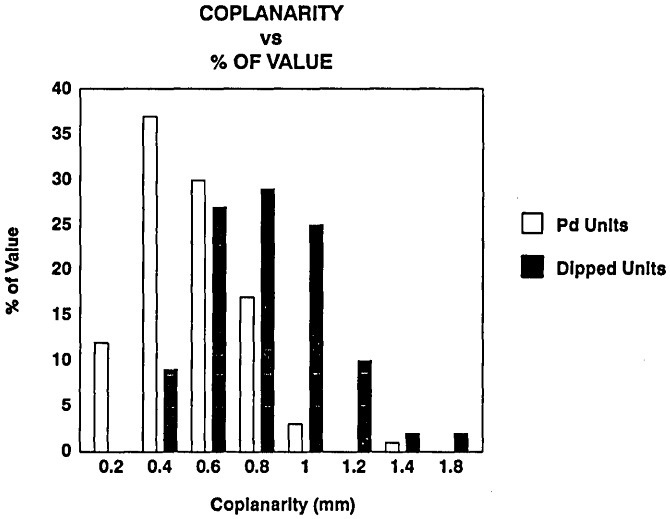


Figure 2. Coplanarity Results

Table 4. Lead-Frame Platings by Package Type

PACKAGE	SUFFIX	LEAD FRAME
132-pin PQFP	PQ	Palladium
120-pin TQFP	PCB	Palladium
80-pin TQFP	PN	Solder
64-pin TQFP	PM	Solder
56-pin SSOP	DL	Palladium

Testability

Another issue introduced by the onset of fine-pitch surface-mount packages involves testing circuit boards. With denser printed-circuit boards heavily populated with fine-pitch surface-mount packages, the issues involved with functional testing should be addressed. One of the most cost-effective solutions is the implementation of boundary-scan methodology defined by the joint test action group (JTAG) and adopted by the IEEE 1149.1 committee. JTAG devices incorporate on-chip *test points* called boundary scan cells and utilize a serial scan protocol through the device. Devices with JTAG can be designed into the data path and provide the controllability and observability needed to troubleshoot manufacturing defects.

Design/Preproduction Considerations

For designers who wish to implement fine-pitch packaging, TI provides an easy alternative for the development of prototypes and breadboarding. TI has worked with several test-socket manufacturers who provide accurate and easy-to-use through-hole test sockets for all of their surface-mount packaging. In addition to test sockets, TI also offers mechanical packages. These are packages that include lead frames without the silicon and meet all mechanical specifications. Mechanical packages provide an inexpensive means for manufacturing capability studies, machine setup, personnel training, and process development work (see Table 5).

Table 5. Available Fine-Pitch Test Sockets and Mechanical Packages

SOCKET TYPE	MANUFACTURER	PART NUMBER	DESCRIPTION
64-pin TQFP	Yamaichi	IC51-0644-807	Through hole
56-pin SSOP	Yamaichi	IC51-0562-1514	Through hole
80-pin TQFP	Yamaichi	IC51-0804-808	Through hole
120-pin TQFP	Yamaichi	IC51-1204-1596	Through hole
132-pin PQFP	Yamaichi	IC51-828-KS12338	Through hole

PACKAGE	TI PART NUMBER
64-pin TQFP	SN700870PM
56-pin SSOP	SN250011DLR
80-pin TQFP	SN700871PN
120-pin TQFP	SN700782PCB

Conclusion

Designs that incorporate fine-pitch packages have the advantage of critical board-space reduction. As designers continue to implement higher levels of integration, board space remains at a premium. With the implementation of concurrent engineering practices from design to test to manufacturing, many packaging difficulties can be overcome. Fine-pitch packaging is the designers' easiest option to reduce critical board space without the loss of higher chip integration.

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Romm, D., McLellan, N., "Evaluation of Water Soluble and No-Clean Solder Pastes with Palladium Plated and Solder Plated SMT Devices".

Acknowledgement

This application note was authored by Tom Jackson, Advanced System Logic – Semiconductor Group, Texas Instruments Incorporated.

Metastability Performance of Clocked FIFOs

First-In, First-Out Technology

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Introduction

This report is intended to help the user understand more clearly the issues relating to the metastable performance of Texas Instruments (TI) clocked FIFOs in asynchronous system applications. It discusses basic metastable operation theory, shows the equations used to calculate metastable failure rates for one and two stages of synchronization, and describes the approach TI has used for synchronizing the status flags on its series of clocked FIFOs. Additionally, a test setup for measuring the failure rate of a device to determine its metastability parameters is shown, and results are given for both an advanced BiCMOS (ABT) FIFO and an advanced CMOS (ACT) FIFO. Using these parameters, calculations of MTBF under varying conditions are performed.

Metastability

Metastability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state. A common example of this is the case of data violating the setup and hold specifications of a latch or a flip-flop. In a synchronous system, the data always has a fixed relationship with respect to the clock. When that relationship obeys the setup and hold requirements for the device, the output goes to a valid state within its specified propagation delay time. However, in an asynchronous system, the relationship between data and clock is not fixed; therefore, occasional violations of setup and hold times can occur. When this happens, the output may go to an intermediate level between its two valid states and remains there for an indefinite amount of time before resolving itself or it may simply be delayed before making a normal transition[1]. In either case, a metastable event has occurred.

Metastable events can occur in a system without causing a problem, so it is necessary to define what constitutes a failure before attempting to calculate a failure rate. For a simple CMOS latch, as shown in Figure 1, valid data must be present on the input for a specified period of time before the clock signal arrives (setup time) and must remain valid for a specified period of time after the clock transition (hold time) to assure that the output functions predictably. This leaves a small window of time with respect to the clock (t_0) during which the data is not allowed to change. If a data edge does occur within this aperture, the output may go to an intermediate level and remains there for an indefinite amount of time before resolving itself either high or low, as illustrated in Figure 2. This metastable event can cause a failure only if the output has not resolved itself by the time that it must be valid for use (for example, as an input to another stage). Therefore, the amount of resolve time allowed a device plays a large role in calculating its failure rate.

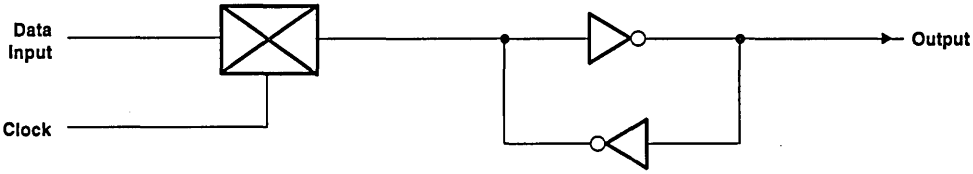

Figure 1. A Simple CMOS Latch

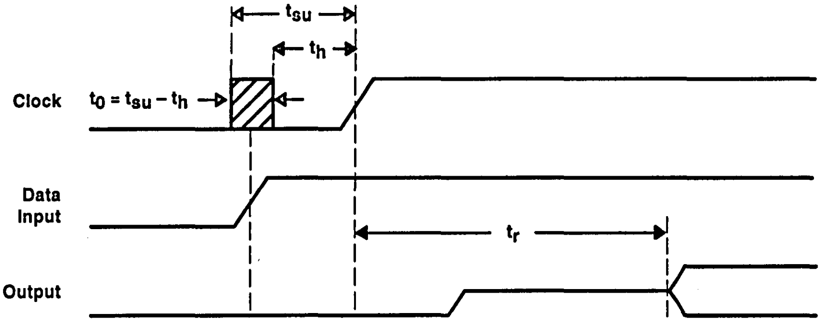

Figure 2. Output at Intermediate Level Due to Data Edge Within t_0 Aperture

The probability of a metastable state persisting longer than a time t_r decreases exponentially as t_r increases[2]. This relationship can be characterized by equation 1:

$$f_{(r)} = e^{(-t_r/\tau)} \tag{1}$$

where the function f(r) is the probability of nonresolution as a function of resolve time allowed, t_r, and the circuit time constant τ (which has also been shown to be inversely proportional to the gain-bandwidth product of the circuit)[3,4].

For a single-stage synchronizer with a given clock frequency and an asynchronous data edge that has a uniform probability density within the clock period, the rate of generation of metastable events can be calculated by taking the ratio of the setup and hold time window described above to the time between clock edges and multiplying by the data edge frequency. This generation rate of metastable events coupled with the probability of nonresolution of an event as a function of the time allowed for resolution gives the failure rate for that set of conditions. The inverse of the failure rate is the mean time between failure (MTBF) of the device and is calculated with the formula shown in equation 2:

$$\frac{1}{\text{failure rate}} = \text{MTBF}_1 = \frac{e^{(t_r/\tau)}}{t_0\, f_c\, f_d} \tag{2}$$

Where:

t_r = the resolve time allowed in excess of the normal propagation delay time of the device
t = the metastability time constant for a flip-flop
t_0 = a constant related to the width of the time window or aperture wherein a data edge will trigger a metastable event
f_c = the clock frequency
f_d = the asynchronous data edge frequency

The parameters t_0 and t are constants that are related to the electrical characteristics of the device in question. The simplest way to determine their values is to measure the failure rate of the device under specified conditions and solve for them directly. If the failure rate of a device is measured at different resolve times and plotted, the result is an exponentially decaying curve. When plotted on a semilogarithmic scale, this becomes a straight line the slope of which is equal to τ. Therefore, two data points on the line are sufficient to calculate the value of τ using equation 3:

$$\tau = \frac{t_{r2} - t_{r1}}{\ln(N1/N2)} \tag{3}$$

Where:

t_{r1} = resolve time 1
t_{r2} = resolve time 2
N1 = the number of failures relative to t_{r1}
N2 = the number of failures relative to t_{r2}

After determining the value for τ, t_0 may be solved for directly.

The formula for calculating the MTBF of a two-stage synchronizer, equation 4, is merely an extension of equation 2:

$$\text{MTBF}_2 = \frac{e^{(t_{r1}/\tau)}}{t_0\, f_c\, f_d} \times e^{(t_{r2}/\tau)} \tag{4}$$

Where:

t_{r1} = the resolve time allowed for the first stage of the synchronizer
t_{r2} = the resolve time allowed in excess of the normal propagation delay
f_c, f_d, t and t_0 are as defined previously, with t and t_0 assumed to be the same for both stages

The first term calculates the MTBF of the first stage of the synchronizer, which in effect becomes the generation rate of metastable events for the next stage. The second term then calculates the probability that the metastable event will be resolved based on the value of t_{r2}, the resolve time allowed external to the synchronizer. The product of the two terms gives the overall MTBF for the two-stage synchronizer.

TI Clocked FIFOs

The TI clocked FIFOs are designed to reduce the occurrence of metastable errors due to asynchronous operation. This is achieved through the use of two- and three-stage synchronizing circuits that generate the status flag outputs IR and OR (output ready). In a typical application, words may be written to and then read from the FIFO at varying rates independent of one another, resulting in asynchronous flag signal generation (internally) at the boundary conditions of full and empty. For example, consider the operation when the FIFO is at the full boundary condition with writes taking place faster than and asynchronously to reads. The IR flag will be low, signifying that the FIFO is full and can accept no more words. When a read occurs, the FIFO is no longer completely full. This causes an internal flag signal to go high, allowing another write to take place. Since the exit from the full state happens asynchronously to the write clock (WRTCLK) of the FIFO, this flag is not useful as a system write enable signal. The solution is to synchronize this internal flag to the write clock through two D-type flip-flop stages and output this synchronized signal as the IR flag (see Figure 3). The OR status flag is generated in a similar manner at the empty boundary condition and is synchronized to the read clock through a three-stage synchronizing circuit.

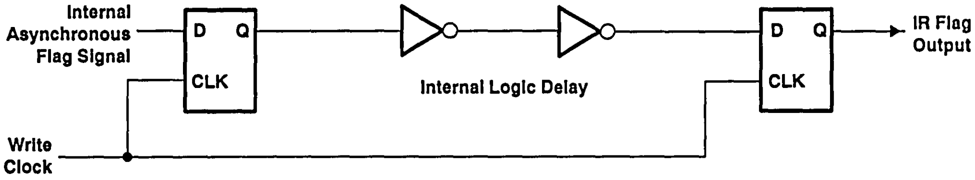

Figure 3. IR Flag Synchronizer

The remainder of this report pertains to the metastability performance of the two-stage IR synchronizer, which is the limiting case of the two in terms of MTBF characteristics. The internal flag signal that goes high on a read and low on a write is synchronized to the write clock through two D-type flip-flop stages. Since this results in the IR flag status of the FIFO being delayed for two clock cycles, a predictive circuit is used to clock the status into the synchronizer at (full minus two) words so that the action of the IR flag going low coincides with the actual full status of the FIFO. However, once the FIFO is full and IR is low, a read that causes the internal flag to go high is not reflected in the status of the IR flag until two write clocks occurr.

With the FIFO full and the IR flag low, a read causes the internal flag signal to go high. This signal is clocked into the first stage of the two-stage synchronizer on the next write clock. Because these two signals are asynchronous to one another, the potential for the output of the first stage of the synchronizer to go to a metastable state exists. If this condition persists until the next write clock rising edge, a metastable condition could be generated in the second stage and reflected on the IR flag output. This metastable condition manifests itself as a delay in propagation time and is considered a failure only if it exceeds the maximum delay allowed in a design.

The effectiveness of the two-stage synchronizer becomes apparent when attempting to generate failures at a rate high enough to count in a reasonable period of time. A metastable event generated in the first stage must persist until the next write clock, i.e., when that data is transferred to the second stage. The resolve time for the first stage is governed by the frequency or period of the write clock. At slower frequencies, the failure rate of the first stage is very low, resulting in a low metastable generation rate to the second stage. The second stage of the synchronizer further reduces the probability of a metastable failure based on the resolve time allowed at the output. The overall failure rate of the device may be affected by increasing the initial asynchronous data generation rate (adding jitter to the data centered about the setup and hold window), by decreasing the resolve time of the first stage (increasing the write clock frequency), and also by reducing the external resolve time at the output.

Test Setup for Measuring FIFO Flag Metastability

The failure rate of a device is measured on a test fixture as shown in Figure 4. The input waveforms used on this setup are also shown in Figure 4. Rising data is jittered asynchronously about the setup and hold aperture of the device under test (DUT) in a ±400-ps window with respect to the device clock (CLK). The output of the DUT is then clocked into two separate flip-flops, FF1 and FF2, by two different clock signals, CLK1 and CLK2. The resolve time t_r is set by the relationship between CLK1 and CLK and is measured as the delta between the normal output transition time and the rising edge of CLK1 minus the setup time required for FF1. CLK2 occurs long enough after CLK1 to allow sufficient time for the DUT to have resolved itself to a valid state. The outputs of FF1 and FF2 are compared by the exclusive OR gate, the output state of which is latched into FF3 by CLK3. When a metastable failure occurs, the output of the exclusive OR gate goes high caused by FF1 and FF2 having opposite data due to the DUT not having resolved itself by time t_r. On the next cycle, low data is clocked into the DUT and FF1 and FF2 in order to reset the status latch, FF3. Failures are counted for different resolve times, and τ is then calculated using equation 3.

Using the test setup in Figure 4, failure rates are measured for both an SN74ABT7819, 512 × 18 × 2 clocked FIFO, and an SN74ACT7807, 2K × 9 clocked FIFO. The device is initially written full to set IR low at the boundary condition. A read clock is generated to send the internal flag high, and a jitter signal is superimposed on it to sweep asynchronously with respect to the write clock in an envelope 800 ps wide and centered such that the IR flag goes high alternately on the second and third write clocks. The nominal write-clock frequency of the test setup is 40 MHz but to increase the failure rate to an observable level, a pulse is injected into the write-clock stream just after the read clock occurs such that the first and second write clocks (the ones that clock the status through the synchronizer) are only 5.24 ns apart. This increases the effective write clock frequency to 191 MHz, reducing the resolve time allowed the first stage and increasing the failure rate.

This test setup and these actions together create the necessary conditions to generate a metastable occurrence on the IR output that is seen after the second write clock and manifests itself as a delay in propagation time. In this instance, the write clock is the synchronizing clock and the read clock generates the asynchronous internal data signal. CLK1 is adjusted to vary the external resolve time, t_{r2}, and the resulting failure rates are recorded.

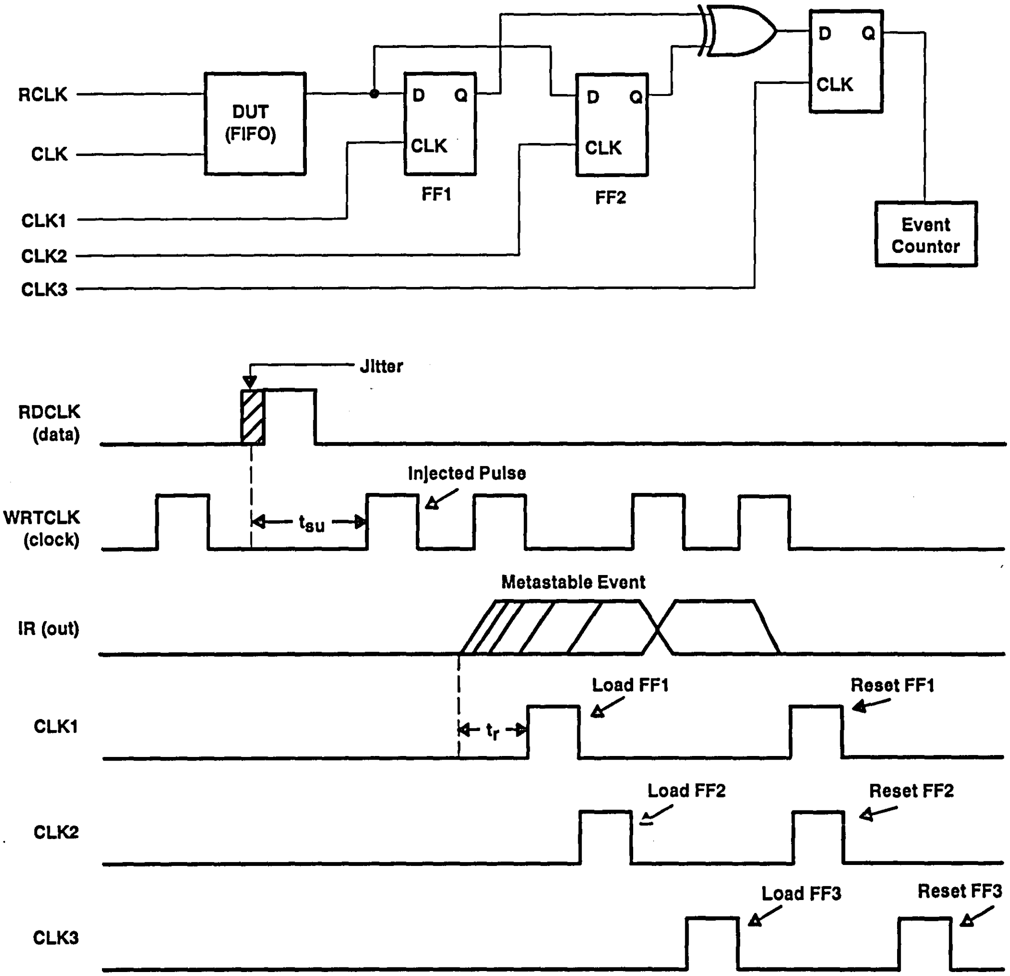

Figure 4. Metastable Event Counter and Input Waveforms

Test Results

Table 1. SN74ABT7819 Failure Rates†

RESOLVE TIME, t_{r2} (ns)	NUMBER OF FAILURES/HOUR	NUMBER OF FAILURES/SECOND	MTBF (seconds)
0.27	890	0.2472	4.04
0.39	609	0.1692	5.91
0.53	396	0.1101	9.08

† V_{CC} = 4.5 V, T_A = 25°C

After measuring the metastable performance of the SN74ABT7819, some assumptions must be made in order to calculate the parameters τ and t_0. Because the individual flip-flops comprising the two-stage synchronizer cannot be measured separately, it is first assumed that the values for τ and t_0 are the same for both. This is a safe assumption, as these constants are driven by the process technology and because the schematics are identical. The other assumption made involves determining the resolve time allowed in the first stage of the synchronizer. The clock period is set at 5.24 ns, but the delay through the flip-flop and the setup time to the next stage must be subtracted from the clock period to arrive at the true resolve time (t_{r1}). These values could not be measured directly and were, therefore, estimated from SPICE analysis to be 1.3 ns.

Using equation 4 and the measured failure rates to calculate τ results in a value of 0.33 ns for the conditions given. The following values from the test setup must be used in order to solve for t_0:

Where:

t_{r1} = 3.94 ns (5.24-ns clock period – 1.3-ns setup and delay time)
t_{r2} = 0.27 ns (set externally at IR output by CLK1)
f_c = 40 MHz
f_d = 125 MHz (4-MHz input adjusted by 25/0.8 jitter ratio)
$MTBF^2$ = 4.04 s

Substituting these values into equation 4 and solving for t_0 yields a value of 16.9 ps.

The table below summarizes the results for the SN74ABT7819 and SN74ACT7807 clocked FIFOs. An internal setup and delay time of 1.8 ns was assumed for the SN74ACT7807.

Table 2. Values of τ and t_0 for SN74ABT7819 and SN74ACT7807

T_A	V_{CC}	SN74ABT7819		SN74ACT7807	
		τ (ns)	t_0 (ps)	τ (ns)	t_0 (ps)
25°C	4.5 V	0.33	16.9	0.50	1.13
	5 V	0.30	7	0.40	2.05
	5.5 V	0.23	28.8	0.30	9.40

A word of caution: these numbers indicate the performance of only a few devices and are not intended to represent a fully characterized parameter. However, they should be valid for the purpose of relative performance comparisons, and the values do fall within the expected range given the circuit configuration and process technology in which the devices are fabricated.

MTBF Comparison

With the constants τ and t_0 now known, calculations of the MTBF of the device under different operating conditions may be performed. First, however, consider an example of the metastability performance of a single-stage synchronizer using equation 1 and the circuit constants τ and t_0 from Table 2. Assume an application running with a 33-MHz write clock, an 8-MHz read clock, a 9-ns maximum propagation delay time for the IR path, and a 5-ns setup time for IR to the next device. Therefore:

t_r = 16 ns (30-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 33 MHz
f_d = 8 MHz

Using equation 2 to calculate the MTBF gives 2.55 y 10^{17} seconds or a little bit more than 8 billion years.

The reliability of a one-stage synchronizer degrades as operating frequency increases. With a 50-MHz write clock, a 12-MHz read clock, a 9-ns maximum delay, and a 5-ns setup time:

t_r = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 50 MHz
f_d = 12 MHz

Substituting these values into equation 2 yields an MTBF of about 2 hours. This performance is unacceptable, even with a device fabricated in the 0.8-mm BiCMOS process, which is more resistant to metastability than other processes.

The benefits of two-stage synchronization become evident with the next example. Using the conditions stated in the last example:

t_{r1} = 18.7 ns (20-ns clock period – 1.3-ns setup and delay time)
t_{r2} = 6 ns (20-ns clock period – 9-ns propagation delay – 5-ns t_{su})
f_c = 50 MHz
f_d = 12 MHz

Using equation 4 to calculate the MTBF gives 3.16 y 10^{28} seconds or 1.00 y 10^{21} years.

Table 3 gives a performance summary of both one- and two-stage synchronizing solutions under different conditions.

Table 3. MTBF Comparisons†

CONDITIONS	ACT 1 STAGE	ABT 1 STAGE	ACT 2 STAGE	ABT 2 STAGE
f_c = 33 MHz, f_d = 8 MHz	8400 years	8.1 × 10^9 years	2.62 × 10^{28} years	4.77 × 10^{47} years
f_c = 40 MHz, f_d = 10 MHz	92 days	1400 years	3.56 × 10^{19} years	2.18 × 10^{34} years
f_c = 50 MHz, f_d = 12 MHz		2 hours	4.90 × 10^{10} years	1.00 × 10^{21} years
f_c = 67 MHz, f_d = 16 MHz			417 years	1.28 × 10^9 years
f_c = 80 MHz, f_d = 20 MHz				2900 years

† Assumptions for the MTBF comparisons:

1) The values for t_0 and τ are those given previously for both the ABT and ACT devices with V_{CC}= 4.5 V, T_A = 25°C.
2) Flag propagation delay time (IR or OR) is assumed to be 9 ns.
3) Setup times to the next device are 5 ns (up to 50-MHz operation), 4 ns (up to 67-MHz operation), and 3 ns (up to 80-MHz operation).

Conclusion

Metastability failures must be accounted for in the design of asynchronous digital circuits. These failures become increasingly prevalent at higher operating frequencies. When higher frequencies are used, extreme care must be taken to ensure that system reliability is not adversely affected due to inadequate synchronization methods.

Clocked FIFOs from Texas Instruments provide a solution to this problem by synchronizing the boundary flags with at least two flip-flop stages to improve the metastable MTBF over one-stage synchronization. This architecture allows designers to utilize the high-throughput performance of the memory without endangering the reliability of their end products.

Footnotes

1. J. Horstmann, H. Eichel, and R. Coates, "Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test," IEEE Journal of Solid State Circuits, February 1989, p. 146.
2. H. Veendrick, "The Behavior of Flip-Flops Used as Synchronizers and Prediction of Their Failure Rate," IEEE Journal of Solid State Circuits, April 1980, p. 169.
3. S. T. Flannagan, "Synchronization Reliability in CMOS Technology," IEEE Journal of Solid State Circuits, August 1985, p. 880.
4. T. Kacprzak and A. Albicki, "Analysis of Metastable Operation in RS CMOS Flip-Flops," IEEE Journal of Solid State Circuits, February 1987, p. 59.
5. L. Kleeman and A. Cantoni, "Metastable Behavior in Digital Systems," IEEE Design and Test of Computers, December 1987, p. 4.

Acknowledgement

This application report was authored by Chris Wellheuser, Advanced System Logic – Semiconductor Group, Texas Instruments Incorporated.

FIFO Memories:
Solution to Reduce FIFO Metastability

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As system operating frequencies continue to increase in excess of 33 MHz, designers must begin to address the issues of overall system reliability due to increased chance of a metastable event occurring. A metastable event is defined as the time period when the output of a logic device is neither at a logic H nor at a logic L but rather in an indeterminate level. The chance of a metastable occurrence is exponentially increased if single-stage synchronization is employed, as in the case of the '722xx sync-style devices versus the two-stage synchronization that is implemented by Texas Instruments (TI) (see Figure 1). The following information assists designers in understanding and to improve upon the metastable characteristics of '722xx sync-style devices and their reliability.

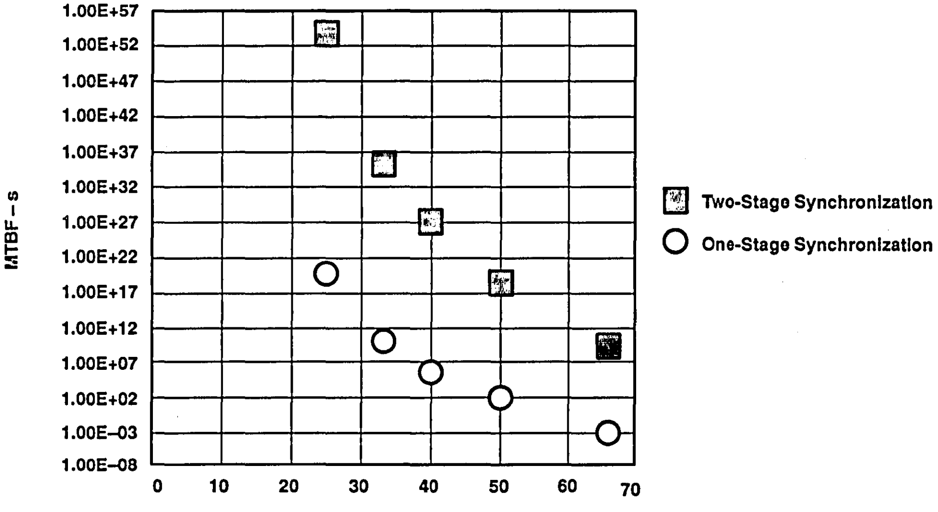


Figure 1. MTBF for Metastability as a Function of Frequency

Metastability may occur when using a FIFO to synchronize two digital signals operating at different frequencies. This type of application is a familiar one to many design engineers. Triggering a metastable event is common in single-stage (single flip-flop) synchronized FIFOs that are used to synchronize different clock signals (see Figure 2). With this method, the asynchronous input might change states too close to the clock transition, violating the flip-flop's setup and hold times. This causes an increase in resolve time (t_r) which then results in an overall increase in propagation delay (t_{pd}). Once a metastable event is triggered, the probability of the output recovering to a *high* or *low* level increases exponentially with the increased resolve time. The expected time until the output of a single flip-flop with asynchronous data has a metastable event is described by the mean time between failure (MTBF) equation (see equation 1). The first term of the equation is the probability that the asynchronous data will trigger a metastable event. The second term is the data rate. The third and final term is the probability of the metastable event recovering given the resolve time. A linear increase in resolve time exponentially increases the MTBF of a metastable event.

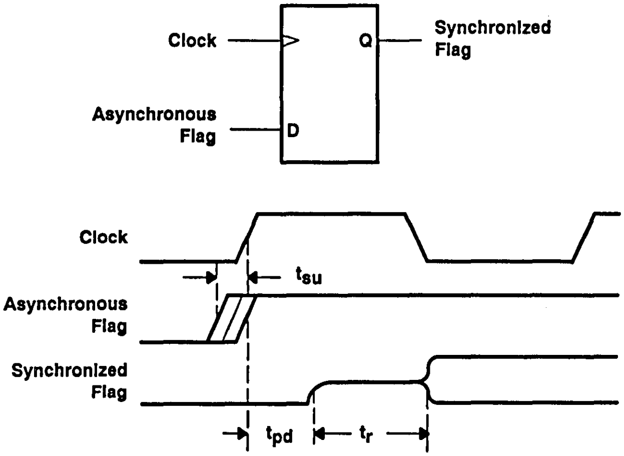


Figure 2. Single-Stage Synchronizer

$$MTBF_1 = \frac{1}{t_o f_c} \times \frac{1}{f_d} \times exp\left(\frac{t_r}{\tau}\right) \tag{1}$$

Where:

t_o = flip-flop constant representing the time window during which changing data invokes a failure
t_r = resolve time allowed in excess of the normal propagation delay
τ = flip-flop constant related to the settling time of a metastable event
f_c = clock frequency
f_d = asynchronous data frequency. (For OR-flag analysis, it is the frequency at which data is written to empty memory. For IR-flag analysis, it is the frequency at which data is read from full memory.)

TI has increased the metastable MTBF by several orders of magnitude over single-stage synchronization with its advanced FIFO family by employing two-stage synchronization (see Figure 3). The output of the first flip-flop is clocked into the second flip-flop on the next clock cycle. For the output of the second stage to become metastable, the first stage must have a metastable event that lasts long enough to encroach upon the setup time of the second stage. The addition of the second flip-flop to the single-stage synchronizer allows the flip-flops more time to resolve any metastable output. This is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. The mean time between failure for a two-stage synchronizer is given in equation 2. All terms, except for the third one, are the same as in equation 1. The third term represents the additional propagation delay through the added flip-flop.

$$MTBF_2 = \frac{1}{t_o f_c} \times \frac{1}{f_d} \times exp\left[\frac{\frac{1}{f_c} - t_{pd}}{\tau}\right] \times exp\left(\frac{t_r}{\tau}\right) \tag{2}$$

t_{pd} = propagation delay through the first flip-flop
$MTBF_2$ = $MTBF_1$

Where:

t_r = $t_r + (1/f_c - t_{pd})$

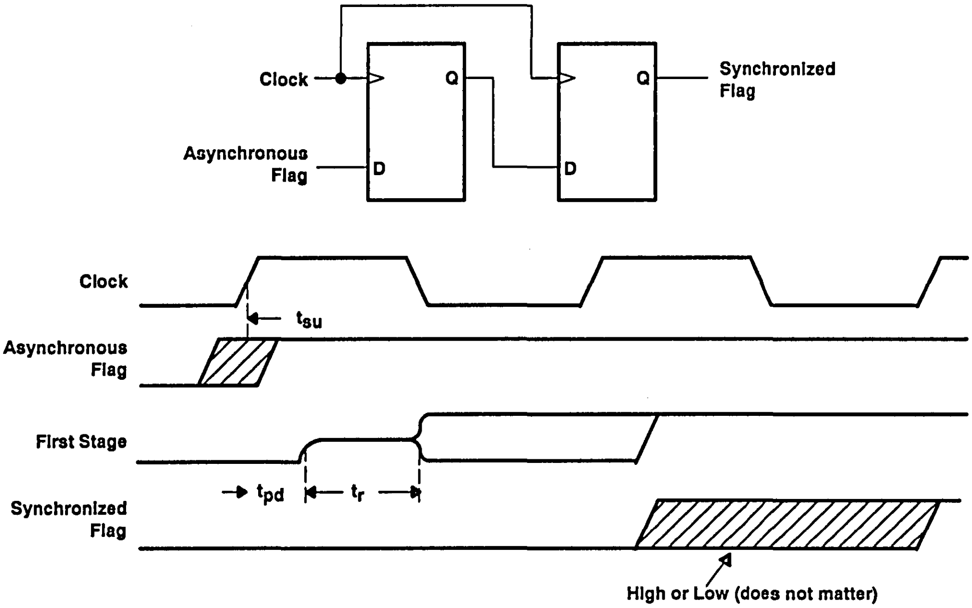


Figure 3. Two-Stage Synchronizer

The functional block diagram in Figure 4 illustrates the connections necessary to add the second-stage synchronization to the '72211 sync FIFO. In Figure 5, a quick and inexpensive schematic to resolve metastability of a sync FIFO is diagrammed. In this case, the FIFO is the '72211LJ and, by implementing a single TI SN74F74 D-type positive-edge-triggered flip-flop and a TI SN74F08 two-input positive AND gate, the metastability characteristics of this circuit can be dramatically improved. The TI SN74F74 acts as the second stage for this circuit, increasing the resolve time as described in the above paragraphs. The TI SN74F08 is implemented to act as the control-empty and control-full flags to the receiving device. These control lines of the first-stage and second-stage synchronized flags are then ANDed together to create the control flags (control empty and control full). The control lines are essentially read enables that ensure the synchronization of the device. As is demonstrated by the logic diagram and truth table, synchronization is complete only when the empty flags ($\overline{EF}$) of both the second stage (truth table input A) and the device (truth table input B) are high. The empty flag is used for read control, and the full flag ($\overline{FF}$) is used for write control. If either flag from the synchronizer or the device is held low or becomes metastable, a read is not permitted (truth table output Y) until the write flag is synchronized.

As can be seen in today's digital systems, synchronous and asynchronous operations can and will produce random errors due to metastability in single-stage FIFO designs like those of the '722xx sync FIFO family. The described method of implementing a second stage for flag synchronization is extremely useful for clock speeds that are either approaching or exceeding 33 MHz. Metastability can be virtually eliminated in the '722xx sync FIFO family by the simple addition of a second flip-flop. The second-stage synchronizer greatly reduces metastability, thereby increasing the MTBF and allowing designers to use faster microprocessors and higher data-transfer rates for greater overall system performance and reliability.

To reduce metastability and improve system reliability, TI offers a complete line of high-performance FIFO memory devices. TI's FIFOs have dual-stage synchronization designed onto each chip. This eliminates the need for any external discrete solution and reduces critical board space by fully utilizing TI's family of fine-pitch surface-mount packaging.

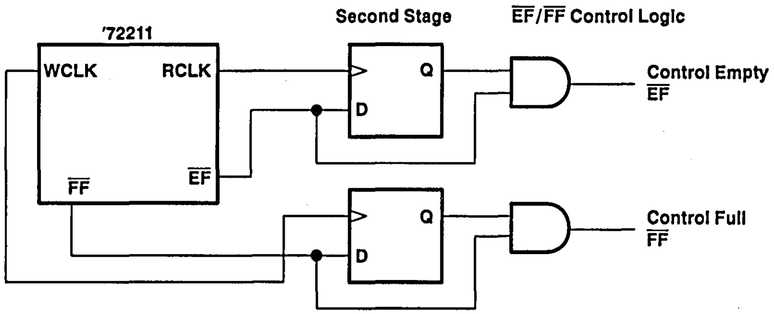
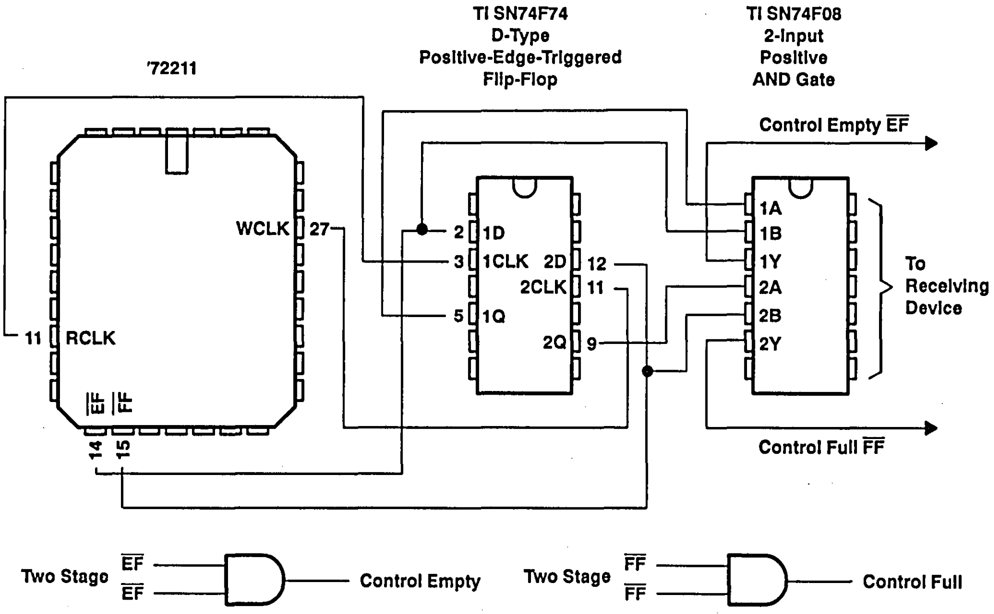


Figure 4. Connecting the Second-Stage Synchronizer to the '72211 Sync FIFO



INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

Figure 5. Resolving Metastability of a Sync FIFO

Acknowledgement

This application note was authored by Tom Jackson, Advanced System Logic – Semiconductor Group, Texas Instruments Incorporated.

1K × 9 × 2 Asynchronous FIFOs SN74ACT2235 and SN74ACT2236

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Contents

List of Illustrations

Introduction

Texas Instruments (TI) designed the SN74ACT2235 to meet a variety of synchronous or asynchronous bidirectional applications. Two 1K x 9 first-in, first-out (FIFO) memories are arranged in parallel to buffer data in opposite directions. Data ports may also exchange real-time data. Three-state control (GAB, GBA) and real-time/stored data select (SAB, SBA) match the popular '652 transceiver logic. Produced in TI's EPIC™ CMOS process, the inputs accept TTL-voltage levels. An option to the 'ACT2235 is the 'ACT2236, which has '646 transceiver control (DIR, $\overline{G}$). The functional block diagram for the SN74ACT2235 is shown in Figure 1.

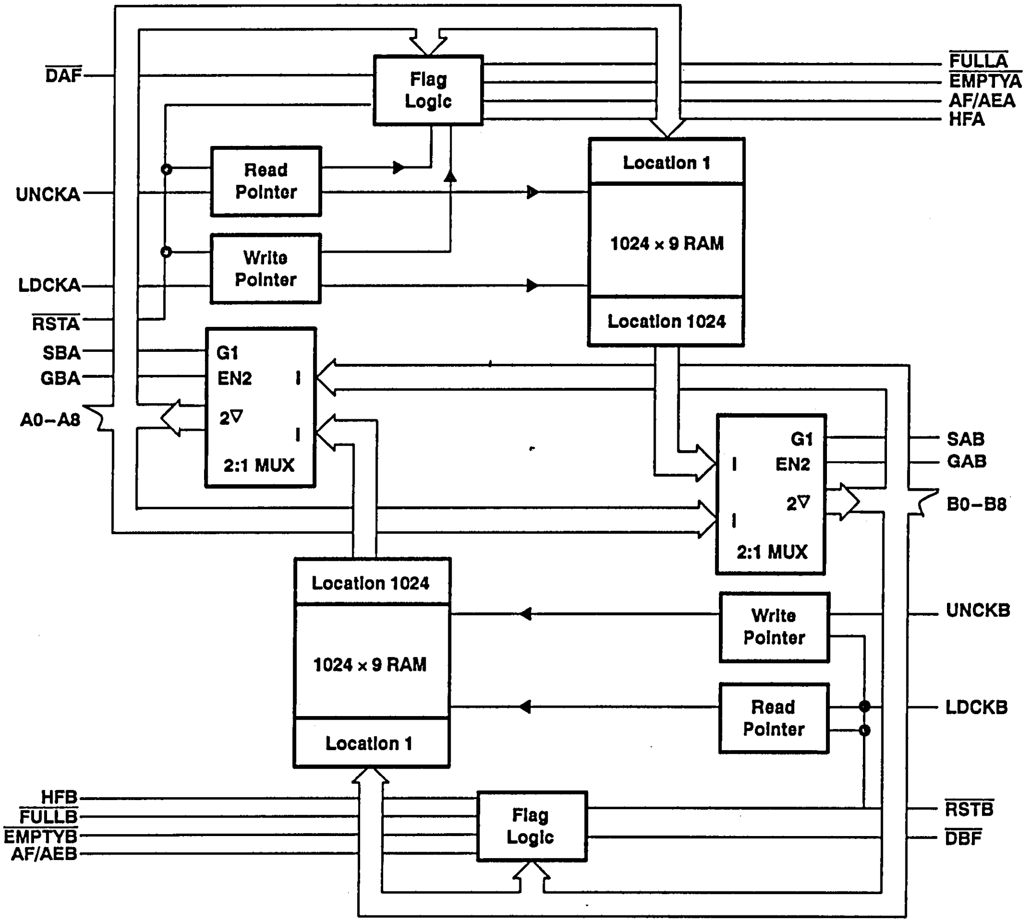
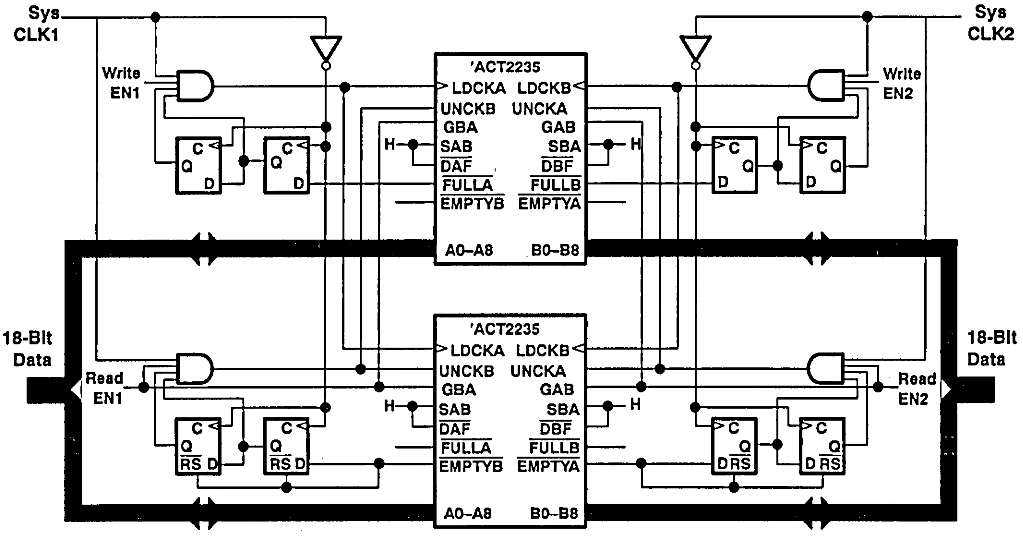


Figure 1. SN74ACT2235 Block Diagram

FIFO Control

The 'ACT2235 consists of two FIFO memories, FIFOA and FIFOB. Both FIFOs can be accessed from either port A or port B. Four control signal lines (GAB, GBA, SAB and SBA) control the eight possible data flow paths through the device (these data paths are illustrated in the device data sheet). Each FIFO has a load clock (LDCK) that writes data into memory and an unload clock (UNCK) that reads the data in the same order it was written. Both clocks are positive-edge-triggered and may operate asynchronously to one another. The first word loaded into an empty FIFO propagates directly to the outputs and the $\overline{\text{EMPTY}}$ flag switches high. $\overline{\text{EMPTY}}$ represents the valid state of data on the outputs (data is valid when $\overline{\text{EMPTY}}$ is high and invalid when $\overline{\text{EMPTY}}$ is low). $\overline{\text{EMPTY}}$ may be used to enable an UNCK pulse when it is synchronized with the bus that reads the data. $\overline{\text{FULL}}$ can qualify a LDCK pulse in the same way.

Figure 2 is an example of an 'ACT2235 interfacing two asynchronous systems. Each system provides a read enable, write enable, and free-running clock. Synchronization of a flag to the system clock is needed to use it as device clock control. Although the flag's high-to-low transition is synchronous to the clock it enables, the low-to-high transition is asynchronous. The output of the latch qualifying this transition has the possibility of going metastable when bistable (setup and hold) conditions are not met. An output is metastable if it lingers between the specified V_{OH} and V_{OL} levels. Two-stage synchronization of the flags reduces the probability of a metastable-induced failure.



NOTE: Two devices are used for 18-bit width expansion.

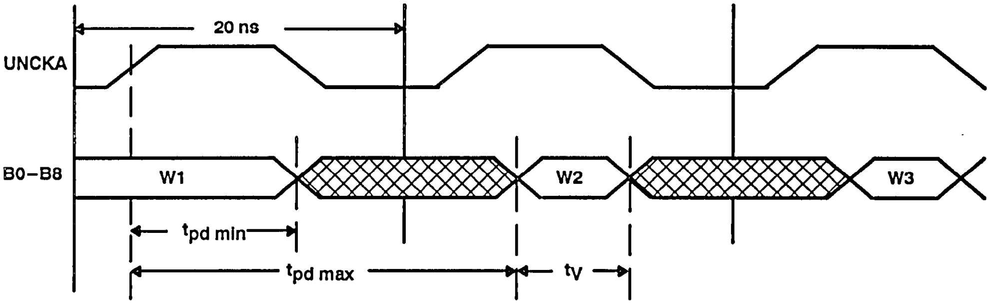
Figure 2. Controlling the 'ACT2235 Using a Clock, Write Enable, and Read Enable Per System

High-Frequency Applications

A unique feature of the 'ACT2235 is that the UNCK cycle time may be less than the device access time. The 'ACT2235-20 has a maximum LDCK and UNCK frequency of 50 MHz (20-ns cycle time) and a 25-ns maximum access time (t_{pd} UNCKA or UNCKB to B bus or A bus). In a series of FIFO reads, the next access may be initiated before the present one is complete. The largest concern associated with this technique is the length of time data will be assured as valid. Minimum access time from the rising edge of UNCK may also be viewed as minimum data hold time. Timing for this relationship is shown in Figure 3. Valid data time from the 'ACT2235 over the commercial temperature range and ±10% V_{CC} is given by equation 1:

$$t_v = t_c + t_{pd}\text{min} - t_{pd}\text{max} \qquad (1)$$

Data from an 'ACT2235 operating at a 50-MHz clock frequency is valid for at least 7 ns. This allows a 4-ns setup and 1-ns hold with a 2-ns tolerance to the next device in the data path.



For 'ACT2235-20: $t_{pd\ min}$ = 12 ns, $t_{pd\ max}$ = 25 ns, t_V = 7 ns

Figure 3. Read Operation When Cycle Time Is Less Than Access Time

Programmable Flags

Data is often transmitted in packets, where each packet is a specific number of bytes and must be delivered in an unbroken stream. A FIFO transmitting packeted data needs a flag that shows the number of bytes stored. This keeps from breaking the transmission of a packet due to an empty or full condition. The 'ACT2235 has a programmable almost-full/almost-empty flag for this application. The AF/AEA offset value (X) and the AF/AEB offset value (Y) are programmed separately. AF/AEA is high when FIFOA contains X or fewer words or (1024 – X) or more words. It is low when FIFOA contains between (X + 1) and (1023 – X) words. AF/AEB functions in the same manner with its programmed value Y. The programmed or default value of 256 is chosen during a reset of each FIFO.

Flag programming logic is illustrated in Figure 4. Programming the AF/AE flag value for each FIFO is done with the define-flag ($\overline{\text{DAF}}$, $\overline{\text{DBF}}$) inputs and resets ($\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$). Define-flag inputs are negative-edge-triggered clocks that store input data to a register. If $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ is low when the rising edge of $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ occurs, the registered value is used for the FIFO's AF/AE flag. The flag uses the default value of 256 if $\overline{\text{DAF}}$ or $\overline{\text{DBF}}$ is high during the rising edge of $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$.

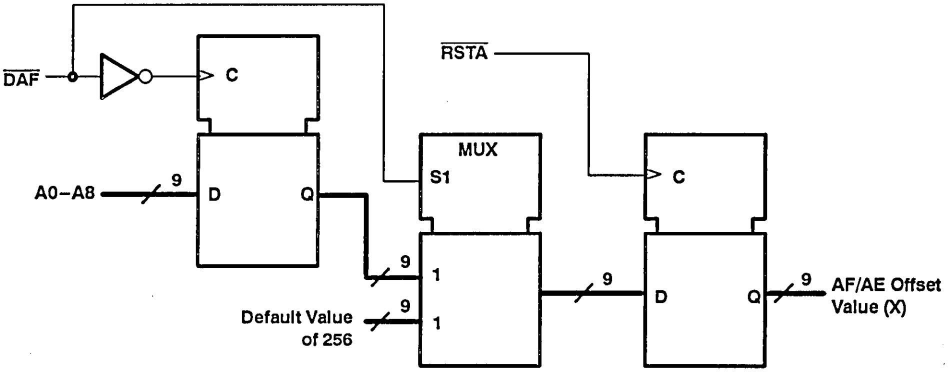


Figure 4. AF/AEA Flag Programming Logic for FIFOA

Programming both flag offset values from either port is possible using real-time select. Figure 5 is a timing example of programming AF/AEB from port A. To program the AF/AEB offset value (Y) from port A, the binary value for Y is on A0–A8, SAB is low, and GAB is high. With this configuration, the port-A data appears on the inputs of FIFOB and a falling edge of $\overline{\text{DBF}}$ stores the Y value.

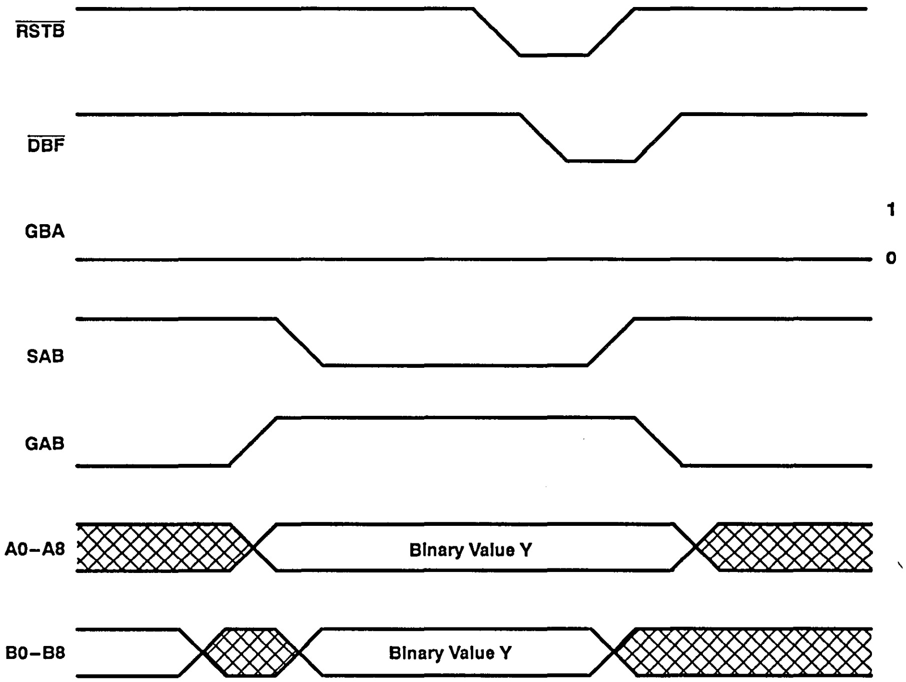


Figure 5. Programming AF/AEB Flag of FIFOB From Port A

Output Drive

Charging and discharging the load of a bus with acceptable speed requires high device-output drive. The I/O ports of the 'ACT2235 provide 16-mA I_{OL} and 8-mA I_{OH} for this task.

Most memory devices have low drive capability and require buffers to interface a bus. They do not use larger transistors that support high current because the rate of change of current with respect to time (di/dt) increases. When several transistors switch simultaneously, the rate of change of current through ground and V_{CC} lines multiplies. Voltage transients on the power lines are given by equation 2:

$$V = -L \; di/dt \tag{2}$$

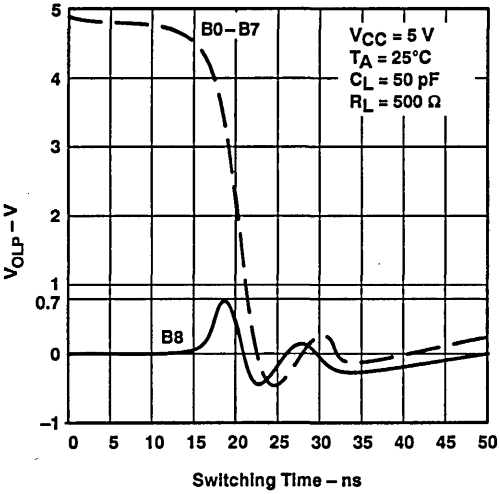
Where:

L = inductance of the bond wire and package lead

The 'ACT2235 provides a two-fold solution to allow high output current capability with low noise. One solution is to reduce inductance of ground and V_{CC} lines. The 'ACT2235 has four GND and two V_{CC} pins in parallel. The resulting ground inductance is about 1/4 that of a single connection and divides V_{CC} inductance in half.

Reducing di/dt per output transistor is another way to minimize voltage transients. TI's patented output edge control (OEC™) design divides a large transistor into smaller segments that turn on in series and turn off simultaneously. OEC™ lowers di/dt, maintains a quick voltage transition through threshold, and avoids the high power consumed when gradually turned off.[1]

The result of a V_{OLP} test on the 'ACT2235 is shown in Figure 6. V_{OLP} is a measurement of ground voltage noise when all outputs of a bus are switched from high to low. Eight of nine outputs of a bus are switched, and the peak voltage rise of the steady state low output is measured. Maximum ground voltage rise is only 700 mV. The output fall time is less than 3 ns with a 50-pF load.



NOTE: Eight bus outputs switching, one remains low

Figure 6. 'ACT2235 V_{OLP} Measurement

Conclusion

The 'ACT2235 and 'ACT2236 provide several advantages for high-speed asynchronous bus interface. Simple control logic offers great design flexibility. Programmable flags may be used for data flow optimization. High-output drive for bus leading is balanced with noise reduction through package and circuit design.

Acknowledgement

This application note was authored by Kam Kittrell, Advanced System Logic – Semiconductor Group, Texas Instruments Incorporated.

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[1] Advanced CMOS Logic Designer's Handbook, pages 3–1 through 3–12.

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Multi-Q™ 18-Bit FIFO	2
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Contents

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 74ACT7803 -15 DL R

Prefix

SN = Standard prefix
SNJ = MIL-STD-883, Class B

Unique Circuit Description

MUST CONTAIN FIVE TO NINE CHARACTERS
(from individual data sheet)

Speed Sort

In nanoseconds

Package

MUST CONTAIN ONE TO THREE LETTERS

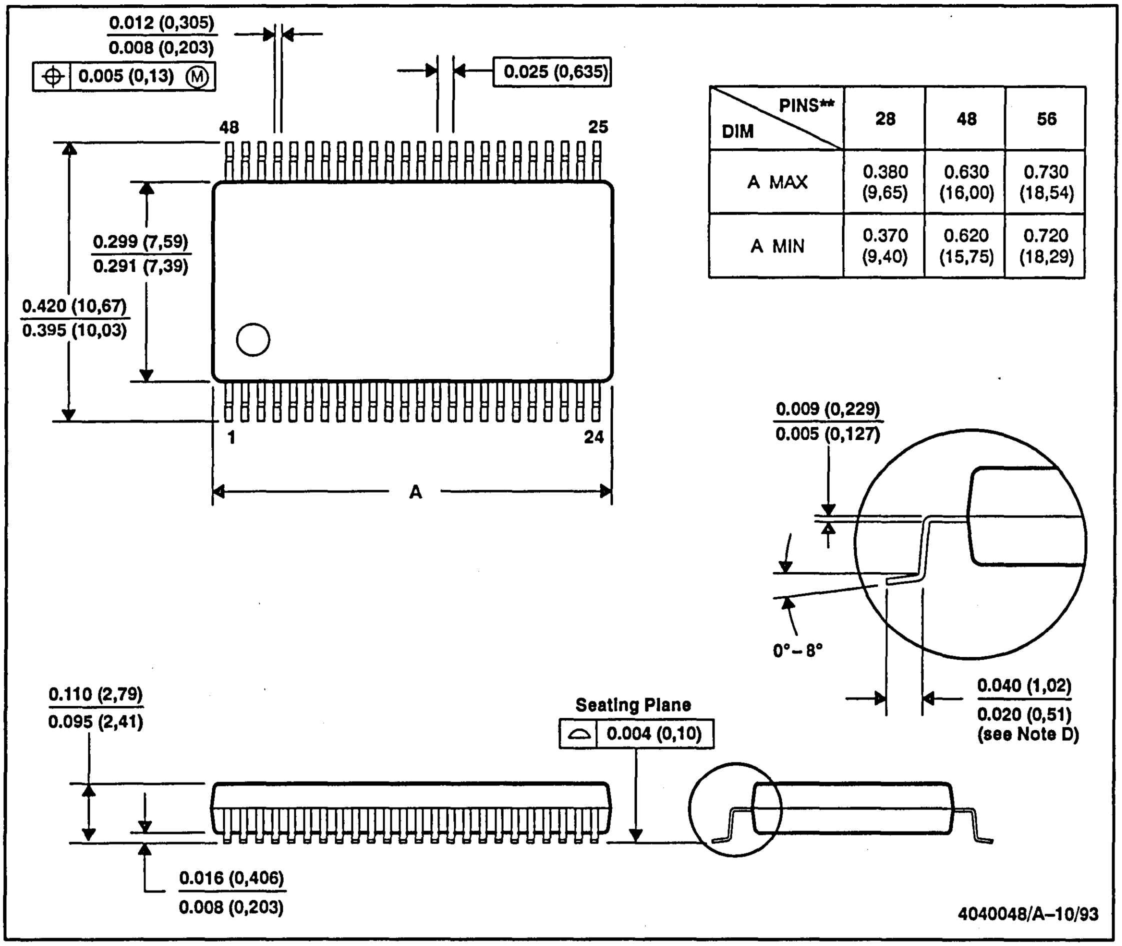
DL, DV, DW = plastic small-outline package (SOIC)
FN, RJ = plastic J-leaded chip carrier
N, NP, NT = plastic dual-in-line package
PH = JEDEC metric plastic quad flat package
PAG, PCB, PZ,
PM, PN = plastic thin quad flat package
PQ = JEDEC plastic quad flat package

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

DL/R-PDSO-G** **PLASTIC SHRINK SMALL-OUTLINE PACKAGE**

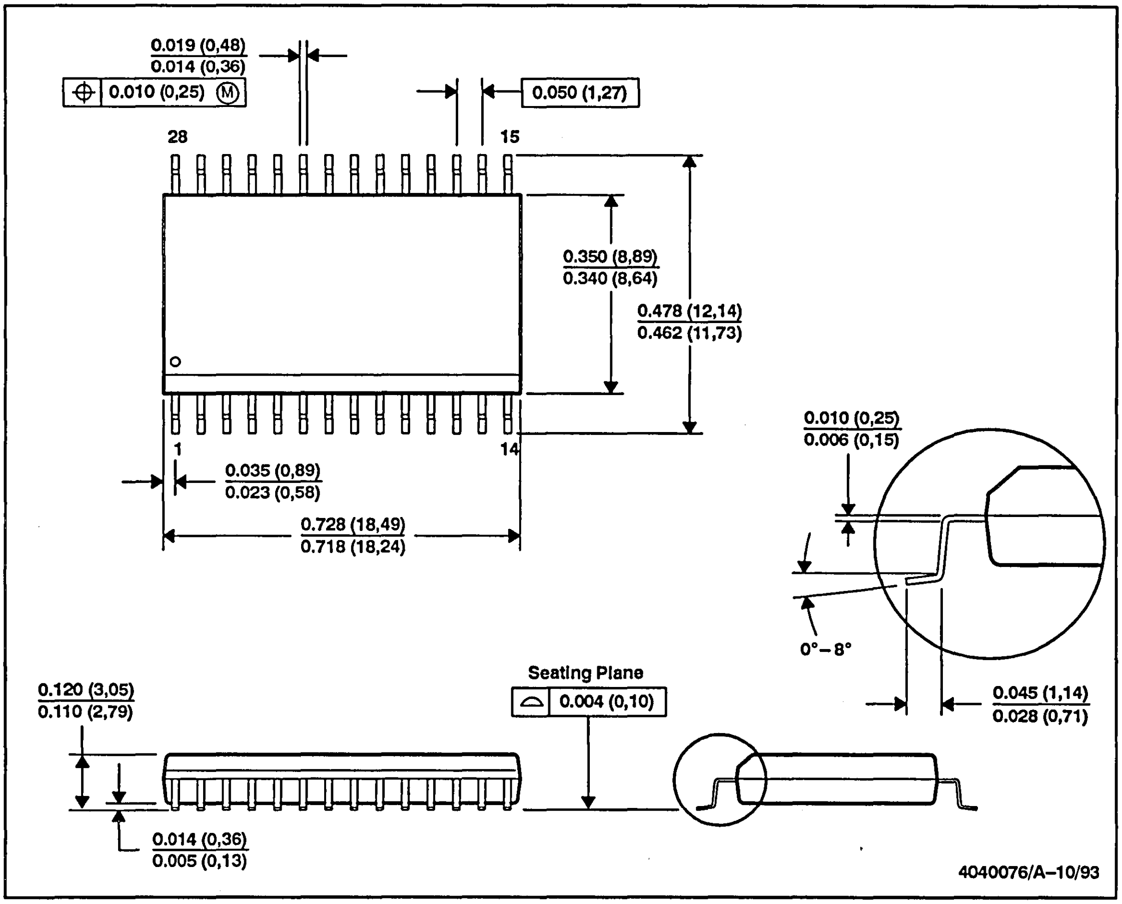
48-PIN SHOWN



PINS** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES:
- E. All linear dimensions are in inches (millimeters).
- F. This drawing is subject to change without notice.
- G. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- H. Foot length is measured from lead top to point 0.010 (0.254) above seating plane.

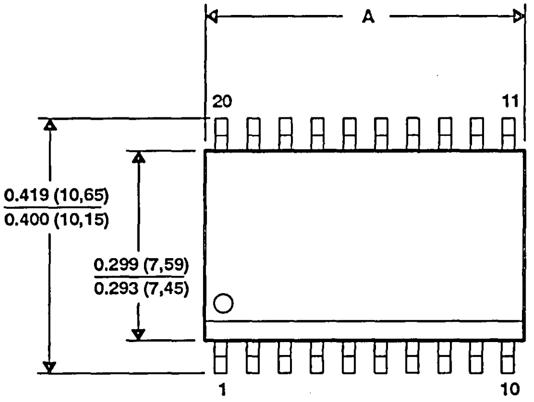
DV/R-PDSO-G28 **PLASTIC SMALL-OUTLINE PACKAGE**



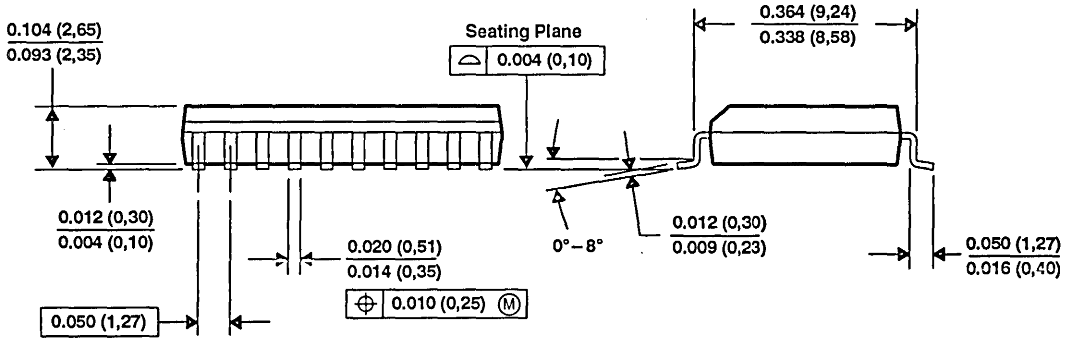
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

DW/R-PDSO-G** PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)



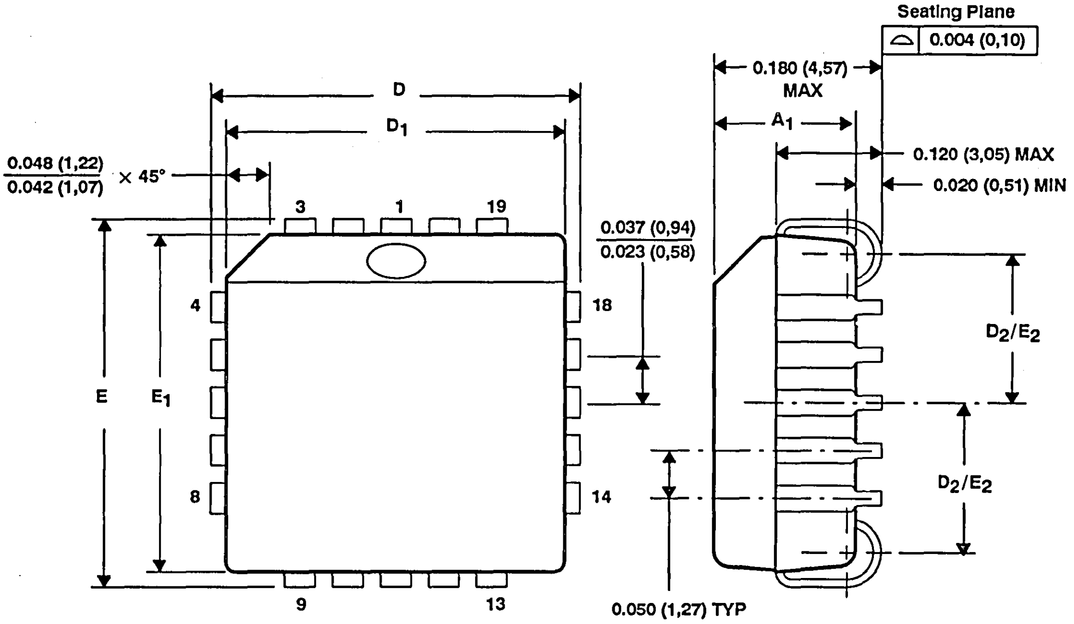
4040000/A–10/93

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

FN/S-PQCC-J**

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



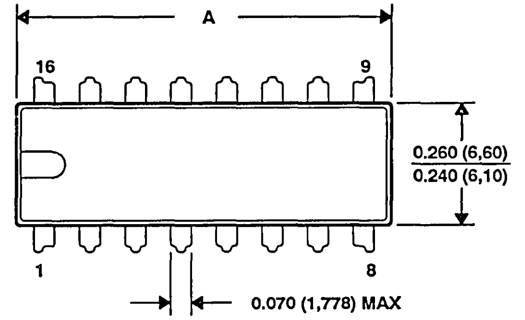
JEDEC OUTLINE	NO. OF PINS**	A_1		D/E		D_1/E_1		D_2/E_2	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
MS-018AA	20	0.062 (0,16)	0.083 (0,21)	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
MS-018AB	28	0.062 (0,16)	0.083 (0,21)	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
MS-018AC	44	0.062 (0,16)	0.083 (0,21)	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
MS-018AD	52	0.062 (0,16)	0.083 (0,21)	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
MS-018AE	68	0.062 (0,16)	0.083 (0,21)	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.441 (11,20)	0.469 (11,91)
MS-018AF	84	0.059 (0,15)	0.080 (0,20)	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/A–10/93

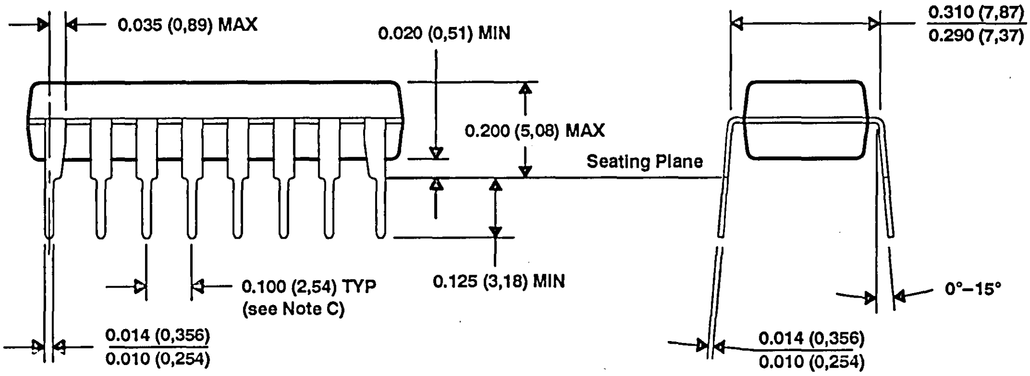
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

N/R-PDIP-T** PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



PINS** DIM	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

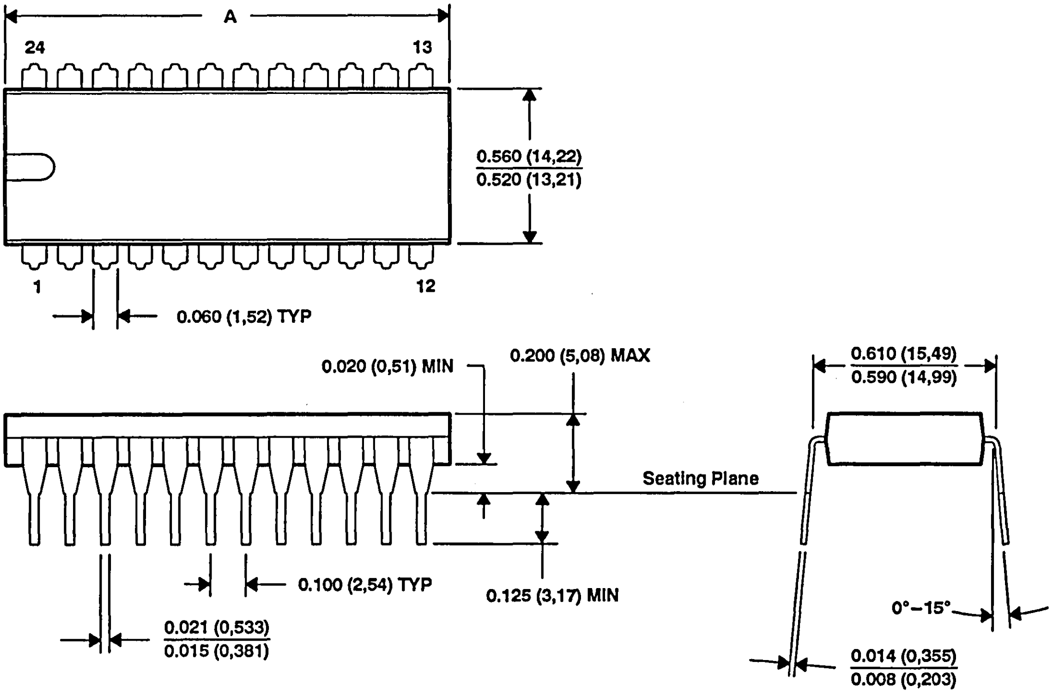


4040049/A–10/93

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

N/R-PDIP-T** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

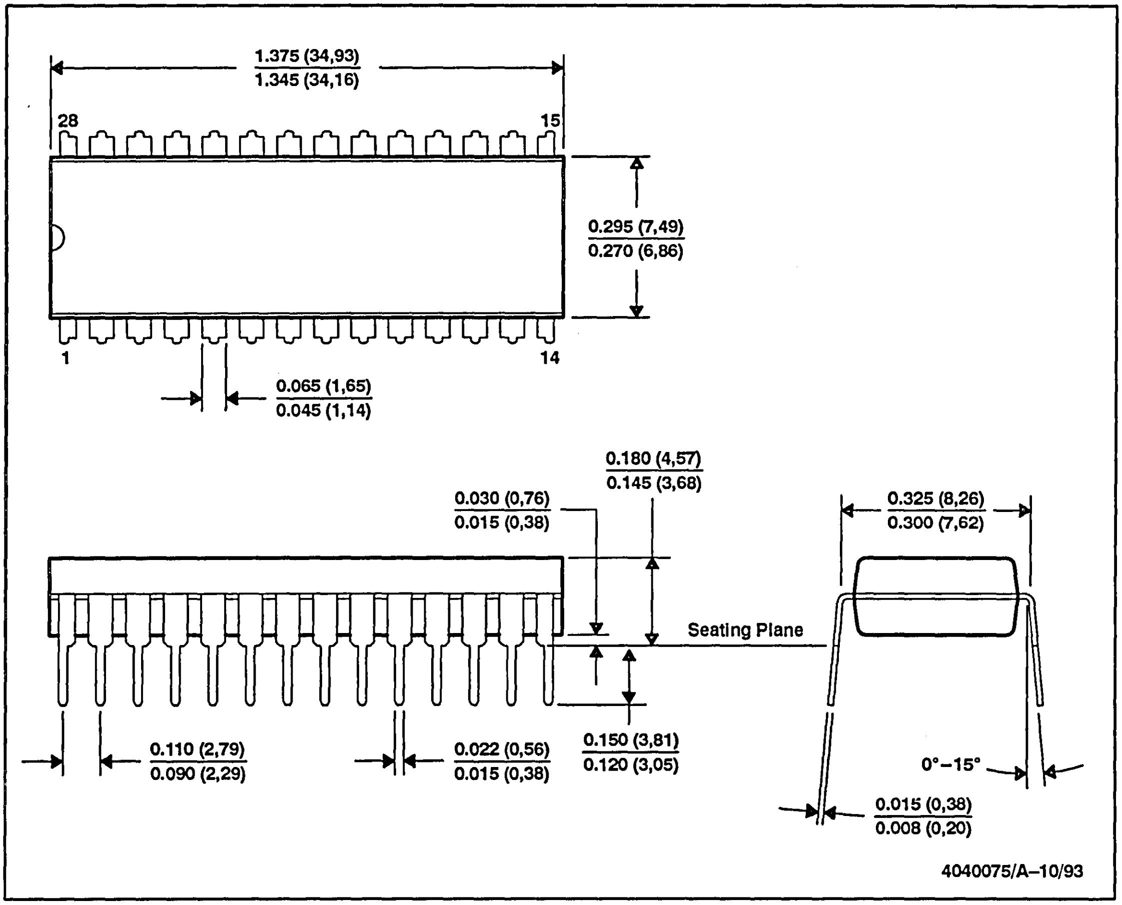


PINS ** DIM	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

NP/R-PDIP-T28 **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).

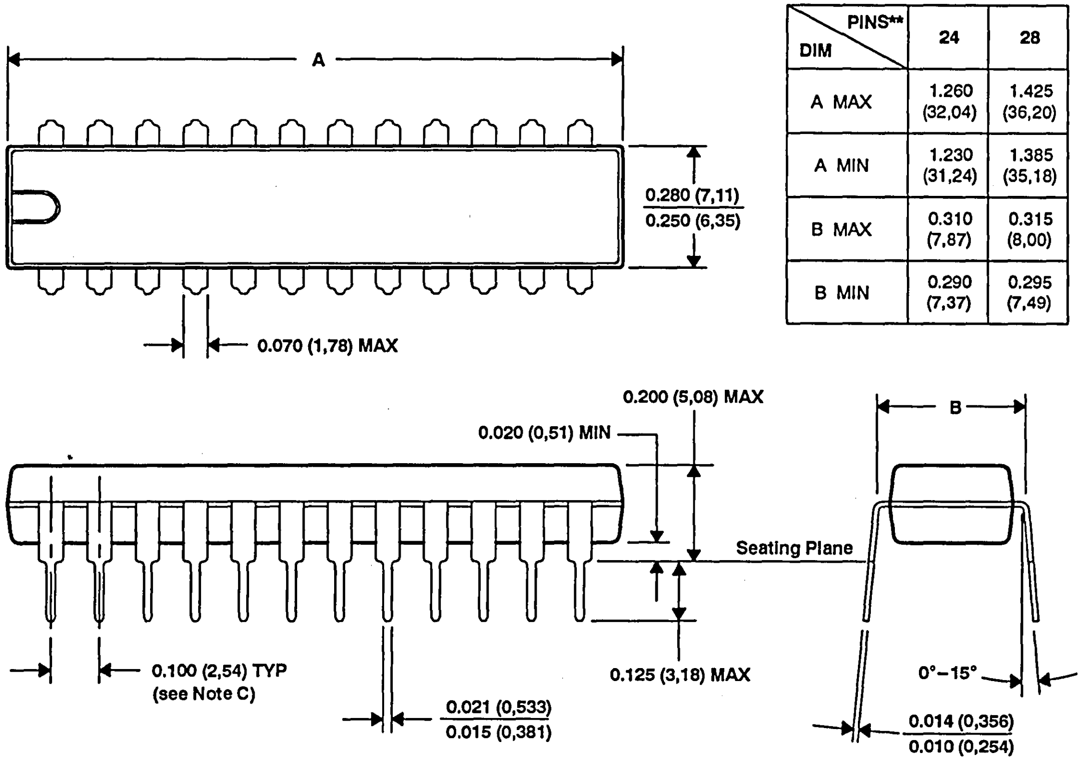
B. This drawing is subject to change without notice.

C. Body dimemsions do not include mold flash or protrusion.

NT/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

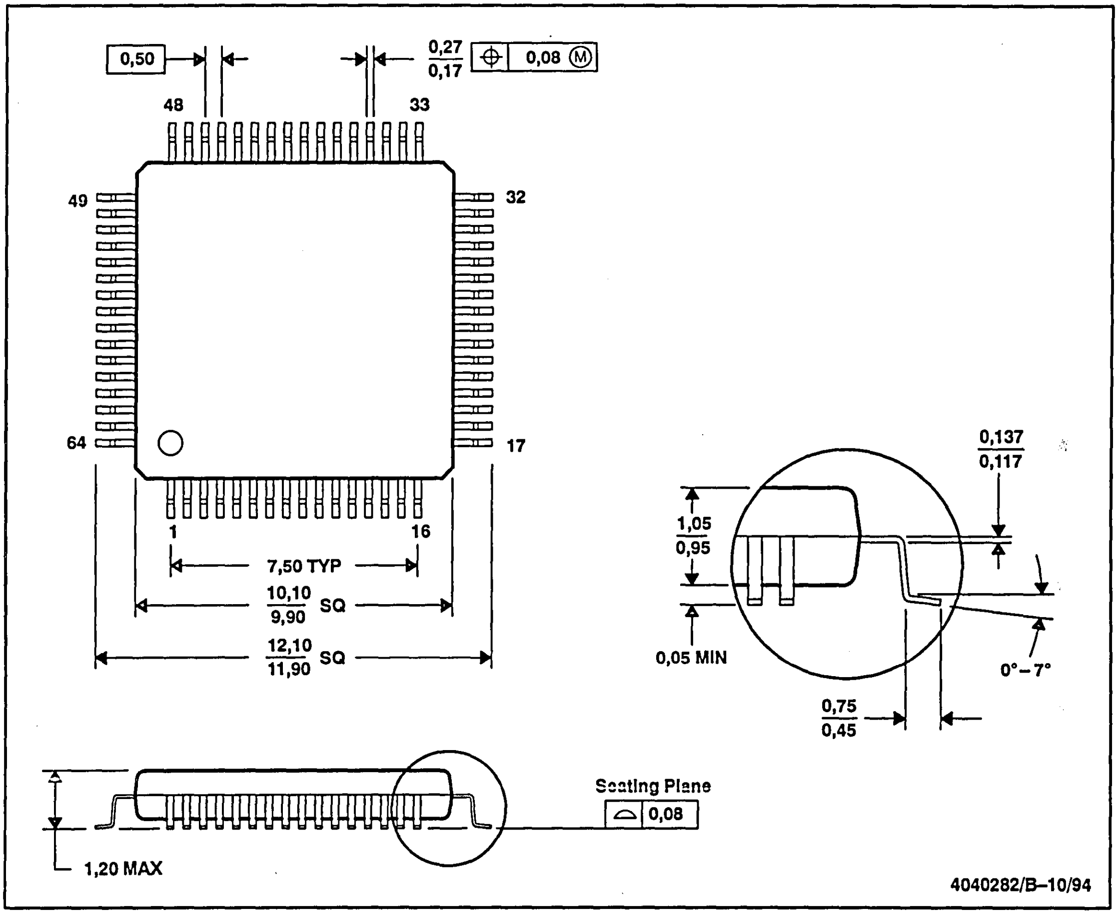


DIM \ PINS**	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

4040050/A–10/93

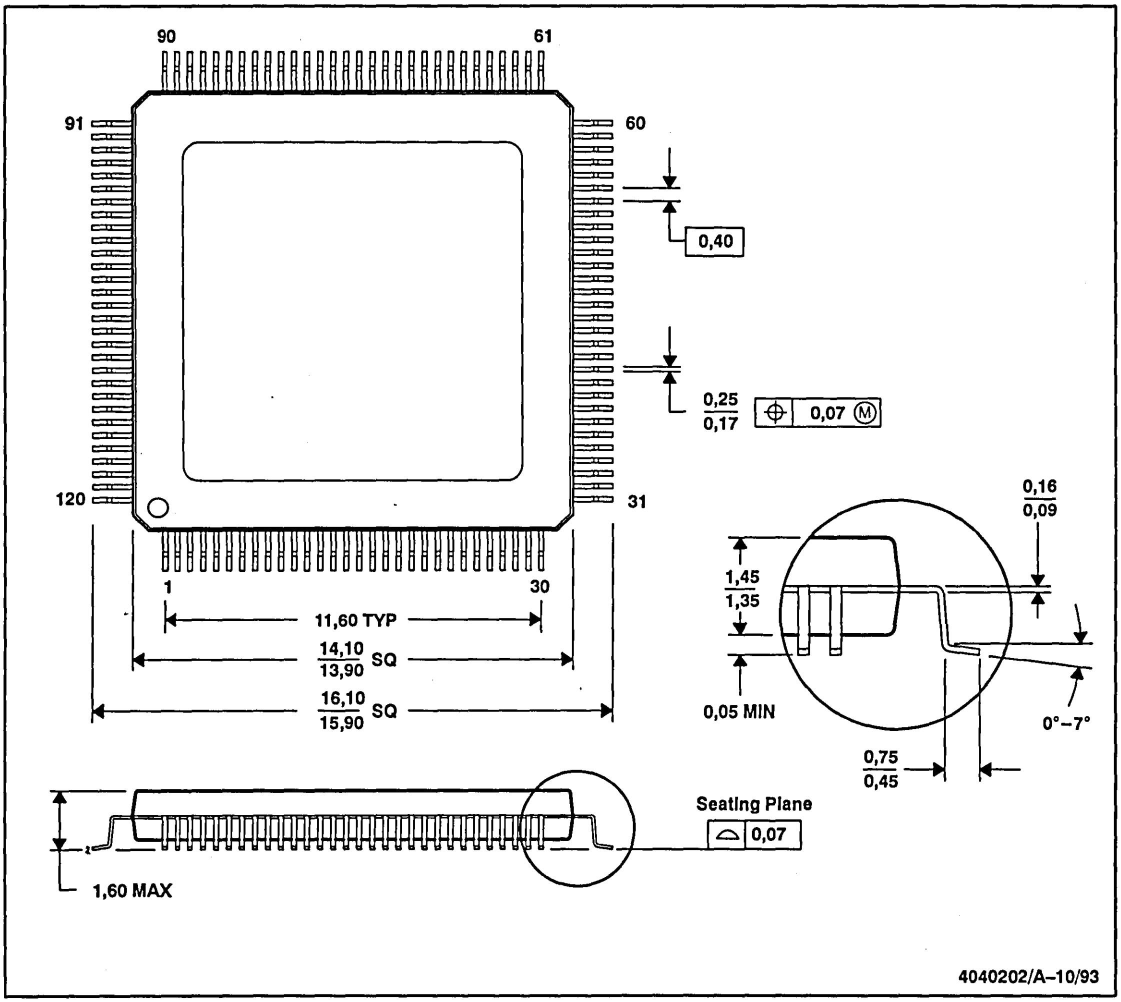
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

PAG/S-PQFP-G64 PLASTIC QUAD FLATPACK



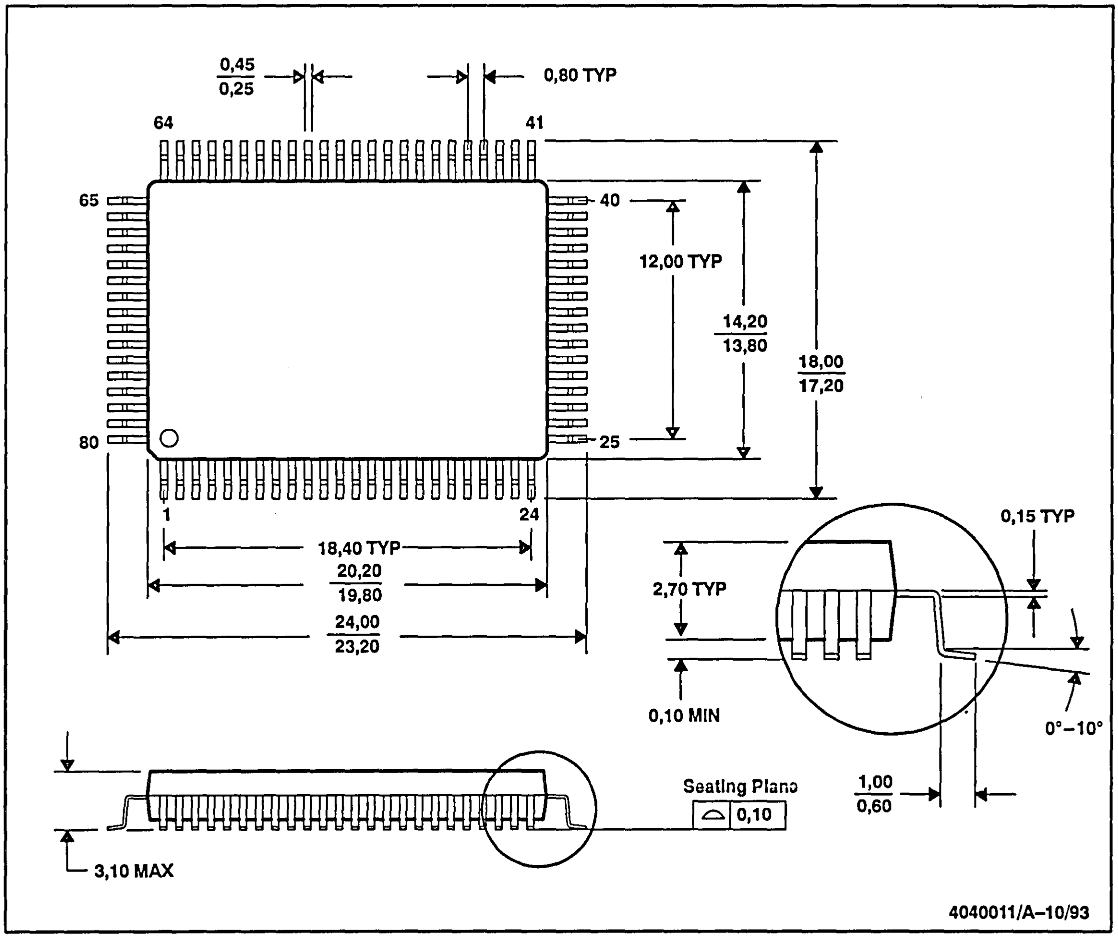
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PCB/S-PQFP-G120 **PLASTIC QUAD FLATPACK**



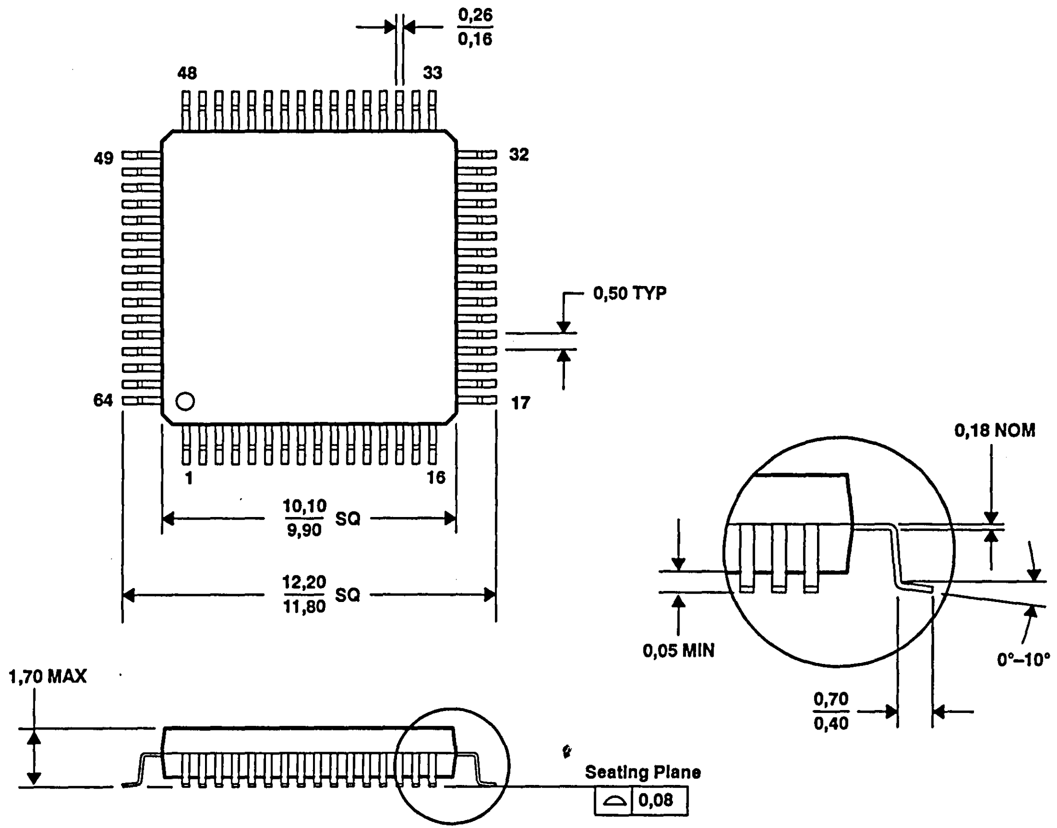
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Allowable protrusion is 0,25mm maximum per side.
- D. Thermally enhanced molded plastic package (HSP).

PH/R-PQFP-G80 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

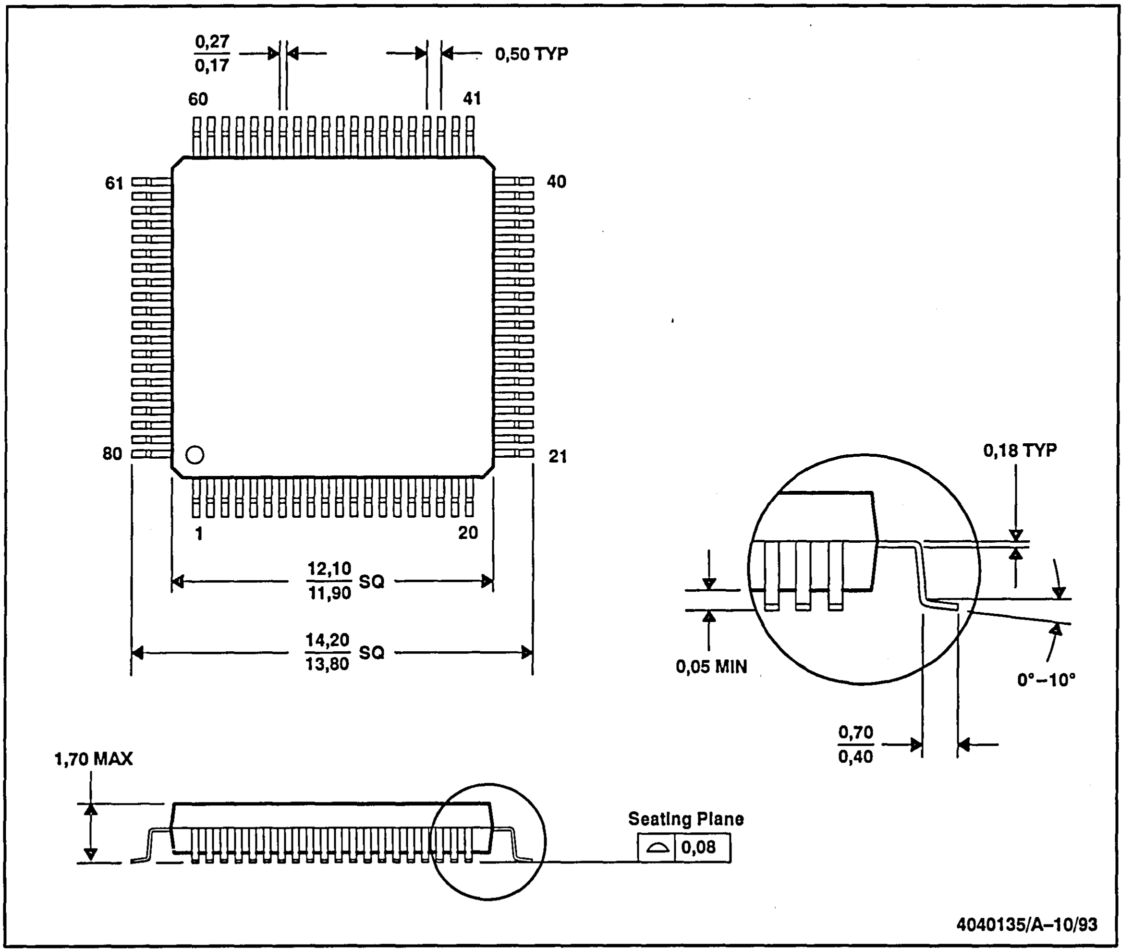
PM/S-PQFP-G64 PLASTIC QUAD FLATPACK



4040152/A–10/93

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.

PN/S-PQFP-G80 **PLASTIC QUAD FLATPACK**

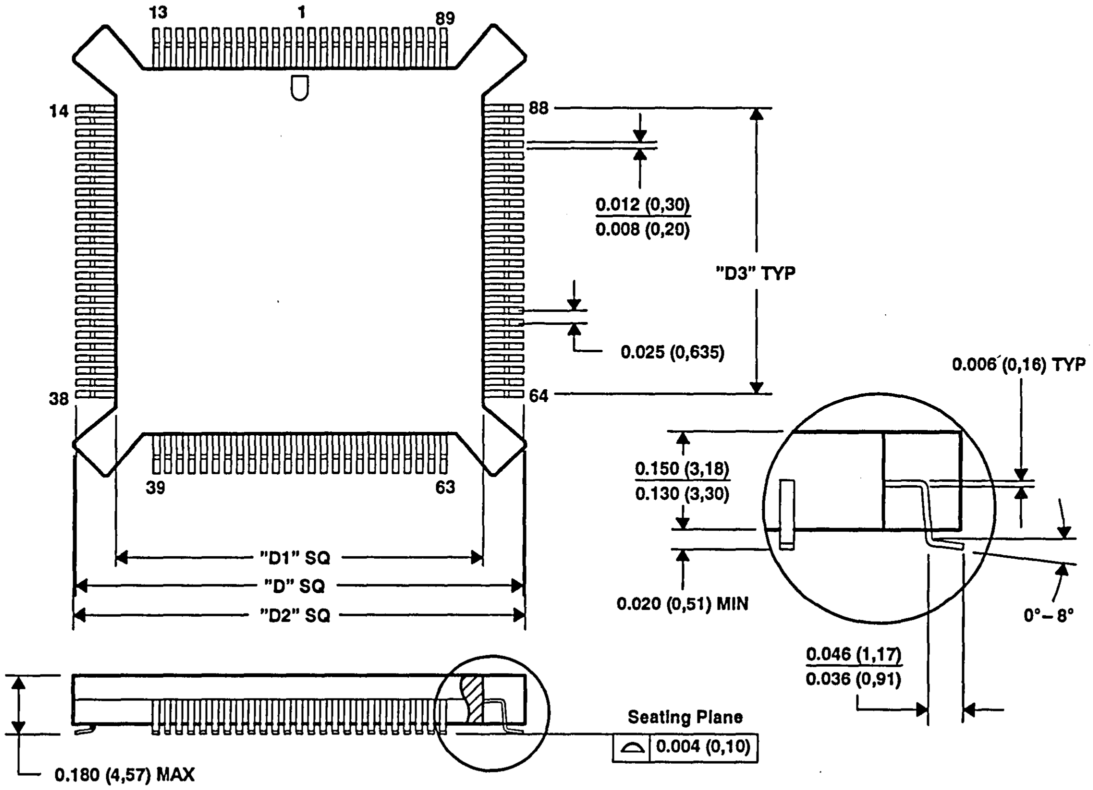


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PQ/S-PQFP-G***

PLASTIC QUAD FLATPACK

100 LEAD SHOWN



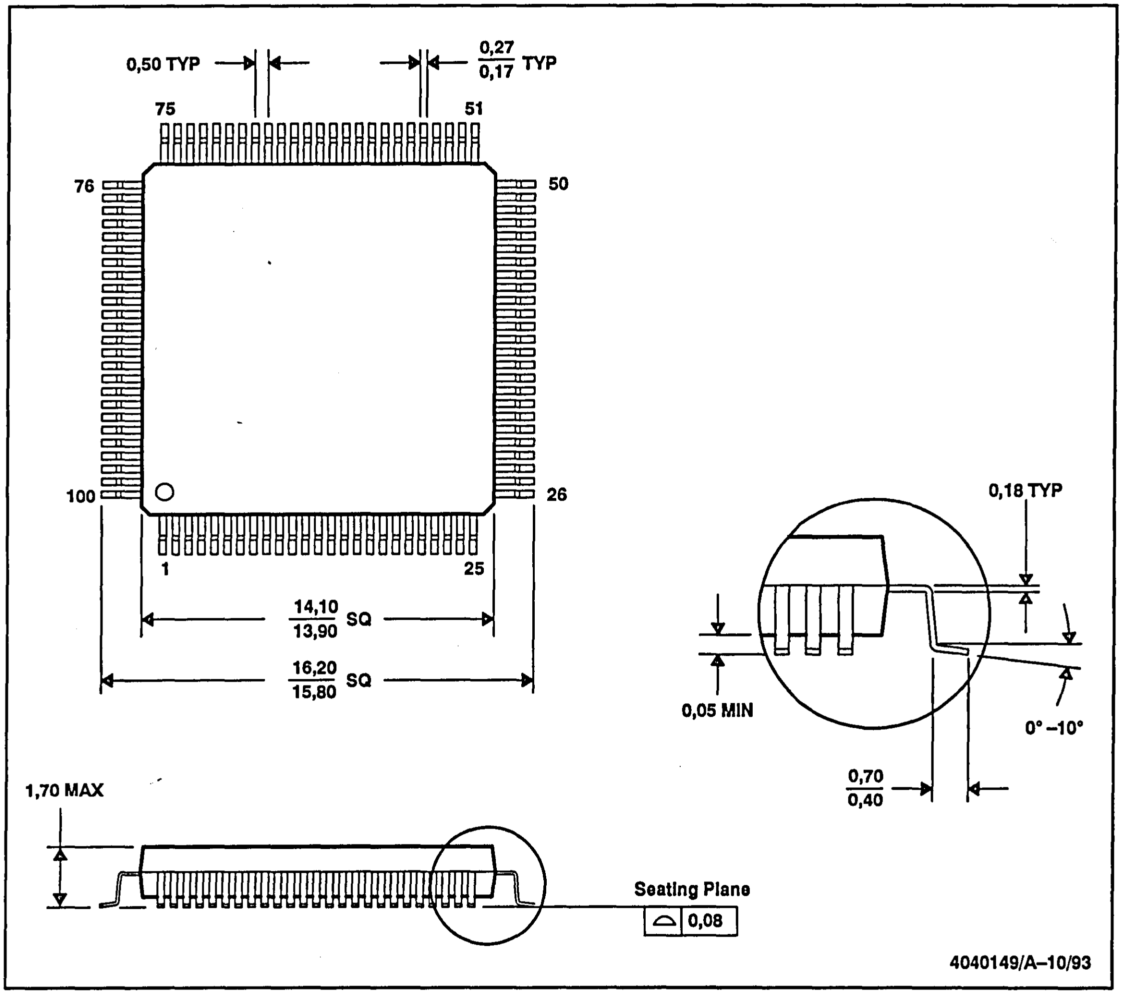
DIM \ LEADS***		100 PQ	132 PQ
JEDEC OUTLINE		MO-069AD	MO-069AE
"D"	MAX	0.890 (22,61)	1.090 (27,69)
	MIN	0.870 (22,10)	1.070 (27,18)
"D1"	MAX	0.766 (19,46)	0.966 (24,54)
	MIN	0.734 (18,64)	0.934 (24,72)
"D2"	MAX	0.912 (22,16)	1.112 (28,25)
	MIN	0.888 (22,56)	1.088 (27,64)
"D3"	TYP	0.600 (15,24)	0.800 (20,32)

4040045/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

PZ/S-PQFP-G100

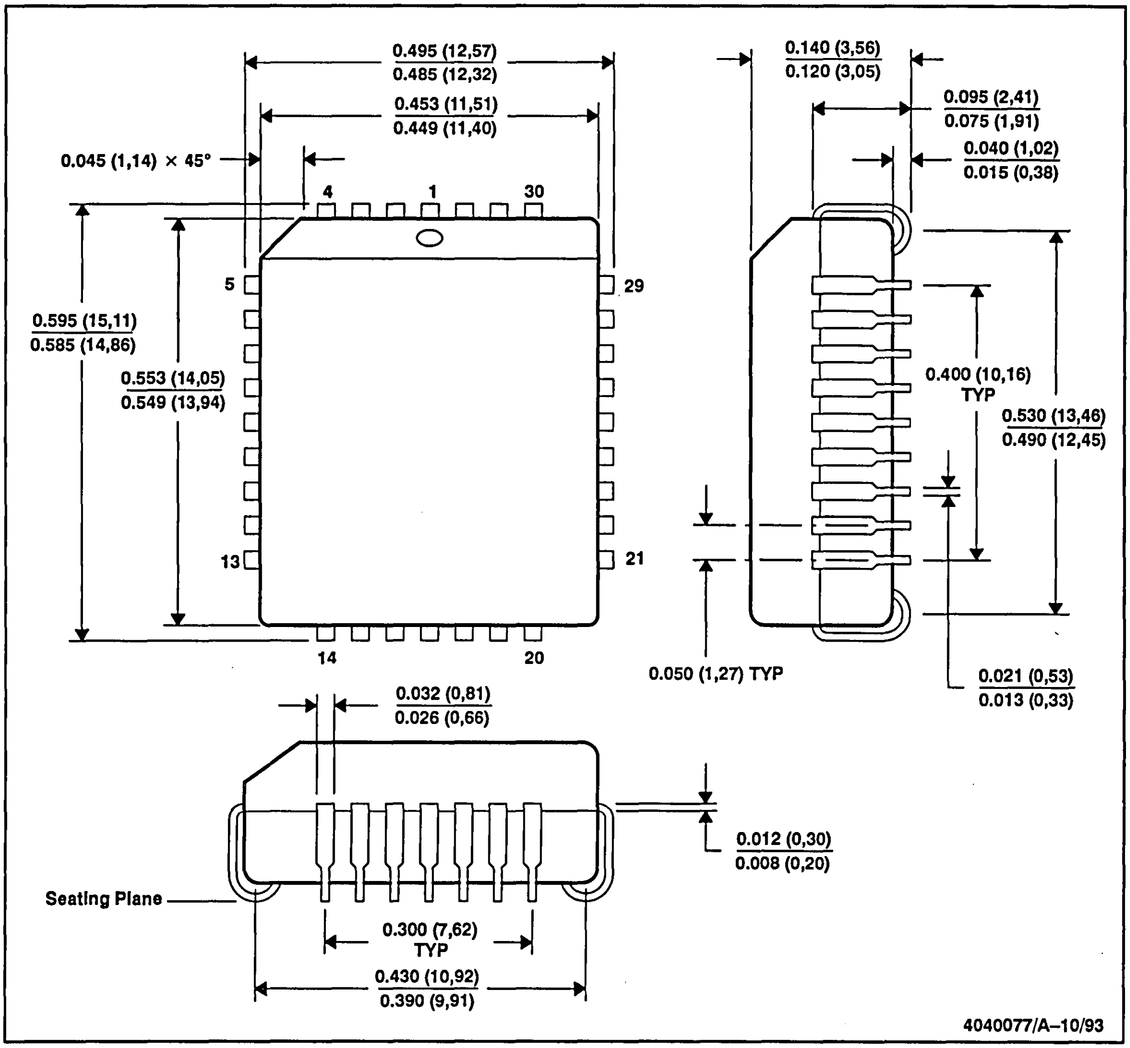
PLASTIC QUAD FLATPACK



4040149/A–10/93

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

RJ/R-PQCC-J32 **PLASTIC J-LEADED CHIP CARRIER**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Formed leads shall be planar with respect to one another within 0.004 (0,10) at the seating plane.

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