TEXAS INSTRUMENTS

# F Logic (SN54/74F)

Data Book

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1994

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# F Logic Data Book
# (SN54/74F)

TEXAS INSTRUMENTS

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## INTRODUCTION

In this volume, Texas Instruments presents technical information on the SN54/74F TTL logic family. The combination of the SN54/74F family with other Texas Instruments advanced families of TTL integrated circuits, Advanced Low-Power Schottky† (ALS) and Advances Schottky (AS), offers the industry the broadest spectrum of advanced bipolar logic products available from any supplier. In addition, the SN54/74F TTL logic family provides the system designer with a pin-for-pin compatible alternate source for SN54/74F devices in standard 300-mil plastic dual-in-line packages (DIPs) along with plastic small-outline (SO) packages, ceramic chip carriers, and ceramic DIPs. Texas Instruments offers all of the above packages with the service levels, quality, and reliability that users have come to expect in a logic family.

The SN54/74F TTL data sheets have been configured for ease of use. They stand alone and require a minimum of reference to other sections for supporting information. Each data sheet has complete absolute maximum ratings, recommended operating conditions, timing requirements (if applicable), and electrical characteristics. The input/output loading and fanout characteristics of each circuit are specified in terms of actual load-current value in amperes. Pinouts are specified using Texas Instruments TTL name conventions.

The following definitions are for the system design engineer who prefers to use unit loads. One unit load in the high state is defined to be 20 μA. One unit load in the low state is defined to be 0.6 mA.

Logic symbols prepared in accordance with IEEE and IEC standards, logic diagrams, and pinout assignments are provided for all SN54/74F TTL devices. The logic diagrams are provided for the understanding of the logic operation of the device and should not be used to estimate propagation delays. Package dimensions given in the mechanical data section of this book are, with one exception, in inches with metric measurements in parentheses. This is to simplify board layout for designers involved in metric conversion and new designs.

In addition to providing pin-compatible alternate sources to common SN54/74F devices, Texas Instruments has also expanded the family to include new functions and packages. With these new solutions, the system designer has attractive options for new designs and/or upgrades to existing designs.

The SN54/74F240, '244, '245, '373, '374, and '543 functions are now available in standard packages and fine-pitch, EIAJ standard shrink small-outline packages (SSOP) with 0.65-mm pitch for board-area-conscious designs.

The Texas Instruments SN54/74F TTL logic family offers several new logic devices. Included among the new functions are:

| | |
|---|---|
| 'F520 | 8-bit identity comparator with input pullup resistors and open-collector outputs |
| 'F621 | Open-collector octal bus transceiver |
| 'F1056 | 8-bit enhanced single diode bus-termination array |

All devices offered can be characterized into distinct logic functions that address several different applications areas. The following functional group table summarizes these groups and lists specific application areas that the functions address.

Complete technical data for any TI Advanced System Logic product is available from the nearest TI field sales office, local authorized TI distributor, or directly by calling the Advanced System Logic hotline at (214) 997-5202.

## FUNCTIONAL GROUPS

| FUNCTION | APPLICATIONS |
|---|---|
| Binary/Decade Counters | Synchronous dividers and multipliers |
| | Timing circuits and state-machine sequencers |
| | Pulse and sync generation |
| | Code-conversion circuits |
| | Analog-to-digital and digital-to-analog conversion circuits |
| | Modulo-n event counters and rate multipliers |
| Decoders | Memory, board, processor, and component-enable generation |
| | Minterm generation and data-flow control |
| | Clock-phase splitter and decoder trees |
| | Demultiplexing for clock distribution and scanning switch encoders |
| | Program counters and digital display systems |
| Dual Flip-Flops | Extra register bits (e.g., guard bits and carry bits) |
| | Synchronizing asynchronous inputs, interrupts, and control signals |
| | Finite or algorithmic state machine state bits |
| | Customized modulo-n event counters |
| Gates | Combinational logic |
| Identity Comparators | Peripheral and board enables, address decodes, and cache-tag comparisons |
| | Page-memory boundary detection, page-fault detection, and error detection and correction |
| Multiplexers/Demultiplexers | Implementing combinational logic (function) tables |
| | Data-flow-control and parallel-to-serial converters |
| | Multiplexing trees, asynchronous shifting, and sorting |
| Octal Buffers/Transceivers | Error-detection and correction circuits |
| | Hamming code generation |
| Octal Flip-Flops | Bus-interface, pipeline registers, and customized shift registers |
| | Ring counters, Johnson counters, pattern generators, and custom modulo-n event counters |
| | Synchronizing asynchronous inputs, interrupts, and control signals |
| Shifters/Shift Registers | Serial-to-parallel conversion or parallel-to-serial conversion |
| | Clock-phase generation, custom counters, and random-number generators |
| | Pipeline registers, accumulators, and digital filters |
| | On-board diagnostics and multiply and divide by $2^n$ |
| | CPU design and array processors |

## PRODUCT STAGE STATEMENTS

*Product stage statements* are used on Texas Instruments data sheets to indicate the development stage(s) of the product(s) specified in the data sheets.

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If not all products specified in a data sheet are at the PRODUCTION DATA stage, then the first statement below is placed in the lower left corner of the first page of the data sheet. Subsequent pages of the data sheet containing PRODUCT PREVIEW information or ADVANCE INFORMATION are then marked in the lower left-hand corner with the appropriate statement given below:

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## INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

## operating conditions and characteristics (in sequence by letter symbols)

**$C_i$** **Input capacitance**

The internal capacitance at an input of the device

**$C_o$** **Output capacitance**

The internal capacitance at an output of the device

**$C_{pd}$** **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

**$f_{max}$** **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

**$I_{CC}$** **Supply current**

The current into* the $V_{CC}$ supply terminal of an integrated circuit

**$\Delta I_{CC}$** **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$

**$I_{CEX}$** **Output high leakage current**

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O$ = 5.5 V.

**$I_{I(hold)}$** **Input hold current**

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

**$I_{IH}$** **High-level input current**

The current into* an input when a high-level voltage is applied to that input

**$I_{IL}$** **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

**$I_{off}$** **Input/output power-off leakage current**

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{CC}$ = 0 V

**$I_{OH}$** **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

**$I_{OL}$** **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

# GLOSSARY
# SYMBOLS, TERMS, AND DEFINITIONS

**$I_{OZ}$** **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output

**$t_a$** **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

**$t_c$** **Clock cycle time**

Clock cycle time is $1/f_{max}$.

**$t_{dis}$** **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or $t_{PLZ}$. Open-collector outputs will change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

**$t_{en}$** **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or $t_{PZL}$. Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

**$t_h$** **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

**$t_{pd}$** **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or $t_{PLH}$)

**$t_{PHL}$** **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

**$t_{PHZ}$** **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

**$t_{PLH}$** **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

*Current out of a terminal is given as a negative value.

**$t_{PLZ}$** **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

**$t_{PZH}$** **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

**$t_{PZL}$** **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

**$t_{su}$** **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

**$t_w$** **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

**$V_{IH}$** **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

**$V_{IL}$** **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

**$V_{OH}$** **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output

**$V_{OL}$** **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output

**$V_{IT+}$** **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, $V_{IT-}$

**$V_{IT-}$** **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{IT+}$

# EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

| | | |
|---|---|---|
| H | = | high level (steady state) |
| L | = | low level (steady state) |
| ↑ | = | transition from low to high level |
| ↓ | = | transition from high to low level |
| → | = | value/level or resulting value/level is routed to indicated destination |
| ↶ | = | value/level is re-entered |
| X | = | irrelevant (any input, including transitions) |
| Z | = | off (high-impedance) state of a 3-state output |
| a . . . h | = | the level of steady-state inputs A through H respectively |
| $Q_0$ | = | level of Q before the indicated steady-state input conditions were established |
| $\overline{Q}_0$ | = | complement of $Q_0$ or level of $\overline{Q}$ before the indicated steady-state input conditions were established |
| $Q_n$ | = | level of Q before the most recent active transition indicated by ↓ or ↑ |
| ⎍ | = | one high-level pulse |
| ⎴ | = | one low-level pulse |
| Toggle | = | each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑ |

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, $Q_0$, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

**FUNCTION TABLE**

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLEAR | MODE | | CLOCK | SERIAL | | PARALLEL | | | | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| | S1 | S0 | | LEFT | RIGHT | A | B | C | D | | | | |
| L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| H | X | X | L | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c | d | a | b | c | d |
| H | L | H | ↑ | X | H | H | H | H | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | L | L | L | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output $Q_A$, data entered at B will be at $Q_B$, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at $Q_A$ is now at $Q_B$, the previous levels of $Q_B$ and $Q_C$ are now at $Q_C$ and $Q_D$, respectively, and the data previously at $Q_D$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at $Q_B$ is now at $Q_A$, the previous levels of $Q_C$ and $Q_D$ are now at $Q_B$ and $Q_C$, respectively, and the data previously at $Q_A$ is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

## FUNCTIONAL TESTING

Functional testing is performed on all logic devices by the execution of a set of functional patterns located in the test program. These patterns are used to guarantee conformance to the truth table and simulate operation in an actual system.

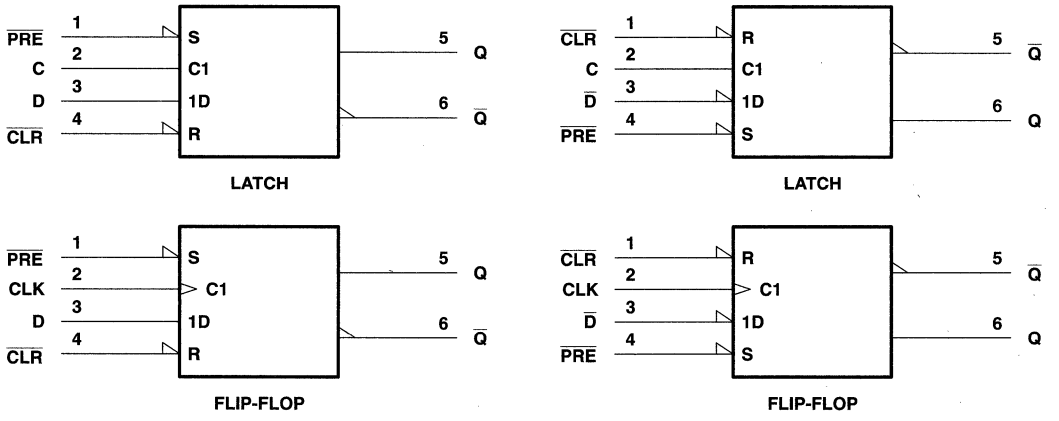
Problems are frequently discovered in functional testing when $V_{IH(min)}$ and $V_{IL(max)}$ are used as the input conditions to exercise the function table. $V_{IH(min)}$ and $V_{IL(max)}$ are input conditions that are used in parametric testing. These problems occur because of the noise that is present on the test heads of automated test equipment with long cables. Parametric tests such as $V_{OH}$, $V_{OL}$, $I_{OZH}$, or $I_{OZL}$ are done at a relatively slow repetition rate, and any noise that is present on the test head will have settled out before the outputs are measured. However, during functional testing the outputs are sensed much sooner, before the noise on the inputs has settled out and the output has reached its final and correct state.

The functional patterns that are applied to the device under test are 0-V to 3-V transitions as defined in the parameter measurement information section. The use of $V_{IH}$ = 3 V and $V_{IL}$ = 0 V during functional testing does not imply that the devices are noise sensitive since the environment that the device sees on a system's printed circuit board is much less severe than a noisy production test environment. Therefore, $V_{IH(min)}$ and $V_{IL(max)}$ should not be used to test functionality of SN54/74F devices.

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.




The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators ( ◺ ) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the SN54/74F family. In general, the junction temperature for any device can be calculated using equation 1.

$$T_J = R_{\theta JA}[(V_{CC} \times I_{CC}) + (N \times I_{OL} \times V_{OL})] + T_A \quad (1)$$

where:

$T_J$ = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
$V_{CC}$ = supply voltage (5 V for typical, 5.5 V for maximum)
$I_{CC}$ = supply current (specified on device data sheet)
$N$ = number of outputs
$I_{OL}$ = low-level output current
$V_{OL}$ = low-level output voltage
$T_A$ = free-air temperature

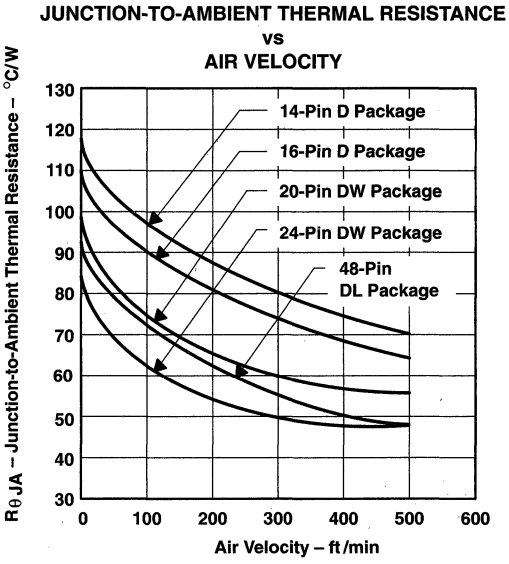



**Figure 1**

Typical junction temperature can be calculated using equation 1 directly with typical values of $I_{CC}$ taken from the data sheets and $V_{CC}$ = 5 V. To calculate maximum junction temperature, it is necessary to take into account the spread of $I_{CC}$ values for a population. Due to the specification practices that have been followed, it is useful to use slightly different calculations for SN54F and SN74F devices.

Maximum junction temperature for SN54F parts can be calculated using equation 1 with $I_{CC}$ being the maximum value specified on the data sheet and $V_{CC}$ = 5.5 V. In fact, $I_{CC}$ for series 54 devices at the temperature extremes of –55°C to 125°C will be higher than for series 74 devices at the temperature extremes of 0°C to 70°C.

The SN54/74F family data sheets give a single maximum value for $I_{CC}$. If that value is used to calculate maximum junction temperature for SN74F devices, an unrealistically high value will result. Instead, equation 2 can be used. This uses the factor 1.31 to scale the typical value of $I_{CC}$ up to a practical maximum value for process variations and thermal effects.

Thus, for SN74F devices:

$$T_{J(max)} = R_{\theta JA}[(5.5 \times 1.31 \times I_{CC(typ)}) + N \times I_{OL} \times V_{OL})] + T_A \quad (2)$$

## DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

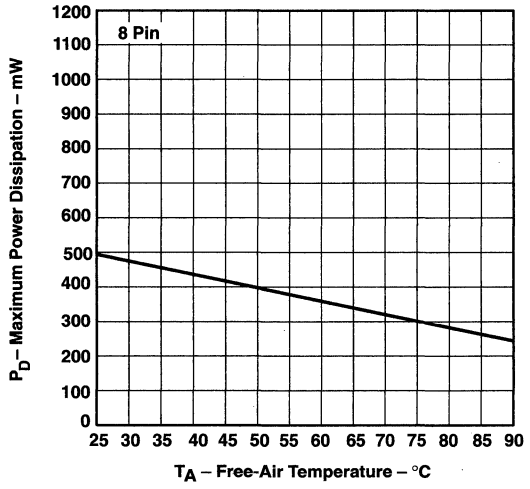



Figure 2

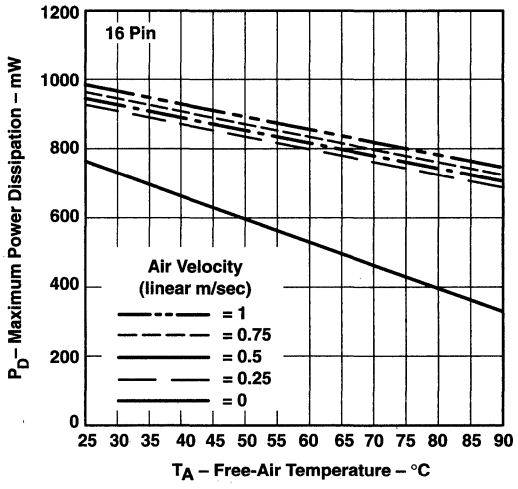



Figure 3

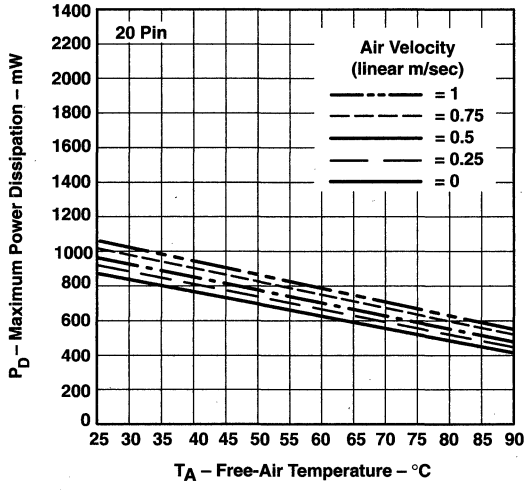



Figure 4

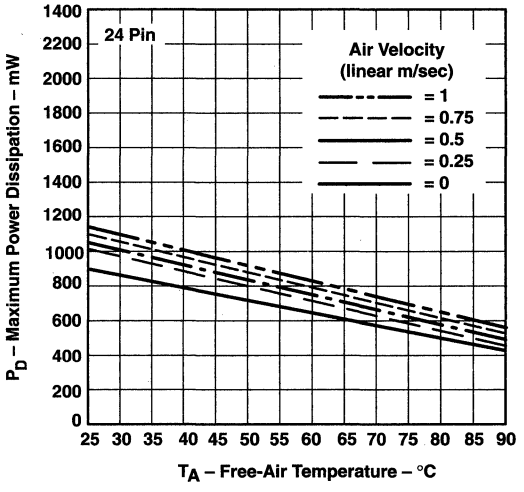



Figure 5

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type and list all available or planned options of that function. The technology columns identify the appropriate family and a particular data book where more information can be found. The applicable literature number, composed of either seven or eight alphanumeric characters, can be found at the lower right-hand corner on the back cover of each publication.

List of additional Advanced System Logic data books:

| | | |
|---|---|---|
| ABT Devices | Advanced BiCMOS Technology | SCBD002A |
| AC and ACT Devices | Advanced CMOS Logic Data Book | SCAD001C |
| Advanced Logic Devices | Advanced Logic and Bus-Interface Data Book | SCYD001 |
| ALS and AS Devices† | ALS/AS Logic Data Book | SDAD001B |
| BCT Devices† | BiCMOS Bus-Interface Logic Data Book | SCBD001A |
| FIFO Devices | High-Performance FIFO Memories Data Book | SCAD003A |
| HC and HCT Devices | High-Speed CMOS Logic Data Book | SCLD001C |
| LV, LVC, LVT, and ALVC Devices† | Low-Voltage Logic Data Book | SCBD003 |
| SCOPE™ Devices | SCOPE™ Product Information | SSYV001 |
| Std TTL, LS, and S Devices | TTL Logic Data Book | SDLD001A |

† Updated data book planned for this technology

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## GATES

### Positive-NAND Gates

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| 8-Input | | '30 | ✔ | ✔ | ✔ | | | | | | | | |
| | | '11030 | | | | | | ✔ | ✔ | | | | |
| 13-Input | | '133 | ✔ | | | ✔ | | | | | | | |
| Dual 2-Input | | '8003 | ✔ | | | | | | | | | | |
| Dual 4-Input | | '20 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '40 | ✔ | | | | | | | | | | |
| | | '11020 | | | | | | ✔ | ✔ | | | | |
| Triple 3-Input | | '10 | ✔ | ✔ | ✔ | ✔ | | | | | | | + |
| | | '1010 | ✔ | | | | | | | | | | |
| | | '11010 | | | | | | ✔ | ✔ | | | | |
| Quad 2-Input | | '00 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | ✔ | + |
| | | '11000 | | | | | | ✔ | ✔ | | | | |
| | | '37 | ✔ | | | | | | | | | | |
| | OC | '38 | ✔ | | ✔ | | | | | | | | |
| | | '132 | | | | ✔ | | | | | | | |
| | | '11132 | | | | | | ✔ | ✔ | | | | |
| | | '1000 | | ✔ | | | | | | | | | |
| Hex 2-Input | | '804 | ✔ | ✔ | | | | | | | | | |
| Quad 2-Input | OC | '01 | ✔ | | | ✔ | | | | | | | |
| | | '03 | ✔ | | | ✔ | | | | | | | |

### Positive-AND Gates

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| Quad 2-Input | OC | '09 | ✔ | | | ✔ | | | | | | | |
| | | '7001 | | | | ✔ | | | | | | | |
| Dual 4-Input | | '21 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11021 | | | | | | ✔ | ✔ | | | | |
| Triple 3-Input | | '11 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11011 | | | | | | ✔ | ✔ | | | | |
| Quad 2-Input | | '08 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | ✔ | + |
| | | '1008 | | ✔ | | | | | | | | | |
| | | '11008 | | | | | | ✔ | ✔ | | | | |
| Hex 2-Input | | '808 | | ✔ | | | | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## Positive-OR/NOR Gates

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| Triple 3-Input | | '4075 | | | | ✔ | | | | | | | |
| Quad 2-Input | | '32 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | ✔ | + |
| | | '1032 | | ✔ | | | | | | | | | |
| | | '11032 | | | | | | ✔ | ✔ | | | | |
| | | '7032 | | | | ✔ | | | | | | | |
| Hex 2-Input | | '832 | ✔ | ✔ | | ✔ | | | | | | | |
| Dual 5-Input | | '260 | | | ✔ | | | | | | | | |
| Triple 3-Input | | '27 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11027 | | | | | | ✔ | ✔ | | | | |
| Quad 2-Input | | '02 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | ✔ | + |
| | OC | '33 | ✔ | | | | | | | | | | |
| | | '7002 | | | | ✔ | | | | | | | |
| | | '11002 | | | | | | ✔ | ✔ | | | | |
| Hex 2-Input | | '805 | ✔ | ✔ | | ✔ | | | | | | | |

## OR/NOR Gates

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs | | '86 | ✔ | ✔ | ✔ | ✔ | | | | | | | + |
| | | '11086 | | | | | | ✔ | ✔ | | | | |
| Quad 2-Input Exclusive-OR Gates | OC | '136 | ✔ | | | | | | | | | | |
| Quad 2-Input Exclusive-NOR Gates | OD | '266 | | | | ✔ | | | | | | | |
| | | '810 | ✔ | | | | | | | | | | |
| | OC | '811 | ✔ | | | | | | | | | | |

## AND-OR Gates

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| Dual 2-Wide 2-Input, 3-Input | | '51 | | | ✔ | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## INVERTING/NONINVERTING BUFFERS

### Hex Inverters/Noninverters

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| Hex Inverters | | '04 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | ✔ | + |
| | | 'U04 | | | | ✔ | | | | | | ✔ | + |
| | | '11004 | | | | | | ✔ | ✔ | | | | |
| | OC | '05 | ✔ | | | ✔ | | | | | | | |
| | | '14 | | | | ✔ | | | | | | ✔ | + |
| | | '11014 | | | | | | ✔ | ✔ | | | | |
| | | '1004 | ✔ | ✔ | | | | | | | | | |
| | | '1005 | ✔ | | | | | | | | | | |
| Hex Noninverters | | '11034 | | | | | | ✔ | ✔ | | | | |
| | OC | '35 | ✔ | | | | | | | | | | |
| | | '1034 | ✔ | ✔ | | | | | | | | | |
| | OC | '1035 | ✔ | | | | | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## BUFFERS/DRIVERS AND BUS TRANSCEIVERS

### Buffers/Drivers

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Quad Buffers/Drivers | 3S | '125 | | | ✔ | ✔ | ✔ | | | ✔ | ✔ | ✔ | | + | |
| | | '126 | | | ✔ | ✔ | | | | ✔ | ✔ | | | | |
| Noninverting Hex Buffers/Drivers | 3S | '365 | | | | ✔ | | | | | | | | | |
| | | '367 | | | | ✔ | | | | | | | | | |
| Inverting Hex Buffers/Drivers | 3S | '368 | | | | ✔ | | | | | | | | | |
| Noninverting Octal Buffers/Drivers | 3S | '241 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | | | | |
| | | '11241 | | | | | | ✔ | ✔ | | | | | | |
| | | '25241 | | | | | | | | | + | | | | |
| | | '244 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | | ✔ | + | |
| | | '244A | | | | | | | | | | ✔ | | | |
| | | '11244 | | | | | | ✔ | ✔ | | | | | | |
| | | '1244 | ✔ | | | | | | | | | | | | |
| | | '25244 | | | | | | | | ✔ | + | | | | |
| | | '541 | ✔ | | ✔ | ✔ | ✔ | | | ✔ | ✔ | | | + | |
| | OC | '757 | | ✔ | | | | | | ✔ | | | | | |
| | | '760 | ✔ | ✔ | | | | | | ✔ | | | | | |
| | | '25760 | | | | | | | | + | | | | | |
| Inverting Octal Buffers/Drivers | 3S | '240 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | ✔ | ✔ | + | |
| | | '11240 | | | | | | ✔ | ✔ | | | | | | |
| | | '1240 | ✔ | | | | | | | | | | | | |
| | | '25240 | | | | | | | | ✔ | | | | | |
| | | '466 | ✔ | | | | | | | | | | | | |
| | | '540 | ✔ | | | ✔ | ✔ | | | ✔ | ✔ | | | + | |
| | OC | '756 | ✔ | ✔ | | | | | | ✔ | | | | | |
| | | '763 | ✔ | ✔ | | | | | | | | | | | |
| Inverting and Noninverting Octal Buffers/Drivers | 3S | '230 | | ✔ | | | | | | | | | | | |
| | OC | '762 | | ✔ | | | | | | | | | | | |
| Triple 4-Input OR/NOR Drivers | | '11802 | | | | | | | ✔ | | | | | | |
| Noninverting 10-Bit Buffers/Drivers | 3S | '827 | | | | | | | | | ✔ | | | | |
| | | '11827 | | | | | | ✔ | ✔ | | | | | | |
| | | '29827 | ✔ | | | | | | | ✔ | | | | | |
| Inverting 10-Bit Buffers/Drivers | 3S | '828 | | | | | | | | | + | | | | |
| | | '11828 | | | | | | ✔ | ✔ | | | | | | |
| | | '29828 | ✔ | | | | | | | ✔ | | | | | |
| Noninverting 16-Bit Buffers/Drivers | 3S | '16241 | | | | | | | ✔ | | ✔ | | | | |
| | | '16244 | | | | | | ✔ | ✔ | | ✔ | | | + | + |
| | | '16244A | | | | | | | | | | ✔ | | | |
| | | '16541 | | | | | | | ✔ | | ✔ | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## BUFFERS/DRIVERS AND BUS TRANSCEIVERS

### Buffers/Drivers (continued)

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Inverting 16-Bit Buffers/Drivers | 3S | '16240 | | | | | | ✔ | ✔ | | ✔ | | | + | + |
| | | '16540 | | | | | | | ✔ | | ✔ | | | | |
| Noninverting 18-Bit Buffers/Drivers | 3S | '16825 | | | | | | | ✔ | | ✔ | | | | |
| Inverting 18-Bit Buffers/Drivers | 3S | '16826 | | | | | | | | | + | | | | |
| Noninverting 20-Bit Buffers/Drivers | 3S | '16827 | | | | | | | ✔ | | ✔ | | | | + |
| Inverting 20-Bit Buffers/Drivers | 3S | '16828 | | | | | | | | | + | | | | + |
| Octal Buffers/Drivers With Input Pullup Resistors | | '746 | ✔ | | | | | | | | | | | | |

### Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Noninverting 18-Bit Universal Bus Transceivers (UBT™) | 3S | '16500 | | | | | + | | | + |
| | | '16500B | | | | ✔ | | | | |
| Noninverting 18-Bit Universal Bus Transceivers (UBT™) | 3S | '16501 | | | | ✔ | + | | + | + |
| | | '16600 | | | | ✔ | | | | + |
| | | '16601 | | | | ✔ | | | | + |
| Noninverting 36-Bit Universal Bus Transceivers (UBT™) | 3S | '32501 | | | | ✔ | | | | |
| Noninverting 16-Bit Tri-Port Universal Bus Exchangers (UBE™) | 3S | '32316 | | | | ✔ | | | | |
| Noninverting 18-Bit Tri-Port Universal Bus Exchangers (UBE™) | 3S | '32318 | | | | ✔ | | | | |
| 18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port | 3S | '162500 | | | | + | | | | |
| | | '162501 | | | | + | | | | |
| | | '162600 | | | | + | | | | |
| | | '162601 | | | | ✔ | | | | |
| SCOPE™ 18-Bit Universal Bus Transceivers (UBT™) | 3S | '18502 | | | | ✔ | + | | | |
| SCOPE™ 20-Bit Universal Bus Transceivers (UBT™) | 3S | '18504 | | | | ✔ | + | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## BUFFERS/DRIVERS AND BUS TRANSCEIVERS

### Bus Transceivers

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Noninverting Quad Transceivers | 3S | '243 | ✔ | | ✔ | | | | | | | | | | |
| Inverting Quad Transceivers | OC | '758 | ✔ | | | | | | | | | | | | |
| | 3S | '242 | | | ✔ | | | | | | | | | | |
| Noninverting Octal Transceivers | 3S | '245 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | ✔ | ✔ | + | |
| | | '1245 | ✔ | | | | | | | | | | | | |
| | | '11245 | | | | | | ✔ | ✔ | | | | | | |
| | | '25245 | | | | | | | | ✔ | ✔ | | | | |
| | | '645 | ✔ | ✔ | | ✔ | ✔ | | | | | | | | |
| | | '1645 | ✔ | | | | | | | | | | | | |
| | OC | '621 | ✔ | | ✔ | | | | | | | | | | |
| | | '641 | ✔ | ✔ | | | | | | | | | | | |
| | OC/3S | '639 | ✔ | ✔ | | | | | | | | | | | |
| Inverting Octal Transceivers | 3S | '620 | ✔ | | | | | | | ✔ | ✔ | | | | |
| | | '623 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | | | | |
| | | '11623 | | | | | | | ✔ | | | | | | |
| | | '640 | ✔ | ✔ | | ✔ | | | | ✔ | ✔ | | | | |
| | | '1640 | ✔ | | | | | | | | | | | | |
| | | '11640 | | | | | | | ✔ | | | | | | |
| | OC | '642 | ✔ | | | | | | | | | | | | |
| | | '25642 | | | | | | | | ✔ | | | | | |
| | OC/3S | '638 | ✔ | ✔ | | | | | | | | | | | |
| Noninverting 9-Bit Transceivers | 3S | '863 | | | | | | | | | ✔ | | | + | |
| | | '29863 | ✔ | | | | | | | ✔ | | | | | |
| Inverting 9-Bit Transceivers | 3S | '29864 | | | | | | | | ✔ | | | | | |
| Noninverting 10-Bit Transceivers | 3S | '861 | | | | | | | | | + | | | | |
| | | '29861 | | | | | | | | ✔ | | | | | |
| Inverting 10-Bit Transceivers | 3S | '29862 | | | | | | | | ✔ | | | | | |
| Noninverting 16-Bit Transceivers | 3S | '16245 | | | | | | ✔ | ✔ | | ✔ | ✔ | | + | + |
| | | '16623 | | | | | | ✔ | ✔ | | ✔ | | | | |
| Inverting 16-Bit Transceivers | 3S | '16640 | | | | | | ✔ | ✔ | | ✔ | | | | |
| | | '16620 | | | | | | ✔ | ✔ | | + | | | | |
| Noninverting 18-Bit Transceivers | 3S | '16863 | | | | | | | ✔ | | ✔ | | | | |
| Inverting 18-Bit Transceivers | 3S | '16864 | | | | | | | | | + | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## BUFFERS/DRIVERS AND BUS TRANSCEIVERS

### Bus Transceivers (continued)

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Noninverting 20-Bit Transceivers | 3S | '16861 | | | | | | | ✔ | | + | | | | |
| Inverting 20-Bit Transceivers | 3S | '16862 | | | | | | | | | + | | | | |
| Noninverting Octal Registered Transceivers | 3S | '11470 | | | | | | | ✔ | | | | | | |
| | | '543 | | | ✔ | | | | | ✔ | ✔ | ✔ | | + | |
| | | '11543 | | | | | | | ✔ | | | | | | |
| | | '646 | ✔ | ✔ | | ✔ | ✔ | | | ✔ | ✔ | ✔ | | + | |
| | | '646A | | | | | | | | | ✔ | | | | |
| | | '11646 | | | | | | ✔ | ✔ | | | | | | |
| | | '652 | ✔ | ✔ | | ✔ | ✔ | | | ✔ | ✔ | ✔ | | + | |
| | | '11652 | | | | | | ✔ | ✔ | | | | | | |
| | | '2952 | | | | | | | | ✔ | + | ✔ | | + | |
| | | '2952A | | | | | | | | | ✔ | | | | |
| | OC/3S | '653 | ✔ | | | | | | | | | | | | |
| | | '654 | ✔ | | | | | | | | | | | | |
| Inverting Octal Registered Transceivers | 3S | '544 | | | | | | | | ✔ | + | | | | |
| | | '11544 | | | | | | | ✔ | | | | | | |
| | | '648 | ✔ | ✔ | | | | | | ✔ | + | | | | |
| | | '11648 | | | | | | | ✔ | | | | | | |
| | | '651 | ✔ | ✔ | | | | | | ✔ | ✔ | | | | |
| | | '2953 | | | | | | | | ✔ | + | | | | |
| Noninverting 16-Bit Registered Transceivers | 3S | '16470 | | | | | | | ✔ | | ✔ | | | | |
| | | '16543 | | | | | | ✔ | ✔ | | ✔ | + | | + | + |
| | | '16646 | | | | | | ✔ | ✔ | | ✔ | + | | + | + |
| | | '16652 | | | | | | ✔ | ✔ | | ✔ | + | | + | + |
| | | '16952 | | | | | | | ✔ | | ✔ | + | | + | + |
| Inverting 16-Bit Registered Transceivers | 3S | '16471 | | | | | | | | | + | | | | |
| | | '16544 | | | | | | | ✔ | | + | | | | |
| | | '16648 | | | | | | | ✔ | | + | | | | |
| | | '16651 | | | | | | | ✔ | | + | | | | |
| | | '16953 | | | | | | | | | + | | | | |

✔ Product available in technology indicated
\+ New product planned in technology indicated

## BUFFERS/DRIVERS AND BUS TRANSCEIVERS

### Bus Transceivers (continued)

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Noninverting 18-Bit Registered Transceivers | 3S | '16472 | | | | | | ✔ | | | | | | | |
| | | '16474 | | | | | | | ✔ | | | | | | |
| | | '16500 | | | | | | | | | ✔ | + | | + | + |
| | | '16501 | | | | | | | | | ✔ | + | | + | + |
| | | '16600 | | | | | | | | | ✔ | | | | + |
| | | '16601 | | | | | | | | | ✔ | | | | + |
| Inverting 18-Bit Registered Transceivers | 3S | '16475 | | | | | | | ✔ | | | | | | |
| Noninverting 36-Bit Transceivers | 3S | '32245 | | | | | | | | | + | | | | |
| Noninverting 36-Bit Registered Transceivers | 3S | '32501 | | | | | | | | | ✔ | | | | |
| | | '32543 | | | | | | | | | ✔ | | | | |
| 8-/9-Bit Bus Transceivers With Parity Checkers/ Generators | 3S | '657 | | | ✔ | | | | | ✔ | + | | | | |
| | | '659 | | | | | ✔ | | | | | | | | |
| | | '833 | | | | | | | | | + | | | | |
| | | '834 | | | | | | | | | + | | | | |
| | | '853 | | | | | | | | | + | | | | |
| | | '854 | | | | | | | | | + | | | | |
| | | '899 | | | | | | | | ✔ | | | | | |
| | 3S/OC | '29833 | ✔ | | | | | | | ✔ | | | | | |
| | | '29834 | | | | | | | | ✔ | | | | | |
| | | '29853 | ✔ | | | | | | | ✔ | | | | | |
| | | '29854 | ✔ | | | | | | | ✔ | | | | | |
| Dual 8-/9-Bit Bus Transceivers With Parity Checkers/ Generators | 3S | '16833 | | | | | | | ✔ | | ✔ | | | | |
| | | '16657 | | | | | | | ✔ | | ✔ | | | | |
| | | '16853 | | | | | | | | | ✔ | | | | |
| Universal Transceivers/Port Controllers | 3S | '856 | | ✔ | | | | | | | | | | | |
| Noninverting 16-Bit Tri-Port Registered Bus Exchangers | 3S | '32316 | | | | | | | | | ✔ | | | | |
| Noninverting 18-Bit Tri-Port Registered Bus Exchangers | 3S | '32318 | | | | | | | | | ✔ | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## BUFFERS/DRIVERS AND BUS TRANSCEIVERS

### MOS Memory Drivers/Transceivers

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| Octal Transceivers With Series Resistors on Output | 3S | '2623 | | ✔ | | | | | | | |
| Octal Buffers/Drivers With Series Resistors on Output | 3S | '2240 | ✔ | | | | | | | ✔ | ✔ |
| | | '2241 | | | | | | | | ✔ | ✔ |
| | | '2244 | | | | | | | | ✔ | ✔ |
| | | '2541 | ✔ | | | | | | | | |
| Octal Transceivers With Series Resistors on B Port | 3S | '2245 | | | | | | | | ✔ | + |
| Octal Latches With Series Resistors on Output | 3S | '2574 | | | | | | | | + | |
| 10-Bit Buffers/Drivers With Series Resistors | 3S | '2827 | | | | | | | | ✔ | |
| | | '2828 | | | | | | | | ✔ | |
| 11-Bit Buffers/Drivers With Series Resistors | 3S | '2410 | | | | | | | | ✔ | |
| | | '2411 | | | | | | | | + | |
| | | '5400 | | | | | | | | | ✔ |
| | | '5401 | | | | | | | | | ✔ |
| 12-Bit Buffers/Drivers With Series Resistors | 3S | '5402 | | | | | | | | | ✔ |
| | | '5403 | | | | | | | | | ✔ |
| 16-Bit Buffers/Drivers With Series Resistors | 3S | '162240 | | | | | | | | | + |
| | | '162244 | | | | | | | | | ✔ |
| 16-Bit Transceivers With Series Resistors | 3S | '162245 | | | | | | | | | + |
| 18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port | 3S | '162500 | | | | | | | | | + |
| | | '162501 | | | | | | | | | + |
| | | '162600 | | | | | | | | | + |
| | | '162601 | | | | | | | | | ✔ |
| 12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port | 3S | '162260 | | | | | | | | | ✔ |

✔ Product available in technology indicated
+ New product planned in technology indicated

## TESTABILITY BUS-INTERFACE CIRCUITS

### JTAG/IEEE 1149.1 Testability Circuits

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | F | HC | HCT | AC | ACT | BCT | ABT | LVT |
| Buffers/Drivers | 8 | 3S | '8240A | | | | | | ✔ | | |
| | | | '8244A | | | | | | ✔ | | |
| Transceivers | 8 | 3S | '8245 | | | | | | | ✔ | |
| | | | '8245A | | | | | | ✔ | | |
| | 18 | 3S | '18245 | | | | | | | ✔ | + |
| Transparent Latches | 8 | 3S | '8373A | | | | | | ✔ | | |
| Flip-Flops | 8 | 3S | '8374A | | | | | | ✔ | | |
| Registered Transceivers | 8 | 3S | '8543 | | | | | | | ✔ | |
| | | | '8646 | | | | | | | ✔ | |
| | | | '8652 | | | | | | | ✔ | |
| | | | '8952 | | | | | | | ✔ | |
| | 18 | 3S | '18502 | | | | | | | ✔ | + |
| | | | '18646 | | | | | | | ✔ | |
| | | | '18652 | | | | | | | + | |
| | 20 | 3S | '18504 | | | | | | | ✔ | + |
| Test Bus Controllers | | 3S | '8990 | | | | | ✔ | | | |
| Digital Bus Monitors | | 3S | '8994 | | | | | ✔ | | | |
| Scan Path Linkers With Identification Buses | 4 | 3S | '8997 | | | | | ✔ | | | |
| | 8 | 3S | '8999 | | | | | ✔ | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated



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## FLIP-FLOPS AND LATCHES

### Flip-Flops

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Dual J-K Edge Triggered | | '73 | | | | ✔ | | | | | | | | | |
| | | '76 | | | | ✔ | | | | | | | | | |
| | | '109 | ✔ | ✔ | ✔ | ✔ | | | | | | | | | |
| | | '11109 | | | | | | ✔ | ✔ | | | | | | |
| | | '112 | ✔ | | ✔ | ✔ | | | | | | | | + | |
| | | '11112 | | | | | | ✔ | ✔ | | | | | | |
| | | '113 | ✔ | | | ✔ | | | | | | | | | |
| | | '114 | ✔ | | | | | | | | | | | | |
| Dual D-Type | | '74 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | ✔ | + | |
| | | '11074 | | | | | | ✔ | ✔ | | | | | | |
| Dual D-Type With 2-Input NAND/NOR Gates | | '7074 | | | | ✔ | | | | | | | | | |
| | | '7075 | | | | ✔ | | | | | | | | | |
| | | '7076 | | | | ✔ | | | | | | | | | |
| Dual 4-Bit D-Type Edge Triggered | 3S | '874 | ✔ | ✔ | | | | | | | | | | | |
| | | '11874 | | | | | | | ✔ | | | | | | |
| | | '876 | ✔ | ✔ | | | | | | | | | | | |
| | | '879 | ✔ | ✔ | | | | | | | | | | | |
| Quad D-Type | | '173 | | | | ✔ | | | | | | | | | |
| | | '175 | ✔ | ✔ | ✔ | ✔ | | | | | | | | | |
| | | '11175 | | | | | | ✔ | ✔ | | | | | | |
| Hex D-Type | | '174 | ✔ | ✔ | ✔ | ✔ | | | | | | | ✔ | | |
| | | '11174 | | | | | | ✔ | ✔ | | | | | | |
| | | '378 | | | ✔ | ✔ | | | | | | | | | |
| Octal D-Type True Data | 3S | '374 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | | + | + | |
| | | '11374 | | | | | | ✔ | ✔ | | | | | | |
| | | '574 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | ✔ | + | + | |
| Octal D-Type True Data With Clear | | '273 | ✔ | | | ✔ | ✔ | | | | ✔ | ✔ | + | | |
| | | '11273 | | | | | | ✔ | ✔ | | | | | | |
| | 3S | '575 | ✔ | ✔ | | | | | | | | | | | |
| | | '874 | ✔ | ✔ | | | | | | | | | | | |
| Octal D-Type True Data With Clock Enable | | '377 | | | ✔ | ✔ | ✔ | | | | ✔ | | | | |
| | | '11377 | | | | | | ✔ | ✔ | | | | | | |
| Octal D-Type Inverting | 3S | '534 | ✔ | ✔ | | ✔ | | | | ✔ | ✔ | | | | |
| | | '11534 | | | | | | ✔ | ✔ | | | | | | |
| | | '564 | ✔ | | | | | | | | | | | | |
| | | '576 | ✔ | ✔ | | | | | | | | | | | |
| | | '29826 | | | | | | | | ✔ | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## FLIP-FLOPS AND LATCHES

### Flip-Flops (continued)

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Octal Dual-Ranked True Data | 3S | '4374 | | ✔ | | | | | | | | | | | |
| Octal Inverting With Clear | 3S | '577 | ✔ | | | | | | | | | | | | |
| | | '879 | ✔ | ✔ | | | | | | | | | | | |
| Octal Inverting With Preset | 3S | '876 | ✔ | ✔ | | | | | | | | | | | |
| Octal True Data | 3S | '825 | | ✔ | | | | | | | | | | | |
| | | '11825 | | | | | | | ✔ | | | | | | |
| | | '29825 | | | | | | | | ✔ | | | | | |
| 9-Bit True Data | 3S | '823 | | ✔ | | | | | | | ✔ | | | + | |
| | | '29823 | ✔ | | | | | | | ✔ | | | | | |
| 9-Bit Inverting | 3S | '824 | | ✔ | | | | | | | | | | | |
| | | '29824 | ✔ | | | | | | | | | | | | |
| 10-Bit True Data | 3S | '821 | | ✔ | | | | | | | ✔ | | | + | |
| | | '1821 | | ✔ | | | | | | | | | | | |
| | | '11821 | | | | | | | ✔ | | | | | | |
| | | '29821 | ✔ | | | | | | | ✔ | | | | | |
| 10-Bit Inverting | 3S | '29822 | | | | | | | | ✔ | | | | | |
| 16-Bit D-Type True Data With Clock Enable | | '16377 | | | | | | | | | + | | | | |
| 16-Bit Noninverting | 3S | '16374 | | | | | | ✔ | ✔ | | ✔ | ✔ | | + | + |
| 16-Bit Inverting | 3S | '16534 | | | | | | | | | + | | | | |
| 18-Bit Noninverting | 3S | '16823 | | | | | | | ✔ | | ✔ | | | | + |
| 20-Bit Noninverting | 3S | '16821 | | | | | | | ✔ | | ✔ | | | | + |

✔ Product available in technology indicated
+ New product planned in technology indicated

## FLIP-FLOPS AND LATCHES

### Latches

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| Bistable | 4 | | '75 | | | | ✔ | | | | | | | | | |
| | | | '375 | | | | ✔ | | | | | | | | | |
| D-Type Edge Triggered Inverting and Noninverting | 8 | | '996 | ✔ | | | | | | | | | | | | |
| D-Type Transparent Readback Latch, True | 8 | 3S | '990 | ✔ | | | | | | | | | | | | |
| | 9 | 3S | '992 | ✔ | | | | | | | | | | | | |
| | 10 | 3S | '994 | ✔ | | | | | | | | | | | | |
| D-Type Transparent With Clear, True Outputs | 8 | 3S | '666 | ✔ | | | | | | | | | | | | |
| D-Type Transparent With Clear, Inverting Outputs | 8 | 3S | '667 | ✔ | | | | | | | | | | | | |
| D-Type Transparent True | 8 | 3S | '373 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | | + | + | |
| | | | '11373 | | | | | | ✔ | ✔ | | | | | | |
| | | | '573 | ✔ | ✔ | ✔ | ✔ | ✔ | | | ✔ | ✔ | ✔ | + | + | |
| | 16 | 3S | '16373 | | | | | | ✔ | ✔ | | ✔ | ✔ | | + | + |
| | | | '16373A | | | | | | | | | ✔ | | | | |
| | 32 | 3S | '32373 | | | | | | | | | + | | | | |
| D-Type Dual 4-Bit Transparent True | 8 | 3S | '873 | ✔ | ✔ | | | | | | | | | | | |
| | | | '11873 | | | | | | ✔ | | | | | | | |
| D-Type Transparent Inverting | 8 | 3S | '533 | ✔ | ✔ | | | | | | ✔ | ✔ | | | | |
| | | | '11533 | | | | | | ✔ | ✔ | | | | | | |
| | | | '563 | ✔ | | | ✔ | | | | | | | | | |
| | | | '580 | ✔ | ✔ | | | | | | | | | | | |
| | 16 | 3S | '16533 | | | | | | | | | + | | | | |
| Dual 4-Bit Transparent Inverting | 8 | 3S | '880 | ✔ | ✔ | | | | | | | | | | | |
| 2-Input Multiplexed | 8 | 3S | '604 | | | | ✔ | | | | | | | | | |
| Addressable | 8 | 2S | '259 | ✔ | | | ✔ | | | | | | | | | |
| | | Q | '4724 | | | | ✔ | | | | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## FLIP-FLOPS AND LATCHES

### Latches (continued)

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LVT | LV | LVC | ALVC |
| D-Type True Inputs | 8 | 3S | '845 | ✔ | | | | | | | | | | | | |
| | | | '29845 | ✔ | | | | | | | | | | | | |
| | 9 | 3S | '843 | ✔ | ✔ | | | | | | | + | | | + | |
| | | | '1843 | | ✔ | | | | | | | | | | | |
| | | | '29843 | | | | | | | | ✔ | | | | | |
| | 10 | 3S | '841 | ✔ | ✔ | | | | | | | + | | | + | |
| | | | '29841 | ✔ | | | | | | | ✔ | | | | | |
| | 18 | 3S | '16843 | | | | | | | | | + | | | | + |
| | 20 | 3S | '16841 | | | | | | | ✔ | | ✔ | | | | + |
| D-Type Inverting Inputs | 8 | 3S | '846 | ✔ | | | | | | | | | | | | |
| | | | '29846 | | | | | | | | ✔ | | | | | |
| | 9 | 3S | '29844 | | | | | | | | ✔ | | | | | |
| | 10 | 3S | '842 | ✔ | ✔ | | | | | | | | | | | |
| | | | '29842 | ✔ | | | | | | | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated



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# REGISTERS

## Shift Registers

| DESCRIPTION | NO. OF BITS | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | LV |
| Parallel In, Parallel Out, Bidirectional | 4 | | '194 | | ✔ | | | | | | | |
| | | | '11194 | | | | | | ✔ | ✔ | | |
| | 8 | | '299 | ✔ | | ✔ | | | | | | |
| | | | '323 | ✔ | | | | | | | | |
| Parallel In, Parallel Out | 4 | | '195 | | ✔ | | | | | | | |
| Serial In, Parallel Out | 8 | | '164 | ✔ | | | ✔ | | | | | + |
| Parallel In, Serial Out | 8 | | '165 | ✔ | | | ✔ | | | | | |
| | | | '166 | ✔ | | | ✔ | | | | | |
| Serial In, Parallel Out With Output Latches | 8 | 3S | '594 | | | | ✔ | | | | | |
| | | | '595 | | | | ✔ | | | | | |
| Parallel Out | 10 | | '11898 | | | | | | ✔ | ✔ | | |
| Noninverting | 8 | 3S | '299 | ✔ | | | | | | | | |
| | 9 | 3S | '29823 | ✔ | | | | | | | | |

## Register Files

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| Dual 16 Word × 4 Bits | 3S | '870 | ✔ | | | | | | | | |
| | | '871 | | ✔ | | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## COUNTERS

### Synchronous Counters – Positive Edge Triggered

| DESCRIPTION | PARALLEL LOAD | TYPE | TECHNOLOGY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT |
| 4-Bit Decade Up/Down | Sync | '568 | ✔ | | | | | | | |
| 4-Bit Binary | Sync | '161 | ✔ | ✔ | ✔ | ✔ | | | | |
| | | '163 | ✔ | ✔ | ✔ | ✔ | | | | |
| | | '561 | ✔ | | | | | | | |
| 4-Bit Binary Up/Down | Sync | '169 | ✔ | ✔ | ✔ | | | | | |
| | | '569 | ✔ | | | | | | | |
| | | '8169 | ✔ | | | | | | | |
| | Async | '191 | ✔ | | | ✔ | | | | |
| | | '11191 | | | | | | ✔ | ✔ | |
| | | '193 | ✔ | | | ✔ | | | | |
| 8-Bit Up/Down | Sync Clear | '869 | ✔ | ✔ | | | | | | |
| | Async Clear | '867 | ✔ | ✔ | | | | | | |
| | | '11867 | | | | | | | ✔ | |
| Divide-by-10 Counter | Sync | '4017 | | | | ✔ | | | | |

### Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

| DESCRIPTION | PARALLEL LOAD | TYPE | TECHNOLOGY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT |
| Dual 4-Bit Binary | None | '393 | | | | ✔ | | | | |
| 12-Bit Binary | Sync | '4040 | | | | ✔ | | | | |
| 14-Bit Binary | Sync | '4020 | | | | ✔ | | | | |
| | | '4060 | | | | ✔ | | | | |
| | | '4061 | | | | ✔ | | | | |

### 8-Bit Binary Counters With Registers

| DESCRIPTION | PARALLEL LOAD | TYPE | TECHNOLOGY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT |
| Parallel Register Outputs | 3S | '590 | | | | ✔ | | | | |
| | | '11590 | | | | | | ✔ | ✔ | |
| Parallel Register Inputs | 3S | '11593 | | | | | | ✔ | ✔ | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

### Encoders/Data Selectors/Multiplexers

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| Quad 2-to-1 | | '157 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | + |
| | | '11157 | | | | | | ✔ | ✔ | | | | |
| | | '158 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11158 | | | | | | ✔ | ✔ | | | | |
| | | '298 | | ✔ | | | | | | | | | |
| | 3S | '257 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | | + |
| | | '11257 | | | | | | ✔ | ✔ | | | | |
| | | '258 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11258 | | | | | | | ✔ | | | | |
| Dual 4-to-1 | | '153 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11153 | | | | | | ✔ | ✔ | | | | |
| | | '352 | ✔ | | | | | | | | | | |
| | 3S | '253 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11253 | | | | | | ✔ | ✔ | | | | |
| | | '353 | | ✔ | | | | | | | | | |
| | | '11353 | | | | | | | ✔ | | | | |
| Hex 2-to-1 Universal Multiplexer | 3S | '857 | ✔ | | | | | | | | | | |
| 8-to-1 | | '151 | ✔ | ✔ | ✔ | ✔ | | | | | | | |
| | | '11151 | | | | | | ✔ | ✔ | | | | |
| | 3S | '251 | ✔ | | ✔ | ✔ | | | | | | | |
| | | '11251 | | | | | | ✔ | | | | | |
| | | '354 | | | | ✔ | | | | | | | |
| 16-to-1 | 3S | '250 | | ✔ | | | | | | | | | |
| | | '850 | | ✔ | | | | | | | | | |
| | | '851 | | ✔ | | | | | | | | | |
| Full BCD | | '147 | | | | ✔ | | | | | | | |
| Cascadable Octal | | '148 | | | | ✔ | | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

### Decoders/Demultiplexers

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT | LV | LVC |
| Dual 2-to-4 | | '239 | | | | ✔ | | | | | | | |
| Dual 2-to-4 | | '139 | ✔ | | | ✔ | ✔ | | | | | | + |
| | | '11139 | | | | | | ✔ | ✔ | | | | |
| | OC | '156 | ✔ | | | | | | | | | | |
| 3-to-8 | | '138 | ✔ | ✔ | ✔ | ✔ | ✔ | | | | | ✔ | + |
| | | '11138 | | | | | | ✔ | ✔ | | | | |
| | | '238 | | | | | ✔ | | | | | | |
| | | '11238 | | | | | | ✔ | ✔ | | | | |
| 3-to-8 With Address Registers | | '131 | | ✔ | | | | | | | | | |
| | | '137 | ✔ | | | ✔ | | | | | | | + |
| 3-to-8 With Address Latches | | '237 | | | | ✔ | | | | | | | |
| 4-to-10 BCD-to-Decimal | | '42 | | | | ✔ | | | | | | | |
| 4-to-16 | | '154 | | | | ✔ | | | | | | | |
| 4-to-16 With Address Latches | | '4514 | | | | ✔ | | | | | | | |
| | | '4515 | | | | ✔ | | | | | | | |
| Dual 2-to-4 for Battery Backed-Up Memories | | '2414 | | | | | | | | ✔ | | | |

### Shifters

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 4-Bit Shifter | 3S | '350 | | | ✔ | | | | | | |

✔ Product available in technology indicated
\+ New product planned in technology indicated

## COMPARATORS AND PARITY GENERATORS/CHECKERS

### Comparators

| DESCRIPTION | | | | | | | | TYPE | TECHNOLOGY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INPUT | P=Q | $\overline{P=Q}$ | P>Q | $\overline{P>Q}$ | P<Q | OUTPUT | ENABLE | | ALS | AS | F | HC | HCT | AC | ACT | BCT |
| 8-Bit With 20-kΩ Pullup | Yes | No | No | No | No | OC | Yes | '518 | ✔ | | | | | | | |
| | No | Yes | No | No | No | 2S | Yes | '520 | ✔ | | ✔ | | | | | |
| | | | | | | | | '11520 | | | | | | ✔ | ✔ | |
| | No | Yes | No | No | No | OC | Yes | '522 | ✔ | | | | | | | |
| | No | Yes | No | Yes | No | 2S | No | '682 | | | | ✔ | | | | |
| 8-Bit Standard | Yes | No | No | No | No | OC | Yes | '519 | ✔ | | | | | | | |
| | No | Yes | No | No | No | 2S | Yes | '521 | ✔ | | ✔ | | | | | |
| | | | | | | | | '11521 | | | | | | ✔ | ✔ | |
| | No | Yes | No | Yes | No | 2S | No | '684 | | | | ✔ | | | | |
| | No | Yes | No | No | No | 2S | Yes | '688 | ✔ | | | ✔ | | | | |
| 8-Bit Latched P | No | No | Yes | No | Yes | 2S | Yes | '885 | | ✔ | | | | | | |
| 8-Bit Latched P and Q | Yes | No | Yes | No | Yes | L | Yes | '866 | | ✔ | | | | | | |

### Address Comparators

| DESCRIPTION | OUTPUT ENABLE | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 16-Bit to 4-Bit | Yes | '677 | ✔ | | | | | | | | |
| 12-Bit to 4-Bit | Yes | '679 | ✔ | | | | | | | | |

### Parity Generators/Checkers

| DESCRIPTION | NO. OF BITS | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| Odd/Even Generators/Checkers | 9 | '280 | ✔ | ✔ | ✔ | ✔ | | | | | |
| | | '11280 | | | | | | ✔ | ✔ | | |
| | | '286 | | ✔ | | | | | | | |
| | | '11286 | | | | | | ✔ | ✔ | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## BUS SWITCHES AND 5-V/3-V VOLTAGE TRANSLATORS

### Crossbar Technology (CBT)

| DESCRIPTION | TYPE | TECHNOLOGY |
|---|---|---|
| | | CBT |
| Dual 4-Bit With '244 Pinout | '3244 | + |
| 8-Bit With '245 Pinout | '3245 | + |
| 10-Bit Bus Exchanger | '3383 | + |
| Dual 5-Bit | '3384 | + |
| 10-Bit With Precharged Outputs for Live Insertion | '6800 | + |
| 18-Bit Bus Exchanger | '16209 | + |
| 24-Bit Bus Exchanger | '16212 | + |
| 12-Bit 3-to-1 Bus Select | '16214 | + |

## ARITHMETIC CIRCUITS

### Parallel Binary Adders

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 4-Bit | | '283 | | | ✔ | ✔ | | | | | |

### Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

| DESCRIPTION | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 4-Bit Arithmetic Logic Units: Function Generator | | '181 | | ✔ | | | | | | | |
| | | '11181 | | | | | | | ✔ | | |
| | | '881 | | ✔ | | | | | | | |
| 4-Bit Arithmetic Logic Units With Ripple Carry | | '382 | | | ✔ | | | | | | |

✔ Product available in technology indicated
+ New product planned in technology indicated

## FIFO MEMORIES

### First-In, First-Out Memories (FIFOs)

| DESCRIPTION | | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SIZE | TYPE† | | | LS | S | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 16 Words × 4 Bits | U | 3S | '232B | | | ✔ | | | | | | | | |
| 16 Words × 5 Bits | U | 3S | '225 | | ✔ | | | | | | | | | |
| | | | '229B | | | ✔ | | | | | | | | |
| | | | '233B | | | ✔ | | | | | | | | |
| 32 Words × 9 Bits | B | 3S | '2238 | | | ✔ | | | | | | | | |
| 64 Words × 4 Bits | U | 3S | '234 | | | ✔ | | | | | | | | |
| | | | '236 | | | ✔ | | | | | | | | |
| 64 Words × 5 Bits | U | 3S | '235 | | | ✔ | | | | | | | | |
| 64 Words × 8 Bits | U | 3S | '2232A | | | ✔ | | | | | | | | |
| 64 Words × 9 Bits | U | 3S | '2233A | | | ✔ | | | | | | | | |
| 64 Words × 18 Bits | U, C | 3S | '7813 | | | | | | | | | ✔ | | |
| | U | 3S | '7814 | | | | | | | | | ✔ | | |
| 64 Words × 36 Bits | B, C | 3S | '3612 | | | | | | | | | | | + |
| | | | '3614 | | | | | | | | | | | + |
| | U, C | 3S | '3611 | | | | | | | | | | | + |
| | | | '3613 | | | | | | | | | | | + |
| Dual 64 × 1 | C | 3S | '2226 | | | | | | | | | ✔ | | |
| | | | '2227 | | | | | | | | | ✔ | | |
| Dual 256 × 1 | C | 3S | '2228 | | | | | | | | | ✔ | | |
| | | | '2229 | | | | | | | | | ✔ | | |
| 256 Words × 9 Bits | U | 3S | '7200 | | | | | | | | | ✔ | | |
| 256 Words × 18 Bits | U, C | 3S | '7805 | | | | | | | | | ✔ | | |
| | U | 3S | '7806 | | | | | | | | | ✔ | | |
| 256 × 36 × 2 Bits | B, C | 3S | '3622 | | | | | | | | | + | | |
| 512 Words × 9 Bits | U | 3S | '7201 | | | | | | | | | ✔ | | |
| | U, S | 3S | '72211 | | | | | | | | | ✔ | | |
| 512 Words × 18 Bits | U, C | 3S | '7803 | | | | | | | | | ✔ | | |
| | U | 3S | '7804 | | | | | | | | | ✔ | | |
| | B, C | 3S | '7819 | | | | | | | | | | | ✔ |
| | B | 3S | '7820 | | | | | | | | | | | ✔ |
| 512 Words × 32 Bits | B, C | 3S | '3638 | | | | | | | | | + | | |
| 512 Words × 36 Bits | U, C | 3S | '3631 | | | | | | | | | + | | |
| | B, C | 3S | '3632 | | | | | | | | | ✔ | | |

† U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
+ New product planned in technology indicated

## FIFO MEMORIES

### First-In, First-Out Memories (FIFOs) (continued)

| DESCRIPTION | | OUTPUT | TYPE | TECHNOLOGY | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SIZE | TYPE† | | | LS | S | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 1K Words × 9 Bits | B | 3S | '2235 | | | | | | | | | ✔ | | |
| | | | '2236 | | | | | | | | | ✔ | | |
| | U | 3S | '7202 | | | | | | | | | ✔ | | |
| | U, S | 3S | '72221 | | | | | | | | | ✔ | | |
| 1K Words × 18 Bits | U, C | 3S | '7801 | | | | | | | | | ✔ | | |
| | | | '7811 | | | | | | | | | ✔ | | |
| | | | '7881 | | | | | | | | | + | | |
| | U | 3S | '7802 | | | | | | | | | ✔ | | |
| 1K Words × 36 Bits | U, C | 3S | '3641 | | | | | | | | | + | | |
| 1K × 36 × 2 Bits | B, C | 3S | '3642 | | | | | | | | | + | | |
| 2K Words × 9 Bits | U, C | 3S | '7807 | | | | | | | | | ✔ | | |
| | U | 3S | '7203 | | | | | | | | | + | | |
| | | | '7808 | | | | | | | | | ✔ | | |
| | U, S | 3S | '72231 | | | | | | | | | ✔ | | |
| 2K Words × 18 Bits | U, C | 3S | '7882 | | | | | | | | | + | | |
| 2K Words × 36 Bits | U, C | 3S | '3651 | | | | | | | | | + | | |
| 4K Words × 9 Bits | U | 3S | '7204 | | | | | | | | | ✔ | | |
| | U, S | 3S | '72241 | | | | | | | | | ✔ | | |
| 4K Words × 18 Bits | U, C | 3S | '7884 | | | | | | | | | + | | |

† U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
+ New product planned in technology indicated

## CLOCK DISTRIBUTION CIRCUITS

### Clock Distribution Circuits (CDC)

| DESCRIPTION | TYPE | TECHNOLOGY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | ALS | AS | F | HC | HCT | AC | ACT | BCT | ABT |
| 3.3-V Hex Inverting Clock Drivers/Buffers | '203 | | | | | | ✔ | | | |
| Hex Inverting Clock Drivers/Buffers | '204 | | | | | | ✔ | | | |
| Dual 1-to-4 Clock Drivers/Buffers | '208 | | | | | | | ✔ | | |
| | '209 | | | | | | ✔ | | | |
| Octal Divide-by-2 Clock Drivers (6 inverting, 2 noninverting) | '303 | | ✔ | | | | | | | |
| Octal Divide-by-2 Clock Drivers (8 noninverting) | '305 | | ✔ | | | | | | | |
| Octal Divide-by-2 Clock Drivers (4 inverting, 4 noninverting) | '304 | | ✔ | | | | | | | |
| 1-to-6 Clock Drivers | '328 | | | | | | | | | ✔ |
| | '328A | | | | | | | | | + |
| | '329 | | | | | | | | | ✔ |
| | '329A | | | | | | | | | ✔ |
| 1-to-6 Clock Drivers With Output Enable | '391 | | | | | | | | | ✔ |
| | '392 | | | | | | | | | ✔ |
| 1-to-8 Clock Drivers | '340 | | | | | | | | | ✔ |
| | '341 | | | | | | | | | ✔ |
| 1-to-8, Divide-by-2 Clock Drivers | '337 | | | | | | | | | ✔ |
| | '339 | | | | | | | | | ✔ |
| Phase-Locked Loop 1-to-12 Clock Drivers | '582 | | | | | | | | | + |
| | '586 | | | | | | | | | + |
| | '2586 | | | | | | | | | + |

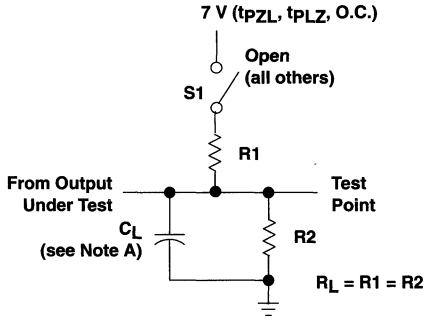
✔ Product available in technology indicated
+ New product planned in technology indicated

## ECL TRANSLATORS

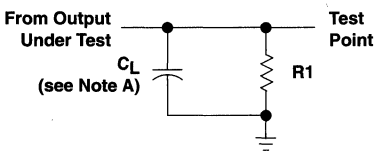
### ECL-to-TTL or TTL-to-ECL Translators

| DESCRIPTION | LEVEL TRANSLATION | OUTPUT | TYPE |
|---|---|---|---|
| Octal Bus Driver, Inverting | ECL-to-TTL | 3S | 10KHT5540 |
| | TTL-to-ECL | OE | 10KHT5542 |
| Octal Bus Driver, Noninverting | ECL-to-TTL | 3S | 10KHT5541 |
| | TTL-to-ECL | OE | 10KHT5543 |
| | | | 100KT5543 |
| Octal D-Type Latch, True | ECL-to-TTL | 3S | 10KHT5573 |
| | | | 100KT5573 |
| Octal D-Type Flip-Flop, True | ECL-to-TTL | 3S | 10KHT5574 |
| | TTL-to-ECL | OE | 10KHT5578 |
| | | | 100KT5578 |

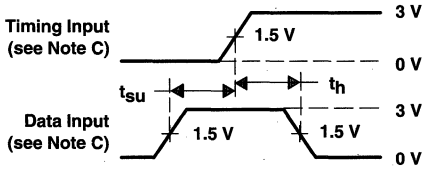
## LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR SN54/74F DEVICES



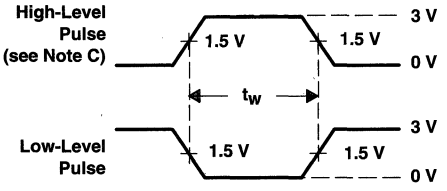

LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



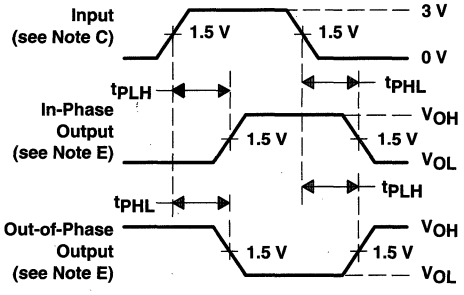

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



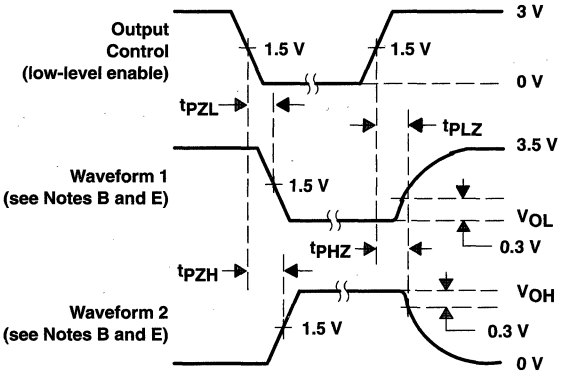

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one transition per measurement.

General Information 1
Data Sheets 2
Application Report 3
Mechanical Data 4

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

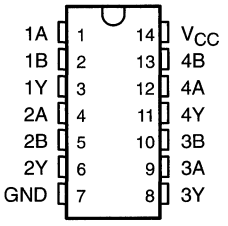
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54F00 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F00 is characterized for operation from 0°C to 70°C.

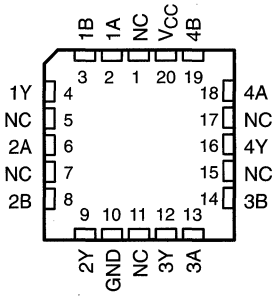
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

**SN54F00 . . . J PACKAGE**
**SN74F00 . . . D OR N PACKAGE**
**(TOP VIEW)**

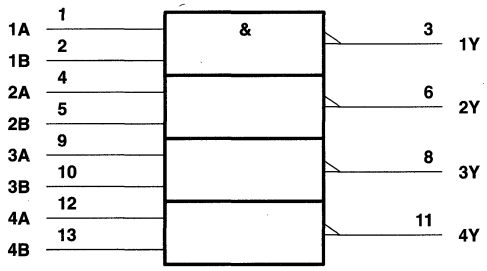



**SN54F00 . . . FK PACKAGE**
**(TOP VIEW)**



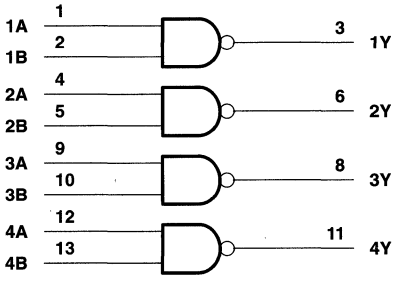

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F00 ..... −55°C to 125°C
SN74F00 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F00 | | | SN74F00 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F00 | | | SN74F00 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 1.9 | 2.8 | | 1.9 | 2.8 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 6.8 | 10.2 | | 6.8 | 10.2 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F00 | | | SN54F00 | | SN74F00 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 1.6 | 3.3 | 5 | 2 | 7 | 1.6 | 6 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 4.3 | 1.5 | 6.5 | 1 | 5.3 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

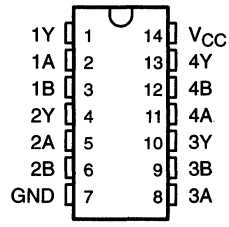
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN54F02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F02 is characterized for operation from 0°C to 70°C.

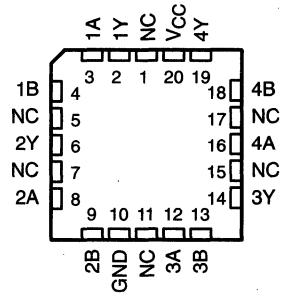
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

**SN54F02 . . . J PACKAGE**
**SN74F02 . . . D OR N PACKAGE**
**(TOP VIEW)**

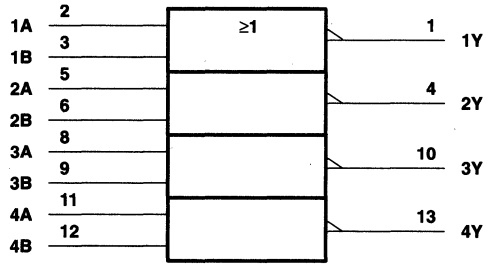



**SN54F02 . . . FK PACKAGE**
**(TOP VIEW)**



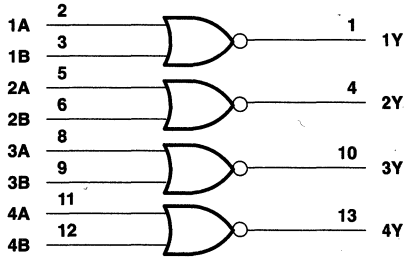

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F02 ..... −55°C to 125°C
SN74F02 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F02 | | | SN74F02 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F02 | | | SN74F02 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 3.7 | 5.6 | | 3.7 | 5.6 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 8.7 | 13 | | 8.7 | 13 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CCL}$ is measured with one input at 4.5 V and all others grounded.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F02 | | | SN54F02 | | SN74F02 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 1.7 | 4 | 5.5 | 1.7 | 7.5 | 1.7 | 6.5 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 4.3 | 1 | 6.5 | 1 | 5.3 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

SDFS037A – MARCH 1987 – REVISED OCTOBER 1993

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

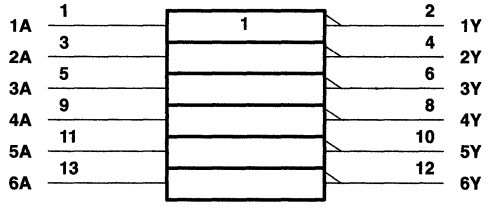
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54F04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F04 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each inverter)**

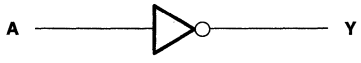
| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic symbol†



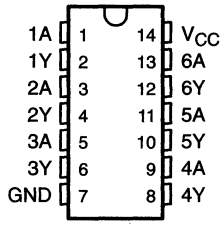

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram, each inverter (positive logic)

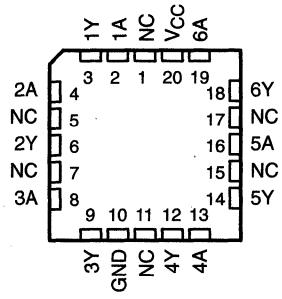



Pin numbers shown are for the D, J, and N packages.

**SN54F04 . . . J PACKAGE**
**SN74F04 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F04 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F04 ..... −55°C to 125°C
SN74F04 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F04 | | | SN74F04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F04 | | | SN74F04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 2.8 | 4.2 | | 2.8 | 4.2 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 10.2 | 15.3 | | 10.2 | 15.3 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F04 | | | SN54F04 | | SN74F04 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.6 | 3.3 | 5 | 1.2 | 7 | 1.6 | 6 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 4.3 | 1 | 6.5 | 1 | 5.3 | |

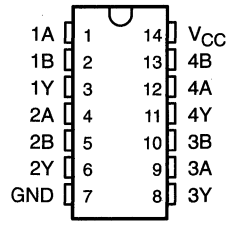
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

SDFS038A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

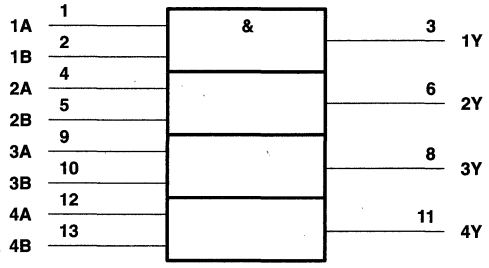
The SN74F08 contains four independent 2-input AND gates. It performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74F08 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram, each gate (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 5.5 | 8.3 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 8.6 | 12.9 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 2.2 | 3.8 | 5.6 | 2.2 | 6.6 | ns |
| $t_{PHL}$ | | | 1.7 | 3.6 | 5.3 | 1.7 | 6.3 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

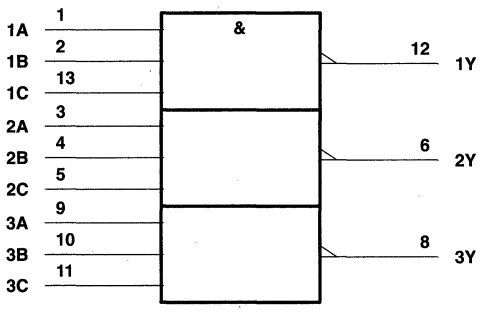
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54F10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F10 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each gate)**

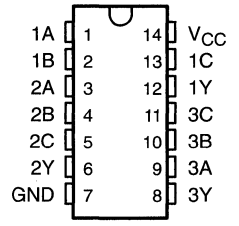
| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

## logic symbol†

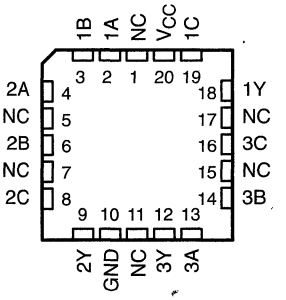



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

**SN54F10 . . . J PACKAGE**
**SN74F10 . . . D OR N PACKAGE**
**(TOP VIEW)**

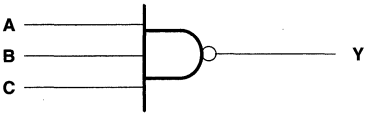



**SN54F10 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F10 ..... −55°C to 125°C
SN74F10 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F10 | | | SN74F10 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F10 | | | SN74F10 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 1.4 | 2.1 | | 1.4 | 2.1 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 5.1 | 7.7 | | 5.1 | 7.7 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F10 | | | SN54F10 | | SN74F10 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, or C | Y | 1.6 | 3.3 | 5 | 1.2 | 7 | 1.6 | 6 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 4.3 | 1 | 6.5 | 1 | 5.3 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

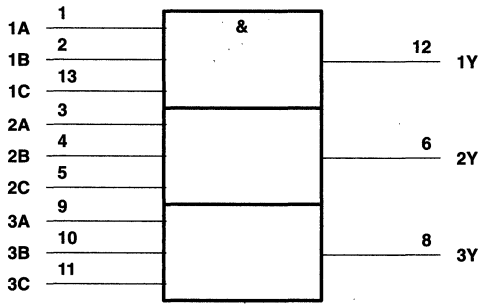
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \bullet B \bullet C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54F11 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F11 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each gate)**

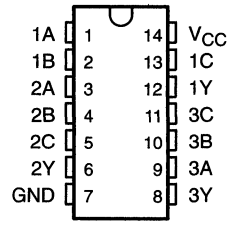
| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

## logic symbol†

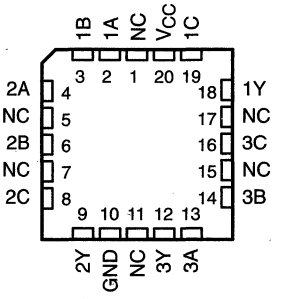



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

**SN54F11 . . . J PACKAGE**
**SN74F11 . . . D OR N PACKAGE**
**(TOP VIEW)**

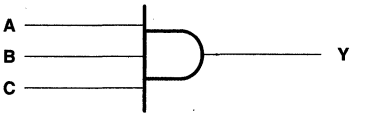



**SN54F11 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F11 ..... −55°C to 125°C
SN74F11 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F11 | | | SN74F11 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F11 | | | SN74F11 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 4.1 | 6.2 | | 4.1 | 6.2 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 6.5 | 9.7 | | 6.5 | 9.7 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F11 | | | SN54F11 | | SN74F11 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, or C | Y | 2.2 | 3.8 | 5.6 | 1.7 | 7.5 | 2.2 | 6.6 | ns |
| $t_{PHL}$ | | | 1.7 | 3.7 | 5.5 | 1.2 | 7.5 | 1.7 | 6.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

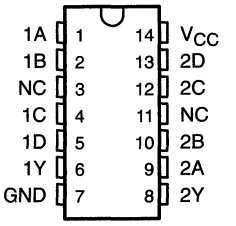
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54F20 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F20 is characterized for operation from 0°C to 70°C.

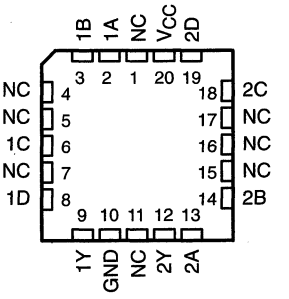
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |

**SN54F20 . . . J PACKAGE**
**SN74F20 . . . D OR N PACKAGE**
**(TOP VIEW)**

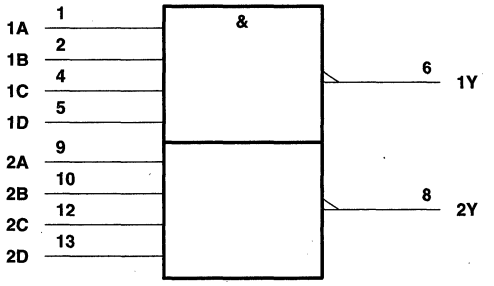



**SN54F20 . . . FK PACKAGE**
**(TOP VIEW)**



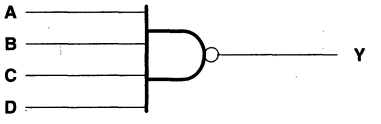

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F20 ..... −55°C to 125°C
SN74F20 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F20 | | | SN74F20 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F20 | | | SN74F20 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 0.9 | 1.4 | | 0.9 | 1.4 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 3.4 | 5.1 | | 3.4 | 5.1 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F20 | | | SN54F20 | | SN74F20 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, C, or D | Y | 1.6 | 3.3 | 5 | 1.2 | 7 | 1.6 | 6 | ns |
| $t_{PHL}$ | | | 1 | 2.8 | 4.3 | 1 | 6.5 | 1 | 5.3 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

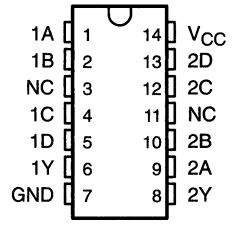
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \bullet B \bullet C \bullet D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54F21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F21 is characterized for operation from 0°C to 70°C.

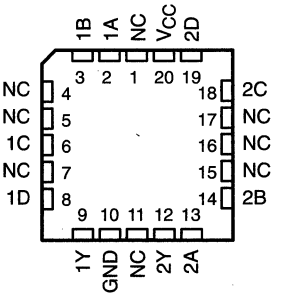
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| H | H | H | H | H |
| L | X | X | X | L |
| X | L | X | X | L |
| X | X | L | X | L |
| X | X | X | L | L |

**SN54F21 . . . J PACKAGE**
**SN74F21 . . . D OR N PACKAGE**
**(TOP VIEW)**

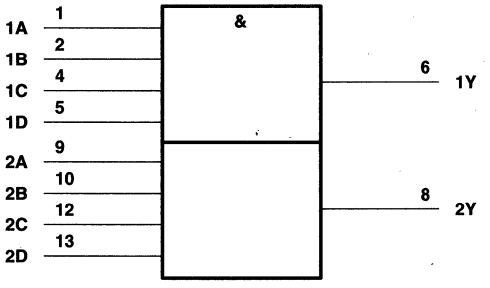



**SN54F21 . . . FK PACKAGE**
**(TOP VIEW)**



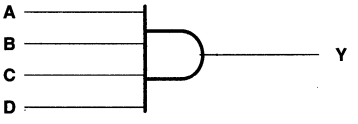

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F21 ..... −55°C to 125°C
SN74F21 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F21 | | | SN74F21 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F21 | | | SN74F21 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 2.8 | 4.3 | | 2.8 | 4.3 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 4.7 | 7.3 | | 4.7 | 7.3 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F21 | | | SN54F21 | | SN74F21 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, C, or D | Y | 1 | 3.2 | 4.7 | 1 | 5.6 | 1 | 5.3 | ns |
| $t_{PHL}$ | | | 1.5 | 3.4 | 5.1 | 1.5 | 5.9 | 1.5 | 5.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

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- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

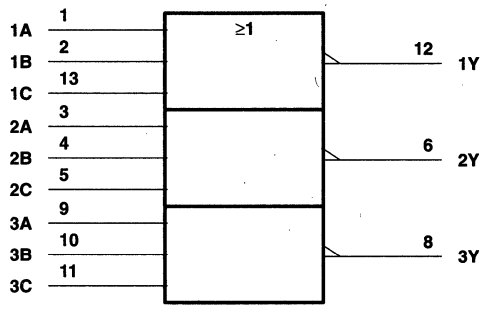
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ or $Y = \overline{A + B + C}$ in positive logic.

The SN54F27 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F27 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each gate)**

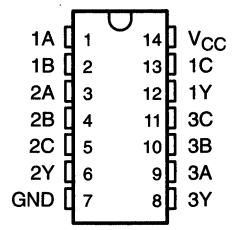
| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | X | X | L |
| X | H | X | L |
| X | X | H | L |
| L | L | L | H |

## logic symbol†

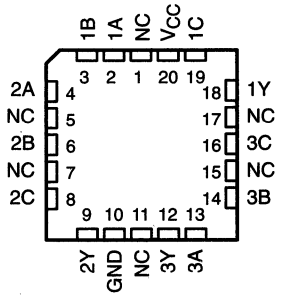



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

**SN54F27 . . . J PACKAGE**
**SN74F27 . . . D OR N PACKAGE**
**(TOP VIEW)**

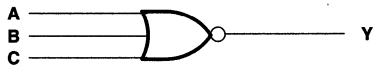



**SN54F27 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F27 ..... −55°C to 125°C
SN74F27 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F27 | | | SN74F27 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F27 | | | SN74F27 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 3.8 | 5.5 | | 3.8 | 5.5 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 8.4 | 12 | | 8.4 | 12 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CCL}$ is measured with one input at 4.5 V and all others grounded.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F27 | | | SN54F27 | | SN74F27 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, or C | Y | 1.2 | 3.1 | 5 | 1 | 6 | 1 | 5.5 | ns |
| $t_{PHL}$ | | | 1 | 2.1 | 4.5 | 1 | 5.5 | 1 | 4.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

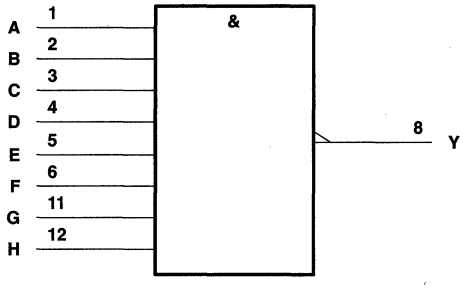
These devices contain a single 8-input NAND gate. They perform the Boolean functions $Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$ in positive logic.

The SN54F30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F30 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

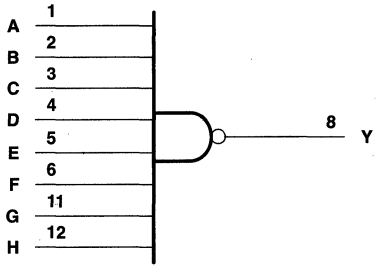
| INPUTS A–H | OUTPUT Y |
|---|---|
| All inputs H | L |
| One or more inputs L | H |

## logic symbol†



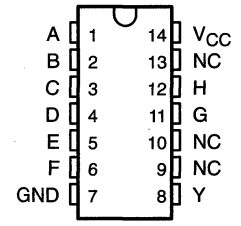

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

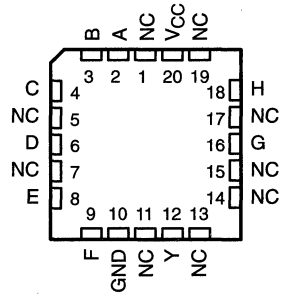



Pin numbers shown are for the D, J, and N packages.

**SN54F30 . . . J PACKAGE**
**SN74F30 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F30 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F30 ..... −55°C to 125°C
SN74F30 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F30 | | | SN74F30 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F30 | | | SN74F30 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 0.7 | 1.5 | | 0.7 | 1.5 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 2.2 | 4 | | 2.2 | 4 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F30 | | | SN54F30 | | SN74F30 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A thru H | Y | 1 | 3.1 | 5 | 1 | 6 | 1 | 5.5 | ns |
| $t_{PHL}$ | | | 1 | 2.6 | 4.5 | 1 | 6 | 1 | 5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

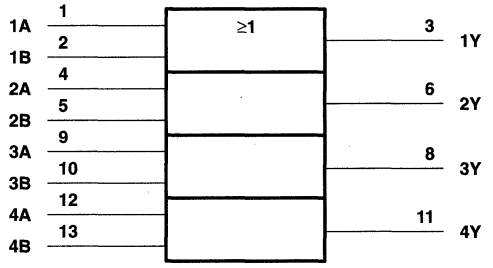
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

The SN54F32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F32 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each gate)**

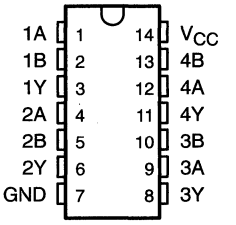
| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

## logic symbol†

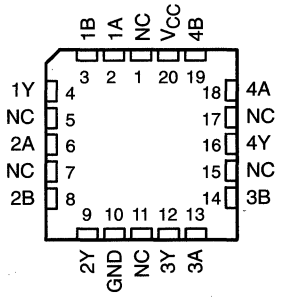



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

**SN54F32 . . . J PACKAGE**
**SN74F32 . . . D OR N PACKAGE**
**(TOP VIEW)**

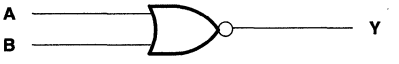



**SN54F32 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## logic diagram, each gate (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F32 ..... −55°C to 125°C
SN74F32 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F32 | | | SN74F32 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F32 | | | SN74F32 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 6.1 | 9.2 | | 6.1 | 9.2 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 10.3 | 15.5 | | 10.3 | 15.5 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CCH}$ is measured with one input per gate at 4.5 V and all others grounded.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F32 | | | SN54F32 | | SN74F32 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 2.2 | 3.8 | 5.6 | 2.2 | 7.5 | 2.2 | 6.6 | ns |
| $t_{PHL}$ | | | 2.2 | 3.6 | 5.3 | 1.7 | 7.5 | 2.2 | 6.3 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

These devices contain four independent 2-input NAND buffer gates with open-collector outputs. They perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

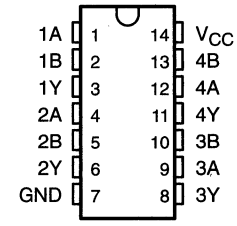
The open-collector outputs require pullup resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher $V_{OH}$ levels.

The SN54F38 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F38 is characterized for operation from 0°C to 70°C.

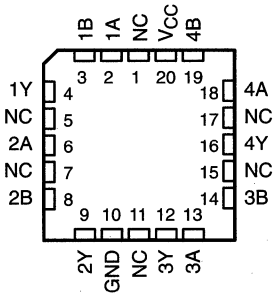
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

**SN54F38 . . . J PACKAGE**
**SN74F38 . . . D OR N PACKAGE**
**(TOP VIEW)**

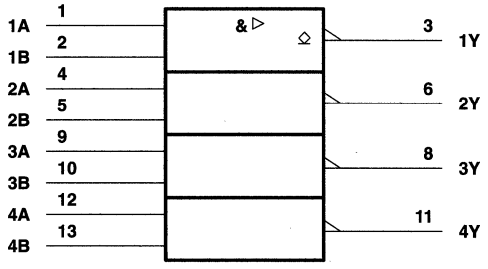



**SN54F38 . . . FK PACKAGE**
**(TOP VIEW)**

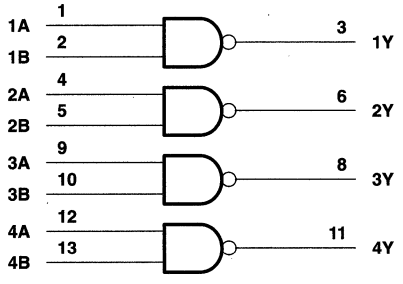



NC – No internal connection

## logic symbol†




## logic diagram (positive logic)




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . −0.5 V to $V_{CC}$
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range: SN54F38 . . . . . −55°C to 125°C
SN74F38 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

| | | SN54F38 | | | SN74F38 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $V_{OH}$ | High-level output voltage | | | 4.5 | | | 4.5 | V |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F38 | | | SN74F38 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | −0.73 | −1.2 | | | −1.2 | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OH}$ | $V_{CC}$ = 4.5 V | | | | 250 | | | 250 | µA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 4 | 7 | | 4 | 7 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 22 | 30 | | 22 | 30 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F38 | | | SN54F38 | | SN74F38 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 6.7 | 9.6 | 12.5 | 6.2 | 14 | 6.7 | 13 | ns |
| $t_{PHL}$ | | | 1 | 2.6 | 5 | 1 | 6.5 | 1 | 5.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

SDFS092 – JANUARY 1989 – REVISED OCTOBER 1993

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

These devices contain 2-wide 2-input and 2-wide 3-input AND-OR-INVERT gates. They perform the following Boolean functions:

$$1Y = \overline{(1A \bullet 1B \bullet 1C) + (1D \bullet 1E \bullet 1F)}$$

$$2Y = \overline{(2A \bullet 2B) + (2C \bullet 2D)}$$

The SN54F51 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F51 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLES**

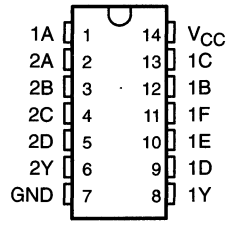
**GATE 1**

| INPUTS | | | | | | OUTPUT |
|---|---|---|---|---|---|---|
| 1A | 1B | 1C | 1D | 1E | 1F | 1Y |
| H | H | H | X | X | X | L |
| X | X | X | H | H | H | L |
| All other combinations | | | | | | H |

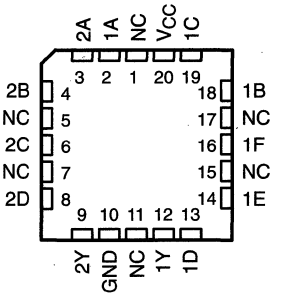
**GATE 2**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| 2A | 2B | 2C | 2D | 2Y |
| H | H | X | X | L |
| X | X | H | H | L |
| All other combinations | | | | H |

**SN54F51 . . . J PACKAGE**
**SN74F51 . . . D OR N PACKAGE**
**(TOP VIEW)**

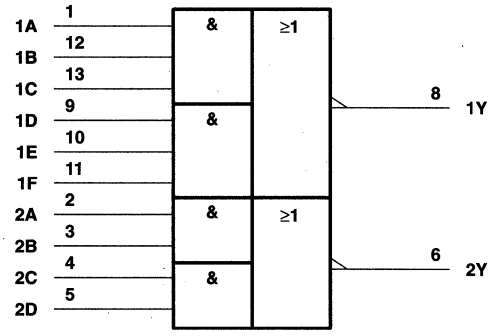



**SN54F51 . . . FK PACKAGE**
**(TOP VIEW)**



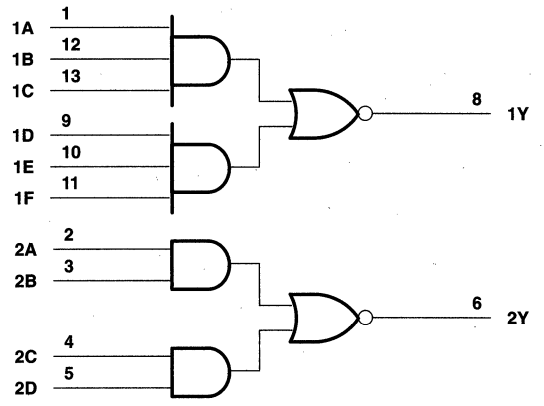

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F51 ..... −55°C to 125°C
SN74F51 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F51 | | | SN74F51 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F51 | | | SN74F51 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = − 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = − 1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.35 | 0.5 | | 0.35 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 100 | | | 100 | µA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | − 0.6 | | | − 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 1.8 | 3 | | 1.8 | 3 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 5.5 | 7.5 | | 5.5 | 7.5 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F51 | | | SN54F51 | | SN74F51 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any input | Y | 2 | 3.5 | 5.5 | 1.5 | 7.5 | 1.5 | 6.5 | ns |
| $t_{PHL}$ | | | 1 | 2.5 | 4 | 1 | 5 | 1 | 4.5 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

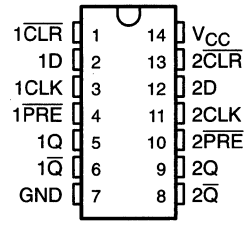
The SN54F74 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F74 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

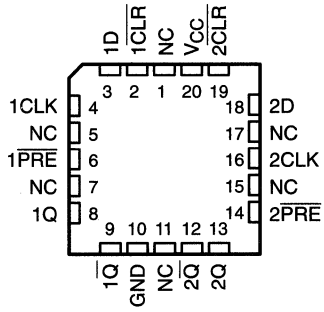
| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H† | H† |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

† The output levels are not guaranteed to meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

**SN54F74 . . . J PACKAGE**
**SN74F74 . . . D OR N PACKAGE**
**(TOP VIEW)**

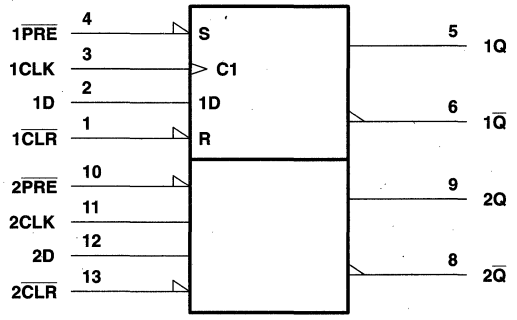



**SN54F74 . . . FK PACKAGE**
**(TOP VIEW)**



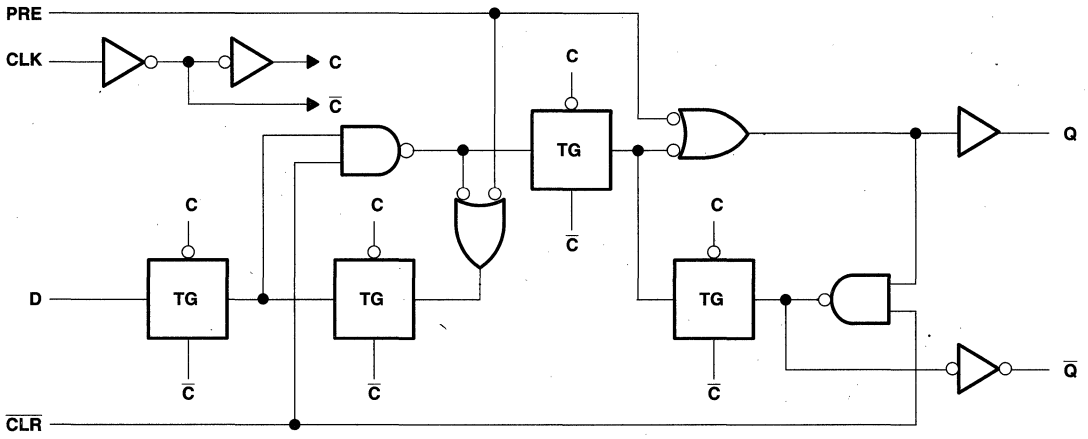

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram, each flip-flop (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F74 ..... −55°C to 125°C
SN74F74 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F74 | | | SN74F74 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F74 | | | SN74F74 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | Data, CLK | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | −1.8 | | | −1.8 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 10.5 | 16 | | 10.5 | 16 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with D, CLK, and $\overline{PRE}$ grounded then with D, CLK, and $\overline{CLR}$ grounded.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F74 | | SN74F74 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 'F74 | | | | | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 80 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLK high, $\overline{PRE}$ or $\overline{CLR}$ low | 4 | | 4 | | 4 | | ns |
| | | CLK low | 5 | | 6 | | 5 | | |
| $t_{su}$ | Setup time, data before CLK↑ | High | 2 | | 3 | | 2 | | ns |
| | | Low | 3 | | 4 | | 3 | | |
| | Setup time, inactive-state before CLK↑§ | $\overline{PRE}$ or $\overline{CLR}$ to CLK | 2 | | 3 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | High | 1 | | 2 | | 1 | | ns |
| | | Low | 1 | | 2 | | 1 | | |

§ Inactive-state setup time is also referred to as recovery time.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F74 | | | SN54F74 | | SN74F74 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 145 | | 80 | | 100 | | MHz |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 3 | 4.9 | 6.8 | 3.8 | 8.5 | 3 | 7.8 | ns |
| $t_{PHL}$ | | | 3.6 | 5.8 | 8 | 4.4 | 10.5 | 3.6 | 9.2 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2.4 | 4.2 | 6.1 | 3.2 | 8 | 2.4 | 7.1 | ns |
| $t_{PHL}$ | | | 2.7 | 6.6 | 9 | 3.5 | 11.5 | 2.7 | 10.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

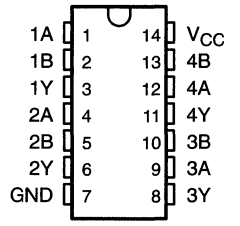
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54F86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F86 is characterized for operation from 0°C to 70°C.

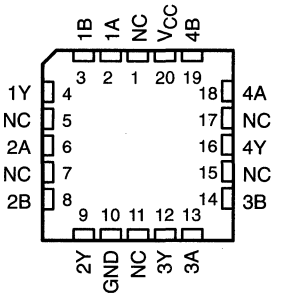
**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

**SN54F86 . . . J PACKAGE**
**SN74F86 . . . D OR N PACKAGE**
**(TOP VIEW)**

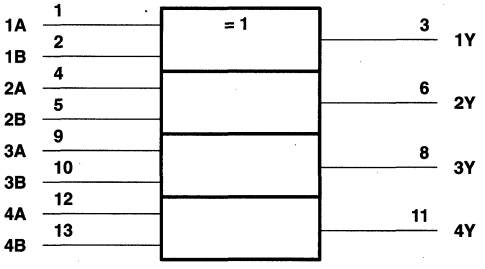



**SN54F86 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## logic symbol†

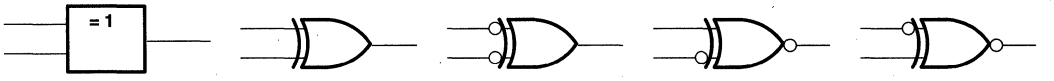



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## exclusive-OR logic

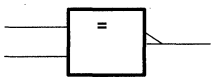
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

**EXCLUSIVE-OR**



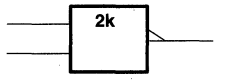

These are five equivalent exclusive-OR symbols valid for an 'F86 gate in positive logic; negation may be shown at any two ports.

**LOGIC-IDENTITY ELEMENT**



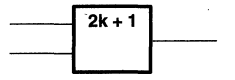

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

**EVEN-PARITY ELEMENT**




The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

**ODD-PARITY ELEMENT**




The output is active (high) if an odd number of outputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F86 ..... −55°C to 125°C
SN74F86 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F86 | | | SN74F86 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F86 | | | SN74F86 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –60 | | –150 | –60 | | –150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 15 | 23 | | 15 | 23 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 18 | 28 | | 18 | 28 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCH}$ is measured with outputs open, and the A or B input (not both) at 4.5 V. Remaining inputs are grounded.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F86 | | | SN54F86 | | SN74F86 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B (other input low) | Y | 3 | 4 | 5.5 | 3 | 7 | 3 | 6.5 | ns |
| $t_{PHL}$ | | | 3 | 4.2 | 5.5 | 2.6 | 8 | 3 | 6.5 | |
| $t_{PLH}$ | A or B (other input low) | Y | 3.5 | 5.3 | 7 | 3.5 | 10 | 3.5 | 8 | ns |
| $t_{PHL}$ | | | 3 | 4.7 | 6.5 | 3 | 8 | 3 | 7.5 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

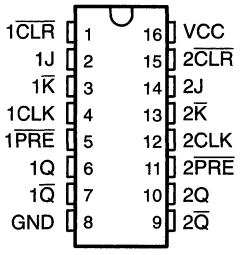
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

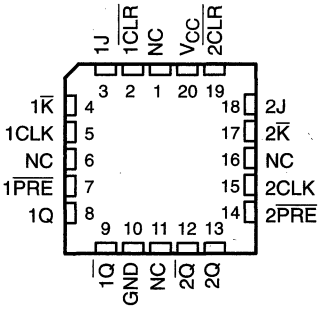
These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and $\overline{K}$ input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The SN54F109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F109 is characterized for operation from 0°C to 70°C.

**SN54F109 . . . J PACKAGE**
**SN74F109 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F109 . . . FK PACKAGE**
**(TOP VIEW)**



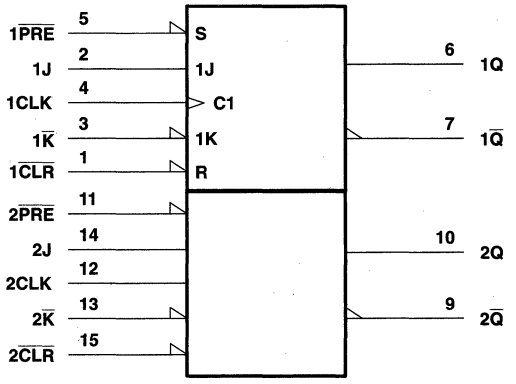

NC – No internal connection

**FUNCTION TABLE**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | $\overline{K}$ | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | $Q_0$ | $\overline{Q}_0$ |

† The output levels are not guaranteed to meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
‘Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F109 ..... −55°C to 125°C
SN74F109 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F109 | | | SN74F109 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F109 | | | SN74F109 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = − 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = − 1 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | J, $\overline{K}$, CLK | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | − 0.6 | | | − 0.6 | mA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | − 1.8 | | | − 1.8 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 11.7 | 17 | | 11.7 | 17 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F109 | | SN74F109 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 'F74 | | | | | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 70 | 0 | 90 | MHz |
| $t_w$ | Pulse duration | CLK high, $\overline{PRE}$ or $\overline{CLR}$ low | 4 | | 4 | | 4 | | ns |
| | | CLK low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time, data before CLK↑ | High | 3 | | 3 | | 3 | | ns |
| | | Low | 3 | | 3 | | 3 | | |
| | Setup time, inactive-state before CLK↑§ | $\overline{PRE}$ or $\overline{CLR}$ to CLK | 2 | | 2 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | High | 1 | | 1 | | 1 | | ns |
| | | Low | 1 | | 1 | | 1 | | |

§ Inactive-state setup time is also referred to as recovery time.

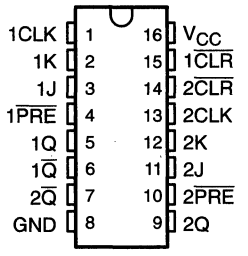
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX¶ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F109 | | | SN54F109 | | SN74F109 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 150 | | 70 | | 90 | | MHz |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 3 | 4.9 | 7 | 3 | 9 | 3 | 8 | ns |
| $t_{PHL}$ | | | 3.6 | 5.8 | 8 | 3.6 | 10.5 | 3.6 | 9.2 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2.4 | 4.8 | 7 | 2.4 | 9 | 2.4 | 8 | ns |
| $t_{PHL}$ | | | 2.7 | 6.6 | 9 | 2.7 | 11.5 | 2.7 | 10.5 | |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)




## description

The SN74F112 contains two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. The SN74F112 can perform as a toggle flip-flop by tying J and K high.

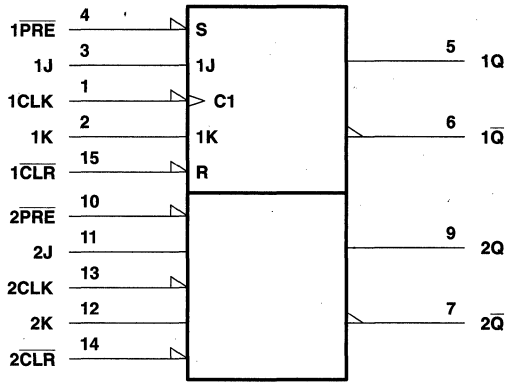
The SN74F112 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

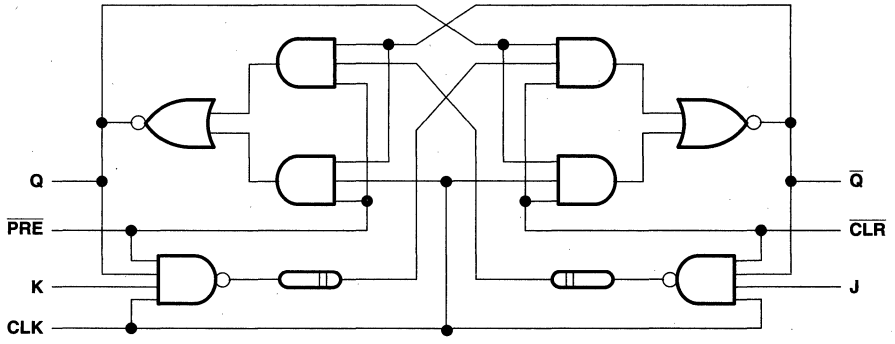
† The output levels in this configuration are not guaranteed to meet the minimum levels for $V_{OH}$. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram, each flip-flop (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | J or K | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | mA |
| | $\overline{PRE}$ or $\overline{CLR}$ | | | | | −3 | |
| | CLK | | | | | −2.4 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 12 | 19 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with all outputs open, the Q and $\overline{Q}$ outputs alternately high and the clock input grounded at the time of measurement.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | 0 | 110 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLK high or low | 4.5 | | 5 | | ns |
| | | $\overline{CLR}$ or $\overline{PRE}$ low | 4.5 | | 5 | | |
| $t_{su}$ | Setup time, data before CLK↓ | High | 4 | | 5 | | ns |
| | | Low | 3 | | 3.5 | | |
| $t_h$ | Hold time, data after CLK↓ | High | 0 | | 0 | | ns |
| | | Low | 0 | | 0 | | |
| $t_{su}$ | Setup time, inactive state, data before CLK↓§ | $\overline{CLR}$ or $\overline{PRE}$ high | 4 | | 5 | | ns |

§ Inactive-state state setup time is also referred to as recovery time.

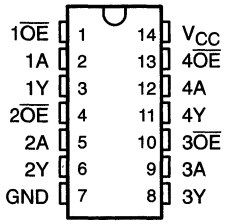
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 110 | 130 | | 100 | | MHz |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 1.2 | 4.6 | 6.5 | 1.2 | 7.5 | ns |
| $t_{PHL}$ | | | 1.2 | 4.6 | 6.5 | 1.2 | 7.5 | |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 1.2 | 4.1 | 6.5 | 1.2 | 7.5 | ns |
| $t_{PHL}$ | | | 1.2 | 4.1 | 6.5 | 1.2 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

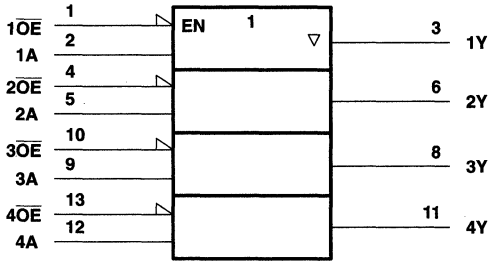
The SN74F125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output enable ($\overline{OE}$) input is high.

The SN74F125 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

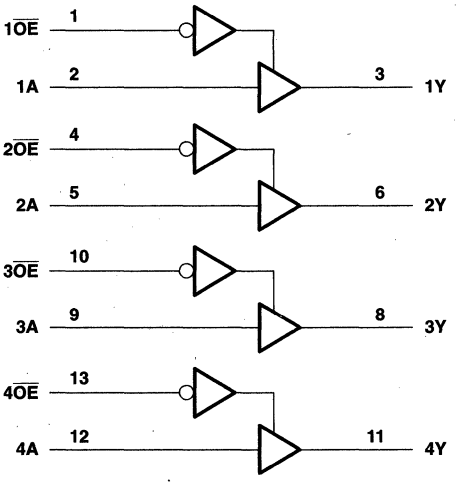
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 128 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = −15 mA | 2 | 3.1 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | 0.4 | 0.55 | V |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −20 | µA |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | µA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 17 | 24 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 28 | 40 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 25 | 35 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

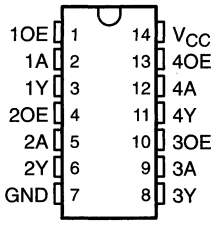
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.2 | 3.6 | 6 | 1.2 | 6.5 | ns |
| $t_{PHL}$ | | | 2.2 | 5.1 | 7.5 | 2.2 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 2.7 | 5.1 | 7.5 | 2.7 | 8.5 | ns |
| $t_{PZL}$ | | | 3.2 | 5.6 | 8 | 3.2 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1 | 3.1 | 5 | 1 | 6 | ns |
| $t_{PLZ}$ | | | 1 | 3.1 | 5.5 | 1 | 6 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

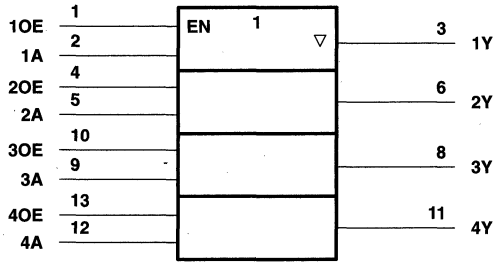
The SN74F126 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output enable (OE) input is low.

The SN74F126 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

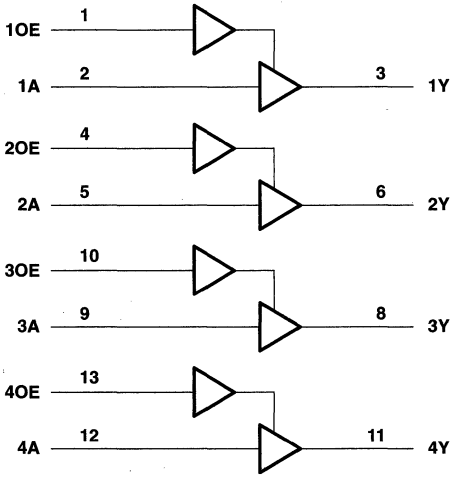
| INPUTS | | OUTPUT |
|---|---|---|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 128 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = −15 mA | 2 | 3.1 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | 0.4 | 0.55 | V |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −20 | μA |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | μA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 20 | 30 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 32 | 48 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 26 | 39 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

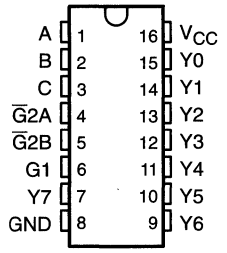
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 2 | 4 | 6.5 | 2 | 7 | ns |
| $t_{PHL}$ | | | 3 | 5.5 | 8 | 2.8 | 8.5 | |
| $t_{PZH}$ | OE | Y | 3.8 | 6 | 7.5 | 3.3 | 8.5 | ns |
| $t_{PZL}$ | | | 3.8 | 6 | 8 | 3.5 | 8.5 | |
| $t_{PHZ}$ | OE | Y | 2 | 4.5 | 6.5 | 2 | 7.5 | ns |
| $t_{PLZ}$ | | | 3 | 5.5 | 7.5 | 3 | 8 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

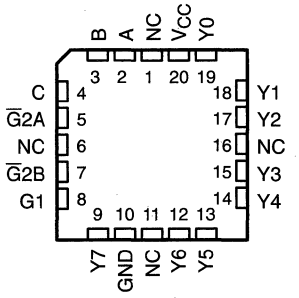
SDFS051A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F138 . . . J PACKAGE**
**SN74F138 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F138 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'F138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

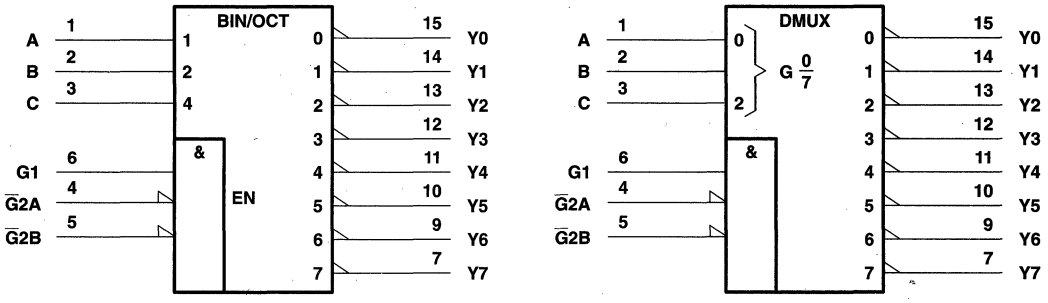
The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54F138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F138 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

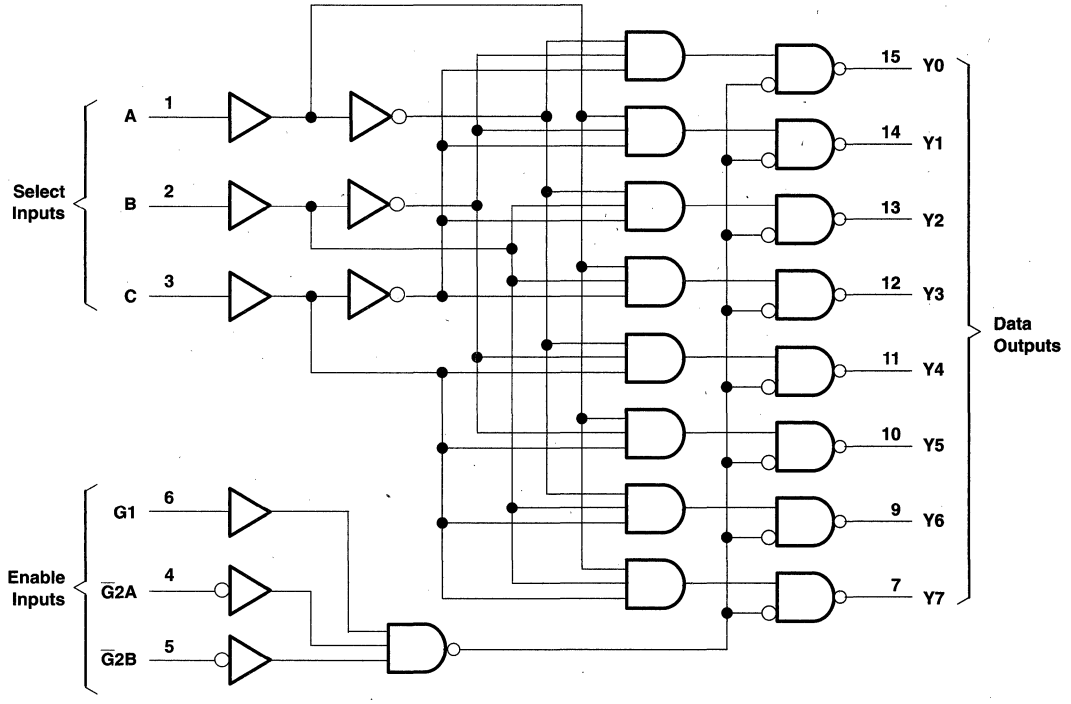
| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

## logic symbols (alternatives)†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F138 ..... −55°C to 125°C
SN74F138 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F138 | | | SN74F138 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F138 | | | SN74F138 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 13 | 20 | | 13 | 20 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured with outputs enabled and open.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F138 | | | SN54F138 | | SN74F138 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, or C | Y | 2.7 | 5.2 | 7.5 | 2.7 | 12 | 2.7 | 8.5 | ns |
| $t_{PHL}$ | | | 3.2 | 5.7 | 8 | 3.2 | 9.5 | 3.2 | 9 | |
| $t_{PLH}$ | $\overline{G}$2A or $\overline{G}$2B | Y | 2.7 | 5 | 7 | 2.7 | 11 | 2.7 | 8 | ns |
| $t_{PHL}$ | | | 2.2 | 4.9 | 7 | 2.2 | 8 | 2.2 | 7.5 | |
| $t_{PLH}$ | G1 | Y | 3.2 | 5.8 | 8 | 3.2 | 12.5 | 3.2 | 9 | ns |
| $t_{PHL}$ | | | 2.7 | 5.2 | 7.5 | 2.7 | 8.5 | 2.7 | 8.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

SDFS023A – D2932, MARCH 1987 – REVISED OCTOBER 1993

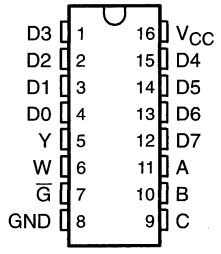
- **8-Line to 1-Line Multiplexers Can Perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

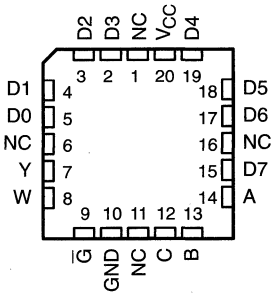
These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe ($\overline{G}$) input must be at a low logic level to enable the data selection/multiplexing function. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54F151B is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F151B is characterized for operation from 0°C to 70°C.

**SN54F151B . . . J PACKAGE**
**SN74F151B . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F151B . . . FK PACKAGE**
**(TOP VIEW)**



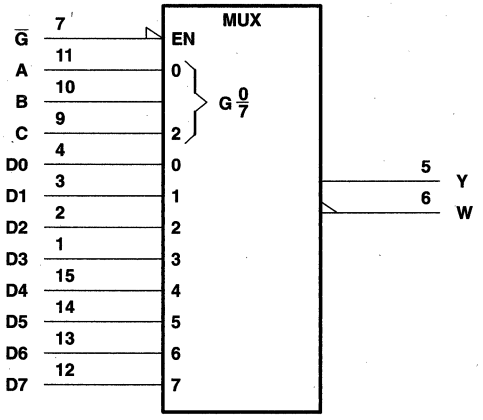

NC – No internal connection

**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| SELECT | | | STROBE | | |
| C | B | A | $\overline{G}$ | Y | W |
| X | X | X | H | L | H |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

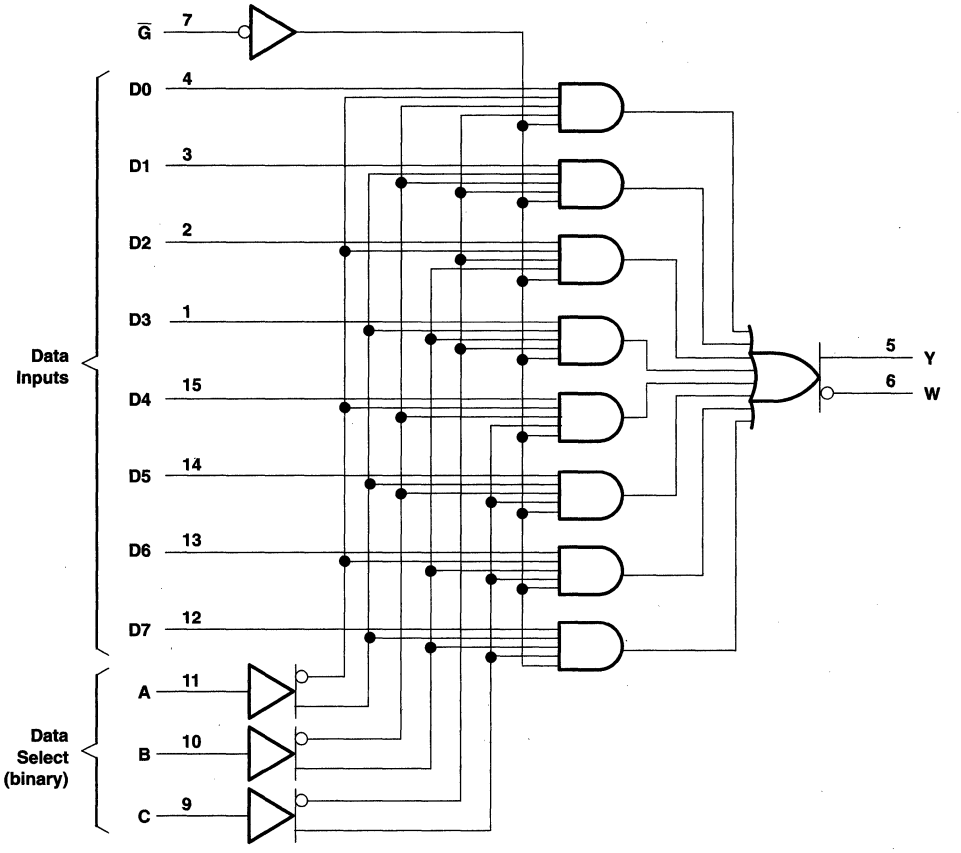
D0, D1, . . . D7 = the level of the respective D input.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F151B ..... 40 mA
SN74F151B ..... 48 mA
Operating free-air temperature range: SN54F151B ..... −55°C to 125°C
SN74F151B ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage rating may be exceeded provided that the input current rating is observed.

## recommended operating conditions

| | | SN54F151B | | | SN74F151B | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F151B | | | SN74F151B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 13.5 | 21 | | 13.5 | 21 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F151B | | | SN54F151B | | SN74F151B | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, or C | W | 3.8 | 5.2 | 9 | 2 | 11.5 | 3.5 | 9.5 | ns |
| $t_{PHL}$ | | | 2.9 | 4.3 | 7.5 | 2.6 | 8 | 2.7 | 7.5 | |
| $t_{PLH}$ | A, B, or C | Y | 4.5 | 6 | 10.5 | 4 | 13.5 | 4 | 12 | ns |
| $t_{PHL}$ | | | 4 | 5.6 | 9 | 3.6 | 9.5 | 3.6 | 9 | |
| $t_{PLH}$ | $\overline{G}$ | W | 3 | 4.1 | 6.1 | 3 | 7.5 | 3 | 7 | ns |
| $t_{PHL}$ | | | 2.8 | 3.5 | 6 | 2.5 | 6.5 | 2.5 | 6 | |
| $t_{PLH}$ | $\overline{G}$ | Y | 4.4 | 5.3 | 9.5 | 3.8 | 12 | 3.8 | 10.5 | ns |
| $t_{PHL}$ | | | 3.5 | 4.5 | 7 | 3 | 8 | 3 | 7.5 | |
| $t_{PLH}$ | Data (any D) | W | 2.7 | 3.6 | 6.5 | 1.8 | 7.5 | 2.3 | 7 | ns |
| $t_{PHL}$ | | | 1.2 | 1.9 | 4 | 1 | 6 | 1 | 5 | |
| $t_{PLH}$ | Data (any D) | Y | 2.9 | 3.7 | 6.5 | 2.4 | 8.5 | 2.5 | 7.5 | ns |
| $t_{PHL}$ | | | 3.3 | 4.2 | 7 | 2.1 | 9 | 2.6 | 7.5 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

SDFS052A – D2932, MARCH 1987 – REVISED OCTOBER 1993

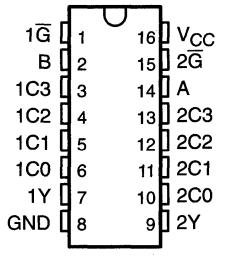
- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to N Lines)**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

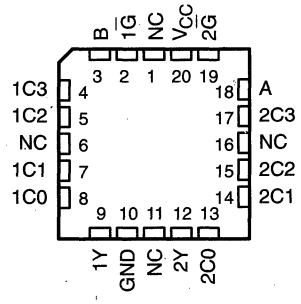
These data selectors/multiplexers contain inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe ($\overline{G}$) inputs are provided for each of the two 4-line sections.

The SN54F153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F153 is characterized for operation from 0°C to 70°C.

**SN54F153 . . . J PACKAGE**
**SN74F153 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F153 . . . FK PACKAGE**
**(TOP VIEW)**



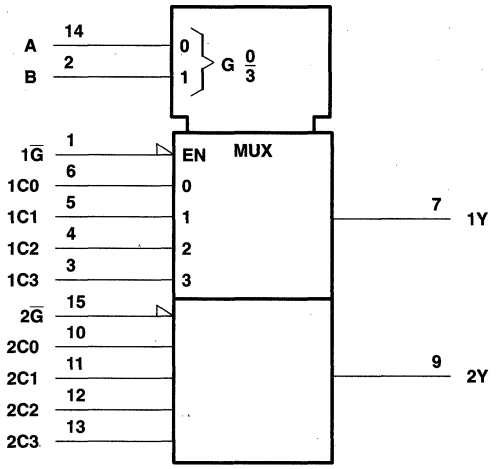

NC – No internal connection

**FUNCTION TABLE**

| INPUTS | | | | | | STROBE $\overline{G}$ | OUTPUT Y |
|---|---|---|---|---|---|---|---|
| SELECT | | DATA | | | | | |
| B | A | C0 | C1 | C2 | C3 | | |
| X | X | X | X | X | X | H | L |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

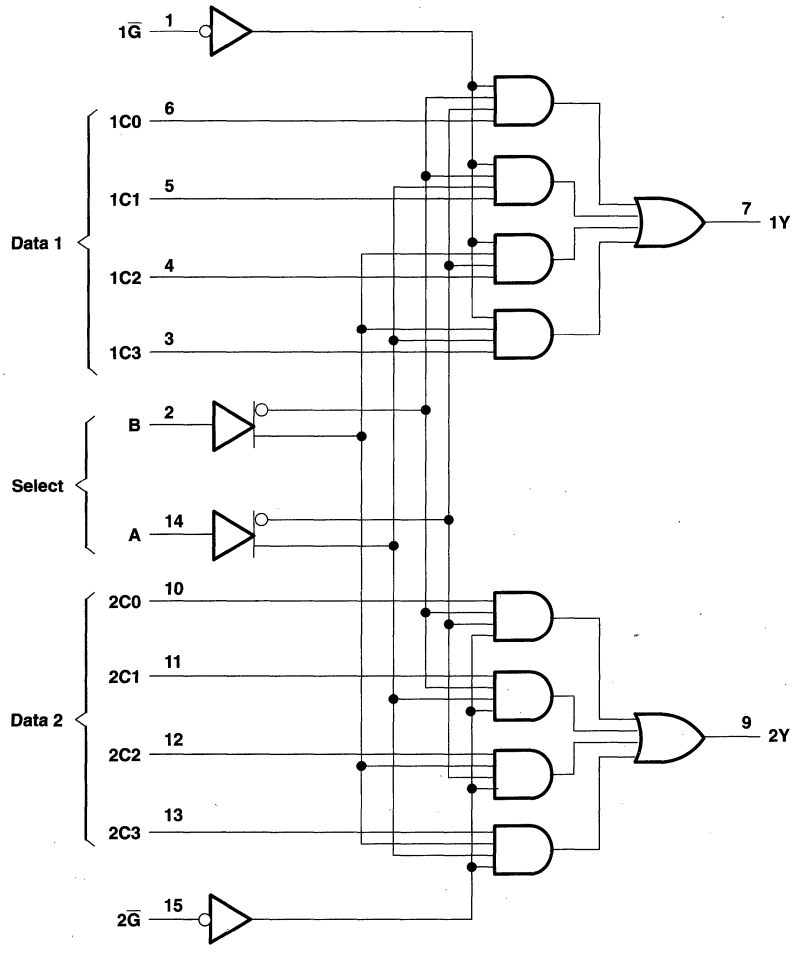
Select inputs A and B are common to both sections.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F153 ..... −55°C to 125°C
SN74F153 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage rating may be exceeded provided that the input current rating is observed.

## recommended operating conditions

| | | SN54F153 | | | SN74F153 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F153 | | | SN74F153 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 12 | 20 | | 12 | 20 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F153 | | | SN54F153 | | SN74F153 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 3.7 | 7.7 | 10.5 | 3.7 | 14 | 3.7 | 12 | ns |
| $t_{PHL}$ | | | 2.7 | 6.6 | 9 | 2.7 | 11 | 2.7 | 10.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | 3.7 | 6.7 | 9 | 3.7 | 11.5 | 3.7 | 10.5 | ns |
| $t_{PHL}$ | | | 2.2 | 5.3 | 7 | 1.7 | 9 | 1.7 | 8 | |
| $t_{PLH}$ | C | Y | 2.2 | 4.9 | 7 | 1.7 | 9 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 2.2 | 4.7 | 6.5 | 1.7 | 8 | 1.7 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SDFS053A – MARCH 1987 – REVISED OCTOBER 1993

- **Buffered Inputs and Outputs**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

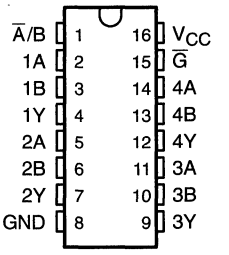
The 'F157A is a quadruple 2-input data selector/multiplexer featuring a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The 'F157A provides true data.

The SN54F157A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F157A is characterized for operation from 0°C to 70°C.

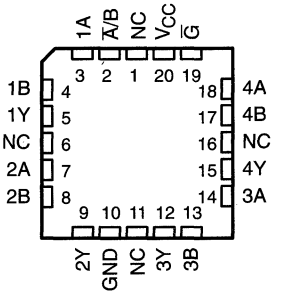
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | $\overline{A}$/B | A | B | Y |
| H | X | X | X | L |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

**SN54F157A . . . J PACKAGE**
**SN74F157A . . . D OR N PACKAGE**
**(TOP VIEW)**



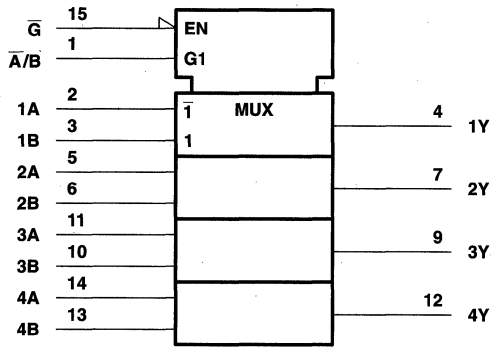

**SN54F157A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

SDFS053A – MARCH 1987 – REVISED OCTOBER 1993

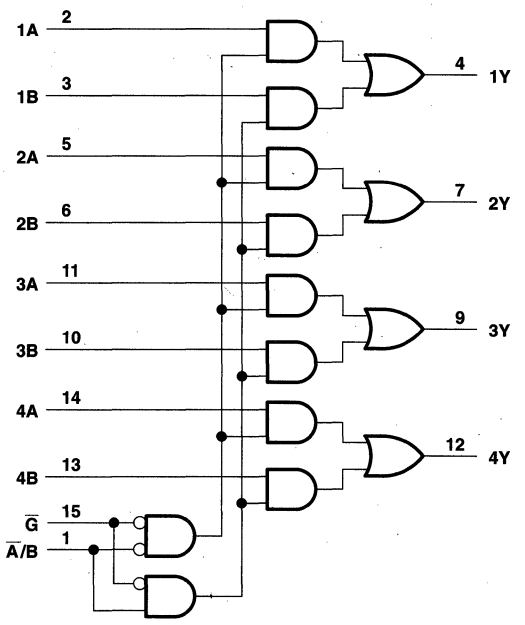
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F157A ..... −55°C to 125°C
SN74F157A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage rating may be exceeded provided that the input current rating is observed.

## recommended operating conditions

| | | SN54F157A | | | SN74F157A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F157A | | | SN74F157A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 15 | 23 | | 15.5 | 23 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F157A | | | SN54F157A | | SN74F157A | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | $\overline{A}$/B | Y | 3.2 | 6.6 | 10 | 3.2 | 12 | 3.2 | 11 | ns |
| $t_{PHL}$ | | | 2.2 | 4.6 | 7 | 2.2 | 9 | 2.2 | 8 | |
| $t_{PLH}$ | $\overline{G}$ | Y | 4.2 | 6.6 | 9.5 | 4.2 | 13 | 4.2 | 11 | ns |
| $t_{PHL}$ | | | 1.7 | 4.1 | 6.5 | 1.7 | 7.5 | 1.7 | 7 | |
| $t_{PLH}$ | A or B | Y | 1.7 | 4.1 | 6 | 1.7 | 7.5 | 1.7 | 6.5 | ns |
| $t_{PHL}$ | | | 1.7 | 3.6 | 5.5 | 1 | 7.5 | 1.2 | 7 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SDFS054A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Buffered Inputs and Outputs**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

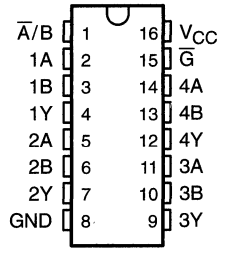
The 'F158A is a quadruple 2-input data selector/multiplexer featuring a direct strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The 'F158A provides inverted data.

The SN54F158A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F158A is characterized for operation from 0°C to 70°C.

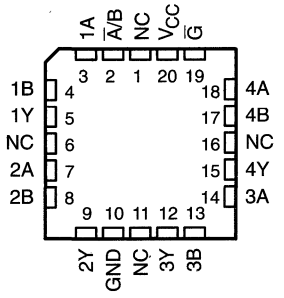
**FUNCTION TABLE**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{G}$ | $\overline{A}$/B | A | B | Y |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

**SN54F158A . . . J PACKAGE**
**SN74F158A . . . D OR N PACKAGE**
**(TOP VIEW)**

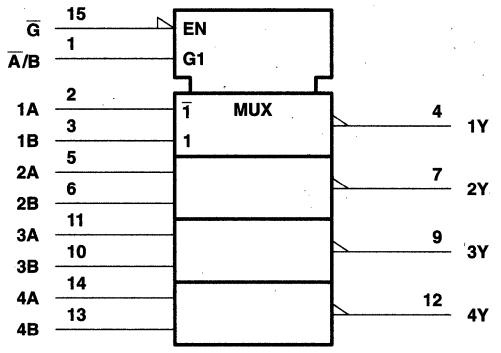



**SN54F158A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

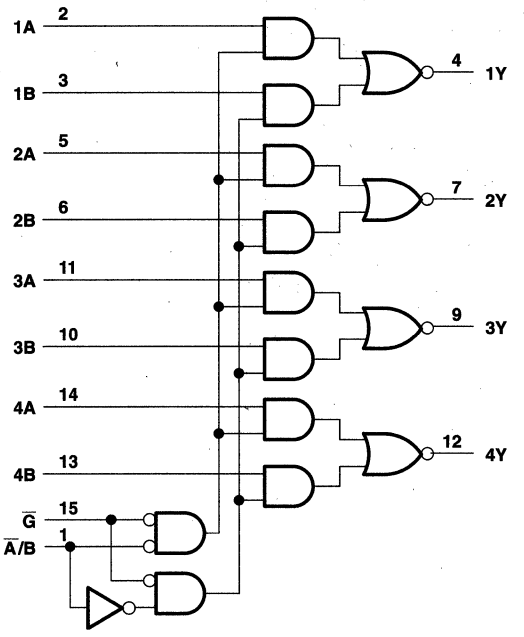
## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F158A ..... −55°C to 125°C
SN74F158A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage rating may be exceeded provided that the input current rating is observed.

## recommended operating conditions

| | | SN54F158A | | | SN74F158A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F158A | | | SN74F158A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 10 | 15 | | 10 | 15 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

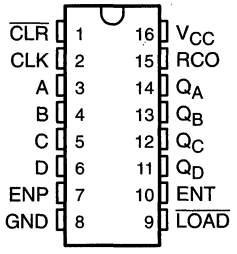
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F158A | | | SN54F158A | | SN74F158A | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | $\overline{A}$/B | Y | 2.2 | 5.1 | 8.5 | 2.2 | 10.5 | 2.2 | 9.5 | ns |
| $t_{PHL}$ | | | 1.7 | 4.1 | 6.5 | 1.7 | 8 | 1.7 | 7 | |
| $t_{PLH}$ | $\overline{G}$ | Y | 1.7 | 4.1 | 6 | 1.7 | 8 | 1.7 | 7 | ns |
| $t_{PHL}$ | | | 1.2 | 3.6 | 6 | 1.2 | 7 | 1.2 | 6.5 | |
| $t_{PLH}$ | A or B | Y | 1.7 | 3.6 | 5.9 | 1.7 | 8.5 | 1.7 | 7 | ns |
| $t_{PHL}$ | | | 1 | 2.1 | 4 | 1 | 5 | 1 | 4.5 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SDFS056A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

This synchronous, presettable, 4-bit binary counter features an internal carry look-ahead circuitry for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters; however, counting spikes may occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, it may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load ($\overline{\text{LOAD}}$) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the SN74F161A is asynchronous and a low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

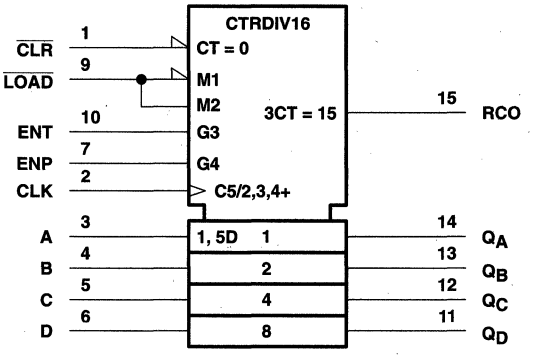
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (ENP, ENT) inputs and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT if fed forward to enable RCO. RCO thus enabled will produce a high-level pulse while the count is 15 (HHHH). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed regardless of the level of the clock input.

The SN74F161A features a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

The SN74F161A is characterized for operation from 0°C to 70°C.

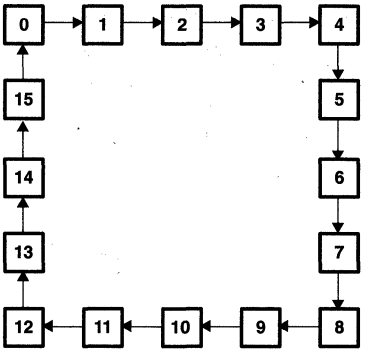
SDFS056A – D2932, MARCH 1987 – REVISED OCTOBER 1993

## logic symbol†

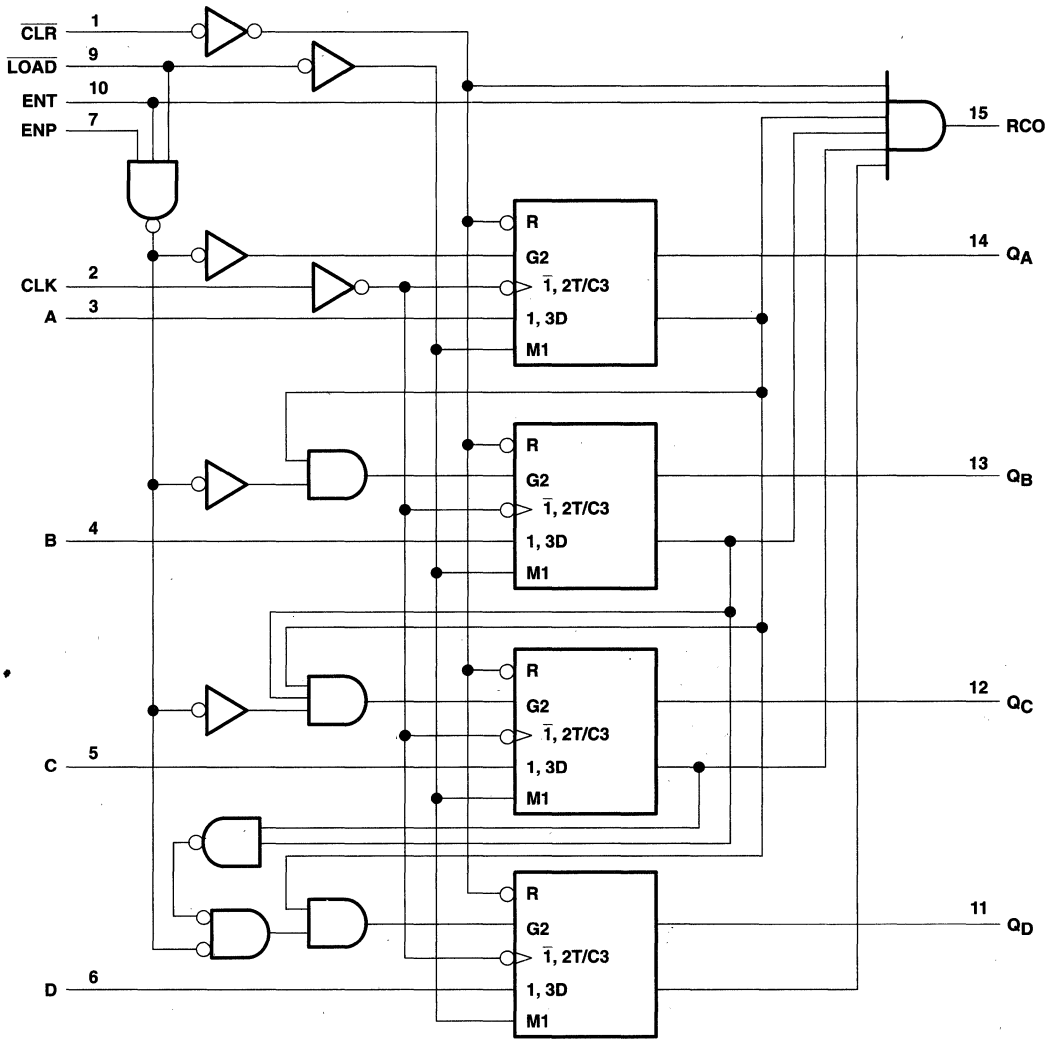



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

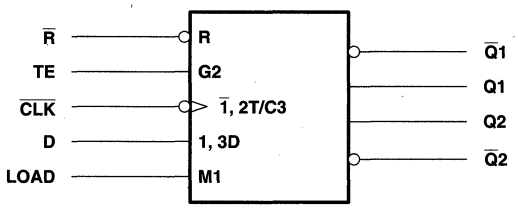
## state diagram



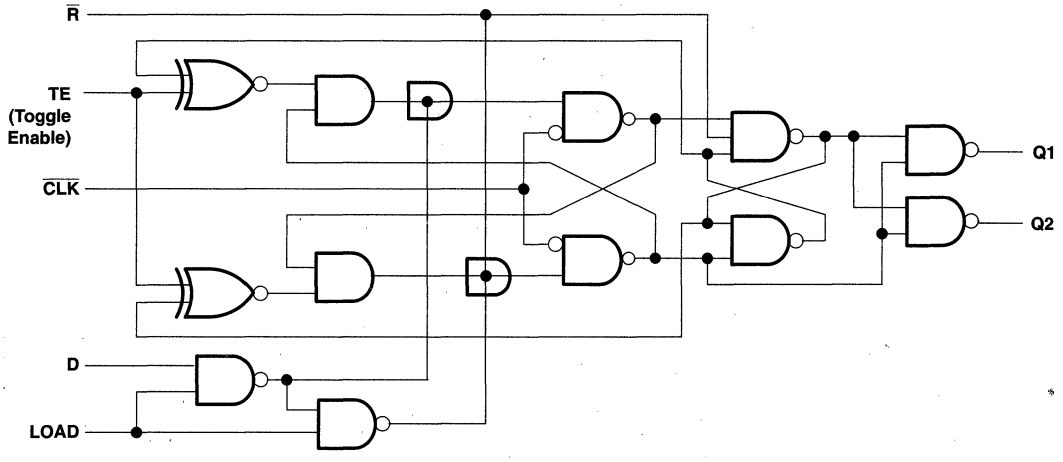
## logic diagram (positive logic)



## logic symbol, each flip-flop



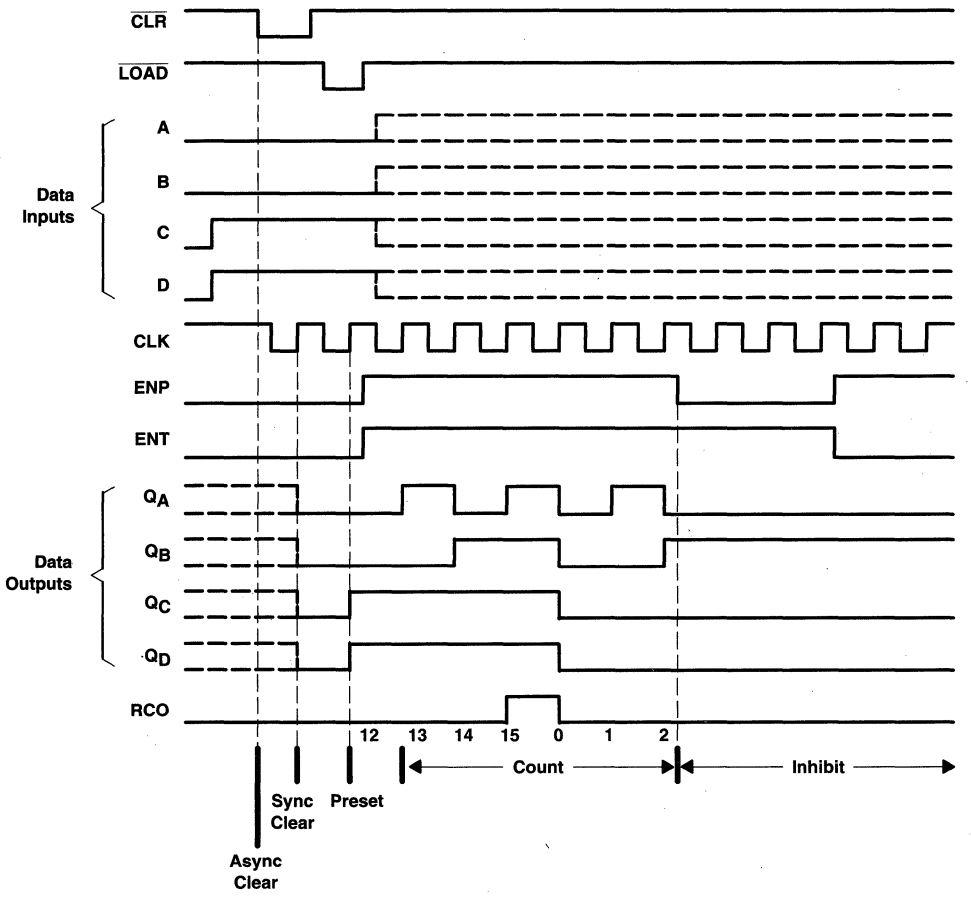

## logic diagram, each flip-flop (positive logic)



## typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | ENP, CLK, A, B, C, D | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | mA |
| | ENT, $\overline{LOAD}$ | | | | | −1.2 | |
| | $\overline{CLR}$ | | | | | −0.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 37 | 55 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 0 | 100 | 0 | 90 | MHz |
| $t_w$ | Pulse duration | CLK high or low (loading) | | 5 | | 5 | | ns |
| | | CLK (counting) | High | 4 | | 4 | | |
| | | | Low | 6 | | 7 | | |
| | | $\overline{CLR}$ low | | 5 | | 5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | High or low | 5 | | 5 | | ns |
| | | $\overline{LOAD}$ before CLK↑ | High | 11 | | 11.5 | | |
| | | | Low | 8.5 | | 9.5 | | |
| | | ENP and ENT before CLK↑ | High | 11 | | 11.5 | | |
| | | | Low | 5 | | 5 | | |
| $t_h$ | Hold time | Data after CLK↑ | High or low | 2 | | 2 | | ns |
| | | $\overline{LOAD}$ after CLK↑ | High | 2 | | 2 | | |
| | | | Low | 0 | | 0 | | |
| | | ENP and ENT after CLK↑ | High or low | 0 | | 0 | | |
| $t_{su}$ | Inactive-state setup time, $\overline{CLR}$ high before CLK↑† | | | 6 | | 6 | | ns |

† Inactive-state state setup time is also referred to as recovery time.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX‡ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 120 | | 90 | | MHz |
| $t_{PLH}$ | CLK ($\overline{LOAD}$ high) | Any Q | 2.7 | 5.1 | 7.5 | 2.7 | 8.5 | ns |
| $t_{PHL}$ | | | 2.7 | 7.1 | 10 | 2.7 | 11 | |
| $t_{PLH}$ | CLK ($\overline{LOAD}$ low) | Any Q | 3.2 | 5.6 | 8.5 | 3.2 | 9.5 | ns |
| $t_{PHL}$ | | | 3.2 | 5.6 | 8.5 | 3.2 | 9.5 | |
| $t_{PLH}$ | CLK | RCO | 4.2 | 9.6 | 14 | 4.2 | 15 | ns |
| $t_{PHL}$ | | | 4.2 | 9.6 | 14 | 4.2 | 15 | |
| $t_{PLH}$ | ENT | RCO | 1.7 | 4.1 | 7.5 | 1.7 | 8.5 | ns |
| $t_{PHL}$ | | | 1.7 | 4.1 | 7.5 | 1.7 | 8.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 4.7 | 8.6 | 12 | 4.7 | 13 | ns |
| | | RCO | 3.7 | 7.6 | 10.5 | 3.7 | 11.5 | |

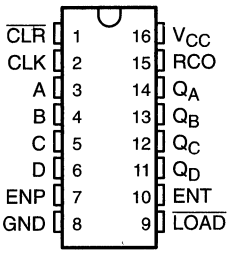
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

SDFS088 – MARCH 1987 – REVISED OCTOBER 1993

- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

This synchronous, presettable, 4-bit binary counter features an internal carry look-ahead circuitry for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters; however, counting spikes may occur on the ripple carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, it may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load ($\overline{\text{LOAD}}$) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the SN74F163A is synchronous and a low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of the clock regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

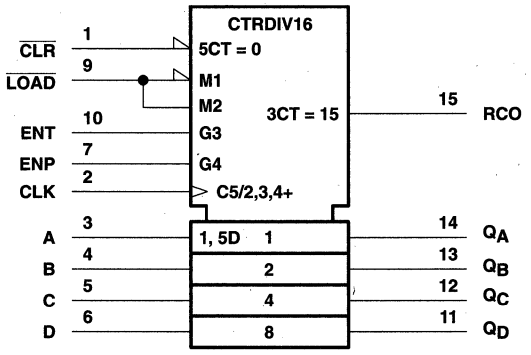
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (ENP, ENT) inputs and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT if fed forward to enable RCO. RCO thus enabled will produce a high-level pulse while the count is 15 (HHHH). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed regardless of the level of the clock input.

The SN74F163A features a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

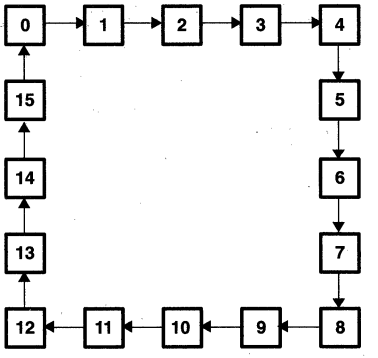
The SN74F163A is characterized for operation from 0°C to 70°C.

SDFS088 – MARCH 1987 – REVISED OCTOBER 1993

## logic symbol†

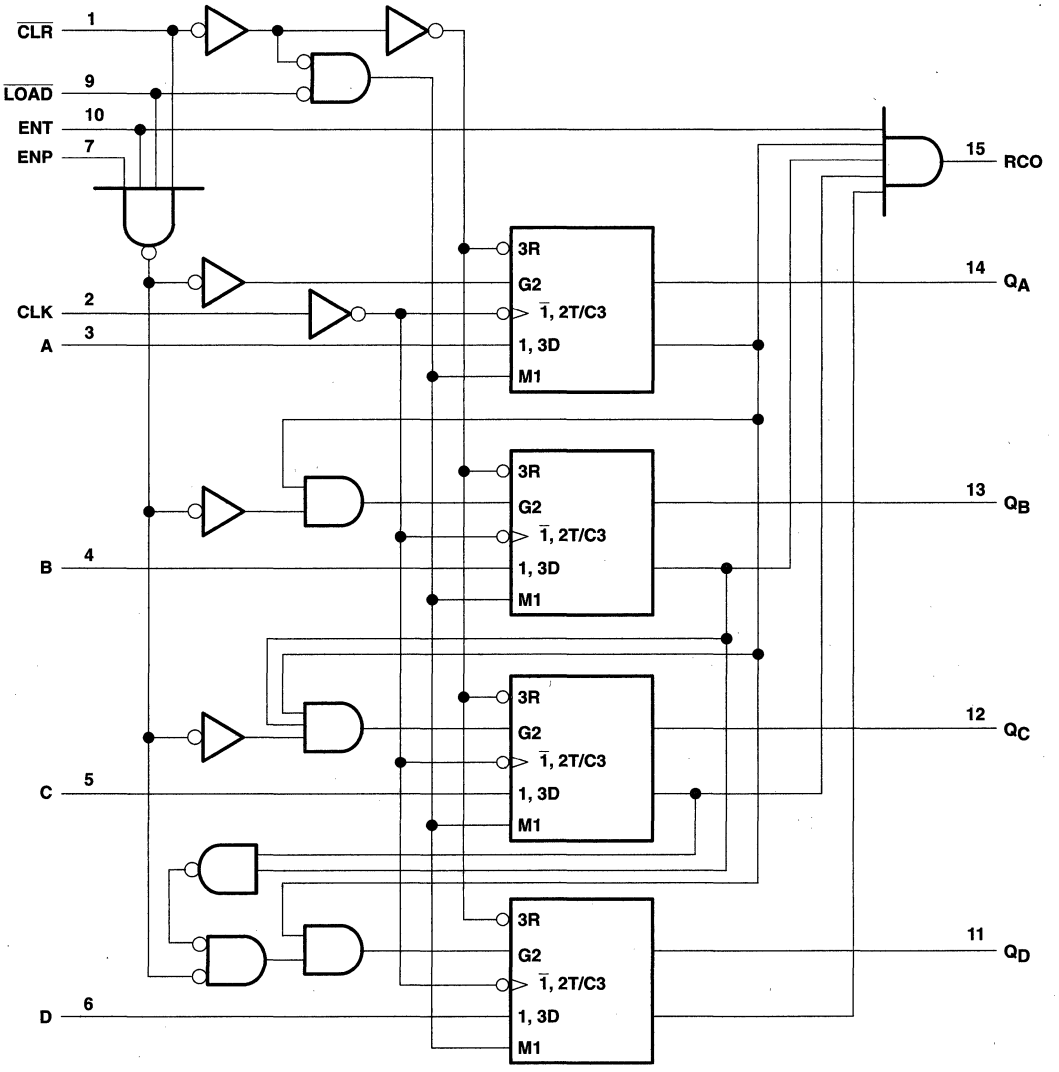



## state diagram

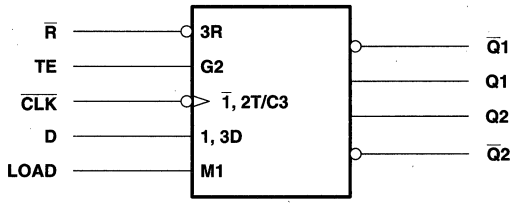



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

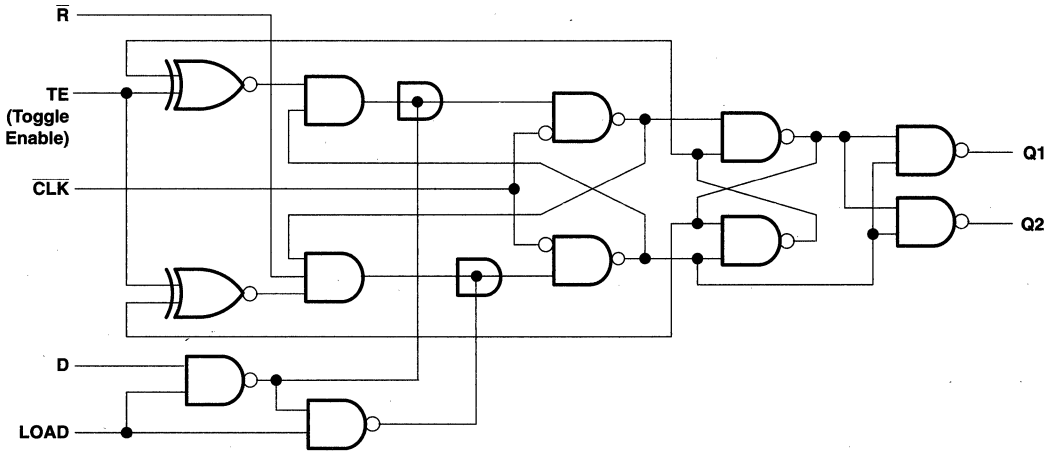
## logic diagram (positive logic)



## logic symbol, each flip-flop



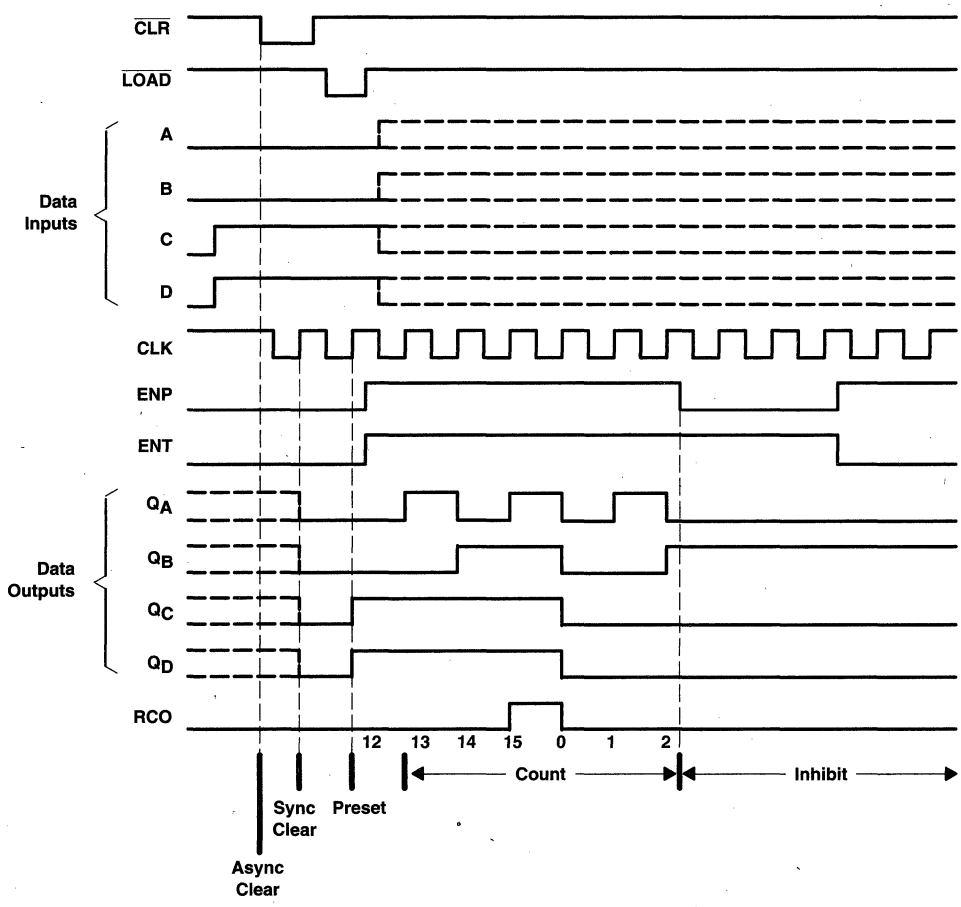

## logic diagram, each flip-flop (positive logic)



## typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | ENP, CLK, A, B, C, D | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | mA |
| | ENT, $\overline{LOAD}$ | | | | | −1.2 | |
| | $\overline{CLR}$ | | | | | −1.2 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 37 | 55 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 0 | 100 | 0 | 90 | MHz |
| $t_w$ | Pulse duration | CLK high or low (loading) | | 5 | | 5 | | ns |
| | | CLK (counting) | High | 4 | | 4 | | |
| | | | Low | 6 | | 7 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | High or low | 5 | | 5 | | ns |
| | | $\overline{LOAD}$ and $\overline{CLR}$ before CLK↑ | High | 11 | | 11.5 | | |
| | | | Low | 8.5 | | 9.5 | | |
| | | ENP and ENT before CLK↑ | High | 11 | | 11.5 | | |
| | | | Low | 5 | | 5 | | |
| $t_h$ | Hold time | Data after CLK↑ | High or low | 2 | | 2 | | ns |
| | | $\overline{LOAD}$ and $\overline{CLR}$ after CLK↑ | High | 2 | | 2 | | |
| | | | Low | 0 | | 0 | | |
| | | ENP and ENT after CLK↑ | High or low | 0 | | 0 | | |

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 120 | | 90 | | MHz |
| $t_{PLH}$ | CLK ($\overline{LOAD}$ high) | Any Q | 2.7 | 5.1 | 7.5 | 2.7 | 8.5 | ns |
| $t_{PHL}$ | | | 2.7 | 7.1 | 10 | 2.7 | 11 | |
| $t_{PLH}$ | CLK ($\overline{LOAD}$ low) | Any Q | 3.2 | 5.6 | 8.5 | 3.2 | 9.5 | ns |
| $t_{PHL}$ | | | 3.2 | 5.6 | 8.5 | 3.2 | 9.5 | |
| $t_{PLH}$ | CLK | RCO | 4.2 | 9.6 | 14 | 4.2 | 15 | ns |
| $t_{PHL}$ | | | 4.2 | 9.6 | 14 | 4.2 | 15 | |
| $t_{PLH}$ | ENT | RCO | 1.7 | 4.1 | 7.5 | 1.7 | 8.5 | ns |
| $t_{PHL}$ | | | 1.7 | 4.1 | 7.5 | 1.7 | 8.5 | |

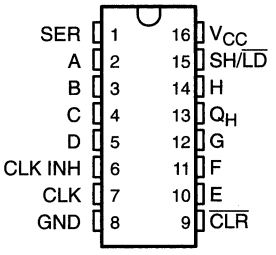
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

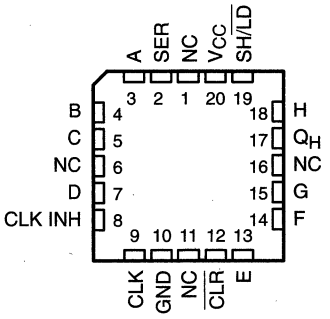
SDFS032A – D3213, JANUARY 1989 – REVISED OCTOBER 1993

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F166A . . . J PACKAGE**
**SN74F166A . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F166A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'F166A parallel-in or serial-in, serial-out registers feature gated clock (CLK INH and CLK) inputs and an overriding clear ($\overline{CLR}$) input. The parallel-in or serial-in modes are established by the shift/load (SH/$\overline{LD}$) input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive OR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only when the clock input is high. The direct clear ($\overline{CLR}$) overrides all other inputs, including the clock, and resets all flip-flops to zero.

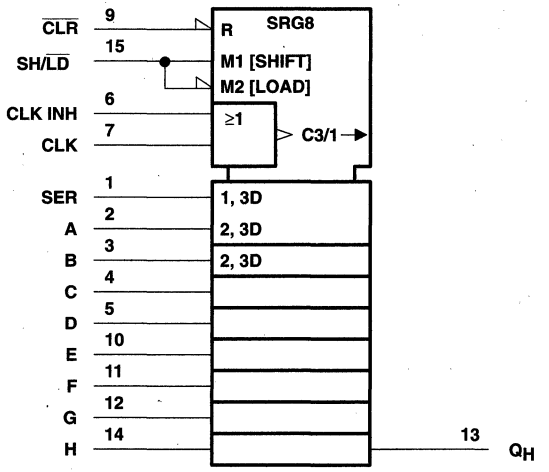
The SN54F166A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F166A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | | INTERNAL OUTPUTS | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | SH/$\overline{LD}$ | CLK INH | $\overline{CLR}$ | SER | PARALLEL A . . . H | $Q_A$ | $Q_B$ | $Q_H$ |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | L | ↑ | X | a . . . h | a | b | h |
| H | H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | X | H† | ↑ | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |

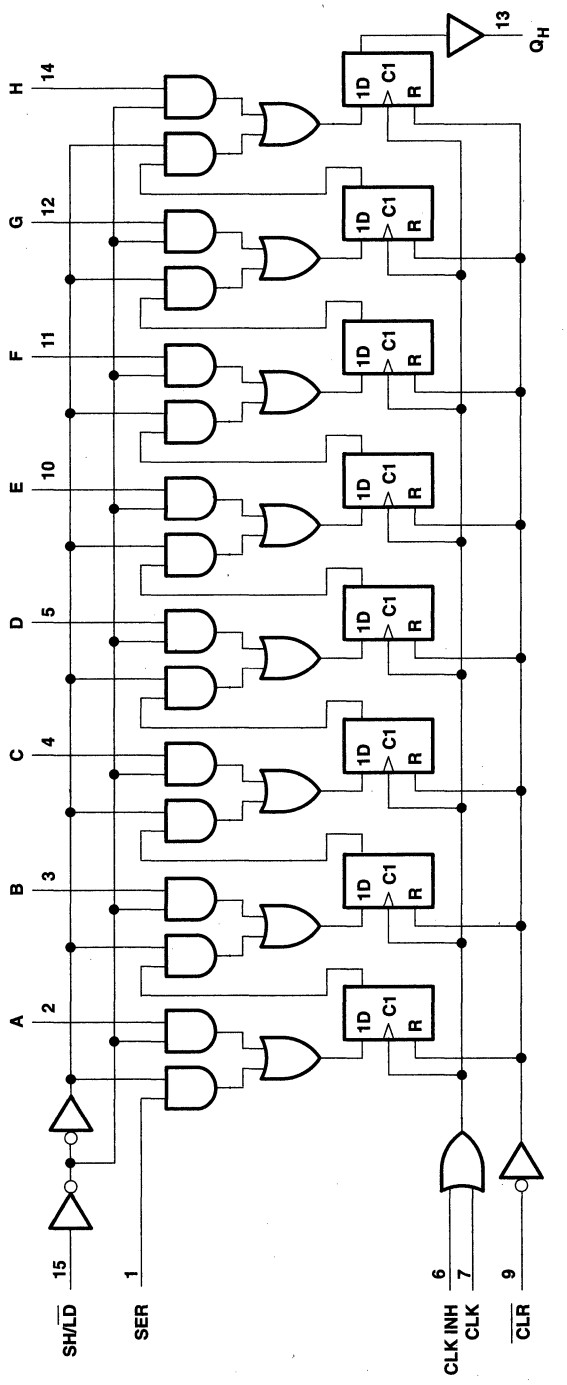
† The CLK INH input was taken to the high level in a prior configuration when CLK was high.

## logic symbol†



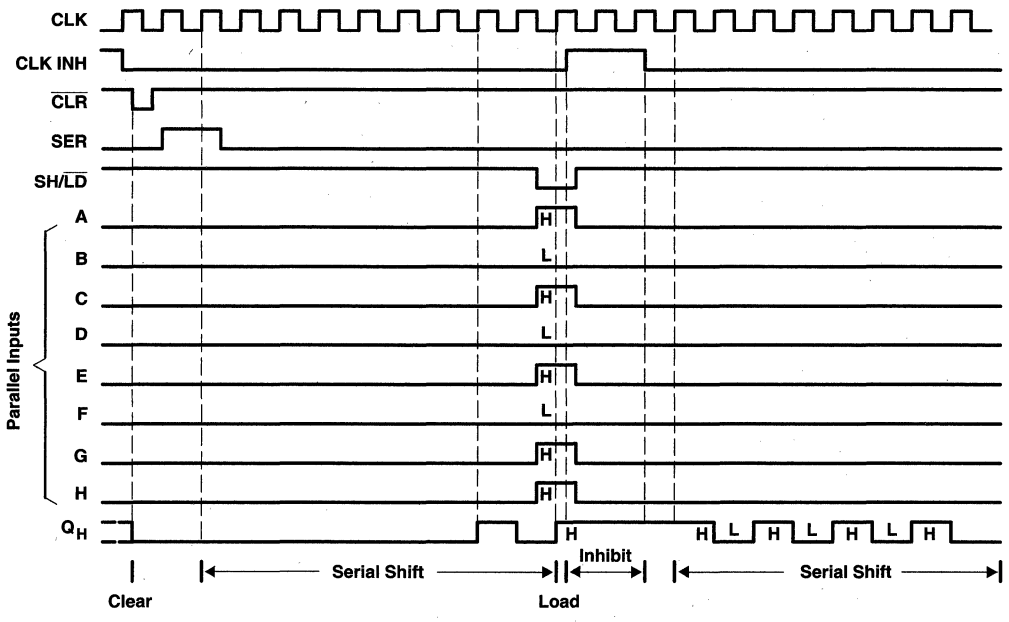

† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic symbol (positive logic)




Pin numbers shown are for the D, J, and N packages.

## typical clear, shift, load, inhibit, and shift operations




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... – 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... – 1.2 V to 7 V
Input current range ..... –30 mA to 5 mA
Voltage applied to any output in the high state, $V_O$ ..... – 0.5 V to $V_{CC}$
Current into any output in the low state, $I_O$ ..... 40 mA
Operating free-air temperature range: SN54F166A ..... – 55°C to 125°C
SN74F166A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions

| | | SN54F166A | | | SN74F166A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | – 18 | | | – 18 | mA |
| $I_{OH}$ | High-level output current | | | – 1 | | | – 1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | SN54F166A | | | SN74F166A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | | – 1.2 | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA | | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | | 0.35 | 0.5 | | 0.35 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | Control inputs | | | 40 | | | 40 | µA |
| | | | Others | | | 20 | | | 20 | |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | Control inputs | | | –40 | | | –40 | µA |
| | | | Others | | | –20 | | | –20 | |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | – 60 | | – 150 | – 60 | | – 150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | | | | 43 | 70 | | 43 | 70 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing characteristics

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 'F166A | | SN54F166A | | SN74F166A | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 135 | | | 0 | 110 | MHz |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 4 | | 4 | | 4 | | ns |
| | | CLK high | 4 | | 4 | | 4 | | |
| | | CLK low | 4 | | 4 | | 4 | | |
| $t_{su}$ | Setup time before CLK↑ | SH/$\overline{LD}$ high | 2.5 | | 2.5 | | 2.5 | | ns |
| | | SER | 3.5 | | 3.5 | | 3.5 | | |
| | | CLK INH low | 2.5 | | 2.5 | | 2.5 | | |
| | | A . . . H | 4 | | 4 | | 4 | | |
| | | $\overline{CLR}$ high | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ | Hold time after CLK↑ | SH/$\overline{LD}$ high | 1 | | 1 | | 1 | | ns |
| | | SER | 1.5 | | 1.5 | | 1.5 | | |
| | | CLK INH low | 1.5 | | 1.5 | | 1.5 | | |
| | | A . . . H | 1 | | 1 | | 1 | | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics (see Figure 1)

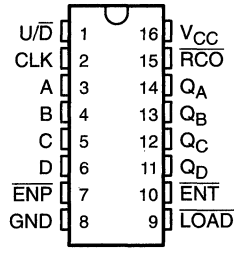
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C† | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F166A | | | SN54F166A | | SN74F166A | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 135 | 175 | | | | 110 | | MHz |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | 4.8 | 6 | 7.1 | 4.2 | 13.4 | 4.4 | 8.3 | ns |
| $t_{PLH}$ | CLK | $Q_H$ | 4.6 | 5.9 | 7.1 | 4 | 9.4 | 4.2 | 8.2 | ns |
| $t_{PHL}$ | | | 4.6 | 5.8 | 6.9 | 3.9 | 9.4 | 4.1 | 8 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Load circuits and waveforms are shown in Section 1.

SDFS057A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

This synchronous, presettable, 4-bit up/down decade counter features an internal carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

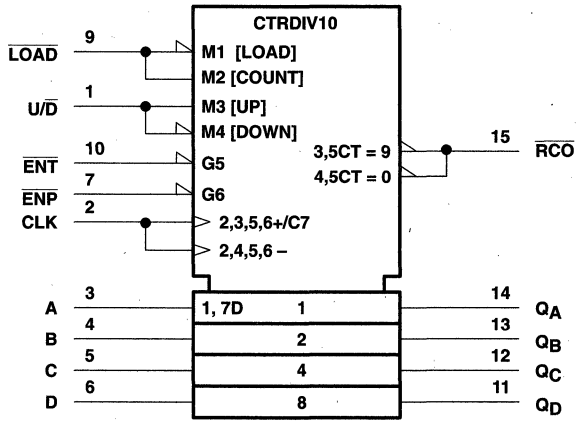
This counter is fully programmable; that is, it may be preset to any number between 0 and its maximum count. The load-input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and a ripple-carry ($\overline{RCO}$) output. Both $\overline{ENP}$ and $\overline{ENT}$ must be low to count. The direction of the count is determined by the level of the up/down (U/$\overline{D}$) input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the $\overline{RCO}$. $\overline{RCO}$ thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

The SN74F168 features a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$ or U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

The SN74F168 is characterized for operation from 0°C to 70°C.

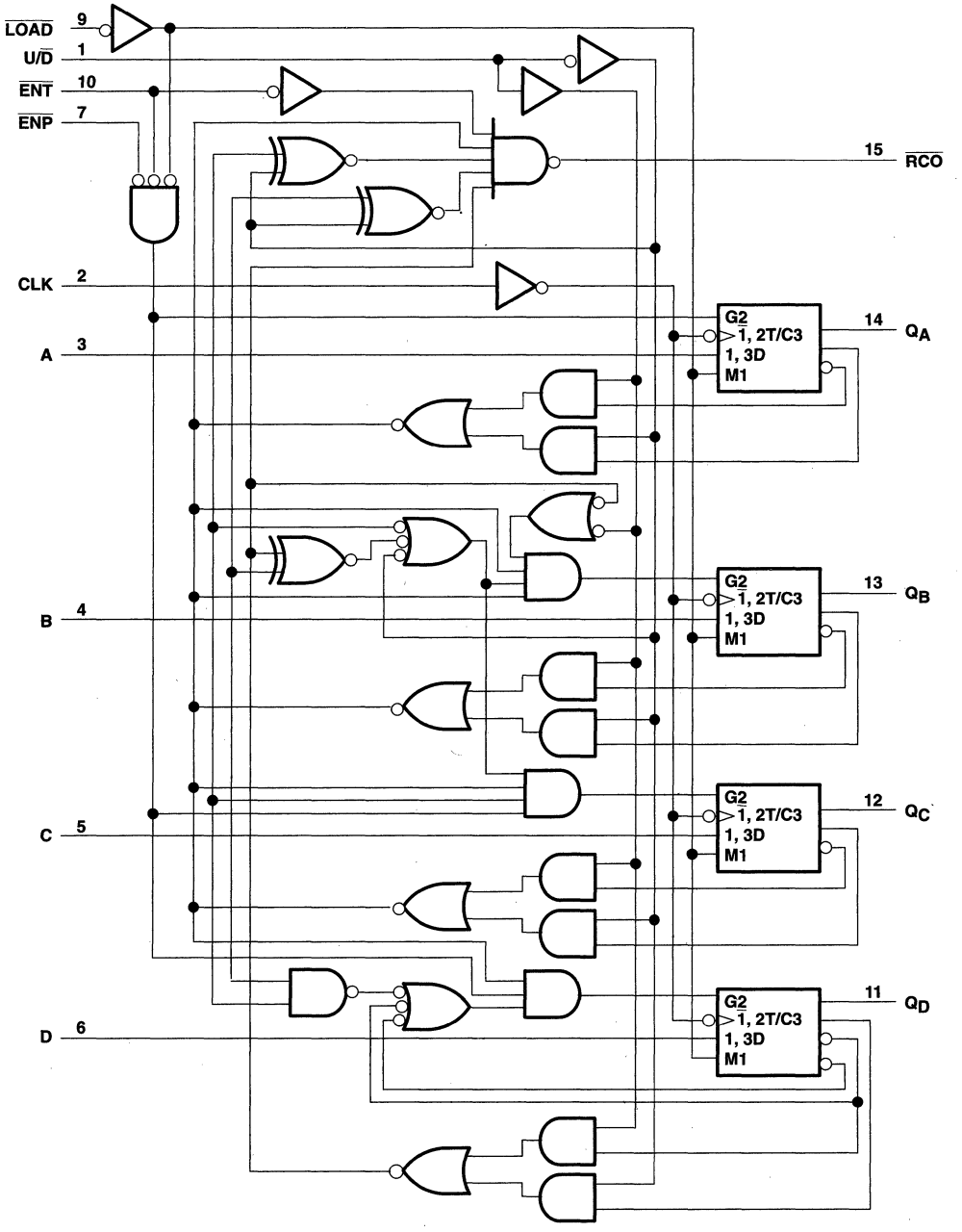
## logic symbol†



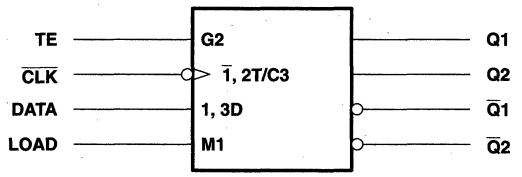

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SDFS057A – D2932, MARCH 1987 – REVISED OCTOBER 1993

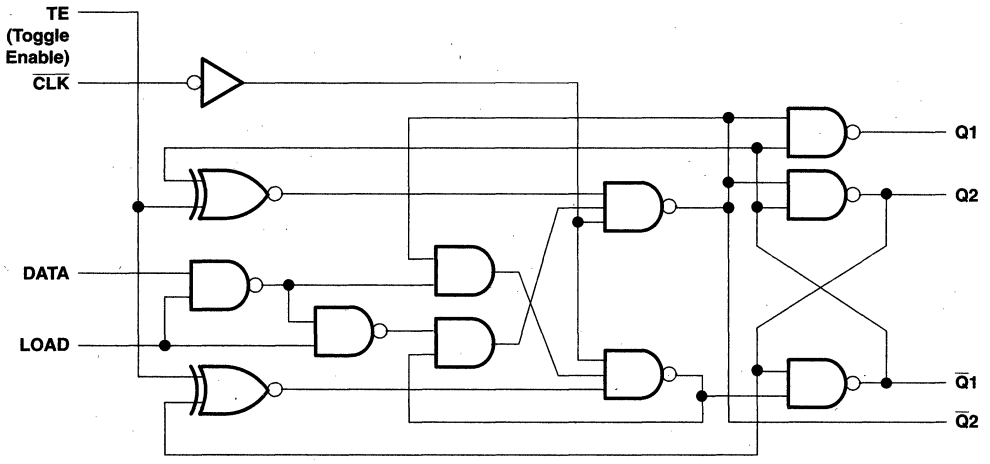
## logic diagram (positive logic)



## logic symbol, each flip-flop




## logic diagram, each flip-flop (positive logic)



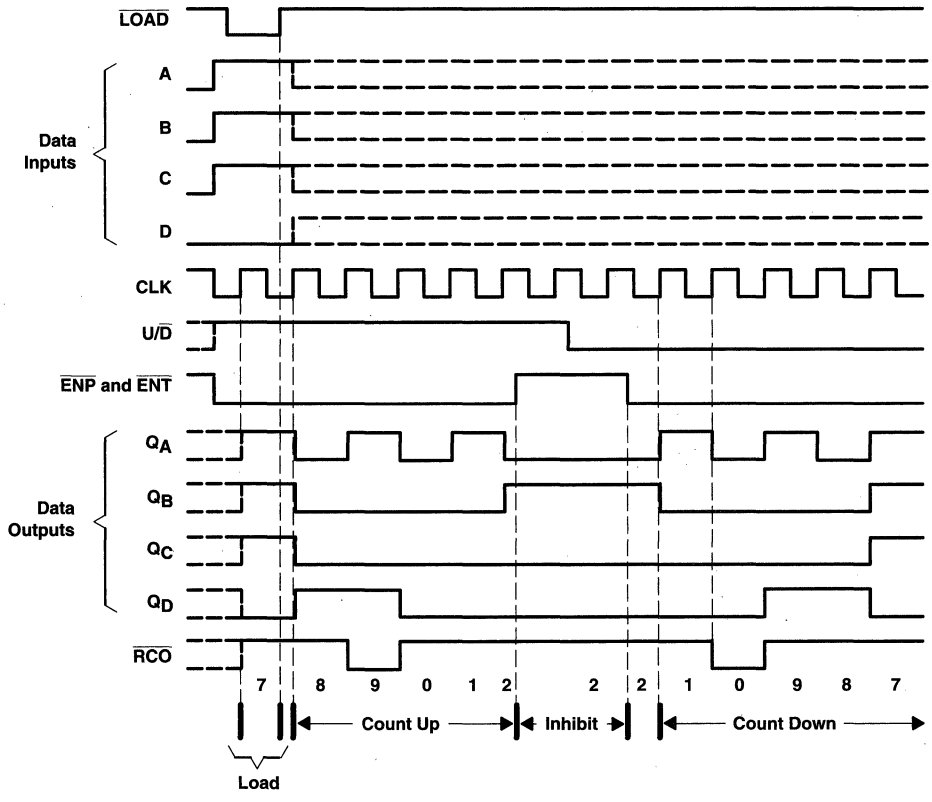

**FUNCTION TABLE**
**(each flip-flop)**

| COUNTER INPUTS | | FLIP-FLOP INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| $\overline{LOAD}$ | CLK | LOAD | TE | $\overline{CLK}$ | DATA | Q | $\overline{Q}$ |
| L | ↑ | H | L | ↓ | H | H | L |
| L | ↑ | H | L | ↓ | L | L | H |
| H | ↑ | L | H | ↓ | X | $\overline{Q}_0$ | $Q_0$ |
| H | ↑ | L | L | ↓ | X | $Q_0$ | $\overline{Q}_0$ |

## typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $\overline{ENT}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1.2 | mA |
| | All others | | | | | −0.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 38 | 52 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with B and $\overline{ENT}$ inputs high and all other inputs low.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 0 | 100 | 0 | 90 | MHz |
| $t_w$ | Pulse duration | CLK high or low | | 5 | | 5.5 | | ns |
| $t_{su}$ | Setup time | Data before CLK↑ | High or low | 4 | | 4.5 | | ns |
| | | $\overline{LOAD}$ before CLK↑ | High or low | 8 | | 9 | | |
| | | $\overline{ENP}$ and $\overline{ENT}$ before CLK↑ | High or low | 5 | | 6 | | |
| | | U/$\overline{D}$ before CLK↑ | High | 11 | | 12.5 | | |
| | | | Low | 16.5 | | 18 | | |
| $t_h$ | Hold time | Data after CLK↑ | High or low | 3 | | 3.5 | | ns |
| | | $\overline{LOAD}$ after CLK↑ | High or low | 0 | | 0 | | |
| | | $\overline{ENP}$ and $\overline{ENT}$ after CLK↑ | High or low | 0 | | 0 | | |
| | | U/$\overline{D}$ after CLK↑ | High or low | 0 | | 0 | | |

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 115 | | 90 | | MHz |
| $t_{PLH}$ | CLK | Q | 2.2 | 6.1 | 8.5 | 2.2 | 9.5 | ns |
| $t_{PHL}$ | | | 3.2 | 8.6 | 11.5 | 3.2 | 13 | |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 4.7 | 11.6 | 15.5 | 4.7 | 17 | ns |
| $t_{PHL}$ | | | 3.2 | 8.1 | 11 | 3.2 | 12.5 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 1.7 | 4.1 | 6 | 1.7 | 7 | ns |
| $t_{PHL}$ | | | 1.7 | 5.6 | 8 | 1.7 | 9 | |
| $t_{PLH}$ | U/$\overline{D}$ | $\overline{RCO}$ | 2.7 | 8.1 | 11 | 2.7 | 12.5 | ns |
| $t_{PHL}$ | | | 3.2 | 12.1 | 16 | 3.2 | 17.5 | |

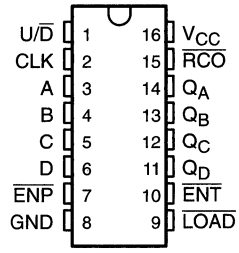
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

# SN74F169
# SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER

SDFS089 – MARCH 1987 – REVISED OCTOBER 1993

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

This synchronous, presettable, 4-bit up/down binary counter features an internal carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

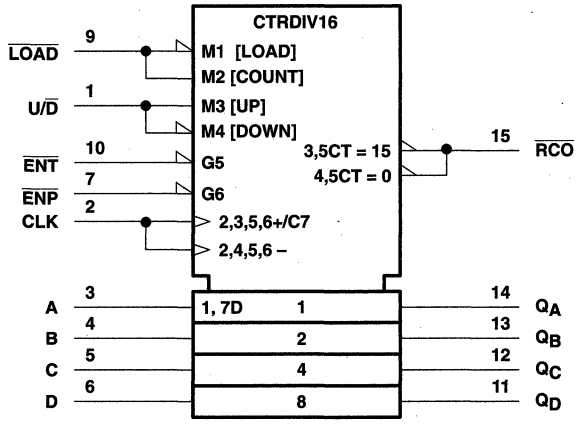
This counter is fully programmable; that is, it may be preset to any number between 0 and its maximum count. The load-input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and a ripple-carry ($\overline{RCO}$) output. Both $\overline{ENP}$ and $\overline{ENT}$ must be low to count. The direction of the count is determined by the level of the up/down (U/$\overline{D}$) input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the $\overline{RCO}$. $\overline{RCO}$ thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

The SN74F169 features a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$ or U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

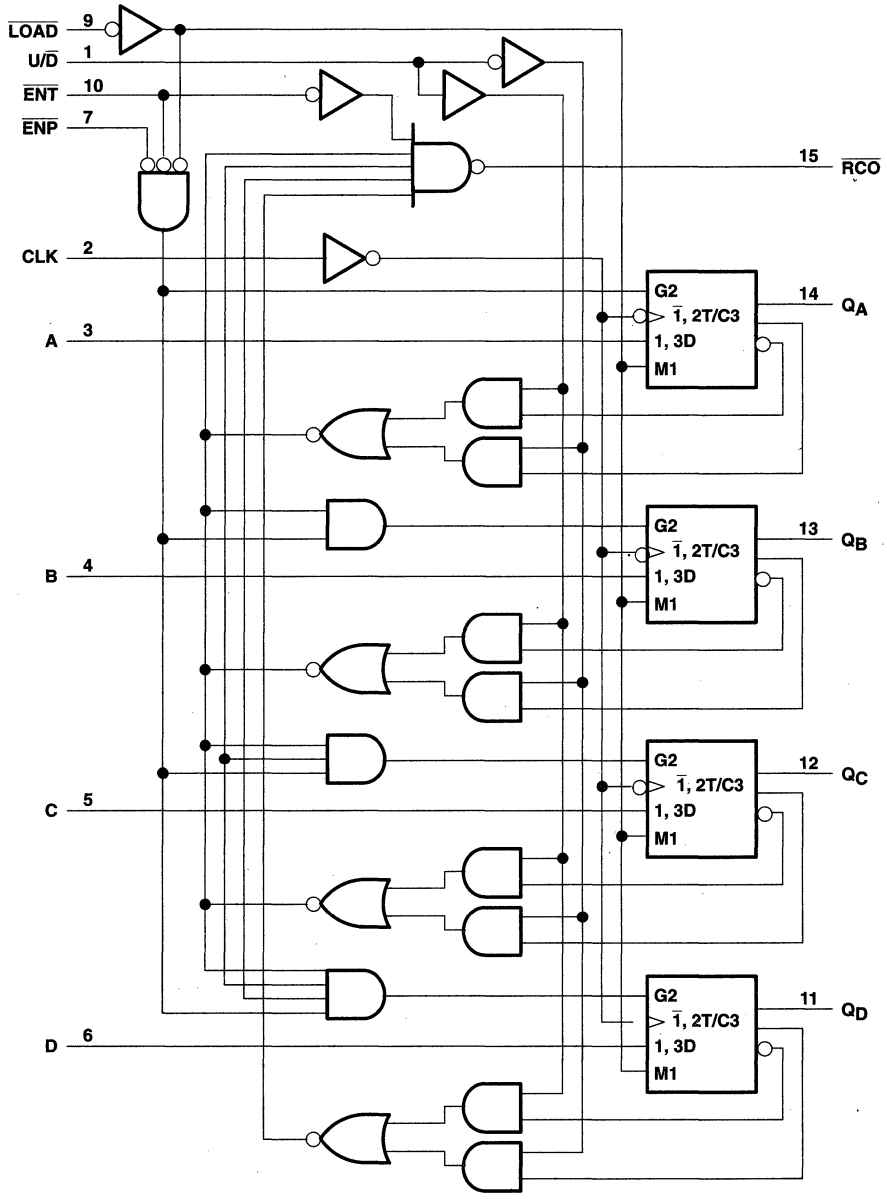
The SN74F169 is characterized for operation from 0°C to 70°C.

## logic symbol†

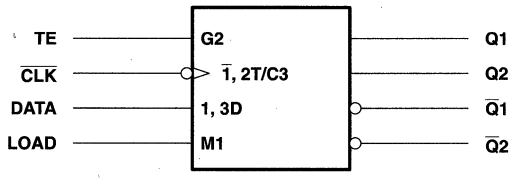



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

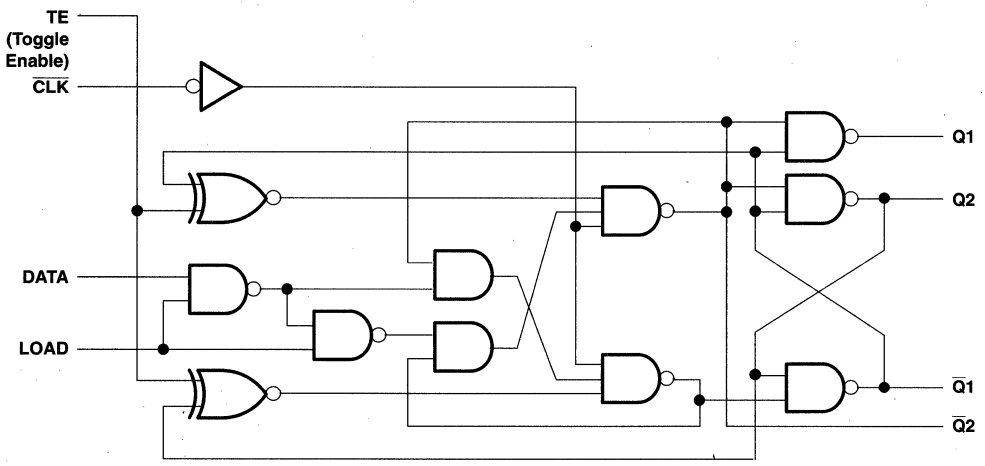
## logic diagram (positive logic)



## logic symbol, each flip-flop




## logic diagram, each flip-flop (positive logic)



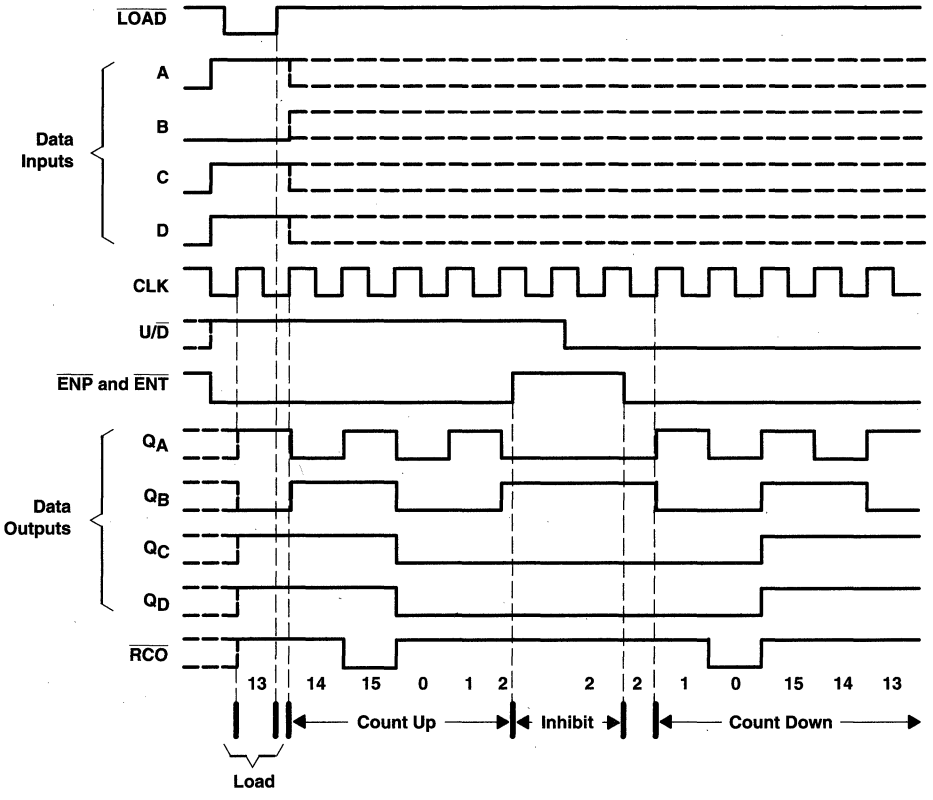

**FUNCTION TABLE**
**(each flip-flop)**

| COUNTER INPUTS | | FLIP-FLOP INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| $\overline{\text{LOAD}}$ | CLK | LOAD | TE | $\overline{\text{CLK}}$ | DATA | Q | $\overline{\text{Q}}$ |
| L | ↑ | H | L | ↓ | H | H | L |
| L | ↑ | H | L | ↓ | L | L | H |
| H | ↑ | L | H | ↓ | X | $\overline{Q}_0$ | $Q_0$ |
| H | ↑ | L | L | ↓ | X | $Q_0$ | $\overline{Q}_0$ |

## typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $\overline{ENT}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1.2 | mA |
| | All others | | | | | −0.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 38 | 52 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured after applying a momentary 4.5 V, then ground, to the clock input with B and $\overline{ENT}$ inputs high and all other inputs low.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 0 | 100 | 0 | 90 | MHz |
| $t_w$ | Pulse duration | CLK high or low | | 5 | | 5.5 | | ns |
| $t_{su}$ | Setup time | Data before CLK↑ | High or low | 4 | | 4.5 | | ns |
| | | $\overline{LOAD}$ before CLK↑ | High or low | 8 | | 9 | | |
| | | $\overline{ENP}$ and $\overline{ENT}$ before CLK↑ | High or low | 5 | | 6 | | |
| | | U/$\overline{D}$ before CLK↑ | High | 11 | | 12.5 | | |
| | | | Low | 7 | | 8 | | |
| $t_h$ | Hold time | Data after CLK↑ | High or low | 3 | | 3.5 | | ns |
| | | $\overline{LOAD}$ after CLK↑ | High or low | 0 | | 0 | | |
| | | $\overline{ENP}$ and $\overline{ENT}$ after CLK↑ | High or low | 0 | | 0 | | |
| | | U/$\overline{D}$ after CLK↑ | High or low | 0 | | 0 | | |

## switching characteristics (see Note 3)

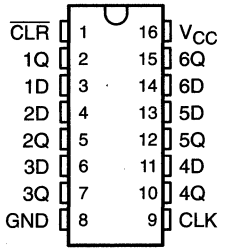
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 115 | | 90 | | MHz |
| $t_{PLH}$ | CLK | Q | 2.2 | 6.1 | 8.5 | 2.2 | 9.5 | ns |
| $t_{PHL}$ | | | 3.2 | 8.6 | 11.5 | 3.2 | 13 | |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 4.7 | 11.6 | 15.5 | 4.7 | 17 | ns |
| $t_{PHL}$ | | | 3.2 | 8.1 | 11 | 3.2 | 12.5 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 1.7 | 4.1 | 6 | 1.7 | 7 | ns |
| $t_{PHL}$ | | | 1.7 | 5.6 | 8 | 1.7 | 9 | |
| $t_{PLH}$ | U/$\overline{D}$ | $\overline{RCO}$ | 2.7 | 8.1 | 11 | 2.7 | 12.5 | ns |
| $t_{PHL}$ | | | 3.2 | 7.6 | 10.5 | 3.2 | 12 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Contains Six Flip-Flops With Single-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  **Buffer/Storage Registers**
  **Shift Registers**
  **Pattern Generators**
- **Fully Buffered Outputs for Maximum Isolation From External Disturbances**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

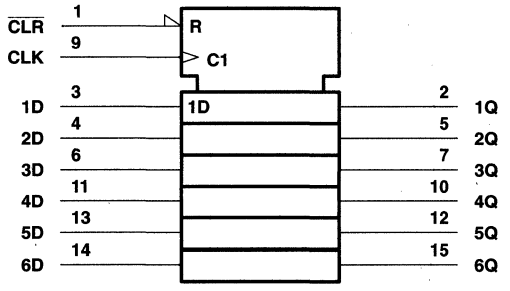
This monolithic, positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74F174A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

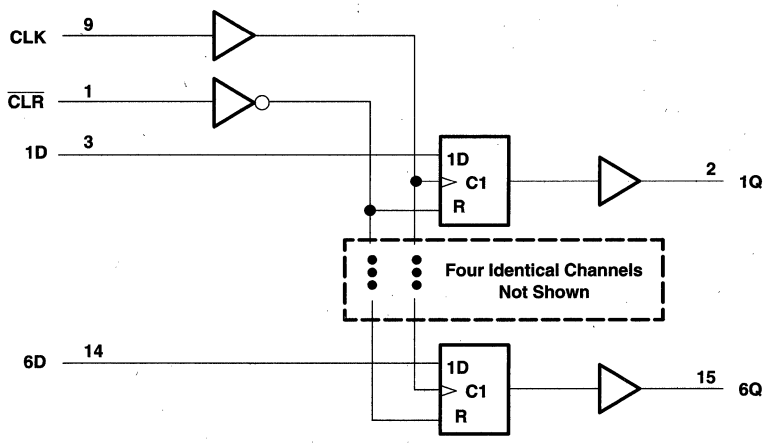
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q |
| H | L | X | $Q_0$ |
| H | ↑ | H | H |
| H | ↑ | L | L |
| L | X | X | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage applied to any output in the high state . . . . . −0.5 V to $V_{CC}$
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | – 60 | | – 150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 30 | 45 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | See Note 3 | | 39 | 55 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTES: 2. $I_{CCH}$ is measured with all outputs open, all data inputs and enable input at 4.5 V, and the clock input at 4.5 V after being momentarily grounded.
3. $I_{CCL}$ is measured with all outputs open, all data inputs and enable input at 0 V, and the clock input at 4.5 V after being momentarily grounded.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 80 | MHz |
| $t_w$ | Pulse duration | CLK high | 4 | | 4 | | ns |
| | | CLK low | 6 | | 6 | | |
| | | $\overline{CLR}$ low | 5 | | 5 | | |
| $t_{su}$ | Setup time before CLK↑ | Data high or low | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ high¶ | 5 | | 5 | | |
| $t_h$ | Hold time after CLK↑ | Data high or low | 0.5 | | 1 | | ns |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
¶ Inactive-state setup time is also referred to as recovery time.

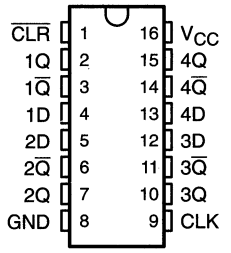
## switching characteristics (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 140 | | 80 | | MHz |
| $t_{PLH}$ | CLK | Any Q | 2.7 | 4.5 | 8 | 2.7 | 9 | ns |
| $t_{PHL}$ | | | 3.4 | 4.2 | 10 | 3.3 | 11 | |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 4.2 | 6.3 | 14 | 4.2 | 15 | ns |

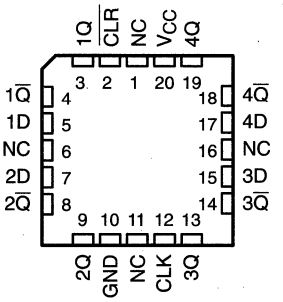
NOTE 4: Load circuits and waveforms are shown in Section 1.

- **Contain Four Flip-Flops With Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  **Buffer/Storage Registers**
  **Shift Registers**
  **Pattern Generators**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F175 . . . J PACKAGE**
**SN74F175 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F175 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

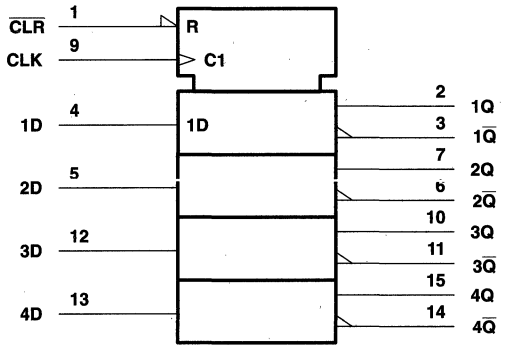
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting setup time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54F175 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F175 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

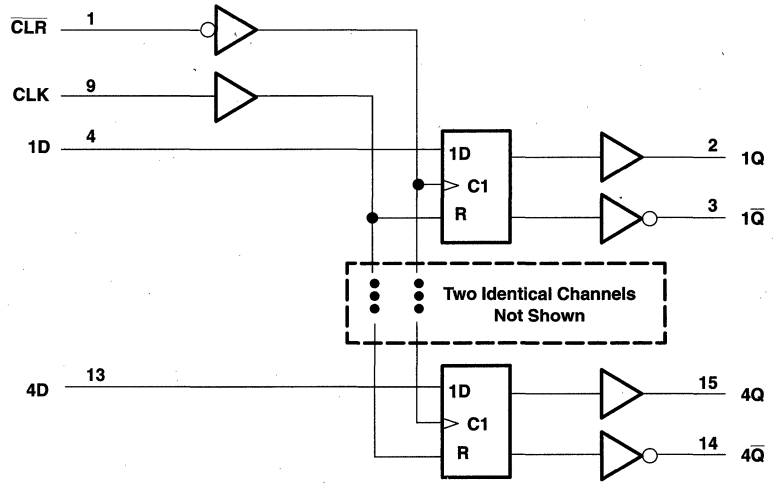
| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . −0.5 V to $V_{CC}$
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F175 . . . . . −55°C to 125°C
SN74F175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F175 | | | SN74F175 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F175 | | | SN74F175 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 22.5 | 34 | | 22.5 | 34 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured with outputs open with 4.5 V applied to all data inputs after a momentary ground followed by 4.5 V applied to CLK.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C 'F175 | | SN54F175 | | SN74F175 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLK high | 4 | | 4 | | 4 | | ns |
| | | CLK low | 5 | | 5 | | 5 | | |
| | | $\overline{CLR}$ low | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time, data before CLK↑ | High or low | 3 | | 3 | | 3 | | ns |
| | Setup time, inactive state, data before CLK↑† | $\overline{CLR}$ high | 5 | | 5 | | 5 | | |
| $t_h$ | Hold time, data after CLK↑ | High or low | 1 | | 1 | | 1 | | ns |

† Inactive-state setup time is also referred to as recovery time.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C 'F175 | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX‡ SN54F175 | | SN74F175 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | 140 | | 100 | | 100 | | MHz |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 3.2 | 4.6 | 6.5 | 2.7 | 8.5 | 3.2 | 7.5 | ns |
| $t_{PHL}$ | | | 3.2 | 6.1 | 8.5 | 3.2 | 10.5 | 3.2 | 9.5 | |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{Q}$ | 3.2 | 6.1 | 8.5 | 3.2 | 10 | 3.2 | 9 | ns |
| $t_{PHL}$ | | Q | 3.7 | 8.6 | 11.5 | 3.7 | 15 | 3.7 | 13 | |

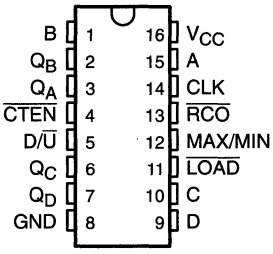
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

# SN74F190A
# SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTER WITH RESET AND RIPPLE CLOCK

SDFS026B – D3690, JULY 1990 – REVISED OCTOBER 1993

- **High-Speed $f_{max}$ of 125 MHz Typical**
- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

The SN74F190A is a synchronous, 4-bit decade reversible up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

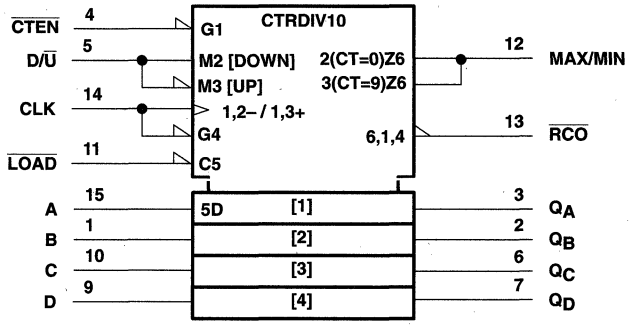
The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the enable ($\overline{CTEN}$) input is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up, and when D/$\overline{U}$ is high, it counts down.

This counter features a fully independent clock circuit. Changes at the control ($\overline{CTEN}$ and D/$\overline{U}$) inputs that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times. This counter is fully programmable; that is, it may be preset to any number between 0 and 9 by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independent of the level of the clock input. This feature allows the counter to be used as a modulo-N divider by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is minimum (0) counting down or maximum (9) counting up. The ripple-clock ($\overline{RCO}$) output produces a low-level output pulse under those same conditions, but only while the clock input is low. The counter can easily be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used or to the clock input if parallel enabling is used. The maximum/minimum count (MAX/MIN) output can be used to accomplish look-ahead for high speed operation.

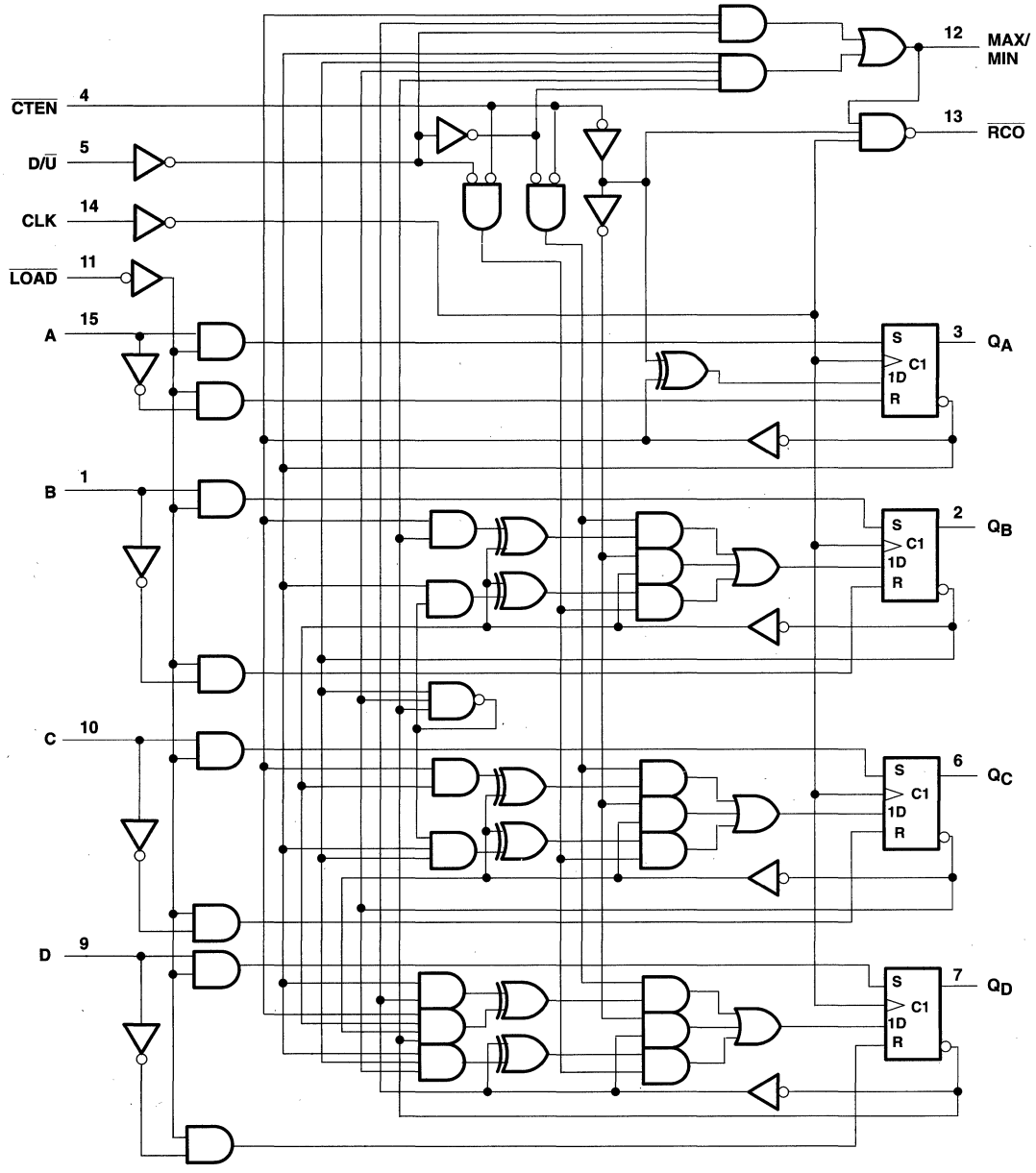
The SN74F190A is characterized for operation from 0°C to 70°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

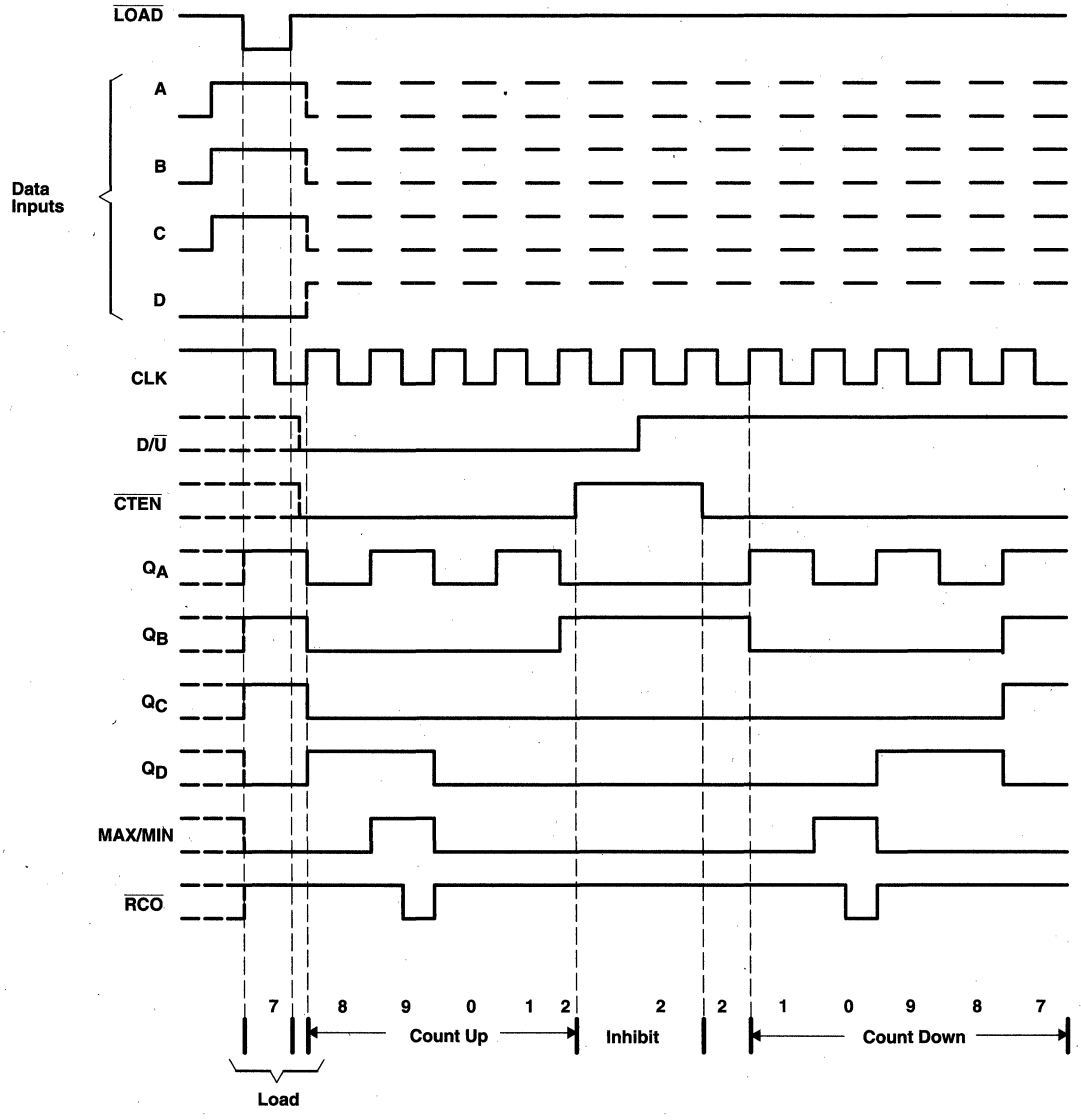
## logic diagram (positive logic)



## typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... – 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... –1.2 V to 7 V
Input current range ..... – 30 mA to 5 mA
Voltage applied to any output in the high state ..... – 0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0 °C to 70 °C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded if the input-current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | 18 | mA |
| $I_{OH}$ | High-level output current | | | – 1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | $\overline{CTEN}$ | | | – 1.8 | mA |
| | | | Others | | | – 0.6 | |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | – 60 | | – 150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | Outputs open | | | 40 | 55 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 90 | 0 | 90 | MHz |
| $t_w$ | Pulse duration | $\overline{LOAD}$ low | 6 | | 6 | | ns |
| | | CLK high | 4 | | 4 | | |
| | | CLK low | 7 | | 7 | | |
| $t_{su}$ | Setup time | Data before $\overline{LOAD}$↑ | 4 | | 4 | | ns |
| | | $\overline{CTEN}$ before CLK↑ | 6.5 | | 6.5 | | |
| | | D/$\overline{U}$ before CLK↑ | 15 | | 15 | | |
| | | $\overline{LOAD}$ inactive before CLK↑ | 10 | | 10 | | |
| $t_h$ | Hold time | Data after $\overline{LOAD}$↑ | 2 | | 2 | | ns |
| | | $\overline{CTEN}$ after CLK↑ | 1 | | 1 | | |
| | | D/$\overline{U}$ after CLK↑ | 0 | | 0 | | |

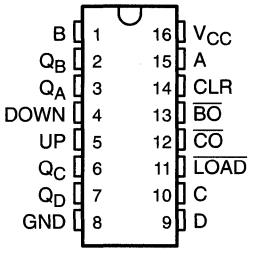
## switching characteristics (see Note )

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 90 | | | 90 | | MHz |
| $t_{PLH}$ | CLK | Any Q | 2.5 | 4.8 | 8 | 2 | 8.5 | ns |
| $t_{PHL}$ | | | 5 | 7 | 11.5 | 5 | 12 | |
| $t_{PLH}$ | CLK | MAX/MIN | 6.5 | 9.4 | 12.5 | 6 | 13 | ns |
| $t_{PHL}$ | | | 6 | 8.9 | 11 | 6 | 12 | |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 2.5 | 5.2 | 7.5 | 2 | 8 | ns |
| $t_{PHL}$ | | | 3 | 4.8 | 7.5 | 2.5 | 8 | |
| $t_{PLH}$ | $\overline{CTEN}$ | $\overline{RCO}$ | 2 | 5.7 | 7 | 2 | 7.8 | ns |
| $t_{PHL}$ | | | 3 | 5 | 7.5 | 3 | 8 | |
| $t_{PLH}$ | D/$\overline{U}$ | $\overline{RCO}$ | 8 | 13 | 16 | 8 | 17.8 | ns |
| $t_{PHL}$ | | | 4.5 | 8.1 | 10.5 | 4 | 11 | |
| $t_{PLH}$ | D/$\overline{U}$ | MAX/MIN | 4 | 7.9 | 9.8 | 3 | 11.3 | ns |
| $t_{PHL}$ | | | 3 | 7.5 | 9.5 | 3 | 10 | |
| $t_{PLH}$ | A, B, C, or D | Any Q | 2 | 4.7 | 7 | 1.5 | 7.5 | ns |
| $t_{PHL}$ | | | 6.5 | 8.9 | 12 | 6.5 | 13 | |
| $t_{PLH}$ | A, B, C, or D | MAX/MIN | 5.5 | 10.5 | 13.6 | 5 | 15.4 | ns |
| $t_{PHL}$ | | | 6.5 | 10 | 13 | 6 | 14 | |
| $t_{PLH}$ | A, B, C, or D | $\overline{RCO}$ | 6 | 15 | 18.6 | 6 | 21.1 | ns |
| $t_{PHL}$ | | | 6 | 9.5 | 13.5 | 6 | 15 | |
| $t_{PLH}$ | $\overline{LOAD}$ | Any Q | 4.5 | 7.7 | 9.8 | 4 | 11.4 | ns |
| $t_{PHL}$ | | | 5.5 | 9.9 | 12.1 | 5 | 13.1 | |
| $t_{PLH}$ | $\overline{LOAD}$ | MAX/MIN | 5.5 | 12.3 | 15.2 | 5.5 | 17 | ns |
| $t_{PHL}$ | | | 6 | 11.7 | 14 | 6 | 15.6 | |
| $t_{PLH}$ | $\overline{LOAD}$ | $\overline{RCO}$ | 8.5 | 16.8 | 19.9 | 8.5 | 23.2 | ns |
| $t_{PHL}$ | | | 7.5 | 11.6 | 14 | 7 | 15.2 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **High-Speed $f_{max}$ of 100 MHz Typical**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

The SN74F193A is a synchronous, 4-bit binary up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count/clock (UP or DOWN) input. The direction of the count is determined by which count input is pulsed while the other count input is high.

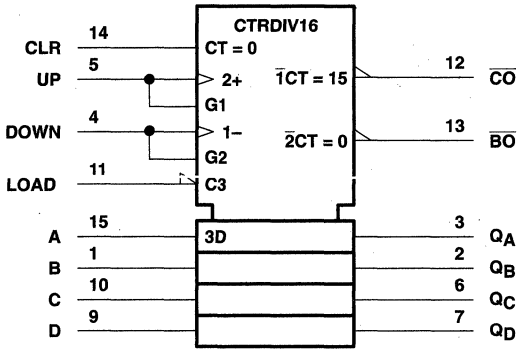
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the $\overline{LOAD}$ input and entering the desired data at the data (D) inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A high level applied to the clear (CLR) input forces all outputs to the low level. The clear function is independent of the count and load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ($\overline{BO}$) output produces a low-level pulse while the count is zero (all Q outputs low) and the DOWN input is low. Similarily, the carry ($\overline{CO}$) output produces a low-level pulse while the count is 15 (all Q outputs high) and the UP input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

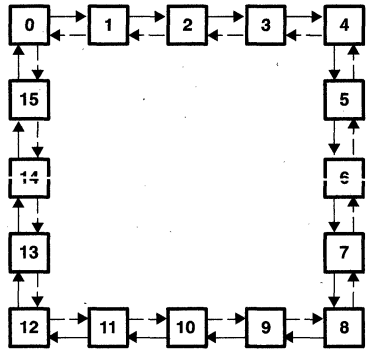
The SN74F193A is characterized for operation from 0°C to 70°C.

## logic symbol†



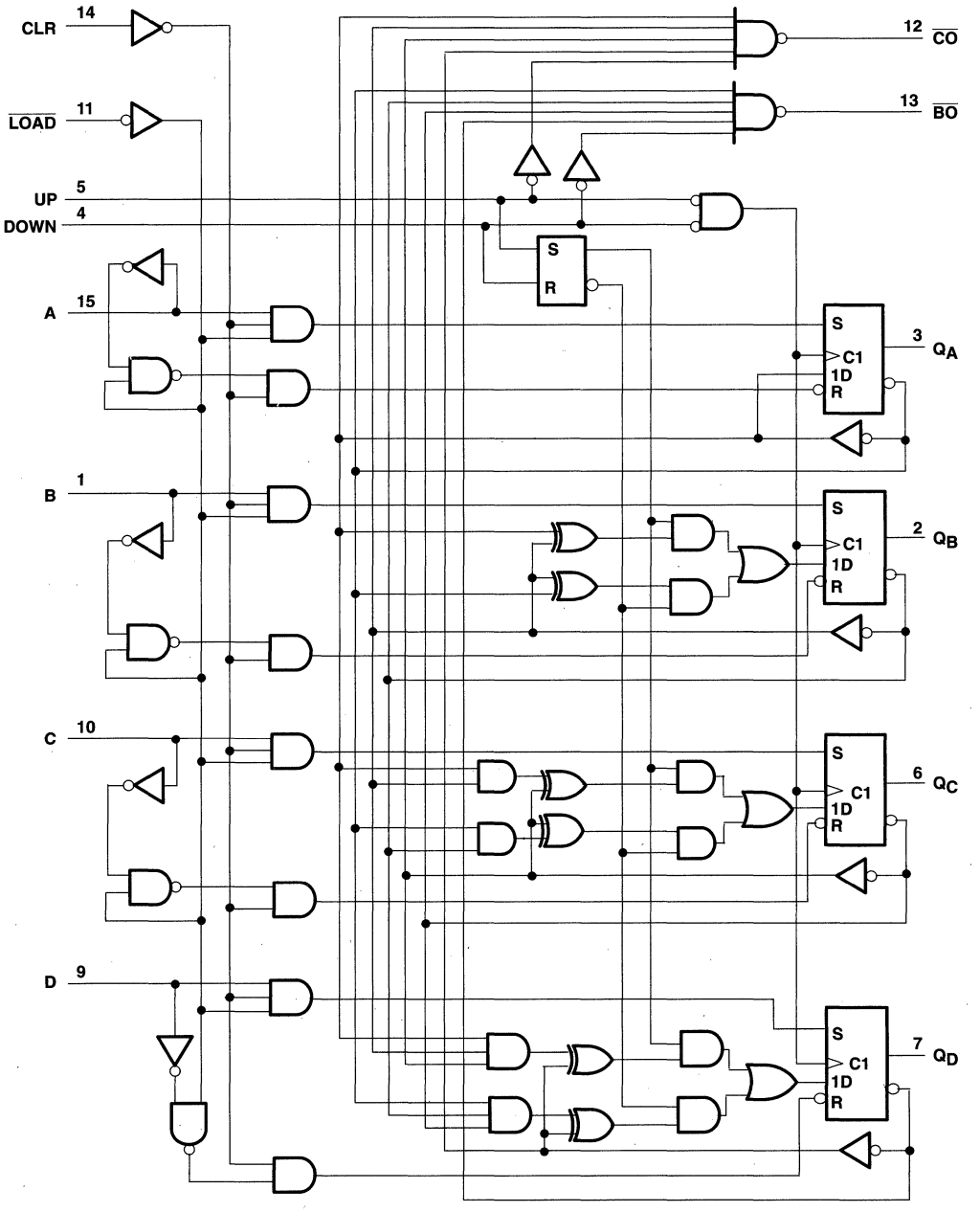

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## state diagram




Count up ⟶
Count down ⟶

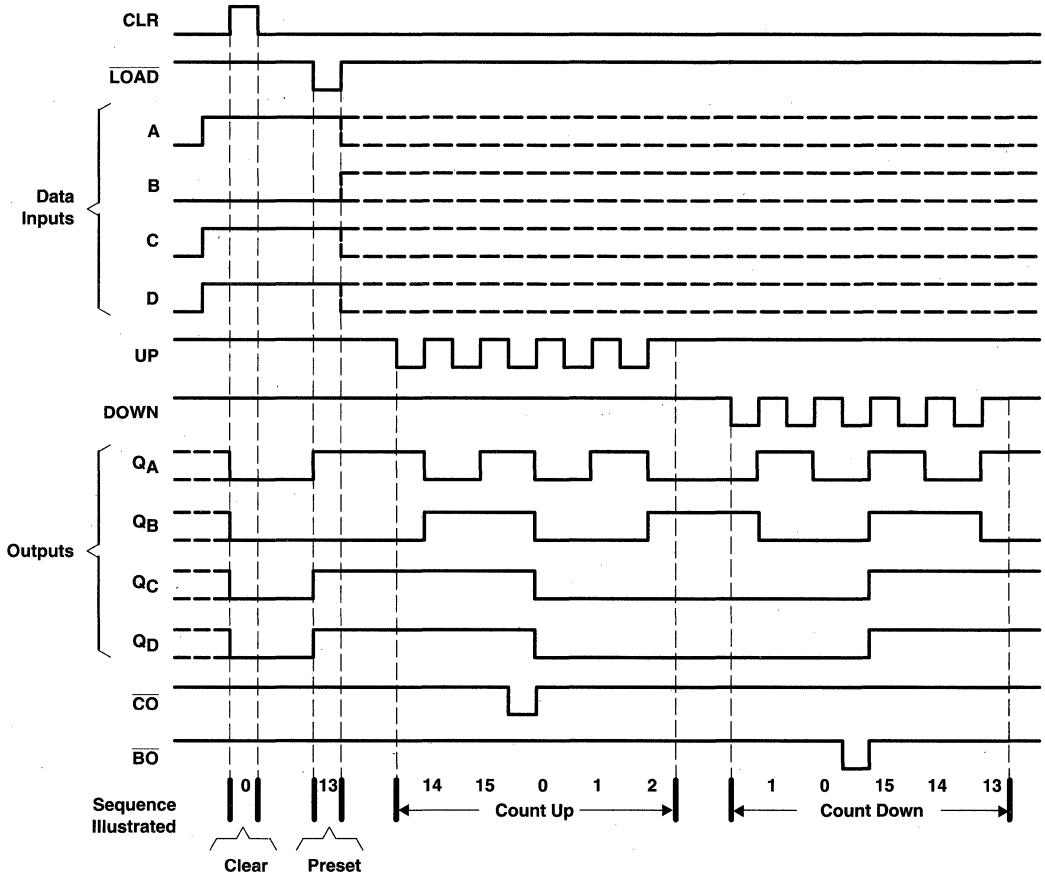
## logic diagram (positive logic)



## typical clear, load, and count sequence

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen (carry), zero, one, and two
4. Count down to one, zero (borrow), fifteen, fourteen, and thirteen



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . – 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . – 30 mA to 5 mA
Voltage applied to any output in the high state . . . . . – 0.5 V to $V_{CC}$
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded if the input-current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | 18 | mA |
| $I_{OH}$ | High-level output current | | | – 1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to 3 mA | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | UP | | | – 1.8 | mA |
| | | | Others | | | – 0.6 | |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | – 60 | | – 150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | Outputs open | | | 34 | 54 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 85 | 0 | 85 | MHz |
| $t_w$ | Pulse duration | CLR high | 4 | | 4 | | ns |
| | | $\overline{LOAD}$ low | 5.5 | | 5.5 | | |
| | | UP or DOWN high | 4 | | 4 | | |
| | | UP or DOWN low | 6 | | 6 | | |
| $t_{su}$ | Setup time | Data before $\overline{LOAD}$ inactive | 3.5 | | 3.5 | | ns |
| | | CLR inactive before UP↑ or DOWN↑ | 5 | | 5 | | |
| | | $\overline{LOAD}$ inactive before UP↑ or DOWN↑ | 7.5 | | 7.5 | | |
| $t_h$ | Hold time | Data after $\overline{LOAD}$ inactive | 2.5 | | 2.5 | | ns |

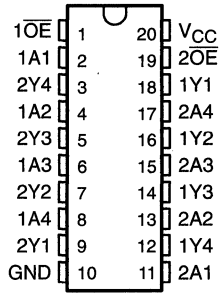
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 85 | 100 | | 85 | | MHz |
| $t_{PLH}$ | UP or DOWN | $\overline{CO}$ or $\overline{BO}$ | 2.5 | | 8.5 | 2.5 | 9 | ns |
| $t_{PHL}$ | | | 3 | | 8 | 3 | 9 | |
| $t_{PLH}$ | UP or DOWN | Any Q | 2.5 | | 8.5 | 2.5 | 9 | ns |
| $t_{PHL}$ | | | 5 | | 12 | 5 | 13 | |
| $t_{PLH}$ | A, B, C, or D | Any Q | 2 | | 7 | 1.5 | 8 | ns |
| $t_{PHL}$ | | | 6 | | 13.5 | 5 | 15 | |
| $t_{PLH}$ | $\overline{LOAD}$ | Any Q | 4.5 | | 10 | 4 | 11 | ns |
| $t_{PHL}$ | | | 5.5 | | 12 | 5 | 13 | |
| $t_{PHL}$ | CLR | Any Q | 5 | | 11 | 5 | 12 | ns |
| $t_{PLH}$ | | $\overline{CO}$ | 6 | | 12 | 5.5 | 13 | |
| $t_{PHL}$ | CLR | $\overline{BO}$ | 5 | | 11 | 5 | 12 | ns |
| $t_{PLH}$ | $\overline{LOAD}$ | $\overline{CO}$ or $\overline{BO}$ | 6 | | 13.5 | 6 | 15 | ns |
| $t_{PHL}$ | | | 6 | | 12.6 | 6 | 13.8 | |
| $t_{PLH}$ | A, B, C, or D | $\overline{CO}$ or $\overline{BO}$ | 5.5 | | 13 | 5 | 14 | ns |
| $t_{PHL}$ | | | 4.5 | | 12.5 | 4.5 | 13.5 | |

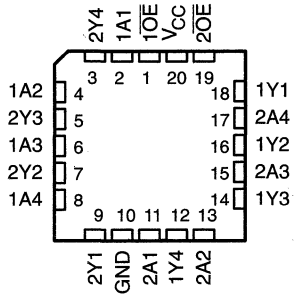
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

**SN54F240 . . . J PACKAGE**
**SN74F240 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**




**SN54F240 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F241 and 'F244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The 'F240 is organized as two 4-bit buffers/line drivers with separate output enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

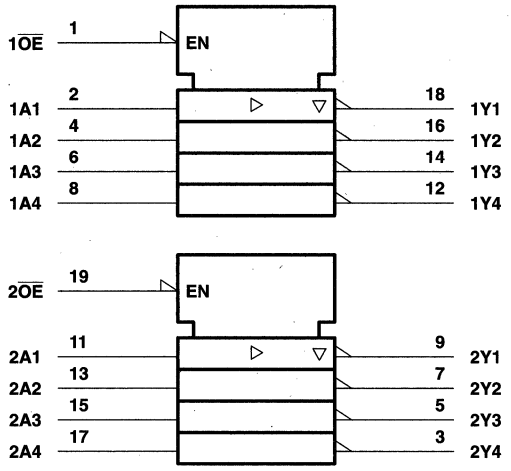
The SN74F240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F240 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

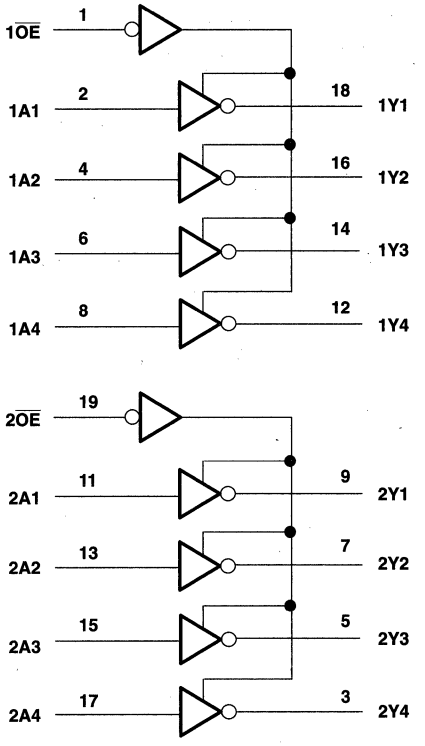
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

### logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F240 ..... 96 mA
SN74F240 ..... 128 mA
Operating free-air temperature range: SN54F240 ..... −55°C to 125°C
SN74F240 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F240 | | | SN74F240 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F240 | | | SN74F240 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | μA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1 | | | −1 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 19 | 29 | | 19 | 29 | mA |
| | | Outputs low | | 50 | 75 | | 50 | 75 | |
| | | Outputs disabled | | 42 | 63 | | 42 | 63 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F240 | | | SN54F240 | | SN74F240 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any A | Y | 2.2 | 4.7 | 7 | 2.2 | 9 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 1.2 | 3.1 | 4.7 | 1.2 | 6 | 1.2 | 5.7 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.2 | 3.1 | 5.3 | 1.2 | 6.7 | 1.2 | 6.1 | ns |
| $t_{PZL}$ | | | 3.2 | 6.5 | 9 | 3.2 | 10.5 | 3.2 | 10 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.2 | 3.6 | 5.3 | 1.2 | 6.5 | 1.2 | 6.3 | ns |
| $t_{PLZ}$ | | | 1.2 | 5.6 | 8 | 1.2 | 12.5 | 1.2 | 9.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

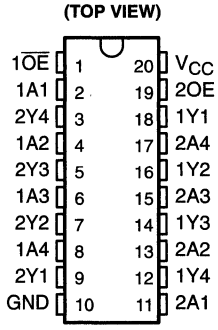
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

## description

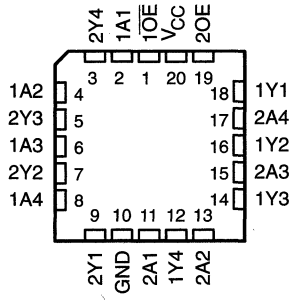
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F240 and 'F244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The SN54F241 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F241 is characterized for operation from 0°C to 70°C.

**SN54F241 . . . J PACKAGE**
**SN74F241 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F241 . . . FK PACKAGE**
**(TOP VIEW)**

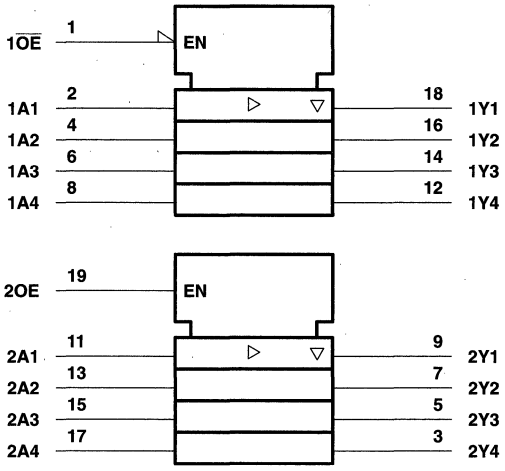



**FUNCTION TABLES**

| INPUTS | | OUTPUT |
|---|---|---|
| 1$\overline{OE}$ | 1A | 1Y |
| H | X | Z |
| L | H | H |
| L | L | L |

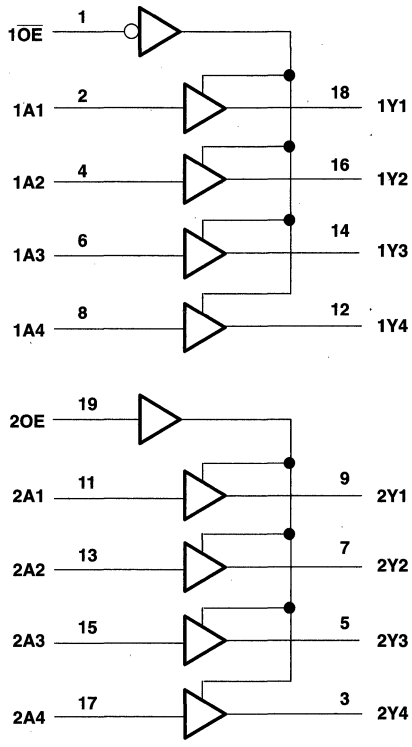
| INPUTS | | OUTPUT |
|---|---|---|
| 2OE | 2A | 2Y |
| H | H | H |
| H | L | L |
| L | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F241 ..... 96 mA
SN74F241 ..... 128 mA
Operating free-air temperature range: SN54F241 ..... −55°C to 125°C
SN74F241 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F241 | | | SN74F241 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F241 | | | SN74F241 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | μA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | OE or $\overline{OE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1 | | | −1 | mA |
| | Any A | | | | | −1.6 | | | −1.6 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | Outputs high | | 40 | 60 | | 40 | 60 | mA |
| | | | Outputs low | | 60 | 90 | | 60 | 90 | |
| | | | Outputs disabled | | 60 | 90 | | 60 | 90 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

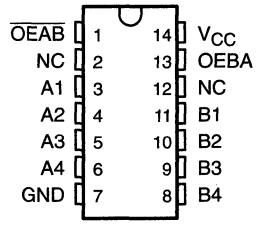
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F241 | | | SN54F241 | | SN74F241 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any A | Y | 1.7 | 3.6 | 5.2 | 1.2 | 6.5 | 1.7 | 6.2 | ns |
| $t_{PHL}$ | | | 1.7 | 3.6 | 5.2 | 1.2 | 7 | 1.7 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ or OE | Y | 1.2 | 3.9 | 5.7 | 1.2 | 7 | 1.2 | 6.7 | ns |
| $t_{PZL}$ | | | 1.2 | 5 | 7 | 1.2 | 8.5 | 1.2 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ or OE | Y | 1.2 | 4.1 | 6 | 1.2 | 7 | 1.2 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 4.1 | 6 | 1.2 | 7.5 | 1.2 | 7 | |

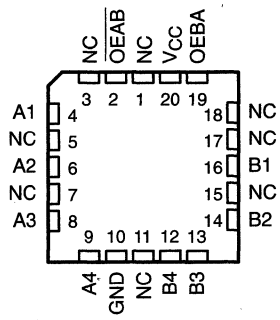
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Asynchronous Communication Between Data Buses**
- **Local Bus-Latch Capability**
- **Inverting Logic**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F242 . . . J PACKAGE**
**SN74F242 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F242 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These quadruple bus transceivers are designed for asynchronous communications between data buses. The control function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEBA and $\overline{\text{OEAB}}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

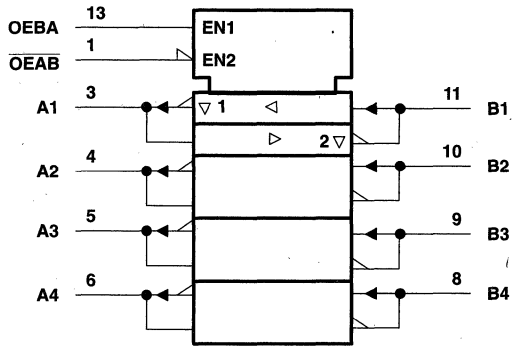
The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous enabling of OEBA and $\overline{\text{OEAB}}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) remain at their states. The 4-bit codes appearing on the two sets of buses will be complementary for the 'F242.

The SN54F242 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F242 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

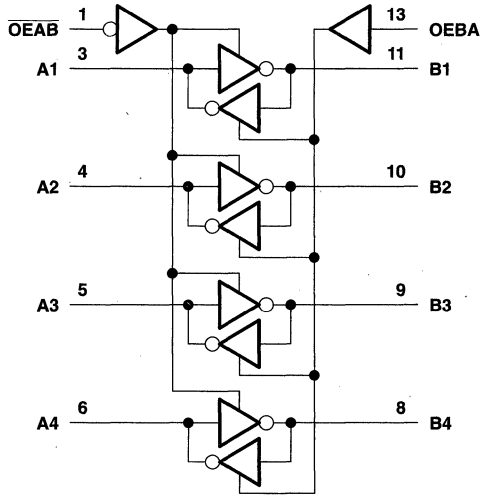
| INPUTS | | FUNCTION |
|---|---|---|
| $\overline{\text{OEAB}}$ | OEBA | |
| L | L | $\overline{\text{A}}$ to B |
| H | H | $\overline{\text{B}}$ to A |
| H | L | Isolation |
| L | H | Latch A and B (A = $\overline{\text{B}}$) |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F242 ..... 96 mA
SN74F242 ..... 128 mA
Operating free-air temperature range: SN54F242 ..... −55°C to 125°C
SN74F242 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F242 | | | SN74F242 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F242 | | | SN74F242 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | A or B port | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | Control inputs | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | A or B port‡ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | μA |
| | Control inputs | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1 | | | −1 | mA |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, See Note 2 | Outputs high | | 30 | 46 | | 30 | 46 | mA |
| | | | Outputs low | | 46 | 69 | | 46 | 69 | |
| | | | Outputs disabled | | 42 | 63 | | 42 | 63 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured either with all transceivers enabled in only one direction or all transceivers disabled.

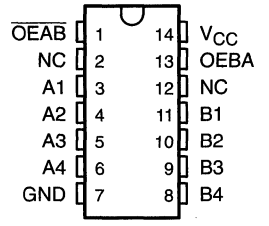
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX¶ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F242 | | | SN54F242 | | SN74F242 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 2.2 | 4.1 | 6.5 | 2.2 | 9 | 2.2 | 7.5 | ns |
| $t_{PHL}$ | | | 1 | 2.6 | 4.5 | 0.5 | 5 | 1 | 4.5 | |
| $t_{PZL}$ | Enable | A or B | 2.7 | 5.6 | 7.5 | 2.2 | 10 | 2.7 | 8.5 | ns |
| $t_{PZH}$ | | | 2.7 | 6.1 | 9 | 2.2 | 12 | 2.7 | 10.5 | |
| $t_{PHZ}$ | Disable | A or B | 1.8 | 6.6 | 9 | 1.8 | 11 | 1.8 | 9.5 | ns |
| $t_{PLZ}$ | | | 2.7 | 5.6 | 9.5 | 2.3 | 13.5 | 2.7 | 11 | |

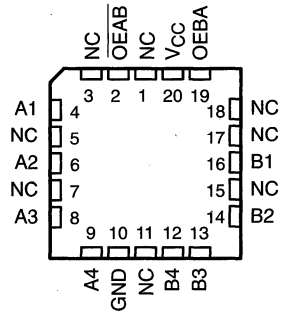
¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Asynchronous Communication Between Data Buses**
- **Local Bus-Latch Capability**
- **True Logic**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F243 . . . J PACKAGE**
**SN74F243 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F243 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These quadruple bus transceivers are designed for asynchronous communications between data buses. The control function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEBA and $\overline{\text{OEAB}}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

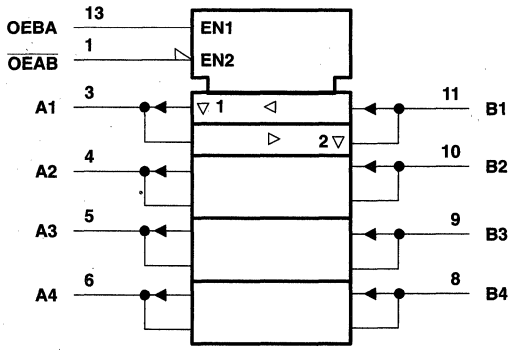
The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous enabling of OEBA and $\overline{\text{OEAB}}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) remain at their states. The 4-bit codes appearing on the two sets of buses will be identical for the 'F243.

The SN54F243 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F243 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

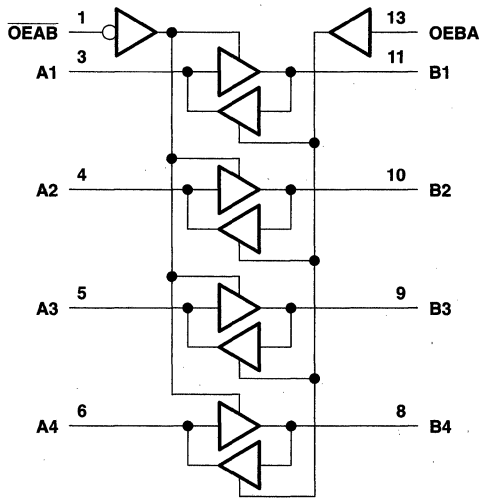
| INPUTS | | FUNCTION |
|---|---|---|
| $\overline{\text{OEAB}}$ | OEBA | |
| L | L | A to B |
| H | H | B to A |
| H | L | Isolation |
| L | H | Latch A and B (A = B) |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F243 ..... 96 mA
SN74F243 ..... 128 mA
Operating free-air temperature range: SN54F243 ..... −55°C to 125°C
SN74F243 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F243 | | | SN74F243 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F243 | | | SN74F243 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | A or B port | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | Control inputs | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | A or B port‡ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | µA |
| | Control inputs | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1 | | | −1.6 | mA |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, See Note 2 | Outputs high | | 64 | 80 | | 64 | 80 | mA |
| | | | Outputs low | | 64 | 90 | | 64 | 90 | |
| | | | Outputs disabled | | 71 | 90 | | 71 | 90 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured either with all transceivers enabled in only one direction or all transceivers disabled.

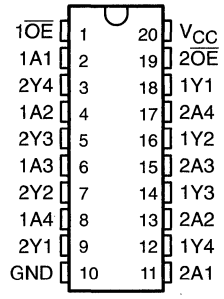
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX¶ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F243 | | | SN54F243 | | SN74F243 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.7 | 3.6 | 5.2 | 1.2 | 6.5 | 1.2 | 6.2 | ns |
| $t_{PHL}$ | | | 1.7 | 3.6 | 5.2 | 1.2 | 8.5 | 1.2 | 6.5 | |
| $t_{PZH}$ | Enable | A or B | 1.2 | 3.9 | 5.7 | 1.2 | 8 | 1.2 | 6.7 | ns |
| $t_{PZL}$ | | | 1.2 | 5.4 | 7.5 | 1.2 | 10.5 | 1.2 | 8.5 | |
| $t_{PHZ}$ | Disable | A or B | 1.2 | 4.1 | 6 | 1 | 7.5 | 1 | 7 | ns |
| $t_{PLZ}$ | | | 2 | 4.5 | 6 | 2 | 8.5 | 2 | 7 | |

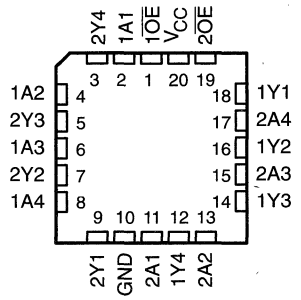
¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

**SN54F244 . . . J PACKAGE**
**SN74F244 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**




**SN54F244 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F240 and 'F241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The 'F244 is organized as two 4-bit buffers/line drivers with separate output enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

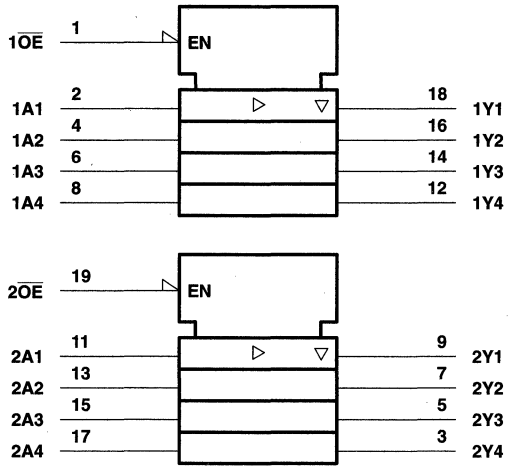
The SN74F244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F244 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

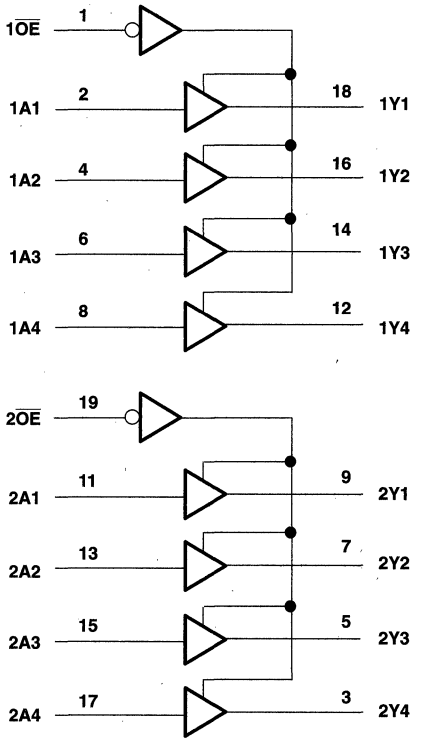
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F244 ..... 96 mA
SN74F244 ..... 128 mA
Operating free-air temperature range: SN54F244 ..... −55°C to 125°C
SN74F244 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F244 | | | SN74F244 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F244 | | | SN74F244 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $\overline{OE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1 | | | −1 | mA |
| | Any A | | | | | −1.6 | | | −1.6 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, Outputs open | Outputs high | | 40 | 60 | | 40 | 60 | mA |
| | | | Outputs low | | 60 | 90 | | 60 | 90 | |
| | | | Outputs disabled | | 60 | 90 | | 60 | 90 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F244 | | | SN54F244 | | SN74F244 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.7 | 3.6 | 5.2 | 2 | 6.5 | 1.7 | 6.2 | ns |
| $t_{PHL}$ | | | 1.7 | 3.6 | 5.2 | 2 | 7 | 1.7 | 6.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.2 | 3.9 | 5.7 | 2 | 7 | 1.2 | 6.7 | ns |
| $t_{PZL}$ | | | 1.2 | 5 | 7 | 2 | 8.5 | 1.2 | 8 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.2 | 4.1 | 6 | 2 | 7 | 1.2 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 4.1 | 6 | 2 | 7.5 | 1.2 | 7 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines Directly**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

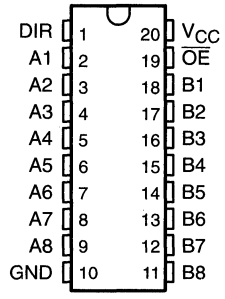
## description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

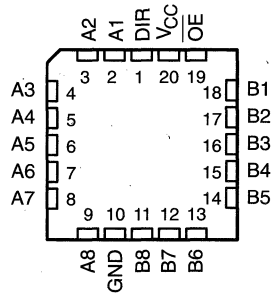
The SN74F245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F245 is characterized for operation from 0°C to 70°C.

**SN54F245 . . . J PACKAGE**
**SN74F245 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**



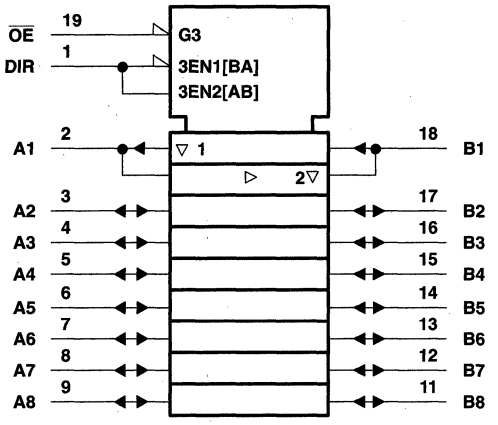

**SN54F245 . . . FK PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**

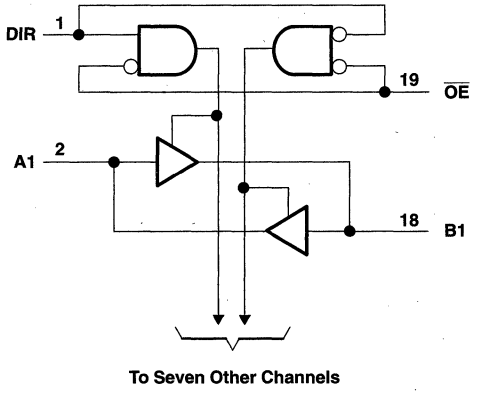
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | −0.5 V to 7 V |
| Input voltage range, $V_I$ (except I/O ports) (see Note 1) | | −1.2 V to 7 V |
| Input current range | | −30 mA to 5 mA |
| Voltage range applied to any output in the disabled or power-off state | | −0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | | −0.5 V to $V_{CC}$ |
| Current into any output in the low state: | SN54F245 (A1 thru A8) | 40 mA |
| | SN54F245 (B1 thru B8) | 96 mA |
| | SN74F245 (A1 thru A8) | 48 mA |
| | SN74F245 (B1 thru B8) | 128 mA |
| Operating free-air temperature range: | SN54F245 | −55°C to 125°C |
| | SN74F245 | 0°C to 70°C |
| Storage temperature range | | −65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | | SN54F245 | | | SN74F245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | A1 thru A8 | | | −3 | | | −3 | mA |
| | | B1 thru B8 | | | −12 | | | −15 | |
| $I_{OL}$ | Low-level output current | A1 thru A8 | | | 20 | | | 24 | mA |
| | | B1 thru B8 | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F245 | | | SN74F245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | A1 thru A8 | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | B1 thru B8 | $V_{CC}$ = 4.5 V | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | Any output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | A1 thru A8 | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | B1 thru B8 | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | A and B | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | DIR, $\overline{OE}$ | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$‡ | A and B | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | µA |
| | DIR, $\overline{OE}$ | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | A and B | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.65 | | | −0.65 | mA |
| | DIR, $\overline{OE}$ | | | | | −1.2 | | | −1.2 | |
| $I_{OS}$§ | A1 thru A8 | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| | B1 thru B8 | | | −100 | | −225 | −100 | | −225 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | Outputs high | | 70 | 90 | | 70 | 90 | mA |
| | | | Outputs low | | 95 | 120 | | 95 | 120 | |
| | | | Outputs disabled | | 85 | 110 | | 85 | 110 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

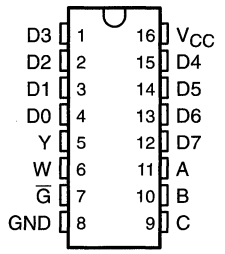
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F245 | | | SN54F245 | | SN74F245 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.7 | 3.8 | 6 | 1.2 | 7.5 | 1.7 | 7 | ns |
| $t_{PHL}$ | | | 1.7 | 4.2 | 6 | 1.2 | 7.5 | 1.7 | 7 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 2.2 | 4.9 | 7 | 1.7 | 9 | 2.2 | 8 | ns |
| $t_{PZL}$ | | | 2.7 | 5.6 | 8 | 2.2 | 10 | 2.7 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 2.2 | 4.6 | 6.5 | 1.7 | 9 | 2.2 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.2 | 4.6 | 6.5 | 1.2 | 10 | 1.2 | 7.5 | |

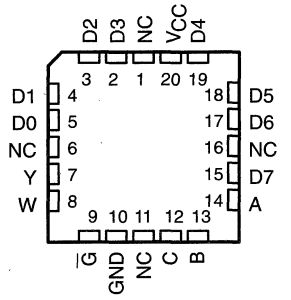
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **3-State Versions of SN54F151B and SN74F151B**
- **3-State Outputs Interface Directly With System Bus**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F251B . . . J PACKAGE**
**SN74F251B . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F251B . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These data selectors/multiplexers contain full binary decoding to select one of eight data sources and feature strobe-controlled complementary outputs. The 3-state outputs can interface with and drive data lines of bus-organized systems. When the strobe ($\overline{G}$) input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly.

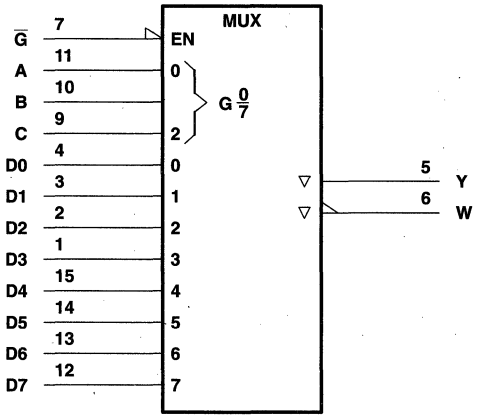
The SN54F251B is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F251B is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| SELECT | | | STROBE | | |
| C | B | A | $\overline{G}$ | Y | W |
| X | X | X | H | Z | Z |
| L | L | L | L | D0 | $\overline{D0}$ |
| L | L | H | L | D1 | $\overline{D1}$ |
| L | H | L | L | D2 | $\overline{D2}$ |
| L | H | H | L | D3 | $\overline{D3}$ |
| H | L | L | L | D4 | $\overline{D4}$ |
| H | L | H | L | D5 | $\overline{D5}$ |
| H | H | L | L | D6 | $\overline{D6}$ |
| H | H | H | L | D7 | $\overline{D7}$ |

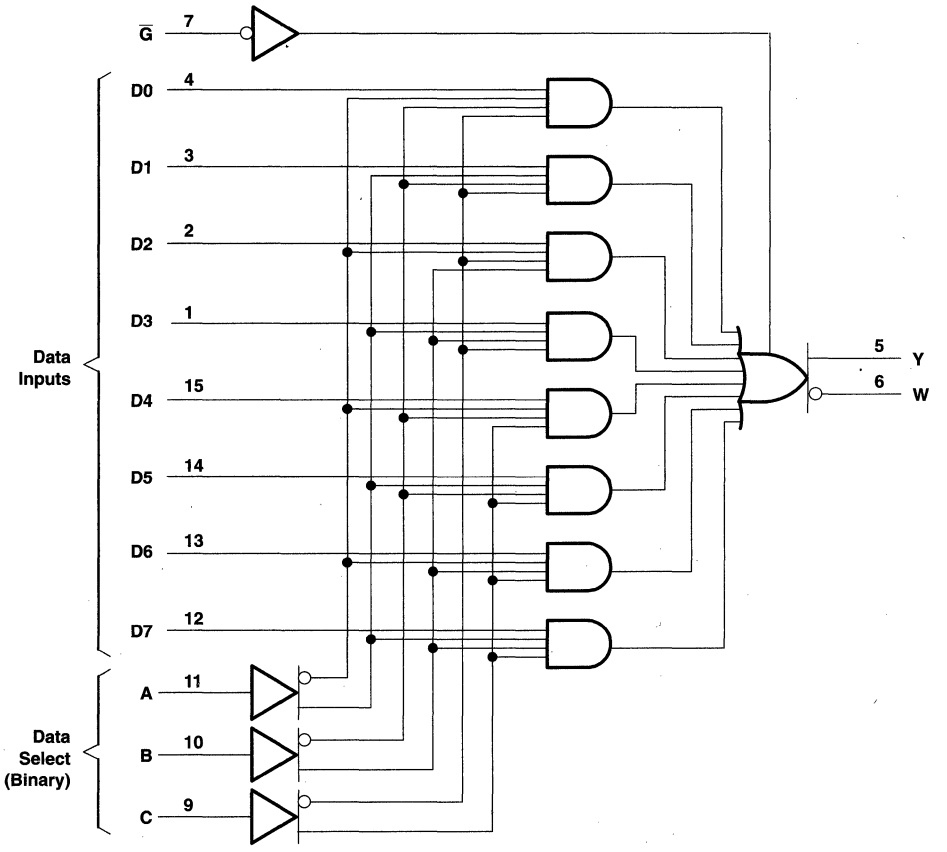
D0, D1, . . . D7 = the level of the respective D input.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | −0.5 V to 7 V |
| Input voltage range (see Note 1) | | −1.2 V to 7 V |
| Input current range | | −30 mA to 5 mA |
| Voltage range applied to any output in the disabled or power-off state | | −0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | | −0.5 V to $V_{CC}$ |
| Current into any output in the low state: | SN54F251B | 40 mA |
| | SN74F251B | 48 mA |
| Operating free-air temperature range: | SN54F251B | −55°C to 125°C |
| | SN74F251B | 0°C to 70°C |
| Storage temperature range | | −65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F251B | | | SN74F251B | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F251B | | | SN74F251B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | μA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, See Note 2 | Condition A | | 15 | 22 | | 15 | 22 | mA |
| | | Condition B | | 16 | 24 | | 16 | 24 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with the outputs open under the following conditions:
A. Select input and data input at 4.5 V, output control grounded
B. All inputs at 4.5 V

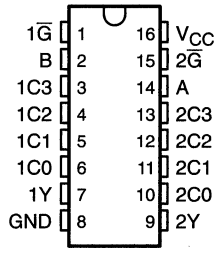
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F251B | | | SN54F251B | | SN74F251B | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, or C | W | 3.5 | 5.4 | 9 | 3.5 | 11.5 | 3.5 | 9.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4.4 | 7.5 | 2.5 | 8 | 2.5 | 7.5 | |
| $t_{PLH}$ | A, B, or C | Y | 4.5 | 6.2 | 10.5 | 3.5 | 14 | 4 | 12.5 | ns |
| $t_{PHL}$ | | | 4 | 6 | 8.5 | 3 | 10.9 | 3.5 | 9 | |
| $t_{PLH}$ | Any D | W | 2.5 | 3.7 | 6.5 | 1.8 | 8 | 2 | 7 | ns |
| $t_{PHL}$ | | | 1 | 1.9 | 4 | 1 | 6 | 1 | 5 | |
| $t_{PLH}$ | Any D | Y | 3 | 3.8 | 7 | 2.3 | 9 | 2.3 | 8 | ns |
| $t_{PHL}$ | | | 3 | 4.5 | 7 | 2.3 | 9 | 2.5 | 8 | |
| $t_{PZH}$ | $\overline{G}$ | W | 2.5 | 3.6 | 6 | 2 | 7 | 2 | 7 | ns |
| $t_{PZL}$ | | | 2.5 | 3.8 | 6 | 2.5 | 7.5 | 2.5 | 6.5 | |
| $t_{PHZ}$ | $\overline{G}$ | W | 1.9 | 2.5 | 5.5 | 1.4 | 6 | 1.5 | 6 | ns |
| $t_{PLZ}$ | | | 1 | 2.4 | 4.5 | 1 | 5 | 1 | 4.5 | |
| $t_{PZH}$ | $\overline{G}$ | Y | 3.4 | 4.8 | 7 | 2.7 | 8.5 | 2.9 | 8.5 | ns |
| $t_{PZL}$ | | | 2.9 | 4 | 7.5 | 2.6 | 9 | 2.6 | 8 | |
| $t_{PHZ}$ | $\overline{G}$ | Y | 1.9 | 2.5 | 5.5 | 1.7 | 5.5 | 1.8 | 5.5 | ns |
| $t_{PLZ}$ | | | 1 | 2.3 | 4.5 | 1 | 5.5 | 1 | 4.5 | |

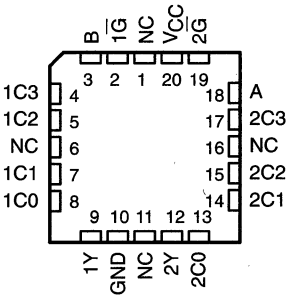
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **3-State Versions of SN54F153 and SN74F153**
- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F253 . . . J PACKAGE**
**SN74F253 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F253 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These data selectors/multiplexers contain inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$) inputs. The output is disabled when its strobe is high.

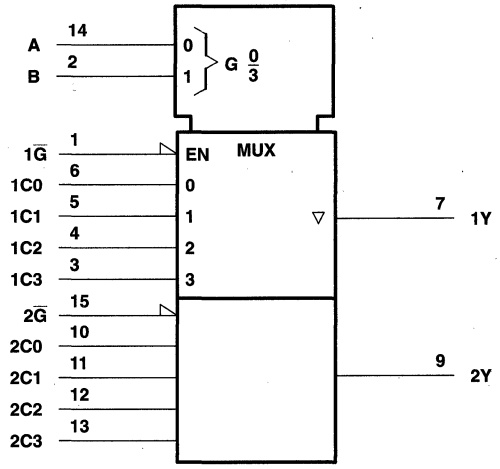
The SN54F253 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F253 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | | STROBE $\overline{G}$ | OUTPUT Y |
|---|---|---|---|---|---|---|---|
| SELECT | | DATA | | | | | |
| B | A | C0 | C1 | C2 | C3 | | |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

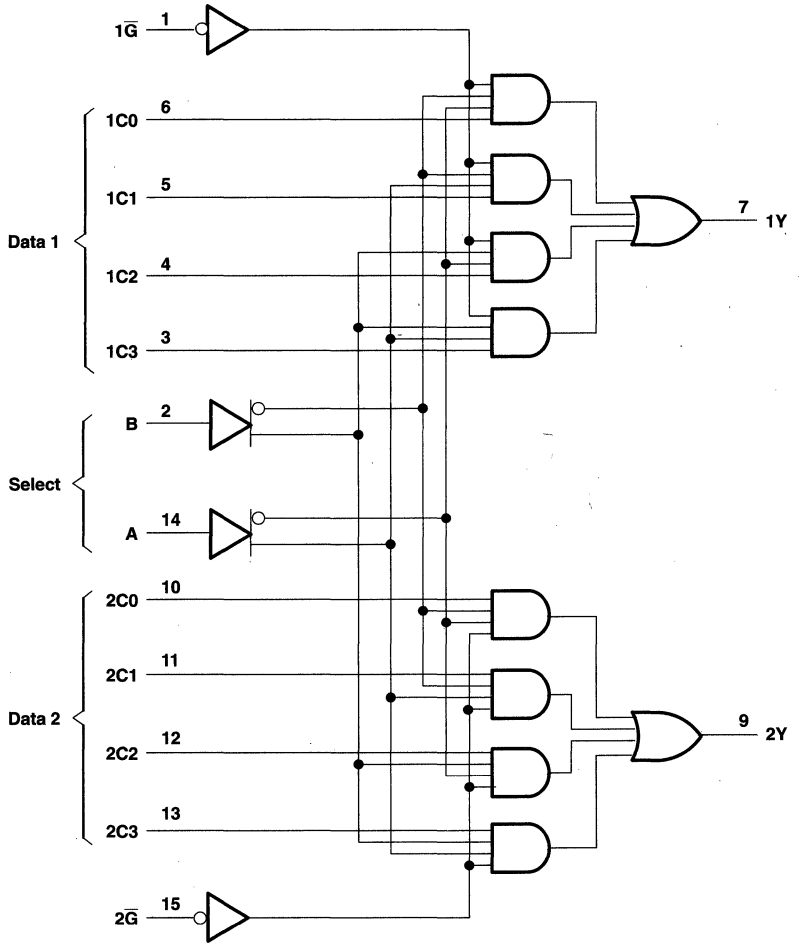
Select inputs A and B are common to both sections.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F253 ..... 40 mA
SN74F253 ..... 48 mA
Operating free-air temperature range: SN54F253 ..... −55°C to 125°C
SN74F253 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

| | | SN54F253 | | | SN74F253 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F253 | | | SN74F253 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = − 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = − 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = − 1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | − 0.6 | | | − 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, See Note 2 | Condition A | | 11.5 | 16 | | 11.5 | 16 | mA |
| $I_{CCL}$ | | Condition B | | 16 | 23 | | 16 | 23 | |
| $I_{CCZ}$ | | Condition C | | 16 | 23 | | 16 | 23 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with the outputs open under the following conditions:
A. Inputs A, B, 1C3, and 2C3 at 4.5 V, other inputs grounded
B. All inputs grounded
C. Inputs $1\overline{G}$ and $2\overline{G}$ at 4.5 V, other inputs grounded

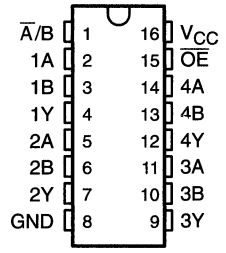
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F253 | | | SN54F253 | | SN74F253 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 3.7 | 8.1 | 11.5 | 2.7 | 15 | 3.7 | 13 | ns |
| $t_{PHL}$ | | | 2.2 | 6.1 | 9 | 1.7 | 11 | 2.2 | 10 | |
| $t_{PLH}$ | Any C | Any Y | 2.2 | 5.1 | 7 | 1.7 | 9 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 1.7 | 4.1 | 6 | 1.7 | 8 | 1.7 | 7 | |
| $t_{PZH}$ | $\overline{G}$ | Any Y | 2.2 | 5.6 | 8 | 1.7 | 10 | 2.2 | 9 | ns |
| $t_{PZL}$ | | | 2.2 | 5.6 | 8 | 1.7 | 10 | 2.2 | 9 | |
| $t_{PHZ}$ | $\overline{G}$ | Any Y | 1.2 | 3.3 | 5 | 1.2 | 6.5 | 1.2 | 6 | ns |
| $t_{PLZ}$ | | | 1.2 | 4 | 6 | 1.2 | 8 | 1.2 | 7 | |

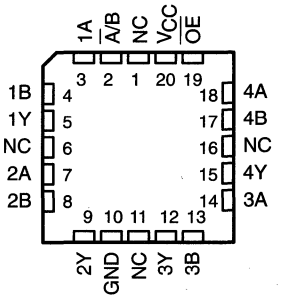
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuit and waveforms are shown in Section 1.

- **3-State Outputs Interface Directly With System Bus**
- **Provides Bus Interface From Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F257 . . . J PACKAGE**
**SN74F257 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F257 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

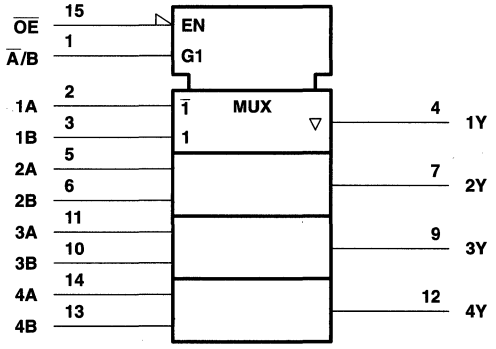
The 'F257 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output enable ($\overline{OE}$) input is at a high logic level.

The SN54F257 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F257 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

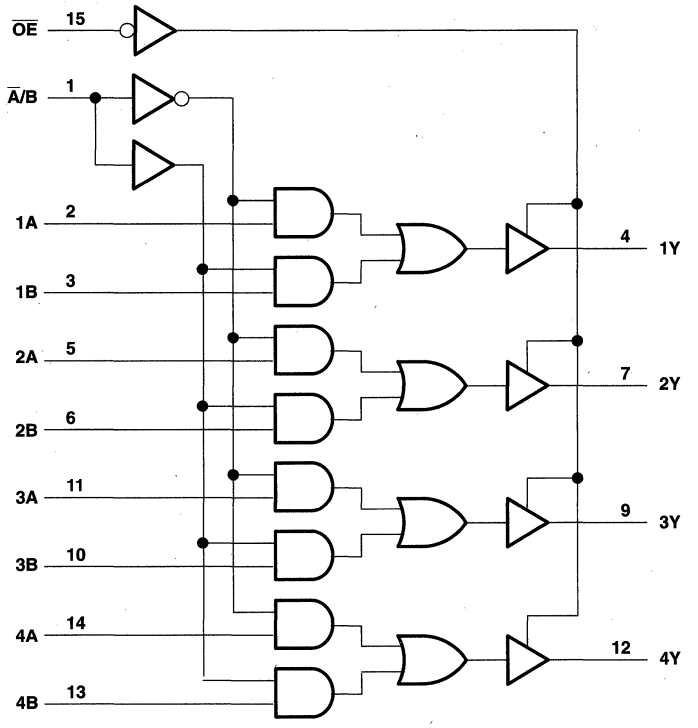
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | $\overline{A}$/B | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | L |
| L | L | H | X | H |
| L | H | X | L | L |
| L | H | X | H | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F257 ..... 40 mA
SN74F257 ..... 48 mA
Operating free-air temperature range: SN54F257 ..... −55°C to 125°C
SN74F257 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F257 | | | SN74F257 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F257 | | | SN74F257 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | μA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, See Note 2 | Condition A | | 9 | 15 | | 9 | 15 | mA |
| $I_{CCL}$ | | Condition B | | 14.5 | 22 | | 14.5 | 22 | |
| $I_{CCZ}$ | | Condition C | | 15 | 23 | | 15 | 23 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with the outputs open under the following conditions:
A. $\overline{A}$/B and all B inputs at 4.5 V, other inputs grounded
B. All B inputs at 4.5 V, other inputs grounded
C. $\overline{OE}$ and all B data inputs at 4.5 V, other inputs grounded

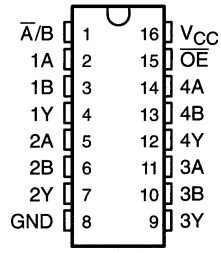
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F257 | | | SN54F257 | | SN74F257 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Any Y | 2.2 | 4.1 | 6 | 2.2 | 8 | 2.2 | 7 | ns |
| $t_{PHL}$ | | | 1.2 | 3.8 | 5.5 | 1 | 8 | 1.2 | 6.5 | |
| $t_{PLH}$ | A/B | Any Y | 3.7 | 9.7 | 13 | 3.7 | 15.5 | 3.7 | 15 | ns |
| $t_{PHL}$ | | | 2.7 | 6.1 | 8.5 | 2.7 | 10.5 | 2.7 | 9.5 | |
| $t_{PZH}$ | $\overline{G}$ | Any Y | 2.2 | 5.5 | 7.5 | 2.2 | 9.5 | 2.2 | 8.5 | ns |
| $t_{PZL}$ | | | 2.2 | 5.1 | 7.5 | 2.2 | 10 | 2.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{G}$ | Any Y | 1.2 | 3.9 | 6 | 1.2 | 7 | 1.2 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 4.1 | 6 | 1.2 | 9.5 | 1.2 | 7 | |

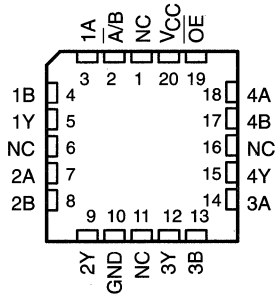
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Interface Directly With System Bus**
- **Provides Bus Interface From Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F258 . . . J PACKAGE**
**SN74F258 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F258 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

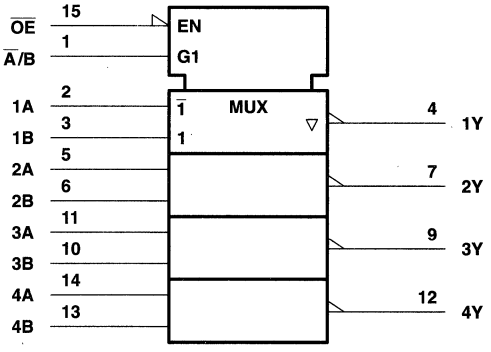
The 'F258 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54F258 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F258 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

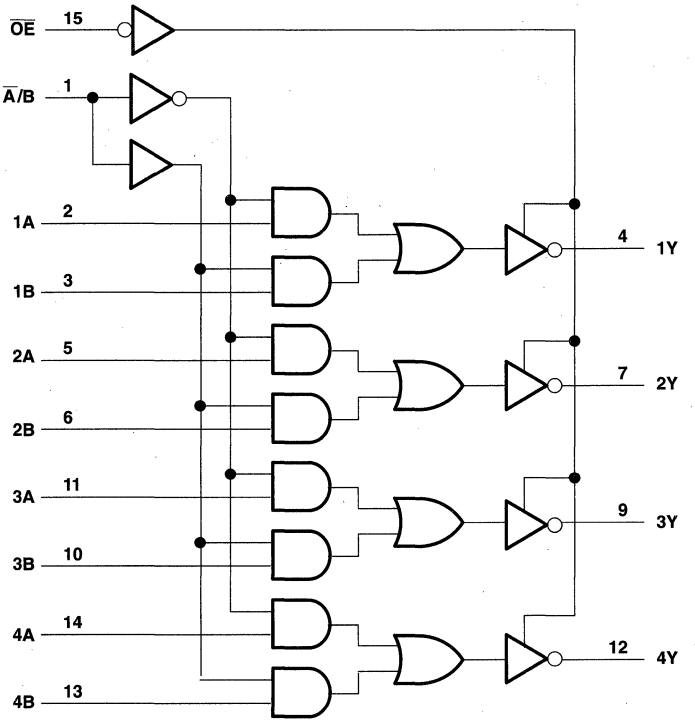
| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | $\overline{A}$/B | A | B | Y |
| H | X | X | X | Z |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | −0.5 V to 7 V |
| Input voltage range (see Note 1) | | −1.2 V to 7 V |
| Input current range | | −30 mA to 5 mA |
| Voltage range applied to any output in the disabled or power-off state | | −0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | | −0.5 V to $V_{CC}$ |
| Current into any output in the low state: | SN54F258 | 40 mA |
| | SN74F258 | 48 mA |
| Operating free-air temperature range: | SN54F258 | −55°C to 125°C |
| | SN74F258 | 0°C to 70°C |
| Storage temperature range | | −65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F258 | | | SN74F258 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F258 | | | SN74F258 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, See Note 2 | Condition A | | 6.2 | 9.5 | | 6.2 | 9.5 | mA |
| $I_{CCL}$ | | Condition B | | 15.1 | 23 | | 15.1 | 23 | |
| $I_{CCZ}$ | | Condition C | | 11.3 | 17 | | 11.3 | 17 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with the outputs open under the following conditions:
A. All B inputs at 4.5 V, other inputs grounded
B. $\overline{A}$/B and all B inputs at 4.5 V, other inputs grounded
C. $\overline{OE}$ and all B inputs at 4.5 V, other inputs grounded

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F258 | | | SN54F258 | | SN74F258 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Data (A or B) | Any Y | 1 | 3.6 | 5.3 | 1 | 7.5 | 1 | 6 | ns |
| $t_{PHL}$ | | | 1 | 3.1 | 4.7 | 1 | 6 | 1 | 5.5 | |
| $t_{PLH}$ | A/B | Any Y | 3.2 | 6.1 | 8.5 | 3.2 | 12 | 3.2 | 9.5 | ns |
| $t_{PHL}$ | | | 3.2 | 6.9 | 9.5 | 3.2 | 11.5 | 3.2 | 11 | |
| $t_{PZH}$ | $\overline{G}$ | Any Y | 2.2 | 5.5 | 7.5 | 2.2 | 11 | 2.2 | 8.5 | ns |
| $t_{PZL}$ | | | 2.2 | 5.1 | 7.5 | 2.2 | 9.5 | 2.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{G}$ | Any Y | 1.2 | 3.9 | 6 | 1 | 7 | 1.2 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 4.1 | 6 | 1.2 | 9 | 1.2 | 7 | |

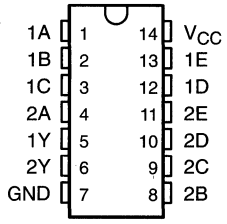
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

SDFS012A – D3214, JANUARY 1989 – REVISED OCTOBER 1993

- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)

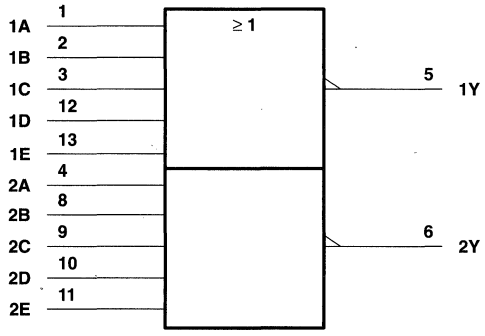



## description

The SN74F260 contains two independent 5-input positive-NOR gates. It performs the Boolean functions $Y = \overline{A + B + C + D + E}$ in positive logic.

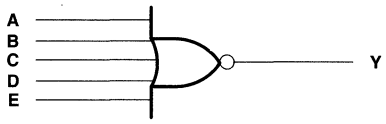
The SN74F260 is characterized for operation from 0°C to 70°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram, each gate (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | −1.2 V to 7 V |
| Input current range | −30 mA to 5 mA |
| Voltage range applied to any output in the high state | −0.5 V to $V_{CC}$ |
| Current into any output in the low state | 40 mA |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 4.6 | 6.5 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 7.3 | 9.5 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, C, D, E | Y | 1.7 | 4 | 5.5 | 1.2 | 6.5 | ns |
| $t_{PHL}$ | | | 1 | 2.5 | 4 | 1 | 4.5 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

SDFS008A – D2932, APRIL 1986 – REVISED OCTOBER 1993

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for N-Bits Parity**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

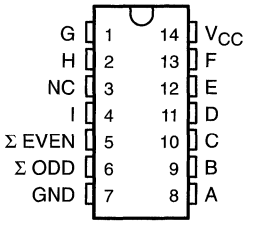
These universal, monolithic, 9-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The SN54F280B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F280B is characterized for operation from 0°C to 70°C.

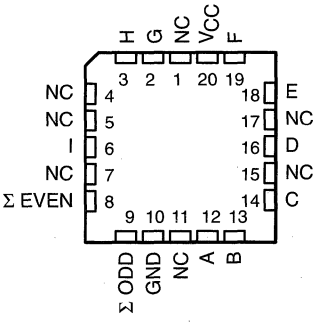
**FUNCTION TABLE**

| NO. OF INPUTS A THRU I THAT ARE HIGH | OUTPUTS | |
|---|---|---|
| | Σ EVEN | Σ ODD |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

**SN54F280B . . . J PACKAGE**
**SN74F280B . . . D OR N PACKAGE**
**(TOP VIEW)**

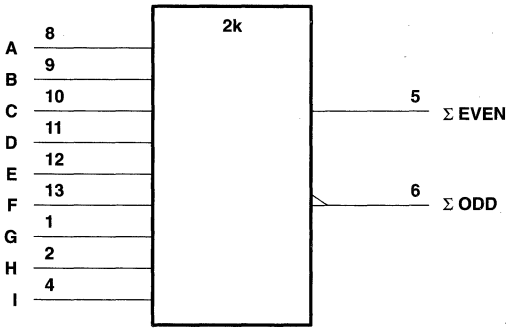



**SN54F280B . . . FK PACKAGE**
**(TOP VIEW)**



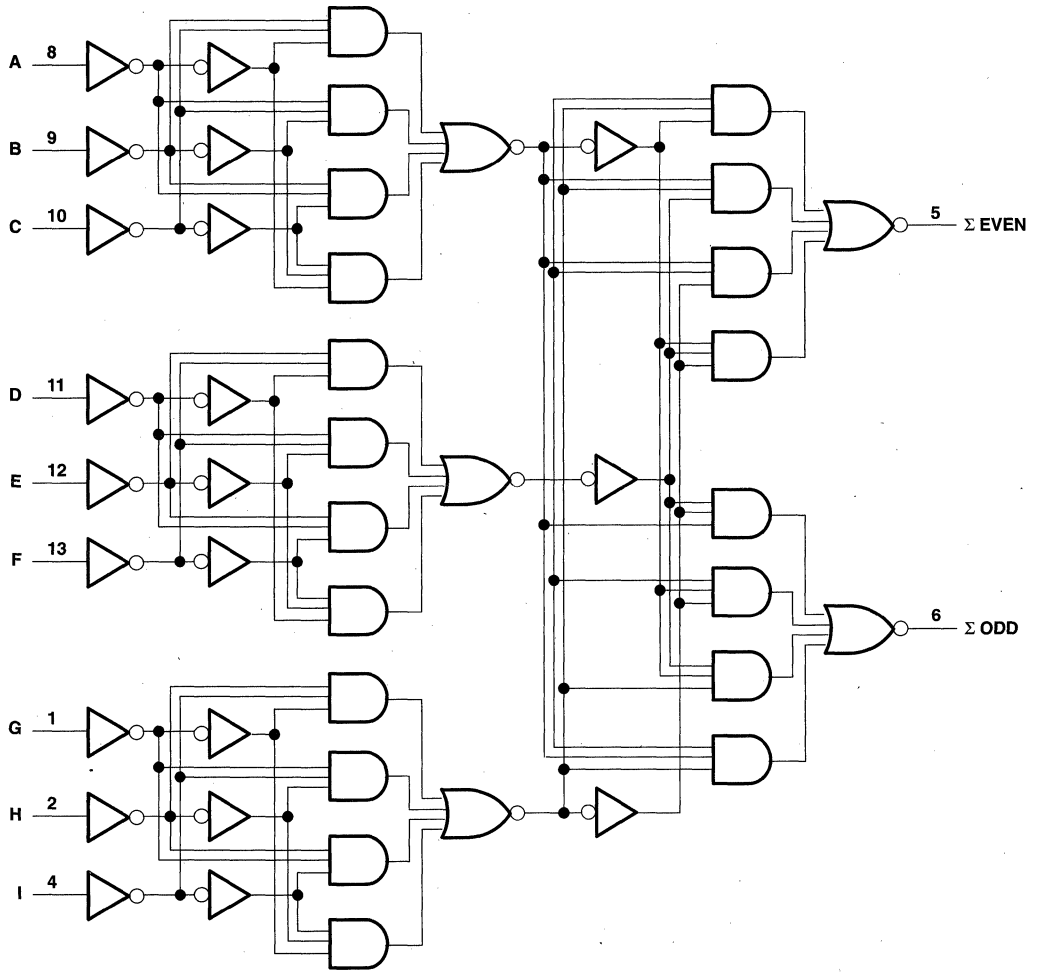

NC – No internal connection

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F280B ..... −55°C to 125°C
SN74F280B ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F280B | | | SN74F280B | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F280B | | | SN74F280B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −20 | | | −20 | µA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 26 | 35 | | 26 | 35 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

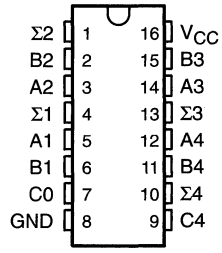
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F280B | | | SN54F280B | | SN74F280B | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any input | Σ EVEN | 3.2 | 6.1 | 9 | 2.7 | 13 | 2.7 | 10 | ns |
| $t_{PHL}$ | | | 3.2 | 6.6 | 10 | 2.7 | 15 | 2.7 | 11 | |
| $t_{PLH}$ | Any input | Σ ODD | 3.2 | 6.1 | 9 | 2.7 | 14 | 2.7 | 10 | ns |
| $t_{PHL}$ | | | 3.2 | 6.6 | 10 | 2.7 | 14 | 2.7 | 11 | |

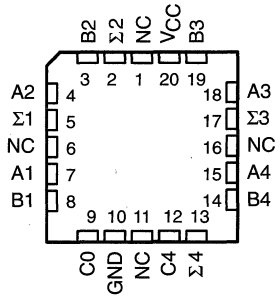
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Full-Carry Look-Ahead Across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance With the Economy of Ripple Carry**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F283 . . . J PACKAGE**
**SN74F283 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54F283 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The 'F283 is a full adder that performs the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) output is obtained from the fourth bit.

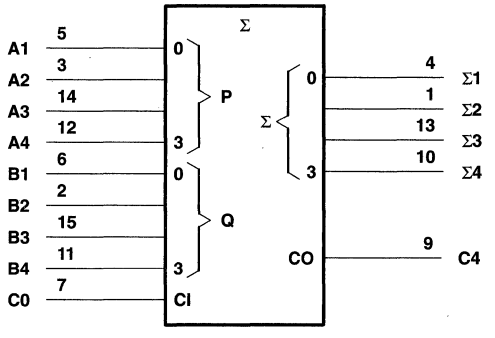
The device features full internal look-ahead across all four bits generating the carry term C4 in typically 5.7 ns. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End-around carry can be accomplished without the need for logic or level inversion.

The 'F283 can be used with either all-active-high (positive logic) or all-active-low (negative logic) operands.

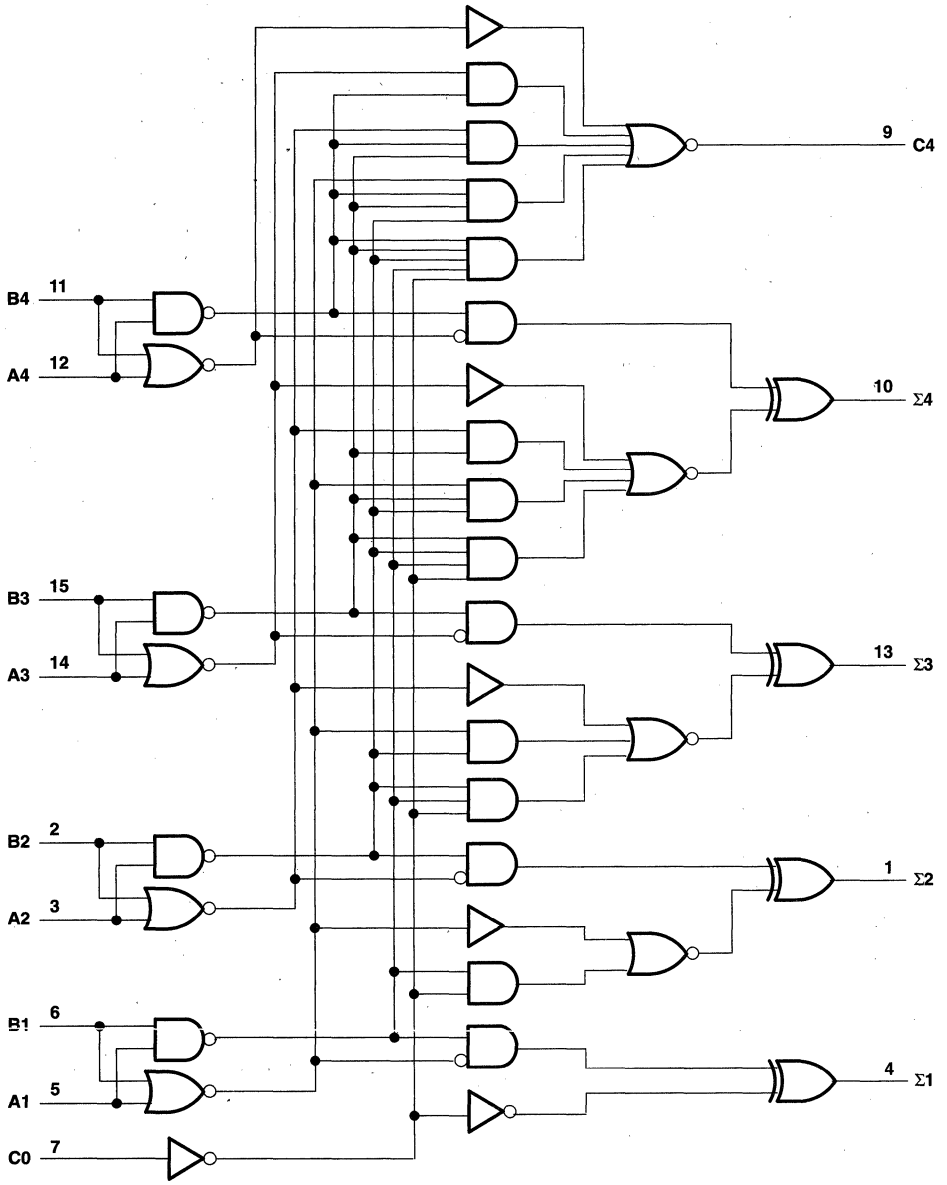
The SN54F283 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F283 is characterized for operation from 0°C to 70°C.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | WHEN C0 = L | | | WHEN C0 = H | | |
| | | | | WHEN C2 = L | | | WHEN C2 = H | | |
| A1 | B1 | A2 | B2 | Σ1 | Σ2 | C2 | Σ1 | Σ2 | C2 |
| A3 | B3 | A4 | B4 | Σ3 | Σ4 | C4 | Σ3 | Σ4 | C4 |
| L | L | L | L | L | L | L | H | L | L |
| H | L | L | L | H | L | L | L | H | L |
| L | H | L | L | H | L | L | L | H | L |
| H | H | L | L | L | H | L | H | H | L |
| L | L | H | L | L | H | L | H | H | L |
| H | L | H | L | H | H | L | L | L | H |
| L | H | H | L | H | H | L | L | L | H |
| H | H | H | L | L | L | H | H | L | H |
| L | L | L | H | L | H | L | H | H | L |
| H | L | L | H | H | H | L | L | L | H |
| L | H | L | H | H | H | L | L | L | H |
| H | H | L | H | L | L | H | H | L | H |
| L | L | H | H | L | L | H | H | L | H |
| H | L | H | H | H | L | H | L | H | H |
| L | H | H | H | H | L | H | L | H | H |
| H | H | H | H | L | H | H | H | H | H |

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F283 ..... −55°C to 125°C
SN74F283 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F283 | | | SN74F283 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F283 | | | SN74F283 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | Any A or B | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1.2 | | | −1.2 | mA |
| | C0 | | | | | −0.6 | | | −0.6 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 4.5 V | | 36 | 55 | | 36 | 55 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

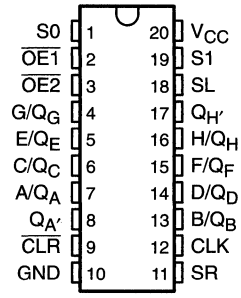
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F283 | | | SN54F283 | | SN74F283 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | C0 | Σ | 2.7 | 6.6 | 9.5 | 2.7 | 14 | 2.7 | 10.5 | ns |
| $t_{PHL}$ | | | 3.2 | 6.6 | 9.5 | 3.2 | 14 | 3.2 | 10.5 | |
| $t_{PLH}$ | A or B | Σ | 3.2 | 6.6 | 9.5 | 3.2 | 14 | 3.2 | 10.5 | ns |
| $t_{PHL}$ | | | 2.7 | 6.6 | 9.5 | 2.7 | 14 | 2.7 | 10.5 | |
| $t_{PLH}$ | C0 | C4 | 2.7 | 5.3 | 7.5 | 2.7 | 10.5 | 2.7 | 8.5 | ns |
| $t_{PHL}$ | | | 2.2 | 5 | 7 | 2.2 | 10 | 2.2 | 8 | |
| $t_{PLH}$ | A or B | C4 | 2.7 | 5.3 | 7.5 | 2.7 | 10.5 | 2.7 | 8.5 | ns |
| $t_{PHL}$ | | | 2.2 | 4.9 | 7 | 2.2 | 10 | 2.2 | 8 | |

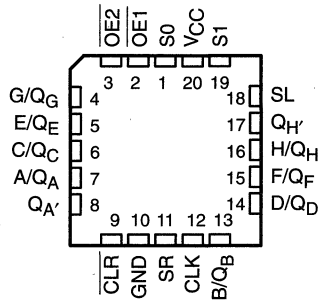
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Four Modes of Operation:**
  - **Hold (Store)**
  - **Shift Right**
  - **Shift Left**
  - **Load Data**
- **Operates With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - **Stacked or Push-Down Registers**
  - **Buffer Storage**
  - **Accumulator Registers**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F299 . . . J PACKAGE**
**SN74F299 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F299 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear ($\overline{CLR}$) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs but has no effect on clearing, shifting, or storage of data.

The SN54F299 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F299 is characterized for operation from 0°C to 70°C.

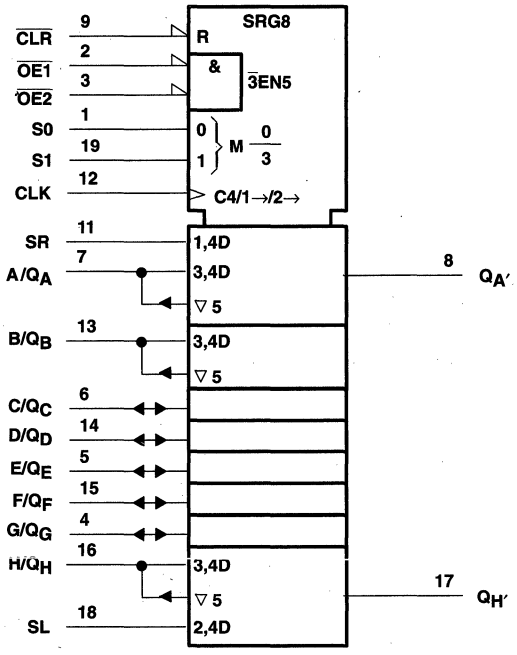
**FUNCTION TABLE**

| MODE | INPUTS | | | | | | | | I/O PORTS | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | S1 | S0 | $\overline{OE1}$† | $\overline{OE2}$† | CLK | SL | SR | A/$Q_A$ | B/$Q_B$ | C/$Q_C$ | D/$Q_D$ | E/$Q_E$ | F/$Q_F$ | G/$Q_G$ | H/$Q_H$ | $Q_{A'}$ | $Q_{H'}$ |
| Clear | L | X | L | L | L | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | L | X | L | L | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | H | H | X | X | X | X | X | X | X | X | X | X | X | X | X | L | L |
| Hold | H | L | L | L | L | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| | H | X | X | L | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | H | $Q_{Gn}$ |
| | H | L | H | L | L | ↑ | X | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | L | $Q_{Gn}$ |
| Shift Left | H | H | L | L | L | ↑ | H | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | H | $Q_{Bn}$ | H |
| | H | H | L | L | L | ↑ | L | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | L | $Q_{Bn}$ | L |
| Load | H | H | H | X | X | ↑ | X | X | a | b | c | d | e | f | g | h | a | h |

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

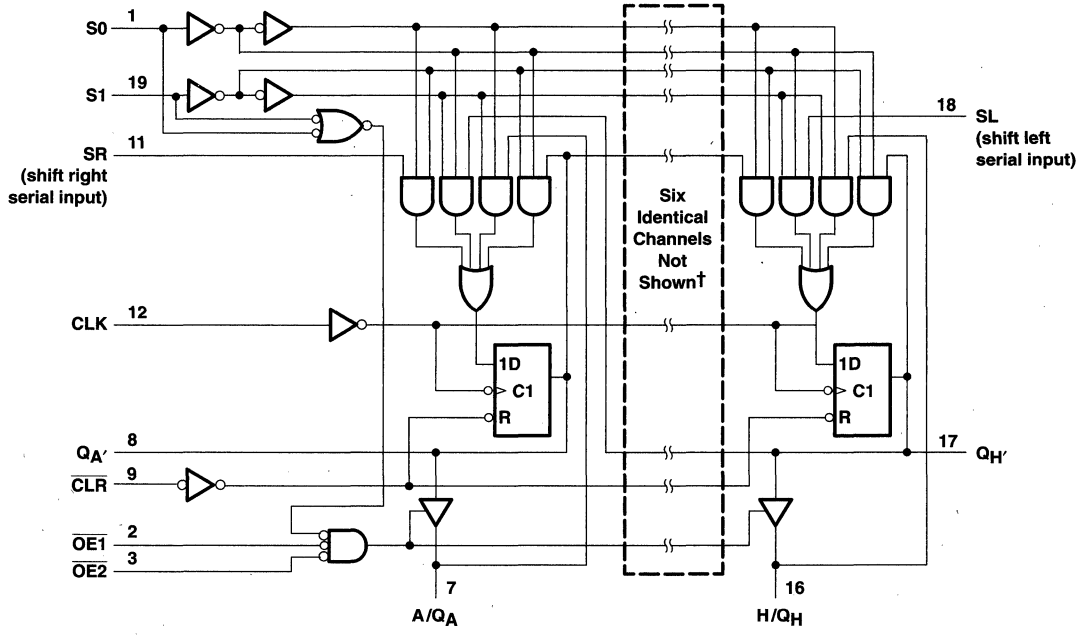
† When one or both output-enable inputs are high the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

## logic symbol‡




‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




† I/O ports not shown: B/$Q_B$ (13), C/$Q_C$ (6), D/$Q_D$ (14), E/$Q_E$ (5), F/$Q_F$ (15), and G/$Q_G$ (4).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | −0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | | −1.2 V to 7 V |
| Input current range | | −30 mA to 5 mA |
| Voltage range applied to any output in the disabled or power-off state | | −0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | | −0.5 V to $V_{CC}$ |
| Current into any output in the low state: | $Q_{A'}$ or $Q_{H'}$ | 40 mA |
| | SN54F299 ($Q_A$ thru $Q_H$) | 40 mA |
| | SN74F299 ($Q_A$ thru $Q_H$) | 48 mA |
| Operating free-air temperature range: | SN54F299 | −55°C to 125°C |
| | SN74F299 | 0°C to 70°C |
| Storage temperature range | | −65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | | SN54F299 | | | SN74F299 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | $Q_{A'}$ or $Q_{H'}$ | | | −1 | | | −1 | mA |
| | | $Q_A$ thru $Q_H$ | | | −3 | | | −3 | |
| $I_{OL}$ | Low-level output current | $Q_{A'}$ or $Q_{H'}$ | | | 20 | | | 20 | mA |
| | | $Q_A$ thru $Q_H$ | | | 20 | | | 24 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F299 | | | SN74F299 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $Q_A$ thru $Q_H$ | | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | Any output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| | $Q_A$ thru $Q_H$ | | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | A thru H | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | Any other | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$‡ | A thru H | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | µA |
| | Any other | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | A thru H | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.65 | | | −0.65 | mA |
| | S0 or S1 | | | | | −1.2 | | | −1.2 | |
| | Any other | | | | | −0.6 | | | −0.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 68 | 95 | | 68 | 95 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports ($Q_A$ thru $Q_H$), the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with $\overline{OE1}$, $\overline{OE2}$, and CLK at 4.5 V.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F299 | | SN74F299 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 'F299 | | | | | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 0 | 70 | 0 | 65 | 0 | 70 | MHz |
| $t_w$ | Pulse duration | CLK high or low | | 7 | | 8 | | 7 | | ns |
| | | $\overline{CLR}$ low | | 7 | | 8 | | 7 | | |
| $t_{su}$ | Setup time before CLK↑ | S0 or S1 | High or low | 8.5 | | 9.5 | | 8.5 | | ns |
| | | $A/Q_A$ thru $H/Q_H$, SR, or SL | High or low | 5.5 | | 6.5 | | 5.5 | | |
| | Inactive-state setup time before CLK↑† | $\overline{CLR}$ | High | 7 | | 13 | | 7 | | |
| $t_h$ | Hold time after CLK↑ | S0 or S1 | High or low | 0 | | 0 | | 0 | | ns |
| | | $A/Q_A$ thru $H/Q_H$, SR, or SL | High or low | 2 | | 2 | | 2 | | |

† Inactive-state setup time is also referred to as recovery time.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX‡ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F299 | | | SN54F299 | | SN74F299 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 70 | 100 | | 65 | | 70 | | MHz |
| $t_{PLH}$ | CLK | $Q_{A'}$ or $Q_{H'}$ | 3.2 | 6.6 | 9 | 2.7 | 10.5 | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 2.7 | 6.1 | 8.5 | 2.2 | 10 | 2.7 | 9.5 | |
| $t_{PLH}$ | CLK | $Q_A$ thru $Q_H$ | 3.2 | 6.6 | 9 | 2.7 | 11 | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 4.2 | 8.1 | 11 | 3.7 | 12.5 | 4.2 | 12 | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_{A'}$ or $Q_{H'}$ | 3.7 | 7.1 | 9.5 | 3.2 | 11.5 | 3.7 | 10.5 | ns |
| | | $Q_A$ thru $Q_H$ | 5.7 | 10.6 | 14 | 5 | 15.5 | 5.7 | 15 | |
| $t_{PZH}$ | $\overline{OE1}$ or $\overline{OE2}$ | $Q_A$ thru $Q_H$ | 2.7 | 5.6 | 8 | 2.2 | 10.5 | 2.7 | 9 | ns |
| $t_{PZL}$ | | | 3.2 | 6.6 | 10 | 2.7 | 12 | 3.2 | 11 | |
| $t_{PHZ}$ | $\overline{OE1}$ or $\overline{OE2}$ | $Q_A$ thru $Q_H$ | 1.7 | 4.1 | 6 | 1.7 | 9 | 1.7 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.6 | 5.5 | 1.2 | 7.5 | 1.2 | 6.5 | |

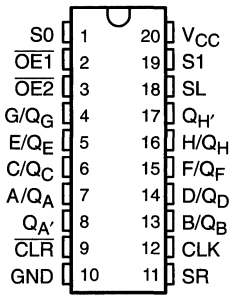
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

# SN74F323
# 8-BIT UNIVERSAL SHIFT-STORAGE REGISTER WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

SDFS072A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Four Modes of Operation:**
  - **Hold (Store)**
  - **Shift Right**
  - **Shift Left**
  - **Load Data**
- **Operates With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Synchronous Clear**
- **Applications:**
  - **Stacked or Push-Down Registers**
  - **Buffer Storage**
  - **Accumulator Registers**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

This 8-bit universal register features multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs synchronously when the clear ($\overline{CLR}$) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs but this has no effect on clearing, shifting, or storage of data.

The SN74F323 is characterized for operation from 0°C to 70°C.

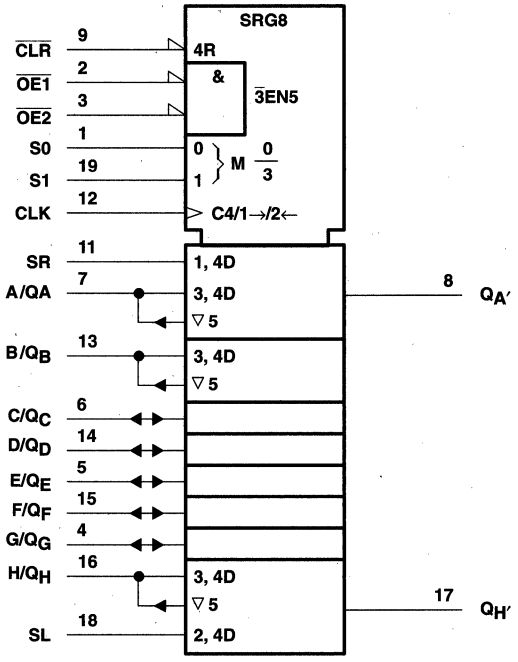
**FUNCTION TABLE**

| MODE | INPUTS | | | | | | | | I/O PORTS | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | S1 | S0 | $\overline{OE1}$† | $\overline{OE2}$† | CLK | SL | SR | $A/Q_A$ | $B/Q_B$ | $C/Q_C$ | $D/Q_D$ | $E/Q_E$ | $F/Q_F$ | $G/Q_G$ | $H/Q_H$ | $Q_{A'}$ | $Q_{H'}$ |
| Clear | L | X | L | L | L | ↑ | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | L | X | L | L | ↑ | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | H | H | X | X | ↑ | X | X | X | X | X | X | X | X | X | X | L | L |
| Hold | H | L | L | L | L | X | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| | H | X | X | L | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ | $Q_{F0}$ | $Q_{G0}$ | $Q_{H0}$ | $Q_{A0}$ | $Q_{H0}$ |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | H | $Q_{Gn}$ |
| | H | L | H | L | L | ↑ | X | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | L | $Q_{Gn}$ |
| Shift Left | H | H | L | L | L | ↑ | H | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | H | $Q_{Bn}$ | H |
| | H | H | L | L | L | ↑ | L | X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | $Q_{En}$ | $Q_{Fn}$ | $Q_{Gn}$ | $Q_{Hn}$ | L | $Q_{Bn}$ | L |
| Load | H | H | H | X | X | ↑ | X | X | a | b | c | d | e | f | g | h | a | h |

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. These data inputs are loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

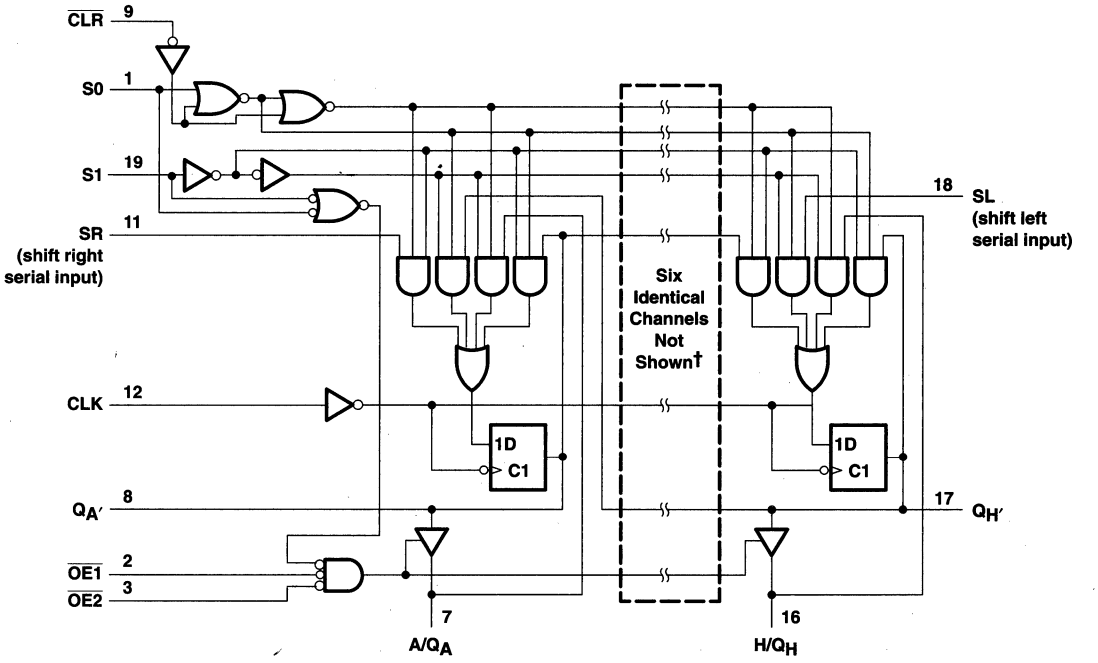
† When one or both output-enable inputs are high the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




† I/O ports not shown: B/$Q_B$ (13), C/$Q_C$ (6), D/$Q_D$ (14), E/$Q_E$ (5), F/$Q_F$ (15), and G/$Q_G$ (4).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: $Q_{A'}$ or $Q_{H'}$ ..... 40 mA
$Q_A$ thru $Q_H$ ..... 48 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | mA |
| $I_{OH}$ | High-level output current | $Q_{A'}$ or $Q_{H'}$ | | | −1 | mA |
| | | $Q_A$ thru $Q_H$ | | | −3 | |
| $I_{OL}$ | Low-level output current | $Q_{A'}$ or $Q_{H'}$ | | | 20 | mA |
| | | $Q_A$ thru $Q_H$ | | | 24 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | $Q_A$ thru $Q_H$ | | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | |
| | | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | |
| | Any output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | 2.7 | | | |
| $V_{OL}$ | $Q_{A'}$ or $Q_{H'}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| | $Q_A$ thru $Q_H$ | | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| $I_I$ | A thru H | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | mA |
| | Any other | | $V_I$ = 7 V | | | 0.1 | |
| $I_{IH}$‡ | A thru H | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | µA |
| | Any other | | | | | 20 | |
| $I_{IL}$‡ | A thru H | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.65 | mA |
| | S0 or S1 | | | | | −1.2 | |
| | Any other | | | | | −0.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 68 | 95 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports ($Q_A$ thru $Q_H$), the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with $\overline{OE1}$, $\overline{OE2}$, and CLK at 4.5 V.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 0 | 70 | 0 | 70 | MHz |
| $t_w$ | Pulse duration | CLK high or low | | 7 | | 7 | | ns |
| $t_{su}$ | Setup time before CLK↑ | S0 or S1 | High or low | 8.5 | | 8.5 | | ns |
| | | $A/Q_A$ thru $H/Q_H$, SR, or SL | High or low | 5 | | 5 | | |
| | | $\overline{CLR}$ | High or low | 10 | | 10 | | |
| $t_h$ | Hold time after CLK↑ | S0 or S1 | High or low | 0 | | 0 | | ns |
| | | $A/Q_A$ thru $H/Q_H$, SR, or SL | High or low | 2 | | 2 | | |
| | | $\overline{CLR}$ | High or low | 0 | | 0 | | |

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 70 | 100 | | 70 | | MHz |
| $t_{PLH}$ | CLK | $Q_{A'}$ or $Q_{H'}$ | 3.2 | 6.6 | 9 | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 2.7 | 6.1 | 8.5 | 2.7 | 9.5 | |
| $t_{PLH}$ | CLK | $Q_A$ thru $Q_H$ | 3.2 | 6.6 | 9 | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 4.2 | 8.1 | 11 | 4.2 | 12 | |
| $t_{PZH}$ | $\overline{OE1}$ or $\overline{OE2}$ | $Q_A$ thru $Q_H$ | 2.7 | 5.6 | 8 | 2.7 | 9 | ns |
| $t_{PZL}$ | | | 3.2 | 6.6 | 10 | 3.2 | 11 | |
| $t_{PHZ}$ | $\overline{OE1}$ or $\overline{OE2}$ | $Q_A$ thru $Q_H$ | 1.7 | 4.1 | 6 | 1.7 | 7 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.6 | 5.5 | 1.2 | 6.5 | |

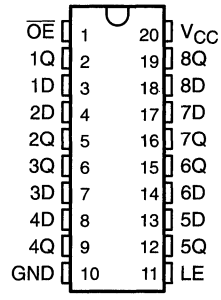
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

# SN54F373, SN74F373
# OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

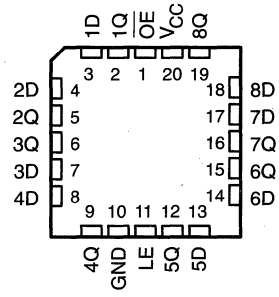
SDFS076A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Eight Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

**SN54F373 . . . J PACKAGE**
**SN74F373 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**




**SN54F373 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'F373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74F373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F373 is characterized for operation from 0°C to 70°C.

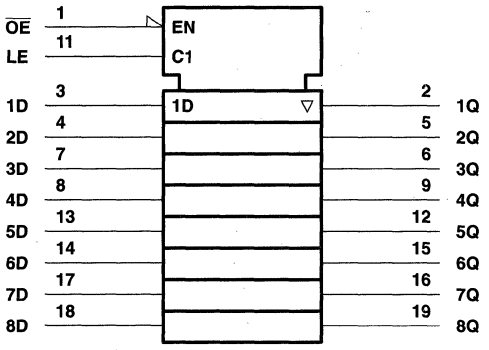
**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |



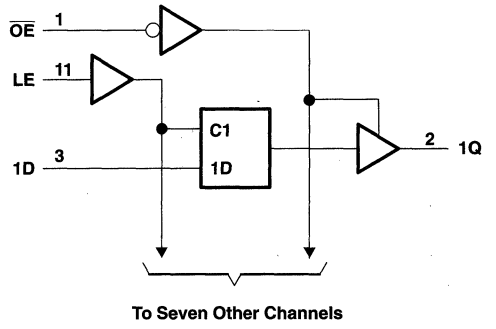
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F373 ..... 40 mA
SN74F373 ..... 48 mA
Operating free-air temperature range: SN54F373 ..... −55°C to 125°C
SN74F373 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F373 | | | SN74F373 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F373 | | | SN74F373 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = − 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = − 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = − 1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | − 0.6 | | | − 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 38 | 55 | | 38 | 55 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCZ}$ is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F373 | | SN74F373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | 'F373 | | | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 6 | | 6 | | 6 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 2 | | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | 3 | | 3 | | 3 | | ns |

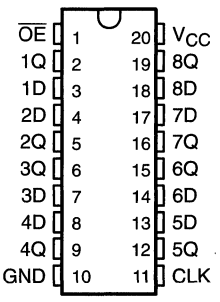
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F373 | | | SN54F373 | | SN74F373 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 2.2 | 4.9 | 7 | 2.2 | 8.5 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 1.2 | 3.3 | 5 | 1.2 | 7 | 1.2 | 6 | |
| $t_{PLH}$ | LE | Q | 4.2 | 8.6 | 11.5 | 4.2 | 15 | 4.2 | 13 | ns |
| $t_{PHL}$ | | | 2.2 | 4.8 | 7 | 2.2 | 8.5 | 2.2 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 1.2 | 4.6 | 11 | 1.2 | 13.5 | 1.2 | 12 | ns |
| $t_{PZL}$ | | | 1.2 | 5.2 | 7.5 | 1.2 | 10 | 1.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1.2 | 4.1 | 6.5 | 1.2 | 10 | 1.2 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.4 | 6 | 1.2 | 7 | 1.2 | 6 | |

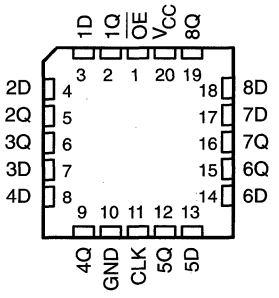
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

**SN54F374 . . . J PACKAGE**
**SN74F374 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**




**SN54F374 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'F374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

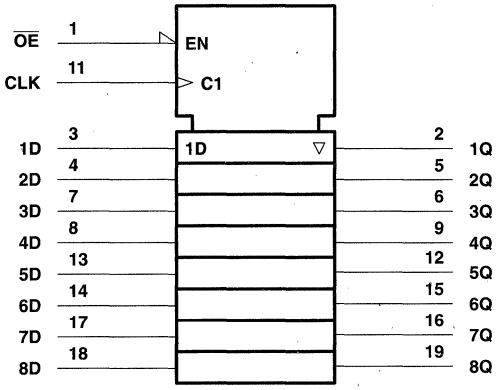
The SN74F374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F374 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

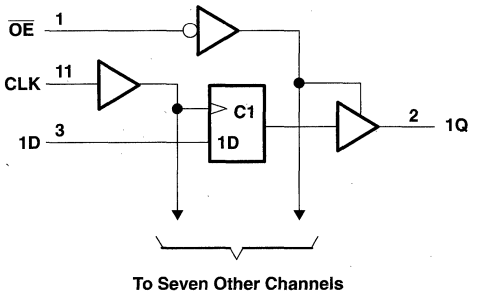
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F374 ..... 40 mA
SN74F374 ..... 48 mA
Operating free-air temperature range: SN54F374 ..... −55°C to 125°C
SN74F374 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F374 | | | SN74F374 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F374 | | | SN74F374 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to –3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | | –50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –60 | | –150 | –60 | | –150 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 55 | 86 | | 55 | 86 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCZ}$ is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F374 | | SN74F374 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 'F374 | | | | | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 60 | 0 | 70 | MHz |
| $t_w$ | Pulse duration | CLK high | 7 | | 7 | | 7 | | ns |
| | | CLK low | 6 | | 6 | | 6 | | |
| $t_{su}$ | Setup time, data before CLK↑ | High | 2 | | 2.5 | | 2 | | ns |
| | | Low | 2 | | 2 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | High | 2 | | 2 | | 2 | | ns |
| | | Low | 2 | | 2.5 | | 2 | | |

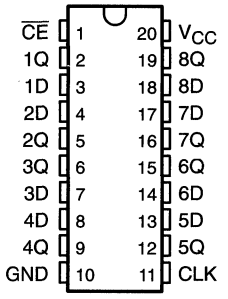
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F374 | | | SN54F374 | | SN74F374 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | | | 60 | | 70 | | MHz |
| $t_{PLH}$ | CLK | Q | 3.2 | 6.1 | 8.5 | 3.2 | 10.5 | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 3.2 | 6.1 | 8.5 | 3.2 | 11 | 3.2 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 1.2 | 8.6 | 11.5 | 1.2 | 14 | 1.2 | 12.5 | ns |
| $t_{PZL}$ | | | 1.2 | 5.4 | 7.5 | 1.2 | 10 | 1.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1.2 | 4.9 | 7 | 1.2 | 8 | 1.2 | 8 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.9 | 5.5 | 1.2 | 7.5 | 1.2 | 6.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Contains Eight D-Type Flip-Flops With Single-Rail Outputs**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Buffered Common Enable Input**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

The SN74F377A is a monolithic, positive-edge-triggered, octal, D-type flip-flop with clock enable inputs. The SN74F377A features a latched clock enable ($\overline{CE}$) input.

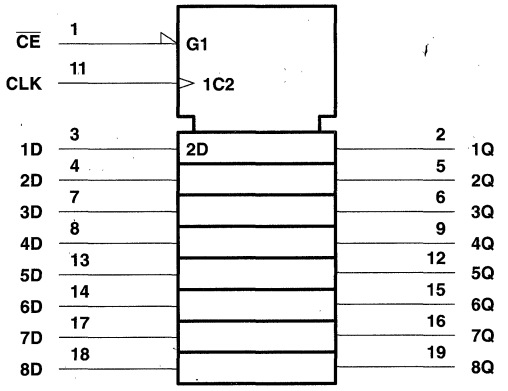
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{CE}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{CE}$ input.

The SN74F377A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

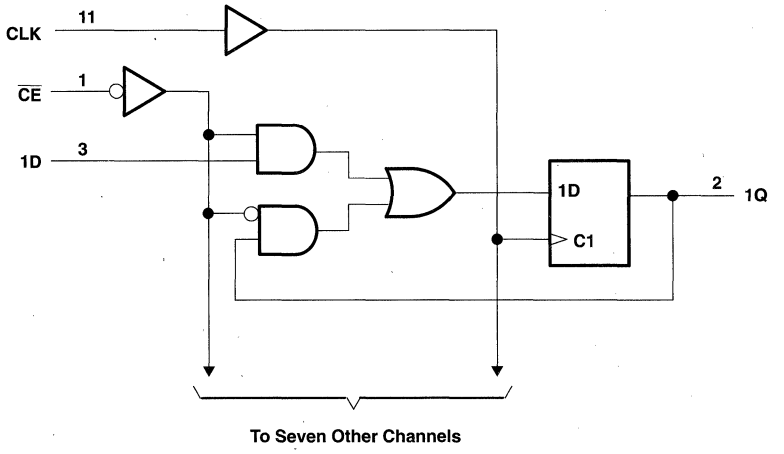
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CE}$ | CLK | D | Q |
| H | X | X | $Q_0$ |
| L | ↑ | H | H |
| L | ↑ | L | L |
| X | L | X | $Q_0$ |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | – 18 | mA |
| $I_{OH}$ | High-level output current | | | – 1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | – 60 | | – 150 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 55 | 72 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | See Note 3 | | 70 | 90 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTES: 2. $I_{CCH}$ is measured after applying a momentary ground, then 4.5 V, to the clock input with all data inputs at 4.5 V and the enable input at GND.
3. $I_{CCL}$ is measured after applying a momentary ground, then 4.5 V, to the clock input with all data and enable inputs at GND.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 110 | 0 | 110 | MHz |
| $t_w$ | Pulse duration | | 4 | | 5 | | ns |
| $t_{su}$ | Setup time before CLK↑ | Data high or low | 2 | | 2 | | ns |
| | | $\overline{CE}$ high | 2.5 | | 2.5 | | |
| | | $\overline{CE}$ low | 4 | | 4.5 | | |
| $t_h$ | Hold time after CLK↑ | Data high or low | 1 | | 1 | | ns |
| | | $\overline{CE}$ high or low | 0 | | 0 | | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

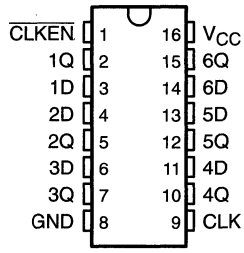
## switching characteristics (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 110 | 125 | | 110 | | MHz |
| $t_{PLH}$ | CLK | Any Q | 4 | 6.5 | 8.5 | 4 | 10 | ns |
| $t_{PHL}$ | | | 4 | 7 | 9 | 4 | 10.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 4: Load circuit and waveforms are shown in Section 1.

- **Contains Six D-Type Flip-Flops With Single-Rail Outputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Buffered Common Enable Input**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**D OR N PACKAGE**
**(TOP VIEW)**




## description

The SN74F378 is a positive-edge-triggered D-type flip-flop with a clock enable ($\overline{\text{CLKEN}}$) input. The SN74F378 is similar to the SN74F174 but features a common clock enable instead of a common clear.

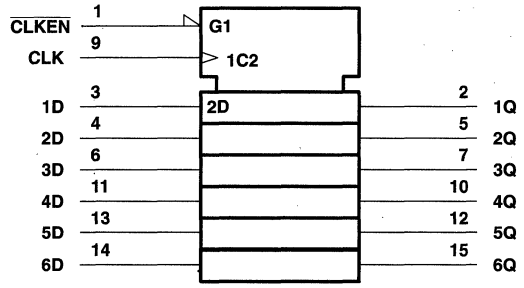
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74F378 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

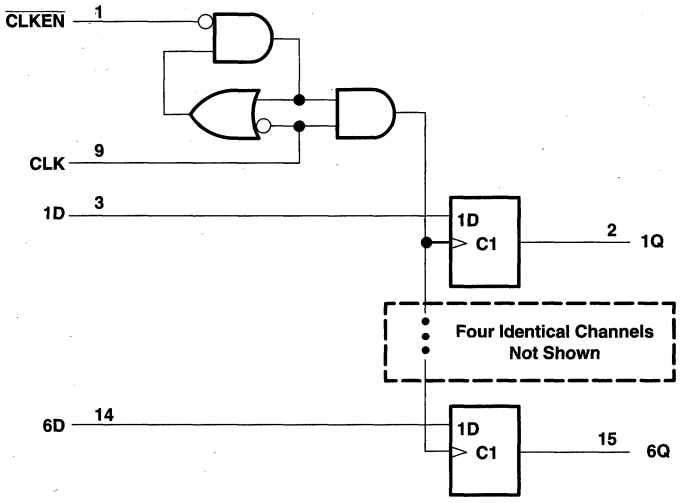
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{\text{CLKEN}}$ | CLK | D | Q |
| H | X | X | $Q_0$ |
| L | ↑ | H | H |
| L | ↑ | L | L |
| X | L | X | $Q_0$ |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | – 60 | | – 150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 30 | 45 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with all outputs open, all data inputs and the enable input grounded, and the clock input at 4.5 V after being momentarily grounded.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 110 | 0 | 110 | MHz |
| $t_w$ | Pulse duration | CLK high | 4 | | 4 | | ns |
| | | CLK low | 6 | | 6 | | |
| $t_{su}$ | Setup time before CLK↑ | Data high or low | 5 | | 5 | | ns |
| | | $\overline{\text{CLKEN}}$ high | 3.5 | | 3.5 | | |
| | | $\overline{\text{CLKEN}}$ low | 5 | | 5 | | |
| $t_h$ | Hold time after CLK↑ | Data high or low | 1 | | 1 | | ns |
| | | $\overline{\text{CLKEN}}$ high or low | 0 | | 0 | | |

## switching characteristics (see Note 3)

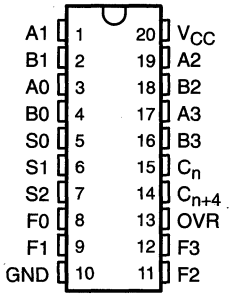
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 110 | 125 | | 110 | | MHz |
| $t_{PLH}$ | CLK | Any Q | 3.3 | 4.5 | 6.1 | 3.1 | 6.7 | ns |
| $t_{PHL}$ | | | 3 | 4.2 | 6 | 2.9 | 6.1 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

SDFS079A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Fully Parallel 4-Bit ALU in 20-Pin Package**
- **Ideally Suited for High-Density Economical Processors**
- **Ripple-Carry ($C_{n+4}$) and Overflow (OVR) Outputs**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**
  - **A Minus B**
  - **B Minus A**
  - **A Plus B**
  - **Five Other Functions**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

The SN74F382 is an arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, and OR functions of the two Boolean variables are provided without the use of external circuits. In addition, the outputs can be cleared (low) or preset (high) as desired. The device provides a ripple-carry ($C_{n+4}$) output to ripple the carry to the $C_n$ input of the next stage. It detects and indicates the two's complement overflow condition via the overflow (OVR) output. OVR is logically equivalent to $C_{n+3} \oplus C_{n+4}$. When the SN74F382 is cascaded to handle word lengths longer than four bits in length, only the most significant OVR is used.

The SN74F382 is characterized for operation from 0°C to 70°C.

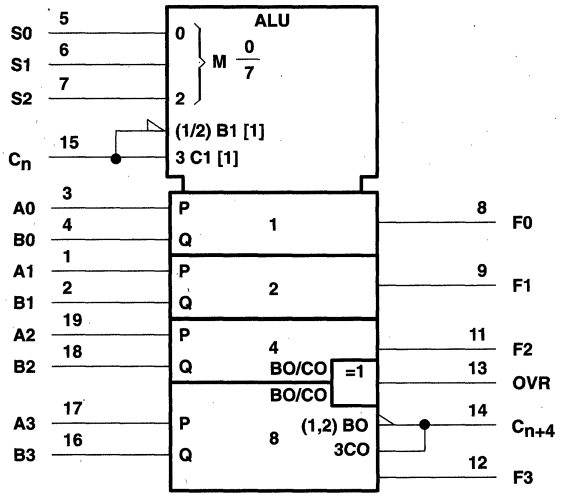
**FUNCTION TABLE**

| SELECTION | | | ARITHMETIC/LOGIC OPERATION |
|---|---|---|---|
| S2 | S1 | S0 | |
| L | L | L | Clear |
| L | L | H | B minus A |
| L | H | L | A minus B |
| L | H | H | A plus B |
| H | L | L | A ⊕ B |
| H | L | H | A + B |
| H | H | L | AB |
| H | H | H | Preset |

**PIN DESIGNATIONS**

| DESIGNATION | PIN NO. | FUNCTION |
|---|---|---|
| A3, A2, A1, A0 | 17, 19, 1, 3 | Word A inputs |
| B3, B2, B1, B0 | 16, 18, 2, 4 | Word B inputs |
| S2, S1, S0 | 7, 6, 5 | Function-select inputs |
| $C_n$ | 15 | Carry input for addition, inverted carry input for subtraction |
| F3, F2, F1, F0 | 12, 11, 9, 8 | Function outputs |
| $C_{n+4}$ | 14 | Ripple-carry output |
| OVR | 13 | Overflow output |
| $V_{CC}$ | 20 | Supply voltage |
| GND | 10 | Ground |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## function table

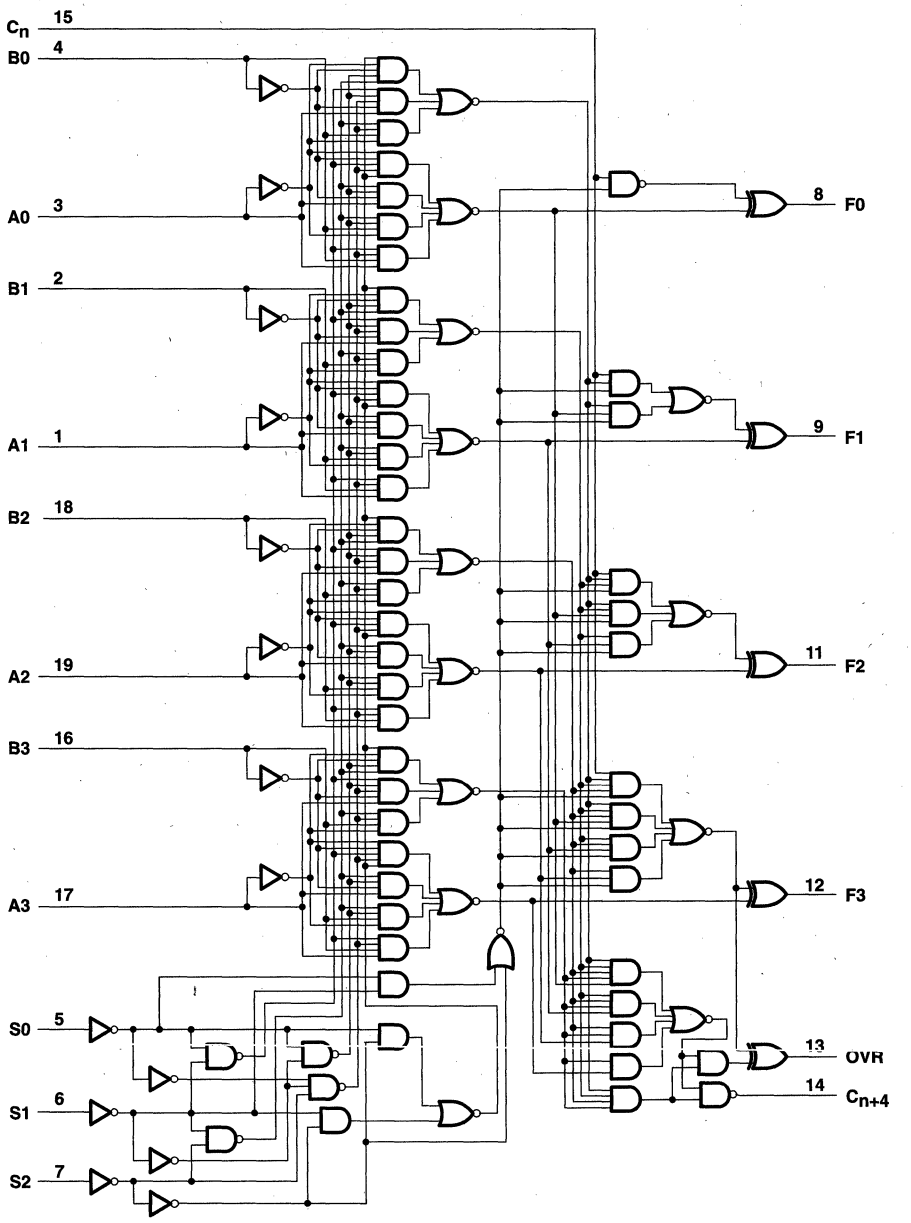
Certain differences exist in the OVR and $C_{n+4}$ function table compared with similar parts from other technologies and other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B) where these outputs perform valuable cascade functions. There are slight differences in the other modes (clear, A + B, A ⊕ B, AB, and preset), in which these outputs strictly *don't care*.

The following function table is a condensed version and assumes for $A_n$ that A0, A1, A2, and A3 inputs all agree, and for $B_n$ that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these OVR and $C_{n+4}$ outputs in all modes of operation to facilitate incoming inspection.

**FUNCTION TABLE**

| ARITHMETIC/LOGIC OPERATION | INPUTS | | | | | | OUTPUTS | | | | OVR | $C_{n+4}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | S2 | S1 | S0 | $C_n$ | $A_n$ | $B_n$ | F3 | F2 | F1 | F0 | | |
| Clear | L | L | L | X | X | X | L | L | L | L | H | H |
| B minus A | L | L | H | L | L | L | H | H | H | H | L | L |
| | | | | L | L | H | H | H | H | L | L | H |
| | | | | L | H | L | L | L | L | L | L | L |
| | | | | L | H | H | H | H | H | H | L | L |
| | | | | H | L | L | L | L | L | L | L | H |
| | | | | H | L | H | H | H | H | H | L | H |
| | | | | H | H | L | L | L | L | H | L | L |
| | | | | H | H | H | L | L | L | L | L | H |
| A minus B | L | H | L | L | L | L | H | H | H | H | L | L |
| | | | | L | L | H | L | L | L | L | L | L |
| | | | | L | H | L | H | H | H | L | L | H |
| | | | | L | H | H | H | H | H | H | L | L |
| | | | | H | L | L | L | L | L | L | L | H |
| | | | | H | L | H | L | L | L | H | L | L |
| | | | | H | H | L | H | H | H | H | L | H |
| | | | | H | H | H | L | L | L | L | L | H |
| A plus B | L | H | H | L | L | L | L | L | L | L | L | L |
| | | | | L | L | H | H | H | H | H | L | L |
| | | | | L | H | L | H | H | H | H | L | L |
| | | | | L | H | H | H | H | H | L | L | H |
| | | | | H | L | L | L | L | L | H | L | L |
| | | | | H | L | H | L | L | L | L | L | H |
| | | | | H | H | L | L | L | L | L | L | H |
| | | | | H | H | H | H | H | H | H | L | H |
| A ⊕ B | H | L | L | X | L | L | L | L | L | L | L | L |
| | | | | X | L | H | H | H | H | H | L | L |
| | | | | L | H | L | H | H | H | H | L | L |
| | | | | H | H | L | H | H | H | H | H | H |
| | | | | X | H | H | L | L | L | L | H | H |
| A + B | H | L | H | X | L | L | L | L | L | L | L | L |
| | | | | X | L | H | H | H | H | H | L | L |
| | | | | X | H | L | H | H | H | H | L | L |
| | | | | L | H | H | H | H | H | H | L | L |
| | | | | H | H | H | H | H | H | H | H | H |
| AB | H | H | L | X | L | L | L | L | L | L | H | H |
| | | | | X | L | H | L | L | L | L | L | L |
| | | | | X | H | L | L | L | L | L | H | H |
| | | | | L | H | H | H | H | H | H | L | L |
| | | | | H | H | H | H | H | H | H | H | H |
| Preset | H | H | H | X | L | L | H | H | H | H | L | L |
| | | | | X | L | H | H | H | H | H | L | L |
| | | | | X | H | L | H | H | H | H | L | L |
| | | | | L | H | H | H | H | H | H | L | L |
| | | | | H | H | H | H | H | H | H | H | H |

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . −0.5 V to $V_{CC}$
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | Any A or B | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −2.4 | mA |
| | Any S | | | | | −0.6 | |
| | $C_n$ | | | | | −3 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 54 | 81 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured with all outputs open, S0 and $C_n$ inputs at 4.5 V, and all other inputs grounded.

## switching characteristics (see Note 3)

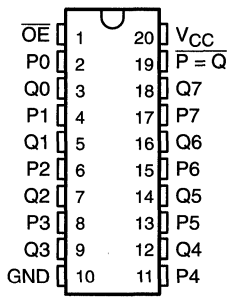
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | $C_n$ | Any F | 2.3 | 5.3 | 11 | 2.3 | 12 | ns |
| $t_{PHL}$ | | | 2.2 | 4.6 | 7.5 | 2.2 | 8.5 | |
| $t_{PLH}$ | Any A or B | Any F | 2.7 | 6.9 | 12 | 2.4 | 13 | ns |
| $t_{PHL}$ | | | 2.5 | 6.1 | 10 | 2.3 | 11 | |
| $t_{PLH}$ | S0, S1, S2 | Any F | 4.7 | 8.3 | 15 | 4.3 | 17 | ns |
| $t_{PHL}$ | | | 3.3 | 7.5 | 14 | 3.3 | 15 | |
| $t_{PLH}$ | Any A or B | $C_{n+4}$ | 3.3 | 6.6 | 10 | 3.3 | 11 | ns |
| $t_{PHL}$ | | | 3.4 | 6.3 | 10 | 3 | 10.5 | |
| $t_{PLH}$ | S0, S1, S2 | OVR or $C_{n+4}$ | 3.6 | 9.8 | 16.5 | 3 | 17.5 | ns |
| $t_{PHL}$ | | | 5 | 8.6 | 13 | 4.6 | 14 | |
| $t_{PLH}$ | $C_n$ | $C_{n+4}$ | 2.2 | 3.9 | 5.5 | 2 | 6.5 | ns |
| $t_{PHL}$ | | | 3 | 4.8 | 6.5 | 2.6 | 7.5 | |
| $t_{PLH}$ | $C_n$ | OVR | 3.3 | 7 | 11 | 3 | 12.5 | ns |
| $t_{PHL}$ | | | 3 | 5 | 6.5 | 3 | 8 | |
| $t_{PLH}$ | Any A or B | OVR | 5.1 | 8.8 | 13 | 4.7 | 15 | ns |
| $t_{PHL}$ | | | 3.3 | 6.9 | 10.5 | 3.3 | 11.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

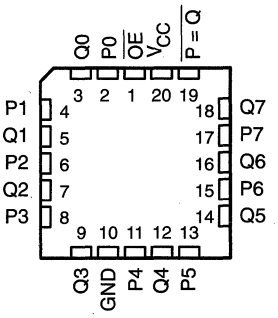
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Compares Two 8-Bit Words**
- **20-kΩ Pullup Resistors on Q Inputs**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F520 . . . J PACKAGE**
**SN74F520 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F520 . . . FK PACKAGE**
**(TOP VIEW)**




## description

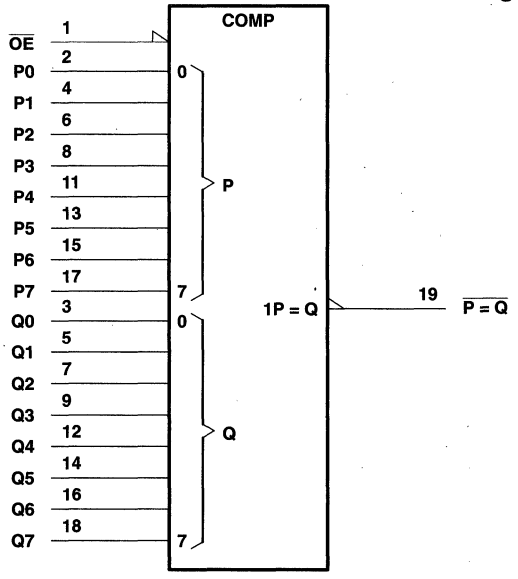
These identity comparators perform comparisons on two 8-bit binary or BCD words. They provide $\overline{P = Q}$ outputs. The 'F520 features 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

The SN54F520 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F520 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

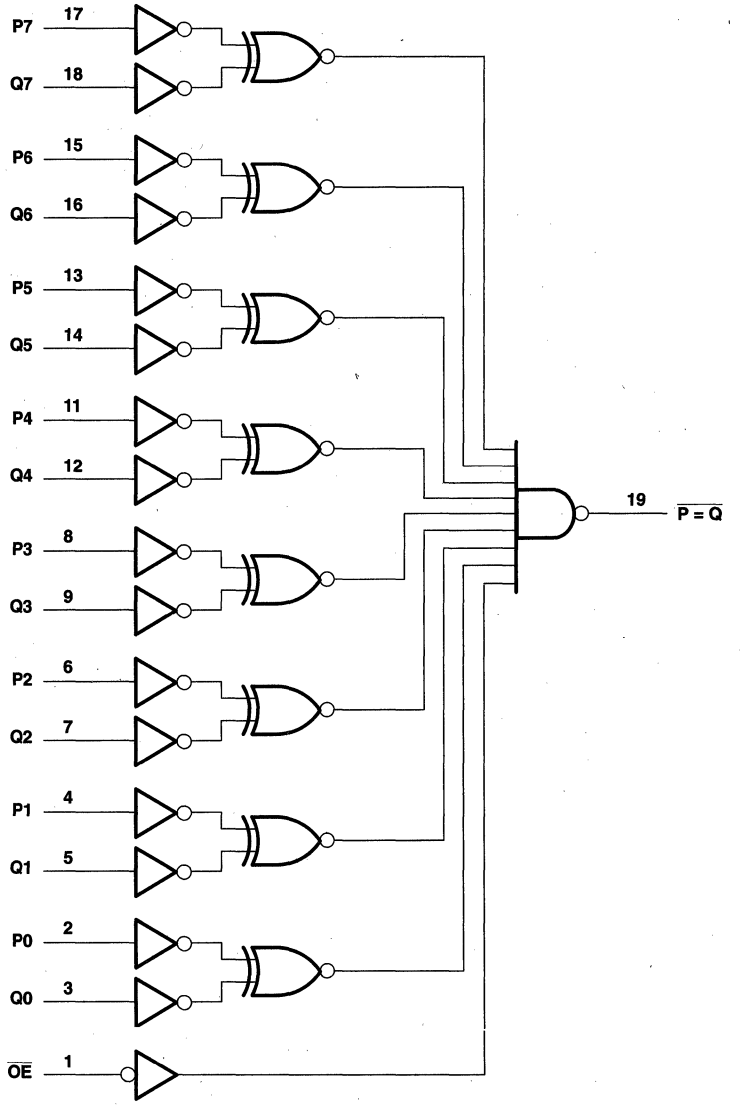
| INPUTS | | OUTPUT |
|---|---|---|
| P, Q | $\overline{OE}$ | $\overline{P = Q}$ |
| P = Q | L | L |
| P ≠ Q | X | H |
| X | H | H |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




NOTE: 20-kΩ pullup resistors are on the Q inputs.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F520 ..... −55°C to 125°C
SN74F520 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F520 | | | SN74F520 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F520 | | | SN74F520 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $\overline{OE}$ and P inputs | $V_{CC}$ = 5.5 V | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | Q inputs | | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | $\overline{OE}$ and P inputs | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| | Q inputs | | | | | −0.3 | | | −0.3 | mA |
| $I_{IL}$ | $\overline{OE}$ and P inputs | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| | Q inputs | | | | | −1 | | | −1 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | See Note 2 | | 21 | 32 | | 21 | 32 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured with all inputs at 4.5 V.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F520 | | | SN54F520 | | SN74F520 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | P or Q | $\overline{P = Q}$ | 3.9 | 5.7 | 7.7 | 3.7 | 10.2 | 3.7 | 8.7 | ns |
| $t_{PHL}$ | | | 4.7 | 7 | 9.3 | 4.4 | 11.3 | 4.4 | 10.3 | |
| $t_{PLH}$ | $\overline{OE}$ | $\overline{P = Q}$ | 3.5 | 4.6 | 5.8 | 3.4 | 7 | 3.4 | 6.4 | ns |
| $t_{PHL}$ | | | 5.2 | 7.5 | 9.5 | 4.9 | 11.2 | 4.9 | 10.4 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

SDFS091 – MARCH 1987 – REVISED OCTOBER 1993

- **Compares Two 8-Bit Words**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

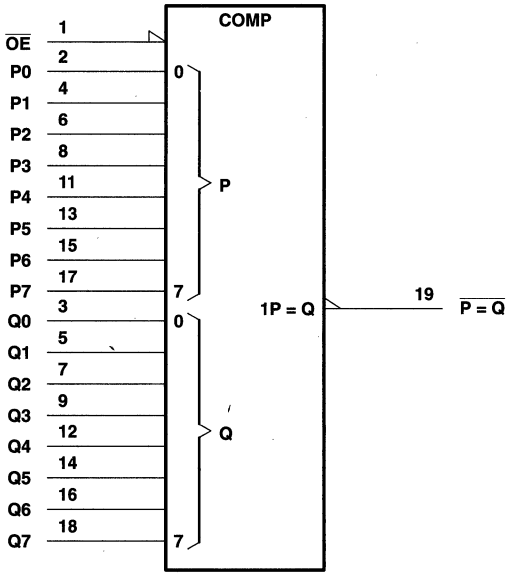
These identity comparators perform comparisons on two 8-bit binary or BCD words. They provide $\overline{P = Q}$ outputs.

The SN54F521 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F521 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

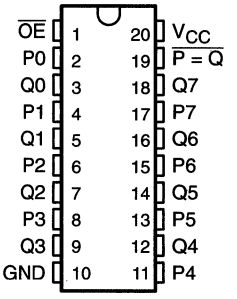
| INPUTS | | OUTPUT |
|---|---|---|
| P, Q | $\overline{OE}$ | $\overline{P = Q}$ |
| P = Q | L | L |
| P ≠ Q | X | H |
| X | H | H |

## logic symbol†

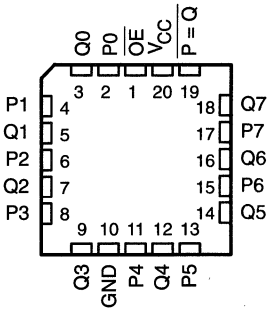



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

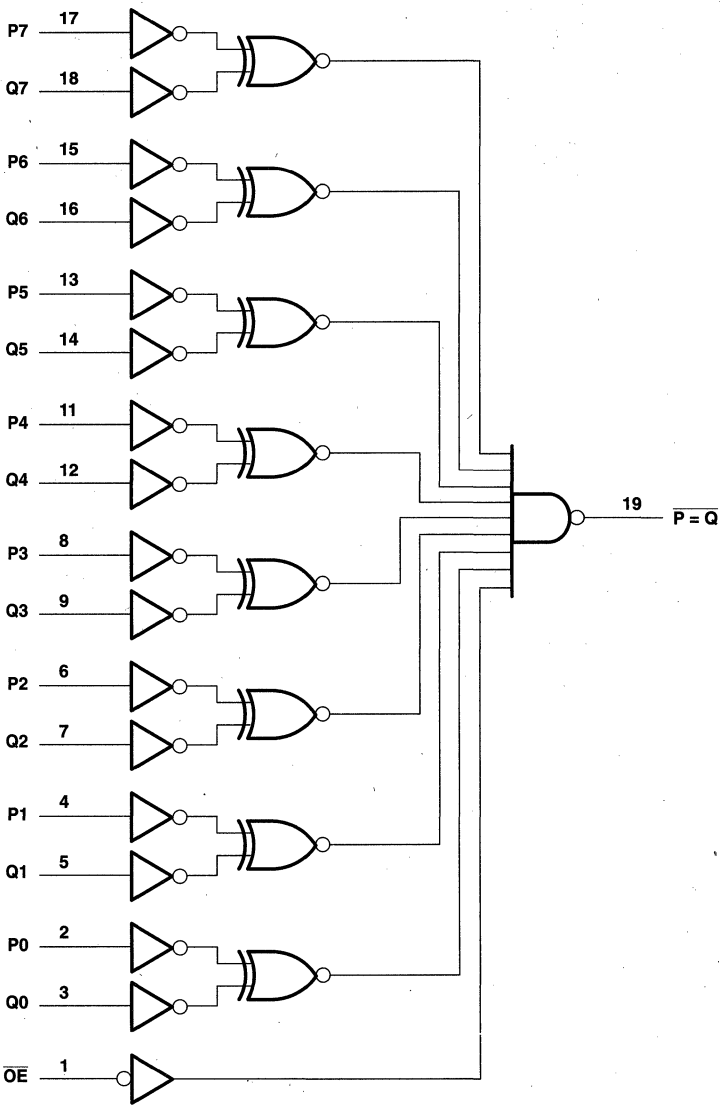
**SN54F521 . . . J PACKAGE**
**SN74F521 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F521 . . . FK PACKAGE**
**(TOP VIEW)**



## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 40 mA
Operating free-air temperature range: SN54F521 ..... −55°C to 125°C
SN74F521 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F521 | | | SN74F521 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F521 | | | SN74F521 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 100 | | | 100 | µA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 21 | 32 | | 21 | 32 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: $I_{CC}$ is measured with all inputs at 4.5 V.

## switching characteristics (see Note 3)

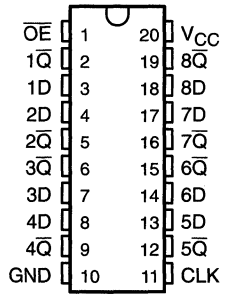
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F521 | | | SN54F521 | | SN74F521 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | P or Q | $\overline{P = Q}$ | 2.7 | 6.6 | 10 | 2.7 | 14 | 2.7 | 11 | ns |
| $t_{PHL}$ | | | 3.7 | 6.6 | 10 | 3.2 | 12 | 3.2 | 11 | |
| $t_{PLH}$ | $\overline{OE}$ | $\overline{P = Q}$ | 2.2 | 4.6 | 6.5 | 2.2 | 8.5 | 2.2 | 7.5 | ns |
| $t_{PHL}$ | | | 2.7 | 6.1 | 9 | 2.7 | 13.5 | 2.7 | 10 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

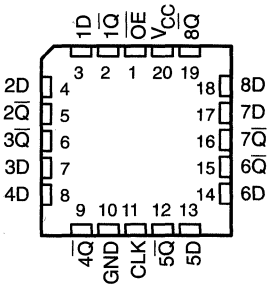
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **3-State Bus-Driving Inverting Outputs**
- **Buffered Control Inputs**
- **Package Options Incude Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F534A . . . J PACKAGE**
**SN74F534A . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F534A . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'F534A are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs are set to the complement of the logic states that were set up at the data (D) inputs. The 'F534A is equivalent to the 'F374 except for having inverted outputs.

A buffered output enable ($\overline{OE}$) control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

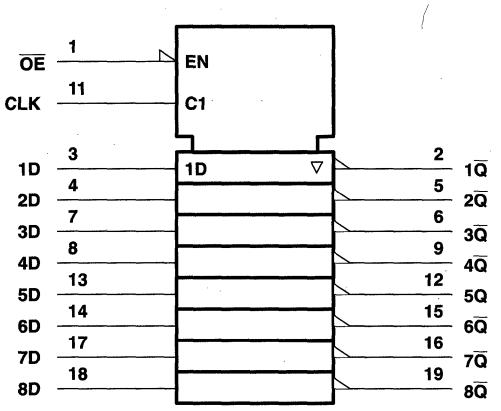
The output enable ($\overline{OE}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54F534A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F534A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

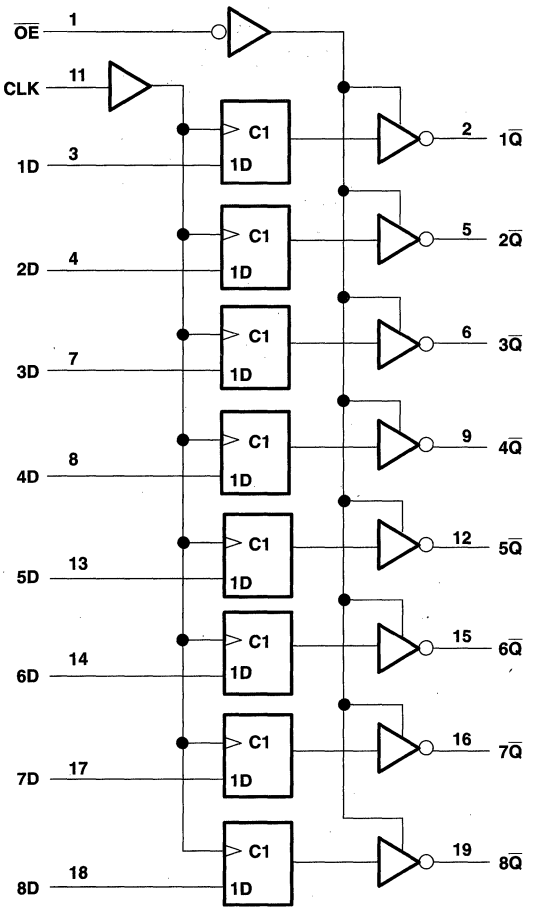
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | $\overline{Q}$ |
| L | ↑ | H | L |
| L | ↑ | L | H |
| L | L | X | $\overline{Q}_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range (see Note 1) ..... −1.2 V to 7 V
Input current ..... +20 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F534A ..... 40 mA
SN74F534A ..... 48 mA
Operating free-air temperature range: SN54F534A ..... −55°C to 125°C
SN74F534A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | SN54F534A | | | SN74F534A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | – 18 | | | – 18 | mA |
| $I_{OH}$ | High-level output current | | | – 3 | | | – 3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F534A | | | SN74F534A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | – 1.2 | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to – 3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | – 50 | | | – 50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | – 60 | | – 150 | – 60 | | – 150 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 55 | 86 | | 55 | 86 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCZ}$ is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 'F534A | | SN54F534A | | SN74F534A | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 60 | 0 | 70 | MHz |
| $t_w$ | Pulse duration | CLK high | 7 | | 7 | | 7 | | ns |
| | | CLK low | 6 | | 6 | | 6 | | |
| $t_{su}$ | Setup time before CLK↑ | Data high | 2 | | 2.5 | | 2 | | ns |
| | | Data low | 2 | | 2.5 | | 2 | | |
| $t_h$ | Hold time after CLK↑ | Data high | 2 | | 2 | | 2 | | ns |
| | | Data low | 2 | | 2.5 | | 2 | | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F534A | | | SN54F534A | | SN74F534A | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | | | 60 | | 70 | | MHz |
| $t_{PLH}$ | CLK | Any $\overline{Q}$ | 3 | 4.5 | 7 | 2.5 | 10.5 | 2.5 | 7.5 | ns |
| $t_{PHL}$ | | | 3 | 4.5 | 7 | 2.5 | 11 | 2.5 | 7.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Any $\overline{Q}$ | 1.2 | 4.5 | 7.5 | 1.2 | 14 | 1.2 | 8.5 | ns |
| $t_{PZL}$ | | | 1.2 | 5 | 7.5 | 1.2 | 10 | 1.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any $\overline{Q}$ | 1.2 | 3.5 | 6.5 | 1.2 | 8 | 1.2 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.5 | 5.5 | 1.2 | 7.5 | 1.2 | 6.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

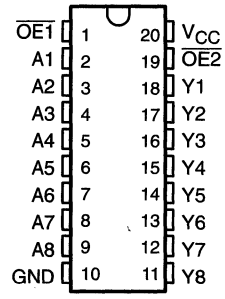
## description

The 'F541 octal buffer/line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

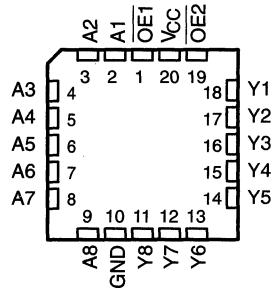
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

The SN54F541 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F251 is characterized for operation from 0°C to 70°C.

**SN54F541 . . . J PACKAGE**
**SN74F541 . . . DW OR N PACKAGE**
**(TOP VIEW)**



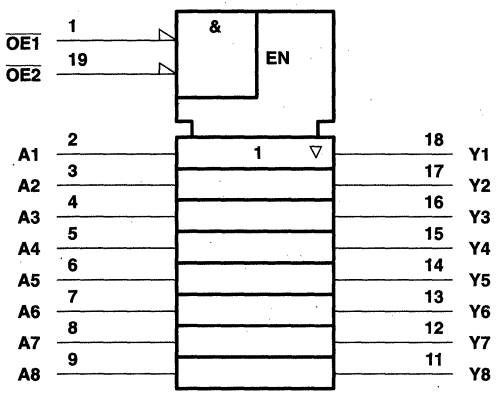

**SN54F541 . . . FK PACKAGE**
**(TOP VIEW)**




**FUNCTION TABLE**

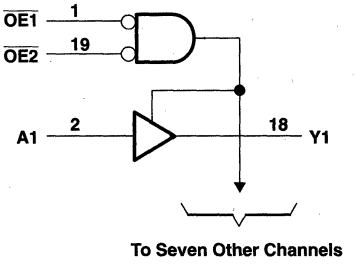
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F541 ..... 96 mA
SN74F541 ..... 128 mA
Operating free-air temperature range: SN54F541 ..... −55°C to 125°C
SN74F541 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F541 | | | SN74F541 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F541 | | | SN74F541 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = −12 mA | 2 | 3.2 | | | | | |
| | | $I_{OH}$ = −15 mA | | | | 2 | 3.1 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | V |
| | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | −100 | | −225 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 28 | 35 | | 28 | 35 | mA |
| | | Outputs low | | 62 | 75 | | 62 | 75 | |
| | | Outputs disabled | | 40 | 55 | | 40 | 55 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

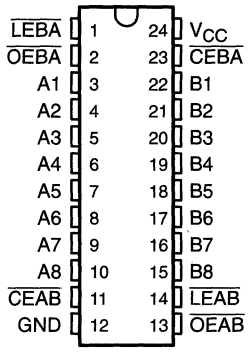
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F541 | | | SN54F541 | | SN74F541 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any A | Y | 1.5 | 3.3 | 5.5 | 1 | 6.5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 2.7 | 5.5 | 1 | 6.5 | 1.5 | 6 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 3 | 5.8 | 8 | 1.7 | 10 | 2.5 | 9.5 | ns |
| $t_{PZL}$ | | | 3.5 | 6.1 | 8.5 | 2.2 | 10 | 3 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.5 | 3.4 | 6 | 1 | 7 | 1.5 | 6.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 2.9 | 5.5 | 1 | 7.5 | 1.5 | 6 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic Small-Outline and Shrink Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DB, DW, OR NT PACKAGE**
**(TOP VIEW)**




## description

The SN74F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow. The A outputs are characterized to sink 24 mA while the B outputs are characterized to sink 64 mA.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The SN74F543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

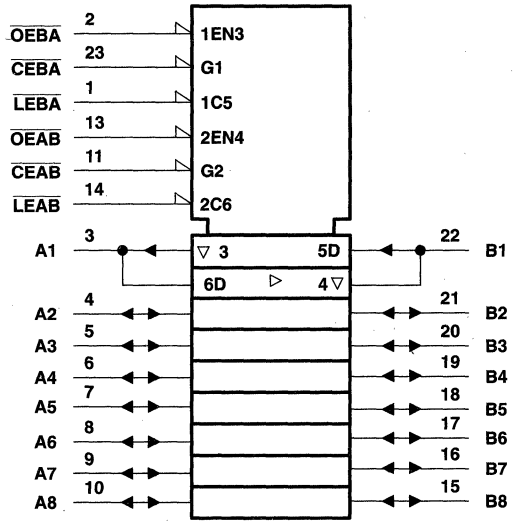
The SN74F543 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE†**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{CEAB}$ | $\overline{LEAB}$ | $\overline{OEAB}$ | A | B |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | $B_0$‡ |
| L | L | L | L | L |
| L | L | L | H | H |

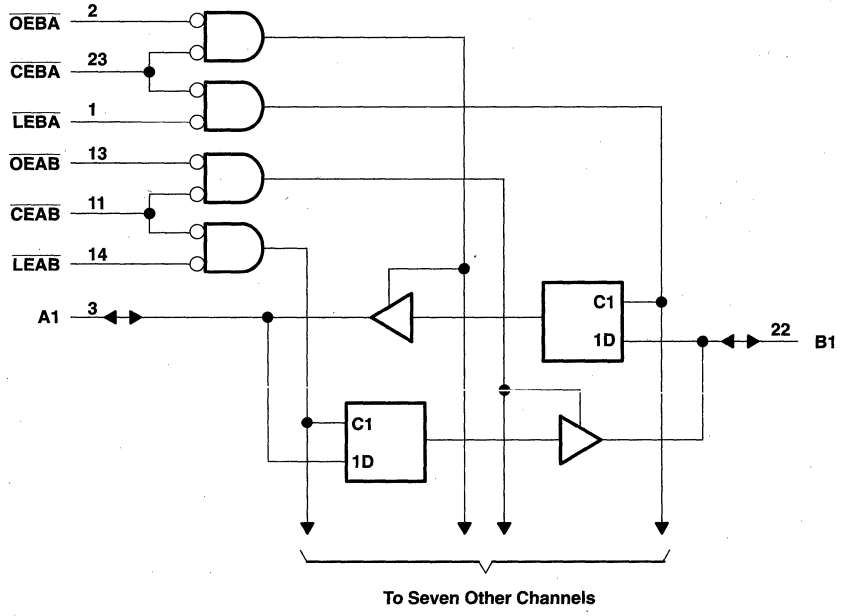
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (excluding I/O ports) (see Note 1) ..... −1.2 V to 7 V
Input current range, $I_{IK}$ ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: A1−A8 ..... 48 mA
B1−B8 ..... 128 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | mA |
| $I_{OH}$ | High-level output current | A1−A8 | | | −3 | mA |
| | | B1−B8 | | | −15 | |
| $I_{OL}$ | Low-level output current | A1−A8 | | | 24 | mA |
| | | B1−B8 | | | 64 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | –1.2 | V |
| $V_{OH}$ | A1–A8 | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | V |
| | | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | |
| | B1–B8 | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | |
| | | | $I_{OH}$ = – 15 mA | 2 | 3.1 | | |
| | Any output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to –3 mA | 2.7 | | | |
| $V_{OL}$ | A1–A8 | $V_{CC}$ = 4.5 V | $I_{OL}$ = 24 mA | | 0.3 | 0.5 | V |
| | B1–B8 | | $I_{OL}$ = 64 mA | | 0.42 | 0.55 | |
| $I_I$ | $\overline{OE}$, $\overline{LE}$, and $\overline{CE}$ | $V_{CC}$ = 5.5 V | $V_I$ = 7 V | | | 0.1 | mA |
| | A and B ports | | $V_I$ = 5.5 V | | | 1 | |
| $I_{IH}$‡ | $\overline{OE}$, $\overline{LE}$, and $\overline{CE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| | A and B ports | | | | | 70 | |
| $I_{IL}$‡ | $\overline{OE}$, $\overline{LE}$, and $\overline{CE}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | –1.2 | mA |
| | A and B ports | | | | | –0.65 | |
| $I_{OS}$§ | A1–A8 | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –60 | | –150 | mA |
| | B1–B8 | | | –100 | | –225 | |
| $I_{CCH}$ | | $V_{CC}$ = 5.5 V | | | 67 | 100 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5 V | | | 83 | 125 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5 V | | | 83 | 125 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX¶ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before latch enable | High or low | 3 | | 3.5 | | ns |
| $t_h$ | Hold time, data after latch enable | High or low | 3 | | 3.5 | | ns |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

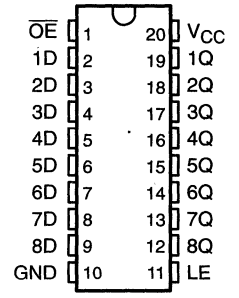
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 2.2 | 5.1 | 7.5 | 2.2 | 8.5 | ns |
| $t_{PHL}$ | | | 2.2 | 4.6 | 6.5 | 2.2 | 7.5 | |
| $t_{PLH}$ | $\overline{LEBA}$ | A | 3.7 | 8.1 | 11 | 4.1 | 12.5 | ns |
| $t_{PHL}$ | | | 3.7 | 8.1 | 11 | 4.1 | 12.5 | |
| $t_{PLH}$ | $\overline{LEAB}$ | B | 3.7 | 8.1 | 11 | 4.1 | 12.5 | ns |
| $t_{PHL}$ | | | 3.7 | 8.1 | 11 | 4.1 | 12.5 | |
| $t_{PZH}$ | $\overline{OE}$ or $\overline{CE}$ | A or B | 2.2 | 6.6 | 9 | 2.2 | 10 | ns |
| $t_{PZL}$ | | | 3.2 | 7.1 | 10.5 | 3.2 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ or $\overline{CE}$ | A or B | 1.7 | 5.6 | 8 | 1.7 | 9 | ns |
| $t_{PLZ}$ | | | 1.7 | 5.1 | 7.5 | 1.7 | 8.5 | |

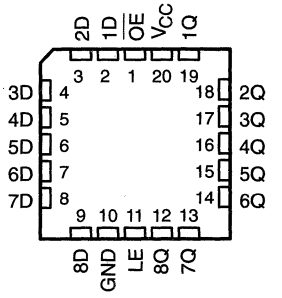
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Eight Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F573 . . . J PACKAGE**
**SN74F573 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F573 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'F573 are transparent D-type latches. While the latch enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

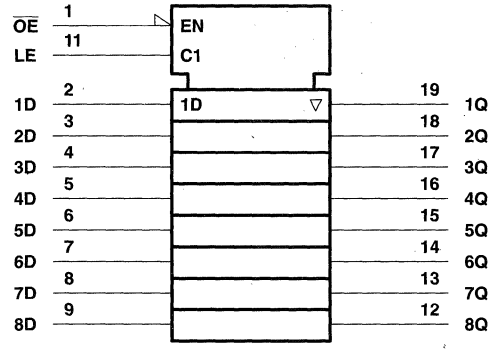
The output enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54F573 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F573 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each latch)**

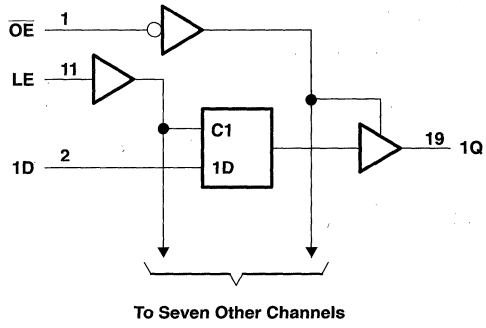
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F573 ..... 40 mA
SN74F573 ..... 48 mA
Operating free-air temperature range: SN54F573 ..... −55°C to 125°C
SN74F573 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F573 | | | SN74F573 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F573 | | | SN74F573 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = −3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −1 mA to −3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | −50 | | | −50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −0.6 | | | −0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 38 | 55 | | 38 | 55 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCZ}$ is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F573 | | SN74F573 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | 'F573 | | | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 6 | | 6 | | 6 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 2 | | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | 3 | | 3 | | 3 | | ns |

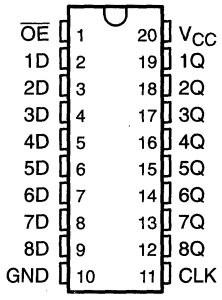
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F573 | | | SN54F573 | | SN74F573 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 2 | 4.9 | 7 | 1.5 | 9 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 1.2 | 3.3 | 5 | 1 | 8 | 1.2 | 6 | |
| $t_{PLH}$ | LE | Q | 4.2 | 8.6 | 11.5 | 3.7 | 13.5 | 4.2 | 13 | ns |
| $t_{PHL}$ | | | 2.2 | 4.8 | 7 | 1.5 | 9 | 2.2 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 1.2 | 4.6 | 11 | 1 | 13 | 1.2 | 12 | ns |
| $t_{PZL}$ | | | 1.2 | 5.2 | 7.5 | 1 | 10 | 1.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1.2 | 4.1 | 6.5 | 1 | 8.5 | 1.2 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.4 | 6 | 1 | 7 | 1.2 | 6 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

This 8-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SN74F574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs will be set to the logic levels that were set up at the data (D) inputs.

A buffered output enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

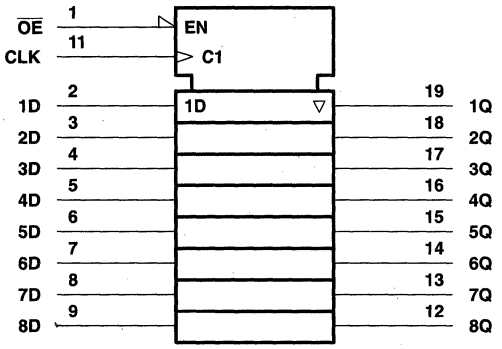
The output enable ($\overline{OE}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74F574 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each flip-flop)**

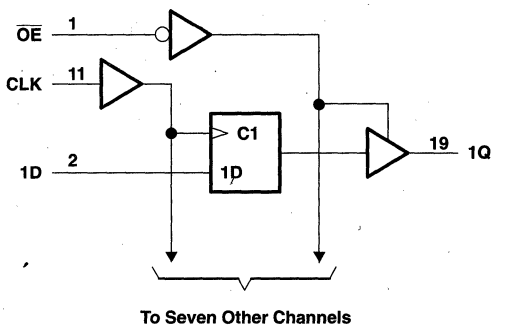
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state ..... 48 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −3 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | – 1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to – 3 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | V |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | – 60 | | – 150 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 55 | 86 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCZ}$ is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

## timing requirements

| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | $V_{CC}$ = 4.5 V to 5.5 V, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 100 | 0 | 100 | MHz |
| $t_w$ | Pulse duration | CLK high | 7 | | 7 | | ns |
| | | CLK low | 6 | | 6 | | |
| $t_{su}$ | Setup time before CLK↑ | Data high | 2 | | 2 | | ns |
| | | Data low | 2 | | 2 | | |
| $t_h$ | Hold time after CLK↑ | Data high | 2 | | 2 | | ns |
| | | Data low | 2 | | 2 | | |

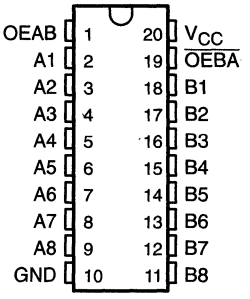
## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | 100 | | | 100 | | MHz |
| $t_{PLH}$ | CLK | Any Q | 3.2 | 6.1 | 8.5 | 3.2 | 10 | ns |
| $t_{PHL}$ | | | 3.2 | 6.1 | 8.5 | 3.2 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Any Q | 1.2 | 8.6 | 11.5 | 1.2 | 12.5 | ns |
| $t_{PZL}$ | | | 1.2 | 4.9 | 7.5 | 1.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Q | 1.2 | 4.9 | 7 | 1.2 | 8 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.9 | 5.5 | 1.2 | 6.5 | |

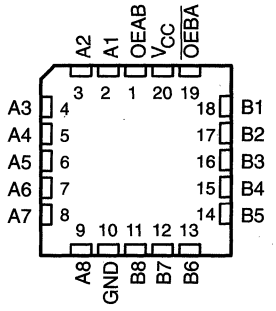
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

- **Local Bus-Latch Capability**
- **Noninverting Logic**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F621 . . . J PACKAGE**
**SN74F621 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F621 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output enable (OEAB and $\overline{\text{OEBA}}$) inputs.

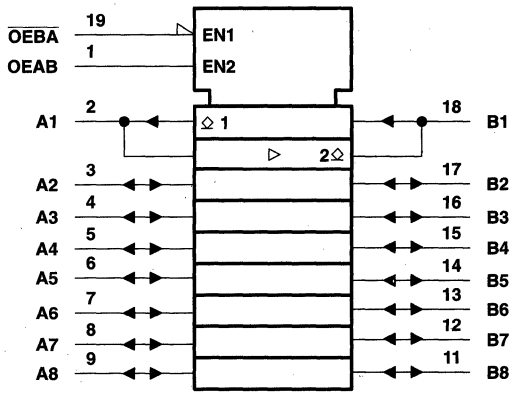
The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54F621 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F621 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

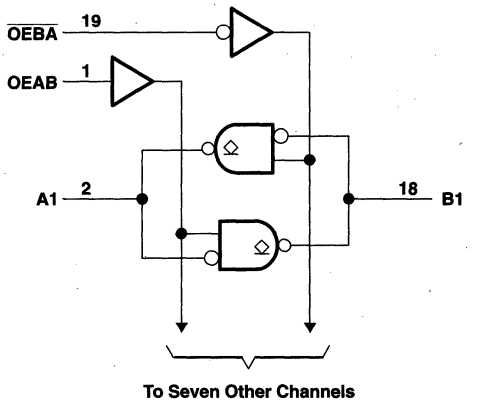
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{\text{OEBA}}$ | OEAB | |
| L | L | B data to A bus |
| L | H | B data to A bus, A data to B bus |
| H | L | Isolation |
| H | H | A data to B bus |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (excluding I/O ports) (see Note 1) ..... −1.2 V to 7 V
Input current range, $I_{IK}$ ..... −30 mA to 5 mA
Voltage range applied to any output in the high state ..... −0.5 V to 5.5 V
Current into any output in the low state: SN54F621 (A1–A8) ..... 40 mA
SN54F621 (B1–B8) ..... 96 mA
SN74F621 (A1–A8) ..... 48 mA
SN74F621 (B1–B8) ..... 128 mA
Operating free-air temperature range: SN54F621 ..... −55°C to 125°C
SN74F621 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | | SN54F621 | | | SN74F621 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{OH}$ | High-level output voltage | | | | 5.5 | | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | | | −18 | mA |
| $I_{OL}$ | Low-level output current | A1–A8 | | | 20 | | | 24 | mA |
| | | B1–B8 | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F621 | | | SN74F621 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | – 1.2 | | | – 1.2 | V |
| $I_{OH}$ | | $V_{CC}$ = 4.5 V, | $V_{OH}$ = 5.5 V | | | 250 | | | 250 | μA |
| $V_{OL}$ | A1–A8 | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | B1–B8 | | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | A and B ports | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | OEAB or $\overline{OEBA}$ | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$‡ | A and B ports | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | μA |
| | OEAB or $\overline{OEBA}$ | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | A and B ports | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.65 | | | – 0.65 | mA |
| | OEAB or $\overline{OEBA}$ | | | | | –0.6 | | | – 0.6 | |
| $I_{CCH}$ | | $V_{CC}$ = 5.5 V | | | 105 | 140 | | 105 | 140 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5 V | | | 105 | 140 | | 105 | 140 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.

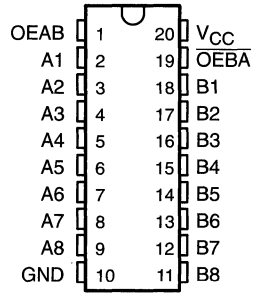
## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F621 | | | SN54F621 | | SN74F621 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 6 | 9.5 | 12 | 5.5 | 13 | 5.5 | 13 | ns |
| $t_{PHL}$ | | | 2.5 | 3.8 | 8 | 2 | 8.5 | 2 | 8.5 | |
| $t_{PLH}$ | B | A | 6 | 9 | 12 | 5.5 | 12.5 | 5.5 | 12.5 | ns |
| $t_{PHL}$ | | | 2.5 | 4 | 7.5 | 2 | 8 | 2 | 8 | |
| $t_{PLH}$ | $\overline{OEBA}$ | A | 6 | 10 | 13.5 | 5.5 | 14 | 5.5 | 14 | ns |
| $t_{PHL}$ | | | 3.5 | 6.5 | 10.5 | 2.5 | 11 | 2.5 | 11 | |
| $t_{PLH}$ | OEAB | B | 7 | 12 | 15 | 6 | 17 | 6 | 17 | ns |
| $t_{PHL}$ | | | 3.5 | 6.5 | 9.5 | 3 | 10 | 3 | 10 | |

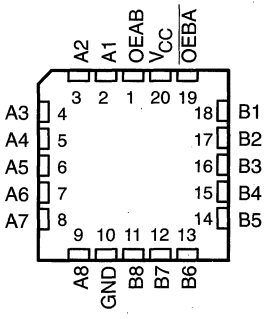
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Local Bus-Latch Capability**
- **Noninverting Logic**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN54F623 . . . J PACKAGE**
**SN74F623 . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54F623 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output enable (OEAB and $\overline{\text{OEBA}}$) inputs.

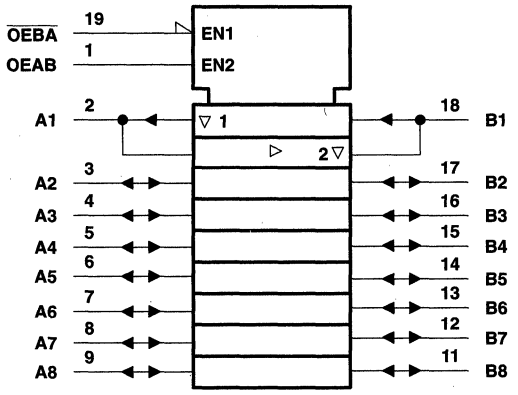
The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54F623 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F623 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

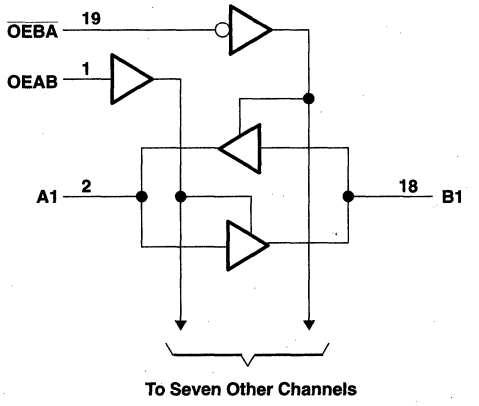
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{\text{OEBA}}$ | OEAB | |
| L | L | B data to A bus |
| L | H | B data to A bus, A data to B bus |
| H | L | Isolation |
| H | H | A data to B bus |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (excluding I/O ports) (see Note 1) ..... −1.2 V to 7 V
Input current range, $I_{IK}$ ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F623 (A1–A8) ..... 40 mA
SN54F623 (B1–B8) ..... 96 mA
SN74F623 (A1–A8) ..... 48 mA
SN74F623 (B1–B8) ..... 128 mA
Operating free-air temperature range: SN54F623 ..... −55°C to 125°C
SN74F623 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

| | | | SN54F623 | | | SN74F623 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | A1–A8 | | | −3 | | | −3 | mA |
| | | B1–B8 | | | −12 | | | −15 | |
| $I_{OL}$ | Low-level output current | A1–A8 | | | 20 | | | 24 | mA |
| | | B1–B8 | | | 48 | | | 64 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54F623 | | | SN74F623 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | – 1.2 | | | – 1.2 | V |
| $V_{OH}$ | A1–A8 | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | B1–B8 | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | | | $I_{OH}$ = – 12 mA | 2 | 3.2 | | | | | |
| | | | $I_{OH}$ = – 15 mA | | | | 2 | 3.1 | | |
| | Any output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to –3 mA | | | | 2.7 | | | |
| $V_{OL}$ | A1–A8 | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | B1–B8 | | $I_{OL}$ = 48 mA | | 0.38 | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | 0.42 | 0.55 | |
| $I_I$ | A and B ports | $V_{CC}$ = 5.5 V | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | OEAB or $\overline{OEBA}$ | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$‡ | A and B ports | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 70 | | | 70 | µA |
| | OEAB or $\overline{OEBA}$ | | | | | 20 | | | 20 | |
| $I_{IL}$‡ | A and B ports | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.65 | | | – 0.65 | mA |
| | OEAB or $\overline{OEBA}$ | | | | | – 0.6 | | | – 0.6 | |
| $I_{OS}$§ | A1–A8 | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | – 60 | | – 150 | – 60 | | – 150 | mA |
| | B1–B8 | | | – 100 | | – 225 | – 100 | | – 225 | |
| $I_{CCH}$ | | $V_{CC}$ = 5.5 V, | Any output = 4.5 V | | 110 | 140 | | 110 | 140 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5 V | OEAB or $\overline{OEBA}$ = 4.5 V, A1–A8 = GND | | 110 | 140 | | 110 | 140 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5 V | $\overline{OEBA}$ or A1–A8 = 4.5 V, OEAB = GND | | 99 | 130 | | 99 | 130 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

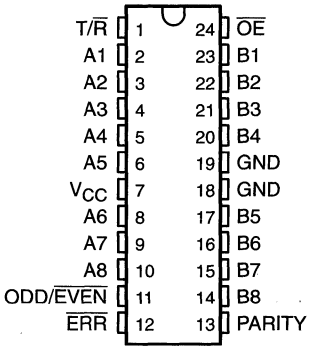
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F623 | | | SN54F623 | | SN74F623 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | B | 1.2 | 3.6 | 5.5 | 1.1 | 6.8 | 1.2 | 6.5 | ns |
| $t_{PHL}$ | | | 2.2 | 4.6 | 7 | 1.6 | 8 | 1.7 | 7.5 | |
| $t_{PLH}$ | B | A | 1.2 | 3.6 | 5.5 | 1.1 | 6.8 | 1.2 | 6.5 | ns |
| $t_{PHL}$ | | | 1.7 | 4.1 | 6.5 | 1.6 | 8 | 1.7 | 7.5 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 3.1 | 8.1 | 10.5 | 2.7 | 12.4 | 3.1 | 12 | ns |
| $t_{PZL}$ | | | 2.8 | 7.1 | 9.5 | 2.5 | 10.3 | 2.8 | 10 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 1.7 | 4.1 | 6.5 | 1.6 | 8.3 | 1.7 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.7 | 4.1 | 6.5 | 1.5 | 7.4 | 1.7 | 7 | |
| $t_{PZH}$ | OEAB | B | 2.8 | 7.6 | 10 | 2.7 | 12 | 2.8 | 11.5 | ns |
| $t_{PZL}$ | | | 2.8 | 6.6 | 9 | 2.8 | 10 | 2.9 | 9.5 | |
| $t_{PHZ}$ | OEAB | B | 2.2 | 5.6 | 8.5 | 1.9 | 10 | 2.2 | 10 | ns |
| $t_{PLZ}$ | | | 3.2 | 6.6 | 9 | 3.1 | 10.7 | 3.2 | 10 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Combines 'F245 and 'F280B Functions in One Package**
- **High-Impedance N-P-N Inputs for Reduced Loading (70 μA in Low and High States)**
- **High Output Drive and Light Bus Loading**
- **3-State B Outputs Sink 64 mA and Source 15 mA**
- **Input Diodes for Termination Effects**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

**DW OR NT PACKAGE**
**(TOP VIEW)**




## description

The SN74F657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a specified current sinking capability of 24 mA at the A port and 64 mA at the B port.

The transmit/receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. When T/$\overline{R}$ is high, data is transmitted from the A port to the B port. When T/$\overline{R}$ is low, data is received at the A port from the B port.

When the output enable ($\overline{OE}$) input is high, both the A and B ports are placed in a high-impedance state (disabled). The ODD/$\overline{EVEN}$ input allows the user to select between odd or even parity systems. When transmitting from A port to B port (T/$\overline{R}$ high), PARITY is an output from the generator/checker. When receiving from B port to A port (T/$\overline{R}$ low), PARITY is an input.

When transmitting (T/$\overline{R}$ high), the parity select (ODD/$\overline{EVEN}$) input is made high or low as appropriate. The A port is then polled to determine the number of high bits.The PARITY output goes to the logic state determined by ODD/$\overline{EVEN}$ and the number of high bits on A port. When ODD/$\overline{EVEN}$ is low (for even parity) and the number of high bits on A port is odd, the PARITY will be high, transmitting even parity. If the number of high bits on A port is even, the PARITY will be low, keeping even parity.

When in the receive mode (T/$\overline{R}$ low), the B port is polled to determine the number of high bits. If ODD/$\overline{EVEN}$ is low (for even parity) and the number of highs on B port is:

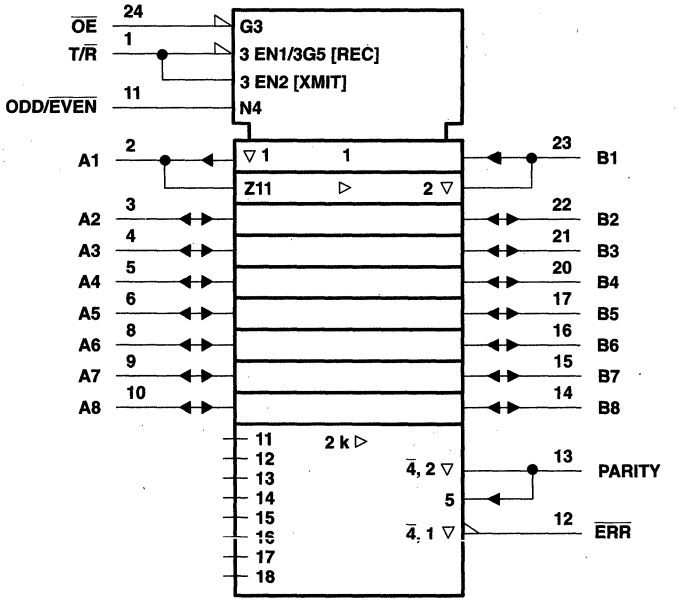
1. Odd and the PARITY input is high, then $\overline{ERR}$ will be high signifying no error.
2. Even and the PARITY input is high, then $\overline{ERR}$ will be low indicating an error.

The SN74F657 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

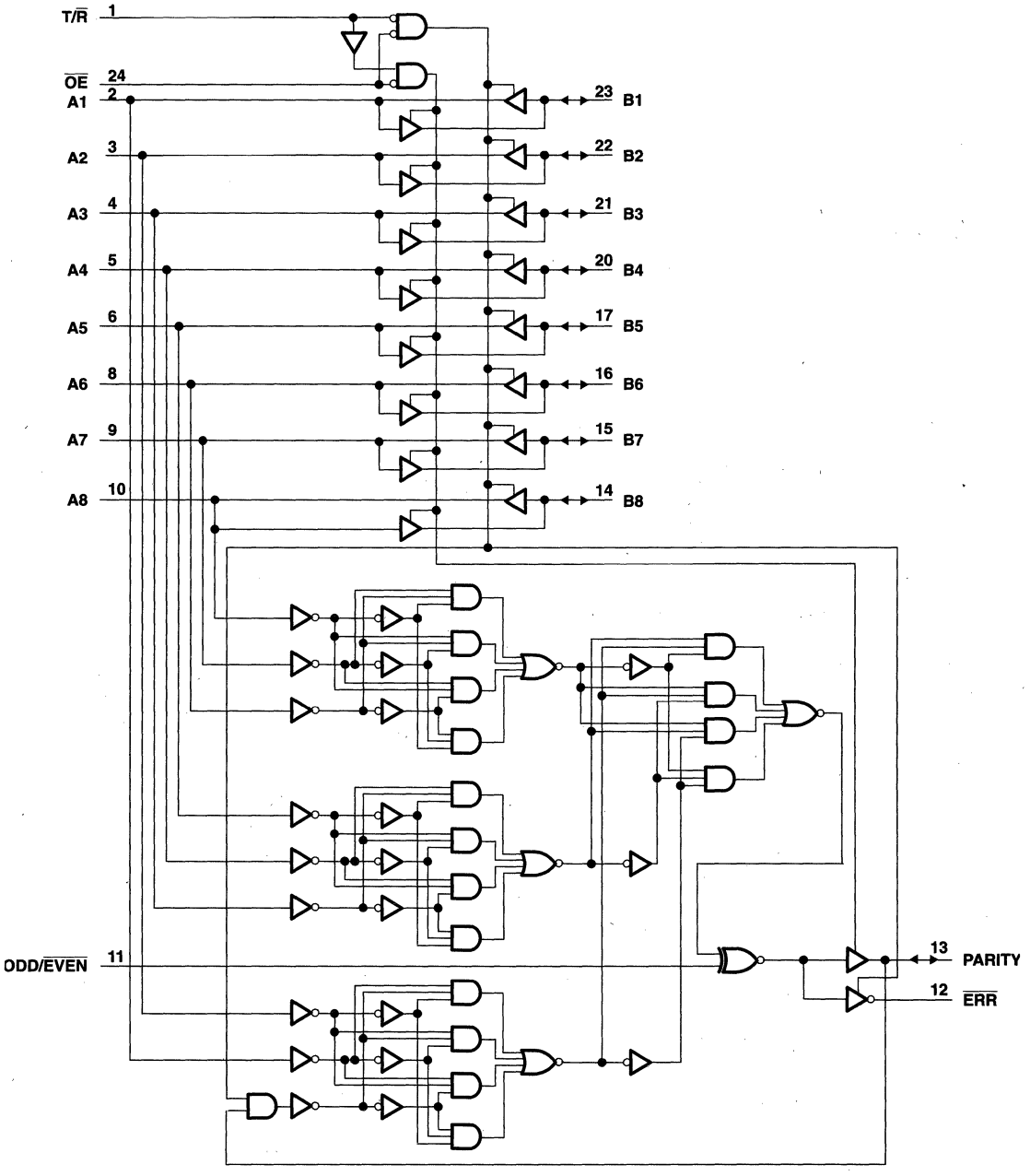
| NUMBER OF A OR B INPUTS THAT ARE HIGH | INPUTS | | | INPUT/OUTPUT PARITY | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{OE}$ | T/$\overline{R}$ | ODD/$\overline{EVEN}$ | | $\overline{ERR}$ | OUTPUT MODE |
| 0, 2, 4, 6, 8 | L | H | H | H | Z | Transmit |
| | L | H | L | L | Z | Transmit |
| | L | L | H | H | H | Receive |
| | L | L | H | L | L | Receive |
| | L | L | L | H | L | Receive |
| | L | L | L | L | H | Receive |
| 1, 3, 5, 7 | L | H | H | L | Z | Transmit |
| | L | H | L | H | Z | Transmit |
| | L | L | H | H | L | Receive |
| | L | L | H | L | H | Receive |
| | L | L | L | H | H | Receive |
| | L | L | L | L | L | Receive |
| Don't care | H | X | X | Z | Z | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (excluding I/O ports) (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: A1–A8 ..... 48 mA
B1–B8 ..... 128 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | A1–A8 | | | −3 | mA |
| | | B1–B8, PARITY, $\overline{ERR}$ | | | −12 | |
| $I_{OL}$ | Low-level output current | A1–A8 | | | 24 | mA |
| | | B1–B8, PARITY, $\overline{ERR}$ | | | 64 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = – 18 mA | | | | – 1.2 | V |
| $V_{OH}$ | Any output | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 3 mA | | 2.4 | 3.3 | | V |
| | B1–B8, PARITY, $\overline{ERR}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = – 15 mA | | 2 | 3.1 | | |
| | Any output | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to – 3 mA | | 2.7 | | | |
| $V_{OL}$ | A1–A8 | $V_{CC}$ = 4.5 V | $I_{OL}$ = 24 mA | | | 0.35 | 0.5 | V |
| | B1–B8, PARITY, $\overline{ERR}$ | | $I_{OL}$ = 64 mA | | | 0.42 | 0.55 | |
| $I_I$ | T/$\overline{R}$ | $V_{CC}$ = 0, | $V_I$ = 7 V, | $\overline{OE}$ = 4.5 V | | | 0.1 | mA |
| | $\overline{OE}$ | $V_{CC}$ = 0, | $V_I$ = 7 V, | T/$\overline{R}$ = 4.5 V | | | 0.1 | |
| | ODD/$\overline{EVEN}$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | | 0.1 | |
| | A1–A8 | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | | 2 | |
| | B1–B8 | | | | | | 1 | |
| $I_{IH}$‡ | A, B, PARITY | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 70 | µA |
| | T/$\overline{R}$, $\overline{OE}$ | | | | | | 40 | |
| | ODD/$\overline{EVEN}$ | | | | | | 20 | |
| $I_{IL}$‡ | A, B, PARITY | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | | – 70 | µA |
| | T/$\overline{R}$, $\overline{OE}$ | | | | | | – 40 | |
| | ODD/$\overline{EVEN}$ | | | | | | – 20 | |
| $I_{OS}$§ | A1–A8 | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | | – 60 | | – 150 | mA |
| | B1–B8 | | | | – 100 | | – 225 | |
| $I_{OZH}$ | $\overline{ERR}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 50 | µA |
| $I_{OZL}$ | $\overline{ERR}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | | –50 | µA |
| $I_{CCH}$ | | $V_{CC}$ = 5.5 V | | | | 90 | 125 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5 V | | | | 106 | 150 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5 V | | | | 98 | 145 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 2.5 | 4.2 | 7.5 | 2.5 | 8 | ns |
| $t_{PHL}$ | | | 3 | 4 | 7.5 | 3 | 8 | |
| $t_{PLH}$ | A | PARITY | 6 | 8.4 | 14 | 6 | 16 | ns |
| $t_{PHL}$ | | | 6.8 | 8.5 | 15 | 6.8 | 16 | |
| $t_{PLH}$ | ODD/$\overline{\text{EVEN}}$ | PARITY, $\overline{\text{ERR}}$ | 4 | 6.4 | 11 | 4 | 12 | ns |
| $t_{PHL}$ | | | 4.5 | 6.9 | 11.5 | 4.5 | 12.5 | |
| $t_{PLH}$ | B | $\overline{\text{ERR}}$ | 8 | 12.7 | 20.5 | 7.5 | 22.5 | ns |
| $t_{PHL}$ | | | 8 | 13.4 | 20.5 | 7.5 | 22.5 | |
| $t_{PLH}$ | PARITY | $\overline{\text{ERR}}$ | 6 | 8.1 | 15.5 | 6 | 16.5 | ns |
| $t_{PHL}$ | | | 7.5 | 8.8 | 15.5 | 7.5 | 17 | |
| $t_{PZH}$ | $\overline{\text{OE}}$ | A, B, PARITY, or $\overline{\text{ERR}}$‡ | 3 | 5.3 | 8 | 3 | 9 | ns |
| $t_{PZL}$ | | | 4 | 5.4 | 9.5 | 4 | 11 | |
| $t_{PHZ}$ | $\overline{\text{OE}}$ | A, B, PARITY, or $\overline{\text{ERR}}$‡ | 2 | 4.2 | 7.5 | 2 | 8 | ns |
| $t_{PLZ}$ | | | 2 | 3.7 | 6 | 2 | 6.5 | |

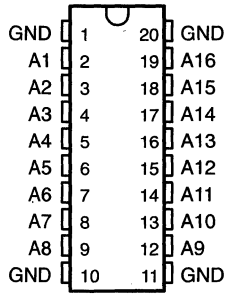
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These delay times reflect the 3-state recovery time only and not the signal through the buffers or parity check circuitry. To assure valid information at the $\overline{\text{ERR}}$ output pin, time must be allowed for the signal to propagate through the drivers (B to A), and to the $\overline{\text{ERR}}$ output. Valid data at the $\overline{\text{ERR}}$ output is greater than or equal to (B to A) + (A to PARITY).

NOTE 2: Load circuits and waveforms are shown in Section 1.

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 300 mA**
- **16-Bit Array Structure Suited for Bus-Oriented Systems**

**DW PACKAGE**
**(TOP VIEW)**

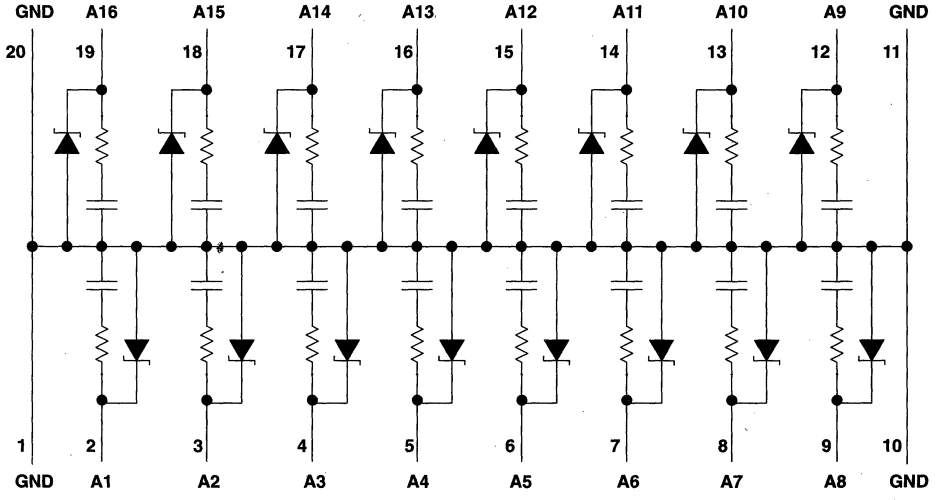



## description

This bus-termination array is designed to reduce reflection noise and minimize ringing on high-performance bus lines. The SN74F1016 features a 16-bit R-C network and Schottky barrier diode array. These Schottky diodes provide clamp-to-ground functionality and serve to minimize overshoot and undershoot of high-speed switching buses.

The SN74F1016 is characterized for operation from 0°C to 70°C.

## schematic diagram




Resistor = 50 Ω ± 10%
Capacitor = 47 pF ± 10%, $V_R$ = 2.5 V, f = 1 MHz
Diode = Schottky

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, $V_R$ ..... 7 V
Continuous forward current, $I_F$: Any D terminal from GND ..... 50 mA
Total through all GND terminals ..... 170 mA
Repetitive peak forward current, $I_{FRM}$‡: Any D terminal from GND ..... 300 mA
Total through all GND terminals ..... 1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature ..... 500 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ These values apply for $t_w \leq 100$ µs, duty cycle ≤ 20%.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### single-diode operation (see Note 1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_R$ | Static reverse current | $V_R$ = 7 V | | | 2 | µA |
| $V_{FM}$ | Peak forward voltage | $I_F$ = 200 mA | | 1.25 | | V |
| $C_t$ | Total capacitance | $V_R$ = 0 | | | 80 | pF |
| | | $V_R$ = 2 V | | | 60 | |
| | | $V_R$ = 3 V | | | 55 | |

† All typical values are at $T_A$ = 25°C.
NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

### multiple-diode operation

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_X$ | Internal crosstalk current | Total GND current = 1.2 A, See Note 2 | | 10 | 50 | µA |

NOTE 2: $I_X$ is measured under the following conditions with one diode static, all others switching:
Switching diodes: $t_W$ = 100 µs, duty cycle = 20%;
Static diode: $V_R$ = 5 V; the static diode input current is the internal crosstalk current $I_X$.

### switching characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{rr}$ | Reverse recovery time | $I_F$ = 10 mA, $I_{RM(REC)}$ = 10 mA, $I_{R(REC)}$ = 1 mA, $R_L$ = 100 Ω | | 8 | 10 | ns |

### undershoot characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{US}$ | Undershoot voltage | $t_f$ = 2 ns, $t_W$ = 50 ns, $V_{IH}$ = 5 V, $V_{IL}$ = 0, $Z_S$ = 25 Ω, $Z_O$ = 50 Ω, L = 36-inch coaxial cable | | 0.7 | 0.8 | V |

## APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1016 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in Figure 1. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current voltage for the SN74F1016 is shown in Figure 1.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

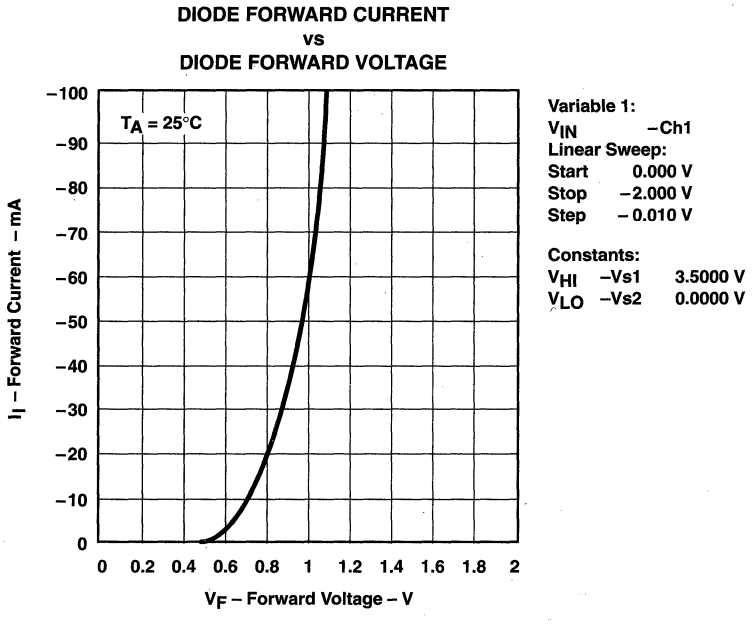
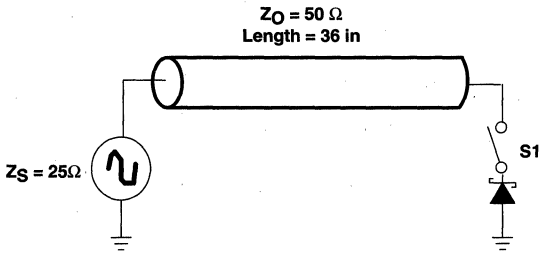
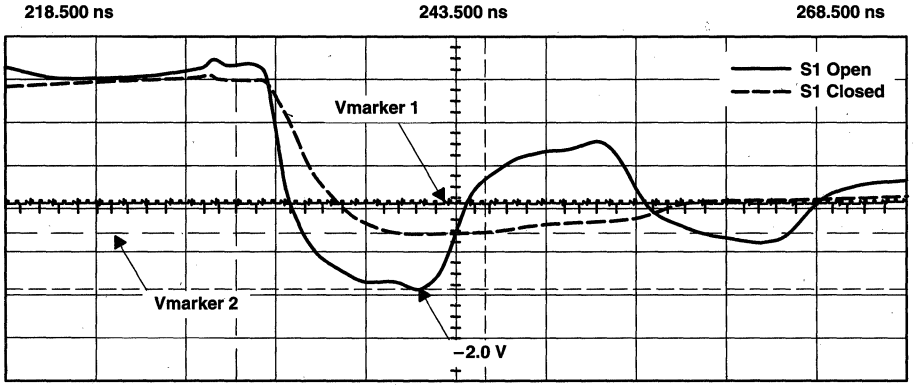



**Figure 1**




(a) UNDERSHOOT TEST SETUP



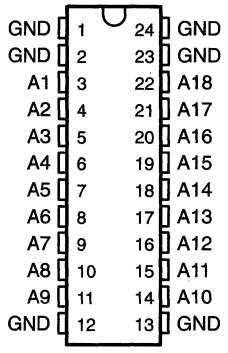

| | | | | | |
|---|---|---|---|---|---|
| Ch. 1 | = | 1.00 V/div | Offset | = | −20.00 mV |
| Timebase | = | 5.00 ns/div | Delay | = | 243.5 ns |
| Vmarker 1 | = | 0.00 V | Delta V | = | −640.00 mV |
| Vmarker 2 | = | −640.00 mV | | | |

(b) SCOPE DISPLAY

**Figure 2. Undershoot Test Setup and Scope Display**

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 300 mA**
- **18-Bit Array Structure Suited for Bus-Oriented Systems**

**DW PACKAGE**
**(TOP VIEW)**

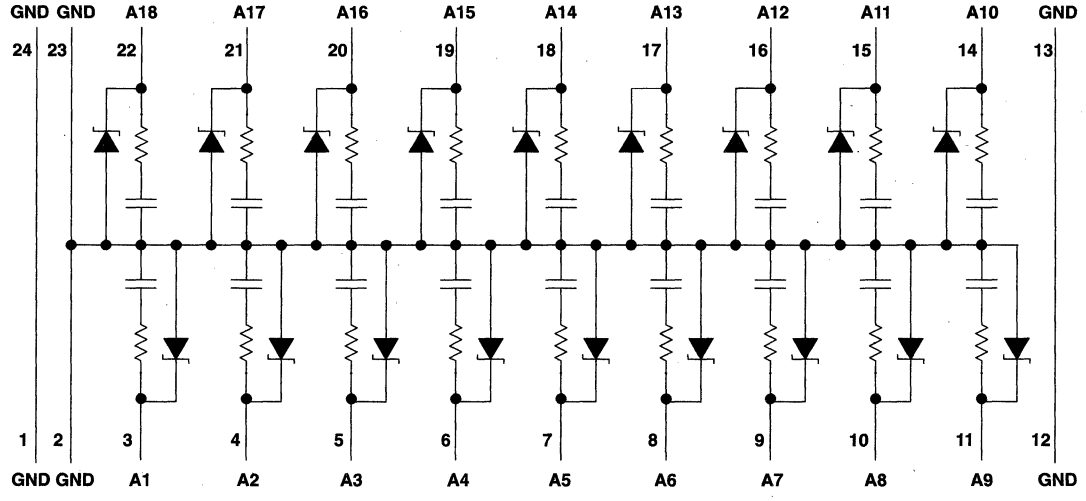



## description

This bus-termination array is designed to reduce reflection noise and minimize ringing on high-performance bus lines. The SN74F1018 features an 18-bit R-C network and Schottky barrier diode array. These Schottky diodes provide clamp-to-ground functionality and serve to minimize overshoot and undershoot of high-speed switching buses.

The SN74F1018 is characterized for operation from 0°C to 70°C.

## schematic diagram




Resistor = 50 Ω ± 10%
Capacitor = 47 pF ± 10%, $V_R$ = 2.5 V, f = 1 MHz
Diode = Schottky

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, $V_R$ ..... 7 V
Continuous forward current, $I_F$: Any D terminal from GND ..... 50 mA
Total through all GND terminals ..... 170 mA
Repetitive peak forward current, $I_{FRM}$‡: Any D terminal from GND ..... 300 mA
Total through all GND terminals ..... 1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature ..... 500 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ These values apply for $t_w \leq 100$ µs, duty cycle ≤ 20%.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### single-diode operation (see Note 1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_R$ | Static reverse current | $V_R$ = 7 V | | | 2 | µA |
| $V_F$ | Static forward voltage | $I_F$ = 18 mA | | 0.8 | 1 | V |
| | | $I_F$ = 50 mA | | 1 | 1.2 | |
| $V_{FM}$ | Peak forward voltage | $I_F$ = 200 mA | | 1.25 | | V |
| $C_t$ | Total capacitance | $V_R$ = 0 | | | 80 | pF |
| | | $V_R$ = 2 V | | | 60 | |
| | | $V_R$ = 3 V | | | 55 | |

† All typical values are at $T_A$ = 25°C.
NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

### multiple-diode operation

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_X$ | Internal crosstalk current | Total GND current = 1.2 A, See Note 2 | | 10 | 50 | µA |

NOTE 2: $I_X$ is measured under the following conditions with one diode static, all others switching:
Switching diodes: $t_w$ = 100 µs, duty cycle = 20%;
Static diode: $V_R$ = 5 V; the static diode input current is the internal crosstalk current $I_X$.

### switching characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{rr}$ | Reverse recovery time | $I_F$ = 10 mA, $I_{RM(REC)}$ = 10 mA, $i_{R(REC)}$ = 1 mA, $R_L$ = 100 Ω | | 8 | 10 | ns |

### undershoot characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{US}$ | Undershoot voltage | $t_f$ = 2 ns, $t_w$ = 50 ns, $V_{IH}$ = 5 V, $V_{IL}$ = 0, $Z_S$ = 25 Ω, $Z_O$ = 50 Ω, L = 36-inch coaxial cable | | 0.7 | 0.8 | V |

## APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1018 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in Figure 1. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current voltage for the SN74F1018 is shown in Figure 1.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

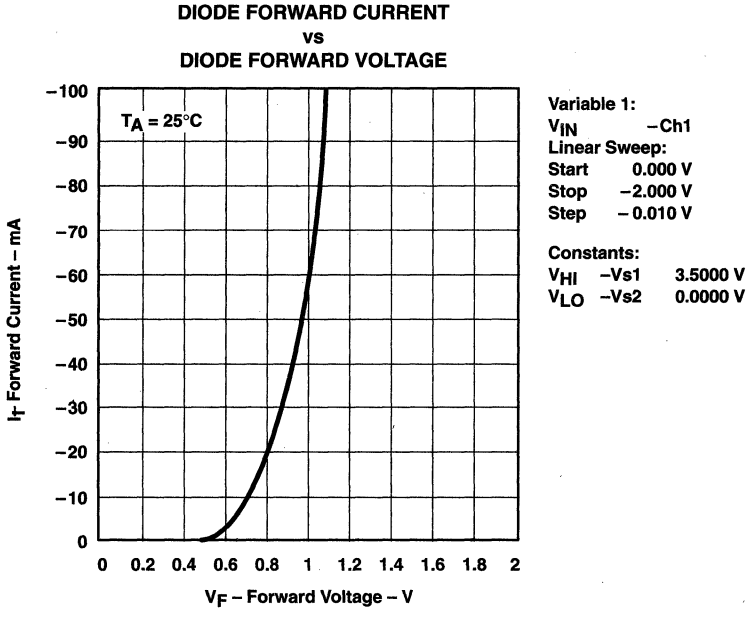
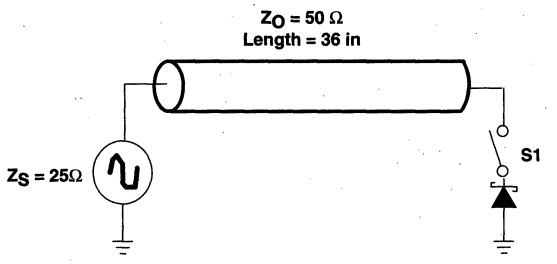
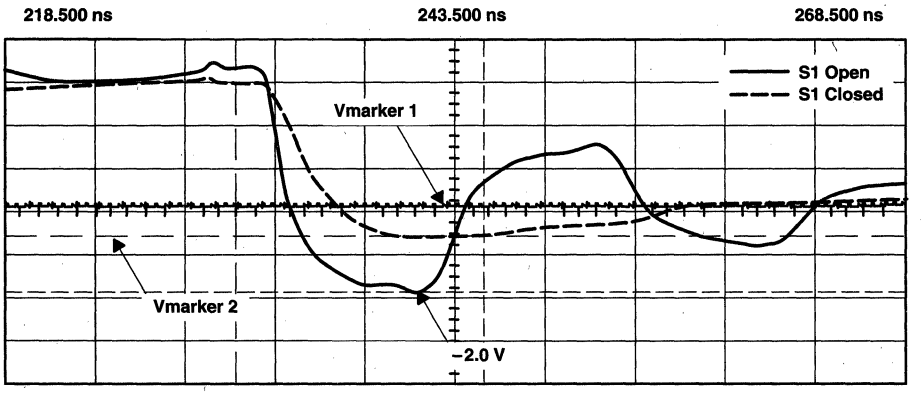



**Figure 1**




(a) UNDERSHOOT TEST SETUP



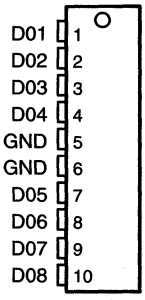

| | | | |
|---|---|---|---|
| Ch. 1 | = 1.00 V/div | Offset | = −20.00 mV |
| Timebase | = 5.00 ns/div | Delay | = 243.5 ns |
| Vmarker 1 | = 0.00 V | Delta V | = −640.00 mV |
| Vmarker 2 | = −640.00 mV | | |

(b) SCOPE DISPLAY

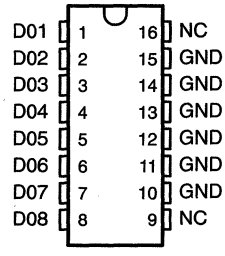
**Figure 2. Undershoot Test Setup and Scope Display**

- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 300 mA**
- **8-Bit Array Structure Suited for Bus-Oriented Systems**

**SC PACKAGE**
**(TOP VIEW)**




**D PACKAGE**
**(TOP VIEW)**



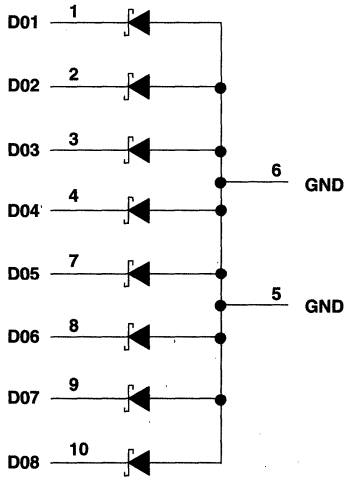

## description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for GND clamp.

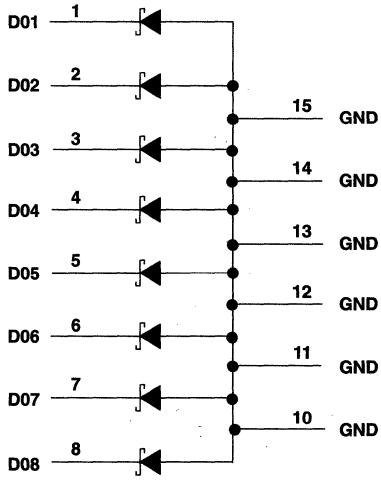
The SN74F1056 is characterized for operation from 0°C to 70°C.

## schematic diagrams

**SC Package**




**D Package**



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, $V_R$ ..... 7 V
Continuous forward current, $I_F$: Any D terminal from GND ..... 50 mA
Total through all GND terminals ..... 170 mA
Repetitive peak forward current, $I_{FRM}$‡: Any D terminal from GND ..... 300 mA
Total through all GND terminals ..... 1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature ..... 500 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ These values apply for $t_w \leq 100$ µs, duty cycle ≤ 20%.

## electrical characteristics over recommended operating free-air temperature range (unless other noted)

### single-diode operation (see Note 1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP§ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_R$ | Static reverse current | $V_R$ = 7 V | | | | 2 | µA |
| $V_F$ | Static forward voltage | $I_F$ = 18 mA | | | 0.8 | 1 | V |
| | | $I_F$ = 50 mA | | | 1 | 1.2 | |
| $V_{FM}$ | Peak forward voltage | $I_F$ = 200 mA | | | 1.23 | | V |
| $C_t$ | Total capacitance | $V_R$ = 0, | f = 1 MHz | | 3 | 3.75 | pF |
| | | $V_R$ = 2 V, | f = 1 MHz | | 2.5 | 3 | |

§ All typical values are at $T_A$ = 25°C.
NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

### multiple-diode operation

| PARAMETER | | TEST CONDITIONS | | MIN | TYP§ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_X$ | Internal crosstalk current | Total GND current = 1.2 A, | See Note 2 | | 10 | 50 | µA |

NOTE 2: $I_X$ is measured under the following conditions with one diode static, all others switching:
.. Switching diodes: $t_w$ = 100 µs, duty cycle = 20%;
.. Static diode: $V_R$ = 5 V; the static diode input current is the internal crosstalk current $I_X$.

### switching characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{rr}$ | Reverse recovery time | $I_F$ = 10 mA, $I_{RM(REC)}$ = 10 mA, $I_{R(REC)}$ = 1 mA, $R_L$ = 100 Ω | | 5 | 7 | ns |

### undershoot characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{US}$ | Undershoot voltage | $t_f$ = 2 ns, $t_w$ = 50 ns, $V_{IH}$ = 5 V, $V_{IL}$ = 0, $Z_S$ = 25 Ω, $Z_O$ = 50 Ω, L = 36-inch coax | | 0.6 | 0.7 | V |

## APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1056 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current voltage for the SN74F1056 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 2(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

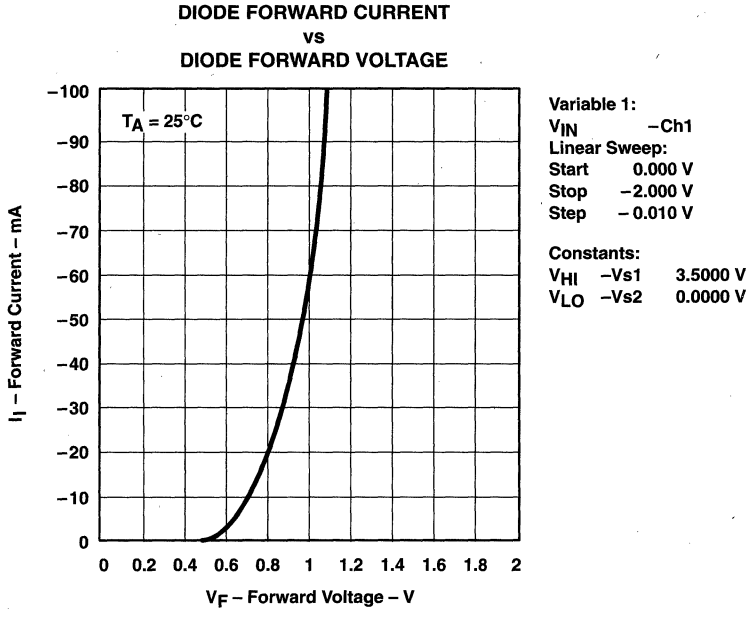
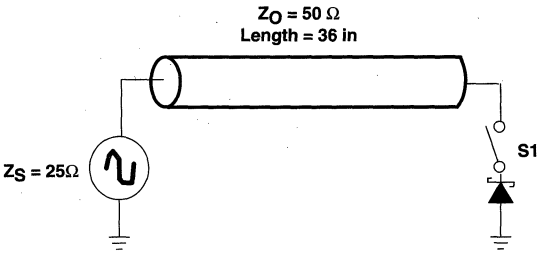
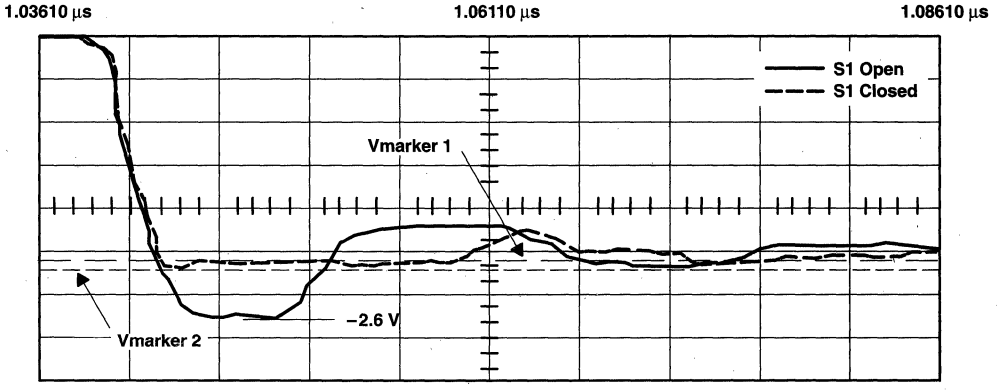



**Figure 1**




(a) UNDERSHOOT TEST SETUP



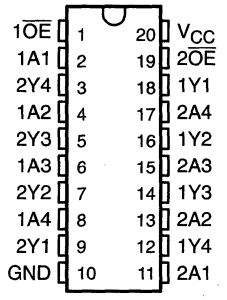

| | | | |
|---|---|---|---|
| Ch. 1 | = 2.000 V/div | Offset | = 2.340 V |
| Timebase | = 5.00 ns/div | Delay | = 1.06110 µs |
| Vmarker 1 | = 0.0000 V | Delta V | = −600.0 mV |
| Vmarker 2 | = −600.00 mV | | |

(b) SCOPE DISPLAY

**Figure 2. Undershoot Test Setup and Scope Display**

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

**SN74F2244 . . . DW, OR N PACKAGE**
**(TOP VIEW)**




## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

25Ω resistors in the lower output circuit reduce ringing and eliminate the need for external resistors.

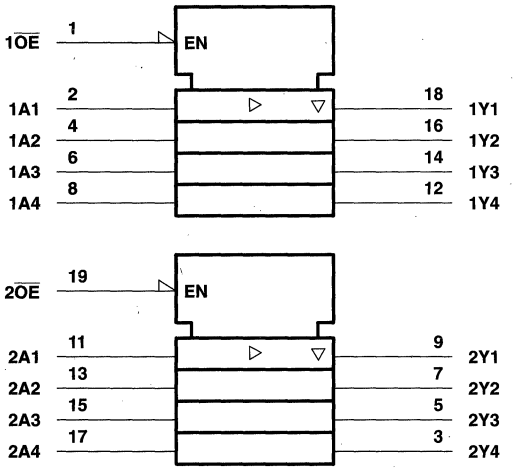
The SN74F2244 is characterized for operation form 0°C to 70°C.

**FUNCTION TABLE**
**(each buffer)**

| OUTPUT CONTROL | DATA INPUT | OUTPUT |
|---|---|---|
| $\overline{1G}$, $\overline{2G}$ | A | Y |
| H | X | Z |
| L | L | L |
| L | H | H |

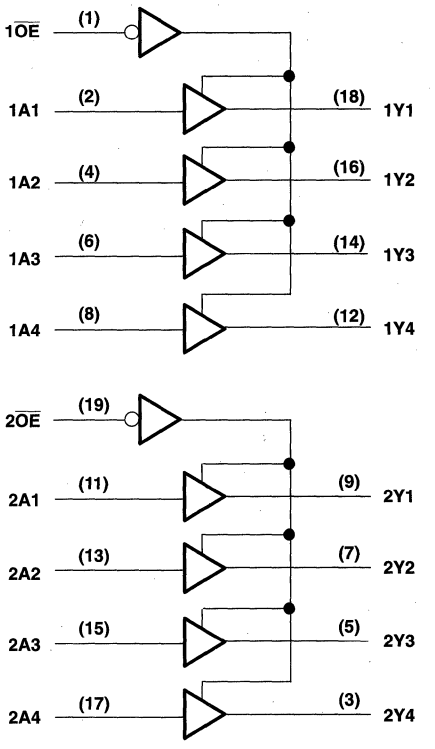
PRODUCT PREVIEW

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ..... −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ..... −1.2 V to 7 V
Input current range ..... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to $V_{CC}$
Current into any output in the low state: ..... 30 mA
Operating free-air temperature range: ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

PRODUCT PREVIEW

## recommended operating conditions

| | | SN74F2244 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN74F2244 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −3 mA | 2.4 | 2.8 | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = −15 mA | 2 | 2.3 | | |
| | | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −3 mA | 2.7 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 1 mA | | 0.2 | 0.5 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.5 | 0.75 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | 0.1 | mA |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 7 V | | | 50 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | −50 | µA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | Any $\overline{G}$ input | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | −1 | mA |
| | Any A input | | | | | −1.6 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −100 | | −225 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, Outputs open | Outputs high | | 40 | 60 | mA |
| | | | Outputs low | | 60 | 90 | |
| | | | Outputs disabled | | 60 | 90 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_1$ = 500 Ω, $R_2$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_1$ = 500 Ω, $R_2$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | 'F2244 | | | SN74F2244 | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.5 | | 7 | 1.5 | 7 | ns |
| $t_{PHL}$ | | | 2.5 | | 8 | 2.0 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.5 | | 9 | 1.0 | 9.5 | ns |
| $t_{PZL}$ | | | 2.5 | | 11.5 | 2.5 | 12.0 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.5 | | 9 | 1.0 | 9.5 | ns |
| $t_{PLZ}$ | | | 1.5 | | 8.5 | 1.5 | 9.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

PRODUCT PREVIEW

General Information 1
Data Sheets 2
Application Report 3
Mechanical Data 4

# Radiation Exposure Test Results of F Logic Functions

## Introduction

Military system functionality in a radiation environment is increasingly becoming more of a design criteria. System designers have a need for comparative integrated circuits radiation tolerance data, because exposure to gamma radiation degrades the performance of integrated circuits. The amount of performance degradation for various manufacturers' logic families is variable since process technologies differ. Comparison studies that expose various vendors' logic devices to radiation can be used to determine a logic family's suitability for use in a system. These studies may, in fact, influence the selection of product for design in.

There are numerous guidelines/methods for radiation testing. Also, there is room for interpretation regarding the failure modes of irradiated logic devices. Some IC manufacturers define a radiation-induced failure as the total-dose level at which a logic error occurs. Others define failure at the point at which data sheet parametrics are exceeded. These variable test methodologies and definitions make direct comparisons of existing studies difficult. Therefore, many OEMs have developed their own radiation test criteria to assure program compliance.

It is helpful to have some generic radiation data to use as comparisons for initial selection of logic families for new designs. To that end, the following is offered as a guide for that selection process. The data is presented in two sections:

1. Results of testing done by Texas Instruments, and
2. Results of testing done by a third-party OEM and printed herein with their permission.

The comparisons are necessarily generic and any conclusions that are drawn from the data may warrant further investigation. Results of the tests do indicate the TI F logic product is more radiation tolerant than currently available FAST™ product.

## Testing Performed by TI

Failure to meet data sheet parametric specifications is one consequence of exposing devices to radiation. After a device is irradiated, typically the first parametric specification to be violated is the input leakage current ($I_{IH}$) as it will increase beyond the maximum data book limit. For the radiation tolerance tests done by TI, the parameter monitored was $I_{IH}$. The data book maximum limit for this parameter is 20 μA for the F logic family. In typical system applications with 10 unit loads, 200 μA is considered a representative value for $I_{IH}$. Test conditions simulated a total-dose radiation environment.

Both the supply voltage ($V_{CC}$) and the inputs were kept at 5.5 V during irradiation. The dose rate was 201.9 rad(Si)/second, and the highest readings in each sample of four units of each device type ('54F00, '54F74, '54F244) are tabulated in Table 1. Initial tests were done with total doses of 50, 100, 200, and 100 krad(Si). Since some devices were beyond the 20 μA data book limit at the 50 krad(Si) total dose level, an additional test point of 20 krad(Si) was added. A few tests were stopped at 200 krad(Si) because the devices read over the full-scale test capability of 3031 μA. Full MIL-STD-883C-compliant product from each vendor was used except where indicated.

FAST is a trademark of National Semiconductor Corporation.

The following specific devices and date codes were subjected to the radiation testing:

| Texas Instruments | Date Code |
|---|---|
| '54F00 | B8735Z |
| '54F74 | 8647 |
| '54F244 | 8706 |

| Fairchild Semiconductor | Date Code |
|---|---|
| '54F00 | 8430, Recertification tested 8604 |
| '54F74 | Non-883C compliant P-DIP, 8718 |
| '54F244 | 8641 |

| Motorola Inc. | Date Code |
|---|---|
| '54F00 | 8513B |
| '54F74 | 8640A |
| '54F244 | 8619B |

| Signetics Corporation | Date Code |
|---|---|
| '54F00 | 8717 |
| '54F74 | 8648 |
| '54F244 | 8644 |

**Table 1. Relative Radiation Tolerance**

| PARAMETER | TEXAS INSTRUMENTS | FAIRCHILD | MOTOROLA | SIGNETICS |
|---|---|---|---|---|
| **'54F00** | | | | |
| $I_{IH}$ at 20 krad(Si) | — | <0.1 μA | 380.1 μA | — |
| $I_{IH}$ at 50 krad(Si) | 14.3 μA | 2.4 μA | 1231.1 μA | 2725 μA |
| $I_{IH}$ at 100 krad(Si) | 174.4 μA | 283.7 μA | 2114.3 μA | >3031 μA |
| $I_{IH}$ at 200 krad(Si) | 526.2 μA | 840.1 μA | >3031 μA | >3031 μA |
| $I_{IH}$ at 500 krad(Si) | 834.9 μA | 1408.3 μA | >3031 μA | — |
| $I_{IH}$ at 1000 krad(Si) | 739.5 μA | 1570.8 μA | >3031 μA | — |
| **'54F74** | | | | |
| $I_{IH}$ at 20 krad(Si) | — | 597.8 μA | 6.95 μA | 192.7 μA |
| $I_{IH}$ at 50 krad(Si) | 7.2 μA | >3031 μA | 230.9 μA | 1648.9 μA |
| $I_{IH}$ at 100 krad(Si) | 138 μA | >3031 μA | 389.3 μA | >3031 μA |
| $I_{IH}$ at 200 krad(Si) | 475.4 μA | >3031 μA | 713.1 μA | >3031 μA |
| $I_{IH}$ at 500 krad(Si) | 732.5 μA | — | 1417.2 μA | — |
| $I_{IH}$ at 1000 krad(Si) | 648.4 μA | — | 1528.3 μA | — |
| **'54F244** | | | | |
| $I_{IH}$ at 20 krad(Si) | — | 48.6 μA | 350.9 μA | 59.4 μA |
| $I_{IH}$ at 50 krad(Si) | 0.7 μA | 583.1 μA | 1062 μA | 280.7 μA |
| $I_{IH}$ at 100 krad(Si) | 64.7 μA | 2972.1 μA | 1650.1 μA | 751.9 μA |
| $I_{IH}$ at 200 krad(Si) | 296.7 μA | >3031 μA | 2644 μA | 1296.8 μA |
| $I_{IH}$ at 500 krad(Si) | 560.2 μA | — | >3031 μA | 1545 μA |
| $I_{IH}$ at 1000 krad(Si) | 525.5 μA | — | — | 1395.5 μA |

NOTE: Supply voltage $V_{CC}$ and input voltage $V_{IH}$ were both 5.5 V during irradiation.
Dose rate = 201.9 rad(Si)/second
Tester full-scale limit for $I_{IH}$ = 3031 μA max
Table listings were the highest $I_{IH}$ reading obtained in each sample of four units.

## Third-Party OEM Test Results†

Eight samples of the '54F04 hex inverters and '54F11 triple 3-input AND gates along with four samples of a '54F20 dual 4-input NAND gate were tested in a total-dose environment. They were exposed to gamma radiation and irradiated at approximately 500 rad(Si)/minute or 8 rad(Si)/second. Test data was taken every 2 krad(Si) up to 30 krad total dose. If the first four samples showed no significant degradation, the remaining parts were irradiated at 1000 rad(Si)/minute or 16.7 rad(Si)/second and data was taken every 5 krad(Si) up to 100 krad(Si). All devices were exercised, both functionally and parametrically, using the Eagle Multiplexer with the NUGPMUX test package on the EAGLE LSI-4 automated test equiment.

In addition to monitoring $I_{IH}$, the propagation delay ($t_{pd}$) of four samples of each device type was measured independently at baseline and following exposure to the highest total dose level tested – between 60 and 80 krad(Si). A custom propagation delay fixture was used. In all cases, one input received a 3-V amplitude square wave while the other inputs were tied to 5 V or 0 V so that the output yielded a positive square wave. The propagation delay was then measured using the 50% points of the input and output waveforms as reference. *No significant degradation was observed in any of the devices tested.*

During irradiation, the parts were statically biased with highs and lows as in Table 2 and dc parametric test conditions were selected according to data book specifications.

**Table 2. Biasing Schemes for Devices**

| PART | S/N | PIN NUMBER | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| '54F00 | 1–4 | H | X | L | X | H | X | GND | X | L | X | H | X | L | $V_{CC}$ |
| | 5–8 | H | X | L | X | H | X | GND | X | L | X | H | X | L | $V_{CC}$ |
| '54F11 | 1–4 | H | L | H | L | H | X | GND | X | L | H | L | X | L | $V_{CC}$ |
| | 5–8 | H | L | H | L | H | X | GND | X | L | H | L | X | L | $V_{CC}$ |
| '54F20 | 5–8 | H | L | NC | H | L | X | GND | X | H | H | NC | H | H | $V_{CC}$ |

† Only Texas Instruments Incorporated product was used in the study.

Dosimetry data showed that each device received radiation at a slightly different dose rate due to its positioning on the multiplexer. The actual exposure is shown in Table 3.

**Table 3. Actual Dose Rates**

| DEVICE | S/N | DOSE RATE/ rad(Si) | AVERAGE | Δ% POSITION |
|---|---|---|---|---|
| '54F04 | 1 | 472 | 496 | 12.5 |
| | 2 | 498 | | |
| | 3 | 484 | | |
| | 4 | 531 | | |
| | 5 | 939 | 1011 | 16 |
| | 6 | 1003 | | |
| | 7 | 1016 | | |
| | 8 | 1089 | | |
| '54F11 | 1 | 472 | 496 | 12.5 |
| | 2 | 498 | | |
| | 3 | 484 | | |
| | 4 | 531 | | |
| | 5 | 1038 | 1144 | 25.5 |
| | 6 | 1090 | | |
| | 7 | 1145 | | |
| | 8 | 1303 | | |
| '54F20 | 1 | 1038 | 1144 | 25.5 |
| | 2 | 1090 | | |
| | 3 | 1145 | | |
| | 4 | 1303 | | |

The minimum, mean, and maximum values for all parameters are shown for all device types in Tables 4 through 9. Table 4 and Figure 1 exhibit the input leakage current for the '54F04. Similarly, Tables 5 and 6 and Figures 2 and 3 represent the parametric performance for the $I_{IH}$ and $I_{CC}$ for the '54F20, respectively. And finally, Tables 7 through 9 and Figures 4 through 9 correspond to $I_{IH}$, $I_{CC}$, and $V_{OH}$ of the '54F11.

## Summary

The tests performed by Texas Instruments can be used as a gauge of relative radiation tolerance of various vendors' 54F-type logic families. Defining the data sheet parametric failure points, as opposed to defining the points where logic error occur, was the basis for both studies. Test results do indicate that the TI 54F logic family is more radiation tolerant within the constraints of the parameters monitored. Significantly lower $I_{IH}$ readings were recorded for TI 54F logic devices at several total-dose levels. An additional point for comparison is the data contained in the third-party OEM study.

The study that was performed by the third-party OEM gives a definition of radiation tolerance of TI 54F devices that is based on additional data sheet parametrics. Although no functional failure was observed in any of the eight samples of the devices tested, the dc parametrics did show some degradation. The various parameters monitored were the input leakage current ($I_{IH}$), the supply current ($I_{CC}$), and the output voltage ($V_{OH}$). Data sheet parametric failures for input leakage current for the '54F04, '54F11, and '54F20 were exhibited at 65, 60, and 70 krad(Si) total dose, respectively. The supply current exceeded data book specifications at 51 and 55 krad(Si) for the '54F20 and '54F11, respectively. No significant degradation was observed in the supply current for the '54F04 to 85 krad(Si). The output voltage for the '54F11 fell below the data book minimum specified value at total-dose levels exceeding 45 krad(Si). No degradation in propagation delays ($t_{pd}$) was observed in any of the devices irradiated.

PART NUMBER: '54F04 S/N 5–8
DATE CODE: A8709
VENDOR: TI
TEST DATE: 3-OCT-88

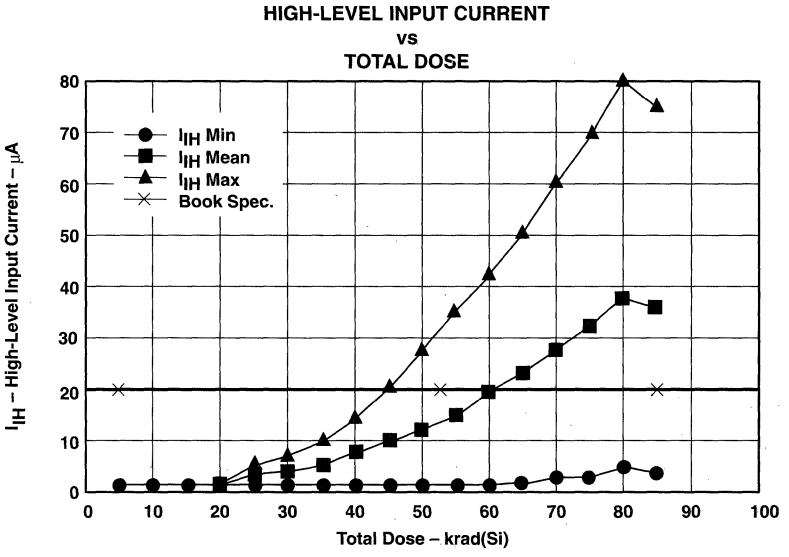



**Figure 1**

**Table 4. High-Level Input Current vs Total Dose – '54F04**

| TOTAL DOSE/ krad(Si) | $I_{IH}$ (μA) @ $V_I$ = 2.7 V | | |
|---|---|---|---|
| | MIN | MEAN | MAX |
| 00 | 0.2 | 0.2 | 0.2 |
| 05 | 0.2 | 0.2 | 0.2 |
| 10 | 0.2 | 0.2 | 0.2 |
| 15 | 0.2 | 0.2 | 0.2 |
| 20 | 0.2 | 0.3 | 0.6 |
| 25 | 0.2 | 1.1 | 2.6 |
| 30 | 0.2 | 2.5 | 5.8 |
| 35 | 0.2 | 4.5 | 10.3 |
| 40 | 0.2 | 6.8 | 15.3 |
| 45 | 0.2 | 9.5 | 21.1 |
| 50 | 0.2 | 12.4 | 27.5 |
| 55 | 0.5 | 15.7 | 34.5 |
| 60 | 0.8 | 19.3 | 42.2 |
| 65 | 1.2 | 23.3 | 50.4 |
| 70 | 1.8 | 27.7 | 59.3 |
| 75 | 2.6 | 32.3 | 68.6 |
| 80 | 3.6 | 37.2 | 77.8 |
| 85 | 3.2 | 35.9 | 75.5 |
| Book Spec | — | — | 20 |

PART NUMBER: '54F20 S/N 1–4
DATE CODE: 8726
VENDOR: TI
TEST DATE: 4-OCT-88

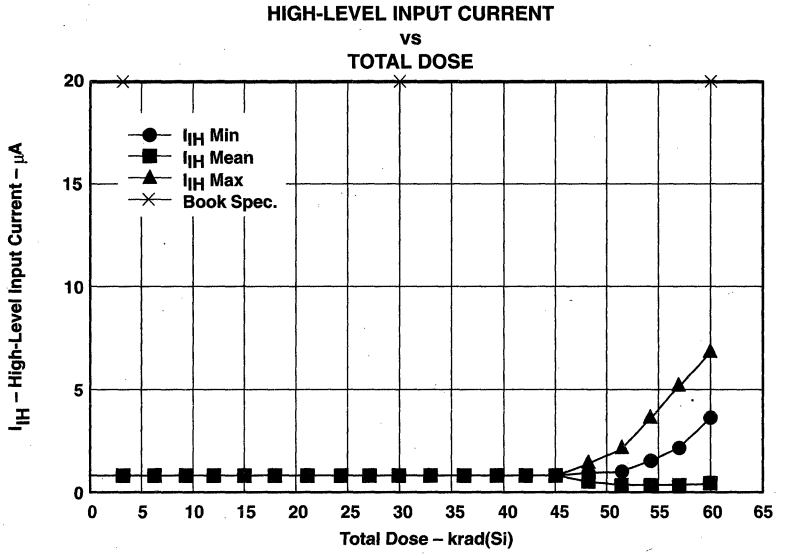



Figure 2

Table 5. High-Level Input Current vs Total Dose – '54F20

| TOTAL DOSE/ krad(Si) | $I_{IH}$ (μA) @ $V_I$ = 2.7 V | | |
|---|---|---|---|
| | MIN | MEAN | MAX |
| 00 | 0.5 | 0.5 | 0.5 |
| 03 | 0.5 | 0.5 | 0.5 |
| 06 | 0.5 | 0.5 | 0.5 |
| 09 | 0.5 | 0.5 | 0.5 |
| 12 | 0.5 | 0.5 | 0.5 |
| 15 | 0.5 | 0.5 | 0.5 |
| 18 | 0.5 | 0.5 | 0.5 |
| 21 | 0.5 | 0.5 | 0.5 |
| 24 | 0.5 | 0.5 | 0.5 |
| 27 | 0.5 | 0.5 | 0.5 |
| 30 | 0.5 | 0.5 | 0.5 |
| 33 | 0.5 | 0.5 | 0.5 |
| 36 | 0.5 | 0.5 | 0.5 |
| 39 | 0.4 | 0.5 | 0.5 |
| 42 | 0.4 | 0.5 | 0.5 |
| 45 | 0.4 | 0.4 | 0.4 |
| 48 | 0.3 | 0.5 | 0.9 |
| 51 | 0.3 | 0.8 | 1.8 |
| 54 | 0.3 | 1.4 | 3.2 |
| 57 | 0.3 | 2.2 | 4.9 |
| 60 | 0.5 | 3.3 | 7.2 |
| Book Spec | — | — | 20 |

PART NUMBER: '54F20 S/N 1–4
DATE CODE: 8726
VENDOR: TI
TEST DATE: 4-OCT-88

SUPPLY CURRENT
vs
TOTAL DOSE

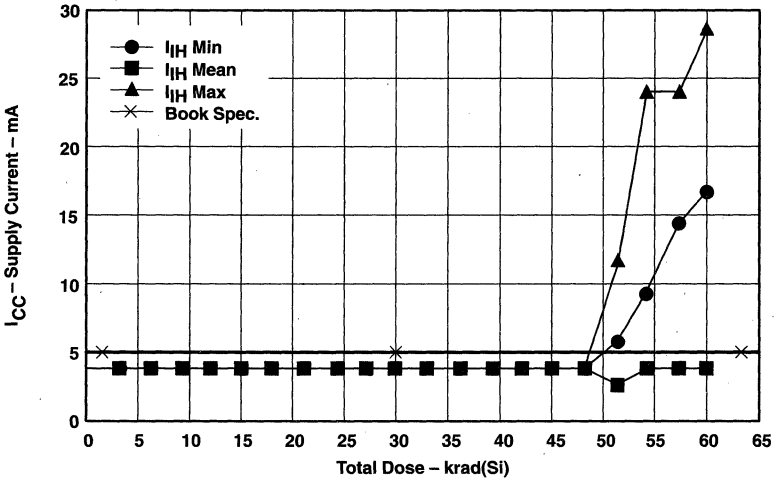



Figure 3

Table 6. Supply Current vs Total Dose – '54F20

| TOTAL DOSE/ krad(Si) | $I_{CCH}$ (mA) @ $V_{CC}$ = 5.5 V | | |
|---|---|---|---|
| | MIN | MEAN | MAX |
| 00 | 3.962 | 4.007 | 4.042 |
| 03 | 3.958 | 4.003 | 4.04 |
| 06 | 3.954 | 4 | 4.037 |
| 09 | 3.946 | 3.996 | 4.043 |
| 12 | 3.948 | 3.994 | 4.032 |
| 15 | 3.945 | 3.992 | 4.029 |
| 18 | 3.941 | 3.99 | 4.028 |
| 21 | 3.94 | 3.988 | 4.026 |
| 24 | 3.941 | 3.987 | 4.024 |
| 27 | 3.937 | 3.985 | 4.023 |
| 30 | 3.936 | 3.983 | 4.021 |
| 33 | 3.936 | 3.983 | 4.02 |
| 36 | 3.933 | 3.981 | 4.019 |
| 39 | 3.932 | 3.979 | 4.017 |
| 42 | 3.932 | 3.979 | 4.017 |
| 45 | 3.931 | 3.979 | 4.017 |
| 48 | 3.93 | 3.978 | 4.015 |
| 51 | 3.078 | 5.667 | 11.629 |
| 54 | 3.974 | 8.782 | 23.159 |
| 57 | 4.015 | 14.447 | 23.243 |
| 60 | 4.015 | 16.91 | 28.721 |
| Book Spec | — | — | 5.1 |

PART NUMBER: '54F11 S/N 5–8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

HIGH-LEVEL INPUT CURRENT
vs
TOTAL DOSE

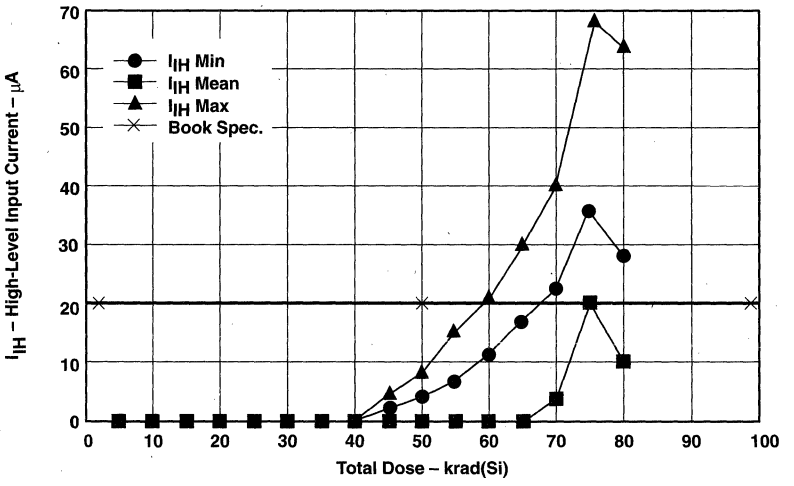



Figure 4

Table 7. High-Level Input Current vs Total Dose – '54F11

| TOTAL DOSE/ krad(Si) | $I_{IH}$ (μA) @ $V_I$ = 2.7 V | | |
|---|---|---|---|
| | MIN | MEAN | MAX |
| 00 | 0.5 | 0.5 | 0.5 |
| 05 | 0.5 | 0.5 | 0.5 |
| 10 | 0.5 | 0.5 | 0.5 |
| 15 | 0.5 | 0.5 | 0.5 |
| 20 | 0.5 | 0.5 | 0.5 |
| 25 | 0.5 | 0.5 | 0.5 |
| 30 | 0.4 | 0.4 | 0.5 |
| 35 | 0.4 | 0.4 | 0.4 |
| 40 | 0.4 | 0.7 | 1.1 |
| 45 | 0.4 | 1.7 | 3.6 |
| 50 | 0.4 | 3.6 | 7.5 |
| 55 | 0.5 | 6.8 | 13.4 |
| 60 | 0.9 | 11 | 20.9 |
| 65 | 0.7 | 16 | 29.8 |
| 70 | 4.2 | 22.7 | 40 |
| 75 | 20.6 | 45.1 | 66.8 |
| 80 | 10.4 | 38.4 | 64.2 |
| Book Spec | — | — | 20 |

PART NUMBER: '54F11 S/N 5–8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

SUPPLY CURRENT
vs
TOTAL DOSE

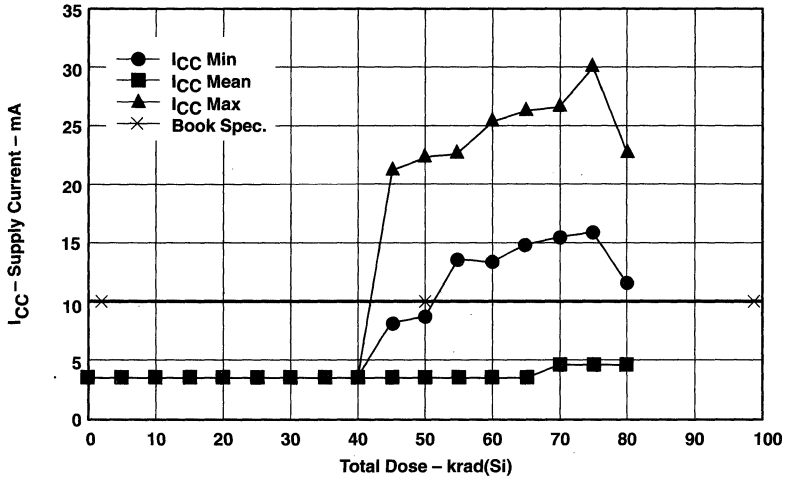



Figure 5

**Table 8. Supply Current vs Total Dose – '54F11**

| TOTAL DOSE/ krad(Si) | $I_{CCH}$ (mA) @ $V_{CC}$ = 5.5 V | | |
|---|---|---|---|
| | MIN | MEAN | MAX |
| 00 | 3.41 | 3.48 | 3.55 |
| 05 | 3.41 | 3.48 | 3.55 |
| 10 | 3.41 | 3.47 | 3.54 |
| 15 | 3.4 | 3.5 | 3.53 |
| 20 | 3.39 | 3.46 | 3.53 |
| 25 | 3.4 | 3.47 | 3.54 |
| 30 | 3.4 | 3.47 | 3.54 |
| 35 | 3.39 | 3.47 | 3.54 |
| 40 | 3.41 | 3.46 | 3.5 |
| 45 | 3.41 | 7.94 | 21.43 |
| 50 | 3.37 | 8.2 | 22.57 |
| 55 | 3.34 | 12.94 | 22.92 |
| 60 | 3.35 | 12.82 | 25.49 |
| 65 | 3.36 | 14.91 | 26.54 |
| 70 | 4.61 | 15.16 | 26.96 |
| 75 | 4.62 | 15.52 | 30.53 |
| 80 | 4.63 | 11.1 | 22.7 |
| Book Spec | — | — | 9.7 |

PART NUMBER: '54F11 S/N 5–8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

HIGH-LEVEL OUTPUT VOLTAGE
vs
TOTAL DOSE

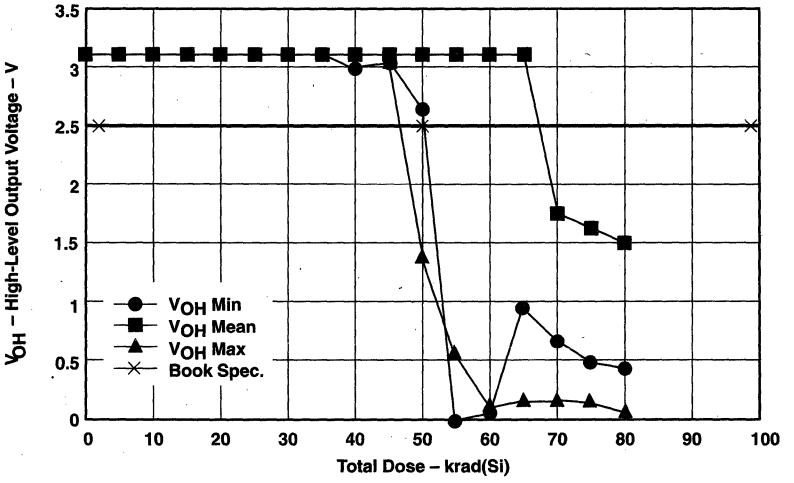



Figure 6

Table 9. High-Level Output Voltage vs Total Dose – '54F11

| TOTAL DOSE/ krad(Si) | $V_{OH}$ @ $I_{OH}$ = –1 mA | | |
|---|---|---|---|
| | MIN | MEAN | MAX |
| 00 | 3.063 | 3.066 | 3.069 |
| 05 | 3.064 | 3.067 | 3.072 |
| 10 | 3.064 | 3.068 | 3.073 |
| 15 | 3.065 | 3.069 | 3.074 |
| 20 | 3.065 | 3.069 | 3.074 |
| 25 | 3.065 | 3.069 | 3.074 |
| 30 | 3.065 | 3.069 | 3.074 |
| 35 | 3.065 | 3.07 | 3.077 |
| 40 | 3.011 | 3.056 | 3.077 |
| 45 | 3.069 | 3.073 | 3.082 |
| 50 | 1.411 | 2.657 | 3.075 |
| 55 | 0.551 | 0.035 | 3.076 |
| 60 | 0.076 | 0.032 | 3.073 |
| 65 | 0.15 | 0.994 | 3.073 |
| 70 | 0.15 | 0.654 | 1.719 |
| 75 | 0.15 | 0.512 | 1.597 |
| 80 | 0.051 | 0.469 | 1.523 |
| Book Spec | 2.5 | — | — |

General Information 1
Data Sheets 2
Application Report 3
Mechanical Data 4

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

**EXAMPLE:** **SN** **74F240** **DW** **R**

**Prefix**

| | | |
|---|---|---|
| Blank | = | (Standard product) |
| SN | = | Standard prefix |
| SNJ | = | JEDEC Publication 101, Class B |
| JANB | = | MIL-M-38510 Qualified |

**Unique Circuit Description**

MUST CONTAIN FIVE TO NINE CHARACTERS

(from individual data sheet)

**Package**

MUST CONTAIN ONE TO TWO LETTERS

| | | |
|---|---|---|
| D | = | plastic narrow-body small outline |
| DB | = | plastic shrink small outline |
| DW | = | plastic wide-body small outline |
| FK | = | ceramic chip carrier |
| J, JT | = | ceramic dual in line |
| N, NT | = | plastic dual in line |
| SC | = | plastic single in line |

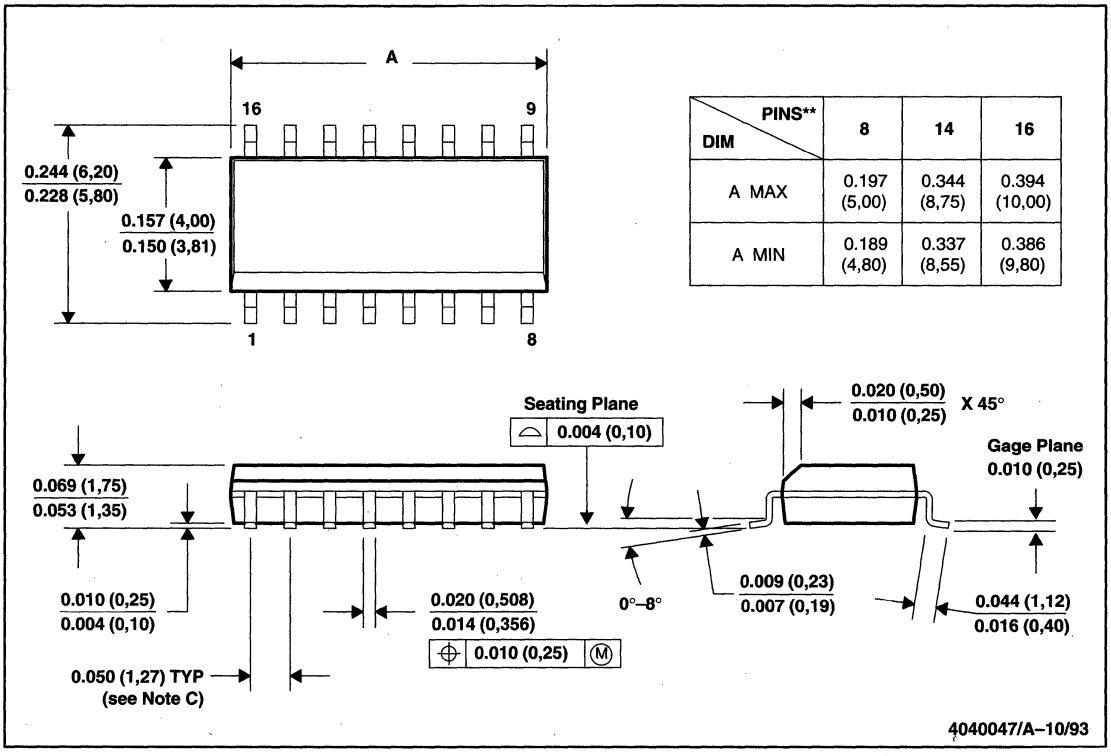
**Tape and Reel Packaging**

Must be designated by the letter R and valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

**D/R-PDSO-G****

**PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE**

**16-PIN SHOWN**



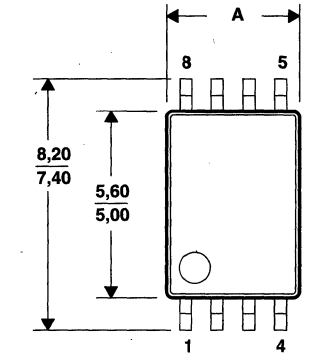

| DIM \ PINS** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

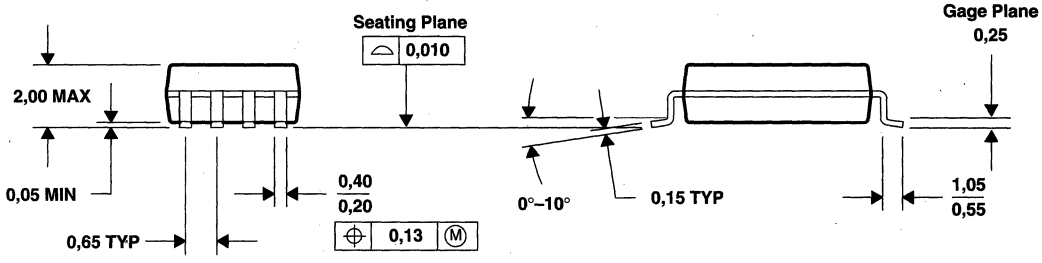
**DB/R-PDSO-G****

**PLASTIC SMALL-OUTLINE PACKAGE**

**8-PIN SHOWN**




| DIM \ PINS** | 8 | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|---|
| A MAX | 3,30 | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 2,70 | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

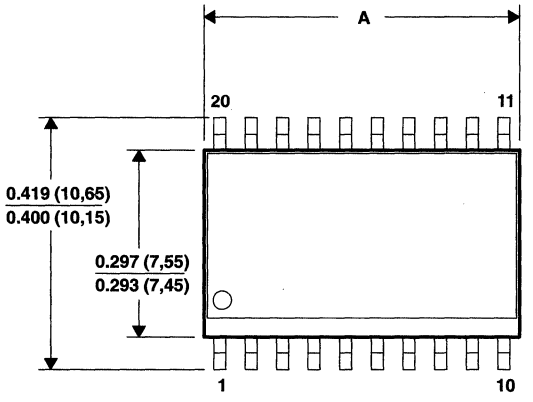



4040065/A–10/93

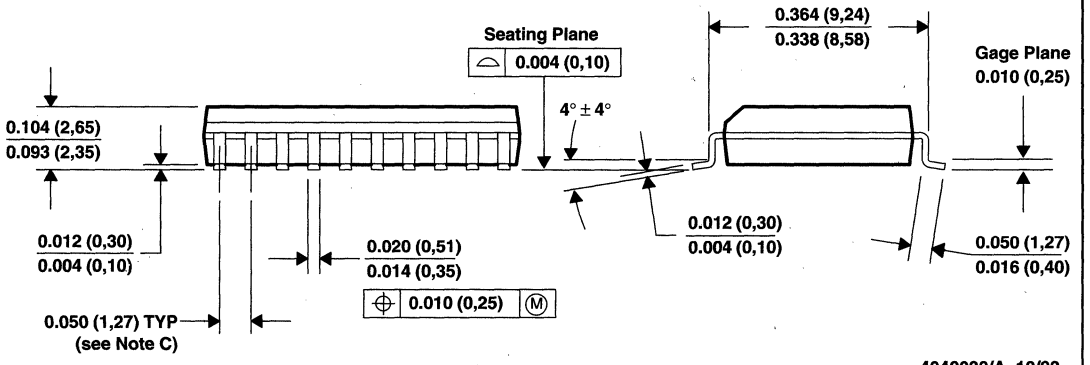
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0,15.

**DW/R-PDSO-G****
**20-PIN SHOWN**

**PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE**




| DIM \ PINS** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.602 (15,29) | 0.696 (17,68) |
| A MAX | 0.408 (10,36) | 0.508 (12,90) | 0.610 (15,49) | 0.704 (17,88) |



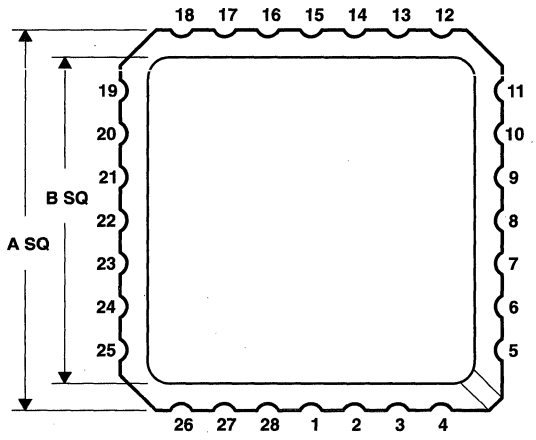

4040000/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

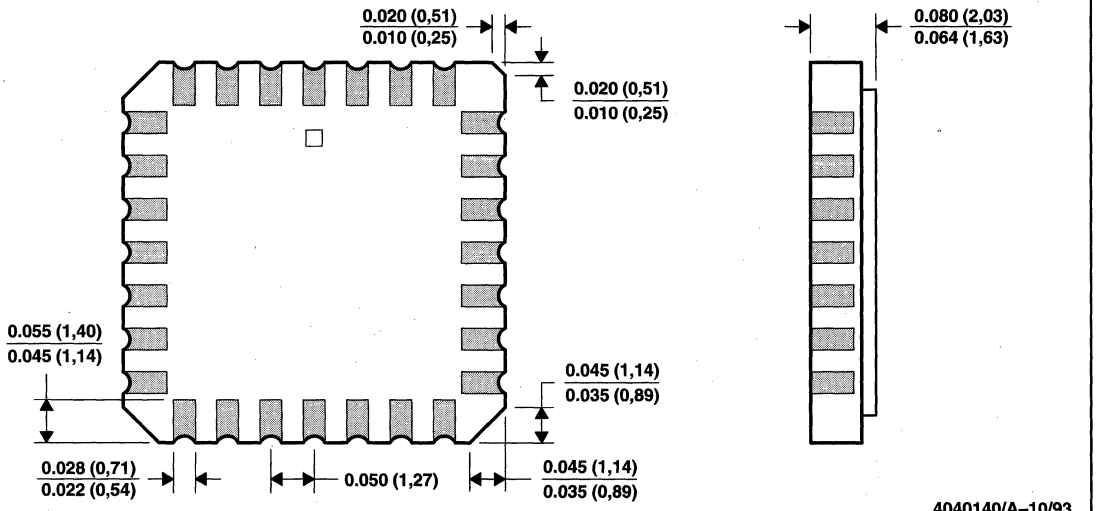
**FK/S-CQCC-N****

**28-TERMINAL PACKAGE SHOWN**

**LEADLESS CERAMIC CHIP CARRIER PACKAGE**




| JEDEC OUTLINE DESIGNATION | NUMBERS OF ** TERMINALS | A | | B | |
|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX |
| MS004CB | 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| MS004CC | 28 | 0.422 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| MS004CD | 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| MS004CE | 52 | 0.730 (18,78) | 0.761 (19,32) | 0.485 (12,58) | 0.560 (14,22) |
| MS004CF | 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| MS004CG | 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



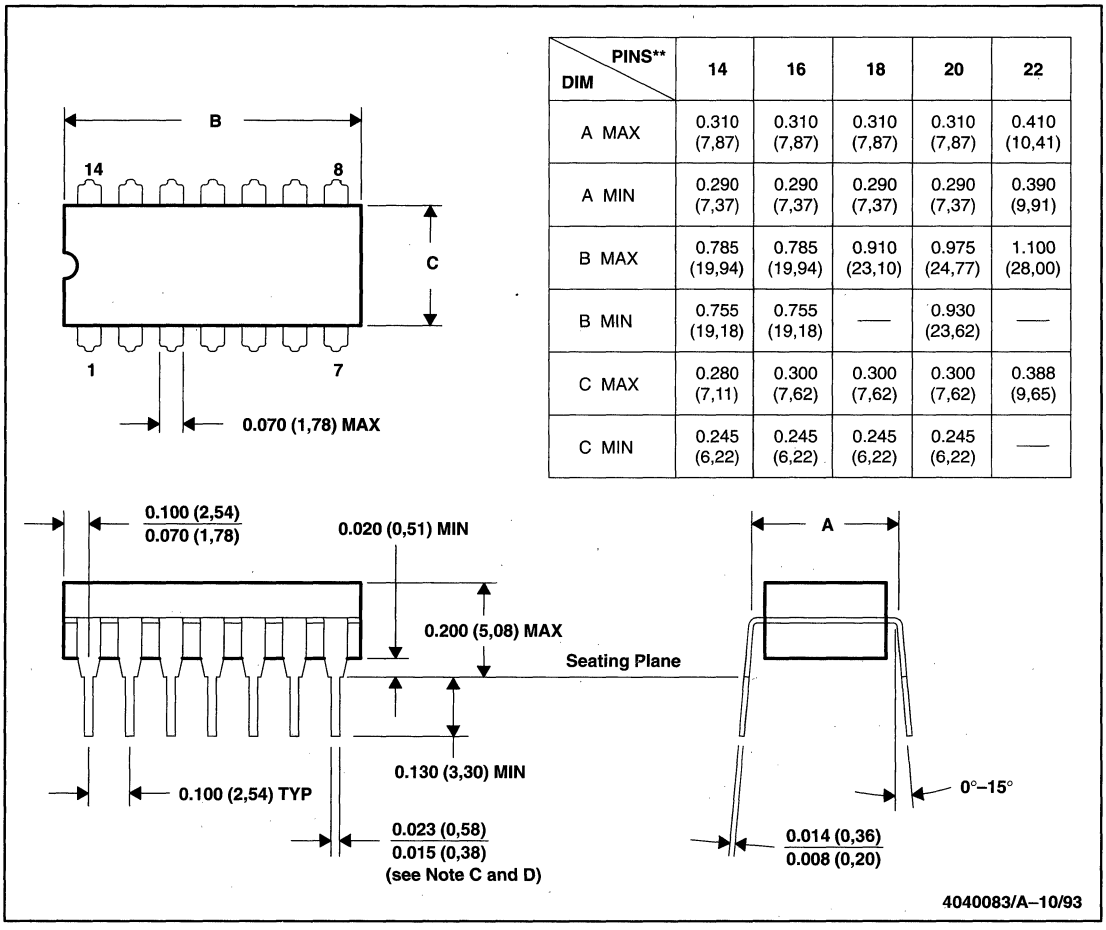

4040140/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Three-layer ceramic base with a metal lid and braze seal.
D. FK package terminal assignments conform to JEDEC Standards 1,2 and 11.
E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.

**J/R-GDIP-T****

**CERAMIC DUAL-IN-LINE PACKAGE**

**14-PIN SHOWN**



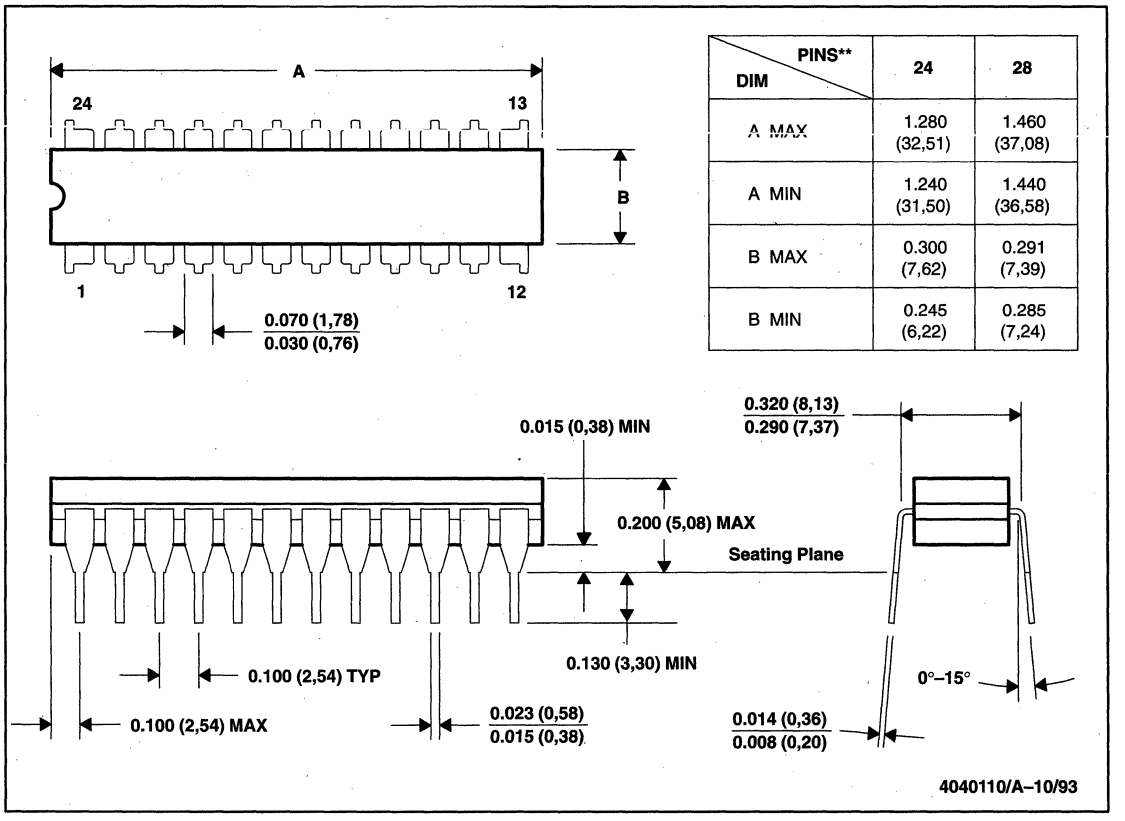

| DIM \ PINS** | 14 | 16 | 18 | 20 | 22 |
|---|---|---|---|---|---|
| A MAX | 0.310 (7,87) | 0.310 (7,87) | 0.310 (7,87) | 0.310 (7,87) | 0.410 (10,41) |
| A MIN | 0.290 (7,37) | 0.290 (7,37) | 0.290 (7,37) | 0.290 (7,37) | 0.390 (9,91) |
| B MAX | 0.785 (19,94) | 0.785 (19,94) | 0.910 (23,10) | 0.975 (24,77) | 1.100 (28,00) |
| B MIN | 0.755 (19,18) | 0.755 (19,18) | — | 0.930 (23,62) | — |
| C MAX | 0.280 (7,11) | 0.300 (7,62) | 0.300 (7,62) | 0.300 (7,62) | 0.388 (9,65) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.245 (6,22) | 0.245 (6,22) | — |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This dimension does not apply for solder-dipped leads.
D. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

**JT/R-GDIP-T****

**CERAMIC DUAL-IN-LINE PACKAGE**

**24-PIN SHOWN**

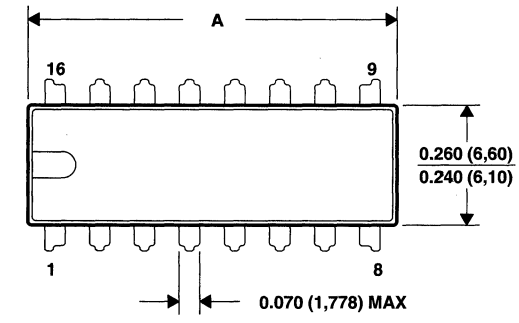



| DIM \ PINS** | 24 | 28 |
|---|---|---|
| A MAX | 1.280 (32,51) | 1.460 (37,08) |
| A MIN | 1.240 (31,50) | 1.440 (36,58) |
| B MAX | 0.300 (7,62) | 0.291 (7,39) |
| B MIN | 0.245 (6,22) | 0.285 (7,24) |

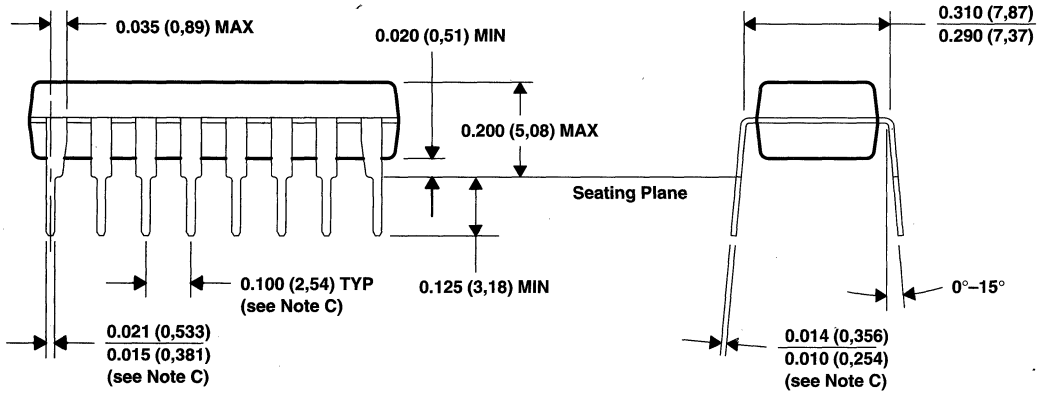
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is glass seal.

**N/R-PDIP-T**** **PLASTIC DUAL-IN-LINE PACKAGE**

**16-PIN SHOWN**




| DIM \ PINS** | 14 | 16 | 20 |
|---|---|---|---|
| A MAX | 0.780 (19,80) | 0.775 (19,69) | 0.975 (24,77) |
| A MIN | 0.710 (18,00) | 0.745 (18,92) | 0.940 (23,88) |



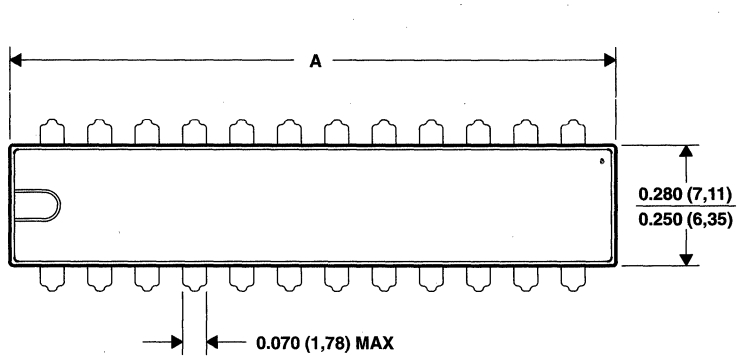

4040049/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

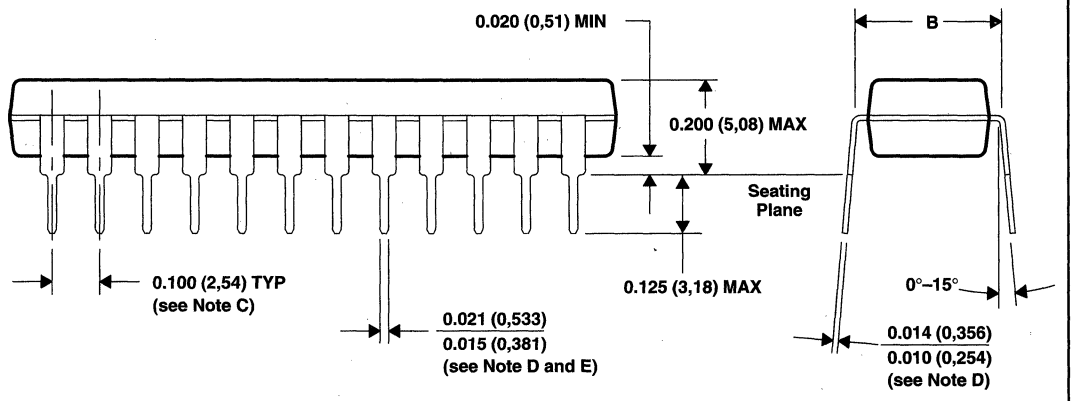
**NT/R-PDIP-T****

**PLASTIC DUAL-IN-LINE PACKAGE**

**24-PIN SHOWN**



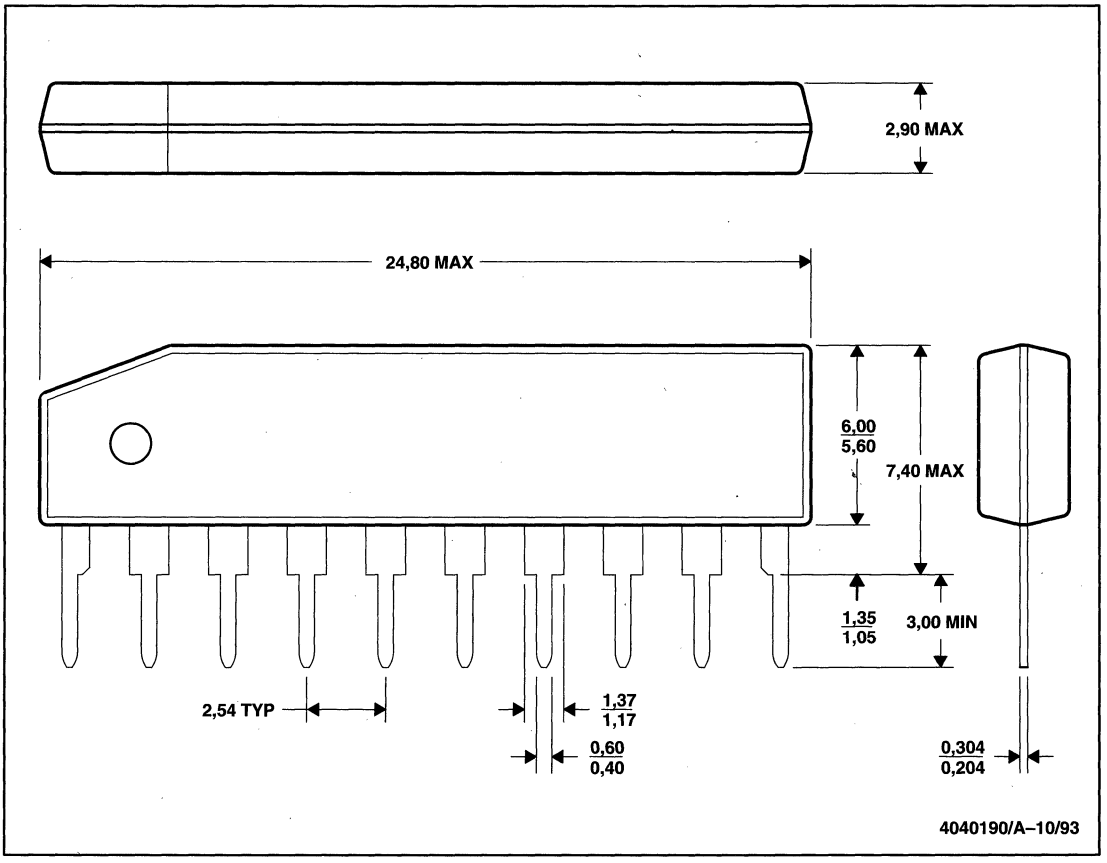

| DIM \ PINS** | 24 | 28 |
|---|---|---|
| A MAX | 1.260 (32,04) | 1.425 (36,20) |
| A MIN | 1.230 (31,24) | 1.385 (35,18) |
| B MAX | 0.310 (7,87) | 0.315 (8,00) |
| B MIN | 0.290 (7,37) | 0.295 (7,49) |




4040050/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder-dipped leads.
E. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

**SC/R-PSIP-T10** **PLASTIC SINGLE-IN-LINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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