



Low-Voltage Logic LV, LVC, LVT, LVTZ, ALVC, CBT, and GTL Families

Data Book

Data Book

Low-Voltage Logic

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Low-Voltage Logic Data Book



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INTRODUCTION

The 3.3-V era has arrived! The combination of continuous advancement in semiconductor wafer fabrication technologies and the proliferation of battery-powered computing devices has changed the system design methodologies of the past, and indeed our entire industry. This new era will bring an entirely new set of possibilities for computing and hand-held instruments. Products that will run faster, consume less power, and use fewer total system components than ever before. Products that will be smaller and lighter, yet maintain interface compatibility with existing industry standard bus architectures. Products that will in turn bring on the next era in the computer industry.

Welcome to the 1994 Texas Instruments Low-Voltage Logic Data Book. A single family of 3.3-V logic products could not possibly cover the diverse needs of all of the end equipment segments. Products ranging from hand-held point-of-sale terminals, notebook and laptop personal computers, low-power environmentally conscious desktop computers and peripherals, and high-performance RISC and CISC workstation platforms will all share the need for low-voltage technology, but will each have radically different price, performance, and feature requirements for the logic they will employ. As a response to these diverse needs, Texas Instruments has developed four independent logic families:

Low-Voltage HCMOS (LV) Low-Voltage CMOS (LVC) Low-Voltage Technology (LVT) Advanced Low-Voltage CMOS (ALVC)

These products span four generations of CMOS and BiCMOS process technologies and years of fine-pitch packaging and innovative circuit developments to deliver a set of products for each of these end-equipment segments. In addition to popular octal and Widebus™ bus-interface circuits, two of the families also include SSI and MSI logic functions to help streamline design and facilitate time to market. Voltage translators are also provided to bridge the gap between the 5-V and 3.3-V worlds as well as the CBT family of ultra high-speed bus switches which can be easily adapted to these mixed 3.3-V/5-V environments. Designers of high-speed backplane applications will have great interest in the GTL family of transceivers.

Some of the information in this data book is in product preview form. For more information on these products including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments field sales representative, authorized distributor, or call our Advanced Logic hotline at (214) 997-5202.

We hope you will agree that Texas Instruments has developed the most complete line of low-voltage logic products in the industry. We also hope that these products will meet your system and design needs.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i Input capacitance

The internal capacitance at an input of the device

Co Output capacitance

The internal capacitance at an output of the device

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{\rm pd} \ V_{\rm CC}^2 \ f + I_{\rm CC} \ V_{\rm CC}$.

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

∆I_{CC} Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

I_{CEX} Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_{\rm O} = 5.5 \text{ V}$.

I_{I(hold)} Input hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state.

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input.

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input.

Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and $V_{\rm CC}$ = 0 V

IOH High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} Low-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

^{*}Current out of a terminal is given as a negative value.



Off-state (high-impedance-state) output current (of a 3-state output) OZPU/PD

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

Access time ta

The time interval between the application of a specified input pulse and the availability of valid signals at an output

tc Clock cycle time

Clock cycle time is 1/f_{max}.

Disable time (of a 3-state or open-collector output) tdis

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, t_{dis} = t_{PHZ} or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling, so t_{dis} = t_{PLH}.

Enable time (of a 3-state or open-collector output) ten

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{OE}). For 3-state outputs, ten = tpzH or tpzL. Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHI}$.

Hold time th

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

Propagation delay time tpd

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level (tpd = tpH or tpl H)

tPHL Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

tPHZ Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

Propagation delay time, low-to-high level output **t**PLH

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

^{*}Current out of a terminal is given as a negative value



t_{PLZ} Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{IT} Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT}...

V_{IT} Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{\text{IT+}}$.



EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level

↓ = transition from high to low level

= value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)

Z = off (high-impedance) state of a 3-state output

a . . . h = the level of steady-state inputs A through H respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

 $\overline{\mathbb{Q}}_0$ = complement of \mathbb{Q}_0 or level of $\overline{\mathbb{Q}}$ before the indicated steady-state input

conditions were established

 Q_n = level of Q before the most recent active transition indicated by \downarrow or \uparrow

= one high-level pulse
= one low-level pulse

Toggle = each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, $\neg \neg \neg \neg \neg$, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)



Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS											OUTPUTS			
CLEAR	МО	DE	CLOCK	SERIAL			PARA	LLEL		۵.	Ω-			
CLEAR	S1 S0	SO	CLUCK	LEFT	RIGHT	Α	В	С	D	QA	QB	дС	QD	
L	Х	Х	Х	X	Х	Х	Х	Х	Х	L	L	L	L	
н	Х	X	L	×	X	Х	Х	Χ	Χ	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	
н	Н	Н	1	×	Х	a	b	С	d	а	b	С	d	
н	L	Н	1	×	Н	н	Н	Н	Н	н	Q_{An}	Q_{Bn}	QCn	
н	L	Н	1	X	L	L	L	L	L	L	Q_{An}	\mathtt{Q}_{Bn}	QCn	
н	Н	L	1	н	X	x	Х	Χ	Χ	QBn	QCn	\mathtt{Q}_{Dn}	н	
н	Н	L	↑	L	X	X	X	Х	Х	QBn	Q_{Cn}	Q_{Dn}	L	
н	L	L	Х	X	X	Х	X	X	Χ	Q _{A0}	Q _{B0}	Q _{C0}	Q_{D0}	

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A , data entered at B will be at Q_B , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B , the previous levels of Q_B and Q_C are now at Q_C and Q_D , respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

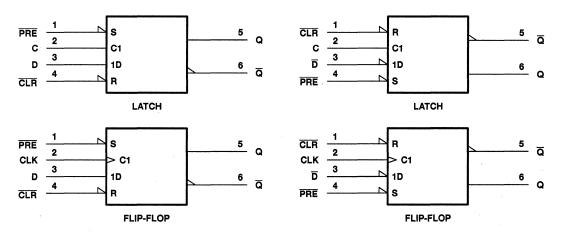


D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called preset (PRE). An input that causes a \overline{Q} output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and \overline{Q} exchange names, the preset and clear pins also exchange names. The polarity indicators (\triangleright) on \overline{PRE} and \overline{CLR} remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow. Figures 2, 3, 4, and 5 are derating curves for the DB package.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the LVL family. In general, the junction temperature for any device can be calculated using using the following equation.

$$T_J = R_{\Theta JA} \times P_T + T_A$$

where:

T_{.1} = virtual junction temperature

 $R_{A,IA}$ = thermal resistance, junction to free air

P_T = total power dissipation of the device (see Section 15, package thermal considerations)

 T_{Δ} = free-air temperature

JUNCTION-TO-AMBIENT THERMAL RESISTANCE

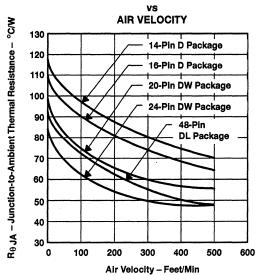
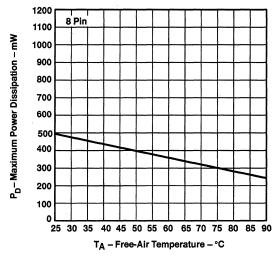


Figure 1

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)



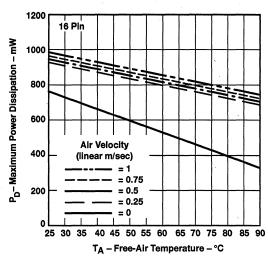
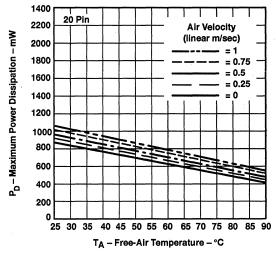


Figure 2

Figure 3



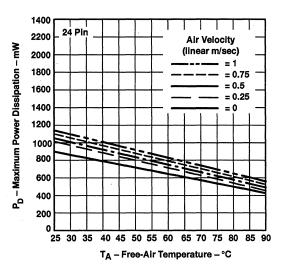


Figure 4

Figure 5

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type and list all available or planned options of that function. The technology columns identify the appropriate family and a particular data book where more information can be found. The applicable literature number, composed of either seven or eight alphanumeric characters, can be found at the lower right-hand corner on the back cover of each publication.

List of additional Advanced System Logic data books:

ABT Devices†	Advanced BiCMOS Technology	SCBD002A
AC and ACT Devices	Advanced CMOS Logic Data Book	SCAD001C
Advanced Logic Devices	Advanced Logic and Bus-Interface Data Book	SCYD001
ALS and AS Devices†	ALS/AS Logic Data Book	SDAD001B
ATM and SONET Devices†	ATM and SONET Product Information	SDNS023
BCT Devices	BiCMOS Bus-Interface Logic Data Book	SCBD001B
CDC Devices	Clock-Distribution Circuits Data Book	SCAD004
F Devices	F Logic (SN54/74F) Data Book	SDFD001B
FIFO Devices†	High-Performance FIFO Memories Data Book	SCAD003A
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
SCOPE™ Devices†	SCOPE™ Product Information	SSYV001
SPICE I/O Models	Advanced Bus Interface SPICE I/O Models	SCBD004
Std TTL, LS, and S Devices	TTL Logic Data Book	SDLD001A

[†] Updated data book planned for this technology.

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GATES

Positive-NAND Gates

DESCRIPTION	CUTDUT	TVDE					TE	CHNOL	OGY				
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT	LV	LVC
		′30	~	~	~								
8-Input		′11030						~	~				
13-Input		′133	~			~							
Dual 2-Input		′8003	~										
		′20	~	~	~	~							
Dual 4-Input		′40	~										
	′11020						~	~					
Triple 3-Input		′10	~	~	~	~							+
		′1010	~										
		′11010				}		~	~				
		′00	~	~	~	1	~					~	+
		′11000						~	~				
		′37	V										
Quad 2-Input	ОС	′38	~		~								
		′132				~							
		′11132						~	~				
		′1000		~									
Hex 2-Input		′804	V	~									
Ound Oleman	ОС	′01	V			~							
Quad 2-Input	00	′03	~			~							-

Positive-AND Gates

DESCRIPTION	ОИТРИТ	TYPE					TE	CHNOLO	OGY				
DESCRIPTION	COIPOI	ITPE	ALS	AS	F	HC	нст	AC	ACT	ВСТ	ABT	LV	LVC
Quad 2-Input	oc	′09	~			~							
Quad 2-Input		′7001				~							
Dual 4 land		′21	~	V	~	~							
Dual 4-Input		′11021						~	~				
Triple O long st	′11	′11	~	~	~	~							
Triple 3-Input		′11011						~	~				
		′08	~	~	~	~	~					~	+
Quad 2-Input		′1008		V									
		′11008						~	~				
Hex 2-Input		′808		~									



 [✓] Product available in technology indicated
 + New product planned in technology indicated

GATES

Positive-OR/NOR Gates

DESCRIPTION	ОИТРИТ	TVDE					TE	CHNOLO	OGY				
DESCRIPTION	COIPOI	TYPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	LV	LVC
Triple 3-Input		′4075				~							
Quad 2-Input		′32	~	~	~	~	~					~	+
		′1032		V									
	′11032						~	~					
		′7032				~		,					
Hex 2-Input		′832	~	V		~							
Dual 5-Input		′260			~								
Trials O land		′27	V	~	~	~							
Triple 3-Input		′11027						~	~				
		′02	~	~	~	~	~					~	+
0 101 1	OC .	′33	~										
Quad 2-Input		′7002				V							
		′11002						~	~				
Hex 2-Input		′805	~	~		~							

OR/NOR Gates

DECODIDION	OUTPUT	TYPE					TEC	CHNOLO	OGY				
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	LV	LVC
Quad 2-Input Exclusive-OR Gates		′86	~	~	~	~							+
With Totem-Pole Outputs		′11086						~	~				
Quad 2-Input Exclusive-OR Gates	ос	′136	V										
	OD	′266				~							
Quad 2-Input Exclusive-NOR Gates		′810	~										
Exolusive HOTT dates	ОС	′811	~										

AND-OR Gates

DESCRIPTION	OUTPUT	TYPE				TE	CHNOLO	GY			
DESCRIPTION	COIPOI	ITPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Dual 2-Wide 2-Input, 3-Input		′51			~						



 [✓] Product available in technology indicated
 + New product planned in technology indicated

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

DECODIDATION	CUITDUIT	TVDE					TE	CHNOL	OGY				
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	LV	LVC
		′04	~	~	~	~	~					~	+
		′U04				~						~	+
		′11004						~	~				
Han bereaten	ОС	′05	~			~							
Hex Inverters		′14				~						V	+
		′11014						~	V				
		′1004	~	~									
		′1005	~										
		′11034						~	V				
Hex	oc	′35	~										
Noninverters		′1034	~	~									
	OC	′1035	~										

 [✓] Product available in technology indicated
 + New product planned in technology indicated

Buffers/Drivers

DESCRIPTION	ОИТРИТ	TYPE						TE	CHNOL	OGY					
DESCRIPTION	COIPOI	ITPE	ALS	AS	F	нс	HCT	AC	ACT	ВСТ	ABT	LVT	LV	LVC	ALVC
Quad Buffers/Drivers	38	′125			~	1	~			~	~	~		+	
		′126			~	V				~	~			+	
Noninverting	38	′365				1									
Hex Buffers/Drivers		′367				~								<u> </u>	
Inverting Hex Buffers/Drivers	38	′368				~		·							
		′241	~	~	~	~	~			~	~			+	
		′11241						~	~						
		′25241									+				
		′244	V	~	V	V	~			~	~		V	+	
	38	′244A										V			
Noninverting		′11244						~	~						
Octal Buffers/Drivers	ĺ	′1244	~												
		′25244								~	+				
		′541	V		· V	V	~			~	V			+	
		′757		~						V					
	ос	′760	~	~						~					
		′25760								+					
		′240	~	~	~	~	~			~	~	~	~	+	
		′11240						~	V						
		′1240	V												
Inverting	38	′25240								~					
Octal Buffers/Drivers		′466	~												
	ŀ	′540	~			~	~			~	~			+	
		′756	~	~						~					
	oc	′763	~	~											
Inverting and	38	′230		~										<u> </u>	
Noninverting															
Octal Buffers/Drivers	oc	′762		~										ļ	
Triple 4-Input OR/NOR Drivers		′11802							~						
Marchania Pari		′827									~			~	
Noninverting 10-Bit Buffers/Drivers	38	′11827						~	~						
TO DICEONO DICTOR		′29827	~							~					
		′828									+			+	
Inverting 10-Bit Buffers/Drivers	38	′11828						٧	~						
. O Dit Danois/Directs		′29828	~							~					
		′16241							~		~			+	
Noninverting	00	′16244						~	1		~			+	+
16-Bit Buffers/Drivers	38	′16244A										1			
		′16541							V		V			+	

[✓] Product available in technology indicated

⁺ New product planned in technology indicated



Buffers/Drivers (Continued)

DECODIDEION	ОИТРИТ	TVDE						TE	CHNOL	OGY					
DESCRIPTION	OUIPUI	TYPE	ALS	AS	F	нс	нст	AC	ACT	ВСТ	ABT	LVT	LV	LVC	ALVC
Inverting	200	′16240						V	~		~			+	+
16-Bit Buffers/Drivers	3S	′16540							~		~				
Noninverting 18-Bit Buffers/Drivers	38	′16825							~		~				+
Inverting 18-Bit Buffers/Drivers	38	′16826									+				
Noninverting 20-Bit Buffers/Drivers	38	′16827							V		V				+
Inverting 20-Bit Buffers/Drivers	38	′16828									+				+
Octal Buffers/Drivers With Input Pullup Resistors		′746	~												

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DECODIDEION	CUTDUT	TVDE				TECHNO	DLOGY			
DESCRIPTION	OUTPUT	TYPE	AC	ACT	ВСТ	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit	38	′16500					~			+
Universal Bus Transceivers (UBT™)	35	′16500B				V				
		′16501				~	V		+	+
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	38	′16600				~				+
Oniversal Dus Transceivers (ODT)		′16601				~				+
Noninverting 36-Bit Universal Bus Transceivers (UBT™)	38	′32501				V				
Noninverting 16-Bit Tri-Port Universal Bus Exchangers (UBE™)	38	′32316				v				
Noninverting 18-Bit Tri-Port Universal Bus Exchangers (UBE™)	38	′32318		,		~				
		′162500				V				
18-Bit Universal Bus Transceivers	00	′162501				~				
(UBT™) With Series Resistors on B Port	3S	′162600				+				
		′162601				~				
SCOPE™ 18-Bit Universal Bus Transceivers (UBT™)	38	′18502				~	+			
SCOPE™ 20-Bit Universal Bus Transceivers (UBT™)	3S	′18504				~	+			

[✔] Product available in technology indicated



⁺ New product planned in technology indicated

Bus Transceivers

DESCRIPTION	ОИТРИТ	TYPE						TE	CHNOL	OGY					
DESCRIPTION	JUIPUI	ITPE	ALS	AS	F	НС	HCT	AC	ACT	вст	ABT	LVT	LV	LVC	ALVC
Noninverting Quad Transceivers	38	′243	~		~			į,							
Inverting	ОС	′758	~												
Quad Transceivers	38	′242			~										
		′245	~	~	~	~	V			V	~		~	+	
		′245A										V			
		′1245	~												
	38	′11245						V	V						
Noninverting		′25245								V	~				
Octal Transceivers		′645	~	~		~	~								
		′1645	~											1	
	00	′621	~	,	~										
	oc	′641	~	~											
	OC/3S	′639	~	V											
		′620	~							~	V			ļ	
		[′] 623	~	~	1	~	~			~	~				
_		′11623							V						
	38	′640	V	~		1				~	1				
Inverting		′1640	V												
Octal Transceivers		′11640							1						
		′642	~						٠.						-
	oc	′25642				 	 		 	~				17	
	OC/3S	′638	~	~		 			<u> </u>		l				
Noninverting		′863				 					V			+	
9-Bit Transceivers	38	′29863	~							~	<u> </u>			 	
Inverting 9-Bit Transceivers	38	′29864			-					~					
Noninverting		′861				1					+	l		 	
10-Bit Transceivers	38	′29861				1				~		l		<u> </u>	
Inverting 10-Bit Transceivers	38	′29862								~					
		′16245						~	V		~			+	+
Noninverting	38	′16245A				t					~	1		†	†
16-Bit Transceivers		′16623						~	~		~	 		†	
Inverting		′16640				†		~	1		~			İ	
16-Bit Transceivers	38	′16620						~	1		+	 		<u> </u>	
Noninverting 18-Bit Transceivers	38	′16863							~		~				
Inverting 18-Bit Transceivers	38	′16864									+				

 [✓] Product available in technology indicated
 + New product planned in technology indicated



Bus Transceivers (Continued)

DESCRIPTION	ОИТРИТ	TYPE						TE	CHNOL	OGY					
DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	LVT	LV	LVC	ALVC
Noninverting 20-Bit Transceivers	38	′16861							1		+				
Inverting 20-Bit Transceivers	38	′16862									+				
		′11470							~						
		′543			1					~	~	~		+	
		′11543							~						
		′646	~	~		~	~			~	~	~		+	
	38	′646A									~				
Noninverting Octal Registered	33	′11646						~	~						
Transceivers		′652	~	~		~	~			~	~	~		+	
		′11652						V	~						
		′2952								~	+	~		+	
		′2952A									~				
	OC/3S	′653	~												
	00/33	′654	1												
		′544								~	+			+	
		′11544							V						
Inverting Octal Registered	38	′648	1	~						~	+				
Transceivers	00	′11648							1						
		′651	1	~						~	~				
		′2953	<u> </u>			<u> </u>				~	+				
		′16470							~		~				
Noninverting		′16543	<u> </u>					~	~		~	~		+	+
16-Bit Registered	38	′16646						~	~		~	~		+	+
Transceivers		′16652						~	~		~	+		+	+
		′16952							~		~	~		+	+
		′16471									+				
Inverting		′16544							~		+			+	
16-Bit Registered	3S	′16648							~		+				
Transceivers		′16651							~		+				
		′16953									+				



 [✓] Product available in technology indicated
 + New product planned in technology indicated

Bus Transceivers (Continued)

DESCRIPTION	OUTDUT	TYPE						TE	CHNOL	OGY					
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	нс	HCT	AC	ACT	вст	ABT	LVT	LV	LVC	ALVC
		′16472						~							
		′16474							~						
Noninverting	-00	′16500									~	~		+	+
18-Bit Registered Transceivers	38	′16501									~	+		+	+
		′16600									~				+
		′16601									~				+
Inverting 18-Bit Registered Transceivers	38	′16475							~						
Noninverting 36-Bit Transceivers	38	′32245									+				
Noninverting 36-Bit Registered	38	′32501									V				
Transceivers		′32543	ļ								-				
		′657			V					~	+				
		′659					~								
		′833									+				
0 10 D'' D	38	′834									+				
8-/9-Bit Bus Transceivers		′853									+				
With Parity		′854									+				
Checkers/ Generators		′899								~					
Generalors		′29833	V							~					
	3S/OC	′29834								~					
	35/00	′29853	V							1					
		′29854	~							~					
Dual 8-/9-Bit Bus Transceivers		′16833							~		~				
With Parity Checkers/	38	′16657							~		~				
Generators		′16853									~				
Universal Transceivers/Port Controllers	38	′856		~											
Noninverting 16-Bit Tri-Port Registered Bus Exchangers	38	′32316													
Noninverting 18-Bit Tri-Port Registered Bus Exchangers	38	′32318									,				

[✔] Product available in technology indicated



⁺ New product planned in technology indicated

MOS Memory Drivers/Transceivers

DESCRIPTION	ОИТРИТ	TVDE						TECH	NOLOG	Υ				
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	нс	HCT	AC	ACT	вст	ABT	LVT	LVC	ALVC
Octal Transceivers With Series Resistors on Output	38	′2623		~										
		′2240	~							~	~			
Octal Buffers/Drivers With	38	′2241								~	~			
Series Resistors on Output	35	′2244								~	V			
		′2541	~									,		
Octal Transceivers With Series Resistors on B Port	38	′2245								~	+			
Octal Latches With Series Resistors on Output	38	′2574								+				
10-Bit Buffers/Drivers With	00	′2827								~				
Series Resistors	38	′2828								~				
		′2410				,				~				
11-Bit Buffers/Drivers With	38	′2411								+				
Series Resistors	35	′5400									~			
		′5401									~			
12-Bit Buffers/Drivers With	38	′5402									~			
Series Resistors	33	′5403									~			
16-Bit Buffers/Drivers With	38	′162240									+			
Series Resistors	33	′162244									~	+	+	+
16-Bit Transceivers With Series Resistors	38	′162245									~	+	+	+
18-Bit Universal Bus		′162500									+			
Transceivers	38	′162501									+			+
(UBT™) With Series	35	′162600									+			
Resistors on B Port		′162601									V			+
12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port	38	′162260									v			

[✔] Product available in technology indicated



⁺ New product planned in technology indicated

TESTABILITY BUS-INTERFACE CIRCUITS

JTAG/IEEE 1149.1 Testability Circuits

DESCRIPTION	NO. OF	OUTPUT	TYPE				TECHN	IOLOGY			
DESCRIPTION	BITS	OUIPUI	ITPE	F	HC	HCT	AC	ACT	ВСТ	ABT	LVT
D. #/D.:		38	′8240A						~		
Buffers/Drivers	8	35	′8244A						~		
		200	′8245							~	
Transceivers	8	3S	′8245A				Υ.		~		
	18	38	′18245							~	+
Transparent Latches	8	38	′8373A						~		
Flip-Flops	8	38	′8374A						V		
			′8543								
	8	38	′8646							~	
	8	35	′8652							~	
Deviatered Transactives			′8952							~	
Registered Transceivers			′18502							~	+
	18	38	′18646							~	
			′18652							+	
	20	38	′18504							~	+
Test Bus Controllers		38	′8990					~			
Digital Bus Monitors		38	′8994					~			
Scan Path Linkers	4	38	′8997					V			
With Identification Buses	8	38	′8999					V			

[✔] Product available in technology indicated

⁺ New product planned in technology indicated

Flip-Flops

DESCRIPTION	OUTPUT	TYPE						TE	CHNOL	.OGY					
DESCRIPTION	COTPOT	ITPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	LVT	LV	LVC	ALVC
		′73				~				<u> </u>					
u.		′76				~									
		′109	1	~	~	~									
Dual J-K		′11109						~	~						
Edge Triggered		′112	1		1	~			<u> </u>					+	
		′11112						~	~						
		′113	1			1									
		′114	~												
Dual D-Type		′74	~	V.	~	~	~						~	+	
Duai D-Type		′11074						~	~						
Dual D-Type		′7074				1									
With 2-Input		′7075				~									
NAND/NOR Gates		′7076				~									
		′874	~	~											
Dual 4-Bit D-Type	38	′11874							~						
Edge Triggered	33	′876	~	~											
		′879	~	1											
		′173				~									
Quad D-Type		′175	~	~	~	~									
		′11175						~	~						
		′174	~	~	~	~							~		
Hex D-Type		′11174						>	~						
		′378			~	~									
		′374	~	~	~	~	~			~	~		+	+	
Octal D-Type True Data	38	′11374						~	~						
		′574	~	٧	~	~	~			~	~	~	+	+	
		′273	~			~	~				~	~	+		
Octal D-Type True Data		′11273						~	~						
With Clear	38	′575	~	~											
	33	′874	~	1											
Octal D-Type		′377			V	~	~				~				
True Data With Clock Enable		′11377						~	~						
		′534	~	~		~				~	~				
		′11534						~	~						
Octal D-Type Inverting	38	′564	~												
mverung		′576	~	~											
		′29826								V					1



 [✓] Product available in technology indicated
 + New product planned in technology indicated

Flip-Flops (Continued)

DESCRIPTION	ОИТРИТ	TYPE						TE	CHNOL	OGY					
	OUIPUI	ITPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT	LVT	LV	LVC	ALVC
Octal Dual-Ranked True Data	38	′4374		V											
Octal Inverting		′577	~												
With Clear	3S	′879	~	~											
Octal Inverting With Preset	38	′876	V	٧											
		′825		~											
Octal True Data	38	′11825							~						
		′29825								~					
9-Bit True Data	38	′823		~							~			+	
	35	′29823	~							~					
O Dit Invention	38	′824		~			′								
9-Bit Inverting	33	′29824	1												
		′821		>							~			+	
10-Bit True Data	38	′1821		~											
10-bit ffue Data	33	′11821							~						
		′29821	<							~					
10-Bit Inverting	38	′29822								~					
16-Bit D-Type True Data With Clock Enable		′16377					7				+				
16-Bit Noninverting	38	′16374						~	V		~	~		+	+
16-Bit Inverting	38	′16534									+				
18-Bit Noninverting	38	′16823							~		~				+
20-Bit Noninverting	38	′16821							~		~				+

 [✓] Product available in technology indicated
 + New product planned in technology indicated

Latches

DESCRIPTION OF BITS		OUTPUT	TYPE						TE	CHNOL	.OGY					
		OUIPUI	ITPE	ALS	AS	F	нс	нст	AC	ACT	вст	ABT	LVT	LV	LVC	ALVC
Bistable 4			′75				~									
	4		′375				~									
D-Type Edge Triggered Inverting and Noninverting	8		′996													
D-Type	8	38	′990	~												
Transparent Readback	9	38	′992	~												
Latch, True	10	38	′994	V												
D-Type Transparent With Clear, True Outputs	8	38	′666	v												
D-Type Transparent With Clear, Inverting Outputs	8	38	′667	v												
8		′373	~	~	~	~	~			~	~		+	+		
	8	38	′11373						~	~						
D-Type Transparent			′573	~	~	1	~	~			~	~	~	+	+	
True	16	38	′16373						~	~		~	~		+	+
			′16373A							ļ		~				
	32	38	′32373				ļ					+				
D-Type Dual 4-Bit	8	8 38	′873	~	~											
Transparent True	_		′11873						~							
			′533	~	~	ļ					~	~				
D-Type	8	38	′11533				ļ		~	~						
Transparent Inverting			′563	~		ļ	~			ļ						
inverting			′580	~	~					ļ						
	16	38	′16533									+				
Dual 4-Bit Transparent Inverting	8	38	′880	~	~											
2-Input Multiplexed	8	38	′604				~									
Addrospable	8	28	′259	~			~									
Addressable	0	Q	′4724				V									



 [✓] Product available in technology indicated
 + New product planned in technology indicated

Latches (Continued)

DESCRIPTION	NO.			TECHNOLOGY												
	OF BITS	OUTPUT	TYPE	ALS	AS	F	нс	нст	AC	ACT	вст	ABT	LVT	LV	LVC	ALVC
D-Type True Inputs			′845	~												
	8	38	′29845	~												
			′843	~	~							~			+	
	9	38	′1843		~											
			′29843								~					
	10	00	′841	~	~							+			+	
	10	38	′29841	~							V					
	18	38	′16843									+				+
	20	38	′16841							~		~				+
		00	′846	~												
	8	38	′29846								~					
D-Type Inverting Inputs	9	38	′29844								V					
mirchang mpats	10	20	′842	V	~											
	10	38	′29842	1												

 [✓] Product available in technology indicated
 + New product planned in technology indicated

REGISTERS

Shift Registers

DESCRIPTION	NO. OF	OUTDUT	TYPE	TECHNOLOGY										
	BITS	OUTPUT		ALS	AS	F	HC	нст	AC	ACT	ВСТ	LV		
	1		′194		~									
Parallel In,	4		′11194						~	~				
Parallel Out, Bidirectional			′299	~		~								
	8		′323	~										
Parallel In, Parallel Out	4		′195		~									
Serial In, Parallel Out	8		′164	~			~					+		
Davellel In Cariel Oct	8		′165	~			~							
Parallel In, Serial Out			′166	~			~							
Serial In, Parallel Out	8		38	′594				~						
With Output Latches	8	35	′595				~							
Parallel Out	10		′11898						~	~				
Nania vadia a	8	38	′299	~										
Noninverting	9	38	′29823	~										

Register Files

DESCRIPTION	ОИТРИТ	CUTPUT	TYPE	TECHNOLOGY											
		ITPE	ALS	AS	F	HC	HCT	AC	ACT	вст	ABT				
Dual 16 Word × 4 Bits	38	′870	V												
		′871		~											

 [✓] Product available in technology indicated
 + New product planned in technology indicated

COUNTERS

Synchronous Counters – Positive Edge Triggered

DECODIDATION	PARALLEL	TYPE				TECHN	OLOGY		,	
DESCRIPTION	LOAD	ITPE	ALS	AS	F	нс	HCT	AC	ACT	ВСТ
4-Bit Decade Up/Down	Sync	′568	V							
		′161	~	· V	~	~				
4-Bit Binary	Sync	′163	~	~	~	~				
		′561	~							
	Sync	′169	~	~	~					
		′569	~							
		′8169	~							
4-Bit Binary Up/Down		′191	~			~				
	Async	′11191						V	~	
		′193	~			~				
8-Bit Up/Down	Sync Clear	′869	~	~						
	Async Clear	′867	~	~						
		′11867							~	
Divide-by-10	Sync	′4017				~				

Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DECODIDATION	PARALLEL	TVDE				TECHN	OLOGY			
DESCRIPTION	LOAD	TYPE	ALS	AS	F	НС	НСТ	AC	ACT	ВСТ
Dual 4-Bit Binary	None	′393				~				
12-Bit Binary	Sync	′4040				~				
		′4020				~				
14-Bit Binary	Sync	′4060				~			-	
		′4061				~				

8-Bit Binary Counters With Registers

DESCRIPTION	PARALLEL	TYPE	TECHNOLOGY									
DESCRIPTION	LOAD		ALS	AS	F	HC	HCT	AC	ACT	BCT		
Parallel Register Outputs	00	′590				~						
	3S	′11590						~	~			
Parallel Register Inputs	38 "	′11593						~	~			

[✓] Product available in technology indicated

⁺ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	OUTPUT	TYPE					TEC	CHNOLO	OGY				
DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	LV	LVC
		′157	V	~	~	~	~						+
		′11157						~	~				
		′158	~	~	~	~							
		′11158						~	~				
Quad 2-to-1		′298		~									
		′257	~	~	~	~	~						+
	38	′11257						~	~				
	35	′258	~	~	~	~							
		′11258							~				
		′153	~	V	~	~							
		′11153						~	~				
Dual 4-to-1		′352	~										
		′253	~	~	~	~							
	38	′11253						~	~				
	35	′353		~									
		′11353							~				
Hex 2-to-1 Universal Multiplexer	38	′857	V										
		′151	~	~	~	~							
		′11151						~	~				
8-to-1		′251	~		~	~							
		′11251						~					
		′354				1							
		′250		~									
16-to-1	38	′850		V.									
		′851		~									
Full BCD		′147				~							
Cascadable Octal		′148				~							

[✓] Product available in technology indicated



⁺ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Decoders/Demultiplexers

DECODIDATION	CUIDUIT	TVDF					TEC	HNOL	OGY				
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	НС	нст	AC	ACT	ВСТ	ABT	LV	LVC
Dual 2-to-4		′239				~							
		′139	~			V	~						+
Dual 2-to-4		′11139						~	~				
	ОС	′156	~										
		′138	V	~	~	~	~					~	+
0.45.0		′11138						~	~				
i-to-8		′238					~						
		′11238						~	~				
3-to-8 With		′131		~									
Address Registers		′137	~			~							+
3-to-8 With Address Latches		′237				~							
4-to-10 BCD-to-Decimal		′42				~							
4-to-16		′154				~							
-to-16 With ddress Latches		′4514				V							
		′4515				~							
Dual 2-to-4 for Battery Backed-Up Memories		′2414								1			

Shifters

DESCRIPTION	ОИТРИТ	TYPE				TE	CHNOLO	GY			
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Shifter	38	′350			V						

[✔] Product available in technology indicated

⁺ New product planned in technology indicated

COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

			DESC	RIPTIC	N			TVDE				TECHN	OLOGY	,		
INPUT	P=Q	P=Q	P>Q	P>Q	P <q< th=""><th>OUTPUT</th><th>ENABLE</th><th>TYPE</th><th>ALS</th><th>AS</th><th>F</th><th>НС</th><th>нст</th><th>AC</th><th>ACT</th><th>ВСТ</th></q<>	OUTPUT	ENABLE	TYPE	ALS	AS	F	НС	нст	AC	ACT	ВСТ
	Yes	No	No	No	No	ОС	Yes	′518	~							
8-Bit With	NI-	V		NI-	No	00	V	′520	~		V					
20-kΩ	No	Yes	No	No	INO	28	Yes	′11520						~	V	
Pullup	No	Yes	No	No	No	ОС	Yes	′522	~							
	No	Yes	No	Yes	No	2S	No	′682				~				
	Yes	No	No	No	No	ОС	Yes	′519	~							
	NI	\/	NI-	NI-		00		′521	~		~					
8-Bit Standard	No	Yes	No	No	No	2S	Yes	′11521						~	~	
Otandard	No	Yes	No	Yes	No	2S	No	′684				~				
	No	Yes	No	No	No	2S	Yes	′688	~			~				
8-Bit Latched P	No	No	Yes	No	Yes	28	Yes	′885		V						
8-Bit Latched P and Q	Yes	No	Yes	No	Yes	L	Yes	′866		~						

Address Comparators

DESCRIPTION	OUTPUT	TYPE		,		TE	CHNOLO	GY			
DESCRIPTION	ENABLE	ITPE	ALS	AS	F	нс	HCT	AC	ACT	вст	ABT
16-Bit to 4-Bit	Yes	′677	~								,
12-Bit to 4-Bit	Yes	′679	~								

Parity Generators/Checkers

DESCRIPTION	NO. OF	TYPE				TE	CHNOLO	GY			
DESCRIPTION	BITS	ITPE	ALS	AS	F	HC	нст	AC	ACT	вст	ABT
		′280	V	V	~	~					
0.14/5		′11280						7	~		
Odd/Even	1 -	′286		~							
		′11286						~	~		

[✔] Product available in technology indicated



⁺ New product planned in technology indicated

BUS SWITCHES AND 5-V/3-V VOLTAGE TRANSLATORS

Crossbar Technology (CBT)

DECORIDATION	TVDE	TECHNOLOGY
DESCRIPTION	TYPE	CBT
Dual 4-Bit With '244 Pinout	′3244	·
8-Bit With '245 Pinout	′3245	V
10-Bit Bus Exchanger	′3383	V
Dual 5-Bit	′3384	V
10-Bit With Precharged Outputs for Live Insertion	′6800	+
18-Bit Bus Exchanger	′16209	+
24-Bit Bus Exchanger	′16212	+
12-Bit 3-to-1 Bus Select	′16214	+

ARITHMETIC CIRCUITS

Parallel Binary Adders

DESCRIPTION	ОИТРИТ	TYPE	TECHNOLOGY										
DESCRIPTION	COIPOI	ITPE	ALS AS F HC HCT AC ACT BCT ABT										
4-Bit		′283			~	~							

Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DESCRIPTION	CUITDUIT	TVDE				TE	CHNOLO	DUTPUT TYPE TECHNOLOGY			
DESCRIPTION	COIPOI	ITPE	ALS	AS	F	нс	HCT	AC	ACT	BCT	ABT
4-Bit Arithmetic Logic Units:		′181		~							
4-Bit Arithmetic Logic Units: Function Generator		′11181							~		
		′881		~							
4-Bit Arithmetic Logic Units With Ripple Carry		′382			~						

[✔] Product available in technology indicated

⁺ New product planned in technology indicated

FIFO MEMORIES

First-In. First-Out Memories (FIFOs)

DESCRIPTIO	N	OUTDUT	TVDE		TECHNOLOGY										
SIZE	TYPET	OUTPUT	TYPE	LS	S	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT	
16 Words × 4 Bits	U	38	′232B			~									
			′225		V										
16 Words × 5 Bits	U	38	′229B			~			1						
			′233B			V									
32 Words × 9 Bits	В	3S	′2238			~									
64 Words × 4 Bits	U	38	′234			V									
04 Words × 4 Bits	"		′236			~									
64 Words × 5 Bits	U	38	′235			V									
64 Words × 8 Bits	U	3S	′2232A			~									
64 Words × 9 Bits	U	3S	′2233A			~									
C4 Manda v 10 Dita	U, C	38	′7813									~			
64 Words × 18 Bits	U	3S	′7814									V			
64 Words × 36 Bits	B.C	20	′3612											~	
	B, C	38	′3614											~	
	U, C	38	′3611								+	+			
	0,0	33	′3613											~	
Dual 64 × 1	С	38	′2226									V			
Dual 64 X I	C	33	′2227									~			
Dual 256 × 1	С	20	′2228									~			
Duai 256 x 1		3S	′2229									~			
256 Words × 9 Bits	U	38	7200									V			
256 Words × 18 Bits	U, C	3S	′7805									~			
200 Words X 10 Dits	U	3S	′7806									~			
256 × 36 × 2 Bits	B, C	38	′3622									+			
512 Words × 9 Bits	U	3S	7201									~			
512 Words X 9 Dits	U, S	3S	72211									~			
	U, C	38	′7803									~			
512 Words × 18 Bits	U	3S	′7804									~			
512 Words X 16 Dits	B, C	3S	′7819											~	
	В	3S	′7820											~	
512 Words × 32 Bits	B, C	38	′3638									~			
E10 Mordo y 26 Dita	U, C	38	′3631									+			
512 Words × 36 Bits	B, C	38	′3632									~			

[†]U = Unidirectional



B = Bidirectional

C = Clocked

S = Synchronized

 [✓] Product available in technology indicated
 + New product planned in technology indicated

FIFO MEMORIES

First-In, First-Out Memories (FIFOs) (Continued)

DESCRIPTIO	N	OUTDUT	TVDE					TEC	CHNOL	OGY		-		
SIZE	TYPET	OUTPUT	TYPE	LS	S	ALS	AS	F	HC	НСТ	AC	ACT	ВСТ	ABT
	В	38	′2235									~		
1K Words × 9 Bits] P	35	′2236	,								~		
IK Words x 9 Bits	U	38	7202									~		
	U, S	38	72221									~		
			′7801									~		
1K Words × 18 Bits	U, C	38	′7811									~		
			′7881									+		
	U	38	′7802									~		
1K Words × 36 Bits	U, C	38	′3641									+		
1K × 36 × 2 Bits	B, C	38	′3642									+		
	U, C	38	′7807									~		
2K Words × 9 Bits	U	38	′7203									~		
ZK WOIGS X 9 DILS	0	33	′7808									~		
	U, S	38	72231									~		1
2K Words × 18 Bits	U, C	38	′7882									+		
2K Words × 36 Bits	U, C	38	′3651									+		
4K Marda v O Bit-	U	38	′7204									~		
4K Words × 9 Bits	U, S	38	72241									V		
4K Words × 18 Bits	U, C	38	′7884									+		

[†]U = Unidirectional

B = Bidirectional

C = Clocked

S = Synchronized

[✓] Product available in technology indicated

⁺ New product planned in technology indicated

CLOCK-DISTRIBUTION CIRCUITS

Clock-Distribution Circuits (CDC)

DESCRIPTION	TVDE				TE	CHNOLO	GΥ			
DESCRIPTION	TYPE	ALS	AS	F	НС	HCT	AC	ACT	ВСТ	ABT
3.3-V Hex Inverting Clock Drivers/Buffers	′203						V			
Hex Inverting Clock Drivers/Buffers	′204						~			
Double to A Oberla Driver (D. Krau	′208							V		
Dual 1-to-4 Clock Drivers/Buffers	′209						V			
Octal Divide-by-2 Clock Drivers (6 inverting, 2 noninverting)	′303		V							
Octal Divide-by-2 Clock Drivers (8 noninverting)	′305		V							
Octal Divide-by-2 Clock Drivers (4 inverting, 4 noninverting)	′304		V.							
	′328									~
1-to-6 Clock Drivers	′328A									+
1-to-b Clock Drivers	′329									~
	′329A									~
1-to-6 Clock Drivers	′391									~
With Output Enable	′392									~
1 to 9 Clock Drivers	′340									~
1-to-8 Clock Drivers	′341									~
4 to 0. Divide has 0. Clearly Delivers	′337									~
1-to-8, Divide-by-2 Clock Drivers	′339									~
	′582									+
Phase-Locked Loop 1-to-12 Clock Drivers	′586									+
1.10 12 0.000 0.000	′2586									+

[✓] Product available in technology indicated

ECL TRANSLATORS

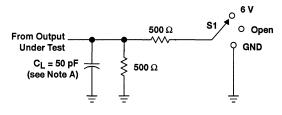
ECL-to-TTL or TTL-to-ECL Translators

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE
Cotal Bus Driver Investina	ECL-to-TTL	38	10KHT5540
Octal Bus Driver, Inverting	TTL-to-ECL	OE	10KHT5542
	ECL-to-TTL	38	10KHT5541
Octal Bus Driver, Noninverting	TTL-to-ECL	OE -	10KHT5543
	11L-10-EGL) OE	100KT5543
Catal D. Taras Latas Trans	501 to 171	38	10KHT5573
Octal D-Type Latch, True	ECL-to-TTL	35	100KT5573
	ECL-to-TTL	38	10KHT5574
Octal D-Type Flip-Flop, True	TTI to FOI	OE -	10KHT5578
	TTL-to-ECL	OE	100KT5578



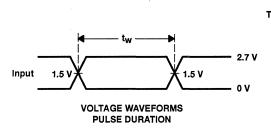
⁺ New product planned in technology indicated

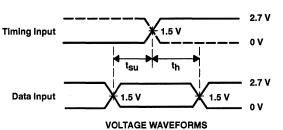
LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR LVC, LVT, LVTZ, AND ALVC DEVICES



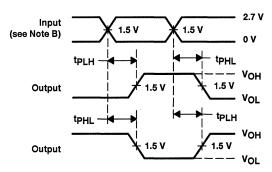
TEST	S1
tPLH/tPHL	Open
tpLz/tpzL	6 V
tPHZ/tPZH	GND

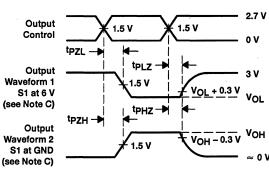
LOAD CIRCUIT FOR OUTPUTS





SETUP AND HOLD TIMES





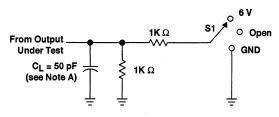
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

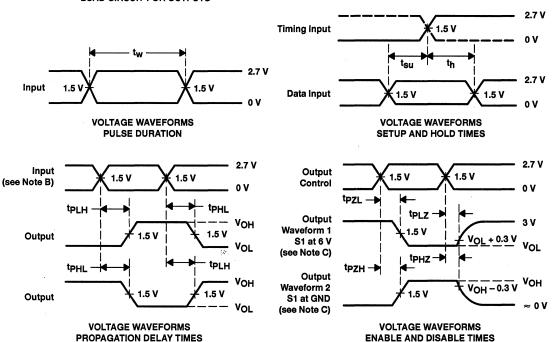
LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR LV MSI AND OCTAL DEVICES



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND

LOW- AND HIGH-LEVEL ENABLING

LOAD CIRCUIT FOR OUTPUTS

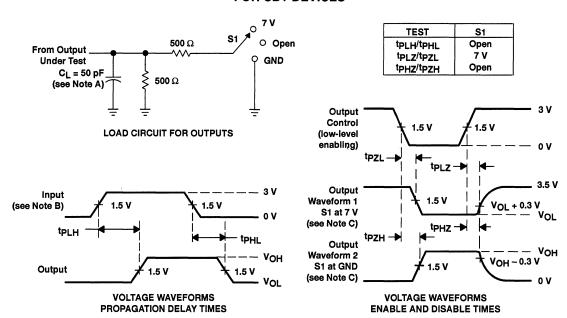


NOTES: A. CL includes probe and jig capacitance.

INVERTING AND NONINVERTING OUTPUTS

- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

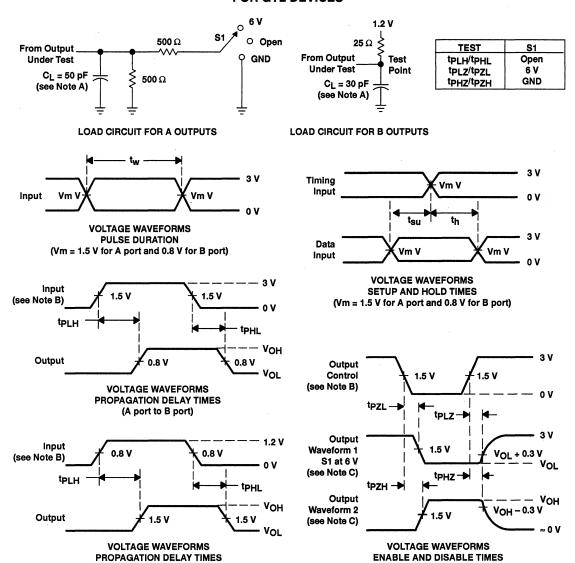
LOAD CIRCUIT AND VOLTAGE WAVEFORMS **FOR CBT DEVICES**



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5$ ns, $t_{f} \leq 2.5$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR GTL DEVICES



NOTES: A. Ci includes probe and jig capacitance.

(B port to A port)

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.

(A port)

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.



General Information	1
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LVT OCTALS

Features

- State-of-the-art 0.8-μ EPIC-IIB™ BiCMOS process
- No input-diode clamp to V_{CC}
- Fully compatible (input and output) with 5-V systems
- −32-mA/64-mA drive current
- Low standby current (190 μA)
- Bus-hold cell on data inputs and I/O pins
- SOIC, EIAJ SSOP, and TSSOP packaging
- TI has established two worldwide alternate sources

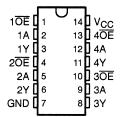
Benefits

- Propagation delays as fast as 4 ns maximum for improved performance
- Interfaces directly to industry standard buses and 5-V integrated circuits
- Supports live insertion
- Drives large loads, buses, or memory arrays
- Extends battery life
- Eliminates passive pullup resistors on local buses
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

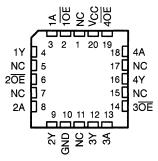
SCBS133B - MAY 1992 - REVISED FEBRUARY 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

SN54LVT125...J PACKAGE SN74LVT125...D, DB, OR PW PACKAGE (TOP VIEW)



SN54LVT125...FK PACKAGE (TOP VIEW)



NC - No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT125 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT125 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE (each buffer)

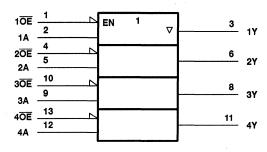
INP	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

TEXAS INSTRUMENTS

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

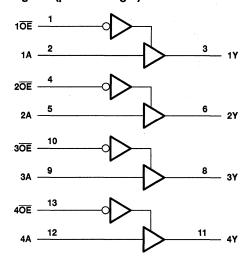
SCBS133B - MAY 1992 - REVISED FEBRUARY 1994

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT125
SN74LVT125
Current into any output in the high state, I _O (see Note 2): SN54LVT125
SN74LVT125 64 m/
Input clamp current, $I_{ K }(V_{ C })$ —50 m/
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package
DB or PW package 0.5 W
Storage temperature range -65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and VO > VCC.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



recommended operating conditions (see Note 4)

			SN54L	VT125	SN74L	VT125	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3,6	2.7	3.6	V
VIH	High-level input voltage		2	Ţ,	2		٧
VIL	Low-level input voltage			0.8		0.8	٧
٧ı	Input voltage			5.5		5.5	٧
loн	High-level output current		<u>(</u>	-24		-32	mA
lOL	Low-level output current		Ñ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS133B - MAY 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	_	FOT COMPLETIONS		SN	54LVT1	25	SN	74LVT1	25		
PARAMETER	!	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VιΚ	$V_{CC} = 2.7 \text{ V},$	l _l = –18 mA				-1.2			-1.2	V	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I _{OH} = -100 μA		VCC-0	.2		VCC-C	.2			
V	V _{CC} = 2.7 V,	IOH = - 8 mA	30000-1-1-1-1	2.4			2.4			v	
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						· ·	
	ACC = 2 A	I _{OH} = -32 mA					2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA							0.5		
Voi		I _{OL} = 16 mA				0.4			0.4	v	
VOL	\\ 2\\	I _{OL} = 32 mA				0.5			0.5	V	
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55					
		IOL = 64 mA				42.			0.55		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				10			10		
1.		VI = VCC or GND	Control pins		24	±1			±1	μА	
l _l	V _{CC} = 3.6 V	V _I = V _{CC}	Data pins		X.	1			1	μА	
		V _I = 0	Data pins		\$	- 5			- 5		
l _{off}	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V		l c	Y				±100	μA	
lea en	Vac 2V	V _I = 0.8 V	Data innute	75			75				
l(hold)	V _{CC} = 3 V	V _I = 2 V	Data inputs	-75			-75			μА	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μА	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			- 5	μА	
			Outputs high		0.12	0.19		0.12	0.19		
ICC	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		4.5	7		4.5	7	mA	
.00	V _I = V _{CC} or GND		Outputs disabled	0.12 0.19				0.12	0.19	ША	
ΔICC§	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.3			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Co	V _O = 3 V or 0							8		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS133B - MAY 1992 - REVISED FEBRUARY 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54L	VT125			SN	74LVT1:	25		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	VC	C = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	Α		1	4.2	,55	4.7	1	2.7	4		4.5 ns	
t _{PHL}	^	ľ	1	4.1	25	5.1	1	2.9	3.9		4.9	113
^t PZH	ŌĒ	_	1	4.9		6.2	1	3.4	4.7		6	ns
tPZL	OE		1.1	4,0		6.7	1.1	3.4	4.7		6.5	115
t _{PHZ}	ŌĒ	_	1.8	,6.3		5.9	1.8	3.7	5.1		5.7	
tPLZ	OL.		1.3	4.7		4.2	1.3	2.6	4.5		4	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

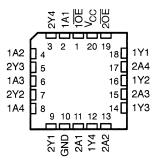
SCBS134D - SEPTEMBER 1992 - REVISED FEBRUARY 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)
 Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

SN54LVT240 ... J PACKAGE SN74LVT240 ... DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT240 . . . FK PACKAGE (TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT240 is organized as two 4-bit buffer/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

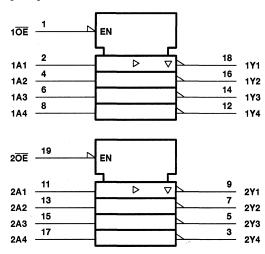
The SN74LVT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT240 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT240 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE (each buffer)

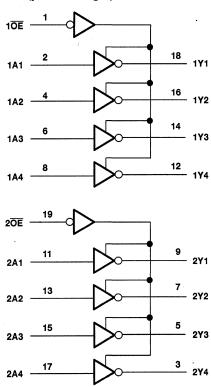
INP	UTS	OUTPUT
ŌĒ	Α	Υ
L	Н	L
L	L	Н
Н	Х	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS134D - SEPTEMBER 1992 - REVISED FEBRUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

O all alles	0.5144 4.014
Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1	
Current into any output in the low state, IO: SN54LVT240	
SN74LVT240	
Current into any output in the high state, IO (see Note 2): SN54LVT240	48 MA
SN74LVT240	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	
DW package	1.6 W
	0.7 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54L	VT240	SN74L	VT240	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	V _{CC} Supply voltage				2.7	3.6	V
VIH	High-level input voltage				2		V
VIL	Low-level input voltage			Ø.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current		Į	-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SCBS134D - SEPTEMBER 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT240			SN	UNIT		
PANAMETEN				MIN	TYP	MAX	MIN	TYPT	MAX	UNII
VIK	V _{CC} = 2.7 V,	l _l = –18 mA				-1.2	-		-1.2	V
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I _{OH} = -100 μA		VCC-C	.2		VCC-C).2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V,	I _{OH} = -24 mA		2						,
	V _{CC} = 3 V,	I _{OH} = -32 mA					2			
	$V_{CC} = 2.7 \text{ V},$	I _{OL} = 100 μA				0.2			0.2	
	$V_{CC} = 2.7 \text{ V},$	I _{OL} = 24 mA				0.5			0.5	
VOL	V _{CC} = 3 V,	I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V,	I _{OL} = 32 mA				0.5			0.5	, v
	V _{CC} = 3 V,	I _{OL} = 48 mA				0.55				
	V _{CC} = 3 V,	I _{OL} = 64 mA			4	%;" /			0.55	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V			40	10			10	
lj	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control pins		\Q_{x_1}	±1			±1	μА
''	V _{CC} = 3.6 V,	VI = VCC	Data pins		\mathcal{G}	1			1	μΑ
	V _{CC} = 3.6 V,	V _I = 0	Data piris	Š) ·	-5			-5	
l _{off}	V _{CC} = 0,	V_{I} or $V_{O} = 0$ to 4.5 V		8.5					±100	μΑ
lia in	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75			75			μА
l(hold)	VCC = 2 V	V _I = 2 V	Ainputs	-75			-75			μА
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μΑ
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μΑ
			Outputs high		0.12	0.19		0.12	0.19	
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	12		8.6	12	mA
100	V _I = V _{CC} or GND		Outputs disabled		0.12	0.19		0.12	0.19	IIIA
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				4			. 4		pF
Co	V _O = 3 V or 0				8			8		рF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS134D - SEPTEMBER 1992 - REVISED FEBRUARY 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 5)

			18		SN54LVT240			SN74LVT240				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =		V _{CC} =	2.7 V	٧c	C = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	А		1	4.2	,S'	5.2	. 1	2.9	4.1		5.2	ns
tPHL		'	1.3	3.7	2.	4.1	1.3	2.5	3.5		4	113
^t PZH	ŌĒ	V	1.2	4.7%		5.7	1.2	3.2	4.6		5.6	200
tPZL	OE .	r	1.5	4.8	-	5.9	1.4	3.5	4.7		5.8	ns
tPHZ	ŌĒ	_	2	5.3		5.7	2	3.6	5.2		5.5	no.
tPLZ)	T	1.9	<a>4.6		4.6	1.9	3.2	4.4		4.4	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SCAS352 - MARCH 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

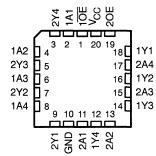
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT241 . . . J PACKAGE SN74LVT241 . . . DB, DW, OR PW PACKAGE (TOP VIEW)

		T	1
10E [1	O 20	D v _{cc}
1A1 [2	19	
2Y4 [3	18	1Y1
1A2 [17	2A4
2Y3 [16	1Y2
1A3 [6	15] 2A3
2Y2 [7	14] 1Y3
1A4 [8	13	2A2
2Y1 [9	12] 1Y4
GND [10	11] 2A1

SN54LVT241 . . . FK PACKAGE (TOP VIEW)



The 'LVT241 is organized as two 4-bit line drivers with separate output-enable (1OE, 2OE) inputs. When 1OE is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When 1OE is high or 2OE is low, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT241 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT241 is characterized for operation from –40°C to 85°C.

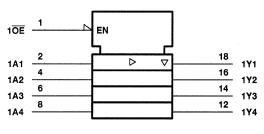
FUNCTION TABLES

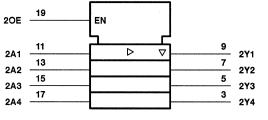
INP	JTS	OUTPUT
1OE	1A	1Y
L	Н	Н
L	L	L
. н	Χ	Z

. INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	Χ	Z

logic symbol†

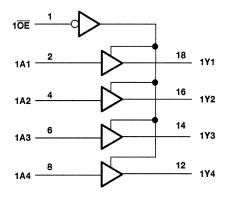
PRODUCT PREVIEW

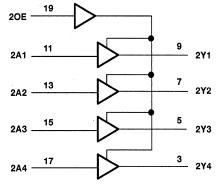




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SCAS352 - MARCH 19

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) −0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT241
SN74LVT241
Current into any output in the high state, I _O (see Note 2): SN54LVT241
SN74LVT241 64 mA
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$) — 50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range — 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54L	VT241	SN74L	VT241	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage				2		V
VIL	Low-level input voltage					0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current	-		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



SCAS352 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	ER TEST CONDITIONS			SN	154LVT24	41	SN	74LVT2	41		
PARAMETER				MiN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	٧	
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C).2		VCC-C).2			
\/a	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			V	
Vон	V _{CC} = 3 V	I _{OH} = -24 mA		2						V	
	ACC = 2 A	I _{OH} = -32 mA					2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
Voi		I _{OL} = 16 mA				0.4			0.4	٧	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	٧	
	\ \CC = 2 \	I _{OL} = 48 mA				0.55					
		I _{OL} = 64 mA	•						0.55		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				10			10		
1.		V _I = V _{CC} or GND	Control pins			±1			±1	μΑ	
lı lı	V _{CC} = 3.6 V	VI = VCC	Data pins			1			1	μΑ	
		V _I = 0	Data pins			-5			-5		
l _{off}	V _{CC} = 0,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$							±100	μА	
lia in	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75			75			μА	
li(hold)	ACC = 2 A	V _I = 2 V	Airiputs	-75			-75			μΑ	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μΑ	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μΑ	
			Outputs high		0.12	0.5		0.12	0.19		
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	14		8.6	12	mA	
$V_{I} = V_{CC}$ or GND			Outputs disabled		0.12	0.5		0.12	0.19		
ΔI _{CC} §	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.3			0.2	mA	
Ci	V _I = 3 V or 0				4			4		рF	
Co	V _O = 3 V or 0				8			8		рF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT243, SN74LVT243 3.3-V ABT QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

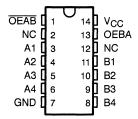
SCAS353 - MARCH 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

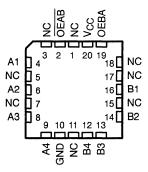
description

These quadruple bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT243 ... J PACKAGE SN74LVT243 ... D, DB, OR PW PACKAGE (TOP VIEW)



SN54LVT243 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The 'LVT243 is designed for asynchronous communications between data buses. The control-function implementation allows for maximum flexibility in timing. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEBA and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous enabling of OEBA and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) remain at their states. The 4-bit codes appearing on the two sets of buses will be identical for the 'LVT243.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT243 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT243 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT243 is characterized for operation from –40°C to 85°C.

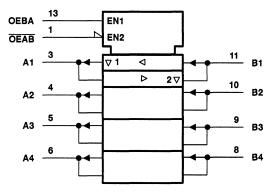


FUNCTION TABLE

INP	UTS	FUNCTION
OEAB	OEBA	FUNCTION
L	Ł	A to B
н	Н	B to A
Н	L	Isolation
L	н	Latch A and B (A = B)

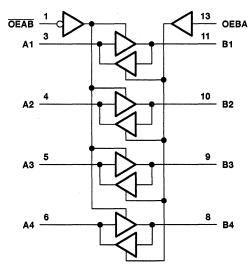
logic symbolt

PRODUCT PREVIEW



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.



SN54LVT243, SN74LVT243 3.3-V ABT QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS353 - MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cupply valtage vapa. V	051/4-461/
Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-05 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	. −0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT243	96 mA
SN74LVT243	
Current into any output in the high state, IO (see Note 2): SN54LVT243	48 mA
SN74LVT243	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

					SN74LVT243		UNIT
			MIN	MAX	MIN	MAX	ONIT
Vcc	Supply voltage				2.7	3.6	V
VIH	High-level input voltage				2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



SN54LVT243, SN74LVT243 3.3-V ABT QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS353 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT243			SN74LVT243			UNIT	
PARAMETER				MIN	TYPT	MAX	MIN	TYPT	MAX	UNII	
VIK	V _{CC} = 2.7 V,	l _I = -18 mA				-1.2			-1.2	٧	
	V _{CC} = MIN to MAX [‡] , I _{OH} = -100 μA			VCC-0	.2		VCC-C	.2			
VOH	$V_{CC} = 2.7 \text{ V},$	IOH = - 8 mA	2.4			2.4			V		
	V _{CC} = 3 V	IOH = -24 mA		2						'	
	VCC = 3 V	I _{OH} = -32 mA					2				
VoL	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VGG = 2.7 V	I _{OL} = 24 mA				0.5			0.5	5	
		I _{OL} = 16 mA				0.4			0.4	l _v	
	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V	
	ACC = 2 A	I _{OL} = 48 mA				0.55					
		IOL = 64 mA							0.55		
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	OtL-i			±1			±1	μА	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins			10			10		
lj	V _{CC} = 3.6 V	V _I = 5.5 V				100			20		
		V _I = V _{CC}	A or B ports§			5			5		
		V _I = 0				-10			-10		
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V							±100	μА	
^I I(hold)	V _{CC} = 3 V	V _I = 0.8 V	A av B navta	75			75			μΑ	
		V ₁ = 2 V	A or B ports	-75			-75				
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μA	
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ	
lcc		I _O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA	
	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Outputs low		8.8	14		8.8	12		
			Outputs disabled		0.13	0.5		0.13	0.19		
ΔICC [¶]	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.3			0.2	mA	
Ci	V ₁ = 3 V or 0									pF	
Cio	V _O = 3 V or 0									pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

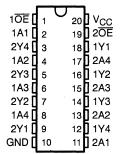
[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

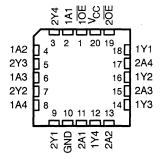
SCBS135B - AUGUST 1992 - REVISED MARCH 1994

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flatpacks (W), and Ceramic DIPS (J)

SN54LVT244 . . . J OR W PACKAGE SN74LVT244 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT244 . . . FK PACKAGE (TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each buffer)

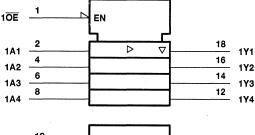
INP	UTS	OUTPUT
ŌĒ	Α	Υ
L	Н	Н
L	L	L
Н	Х	z

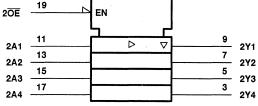
PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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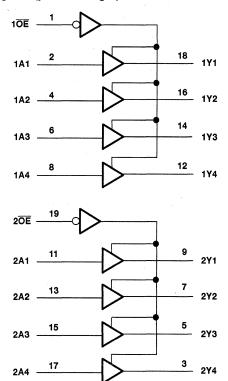
logic symbol†





† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or pow	
Current into any output in the low state, Io: SN54LVT244	96 mA
SN74LVT244	128 mA
Current into any output in the high state, IO (see Note 2): S	3N54LVT244 48 mA
	SN74LVT244 64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see N	
	DW package 1.6 W
	PW package 0.7 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



recommended operating conditions (see Note 4)

			SN54L	VT244	SN74L	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
ViH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
٧ı	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT244, **SN74LVT244** 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS135B - AUGUST 1992 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		EST CONDITIONS		SN54LVT244			SN	74LVT2	44	UNIT
PANAMEIEN		EST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNII
VIK	$V_{CC} = 2.7 \text{ V},$	lj = −18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to MAX}^{\ddagger}$,	I _{OH} = -100 μA		VCC-C).2		VCC-C).2		
V	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4	-		2.4			v
VOH	V _{CC} = 3 V,	I _{OH} = -24 mA		2						V
	V _{CC} = 3 V,	IOH = -32 mA					2			
	$V_{CC} = 2.7 \text{ V},$	I _{OL} = 100 μA				0.2			0.2	
	V _{CC} = 2.7 V,	I _{OL} = 24 mA				0.5			0.5	
V	V _{CC} = 3 V,	I _{OL} = 16 mA				0.4			0.4	v
v_{OL}	V _{CC} = 3 V,	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V,	I _{OL} = 48 mA				0.55				. 1
:	V _{CC} = 3 V,	I _{OL} = 64 mA							0.55	.
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				50			10	
lı .	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control pins			±1			±1	μА
	V _{CC} = 3.6 V,	VI = VCC	Data pins			1			1	μ^
	V _{CC} = 3.6 V,	V ₁ = 0	Data piris			-5			-5	
loff	V _{CC} = 0,	V_1 or $V_0 = 0$ to 4.5 V							±100	μA
lia in	V _{CC} = 3 V,	V _I = 0.8 V	A inputs	75			75			μА
l(hold)	V _{CC} = 3 V,	V _I = 2 V	Airipuis	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μA
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				∸1			-1	μA
			Outputs high		0.12	0.39		0.12	0.19	
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	14		8.6	12	mA
100	V _I = V _{CC} or GND		Outputs disabled		0.12	0.39		0.12	0.19	IIIA
ΔICC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} - 0.6 or GND	V,			0.3			0.2	mA
Ci	V _I = 3 V or 0				4			. 4		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT244, SN74LVT244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS135B - AUGUST 1992 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

·				SN54L	VT244			SN	74LVT2	44			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V				V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V V _{CC} = 2.			2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
^t PLH	Α		0.5	4.7		5.2	1	2.5	4.3		5	ns	
^t PHL		r	0.5	4.4		5.4	1	2.5	4.2		5.2	113	
tPZH	OF	_	0.8	5.4		6.5	1	2.7	5.2		6.3	ns	
tPZL	ŌĒ	T T	0.8	5.4		7.6	1.1	3.1	5.2		6.7	115	
tPHZ	ŌĒ	V	1.5	6.2		6.9	2.1	3.9	5.6		6.3	20	
tPLZ	OE.	, ,	1.2	5.5		6	1.8	3.2	5.1		5.6	ns	

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT244A, SN74LVT244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

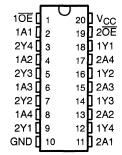
SCAS354 - FEBRUARY 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

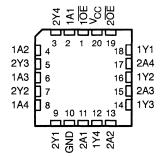
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT244A . . . J PACKAGE SN74LVT244A . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT244A . . . FK PACKAGE (TOP VIEW)



The 'LVT244A is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT244A is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT244A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

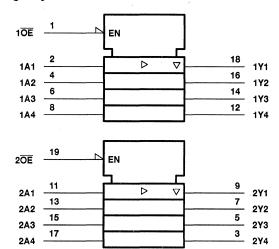
INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X	Z



SN54LVT244A, SN74LVT244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

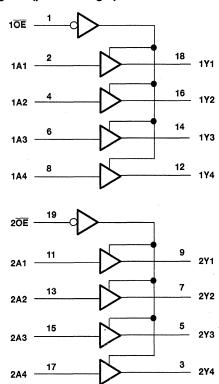
SCAS354 - FEBRUARY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V t	0 4.6 V
Input voltage range, V _I (see Note 1)	' to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)0.5 \	' to 7 V
Current into any output in the low state, Io: SN54LVT244A	96 mA
SN74LVT244A 1	28 mA
Current into any output in the high state, IO (see Note 2): SN54LVT244A	48 mA
SN74LVT244A	64 mA
Input clamp current, $I_{ K }(V_{ } < 0)$ -	50 mA
Output clamp current, I_{OK} ($V_O < 0$)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range—65°C to	150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



recommended operating conditions (see Note 4)

			SN54LV	T244A	A SN74LVT244A		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Ţ,	2		V
VIL	Low-level input voltage			Ø.8		0.8	V
VI	Input voltage		,	(5.5		5.5	V
ЮН	High-level output current		\$	* –2 4		-32	mA
lOL	Low-level output current		ŞĨ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT244A, SN74LVT244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS354 - FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TOT CONDITIONS		SN	54LVT24	4A	SN	74LVT24	4A	UNIT	
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	UNII	
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = -18 mA				-1.2			-1.2	V	
	V _{CC} = MIN to MAX‡,	l _{OH} = -100 μA		VCC-C	.2		VCC-C).2			
\/a	V _{CC} = 2.7 V,	I _{OH} = - 8 mA		2.4			2.4			٧	
∨он	V _{CC} = 3 V,	I _{OH} = – 24 mA		2						V	
	V _{CC} = 3 V,	I _{OH} = -32 mA					2				
	$V_{CC} = 2.7 \text{ V},$	I _{OL} = 100 μA				0.2			0.2		
	$V_{CC} = 2.7 \text{ V},$	I _{OL} = 24 mA				0.5			0.5		
Voi	V _{CC} = 3 V,	I _{OL} = 16 mA				0.4			0.4	V	
VOL	V _{CC} = 3 V,	I _{OL} = 32 mA				0.5			0.5	V	
	V _{CC} = 3 V,	I _{OL} = 48 mA				0.55					
	V _{CC} = 3 V,	I _{OL} = 64 mA			Į.	**************************************			0.55		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V			Ţ,	10			10		
l _l	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control pins			±1			±1	μА	
''	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC}	Data pins		<u>"</u>	1			1	μ,	
	$V_{CC} = 3.6 \text{ V},$	V _I = 0	Data pins	8	Σ	-5			-5		
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V		E					±100	μΑ	
lia in	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75			75			μА	
l(hold)	VCC = 3 V	V _I = 2 V	Airiputs	-75			-75			μΛ	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μА	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μА	
			Outputs high		0.12	0.5		0.12	0.19		
lcc,	V _{CC} = 3.6 V,	l _O = 0,	Outputs low		8.6	14		8.6	12	mA	
.00	V _I = V _{CC} or GND		Outputs disabled		0.12	0.5		0.12	0.19		
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} of	One input at V _{CC} – 0.6 or GND	V,			0.3			0.2	mA	
C _i	V _I = 3 V or 0				4			4		pF	
Co	V _O = 3 V or 0				8			8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT244A, SN74LVT244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS354 - FEBRUARY 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

	*			SN54L\	/T244A			SN7	74LVT24	4A			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	٧c	c = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
tPLH	А		0.5	4.7	.4	5.2	1	2.5	4.1		5	ns	
t _{PHL}	^	T T	0.5	4.4	89	5.4	1	2.5	4.1		5.2	115	
t _{PZH}	ŌĒ		0.8	5.4	Q	6.5	1	2.7	5.2		6.3	ns	
tPZL	OE	l OE	· ·	0.8	5.4		7.6	1.1	3.1	5.2		6.7	115
t _{PHZ}	ŌĒ		1.5	6.2		6.9	1.9	3.9	5.6		6.3	200	
tPLZ		OE	OE Y	l r	1.2	5.5		6	1.8	3.2	5.1		5.6

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT245 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

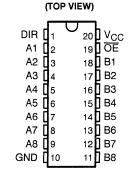
SCAS413 - MARCH 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Ceramic Chip Carriers (FK) and DIPs (J)

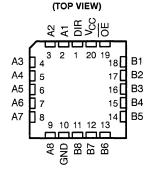
description

This octal bus transceiver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN54LVT245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.



J PACKAGE



FK PACKAGE

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVT245 is characterized for operation over the full military temperature range of -55°C to 125°C.

FUNCTION TABLE

INP	UTS	OPERATION
ŌE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

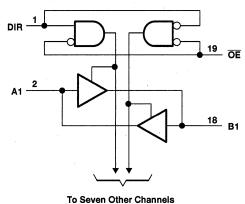


SCAS413 - MARCH 1994

logic symbol†

3EN1[BA] 3EN2[AB] 18 2∇ \triangleright 17 **B2** 16 В3 15 **B4** 14 В5 13 A6 **B6** 12 Α7 **B7** 11 **8**A В8

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO	96 mA
Current into any output in the high state, I _O (see Note 2)	48 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	–50 mA
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage		2		٧
VIL	Low-level input voltage			0.8	٧
٧ı	Input voltage			5.5	٧
ЮН	High-level output current			-24	mA
loL	Low-level output current			48	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10	ns/V
TA	Operating free-air temperature		-55	125	°C

NOTE 3: Unused or floating control inputs must be held high or low.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This current will only flow when the output is in the high state and $V_O > V_{CC}$.

3.3-V ABT OCTAL BUS TRANSCEIVER **WITH 3-STATE OUTPUTS**

SCAS413 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN TYPT	MAX	UNIT	
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA			-1.2	٧	
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	I _{OH} = -100 μA		V _{CC} -0.2			
Voн	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4		٧	
	V _{CC} = 3 V,	I _{OH} = -24 mA		2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA			0.5		
v_{OL}		I _{OL} = 16 mA			0.4	· V	
	V _{CC} = 3 V	$I_{OL} = 32 \text{ mA}$			0.5		
		I _{OL} = 48 mA			0.55		
	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control pins		±1		
	$V_{CC} = 0$ or MAX‡,	V _I = 5.5 V	Control pins		10		
lı	V _{CC} = 3.6 V	V _I = 5.5 V			100	_ μΑ	
		V _I = V _{CC}	A or B ports§		5		
		V _I = 0			-10		
liai-s	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75		μА	
l(hold)	VCC = 0 V	V _I = 2 V	A of B ports	-75		μΛ	
^l ozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			1	μΑ	
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V			-1	μΑ	
			Outputs high	0.13	0.39		
lcc	$V_{CC} = 3.6 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_{O}=0$,	Outputs low	8.8	14	mA	
	1 = 100 or 214B		Outputs disabled	0.13	0.39		
ΔICC¶	V _{CC} = 3 V to 3.6 V, O Other inputs at V _{CC} or Gi	ne input at V _{CC} – 0.6 V, ND			0.3	mA	
Ci	V _I = 3 V or 0			4		pF	
C _{io}	V _O = 3 V or 0			10		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT245 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS413 - MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	UNIT	
	(114-01)	(OUTPUT)	MIN	MAX	MIN	MAX	
^t PLH	A or B	B or A	0.5	4.4		5.2	ns
t _{PHL}		BUIA	0.5	4.2		4.8	
^t PZH	ŌĒ	A or B	0.8	5.9		7.3	ns
^t PZL	OE	AGIB	1	5.9		7.2	
^t PHZ	ŌĒ	A or B	1.5	6.5		7.2	ns
^t PLZ	J. J.	7010	1.5	6.1		6.5	115

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT245A, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

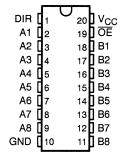
SCBS130D - MAY 1992 - REVISED FEBRUARY 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

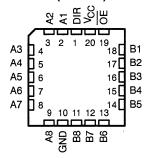
description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT245A . . . J PACKAGE SN74LVT245A . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT245A . . . FK PACKAGE (TOP VIEW)



The 'LVT245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT245A is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT245A is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT245A is characterized for operation from -40° C to 85°C.

FUNCTION TABLE

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

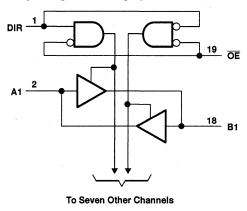
TEXAS INSTRUMENTS

SCBS130D - MAY 1992 - REVISED FEBRUARY 1994

logic symbol†

ŌĒ GЗ 3EN1[BA] 3EN2[AB] 18 2∇ 17 **B2** 16 АЗ ВЗ 15 Α4 **B4** 14 A5 **B**5 7 13 В6 A6 8 12 **B7 A7** 11 **A8 B8**

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT245A	96 mA
SN74LVT245A	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT245A	48 mA
SN74LVT245A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	50 mA
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and VO > VCC.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT245A, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS130D - MAY 1992 - REVISED FEBRUARY 1994

recommended operating conditions (see Note 4)

			SN54LV	T245A	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Ü	2		V
VIL	Low-level input voltage			0.8		0.8	V
Vi	Input voltage		,<	5.5		5.5	V
ЮН	High-level output current		Į.	-24		-32	mA
lOL	Low-level output current		Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TA	Operating free-air temperature		~-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT245A, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130D - MAY 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN	54LVT24	5A	SN	74LVT24	5A	UNIT
PANAMETER	'	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII
۷ıK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	$V_{CC} = MIN \text{ to MAX}^{\ddagger}$,	IOH = ~100 μA		VCC-C).2		VCC-C).2		
V	V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = -24 mA I _{OH} = -32 mA		2						٧
	VCC = 3 V						2			
	V _{CC} = 2.7 V	V 0.7.V				0.2			0.2	
	V(() = 2.7 V	I _{OL} = 24 mA				0.5		,	0.5	
VOL		I _{OL} = 16 mA				0.4			0.4	ν
VOL	V _{CC} = 3 V					0.5			0.5	٧
	\(\(\(\) \	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA				42			0.55	
	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND	Control pins		Š	∜ ±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins		34	10			10	
11		V _I = 5.5 V			<u> </u>	100			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		,S	5			5	
		V _I = 0		J & -10		-10		-10		
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V		<i>₹</i>					±100	μA
li a i n	VCC = 3 V	V ₁ = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 0 V	V _I = 2 V	A or B ports	-75			-75			μΛ
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μA
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μA
			Outputs high		0.13	0.5		0.13	0.19	
lcc	V _{CC} = 3.6 V,	$I_O = 0$,	Outputs low		8.8	14		8.8	12	mA
	V _I = V _{CC} or GND		Outputs disabled		0.13	0.5		0.13	0.19	
AICC¶		$_{CC}$ = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND				0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		рF
C _{io}	V _O = 3 V or 0	•			10			10		pF

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT245A, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130D - MAY 1992 - REVISED FEBRUARY 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

		TO (OUTPUT)		SN54L\	/T245A							
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	A or B	B or A	1	4.6	,S.	5.3	1	2.5	4		5.2	ns
t _{PHL}	Aorb	BULA	1	4.1	Ø.	5.7	1	2.5	4		5.5	113
t _{PZH}	ŌĒ	A or B	1.1	6.1	*	7.2	1.1	3.3	5.9		7.1	ns
tPZL		OE A OF B	1.5	6.6		8	1.5	3.8	6.5	-	7.9	115
t _{PHZ}	ŌĒ	A or B	2.2	_்6.2		7	2.2	4.3	5.9		6.5	ns
†PLZ		OE A OF B	7016	2	[©] 6.3		5.9	2	3.9	5.5		5.6

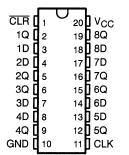
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

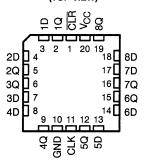
SCBS136C - MAY 1992 - REVISED FEBRUARY 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

SN54LVT273 ... J PACKAGE SN74LVT273 ... DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT273 . . . FK PACKAGE (TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

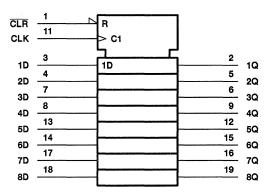
The SN54LVT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT273 is characterized for operation from –40°C to 85°C.

SCBS136C - MAY 1992 - REVISED FEBRUARY 1994

FUNCTION TABLE (each flip-flop)

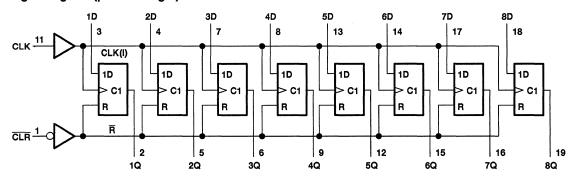
	INPUTS	OUTPUT	
CLR	CLK	D	Q
L	Х	Х	L
Н	1	Н	Н
Н	1	L	Ļ
Н	H or L	Х	Q ₀

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS136C - MAY 1992 - REVISED FEBRUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	
Current into any output in the low state, I _O : SN54LVT273	
SN74LVT273	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT273	48 mA
SN74LVT273	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

	·	SN54LVT2		SN74L	VT273	UNIT
		MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage	2.7	3,6	2.7	3.6	٧
VIH	High-level input voltage	2	ŢŢ.	2		٧
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	.4	5.5		5.5	٧
ЮН	High-level output current	, Ç	-24		-32	mA
lOL	Low-level output current	ĄŠ	48		64	mA
Δt/Δν	Input transition rise or fall rate	S. C.	10		10	ns/V
TA	Operating free-air temperature	_55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136C - MAY 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SN54LVT273			SN			
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = -18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C	.2		VCC-C).2		
V	$V_{CC} = 2.7 \text{ V},$	IOH = - 8 mA		2.4			2.4	•		v
VOH	V _{CC} = 3 V	IOH = -24 mA		2	,					V
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	V(() = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	V
V_{OL}	V _{CC} = 3 V	I _{OL} = 32 mA			Š	0.5			0.5	· •
		I _{OL} = 48 mA			Ž ⁴	0.55				
		I _{OL} = 64 mA			A				0.55	
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V				10			10	
lį	V _{CC} = 3.6 V	$V_I = V_{CC}$ or GND	Control pins		Y	±1			±1	μА
Ч		VI = VCC	Data pins	4.		1			1	μΛ
		V _I = 0	Data pins			-5			-5	
II(hold)	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА
·I(Hola)	*66-01	V _I = 2 V	Data inputo	-75			-75			μ,
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs high		0.12	0.19		0.12	0.19	mA
	V _I = V _{CC} or GND		Outputs low		8.6	12		8.6	12	
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or					0.2			0.2	mA
Ci	V _I = 3 V or 0							4		рF
Co	V _O = 3 V or 0							8		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54L	VT273						
			V _{CC} = 3.3 V ± 0.3 V				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^f clock	Clock frequency						0	150			MHz
t _w	Pulse duration				70,7		3.3		3.3		ns
	Setup time before CLKT	Data high or low		್ದರೆ	76.		2.3		2.7		20
t _{su}	Setup time before CLK	CLR high		₹%			2.7		3.2		ns
th	Hold time after CLK↑	Data high or low					0		0		ns

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136C - MAY 1992 - REVISED FEBRUARY 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER FROM (INPUT)		SN54LVT273										
	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
fmax					A		150					MHz
tPLH	CLK	Any Q		فد	223		1.7	3.5	5.5		6.3	ns
tPHL	OLK	CLK Any Q		8870	200		1.9	3.5	5.5		5.9	115
t _{PHL}	CLR	Any Q		. ⊘.			1.3	3.2	5.1		6.2	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SCBS137B - MAY 1992 - REVISED FEBRUARY 1994

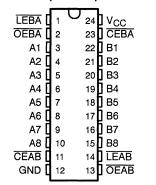
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (JT)

description

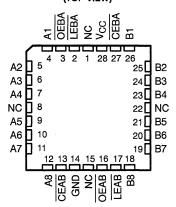
These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

SN54LVT543 . . . JT PACKAGE SN74LVT543 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT543 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SCBS137B - MAY 1992 - REVISED FEBRUARY 1994

description (continued)

The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

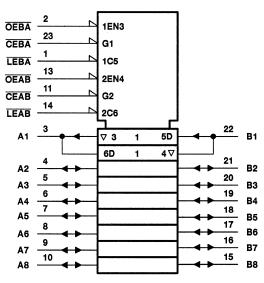
The SN54LVT543 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT543 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INPL	JTS	**********	OUTPUT
CEAB	LEAB	OEAB	Α	В
Н	Х	Х	Х	Z
Х	X	Н	Χ	z
L	Н	L	X	В ₀ ‡
L	L	L	L	L
L	L	L	Н	Н

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

logic symbol§

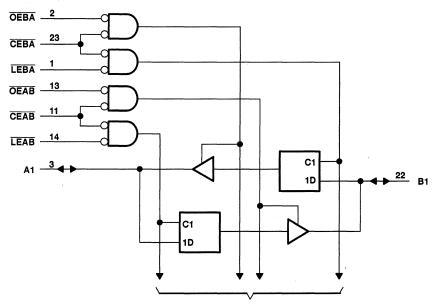


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

[‡] Output level before the indicated steady-state input conditions were established.

SCRS137B - MAY 1992 - REVISED FERRIJARY 1994

logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT543	96 mA
SN74LVT543	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT543	48 mA
SN74LVT543	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



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recommended operating conditions (see Note 4)

			SN54L	VT543	SN74L	VT543	UNIT	
1	•		MIN	MAX	MIN	MAX	01411	
VCC	Supply voltage		2.7	3,6	2.7	3.6	V	
VIH	High-level input voltage		2	Ţ,	2		٧	
VIL	Low-level input voltage			0.8		0.8	V	
Vi	Input voltage			5.5		5.5	V	
ЮН	High-level output current		Q [*]	-24		-32	mA	
loL	Low-level output current		ĄŠ	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	SF	10		10	ns/V	
TA	Operating free-air temperature		[*] –55	125	-40	85	့	

NOTE 4: Unused or floating control inputs must be held high or low.

SCBS137B - MAY 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SN	54LVT5	13	SN	74LVT54	13	LINUT
PARAMETER	I	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I _{OH} = -100 μA		VCC-0	.2		VCC-C	.2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	I _{OH} = - 24 mA		2						, v
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	•
	\vCC = 3 v	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA				12		0.5		
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control pins			∜ ±1			±1	
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V	Control pins			10			10	
Ц	V _{CC} = 3.6 V	V _I = 5.5 V				20			20	μA
		V _I = V _{CC}	A or B ports§		jS	5			5	
		V _I = 0			3	-10			-10	
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V		₫.					±100	μА
ha is	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 2 V	V _I = 2 V	A of B ports	-75			-75			μ.Α.
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μA
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
			Outputs high		0.13	0.19		0.13	0.19	
VCC =	V _{CC} = 3.6 V,	l _O = 0,	Outputs low		8.8	12		8.8	12	mA
.00	V _I = V _{CC} or GND		Outputs disabled		0.13	0.19		0.13	0.19	1151
ΔICC¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	One input at V _{CC} – 0.6 r GND	V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4.5			4.5		pF
C _{io}	V _O = 3 V or 0	1			11			11		рF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS137B - MAY 1992 - REVISED FEBRUARY 1994

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

					SN54L	VT543			SN74L	VT543		4
				V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT
				MIN	MIN MAX		MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration	LEAB or LEBA low		3.3		3.3		3.3		3.3		ns
	Setup time	Data before LEAB or LEBA↑	High	0		≥ 0		0		0		ns ns
			Low	0.8		₹ 1.1		0.8		1.1		
tsu	Setup time	Data before CEAB or	High	0	1	, 0		0		0		
	l	CEBA↑ Low		0.9	Ž	1.2		0.9		1.2		
	Data after LEAB or LEBA↑		1.7	ĮŠ,	1.7		1.7		1.7		no	
^t h	rioid time	Data after CEAB or CEBA↑		1.8	Q"	1.8		1.8		1.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

	-			SN54L	VT543							
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V		C = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
,			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
^t PLH	A or B	B or A	1	4.9		5.7	1	2.9	4.7		5.5	ns
^t PHL		BUIA	1	4.8		6	1	3.3	4.6		5.8	115
tPLH .	tPLH LE	A or B	1	6.1	Z.	7.5	1	4	5.9		7.3	ns
t _{PHL}		AOIB	1	5.9	L)	7.5	1	4.1	5.7		7.3	115
tPZH	ŌĒ	A or B	1	6,	3 "	7.8	1	4.1	5.8		7.6	ns
tPZL	OE .	AUID	1.1	6.6		8.4	1.1	4.5	6.4		8.2	113
t _{PHZ}	ŌĒ	A or B	2.4	6.7		7.3	2.4	4.8	6.5		7.1	ns
t _{PLZ}	OE	AOIB	2	<i>§</i> ₹ 6		6.1	2	4	5.8		5.9	110
t _{PZH}	CE	A or B	1	6.2		7.8	1	4.2	6		7.6	ns
tPZL	OE .	A 01 B	1.4	6.9		8.5	1.4	4.7	6.7		8.3	113
t _{PHZ}	CE	A or B	2.3	6.6		7.3	2.3	4.7	6.4		7.1	ns
t _{PLZ})E	AUID	2	5.6		5.8	2	3.8	5.4		5.6	118

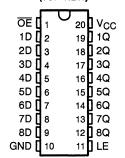
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

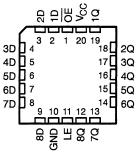
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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flatpacks (W), and DIPS (J)

SN54LVT573...J OR W PACKAGE SN74LVT573...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT573...FK PACKAGE (TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

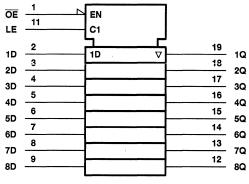
The SN54LVT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT573 is characterized for operation from –40°C to 85°C.

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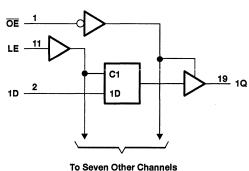
FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Η,	L	L
L	L	Χ	Q_0
Н	X	Χ	Z

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off	state, VO (see Note 1)0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT573	96 mA
SN74LVT573	128 mA
Current into any output in the high state, IO (see Note 2): SN54LV	/T573 48 mA
SN74L\	/T573 64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3):	DB package 0.6 W
· · · · · · · · · · · · · · · · · · ·	DW package 1.6 W
	PW package 0.7 W
Storage temperature range	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This current will only flow when the output is in the high state and $V_O > V_{CC}$.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS138B - MAY 1992 - REVISED FEBRUARY 1994

recommended operating conditions (see Note 4)

			SN54L	VT573	SN74L	UNIT		
			MIN	MAX	MIN MAX		UNIT	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧	
٧ _{IH}	High-level input voltage		2		2		V	
VIL	Low-level input voltage			0.8		0.8	V	
۷ı	Input voltage			5.5		5.5	V	
ЮН	High-level output current			-24		-32	mA	
lOL	Low-level output current			48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES **WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				54LVT5	73	SN	74LVT5	73	11517
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	lj = -18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	I _{OH} = -100 μA	-	VCC-C	.2		VCC-C).2		
V/~	$V_{CC} = 2.7 \text{ V},$	I _{OH} = - 8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						V
	ACC = 2 A	I _{OH} = -32 mA					2			
1	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	ACC = 2 A	I _{OL} = 48 mA				0.55				
		IOL = 64 mA							0.55	
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V				50			10	
1.		$V_I = V_{CC}$ or GND	Control pins			±1			±1	μА
lį.	V _{CC} = 3.6 V	V _I = V _{CC}	Data inputs			1			1	μА
		V _I = 0	Data Inputs			-5			-5	
l _{off}	V _{CC} = 0,	V_I or $V_O = 0$ to 4.5 V							±100	μΑ
1	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА
lH .	VCC = 3 V	V _I = 2 V	Data Inputs	-75			-75			μΛ
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
			Outputs high		0.13	0.39		0.13	0.19	
lcc	V _{CC} = 3.6 V,	$I_{\bigcirc} = 0$,	Outputs low		8.6	14		8.6	12	mA
100	V _I = V _{CC} or GND		Outputs disabled		0.13	0.39		0.13	0.19	1101
ΔICC§	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o	One input at V _{CC} – 0.6 r GND	V,			0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Со	V _O = 3 V or 0				8			8		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54L	VT573						
			VCC =	3.3 V 3 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
1			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high		3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	High or low	1		0.9		0.7		0.6		ns
th	Hold time, data after LE↓	High or low	1.8		2		1.6		1.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54L	VT573			SN	74LVT5	73					
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT			
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX				
t _{PLH}	D	Q	0.5	4.7		4.9	1	2.5	4.2		4.7	ns			
tPHL	D	<u> </u>	0.5	4.9		5.4	1	2.7	4.3		5.2	120			
t _{PLH}	LE	a	1	6		6.9	1.6	3.5	5.6		6.3	ns			
^t PHL	LL	y	1.4	6.9		7.6	2.5	4.3	6.5		7.2	110			
^t PZH	ŌĒ	Q	0.5	5.3		6.4	1	2.8	5.1		6.2	ns			
tPZL	OE .	3	0.7	5.7		7.2	1.3	3.3	5.5		6.6	110			
t _{PHZ}	ŌĒ	0	Q -		OE O	1.2	5.9		6.9	2	3.7	5.7		6.7	ns
tPLZ	OE	OE		1	5.4		5.5	1.5	3	4.6		5.1	115		

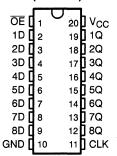
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

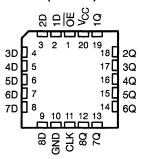
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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flatpacks (W), and DIPS (J)

SN54LVT574...J OR W PACKAGE SN74LVT574...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT574...FK PACKAGE (TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT574 is characterized for operation from –40°C to 85°C.

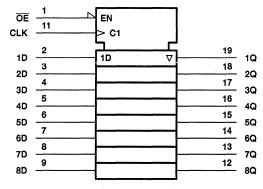
SCBS139B - MAY 1992 - REVISED FEBRUARY 1994

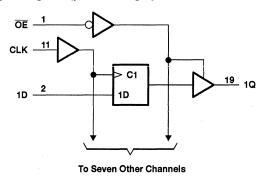
FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Χ	Q_0
Н	Χ	Χ	z

logic symbol†

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) -0.5 V to 7 V SN74LVT574 64 mA DW package 1.6 W PW package 0.7 W

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS139B - MAY 1992 - REVISED FEBRUARY 1994

recommended operating conditions (see Note 4)

			SN54L	VT574	SN74L	VT574	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
ViH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	V
٧ı	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	_	EST CONDITIONS		SN	154LVT5	74	SN	174LVT5	74	UNIT
PARAMETER	<u>'</u>	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII
VIK	V _{CC} = 2.7 V,	lլ = −18 mA				-1.2		\	-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C).2		VCC-C).2		
	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			v
, AOH	V _{CC} = 3 V	IOH = - 24 mA		2						· •
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
v_{OL}		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	, v
	VCC-0 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				50			10	
11		V _I = V _{CC} or GND	Control pins			±1			±1	μА
'1	V _{CC} = 3.6 V	V _I = V _{CC}	Data inputs			1			1	μΛ
		V _I = 0	Data Inputs			-5			-5	
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V							±100	μA
li (h. a.l.al)	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА
l(hold)	VCC = 0 V	V _I = 2 V	Data Inputs	-75			-75			μΛ
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ
			Outputs high		0.13	0.39		0.13	0.19	
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.7	14		8.7	12	mA
	V _I = V _{CC} or GND		Outputs disabled		0.13	0.39		0.13	0.19	
ΔlCC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – 0.6 r GND	V,			0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		рF
Со	V _O = 3 V or 0				8			8		рF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT574								
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	High or low	2		2.4		2		2.4		ns
th	Hold time, data after CLK↑	High or low	0.9		0.9		0.3		0		ns



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54LVT574				SN	74LVT5	74		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		٧	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
fmax			150		150		150			150		MHz
t _{PLH}	CLK	Q	1	5.9		6.6	1.7	3.6	5.4		6.2	ns
t _{PHL}	OLK	"	1	6.1		6.8	2.4	4.3	5.9		6.6	115
^t PZH	ŌĒ	Q	0.5	5.9		7.1	1	2.9	4.8		5.9	ns
tPZL	OE	۷	0.5	5.3		6.4	1.3	3.4	5.1		6.2	115
tPHZ	ŌĒ	0	0.7	5.9		6.6	1.9	4	5.5		5.9	
tPLZ	OE .	Q	0.5	5.1		5.1	1.7	3.2	4.5		4.5	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

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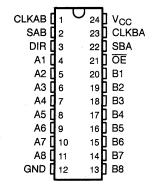
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flatpacks (W), and DIPS (JT)

description

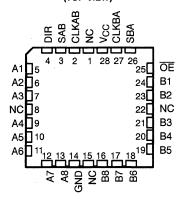
These bus transceivers and registers are designed specifically for low-voltage (3.3-V) $V_{\rm CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the

SN54LVT646 . . . JT OR W PACKAGE SN74LVT646 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT646...FK PACKAGE (TOP VIEW)



NC - No internal connection

A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



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description (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT646 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT646 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE

		INP	UTS			DATA	A I/Os	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Х	Х	1	Х	X	Х	Input	Unspecified [†]	Store A, B unspecified†
Х	X	X	1	· X	Χ,	Unspecified [†]	Input	Store B, A unspecified†
Н	Х	1	1	Х	Х	Input	Input	Store A and B data
Н	Х	H or L	H or L	Х	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	Χ	H.	Output	Input	Stored B data to A bus
L	Н	X	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	Х	Н	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS140B - MAY 1992 - REVISED JANUARY 1994

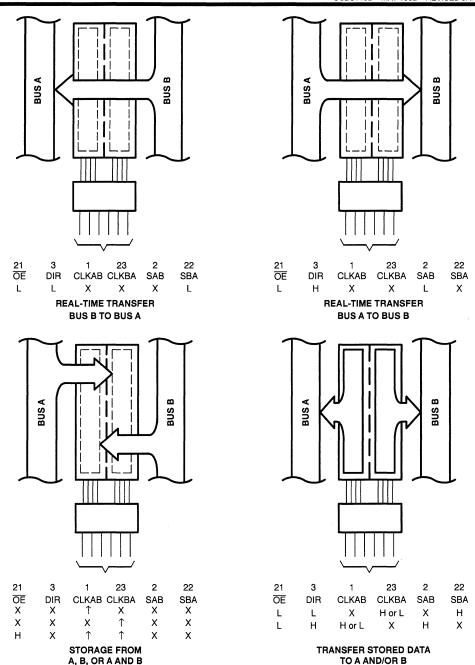


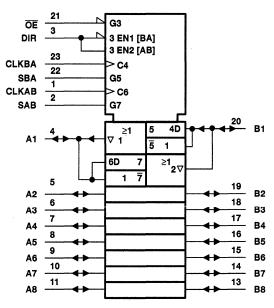
Figure 1. Bus-Management Functions

Pin numbers shown are for the DB, DW, JT, PW, and W packages.



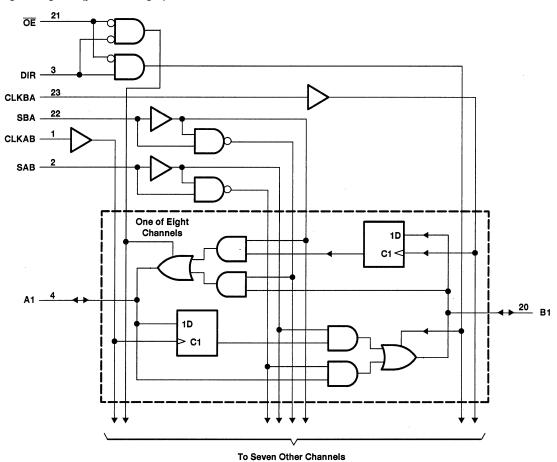
SN54LVT646, **SN74LVT646** 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS140B - MAY 1992 - REVISED JANUARY 1994

logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) .	
Current into any output in the low state, Io: SN54LVT646	
SN74LVT646	128 mA
Current into any output in the high state, I _O (see Note 2): \$N54LVT646	48 mA
SN74LVT646	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	
DW package	
PW package	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions (see Note 4)

			SN54L	VT646	SN74L	VT646	LINIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage	•		0.8		0.8	V
Vį	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	_	TEST CONDITIONS				46	SN	74LVT6	46	LIMIT
PARAMETER	I	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	l _{OH} = -100 μA		V _{CC} -C).2		VCC-0	.2		
Vari	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			V.
VOH	V _{CC} = 3 V	IOH = -24 mA		2						٧.
	ACC = 2 A	IOH = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	ACC = 2 A	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control pins			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins			10			10	
lj.	V _{CC} = 3.6 V	V _I = 5.5 V				100			20	μА
		VI = VCC	A or B ports§			1			1	
		V _I = 0				-5			-5	
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V							±100	μΑ
' ha is	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
^I I(hold)		V _I = 2 V	A of B ports	-75			-75			μ/\
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
^I OZL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ
			Outputs high		0.13	0.39		0.13	0.19	
loc	$V_{CC} = 3.6 \text{ V},$	IO = 0,	Outputs low		8.8	14		8.8	12	mA
lcc v	V _I = V _{CC} or GND	Outputs disabled		0.13	0.39		0.13	0.19	IIIA	
ΔICC [¶]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	One input at V _{CC} – 0.6 r GND	V,			0.3			0.2	mA
Ci	V _I = 3 V or 0				4.5			4.5		pF
C _{io}	V _O = 3 V or 0				11			11		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54L	VT646			SN74L	VT646		
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^f clock	Clock frequency		0	150	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
	Setup time, A or B before CLKAB↑ or	High	1.5		1.5		1.3		1.3		
tsu	CLKBA1	Low	2.5		3.0		2		2.4		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑		0.9		0.9		0.4		0.4		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54L	VT646			SN	74LVT6	46			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
fmax			150				150					MHz	
tPLH	CLKBA or	A or B	1.2	5.9		6.9	1.8	3.8	5.7		6.7	no	
t _{PHL}	CLKAB	AUID	1.2	5.9		6.6	2.1	3.8	5.7		6.4	ns	
^t PLH	A or B	B or A	0.8	4.9		5.6	1.3	2.8	4.7		5.4	ns	
t _{PHL}	AOIB	BULK	0.6	4.8		5.5	1	2.7	4.6		5.3	115	
t _{PLH}		CDA == CAD‡	A or B	1	6.4		7.4	1.4	3.7	6.2		7.2	ns
^t PHL	SBA or SAB†	AOIB	1	6.4		. 7	1.4	3.8	6.2		6.8	115	
tPZH	ŌĒ	A or B	0.6	6		7.4	1	3	5.8		7.2		
^t PZL	OE	AOrb	0.6	6.2		7.5	1	3.2	6		7.3	ns	
t _{PHZ}	ŌĒ	A or B	1.4	6.7		7.1	2.3	4.3	6.5		6.9	ns	
tPLZ	OE	AOIB	1.4	6.4		6.5	2.2	3.8	5.8		5.9	115	
^{-t} PZH	DIB	A or B	0.6	6.7		7.7	1	3.4	6.5		7.5		
tPZL	DIR	DIR A or B	0.8	6.5		7.3	1.2	3.4	6.3		7.1	ns	
t _{PHZ}	DIR	A a D	0.8	7.4		8.3	1.7	4.1	7.2		8.1		
tPLZ	חוט	A or B	1	6.7		7	1.5	3.5	5.8		6.3	ns	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

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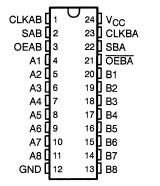
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (JT)

description

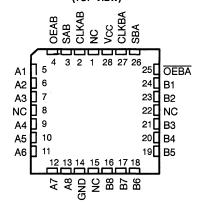
These bus transceivers and registers are designed specifically for low-voltage (3.3-V) $V_{\rm CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

SN54LVT652 . . . JT PACKAGE SN74LVT652 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT652...FK PACKAGE (TOP VIEW)



NC - No internal connection

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT652 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT652 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT652 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE

		INPU	гѕ			DATA	A 1/0†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FONCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	Н	1	1	X	Х	Input	Input	Store A and B data
X	Н	1.	H or L	X	Х	Input	Unspecified [‡]	Store A, hold B
Н	Н	1	1	X ‡	Х	Input	Output	Store A in both registers
L	X	H or L	1	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	1	1	X	X‡	Output	Input	Store B in both registers
L	L	X	Χ	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	Н	Output	Input	Stored B data to A bus
Н	Н	Χ	X	L	Х	Input	Output	Real-time A data to B bus
н	Н	H or L	X	Н	Х	Input	Output	Stored A data to B bus
н	L .	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

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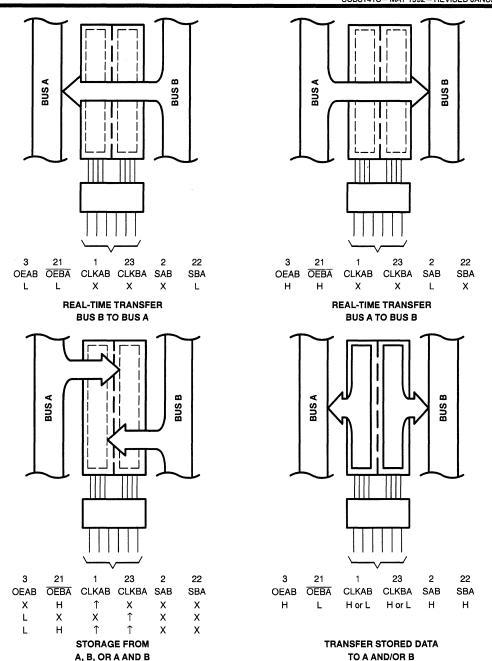


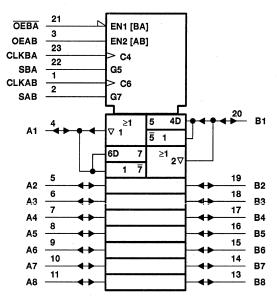
Figure 1. Bus-Management Functions

Pin numbers shown are for the DB, DW, JT, and PW packages.



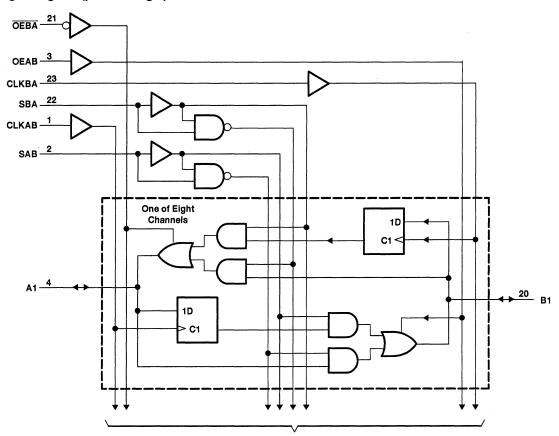
SCBS141C - MAY 1992 - REVISED JANUARY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DB, DW, JT, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high state or power-off state, V_{Ω} (see Note 1)	
Current into any output in the low state, Io: SN54LVT652	
SN74LVT652	
Current into any output in the high state, IO (see Note 2): SN54LVT652	48 mA
SN74LVT652	
Input clamp current, $I_{IK}(V_1 < 0)$	
Output clamp current, I_{OK} ($V_O < 0$)	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	
DW package	
PW package	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions (see Note 4)

			SN54L	VT652	SN74L	VT652	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	Ž.	2		٧
VIL	Low-level input voltage			Ø.0.8		0.8	٧
VI	Input voltage		. «	5.5		5.5	٧
ЮН	High-level output current		Į.	-24		-32	mA
loL	Low-level output current		Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Ŗ.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	_	FOT COUNTIONS		SN	54LVT6	52	SN	74LVT6	52	LINUT
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX‡,	I _{OH} = -100 μA		VCC-C).2		VCC-C	.2		
Vari	V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			2.4			V
VOH	V 2V	IOH = -24 mA		2						V
	V _{CC} = 3 V	IOH = -32 mA					2			
	V 27V	I _{OL} = 100 μA				0.2			0.2	
	V _{CC} = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Vai		I _{OL} = 16 mA				0.4			0.4	V
VOL	V 2V	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA		0.55						
		I _{OL} = 64 mA			1	2			0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Cambrol nine		2	±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins		8"	10			10	
lj	V _{CC} = 3.6 V	V _I = 5.5 V			/~	20			20	μΑ
		VI = VCC	A or B ports§	· «	37	5			5	
		V _I = 0		Š		-10			-10	
l _{off}	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$							±100	μΑ
lia in	V _{CC} = 3 V	V _j = 0.8 V	A or B ports	75			75			μА
l(hold)	vCC = 2 v	V _I = 2 V	A or B ports	-75			-75			μΑ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ
lozL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ
	,		Outputs high		0.13	0.19		0.13	0.19	
loo	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low		8.8	12		8.8	12	mA
100	$V_I = V_{CC}$ or GND		Outputs disabled		0.13	0.19		0.13	0.19	
∆ICC [¶]	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
C _i	V _I = 3 V or 0				4.5			4.5		pF
C _{io}	V _O = 3 V or 0				11			11		pF

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54L	VT652			SN74L	VT652		
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	. 0	150	MHz
t _W	Pulse duration, CLK high or lov	V			10.7		3.3		3.3		ns
	Setup time, A or B before	Data high		~Q\	K.		1.2		1.2		
^t su	CLKAB↑ or CLKBA↑	Data low		4,90			2		2.5		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑						0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54L	VT652			SN	74LVT6	52				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	± 0.3 V			2.7 V	UNIT		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX			
fmax							150			150		MHz		
tPLH	CLKBA or	A or B					1.8	3.7	6		6.9	ns		
tPHL	CLKAB	A OI B					2	3.7	5.7		6.4	113		
^t PLH	A or B	B or A					1.2	2.8	4.7		5.5	ns		
t _{PHL}	AUIB	BOIA			Ö		1	2.6	4.6		5.3	110		
t _{PLH}	004 - 048t	CDA CADT	SBA or SAB‡	A or B					1.4	3.7	6.4		7.6	ns
t _{PHL}	SBA OF SAB+	AOIB		Ŝ			1.4	4	6.2		6.8	110		
^t PZH	OEBA	Α		_SŠ ⁷			1	2.9	5.8		7.2	ns		
^t PZL	OEBA	A		K.			1	3	6		7.3	10		
tPHZ	OFFIA	Α		-W.			2.2	3.9	6.5		6.9	ns		
t _{PLZ}	OEBA	A					1.8	3.2	5.8		5.9	IIS		
^t PZH	OEAB	В					1	3.3	6.5		7.5			
^t PZL		В					1.2	3.4	6.3		7.1	ns		
t _{PHZ}	OEAR	OFAR R					1.7	4.5	7.2		8.1			
^t PLZ	OEAB	В					1.5	3.8	5.8		6.3	ns		

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

[‡] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and and Ceramic DIPs (JT)

description

These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high

SN54LVT2952 . . . JT PACKAGE SN74LVT2952 . . . DB. DW. OR PW PACKAGE (TOP VIEW) 24 🛮 V_{CC} В8 П B7 🛛 2 23 A8 В6 Пз 22 N A7 B5 **1**4 21 A6 B4 **∏** 5 20 A5 B3 | 6 19**∏** A4 18 A3 B2 [] 7 В1 П 17 T A2 OEAB 9 16 A1 CLKAB 10 15 OEBA

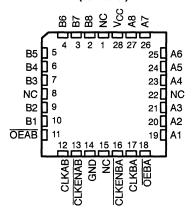
SN54LVT2952...FK PACKAGE (TOP VIEW)

14 CLKBA

13 CLKENBA

CLKENAB 11

GND 1 12



NC - No internal connection

transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT2952 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT2952 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT2952 is characterized for operation from -40°C to 85°C.



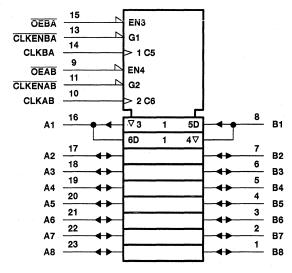
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FUNCTION TABLET

	INPUT	S		OUTPUT
CLKENAB	CLKAB	OEAB	Α	В
Н	Х	L	Х	B ₀ ‡
X	H or L	L	Χ	В ₀ ‡ В ₀ ‡
L	1	L	L	L
L	1	L	Н	н
Х	X	Н	Х	Z

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

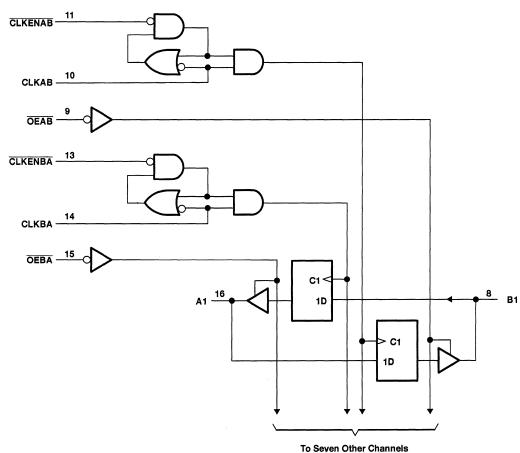
logic symbol§



 \S This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

[‡] Level of B before the indicated steady-state input conditions were established.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to Input voltage range, V _I (see Note 1)0.5 V to	
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)0.5 V t	
Current into any output in the low state, Io: SN54LVT2952	
SN74LVT2952	
Current into any output in the high state, IO (see Note 2): SN54LVT2952	8 mA
SN74LVT2952 6	4 mA
Input clamp current, $I_{ K }(V_1 < 0)$	0 mA
Output clamp current, I_{OK} ($V_O < 0$)	0 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	65 W
DW package	1.7 W
PW package).7 W
Storage temperature range ——65°C to 1	50°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions (see Note 4)

			SN54LV	T2952	SN74LV	T2952	LIMIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Ü	2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
٧ı	Input voltage		١	5.5		5.5	٧
ЮН	High-level output current		J. S	-24		-32	mA
loL	Low-level output current	`	25	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	- 33°	10		10	ns/V
TA	Operating free-air temperature		~-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	_	FOT COMPITIONS		SN	54LVT29	52	SN	74LVT29	52	LIMIT
PARAMETER	'	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	I _{OH} = -100 μA		VCC-C).2		VCC-C).2		
Vou	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	IOH = -24 mA		2						•
	VCC = 3 V	$I_{OH} = -32 \text{ mA}$					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VoL		$I_{OL} = 16 \text{ mA}$			0.4			0.4	V	
VOL	V _{CC} = 3 V	$I_{OL} = 32 \text{ mA}$				0.5			0.5	٧
	1 *CC = 0 *	I _{OL} = 48 mA				्0.55				
		IOL = 64 mA	<u>'</u>]		Ø			0.55	
	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND	Control pins	<u> </u>	ŢĞ.	` ±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins		,Q*	10			10	
l _l	V _{CC} = 3.6 V	V _I = 5.5 V]	L	<u>\$7</u>	20	<u> </u>		20	μΑ
		VI = VCC	A or B ports§	Ţ,	Q"	5			5	
		V _I = 0		S	ř	-10			-10	
loff	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5	V						±100	μΑ
lia i s	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 0 V	V _I = 2 V	A OF B PORTS	-75			-75			μ.
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ
	V 0.0 V	1- 0	Outputs high	<u> </u>	0.13	0.19		0.13	0.19	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	I _O = 0,	Outputs low		8.8	12		8.8	12	mΑ
		Outputs disabled		0.13	0.19		0.13	0.19		
ΔICC¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} of	$_{\rm CC}$ = 3 V to 3.6 V, One input at V $_{\rm CC}$ – 0.6 ther inputs at V $_{\rm CC}$ or GND				0.2			0.2	mA
C _i	V _I = 3 V or 0				4.5			4.5		рF
Cio	V _O = 3 V or 0				11.5			11.5		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT2952, SN74LVT2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS152C - MAY 1992 - REVISED FEBRUARY 1994

timing requirement over recommended operating free-air temperature range (unless otherwise noted)

					SN54LVT2952			SN74LVT2952				
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency								150		150	MHz
	Pulse duration		CLK high			,A		3.3		3.3		ns
t _w	Puise duration	Pulse duration				2.9		3.3		3.3		
		A or B	High	2.6		2.9		2.5		2.8		
١.	Oatum times hafana Ol I/A	AUB	Low	2.6	A	3.1		2.5		3		
t _{su}	Setup time before CLK↑	CE	High	0.9	.37	0.8		0.9		0.8		ns
		I CE	Low	2.5	Q'	2.7		2.4		2.7		
th	Hold time after CLK↑	A or B		1.5	Q*	0.7		1.5		0.7		ne
		CE		2.6		2.6		2.5		2.6		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54L	/T2952			SN	74LVT29	52			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
fmax					42		150			150		MHz	
tPLH	CLKBA or CLKAB	CLKBA or	A or B	1.3	6.4	2.7	7.4	1.3	3.6	6.1	2.7	7.1	ns
t _{PHL}		AOID	1.8	6.1	2.7	7	1.8	3.7	6	2.7	6.9	110	
tPZH	OEBA or OEAB	A or B	1	6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	ns	
tPZL		A 01 B	1.1	6.6	2.9	8.2	1.2	3.2	6.5	2.9	8	110	
tPHZ	OEBA or OEAB	A or B	1	ু	2.7	7.6	1	4.1	6.3	2.7	6.9	ns	
tPLZ		AUID	1.6	^ℚ .5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	115	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

General Information	1
LVT Octals	2
LVTZ Octals: Power-Up, 3-State	3
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LVTZ OCTALS

Features

- Power-up 3-state between 0 V and 1.5 V without an external pullup resistor or voltage supervisor is assured
- Mixed-mode circuitry
- Expanded V_{CC} range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- SOIC, EIAJ SSOP, and TSSOP packaging

Benefits

- Prevents loading and bus contention when V_{CC} is ramping during power up
- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family - not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion

SN54LVTZ240, SN74LVTZ240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

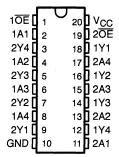
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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)
 Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

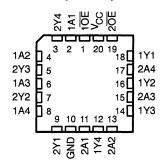
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTZ240 . . . J PACKAGE SN74LVTZ240 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTZ240 ... FK PACKAGE (TOP VIEW)



The 'LVTZ240 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTZ240 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTZ240 is characterized for operation from –40°C to 85°C.

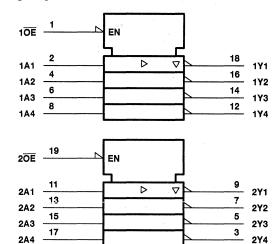
FUNCTION TABLE (each buffer)

INPL	JTS	OUTPUT
OE	Α	Y
L	Η	L
L	L	Н
Н	X	Z



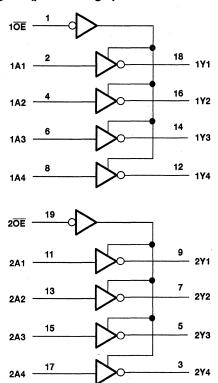
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supp	oly voltage range, V _{CC}	-0.5 V to 4.6 V
Input	t voltage range, V _I (see Note 1)	0.5 V to 7 V
Volta	ige range applied to any output in the high state or power-off state, V_{O} (see Note 1)	\dots -0.5 V to 7 V
Curre	ent into any output in the low state, IO: SN54LVTZ240	96 mA
	SN74LVTZ240	128 mA
Curre	ent into any output in the high state, IO (see Note 2): SN54LVTZ240	48 mA
	SN74LVTZ240	64 mA
Input	t clamp current, I _{IK} (V _I < 0)	50 mA
Outp	out clamp current, I _{OK} (V _O < 0)	50 mA
Maxir	mum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	0.6 W
	DW package	1.6 W
	PW package	0.7 W
Stora	age temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



SN54LVTZ240, SN74LVTZ240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS301 - SEPTEMBER 1993 - REVISED FEBRUARY 1994

recommended operating conditions

			SN54LV1	Z240	SN74LVTZ240		UNIT	
			MIN	MAX	MIN	MAX	ONII	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V	
ViH	High-level input voltage		2		2		V	
V _{IL}	Low-level input voltage			0,8		0.8	V	
۷Į	Input voltage			₹ 6.5		5.5	V	
ЮН	High-level output current			~24		-32	mA	
lOL	Low-level output current		Į, Ç	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V	
Δt/ΔV _{CC}	Power-up ramp rate		€200		200		μs/V	
TA	Operating free-air temperature		-55	125	-40	85	°C	

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	_	FOT COMPLETIONS		SN	54LVTZ2	40	SN	74LVTZ	240	UNIT
PARAMETER	ļ .	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	V _{CC} = 2.7 V,	lj = −18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C).2		VCC-0	.2		
Vari	V _{CC} = 2.7 V,	I _{OH} = -8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	I _{OH} = - 24 mA		2						· V
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	•
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		IOL = 64 mA					İ		0.55	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V				10			10	
l _l		VI = VCC or GND	Control pins		&	±1			±1	μА
. "	V _{CC} = 0 to 3.6 V	VI = VCC	Data pins		14	1			1	μΛ
		V _I = 0	Data piris		~	-5			-5	
loff	$V_{CC} = 0 V$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$		ئـــــــــــــــــــــــــــــــــــــ	\$				±100	μΑ
^l ozpu [¶]	$V_{CC} = 0 V \text{ to 1.5,}$	$V_O = 0.5 \text{ to } 3 \text{ V},$	OE = X	Ĵ	7				±50	μΑ
^I OZPD [¶]	$V_{CC} = 1.5 \text{ V to 0},$	$V_O = 0.5 \text{ to } 3 \text{ V},$	OE = X	Q ^C					±50	μΑ
11711-18	V _C C = 3 V	V _I = 0.8 V	A inputs	75			75			μА
li(hold)	VCC = 0 V	V _I = 2 V	Airiputs	-75			-75			μΛ
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μΑ
lozL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V		<u></u>		-5			-5	μΑ
			Outputs high		0.12	0.5		0.12	0.225	
Icc	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low		8.6	14		8.6	12	mA
.00	V _I = V _{CC} or GND		Outputs disabled		0.12	0.5		0.12	0.225	
Δl _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	One input at V _{CC} – 0.6 r GND	3 V,			0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

[¶] This parameter is guaranteed by characterization.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 4)

				SN54LVTZ240				SN74LVTZ240						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	V	± 0.3 V	٧	V _{CC} =	2.7 V	UNIT		
			MIN	MAX	WIN	MAX	MIN	TYPT	MAX	MIN	MAX			
^t PLH	А		1	4.5	35	5.4	1	2.5	4.3		5.2	no		
t _{PHL}	^	, , , , , , , , , , , , , , , , , , ,	1	4.5	8	5.2	1	2.5	4.3		5	ns		
^t PZH	ŌĒ		1	5.4	~	6.5	1	2.7	5.2		6.3	ns		
t _{PZL}) OE	ľ	1	5.4		7.4	1	3.1	5.2		6.7	115		
tPHZ	ŌĒ	Y	2	25.8		6.5	2	3.9	5.6		6.3	ns		
tPLZ			1.6	₡ 5.3		5.8	1.6	3.2	5.1		5.6	115		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)
 Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

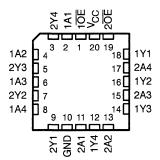
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTZ244 . . . J PACKAGE SN74LVTZ244 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTZ244 . . . FK PACKAGE (TOP VIEW)



The 'LVTZ244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTZ244 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTZ244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	UTS	OUTPUT
ŌE	Α	Υ
L	Н	Н
L	L_	L
Н	Χ	Z

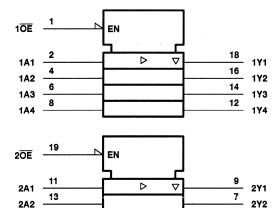
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logic symbol†

15

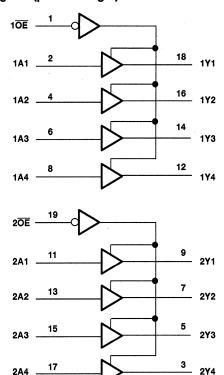
17

2A3



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

5 2Y3

3 2Y4

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVTZ244	96 mA
SN74LVTZ244	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTZ244	48 mA
SN74LVTZ244	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	
DW package	
PW package	
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



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recommended operating conditions

			SN54LV	TZ244	SN74LV	TZ244	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		. 2	12	2		V
VIL	Low-level input voltage			0.8		0.8	V
٧ _I	Input voltage			5.5		5.5	V
ЮН	High-level output current			҈ −24		-32	mA
loL	Low-level output current		1 35	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	20"	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		₹200		200		μs/V
TA	Operating free-air temperature	,	-55	125	-40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	_	FOT COMPLETIONS	•	SN	54LVTZ2	44	SN	74LVTZ	244	
PARAMETER	•	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNIT
VιK	$V_{CC} = 2.7 \text{ V},$	l _l = –18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to MAX}^{\ddagger}$,	I _{OH} = -100 μA		VCC-C).2		VCC-C).2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						· ·
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
v_{OL}		I _{OL} = 16 mA				0.4			0.4	v
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	'
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		IOL = 64 mA							0.55	
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V				10			10	
lj .		V _I = V _{CC} or GND	Control pins			/ ±1			±1	μА
'1	V _{CC} = 0 to 3.6 V	V _I = V _{CC}	Data pins		- ()	1			1	μ.Α.
		V _I = 0	Data pins		Z.	-5			-5	
loff	V _{CC} = 0 V,	V_1 or $V_0 = 0$ to 4.5 V		Ŝ	<u> </u>				±100	μΑ
^I OZPU [¶]	$V_{CC} = 0 V \text{ to 1.5,}$	$V_O = 0.5 \text{ to } 3 \text{ V},$	OE = X	٥	7				±50	μА
^I OZPD [¶]	$V_{CC} = 1.5 \text{ V to 0},$	$V_O = 0.5 \text{ to 3 V},$	OE = X	₫ [©]					±50	μА
1175-1-15	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75			75			μА
l(hold)		V _I = 2 V	Allipuis	-75			-75			μΛ
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μΑ
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μΑ
			Outputs high		0.12	0.5		0.12	0.225	
Icc	V _{CC} = 3.6 V,	l _O = 0,	Outputs low		8.6	14		8.6	12	mA
	V _I = V _{CC} or GND		Outputs disabled		0.12	0.5		0.12	0.225	
ΔI _{CC} §	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o	One input at V _{CC} – 0.6 r GND	V,			0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

[¶] This parameter is guaranteed by characterization.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

			SN54LVTZ244									
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	Vo	CC = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	Α		1	4.7	.5	5.2	1	2.5	4.1		5	ns
^t PHL	^	, , , , , , , , , , , , , , , , , , ,	1	4.4	Æ.	5.4	1	2.5	4.1		5.2	115
t _{PZH}	ŌĒ	V	1	5.4		6.5	1	2.7	5.2		6.3	ns
t _{PZL}	OE .	'	1.1	5,4	,	7.6	1.1	3.1	5.2		6.7	115
t _{PHZ}	ŌĒ	Y	1.9	6.2		6.9	1.9	3.9	5.6		6.3	
tPLZ	J OE		1.8	₹5.5		6	1.8	3.2	5.1		5.6	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

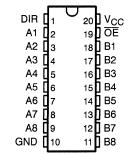
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)
 Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

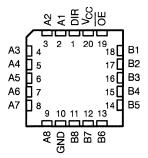
description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTZ245... J PACKAGE SN74LVTZ245... DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTZ245 . . . FK PACKAGE (TOP VIEW)



The 'LVTZ245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTZ245 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTZ245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

I	NPUTS	OPERATION
OI	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

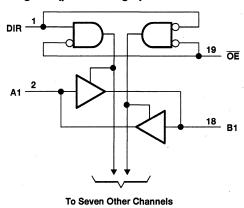
TEXAS INSTRUMENTS

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logic symbol†

ŌĒ DIR 3EN1[BA] 3EN2[AB] 18 В1 2∇ 17 16 вз АЗ 15 В4 14 Α5 **B**5 13 Α6 **B6** 12 **A7 B7** 9 11 **B8**

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVTZ245	96 mA
SN74LVTZ245	128 mA
Current into any output in the high state, I _O (see Note 2): SN54LVTZ245	48 mA
SN74LVTZ245	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	
DW package	1.6 W
PW package	
Storage temperature range	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and VO > VCC.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS303 - DECEMBER 1993 - REVISED FEBRUARY 1994

recommended operating conditions

			SN54LV	TZ245	SN74LV	TZ245	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIН	High-level input voltage		2	,sh	2		V
VIL	Low-level input voltage			8.0		0.8	V
VI	Input voltage		Á	5.5		5.5	V
lОН	High-level output current			-24		-32	mA
lOL	Low-level output current		3	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	1,0"	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		[©] 200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	_	EST CONDITIONS		SN	54LVTZ2	245	SN	74LVTZ2	245	UNIT
PANAMETER	! !	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	V _{CC} = 2.7 V,	i _j = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX‡,	I _{OH} = -100 μA	······································	VCC-C	.2		VCC-C).2		
¥	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			.,
VОН	V 2V	I _{OH} = -24 mA		2						V
	V _{CC} = 3 V	I _{OH} = -32 mA			,,,		2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
V		I _{OL} = 16 mA				0.4			0.4	V
V_{OL}	\\ 0\\	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Combust mins			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins		3	10			10	
lį		V _I = 5.5 V			34	100			20	μA
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		~	5			5	
		V _I = 0	1		<u>.</u> 3	-10			-10	
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V		á	>				±100	μΑ
lozpu [¶]	V _{CC} = 0 to 1.5 V,	$V_O = 0.5 \text{ V to 3 V},$	OE = X	4°					±50	μА
^I OZPD [¶]	V _{CC} = 1.5 V to 0,	$V_O = 0.5 \text{ V to 3 V},$	OE = X						±50	μА
l	V 2V	V _I = 0.8 V	A or B ports	75			75			
l(hold)	V _{CC} = 3 V	V _I = 2 V	A or B ports	-75			-75			μА
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V	*			-1			-1	μА
			Outputs high		0.13	0.5		0.13	0.19	
ICC	V _{CC} = 3.6 V,	I _O = 0,	Outputs low		8.8	14		8.8	12	mA
.00	V _I = V _{CC} or GND		Outputs disabled		0.13	0.5		0.13	0.19	111/4,
ΔICC#	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	One input at V _{CC} – 0.6 r GND	V,			0.3			0.2	mA
Ci	V _I = 3 V or 0	, S			4			4		pF
C _{io}	V _O = 3 V or 0				10			10		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

[¶] This parameter is guaranteed by characterization.

[#]This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

			SN54LVTZ245									
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
	·		MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1	4.6	.54	5.3	1	2.5	4		5.2	ns
^t PHL	AOIB	BUA	1	4.1	24	5.7	1	2.5	4		5.5	113
^t PZH	ŌĒ	A or B	1.1	6.1	~	7.2	1.1	3.3	5.9		7.1	ns
tPZL	OE .	7016	1.5	6.6		8	1.5	3.8	6.5		7.9	113
t _{PHZ}	OE.	ŌĒ A or B	2.2	6.2		7	2.2	4.3	5.9		6.5	ns
tPLZ	OE .		2	₡ 6.3		5.9	2	3.9	5.5		5.6	118

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

General Information	1
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Features

- State-of-the-art 0.8-μ EPIC-IIB™ BiCMOS process
- No input-diode clamp to V_{CC}
- Fully compatible (input and output) with 5-V systems
- −32-mA/64-mA drive current
- Low standby current (90 μA–190 μA)
- Bus-hold cell on data inputs and I/O pins
- 2.7-V to 3.6-V V_{CC} range
- JEDEC SSOP Widebus™ and EIAJ TSSOP Shrink Widebus™ packaging
- TI has established alternate sources

Benefits

- Propagation delays as fast as 4.1 ns maximum for improved performance
- Interfaces directly to industry standard buses and 5-V integrated circuits
- Supports live insertion
- Drives large loads, buses, or memory arrays
- Extends battery life
- Eliminates passive pullup resistors on local buses
- Fully characterized for unregulated battery operation
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

SN54LVT162240, SN74LVT162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS259A - JULY 1993 - REVISED FEBRUARY 1994

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments
 Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162240 . . . WD PACKAGE SN74LVT162240 . . . DGG OR DL PACKAGE (TOP VIEW)

		7-7-	
10E [1	O 48	2 <u>0E</u>
1Y1 [2		1A1
1Y2 [3	46	1A2
GND [4	45	GND
1Y3 [1A3
1Y4 [43] 1A4
V _{CC}			Vcc
2Y1 [2A1
2Y2 [2A2
GND [GND
2Y3 🛚			2A3
2Y4 🛚			2A4
3Y1 [3A1
3Y2 [3A2
GND [34] GND
3Y3 [33] 3A3
3Y4 [32	3A4
v _{cc} [18	31	Vcc
4Y1 [4A1
4Y2 [4A2
GND [] GND
4Y3 [] 4A3
4Y4 [] 4A4
40E [24	25	30E

description

The 'LVT162240 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to $12 \, \text{mA}$, include $22 - \Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SN54LVT162240, SN74LVT162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS259A - JULY 1993 - REVISED FEBRUARY 1994

description (continued)

The SN74LVT162240 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	L
L	L	Н
н	Χ	Z



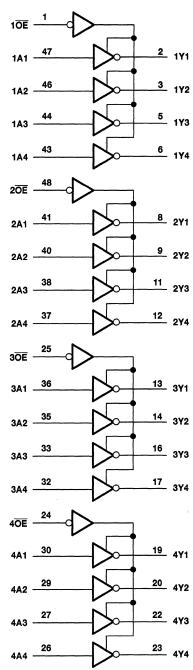
SN54LVT162240, SN74LVT162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS259A – JULY 1993 – REVISED FEBRUARY 1994

logic symbol†

1ŌE	1	EN1				
2OE	48	EN2				
30E	25	EN3				
4OE	24	EN4				
40L		Γ"		_	l	
1A1	47	Γ'''	1	1▽	2	1Y1
1A2	46				3	1Y2
1A3	44				5	1Y3
1A4	43	<u> </u>			6	1Y4
2A1	41	J	1	2 ▽	8	2Y1
2A2	40	<u> </u>	·		9	2Y2
2A2	38				11	
2A3	37				12	2Y3
	36	}	1	3 ▽	13	2Y4
3A1	35	├		3 ∨	14	3Y1
3A2	33	├			16	3Y2
3A3	32	-			17	3Y3
3A4	30	 		4	19	3Y4
4A1	29	 	1	4 ▽	20	4Y1
4A2	27	 			22	4Y2
4A3	26	<u> </u>			23	4Y3
4A4		<u> </u>			<u> </u>	4 Y 4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN54LVT162240, SN74LVT162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS259A - JULY 1993 - REVISED FEBRUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) .	
Current into any output in the low state, IO	30 mA
Current into any output in the high state, IO (see Note 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	
DL package	
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and VO > VCC.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

					SN74LV	T162240	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	H High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	V
ЮН	OH High-level output current			-12		-12	mA
IOL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



SN54LVT162240, SN74LVT162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS **WITH 3-STATE OUTPUTS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		TEST CONDITIONS		SN54LVT	162240	0 SN74LVT162240		
PARAMETER		TEST CONDITIONS			MAX	MIN	MAX	UNIT
VIK	V _{CC} = 2.7 V,	l _l = -18 mA			-1.2		-1.2	٧
VOH	V _{CC} = 3 V,	I _{OH} = - 12 mA		2		2		V
V _{OL}	V _{CC} = 3 V,	I _{OL} = 12 mA			0.8		8.0	٧
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V			10		10	
١.		$V_I = V_{CC}$ or GND	Control pins		±1		±1	
4	$V_{CC} = 3.6 V,$	VI = VCC	Data nina		1		1	μΑ
		V _I = 0	Data pins		-5		-5	
l _{off}	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$	′				±100	μА
lia i n	V _{CC} = 3 V	V ₁ = 0.8 V	A inputs	75		75		μА
l(hold)	VCC = 3 V	V _I = 2 V	Airiputs	-75		-75		щ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			1		1	μА
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V			-1		-1	μА
			Outputs high		0.19		0.1	
lcc	$V_{CC} = 3.6 \text{ V}, \qquad I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	1O = 0,	Outputs low		5		5	mA
	At = ACC or GIAD		Outputs disabled		0.19		0.1	
Δl _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND				0.2		0.2	mA
Ci	V _I = 3 V or 0							рF
Co	V _O = 3 V or 0		_					pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. § This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT16244A, SN74LVT16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments
 Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16244A . . . WD PACKAGE SN74LVT16244A . . . DGG OR DL PACKAGE (TOP VIEW)

		
1 OE	d , C	48 2 0E
1Y1	2	47 🕽 1A1
1Y2	[]3	46] 1A2
GND	[]4	45 🕽 GND
1Y3	[]5	44 🛘 1A3
1Y4	[]6	43 [] 1A4
v_{cc}	[]7	42] V _{CC}
2Y1	[]8	41 🛮 2A1
2Y2	[]9	40 🛮 2A2
GND	10	39 🕽 GND
2Y3	[] 11	38 🛘 2A3
2Y4		37] 2A4
3Y1	13	36 🛚 3A1
3Y2		35 🛘 3A2
GND		34 🛘 GND
3Y3	[] 16	33 🛘 3A3
3Y4		32] 3A4
V_{CC}	18	31 🕽 V _{CC}
4Y1		30] 4A1
4Y2		29 🛮 4A2
GND		28 🛛 GND
] 22	27 [] 4A3
4Y4		26 [] 4A4
4 0E	[]24	25 3 0E

description

The 'LVT16244A is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

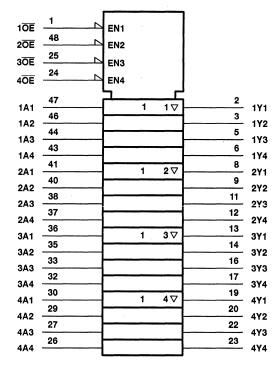
The SN74LVT16244A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16244A is characterized for operation from –40°C to 85°C.

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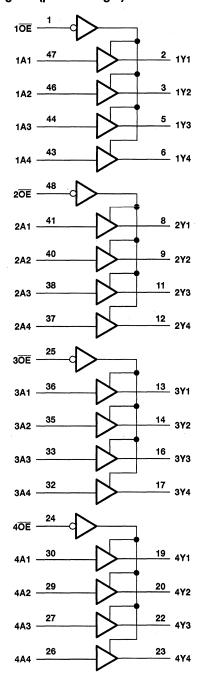


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} —0.5 Input voltage range, V_{I} (see Note 1) —0	.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)0	.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16244A	96 mA
SN74LVT16244A	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16244A	48 mA
SN74LVT16244A	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, $I_{OK}(V_O < 0)$	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.2 W
Storage temperature range –65°C	C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LV	T16244A	SN74LV1	16244A	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	H High-level input voltage		2	47	2		٧
VIL	Low-level input voltage			Ø.8		0.8	V
٧ı	Input voltage			[©] 5.5		5.5	V
IОН	High-level output current		٥.	~ -24		-32	mA
lOL	Low-level output current		ß	48		64	mA `
Δt/Δν	Input transition rise or fall rate	Outputs enabled	1 27	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT16244A, SN74LVT16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				SN54LVT16244A SN7			SN74LVT16244A		
PARAMETER		TEST CONDITIONS		MIN	MAX	MIN	TYPT	MAX	UNIT	
٧ _{IK}	V _{CC} = 2.7 V,	ij = -18 mA		-1.2			-1.2	V		
	V _{CC} = MIN to MAX‡,	I _{OH} = -100 μA	V _{CC} -0.2		VCC-C).2				
Vari	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4		2.4			v	
VOH	V- 0V	I _{OH} = -24 mA		2					V	
	V _{CC} = 3 V	I _{OH} = -32 mA				2	7			
	V 07V	I _{OL} = 100 μA			0.2			0.2		
	V _{CC} = 2.7 V	I _{OL} = 24 mA			0.5			0.5		
		I _{OL} = 16 mA			0.4		*	0.4	.,	
VOL	V 0V	I _{OL} = 32 mA			0.5			0.5	٧	
	V _{CC} = 3 V	I _{OL} = 48 mA		0,55						
		I _{OL} = 64 mA			Ø.			0.55		
	$V_{CC} = 0$ or MAX [‡] , $V_I = 5.5 \text{ V}$				10 ±1			10		
l.		VI = VCC or GND	Control pins		` ±1			±1		
-II	V _{CC} = 3.6 V	V _I = V _{CC}	Data sina	.Ş.	1			1	μА	
		V _I = 0	Data pins	ि	-5			-5		
loff	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$	•	S.				±100	μΑ	
lia in	V 2 V	V _I = 0.8 V	A inquito	75		75				
l(hold)	VCC = 3 V	V _I = 2 V	A inputs	-75		-75			μА	
lozh	V _{CC} = 3.6 V,	V _O = 3 V			5			5	μА	
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μА	
		Outputs high	Outputs high		0.09			0.09		
Icc	$V_{CC} = 3.6 \text{ V}, \qquad I_{O} = 0,$	IO = 0,	Outputs low		5			5	mA	
	V _I = V _{CC} or GND		Outputs disabled		0.09			0.09		
Δl _{CC} §	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA	
Ci	V _I = 3 V or 0						4		pF	
Со	V _O = 3 V or 0	,					10		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT16244A, SN74LVT16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER				SN54LV	T16244A			UNIT				
	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	}
t _{PLH}	۸	Y	1	4.2	75	5.1	1	2.3	4.1		5	
^t PHL	A		1	4.2	S.º	5.3	1	2.3	4.1		5.2	ns
tPZH	ŌE Y		1	5.3,	*	6.4	1	2.6	5.2		6.3	ns
^t PZL		1	5.8		6.8	1	2.6	5.2		6.7	115	
^t PHZ	ŌĒ	V	2.1	5.9		6.4	2.2	3.9	5.7		6.3	
tPLZ	OE	· '	1.9	₹ 5.3		5.7	2	3.7	5.1		5.6	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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28 GND

27 **[**] 4A3 26 **[**] 4A4

25 3OE

GND 1 21

4Y3 [] 22

4Y4 **1**23

40E **1**24

 Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required 	SN54LVT162244 WD PACKAGE SN74LVT162244 DGG OR DL PACKAGE (TOP VIEW)
 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation 	1OE 1 48 2OE 1Y1 2 47 1A1 1Y2 3 46 1A2 GND 4 45 GND
 Members of the Texas Instruments Widebus™ Family 	1Y3 0 5 44 1 1A3 1Y4 0 6 43 1 1A4
 Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V VCC) 	V _{CC}
 Supports Unregulated Battery Operation Down to 2.7 V 	GND 0 10 39 0 GND 2Y3 0 11 38 0 2A3
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	2Y4 [] 12 37 [] 2A4 3Y1 [] 13 36 [] 3A1
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model 	3Y2 [] 14 35 [] 3A2 GND [] 15 34 [] GND 3Y3 [] 16 33 [] 3A3
(C = 200 pF, R = 0) ■ Latch-Up Performance Exceeds 500 mA	3Y4 0 17 32 0 3A4 V _{CC} 0 18 31 0 V _{CC}
Per JEDEC Standard JESD-17	4Y1 [] 19 30 [] 4A1 4Y2 [] 20 29 [] 4A2

 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise

Bus-Hold Data Inputs Eliminate the Need

for External Pullup Resistors

Supports Live Insertion

Flow-Through Architecture Optimizes
 PCB Layout

 Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

description

The 'LVT162244 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical \overline{OE} (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include $22-\Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated.



SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

The SN74LVT162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	UTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Ι	Х	Z

SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS

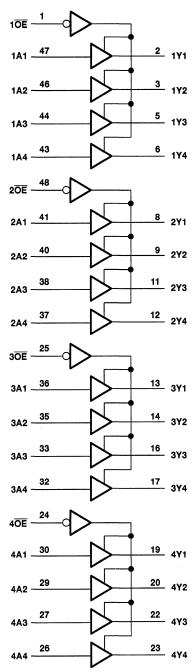
WITH 3-STATE OUTPUTS SCBS258A – JUNE 1993 – REVISED FEBRUARY 1994

logic symbol†

					- 1	
10E	1	EN1				
20E	48	EN2				
3OE	25	EN3				
40E	24	EN4				
40E		L ''''		لے		
1A1	47		1	1 ▽	2	1Y1
1A2	46	_			3	1Y2
1A3	44				5	1Y3
1A4	43	_			6	1Y4
2A1	41		1	2 ▽	8	2Y1
2A2	40	_			9	2Y2
2A3	38	_			11	2Y3
2A4	37				12	2Y4
3A1	36		1	3 ▽	13	3Y1
3A2	35				14	3Y2
3A3	33				16	3Y3
3A4	32				17	3Y4
4A1	30	 	1	4 ▽	19	4Y1
4A2	29		•		20	4Y2
4A3	27				22	4Y3
4A4	26	\vdash			23	4Y4
7/17		L				717

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS258A - JUNE 1993 - REVISED FEBRUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) .	0.5 V to 7 V
Current into any output in the low state, IO	30 mA
Current into any output in the high state, I _O (see Note 2)	30 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and VO > VCC.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

				T162244	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	ONIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
Іон	High-level output current			-12		-12	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS258A - JUNE 1993 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SN5	4LVT162	244	SN7				
PARAMETER		TEST CONDITIONS				MAX	MIN	TYPT	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	l _l = −18 mA	·			-1.2			-1.2	٧	
Voн	V _{CC} = 3 V,	I _{OH} = - 12 mA		2			2			V	
VOL	V _{CC} = 3 V,	I _{OL} = 12 mA				0.8			0.8	٧	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V				10			10		
1.		V _I = V _{CC} or GND	Control pins			±1			±1	μА	
lį	V _{CC} = 3.6 V	V _I = V _{CC}	Data sina		1	1			1		
	[.	V _I = 0	Data pins			-5			-5	ĺ	
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V						±100	μА	
		V _I = 0.8 V	V _I = 0.8 V				75			T	
^I I(hold)	V _{CC} = 3 V	V _I = 2 V	A inputs	-75			-75			μА	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μΑ	
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μА	
			Outputs high			0.19			0.09	mA	
ICC	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Outputs low			5			5		
Al = ACC or GIAD		Outputs disabled			0.19			0.09			
Δl _{CC} §	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC}	One input at V _{CC} – or GND	0.6 V,			0.2			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Co	V _O = 3 V or 0				10			10		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 5)

				SN54LV	T162244			SN7	4LVT162	244		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		Vcc =	2.7 V	V	± 0.3 V	V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
t _{PLH}	А	Υ	1.4	5.2		6.1	1.4	3.2	4.9		5.8	ns
t _{PHL}	^		1.1	5.1		6.3	1.1	3.1	5		6.1	115
^t PZH	ŌĒ	V	1	6.6		7.3	1	4.7	6.4		7.1	ns
^t PZL	OE	1	1.4	5.7		7.4	1.4	3.4	5.6		7.3	115
tPHZ	ŌĒ	V	2.6	6.9		7.6	2.6	4.5	6.6		7.3	ns
tPLZ		ľ	2.6	6.1		6.8	2.6	3.6	5.8		6.5	115

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

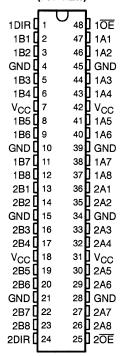
^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT16245A, SN74LVT16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143B - MAY 1992 - REVISED MARCH 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Packaged in Plastic 300-mil Shrink
 Small-Outline (DL) and Thin Shrink
 Small-Outline (DGG) Packages and 380-mil
 Fine-Pitch Ceramic Flat (WD) Packages
 Using 25-mil Center-to-Center Spacings

SN54LVT16245A... WD PACKAGE SN74LVT16245A... DGG OR DL PACKAGE (TOP VIEW)



description

The 'LVT16245A is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16245A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16245A is characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS

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SCBS143B - MAY 1992 - REVISED MARCH 1994

FUNCTION TABLE (each 8-bit section)

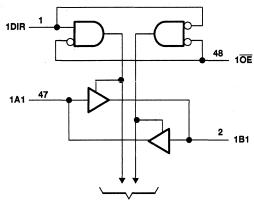
INP	UTS	ODEDATION
ŌE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	×	Isolation

logic symbolt

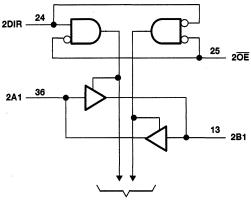
10E G3 3 EN1 [BA] 1DIR 3 EN2 [AB] 25 G6 2OE 24 2DIR 6 EN4 [BA] 6 EN5 [AB] 1A1 1B1 ◁ 2∇ \triangleright 46 1B2 1A2 44 5 1A3 1**B**3 43 6 1A4 1**B**4 8 41 1B5 1A5 40 9 1A6 1**B**6 38 11 1A7 1**B**7 37 12 1A8 1**B**8 36 13 2A1 2B1 ◁ 5∇ \triangleright 35 14 2A2 2B2 16 33 2A3 2B3 32 17 2B4 2A4 30 19 2A5 2B5 29 20 2B6 2A6 27 22 2A7 2B7 26 23 2A8 2B8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SCBS143B - MAY 1992 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, IO: SN54LVT16245A	
SN74LVT16245A	
Current into any output in the high state, IO (see Note 2): SN54LVT16245A	
SN74LVT16245A	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and VO > VCC.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LV	Г16245А	SN74LV	Г16245А	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3,6	2.7	3.6	V
VIH	High-level input voltage	2	Ø	2		V	
VIL	Low-level input voltage		0.8		0.8	V	
VI	Input voltage		,4	ૈ 5.5		5.5	V
ІОН	High-level output current		Ş	-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S. S.	10		10	ns/V
T _A	Operating free-air temperature			125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SCBS143B - MAY 1992 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	AMETER TEST CONDITIONS			SN5	4LVT162	45A	SN74LVT16245A			UNIT
PARAMETER			MIN	TYPT	MAX	MIN	TYPT	MAX	UNII	
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = –18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C).2		VCC-C).2		
V	$V_{CC} = 2.7 \text{ V},$	IOH = - 8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						ı v
	ACC = 2 A	IOH = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
,		I _{OL} = 16 mA				0.4			0.4	v
VOL	V 2V	I _{OL} = 32 mA				0.5			0.5	· ·
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		i _{OL} = 64 mA				0.55		İ		
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Commel mine		, é				±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins	<i>y</i> 10		10				
lj		V _I = 5.5 V			.~	20			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		S	1			1	
		V _I = 0			Ş Y	-5			-5	
loff	V _{CC} = 0,	$V_{1} \text{ or } V_{0} = 0 \text{ to } 4.5$	V	45					±100	μA
lia in	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			
l(hold)	ACC = 2 A	V ₁ = 2 V	A or B ports	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1		,	1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μA
			Outputs high			0.09			0.09	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low			5			5	mA
	AI = ACC OLGIND		Outputs disabled			0.09			0.09	
ΔICC [¶]	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0			1	11	***************************************		11		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS143B - MAY 1992 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

			SN54LVT16245A			SN74LVT16245A						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =		V _{CC} =	2.7 V	V	CC = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
^t PLH	A or B	B or A			34		1	2.4	4.1		5	ns
^t PHL	AOIB	BUIA			Æ.		1	2.3	4.1		5.2	115
^t PZH	OF.	A or B			· .		1	3	5.3		6.3	ns
t _{PZL}	ŌĒ	AUID		Ň			1	3.1	5.2		6.7	113
^t PHZ	ŌĒ	A or B		33			2.7	4.6	6.4		7.2	ns
t _{PLZ}		AUD		4			2.6	4.3	5.8		6.1	115

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SCBS260A - JUNE 1993 - REVISED FEBRUARY 1994

•	A-Port Outputs Have Equivalent 22-Ω
	Series Resistors, So No External Resistors
	Are Required

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162245 . . . WD PACKAGE SN74LVT162245 . . . DGG OR DL PACKAGE (TOP VIEW)

1DIR	1	U	48	10E
1B1 🛚	2		47	1A1
1B2 [3] 1A2
GND [4] GND
1B3 🛚	5		44	1A3
1B4 [43] 1A4
V _{CC} [7		42	Vcc
1B5 [8		41] 1A5
1B6 🛚			40	1A6
GND [39] GND
1B7 [] 1A7
1B8 🛚				1A8
2B1 🛛			36	2A1
2B2 [35	2A2
GND [34] GND
2B3 [2A3
2B4 🛛			32	2A4
v _{cc} [31	Vcc
2B5 🛛				2A5
2B6 [2A6
GND [] GND
2B7 🛛				2A7
2B8 [2A8
2DIR [24		25	20E
1				ı

description

The 'LVT162245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include $22-\Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SCBS260A - JUNE 1993 - REVISED FEBRUARY 1994

description (continued)

The SN74LVT162245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

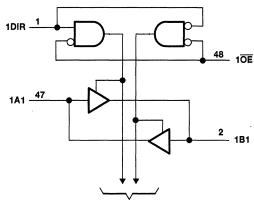
INP	UTS	ODERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L.	Н	A data to B bus
Н	X	Isolation

logic symbol†

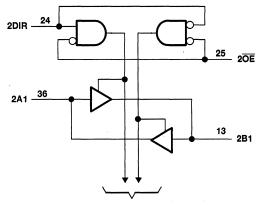
10E G3 1DIR 3 EN1 [BA] 3 EN2 [AB] 25 G6 2OE 24 2DIR 6 EN4 [BA] 6 EN5 [AB] ▽ 1 1B1 ◁ \triangleright 2∇ 46 1A2 1**B**2 5 44 1A3 1**B**3 43 6 1A4 1**B**4 41 8 1**B**5 1A5 40 9 1A6 1**B**6 38 11 1A7 **1B7** 37 12 1A8 1**B**8 36 13 2B1 2A1 ◁ D 5 ▽ 35 14 2A2 2**B**2 33 16 2A3 2B3 32 17 2A4 2B4 30 19 2B5 2A5 20 2A6 2B6 27 22 2A7 2B7 23 2A8 2B8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels



SCBS260A - JUNE 1993 - REVISED FEBRUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT162245 (except A port)
SN74LVT162245 (except A port)
A port
Current into any output in the high state, I _O (see Note 2): SN54LVT162245 (B port)
SN74LVT162245 (B port)
A port
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package 0.85 W
DL package 1.2 W
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and VO > VCC.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LV	Γ162245	SN74LV	Γ162245	
		•	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
٧ _{IH}	High-level input voltage		2		2		V
VIL	Low-level input voltage		0.8		0.8	٧	
۷Į	Input voltage		5.5		5.5	V	
1	Link lavel autout automat	B port		-24		-32	
ЮН	High-level output current	A port		-12		-12	mA
1	I are lavel autorit armont	A port		12		12	^
lOL	Low-level output current	B port		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.



SCBS260A - JUNE 1993 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT1	62245	SN74LVT162245		UNIT	
PARAMETER		TEST CONDITIONS		MIN	MAX	MIN	MAX	UNII
VIK	V _{CC} = 2.7 V,	l = -18 mA			-1.2		-1.2	٧
	V _{CC} = 3 V,	I _{OH} = - 12 mA	A port	2		2		
	V _{CC} = MIN to MAX [†] ,	l _{OH} = -100 μA		V _{CC} -0.2		V _{CC} -0.2		
Vон	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4		2.4		V
	V _{CC} = 3 V	IOH = - 24 mA		2				
	VCC = 3 V	I _{OH} = -32 mA				2		
		I _{OL} = 12 mA	A port		0.8		0.8	
	V _{CC} = 2.7 V	l _{OL} = 100 μA			0.2		0.2	
		I _{OL} = 24 mA			0.5		0.5	
VOL		I _{OL} = 16 mA	B port		0.4		0.4	V
	V _{CC} = 3 V	I _{OL} = 32 mA] b port		0.5		0.5	
	ACC = 2 A	I _{OL} = 48 mA			0.55			
		I _{OL} = 64 mA					0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1		±1	
	$V_{CC} = 0$ or MAX^{\dagger} ,	V _I = 5.5 V	Control pins		10		10	μА
11		V _I = 5.5 V			20		20	
	V _{CC} = 3.6 V	VI = VCC	A or B ports‡		5		5	
		V _I = 0			-10		-10	
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V #					±100	μА
1	V 2 V	V _I = 0.8 V	A or B ports	75		75		
l(hold)	V _{CC} = 3 V	V _i = 2 V	TA or B ports	-75		-75		μA
lozh	V _{CC} = 3.6 V,	V _O = 3 V			1		1	μA
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μА
			Outputs high		0.1		0.1	
loo		l _O = 0,	Outputs low		5		5	mA
$V_{I} = V_{CC}$ or	V _I = V _{CC} or GND	· V _{CC} or GND			0.1		0.1	ША
ΔlCC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – 0.6 V, r GND			0.2		0.2	mA
Ci	V _I = 3 V or 0							pF
Cio	V _O = 3 V or 0							рF

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] Unused pins at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16373 . . . WD PACKAGE SN74LVT16373 . . . DGG OR DL PACKAGE (TOP VIEW)

10E [I ₁ └	48 1LE
1Q1 [47 [] 1D1
1Q2 [46] 1D2
GND [4	45 GND
1Q3 [44 🛭 1D3
1Q4 [43 [] 1D4
Vcc [42 [] V _{CC}
1Q5 [41 [] 1D5
1Q6 [40 [] 1D6
GND [39 🛛 GND
1Q7 [38 🛭 1D7
1Q8 [37 🛭 1D8
2Q1 [36 🛭 2D1
2Q2 [35 2D2
GND [34 🛛 GND
2Q3 [33 🛛 2D3
2Q4 [32 2 2D4
V _{CC} [31 2 V _{CC}
2Q5 [30 2D5
2Q6 [29 [] 2D6
GND [I — ·	28 🛛 GND
2Q7 [1	27 [] 2D7
2Q8		26 2D8
20E [24	25 2LE

description

The 'LVT16373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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description (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16373 is characterized for operation from –40°C to 85°C.

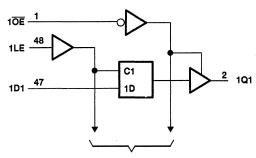
FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Χ	Q ₀
Н	X	Χ	z

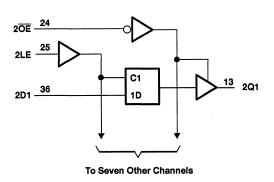
logic symbol†

10E 1EN 48 1LE СЗ 24 2OE 2EN 25 2LE C4 47 2 1Q1 1D1 3D 1 🗸 3 46 1D2 1Q2 44 5 1D3 1Q3 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 1Q7 37 12 1Q8 1D8 36 13 4D 2D1 2 ▽ 2Q1 35 14 2Q2 2D2 33 16 2D3 2Q3 17 2Q4 2D4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 2Q8

logic diagram (positive logic)



To Seven Other Channels



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	
Current into any output in the low state, IO: SN54LVT16373	96 mA
SN74LVT16373	128 mA
Current into any output in the high state, I _O (see Note 2): SN54LVT16373	48 mA
SN74LVT16373	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LV	T16373	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VιΗ	High-level input voltage		2	Ú,	2		٧
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			[©] 5.5		5.5	٧
ЮН	High-level output current		.û	-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Z.	10		10	ns/V
TA	Operating free-air temperature			125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DARAMETER	TEST CONDITIONS			SNS	4LVT16	373	SN7	4LVT16	373	
PARAMETER	'	EST CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	$V_{CC} = MIN \text{ to MAX}^{\ddagger}$,	I _{OH} = -100 μA		V _{CC} -0).2		VCC-C).2		
Vou	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			٧
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						v
	ACC = 2 A	I _{OH} = -32 mA	OH = −32 mA				2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	V(() = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	ACC = 2 A	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA	I _{OL} = 64 mA		, s	Ç.			0.55	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V			Ţ,	10			10	
ь	:	V _I = V _{CC} or GND	Control pins		Q^*	±1			±1	
11	V _{CC} = 3.6 V	VI = VCC	Data pins		S)	1			1	μΑ
		V _I = 0	Data piris	(Ò.	-5			-5	
l _{off}	V _{CC} = 0,	V_I or $V_O = 0$ to 4.5 V		Į.					±100	μA
tra in	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			
^I I(hold)	VCC = 3 V	V _I = 2 V	Data inputs	-75			-75			μΑ
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μA
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μA
			Outputs high			0.09			0.09	
lcc	V _{CC} = 3.6 V,	$l_{O} = 0$,	Outputs low			5			5	mA
.00	V _I = V _{CC} or GND		Outputs disabled			0.09			0.09	110
Δl _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – 0.6 r GND	V,		-	0.2			0.2	mA
Ci	V _I = 3 V or 0				5			5		pF
Co	V _O = 3 V or 0				9.5			9.5		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16373				SN74LVT16373			
		V _{CC} =	: 3.3 V 3 V	Vcc =	2.7 V	V _{CC} =	: 3.3 V .3 V	V _{CC} =	2.7 V	UNIT
		MIN	MAX	/MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	3.3	Ó	ু 3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	0.5	38%	0.5		0.5		0.5		ns
th	Hold time, data after LE↓	1.8	.₫.	2		1.8		2		ns



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54LV	T16373		SN74LVT16373					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q	1.3	5.1	de.	5.8	1.3	2.7	5		5.7	ns
tPHL]	, Q	1.4	5		5.8	1.4	2.9	4.9		5.7	115
t _{PLH}	15	LE Q	2.1	7	JG"	7.5	2.1	3.6	6		6.8	ns
tPHL	LE		3	8.1	₫"	9.4	3	4.7	6.9		8.8	113
^t PZH	ŌĒ	Q	1	5.6	ř	6.4	1	2.9	5.3		6.3	ns
tPZL	OE	OE Q	1.3	5,3		6	1.3	3	5.1		5.9	10
t _{PHZ}	ŌĒ	Q	2.7	7.2		8.2	2.7	4.3	6.8		7.6	ns
tPLZ		3	2.6	6.1		6.2	2.6	4	5.8		5.9	118

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.



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•	Output Ports Have Equivalent 22- Ω Series
	Resistors, So No External Resistors Are
	Required

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments
 Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162373... WD PACKAGE SN74LVT162373... DGG OR DL PACKAGE (TOP VIEW)

	_	_	_	•
10E [1	U	48	1LE
1Q1 [2		47	1D1
1Q2 [3		46	1D2
GND [4		45] GND
1Q3 [5		44] 1D3
1Q4 [6		43] 1D4
v _{cc} [7		42] V _{CC}
1Q5 [8		41] 1D5
1Q6 [9		40] 1D6
GND [10		39] GND
1Q7 [11		38] 1D7
1Q8 [12		37] 1D8
2Q1 [13		36	2D1
2Q2 [14		35	2D2
GND [15		34	GND
2Q3 [16		33	2D3
2Q4 🛚	17		32	2D4
v _{cc} [18		31	V _{CC}
2Q5 [19		30	2D5
2Q6	20		29	2D6
GND]			28	GND
2Q7			27	2D7
2Q8 🛚			26	2D8
20E	24		25	2LE

description

The 'LVT162373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

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description (continued)

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162373 is characterized for operation from –40°C to 85°C.

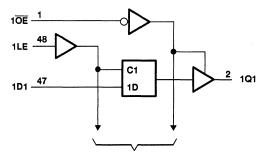
FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	z

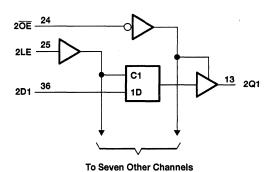
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logic	symbol†				
1ŌE	1	1EN			
1LE	48	СЗ			
2OE	24	2EN			
2LE	25	C4			
454	47			2	
1D1	46	3D	1 ▽	3	1Q1
1D2	44			5	1Q2
1D3	43			6	1Q3
1D4	41			8	1Q4
1D5	40			9	1Q5
1D6	38	1		11	1Q6
1D7	37			12	1Q7
1D8	36			13	1Q8
2D1	35	4D	2 ▽	14	2Q1
2D2		-			2Q2
2D3	33			16	2Q3
2D4	32	-		17	2Q4
2D5	30			19	2Q5
2D6	29			20	2Q6
2D7	27			22	2Q7
2D8	26			23	2Q8

logic diagram (positive logic)



To Seven Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io
Current into any output in the high state, I_O (see Note 2)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package 0.85 W
DL package
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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recommended operating conditions (see Note 4)

		,	SN54LV	T162373	SN74LV	UNIT	
	v		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage				2		V
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-12		-12	mA
lol	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TECT COMPLETIONS		SN54LV1	T162373	SN74LV	162373	LINUT
PARAMETER		TEST CONDITIONS		MIN	MAX	MIN	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA			-1.2		-1.2	٧
Voн	V _{CC} = 3 V,	I _{OH} = - 12 mA		2	,	2		٧
V _{OL}	V _{CC} = 3 V,	I _{OL} = 12 mA			0.8		0.8	٧
	$V_{CC} = 0$ or MAX^{\dagger} ,	V _I = 5.5 V			10		10	
1.		VI = VCC or GND	Control pins		±1		±1	
lj	V _{CC} = 3.6 V	VI = VCC	Data sina		1		1	μΑ
		V _I = 0	Data pins		-5		-5	
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V					±100	μА
l	V 2V	V _I = 0.8 V	A inputs	75		75		
l(hold)	VCC = 3 V	V _I = 2 V	A inputs	-75		-75		μΑ
lozh	V _{CC} = 3.6 V,	V _O = 3 V	1		1		1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μА
			Outputs high		0.19		0.1	
loo	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low		5		5	mA
ICC	V _I = V _{CC} or GND		Outputs disabled		0.19		0.1	III/A
∆lCC [‡]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} of				0.2		0.2	mA
. C _i	V _I = 3 V or 0							pF
Co	V _O = 3 V or 0							pF

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power	SN54LVT16374 WD PACKAGE SN74LVT16374 DGG OR DL PACKAGE (TOP VIEW)
Dissipation	_,,
Members of the Texas Instruments	1 <u>0E</u>
<i>Widebus</i> ™ Family	1Q1 2 47 1D1
Supports Mixed-Mode Signal Operation	1Q2 3 46 1D2
(5-V Input and Output Voltages With	GND 4 45 GND
3.3-V V _{CC})	1Q3 05 44 0 1D3
Supports Unregulated Battery Operation	1Q4 []6 43 [] 1D4
Down to 2.7 V	V _{CC}
2 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	1Q6 0 40 1D6
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	GND 10 39 GND
- A	1Q7 0 11 38 0 1D7
ESD Protection Exceeds 2000 V Per STD 9930 Method 2015 Freeder	1Q8 0 12 37 0 1D8
MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model	2Q1 0 13 36 0 2D1
(C = 200 pF, R = 0)	2Q2 14 35 2D2
	GND 15 34 GND
Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17	2Q3 16 33 2D3
	2Q4 🛘 17 32 🗓 2D4
Bus-Hold Data Inputs Eliminate the Need September 1 September 1 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2 September 2	V _{CC}
for External Pullup Resistors	2Q5 🛛 19 30 🗓 2D5
Supports Live Insertion	2Q6 🛛 20 29 🕽 2D6
 Distributed V_{CC} and GND Pin Configuration 	GND
Minimizes High-Speed Switching Noise	2Q7 🛛 22 27 🖸 2D7
Flow-Through Architecture Optimizes	2Q8 🛮 23 26 🗓 2D8
PCB Layout	2 0E 🛛 24 25 🖟 2CLK
Packaged in Plastic 300-mil Shrink	<u> </u>
Small-Outline (DL) and Thin Shrink	
Small-Outline (DGG) Packages and 380-mil	

description

The 'LVT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings



SCBS145B - MAY 1992 - REVISED FEBRUARY 1994

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each flip-flop)

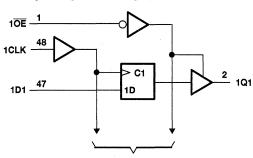
			• •
	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	↑	Ĺ	L
L	H or L	Χ	Q ₀
Н	Χ	Χ	z

logic symbol†

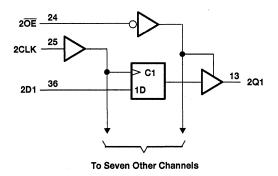
10E 1EN 48 1CLK C1 24 20E 2EN 25 2CLK C2 47 2 1D 1 🗸 1Q1 1D1 46 3 1Q2 1D2 5 44 1Q3 1D3 43 6 1Q4 1D4 41 8 1D5 1Q5 40 9 1D6 1Q6 11 38 1Q7 1D7 37 12 1D8 1Q8 36 13 2 ▽ 2D1 2D 2Q1 35 14 2Q2 2D2 33 16 2D3 2Q3 32 17 2D4 2Q4 19 30 2Q5 2D5 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 2Q8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16374
SN74LVT16374
Current into any output in the high state, I _O (see Note 2): SN54LVT16374
SN74LVT16374
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$) — 50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package 0.85 W
DL package
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

			SN54LV	T16374	SN74LVT16374		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	ŢŢ.	2		V
VIL	Low-level input voltage			Ø .8		0.8	V
VI	Input voltage		·	5.5		5.5	٧
ЮН	High-level output current		Ų.	-24		-32	mA
loL .	Low-level output current		1 8	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SCBS145B - MAY 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SNS	54LVT16	374	SN7	4LVT16	374	UNIT	
PARAMETER	·	EST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNII	
VIK	V _{CC} = 2.7 V,	l _l = −18 mA				-1.2			-1.2	V	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger}$,	l _{OH} = -100 μA		VCC-C).2		VCC-C).2			
Vou	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			v	
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						, ,	
	∧CC = 2 ∧	IOH = -32 mA					2			ľ	
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
Voi		I _{OL} = 16 mA				0.4			0.4	v	
VOL	V _{CC} = 3 V					0.5			0.5	v	
	VCC = 3 V	I _{OL} = 48 mA				0.55					
		i _{OL} = 64 mA			a a	Ø			0.55		
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V				10			10		
l.	V _{CC} = 3.6 V	VI = VCC or GND	Control pins		_⟨⟨⟨`	±1			±1	μΑ	
ч		$V_{CC} = 3.6 \text{ V}$ $V_I = V_{CC}$ Data pins		Data nina		S	1			1	μΑ
		V _I = 0	Data piris	ć	Ş	-5			-5		
l _{off}	V _{CC} = 0,	V_{I} or $V_{O} = 0$ to 4.5 V		Į.	*				±100	μA	
tia is	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА	
[[] I(hold)	ACC = 2 A	V _I = 2 V	Data inputs	-75			-75			μΑ	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μА	
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μA	
			Outputs high			0.1			0.1		
loo	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low			5			5	mA	
lcc	$V_I = V_{CC}$ or GND		Outputs disabled			0.1			0.1	mA	
Δl _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	CC = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2			0.2	mA	
Ci	V _I = 3 V or 0				5			5		pF	
Со	V _O = 3 V or 0				9.5			9.5		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16374								
			V _{CC} = 3.3 V ± 0.3 V				V _{CC} = 3.3 ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	[≪] 0	150	0	150	0	150	MHz
t _W	Pulse duration, CLK high or low		3.3	3	3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	High or low	2.2	_∂′	2.6		2.2		2.6		ns
th	Hold time, data after CLK↑	High or low	0.6	Q"	0		0.6		0		ns

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

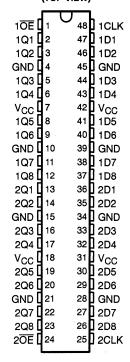
				SN54LV	T16374			SN7	4LVT16	374		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		Vcc =	2.7 V	V	CC = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
f _{max}			150		150		150			150		MHz
t _{PLH}	CLK	Q	1.9	6.6	,\$"	7.4	1.9	3.6	6.3		7	ns
t _{PHL}	OLK	y	2.3	6.9	25	7.5	2.3	4.1	6.6		7.2	10
^t PZH	ŌĒ	Q	1	5.6	~	6.4	1	2.7	5.3		6.3	
tPZL	OE.	4	1.3	5,3		6	1.3	2.8	5.1		5.9	ns
t _{PHZ}	ŌĒ	Q	2.7	7.2		8.2	2.7	4.3	6.8		7.6	200
tPLZ		<u> </u>	2.6	₹6.1		8.2	2.6	3.9	5.8		5.9	ns

 \uparrow All typical values are at V_{CC} = 3.3 V, T_A = 25°C. NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SCBS262A - JULY 1993 - REVISED FEBRUARY 1994

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments
 Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162374...WD PACKAGE SN74LVT162374...DGG OR DL PACKAGE (TOP VIEW)



description

The 'LVT162374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT162374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.



SCBS262A - JULY 1993 - REVISED FEBRUARY 1994

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include $22-\Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to \vec{V}_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162374 is characterized for operation from –40°C to 85°C.

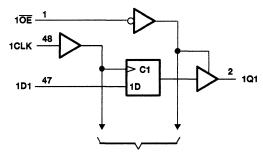
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	X	Q ₀
Н	X	Х	Z

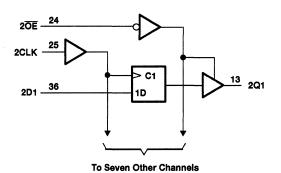
SCBS262A - JULY 1993 - REVISED FEBRUARY 1994

logic	symbol†			
10E 1CLK 20E 2CLK	1 48 24 25 47 46	1EN > C1 2EN > C2 1D 1 ▽	2 3	1Q1
1D2 1D3	44		5	1Q2 1Q3
1D4 1D5	41		8	1Q4 1Q5
1D6 1D7	38 37		11	1Q6 1Q7
1D8 2D1 2D2	36 35	2D 2 ▽	13 14	1Q8 2Q1 2Q2
2D2 2D3 2D4	33 32		16 17	2Q3 2Q4
2D5 2D6	30 29		19 20	2Q5 2Q6
2D7 2D8	26		22	2Q7 2Q8

logic diagram (positive logic)



To Seven Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, IO
Current into any output in the high state, IO (see Note 2)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package 0.85 W
DL package
Storage temperature range ——65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and VO > VCC.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS262A - JULY 1993 - REVISED FEBRUARY 1994

recommended operating conditions (see Note 4)

		•	SN54LV	LVT162374 SN74LVT162374			UNIT
İ			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
ViH	High-level input voltage				2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current ,			-12		-12	mA
lOL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS				Г162374	SN74LV	UNIT	
PARAMETER		MIN	MAX	MIN	MAX	UNII		
VIK	V _{CC} = 2.7 V,	l _l = -18 mA			-1.2		-1.2	V
Voн	V _{CC} = 3 V,	I _{OH} = - 12 mA		2		2		٧
VOL	V _{CC} = 3 V,	I _{OL} = 12 mA			0.8		0.8	V
	V _{CC} = 0 or MAX [†] ,	V _I = 5.5 V			10		10	
t.	V _I = V _{CC} or GND Control pins	Control pins		±1		±1		
IJ	V _{CC} = 3.6 V	V _I = V _{CC}	Data nina		1		1	μΑ
		V ₁ = 0	Data pins		-5		-5	
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V				±100	μΑ	
	V _{CC} = 3 V	V _I = 0.8 V	A immusta	75		75		
l(hold)		V _I = 2 V	A inputs	-75		-75		μA
lozh	V _{CC} = 3.6 V,	V _O = 3 V			1		. 1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μА
			Outputs high		0.19		0.1	
laa	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low	5		5		mA
lcc	V _I = V _{CC} or GND		Outputs disabled	1 () 7			0.1	IIIA
ΔICC [‡]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC}				0.2		0.2	mA
Ci	V _I = 3 V or 0				,			pF
Co	V _O = 3 V or 0							pF

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS146A - MAY 1992 - REVISED MARCH 1994

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16500 WD PACKAGE
SN74LVT16500 DGG OR DL PACKAGE
(TOP VIEW)

	_	U		L
OEAB		_		GND
LEAB	2		55	CLKAB
A1			54] B1
GND			53] GND
A2 [5] B2
A3 [] B3
V _{CC} [7		50] v _{cc}
A4 [] B4
A5 [] B5
A6 [47] B6
GND [GND
A7 [] B7
A8 [] B8
A9 [] B9
A10	15] B10
A11 [] B11
A12			40	B12
GND [] GND
A13[B13 ·
A14[20] B14
A15[] B15
V _{CC} [22] v _{cc}
A16[23		34] B16
A17[24		33] B17
GND [32] GND
A18[31	B18
OEBA [30	CLKBA
LEBA [28		29] GND

description

The 'LVT16500 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

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SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS146A - MAY 1992 - REVISED MARCH 1994

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16500 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLET

	OUTPUT			
OEAB	LEAB	CLKAB	Α	В
L	X	Х	Х	Z
н	Н	X	L	L
н	Н	X	Н	н
н	L	\downarrow	L	L
н	L	\downarrow	Н	н
Н	L	Н	Χ	В ₀ ‡ В ₀ §
н	L	L	Х	B ₀ §

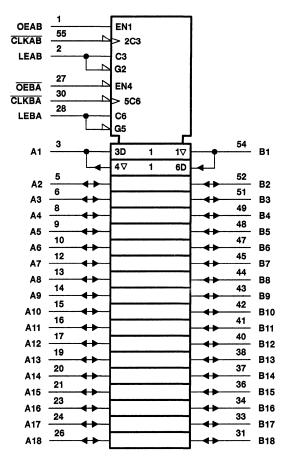
[†]A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

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logic symbol†

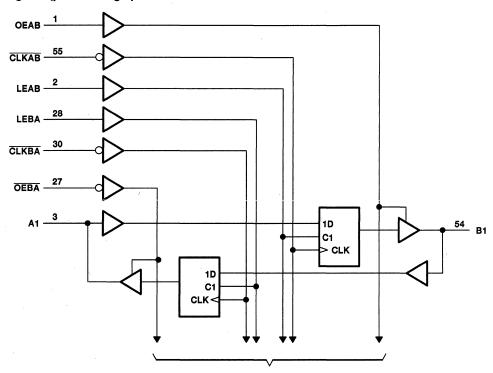


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	
Current into any output in the low state, IO: SN54LVT16500	96 mA
SN74LVT16500	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16500	48 mA
SN74LVT16500	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range –6	35°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and VO > VCC.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.



SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS146A - MAY 1992 - REVISED MARCH 1994

recommended operating conditions (see Note 4)

							UNIT
			MIN	MAX	MIN	MAX	UNII
VCC ·	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	2	Q.	2		٧	
VIL	Low-level input voltage		Æ0.8		0.8	٧	
VI	Input voltage	, a	্বী 5.5		5.5	٧	
ЮН	High-level output current		Ş	-24		-32	mA
IOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	85	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN5	4LVT16	500	SN	UNIT			
PARAMETER		EST CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	UNII	
VιK	$V_{CC} = 2.7 \text{ V},$	l _l = −18 mA				-1.2			-1.2	٧	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger}, I_{OH} = -100 \mu A$).2		Vcc-0	.2			
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = - 8 mA		2.4			2.4			V	
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						٧	
	VCC = 3 V	I _{OH} = -32 mA					2				
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
Voi		I _{OL} = 16 mA				0.4			0.4	V	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	٧	
	ACC = 2 A	I _{OL} = 48 mA			0.55						
		I _{OL} = 64 mA			A.			0.55			
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Cantral pina		18	* ±1			±1		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins		S.F.	10			10		
11	V _{CC} = 3.6 V	V _I = 5.5 V			8	20			20	μΑ	
		V _I = V _{CC}	A or B ports§	4	3	5			5		
		V _I = 0		Ş	>	-10			-10		
l _{off}	V _{CC} = 0,	V_I or $V_O = 0$ to 4.5 V		~					±1.00	μА	
ha - i s	V _{CC} = 3 V	V _I = 0.8 V	I = 0.8 V A or B ports				75			μА	
l(hold)	VCC = 3 V	V _I = 2 V	A of B ports	-75			-75			μΛ	
^I OZH	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μА	
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μА	
			Outputs high			0.12			0.12		
Icc	V _{CC} = 3.6 V,	IO = 0,	Outputs low			5			5	mA	
icc	V _I = V _{CC} or GND	Outputs disabled			0.12			0.12	111/4		
∆ICC [¶]	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA	
Ci	V ₁ = 3 V or 0				3.5			3.5		pF	
C _{io}	V _O = 3 V or 0				12			12		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16500				SN74LVT16500				
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	125	0	150	0	125	MHz
t _W F	Pulse duration	LE high	3.3		3.3		3.3		3.3		
	ruise duration	CLK high or low	3.3		3,3		3.3		3.3		ns
		A before CLKAB↓	1.8		\$1.1		1.8		1.1		
	0-1	B before CLKBA↓	1.9		1.2		1.9		1.2		
t _{su} Setup t	Setup time	A or B before LE↓, CLK high	2.2	S	1.3		2.2		1.3		ns
		A or B before LE↓, CLK low	2.7	S	1.9		2.7		1.9		
th Hold time	Liold times	A or B after CLK↓	1.2	Q.	1.2		1.2		1.2		
	moia time	A or B after LE↓	0.9		1.1		0.9		1.1		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

			SN54LVT16500										
PARAMETER	FROM (INPUT)	1	1 00		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
fmax			150		125		150			125		MHz	
tPLH	B or A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns	
tPHL		B or A	AUID	1.6	6		7.8	1.6	3.2	5.9		7.7	TIS
^t PLH	LEBA or LEAB	1 CDA 1 CAD	A or B	2.3	7.3		8.9	2.3	4	7		8.5	ns
^t PHL		A OI B	2.7	8.2	V,	9.8	2.7	4.3	7.9		9.7	115	
^t PLH	CLKBA or	A or B	2	7.4		8.8	2	4.1	7		8.3	ns	
^t PHL	CLKAB	AOIB	2.4	83		10	2.4	4.4	7.9		9.9	IIS	
t _{PZH}	OEBA or OEAB	A or B	1.2	5.2		6.1	1.2	3	5		5.9	ns	
^t PZL		ζ 5	1.5	[≪] 5.9		7	1.5	3	5.8		6.9	118	
t _{PHZ}	OEBA or	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	ns	
^t PLZ	OEAB	A OI B	2.8	7.3		7.7	2.8	4.7	6.7		7.2	115	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc)
- Supports Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16501 ... WD PACKAGE SN74LVT16501 ... DGG OR DL PACKAGE (TOP VIEW)

			1
OEAB	d ₁	O 56	GND
LEAB	[2	55	CLKAB
A1	[]3	54] B1
GND	[]4	53] GND
A2	[5	52] B2
A3	[]6	51] B3
V_{CC}	[]7	50	₫ v _{cc}
A4	18	49] в4] в5
A5] 9	48] B5
A6	10	47] B6
GND] 11	46	GND
	12		[] B7
	13	44] B8
	1 4	43] B9
A10	15	42	B 10
	1 16	41	D B11
A12		40	B12
GND		39	GND
A13		38	B13
A14		37	B14
	21	36	B15
	22	35	[v _{cc}
A16		34	B16
	1 24	33	B17
GND	25	32] GND
A18	26	31	B18
] 27		CLKBA
LEBA	[]28	29] GND

description

The 'LVT16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16501 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16501 is characterized for operation from –40°C to 85°C.

FUNCTION TABLET

	INP		OUTPUT	
OEAB	LEAB	CLKAB	Α	В
L	Х	X	Х	Z
Н	Н	Χ	L	L
Н	Н	X	Н	Н
Н	L	↑	L	L
н	L	\uparrow	Н	Н
н	L	Н	Χ	в ₀ ‡ в ₀ §
Н	L	L	Х	В ₀ §

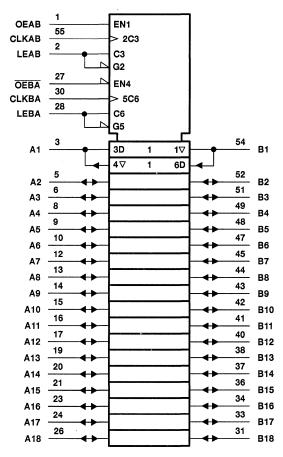
[†]A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.

Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

[§] Output level before the indicated steady-state input conditions were established.

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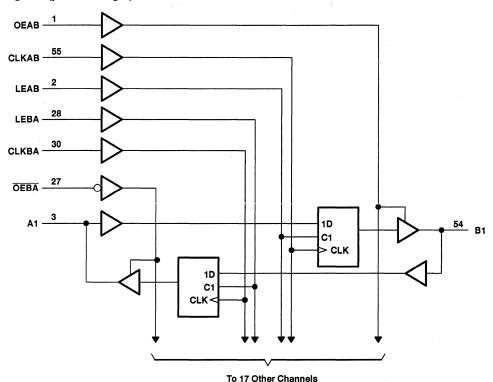
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS147A - MAY 1992 - REVISED FEBRUARY 1994

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16501
SN74LVT16501
Current into any output in the high state, I _O (see Note 2): SN54LVT16501
SN74LVT16501 64 mA
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, $ _{OK}$ ($V_O < 0$) — 50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS147A - MAY 1992 - REVISED FEBRUARY 1994

recommended operating conditions (see Note 4)

			SN54LV	T16501	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	L.J.	2		V
VIL	Low-level input voltage			Ø 0.8		0.8	V
Vi	Input voltage		, s	5.5		5.5	V
ЮН	High-level output current		Ş	-24		-32	mA
lOL	Low-level output current		\display \(\tilde{\infty} \)	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ပဲ

NOTE 4: Unused or floating control inputs must be held high or low.

SCBS147A - MAY 1992 - REVISED FEBRUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SNS	54LVT16	501	SN7	4LVT16	501	UNIT	
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII	
VIK	$V_{CC} = 2.7 \text{ V},$	l = −18 mA				-1.2			-1.2	٧	
	V_{CC} = MIN to MAX ‡ ,	l _{OH} = -100 μA		VCC-C).2		VCC-C	.2			
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			V	
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						, v	
		I _{OH} = -32 mA					2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2	-		0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
Voi		I _{OL} = 16 mA				0.4		-	0.4	٧	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	٧	
	VCC = 3 V	I _{OL} = 48 mA				0.55					
		i _{OL} = 64 mA			ŝ	Ÿ			0.55		
	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control pins		19	±1			±1		
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V	Control pins		ζζ"	10			10		
ΙĮ	V _{CC} = 3.6 V	V _I = 5.5 V			20			20		μА	
		VI = VCC	A or B ports§	1 -5		1	1		1		
		V ₁ = 0	<u> </u>			-5					
loff	V _{CC} = 0,	V_1 or $V_0 = 0$ to 4.5 V							±100	μΑ	
1175-2125	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА	
l(hold)	•66-04	V _I = 2 V	TA OF B PORTS	– 75			-75			μι	
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ	
			Outputs high			0.12			0.12		
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low			5			5	mA	
,00	V _I = V _{CC} or GND		Outputs disabled			0.12			0.12	111/5	
∆ICC [¶]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – 0.6 r GND	V,			0.2			0.2	mA	
Ci	V _I = 3 V or 0				3.5			3.5		pF	
C _{io}	V _O = 3 V or 0				12			12		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54LV	/T16501		SN74LVT16501				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	150	0	125	0	150	0	125	MHz	
t _w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns	
	ruise duration	CLK high or low	3.3		3,3		3.3		3.3			
		A before CLKAB↑	1.6		2.1		1.6		2.1			
	O at un tima	B before CLKBA↑	1.6		2.1		1.6		2.1			
tsu	Setup time	A or B before LE↓, CLK high	2.6	S	1.9		2.6		1.9		ns	
		A or B before LE↓, CLK low	2	్టర్	. 1.3		2		1.3			
٠.	Hold time	A or B after CLK↑	2	Q.	2.1		2		2.1		ns	
th	Hold liftle	A or B after LE↓	0.9		1.2		0.9		1.2			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

					T16501			SN74LV	T16501		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		125		150		125		MHz
tPLH	D A	A or B	1.7	5.4		5.8	1.7	5.4		6.8	ns
t _{PHL}	B or A	AOFB	1.6	6	i i i	7.8	1.6	5.9		7.7	ns
tPLH	LEBA or LEAB	A or B	2.3	6.6	Ž.	7.6	2.3	7		8.5	ns
t _{PHL}		AUD	2.7	8.2	82	9.8	2.7	7.9		9.7	
tPLH	CLKBA or	A or B	2.5	6.9	1	7.9	2.5	7.9		9.2	
^t PHL	CLKAB	AOID	3.5	9.4		10.7	3.5	8.9		10.4	ns
^t PZH	OFDA OFAD	A or B	1.2	5 .1		6.1	1.2	5		5.9	
^t PZL	OEBA or OEAB	AUIB	1.5	³⁰ 5.9		7	1.5	5.8		6.9	ns
t _{PHZ}	OEBA or OEAB	A or B	2.7	7.5		8.5	2.7	7.4		8.3	ns
tPLZ	OLDA OF OEAB	AUID	2.8	6.8		7.5	2.8	6.7		7.2	115

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power 			PACKAGE R DL PACKAGE)
Dissipation			L
Members of the Texas Instruments	1OEAB		1 OEBA
Widebus™ Family	1LEAB		1LEBA
•	1CEAB		1CEBA
Supports Mixed-Mode Signal Operation Supports and Output Vallages William	GND [] GND
(5-V Input and Output Voltages With] 1B1
3.3-V V _{CC})	1A2 [] 1B2
Supports Unregulated Battery Operation	v _{cc} [⊉ ∨ _{CC}
Down to 2.7 V	1A3 [] 1B3
 Typical V_{OLP} (Output Ground Bounce) 	1A4 [1B4
< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	1A5 [] 1B5
ESD Protection Exceeds 2000 V Per	GND [3	GND
MIL-STD-883C, Method 3015; Exceeds	1A6 [3] 1B6
200 V Using Machine Model	1A7 [] 1B7
(C = 200 pF, R = 0)	1A8 [3	1B8
Latch-Up Performance Exceeds 500 mA	2A1 [1	2B1
Per JEDEC Standard JESD-17	2A2 [] 2B2
	2A3 [1] 2B3
Bus-Hold Data Inputs Eliminate the Need Feetened Bullium Resistante	GND [] GND
for External Pullup Resistors	2A4 [] 2B4
Supports Live Insertion	2A5 [] 2B5
 Distributed V_{CC} and GND Pin Configuration 	2A6 [3] 2B6
Minimizes High-Speed Switching Noise	v _{cc} [] v _{cc}
Flow-Through Architecture Optimizes	2A7 [23 34	2B7
PCB Layout	2A8 [3] 2B8
Packaged in Plastic 300-mil Shrink	GND [1] GND
Small-Outline (DL) and Thin Shrink	2CEAB		2CEBA
Small-Outline (DGG) Packages and 380-mil	2LEAB		2LEBA
Fine-Pitch Ceramic Flat (WD) Packages	2 OEAB [28 29	2 OEBA

description

The 'LVT16543 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated.

Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings



SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

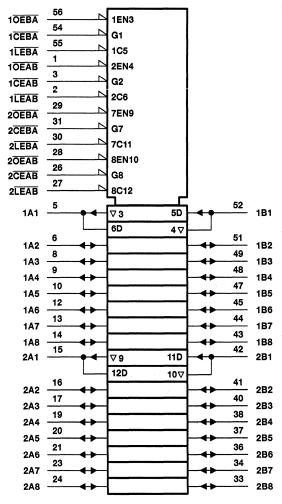
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description (continued)

The SN74LVT16543 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

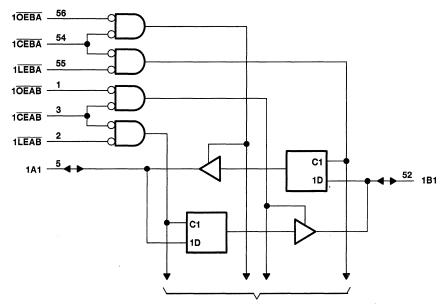
The SN54LVT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16543 is characterized for operation from –40°C to 85°C.

logic symbol†

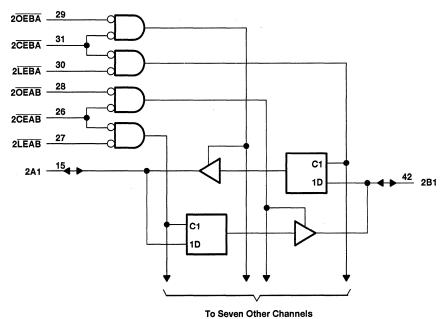


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



TO COVOIT OUT OTTAINION

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FUNCTION TABLET (each 8-bit section)

	INPL		OUTPUT	
CEAB	LEAB	OEAB	Α	В
Н	Х	Х	Х	Z
X	X	Н	Χ	z
L	Н	· L	Χ	в ₀ ‡
L	L	L	L	L
L	L	L	Н	н

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC}	
Input voltage range, V _I (see Note 1)	Supply voltage range, V _{CC} –0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)0.5 V to 7 V Current into any output in the low state, I_O : SN54LVT16543 96 mA SN74LVT16543 128 mA Current into any output in the high state, I_O (see Note 2): SN54LVT16543 48 mA SN74LVT16543 64 mA Input clamp current, I_{IK} ($V_I < 0$)50 mA Output clamp current, I_{OK} ($V_O < 0$)50 mA Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package 1 W DL package 1.4 W	Input voltage range, V ₁ (see Note 1) -0.5 V to 7 V
Current into any output in the low state, I $_{O}$: \$N54LVT16543	
$\begin{array}{c} \text{SN74LVT16543} & 128 \text{ mA} \\ \text{Current into any output in the high state, I}_O \text{ (see Note 2): SN54LVT16543} & 48 \text{ mA} \\ \text{SN74LVT16543} & 64 \text{ mA} \\ \text{Input clamp current, I}_{\text{IK}} \text{ (V}_{\text{I}} < 0) & -50 \text{ mA} \\ \text{Output clamp current, I}_{\text{OK}} \text{ (V}_O < 0) & -50 \text{ mA} \\ \text{Maximum power dissipation at T}_{\text{A}} = 55^{\circ}\text{C (in still air) (see Note 3): DGG package} & 1 \text{ W} \\ \text{DL package} & 1.4 \text{ W} \\ \end{array}$	Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the high state, I_O (see Note 2): SN54LVT16543	Current into any output in the low state, IO: SN54LVT16543
	SN74LVT16543
	Current into any output in the high state, I _O (see Note 2): SN54LVT16543
$\begin{tabular}{ll} Input clamp current, $I_{ K}$ ($V_{ }$ < 0) & -50 mA \\ Output clamp current, I_{OK} ($V_{ O}$ < 0) & -50 mA \\ Maximum power dissipation at $T_{ A}$ = 55°C (in still air) (see Note 3): DGG package & 1 W & DL package & 1.4 W \\ \end{tabular}$	
Output clamp current, I_{OK} ($V_O < 0$)	
DL package 1.4 W	
·	Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
Storage temperature range –65°C to 150°C	DL package
	Storage temperature range ——65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

			SN54LV	T16543	SN74LV	UNIT		
	•		MIN	MAX	MIN	MAX	ONT	
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧	
VIH	High-level input voltage		2	ii.	2		٧	
VIL	Low-level input voltage			0.8		0.8	٧	
٧ı	Input voltage		Á	[©] 5.5		5.5	V	
IOH	High-level output current		Û.	° –24		-32	mA	
lOL	Low-level output current		_33'	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	T &	10		10	ns/V	
TA	Operating free-air temperature		~55	125	-40	85	°C	

NOTE 4: Unused or floating control inputs must be held high or low.

[‡] Output level before the indicated steady-state input conditions were established.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	1	TOT CONDITIONS		SNS	4LVT16	543	SN7	74LVT16	543	
PARAMETER	'	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	0.2 0.5 0.4 0.5 0.55 ±1 10 20 5 -10 ±100	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	l _{OH} = -100 μA		VCC-C).2		VCC-C).2		
Vari	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			V
∨он	V00 - 3 V	I _{OH} = -24 mA		2						V
	VCC = 3 V	I _{OH} = -32 mA					2		0.2 0.5 0.4 0.5 0.55 ±1 10 20 5 -10 ±100	
	V00 - 27V	l _{OL} = 100 μA				0.2			0.2	
	vCC = 2.7 v	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V _{CC} = 2.7 V, I _I = -18 mA	I _{OL} = 32 mA				0.5			0.5	V
		I _{OL} = 64 mA				A Company			0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control pine		78	±1			±1	
	V _{CC} = 0 or MAX [‡] ,	V _j = 5.5 V	Control pins		8.	10			10	
ΙΙ	V _{CC} = 3.6 V	V _I = 5.5 V			6	20			20	μА
		VI = VCC	A or B ports§	5		5				
		V _I = 0		Q.	>	-10			-10	
l _{off}	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5$	V	- «					±100	μΑ
lea en	Vac 2.V	V _I = 0.8 V	A or B porto	75			75			μА
li(hold)	VCC = 3 V	V _j = 2 V	A Of B ports	-75			-75			μ-
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ
	V 00V		Outputs high			0.12			0.12	
lcc		IO = 0,	Outputs low			5			5	mΑ
	11-100 or arra		Outputs disabled			0.12			0.12	
ΔICC¶			- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				13			13		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

 $[\]P$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

					SN54LV	T16543			SN74LV	T16543		
				V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration	on, LEAB or LEBA low		3.3		3.3		3.3		3.3		ns
		Data before LEAB↑ or LEBA↑	High	0.8		0.5		0.8		0.5	-	200
١.	Catum times	Data before LEAD For LEBAT	Low	1.5		1.9		1.5		V _{CC} = 2.7 V (MIN MAX 3.3 0.5 1.9 0.4 1.9 0 1.3 0	ns	
tsu	Setup time	Data before CEAB↑ or CEBA↑	High	0.7		€0.4		0.7		0.4		no
		Data before CEABT of CEBAT	Low	1.6		<u>^</u> 1.9		1.6		1.9		ns
		Data after LEAB↑ or LEBA↑	High	0.8	À	0		0.8		0		
 	Hold time	Data after LEABT OF LEBAT	Low	1.2	70,	1.3		1.2		1.3		ns
th	Hold time	Data after CEAB↑ or CEBA↑	High	0.8	Q"	0		0.8		0		no
		Data after CLAB FOR CEBA F	Low	1.3		1.4		1.3		1.4		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Note 5)

				SN54LV	T16543	7		SN7	4LVT16	543		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	A or B	B or A	1.4	4.5		5	1.4	2.7	4.6		5.5	ns
t _{PHL}	AOIB	BUIA	1.3	4.5		5.3	1.3	2.9	4.6	,	5.8	115
tPLH	ĪĒ	A or B	1.3	6.8	À	8.5	1.7	3.7	6.3	•	8.1	ns
tPHL	LE .	AUIB	1.5	6.5	25	8.3	1.9	3.7	6		7.8	115
tPZH	ŌĒ	A or D	1.4	5.7	\$5	7.3	1.5	3.3	5.8		7.6	ns
tPZL	OE .	A or B	1.6	5,6		7.4	1.6	3.3	6.2		8.2	115
tPHZ	ŌĒ	A or B	2	6,1		6.6	2	4.1	6.5		7.1	ns
tPLZ	OE	AOIB	2.7	5.2		5.4	2.7	3.9	5.8		5.9	115
t _{PZH}	CE	A or B	1.4	× 5.5		6.7	1.5	3.3	6		7.6	20
tPZL	CE	A OLD	1.6	5.5		6.7	1.7	3.3	6.4		8.3	ns
t _{PHZ}	CE	A or D	2	6.2		6.6	2	4.1	6.4		7.1	
tPLZ	OE .	A or B	2.6	5.3		5.5	2.6	4	5.4		5.6	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

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SN54LVT16646 . . . WD PACKAGE State-of-the-Art Advanced BiCMOS SN74LVT16646 . . . DGG OR DL PACKAGE Technology (ABT) Design for 3.3-V (TOP VIEW) **Operation and Low-Static Power** Dissipation 1DIR [56 10E **Members of the Texas Instruments** 1CLKAB 12 55 1 1CLKBA Widebus™ Family 1SAB 🛮 3 54**∏** 1SBA Supports Mixed-Mode Signal Operation GND []4 53 GND (5-V Input and Output Voltages With 1A1 🛮 5 52 1B1 3.3-V V_{CC}) 1A2 **[**] 6 51 1B2 Supports Unregulated Battery Operation 50 VCC V_{CC} 47 Down to 2.7 V 1A3 🛮 8 49 1B3 1A4 🛮 9 48**∏** 1B4 Typical V_{OLP} (Output Ground Bounce) 1A5 1 10 47 1B5 < 0.8 V at V_{CC} = 3.3 V, T_{Δ} = 25°C GND 11 46 GND ESD Protection Exceeds 2000 V Per 45 1B6 1A6 🛮 12 MIL-STD-883C, Method 3015; Exceeds 1A7 **[]** 13 44 1 1B7 200 V Using Machine Model 1A8 **∏** 14 43**∏** 1B8 (C = 200 pF, R = 0)2A1 15 42 2B1 Latch-Up Performance Exceeds 500 mA 2A2 16 41 2B2 Per JEDEC Standard JESD-17 2A3 **∏** 17 40 T 2B3 Bus-Hold Data Inputs Eliminate the Need GND [] 18 39 | GND for External Pullup Resistors 2A4 [] 19 38 2B4 Supports Live Insertion 2A5 20 37 T 2B5 2A6 🛮 21 36 **□** 2B6 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise V_{CC} 1 22 35 V_{CC} 2A7 **[**] 23 34 2B7 Flow-Through Architecture Optimizes 2A8 🛮 24 33 2B8 PCB Layout GND 1 25 32 | GND Packaged in Plastic 300-mil Shrink 2SAB 1 26 31 1 2SBA Small-Outline (DL) and Thin Shrink 2CLKAB [27 30 2CLKBA Small-Outline (DGG) Packages and 380-mil 2DIR 1 28 29 20E

description

The 'LVT16646 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode $(\overline{OE} \text{ high})$, A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Widebus is a trademark of Texas Instruments Incorporated.

Fine-Pitch Ceramic Flat (WD) Packages
Using 25-mil Center-to-Center Spacings



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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16646 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

		INP	UTS			DATA	A I/Os	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Χ	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified [†]
Χ	X	Х	1	X	Х	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	↑	1	Х	Х	Input	Input	Store A and B data
Н	X	H or L	H or L	X	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	Ĺ	Χ	H or L	X	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	X	Н	Х	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS149A - MAY 1992 - REVISED MARCH 1994

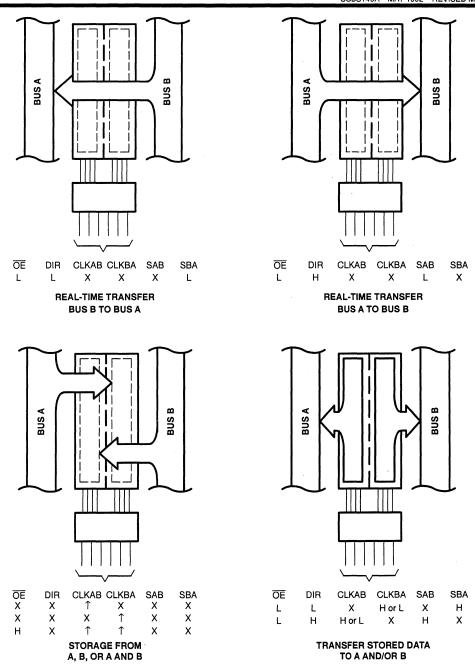
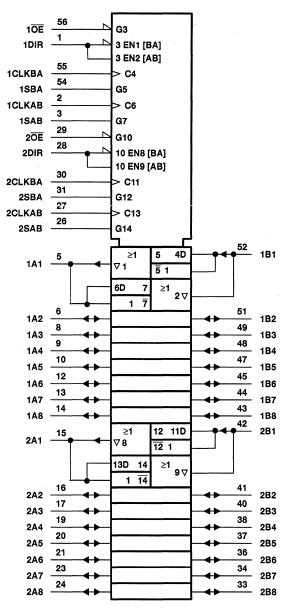


Figure 1. Bus-Management Functions



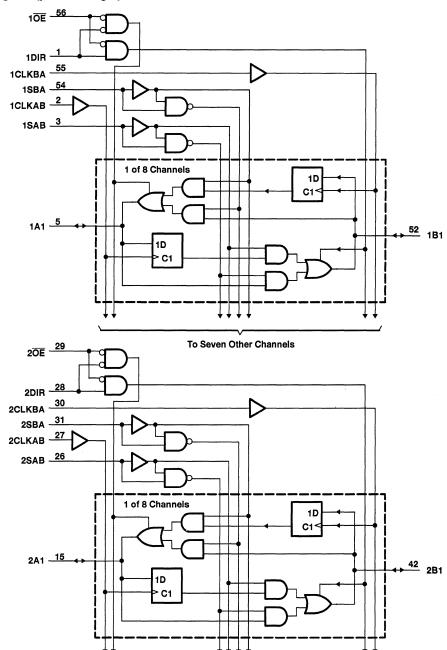
SCBS149A - MAY 1992 - REVISED MARCH 1994

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





To Seven Other Channels

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16646	96 mA
SN74LVT16646	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16646	
SN74LVT16646	
Input clamp current, $I_{IK}(V_I < 0)$	
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

recommended operating conditions (see Note 4)

			SN54LV	T16646	SN74LV	T16646	UNIT
	X		MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	i di	2		٧
VIL	Low-level input voltage			0.8		0.8	V
VI	input voltage		,	[©] 5.5		5.5	V
ЮН	High-level output current		ن.	-24		-32	mA
lOL	Low-level output current		Į Š	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature			125	-40	85	•C

NOTE 4: Unused or floating control inputs must be held high or low.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	-	TOT CONDITIONS		SN	54LVT16	546	SN7	4LVT16	646	115117
PARAMETER	· '	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
V _{IK}	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA	·			-1.2			-1.2	V
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	I _{OH} = -100 μA		VCC-0).2		VCC-0	.2		
Va.,	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	IOH ≈ - 24 mA		2						V
	VCC = 2 V	I _{OH} = -32 mA					2			
	V 07V	I _{OL} = 100 μA				0.2			0.2	
	V _{CC} = 2.7 V	IOL = 24 mA				0.5			0.5	
V		I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	ACC = 2 A	I _{OL} = 48 mA				0.55				
		IOL = 64 mA				77			0.55	
:	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control pins		7.5	±1			±1	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V	Control pins		8	10			10	
ł į		V _I = 5.5 V			A.,	20			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§	Ž	ें	5			5	
		V _I = 0		1	>	-10			-10	
l _{off}	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5	V	*					±100	μА
ha in	Vac. 3.V	V _I = 0.8 V	A or B ports	75			75			
l(hold)	VCC = 3 V	V _I = 2 V	A or B ports	-75			-75			μΑ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3. V				1			1	μΑ
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ
	.,		Outputs high			0.12			0.12	
ICC	V _{CC} = 3.6 V, V _I = V _{CC} or GND	l _O = 0,	Outputs low			5			5	mA
	41 = 400 or arra		Outputs disabled			0.12			0.12	
ΔICC [¶]	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o		- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				3.5			3.5		рF
C _{io}	V _O = 3 V or 0				12			12		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54LV	T16646			SN74LV	T16646		
			V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	,S*0	150	0	150	0	150	MHz
tw	Pulse duration, CLK high or low		3.3		% 3.3		3.3		3.3		ns
ſ	Setup time,	Data high	1.3	- 2	· 1.4		1.3		1.4		ns
t _{su}	A or B before CLKAB↑ or CLKBA↑	Data low	2.4	25	3		2.4		3		115
Ī	Hold time,	Data high	0.5	- 0°	0		0.5		0		ns
^t h	A or B after CLKAB↑ or CLKBA↑	Data low	0.6	₹.	0.5		0.5		0.5		118

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

				SN54LV	T16646			SN7	4LVT16	646		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
f _{max}			150				150					MHz
tPLH	CLKBA or	A or B	1.8	6		6.9	1.8	3.8	5.7		6.7	ns
t _{PHL}	CLKAB	AOIB	2.1	5.9		6.6	2.1	3.9	5.7		6.5	10
tPLH	A or B	B or A	1.3	4.9	2	5.6	1.3	3	4.7		5.4	ns
t _{PHL}	AOID	BOLA	1	4.8	- 37	5.8	1	3.1	4.7		5.6	118
tPLH	ODA CADT	A or B	1.4	6.4	24	7.4	1,4	4	6.2		7.2	ns
t _{PHL}	SBA or SAB‡	AOID	1.4	6.4	N.	7.4	1.4	4.3	6.2		7.2	115
^t PZH	ŌĒ	A or B	1	5.7	,	7.4	1	3	5.4		6.4	ns
t _{PZL}	OE I	AOID	1	6,5		7.5	1	3.1	5.6		6.5	115
tPHZ_	ŌĒ	A or B	2.3	₡6.7		7.1	2.3	4.6	6.5		6.9	ns
^t PLZ	OE .	AUID	2.2	6		6.5	2.2	4.5	5.8		5.9	115
^t PZH	DIR	A or B	1	5.9		7.7	1	3.3	5.7		6.7	20
t _{PZL}	DIK	AULB	1.2	5.9		7.3	1.2	3.5	5.8		6.7	ns
^t PHZ	DIR	A or B	1.7	7.3		8.5	1.7	4.7	7.2		8.3	no
^t PLZ	DIK	AOFB	1.5	7.8		7.4	1.5	4.9	6.6		7.2	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

[‡] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

20EAB [28

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	30831307	A - WAT 1992	- HEVISED FEBRU
State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power	SN54LVT166 SN74LVT16652 . (T		
Dissipation	10EAB [1 OEBA
 Members of the Texas Instruments 	1CLKAB		1 1 CLKBA
<i>Widebus</i> ™ Family	3		
Supports Mixed-Mode Signal Operation	1SAB []		1SBA
• • • • • • • • • • • • • • • • • • • •	GND []	2	GND
(5-V Input and Output Voltages With	1A1 [] t		1B1
3.3-V V _{CC})	1A2 🛚 (1B2
 Supports Unregulated Battery Operation 	v _{cc} []:	7 50] v _{cc}
Down to 2.7 V	1A3 🛛 8		1B3
 Typical V_{OLP} (Output Ground Bounce) 	1A4 🛚 9	9 48	1B4
< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	1A5 🛚		1B5
ESD Protection Exceeds 2000 V Per	GND 🗓	11 46	GND
MIL-STD-883C, Method 3015; Exceeds	1A6 🔲 ·	12 45	1B6
200 V Using Machine Model	1A7 🚺 ·	13 44	1B7
(C = 200 pF, R = 0)	1A8 🚺	14 43] 1B8
Latch-Up Performance Exceeds 500 mA	2A1 🚺	15 42] 2B1
Per JEDEC Standard JESD-17	2A2 [·	16 41	2B2
	2A3 🚺	17 40	2B3
Bus-Hold Data Inputs Eliminate the Need	GND []	18 39	GND
for External Pullup Resistors	2A4 🚺	19 38	2B4
Supports Live Insertion	2A5 🚺	20 37	2B5
 Distributed V_{CC} and GND Pin Configuration 	2A6 🛛 2	21 36	2B6
Minimizes High-Speed Switching Noise	v _{cc} []2	22 35	V _{CC}
Flow-Through Architecture Optimizes	2A7 🛛 2		2B7
PCB Layout	2A8 🛛 2	24 33	2B8
Packaged in Plastic 300-mil Shrink	GND 🛛 2	25 32	GND
Small-Outline (DL) and Thin Shrink	2SAB [2		2SBA
Small-Outline (DGG) Packages and 380-mil	2CLKAB 🛛	27 30	2CLKBA
oman-outline (Daa) Fackages and soo-iiii	20Б4В Д3		2 <u>OEBX</u>

description

The 'LVT16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and \overline{OEBA} . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

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Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings



20EBA

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

		INPU	rs			DATA	A 1/0†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	X	Х	Input	Input	Isolation
L	Н	1	1	X	Х	Input	Input	Store A and B data
Х	Н	1	H or L	X	Х	Input	Unspecified [‡]	Store A, hold B
Н	Н	↑	1	X ‡	Х	Input	Output	Store A in both registers
L	X	H or L	. 1	Х	Х	Unspecified [‡]	Input	Hold A, store B
L	L	↑	1	X	x‡	Output	Input	Store B in both registers
L	L	X	X	Х	L	Output	. Input	Real-time B data to A bus
L	L	Χ	H or L	Х	Н	Output	Input	Stored B data to A bus
Н	Н	Χ	Х	L	Х	Input	Output	Real-time A data to B bus
Н	Н	H or L	Х	Н	Х	Input	Output	Stored A data to B bus
н	L	H or L	H or L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

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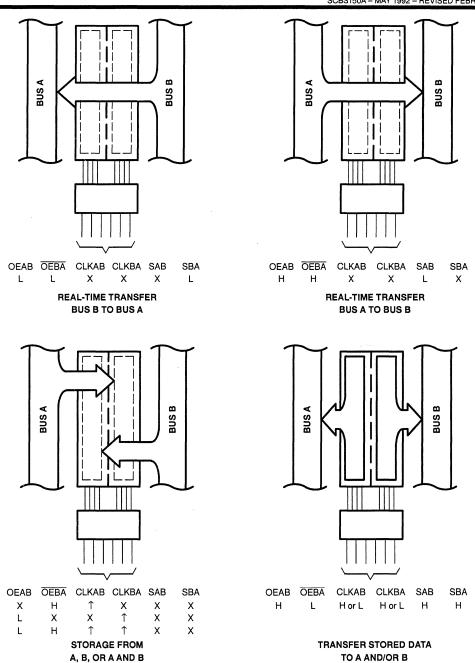
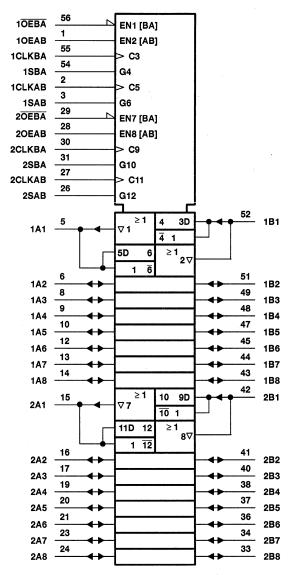


Figure 1. Bus-Management Functions



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logic symbol†

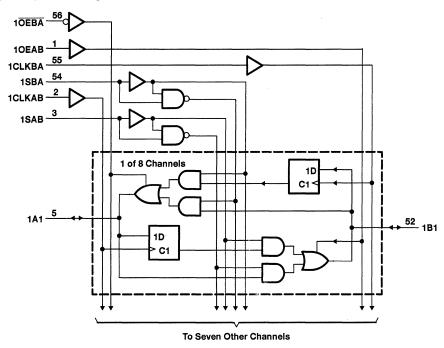


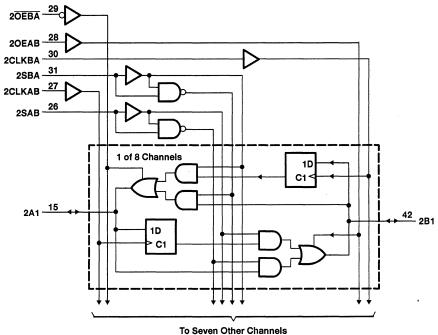
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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logic diagram (positive logic)







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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16652
SN74LVT16652
Current into any output in the high state, I _O (see Note 2): SN54LVT16652
SN74LVT16652 64 mA
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range —65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- This current will only flow when the output is in the high state and VO > VCC.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

	,		SN54LV	T16652	SN74LV	T16652	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
٧ _I	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16652		SN74LVT16652		UNIT
PARAMETER		MIN	MAX	MIN	MAX	UNII		
VIK	V _{CC} = 2.7 V,	í _l = –18 mA		-1.2		-1.2	٧	
	V _{CC} = MIN to MAX†	= MIN to MAX † , IOH = -100μ A			2			
\/-··	V _{CC} = 2.7 V, I _{OH} = -8 mA			2.4		2.4		V
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		. 2				٧
		I _{OH} = -32 mA				2		
	V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2		0.2	
	VCC = 2.7 V	I _{OL} = 24 mA			0.5		0.5	V
V	VCC = 3 V	I _{OL} = 16 mA			0.4		0.4	
v_{OL}		I _{OL} = 32 mA			0.5		0.5	
		I _{OL} = 48 mA			0.55			
		I _{OL} = 64 mA					0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control nine		±1		±1	μА
	$V_{CC} = 0$ or MAX^{\dagger} ,	V _I = 5.5 V	Control pins		10		10	
lj	V _{CC} = 3.6 V	V _I = 5.5 V	A or B ports‡		20		20	
		V _I = V _{CC}			5		5	
		V _I = 0			-10		-10	
l _{off}	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5 V			,	±100	μΑ	
lea en	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75		75		
l(hold)		V _I = 2 V	A or B ports	-75		-75		μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V			1		1	. μΑ
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μΑ
	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Outputs high		0.1		0.1	
lcc		$I_{O}=0,$	Outputs low		5		5	mΑ
	AL = ACC OL CLAD		Outputs disabled		0.1		0.1	
ΔICC§	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			0.2		0.2	mA	
Ci	V _I = 3 V or 0							рF
C _{io}	V _O = 3 V or 0							рF

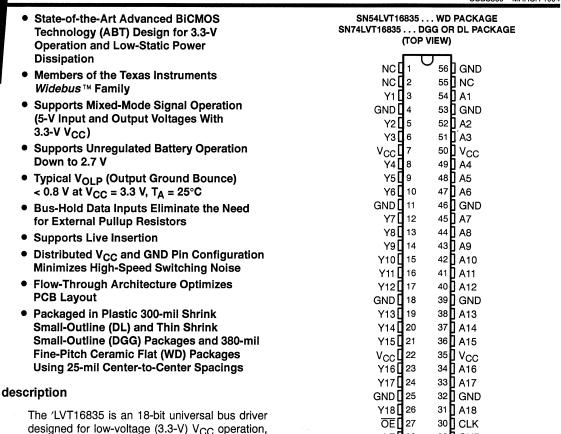
For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] Unused pins at V_{CC} or GND

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of the clock. When \overline{OE} is high, the outputs are in the high-impedance state.

LE [] 28

29 | GND

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16835 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16835 is characterized for operation from -40°C to 85°C.

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but with the capability to provide a TTL interface to

a 5-V system environment.

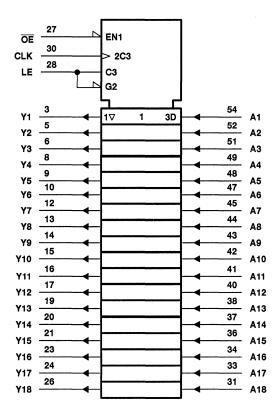


FUNCTION TABLE

	INP		OUTPUT	
OE	LE	CLK	Α	Υ
Н	Х	X	Х	Z
L	Н	X	L	L
L	Н	X	Н	Н
L	L	1	L	L
L	L	1	Н	Н
L	L	Н	Х	Y ₀ † Y ₀ ‡
L	L	L	Х	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low.

logic symbol[†]

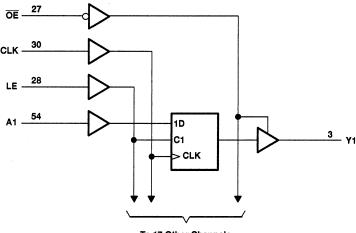


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[‡] Output level before the indicated steady-state input conditions were established.

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logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16835
SN74LVT16835
Current into any output in the high state, I _O (see Note 2): SN54LVT16835 48 mA
SN74LVT16835
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package
DL package
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



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recommended operating conditions (see Note 4)

			SN54LV1	16835	SN74LVT16835		UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	Supply voltage		3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	ů

NOTE 4: Unused or floating control inputs must be held high or low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16835		SN74LVT16835		UNIT	
PARAMETER	TEST CONDITIONS				MAX	MIN	MAX	UNII	
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = –18 mA		-1.2		-1.2	V		
	V _{CC} = MIN to MAX [†] ,	N to MAX [†] , I _{OH} = -100 μA			?	V _{CC} -0.2	2		
\/a	$V_{CC} = 2.7 \text{ V}, \qquad I_{OH} = -8 \text{ mA}$			2.4		2.4		V	
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2				v	
		I _{OH} = -32 mA				2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA			0.2		0.2		
	VCC = 2.7 V	I _{OL} = 24 mA			0.5		0.5	· v	
Voi	V _{CC} = 3 V	I _{OL} = 16 mA			0.4		0.4		
VOL		I _{OL} = 32 mA			0.5		0.5		
		I _{OL} = 48 mA			0.55				
		I _{OL} = 64 mA					0.55		
	$V_{CC} = 0$ or MAX^{\dagger} ,	$C = 0$ or MAX † , $V_{\parallel} = 5.5 \text{ V}$			10		10		
	V _{CC} = 3.6 V	V _I = V _{CC} or GND	Control pins	1	±1		±1		
lį		$V_I = V_{CC}$	A inputs‡		1		1	μА	
		V _I = 5.5 V			20		20		
		V ₁ = 0			-5		-5		
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V				±100	μА		
1	V _{CC} = 3 V	V _I = 0.8 V	A inpute	75		75			
l (hold)		V _I = 2 V	A inputs	-75		-75		μΑ	
lozh	V _{CC} = 3.6 V,	V _O = 3 V			1		1	μA	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μА	
		I _O = 0,	Outputs high		0.1		0.1		
lcc	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Outputs low		5		5	mA	
	AL = ACC OL CIAD		Outputs disabled		0.1		0.1		
ΔI _{CC} §	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} of	One input at V _{CC} – 0.6 V, or GND			0.2		0.2	mA	
Ci	V _I = 3 V or 0							pF	
Co	V _O = 3 V or 0							рF	

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] Unused pins at V_{CC} or GND

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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I v_{cc}

🛮 2B7

31 2 2CLKENBA

30 T 2CLKBA

29 20EBA

33 2B8

32 GND

2A7 🛮 23

2A8 🛮 24

GND 1 25

2CLKENAB 26

2CLKAB 1 27

20EAB 1 28

	CODOTOTI MINITION TRANSPORT	
 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation 	SN54LVT16952 WD PACKAGE SN74LVT16952 DGG OR DL PACKAG (TOP VIEW)	ìΕ
 Members of the Texas Instruments Widebus™ Family 	10EAB	.
 Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V Vcc) 	GND 4 53 GND 1A1 5 52 1B1 1A2 6 51 1B2	١
 Supports Unregulated Battery Operation Down to 2.7 V 	V _{CC} 07 50 V _{CC} 1A3 08 49 1B3	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1A4 0 9 48 0 1B4 1A5 0 10 47 0 1B5	
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, 	GND 11	
R = 0) Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17	2A1	
 Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors 	GND 118 39 GND 2A4 119 38 2B4	
Supports Live Insertion	2A5 [] 20 37 [] 2B5	
 Distributed V_{CC} and GND Pin Configuration 	2A6 🛮 21 36 🗓 2B6	

- **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes **PCB Layout**
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

description

The 'LVT16952 is a 16-bit registered transceiver designed for low-voltage (3.3-V) VCC operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

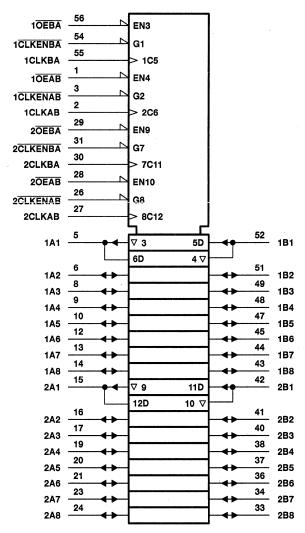
The SN54LVT16952 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16952 is characterized for operation from -40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated



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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

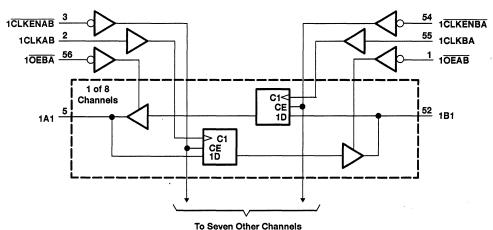
SCBS151A - MAY 1992 - REVISED JANUARY 1994

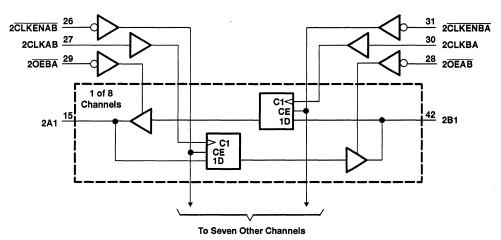
FUNCTION TABLET

	OUTPUT			
CLKENAB	CLKAB	OEAB	Α	В
Н	Х	L	Х	В ₀ ‡ В ₀ ‡
X	L	L	Χ	в ₀ ‡
L	1	L	L	L
L	1	L	Н	Н
X	X	Н	Х	z

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

logic diagram (positive logic)





[‡] Level of B before the indicated steady-state input conditions were established.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4	4.6 V
Input voltage range, V _I (see Note 1)	o 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to	o 7 V
Current into any output in the low state, IO: SN54LVT16952	6 mA
SN74LVT16952	8 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16952	8 mA
SN74LVT16952 64	4 mA
Input clamp current, $I_{ K }(V_1 < 0)$ —50	0 mA
Output clamp current, I _{OK} (V _O < 0)	0 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	. 1 W
DL package	.4 W
Storage temperature range ——65°C to 1	50°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT	16952	SN74LV	Г16952	UNIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	IH High-level input voltage			<u>\$</u> 0.8	. 2		٧
VIL	L Low-level input voltage					0.8	٧
VI	Input voltage		l å	5.5		5.5	٧
ЮН	High-level output current		6	-24		-32	mA
lOL	Low-level output current		8	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	\$0,	10		10	ns/V
TA	Operating free-air temperature		₹ –55	125	-40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS			SN54LVT16952			SN74LVT16952			
PARAMETER				MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	l _{OH} = -100 μA		VCC-C).2		VCC-0).2		
Vall	V _{CC} = 2.7 V,	1 _{OH} = -8 mA		2.4			2.4			v
Voн	V _{CC} = 3 V	IOH = - 24 mA		2						, v
	ACC = 2 A	I _{OH} = −32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		IOL = 16 mA				0.4			0.4	V
VOL.	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	'
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		IOL = 64 mA				dis			0.55	
	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control pins		Š	<√ ±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control pins		Į.	10			10	
l _l		V _I = 5.5 V				20			20	μА
	V _{CC} = 3.6 V	VI = VCC	A or B ports§		S	1			1	
		V ₁ = 0			5	-5			- 5	
l _{off}	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5 V		<i>&</i> *					±100	μΑ
1.4 1-5	V _{CC} = 3 V	V _I ≈ 0.8 V	A or B ports	75			75			μА
l _I (hold)	VCC = 0 V	V _I = 2 V	A of B ports	-75			-75			μν
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			_1	μΑ
			Outputs high			0.12			0.12	
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low			5			5	mA
, CO	V _I = V _{CC} or GND	Outputs disabled			0.12			0.12		
∆ICC [¶]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	One input at V _{CC} – 0.6 GND	V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				13			13		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

 $[\]P$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54LVT16952			SN74LVT16952				
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	0	150	MHz
t _W Pulse duration	CLKEN high	3.3		3.3		3.3		3.3			
	Puise duration	CLK high or low	3.3		3 .3		3.3		3.3		ns
		Data before CLK high or low	2.1		//2.9		2.1		2.9		
t _{SU} Setup time	CLKEN before CLK, data high or low	1.2		1.6		1.2		1.6		ns	
t _h Hold time	Data after CLK high or low	0.7	Ñ	0.7		0.7		0.7			
	CLKEN after CLK, data high or low	1.4	ê.	1.5		1.4		1.5		ns	

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Note 5)

-			SN54LVT16952				SN74LVT16952						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V						V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
fmax			150		160		150			150		MHz	
^t PLH	CLKBA or	A or B	2	5.4	25	6.1	2	3.4	5.8		7.1	ns	
t _{PHL}	CLKAB	Aorb	2	5.4	S.	5.7	2	3.4	5.8		6.9	118	
t _{PZH}	OEBA or	A or B	1	4.7	•	5.8	1	2.7	5.6		6.7		
tPZL_	OEAB	AOIB	1.2	<i>4</i> 6		5.5	1.2	2.7	6.5		8	ns	
t _{PHZ}	OEBA or	A or B	2.3	5.7		6.1	2.3	3.9	6.3		6.9	ns	
†PLZ	ŌĒĀB	7016	2.2	[≪] 5.2		5.3	2.2	3.9	5.1		5.3	115	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

General Information	1
LVT Octals	2
LVTZ Octals: Power-Up, 3-State	3
LVT Widebus™	4
LVT JTAG/IEEE 1149.1	5
GTL Transceivers and Backplane Drivers	6
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LV MSI and Octals	10
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LVT JTAG/IEEE 1149.1

Features

- Compatibility with IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) and boundary-scan architecture
- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- Expanded V_{CC} range from 2.7 V to 3.6 V

- EIAJ TSSOP, JEDEC SSOP, and EIAJ TQFP fine-pitch surface-mount packaging
- **Bus-hold circuitry**
- 18-bit and 20-bit UBT™ architectures
- Additional SCOPE™ instructions available such as:
 - Parallel Signature Analysis (PSA)
 - Pseudo-Random Pattern Generation (PRPG)
- Test-mode or normal-mode operation
- Members of the Texas Instruments SCOPE™ family of testability products
- TI has established an alternate source

Benefits

- Facilitate testing of complex circuit board assemblies via a 4-wire test access port
- No system throughput or cycle time penalty for boundary-scan implementation
- 3.3-V logic family with equivalent drive performance of 5-V ABT logic family - not just a recharacterized, scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- Functional equivalents to standard ABT devices offer system and test designers flexible integration options
- Save valuable board space
- Reduce component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Advanced integration, as one UBT™ can replace nearly all common bus-interface logic
- Built-in self-test feature allows easy upgrade for advanced JTAG test applications
- IEEE Standard 1149.1-1990 protocol can be bypassed for applications not requiring boundary scan
- Compatible with complete line of system-level test products including controllers, bus monitors, scan path linkers, scan path selectors, application-specific products, and very large-scale integration products
- Standardization that comes from a common product approach

Information regarding the tap control state diagram, signal descriptions, and other related JTAG/IEEE 1149.1 information for the 'LVT18245, 'LVT18502, 'LVT182502, 'LVT18504, 'LVT182504, 'LVT18640, 'LVT18640, 'LVT182646, 'LVT182646, 'LVT182652 is similar to that for the 'ABT18245. Therefore, this information will only be provided in the data sheet for the 'ABT18245 in section 9 of the 1993 ABT data book. Please contact your local TI sales representative for further information.

} .

SN54LVT18245, SN74LVT18245 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS

SCBS161A - AUGUST 1993 - REVISED MARCH 1994

- Members of the Texas Instruments SCOPE™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- SCOPE™ Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation
 From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18245 . . . WD PACKAGE SN74LVT18245 . . . DGG OR DL PACKAGE (TOP VIEW)

1DIR	1	56	10E
1B1 [2	55	1A1
1B2	3	54	1A2
GND[4	53] GND
1B3 [1A3
1B4[51	1A4
v _{cc} [7	50	V _{CC}
1B5	8	49	1A5
1B6[9	48	1A6
1B7 🕻	10	47	1A7
GND[11	46	GND
1B8 🛚	12	45	1A8
1B9 [13	44	1A9
2B1 [2A1
2B2 [42	2A2
2B3 [41	2A3
2B4 [40	2A4
GND [39	GND
2B5 [19	38	2A5
2B6 🛚	20	37	2A6
2B7 🛚		36	2A7
v _{cc} [22	35	Vcc
2B8 🛚			2A8
2B9 🛭			2A9
GND [32	GND
2DIR		31	20E
TDO		30	TDI
TMS[28	29	TCK

description

The SN54LVT18245 and SN74LVT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPETM bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable (\overline{OE}) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable (\overline{OE}) can be used to disable the device so that the buses are effectively isolated.

SCOPE and Widebus are trademarks of Texas Instruments Incorporated.



SN54LVT18245, SN74LVT18245 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS

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description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

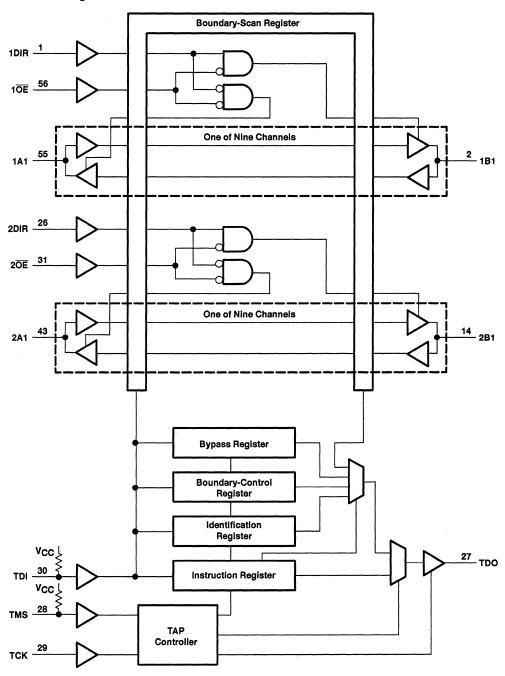
The SN74LVT18245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT18245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT18245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (normal mode, each 9-bit section)

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

functional block diagram





SN54LVT18245, SN74LVT18245 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS SCBS161A-AUGUST 1993 - REVISED MARCH 1994

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1-1A9, 2A1-2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1-1B9, 2B1-2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
GND	Ground
10E, 20E	Normal-function output enables. See function table for normal-mode logic.
тск	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} – Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, IO: SN54LVT18245	
SN74LVT18245	128 mA
Current into any output in the high state, I _O (see Note 2): SN54LVT18245	48 mA
SN74LVT18245	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	
Maximum power dissipation at T _A = 55°C (in still air): DGG package	1 W
DL package	
Storage temperature range –6	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54L\	/T18245	SN74LV	T18245	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vı	Input voltage			5.5		5.5	٧
¹ ОН	High-level output current			-24		-32	mA.
lOL	Low-level output current			24		32	mA
loL‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

^{2.} This current will only flow when the output is in the high state and $V_O > V_{CC}$.

SN54LVT18245, SN74LVT18245 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

		TOT COMPLETIONS		SNS	4LVT18	245	SN7	74LVT18	245	
PARAMETER		TEST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA	· .			-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	l _{OH} = -100 μA		V _{CC} -C	.2		VCC-C).2		
	V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			2.4			V
VOH	V 2V	IOH = - 24 mA		2						V
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Va.		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V 2V	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55				
		iOL = 64 mA							0.55	
	V _{CC} = 3.6 V,	VI = VCC or GND	DIR, ŌĒ,			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	тск			10			10	
		V _I = 5.5 V				50		1	50	
1.		VI = VCC	TDI, TMS			1			1	
lį	V 26V	V _I = 0	1			-100			-100	μА
	V _{CC} = 3.6 V	V _I = 5.5 V				20			20	
		V _I = V _{CC}	A or B ports§			1			1	
		V _I = 0	1			-5			-5	
l _{off}	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V							±100	μА
I	V 2 V	V _I = 0.8 V	A av B marks	75			75			^
l(hold)	V _{CC} = 3 V	V _I = 2 V	A or B ports	-75			-75			μA
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ
			Outputs high			2			2	
loo	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low			15			15	mA
Icc	V _I = V _{CC} or GND		Outputs disabled			2			2	IIIA
ΔI _{CC} ,¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} of		V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				11			11		рF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

SN54LVT18245, SN74LVT18245 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

	-			SN54LV	/T18245			SN74LV	T18245		
			V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _w	Pulse duration	TCK high or low					20				ns
		A, B, DIR, or OE before TCK↑					8				
tsu	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, DIR, or OE after TCK↑					1				
th	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				
td	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.

4. Load circuit and voltage waveforms are shown in Section 1.



SN54LVT18245, SN74LVT18245 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT BUS TRANSCEIVERS SCBS161A - AUGUST 1993 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 3 and 4)

			SN54I	VT18245	S	N74LV	T18245		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	V _{CC} = 3 ± 0.3	3.3 V V	V _{CC} =	2.7 V	UNIT
			MIN MAX	MIN MAX	MIN	MAX	MIN	MAX	
^t PLH	A or B	B or A			1.5	6.5			ns
^t PHL	A or B	BOIX			1.5	6.5			115
^t PZH	ŌĒ	B or A			3	9			ns
tPZL	UE	BULY			3	9			115
^t PHZ	ŌĒ	B or A			3	9.5			ne
t _{PLZ}	OE.	BULA			3	9.5			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

				SN54LV	T18245			SN74LV	T18245		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	: 3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK↓						25				MHz
t _{PLH}	TCK↓	A or B					3	22			ns
t _{PHL}	TOR	AOIB					3	22			115
t _{PLH}	TCK↓	TDO					2	12			ns
tpHL	TURT	100					2	12			118
tpzH	TCK↓	A or B					3	22			ns
^t PZL	TOR	Aorb					3	22			115
t _{PZH}	TOV	TDO					2	12			
t _{PZL}	ICK	TCK↓ TDO					2	12			ns
^t PHZ	TCK↓	A av B					3	22			
tPLZ	ICK	A or B					3	22			ns
^t PHZ	TCK↓ TDO	TOW					2	15			
[†] PLZ		סטו					2	15			ns

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.

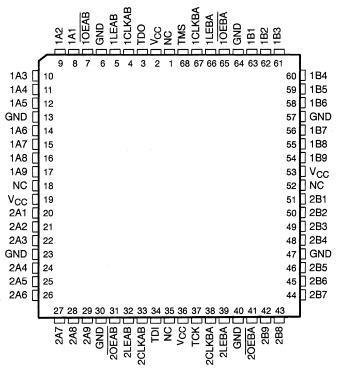
^{4.} Load circuit and voltage waveforms are shown in Section 1.

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- Members of the Texas Instruments
 SCOPE™ Family of Testability Products
- Members of the Texas Instruments
 Widebus ™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182502 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required

- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- SCOPE™ Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm
 Center-to-Center Spacings and 68-Pin
 Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18502, SN54LVT182502...HV PACKAGE (TOP VIEW)

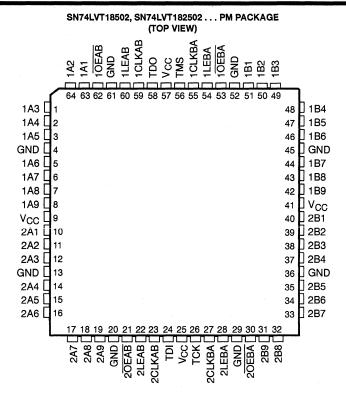


NC - No internal connection

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description

The 'LVT18502 and 'LVT182502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When OEAB is low, the B outputs are active. When OEAB is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the OEBA, LEBA, and CLKBA inputs.



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description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182502, which are designed to source or sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18502 and SN54LVT182502 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT18502 and SN74LVT182502 are characterized for operation from -40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

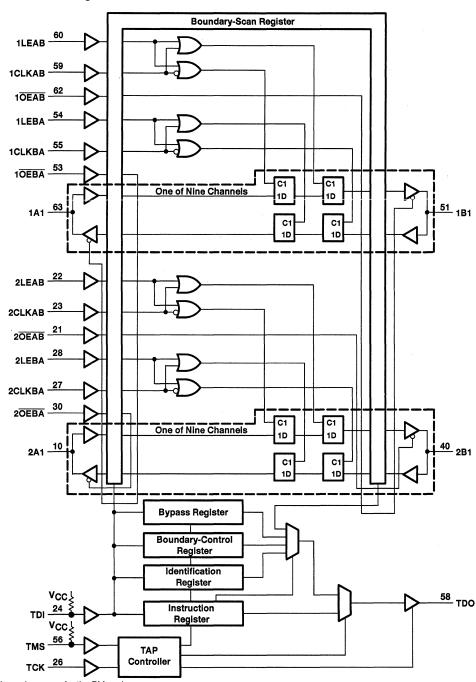
	INP	UTS		OUTPUT
OEAB	LEAB	CLKAB	Α	В
L	L	L	Χ	B ₀ ‡
L	L	↑	L	L
L	L	1	Н	Н
L	Н	Х	L	L
L	Н	Х	Н	н
Н	X	X	Χ	Z

[†] A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established.

SN54LVT18502, SN54LVT182502, SN74LVT18502, SN74LVT182502 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT UNIVERSAL BUS TRANSCEIVERS SCBS162A-AUGUST 1993 - REVISED MARCH 1994

functional block diagram



Pin numbers shown are for the PM package.



SN54LVT18502, SN54LVT182502, SN74LVT18502, SN74LVT182502 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT UNIVERSAL BUS TRANSCEIVERS SCBS162A - AUGUST 1993 - REVISED MARCH 1994

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1-1A9, 2A1-2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1-1B9, 2B1-2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table for normal-mode logic.
10EAB, 10EBA, 20EAB, 20EBA	Normal-function output enables. See function table for normal-mode logic.
тск	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the	e high state or power-off state, VO (see Note 1)0.5 V to 7 V
Current into any output in the low state, I	D: SN54LVT18502 96 mA
•	SN54LVT182502 (A port or TDO) 96 mA
	SN54LVT182502 (B port)
	SN74LVT18502 128 mA
	SN74LVT182502 (A port or TDO) 128 mA
	SN74LVT182502 (B port) 30 mA
Current into any output in the high state,	l _O (see Note 2): SN54LVT18502
	SN54LVT182502 (A port or TDO) 48 mA
	SN54LVT182502 (B port)
	SN74LVT18502 64 mA
	SN74LVT182502 (A port or TDO) 64 mA
	SN74LVT182502 (B port) 30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	
	(in still air): PM package (see Note 3) 1 W

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and VO > VCC.
 - 3. A 75-mil trace length was used to calculate ΘJA.

recommended operating conditions

	, , , , , , , , , , , , , , , , , , ,		SN54LV	T18502	SN74LV	T18502	
			MIN	MAX	MIN	0.8 5.5 -32 32 64 10	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			24		32	mA
lo _L ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

D4 D444FTFD	I	FOT COMPLETIONS		SN5	4LVT18	502	SN7	4LVT18	502	
PARAMETER	1	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	l _l = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		V _{CC} -0	.2		VCC-0).2		
	V _{CC} = 2.7 V,	I _{OH} = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						V
		IOH = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Vai		I _{OL} = 16 mA				0.4			0.4	V
VOL	\\ 0\\	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA			· .	0.55				
•		IOL = 64 mA							0.55	
	V _{CC} = 3.6 V,	VI = VCC or GND	CLK, LE, OE,			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	тск			10			10	
		V _I = 5.5 V				50			50	
1.		VI = VCC	TDI, TMS			1			1	
. II	V 26V	V _I = 0				0.5 0.5 0.55 0.55 ±1 ±1 10 10 50 50	μА			
	V _{CC} = 3.6 V	V _I = 5.5 V				20	ĺ		20	
		VI = VCC	A or B ports§			1			1	
		V _I = 0				-5			-5	
l _{off}	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V						±100	μΑ
lia in	Vac 2V	V _I = 0.8 V	A or B ports	75			75			
l (hold)	V _{CC} = 3 V	V _I = 2 V	A of B ports	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1	-		-1	μA
			Outputs high			2			2	
lcc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	l _O = 0,	Outputs low			15			15	, mA
	41 = 400 or are		Outputs disabled			2			2	
ΔICC¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or	One input at V _{CC} - GND	- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				11			11		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

					SN54LV	T18502			SN74LV	T18502		
				VCC =		V _{CC} =	2.7 V	VCC =		V _{CC} =	2.7 V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA						0	100			MHz
	Pulse duration	CLKAB or CLKBA high	or low					5				
t _W	Puise duration	LEAB or LEBA high						5				ns
		A before CLKAB↑ or B before CLKBA↑						5				
t _{su}	Setup time	A before LEAB↓ or B	CLK high					5				ns
ļ ·		before LEBA↓	CLK low					5				
th	Hold time	A after CLKAB↑ or B after CLKBA↑						0				ns
- 1		A after LEAB↓ or B aft	er LEBA↓					2				

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18502			SN74LV	T18502		
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} =		V _{CC} =	2.7 V	UNIT
		•	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _W	Pulse duration	TCK high or low					20				ns
		A, B, CLK, LE, or OE before TCK↑					8				
t _{su}	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, CLK, LE, or OE after TCK↑					1				
th	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				
t _d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

5. Load circuit and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			1	SN54LV	T18502			SN74LV	T18502						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} =				UNIT				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX]				
fmax	CLKAB or CLKBA	`					100				MHz				
tPLH.	A or B	B or A					2	7							
^t PHL	A 01 B	BOTA					2	7			ns				
^t PLH	CLKAB or CLKBA	B or A					2.5	8.5			ns				
t _{PHL}	OLKAB OF OLKBA						2.5	8.5			115				
tPLH	LEAB or LEBA	B or A					2.5	9			ns				
t _{PHL}	LEAD OF LEBA	BUIA					2.5	9			lis				
^t PZH	OEAB or OEBA	B or A					2	10			ns				
tPZL	OEAD OF OEBA	BULA					2	10			l iis				
^t PHZ	OEAB or OEBA	B or A	P or A	D or A	P or A	OEAR or OERA					2.5	9			ns
^t PLZ	OLAB OF OEBA						2.5	9			l is				

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18502			UNIT			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			3.3 V 3 V	V _{CC} = 2.7 V	
I		-	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK						25	*			MHz
^t PLH	TCK↓	A or B					3	22			ns
^t PHL	I ON↓	AOIB					3	22			118
^t PLH	TCK↓	TDO					2	12			
tPHL_	1004	TDO					2	12			ns
^t PZH	TCK↓	A or B					3	22			ns
tPZL	1004	A 01 B					3	22			119
^t PZH	TCK↓	TDO					2	12			ns
tPZL ·	1004	100					2	12			118
^t PHZ	TCK↓	A or B					3	22			ns
tPLZ	1004	7018					3	22			113
^t PHZ	TCK↓	TDO					2	15			
tPLZ	ION						2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

5. Load circuit and voltage waveforms are shown in Section 1.



SN54LVT18502, SN54LVT182502, SN74LVT18502, SN74LVT182502 3.3-V ABT SCAN TEST DEVICES WITH 18-BIT UNIVERSAL BUS TRANSCEIVERS SCBS162A-AUGUST 1993 - REVISED MARCH 1994

recommended operating conditions

		-	SN54LV	T182502	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VιΗ	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
٧ı	Input voltage			5.5		5.5	V
1	Mich level a devid a ment	A port, TDO		-24		-32	
JOH	High-level output current	B port		-12		-12	mA
1	Lavi laval avitant avimant	A port, TDO		24		32	0
IOL	Low-level output current	B port		12		12	mA
lOL [†]	Low-level output current	A port, TDO		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

DADAMETED		TOT CONDITIONS		SN5	4LVT182	502	SN7	4LVT182	502	
PARAMETER	'	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	l _{OH} = -100 μA		V _{CC} -0	.2		VCC-C	.2		
	$V_{CC} = 2.7 \text{ V},$	$I_{OH} = -8 \text{ mA}$	A nort TDO	2.4			2.4			
Voн		I _{OH} = -24 mA	A port, TDO	2						V
	V _{CC} = 3 V	I _{OH} = -32 mA					2			
		I _{OH} = - 12 mA	B port	2			2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	V(() = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
		I _{OL} = 16 mA	A port, TDO			0.4			0.4	
v_{OL}		I _{OL} = 32 mA	A port, 100			0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
		I _{OL} = 12 mA	B port			0.8			0.8	
	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND	CLK, LE, OE,			±1			±1	
	$V_{CC} = 0$ or MAX‡,	V _I = 5.5 V	TCK			10			10	
		V _I = 5.5 V				50			50	
lj		VI = VCC	TDI, TMS			1			1	μА
'1	V _{CC} = 3.6 V	V _I = 0				-100			-100	μΛ
	VCC = 5.5 V	V _I = 5.5 V				20			20	
		V _I = V _{CC}	A or B ports§			1			1	
		V ₁ = 0				-5			-5	
l _{off}	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5	V						±100	μΑ
l. a t-n	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 3 V	V _I = 2 V	A of B ports	-75			-75			μΛ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ
	V 0 0 V	1 0	Outputs high			2			2	
lcc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	IO = 0,	Outputs low			20			20	mA
	11-100 01 0113		Outputs disabled			2			2	
∆ICC [¶]	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} of	One input at V _{CC} - or GND	- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Cio	V _O = 3 V or 0				11			11		рF
Co	V _O = 3 V or 0				8			8		рF

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 $[\]S$ Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

					SN54LV	T182502			SN74LV	T182502		
				V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA						0	100			MHz
	Pulse duration	CLKAB or CLKBA high or low						5				
tw	Puise duration	LEAB or LEBA high						5			ns	
	Westerland the second s	A before CLKAB↑ or B before CLKBA↑						5				
t _{su}	Setup time	A before LEAB↓ or B	CLK high					5				ns
		before LEBA↓	before LEBA↓ CLK low					5				
th	Hold time	A after CLKAB↑ or Hold time B after CLKBA↑						0				ns
		A after LEAB↓ or B after LEBA↓						2				

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

	_			SN54LV	T182502		,	SN74LV	T182502		
			V _{CC} =		V _{CC} =	2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _W	Pulse duration	TCK high or low					20				ns
		A, B, CLK, LE, or OE before TCK1					. 8				
t _{su}	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, CLK, LE, or OE after TCK↑					1				
th	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				1
^t d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

5. Load circuit and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			1 9	SN54LV	Γ182502			SN74LV	T182502			
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fmax	CLKAB or CLKBA						100				MHz	
^t PLH	A or B	B or A					2	8				
t _{PHL}	AOIB	BOLY					2	8			ns	
tPLH	CLKAB or CLKBA	B or A					2.5	9.5				
t _{PHL}	CLNAB OF CLNBA						2.5	9.5			ns	
tPLH	LEAB or LEBA	B or A					2.5	10			na	
tPHL	LEAD OF LEBA	BULA					2.5	10			ns	
^t PZH	OFAR or OFRA	P or A	OEAB or OEBA B or A					2	11			
^t PZL	OEAD OF OEBA						2	11			ns	
tPHZ	OEAB or OEBA	B or A	OFAR at OFRA					2.5	9			
t _{PLZ}	OEAD OF OEDA						2.5	9			ns	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T182502			SN74LV	T182502		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK						25				MHz
tPLH	TCK↓	A or B					3	25			20
t _{PHL}	ICK\$	AOIB					3	25			ns
tPLH	TCK↓	TDO					2	12			
^t PHL	ICK	100					2	12			ns
^t PZH	TCK↓	A or B					3	25			
tPZL	10A						3	25			ns
^t PZH	TCK↓	TDO					2	12			
tPZL	ICK	100					2	12			ns
tPHZ	TCV	A au D					3	25			
tPLZ	TCK↓	A or B					3	25			ns
t _{PHZ}	TOK	TDO					2	15			
tPLZ	TCK↓	TDO -					2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

5. Load circuit and voltage waveforms are shown in Section 1.

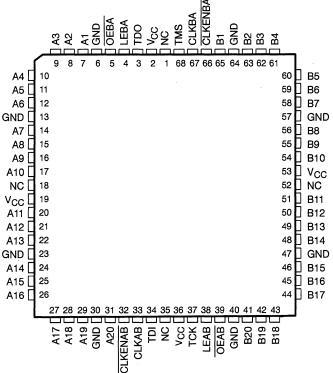


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- Members of the Texas Instruments
 SCOPE™ Family of Testability Products
- Members of the Texas Instruments Widebus ™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182504 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required

- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- SCOPE™ Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm
 Center-to-Center Spacings and 68-Pin
 Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18504, SN54LVT182504 . . . HV PACKAGE (TOP VIEW)

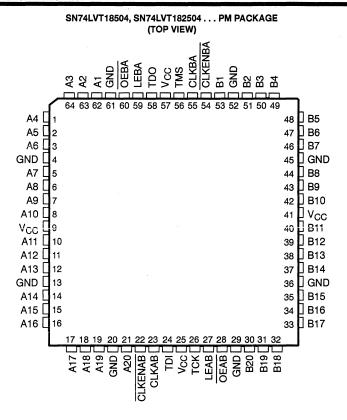


NC - No internal connection

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description

The 'LVT18504 and 'LVT182504 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPETM universal bus transceivers.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), clock-enable (CLKENBA) and CLKENBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKENAB is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and CLKENAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When OEAB is low, the B outputs are active. When OEAB is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the OEBA, LEBA, CLKENBA, and CLKBA inputs.



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description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182504, which are designed to source or sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18504 and SN54LVT182504 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT18504 and SN74LVT182504 are characterized for operation from -40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

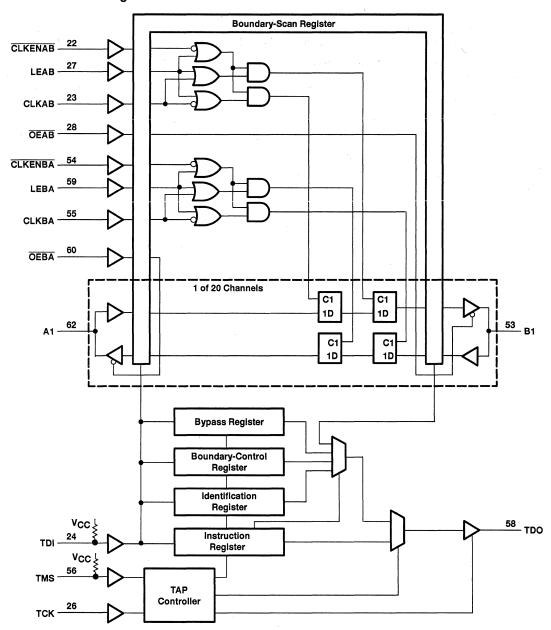
		INPUTS			OUTPUT
OEAB	LEAB	CLKENAB	CLKAB	Α	В
L	L	L	L	Х	B ₀ ‡
L	L	L	1	L	L
L	L	L	1	н	н
L	L	Н	Х	Χ	В ₀ ‡
L	H	X	Х	L	L
L	Н	X	Х	Н	н
Н	X	X	. X	Х	Z

[†] A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, CLKENBA, and CLKBA.

Output level before the indicated steady-state input conditions were established.

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functional block diagram



Pin numbers shown are for the PM package.



SN54LVT18504, SN54LVT182504, SN74LVT18504, SN74LVT182504 3.3-V ABT SCAN TEST DEVICES WITH 20-BIT UNIVERSAL BUS TRANSCEIVERS SCBS163A - AUGUST 1993 - REVISED MARCH 1994

Terminal Functions

TERMINAL NAME	DESCRIPTION
A1-A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1-B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
CLKENAB, CLKENBA	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
OEAB, OEBA	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT18504
SN54LVT182504 (A port or TDO)
SN54LVT182504 (B port)
SN74LVT18504
SN74LVT182504 (A port or TDO)
SN74LVT182504 (B port)
Current into any output in the high state, I _O (see Note 2): SN54LVT18504
SN54LVT182504 (A port or TDO) 48 mA
SN54LVT182504 (B port) 30 mA
SN74LVT18504 64 mA
SN74LVT182504 (A port or TDO) 64 mA
SN74LVT182504 (B port)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air): PM package (see Note 3)
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
 - 3. A 75-mil trace length was used to calculate ΘJA.

recommended operating conditions

		SN54LV	T18504	SN74LV	UNIT		
	*		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2	,	٧
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
Іон	High-level output current			-24		-32	mA
loL	Low-level output current			24		32	mA
lo _L ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

DADAMETER	_	FOT COMPLETIONS		SNS	4LVT18	504	SN7	4LVT18	504	HAUT
PARAMETER	1	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		V _{CC} -C).2		V _{CC} -0	.2		
Vari	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	IOH = -24 mA		2						V
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		I _{OL} = 16 mA				0.4		0.4	V	
VOL	V _{CC} = 3 V	I _{OL} ≈ 32 mA				0.5			0.5	·
	100-34	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
	$V_{CC} \approx 3.6 \text{ V},$	VI = VCC or GND	CLK, CLKEN, LE,			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	ŌĒ, TCK			10			10	
		V _I = 5.5 V				50			50	
l _l	Vcc ≈ 3.6 V	VI = VCC	TDI, TMS			1			1	μA
•1		V _I = 0				-100			-100	μ,
	100 = 0.0 1	V _I = 5.5 V	1			20			20	
		VI = VCC	A or B ports§			1			1	
		V _I = 0				-5			-5	
loff	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5	V						±100	μΑ
l(hold)	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μA
·1(11010)	100-01	V _I = 2 V	, rei a perte	-75			-75			μ.
lozh	V _{CC} = 3.6 V,	V _O = 3 V				<u> </u>			1	μΑ
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V	·			-1			-1	μA
	V _{CC} = 3.6 V,	I _O = 0,	Outputs high			2			2	
ICC	V _I = V _{CC} or GND	10 = 0,	Outputs low			15			15	mA
			Outputs disabled			2			2	
ΔICC¶	$V_{CC} \approx 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} or	One input at V _{CC} - GND	- 0.6 V,			0.2			0.2	mA
C _i	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				11			11		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

					SN54LV	T18504			SN74LV	T18504		
i				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		VCC =	V _{CC} = 3.3 V ± 0.3 V		2.7 V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA	4					0	100			MHz
	Pulse duration	CLKAB or CLKBA	A high or low					5				
t _W	ruise duration	LEAB or LEBA	CLK high or low					5				ns
	Setup time	A before CLKAB1 B before CLKBA1						5				
t _{su}		Setup time	Setup time A before LEAB↓	CLK high					5			
		or B before LEBA↓	CLK low					5				
		CLKEN before CI	_K↑					5				
		A after CLKAB↑ or B after CLKBA↑ 0										
th	Hold time	A after LEAB↓ or B after LEBA↓ 2 CLKEN after CLK↑ 0			/		2				ns	
												

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18504			SN74LV	T18504		
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	1		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	тск					0	25			MHz
t _W	Pulse duration	TCK high or low					20				ns
		A, B, CLK, CLKEN, LE, or OE before TCK1					8				
tsu	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, CLK, CLKEN, LE, or OE after TCK↑					1	,			
^t h	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					. 1	í			
^t d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.



^{5.} Load circuit and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	T18504			SN74LV	T18504		
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fmax	CLKAB or CLKBA						100				MHz
tPLH	A or B	B or A					2	7			
^t PHL	A 01 B	A 01 B 01 A					2	7			ns
t _{PLH}	CLKAB or CLKBA	B or A					2.5	8.5			ns
t _{PHL}	CLKAB or CLKBA	B or A					2.5	8.5			115
tPLH .	LEAB or LEBA	B or A					2.5	9			
t _{PHL}	LEAD OF LEDA	DOLY					2.5	9			ns
^t PZH	OFAR as OFRA	P.or A					2	10			
^t PZL	OEAB or OEBA	B or A					2	10			ns
tPHZ	OEAB or OEBA	P or A					2.5	9			
t _{PLZ}	OEAB or OEBA B or A					2.5	9			ns	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18504			SN74LV	T18504		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fmax	TCK						25				MHz
t _{PLH}	тск↓	A or B					3	22			ns
t _{PHL}	1 OK	AOIB					3	22			115
t _{PLH}	тск↓	TDO					2	12			ns
tPHL	1 GR	100					2	12			110
^t PZH	тск↓	A or B					3	22			ns
tPZL	10K¢	AOIB					3	22			115
^t PZH	TCK↓	TDO					2	12			ns
t _{PZL}	1 CK	100					2	12			115
^t PHZ	TCK↓	A or B					3	22			
tPLZ	1000	7010					3	22			ns
t _{PHZ}	TCK↓	TDO					2	15			ne
tPLZ	1000	CK↓ TDO -					2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.



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recommended operating conditions

			SN54LV	Г182504	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
1	High-level output current	A port, TDO		-24		-32	mA
JOH	nigri-level output current	B port		-12		-12	mA
10.	Low level output ourrent	A port, TDO		24	-	32	-mA
IOL	Low-level output current	B port		12		12	mA
lo _L †	Low-level output current	A port, TDO		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

0404445750	_	FOT COMPLETIONS		SN5	4LVT182	2504	SN7	4LVT182	504	
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C	.2		VCC-0	.2		
	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA	A port, TDO	2.4			2.4			
Vон		IOH = - 24 mA	A port, 100	2						٧
	V _{CC} = 3 V	IOH = -32 mA					2			
		I _{OH} = - 12 mA	B port	- 2			2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	IOL = 24 mA				0.5			0.5	
		IOL = 16 mA	A port, TDO			0.4			0.4	
VOL		IOL ≈ 32 mA	A port, 100			0.5			0.5	
	V _{CC} = 3 V	IOL = 48 mA				0.55				
		IOL = 64 mA	i						0.55	
		IOL = 12 mA	B port			0.8			0.8	
	V _{CC} = 3.6 V,	VI = VCC or GND	CLK, CLKEN, LE,			±1			±1	
	V _{CC} = 0 or MAX [‡] ,	V _I = 5.5 V	ŌĒ, TCK			10			10	
F		V _I = 5.5 V				50			50	
1.	j	V _I = V _{CC}	TDI, TMS			1			1	
l _l		V _I = 0				-100			-100	μА
	V _{CC} = 3.6 V	V _I = 5.5 V				. 20			20	
		VI = VCC	A or B ports§			1			1	
		V _I = 0				-5			-5	
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V						±100	μΑ
1	V 0V	V _I = 0.8 V	A or B ports	75			75			
l(hold)	V _{CC} = 3 V	V _I = 2 V	A or b ports	-75			-75			μΑ
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V		,		-1			-1	μΑ
			Outputs high			2			2	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low			20			20	mΑ
	Al = ACC or GIAD		Outputs disabled			2			2	
Δlcc¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} - r GND	- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Cio	V _O = 3 V or 0				11			11		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

					SN54LV	T182504		Ş	SN74LV	T182504				
				V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
^f clock			4					. 0	100			MHz		
	Pulse duration	CLKAB or CLKBA high or low						5						
t _w	Puise duration	LEAB or LEBA	CLK high or low					5				ns		
	Setup time	A before CLKAB B before CLKBA						5						
t _{su}		A before I EAR	Setup time	A before LEAB↓	CLK high					5				ns
00			CLK low					5						
		CLKEN before C	LK↑					5						
		A after CLKAB1 of B after CLKBA1	or					0						
th	Hold time	lold time A after LEAB↓ or B after LEBA↓					2				ns			
	 	CLKEN after CLK	rt -				,	0						

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T182504						
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
	9		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _w	Pulse duration	TCK high or low					20				ns
	_	A, B, CLK, CLKEN, LE, or OE before TCK1					8				
t _{su}	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, CLK, CLKEN, LE, or OE after TCK1					1				
^t h	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				
td	Delay time	Power up to TCK1					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			5	SN54LV	T182504			SN74LV	T182504		
PARAMETER	FROM (INPUT)			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fmax	CLKAB or CLKBA						100				MHz
t _{PLH}	A or B	B or A					2	8			
^t PHL	AOIB	B 01 A					2	8			ns
t _{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			
t _{PHL}	CLNAB OF CLNBA	BOIA					2.5	9.5			ns
^t PLH	LEAB or LEBA	B or A					2.5	10			ns
tPHL.	LEAD OF LEDA	BOIA					2.5	10			115
tPZH	OEAB or OEBA	B or A					2	11			
tPZL	OEAD OF OEBA	BUA					2	11			ns
^t PHZ	OEAB or OEBA	B or A					2.5	9			20
tPLZ	OLAD OF OEBA	BOLK					2.5	9			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				N54LV	T182504		,	SN74LV	T182504	•	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	: 2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK						25				MHz
^t PLH	TCK↓	A or B					3	25			ns
t _{PHL}	1000	A 01 B					3	25			115
t _{PLH}	тск↓	TDO					2	12			ns
tPHL	1004	150					2	12			115
^t PZH	TCK↓	A or B					3	25			ns
^t PZL	TOR	A OF B					3	25			115
^t PZH	TCK↓	TDO					2	12			ns
^t PZL	10K	100					2	12			115
^t PHZ	TCK↓	A or B					3	25			
t _{PLZ}	ION	A UF B					3	25			ns
^t PHZ	TCK↓	TDO					2	15			
tPLZ	ION	100					2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.





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 Members of the Texas Instruments SCOPE™ Family of Testability Products Members of the Texas Instruments 	SN54LVT18 SN74LVT18640 (
Widebus ™ Family		U	h
State-of-the-Art 3.3-V ABT Design Supports	1DIR		10E
Mixed-Mode Signal Operation (5-V Input	1B1 [] 1A1
and Output Voltages With 3.3-V V _{CC})	1B2		1A2
Support Unregulated Battery Operation	GND		GND
Down to 2.7 V	1B3 [1A3
	1B4 [] 1A4
Bus-Hold Data Inputs Eliminate the Need	V _{CC} [V _{CC}
for External Pullup Resistors	1B5 L		1A5
Compatible With the IEEE Standard	1B6 [] 1A6
1149.1-1990 (JTAG) Test Access Port and	1B7 [1A7
Boundary-Scan Architecture	GND [1B8 [GND
 SCOPE™ Instruction Set 	1B9 [1A8
 IEEE Standard 1149.1-1990 Required 	2B1] 1A9] 2A1
Instructions and Optional CLAMP and			
HIGHZ	2B2 [2B3 [2A2
 Parallel Signature Analysis at Inputs 	2B3 L 2B4 [2A3
 Pseudo-Random Pattern Generation 			2A4
From Outputs	GND [2B5 [] GND] 2A5
 Sample Inputs/Toggle Outputs 	2B5 [2A5 2A6
- Binary Count From Outputs	2B7 [2A6 2A7
- Device Identification			
 Even-Parity Opcodes 	V _{CC} [22 35	V _{CC}
 Packaged in Plastic 300-mil Shrink 	2B8[] 2A8] 2A9
Small-Outline (DL) and Thin Shrink	2B9 [
Small-Outline (DGG) Packages and 380-mil	GND [GND
Fine-Pitch Ceramic Flat (WD) Packages	2DIR [] 2 0E] TDI
Using 25-mil Center-to-Center Spacings	TDO[-
	тмѕ[28 29] тск

description

The SN54LVT18640 and SN74LVT18640 scan test devices with 18-bit inverting bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit inverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPETM bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable (\overline{OE}) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable (\overline{OE}) can be used to disable the device so that the buses are effectively isolated.

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description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT18640 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

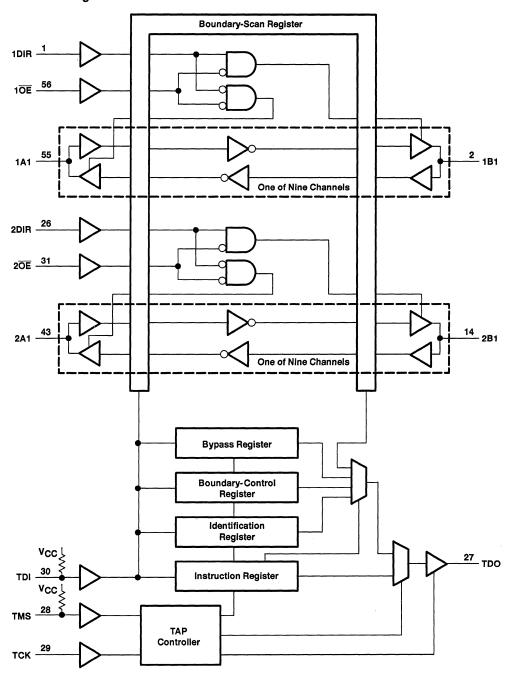
The SN54LVT18640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18640 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (normal mode, each 9-bit section)

INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	Ā data to B bus
Н	Χ	Isolation



functional block diagram





Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1-1A9, 2A1-2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1-1B9, 2B1-2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
GND	Ground
10E, 20E	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT18640	0.0 V t0 7 V
SN74LVT18640	
Current into any output in the high state, I _O (see Note 2): SN54LVT18640	
SN74LVT18640	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, $I_{OK}(V_O < 0)$	
Maximum power dissipation at T _A = 55°C (in still air): DGG package	1 W
DL package	
Storage temperature range –6	35°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and VO > VCC.

recommended operating conditions

			SN54LV	T18640	SN74LV	T18640	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			24		32	mA
loL [‡]	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER		FOT COMPLETIONS		SN5	4LVT18	640	SN7	4LVT18	640	UNIT
PARAMETER	•	FEST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	V _{CC} = 2.7 V,	l _l = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX‡,	I _{OH} = -100 μA		VCC-0	.2		VCC-C).2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						V
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	VCC = 3 V	I _{OL} = 48 mA				0.55				
	<u> </u>	I _{OL} = 64 mA							0.55	
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	DIR, OE,			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	тск			10			10	
		V _I = 5.5 V				50			50	
1.		VI = VCC	TDI, TMS			1			1	μΑ
lj.	V _{CC} = 3.6 V	V _I = 0				-100			-100	μΑ
	VCC = 3.6 V	V _I = 5.5 V				20			20	
		V _I = V _{CC}	A or B ports§			1			1	
	-	V _I = 0				-5			-5	
loff	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V							±100	μА
lia - i-s	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l (hold)	VCC = 3 V	V _I = 2 V	A OF B ports	75			-75			μΛ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μА
^I OZL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μА
			Outputs high			2			2	
lcc	V _{CC} = 3.6 V,	$I_{O}=0$,	Outputs low			15			15	mA
,00	V _I = V _{CC} or GND		Outputs disabled			2			2	IIIA
ΔICC [¶]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} of	One input at V _{CC} - 0.6 or GND	V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0) = 3 V or 0						11		рF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

				SN54LV	T18640			SN74LV	T18640		
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _w	Pulse duration	TCK high or low					20				ns
		A, B, DIR, or OE before TCK↑					8				
tsu	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, DIR, or OE after TCK↑					1			,	
th	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1			***************************************	
t _d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	VCC power up					1				μs

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 3 and 4)

				SN54LV	T18640						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A					1.5	7			
t _{PHL}	AOIB	BULA					1.5	7			ns
^t PZH	ŌĒ	B or A					3	9			ns
^t PZL	OE .	367					3	9			110
^t PHZ	ŌĒ	B or A					3	9.5			ns
^t PLZ	0-	BOIX					3	9.5			113

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

				SN54LV	T18640			SN74LV	T18640		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.3		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fmax	TCK↓						25				MHz
^t PLH	TCK↓	A or B					3	22			
^t PHL	10K4	AOIB					3	22			ns
^t PLH	TCK↓	TDO					2	12			
^t PHL	1000	100					2	12			ns
^t PZH	TCK↓	A or B					3	22			
^t PZL	1CK+	AOIB					3	22			ns
^t PZH	TCK↓	TDO					2	12			
^t PZL	1CK↓	TDO					2	12			ns
^t PHZ	TOK	A or B					3	22			
^t PLZ	TCK↓	A or B					3	22			ns
^t PHZ	тск↓	TDO					2	15			
^t PLZ	TOK↓	TDO					2	15			ns

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.

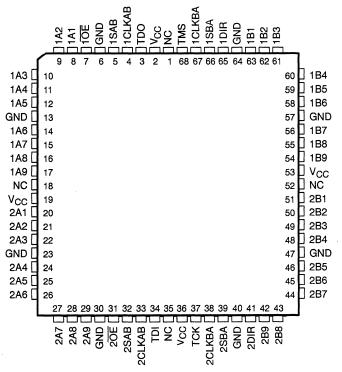
^{4.} Load circuit and voltage waveforms are shown in Section 1.

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- Members of the Texas Instruments
 SCOPE™ Family of Testability Products
- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182646 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required

- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- SCOPE™ Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm
 Center-to-Center Spacings and 68-Pin
 Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18646, SN54LVT182646 . . . HV PACKAGE (TOP VIEW)

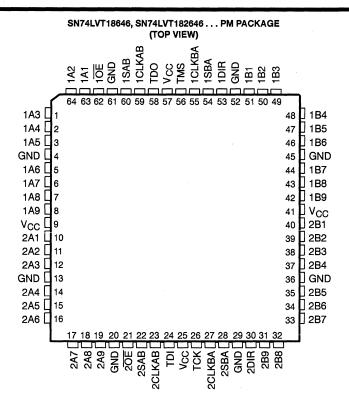


NC - No internal connection

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description

The 'LVT18646 and 'LVT182646 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable (\overline{OE}) and direction (DIR) inputs. When \overline{OE} is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When OE is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.



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description (continued)

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT18646 and 'LVT182646.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182646, which are designed to source or sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18646 and SN54LVT182646 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT18646 and SN74LVT182646 are characterized for operation from -40°C to 85°C.

FUNCTION TABLE (normal mode, each 9-bit section)

		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	OPERATION OR FUNCTION
Х	Х	1	Х	X	Х	Input	Unspecified [†]	Store A, B unspecified [†]
Х	X	X	\uparrow	X	Х	Unspecified†	Input	Store B, A unspecified [†]
Н	Х	1	1	Х	Х	Input	Input	Store A and B data
н	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	, L	X	X	X	Н	Output	Input disabled	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	Χ	Χ	Н	X	Input disabled	Output	Stored A data to B bus

[†] The data output functions can be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



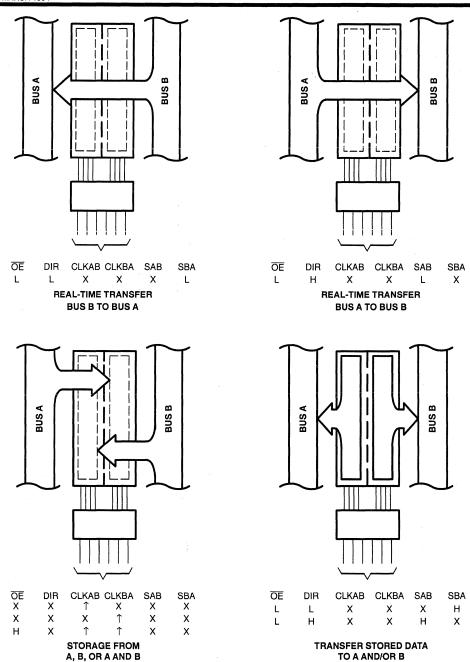
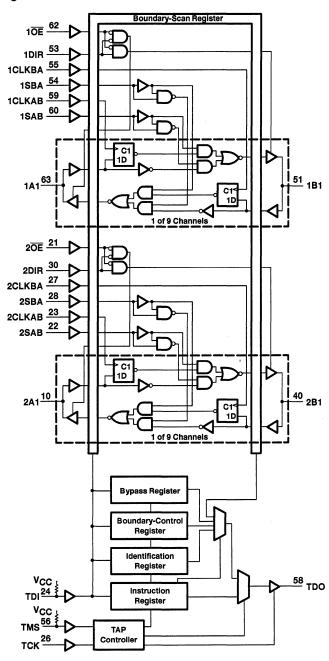


Figure 1. Bus-Management Functions



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functional block diagram



Pin numbers shown are for the PM package.



Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1-1A9, 2A1-2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
GND	Ground
10E, 20E	Normal-function output enables. See function table for normal-mode logic.
1SAB, 1SBA, 2SAB, 2SBA	Normal-function select controls. See function table for normal-mode logic.
тск	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V_{I} (see Note 1)
Voltage range applied to any output in the high state or power-off state, V $_{ m O}$ (see Note 1) $$ $$ $-$ 0.5 V to 7 V
Current into any output in the low state, I _O : SN54LVT18646
SN54LVT182646 (A port or TDO) 96 mA
SN54LVT182646 (B port)
SN74LVT18646
SN74LVT182646 (A port or TDO) 128 mA
SN74LVT182646 (B port)
Current into any output in the high state, IO (see Note 2): SN54LVT18646
SN54LVT182646 (A port or TDO) 48 mA
SN54LVT182646 (B port)
SN74LVT18646 64 mA
SN74LVT182646 (A port or TDO) 64 mA
SN74LVT182646 (B port)
input clamp current, I _{IK} (V _I < 0) –50 mA
Output clamp current, I_{OK} ($V_O < 0$)
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air): PM package (see Note 3)
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- 3. A 75-mil trace length was used to calculate Θ_{JA}.

recommended operating conditions

			SN54LV	T18646	SN74LV	T18646	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			8.0		8.0	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			24		32	mA
loL [‡]	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	_	EST CONDITIONS		SNS	4LVT18	646	SN7	LINUT		
PARAMETER	<u> </u>	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	IOH = -100 μA		VCC-C).2		VCC-C	.2		
Vou	V _{CC} = 2.7 V,	I _{OH} = – 8 mA		2.4			2.4			v
VOH	Vac. 2.V	IOH = -24 mA		2						· ·
	V _{CC} = 3 V	$I_{OH} = -32 \text{ mA}$					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Va.		IOL = 16 mA							0.4	V
VOL	V 2V	IOL = 32 mA				0.5			0.5	V
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		IOL = 64 mA							0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	CLK, DIR, OE, S,			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	тск			10			10	
		V _I = 5.5 V				50			50	
		V _I = V _{CC}	TDI, TMS			1			1	μА
Ч	V _{CC} = 3.6 V	V _I = 0				-100			-100	μА
	VCC = 3.0 V	V _I = 5.5 V				20			20	
		VI = VCC	A or B ports§			1			1	
		V _I = 0				-5			5	
l _{off}	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5$	V						±100	μΑ
lia ion	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 3 V	V _I = 2 V	A of B ports	-75			-75			μΛ
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μA
			Outputs high			2			2	
lcc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low			15			15	mA
	VI = VCC or and		Outputs disabled			2			2	
∆ICC [¶]	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o	One input at V _{CC} - r GND	- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				11			11		рF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	I54LVT18646			SN74LVT18646			
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA					0	100			MHz
t _w	Pulse duration	CLKAB or CLKBA high or low					5				ns
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
th	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18646			SN74LV	T18646		
			V _{CC} =	3.3 V 3 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V				UNIT
Į			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _w	Pulse duration	TCK high or low					20				ns
	_	A, B, CLK, DIR, OE or S before TCK1					8				
tsu	Setup time	TDI before TCK↑					8				ns
	•	TMS before TCK↑					6				
		A, B, CLK, DIR, OE or S after TCK↑					1				
th	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				
^t d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	T18646			SN74LV	T18646		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	,		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	CLKAB or CLKBA						100				MHz
^t PLH	A or B	B or A					2	7			ns
^t PHL	AUD	B 01 A					2	7			115
tPLH	CLKAB or CLKBA	B or A					2.5	8.5			ns
t _{PHL}	OLIVAD OF OLIVDA	BOIA					2.5	8.5			113
tPLH	SAB or SBA	B or A					2	9			ns
tPHL	SAD OF SBA	- BOI A					2	9			115
^t PZH	DIR	B or A					2	10			ns
tPZL	DIN						2	10			110
^t PZH	ŌĒ	B or A					2	10			ns
tPZL	OE .	BOLA					2	10			115
t _{PHZ}	DIR	B or A					3	12			200
^t PLZ	DIN	BUIA					3	12			ns
t _{PHZ}	OE .	P or A					2	11			no
^t PLZ	OE .	OE B or A					2	11			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18646			SN74LV	T18646		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	: 2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK						25				MHz
tPLH .	TCK↓	A or B					3	22			200
t _{PHL}	I ON	AOID					3	22	,		ns
tPLH	TCK↓	TDO					2	12			
tPHL	ION	TDO					2	12			ns
^t PZH	TCK↓	A or B					3	22			
tPZL	ION	AOFB					3	22			ns
^t PZH	TCK↓	TDO					2	12			
tPZL	1 CN	100					2	12			ns
tPHZ	TOV	A D					3	22			
tPLZ	TCK↓	A or B					3	22			ns
^t PHZ	TCK↓	TDO					2	15			
tPLZ	IOK	TDO					2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.



^{5.} Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54LV	Г182646	SN74LV	Г182646	UNIT
1			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5 .5	٧
1	High-level output current	A port, TDO		-24		-32	A
ЮН	nign-level output current	B port		-12		-12	mA
10.	Low-level output current	A port, TDO		24		32	mA
OL	Low-level output current	B port		12		12	mA
lo _L †	Low-level output current	A port, TDO		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER		FOT CONDITIONS		SN5	4LVT182	646	SN7	4LVT182	646		
PARAMETER	•	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	٧	
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C	.2		VCC-C).2			
	V _{CC} = 2.7 V,	I _{OH} = - 8 mA] TDO	2.4			2.4				
Vон		IOH = -24 mA	A port, TDO	2						٧	
	V _{CC} = 3 V	I _{OH} = -32 mA					2				
		I _{OH} = - 12 mA	B port	2			2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
		I _{OL} = 16 mA	A port, TDO	0.4		0.4					
VOL		I _{OL} = 32 mA	A port, TDO			0.5			0.5	V	
	V _{CC} = 3 V	I _{OL} = 48 m/\				0.55					
		I _{OL} = 64 mA							0.55		
		I _{OL} = 12 mA	B port			0.8			0.8		
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	CLK, DIR, $\overline{\text{OE}}$, S,			±1			±1		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	тск			10			10		
	ļ	V ₁ = 5.5 V				50			50		
6.		V _I = V _{CC}	TDI, TMS			1			1	μА	
lį	V 26V	V _I = 0	1	-100				-100	μА		
	V _{CC} = 3.6 V	V _I = 5.5 V				20			20		
		V _I = V _{CC}	A or B ports§			1			1		
		V _I = 0]			-5			-5		
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V						±100	μА	
1	V 2V	V _I = 0.8 V	A au B name	75			75				
[[] I(hold)	VCC = 3 V	V _I = 2 V	A or B ports	-75			-75			μА	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ	
			Outputs high			2			2		
ICC	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0,$	Outputs low			20			20	mΑ	
	At = ACC or GIAD		Outputs disabled			2			2		
ΔICC¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o	One input at V _{CC} - r GND	- 0.6 V,			0.2			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Cio	V _O = 3 V or 0				11			11		pF	
Co	V _O = 3 V or 0				8			8		рF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	T182646			SN74LV	T182646		
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 \		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA					0	100			MHz
t _W	Pulse duration	CLKAB or CLKBA high or low					5				ns
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
t _h	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			7 ;	SN54LV	T182646			SN74LV	T182646		
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _w	Pulse duration	TCK high or low					20				ns
		A, B, CLK, DIR, OE or S before TCK1					8				
t _{su}	Setup time	TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, CLK, DIR, OE or S after TCK↑					1				
^t h	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				
^t d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

		TO (OUTPUT)	SN54LVT182646				SN74LVT182646					
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fmax	CLKAB or CLKBA						100				MHz	
^t PLH	A or B	B or A					2	8			ns	
tphl.	AUB						2	. 8				
t _{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			ns	
^t PHL	OLNAD OF OLNBA						2.5	9.5				
^t PLH	SAB or SBA	B or A					2	10			ns	
^t PHL	SAD OF SDA						2	10				
^t PZH	DIR	B or A					2	11			ns	
[†] PZL	DIN						2	11				
^t PZH	ŌĒ	B or A					2	11			ns	
^t PZL	OE .						2	11				
^t PHZ	DIR	B or A					3	12			ns	
^t PLZ	DIN						3	12				
tPHZ	ŌĒ	B or A					2	11			ns	
tPLZ							2	11				

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

	FROM (INPUT)	то (оитрит)	SN54LV	T182646					
PARAMETER			V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	UNIT	
			MIN MAX	MIN MAX	MIN	MAX	MIN MAX		
f _{max}	TCK				25			MHz	
^t PLH	TCK↓	A or B			3	25		ns	
^t PHL	10K4	AOID			3	25			
tPLH	TCK↓	TDO			2	12		ns	
^t PHL	TOR	100		,	2	12			
^t PZH	TCK↓	A or B			3	25		ns	
^t PZL	I UN	AOID			- 3	25		l ris	
t _{PZH}	TCK↓	TDO			2	12		ns	
tPZL	I CK↓	100			2	12		l is	
^t PHZ	TCK↓	A D			3	25		ns	
tPLZ	10K4	A or B			3	25			
^t PHZ	TCK↓	TDO			2	15			
tPLZ	ICK				2	15		ns	

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

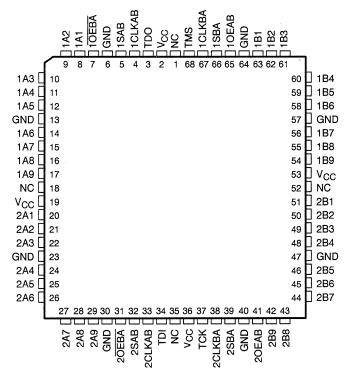


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- Members of the Texas Instruments
 SCOPE™ Family of Testability Products
- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182652 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required

- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- SCOPE™ Instruction Set
 - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
 - Parallel Signature Analysis at Inputs
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Device Identification
 - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm
 Center-to-Center Spacings and 68-Pin
 Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18652, SN54LVT182652...HV PACKAGE (TOP VIEW)

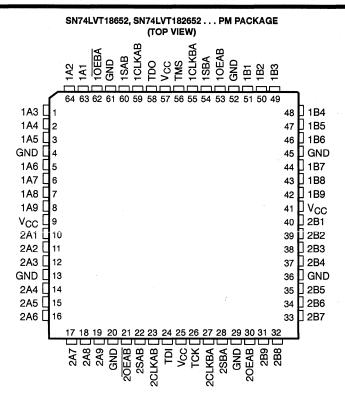


NC - No internal connection

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description

The 'LVT18652 and 'LVT182652 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state.



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description (continued)

Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when $\overline{\text{OEBA}}$ is high. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT18652 and 'LVT182652.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182652, which are designed to source or sink up to 12 mA, include 25- Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18652 and SN54LVT182652 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT18652 and SN74LVT182652 are characterized for operation from -40°C to 85°C.

FUNCTION TABLE (normal mode, each 9-bit section)

INPUTS						DAT	A I/O	OPERATION OR FUNCTION	
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A9 B1 THRU B9		OPERATION OR FUNCTION	
L	Н	L	L	Х	Х	Input disabled	Input disabled	Isolation	
L	Н	1	1	Х	Х	Input	Input	Store A and B data	
×	Н	1	L	X	X	Input	Unspecified [†]	Store A, hold B	
Н	Н	1	1	χ‡	X	Input	Output	Store A in both registers	
L	X	L	1	X	X	Unspecified [†]	Input	Hold A, store B	
L	L	1	1	X	X‡	Output	Input	Store B in both registers	
L	L	Χ	X	X	L	Output	Input	Real-time B data to A bus	
L	L	Χ	X	X	н	Output	Input.	Stored B data to A bus	
Н	Н	X	X	L	X	Input	Output	Real-time A data to B bus	
Н	Н	X	X	Н	Х	Input Output		Stored A data to B bus	
н	L	x	Х	Н	Н	Output Output		Stored A data to B bus and stored B data to A bus	

[†] The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.



Select control = L: clocks can occur simultaneously.
 Select control = H: clocks must be staggered in order to load both registers.

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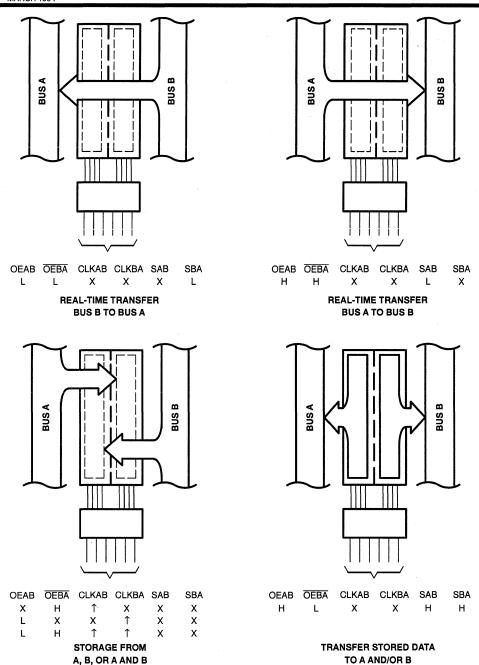
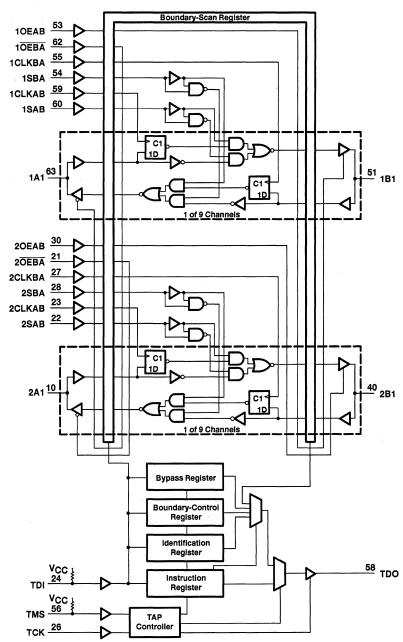


Figure 1. Bus-Management Functions



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functional block diagram



Pin numbers shown are for the PM package.



Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1-1A9, 2A1-2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1-1B9, 2B1-2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
10EAB, 20EAB	Normal-function active-high output enables. See function table for normal-mode logic.
10EBA, 20EBA	Normal-function active-low output enables. See function table for normal-mode logic.
1SAB, 1SBA, 2SAB, 2SBA	Normal-function select controls. See function table for normal-mode logic.
тск	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
Vcc	Supply voltage



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}
SN74LVT18652
SN74LVT182652 (A port or TDO)
SN74LVT182652 (B port)
Current into any output in the high state, I _O (see Note 2): SN54LVT18652
SN54LVT182652 (A port or TDO) 48 mA
SN54LVT182652 (B port)
SN74LVT18652
SN74LVT182652 (A port or TDO) 64 mA
SN74LVT182652 (B port)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air): PM package (see Note 3)
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

- 2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
- 3. A 75-mil trace length was used to calculate ΘJA.

recommended operating conditions

			SN54LV	T18652	SN74LV	T18652	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	·	2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
Vj	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			24		32	mA
lo _L ‡	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	•C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	1	TEST CONDITIONS		SN5	4LVT18	552	SN7	UNIT		
PARAMETER	ļ	IEST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	V _{CC} = 2.7 V,	lı = -18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C	.2		VCC-0	.2		
V	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			٧
VOH	Vac. 2.V	I _{OH} = -24 mA		2						V
	V _{CC} = 3 V	IOH = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	vCC = 2.7 v	i _{OL} = 24 mA				0.5			0.5	
\/		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V 2V	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	IOL = 48 mA				0.55				
		IOL = 64 mA							0.55	
*	V _{CC} = 3.6 V,	VI = VCC or GND	CLK, OEAB,			±1			±1	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V	OEBA, S, TCK			10			10	
		V _I = 5.5 V				50			50	
1.		VI = VCC	TDI, TMS			1			1	μА
ji.	V _{CC} = 3.6 V	V _I = 0				-100			-100	μА
	VCC = 3.0 V	V _I = 5.5 V				20			20	
		VI = VCC	A or B ports§			1			1	
		V ₁ = 0				-5			-5	
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V						±100	μΑ
lia in	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	ACC = 2 A	V _I = 2 V	A OI B poits	-75			-75			μ.
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
			Outputs high			2			2	
ICC	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O} = 0$,	Outputs low			15			15	mA
	ALT ACC OL CIAD		Outputs disabled			2			2	
ΔICC [¶]	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at V_{CC}		- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		рF
C _{io}	V _O = 3 V or 0	/O = 3 V or 0			11			11		рF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at VCC = 3.3 V, TA = 25°C.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

[¶]This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	T18652		SN74LVT18652				
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA					0	100			MHz
t _W	Pulse duration	CLKAB or CLKBA high or low					5				ns
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
th	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18652			SN74LV	T18652		
			V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _w	Pulse duration	TCK high or low					20				ns
t _{su}	Setup time	A, B, CLK, OEAB, OEBA or S before TCK↑					8				
		TDI before TCK↑					8				ns
		TMS before TCK↑					6				
		A, B, CLK, OEAB, OEBA or S after TCK1					1				
th	Hold time	TDI after TCK↑					1				ns
		TMS after TCK↑					1				
^t d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

5. Load circuit and voltage waveforms are shown in Section 1.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	T18652			SN74LV	T18652		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
,			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fmax	CLKAB or CLKBA						100				MHz
^t PLH	A or B	B or A					2	7			
t _{PHL}	AOIB	B 01 X					2	7			ns
^t PLH	CLKAB or CLKBA	B or A					2.5	8.5			ns
^t PHL	CLARB OF CLARBA	BULA					2.5	8.5			118
^t PLH	SAB or SBA	B or A					2	9			
t _{PHL}	SAB OF SBA	BUIA	-				2	9			ns
^t PZH	OF AD OFDA	D or A					2	10			
t _{PZL}	OEAB or OEBA	B or A					2	10			ns
t _{PHZ}	OEAB or OEBA B or A	D or A					1.5	11			
^t PLZ	OEAD OF OEDA	OEBA B or A					1.5	11			ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T18652			SN74LV	T18652		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	: 2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK						25				MHz
tPLH	TCK↓	A or B					3	22			ns
tPHL	1CK+	AUID					3	22			TIS
^t PLH	TCK↓	TDO					2	12			
tPHL	10K↓	100					- 2	12			ns
^t PZH	TCK↓	A or B					3	22			ns
tPZL	10K↓	AUID					3	22			115
^t PZH	TCK↓	, TDO					2	12			
^t PZL	TCK↓	. 100					2	12			ns
t _{PHZ}	TCK↓	A au D					3	22			
^t PLZ	I UK↓	A or B					3	22			ns
tPHZ	тск↓	TDO					2	15			200
[†] PLZ	10K↓	TDO					2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

^{5.} Load circuit and voltage waveforms are shown in Section 1.

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recommended operating conditions

			SN54LV	Г182652	SN74LV	UNIT	
	_		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	٧
lou	High-level output ourrent	A port, TDO		-24		-32	mA
ЮН	High-level output current	B port		-12		-12	IIIA
J	Low-level output current	A port, TDO		24		32	mA
IOL	Low-level output current	B port		12		12	IIIA
lOL [†]	Low-level output current	A port, TDO		48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

[†] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

DADAMETED		FEAT ACMIDITIONS		SN5	4LVT182	652	SN7	4LVT182	652	
PARAMETER	, !	TEST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = −18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX‡,	I _{OH} = -100 μA		VCC-C).2		VCC-C	.2		
	V _{CC} = 2.7 V,	IOH = - 8 mA] TDO	2.4			2.4			
VOH	:	IOH = -24 mA	A port, TDO	2	2				٧	
	V _{CC} = 3 V	I _{OH} = -32 mA				2				
		$I_{OH} = -12 \text{ mA}$	B port	2			2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA	}			0.5			0.5	
		I _{OL} = 16 mA	A nort TDO			0.4			0.4	
VOL		I _{OL} = 32 mA	A port, TDO			0.5			0.5	٧
	V _{CC} = 3 V	IOL = 48 mA]			0.55				
		I _{OL} = 64 mA							0.55	
		I _{OL} = 12 mA	B port			0.8			0.8	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	CLK, OEAB,			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	OEBA, S, TCK			10			10	
		V _I = 5.5 V				50			50	
		VI = VCC	TDI, TMS			1			1	μА
lj .	V _{CC} = 3.6 V	V _I = 0				-100			-100	μА
	vCC = 3.0 v	V _I = 5.5 V				20			20	
		V _I = V _{CC}	A or B ports§			1			1	
		V ₁ = 0	r man re equip			-5			-5	
l _{off}	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5	V						±100	μА
1.0	V-0 2 V	V _i = 0.8 V	A or B ports	75			75			Λ
I (hold)	V _{CC} = 3 V	V _I = 2 V	A or B ports	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
			Outputs high			2			2	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	I _O = 0,	Outputs low			20			20	mA
	AL = ACC OL CIAD		Outputs disabled			2			2	
Δlcc¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} of	$_{CC}$ = 3 V to 3.6 V, One input at $_{CC}$ – 0 ther inputs at $_{VCC}$ or GND				0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Cio	V _O = 3 V or 0				11			11		pF
Co	V _O = 3 V or 0				8			8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LV	T182652		SN74LVT182652				
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MiN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	CLKAB or CLKBA					0	100			MHz
t _w	Pulse duration	CLKAB or CLKBA high or low					5				ns
t _{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
th	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			Ş	SN54LV	T182652		;	SN74LV	T182652		
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK					0	25			MHz
t _W	Pulse duration	TCK high or low					20				ns
		A, B, CLK, OEAB, OEBA or S before TCK↑					8				
t _{su}	Setup time	TDI before TCK↑					8				ns
İ		TMS before TCK↑					6				
		A, B, CLK, OEAB, OEBA or S after TCK1					1				
th	Hold time	TDI after TCK↑					1				ns
l		TMS after TCK↑					1				
^t d	Delay time	Power up to TCK↑					50				ns
t _r	Rise time	V _{CC} power up					1				μs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

5. Load circuit and voltage waveforms are shown in Section 1.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			T :	SN54LV	T182652	····		SN74LV	T182652		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fmax	CLKAB or CLKBA						100				MHz
t _{PLH}	A or B	B or A					2	8			
tPHL		BOTA					2	8		,	ns
^t PLH	CLKAB or CLKBA	B or A					2.5	9.5			
^t PHL	CLKAB OF CLKBA	BUIA					2.5	9.5			ns
^t PLH	SAB or SBA	B or A					2	10			
t _{PHL}	SAB OF SBA	BUIA					2	10			ns
^t PZH	OEAB or OEBA	B or A					2	11			ns
tPZL	OEAD OF OEBA	BUIA					2	11			115
^t PHZ	OEAB or OEBA	B or A					1.5	11			ns
tPLZ	OLAD OF OLDA	BULK					1.5	11			118

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

				SN54LV	T182652		,	SN74LV	T182652		
PARAMETER	FROM (INPUT)	1	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
1			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK						25				MHz
t _{PLH}	TCK↓	A or B					3	25			
tPHL	TOK	AOIB					3	25			ns
tPLH	TCK↓	TDO					2	12			
tPHL		100					2	12			ns
^t PZH	TCK↓	A or B					3	25			ns
tPZL	1 CK	AOIB					3	25			115
^t PZH	TCK↓	TDO					2	12			ns
^t PZL	10K¢	100					2	12			ns
^t PHZ	TCK↓	A or B					3	25			
^t PLZ		A OF B					3	25			ns
t _{PHZ}	TCK↓	TDO					2	15			200
tPLZ	ION	1 100					2	15			ns

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.

^{5.} Load circuit and voltage waveforms are shown in Section 1.

General Information	1
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GTL TRANSCEIVERS AND BACKPLANE DRIVERS

Features

High-speed GTL/TTL translating

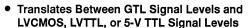
Output edge-rate control (OEC™) options

- EPIC-IIB™ BiCMOS process with special low-voltage enhancements
- Mixed-mode signal operations on A port
- **Bus-hold circuitry**
- Power-on-demand active feedback circuitry
- Widebus™ and UBT™ architectures
- JEDEC SSOP (Widebus™) and EIAJ TSSOP (Shrink Widebus™) packaging

Benefits

- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family - not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- 16- and 18-bit densities for flexible integration
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
- Ideal for high-speed bus applications
- Standardization that comes from a common product approach

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- Member of the Texas Instruments Widebus™ Family
- Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})
- State-of-the-Art BiCMOS Design for Low-Static Power Dissipation
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

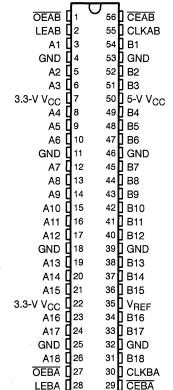
description

This 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be

DGG OR DL PACKAGE (TOP VIEW)



controlled by the chip-enable (\overline{CEAB} and \overline{CEBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CEAB} is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if \overline{CEAB} is also low. Output-enable \overline{OEAB} is active-low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and \overline{CEBA} .

To ensure the high-impedance state during power-up or power-down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16611 is characterized for operation from 0°C to 70°C.

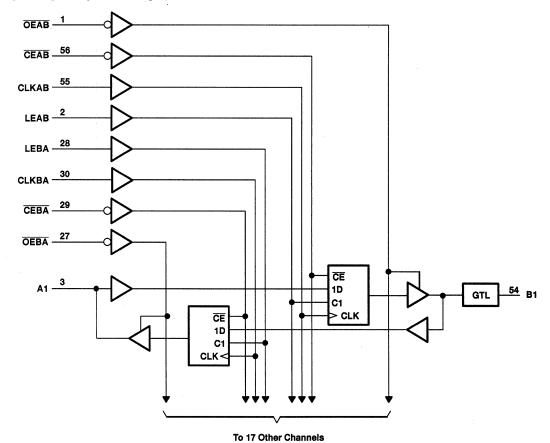
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FUNCTION TABLET

		INPUTS			ОИТРИТ	MODE	
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE	
X	Н	Х	Х	Х	Z		
L	L	L	Н	Χ	в ₀ ‡	Latched storage of A data	
L	L	L	L	Х	в ₀ §		
X	L	Н	Х	L	L	Tronggrand	
Х	L	Н	Χ	Н	н	Transparent	
L	L	L	1	L	L	Clocked storage of A data	
L.	L	L	1	Н	н	Clocked storage of A data	
Н	Ĺ	L	Х	Х	B ₀ §	Clock inhibit	

[†] A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKBA}}$, and $\overline{\text{CEBA}}$.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

[§] Output level before the indicated steady-state input conditions were established.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3-V V _{CC} –0.5 V to 4.6 V
Supply voltage range, 5-V V _{CC}
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)0.5 V to 7 V
Current into any A-port output in the low state, IO
Current into any B-port output in the low state, IO
Current into any A-port output in the high state, IO (see Note 2)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0)
Maximum power dissipation at T _A = 55°C (in still air): DGG package
DL package 1.4 W
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, 3.3 V		3.15	3.3	3.45	V
Supply voltage, 5 V		4.75	5	5.25	1 °
Supply voltage			0.8		V
long to called an	B port			Vcc	V
input voitage	Except B port			5.5)
I link lovel in a decident	B port	V _{REF} +50 m ¹	V		V
nign-ievei input voitage	Except B port	2			
Lave lave line in the sec	B port			V _{REF} -50 mV	V
Low-level input voltage	Except B port			0.8	1 °
Input clamp current				-18	mA
High-level output current	A port			-32	mA
	A port‡			64	
Low-level output current	B port			40	mA
Operating free-air temperature	•	0		70	°C
	Supply voltage, 5 V Supply voltage Input voltage High-level input voltage Low-level input voltage Input clamp current High-level output current Low-level output current	Supply voltage, 5 V Supply voltage B port Input voltage Except B port High-level input voltage Except B port Low-level input voltage B port Input clamp current Except B port Input clamp current A port Low-level output current A port‡ B port B port	Supply voltage, 3.3 V 3.15	Supply voltage, 3.3 V 3.15 3.3 Supply voltage, 5 V 4.75 5 Supply voltage 0.8 Input voltage B port Except B port High-level input voltage B port VREF +50 mV Except B port 2 Low-level input voltage B port Except B port Input clamp current Except B port Fort High-level output current A port A port Low-level output current B port B port	Supply voltage, 3.3 V 3.15 3.3 3.45 Supply voltage, 5 V 4.75 5 5.25 Supply voltage 0.8 VCC Input voltage B port VREF +50 mV High-level input voltage B port VREF +50 mV Except B port 2 Low-level input voltage B port VREF -50 mV Except B port 0.8 Input clamp current A port -18 High-level output current A port [‡] 64 Low-level output current B port 40

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

	PARAMETER	TEST CON	NDITIONS	MIN	TYP	MAX	UNIT	
٧ _{IK}		V _{CC} = 3.15 V,	I _I = −18 mA			-1.2	٧	
		V _{CC} = MIN to MAX [‡] ,	i _{OH} = -100 μA	Vcc-0	0.2			
V_{OH}	A port	V 045.V	I _{OH} = -8 mA	2.4			V	
		V _{CC} = 3.15 V	I _{OH} = - 32 mA	2				
			I _{OL} = 100 μA			0.2		
	A	V 245V	I _{OL} = 16 mA			0.4		
V_{OL}	A port	V _{CC} = 3.15 V	I _{OL} = 32 mA			0.5	٧	
			I _{OL} = 64 mA			0.55		
	B port	V _{CC} = 3.15 V,	I _{OL} = 40 mA			0.4		
	Control pins	V _{CC} = 0 or MAX [‡] ,	V _I = 5.5 V			10	μA	
			V _I = 5.5 V			20		
1.	A port§	V _{CC} = 3.45 V	VI = VCC			1		
iį.		·	V ₁ = 0			-5	μΑ	
	B port	V _{CC} = 3.45 V	VI = VCC			5		
	Броп	VCC = 5.45 V	V _I = 0	1		-5		
l "	A port	V _{CC} = 0	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$			100	μА	
loff	B port		V _I or V _O = 0 to 1.2 V			100	μΑ	
tra ris	A port	V _{CC} = 3.15 V	V _I = 0.8 V	75			μА	
l(hold)	Apolt	VCC = 3.13 V	V _I = 2 V	-75			μς	
lo	A port	V _{CC} = 3.45 V	V _O = 3 V			1	μА	
lozh	B port	VCC = 3.45 V	V _O = 1.2 V			10	μΛ	
lo-	A port	V _{CC} = 3.45 V	V _O = 0.5 V			-1	μА	
lozl	B port	VCC = 5.45 V	V _O = 0.4 V			-10	μΛ	
	A port to B port							
Icc	B port to A port	V _{CC} = 3.45 V, V _I = V _{CC} or GND	$I_{O}=0,$				mA	
	Outputs disabled	71- 100 or are						
ΔICC [¶]		V _{CC} = 3.45 V, A or control inputs at V _{CC} or GND	One input at 2.7 V,		-	1	mA	
Ci	Control pins	V _I = 3.15 V or 0			4		pF	
Cio	A port	V _O = 3.15 V or 0			10		pF	
Cio	B port	Per IEEE1194.0-1991				5	PΓ	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{\text{REF}} = 0.8 \text{ V}$ (unless otherwise noted)

			MIN	MAX	UNIT
^f clock	Clock frequency		0	150	MHz
	Pulse duration				
tw	ruise duration	CLKAB or CLKBA high or low			ns
		A before CLKAB↑	1.5		
		B before CLKAB↑	3		
		A before LEAB↓	0.5		
	Catura tima	B before LEBA↓	1.5		
t _{su}	Setup time	CEAB before CLKAB↑ CEBA before CLKBA↑			ns
		CEAB before LEAB↓			
		CEBA before LEBA↓			
		A after CLKAB↑	1		-
		B after CLKAB↑	0		
		A after LEAB↓	2.5		
	Hald the a	B after LEBA↓	2		
th	Hold time	CEAB after CLKAB↑			ns
		CEBA after CLKBA↑			
		CEAB after LEAB↓			
		CEBA after LEBA↓			

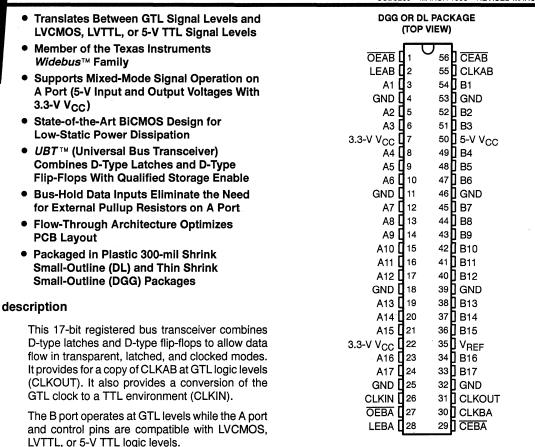
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP MAX	UNIT
fmax				MHz
^t PLH	А	В	3.2	ns
^t PHL	^	Б	3.2	110
^t PLH	LEAB	В	. 4	no
^t PHL	LEAD	В	4	ns
^t PLH	CLKAD	В	4.3	
^t PHL	CLKAB	В	4.3	ns
^t PLH	OF A D	В	4.5	
^t PHL	ŌEAB	В	4.5	ns
t _r	Transition time, B ou	utputs (0.5 V to 1 V)	1.7	ns
tf	Transition time, B ou	utputs (1 V to 0.5 V)	0.6	ns
t _{PLH}	В	_	5.7	
^t PHL	В	A	4	ns
t _{PLH}	LEBA	_	5	
^t PHL	LEBA	A	3.8	ns
^t PLH	CLKBA	^	5.2	
[†] PHL	CLKBA	Α	4.6	ns
^t EN	ŌĒBĀ	۸	6	
t _{DIS}) OEBA	A	6	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



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Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable (\overline{CEAB} and \overline{CEAB}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CEAB} is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if \overline{CEAB} is also low. Output-enable \overline{OEAB} is active-low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEBA}, LEBA, CLKBA, and \overline{CEBA}.

To ensure the high-impedance state during power-up or power-down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16615 is characterized for operation from 0°C to 70°C.

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SN74GTL16615 17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS SCBS269 – MARCH 1993 – REVISED MARCH 1994

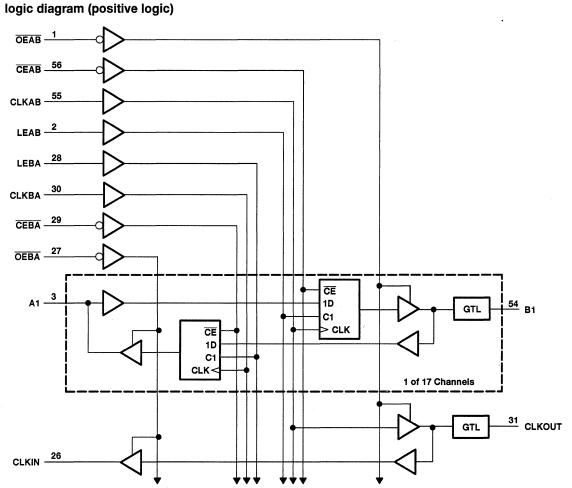
FUNCTION TABLET

		INPUTS			OUTPUT	MODE		
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE		
Х	Н	Х	Х	X	Z	,		
L	L	L	H or L	Χ	в ₀ ‡	Latched storage of A data		
L	L	L	H or L	Χ	в ₀ §			
,X	L	Н	Х	L	L	Transparent		
Х	L	Н	X	Н	Н	Transparent		
L	L	L	1	L	L	Clastrad atomora of A data		
L	L	L	1	Н	н	Clocked storage of A data		
Н	Ĺ	L	Х	Х	B ₀ §	Clock inhibit		

TA-to-B data flow is shown: B-to-A data flow is similar but uses OEBA, LEBA, CLKBA, and

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

[§] Output level before the indicated steady-state input conditions were established.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range 2.2 V V -	1 to 1 C V
Supply voltage range, 3.3 V, V _{CC}	10 4.6 V
Supply voltage range, 5 V, V _{CC}	V to 7 V
Input voltage range, V _I (see Note 1)	V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)0.5	V to 7 V
Current into any A-port output in the low state, IO	128 mA
Current into any B-port output in the low state, IO	. 80 mA
Current into any A-port output in the high state, To (see Note 2)	
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Output clamp current, $I_{OK}(V_O < 0)$	-50 mA
Maximum power dissipation at T _A = 55°C (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range ——65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V	Supply voltage, 3.3 V	Supply voltage, 3.3 V			3.45	V
Vcc	Supply voltage, 5 V		4.75	5	5.25	\ \
V _{REF}	Supply voltage			0.8		V
V.	land, allera	B port			VCC	V
V _I	Input voltage	Except B port			3.45 5.25 VCC 5.5 VREF -50 mV 0.8 -18 -32 64 40	\ \ \
	Lijah laval innut valtaga	B port	VREF +50 mV			٧
VIH	High-level input voltage	Except B port	2		3.45 5.25 V _{CC} 5.5 EF -50 mV 0.8 -18 -32 64	v
\/	Lavaleral incoderate	B port		VF	REF -50 mV	V
VIL	Low-level input voltage	Except B port			0.8	٧
İIK	Input clamp current				-18	mA
ЮН	High-level output current	A port			-32	mA
	Lavida al autorita autorita	A port‡			64	
lOL	Low-level output current	B port			40	mA
TA	Operating free-air temperature		0		70	°C

[‡] Current duty cycle ≤ 50%, f ≥ 1 kHz



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electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN TYPT	MAX	UNIT	
VIK		V _{CC} = 3.15 V,	$V_{CC} = 3.15 \text{ V},$ $I_{J} = -18 \text{ mA}$		-1.2	٧	
		V _{CC} = MIN to MAX [‡] ,	l _{OH} =100 μA	V _{CC} - 0.2			
Vон	A port	V- 0.45.V	I _{OH} = -8 mA	2.4		٧	
		V _{CC} = 3.15 V	I _{OH} = - 32 mA	2			
			I _{OL} = 100 μA		0.2		
		V 045.V	I _{OL} = 16 mA		0.4		
VOL	A port	V _{CC} = 3.15 V	I _{OL} = 32 mA		0.5	V	
			I _{OL} = 64 mA		0.55		
	B port	V _{CC} = 3.15 V,	I _{OL} = 40 mA		0.4		
	Control pins	V _{CC} = 0 or MAX [‡] ,	V _I = 5.5 V		10	μА	
			V _I = 5.5 V		20		
l _l	A port§	V _{CC} = 3.45 V	V _I = V _{CC}		1		
				V _I = 0		-5	μА
	B port	V _{CC} = 3.45 V	VI = VCC		5		
			V _I = 0		-5		
	A port	., .	V _I or V _O = 0 to 4.5 V		100	μА	
off	B port	VCC = 0	V _I or V _O = 0 to 1.2 V		100		
	A port	V _{CC} = 3.15 V	V _I = 0.8 V	75		μА	
l(hold)			V _I = 2 V	-75			
	A port		V _O = 3 V		1	4	
^l OZH	B port	V _{CC} = 3.45 V	V _O = 1.2 V		10		
	CLKIN		V _O = 3 V		5	1	
	A port		V _O = 0.5 V		-1		
lozL	B port	V _{CC} = 3.45 V	V _O = 0.4 V		-10	μА	
	CLKIN	7	V _O = 0.5 V		-5	•	
	A port to B port						
lcc	B port to A port	V _{CC} = 3.45 V,	$I_{O}=0$,			mA	
	Outputs disabled	V _I = V _{CC} or GND					
∆lcc [¶]	-	V _{CC} = 3.45 V, A or control inputs at V _{CC} or GND	One input at 2.7 V,		1	mA	
Ci	Control pins	V _I = 3.15 V or 0		4		pF	
Cio	A port	V _O = 3.15 V or 0		10		pF	
Cio	B port	Per IEEE1194.0-1991			5	pF	



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCBS269 - MARCH 1993 - REVISED MARCH 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

			MIN	MAX	UNIT	
fclock	Clock frequency		0	150	MHz	
	Pulse duration					
t _W	Fulse duration	CLKAB or CLKBA high or low			ns	
		A before CLKAB↑	1.5		T	
		B before CLKAB↑	3			
		A before LEAB↓	0.5			
	Setup time	B before LEBA↓	1.5			
tsu		CEAB before CLKAB↑			ns	
		CEBA before CLKBA↑				
		CEAB before LEAB↓				
		CEBA before LEBA↓				
		A atter CLKAB↑	1	4		
		B after CLKAB↑	0			
		A after LEAB↓	2.5			
	Lield Con-	B after LEBA↓	2			
th	Hold time	CEAB after CLKAB↑			ns	
		CEBA after CLKBA↑				
		CEAB after LEAB↓			İ	
		CEBA after LEBA↓			İ	



SN74GTL16921 20-BIT FLIP-FLOP WITH GTL I/O LEVELS

SCBS313 - JULY 1993 - REVISED MARCH 1994

- EPIC-IIB™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Members of the Texas Instruments Widebus™ Family
- Provides GTL Signals Levels on Both inputs and Outputs
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74GTL16921 has 20 single-bit flip-flops which are designed to provide terminated GTL logic levels.

The device can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. The SN74GTL16921 provides true data at the Q outputs on the positive transition of the clock (CLK) input.

The output-enable (\overline{OE}) input can be used to place the outputs in a high state. The output-enable input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74GTL16921 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z

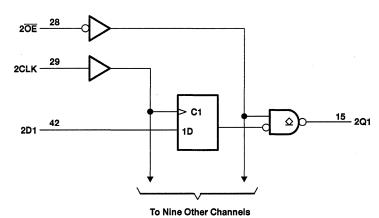
DGG OR DL PACKAGE (TOP VIEW)

		1 1		
10E	[] 1]1CLK
1Q1	[]2	5	55]1D1
1Q2		5	54	1D2
GND	[]4	5	3]GND
1Q3	5	5	52	1D3
1Q4				1D4
V_{CC}	[]7]v _{cc}
1Q5] 1D5
1Q6	9] 1D6
1Q7				1D7
GND	[] 11]GND
1Q8				1D8
1Q9				1D9
1Q10] 1D10
2Q1				2D1
2Q2				2D2
2Q3				2D3
GND	18			GND
2Q4				2D4
2Q5				2D5
2Q6				2D6
V_{CC}				V _{REF}
2Q7				2D7
2Q8	_			2D8
GND				GND
2Q9				2D9
2Q10				2D10
2 0E	28	2	9]2CLK

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To Nine Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Current into any output in the low state, IO	80 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > 0)	±50 mA
Continuous current through V _{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



PRODUCT PREVIEW

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PRODUCT PREVIEW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	3		3.6	٧
VREF	Supply voltage	2/3 V _{CC} – 2	2% 0.8	2/3 V _{CC} + 2%	V
۷ _I	Input voltage	0		VCC	V
۷он	High-level output voltage			3.6	٧
VIH	High-level input voltage	V _{REF} +50	mV		V
VIL	Low-level input voltage			V _{REF} - 50 mV	٧
lκ	Input clamp current			-18	mA
lol	Low-level output current			40	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

	PARAMETER	TES	TEST CONDITIONS		MAX	UNIT
٧ıĸ		V _{CC} = 3 V,	l _l = -18 mA		-1.2	V
VOL		V _{CC} = 3 V,	I _{OL} = 40 mA		0.4	٧
ı.		V _{CC} = 3 V	V _I = V _{CC}		5	
1		ACC = 2 A	V _I = 0		-5	μА
ЮН		V _{CC} = 3 V,	V _{OH} = 3.6 V			μA
la a	Outputs high	V _{CC} = 3 V,	I _O = 0,			mA
ICC	Outputs low	V _I = V _{CC} or GND	_			IIIA
Cį		Per IEEE1194.0-1991		4		pF
Co		Per IEEE1194.0-1991		6		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

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LVC MSI AND OCTALS

Features

- 0.8-μ EPIC-II™ CMOS process
- No input-diode clamp to V_{CC}
- Very low standby current (20 μA)
- −24-mA/24-mA drive current
- 2.7-V to 3.6-V V_{CC} range
- SOIC, EIAJ SSOP, and TSSOP packaging
- TI has established two worldwide alternate sources

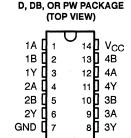
Benefits

- High-performance propagation delays as fast as 6.5 ns
- Saves power, extends battery life
- Drives transmission lines down to 50 Ω
- Fully characterized for unregulated battery operation
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

SN74LVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCAS279 - JANUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC00 performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

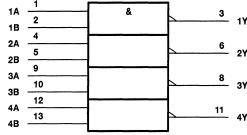
The SN74LVC00 is characterized for operation from -40°C to 85°C.

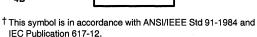
FUNCTION TABLE (each gate)

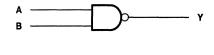
INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
L	Χ	, н
х	L	Н

logic symbol†

logic diagram, each gate (positive logic)







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NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
٧ı	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
lou	High-level output current		-12	mA	
ІОН	riigirievei output carrent	V _{CC} = 3 V		-24	
lo	Low-level output current	V _{CC} = 2.7 V		12	mA
lor	Low-level output current	V _{CC} = 3 V		24	111/
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	·	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLICATE		T _A = -40°C to 85°C		
PARAMETER	TEST CONDITIONS	vcc‡	MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	I _{OH} = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 MA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
lį	V _I = V _{CC} or GND	3.6 V		±5	μА
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF

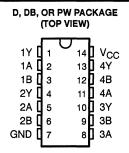
[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74LVC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCAS280 - JANUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
 Train No. (Content Content Process)
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

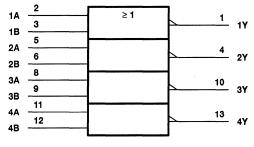
The SN74LVC02 is characterized for operation from -40°C to 85°C.

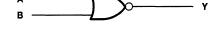
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
Α	В	Υ
Н	Χ	L
Х	Н	L
L	L	н

logic symbol†

logic diagram, each gate (positive logic)





EPIC is a trademark of Texas Instruments Incorporated.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): D package	
	0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ı	Input voltage		0	VCC	, V
Vo	Output voltage		0	VCC	٧
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	1 111/
loi	Low-level output current $ \frac{\text{V}_{\text{CC}} = 2.7 \text{ V}}{\text{V}_{\text{CC}} = 3 \text{ V}} $		12	mA	
IOL		V _{CC} = 3 V		24	111/4
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ů

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLIANCE	v _{cc} ‡	T _A = -40°C to 85°C		
PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	IOH = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		v
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
lj	V _I = V _{CC} or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μA
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)	
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1A 1 14 V _{CC}	
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y U 2 13 U 6A 2A U 3 12 U 6Y 2Y U 4 11 U 5A	
Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DD) and This Object One II Outline	3A [5 10] 5Y 3Y [6 9] 4A	
(DB), and Thin Shrink Small-Outline (PW) Packages	GND [7 8 4Y	

description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74LVC04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbolt

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
	0.5 V to 4.6 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
	–50 mA
	±50 mA
	±50 mA
	±100 mA
	: D package 1.25 W
	DB or PW package 0.5 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
۷Į	Input voltage		0	VCC	V
۷o	Output voltage		0	VCC	V
	High-level output current	V _{CC} = 2.7 V	`	-12	mA
ЮН	riigir-ievei output current	V _{CC} = 3 V		-24	IIIA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate	1	0	10	ns/V
TA	Operating free-air temperature	777	-40	85	ç

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = -40°C to	85°C	UNIT
PARAMETER	TEST CONDITIONS	v _{cc} ‡	MIN TYP	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	10 mA	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4		ľ
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = V _{CC} or GND	3.6 V		±5	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.6		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
	(INPOT)	(001701)	MIN	TYP	MAX	MIN	MAX	
t _{pd}	Α	Υ	1.5	3.8	6		7	ns

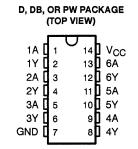
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per inverter	C _L = 50 pF,	f = 10 MHz	24	pF

EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process

- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \overline{A}$.

The SN74LVCU04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol†

2 1 1Y 3 4 2A 2Y 5 6 **3Y** ЗА 9 8 4A 11 10 5A **5Y** 12 13 6A **6Y**

logic diagram, each inverter (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V ₁ –	
Output voltage range, VO (see Note 1)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, IO (VO = 0 to VCC)	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): D package	1.25 W
DB or PW package	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VιΗ	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	V
۷o	Output voltage	,		VCC	V
lou	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	riigir-ievei output current	V _{CC} = 3 V		-24	IIIA
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	V _{CC} = 3 V			24	шх
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ô

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	,, ₊	T _A = -40°C to 85	°C UNIT
PANAMETER	TEST CONDITIONS	v _{cc} ‡	MIN MAX	T ONL
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Vari	I _{OH} = – 12 mA	2.7 V	2.2	\square \vee
VOH	IOH = - 12 IIIA	3 V	2.4	
	I _{OH} = - 24 mA	3 V	2	
	I _{OL} = 100 μA	MIN to MAX	0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V	0.4	V
	I _{OL} = 24 mA	3 V	0.55	
tı	V _I = V _{CC} or GND	3.6 V	±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	μА
Ci	V _I = V _{CC} or GND	3.3 V		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCAS283 - JANUARY 1993 - REVISED MARCH 1994

8 3Y

• EPIC™ (Enhanced-Performance Implanted D, DB, OR PW PACKAGE (TOP VIEW) **CMOS) Submicron Process** Typical V_{OLP} (Output Ground Bounce) V_{CC} 1A < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 1B 🛭 13 4B Typical V_{OHV} (Output V_{OH} Undershoot) 1Y 🗓 3 12 4A > 2 V at V_{CC} = 3.3 V, T_A = 25°C 2A 11 N 4Y Package Options Include Plastic 2B 🛮 5 10 3B Small-Outline (D), Shrink Small-Outline 9[] 3A 2Y 6 (DB), and Thin Shrink Small-Outline (PW)

description

Packages

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC08 performs the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74LVC08 is characterized for operation from -40°C to 85°C.

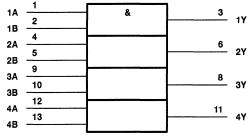
FUNCTION TABLE (each gate)

INP	JTS	OUTPUT
Α	В	Υ
Н	Н	Н
L	Х	L
Х	L	L

logic symbol†

logic diagram, each gate (positive logic)

GND 17



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): D pa	ckage 1.25 W
	r PW package 0.5 W
Storage temperature range	, ,

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		М	N	MAX	UNIT
VCC	Supply voltage	2	.7	3.6	٧
V _{IH}	High-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		2		V
VIL	Low-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	٧
٧ _I	Input voltage		0	VCC	٧
VO	Output voltage		0	VCC	V
lou	V _{CC} = 2.7 V		_	-12	mA
ЮН	High-level output current VCC = 3 V			-24	IIIA
lou	Low-level output current			12	mA
lOL	V _{CC} = 3 V			24	""
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		10	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	\ \ \ +	T _A = -40°C to 85°C		UNIT
PARAMETER	TEST CONDITIONS	vcc‡	MIN	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	10 mA	2.7 V	2.2		v
VOH	I _{OH} = -12 mA	3 V	2.4		, v
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
4	V _I = V _{CC} or GND	3.6 V		±5	μА
Icc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		20	μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF

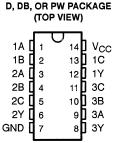
[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC10 TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284 - JANUARY 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This triple 3-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

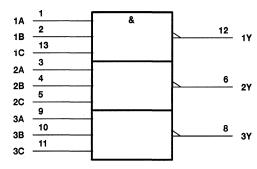
The SN74LVC10 performs the Boolean functions $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN74LVC10 is characterized for operation from -40°C to 85°C.

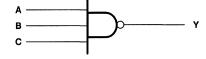
FUNCTION TABLE (each gate)

	INPUTS	OUTPUT	
Α	В	С	Y
Н	Н	Н	L
L	X	Χ	Н
Χ	L	Χ	H
Χ	Х	L	Н

logic symbol†



logic diagram, each gate (positive logic)





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{jK} ($V_j < 0$)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): D package	1.25 W
	0.5 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Vcc	Supply voltage	2.7	3.6	V
VIH	High-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage	0	VCC	٧
Vo	Output voltage	0	VCC	٧
la	High-level output current		-12	mA
ЮН	V _{CC} = 3 V		-24	IIIA
lo	Low-level output current		12	mA
lOL	V _{CC} = 3 V		24	111/
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEGT CONDITIONS		T _A = -40°C to 85°C		UNIT
	TEST CONDITIONS	v _{cc} ‡	MIN	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	lov. 10 mA	2.7 V	2.2		l _v
VOH	IOH = -12 mA	3 V	2.4]
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _I	V _I = V _{CC} or GND	3.6 V		±5	μА
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC14 HEX SCHMITT-TRIGGER INVERTER

SCAS285 - MARCH 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
 Typical V_{OLP} (Output Ground Bounce)
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)						
1A [1	14 V _{CC}				
1Y [2	13 6A				
2A [3	12 6Y				
2Y [4	11 5A				

description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74LVC14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol[†]

1A 1Y 4 2Y 2A 5 6 **3Y** 9 8 4A 4Y 11 10 5A 5Y 13 12 6A 6Y

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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SCAS285 - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V	to 4.6 V
Input voltage range, V ₁ 0.5 V	to 4.6 V
Output voltage range, V _O (see Note 1)	+ 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	:100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range –65°C t	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Vcc	Supply voltage	2.7	3.6	٧
VIH	High-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage	0	VCC	٧
VO	Output voltage	0	VCC	٧
lavi	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current VCC = 3 V		-24	IIIA
la.	Low-level output current		12	mA
lOL	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPITIONS		T _A = -40°C to 85°C		
PARAMETER	TEST CONDITIONS	Vcc‡	MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
M	J 10 mA	2.7 V	2.2		l _v
VOH	I _{OH} = – 12 mA	3 V	2.4		1 °
	I _{OH} = -24 mA	3 V	2		1
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = V _{CC} or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF

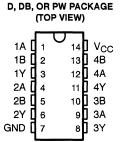
[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

SCAS286 - JANUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

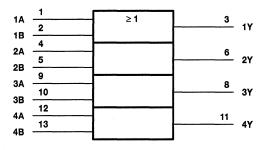
The SN74LVC32 performs the Boolean functions Y = A + B or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN74LVC32 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Х	Н
×	Н	Н
L	L	L

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)





SN74LVC32 **QUADRUPLE 2-INPUT POSITIVE-OR GATE**

SCAS286 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	
Output voltage range, VO (see Note 1)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air): D package	
	0.5 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
VCC	Supply voltage	2.7	3.6	٧
VIH	High-level input voltage V _{CC} = 2.7 V to 3.6	5 V 2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6	8 V	0.8	٧
VI	/ _I Input voltage			٧
VΟ	Output voltage	0	VCC	V
la	V _{CC} = 2.7 V		-12	mA
IOH	High-level output current V _{CC} = 3 V		-24	IIIA
la.	V _{CC} = 2.7 V		12	mA
lor	Low-level output current VCC = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = -40°0	UNIT	
PARAMETER	TEST CONDITIONS	v _{cc} ‡	MIN	MAX	ONIT
	$I_{OH} = -100 \mu A$	MIN to MAX	V _{CC} -0.2		
Va	I _{OH} = – 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		v
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
tį	V _I = V _{CC} or GND	3.6 V		±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS287 - JANUARY 1993 - REVISED MARCH 1994

U V_{CC}

2CLK

10 1 2PRE

Π2<u>Q</u>

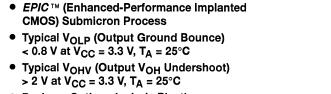
9 1 2Q

8

13 1 2CLR

12 D 2D

D. DB. OR PW PACKAGE (TOP VIEW)



1CLR [1D [] 2 1CLK 3 1PRE 4 Package Options Include Plastic 1Q 5 Small-Outline (D), Shrink Small-Outline 1Q П 6 (DB), and Thin Shrink Small-Outline (PW) GND 7 **Packages**

description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval. data at the D input may be changed without affecting the levels at the outputs.

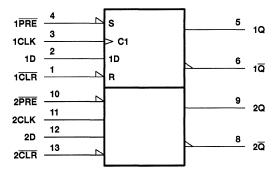
The SN74LVC74 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTI	PUTS
PRE	CLR	CLK	D	Q	O
L	Н	X	Х	Н	٦
Н	L	X	Χ	L	Н
L	L	Х	Χ	H [†]	H [†]
Н	Н	1	Н	Н	L
Н	Н	1	L	L	Н
Н	Н	L	Χ	Q ₀	\overline{Q}_0

[†]This configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

logic symbol‡



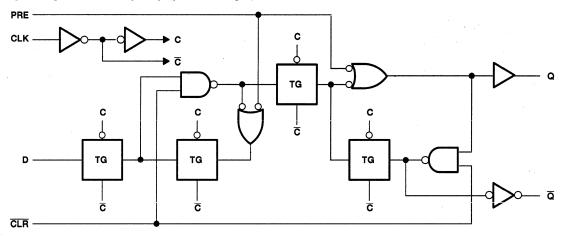
[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN74LVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS287 - JANUARY 1993 - REVISED MARCH 1994

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I	0.5 V to 4.6 V
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage	į.	2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage			VCC	V
۷o	Output voltage				٧
lau	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	nigri-level output current	V _{CC} = 3 V		-24	IIIA
1	Laveland authorit animont	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	MA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



SN74LVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS287 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T +	T _A = -40°C to	85°C	UNIT
PARAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	ONII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vall	IOH = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		'
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
Ч	V _I = V _{CC} or GND	3.6 V		±5	μА
Icc	$V_1 = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.5		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	MHz
	Pulse duration	PRE or CLR low	4		5		
t _W		CLK high or low	5		6		ns
	Catura times hadana CLIVA	Data	3		4		20
t _{su}	Setup time before CLK↑	PRE or CLR inactive	2		3		ns
th	Hold time, data after CLK↑		1		2		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1 TU.3 V		V	V _{CC} = 2.7 V		UNIT
	(IRFO1)	(001701)	MIN	TYP	MAX	MIN	MAX	
f _{max}			150			150		MHz
^t pd	CLK	Q or $\overline{\mathbb{Q}}$	1.5	3.5	9.2		10.2	ns
	PRE or CLR	Q OF Q	1.5	3.7	10.5		11.5	113

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

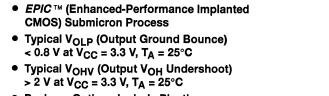
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 10 MHz	27	pF

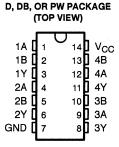


SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS288 - JANUARY 1993 - REVISED MARCH 1994



 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This dual quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC86 performs the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

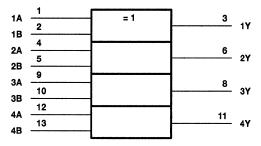
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN74LVC86 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
L L		L
L	Н	Н
Н	L	Н
Н	Н	L

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

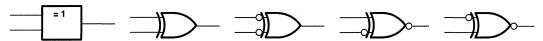
PRODUCT PREVIEW Information concerns products in the formative or



exclusive-OR logic

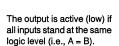
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

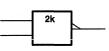


These are five equivalent exclusive-OR symbols valid for an 'LVC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT

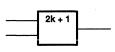


EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air):	D package 1.25 W
	DB or PW package 0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage			VCC	V
۷o	Output voltage				V
1	High-level output current	V _{CC} = 2.7 V		-12	A
ЮН		V _{CC} = 3 V		-24	mA
1		V _{CC} = 2.7 V		12	mA
lOL	Low-level output current V _{CC} = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS		T _A = -40°C to 85°C	UNIT	
PARAMETER	TEST CONDITIONS	vcct	MIN MAX	JUNII	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	10 = 4	2.7 V	2.2] ,	
VOH	I _{OH} = – 12 mA	3 V	2.4	7 °	
	I _{OH} = -24 mA	3 V	2	1	
	I _{OL} = 100 μA	MIN to MAX	0.2		
VOL	I _{OL} = 12 mA	2.7 V	0.4	v	
•	I _{OL} = 24 mA	3 V	0.55		
l _l	V _I = V _{CC} or GND	3.6 V	±5	μА	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20	μA	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	μА	
C _i	V _I = V _{CC} or GND	3.3 V		pF	

TFor conditions shown as MIN of MAX, use the appropriate values under recommended operating conditions.



SN74LVC112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SCAS289 - JANUARY 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1CLK 1 16 V _{CC} 1K 2 15 1CLR
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1K 2 15 1CLR 1J 3 14 2CLR 1PRE 4 13 2CLK
 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline 	1Q 0 5 12 2K 1Q 0 6 11 0 2J
(DB), and Thin Shrink Small-Outline (PW) Packages	2Q 0 7 10 2PRE GND 0 8 9 0 2Q

description

This dual negative-edge-triggered J-K flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. The SN74LVC112 can perform as a toggle flip-flop by tying J and K high.

The SN74LVC112 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUT	PUTS	
PRE	CLR	CLK	J	K	Q	Q
L	Н	Х	Х	Х	Н	L
н	L	Х	Χ	X	L	н
L	L	X	Χ	Х	нt	H†
н	Н	\downarrow	L	L	Q ₀	\overline{Q}_0
Н	Н	\downarrow	Н	L	н	L
Н	Н	\downarrow	L	Н	L	н
Н	Н	\downarrow	Н	Н	Toggle	
Н	Н	Н	Х	Х	Q_0	\overline{Q}_0

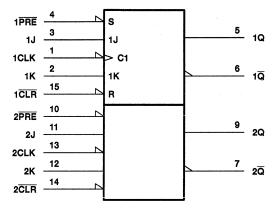
[†] The output levels in this configuration may not meet the minimum levels for VOH. Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.



SN74LVC112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

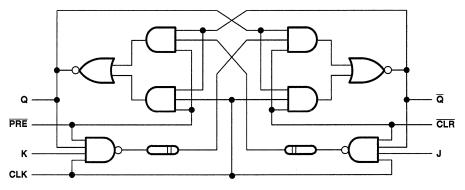
SCAS289 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V ₁ 0.5 V to 4.6 V
Output voltage range, V _O (see Note 1)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at $T_A = 55$ °C (in still air): D package
DB package 0.55 W
PW package 0.5 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.



SN74LVC112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SCAS289 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I Input voltage		0	Vcc	٧	
٧o	Output voltage		0	Vcc	٧
la	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	11114
1	Laveland autorit aumant	V _{CC} = 2.7 V		12	4
IOL	DL Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = -40°C to 85°C		UNIT	
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vall	I _{OH} = – 12 mA	2.7 V	2.2		v	
Voн	IOH = - 12 IIIA	3 V	2.4		V	
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	I _{OL} = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
lį	V _I = V _{CC} or GND	3.6 V		±5	μА	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
C _o	VO = VCC or GND	3.3 V			pF	

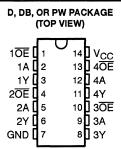
[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS290 - JANUARY 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

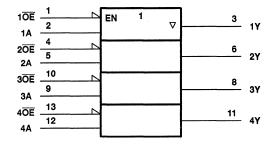
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVC125 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

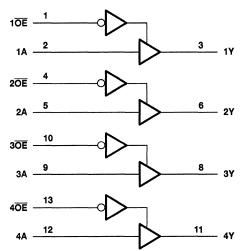
INPUTS		OUTPUT
ŌĒ	Α	Υ
L	Н	Н
L	L	L
н	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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TEXAS INSTRUMENTS

SN74LVC125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS290 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Output voltage range, V _O (see Note 1)	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): D package	ge 1.25 W
DB or P\	V package 0.5 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Vcc	Supply voltage	2.7	3.6	٧
VIH	High-level input voltage V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage	0	VCC	٧
Vο	Output voltage	0	VCC	٧
	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA
ЮН			-24	IIIX
1	OL Low-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		12	mA
IOL			24	111/
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	\ ,, ₊	T _A = -40°C to 85°C		UNIT	
PARAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT	
	l _{OH} = -100 μA	MIN to MAX	X V _{CC} -0.2			
Vou	I _{OH} = - 12 mA	2.7 V	2.2		V	
Voн	IOH = - 12 IIIA	3 V	2.4		V	
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
V_{OL}	I _{OL} = 12 mA	2.7 V		0.4	v	
	I _{OL} = 24 mA	3 V		0.55		
lj .	V _I = V _{CC} or GND	3.6 V		±5	μA	
loz	VO = VCC or GND	3.6 V		±10	μА	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
Со	V _O = V _{CC} or GND	3.3 V			рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS339 - MARCH 1994

 EPIC ™ (Enhanced-Performance Implanted
CMOS) Submicron Process
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C

- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)					
10E [1 0	14 h	Vcc		
1A 🗓	2	13	V _{CC} 40E		
1Y [12			
20E 🚺	4	11 🛭	4Y		
2A 🚺		10]]	30E		
2Y [6	9	ЗА		
GND [7	вħ	3Y		

description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC126 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

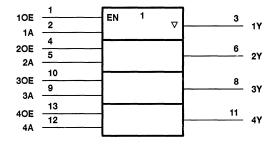
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVC126 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

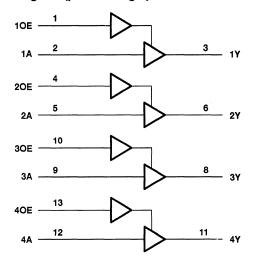
INP	UTS	OUTPUT
OE	Α	Y
Н	Н	Н
н	L	L
L	Х	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74LVC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS339 - MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): D package	
DB or PW package	0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Vcc	Supply voltage	2.7	3.6	V .
VIH	High-level input voltage V _{CC} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷Į	Input voltage	0	VCC	٧
٧o	Output voltage	0	VCC	V
lou	High-level output current		-12	mA
ЮН	V _{CC} = 3 V		-24	111/4
lo	Low-level output current		12	mA
lOL	V _{CC} = 3 V		24	""
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS SCAS339 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

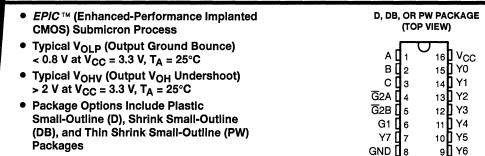
PARAMETER	TEST CONDITIONS		T _A = -40°0	UNIT	
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	IOH = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4]
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V	i		рF

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC137 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

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description

This 3-line to 8-line decoder/demultiplexer with latches on three address inputs is designed for 2.7-V to 3.6-V $V_{\rm CC}$ operation.

The SN74LVC137 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch-enable ($\overline{G}2A$) input is low, the SN74LVC137 acts as a decoder/demultiplexer. when $\overline{G}2A$ transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored provided $\overline{G}2A$ remains high. The output-enable (G1 and $\overline{G}2B$) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high is G1 is low or $\overline{G}2$ is high.

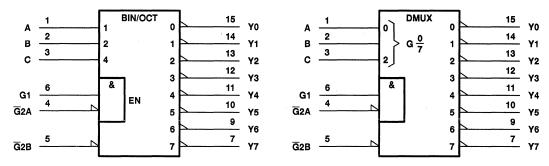
The SN74LVC137 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

LATCH ENABLE	OUTPUT- ENABLE		SELECT INPUTS			OUTPUTS							
G2A	G1	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Х	Н	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	L	X	Х	Χ	Χ	н	Н	Н	Н	Н	Н	Н	н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	н
L	Н	L	L	L	Н	н	L	Н	Н	Н	Н	Н	н
L	Н	L	L	Н	L	н	Н	L	Н	Н	Н	Н	н
L	Н	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	Н
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	н
L	Н	L	Н	L	H.	Н	Н	Н	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	н	Н	Н	Н	Н	Н	L	Н
L	Н	L	Н	Н	Н	н	Н	Н	Н	Н	Н	Н	L
Н	H	L	Х	Х	Х	Outputs corresponding to stored address = L; all other outputs = H							

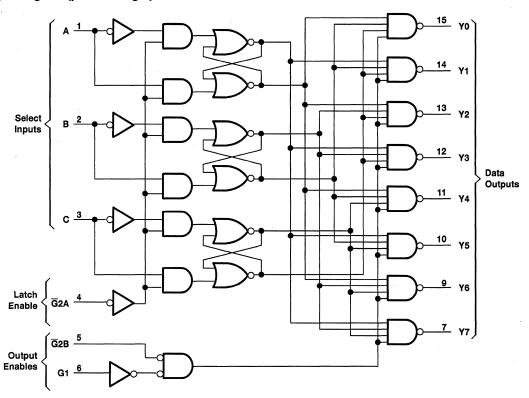


logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN74LVC137 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340 - MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		 -0.5 V to 4.6 V
Input voltage range, V ₁		
Output voltage range, VO (see Note 1)		
Input clamp current, $I_{IK}(V_I < 0)$		 –50 mA
Output clamp current, IOK (VO < 0 or VO > VCC))	 ±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$.		 ±50 mA
Continuous current through V _{CC} or GND		 ±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still		
	PW package	 0.5 W
Storage temperature range		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage				V
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	VCC	٧
٧o	Output voltage		0	VCC	٧
	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	V _{CC} = 3 V	V _{CC} = 3 V		-24	ША
la.	Low level output ourrent	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current V _{CC} = 3 V			24	ША
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



SN74LVC137 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T	T _A = -40°C to 85°C	UNIT		
PARAMETER	TEST CONDITIONS	vcct	MIN MAX	UNII		
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vou	I _{OH} = – 12 mA	2.7 V	2.2	V		
Voн	10H = - 12 11h	3 V	2.4	ľ		
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	MIN to MAX	0.2			
VOL	$I_{OL} = 12 \text{ mA}$	2.7 V	0.4] v		
	$I_{OL} = 24 \text{ mA}$	3 V	0.55			
lį	$V_I = V_{CC}$ or GND	3.6 V	±5	μA		
loz	$V_O = V_{CC}$ or GND	3.6 V	±10	μА		
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20	μА		
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	μА		
C _i	V _I = V _{CC} or GND	3.3 V		pF		
Co	V _O = V _{CC} or GND	3.3 V		pF		

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

GND I 8

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9**∏** Y6

 EPIC™ (Enhanced-Performance Implanted D. DB. OR PW PACKAGE (TOP VIEW) **CMOS) Submicron Process** Typical V_{OLP} (Output Ground Bounce) 16 VCC < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 15 YO B 🛛 2 Typical V_{OHV} (Output V_{OH} Undershoot) С∏з 14 Y1 $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ G2A [] 4 13**∏** Y2 Package Options Include Plastic G2B [] 5 12 Y3 Small-Outline (D), Shrink Small-Outline G1 [] 6 11 Y4 (DB), and Thin Shrink Small-Outline (PW) Y7 🛮 7 10 Y5 **Packages**

description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LVC138 is characterized for operation from -40°C to 85°C.

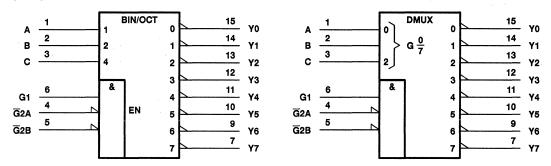
FUNCTION TABLE

ENA	BLE INF	PUTS	SEL	ECT INF	UTS				OUT	PUTS			
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Х	X	н	Х	Χ	Χ	н	Н	Н	Н	Н	Н	Н	Н
L	Х	Х	Х	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	Н	Н	· L	Н	Н	Н	Н	H	Н
Н	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	L



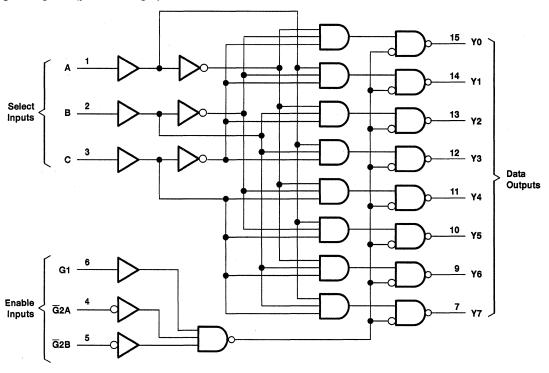
SCAS291 - MARCH 1993 - REVISED MARCH 1994

logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
VCC	Supply voltage	2.7	3.6	٧
VIH	High-level input voltage V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
Vį	Input voltage	0	VCC	٧
VO	Output voltage	0	VCC	٧
lavi	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current V _{CC} = 3 V		-24	IIIA
1	V _{CC} = 2.7 V		12	mA
lOL	DL Low-level output current VCC = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



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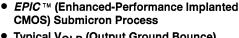
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT CONDITIONS		T _A = -40°0	C to 85°C	UNIT		
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII		
	lOH = -100 μA	MIN to MAX	V _{CC} -0.2				
Voн	IOH = - 12 mA	2.7 V	2.2		V		
VOH	UH 12 11/5	3 V	2.4		V		
	I _{OH} = -24 mA	3 V	2				
	i _{OL} = 100 μA	MIN to MAX		0.2			
VOL	I _{OL} = 12 mA	2.7 V		0.4 V			
	i _{OL} = 24 mA	3 V		0.55			
-	V _I = V _{CC} or GND	3.6 V		±5	μΑ		
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ		
<u>-</u> cc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА		
ΔlCC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} = 0.6 V, Other inputs at V _{CC} or GND			500	μΑ		
C _i	V _I = V _{CC} or GND	3.3 V			pF		
Co	VO = VCC or GND	3.3 V			pF		

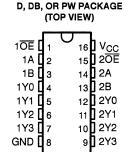
[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS341 - MARCH 1994



- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This dual 2-line to 4-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC139 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

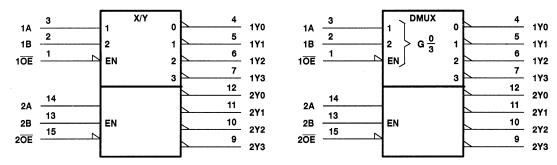
The device comprised of two individual 2-line to 4-line decoders in a single package. The active-low output-enable (\overline{OE}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN74LVC139 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS			OUTPUTS		
ŌĒ	SEL	ECT		0011	-013	
OE	В	Α	. Y0	Y1	Y2	Y 3
Н	Х	Х	Н	Н	Н	Н
L	L	L	L	Н	Н	н
L	L	Н	Н	L	Н	н
L	Н	L	Н	Н	L	н
L	Н	Н	Н	Н	Н	L

logic symbols (alternatives)†

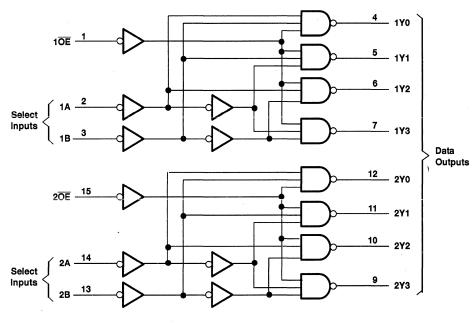


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. EPIC is a trademark of Texas Instruments Incorporated.



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V ₁ 0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)
Input clamp current, $I_{ K }(V_1 < 0)$
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) ±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$ ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air): D package
DB package 0.55 W
PW package
Storage temperature range ——65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS341 - MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷Į	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	٧
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	nigh-level output current	V _{CC} = 3 V		-24	I IIIA
1	Laveland aritmet arrespt	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS	T _A = -40°		C to 85°C	UNIT	
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII	
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2			
V	Jan. 10 mA	2.7 V	2.2		l _v	
VOH	I _{OH} = - 12 mA	3 V	2.4]	
	I _{OH} = -24 mA	3 V	2		1	
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	I _{OL} = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
l ₁	V _I = V _{CC} or GND	3.6 V		±5	μА	
loz	V _O = V _{CC} or GND	3.6 V		±10	μА	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
ΔICC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
Co	V _O = V _{CC} or GND	3.3 V			рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292 - JANUARY 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	A/B 1 16 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A [2 15] G 1B [3 14] 4A 1Y [4 13] 4B
 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline 	2A
(DB), and Thin Shrink Small-Outline (PW) Packages	2Y

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC157 features a common strobe $(\overline{\mathbf{G}})$ input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

The SN74LVC157 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

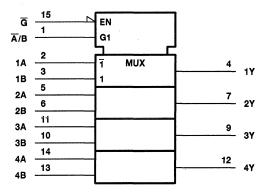
	INPU	OUTPUT		
Ğ	Ā/B	Α	В	Υ
Н	Х	Х	Х	L
L	L	L	Х	L
L	L	Н	X	Н
L	Н	Χ	L	L
L	Н	Χ	Н	н



SN74LVC157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

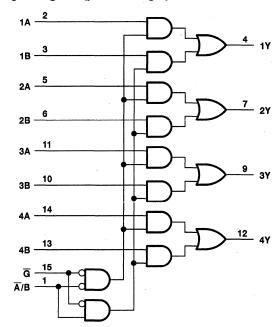
SCAS292 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): D package	
· · · · · · · · · · · · · · · · · · ·	
PW package	
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

SN74LVC157 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage V _{CC}	= 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage V _{CC}	= 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage		0	VCC	V
Vo	Output voltage	-	0	VCC	٧
lau	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $; = 2.7 V		-12	mA
ЮН		; = 3 V		-24	ША
lo.	Low-level output current	; = 2.7 V		12	mA
lOL	V _{CC}	= 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	., .	T _A = -40°C		UNIT
PANAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
	i _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	la 10 mA	2.7 V	2.2		V
VOH	IOH = - 12 mA	3 V	2.4]
	I _{OH} = -24 mA	3 V	2]
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	7 v
	I _{OL} = 24 mA	3 V			
11	V _I = V _{CC} or GND	3.6 V			μА
loz	V _O = V _{CC} or GND	3.6 V			μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

GND [] 8

9 3Y

SCAS342 - MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	Ā/B 1 16 V _{CC}	
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A U 2 15 U G 1B U 3 14 U 4A 1Y U 4 13 U 4B	
 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline 	2A [5 12] 4Y 2B [6 11] 3A	
(DB), and Thin Shrink Small-Outline (PW) Packages	2Y 7 10 3B	

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC158 features a direct strobe $\overline{(G)}$ input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The SN74LVC158 provides inverted data.

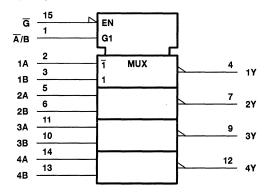
The SN74LVC158 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPU	OUTPUT		
G	Ā/B	Α	В	Y
Н	X	Х	Х	Н
L	L	L	X	н
L	L	Н	Х	L
L	Н	X	L	н
L	Н	Х	Н	L

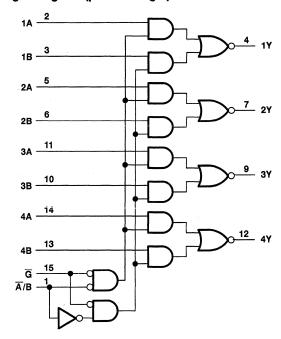


logic symbol†



† This symbol is in accordance with ANSI/IFEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
nput voltage range, V ₁
Output voltage range, V_O (see Note 1)
nput clamp current, $I_{ K }(V_{ }<0)$
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$ ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): D package
DB package
PW package 0.5 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

SN74LVC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS342 - MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VιΗ	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage		0	VCC	V
Vo	Output voltage		0	Vcc	٧
	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	ш
1	Level authorit aumant	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS		T _A = -40°C	T _A = -40°C to 85°C	
PARAMETER	TEST CONDITIONS	v _{cc} t	MIN MAX		UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
M	10 10 1	2.7 V	2.2		v
VOH	IOH = - 12 mA	3 V	2.4		\ \
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	\ \
	I _{OL} = 24 mA	3 V			
İį	V _I = V _{CC} or GND	3.6 V			μA
loz	V _O = V _{CC} or GND	3.6 V			μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC240 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS293 - JANUARY 1993 - REVISED MARCH 1994

 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	10E 1 20 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A1
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	2Y3 5 16 1Y2 1A3 6 15 2A3
(DB), and Thin Shrink Small-Outline (PW) Packages	2Y2
description	2Y1 9 12 1Y4 GND 10 11 2A1

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LVC240 is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

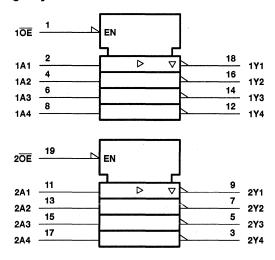
The SN74LVC240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	L
L	L	н
н	Χ	Z

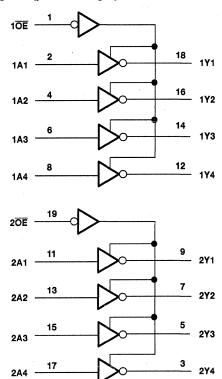


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	/ to 4.6 V
Input voltage range, V ₁ 0.5 \	/ to 4.6 V
Output voltage range, V _O (see Note 1)	c + 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0)$	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	. 0.6 W
DW package	. 1.6 W
PW package	. 0.7 W
Storage temperature range	to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
۷ін	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
la	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
IOH		V _{CC} = 3 V		-24] ""
1	Law layer autout aureant	V _{CC} = 2.7 V		12	1
lOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDI	TIONO		T _A = -40°C to 85°C		UNIT
PARAMETER	TEST CONDI	TIONS	v _{cc} †	MIN	MAX	UNIT
	IOH = -100 μA		MIN to MAX	V _{CC} -0.2		
V		2.7 V	2.2		v	
VOH	I _{OH} = - 12 mA		3 V	2.4		V
	I _{OH} = - 24 mA		3 V	2		
	I _{OL} = 100 μA		MIN to MAX		0.2	
VOL	I _{OL} = 12 mA		2.7 V		0.4	٧
	I _{OL} = 24 mA		3 V		0.55	
l _l	V _I = V _{CC} or GND		3.6 V		±5	μΑ
loz	V _O = V _{CC} or GND		3.6 V		±10	μΑ
lcc	V _I = V _{CC} or GND, I _O	= 0	3.6 V		20	μА
ΔlCC	V _{CC} = 3 V to 3.6 V, Or Other inputs at V _{CC} or GND	ne input at V _{CC} – 0.6 V,			500	μА
Ci	V _I = V _{CC} or GND		3.3 V			pF
Co	VO = VCC or GND		3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC241 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS343 - MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

(TOP VIEW) 1OE 20 VCC 1A1 [] 19**[]** 20E 2Y4 🛮 3 18 T 1Y1 1A2 🛮 4 17 1 2A4 2Y3 [**∏** 1Y2 5 16 1A3 **[**] 6 15**∏** 2A3 2Y2 17 14**∏** 1Y3 1A4 **[**] 8 13 2A2 2Y1 **[**] 9 12 1 1Y4

11 T 2A1

GND Π 10

DB. DW. OR PW PACKAGE

description

This octal buffer/line driver is designed for 2.7-V to $3.6\text{-V}\ \text{V}_{CC}$ operation.

The SN74LVC241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'LVC240 and 'LVC244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{OE} (active-low output-enable) inputs, and complementary \overline{OE} inputs.

The SN74LVC241 is organized as two 4-bit line drivers with separate output-enable ($1\overline{OE}$, 2OE) inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVC241 is characterized for operation from -40°C to 85°C.

FUNCTION TABLES

INPL	JTS	ОИТРИТ
1OE	1A	1Y
L	Н	Н
L	L	L
Н	Χ	Z

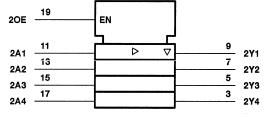
INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
н	L	L
L	Х	Z



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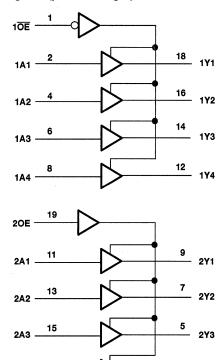
logic symbol†

10E ΕN 18 ∇ 1Y1 1A1 4 16 1A2 1Y2 14 1A3 1Y3 8 12 1Y4 1A4



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ı	Input voltage		0	VCC	٧
۷o	Output voltage		0	VCC	٧
lovi	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
ЮН		V _{CC} = 3 V		-24	IIIA
1	Lave lavel authorit auswant	V _{CC} = 2.7 V		12	A
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS		T _A = -40°C	to 85°C	UNIT	
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX		
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2			
V	Jan. 10 mA	2.7 V	2.2		l v	
VOH	IOH = - 12 mA	3 V	2.4		· ·	
	I _{OH} = -24 mA	3 V	2		ļ	
	I _{OL} = 100 μA	MIN to MAX		0.2		
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
l _l	V _I = V _{CC} or GND	3.6 V		±5	μА	
loz	V _O = V _{CC} or GND	3.6 V		±10	μА	
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
Co	V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS414 - NOVEMBER 1992 - REVISED MARCH 1994

11 2A1

DB, DW, OR PW PACKAGE • EPIC™ (Enhanced-Performance Implanted (TOP VIEW) CMOS) Submicron Process Typical V_{OLP} (Output Ground Bounce) 20 VCC 10E | 1 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 1A1 [19**∏** 2OE Typical V_{OHV} (Output V_{OH} Undershoot) 18 1Y1 2Y4 [] 3 $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ 1A2 17**∏** 2A4 • Package Options Include Plastic 2Y3 1 5 16 1Y2 Small-Outline (DW), Shrink Small-Outline 1A3 **[**] 6 15 T 2A3 (DB), and Thin Shrink Small-Outline (PW) 14 1Y3 2Y2 🛮 **Packages** 1A4 **[** 8 13 2A2 2Y1 19 12 1Y4

description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

GND [

The SN74LVC244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

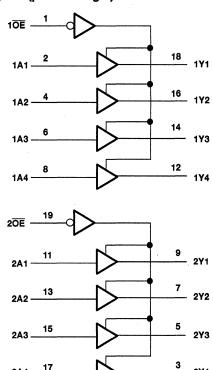
INP	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
н	X	Z

SCAS414 - NOVEMBER 1992 - REVISED MARCH 1994

logic symbol†

10E ΕN 18 D ∇ 1Y1 4 16 1A2 1Y2 6 14 1A3 **1Y3** 8 12 1Y4 2OE ΕN 11 9 \triangleright V 2A1 2Y1 7 13 2A2 2Y2 15 5 2A3 2Y3 17 3 2A4 2Y4

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V ₁) –0.5 V to 4.6 V
Output voltage range, V _O (see Note 1)
Input clamp current, $I_{ K }(V_1 < 0)$ — 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I_O ($V_O = 0$ to V_{CC})
Continuous current through V _{CC} or GND pins
Maximum power dissipation at TA = 55°C (in still air): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range ——65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷Į	Input voltage		0	VCC	٧
٧o	Output voltage		0	VCC	V
lou	V _{CC} = 2.7 V			-12	mA
ЮН	High-level output current VCC = 3 V		-24	111/4	
lai	V _{CC} = 2.7 V			12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	MA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T _A = -40°0	C to 85°C	UNIT
PARAMETER	TEST CONDITIONS	v _{CC} †	MIN T	YP MAX	ONII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	10	2.7 V	2.2		v
VOH	IOH = - 12 mA	3 V	2.4		· •
	!OH = - 24 mA	3 V	2		
	i _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.0 One input at V _{CC} – 0.0	3 V,		500	μА
Ci	V _I = V _{CC} or GND	3.3 V		3	pF
Co	V _O = V _{CC} or GND	3.3 V		3.5	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INPO1)		MIN	MAX	MIN	MAX	
^t pd	A	Y	1.5	7		8	ns
t _{en}	ŌĒ	Υ	1.5	8		9.2	ns
^t dis	ŌĒ	Y	1.5	7.5		8.5	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

SN74LVC244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS414 - NOVEMBER 1992 - REVISED MARCH 1994

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT	
Cnd Power dissipation capacitance per buffer/driver	Outputs enabled	Cı = 50 pF.	f = 10 MHz	20	рF	
Cpd	r ower dissipation capacitatice per buller/driver	Outputs disabled	CL = 50 pr,	1 = 10 1/1/12	2	PΓ



SN74LVC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS218B - JANUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

(TOP VIEW) DIR 🛮 Vcc A1 🛮 2 19 🛛 ŌĒ A2 18**∏** B1 **A3 1** B2 Пвз **A4** 16 П в4 **A5** 14 B5 A6 Α7 13 N B6 12 B7 **A8 B8 GND** 11

DB, DW, OR PW PACKAGE

description

This octal bus transceiver is designed for 2.7-V to $3.6\text{-V}\ \text{V}_{CC}$ operation.

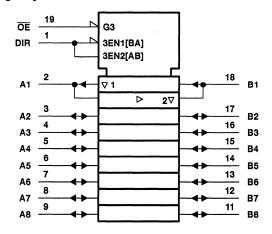
The SN74LVC245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

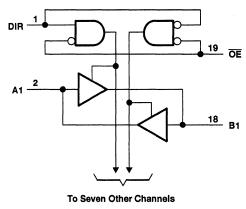
	INP	INPUTS OPERATION			
	ŌĒ	DIR	OPERATION		
I	L	L	B data to A bus		
	L	Н	A data to B bus		
	Н	Х	Isolation		

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage	ply voltage			٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	/ _I Input voltage		0	VCC	٧
۷o	Output voltage		0	VCC	٧
lou	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	IIIA
la.	Law layed a day day and a summand	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	+	T _A = -40°C to 85°C			UNIT	
		TEST CONDITIONS	v _{CC} †	MIN	TYP	MAX	UNII	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2				
		la 10 mA	2.7 V	2.2			v	
VOH		I _{OH} = - 12 mA	3 V	2.4			V	
		I _{OH} = -24 mA	3 V	2				
		I _{OL} = 100 μA	MIN to MAX			0.2		
VOL		I _{OL} = 12 mA	2.7 V			0.4] v	
		I _{OL} = 24 mA	3 V			0.55		
lį		V _I = V _{CC} or GND	3.6 V			±5	μА	
loz‡		VO = VCC or GND	3.6 V			±10	μА	
Icc		$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V			20	μА	
ΔlCC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND				500	μА	
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		3		pF	
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V		4		рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1 ± U.3 V		V _{CC} =	2.7 V	UNIT
	(114701)	(001701)	MIN	MÁX	MIN	MAX	
^t pd	A or B	B or A	1.5	7		8	ns
t _{en}	ŌĒ	A or B	1.5	9		10	ns
^t dis	ŌĒ	A or B	1.5	8		9	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST C	ONDITIONS	TYP	UNIT
<u> </u>	Payer discination canaditance per transcriver	Outputs enabled	C: 50 pF	f ≈ 10 MHz	25	,E
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	CL = 50 pF,	I ≈ IU IVI⊓Z	2	pF

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC4245 OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

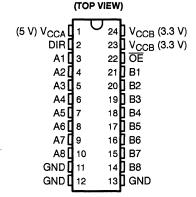
SCAS375 - MARCH 1994



- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} which is set at 3.3 V, and A port has V_{CCA} which is set to operate at 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice-versa.



DB. DW. OR PW PACKAGE

The SN74LVC4245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The pinout of the SN74LVC4245 allows the designer to switch to a normal all 3.3-V or all 5-V 20-pin '245 device without relaying out the board. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245 to achieve the conventional '245 layout.

The SN74LVC4245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

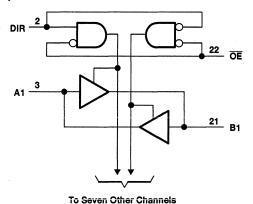
I ONOTION TABLE						
INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Χ	Isolation				



SN74LVC4245 OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS375 - MARCH 1994

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5 V (unless otherwise noted)

Supply voltage range, V _{CCA}	0.5 V to 6 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CCA} + 0.5 V
Output voltage range, VO (see Note 1)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CCA}$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CCA})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CCA})	
Continuous current through V _{CCA} or GND	±100 mA

NOTE 1: This value is limited to 6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 3.3 V (unless otherwise noted)[†]

Supply voltage range, V _{CCB}	-0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 2)	-0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Note 2)	to V _{CCB} + 0.5 V
Output voltage range, VO (see Note 2)	to V _{CCB} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CCB})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CCB})	±50 mA
Continuous current through V _{CCB} or GND	±100 mA

NOTE 2: This value is limited to 4.6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5 V or for V_{CCB} at 3.3 V (unless otherwise noted)[†]

Maximum power dissipation at T _A = 55°C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range –65°C t	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SN74LVC4245 OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS SCAS375 - MARCH 1994

recommended operating conditions for $V_{\mbox{CCA}}$ at 5 V (see Note 3)

		MIN	NOM	MAX	UNIT
VCCA	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	V
VI	Input voltage	0		VCCA	V
Vo	Output voltage	0		VCCA	V
ЮН	High-level output current			-24	mA
lOL	Low-level output current			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	ns/V
TA	Operating free-air temperature	-40		85	°C

recommended operating conditions for $V_{\mbox{\scriptsize CCB}}$ at 3.3 V (see Note 3)

			MIN	MAX	UNIT
VCCB	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CCB} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CCB} = 2.7 V to 3.6 V		8.0	٧
VI	Input voltage		0	VCCB	٧
Vo	Output voltage		0	VCCB	٧
lau	High-level output current	V _{CCB} = 2.7 V		-12 mA	mA
ЮН		V _{CCB} = 3 V		-24] "''
la.	Law law al a shauk a sweet	V _{CCB} = 2.7 V		12	mA
IOL	Low-level output current	V _{CCB} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused of floating pins (input or I/O) must be held high or low.



SN74LVC4245 OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS375 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range for $V_{CCA} = 5 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		VCCB	MIN	MAX	UNIT
		I _{OH} = -100 μA		4.5 V	4.3		V
\/				5.5 V	5.3	,	
VOH		Jan. 24 mA		4.5 V	3.7		V
		$I_{OH} = -24 \text{ mA}$		5.5 V	4.7		
		I _{OL} = 100 μA		4.5 V		0.2	٧
\/-·				5.5 V		0.2	
VOL		I _{OL} = 24 mA		4.5 V		0.55	
1				5.5 V		0.55	
1 ₁	Control pins	VI = VCCA or GND		5.5 V		5	μА
loz†	A or B ports	VO = VCCA or GND		5.5 V			μА
ICC		$V_I = V_{CCA}$ or GND, $I_O = 0$		5.5 V			μА
Δlcc [‡]		One input at 3.4 V, Other in	nputs at V _{CCA} or GND				μА
Ci	Control inputs	VI = V _{CCA} or GND		5 V			pF
Cio	A or B ports	VO = VCCA or GND		5 V			pF

electrical characteristics over recommended operating free-air temperature range for $V_{CCB} = 3.3 \text{ V}$ (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{CCB} §	MIN MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
		10 10	2.7 V	2.2	v
∨он		IOH = -12 mA	3 V	2.4	, v
		I _{OH} = -24 mA	3 V	2	
		I _{OL} = 100 μA	MIN to MAX	0.2	
VOL		I _{OL} = 12 mA	2.7 V	0.4	V
		I _{OL} = 24 mA	3 V	0.55	
lį	Control pins	V _I = V _{CCB} or GND	3.6 V	. 5	μА
loz†		VO = VCCB or GND	3.6 V		μА
Icc		$V_I = V_{CCB}$ or GND, $I_O = 0$	3.6 V		μА
Δlcc [‡]		V _{CCB} = 3 V to 3.6 V, One input at V _{CCB} – 0.6 V, Other inputs at V _{CCB} or GND			μА
Ci	Control inputs	V _I = V _{CCB} or GND	3.3 V		pF
Cio	A or B ports	VO = VCCB or GND	3.3 V		pF

[†] For I/O ports, the parameter IOZ includes the input leakage current.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCCB.

[§] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS294 - JANUARY 1993 - REVISED MARCH 1994

 EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	A/B 1 16 V _{CC} 1A 2 15 OE	
 Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A 2 15 OE 1B 3 14 4A 1Y 4 13 4B	
 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline 	2A	
(DB), and Thin Shrink Small-Outline (PW) Packages	2Y 7 10 3B GND 8 9 3Y	

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

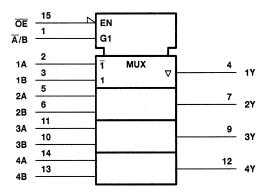
The SN74LVC257 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output enable (\overline{OE}) input is at a high logic level.

The SN74LVC257 is characterized for operation from -40°C to 85°C.

FUNCTION T	VDI C

	OUTPUT			
ŌĒ	A/B	Α	В	Y
Н	Х	Х	Х	Z
L	L	L	X	L
L	L	Н	X	н
L	Н	Χ	L	L
L	Н	Χ	Н	н

logic symbol†



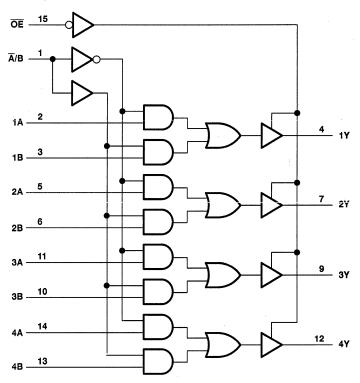
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN74LVC257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS294 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –().5 V to 4.6 V
Input voltage range, V ₁ –(
Output voltage range, V _O (see Note 1)	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range6	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS SCAS294 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	VCC	٧
٧o	Output voltage		0	Vcc	V
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	
la.		V _{CC} = 2.7 V		12	
lOL	Low-level output current V _{CC} = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	+	T _A = -40°C to 85°C		LINUT
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vall	I _{OH} = - 12 mA	2.7 V	2.2		v
Voн	IOH = - 12 IIIA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μA
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	$V_O = V_{CC}$ or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS345 - MARCH 1994

 EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	A/B 1 16 V _{CC} 1A 2 15 OE
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A [2 15] OE 1B [3 14] 4A 1Y 4 13] 4B
 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline 	2A
(DB), and Thin Shrink Small-Outline (PW) Packages	2Y 0 7 10 3B GND 0 8 9 3Y

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

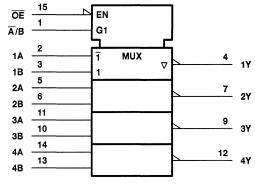
The SN74LVC258 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output enable (\overline{OE}) input is at a high logic level.

The SN74LVC258 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	OUTPUT			
OE	A/B	Α	В	Υ
Н	Х	Х	Х	Z
L	L	L	X	н
L	L	Н	X	L
L	Н	Χ	L	н
L	Н	Χ	Н	L

logic symbol†

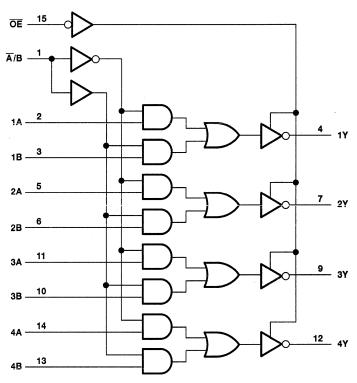


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SCAS345 - MARCH 1994

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V ₁
Output voltage range, V _O (see Note 1)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air): D package
DB package
PW package 0.5 W
Storage temperature range ————————————————————————————————————

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.



SN74LVC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS345 - MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage			Vcc	V
VΟ	Output voltage				V
1	High-level output current $ \frac{\text{V}_{\text{CC}} = 2.7 \text{ V}}{\text{V}_{\text{CC}} = 3 \text{ V}} $		-12	mA	
ЮН		V _{CC} = 3 V		-24	IIIA
1	l and land a dark a sum of	V _{CC} = 2.7 V		12	^
lOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETIONS		$T_A = -40$ °C to 85°C		UNIT
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
	10 mA	2.7 V	2.2		V
Voн	I _{OH} = - 12 mA	3 V	2.4]
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	V
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	
	I _{OL} = 24 mA	3 V		0.55	
1	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS295 - JANUARY 1993 - REVISED MARCH 1994

 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAG (TOP VIEW)	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE 1 20 V _{CC}	
 Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1D 3 18 8D 2D 4 17 7D	
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	2Q [5 16] 7Q 3Q [6 15] 6Q	
(DB), and Thin Shrink Small-Outline (PW) Packages	3D [] 7 14 [] 6D 4D [] 8 13 [] 5D	
description	4Q 0 9 12 0 5Q GND 0 11 0 LE	

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC373 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each latch)

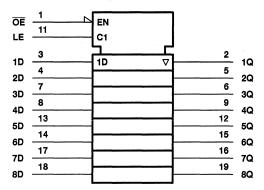
		INPUTS		OUTPUT
	OE	LE	D	Q
I	L	Н	Н	Н
١	L	Н	L	L
ı	L	L	Χ	Q ₀
l	Н	Х	Х	Z



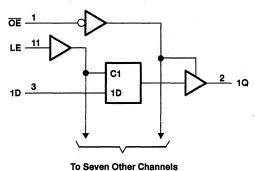
SN74LVC373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS295 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS295 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage	voltage		Vcc	V
ЮН	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
			-24	l IIIA	
1	Love level entrett entrett	V _{CC} = 2.7 V		12	^
lOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	-	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPITIONS		T _A = -40°C to 85°C		UNIT
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	ON I
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	l _{OH} = – 12 mA	2.7 V	2.2		v
Voн	10H = - 12 111A	3 V	2.4		•
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	v
	I _{OL} = 24 mA	3 V		0.55	
lj .	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μA
¹ CC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ
ΔlCC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

GND [] 10

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11 1 CLK

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGI (TOP VIEW)			
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE 1 20 V _{CC}			
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1D 0 3 18 0 8D 2D 0 4 17 0 7D			
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	2Q			
(DB), and Thin Shrink Small-Outline (PW) Packages	3D [] 7 14] 6D 4D [] 8 13] 5D			

description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC374 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	INPUTS		ОИТРИТ
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Χ	Q ₀
Н	X	Χ	z



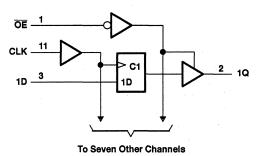
SN74LVC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS296 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†

ΕN 11 CLK C1 3 2 1D 1Q 1D 5 4 2D 2Q 7 6 3Q 3D 9 8 4D **4Q** 12 13 5Q 5D 14 15 6Q 6D 16 17 7D 7Q 19 18 8D 8Q

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V ₁	-0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	to V_{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS296 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷į	Input voltage		0	Vcc	٧
٧o	Output voltage		0	Vcc	٧
ЮН	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-12	A
		V _{CC} = 3 V		-24	mA
la.	Love lovel output output	V _{CC} = 2.7 V		12	A
lOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D. D	TEGT COMPLICATO		T _A = -40°C to 85°C		
PARAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
.,	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
	10 = 4	2.7 V	2.2		v
VOH	I _{OH} = – 12 mA	3 V	2.4		\ \
	I _{OH} = -24 mA	3 V	2		
	l _{OL} = 100 μA	MIN to MAX		0.2	V
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	
	I _{OL} = 24 mA	3 V		0.55	
ΙΙ	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC540 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS297 - JANUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB,	DW, OR PW PACKAGE
	(TOP VIEW)

		$\overline{}$		
OE1 [1	O	20] v _{cc}
A1 [2		19	OE2
A2 [3		18] Y1
A3 [4		17] Y2
A4 [5		16] Y3
A5 [6		15] Y4
A6 [7		14] Y5
A7 [8		13] Y6
A8 🗍	9		12] Y7
GND	10		11	1 Y8

description

This octal buffer/line driver is designed for 2.7-V to $3.6\text{-V}\ \text{V}_{CC}$ operation.

The SN74LVC540 is ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package that facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all corresponding outputs are in the high-impedance state.

The SN74LVC540 is characterized for operation from -40°C to 85°C.

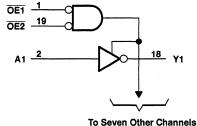
FUNCTION TABLE

	INPUTS		OUTPUT
OE1	OE2	Α	Υ
L	L	L	Н
L	L	Н	L
Н	X	Χ	z
X	Н	X	z

logic symbol†

OE1 ΕN OE2 18 Α1 V Y1 17 **Y2** A2 4 16 **Y3** АЗ 15 Α4 V4 14 6 Α5 **Y5** 7 13 **Y6** A6 8 12 Α7 **Y7** 11 **8**A

logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{IK}(V_I < 0)$	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DB package	
	1.6 W
PW package	0.7 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage V ₀	CC = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage V ₀	CC = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	٧
Vo	Output voltage		Ó	VCC	٧
12	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	rigir-level output current	CC = 3 V		-24	111/4
[₁₋ ,	Low-level output current	CC = 2.7 V		12	mA
lOL	Low-level output current V _{CC} = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	+	T _A = -40°C to 85°C		UNIT
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	ONIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	I _{OH} = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 MA	3 V	2.4		V
	I _{OH} = -24 mA .	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

OCTAL BUFFER/DRIV WITH 3-STATE OUTPUTS

SCAS298 - JANUARY 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE1 1 20 V _{CC} A1 2 19 OE2
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A1 [] 2 19 [] OE2 A2 [] 3 18 [] Y1 A3 [] 4 17 [] Y2
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A4 0 5 16 Y3 A5 0 6 15 0 Y4
(DB), and Thin Shrink Small-Outline (PW) Packages	A6 7 14 75 A7 8 13 76
escription	A8 🛛 9 12 🕽 Y7

description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC541 is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

The SN74LVC541 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

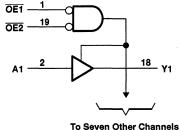
	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Х	Н	Х	Z

logic symbol†

ΕN 19 OE2 18 ∇ **A1 Y1** 3 17 **Y2** Α2 16 4 **Y3** АЗ 5 15 Υ4 A4 6 14 **Y**5 Α5 7 13 Α6 **Y6** 12 8 **Y7** 11 **Y8**

logic diagram (positive logic)

GND 1 10



EPIC is a trademark of Texas Instruments Incorporated.

INSTRUMENTS

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V ₁
Output voltage range, V _O (see Note 1)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
VCC	Supply voltage	2.7	3.6	٧
VIH	High-level input voltage V _{CC} = 2.7 V to 3.6	V 2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6	٧	0.8	٧
٧ı	Input voltage	0	Vcc	٧
Vo	Output voltage	0	Vcc	٧
la	High-level output current		-12	mA
ЮН	V _{CC} = 3 V		-24	111/4
la.	V _{CC} = 2.7 V		12	mA
lOL	OL Low-level output current VCC = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEGT COMPITIONS		T _A = -40°C	T _A = -40°C to 85°C	
	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	10 10 1	2.7 V	2.2		l _v
VOH	IOH = - 12 mA	3 V	2.4		
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
11	$V_I = V_{CC}$ or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μΑ
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS299 - JANUARY 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

DB, DW, OR PW PACKAGE (TOP VIEW)

LEBA [1	U 24	v _{cc}
OEBA [2	23] CEBA
A1 [] B1
A2 🛛			B2
АЗ [20] B3
A4 [] B4
A5 [] B5
A6 [17	B6
A7 🛚			B7
A8 🛛] B8
	11	14	LEAB
GND [12	13] OEAB

The SN74LVC543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

The SN74LVC543 is characterized for operation from -40°C to 85°C.

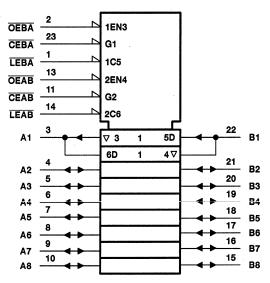
FUNCTION TABLET

	OUTPUT			
CEAB	LEAB	OEAB	Α	В
Н	Х	Х	Х	Z
X	X	н	Χ	z
L	Н	L	Χ	в ₀ ‡
L	L	L	L	L
L	L	L	Н	Н

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

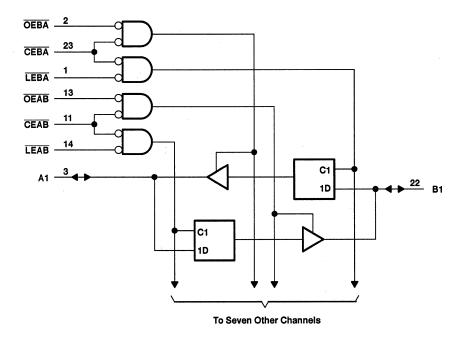
[‡] Output level before the indicated steady-state input conditions were established.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS299 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0 Input voltage range, V _I (except I/O ports) –0	
Input voltage range, V _I (I/O ports) (see Note 1)	
Output voltage range, V _O (see Note 1)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range —65	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
Vį	Input voltage				٧
٧o	Output voltage		0	Vcc	>
lou	High level output ourrent	V _{CC} = 2.7 V		-12	mA
IOH	High-level output current	V _{CC} = 3 V		-24	шА
la.	Low level output ourrent	V _{CC} = 2.7 V		12	mA
IOL	OL Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



SN74LVC543 **OCTAL REGISTERED TRANSCEIVER** WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	,, +	T _A = -40	UNIT		
		TEST CONDITIONS	v _{cc} †	MIN	TYP I	MAX	UNII
		I _{OH} = -100 µA	MIN to MAX	V _{CC} -0.2			
V		I _{OH} = - 12 mA	2.7 V	2.2			V
УОН		10H = - 12111A	3 V	2.4			V
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX			0.2	
VOL		I _{OL} = 12 mA	2.7 V			0.4	V
		I _{OL} = 24 mA	3 V			0.55	
l _l		V _I = V _{CC} or GND	3.6 V			±5	μА
loz‡		V _O = V _{CC} or GND	3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μА
Δlcc		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND				500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		3		pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V		4.3		pF

T For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		,			3.3 V 3 V	V _{CC} =	2.7 V	UNIT
				MIN	MAX	MIN	MAX	
t _W	Pulse duration			4		4		ns
t _{su}	Setup time		Data before LE↑ or CE↑	1.5		1.5		ns
th	Hold time		Data after LE↑ or CE↑	2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V	± 0.3 V	٧	V _{CC} = 2	2.7 V	UNIT
	(INFOT)	(001701)	MIN	TYP§	MAX	MIN	MAX	
	A or B	B or A	1.5	4	8		9	
^t pd	LÉ	B OF A	1.5	4.4	9.5		10.5	ns
	ŌĒ	A D	1.5	3.9	8.5		9.5	- ns
t _{en}	CE	A or B	1.5	4.1	9		10	
.	ŌĒ	A or B	1.5	4.7	8.5		9.5	
^t dis	CE		1.5	4.8	9		10	ns

[§] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS SCAS299 - JANUARY 1993 - REVISED MARCH 1994

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS	TYP	UNIT
	Down dissingtion consitence	Outputs enabled	O. 50 pF 6 10 MHz	20	
Cpd Power dissipation capacitance		Outputs disabled	C _L = 50 pF, f = 10 MHz	10	pF



SN74LVC544 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	LEBA 1 24 V _{CC} OEBA 2 23 CEBA
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A1 [3 22] B1 A2 [4 21] B2
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A3 0 5 20 0 B3 A4 0 6 19 0 B4
(DB), and Thin Shrink Small-Outline (PW)	A5 0 7 18 0 B5
Packages	A6 [] 8 17 [] B6 A7 [] 9 16 [] B7
description	A8 0 10 15 0 B8
This octal registered transceiver is designed for	CEAB 11 14 LEAB

The SN74LVC544 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the inverted data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and OEBA inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to GND through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC544 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INPUTS					
CEAB	LEAB	OEAB	Α	В		
Н	Х	Х	Х	Z		
L	X	Н	Χ	Z		
L	Н	L	Χ	В ₀ ‡		
L	L	L	L	н		
L	L	L	Н	L		

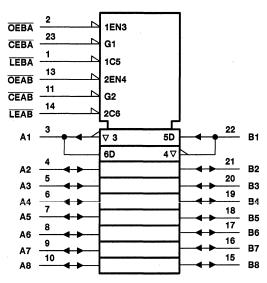
[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

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2.7-V to 3.6-V V_{CC} operation.

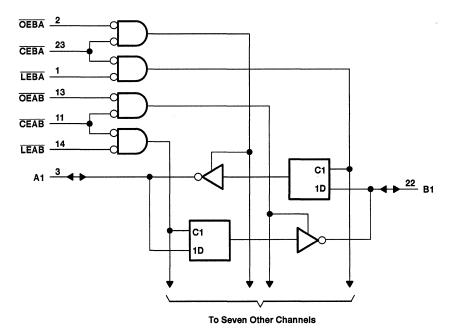
Output level before the indicated steady-state input conditions were established.

logic symbol[†]



 $\ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC544 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS346 - MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6	١٧
Input voltage range, V _I (except I/O ports)	3 V
Input voltage range, V _I (I/O ports) (see Note 1)	
Output voltage range, V _O (see Note 1)) V
Input clamp current, $I_{ K }(V_1 < 0)$ — 50 m	nΑ
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	nΑ
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 m	
Continuous current through V _{CC} or GND ±100 m	
Maximum power dissipation at T _A = 55°C (in still air): DB package	
DW package 1.7	W
PW package 0.7	W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	Vcc	V
۷o	Output voltage		0	Vcc	V
	Ligh level entrut comment	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	l IIIA
	Law lawal autawa awaran	V _{CC} = 2.7 V		12	А
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



SN74LVC544 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS SCAS346 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEST COMPITIONS		T _A = -40°C	C to 85°C	LINUT
PARAMETER		TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V		la 10 mA	2.7 V	2.2		v
VOH		I _{OH} = - 12 mA	3 V	2.4		V
`		I _{OH} = -24 mA	3 V	2		
		i _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
I _I		V _I = V _{CC} or GND	3.6 V		±5	μА
loz [‡]		V _O = V _{CC} or GND	3.6 V		±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
Δlcc		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			рF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS300 - JANUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

(TOP VIEW) OE [20 VCC 1D 2 19 1Q 2D 🛮 3 18 2Q 3D 🛛 4 17 3Q 4D 🛮 5 16**∏** 4Q 5D 🛮 6 15 5Q 6D 🛮 7 14 1 6Q 7D 🛮 8 13 7Q 8D **[**] 9 12 1 8Q GND | 10 11 [] LE

DB, DW, OR PW PACKAGE

description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC573 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each latch)

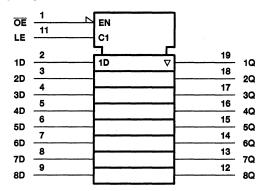
	INPUTS		OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Х	Z



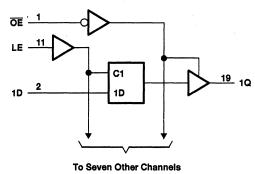
SN74LVC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS300 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V ₁
Output voltage range, V _O (see Note 1)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) ±50 mA
Continuous output current, IO (VO = 0 to VCC) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package
DW package
PW package 0.7 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷Į	V _I Input voltage		0	VCC	٧
٧o	Output voltage	tput voltage		VCC	٧
	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	Flight-level output current	V _{CC} = 3 V			IIIA
lo:	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS300 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	+	T _A = -40°C	to 85°C	UNIT
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	I _{OH} = – 12 mA	2.7 V	2.2		v
Voн	IOH = - 12 IIIA	3 V	2.4	v	v
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V μΑ
	I _{OL} = 24 mA	3 V		0.55	
l _I	$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	$V_O = V_{CC}$ or GND	3.3 V			pF

T For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



OCTAL EDGE-TRIGGERED D-TYPE FLIP-FL WITH 3-STATE OUTPUTS

GND 1 10

SCAS301 - JANUARY 1993 - REVISED MARCH 1994

11 CLK

EPIC™ (Enhanced-Performance Implanted **DB. DW. OR PW PACKAGE** (TOP VIEW) **CMOS) Submicron Process** Typical V_{OLP} (Output Ground Bounce) OE I 20 VCC $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ 1D [2 19 1 1Q Typical V_{OHV} (Output V_{OH} Undershoot) 2D [18 2Q 3 $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ 3D **1** 4 17 T 3Q Package Options Include Plastic 4D 🛮 5 16 4Q Small-Outline (DW), Shrink Small-Outline 5D [15 T 5Q 6 (DB), and Thin Shrink Small-Outline (PW) 6D [7 14 6Q **Packages** 7D 🛮 8 13 T 7Q 8D [12 1 8Q description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC574 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

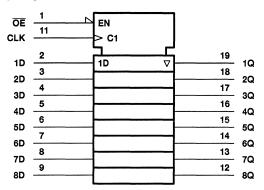
	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	Q ₀
Н	X	Χ	z



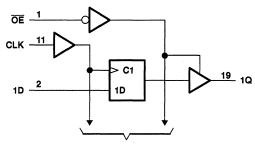
SN74LVC574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS301 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†



logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V ₁
Output voltage range, V _O (see Note 1)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Vcc	V _{CC} Supply voltage			
VIH	High-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI				٧
۷o	Output voltage		VCC	٧
	High-level output current		-12	mA
ЮН	V _{CC} = 3 V	-24		
10.	Low-level output current		12	mΑ
lor	VCC = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	ů

NOTE 2: Unused or floating inputs must be held high or low.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS301 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

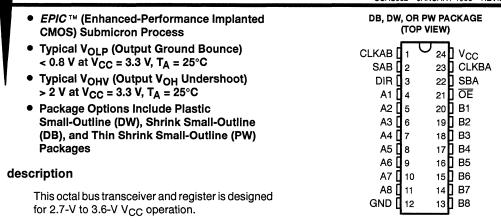
DADAMETED	TEST COMPLICATE		T _A = -40°C to 8	5°C
PARAMETER	TEST CONDITIONS	v _{cc} †	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Voc	IOH = - 12 mA	2.7 V	2.2	\square \vee
Voн	10H = - 12 IIIA	3 V	2.4	
	I _{OH} = -24 mA	3 V	2	
	l _{OL} = 100 μA	MIN to MAX	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4	4 V
	i _{OL} = 24 mA	3 V	0.55	
lμ	V _I = V _{CC} or GND	3.6 V	±5	μА
loz	$V_O = V_{CC}$ or GND	3.6 V	±10	μА
lcc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V	20	μА
ΔICC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		500	μΑ
Ci	V _I = V _{CC} or GND	3.3 V		pF
C _o	V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS302 - JANUARY 1993 - REVISED MARCH 1994



The SN74LVC646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74LVC646 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INP	UTS			DATA	A I/Os	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
X	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified [†]
×	X	Х	1	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	1	1	Х	X	Input	Input	Store A and B data
Н	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



SCAS302 - JANUARY 1993 - REVISED MARCH 1994 BUSA BUSB 8 **BUSA** BUSI 21 OE 23 22 21 22 23 DIR CLKAB CLKBA SAB SBA ŌĒ DIR CLKAB CLKBA SAB SBA L Х Х Χ L Н Х Χ Х L **REAL-TIME TRANSFER REAL-TIME TRANSFER BUS B TO BUS A BUS A TO BUS B BUSA** BUS B 8 21 3 23 2 22 21 3 23 2 22 ŌĒ DIR CLKAB CLKBA SAB SBA ŌĒ DIR CLKAB CLKBA SAB SBA Х Х Χ Х 1 Х Х H or L Х Н L L

Figure 1. Bus-Management Functions

Н

H or L

Х

TRANSFER STORED DATA TO A AND/OR B Х



Х

Н

Χ

Χ

Х

1

1

1

STORAGE FROM

A, B, OR A AND B

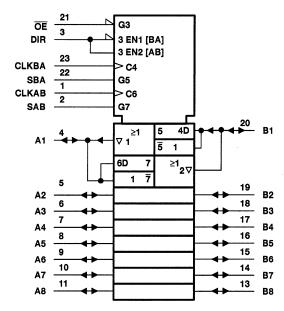
Х

Х

Х

Х

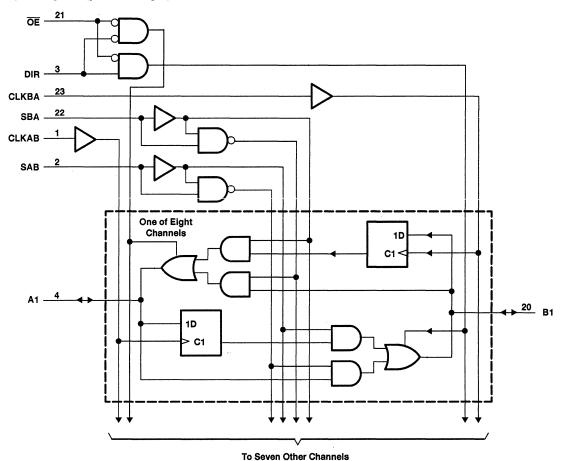
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS302 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)





SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS302 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports)	
Input voltage range, V _I (I/O ports) (see Note 1)	
Output voltage range, VO (see Note 1)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧١	Input voltage	Input voltage		Vcc	٧
٧o	Output voltage		0	Vcc	٧
	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	right-level output current	V _{CC} = 3 V		-24	
la:	Low lovel autout aureant	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current VCC = 3 V			24	MA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS302 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

- BA	DAMETED	TEST COMPITIONS	+	T _A = -40°0	$T_A = -40$ °C to 85°C	
PARAMETER		TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vон		I _{OH} = - 12 mA	2.7 V	2.2	2.2	v
VOH		10H = - 12 IIIA	3 V	2.4		· '
		I _{OH} = -24 mA	3 V	2		
		l _{OL} = 100 μA	MIN to MAX		0.2	
VOL		$I_{OL} = 12 \text{ mA}$	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
4		V _I = V _{CC} or GND	3.6 V		±5	μА
loz‡		VO = VCC or GND	3.6 V		±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
Δlcc		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]mbox{‡}$ For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS303 - JANUARY 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	, ,	PW PACKAGE P VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	CLKAB 1 1 SAB 1 2	V _{CC} 23 CLKBA
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	OEAB [3 A1 [4	22 SBA 21 OEBA
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A2 [5 A3 [6	20 B1 19 B2
(DB), and Thin Shrink Small-Outline (PW) Packages	A4 [] 7 A5 [] 8	18 🕽 B3 17 🕽 B4
description	A6 [] 9 A7 [] 10	16] B5 15] B6
This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.	A8 [] 11 GND [] 12	14] B7 13] B8

The SN74LVC652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The SN74LVC652 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INPU	TS			DATA I/OT		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	X	Х	Input	Input	Isolation
L	Н	↑	↑	X	X	Input	Input	Store A and B data
×	Н	1	H or L	×	X	Input	Unspecified [‡]	Store A, hold B
Н	Н	1	.1	X‡	Х	Input	Output	Store A in both registers
L	Х	H or L	↑	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	1	1	X	χ‡	Output	Input	Store B in both registers
L	L	Χ	Х	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	Н	Output	Input	Stored B data to A bus
Н	Н	Χ	X	L	Х	Input	Output	Real-time A data to B bus
н	Н	H or L	Χ	Н	Х	Input	Output	Stored A data to B bus
н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.



[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

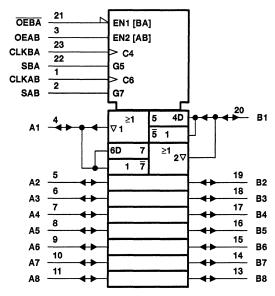
SCAS303 - JANUARY 1993 - REVISED MARCH 1994 **BUSA BUSB** 3 22 3 21 2 22 21 23 23 OEAB OEBA OEAB OEBA CLKAB CLKBA SAB SBA CLKAB CLKBA SAB SBA Χ L Н Х Х Х **REAL-TIME TRANSFER REAL-TIME TRANSFER BUS B TO BUS A BUS A TO BUS B BUSA** BUS B **BUSA** 8 BUSE 22 3 21 23 2 22 3 21 23 2 OEAB **OEBA OEBA** SBA CLKAB CLKBA SAB SBA OEAB SAB CLKAB **CLKBA** Χ Н 1 Х Χ Χ Н L H or L H or L Н Н L Х Х 1 Х Х 1 Н 1 Χ Х STORAGE FROM TRANSFER STORED DATA A, B, OR A AND B TO A AND/OR B

Figure 1. Bus-Management Functions



SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS303 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†

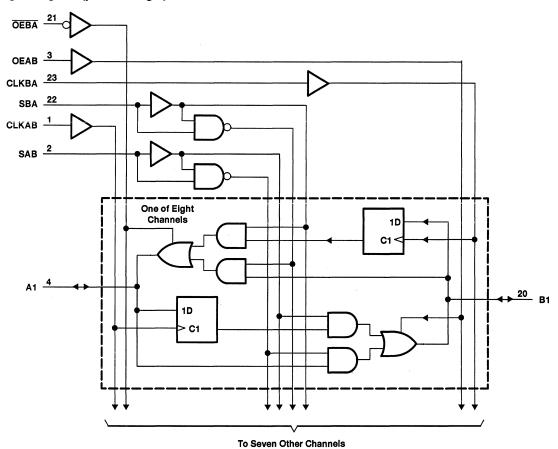


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS303 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)



SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS303 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5	
Input voltage range, V _I (except I/O ports)	V to 4.6 V
Input voltage range, V _I (I/O ports) (see Note 1)	CC + 0.5 V
Output voltage range, VO (see Note 1)	CC + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	. ±50 mA
Continuous output current, IO (VO = 0 to VCC)	. ±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	
DW package	
PW package	0.7 W
Storage temperature range65°C	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧١	Input voltage		0	Vcc	٧
٧o	Output voltage		0	Vcc	V
1	V _{CC} = 2.7 V			-12	mA
ЮН	High-level output current V _{CC} = 3 V		-24	IIIA	
1	Law lavel subside a week	V _{CC} = 2.7 V		12	^
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS303 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEGT COMPLETIONS		T _A = -40°0		
		TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
		l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
l _{v-}		IOH = - 12 mA	2.7 V	2.2		V
∨он		IOH = - 12 IIIA	3 V	2.4]
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
l _l		$V_{I} = V_{CC}$ or GND	3.6 V		±5	μА
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
Δlcc		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC821 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS304 - MARCH 1993 - REVISED MARCH 1994

 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 		PW PACKAGE VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE [1 1D [2	24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2D []3 3D []4	22 2Q 21 3Q
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	4D [5 5D [6	20 [] 4Q 19 [] 5Q
(DB), and Thin Shrink Small-Outline (PW) Packages	6D []7 7D []8	18] 6Q 17] 7Q
description	8D [] 9 9D [] 10	16 8Q 15 9Q
This 10-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V _{CC} operation.	10D [11 GND [12	14 1 10Q 13 CLK

The SN74LVC821 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

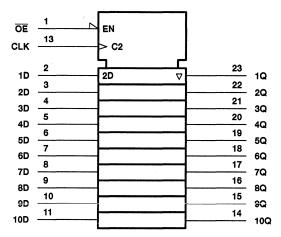
The SN74LVC821 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	INPUTS		ОИТРИТ
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Χ	Q ₀
Н	X	Χ	Z

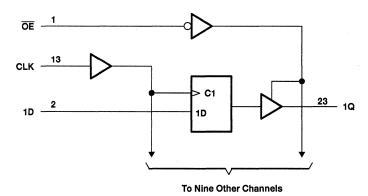


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC821 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS304 - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} Input voltage range, V ₁	
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	– 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package	0.65 W
	1.7 W
	0.7 W
	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ı	Input voltage		0	Vcc	V
Vο	Output voltage		0	Vcc	٧
1	High level output ourrent	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	'''^
1	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

SN74LVC821 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS304 - MARCH 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T _A = -40°C	to 85°C	UNIT	
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX		
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vou	I _{OH} = - 12 mA	2.7 V	2.2		v	
VOH	IOH = - 12 IIIA	3 V	2.4		· ·	
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
l _l	V _I = V _{CC} or GND	3.6 V		±5	μA	
loz	VO = VCC or GND	3.6 V		±10	μΑ	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μA	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
Co	V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS305 - MARCH 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE 1 24 V _{CC}	
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2D [] 3 22 [] 2Q 3D [] 4 21 [] 3Q	
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	4D 0 5 20 4Q 5D 0 19 5Q	
(DB), and Thin Shrink Small-Outline (PW) Packages	6D []7 18] 6Q 7D []8 17] 7Q	
description	8D [] 9 16 [] 8Q 9D [] 10 15 [] 9Q	
This 9-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V _{CC} operation.	CLR (11 14 CLKE) GND (12 13 CLK	1

The SN74LVC823 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable (CLKEN) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The SN74LVC823 has noninverting data (D) inputs. Taking the clear (CLR) input low causes the nine Q outputs to go low independently of the clock.

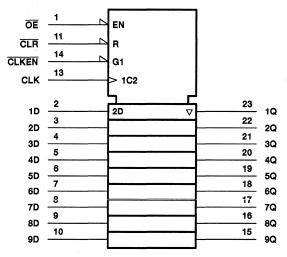
A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC823 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

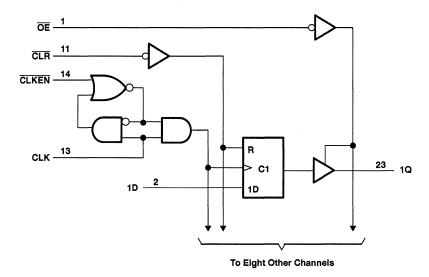
		INPUTS			OUTPUT
ŌĒ	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	Н	L	1	Н	н
L	Н	L	1	L	L
L	Н	Н	X	Χ	Q_0
Н	Χ	Χ	Χ	Χ	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCAS305 - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	– 50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	
	1.7 W
PW package	0.7 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Vcc	Supply voltage	2.7	3.6	V
VIH	High-level input voltage V _{CC} = 2.7 V to 3.	6 V 2		V
VIL	Low-level input voltage $V_{CC} = 2.7 \text{ V to } 3.$	6 V	0.8	V
VI	Input voltage	0	Vcc	V
Vo	Output voltage	0	Vcc	٧
lau	High-level output current		-12	mA
ЮН	V _{CC} = 3 V		-24	IIIA
lai	Low-level output current		12	mA
lor	V _{CC} = 3 V		24	I IIIA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



SN74LVC823 9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS305 - MARCH 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = -40°C to 85°C	UNIT
PANAMETER	TEST CONDITIONS	vcct	MIN MAX	JUNII
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Vou	I _{OH} = - 12 mA	2.7 V	2.2] ,
Voн	10H = - 12 IIIA	3 V	2.4] '
	I _{OH} = -24 mA	3 V	2	
	I _{OL} = 100 μA	MIN to MAX	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4	V
	I _{OL} = 24 mA	3 V	0.55	
lį	V _I = V _{CC} or GND	3.6 V	±5	μА
loz	$V_O = V_{CC}$ or GND	3.6 V	±10	μA
lcc	$V_{I} = V_{CC}$ or GND, $I_{O} = 0$	3.6 V	20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	μА
Ci	V _I = V _{CC} or GND	3.3 V		pF
Co .	$V_O = V_{CC}$ or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC827 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS306A - MARCH 1993 - REVISED JUNE 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This 10-bit buffer/bus driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC827 provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC827 provides true data at its outputs.

The SN74LVC827 is characterized for operation from -40°C to 85°C.

DB, DW, OR PW PACKAGE

(TOP VIEW)

A10 11 14 Y10 GND 12 13 OE2

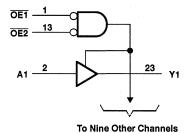
FUNCTION TABLE

	INPUTS	OUTPUT				
OE1	OE2	Α	Y			
L	L	L	L			
L	L	Н	Н .			
н	Х	Χ	Z			
Х	Н	Х	Z			

logic symbol†

OE1 ΕN 13 OF2 23 Α1 **Y1** 22 Α2 **Y2** 4 21 **Y3** 5 20 Α4 **Y**4 6 19 **Y5** Α5 7 18 A6 8 17 **Y7** Α7 9 16 **Y8** 10 15 A9 11 14 Y10 A10

logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I
Output voltage range, V _O (see Note 1)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	Vcc	٧
٧o	Output voltage		0	Vcc	٧
	V _{CC} = 2.7 V			-12	4
IOH	High-level output current VCC = 3 V		-24	mA	
1	Low level output surrent	V _{CC} = 2.7 V		12	^
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = -40°C to	85°C	UNIT
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP	MAX	UNII
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
\/	Jan. 10 mA	2.7 V	2.2		ν
VOH	I _{OH} = – 12 mA	3 V	2.4		
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	٧
VOL	$I_{OL} = 12 \text{ mA}$	2.7 V		0.4	
	I _{OL} = 24 mA	3 V		0.55	
H	$V_I = V_{CC}$ or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
C _i	V _I = V _{CC} or GND	3.3 V	7.5		pF
Co	V _O = V _{CC} or GND	3.3 V	8.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} = 2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MAX	UNII
t _{pd}	Α	Y	1.5	3.5	7	8	ns
ten	ŌĒ	Υ	1.5	4.3	9	11	ns
^t dis	ŌĒ	Y	1.5	4	8	9	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



SN74LVC827 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS306A - MARCH 1993 - REVISED JUNE 1994

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	Ci = 50 pF. f = 10 MHz		25	pF
	Outputs disabled	C _L = 50 pF,	1 = 10 MHZ	2.5	pr

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This 10-bit buffer/bus driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC828 provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC828 provides inverting data at its outputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC828 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS			OUTPUT
ı	OE1	OE2	Α	Υ
	L	L	L	Н
	L	L	Н	L
	Н	X	Χ	Z
	Х	Н	Х	Z

(TOP VIEW)

DB, DW, OR PW PACKAGE

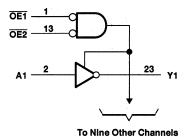
OE1	1	O 24] v _{cc}
A1	12	23] Y1
A2		22] Y2
А3		21] Y3
A4		20] Y4
A5		19] Y5
A6		18] Y6
A7		17] Y7
A8	9	16] Y8
A9	10	15] Y9
A10 (11	14] Y10
GND [12	13	OE2

PRODUCT PREVIEW

logic symbol†

OE1 13 ΕN OE2 23 Y1 3 22 **Y2** Α2 21 АЗ **Y3** 5 20 **Y4** 6 19 Α5 **Y**5 7 18 **Y6** A6 8 17 **Y7** Α7 9 16 **Y8 A8** 10 15 **Y9** 11 A10 Y10

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V ₁
Output voltage range, V _O (see Note 1)
Input clamp current, $I_{ K }(V_{ I } < 0)$
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})
Continuous output current, IO (VO = 0 to VCC)
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
VCC	Supply voltage	2.7	3.6	٧
V _{IH}	High-level input voltage V _{CC} = 2.7 V to 3	3.6 V 2		V
۷ _{IL}	Low-level input voltage $V_{CC} = 2.7 \text{ V to } 3$	3.6 V	0.8	, A
٧ _I	Input voltage	0	Vcc	٧
۷o	Output voltage	0	Vcc	٧
	V _{CC} = 2.7 V		-12	mA
ŌН	High-level output current VCC = 3 V		-24	I IIIA
lo	Low-level output current		12	
lOL	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	T _A = -40°C to 85°C	UNIT	
	TEST CONDITIONS		MIN MAX		
VOH	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
	Jan. 10 mA	2.7 V	2.2	V	
	$I_{OH} = -12 \text{ mA}$	3 V	2.4		
	I _{OH} = -24 mA	3 V	2		
VOL	I _{OL} = 100 μA	MIN to MAX	0.2	V	
	I _{OL} = 12 mA	2.7 V	0.4		
	I _{OL} = 24 mA	3 V	0.55		
l _l	V _I = V _{CC} or GND	3.6 V	±5	μА	
loz	V _O = V _{CC} or GND	3.6 V	±10	μА	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20	μА	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	μА	
Ci	V _I = V _{CC} or GND	3.3 V		pF	
Co	V _O = V _{CC} or GND	3.3 V		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS307 - MARCH 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This 10-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC841 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

(TOP VIEW)

OE 1 24 V_{CC}

1D 2 23 1Q

2D 3 22 2Q

3D 4 21 3Q

4D 5 20 4Q

DB, DW, OR PW PACKAGE

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC841 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z



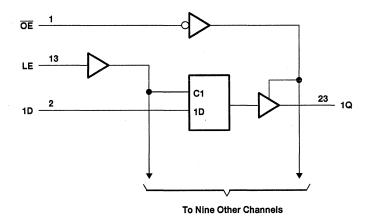
SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS307 - MARCH 1993 - REVISED MARCH 1994

logic symbol†

ŌE LE	13	EN C1		
1D	2		23	1Q
2D	3		22	2Q
3D	4		21	
4D	5		20	3Q 4Q
	6		19	5Q
5D 6D	7		18	6Q
7D	8		17	7Q
8D	9		16	8Q
	10		15	9Q
9D	11		14	
10D				10Q

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS307 - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cumply valtage range V	0 E \/ to 4 G \/
Supply voltage range, V _{CC}	
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	– 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ı	Input voltage		0	VCC	٧
٧o	Output voltage		0	Vcc	٧
lou	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
lOH			-24	ША	
lou	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	V _{CC} = 3 V			24	ША
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ů

NOTE 2: Unused or floating inputs must be held high or low.



SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS307 - MARCH 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	+	T _A = -40°C to 85°C		
PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	Jan. 12 mA	2.7 V	2.2		v
Voн	IOH = - 12 mA	3 V	2.4		V
	I _{OH} = - 24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	V
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	
	I _{OL} = 24 mA	3 V		0.55	
. II	V _I = V _{CC} or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC843 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS308 - MARCH 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This 9-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC843 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

24 1 V_{CC} OE [] 1D 🗓 2 23 1 1Q 2D 🛮 3 22 2Q 3D 🛮 4 21 30 4D 🛮 5 20 0 4Q 5D L 19 L 5Q 6D 🛮 7 18 🛮 6Q 7D []8 17 🛮 7Q 8D 🛮 9 16 0 8Q 9D [] 10 15 🛮 9Q 14 PRE CLR [] 11 13 🛭 LE GND [] 12

DB, DW, OR PW PACKAGE (TOP VIEW)

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC843 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS				
PRE	CLR	ŌĒ	LE	D	Q
L	X	L	Х	X	Н
Н	L	L	X	Χ	L
Н	Н	L	Н	L	L
Н	Н	L	Н	Н	Н
Н	н	L	L	Χ	Q ₀
Х	Х	Н	Х	Х	Z

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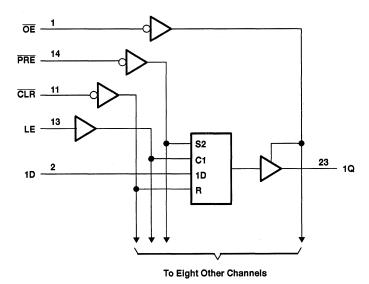
SN74LVC843 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS308 - MARCH 1993 - REVISED MARCH 1994

logic symbol†

OE PRE CLR LE	1 14 11 13	EN S2 R C1		
1D	2	1D 2 ▽	23	1Q
2D	3		22	2Q
3D	4		21	3Q
4D	5		20	4Q
	6		19	
5D 6D	7		18	5Q 6Q
	8		17	
7D	9		16	7Q
8D	10	<u> </u>	15	8Q
9D				9Q

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC843 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS308 - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁	0.5 V to 4.6 V
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DB package	
DW package	1.7 W
PW package	0.7 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
٧ _{IH}	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
VI	Input voltage		0	VCC	٧
Vο	Output voltage		0	Vcc	٧
1	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-12	mA
ЮН			-24	IIIA	
1	Law layed a should a sweeth	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.



SN74LVC843 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS308 - MARCH 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPITIONS		T _A = -40°C to 85°C		UNIT	
PARAMETER	TEST CONDITIONS	vcct	MIN M	AX	UNII	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vou	lour - 12 mA	2.7 V	2.2		v	
Voн	IOH = - 12 mA	3 V	2.4			
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	I _{OL} = 12 mÁ	2.7 V		0.4	٧	
	I _{OL} = 24 mA	3 V	0	.55		
l _į	V _I = V _{CC} or GND	3.6 V		±5	μА	
loz	VO = VCC or GND	3.6 V	±	10	μА	
lcc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		20	μА	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			рF	
Co	VO = VCC or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC861 10-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS309 - MARCH 1993 - REVISED MARCH 1994

EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OEBA 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A2 0 3 22 0 B2 A3 0 4 21 0 B3
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A4 5 20 B4 A5 6 19 B5
(DB), and Thin Shrink Small-Outline (PW) Packages	A6 🛛 7 18 🗍 B6 A7 🗓 8 17 🗍 B7
description	A8 [] 9 16]] B8 A9 [] 10 15]] B9
This 10-bit bus transceiver is designed for 2.7-V to $3.6-V$ V _{CC} operation.	A10 11 14 B10 GND 12 13 OEAB

The SN74LVC861 is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (\overline{OEAB} and \overline{OEBA}) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC861 is characterized for operation from -40°C to 85°C.

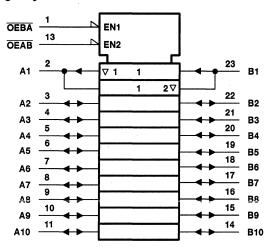
FUNCTION TABLE

INP	UTS	OPERATION	
OEAB	OEBA	OPERATION	
L	Н	A data to B bus	
Н	L	B data to A bus	
н	Н	Isolation	
L	L	Latch A and B (A = B)	

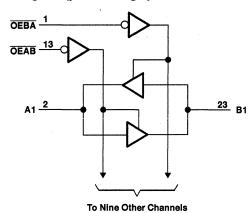
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logic symbol[†]



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Note 1)	.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)0	$.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ I } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: This value is limited to 4.6 V maximum.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC861 10-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCAS309 - MARCH 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 2)

	•		MIN	MAX	UNIT
Vcc	Supply voltage	_	2.7	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
۷ _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
٧į	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	٧
	V _{CC} = 2.7 V			-12	mA
ЮН	High-level output current VCC = 3 V		-24	mA	
1	V _{CC} = 2.7 V			12	A
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CONDITIONS		T	T _A = -40°	C to 85°C	LINUT	
Ρ.	ARAMETER			vcct	MIN	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2			
V		la., 10 mA		2.7 V	2.2		v	
VOH		I _{OH} = - 12 mA		3 V	2.4		V	
		I _{OH} = -24 mA		3 V	2			
VOL		I _{OL} = 100 μA		MIN to MAX		0.2	- v	
		I _{OL} = 12 mA		2.7 V		0.4		
		I _{OL} = 24 mA		3 V		0.55		
11		V _I = V _{CC} or GND		3.6 V		±5	μА	
loz‡		VO = VCC or GND		3.6 V		±10	μА	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$		3.6 V		20	μА	
ΔlCC		V _{CC} = 3 V to 3.6 V, One input Other inputs at V _{CC} or GND	at V _{CC} – 0.6 V,			500	μА	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V			pF	
Cio	A or B ports	VO = VCC or GND		3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC863 9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS310 - MARCH 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OEBA1 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A2 [] 3 22 [] B2 A3 [] 4 21 [] B3
Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DR), and This Shrink Small Outline	A4 0 5 20 0 B4 A5 0 6 19 0 B5
(DB), and Thin Shrink Small-Outline (PW) Packages	A6 [] 7 18 [] B6 A7 [] 8 17 [] B7 A8 [] 9 16 [] B8
description	A9 0 10 15 0 B9
This 9-bit bus transceiver is designed for 2.7-V to $3.6-V$ V _{CC} operation.	OEBA2 11 14 OEAB2 GND 12 13 OEAB1

The SN74LVC863 is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (\overline{OEAB} and \overline{OEBA}) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC863 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP	ODEDATION		
OEAB1	OEAB2	OEBA1	OEBA2	OPERATION
L	L	L	L	Latch A and B
L	L	Н	Х	A to B
L	L	Х	Н	X 10 B
Н	Х	L	L	B to A
Х	Н	L	L	B 10 K
Н	X	Н	Х	
Н	Χ	Χ	Н	Isolation
X	Н	Χ	Н	isolation
×	Н	Н	Х	

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logic symbol†

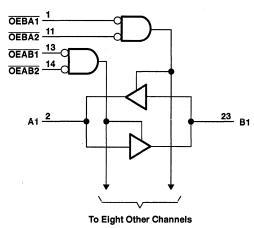
Α7

Α8

10

OEBA1 EN₁ 11 OEBA2 13 OEAB1 EN2 OEAB2 23 V 1 1 22 В2 Α2 21 В3 АЗ 20 В4 A4 19 В5 Α5 18 **B**6 Α6 17

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

... В7 16 В8

15 B9

Supply voltage range, V _{CC}	
Input voltage range, V _I (except I/O ports)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DB package	0.65 W
DW package	1.7 W
	0.7 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	V
٧١	Input voltage		0	Vcc	V
٧o	Output voltage			Vcc	V
	V _{CC} = 2.7 V			-12	A
ЮН	High-level output current VCC = 3 V	V _{CC} = 3 V		-24	mA
lou	Low-level output current	V _{CC} = 2.7 V		12	A
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEGT COMPLETIONS		T _A = -40°0	C to 85°C	UNIT	
PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII	
		IOH = -100 μA	MIN to MAX	V _{CC} -0.2			
		la 10 mA	2.7 V	2.2		l _v l	
Vон		IOH = - 12 mA	3 V	2.4		'	
İ		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	V	
		I _{OL} = 24 mA	3 V		0.55		
l _l		V _I = V _{CC} or GND	3.6 V		±5	μA	
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА	
Icc		$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		20	μА	
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF	
C _{io}	A or B ports	VO = VCC or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC2952 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS311 - JANUARY 1993 - REVISED MARCH 1994

EPIC™ (Enhanced-Performance Implanted **DB. DW. OR PW PACKAGE** (TOP VIEW) **CMOS) Submicron Process** Typical V_{OLP} (Output Ground Bounce) 24 VCC ва П $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ B7 [2 23 🛮 A8 Typical V_{OHV} (Output V_{OH} Undershoot) В6 Пз 22 N A7 $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ B5 **[**] 4 21 A6 B4 **∏** 5 **Package Options Include Plastic** 20 A5 Small-Outline (DW), Shrink Small-Outline B3 **∏** 6 19**∏** A4 (DB), and Thin Shrink Small-Outline (PW) B2 **[**] 7 18 A3 **Packages** В1 Г 8 17 ∏ A2 OEAB 19 16 A1 description CLKAB 10 15 OEBA CLKENAB [11 14 CLKBA This octal bus transceiver and register is designed

for 2.7-V to 3.6-V V_{CC} operation.

GND [12 13] CLKENBA

The SN74LVC2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low.

The SN74LVC2952 is characterized for operation from -40°C to 85°C.

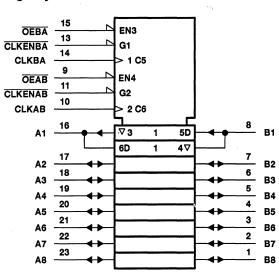
Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

FUNCTION TABLET

	INPUTS					
CLKENAB	CLKAB	OEAB	Α	В		
Н	Х	L	Х	В ₀ ‡		
Х	H or L	L	Χ	В ₀ ‡ В ₀ ‡		
L	1	L	L	L		
L	1	L	H	н		
x	X	Н	Χ	z		

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA. CLKBA, and OEBA.

logic symbol§



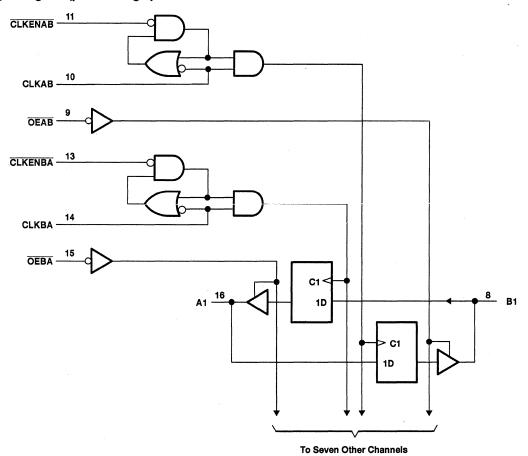
§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

[‡]Level of B before the indicated steady-state input conditions were established.

SN74LVC2952 **OCTAL BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS SCAS311 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)



SCAS311 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports)
Input voltage range, V _I (I/O ports) (see Note 1)
Output voltage range, V _O (see Note 1)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I_O (V_O = 0 to V_{CC})
Continuous current through V _{CC} or GND
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

		MI	N	MAX	UNIT
Vcc	Supply voltage	2	.7	3.6	٧
VIH	High-level input voltage VCC = 2.7 V	to 3.6 V	2		٧
VIL	Low-level input voltage VCC = 2.7 V	to 3.6 V		0.8	V
Vį	Input voltage		0	VCC	٧
٧o	Output voltage		0	VCC	٧
la	V _{CC} = 2.7 V			-12	mA
ЮН	High-level output current VCC = 3 V			-24	MA
la.	V _{CC} = 2.7 V	'		12	mA
lOL	Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	-4	0	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



SN74LVC2952 **OCTAL BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS SCAS311 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	DAMETED	TEST COMPLTIONS		T _A = -40°0	UNIT		
PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNII	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0,2			
		laura 12 mA	2.7 V	2.2		v	
VOH		I _{OH} = - 12 mA	3 V	2.4]	
		I _{OH} = -24 mA	3 V	2		1	
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4] v	
		I _{OL} = 24 mA	3 V		0.55		
l _l		V _I = V _{CC} or GND	3.6 V		±5	μА	
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА	
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	Control inputs	VI = VCC or GND	3.3 V			pF	
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

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LVC Widebus™

Features

- 0.8-μ EPIC-II™ CMOS process
- Bus-hold cell on data inputs and I/Os
- Very low standby current (40 μA)
- -24-mA/24-mA drive current
- 2.7-V to 3.6-V V_{CC} range
- JEDEC SSOP Widebus™ and EIAJ TSSOP Shrink Widebus™ packaging
- TI has established two worldwide alternate sources

Benefits

- High-performance propagation delays as fast as 6.5 ns
- Saves power, extends battery life
- Eliminates passive pullup resistors
- Drives transmission lines down to 50 Ω
- Fully characterized for unregulated battery operation
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

SN74LVC16240 **16-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS

SCAS312 - NOVEMBER 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 48 20E
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y1 02 47 11A1 1Y2 03 46 11A2 GND 04 45 0 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 0 5 44 1 1A3 1Y4 0 6 43 0 1A4
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	V _{CC} 7 42 V _{CC} 2Y1 8 41 2A1
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	2Y2
Small-Outline (DGG) Packages	2Y4
description	3Y2 14 35 3A2
This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.	GND [] 15 34
The SN74LVC16240 is designed specifically to improve both the performance and density of	V _{CC}
3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	4Y2
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical \overline{OE} (active-low output-enable) inputs	4Y3 [22 27] 4A3 4Y4 [23 26] 4A4 4OE [24 25] 3OE

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

		· · · · · · · · · · · · · · · · · · ·
INPUTS		OUTPUT
ŌĒ	Α	Y
L	Н	L
L	L	н
н	X	Z

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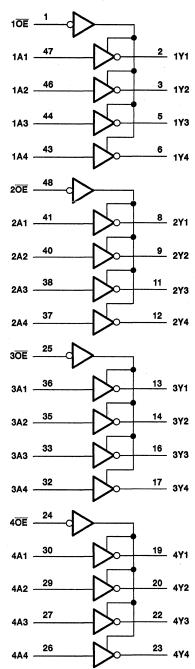
4A3

4A4

26

10E EN1 48 2OE EN₂ 25 3OE EN3 4OE EN4 47 1A1 1 1 🗸 **1Y1** 46 3 1A2 1Y2 5 44 1A3 1Y3 43 6 1A4 **1Y4** 41 8 2A1 2 ▽ 2Y1 40 9 2A2 2Y2 38 11 2A3 2Y3 37 12 2A4 2Y4 36 13 3 ▽ 3A1 3Y1 35 14 3A2 3Y2 33 16 3A3 **3Y3** 32 17 3A4 **3Y4** 30 19 1 4 ▽ 4A1 4Y1 29 20 4A2 **4Y2** 27 22

logic diagram (positive logic)



4Y3

4Y4

23

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DGG package	
	1.2 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _C C = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	٧
Vο	Output voltage		0	VCC	V
lau	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	""
1	I am land a day day and a	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current VCC = 3 V			24	1111
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ô

NOTE 3: Unused or floating control pins must be held high or low.

SN74LVC16240 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS312 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{CC} †	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	2	
		10 10 10	2.7 V	2.2		.,
VOH		I _{OH} = -12 mA	3 V	2.4		٧
		$I_{OH} = -24 \text{ mA}$	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
V_{OL}		I _{OL} = 12 mA	2.7 V		0.4	1 v
		I _{OL} = 24 mA	3 V		0.55	
lį		V _I = V _{CC} or GND	3.6 V		±5	μΑ
1	Data mina	V _I = 0.8 V	0.1/	75		
I(hold)	Data pins	V _I = 2 V	3 V	-75		μΑ
loz		V _O = V _{CC} or GND	3.6 V		±10	μΑ
ICC		V _I = V _{CC} or GND, I _O = 0	3.6 V		40	μА
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci		V _I = V _{CC} or GND	3.3 V			рF
Co		V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 48 20E
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y1
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 5 44 1A3 1Y4 6 43 1A4
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	V _{CC} 7
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	2Y2 9 40 2A2 GND 10 39 GND 2Y3 11 38 2A3
Small-Outline (DGG) Packages description	2Y4
This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V _{CC} operation.	3Y2
The SN74LVC16241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	V _{CC}
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary output-	GND 21 28 GND 4Y3 22 27 4A3 4Y4 23 26 4A4 4OE 24 25 30E
enable (OE and OE) inputs.	

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16241 is characterized for operation from -40°C to 85°C.

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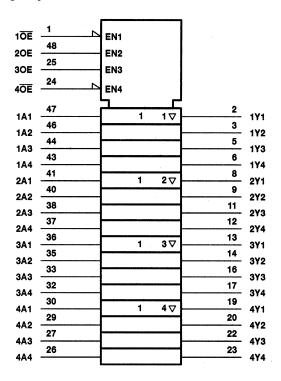
PRODUCT PREVIEW

FUNCTION TABLES

INPL	OUTPUTS	
10E, 40E	1A, 4A	1Y, 4Y
L	Н	Н
L .	L	L
Н	X	z

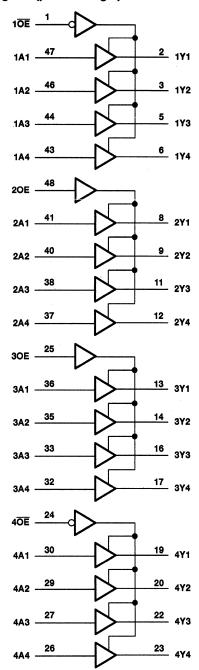
INPL	INPUTS	
20E, 30E	2A, 3A	2Y, 3Y
Н	Н	Н
н	L	L
L	X	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package	0.85 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MI	N I	MAX	UNIT
Vcc	Supply voltage	2.	7	3.6	V
VIH	High-level input voltage VCC = 2.7 V to	o 3.6 V	2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V to	o 3.6 V		0.8	٧
VI	Input voltage		0	Vcc	V
۷o	Output voltage		0	Vcc	٧
lau	High-level output current			-12	mA ·
IOH	V _{CC} = 3 V			-24	IIIA ·
la.	V _{CC} = 2.7 V			12	mΛ
IOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	-4	0	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

SN74LVC16241 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS348 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST CONDITIONS	Vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	VCC-0	.2	
Va		Jan. 10 mA	2.7 V	2.2		v
VOH		I _{OH} = -12 mA	3 V	2.4		٧
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
l _l		V _I = V _{CC} or GND	3.6 V		±5	μА
	Data aire	V _I = 0.8 V	3 V	75		4
I(hold)	Data pins	V _I = 2 V	3,4	-75		μА
loz		V _O = V _{CC} or GND	3.6 V		±10	μA
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔI _{CC}		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci		V _I = V _{CC} or GND	3.3 V			pF
Co		VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS313 - NOVEMBER 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAG (TOP VIEW)			
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>0E</u>	1		2 <u>0E</u>
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y1 1Y2	3	46	1A1 1A2
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	GND 1Y3 1Y4	5	44	GND 1A3 1A4
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown	V _{CC} [2Y1 [7	42	V _{CC}
Resistors	2Y2 [GND [9	40	2A2 GND
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	2Y3 [11	38	2A3
Small-Outline (DGG) Packages	2Y4 [3Y1 [13	36	2A4 3A1
description	3Y2 [GND [3A2
This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.	3Y3 [3Y4 [16	33] GND] 3A3] 3A4
The SN74LVC16244 is designed specifically to improve both the performance and density of	v _{cc} [3	31	V _{CC}
3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	4Y2 [GND [20	29	4A2 GND
The device can be used as four 4-bit buffers, two	4Y3 [4A3
8-bit buffers, or one 16-bit buffer. It provides true	4Y4 [23	26	4 <u>A4</u>
outputs and symmetrical OE (active-low output- enable) inputs.	4 0E [24	25	3 <u>OE</u>

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT			
OE	Α	Y			
L	Н	Н			
L	L	L			
Н	X	Z			

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SN74LVC16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

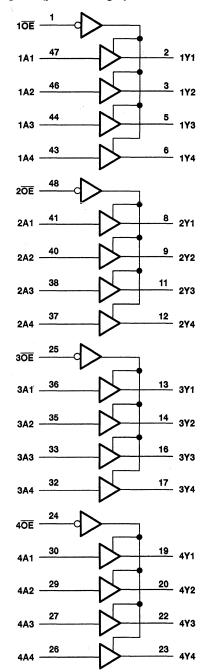
SCAS313 - NOVEMBER 1993 - REVISED MARCH 1994

logic symbol†

					•	
10E 20E 30E 40E	1 48 25 24	EN1 EN2 EN3 EN4				
1A1	47	느	1	1▽	2	474
1A2	46	<u> </u>		- ' \	3	1Y1
	44	 -			5	1Y2
1A3	43	}			6	1Y3
1A4	41	 			8	1Y4
2A1	40	ļ	1	2 ▽	9	2Y1
2A2	38	 			11	2Y2
2A3	37			,	12	2Y3
2A4	36				13	2Y4
3A1	35		1	3 ▽	14	3Y1
3A2	33	 			16	3Y2
3A3	32	 			17	3 Y 3
3A4	30	 			19	3Y4
4A1	29	<u> </u>	1	4 ▽	20	4Y1
4A2	27	<u> </u>			22	4Y2
4A3	26	<u> </u>			23	4Y3
4A4		<u> </u>				4Y4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





PRODUCT PREVIEV

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
	±50 mA
	±50 mA
	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): DGG package 0.85 W
	DL package 1.2 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC} Supply voltage			2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	V
Vο	Output voltage			VCC	٧
lan link i	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	V _{CC} = 3 V	V _{CC} = 3 V		-24	
lai	Low-level output current	V _{CC} = 2.7 V		12	mΑ
lor	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ů

NOTE 3: Unused or floating control pins must be held high or low.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

SN74LVC16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS313 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0	.2	
\ _{\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\}	VOH VOL II II(hold) Data pins IOZ ICC AICC	10.00		2.2		V
VOH		IOH = -12 mA	3 V	2.4		٧
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
lj		V _I = V _{CC} or GND	3.6 V		±5	μА
lia in	V _I	V _I = 0.8 V	3 V	75		μА
'I (hold)	Data pins	V _I = 2 V		-75		
loz		V _O = V _{CC} or GND	3.6 V		±10	μА
icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 ∨	1	40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci		V _I = V _{CC} or GND	,3.3 V			pF
Co		V _O = V _{CC} or GND	3.3 V			рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS314 - NOVEMBER 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION	
ŌĒ	DIR	OPERATION	
L	L	B data to A bus	
L.	Н	A data to B bus	
Н	Χ	Isolation	

DGG OR DL PACKAGE (TOP VIEW)

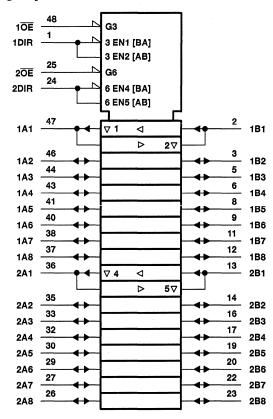
		T		
1DIR	1			10E
1B1				1A1
1B2				1A2
GND	4		45	GND
1B3				1A3
1B4			43] 1A4
Vcc			42	v _{cc}
1B5	8		41	1A5
1B6				1A6
GND				GND
1B7	11] 1A7
1B8				1A8
2B1				2A1
2B2	14			2A2
GND				GND
2B3	16		33	2A3
2B4			32	2A4
v _{cc} [18		31	v _{cc}
2B5	19		30	2A5
2B6	20] 2A6
GND				GND
2B7			27	2A7
2B8 🛭			26	2A8
2DIR	24		25	20E
				ı

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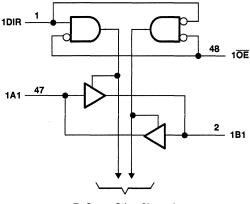
SCAS314 - NOVEMBER 1993 - REVISED MARCH 1994

logic symbol†

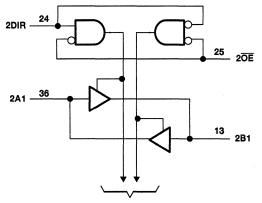


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SN74LVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS314 - NOVEMBER 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package	
DL package	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷Į	Input voltage		0	VCC	V
Vo	Output voltage			Vcc	V
I _{OH} High-	Mark Invalentary to compare	V _{CC} = 2.7 V		-12	mA
	High-level output current	V _{CC} = 3 V		-24	
1	Lave lavel autorit ausward	V _{CC} = 2.7 V		12	A
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.



SN74LVC16245 **16-BIT BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCAS314 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

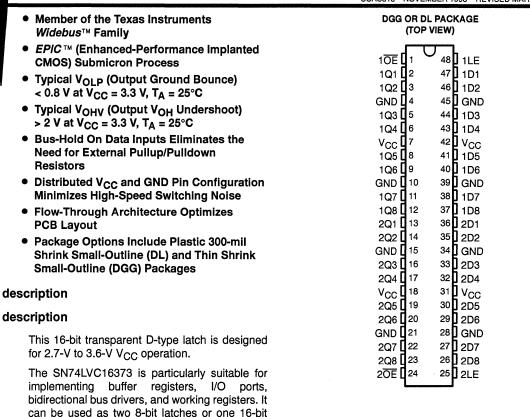
PARAMETER		TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	2	
		10 10	2.7 V	2.2		v
VOH		$I_{OH} = -12 \text{ mA}$	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
lį	Control pins	V _I = V _{CC} or GND	3.6 V		±5	μА
1	Data nina	V _I = 0.8 V	3 V	75		
l(hold)	Data pins	V _I = 2 V		-75		μА
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS315 - NOVEMBER 1993 - REVISED MARCH 1994



A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16373 is characterized for operation from -40°C to 85°C.

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latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels



set up at the D inputs.

FUNCTION TABLE (each 8-bit section)

INPUTS			OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	z

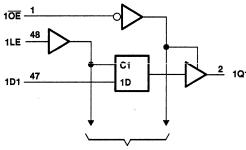
logic symbolt

PRODUCT PREVIEW

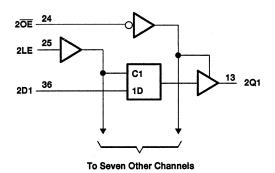
10E	1	1EN			
1LE	48	СЗ			
2OE	24	2EN			
2LE	25	C4			
Æ la la		٢	لے		
1D1	47	3D	1 ▽	2	1Q1
1D2	46		• •	3	1Q2
1D3	44			5	1Q3
1D4	43			6	1Q4
1D5	41			8	
	40			9	1Q5
1D6	38	<u> </u>		11	1Q6
1D7	37			12	107
1D8	36			13	1Q8
2D1	35	4D	2 ▽	14	2Q1
2D2	33			16	2Q2
2D3	32			17	2Q3
2D4	30			19	2Q4
2D5	29			20	2Q5
2D6	27			22	2Q6
2D7	26			23	2Q7
2D8					2Q8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74LVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS315 - NOVEMBER 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
	±100 mA
	: DGG package 0.85 W
, , , , , , , , , , , , , , , , , , , ,	DL package 1.2 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VιΗ	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷ _I	Input voltage		0	Vcc	٧
Vo	Output voltage		0	Vcc	٧
Jan.	High-level output current	V _{CC} = 2.7 V		-12	mA
IOH	nigh-level output current	V _{CC} = 3 V		-24	mA
la.	Laur laural autout aumant	V _{CC} = 2.7 V		12	m^
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.



SN74LVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS315 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		TEST CONDITIONS	v _{cc} †	MIN I	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
.,		10 10	2.7 V	2.2		V
VOH		I _{OH} = -12 mA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
Ц		V _I = V _{CC} or GND	3.6 V		±5	μА
1	Data nina	V _I = 0.8 V	3 V	75		
l(hold)	Data pins	V _I = 2 V		-75		μА
loz		V _O = V _{CC} or GND	3.6 V		±10	μА
icc		$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		40	μА
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci		V _I = V _{CC} or GND	3.3 V			pF
Co		V _O = V _{CC} or GND	3.3 V			рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS316 - NOVEMBER 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 48 1CLK
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q1
 Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q3
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	$V_{CC} \begin{bmatrix} 1 & 42 \\ 1 & 1 \end{bmatrix} V_{CC} $ 1 Q5 $\begin{bmatrix} 1 & 41 \\ 1 & 1 \end{bmatrix}$ 1 D5
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	1Q6 [] 9 40 [] 1D6 GND [] 10 39 [] GND 1Q7 [] 11 38 [] 1D7
 Flow-Through Architecture Optimizes PCB Layout 	1Q8
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	2Q2 [] 14 35 [] 2D2 GND [] 15 34 [] GND 2Q3 [] 16 33 [] 2D3 2Q4 [] 17 32 [] 2D4
description	V _{CC} 18 31 V _{CC} 2Q5 19 30 2D5
This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V _{CC} operation.	2Q6
The SN74LVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.	2Q7 [22 27] 2D7 2Q8 [23 26] 2D8 2OE [24 25] 2CLK

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16374 is characterized for operation from -40°C to 85°C.

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FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Χ	Q ₀
Н	Х	Χ	Z

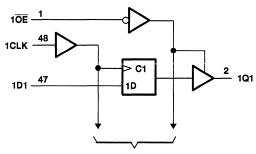
logic symbol†

PRODUCT PREVIEW

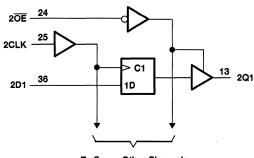
10E 1EN 48 1CLK C1 24 20E 2EN 25 2CLK - C2 47 2 1D1 1D 1 ▽ 1Q1 46 3 1D2 1Q2 44 5 1D3 1Q3 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 1Q7 37 12 1D8 1Q8 36 13 2D1 2D 2 ▽ 2Q1 14 35 2D2 2Q2 33 16 2D3 2Q3 17 32 2D4 2Q4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 23 2D8 2Q8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS316 - NOVEMBER 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DGG package .	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
	Lieb level order to sweet	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	MA
1	V _{CC} = 2.7 V			12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.



SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS316 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	PARAMETER TEST CONDITIONS		vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	VCC-0	.2	
		Jan. 10 mA	2.7 V	2.2		v
VOH		I _{OH} = -12 mA	3 V	2.4		V
		$I_{OH} = -24 \text{ mA}$	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
lj		V _I = V _{CC} or GND	3.6 V		±5	μА
	Data mina	V _I = 0.8 V	3 V	75		4
I (hold)	Data pins	V _I = 2 V		-75		μА
loz		V _O = V _{CC} or GND	3.6 V		±10	μA
icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ One input at $V_{CC} - 0.6 \text{ V,}$ Other inputs at V_{CC} or GND			500	μА
Ci		$V_I = V_{CC}$ or GND	3.3 V			pF
Co		V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16540 provides a high performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable $(\overline{OE1} \text{ or } \overline{OE2})$ input is high, all corresponding outputs are in the high-impedance state.

The SN74LVC16540 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

10E1	1	O	48	10E2
1Y1 [] 1A1
1Y2 [1A2
GND [4		45	GND
1Y3 [5		44	1A3
1Y4 [43	
v _{cc} [42	
1Y5				1A5
1Y6				1A6
GND [GND
1Y7 [1A7
1Y8 [1A8
2Y1				2A1
2Y2				2A2
GND [] GND
2Y3 [2A3
2Y4 L			32	2A4
v _{cc} [18		31	v_{cc}
2Y5				2A5
2Y6				2A6
GND [GND
2Y7				2A7
2Y8				2A8
2 0E1 [24		25	2 0E 2
		_	_	ı

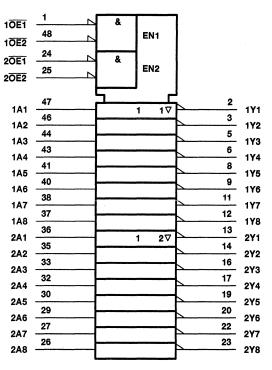
FUNCTION TABLE (each 8-bit section)

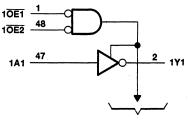
	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	L
Н	X	Χ	Z
Х	н	Χ	Z

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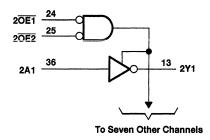
logic symbol†

logic diagram (positive logic)





To Seven Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	/ to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

^{2.} This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷į	Input voltage		0	VCC	٧
٧o	Output voltage		0	Vcc	V
lou	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	"IA
la.	Love lovel as doubt as sweamt	V _{CC} = 2.7 V		12	^
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	vcct	MIN MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
\ _{\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\}		la 12 mA	2.7 V	2.2] v
VOH		IOH = -12 mA	3 V	2.4	7 °
		I _{OH} = -24 mA	3 V	2]
		I _{OL} = 100 μA	MIN to MAX	0.2	
VOL		I _{OL} = 12 mA	2.7 V	0.4	V
		I _{OL} = 24 mA	3 V	0.55	
l _l		V _I = V _{CC} or GND	3.6 V	±5	μА
1	Data sina	V _I = 0.8 V	3 V	75	
l(hold)	Data pins	V _I = 2 V		-75	μА
loz		V _O = V _{CC} or GND	3.6 V	±10	μА
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μА
Δlcc		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	μА
Ci		V _I = V _{CC} or GND	3.3 V		pF
Co		V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

Member of the Texas Instruments Widebus™ Family

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN74LVC16541 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

10E1 [$ _{\scriptscriptstyle 1}$	48	10E2
1Y1 [2	47] 1A1
1Y2 [3	46	1A2
GND [4	45	GND
1Y3 [5] 1A3
1Y4 [] 1A4
v _{cc} [7	42] v _{cc}
1Y5 [1A5
1Y6 [9	40	1A6
GND [39	GND
1Y7 [38	1A7
1Y8 [] 1A8
2Y1 [36	2A1
2Y2		35	2A2
GND [GND
2Y3 [2A3
2Y4 [2A4
V _{CC}	18	31	□ v _{cc}
2Y5 [2A5
2Y6 [2A6
GND [GND
2Y7 [1		2A7
2Y8	1		2 <u>A8</u>
20E1 [24	25	20E2

FUNCTION TABLE (each 8-bit section)

	(000110	DI. 000	
	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
x	Н	X	z

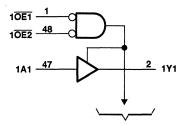
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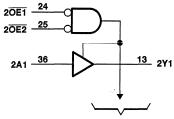
logic symbol†

10E1 EN1 48 10E2 24 & 20E1 25 EN2 20E2 2 1A1 1 🗸 1Y1 46 3 1Y2 1A2 44 5 1A3 1Y3 43 6 1A4 1Y4 41 8 1A5 1Y5 40 9 1A6 **1Y6** 38 11 1A7 1Y7 37 12 1A8 1Y8 36 13 2 ▽ 2Y1 2A1 1 35 14 2A2 2Y2 33 16 2A3 2Y3 32 17 2A4 2Y4 30 19 2A5 2Y5 29 20 2A6 2Y6 27 22 2A7 2Y7 26 2A8 2Y8

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND pins	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package .	0.85 W
	1.2 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧١	Input voltage		0	VCC	٧
Vo	Output voltage		0	Vcc	V
la	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
IOH		V _{CC} = 3 V		-24	III/A
la.	Low-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $			12	4
lOL				24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	Vcc†	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	VCC-0.	2	
V		lov. 10 mA	2.7 V	2.2		v
VOH		IOH = -12 mA	3 V	2.4		v
		I _{OH} = -24 mA	3 V	2		
		l _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
11		V _I = V _{CC} or GND	3.6 V		±5	μА
1	Data pins	V _I = 0.8 V	3 V	75		4
l(hold)		V _I = 2 V	¬	-75		μА
loz		V _O = V _{CC} or GND	3.6 V		±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci		V _I = V _{CC} or GND	3.3 V			pF
Co		VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS317 - NOVEMBER 1993 - REVISED MARCH 1994

Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)		
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1OEAB		1OEBA
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1 CEAB (3 54	1 <u>LEBA</u> 1CEBA GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A1 []	5 52	1B1 1B2
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	V _{CC} [] 1A3 [] 1A4 []	8 49	V _{CC} 1B3 1B4
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	1A5 [GND [1A6 [10 47 11 46] 1B5] GND] 1B6
description	1A7 [] 1A8 []	13 44 14 43] 1B7] 1B8
This 16-bit registered transceiver is designed for low-voltage (3.3 V) $V_{\mbox{CC}}$ operation.	2A1 L 2A2 L 2A3 L	16 41] 2B1] 2B2] 2B3
The SN74LVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate	GND [] 2A4 []	18 39 19 38] GND] 2B4
latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either	2A5 [] : 2A6 [] : V _{CC} [] :	21 36 22 35] 2B5] 2B6] V _{CC}
direction of data flow. The A-to-B enable (CEAB) input must be low in	2A7 [] :	24 33] 2B7] 2B8] CND

mode. With CEAB and OEAB both low, the 3-state
B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

GND [] 25

2CEAB 26

2LEAB [27

20EAB 28

32 🕽 GND

31 2CEBA

30 2LEBA

29 20EBA

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16543 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET (each 8-bit section)

	OUTPUT			
CEAB	CEAB LEAB OEAB			В
Н	Х	X	Х	Z
X	X	Н	Х	Z
L	Н	L	Χ	в ₀ ‡
L	L	L	L	L
L	L	L	Н	н

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

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order to enter data from A or to output data from

B. If CEAB is low and LEAB is low, the A-to-B

latches are transparent; a subsequent low-to-high

transition of LEAB puts the A latches in the storage



[‡] Output level before the indicated steady-state input conditions were established.

10EBA 1EN3 54 G1 1CEBA 55 1LEBA 1C5 1 10EAB 2EN4 3 G2 1CEAB 2 2C6 1LEAB 29 **7EN9** 20EBA 31 G7 2CEBA 30 7C11 2LEBA 28 8EN10 20EAB 26 2CEAB G8 27 2LEAB 8C12 52 1A1 5D 1B1 **⊽**3 6D 4 ▽ 51 1A2 1B2 8 49 1A3 1**B**3 9 48 1A4 1B4 47 10 1A5 1**B**5 12 45 1A6 1**B**6 13 44 1A7 1B7 14 43 1A8 1**B**8 15 42 2A1 ⊽9 11D 2B1 12D 10▽ 16 41 2A2 2B2 17 40 2A3 2B3 19 38 2A4 2B4 20 37 2A5 2B5 21 36 2A6 2B6 23 34 2A7 2B7

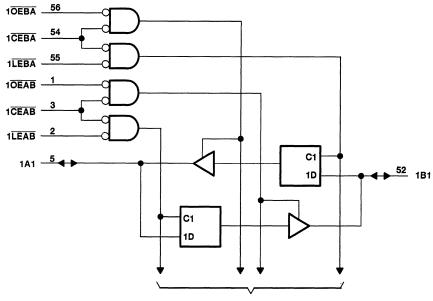
33

2B8

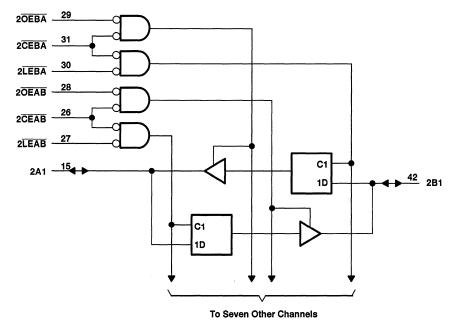
This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

24

logic diagram (positive logic)



To Seven Other Channels





SN74LVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS317 - NOVEMBER 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧.
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	V _I Input voltage			VCC	٧
٧o	Output voltage		0	Vcc	٧
1	High-level output current	V _{CC} = 2.7 V		Vcc	mA
ЮН	riigii-level output current	V _{CC} = 3 V	-12 -24	IIIA	
la.	Low-level output current	V _{CC} = 2.7 V		12	mΑ
lor	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

SN74LVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS317 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
		I _{OH} = -100 μA		V _{CC} -0	.2	
V		lov. 12 mA	2.7 V	2.2		V
VOH		IOH = -12 mA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
VOL		I _{OL} = 100 μA	MIN to MAX		0.2	
		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
lį.	Control inputs	V _I = V _{CC} or GND	3.6 V		±5	μА
ha is	A or B ports	V _I = 0.8 V	3 V	75		μА
I(hold)	A or B ports	V _I = 2 V		-75		μΑ
loz‡		$V_O = V_{CC}$ or GND	3.6 V		±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	VO = VCC or GND	3.3 V			рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC16544 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS351 - MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL (TOP	
 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1OEAB 1 1LEAB 2	56 10EBA 55 1LEBA
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1CEAB [3 GND [4	54 1 1 TEBA 54 1 TEBA 53 1 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A1 [5 1A2 [6	52 1 1B1 51 1 1B2
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown	V _{CC} [] 7 1A3 [] 8	50 V _{CC} 49 183
Resistors Package Options Include Plastic 300-mil	1A4 [9 1A5 [10	48 1 1B4 47 1 1B5
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	GND [11 1A6 [12	46 GND 45 1B6
description	1A7 [13 1A8 [14	44 1 1B7 43 1 1B8
This 16-bit registered transceiver is designed for low-voltage (3.3 V) V _{CC} operation.	2A1	42] 2B1 41] 2B2
The SN74LVC16544 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate	2A3 [] 17 GND [] 18 2A4 [] 19	40
latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each	2A5 [20 2A6 [21	37 2B5 36 2B6
register to permit independent control in either direction of data flow.	V _{CC} [22 2A7 [23	35 V _{CC} 34 2B7
The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from	2A8 [24 GND [25	33
B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high	2 <mark>CEAB</mark> [26 2LEAB [27 2OEAB [28	31] 2 <u>CEBA</u> 30] 2 <u>LEBA</u> 29] 2 <u>OEBA</u>
transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state	20EAB (1 28	29 L 20EBA

B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16544 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET (each 8-bit section)

	INPUTS					
CEAB	LEAB	OEAB	Α	В		
Н	Х	X	Χ	Z		
L	Х	Н	Χ	Z		
L	Н	L	Χ	в ₀ ‡		
L	L	L	L	Н		
L	L	L	Н	L		

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

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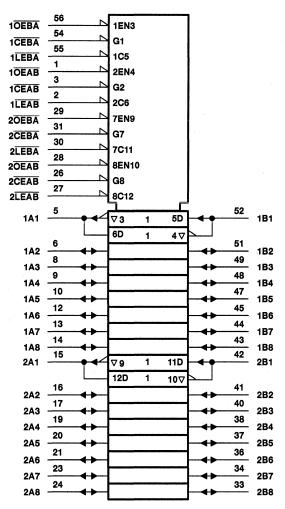


[‡] Output level before the indicated steady-state input conditions were established.

SN74LVC16544 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

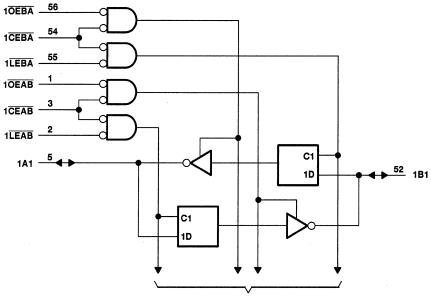
SCAS351 - MARCH 1994

logic symbol†

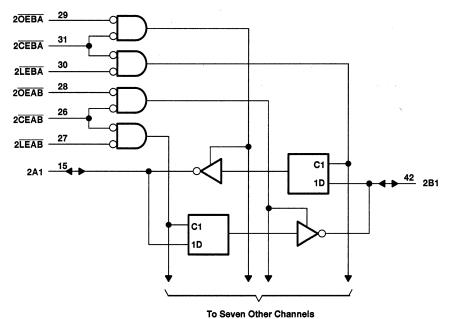


 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels





SN74LVC16544 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS351 - MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air): DGG package .	
DL package	
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Supply voltage		2.7	3.6	٧
High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		8.0	٧
Input voltage		0	VCC	٧
Output voltage		0	VCC	٧
High-level output ourrent	V _{CC} = 2.7 V		-12 -24	mA
riigirievei output current	V _{CC} = 3 V			
Low level output ourrent	V _{CC} = 2.7 V		12	mA
VCC = 3 V			24	IIIA.
Input transition rise or fall rate		0	10	ns/V
Operating free-air temperature		-40	85	္
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current Input transition rise or fall rate	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$	Supply voltage 2.7 High-level input voltage V _{CC} = 2.7 V to 3.6 V 2 Low-level input voltage V _{CC} = 2.7 V to 3.6 V Input voltage 0 Output voltage 0 High-level output current V _{CC} = 2.7 V V _{CC} = 3 V V _{CC} = 2.7 V Low-level output current V _{CC} = 3 V Input transition rise or fall rate 0	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

NOTE 3: Unused or floating control pins must be held high or low.



SN74LVC16544 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS351 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{CC} †	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	.2	
V		lou 12 mA	2.7 V	2.2		V
VOH		IOH = −12 mA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
lį	Control inputs	VI = VCC or GND	3.6 V		±5	μА
1.0	A or B ports	V _I = 0.8 V	3 V	75		
I(hold)	A or B ports	V _I = 2 V	3 V	-75		μА
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	VO = VCC or GND	3.3 V			рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS318 - NOVEMBER 1993 - REVISED MARCH 1994

Member of the Texas Instruments Widebus™ Family		L PACKAGE VIEW)
 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1DIR 1	56 1 0 1 0 10 10 10 10 10 10 10 10 10 10 10 10 10
 Supports Unregulated Battery Operation Down to 2.7 V 	1CLKAB	55 1 1CLKBA 54 1 1SBA
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1A1 [5 1A2 [6	53 GND 52 1B1 51 1B2
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	V _{CC} [] 7 1A3 [] 8	50 V _{CC} 49 1 1B3
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	1A4 🗍 9 1A5 🖟 10	48] 1B4 47] 1B5
 Flow-Through Architecture Optimizes PCB Layout 	GND [] 11 1A6 [] 12	46] GND 45] 1B6
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1A7 [] 13 1A8 [] 14 2A1 [] 15	44
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	2A2 [] 16 2A3 [] 17	41 2B2 40 2B3
Small-Outline (DGG) Packages	GND [18 2A4 [19 2A5 [20	39 GND 38 2B4 37 2B5
description	2A6 [] 21	36 2B6
This 16-bit bus transceiver and register is designed for low-voltage (3.3 V) V _{CC} operation.	V _{CC} [22 2A7 [23	35 V _{CC} 34 2B7
The SN74LVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of his transceiver circuits D-type	2A8 [24 GND [25 2SAB [26	33] 2B8 32] GND 31] 2SBA

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16646.

2CLKAB [27

2DIR

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16646 is characterized for operation from -40°C to 85°C.

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consists of bus transceiver circuits, D-type

flip-flops, and control circuitry arranged for

multiplexed transmission of data directly from the

input bus or from the internal registers.



30 2CLKBA

29 1 20E

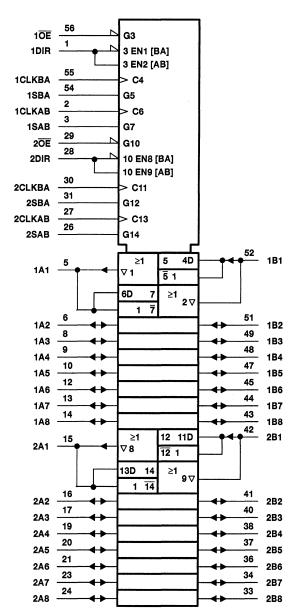
BUS B **BUSA** ŌĒ. DIR CLKAB CLKBA SAB SBA ŌĒ DIR CLKAB CLKBA SAB SBA Н Χ L Χ L L Х Х Χ L **REAL-TIME TRANSFER REAL-TIME TRANSFER BUS B TO BUS A BUS A TO BUS B** BUS B BUS B **BUSA BUSA** ŌĒ ŌĒ SBA CLKAB CLKBA SAB SBA DIR CLKAB CLKBA SAB DIR Х Х 1 Χ Х Х Х L Х H or L Н Χ Х 1 Х Χ Х Н H or L Χ Н Х Н Χ 1 1 Х Χ STORAGE FROM TRANSFER STORED DATA

Figure 1. Bus-Management Functions

TO A AND/OR B

A, B, OR A AND B

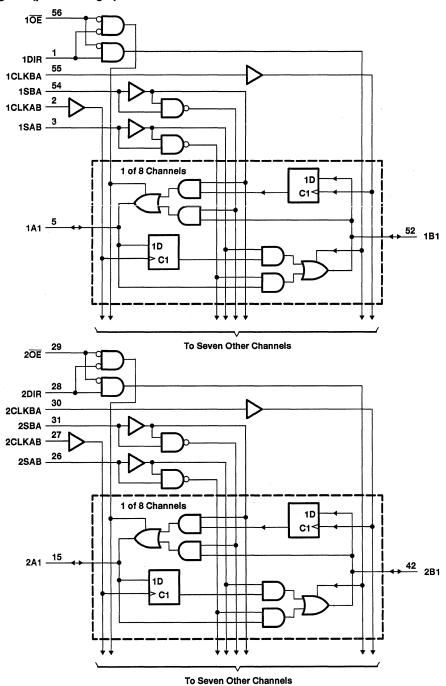




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





SN74LVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS318 - NOVEMBER 1993 - REVISED MARCH 1994

FUNCTION TABLE

	INPUTS					DATA I/Os		OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
X	X	1	X	Х	X	Input	Unspecified [†]	Store A, B unspecified [†]
×	X	X	1	X	Х	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	↑	1	Х	X	Input	Input	Store A and B data
Н	X	H or L	H or L	Х	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	X	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	H or L	Х	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	X	Input	Output	Real-time A data to B bus
L	Н	H or L	Х	Н	Х	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	-0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air):	DGG package 1 W
· · · · · · · · · · · · · · · · · · ·	DL package 1.4 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Supply voltage		2.7	3.6	V
High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
Input voltage		0	Vcc	٧
Output voltage		0	VCC	٧
High level output ourrent	V _{CC} = 2.7 V		-12	mA
nigri-level odiput current	V _{CC} = 3 V		-24	IIIA
Low level output ourrent	V _{CC} = 2.7 V		12	mA
High-level input voltage Low-level input voltage Input voltage	V _{CC} = 3 V		24	111/2
Input transition rise or fall rate		0	10	ns/V
Operating free-air temperature		-40	85	°C
	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current Input transition rise or fall rate	High-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ Low-level input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ Input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ Unput voltage $V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3 \text{ V}$ Low-level output current $V_{CC} = 3 \text{ V}$ Input transition rise or fall rate	Supply voltage 2.7 High-level input voltage VCC = 2.7 V to 3.6 V 2 Low-level input voltage VCC = 2.7 V to 3.6 V Input voltage 0 Output voltage 0 High-level output current VCC = 2.7 V V VCC = 3 V Low-level output current VCC = 2.7 V V VCC = 3 V Input transition rise or fall rate 0	Supply voltage 2.7 3.6 High-level input voltage VCC = 2.7 V to 3.6 V 2 Low-level input voltage VCC = 2.7 V to 3.6 V 0.8 Input voltage 0 VCC Output voltage 0 VCC High-level output current VCC = 2.7 V -12 VCC = 3 V -24 Low-level output current VCC = 2.7 V 12 VCC = 3 V 24 Input transition rise or fall rate 0 10

NOTE 3: Unused or floating control pins must be held high or low.



SN74LVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA		V _{CC} -0	.2	
Vall		lou 12 mA	2.7 V	2.2		V
VOH		IOH = -12 mA	3 V	2.4		٧ .
		I _{OH} = -24 mA	3 V	2		
VoL		I _{OL} = 100 μA	MIN to MAX		0.2	
		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
Ч	Control inputs	V _I = V _{CC} or GND	3.6 V		±5	μΑ
1	A ou B monto	V _I = 0.8 V	3 V	75		4
I(hold)	A or B ports	V _I = 2 V	¬	-75		μΑ
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	VO = VCC or GND	3.3 V			рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]mbox{\ensuremath{\,^{\ddagger}}}\mbox{\ensuremath{\,^{For}\, I/O}}\mbox{\ensuremath{\,^{I/O}}}\mbox{\ensuremat$

SN74LVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16652.

DGG OR DL PACKAGE (TOP VIEW)

10EAB	₁	56	1OEBA
1CLKAB 🛚	2	55	1CLKBA
1SAB	3	54] 1SBA
GND [GND
1A1 🛚	5	52] 1B1
1A2 🕻		51] 1B2
v _{cc} [7	50] v _{cc}
1A3 L	8	49] 1B3
1A4 🛚		48] 1B4
1A5 🛚		47] 1B5
GND [GND
1A6 🛚] 1B6
1A7 🛭		44] 1B7
1A8 🛚		43] 1B8
2A1 🛚		42	2B1
2A2 🏻			2B2
2A3 🛚		40] 2B3
GND 🛚		39	GND
2A4 🏻			2B4
2A5 🏻			2B5
2A6 🛚		36	2B6
v _{cc} [22	35] v _{cc}
2A7 🛭			2B7
2A8 🛚		33	2B8
GND 🛚		32	GND
2SAB			2SBA
2CLKAB			2CLKBA
20EAB	28	29	2 OEBA

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16652 is characterized for operation from -40°C to 85°C.

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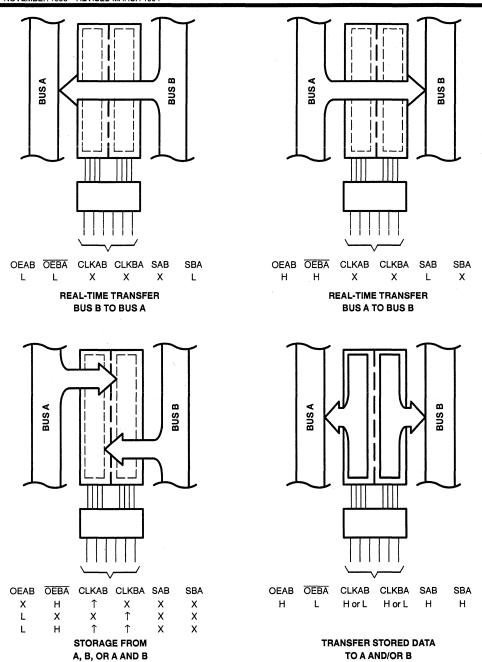
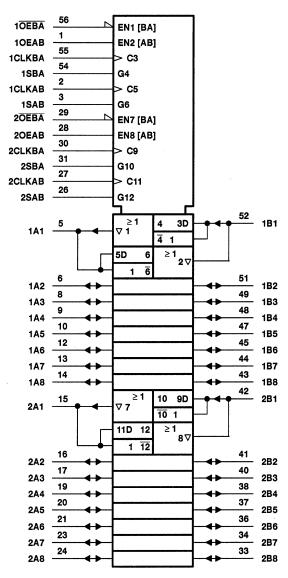


Figure 1. Bus-Management Functions

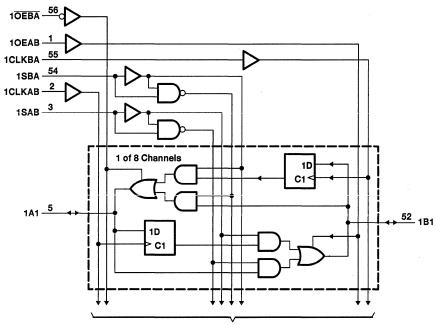


logic symbol†

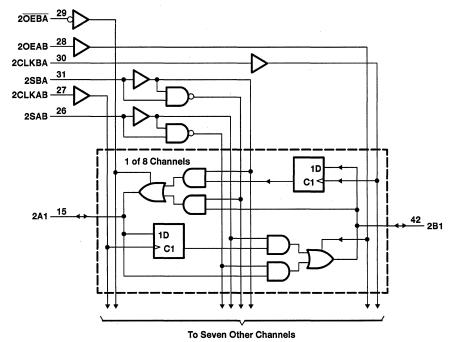


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS319 - NOVEMBER 1993 - REVISED MARCH 1994



To Seven Other Channels



INSTRUMENTS

SN74LVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS			DATA I/OT		OPERATION OR FUNCTION			
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	X	Input	Input	Isolation
L	Н	1	1	X	Х	Input	Input	Store A and B data
X	Н	↑	H or L	X	X	Input	Unspecified [‡]	Store A, hold B
Н	Н	1	1	X‡	X	Input	Output	Store A in both registers
L	X	H or L	1	Х	X	Unspecified‡	Input	Hold A, store B
L	L	1	1	X	X‡	Output	Input	Store B in both registers
L	L	Χ	X	Х	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	X	н	Output	input	Stored B data to A bus
Н	н	X	X	L	Х	Input	Output	Real-time A data to B bus
Н	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus
н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package	
DL package	1.4 W
Storage temperature range	65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

SN74LVC16652 **16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS**

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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	٧
۷o	Output voltage		0	VCC	٧
lau	V _{CC} = 2.7 V			-12	mA
ЮН	High-level output current	V _{CC} = 3 V	-	-24	111/
la.	Law lavel output augment	V _{CC} = 2.7 V		12	A
lOL	Low-level output current V _{CC} = 3 V				mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	v _{CC} †	MIN	MIN MAX	
,		I _{OH} = -100 μA	MIN to MAX	VCC-0	.2	
1/0		I _{OH} = -12 mA	2.7 V	2.2		v
VOH		IOH = - 12 IIIA	3 V	2.4		
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
l _l	Control inputs	V _I = V _{CC} or GND	3.6 V		±5	μА
	A or B morto	V _I = 0.8 V	3 V	75		μА
I(hold)	A or B ports	V _I = 2 V		-75		
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	- 3.3 V			pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]mbox{$^{\pm}$}$ For I/O ports, the parameter IOZ includes the input leakage current.

SN74LVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE (TOP VIEW)

10EAB [] 1

1CLKAB 12

1CEAB 13

GND 4

1A1 **[**]5

1A2 📙 6

V_{CC} **4**7

1A3 🛮 8

1A4 **[**]9

1A5 🛛 10

1A6 🛮 12

1A7 🛮 13

1A8 🛮 14

2A1 15

2A2 II 16

2A3 L 17

GND []18

2A4 [] 19 2A5 [] 20

2A6 L 21

V_{CC} []22

2A7 🛮 23

2A8 🛮 24

GND 125

2CEAB 1 26

2CLKAB 127

20EAB | 28

GND []11

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56 1 1 OEBA

55 1 1CLKBA

54 1 1 CEBA

53 GND

52 1B1

51 1B2

50 V_{CC}

49 1B3 48 1B4

47 1B5

46**∏** GND

45 1 1B6

44 1 1B7

43 1B8

42 2B1

41 1 2B2

40 2B3

39 GND

38 2B4

37 2B5

36 2B6

35 V_{CC}

34 2B7

33 2B8

32 | GND

31 2 2 CEBA

30 2CLKBA

29 20EBA

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or

CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16952 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

		OUTPUT			
	CLKENAB	CLKAB	OEAB	Α	В
	Н	Х	L	Х	B ₀ ‡
١	Χ	L	L	Χ	B ₀ ‡ B ₀ ‡
١	L	1	L.	L	L
	L	1	L	Н	н
1	Χ	X	Н	Χ	z

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

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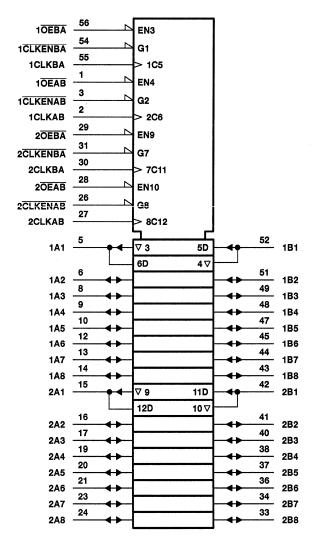


[‡]Level of B before the indicated steady-state input conditions were established.

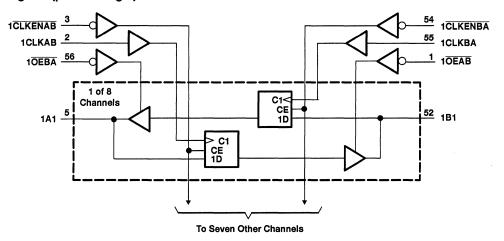
SN74LVC16952 **16-BIT REGISTERED TRANSCEIVER** WITH 3-STATE OUTPUTS

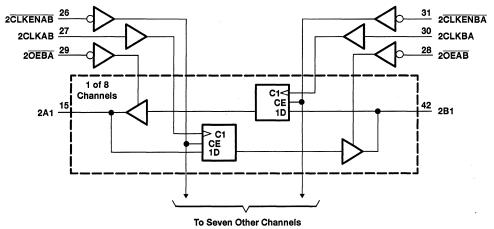
SCAS320 - NOVEMBER 1993 - REVISED MARCH 1994

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package .	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
VCC	Supply voltage		2.7	3.6	V	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V	
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧	
VI	Input voltage		0	VCC	٧	
Vo	Output voltage		0	VCC	٧	
10	High-level output current	V _{CC} = 2.7 V		-12	mA	
IOH,	High-level output current	V _{CC} = 3 V		-24] "''^]	
la:	Low-level output current	V _{CC} = 2.7 V		12	mA	
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	ô	

NOTE 3: Unused or floating control pins must be held high or low.

16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS SCAS320 - NOVEMBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	vcct	MIN MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
		10 = 4	2.7 V	2.2] ,
VOH		IOH = -12 mA	3 V	2.4	7 °
		I _{OH} = -24 mA	3 V	2	1
		I _{OL} = 100 μA	MIN to MAX	0.2	
V_{OL}		I _{OL} = 12 mA	2.7 V	0.4	.] v
		I _{OL} = 24 mA	3 V	0.55	
l _l	Control inputs	VI = VCC or GND	3.6 V	±6	μА
lia in	A or B ports	V _I = 0.8 V	3 V	75	
l(hold)	A of B ports	V _I = 2 V		-75	μA
loz‡		V _O = V _{CC} or GND	3.6 V	±10	μА
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μА
ΔlCC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		500	μА
C _i .	Control inputs	V _I = V _{CC} or GND	3.3 V		pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

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ALVC Widebus™

Features

- State-of-the-art 0.6-μ EPIC-III™ CMOS process
- No input-diode clamp to V_{CC}
- Low standby current (20 μA)
- –24-mA/24-mA drive current
- 2.7-V to 3.6-V V_{CC} range
- JEDEC SSOP Widebus™ and EIAJ TSSOP Shrink Widebus™ packaging

Benefits

- Propagation delays as fast as 4 ns maximum for improved performance
- Saves power, extends battery life
- Drives transmission lines down to 50 Ω
- Fully characterized for unregulated battery operation
- Saves board space and weight; TSSOP compatible with PCMCIA standards

SN74ALVC16240 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS415 - JANUARY 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>OE</u> 1 48 2 <u>OE</u>
Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater	1Y1
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 [15 44] 1A3 1Y4 [16 43] 1A4 V _{CC} [17 42] V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2Y1
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	GND [] 10 39
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	3Y1
description	3Y4 🛛 17 32 🗓 3A4
This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V _{CC} operation.	V _{CC} [] 18 31] V _{CC} 4Y1 [] 19 30] 4A1 4Y2 [] 20 29] 4A2
The SN74ALVC16240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	GND [21 28] GND 4Y3 [22 27] 4A3 4Y4 [23 26] 4A4 4OE [24 25] 3OE
The device can be used as four 4-bit buffers, two	·

The SN74ALVC16240 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

l	INP	JTS	OUTPUT
	ŌĒ	Α	Y
	L	Н	L
	L	L	Н
	Н	Χ	Z

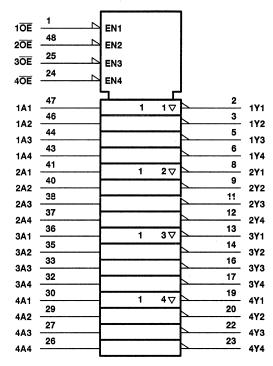
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8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical \overline{OE} (active-low

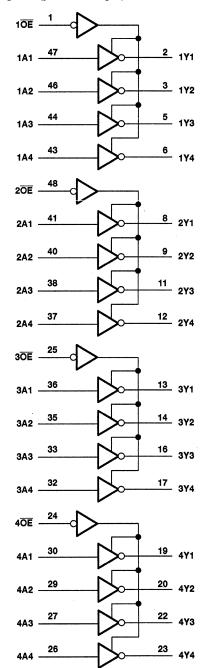
output-enable) inputs.



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
Vi	Input voltage		0	VCC	V
۷o	Output voltage		0	2	٧
1	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
IOH		V _{CC} = 3 V		-24	IIIA
1	Low lovel output ourrent	V _{CC} = 2.7 V		12	mΑ
lOL	Low-level output current V _{CC} = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ô



SN74ALVC16240 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS415 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	lou 12 m/	2.7 V	2.2		V
Voн	I _{OH} = -12 mA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	v
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = V _{CC} or GND	3.6 V		±5	μА
1	V _I = 0.8 V	3 V	75		
^I I(hold)	V _I = 2 V		-75		μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS250 - JANUARY 1993 - REVISED JANUARY 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)			
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1	48 2 0 E		
Designed to Facilitate Incident-Wave	1Y1 [] 2 1Y2 [] 3	47 🛛 1A1 46 🖟 1A2		
Switching for Line Impedances of 50 Ω or Greater	GND 🗓 4	45 GND		
	1Y3] 5	44 🛭 1A3		
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown	1Y4 [] 6	43 1A4		
Resistors	V _{CC}	42 V _{CC}		
Package Options Include Plastic 300-mil	2Y2 [] 9	41 2A1 40 2A2		
Shrink Small-Outline (DL) and Thin Shrink	GND 1 10	39 GND		
Small-Outline (DGG) Packages	2Y3 1 11	38 2A3		
	2Y4 🛮 12	37 🛭 2A4		
description	3Y1 🛛 13	36 🛭 3A1		
This 16-bit buffer/driver is designed for 2.7-V to	3Y2 🛭 14	35 [] 3A2		
3.6-V V _{CC} operation.	GND 🛭 15	34 GND		
The SN74ALVC16244 is designed specifically to	3Y3 [] 16	33 A3		
improve both the performance and density of	3Y4 [17	32 3A4 31 V _{CC}		
3-state memory address drivers, clock drivers,	V _{CC}	30 4A1		
and bus-oriented receivers and transmitters.	4Y2 1 20	29 AA2		
The device can be used as four 4-bit buffers, two	GND 🛮 21	28 GND		
8-bit buffers, or one 16-bit buffer. It provides true	4Y3 🛛 22	27] 4A3		
outputs and symmetrical OE (active-low output-	4Y4 🛮 23	26 2 4A4		
enable) inputs.	4 0E 🛮 24	25 3OE		
Active has held aircuitry is provided to held				

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	Н
L	L	L
Ι	Х	Z

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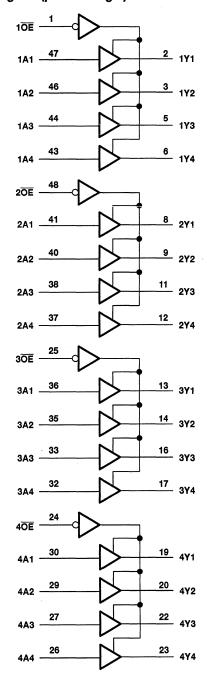


SN74ALVC16244 **16-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCAS250 - JANUARY 1993 - REVISED JANUARY 1994

logic symbol†

10E	1	EN1				
20E	48	EN2				
30E	25					
	24	ENS				
4OE		EN4				
1A1	47		1	1▽	2	1Y1
1A2	46	<u> </u>		· *	3	1Y2
1A3	44				5	1Y3
1A4	43	 			6	1Y4
	41		1	2 ▽	8	
2A1	40			2 ∨	9	2Y1
2A2	38	}	,		11	2Y2
2A3	37	 			12	2Y3
2A4	36	<u> </u>			13	2Y4
3A1	35	 	1	3 ▽	14	3Y1
3A2	33	 			16	3Y2
3A3	32	 			17	3 Y 3
3A4	30	 			19	3Y4
4A1	29	<u> </u>	1	4 ▽	20	4Y1
4A2	27	<u> </u>			22	4Y2
4A3	26	<u> </u>			23	4Y3
4A4		<u>L</u>				4Y4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





SN74ALVC16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS250 - JANUARY 1993 - REVISED JANUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6	٧
Input voltage range, V _I (see Note 1)	
Output voltage range, V_O (see Notes 1 and 2)	٧
Input clamp current, $I_{ K }(V_{ } < 0)$	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	Α
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package 0.85 V	Ν
DL package 1.2 V	Ν
Storage temperature range	C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
۷ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
۷į	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
lou	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	A	
ЮН		V _{CC} = 3 V		-24	mA
lo:	V _{CC} = 2.7 V		12	A	
lOL	Low-level output current V _{CC} = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	. °C



SN74ALVC16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS250 - JANUARY 1993 - REVISED JANUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
V		laur 10 mA	2.7 V	2.2		v	
VOH		I _{OH} = -12 mA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	V	
		I _{OL} = 24 mA	3 V		0.55		
lį	Inputs	V _I = V _{CC} or GND	3.6 V		±5	μА	
l	Doto nino	V _I = 0.8 V	0.1/	75			
I (hold)	Data pins	V _I = 2 V	3 V	-75		μΑ	
loz		V _O = V _{CC} or GND	3.6 V		±10	μА	
icc		$V_{\rm I} = V_{\rm CC}$ or GND, $I_{\rm O} = 0$	3.6 V		40	μΑ	
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА	
Cį		V _I = V _{CC} or GND	3.3 V	3.5		pF	
Co		V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM TO		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
PANAMETEN	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
^t pd	A	Υ	1	2.2	3.6		4	ns
t _{en}	ŌĒ	Υ	1	2.7	5		6	ns
^t dis	ŌĒ	Υ	1	2.9	5		5.2	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER		TEST CONDITIONS	TYP	UNIT	
	Deves dissination considers and his	Outputs enabled	O: 50 = 5 40 MU=	16	
Opd P	Power dissipation capacitance per bit	Outputs disabled	$C_L = 50 \text{ pF, f} = 10 \text{ MHz}$	5	p⊦

SN74ALVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS419 - JANUARY 1993 - REVISED JANUARY 1994

•	Member of	the Texas	Instruments
	Widebus™	Family	

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V $\rm V_{CC}$ operation.

The SN74ALVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

DGG OR DL PACKAGE (TOP VIEW)

1DIR		48	
1B1			1A1
1B2		46	1A2
GND[4	45] GND
1B3	5	44] 1A3
1B4 [43] 1A4
v _{cc} [7	42] v _{cc}
1B5	8		1A5
1B6	9	40	1A6
GND [10] GND
1B7		38	1A7
1B8	12		1A8
2B1			2A1
2B2	14		2A2
GND [GND
2B3			2A3
2B4 [2A4
v _{cc} [18	31] v _{cc}
2B5 [19		2A5
2B6			2A6
GND [GND
2B7			2A7
2B8 [2A8
2DIR [24	25	2 <u>0E</u>

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16245 is characterized for operation from -40°C to 85°C.

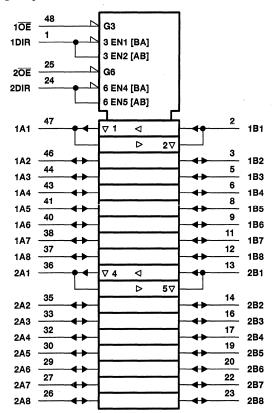
FUNCTION TABLE (each 8-bit section)

- 1	INP	UTS	OPERATION
	ŌĒ	DIR	OPERATION
	L	L	B data to A bus
	L	Н	A data to B bus
	Н	X	Isolation

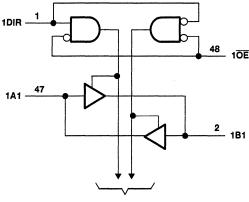
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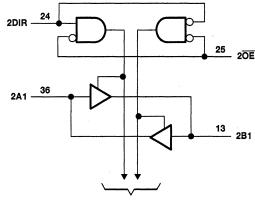
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



To Seven Other Channels



To Seven Other Channels

SN74ALVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS419 - JANUARY 1993 - REVISED JANUARY 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage			3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI			0	VCC	٧
Vo	Output voltage		0	VCC	V
lou	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	riigir-ievei output current	V _{CC} = 3 V		-24	ША
	Low-level output current	V _{CC} = 2.7 V		12	mΑ
IOL	V _{CC} = 3 V			24	111/
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ပ္



SN74ALVC16245 **16-BIT BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCAS419 - JANUARY 1993 - REVISED JANUARY 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	vcct	MIN	TYP MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V		Jan. 10 mA	2.7 V	2.2		v
VOH		IOH = −12 mA	3 V	2.4		v
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	v
		I _{OL} = 24 mA	3 V		0.55	
l _l	Control pins	V _I = V _{CC} or GND	3.6 V		±5	μA
1	Data I/Os	V _I = 0.8 V	0.14	75		μА
l(hold)		V _I = 2 V	3 V	-75		
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		V _I = V _{CC} or GND, I _O = 0	3.6 V		40	μА
ΔlCC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		3.5	pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
PANAMETER			MIN	TYPT	MAX	MIN	MAX	UNII
^t pd	A or B	B or A	1	2.2	3.6		4	ns
t _{en}	ŌĒ	B or A	1	2.7	5		6	ns
^t dis	ŌĒ	B or A	. 1	2.9	5		5.2	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER		TEST CO	TYP	UNIT		
	Device dissination considers and hit	Outputs enabled	C: 50 = F	4 10 MU=	28	
Cpd	Power dissipation capacitance per bit	Outputs disabled	$C_L = 50 pF$,	f = 10 MHz	4	рF

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SCAS416 - MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1DIR 1 48 1 OE 1B1 2 47 1A1	
Inputs Are TTL-Voltage Compatible	1B2 3 46 1A2	
Noninverting Outputs	GND 0 4 45 0 GND	
Flow-Through Architecture Optimizes	1B3 0 5 44 0 1A3	
PCB Layout	1B4 1 6 43 1 1A4	
Bus-Hold On Data Inputs Eliminates the	(5 V) V _{CCB} 7 42 V _{CCA} (3.3 V	' \
Need for External Pullup/Pulldown	1B5 8 41 1 1A5	′
Resistors	1B6 0 9 40 0 1A6	
Package Options Include Plastic 300-mil	GND 1 10 39 GND	
Shrink Small-Outline (DL) and Thin Shrink	1B7 🛛 11 38 🗓 1A7	
Small-Outline (DGG) Packages	1B8 🖟 12 37 🖟 1A8	
oman-outline (bdd) r ackages	2B1 🛛 13 36 🗓 2A1	
description	2B2 🛮 14 35 🗓 2A2	
·	GND 🛛 15 34 🗓 GND	
This 16-bit (dual-octal) noninverting bus	2B3 🛛 16 33 🗓 2A3	
transceiver contains two separate supply rails;	2B4 🛛 17 32 🗍 2A4	
B port has V _{CCB} which is set at 5 V, and A port has	(5 V) V _{CCB} 18 31 2 V _{CCA} (3.3 V)
V _{CCA} which is set to operate at 3.3 V. This allows	2B5 🛮 19 30 🗓 2A5	
for translation from a 3.3-V to a 5-V environment	2B6 🛛 20 29 🖟 2A6	
and vice-versa.	GND 🛛 21 28 🖟 GND	
The SN74ALVC164245 is designed for	2B7 🛛 22 27 🗓 2A7	
asynchronous communication between data	2B8 🛛 23 26 🖸 2A8	
buses. The control-function implementation	2DIR 🛛 24 25 🗓 2ŌĒ	
minimizes external timing requirements.	· • • · · ·	

The SN74ALVC164245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC164245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

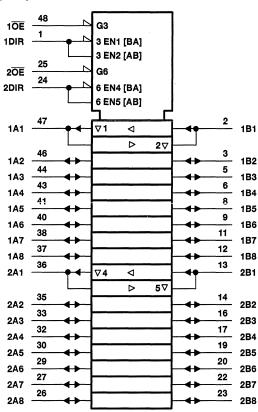
		(000011	
	INP	UTS	OPERATION
i	OE	DIR	OPERATION
	L	L	B data to A bus
	L	Н	A data to B bus
	Н	Χ	Isolation

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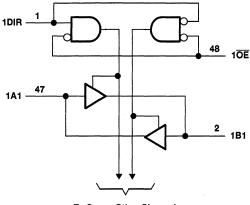


SCAS416 - MARCH 1994

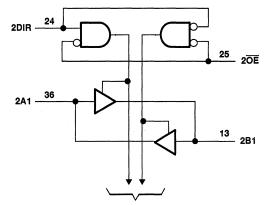
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



To Seven Other Channels



To Seven Other Channels

SCAS416 - MARCH 1994

Supply voltage range, V _{CCB}	_0.5 V to 6 V
Input voltage range, V _I (see Note 1)	V _{CCB} + 0.5 V
Output voltage range, V _O (see Note 1)	V _{CCB} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CCB})	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CCB})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CCB})	±50 mA
Continuous current through V _{CCB} or GND	

NOTE 1: This value is limited to 6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCA} at 3.3 V (unless otherwise noted)[†]

Supply voltage range, V _{CCA}		-0.5 V	to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 2)		-0.5 V	to 4.6 V
Input voltage range, V _I (I/O ports) (see Note 2)	-0.5 V	to V _{CC}	4 + 0.5 V
Output voltage range, VO (see Note 2)	-0.5 V	to V _{CC}	4 + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)			-50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CCA})			±50 mA
Continuous output current, I _O (V _O = 0 to V _{CCA})			±50 mA
Continuous current through V _{CCA} or GND			±100 mA

NOTE 2: This value is limited to 4.6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V or for V_{CCA} at 3.3 V (unless otherwise noted)

Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range –65°C to	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



recommended operating conditions for V_{CCB} at 5 V

		MIN	NOM	MAX	UNIT
VCCB	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2	-		V
VIL	Low-level input voltage			0.8	٧
VI	Input voltage	0		VCCB	V
۷o	Output voltage	0		VCCB	V
ЮН	High-level output current			-24	mA
lOL	Low-level output current			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	ns/V
TA	Operating free-air temperature	-40		85	°C

recommended operating conditions for $\mbox{V}_{\mbox{CCA}}$ at 3.3 \mbox{V}

			MIN	MAX	UNIT
VCCA	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CCA} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage	V _{CCA} = 2.7 V to 3.6 V		0.8	٧
۷ı	Input voltage		0	VCCA	V
٧o	Output voltage		0	VCCA	٧
la	High-level output current	V _{CCA} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CCA} = 3 V		-24	
la:	Low-level output current	V _{CCA} = 2.7 V		12	mA
IOL	Low-level output current	V _{CCA} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



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electrical characteristics over recommended operating free-air temperature range for $V_{CCB} = 5 \text{ V}$ (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{CCB}	MIN	MAX	UNIT
		I _{OH} = -100 μA	4.5 V	4.3		
Vон		ΙΟΗ = -100 μΑ	5.5 V	5.3		v
		Jan. 24 mA	4.5 V	3.7		V
		IOH = -24 mA	5.5 V	4.7		
		la. 100 nA	4.5 V		0.2	
Was		I _{OL} = 100 μA	5.5 V		0.2	v
VOL		La. 24 m4	4.5 V		0.55	V
		I _{OL} = 24 mA	5.5 V		0.55	
łı	Control pins	V _I = V _{CCB} or GND	5.5 V		5	μА
loz†	A or B ports	V _O = V _{CCB} or GND	5.5 V			μА
lcc		$V_I = V_{CCB}$ or GND, $I_O = 0$	5.5 V			μА
ΔICC [‡]		One input at 3.4 V, Other inputs at V _{CCB} or GND				μА
Ci	Control inputs	V _I = V _{CCB} or GND	5 V			pF
Cio	A or B ports	V _O = V _{CCB} or GND	5 V			pF

electrical characteristics over recommended operating free-air temperature range for $V_{CCA} = 3.3 \text{ V}$ (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCCAT	MIN	MAX	UNIT
		l _{OH} = -100 μA	MIN to MAX	VCC-0	.2	
		10 10 1	2.7 V	2.2		v
VOH		I _{OH} = −12 mA	3 V	2.4		v
Ì		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
11	Control pins	V _I = V _{CCA} or GND	3.6 V		5	μА
1	Deta I/Os	V _I = 0.8 V	3 V	75		
l(hold)	Data I/Os	V _I = 2 V		-75		μА
loz‡		VO = VCCA or GND	3.6 V			μА
Icc		V _I = V _{CCA} or GND, I _O = 0	3.6 V			μА
ΔI _{CC} §		V_{CCA} = 3 V to 3.6 V, One input at V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND				μA
Ci	Control inputs	V _I = V _{CCA} or GND	3.3 V			pF
Cio	A or B ports	V _O = V _{CCA} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCCB.

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCI WITH 3-STATE OUTPUTS

SCAS252 - OCTOBER 1993 - REVISED MARCH 1994

EPIC™ (Enhanced-Performance Implanted)
CMOS) Submicron Process
 Member of the Texas Instruments
<i>Widebus</i> ™ Family

- **Supports Unregulated Battery Operation** Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{CC} Overshoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Flow-Through Architecture Optimizes **PCB Layout**
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) **Packages**

description

The SN74ALVC16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single path. Typical applications multiplexing and/or demultiplexing of address and data information in microprocessor- or businterface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A-to-B direction.

DGG OR DL PACKAGE (TOP VIEW)

OEA [1	U	56	OE2B
LE1B				LEA2B
2B3				2B4
GND [3			GND
2B2] 5		52	2B5
2B1 [6		51	2B6
V _{CC} [7		50] v _{cc}
A1 [2B7
A2 [48	2B8
A3 [47] 2B9
GND [11] GND
A4 [2B10
A5 [13			2B11
A6 [43]2B12
A7 [] 1B12
A8 [41] 1B11
A9 [] 1B10
GND [GND
A10 [] 1B9
A11 [] 1B8
A12 [21] 1B7
V _{CC}	22]v _{cc}
1B1 [] 1B6
1B2 [] 1B5
GND [GND
1B3 [] 1B4
LE2B [LEA1B
SEL[28		29	OE1B

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16260 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16260 is characterized for operation from -40°C to 85°C.

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SN74ALVC16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS252 - OCTOBER 1993 - REVISED MARCH 1994

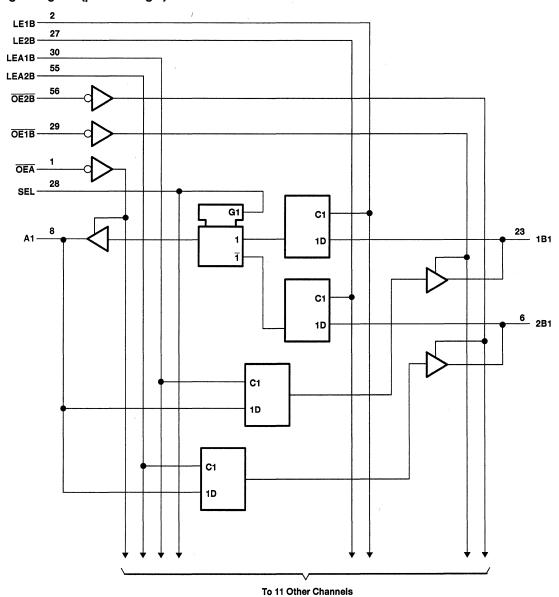
Function Tables

B TO A (OEB = H)

		INPUTS				
1B	2B	SEL	LE1B	LE2B	OEA	A
Н	Х	Н	Н	X	L	Н
L	Χ	Н	Н	X	L	L
Х	Χ	Н	L	X	L	. A ₀
Х	Н	L	X	Н	L	Н
Х	L	L	X	Н	L	Ľ
Х	Χ	L	Χ	L	L	A ₀
Х	Х	Х	Χ	Χ	Н	Z

A TO B (OEA = H)

			OUT	PUTS		
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L.	Н	Н	L	L	L	L
Н	Н	L	L	L	н	2B ₀
L	Н	L	L	L	L	2B ₀
Н	L	Н	L	L	1B ₀	н
L	L	Н	L	Ĺ	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
Х	Х	Χ	Н	Н	Z	Z
X	X	Χ	L	Н	Active	Z
X	Х	X	Н	L	Z	Active
Х	Х	Х	L	L	Active	Active





SN74ALVC16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS252 - OCTOBER 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package .	1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	VCC	٧
۷o	Output voltage		0	VCC	٧
	High-level output current	V _{CC} = 2.7 V		-12 -24	mA
ЮН	rigir-level output current	V _{CC} = 3 V			ША
	Law level autout aureant	V _{CC} = 2.7 V		12	A
lOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS252 - OCTOBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0	.2	
		I _{OH} = -12 mA	2.7 V	2.2		v
VOH		10H = - 12 11IA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
lı	Inputs	$V_I = V_{CC}$ or GND	3.6 V		±5	μА
1.0 . 0	Data pins	V _I = 0.8 V	3 V	75		
l(hold)	Data piris	V _I = 2 V] "	-75		μА
loz		$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μΑ
Ci		V _I = V _{CC} or GND	3.3 V			pF
Со		V _O = V _{CC} or GND	3.3 V			рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



12-BIT TO 24-BIT REGISTERED BUS TRANSCEI WITH 3-STATE OUTPUTS

SCAS417 - OCTOBER 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments Widebus™ Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{CC} Overshoot) $> 2 V at V_{CC} = 3.3 V, T_A = 25 °C$
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) **Packages**

description

The SN74ALVC16269 is a 12-bit to 24-bit registered bus exchanger, which is intended for applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface DRAMs between sync and high-speed microprocessors. The SN74ALVC16269 is designed specifically for low-voltage (3.3 V) V_{CC} operation.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input. provided that the appropriate CLKENA inputs are low. Proper control of these inputs allows two seguential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data will be valid on the bus. The control pins are registered so that all transactions are synchronous with the clock. Data flow is controlled by the active-low output enables (OEA, OEB1, OEB2).

DGG OR DL PACKAGE (TOP VIEW)

_		_	1
OEA [,	56	OEB2
OEB1			CLKENA2
2B3 🕻 :	3	54	2B4
GND []	4		GND
2B2 🛚 (5	52] 2B5
2B1 🛛		51]2B6
v _{cc} 🗓	7	50	₫v _{cc}
A1 🛮 8	3	49	□ 2B7
A2 🛚 9		48	2B8
A3 🗓 ·		47	2B9
GND 🗓		46	GND
A4 🗓 ·		45	2B10
A5 🛚			2B11
A6 🛚		43	2B12
A7 🗓 ·] 1B12
A8 🛚] 1B11
A9 🛚] 1B10
GND 🛚] GND
A10 🛚] 1B9
A11 🛛 2] 1B8
A12 🛚 2] 1B7
V _{CC} 🛚 2	22		Ūν _{cc}
1B1 []2		34	
1B2 🛚 2] 1B5
		32] GND
1B3 🛚 2] 1B4
			CLKENAT
SEL [[2	28	29]clk

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

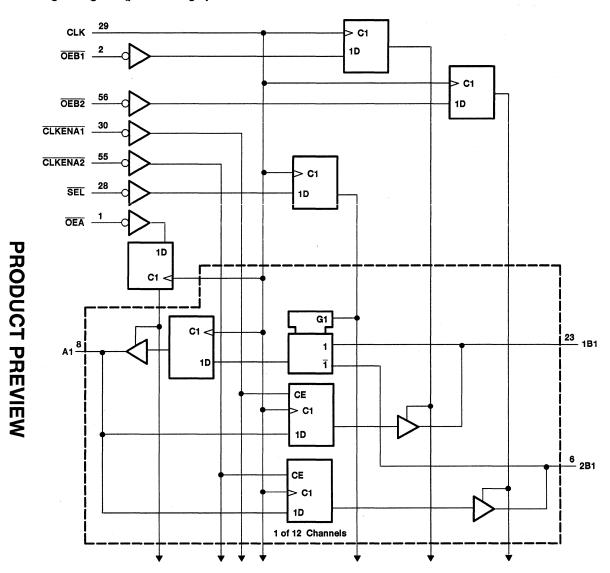
The SN74ALVC16269 is available in Ti's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16269 is characterized for operation from -40°C to 85°C.

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STRUMENTS

logic diagram (positive logic)





SN74ALVC16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS417 - OCTOBER 1993 - REVISED MARCH 1994

Function Tables

OUTPUT-ENABLE TABLE

	INPUTS			OUTPUTS		
	CLK	OEA	OEB	Α	1B, 2B	
ſ	1	Н	Н	Z	Z	
l	1	Н	L	z	Active	
١	1	L	Н	Active	Z	
	1	L	L	Active	Active	

A-TO-B STORAGE TABLE (OEB = L)

	INPUTS				PUTS
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B ₀ †	2B ₀ †
L	X	1	L	L	Χ
L	X	↑	Н	Н	Χ
X	L	↑	L	Х	L
X	L	1	Н	Х	Н

B-TO-A STORAGE TABLE (OEA = L)

	INP	OUTPUT		
CLK	SEL	1B	2B	A
Х	Н	Х	Х	A ₀ †
Х	L	Χ	Χ	A ₀ † A ₀ †
1	Н	L	X	L
↑	Н	Н	Χ	Н
1	L	Χ	L	L
1	L	Χ	Н	н

[†] Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG packa	age 1 W
DL packag	e 1.4 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the *Package Thermal Considerations* application note.



SN74ALVC16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCAS417 - OCTOBER 1993 - REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ı	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	V
lau	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	ША
10.	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current				IIIA
Δt/Δν	Input transition rise or fall rate		. 0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST	CONDITIONS	v _{cc} †	MIN	MAX	UNIT	
		IOH = -100 μA		MIN to MAX	V _{CC} -0	.2		
V		la 10 mA		2.7 V	2.2		V	
VOH		I _{OH} = -12 mA		3 V	2.4		V	
		I _{OH} = -24 mA	I _{OH} = -24 mA					
		I _{OL} = 100 μA		MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	v		
		I _{OL} = 24 mA		3 V		0.55		
l _l	Inputs	VI = VCC or GND		3.6 V		±5	μA	
1	Data nine	V _I = 0.8 V	3 V	75				
l(hold)	Data pins	V _I = 2 V			-75		μА	
loz		V _O = V _{CC} or GND		3.6 V		±10	μА	
ICC		V _I = V _{CC} or GND,	IO = 0	3.6 V		40	μА	
ΔlCC		V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} - 0.6 V,			750	μА	
Ci		V _I = V _{CC} or GND		3.3 V			pF	
Cio		V _O = V _{CC} or GND		3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS433 - OCTOBER 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments Widebus™ Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{CC} Overshoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALVC16270 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3 V) $V_{\rm CC}$ operation.

The device provides for synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate CLKEN inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the CLKENA inputs allow two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). These control pins are registered so that bus direction changes are synchronous with the clock.

DGG OR DL PACKAGE (TOP VIEW)

OEA [, U	56	OEB
CLKEN1B	ļ',		CLKENA2
2B3 [54]2B4
GND [GND
2B2			2B5
2B1			2B6
v _{cc} [7	50	V _{CC}
A1 [8	49]2B7
A2 [9	48	2B8
АЗ [47	2B9
GND [GND
A4 [45	2B10
A5 [44	2B11
A6 [14		2B12
A7 [15]1B12
A8 [16	41]1B11
A9 [40]1B10
GND [18	39	GND
A10 [38	1B9
A11 [37] 1B8
A12 🛚		36]1B7
v _{cc} [22	35	lv _{cc}
1B1 🛭		34	1B6
1B2 🛚		33	1B5
GND [32	GND
1B3 [1B4
CLKEN2B			CLKENA1
SEL [28	29]CLK

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

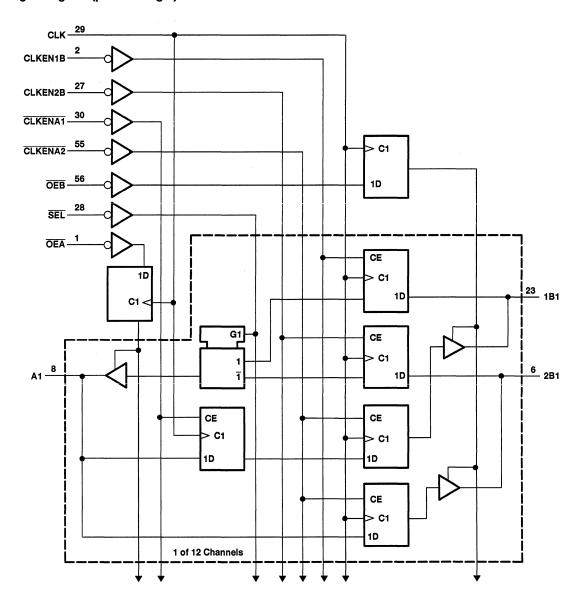
The SN74ALVC16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16270 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



logic diagram (positive logic)





PRODUCT PREVIEW

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS433 - OCTOBER 1993 - REVISED MARCH 1994

Function Tables

OUTPUT-ENABLE TABLE

١	INPUTS			OUTPUTS		
	CLK	OEA	OEB	Α	1B, 2B	
ı	1	Н	Н	Z	Z	
	↑	Н	L	Z	Active	
	1	L	н	Active	z	
	1	L	L	Active	Active	

A-TO-B STORAGE TABLE (OEB = L)

INPUTS				OUT	PUTS
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B ₀ †	2B ₀ †
L	Χ	1	L	L1	x
L	Х	1	Н	Н1	х
х	L	↑	L	х	L
Х	L	1	н	Х	н

¹ Two CLK edges are needed to propagate data.

B-TO-A STORAGE TABLE (OFA = 1)

D-10-A GTOTIAGE TABLE (GEA = E)						
	INPUTS					
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
Н	Х	Х	Н	Х	Χ	A ₀ †
, X	Н	Χ	L	Χ	Χ	A ₀ † A ₀ †
L	X	1	н	L	X	L
L	X	1	Н	Н	Χ	Н
Х	L	1	L	Χ	L	L
х	L	1	L	Χ	Н	Н

[†]Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



SN74ALVC16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS433 - OCTOBER 1993 - REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	Vcc	٧
Vo	Output voltage		0	Vcc	V
la	High-level output current	V _{CC} = 2.7 V		-12	1
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
lai	Low lovel output ourrent	V _{CC} = 2.7 V		12	4
IOL L	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	is v _{cc} †	MIN	MIN MAX		
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
V		I _{OH} = -12 mA	2.7 V	2.2		v	
VOH		10H = - 12 IIIA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX	0.2			
VOL		I _{OL} = 12 mA	2.7 V		0.4	V	
		I _{OL} = 24 mA	3 V		0.55		
lį	Inputs	VI = VCC or GND	3.6 V		±5	μА	
1	Data pins	V _I = 0.8 V	3 V	75			
l(hold)	Data piris	V _I = 2 V	3 V	-75		μА	
loz		V _O = V _{CC} or GND	3.6 V		±10	μА	
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
ΔlCC		V _{CC} = 3 V to 3.6 V, One input at Other inputs at V _{CC} or GND	t V _{CC} – 0.6 V,		750	μА	
Ci		V _I = V _{CC} or GND	3.3 V			pF	
Cio		V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS255 - OCTOBER 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Member of the Texas Instruments Widebus™ Family
- **Supports Unregulated Battery Operation** Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{CC} Overshoot) $> 2 V at V_{CC} = 3.3 V, T_A = 25^{\circ}C$
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) **Packages**

description

The SN74ALVC16271 is a 12-bit to 24-bit bus exchanger, which is intended for applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. It is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the CLKENA inputs are low. Proper control of these inputs allow two sequential 12-bit words to be presented as a 24-bit word on the B port.

DGG OR DL PACKAGE (TOP VIEW)

OEA [1 ₁ \cup	56	OEB
LE1B [55	CLKENA2
2B3 [54] 2B4
GND [53	GND
2B2		52] 2B5
2B1 [51	2B6
V _{CC} [7	50] v _{cc}
A1 [49	2B7
A2 [48	Ll 2B8
A3 [47	2B9
GND [46	GND
A4 [12	45	∐ 2B10
A5 [44	2B11
	14	43	2B12
	15	42	1B12
] 8A		41] 1B11
	17	40] 1B10
GND [18	39	GND
A10 [] 1B9
A11 [37] 1B8
A12 [36] 1B7
V _{CC}		35] v _{cc}
1B1 [34] 1B6
1B2 [24	33	1B5
GND [32	GND
1B3		31] 1B4
LE2B	27	30	CLKENA1
SEL [28	29	CLK

Transparent latches in the B to A path allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{\text{LE}}$) inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16271 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

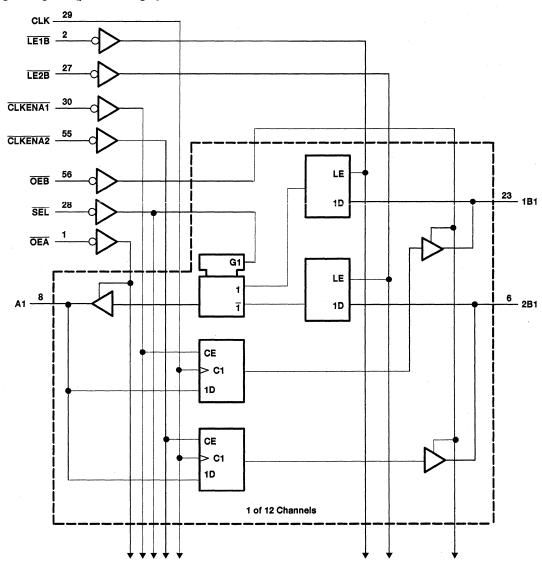
The SN74ALVC16271 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



SN74ALVC16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS SCAS255 - OCTOBER 1993 - REVISED MARCH 1994

logic diagram (positive logic)





SN74ALVC16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS255 - OCTOBER 1993 - REVISED MARCH 1994

Function Tables

OUTPUT-ENABLE TABLE

INP	UTS	OUTPUTS		
OEA OEB		Α	1B, 2B	
Н	Н	Z	Z	
Н	L	z	Active	
L	Н	Active	Z	
L	L	Active	Active	

A-TO-B STORAGE TABLE (OEB = L)

	OUT	PUTS			
CLKENA1	CLKENA2	CLK	A	1B	2B
Н	Н	Х	Х	1B ₀ †	2B ₀ †
L	Χ	1	L	L	Х
L	X	1	Н	Н	х
Х	L	↑	L	×	L
X	L	1	Н	A ₀	Н

B-TO-A STORAGE TABLE (OEA = L)

	INP	OUTPUT		
LE	SEL	1B	2B	Α .
Н	Х	Х	Х	A ₀ †
Н.	· X	Χ	Χ	A ₀ † A ₀ †
L	Н	L	Χ	L
L	Н	Н	Χ	н
L	L	Χ	L	L
L	L	X	Н	н

[†] Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	.5 V to V _{CC} + 0.5 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.



SN74ALVC16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS255 - OCTOBER 1993 - REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VιΗ	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
٧ _I	Input voltage		0	VCC	٧
Vo	Output voltage		, 0	VCC	٧
lou	High-level output current	V _{CC} = 2.7 V	-12		mA
ЮН		V _{CC} = 3 V		-24	""
la.	Low lovel output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current V _{CC} = 3 V			24	. mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	.2		
V		10 mA	2.7 V	2.2		v	
VOH		IOH = -12 mA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
V_{OL}		I _{OL} = 12 mA	2.7 V		0.4	V	
		I _{OL} = 24 mA	3 V	0.55			
lį	Inputs	V _I = V _{CC} or GND	3.6 V		±5	μΑ	
1	Data nina	V _I = 0.8 V	3 V	75			
l(hold)	Data pins	V _I = 2 V	3 V	-75		μΑ	
loz		VO = VCC or GND	3.6 V		±10	μА	
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА	
Ci		V _I = V _{CC} or GND	3.3 V			pF	
C _{io}		VO = VCC or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS256 - OCTOBER 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments
 Widebus™ Family
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{CC} Overshoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALVC16272 is a 12-bit to 24-bit bus exchanger, which is intended for applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. It is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

Data from the A inputs is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the CLKENA inputs are low. A two-stage pipeline is provided in each of the A to 1B and A to 2B paths to serve as a shallow write buffer.

DGG OR DL PACKAGE (TOP VIEW)

		$\tau \tau$		
OEA [1		56	OEB
LE1B	2		55	CLKENA2
2B3 [3		54	2B4
GND [4		53	GND
2B2 [5		52	2B5
2B1 [51	2B6
v _{cc} [7		50] v _{cc}
A1 [8		49	2B7
A2 [48	2B8
АЗ [10		47] 2B9
GND [46	
A4 [45	2B10
A5 [13		44	2B11
A6 [43	2B12
A7 [15		42	1B12
A8 [41] 1B11
A9 [40	1B10
GND [18		39	GND
A10 [19		38	1B9
A11 [20		37	1B8
A12 [36] 1B7
V _{CC} [22		35	
1B1 [23		34	∐ 1B6
1B2 [33] 1B5
GND [32	GND
1B3 [31	
LE2B			30	CLKENA1
SEL	28		29	CIK

Transparent latches are provided in the B to A path to allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable (LE) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16272 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

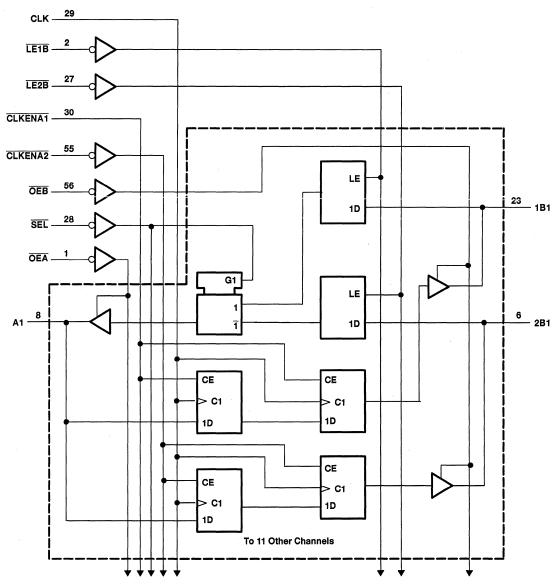
The SN74ALVC16272 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



SN74ALVC16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS SCAS256 - OCTOBER 1993 - REVISED MARCH 1994

logic diagram (positive logic)





SN74ALVC16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS SCAS256 - OCTOBER 1993 - REVISED MARCH 1994

Function Tables

OUTPUT-ENABLE TABLE

INP	UTS	OUTPUTS		
OEA	OEA OEB		1B, 2B	
Н	Н	Z	Z	
н	L	z	Active	
L	Н	Active	Z	
L	L	Active	Active	

A-TO-B STORAGE TABLE (OEB = L)

	OUT	PUTS			
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B ₀ †	2B ₀ †
L	Х	1	L	L1	Χ
. L	Χ	1	Н	Н1	Χ
, X	L	1	L	Х	L
х	L	1	Н	A ₀	Н

¹ Two CLK edges are needed to propagate data.

B-TO-A STORAGE TABLE (OEA = L)

	INPL	OUTPUT		
LE	SEL	1B	2B	Α
Н	Х	Х	Х	A ₀ ‡
Н	X	Χ	Χ	A ₀ ‡ A ₀ ‡
L	Н	L	X	L
L	Н	Н	Χ	н
L	L	Χ	L	L
L	L	Х	Н	Н

[†] Output level before the indicated steady-state input conditions were established.



SN74ALVC16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS256 - OCTOBER 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGC	G package 1 W
DL	package 1.4 W
Storage temperature range	_65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
Vį	Input voltage		0	VCC	٧
۷o	Output voltage		0	20	٧
10	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	
la:	Law lavel output ourrent	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS256 - OCTOBER 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	2	
\ _{\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\}		10 mA	2.7 V	2.2		v
VOH		IOH = -12 mA	3 V	2.4		
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	,
l _l	Inputs	V _I = V _{CC} or GND	3.6 V		±5	μА
lea en	Data nina	V _I = 0.8 V	3 V	75		
l(hold)	Data pins	V _I = 2 V		-75		μА
loz	***************************************	V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔlCC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА
Ci		$V_{I} = V_{CC}$ or GND	3.3 V			рF
C _{io}		V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS257 - JANUARY 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>OE</u> 1 48 1LE
 Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater 	1Q1
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q3
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q5
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	GND [10 39] GND 1Q7 [11 38] 1D7 1Q8 [12 37] 1D8
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	2Q1 [13 36] 2D1 2Q2 [14 35] 2D2 GND [15 34] GND
description	2Q3 [] 16 33 [] 2D3 2Q4 [] 17 32 [] 2D4 V _{CC} [] 18 31 [] V _{CC}
This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V _{CC} operation.	V _{CC} [18 31] V _{CC} 2Q5 [19 30] 2D5 2Q6 [20 29] 2D6
The SN74ALVC16373 is particularly suitable for implementing buffer registers, I/O ports,	GND
bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.	2Q8 [23 26] 2D8 2OE [24 25] 2LE

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16373 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16373 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
н	Х	Х	z

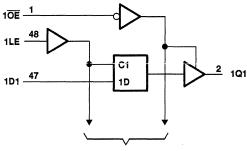
logic symbol†

PRODUCT PREVIEW

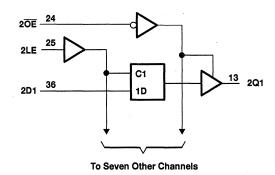
10E 1EN 48 1LE СЗ 24 2OE 2EN 25 2LE C4 47 2 1Q1 1D1 3D 1 ▽ 3 46 1D2 1Q2 44 5 1D3 1Q3 43 6 1D4 1Q4 41 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 1Q7 37 12 1D8 1Q8 13 36 2D1 4D 2Q1 2 ▽ 35 14 2D2 2Q2 33 16 2D3 2Q3 32 17 2D4 2Q4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 2Q8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74ALVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS257 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
lavi	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
la.	Law laws and a summer	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16373 **16-BIT TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS SCAS257 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN MA	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Vou	104	2.7 V	2.2	□
Voн	I _{OH} = -12 mA	3 V	2.4	7 °
	I _{OH} = -24 mA	3 V	2	
	l _{OL} = 100 μA	MIN to MAX	0.	2
VOL	$I_{OL} = 12 \text{ mA}$	2.7 V	0.	4 V
	I _{OL} = 24 mA	3 V	0.5	5
Ιį	V _I = V _{CC} or GND	3.6 V	±	5 μΑ
t	V _I = 0.8 V	3 V	75	
[[] I(hold)	V _I = 2 V		-75	- μΑ
loz	$V_O = V_{CC}$ or GND	3.6 V	±1	DμA
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	4) μΑ
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		75	Αμ
Ci	V _I = V _{CC} or GND	3.3 V		pF
Co	$V_{O} = V_{CC}$ or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS258 - JANUARY 1993 - REVISED MARCH 1994

	SCAS258 - JANUARY 1993 - REVISED MARC
Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 48 1CLK
• Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater	1Q1
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q3
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q5 [8 41] 1D5 1Q6 [9 40] 1D6
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	GND
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	2Q1
description	2Q3 [16 33] 2D3 2Q4 [17 32] 2D4
This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.	V _{CC}
The SN74ALVC16374 is particularly suitable for implementing buffer registers, I/O ports,	GND 0 21 28 GND 2Q7 0 22 27 0 2D7
bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.	2Q8 [23 26] 2D8 2OE [24 25] 2CLK

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16374 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Х	Q ₀
Н	X	Х	Z

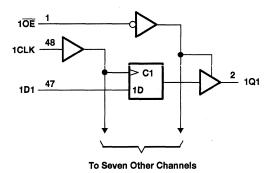
logic symbol†

PRODUCT PREVIEW

10E 1EN 48 1CLK > C1 24 20E 2EN 25 2CLK C2 47 2 1D1 1D 1 ▽ 1Q1 3 46 1Q2 1D2 5 44 1D3 1Q3 43 6 1D4 1Q4 8 41 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 1Q7 37 12 1D8 1Q8 36 13 2D1 2D 2 ▽ 2Q1 35 14 2D2 2Q2 33 16 2D3 2Q3 32 17 2D4 2Q4 19 30 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 2Q8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



2OE 24
2CLK 25
2D1 36 13 2Q1
To Seven Other Channels

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG	
DL p	ackage 1.2 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT	
Vcc	Supply voltage		2.7	3.6	٧	
VιΗ	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧	
٧ı	Input voltage		0	٧cc	٧	
٧o	Output voltage		0	VCC	٧	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24	IIIA	
lo	Low-level output current	V _{CC} = 2.7 V		12	mA	
lOL	Low-level output current	V _{CC} = 3 V		24	ША	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	ပ္	



SN74ALVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS258 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN MAX	UNIT	
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari		2.7 V	2.2] ,	
VOH	I _{OH} = -12 mA	3 V	2.4] "	
	I _{OH} = −24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX	0.2	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4	4 V	
	I _{OL} = 24 mA	3 V	0.55		
l ₁	V _I = V _{CC} or GND	3.6 V	±5	μА	
la in	V _I = 0.8 V	3 V	75] <u>^</u>	
^j l(hold)	V _I = 2 V		-75	μΑ	
loz	$V_O = V_{CC}$ or GND	3.6 V	±10	μА	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μА	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		750	μА	
Ci	V _I = V _{CC} or GND	3.3 V		pF	
Co	$V_O = V_{CC}$ or GND	3.3 V		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS260 - JANUARY 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level.If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)

OEAB [1₁ └	56	GND
LEAB [55	CLKAB
A1 [54	B1
GND [4	53	GND
A2 [52	B2
A3 [6		B3
v _{cc} []7	50	l v _{cc}
A4 [8	49	B4
A4 [A5 [9	48	B5
A6 [10		B6
GND [11	46	GND
A7 [12	45	B7
A8 [13		B8
A9 [14		B9
A10 [15	42	B10
A11 [16		B11
A12 L	17	40	B12
GND [18	39	GND
A13 [38	B13
A14 [B14
A15 [B15
v _{cc} [22		v_{cc}
A16 [23	34	B16
A17 [33	B17
GND [25	32	GND
A18 [26		B18
OEBA [27		CLKBA
LEBA [28	29	GND

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

The SN74ALVC16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16500 is characterized for operation from -40°C to 85°C.

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SN74ALVC16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCAS260 - JANUARY 1993 - REVISED MARCH 1994

FUNCTION TABLET

INPUTS				OUTPUT		
OEAB	LEAB CLKAB A		В			
L	Х	Х	Х	Z		
н	Н	X	L	L		
Н	Н	Χ	Н	н		
н	L	\downarrow	L	L		
Н	L	\downarrow	Н	н		
н	L	Н	Χ	в ₀ ‡ в ₀ \$		
Н	L	L	Х	B ₀ §		

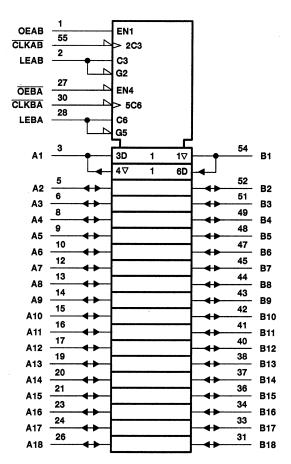
[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

SN74ALVC16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCAS260 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†

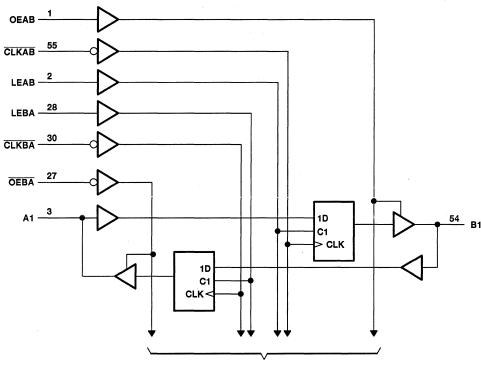


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16500 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCAS260 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3	B): DGG package 1 W
	DL package 1.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



SN74ALVC16500 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCAS260 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	٧
,	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	IIIA
lo	Laur laural authorit authorit	V _{CC} = 2.7 V		12	A
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

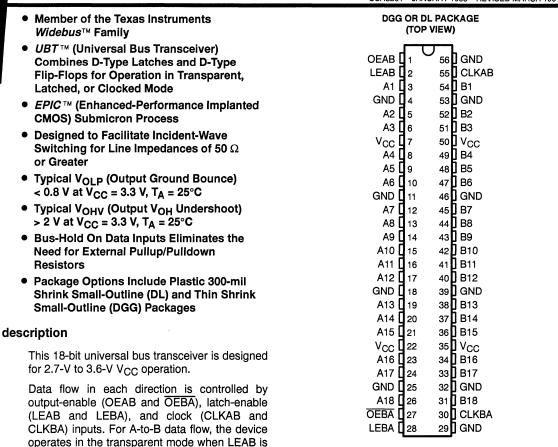
PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0	CC-0.2	
		IOH = -12 mA	2.7 V	2.2		v
VOH		IOH = - 12 IIIA	3 V	2.4		· •
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL		I _{OL} = 12 mA	2.7 V		0.4	
		I _{OL} = 24 mA	3 V		0.55	
4		V _I = V _{CC} or GND	3.6 V		±5	μА
		V _I = 0.8 V	3 V	75		
l(hold)	Data I/Os	V _I = 2 V		-75		μА
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]mbox{\ensuremath{\,^{\ddagger}}}\mbox{\ensuremath{\,\text{For I/O}}}\mbox{\ensuremath{\,\text{ports}}},$ the parameter IOZ includes the input leakage current.

SN74ALVC16501 18-BIT UNIVERSAL BUS TRANSCEIN WITH 3-STATE OUTPUTS

SCAS261 - JANUARY 1993 - REVISED MARCH 1994



Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

The SN74ALVC16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16501 is characterized for operation from -40°C to 85°C.

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high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance



state.

SN74ALVC16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCAS261 – JANUARY 1993 – REVISED MARCH 1994

FUNCTION TABLET

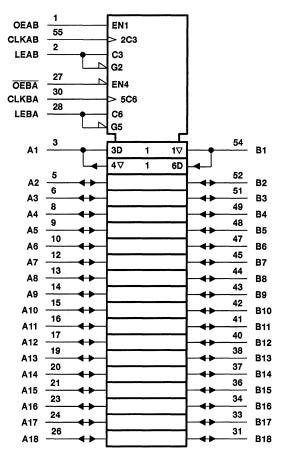
	OUTPUT			
OEAB	LEAB	AB CLKAB A		В
L	X	Х	Х	Z
н	Н	Χ	L	L
н	Н	Х	Н	н
Н	L	1	L	L
Н	L	↑	Н	н
Н	L	Н	Χ	в ₀ ‡ в ₀ \$
н	L	L	Χ	в ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡]Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

[§] Output level before the indicated steady-state input conditions were established.

logic symbol†

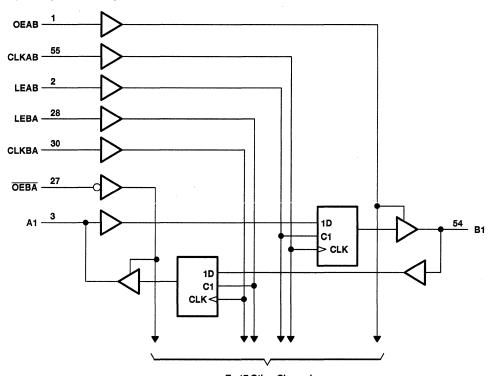


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVC16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS261 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)



To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SN74ALVC16501 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCAS261 - JANUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
۷ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷ _I	Input voltage		0	VCC	V
۷o	Output voltage		0	Vcc	V
lou	High-level output current	V _{CC} = 2.7 V		-12	A
ЮН		V _{CC} = 3 V		-24	mA
lo	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	V _{CC} = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST	CONDITIONS	vcct	MIN M	AX	UNIT
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2		
V		la 10 mA		2.7 V	2.2		V
VOH		I _{OH} = -12 mA		3 V	2.4		V
		I _{OH} = -24 mA		3 V	2		
		I _{OL} = 100 μA		MIN to MAX		0.2	
VOL		I _{OL} = 12 mA		2.7 V		0.4	V
		I _{OL} = 24 mA		3 V	0	.55	
l _l		V _I = V _{CC} or GND		3.6 V		±5	μА
loz‡		VO = VCC or GND		3.6 V	±	10	μА
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V		40	μА
ΔICC		V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,		7	50	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V			рF
Cio	A or B ports	VO = VCC or GND		3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE (TOP VIEW)

SCAS262 - JANUARY 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

10EAB	1	U	EG	1 <u>0eba</u>
1LEAB			55	
1CEAB				1CEBA
GND [GND
1A1 [1B1
1A2 [1B2
v _{cc} [v _{cc}
1A3 [Ŕ		49	1B3
1A4 [1B4
1A5	10		47	1B5
GND [GND
1A6 🛚	12			1B6
1A7 🛚				1B7
1A8 🛚				1B8
2A1 [15		42	2B1
2A2 [16		41	2B2
2A3 🛚	17		40	2B3
GND [18		39] GND
2A4 [38	2B4
2A5 [20		37] 2B5
2A6 🛚] 2B6
v _{cc} [22		35] v _{cc}
2A7 [23			2B7
2A8 🏻	24		33] 2B8
GND [32	GND
2CEAB				2CEBA
2LEAB	27		30	2LEBA

The SN74ALVC16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16543 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

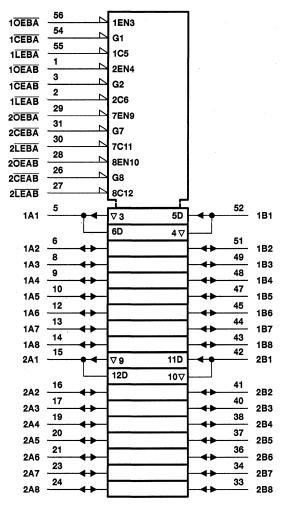


29 20EBA

20EAB | 28

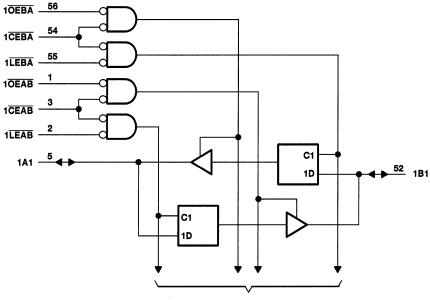
SN74ALVC16543 **16-BIT REGISTERED TRANSCEIVER** WITH 3-STATE OUTPUTS SCAS262 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†

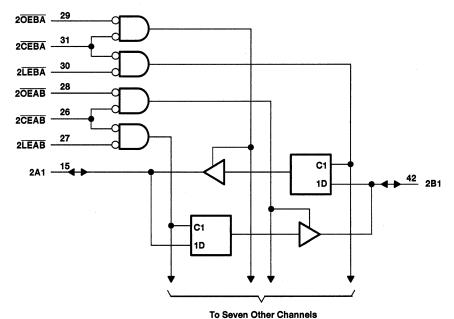


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



FUNCTION TABLET (each 8-bit section)

	INPUTS OUTPL			
CEAB	LEAB	OEAB	Α	В
Н	Х	Х	Х	Z
Х	Х	Н	Χ	z
L	Н	L	Χ	в ₀ ‡
L	L	L	L	L
L	L	L	Н	Н

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
VI	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
la	High-level output current	V _{CC} = 2.7 V		-12	mA
Іон		V _{CC} = 3 V		-24	""
Ī	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	V _{CC} = 3 V			24	111/2
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ŝ



PRODUCT PREVIEW

[‡] Output level before the indicated steady-state input conditions were established.

SN74ALVC16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0	.2	
\/-··		Jan. 10 mA	2.7 V	2.2		v
VOH		IOH = -12 mA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
կ		V _I = V _{CC} or GND	3.6 V		±5	μА
	D-4- 1/O-	V _I = 0.8 V	0.1/	75		
l(hold)	Data I/Os	V _I = 2 V	3 V	-75		μΑ
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μA
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS263 - JANUARY 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, Clocked, or Clock-Enabled Mode
- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and

DGG OR DL PACKAGE (TOP VIEW)

OEAB [₁ ∪	56 CLKENAB
LEAB [55 CLKAB
A1 [54 B1
GND [53 GND
A2 [52 B2
АЗ [51 [] B3
v _{cc} [50 V _{CC}
A4 [8	49 [] B4
A5 🛚		48 D B5
A6 [10	47 🛭 B6
GND [46 🛭 GND
A7 [45 [] B7
A8 [13	44 🛮 B8
A9 [14	43 B9
A10 [15	42 B10
A11 [16	41 B11
A12 [17	40 B12
GND [39] GND
A13 [19	38] B13
A14 [37 B14
A15 🛚		36 B15
V _{CC} [35 V _{CC}
A16 🛚		34 🛮 B16
A17 🛭		33 B17
GND [32] GND
A18 [31 B18
OEBA [27	30 CLKBA
LEBA [28	29 CLKENBA

CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The SN74ALVC16600 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16600 is characterized for operation from -40°C to 85°C.

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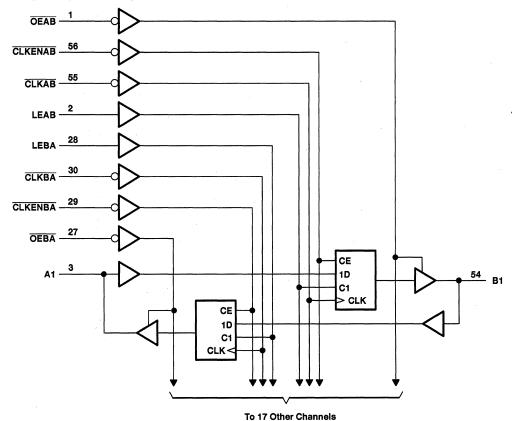


FUNCTION TABLET

	ı	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Χ	Z
Х	L	Н	X	L	L.
X	L	Н	X	Н	н
Н	L	L	Х	Χ	в ₀ ‡
Н	L	L	Х	Χ	в ₀ ‡ в ₀ ‡
L ·	L	L	\downarrow	L	Ľ
L	L	L	\downarrow	Н	Н
Ĺ	L	L	Н	Χ	B ₀ ‡
L	L	L	. L	Χ	B ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKBA}}$, and $\overline{\text{CLKENBA}}$.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

SN74ALVC16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5	V to 4.6 V
Input voltage range, V ₁ (except I/O ports) (see Note 1)	
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	CC + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$. –50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	. ±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	. ±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package	
DL package	
Storage temperature range –65°	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage	1000	2.7	3.6	V
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage		0	VCC	V
٧o	Output voltage	,	0	VCC	٧
la	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16600 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS SCAS263 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0	.2		
\ _{\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\}		IOH = -12 mA	2.7 V	2.2		v	
VOH		IOH = - 12 IIIA	3 V	2.4		٧	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX	,	0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	ν	
		I _{OL} = 24 mA	3 V		0.55		
lį		V _I ≈ V _{CC} or GND	3.6 V		±5	μА	
		V _I ≈ 0.8 V	3 V				
l(hold)	Data I/Os	V _I = 2 V		-75		μА	
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА	
ICC		$V_1 = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μА	
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF	
Cio	A or B ports	VO = VCC or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE (TOP VIEW)

OEAB [] 1

LEAB 2

A1 🛮 3

A2 🛮 5

A3 🛮 6

V_{CC} 🛛 7

A4 🛮 8

A5 🛮 9

A6 🛮 10

A7 🛮 12

A8 🛮 13

A9 🛮 14

A10 🛮 15

A11 16

A12 🛮 17

GND 18

A13 II 19

A14 1 20 A15 1 21

V_{CC} 422

A16 23

A17 1 24

GND 125

A18 🛮 26

OEBA 127

LEBA [] 28

GND 11

GND 4

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56 CLKENAB

55 CLKAB

54 B1

52 B2

51 B3

49 B4

48 **∏** B5

47 [] B6

44 🛮 B8

43 N B9

42 NB10

41 B11

40**∏** B12

39 GND

38 TB13

37 **1** B14

36 B15

35 🛮 V_{CC}

34 B16

33 T B17

32 T GND

31 B18

30 CLKBA

29 CLKENBA

46 GND 45 B7

50 VCC

53 GND

- **Member of the Texas Instruments** Widebus™ Family
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- EPIC ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 V at V_{CC} = 3.3 V, T_A = 25^{\circ}C$
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by

output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and

CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The SN74ALVC16601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16601 is characterized for operation from -40°C to 85°C.

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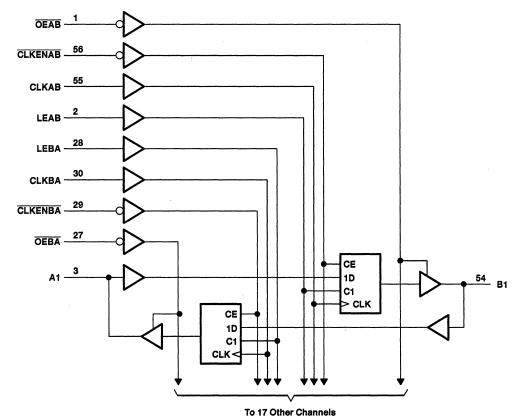


FUNCTION TABLET

	OUTPUT				
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	X	Х	Х	Z
х	L	Н	Χ	L	L
x	L	н	X	Н	н
н	Ł	L	X	Χ	В ₀ ‡ В ₀ ‡
н	L	L	X	Χ	в ₀ ‡
L	L	L	1	L	L
L	L	L	1	Н	н
L	L	L	L	Χ	в ₀ ‡
L	L	L '	Н	Х	В ₀ ‡ В ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

logic diagram (positive logic)



[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

SN74ALVC16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS264 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.	6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.	6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.$	5 V
Output voltage range, VO (see Notes 1 and 2)		
Input clamp current, I_{IK} ($V_I < 0$)	50	mΑ
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50	mΑ
Continuous output current, I _O (V _O = 0 to V _{CC})	±50	mΑ
Continuous current through V _{CC} or GND		
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG packa		
DL package	ge 1.4	1 W
Storage temperature range	-65°C to 150	O°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
٧ı	Input voltage		0	VCC	٧
۷o	Output voltage		0	VCC	٧
1	High lovel output augrent	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24] "'^
la.	Low level output ourrent	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS264 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	2	
V		I _{OH} = –12 mA	2.7 V	2.2		V
VOH		10H = -12 IIIA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
Ιį		V _I = V _{CC} or GND	3.6 V		±5	μА
lia in	Data I/Os	V _I = 0.8 V	3 V	75		
l(hold)	Data I/Os	V _I = 2 V	3 V	-75		μА
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μA
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			рF
Cio	A or B ports	VO = VCC or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS376 - MARCH 1994

- Member of the Texas Instruments
 Widebus™ Family
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, Clocked, or Clock-Enabled Mode
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on All I/O Pins
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)

OEAB	1	O	56	CLKENAB
LEAB	2		55] CLKAB
A1	3] B1
GND	4		53] GND
A2	5		52] B2
А3 [6		51] B3
V _{CC}	7		50] v _{cc}
A4 []8		49] B4
A5 (9		48	B5
A6 [10] B6
GND	11			GND
A7 [12		45] B7
A8	13		44] B8
	14		43] B9
A10	15		42	B10
A11 [16]B11
A12 [40	B12
GND [] GND
A13 [B13
A14 [B14
A15 [36	B15
v _{cc} [22] v _{cc}
A16 [] B16
A17 [33	B17
GND [32	GND
A18 [31] B18
OEBA [27			CLKBA
LEBA [28		29	CLKENBA

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

The B-port outputs, include 25- Ω series resistors to reduce overshoot and undershoot.

The SN74ALVC162601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC162601 is characterized for operation from -40°C to 85°C.

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SN74ALVC162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS376 - MARCH 1994

FUNCTION TABLET

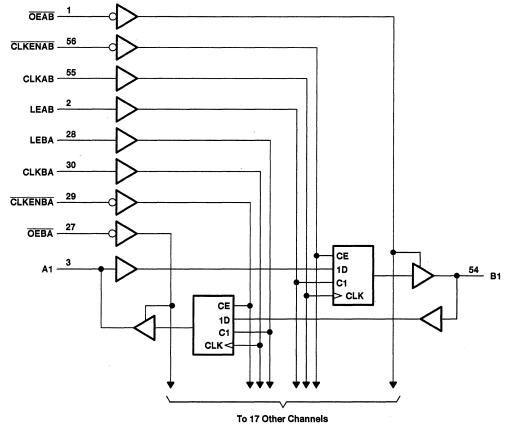
	OUTPUT				
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	X	Х	X	Z
х	L	Н.	Χ	L	L
Х	L	Н	X	Н	н
Н	L	L	, X	Χ	В ₀ ‡ В ₀ ‡
н	L	L	Х	Χ	в ₀ ‡
L	L	L	1	L	L
L	L .	L	1	Н	н
L	L	L	L	Χ	В ₀ ‡ В ₀ §
L	L	L	Н	Х	В ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

[‡] Output level before the indicated steady-state input conditions were established.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

logic diagram (positive logic) OEAB -1



SN74ALVC162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS376 - MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	V
٧ı	Input voltage		0	VCC	V
Vo	Output voltage		0	Vcc	٧
Jau	High-level output current	V _{CC} = 2.7 V			mΑ
ЮН	nigri-level output current	V _{CC} = 3 V			IIIA
loi	Low-level output current	V _{CC} = 2.7 V			mΑ
lOL	Low-level output current				ША
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ပ္



SN74ALVC162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS376 - MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN MAX	UNIT
Vou		I _{OH} = – 100 μA	MIN to MAX	V _{CC} -0.2	
		I _{OH} = -4 mA	2.7 V	2.4	v
VOH	I _{OH} = -6 mA	3 V	2.4]	
		I _{OH} = TBD	7 3'	2	
		I _{OL} =100 μA	MIN to MAX	0.2	
VoL	I _{OL} = 4 mA	2.7 V	0.4	v	
<u> </u>		I _{OL} = 6 mA	0.4] '	
		I _{OH} = TBD	3 V	0.8	
l _l		V _I = V _{CC} or GND	3.6 V	±5	μА
1		V _I = 0.8 V	3 V	75	
I(hold)		V _I = 2 V	7 ° ′	-75	μΑ
loz‡		VO = VCC or GND	3.6 V	±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μА
ΔlCC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	,	750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS265 - JANUARY 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)				
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1DIR 1 56 1 1CLKAB 2 55 1	OE CLKBA			
• Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater	1SAB [] 3 54 [] 1 GND [] 4 53 [] 6	SBA GND			
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1A1 [] 5 52 [] 1 1A2 [] 6 51 [] 1 V _{CC} [] 7 50 [] V	B2			
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A3 [8 49] 1 1A4 [9 48] 1	B3 B4			
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	1A5 [] 10 47 [] 1 GND [] 11 46 [] 0 1A6 [] 12 45 [] 1	AND			
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1A7 [13 44] 1 1A8 [14 43] 1	B7			
Small-Outline (DGG) Packages	2A1 [15 42] 2 2A2 [16 41] 2 2A3 [17 40] 2	2B2			
description This 16-bit bus transceiver and register is	GND 18 39 6	AND			
designed for 2.7-V to 3.6-V V_{CC} operation.	2A4 [] 19 38 [] 2 2A5 [] 20 37 [] 2	2B5			
The SN74ALVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the	2A6 [] 21 36 [] 2 V _{CC} [] 22 35 [] V 2A7 [] 23 34 [] 2	/cc			
A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the	2A7 [24 33] 2 2A8 [24 33] 2 GND [25 32] 6	2B8			
four fundamental bus-management functions that can be performed with the SN74ALVC16646.	2SAB [] 26 31 [] 2 2CLKAB [] 27 30 [] 2	SBA CLKBA			
Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver	2DIR [28 29] 2	OĒ			

the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74ALVC16646 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16646 is characterized for operation from -40°C to 85°C.

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functions. In the transceiver mode, data present at



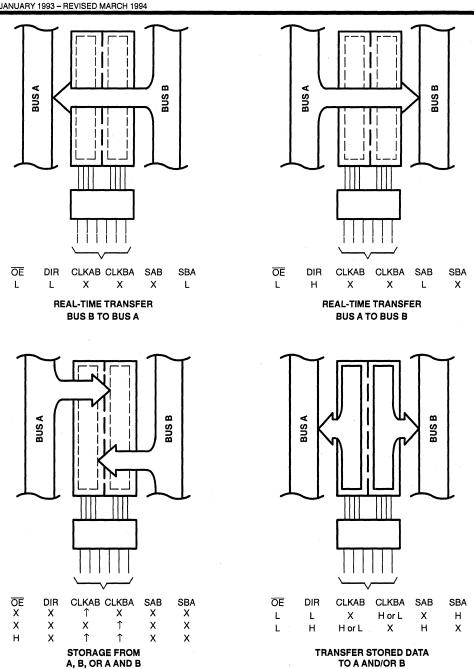


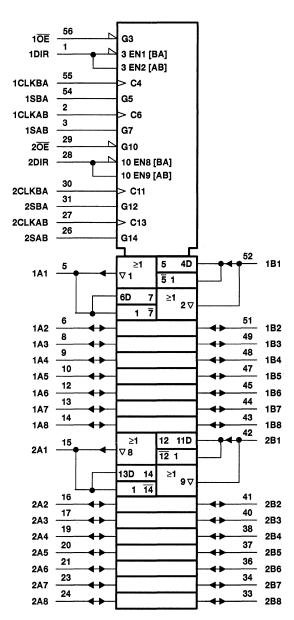
Figure 1. Bus-Management Functions



SN74ALVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS265 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†

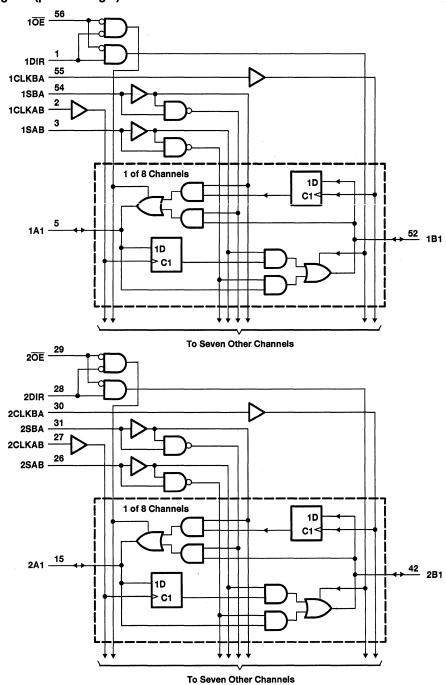


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN74ALVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS265 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)





SN74ALVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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FUNCTION TABLE

	INPUTS						A I/Os	ODERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Х	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified†
Х	X	Х	1	X	Х	Unspecified [†]	Input	Store B, A unspecified†
Н	X	1	1	Х	Х	Input	Input	Store A and B data
н	Х	H or L	H or L	X	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	H or L	Х	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	Х	Н	Х	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V	/
Input voltage range, V _I (except I/O ports) (see Note 1)	
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	/
Output voltage range, V _O (see Notes 1 and 2)	/
Input clamp current, I_{IK} ($V_I < 0$)	١
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	١
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package 1.4 W	
Storage temperature range -65°C to 150°C	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VιΗ	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V_{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧į	Input voltage				V
٧o	Output voltage		0	VCC	V
lou	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
ЮН		V _{CC} = 3 V		-24	111/
lai	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	V _{CC} = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS265 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	2	·
		la 10 mA	2.7 V	2.2		v
VOH		IOH = -12 mA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
Ц		V _I = V _{CC} or GND	3.6 V		±5	μА
lia in	Data I/Os	V _I = 0.8 V	3 V	75		
l(hold)	Data I/Os	V _I = 2 V]	-75		μА
loz‡		VO = VCC or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	Ĺ	40	μА
ΔICC		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	VO = VCC or GND	3.3 V			рF

T For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

(TOP VIEW)

10EAB

1CLKAB 🛚 2

1SAB 🛮 3

GND 4

1A1 🛮 5

1A2 **1**6

V_{CC} **∐** 7

1A3 🛮 8

1A4 🛮 9

1A5 II 10

GND [] 11

1A7 1 13

1A8 II 14

2A1 🛮 15

2A2 🚺 16

2A3 1 17

GND 1 18

2A4 1 19

2A5 20

2A6 D 21

V_{CC} 1 22

2A7 23

2A8 🛮 24

GND 1 25

2SAB 26

2CLKAB 27

20EAB 28

12

1A6 🛮

SCAS266 - JANUARY 1993 - REVISED MARCH 1994

56 1 1 OEBA

55 1 1CLKBA

54 1SBA

53 GND

52 1B1

51 1B2

50 V_{CC}

49 1B3

48 1B4

47 1 1B5 46 GND

45 1B6

44 🛮 1B7

43**∏** 1B8

42 2B1

41 2B2

40**∏** 2B3

39 GND

38 2B4

37 2B5

36 D 2B6

35 🛮 V_{CC}

34 2B7

33 D 2B8

32 GND

31 2SBA

30 2CLKBA

29 20EBA

•	Member of	the Texas Instrui	nents
	Widebus™	Family	

EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process

- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether

real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVC16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

The SN74ALVC16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16652 is characterized for operation from -40°C to 85°C.

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SN74ALVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS266 - JANUARY 1993 - REVISED MARCH 1994

FUNCTION TABLE

		INPU	TS			DATA	A 1/0†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	Н	1	1	X	X	Input	Input	Store A and B data
×	Н	1	H or L	Х	X	Input	Unspecified [‡]	Store A, hold B
н	Н	1	1	x ‡	X	Input	Output	Store A in both registers
L	X	H or L	1	\mathbf{X}^{r}	Х	Unspecified [‡]	Input	Hold A, store B
L	L	1	1	X	x ‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	, X	Н	Output	Input	Stored B data to A bus
н	Н	X ·	X	L	X	Input	Output	Real-time A data to B bus
Н	Н	H or L	Χ	Н	Х	Input	Output	Stored A data to B bus
н	L	H or L	H or L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

SN74ALVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS266 - JANUARY 1993 - REVISED MARCH 1994

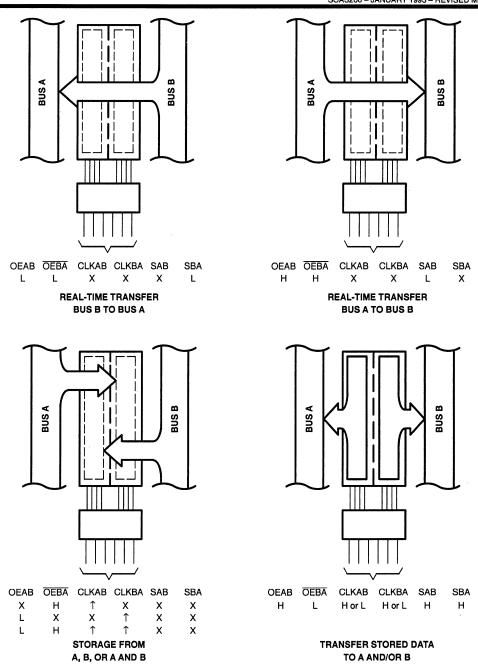


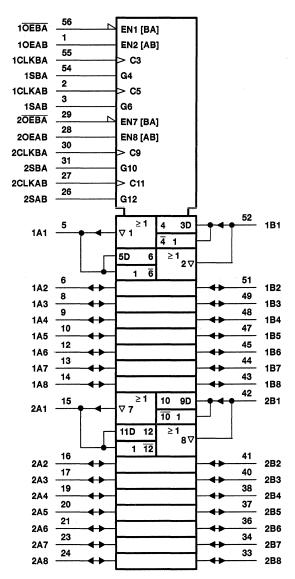
Figure 1. Bus-Management Functions



SN74ALVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS266 - JANUARY 1993 - REVISED MARCH 1994

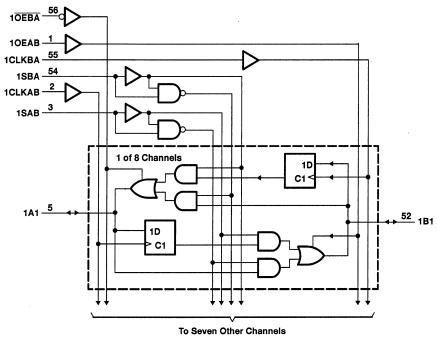
logic symbol†

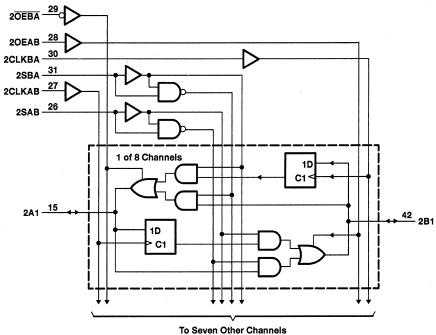


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)







SN74ALVC16652 **16-BIT BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS

SCAS266 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI					٧
Vo	Output voltage				٧
1	High-level output current	V _{CC} = 2.7 V		-12	mΑ
ЮН		V _{CC} = 3 V		-24	111/2
	Love lovel cultivit current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current V _{CC} = 3 V		ŀ	24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ŝ



SN74ALVC16652 **16-BIT BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS SCAS266 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN MA	X UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
\		la 10 mA	2.7 V	2.2	$\exists \ \lor$
VOH		IOH = -12 mA	3 V	2.4	¬ '
		I _{OH} = -24 mA	3 V	2	
		I _{OL} = 100 μA	MIN to MAX	C	.2
VOL		I _{OL} = 12 mA	2.7 V	C	.4 V
į		I _{OL} = 24 mA	3 V	0.	55
lį		V _I = V _{CC} or GND	3.6 V	=	.5 μA
	Data I/Oa	V _I = 0.8 V	2.1/	75	
l(hold)	Data I/Os	V _I = 2 V	3 V	-75	- μΑ
loz‡		V _O = V _{CC} or GND	3.6 V	±	0 μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10 иА
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		7!	60 дА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		pF
Cio	A or B ports	VO = VCC or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS267 - MARCH 1993 - REVISED MARCH 1994

DGG OR DL PACKAGE

ITOD VIEWA

•	Member of the Texas Instruments
	<i>Widebus</i> ™ Family
•	EDIC IM (Enhanced-Performance In

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The SN74ALVC16721's twenty flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs, provided that the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

	(IOP VI	EW)	
		7	
<u>oe</u> [56	CLK
Q1 [55	D1
Q2 [D2
GND [53	GND
Q3 [52] D3
Q4 [6] D4
v _{cc} [7	50]v _{cc}
Q5 [8	49] D5
Q6 [9	48	D6
Q7 [10	47	D7
GND [46	GND
Q8 [12	45	D8
Q9 [13	44	D9
Q10 [14	43	D10
Q10 [Q11 [15	42	D11
Q12 🛛	16	41	D12
Q13 [17	40	D13
GND [39	GND
Q14 [38	D14
Q15 [20	37	D15
Q16 [21	36	D16
v _{cc} [22	35	V _{CC}
Q17 [23	34	D17
Q18 [24		D18
GND [32	GND
Q19 [26	31	D19
Q20 [27	30	D20

NC 28

29 CLKEN

The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16721 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16721 is characterized for operation from -40°C to 85°C.

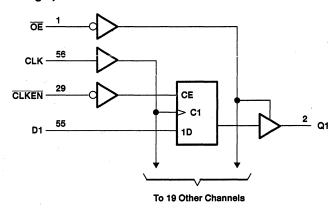
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FUNCTION TABLE (each flip-flop)

	INPU	OUTPUT		
ŌE	CLKEN	CLK	D	q
L	Н	Х	Н	Q ₀
L	L	1	Н	Н
L	L	1	L	L.
L	L	L	Х	Q ₀
Н	X	X	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG	
DL pa	ckage 1.4 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.For more information, refer to the Package Thermal Considerations application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	Vcc	٧
Vo	Output voltage		0	Vcc	٧
		V _{CC} = 2.7 V		-12	A
IOH	High-level output current	V _{CC} = 3 V		-24	mA
1	Lavida and and anima at	V _{CC} = 2.7 V		12	4
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP	MAX	UNIT
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
V	la 10 mA	2.7 V	2.2		v
VOH	I _{OH} = -12 mA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = V _{CC} or GND	3.6 V		±5	μΑ
1	V ₁ = 0.8 V	3 V	75		
l(hold)	V _I = 2 V	3 V	-75		μА
loz	VO = VCC or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μА
Ci	$V_I = V_{CC}$ or GND	3.3 V	4		pF
Co	V _O = V _{CC} or GND	3.3 V	6		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS267 - MARCH 1993 - REVISED MARCH 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

					3.3 V 5 V	V _{CC} =		V _{CC} =	2.7 V	UNIT
	·			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			0	150	0	150	0	150	MHz
t _W	t _w Pulse duration, CLK high or low									ns
	Catum time	Data before CLK↑	High or low	3					,	
t _{su}	Setup time	CLKEN before CLK↑	High or low	3						ns
th Hold time		Data after CLK↑	High or low	0						
th	noid time	CLKEN after CLK1	High or low	0						ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)		3.3 V 5 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INPOT)	(001201)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
t _{PLH}	CLK	Q		4		4.5			ns
t _{PHL}	OLK	<u> </u>		4		4.5			113
^t PZH	ŌĒ	Q		5		5.7			ns
t _{PZL}	OE .	· ·		5		5.7			115
^t PHZ	ŌĒ	. Q		4.5		4.5			ns
tPLZ	OE.	<u> </u>		4.5		4.5			115

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

SN74ALVC16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

SCAS268 - MARCH 1993 - REVISED MARCH 1994

	SCAS268 - MARCH 1993 - REVISED MARCH 1994
 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 56 CLK
 Supports Unregulated Battery Operation Down to 2.7 V 	1Q1
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	V _{CC} 07 50 V _{CC} 3Q1 08 49 0D3
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown	3Q2 🗓 9 48 🖟 NC 4Q1 🗓 10 47 🖟 D4
Resistors Package Options Include Plastic 300-mil	GND
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	5Q1
description	6Q1
This 10-bit flip-flop is designed specifically for low-voltage 3.3-V V _{CC} operation.	GND 18 39 GND 7Q2 19 38 NC
The flip-flops of the SN74ALVC16820 are edge-triggered D-type flip-flops. On the positive	8Q1 020 37 D8 8Q2 021 36 NC
transition of the clock (CLK) input, the device provides true data at the Q outputs.	V _{CC}
A buffered output-enable (OE) input can be used to place the ten outputs in either a normal logic	9Q2
state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither	10Q1
load nor drive the bus lines significantly. The	2 0E [28 29] NC

The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16820 is characterized for operation from -40°C to 85°C.

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load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for

interface or pullup components.

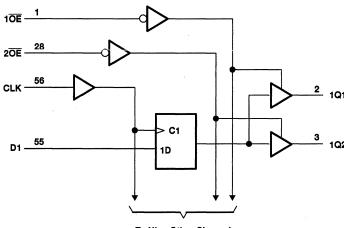


FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE _n t	CLK	D	Q _n †
L	1	Н	Н
L	1	L	L
L	L	Х	Q ₀
Н	Х	Х	Z

†n = 1, 2

logic diagram (positive logic)



To Nine Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Output voltage range, V_O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) ±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$ ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.For more information, refer to the Package Thermal Considerations application note.



SN74ALVC16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS SCAS268 - MARCH 1993 - REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	Vcc	٧
Vo	Output voltage		0	Vcc	V
1	Library and a standard and a summark	V _{CC} = 2.7 V		-12	^
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
la.	Law lavel autout aureant	V _{CC} = 2.7 V		12	A
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	I _{OH} = -12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
Ŋ	V _I = V _{CC} or GND	3.6 V		±5	μА
	V _I = 0.8 V	3 V	75		4
l(hold)	V _I = 2 V		- 75		μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μА
Ci	V _I = V _{CC} or GND	3.3 V	4		pF
Co	VO = VCC or GND	3.3 V	6		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

SCAS268 - MARCH 1993 - REVISED MARCH 1994

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 3.3 V ± 0.15 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low								ns
t _{su}	Setup time, data before CLK↑	High or low	0.8		1				ns
th	Hold time, data after CLK↑	High or low	2		2				ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)		3.3 V 5 V	VC ± 0:	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
tPLH .	CLK	Q		4		4.5			ns
t _{PHL}	OLK	y		4		4.5			113
^t PZH	ŌĒ	Q		5		5.7			ns
tPZL	OE .	3		5		5.7			113
t _{PHZ}	ŌĒ	Q		4.5		4.5			ns
^t PLZ	OL .			4.5		4.5			110

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



SN74ALVC16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS269 - MARCH 1993 - REVISED MARCH 1994

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 0E 1 56 1CLK 1Q1 2 55 1D1
 Supports Unregulated Battery Operation Down to 2.7 V 	1Q2
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q3
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	V _{CC} 7 50 V _{CC} 1Q5 8 49 1D5
 Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1Q6
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink 	1Q8
Small-Outline (DGG) Packages	1Q10
description This 20-bit bus-interface flip-flop is designed	2Q3
specifically for low-voltage (3.3 V) V_{CC} operation.	2Q4
The SN74ALVC16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The twenty flip-flops are edge-triggered D-type flip-flops. On	2Q6
the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.	2Q7
A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic	GND
state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.	2 0E 28 29 2CLK

The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16821 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16821 is characterized for operation from -40°C to 85°C.

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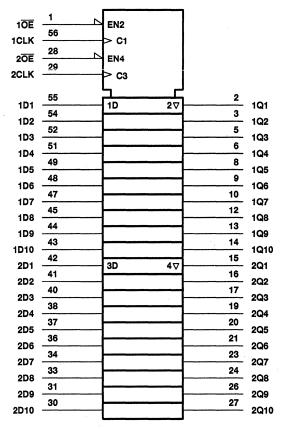
SN74ALVC16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS269 - MARCH 1993 - REVISED MARCH 1994

FUNCTION TABLE (each 10-bit flip-flop)

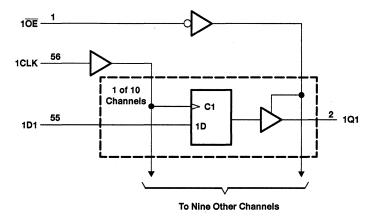
	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	н
L	1	L	L
L	L	Х	Q ₀
Н	X	Х	Z

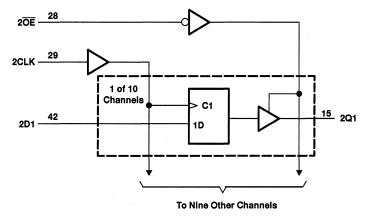
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74ALVC16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS269 - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG packa	
DL package	e 1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
Vj	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
lau	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	riigir-iever odiput carrent	V _{CC} = 3 V		-24	IIIA
lai	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS269 - MARCH 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN 1	TYP MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	I _{OH} = – 12 mA	2.7 V	2.2		v
Voн	10H = -12 11M	3 V	2.4		, v
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = V _{CC} or GND	3.6 V		±5	μA
lia i s	V _I = 0.8 V	3 V	75		
l(hold)	V _I = 2 V		- 75		μΑ
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μA
ΔlCC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μА
Ci	V _I = V _{CC} or GND	3.3 V		4	pF
Co	$V_O = V_{CC}$ or GND	3.3 V		6	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 3.3 V ± 0.15 V				V _{CC} = 2.7 V		UNIT
1			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
t _W	Pulse duration, CLK high or low								ns
t _{su}	Setup time, data before CLK↑	High or low	3						ns
th	Hold time, data after CLK↑	High or low	0						ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO		V _{CC} = 3.3 V ± 0.15 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(INPOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
tPLH	CLK	CLK Q —		4		4.5			ns
tPHL	OLK			4		4.5			115
^t PZH	ŌĒ	Q		5		5.7			ns
tPZL	06	'		5		5.7			113
t _{PHZ}	ŌĒ	Q		4.5		4.5			ns
tPLZ		"		4.5		4.5			115

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



SN74ALVC16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS270 - JANUARY 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVC16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

DGG OR DL PACKAGE (TOP VIEW)

	1	1 1		
1CLR	1	O	56]1CLK
10E	2		55	1CLKEN
1Q1 [3		54] 1D1
GND [4		53] GND
1Q2 [5		52	1D2
1Q3 [51] 1D3
V _{CC} [7		50]v _{cc}
1Q4 [8] 1D4
1Q5 [48] 1D5
1Q6 [1D6
GND [11		46] GND
1Q7 [45	1D7
1Q8 [] 1D8
1Q9 [] 1D9
2Q1 []2D1
2Q2 []2D2
2Q3 []2D3
GND []GND
2Q4 [38]2D4
2Q5				2D5
2Q6]2D6
V _{CC}]v _{cc}
2Q7 [2D7
2Q8 [2D8
GND [GND
2Q9 [2D9
20E				2CLKEN
2CLR	28		29]2CLK

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16823 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16823 is characterized for operation from -40°C to 85°C.

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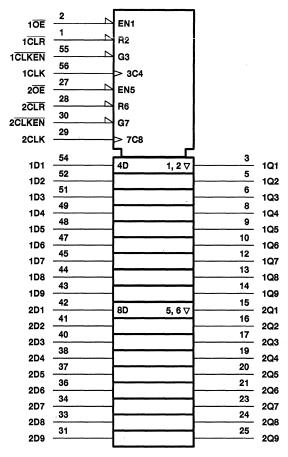
SN74ALVC16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS270 - JANUARY 1993 - REVISED MARCH 1994

FUNCTION TABLE (each 9-bit flip-flop)

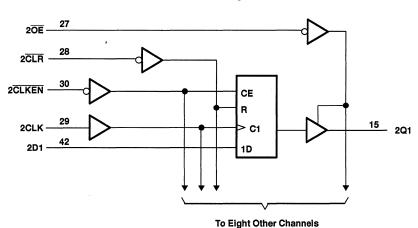
	INPUTS							
ŌĒ	CLR	CLKEN	CLK	D	Q			
L	L	X	Х	Х	L			
L	Н	L	1	Н	Н			
L	Н	L	1	L	L			
L	Н	L .	L	Х	Q ₀			
L	Н	Н	Χ	Х	Q ₀			
Н	Х	Х	Х	Х	Z			

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





SN74ALVC16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS270 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DG	
DL	package 1.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
Vį	Input voltage		0	٧cc	٧
Vo	Output voltage		0	٧cc	٧
	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	111/
lai	Low-level output current	V _{CC} = 2.7 V		12	mΑ
lOL	Low-level output current	V _{CC} = 3 V		24	шА
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ô



18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS270 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Vou	I _{OH} = -12 mA	2.7 V	2.2	v
Voн	IOH = - 12 IIIA	3 V	2.4	ľ
	I _{OH} = -24 mA	3 V	2	
	l _{OL} = 100 μA	MIN to MAX	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4	V
	I _{OL} = 24 mA	3 ∨	0.55	
lį	V _I = V _{CC} or GND	3.6 V	±5	μΑ
lia in	V _I = 0.8 V	3 V	75	μА
l (hold)	V _I = 2 V		-75	
loz	V _O = V _{CC} or GND	3.6 V	±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μΑ
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		750	μА
Ci	V _I = V _{CC} or GND	3.3 ∨		pF
Co	V _O = V _{CC} or GND	3.3 ∨		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16825 18-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS271 - OCTOBER 1993 - REVISED MARCH 1994

- Member of the Texas Instruments
 Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74ALVC16825 is an 18-bit buffer and line driver designed for 2.7-V to 3.6-V V_{CC} operation. It will improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all nine affected outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16825 is available in Tl's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16825 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

		l l		
10E1	Q 1		56	10E2
1Y1	Q 2		55] 1A1
1Y2	Ιз		54	1A2
GND	4		53	GND
1Y3	5		52	
1Y4	6		51] 1A4
Vcc	7		50] v _{cc}
1Y5	8		49] 1A5
1Y6	9		48] 1A6
1Y7	10		47] 1A7
GND	11		46	GND
1Y8	12] 1A8
	13			1A9
GND	14		43	GND
GND	15		42	GND
2Y1	16		41	2A1
2Y2	17		40] 2A2
GND	18		39	GND 2A3
2Y3	19 20		38] 2A3
			37] 2A4
2Y5	21		36	2A5
	22		35] v _{cc}
2Y6	23		34	2A6
	24		33	2A7
	25		32	GND
2Y8	26		31] 2A8
	27		30	2A9
20E1	28		29	2 0E 2

FUNCTION TABLE (each 9-bit section)

		INPUTS	OUTPUT	
Ì	OE1	OE2	Α	Y
Ī	L	L	L	L
l	L	L	Н	Н
١	Н	X	Χ	Z
l	Χ	Н	X	z

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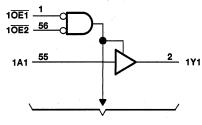


SN74ALVC16825 18-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

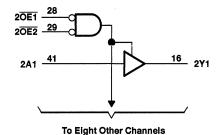
SCAS271 - OCTOBER 1993 - REVISED MARCH 1994

logic symbol† EN₁ 56 10E2 28 20E1 29 EN₂ 20E2 55 1A1 1 🗸 1Y1 3 54 1A2 **1Y2** 52 5 1A3 1Y3 51 6 1A4 1Y4 49 8 1Y5 1A5 48 1A6 **1Y6** 47 10 1A7 177 45 12 1A8 1Y8 44 13 1Y9 1A9 41 16 2A1 2Y1 40 17 2A2 2Y2 38 19 2A2 2Y3 37 20 2Y4 2A3 36 21 2A4 2Y5 34 23 2A5 2Y6 33 24 2A6 2Y7 31 26 2A7 2Y8 30

logic diagram (positive logic)



To Eight Other Channels



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

2Y9

Supply voltage range, V _{CC} –0.	5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	/ _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	$I_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	. ±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	. ±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



SN74ALVC16825 18-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS271 - OCTOBER 1993 - REVISED MARCH 1994

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	V
۷ _I	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	V
	High-level output current	V _{CC} = 2.7 V		-12	^
IOH	High-level output current	V _{CC} = 3 V		-24	mA
la.	Low-level output current	V _{CC} = 2.7 V		12	4
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δv	Input transition rise or fall rate		0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	vcct	MIN	MAX	UNIT	
		I _{OH} = -100 μA		V _{CC} -0.2			
V		10 mA	2.7 V	2.2] , [
VOH		I _{OH} = -12 mA	3 V	2.4		V .	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
v_{OL}		I _{OL} = 12 mA	2.7 V		0.4	.4 V	
		I _{OL} = 24 mA	3 V		0.55		
lj	Control pins	V _I = V _{CC} or GND	3.6 V		±5	μА	
1	Data nina	V _I = 0.8 V	2.1/	75	75		
l(hold)	Data pins	V _I = 2 V	3 V	-75		μА	
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА	
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μА	
Ci		V _I = V _{CC} or GND	3.3 V			pF	
C _{o.}		V _O = V _{CC} or GND	3.3 V			рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVC16827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS272 - JANUARY 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit noninverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC16827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16827 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 10-bit section)

	INPUTS		OUTPUT
OE1	ŌE2	Α	Y
L	L	L	L
L	L	Н	н
Н	X	Χ	z
Х	Н	Х	z

DGG OR DL PACKAGE (TOP VIEW)

			1 1			
10E1		1		56		1 OE 2
1Y1	Q	2				1A1
1Y2		3		54	þ	1A2
GND		4		53		
1Y3		5		52	þ	1A3
1Y4		6		51	þ	A14
V_{CC}		7		50	þ	V_{CC}
1Y5	Q			49	0	1A5
1Y6				48	P	1A6
1Y7				47	þ	1A7
GND		11	,	46	p	GND
1Y8				45	0	1A8
1Y9		13		44	p	1A9
1Y10		14		43	р	1A10
2Y1				42	0	2A1
2Y2	Ц	16		41	р	2A2
2Y3				40	р	2A3
GND	Ц	18		39	р	GND
2Y4						2A4
2Y5		20		37	D	2A5
2Y6		21		36	D	2A6
V_{CC}	9	22		35	0	V_{CC}
2Y7 2Y8	9	23		34	0	2A7
2Y8	Ц	24				2A8
GND						GND
2Y9						2A9
2Y10		27		30	D	2A10
20E1	9	28		29	P	2 <u>0E2</u>
					•	

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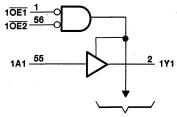
SN74ALVC16827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS272 – JANUARY 1993 – REVISED MARCH 1994

logic symbol†

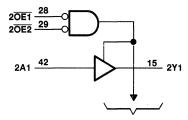
				_	
10E1	1	&	-		
10E2	56	Į.	EN1		
	28	-	1		
20E1	29	1	EN2		
20E2		L] _		
1A1	55		1 1▽	2	1Y1
1A2				3	1Y2
1A3	52		:	5	1Y3
1A4	51			6	1Y4
1A5	49			8	1Y5
1A6	48			9	1Y6
1A7	47	1		10	1 Y 7
1A8	45			12	1Y8
1A9	44			13	1Y9
1A10	43			14	1Y10
2A1	42		1 2∇	15	2Y1
2A2	41			16	2Y2
2A3	40			17	2Y3
2A4	38			19	2Y4
2A5	37			20	2Y5
2A6	36			21	2Y6
2A7	34			23	2Y7
2A8	33			24	2Y8
2A9	31			26	2Y9
2A10	30			27	2Y10

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Nine Other Channels



To Nine Other Channels

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Storage temperature range –	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷į	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	nia
la.	Low lovel extent extent	V _{CC} = 2.7 V		12	mA
lOF	Low-level output current V _{CC} = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	<i>,</i> ℃

SN74ALVC16827 **20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
\/~··	Jan. 10 mA	2.7 V	2.2	v
∨он	IOH = -12 mA	3 V	2.4	\ \
	I _{OH} = -24 mA	3 V	2	
	I _{OL} = 100 μA	MIN to MAX	0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V	0.4	V
	I _{OL} = 24 mA	3 V	0.55	
II	V _I = V _{CC} or GND	3.6 V	±5	μА
1	V _I = 0.8 V	3 V	75	
l(hold)	V _I = 2 V	¬	-75	μА
loz	V _O = V _{CC} or GND	3.6 V	±10	μА
Icc	V _I = V _{CC} or GND, I _O = 0	3.6 V	40	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		750	μА
Ci	V _I = V _{CC} or GND	3.3 V		pF
Co	V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16828 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit inverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16828 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC16828 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16828 is characterized for operation from -40°C to 85°C.

d for

FUNCTION TABLE

(each 10-bit section)							
	INPUTS	OUTPUT					
OE1	OE2	Α	Υ				
L	L	L	Н				
L	L	Н	L				
Н	X	Х	z				
Х	Н	Χ	z				

DGG OR DL PACKAGE (TOP VIEW)

			u			
10E1				56	0	10E2
1Y1	0	2				1A1
1Y2	0	3		54	þ	1A2
					0	GND
1Y3	0	5		52		1A3
1Y4	q	6		51		A14
V_{CC}	q	7		50	þ	V_{CC}
1Y5	q	8		49		1A5
				48	D	1A6
		10		47	D	1A7
		11		46		
1Y8				45	0	1A8
1Y9						1A9
		14		43		1A10
	-	15				2A1
2Y2						2A2
2Y3				40	D	2A3
		18		39	Q	GND
		19		38	Į	2A4
	_	20				2A5
	3	21				2A6
		22		35		V_{CC}
		23				2A7
2Y8						2A8
		25		32	Ц	GND
2Y9					Ų	2A9
	3	27		30	Ų	2A10
20E1	4	28		29	μ	2 OE 2

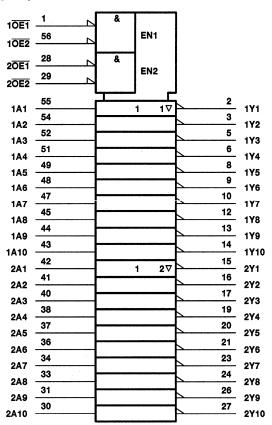
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SN74ALVC16828 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

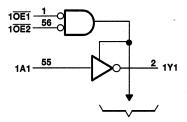
SCAS273 - JANUARY 1993 - REVISED MARCH 1994

logic symbol†

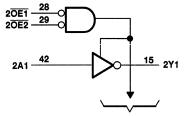


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Nine Other Channels



To Nine Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ I } < 0)$	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	
, , , , , , , , , , , , , , , , , , , ,	DL package 1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage	upply voltage			
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷ _I	Input voltage			VCC	٧
٧o	Output voltage		0	٧cc	٧
	High-level output current	V _{CC} = 2.7 V		-12 m/	mA
ЮН		V _{CC} = 3 V		-24) III/
lo	Lauren and a standard and a standard	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16828 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Vair	la 10 mA	2.7 V	2.2	v
Voн	$I_{OH} = -12 \text{ mA}$	3 V	2.4	v
	I _{OH} = -24 mA	3 V	2	
	I _{OL} = 100 μA	MIN to MAX	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4	٧
	I _{OL} = 24 mA	3 V	0.55	
lj .	$V_I = V_{CC}$ or GND	3.6 V	±5	μΑ
lia in	V _I = 0.8 V	3 V	75	μА
l(hold)	V _I = 2 V		-75	
loz	V _O = V _{CC} or GND	3.6 V	±10	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μА
Δl _{CC}	$V_{\rm CC}$ = 3 V to 3.6 V, One input at $V_{\rm CC}$ – 0.6 V, Other inputs at $V_{\rm CC}$ or GND		750	μА
Ci	V _I = V _{CC} or GND	3.3 V		pF
Co	V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74ALVC16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS274 - JANUARY 1993 - REVISED MARCH 1994

	00/102/1	JANUART I	OOO ILLY
 Member of the Texas Instruments Widebus™ Family 		R DL PACI OP VIEW)	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 0E		1LE
Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater	1Q1	3 54 4 53	1D1 1D2 GND 1D3
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q4 [] 6 V _{CC} [] 7	6 51	1D3 1D4 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q5 [] 8 1Q6 [] 9	8 49	1D5 1D6
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	1Q7	11 46	1D7 GND 1D8
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	1Q9 [1 1Q10 [1 2Q1 [1	13 44 14 43 15 42	1D9 1D10 2D1
description	2Q2 1 2Q3 1 GND 1	17 40	2D2 2D3 GND
This 20-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.	2Q4 [] 1 2Q5 [] 2	19 38	2D4 2D5
The SN74ALVC16841 features 3-state outputs designed specifically for driving highly capacitive	2Q6 [] 2 V _{CC} [] 2		2D6 V _{CC}
or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.	2Q7 0 2 2Q8 0 2 GND 0 2	23 34 24 33	2D7 2D8 GND
The SN74ALVC16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are	2Q9	26 31 27 30	2D9 2D10
transparent D-type latches. The device has	2 0E U 2	28 29	2LE

A buffered output-enable (10E or 20E) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable (\overline{OE}) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16841 is characterized for operation from -40°C to 85°C.

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transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.



SN74ALVC16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS274 - JANUARY 1993 - REVISED MARCH 1994

FUNCTION TABLE (each 10-bit latch)

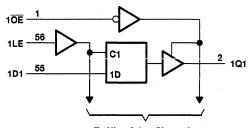
	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Χ	Q ₀
Н	Х	X	z

logic symbolt

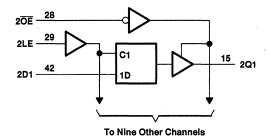
10E EN2 56 1LE C1 28 2OE EN4 29 2LE СЗ 55 2 1D1 1D 1Q1 2 ▽ 54 3 1D2 1Q2 5 52 1D3 1Q3 51 6 1D4 1Q4 49 8 1D5 1Q5 9 48 1D6 1Q6 47 10 1D7 1Q7 45 12 1D8 1Q8 44 13 1D9 1Q9 43 14 1D10 1Q10 42 15 2D1 3D 4 ▽ 2Q1 41 16 2D2 2Q2 40 17 2D3 2Q3 38 19 2D4 2Q4 37 20 2D5 2Q5 36 21 2D6 2Q6 34 23 2D7 2Q7 33 24 2D8 2Q8 31 26 2D9 2Q9 30 27 2D10 2Q10

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Nine Other Channels



SN74ALVC16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS274 - JANUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package	
DL package	
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
۷ _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
٧ı	Input voltage			Vcc	٧
۷o	Output voltage		0	VCC	٧
lou	High-level output current $\frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}}$	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	
loi	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS274 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
V	Jan. 10 mA	2.7 V	2.2	v
VOH	IOH = -12 mA	3 V	2.4	\ \
	I _{OH} = -24 mA	3 V	2	
	I _{OL} = 100 μA	MIN to MAX	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4	V
	I _{OL} = 24 mA	3 V	0.55	
lį	V _I = V _{CC} or GND	3.6 V	±5	μΑ
1	V _I = 0.8 V	3 V	75	
l(hold)	V _I = 2 V	7 ''	- 75	μА
loz	V _O = V _{CC} or GND	3.6 V	±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μΑ
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		750	μА
C _i	V _I = V _{CC} or GND	3.3 V		pF
Co	V _O = V _{CC} or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS275 - JANUARY 1993 - REVISED MARCH 1994

		INT 1993 - REVISED MARCH 199
Member of the Texas Instruments Widebus™ Family	DGG OR DL F (TOP VI	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>CLR</u> [1 1 <u>OE</u> [2	56 1LE
• Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater	1Q1 [] 3 GND [] 4	55 1 1PRE 54 1 1D1 53 1 GND
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q2 [5 1Q3 [6 V _{CC} [7	52 1 1D2 51 1 1D3 50 1 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q4 [] 8 1Q5 [] 9	49 1D4 48 1D5
Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	1Q6	47 1 1D6 46 1 GND 45 1 1D7
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1Q8 🛮 13 1Q9 🗓 14	44 1 1D8 43 1D9
Small-Outline (DGG) Packages	2Q1	42 2D1 41 2D2
description	2Q3 🛭 17 GND 🗓 18	40 J 2D3 39 J GND
This 18-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.	2Q4 [] 19 2Q5 [] 20	38 2D4 37 2D5
The SN74ALVC16843 features 3-state outputs designed specifically for driving highly capacitive	2Q6 [21 V _{CC} [22	36 2D6 35 V _{CC}
or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.	2Q7 [23 2Q8 [24 GND [25	34
The SN74ALVC16843 can be used as two 9-bit latches or one 18-bit latch. The eighteen latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true	2Q9 26 2OE 27 2CLR 28	31 2D9 30 2PRE 29 2LE

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16843 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16843 is characterized for operation from -40°C to 85°C.

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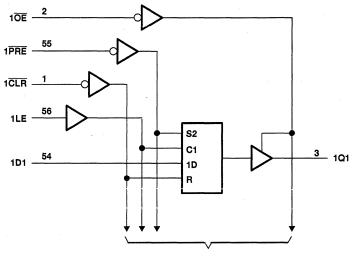


data at its outputs.

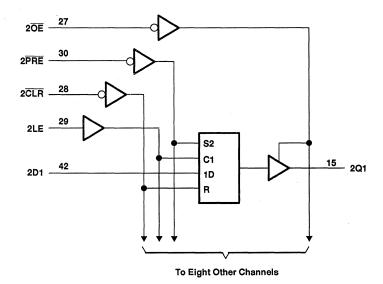
SN74ALVC16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS275 - JANUARY 1993 - REVISED MARCH 1994

logic diagram (positive logic)



To Eight Other Channels



SN74ALVC16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS275 - JANUARY 1993 - REVISED MARCH 1994

FUNCTION TABLE (each 9-bit latch)

	INPUTS						
PRE	CLR	ŌĒ	LE	D	Q		
L	X	L	X	Х	Н		
Н	L	L	X	Χ	L		
Н	Н	L	н	L	L		
Н	Н	L	н	Н	н		
Н	Н	L	L	Χ	Q ₀		
×	X	Н	Х	Χ	z		

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	
, , , , , , , , , , , , , , , , , , , ,	DL package 1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
V_{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
۷Į	Input voltage			VCC	٧
Vo	Output voltage		0	VCC	٧
lou	High-level output current	V _{CC} = 2.7 V		-12	mA
ІОН	riigh-level oalpat carrent	V _{CC} = 3 V		-24	IIIA
1	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	MA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS275 - JANUARY 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
Val	lov. 10 mA	2.7 V	2.2] ,
VOH	IOH = -12 mA	3 V	2.4]
	I _{OH} = -24 mA	3 V	2	
	i _{OL} = 100 μA	MIN to MAX	0.2	
VOL	I _{OL} = 12 mA	2.7 V	0.4] v
	I _{OL} = 24 mA	3 V	0.55	
l _l	V _I = V _{CC} or GND	3.6 V	±5	μА
lia i s	V _I = 0.8 V	3 V	75	
l(hold)	V _I = 2 V	3,	– 75	μΑ
loz	$V_O = V_{CC}$ or GND	3.6 V	±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		750	μА
Ci	V _I = V _{CC} or GND	3.3 V		pF
Co	$V_O = V_{CC}$ or GND	3.3 V		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE

(TOP VIEW)

SCAS277 - JANUARY 1993 - REVISED MARCH 1994

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

				_
1OEAB	ſ.	U	56	1 OEBA
1CLKAB				1CLKBA
1CEAB			54	1CEBA
GND [53	GND
1A1 [52	1B1
1A2			51	1B2
V _{CC}			50	V _{CC}
1A3 [l _R		49	1B3
1A4 [۱		48	1B4
1A5 [47	1B5
GND [46	GND
1A6 [12		45	1B6
1A7 [13		44	1B7
1A8 [43	1B8
2A1 [42	2B1
2A2 [41	2B2
2A3 [40	2B3
GND [39	GND
2A4 [19		38	2B4
2A5 [20		37	2B5
2A6 [36	🛮 2B6
v _{cc} [22		35	₫ v _{cc}
2A7 [23		34] 2B7
2A8 [33] 2B8
GND [GND
2CEAB				2CEBA
2CLKAB				2CLKBA
2 OEAB [28		29	2OEBA

The SN74ALVC16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16952 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INPUTS				
CLKENAB	CLKAB	OEAB	Α	В	
Н	Х	L	Х	B ₀ ‡	
X	L	L	Χ	В ₀ ‡ В ₀ ‡	
L	1	L	L	L	
L	1	L	Н	н	
X	X	Н	Χ	Z	

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

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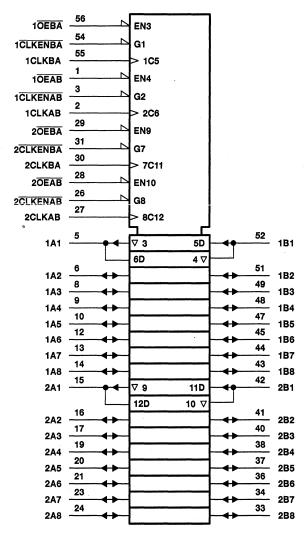
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[‡]Level of B before the indicated steady-state input conditions were established.

SN74ALVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

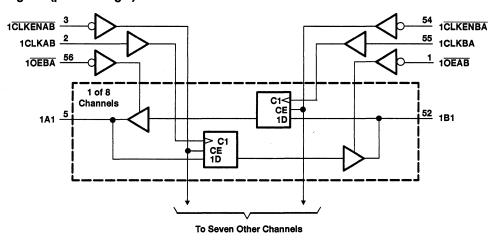
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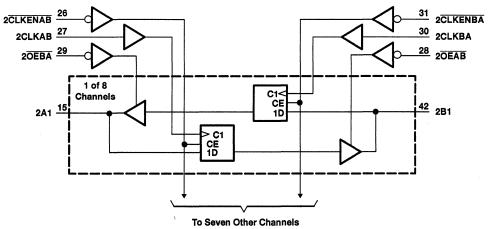
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74ALVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to 4.6 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
VI	Input voltage			VCC	٧
Vo	Output voltage		0	VCC	٧
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
	High-level output current	V _{CC} = 3 V		-24	
	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	HIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C



SN74ALVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.	.2		
		10 m4	2.7 V	2.2		v	
VOH		IOH = -12 mA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧	
		I _{OL} = 24 mA	3 V		0.55		
Ŋ		V _I = V _{CC} or GND	3.6 V		±5	μΑ	
1.4	Data I/Os	V _I = 0.8 V	3 V	2.1/	75		
li(hold)	Data I/Os	V _I = 2 V		-75		μА	
loz‡		V _O = V _{CC} or GND	3.6 V		±10	μА	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			750	μА	
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF	
Cio	A or B ports	VO = VCC or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

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LV MSI AND OCTALS

Features

- 2-μ EPIC™ CMOS process
- Low standby current (20 μA)
- -8-mA/8-mA drive current
- 2.7-V to 3.6-V V_{CC} range
- SOIC, EIAJ SSOP, and TSSOP packaging
- TI has established alternate sources

Benefits

- Medium price/performance designs
- Saves power, extends battery life
- 5-V HCMOS upgrades
- Fully characterized for unregulated battery operation
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS182 - FEBRUARY 1993 - REVISED MARCH 1994

3Y

•	EPIC™ (Enhan	ced-Performance Implanted
	CMOS) 2-µ Pro	cess

- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)						
٠, ١		$\nabla \mathcal{L}_{u}$				
1A 🛭	1	14 V _{CC}				
1B [2	14 V _{CC} 13 4B				
1Y [3	12] 4A				
2A [4	11 🕽 4Y				
2B [5	10 🕽 3B				
2Y [6	9 [] 3A				

GND II 7

description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV00 performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

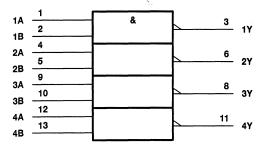
The SN74LV00 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV00 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
Н	Н	L
L	X	Н
Х	L	Н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS182 - FEBRUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VіН	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
٧ı	Input voltage		0		Vcc	٧
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current	,			6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} ‡	MIN	TYP	MAX	UNIT
Vou	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V
Voн	I _{OH} = -6 mA	3 V	2.4			v
Vo	l _{OL} = 100 μA	MIN to MAX			0.2	V
VoL	I _{OL} = 6 mA	3 V			0.4	v
lį	VI = VCC or GND	3.6 V			±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μΑ
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				500	μА
Ci	V _I = V _{CC} or GND	3.3 V		2.5		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS182 - FEBRUARY 1993 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONII
t _{pd}	Α	Υ		9	18		23	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	TYP	UNIT	
Cpc	d Power dissipation capacitance per gate	$C_L = 50 pF$,	f = 10 MHz	23	pF

SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS183 - FEBRUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D,	DB,	OR	PW	PAC	CKAGE	
		mο	P VI	EW))	

1Y [1A [1B [3	U	12	_	V _{CC} 4Y 4B 4A
2Y [2A [2B [GND [4 5 6 7		11 10 9 8		3Y 3B 3A

description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN74LV02 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

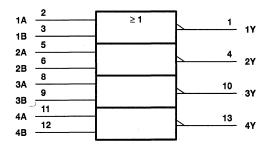
The SN74LV02 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

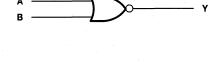
	,	
INP	UTS	OUTPUT
Α	В	Υ
Н	Х	L
X	Н	L
L	L	н
	A H	н х

logic symbol†

logic diagram, each gate (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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SCLS183 - FEBRUARY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range –6	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		VCC	٧
Vο	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
IOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate	_	0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Vou	I _{OH} = -100 μA		MIN to MAX	VCC-0.	2		V
VOH	IOH = - 6 mA		3 V	2.4			V
V	l _{OL} = 100 μA		MIN to MAX			0.2	V
VOL	I _{OL} = 6 mA		3 V			0.4	V
l _l	V _I = V _{CC} or GND		3.6 V			±Ί	μА
lcc	V _I = V _{CC} or GND,	I _O = 0	3.6 V			20	μА
ΔICC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} - 0.6 V,				500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS183 - FEBRUARY 1993 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	Vcc =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
t _{pd}	Α	Y		9	16		20	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	$C_L = 50 pF$,	f = 10 MHz	16	pF

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8 **[**] 4Y

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

(TOP VIEW)									
1A [1	U ₁₄	V _{CC}						
1A [1Y [2	13] V _{CC}] 6A						
	3] 6Y						
2Y [4	11] 5A						
3A [5	10] 5Y] 4A						
3Y [6	9] 4A						

GND II 7

D. DB. OR PW PACKAGE

description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

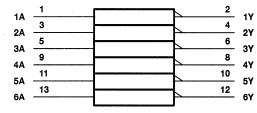
The SN74LV04 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

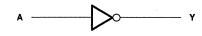
INPUT A	OUTPUT Y
Н	L
L	Ι

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }$ ($V_{ C }$ or $V_{ C }$	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	1.25 W
DB or PW	package 0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
۷ _I	Input voltage		0		Vcc	٧
٧o	Output voltage		0		VCC	V
ЮН	High-level output current				-6	mA
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T _A = -40°C to 85°C			UNIT
PARAMETER			V _{CC} ‡	MIN	TYP	MAX	UNII
Vall	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		٧
Voн	I _{OH} = -6 mA		3 V	2.4			٧
Voi	I _{OL} = 100 μA		MIN to MAX			0.2	٧
VOL	I _{OL} = 6 mA		3 V			0.4	٧
l)	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			20	μĄ
ΔICC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,				500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	Vcc =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
t _{pd}	Α	Υ		7	15		19	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance per inverter	C _L = 50 pF,	f = 10 MHz	18	pF

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9 1 4A

4Y

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)									
1A [1 1Y [2	U ₁₄] V _{CC}] 6A							
1Y 📙 2 2A 🗓 3	13 12] 6A] 6Y							
2Y [] 4	12	5A							
3A 🛮 5	10] 5Y							

3Y **[**

GND II 7

description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \overline{A}$.

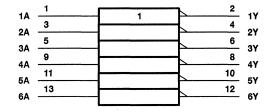
The SN74LVU04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVU04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

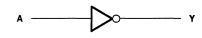
INPUT A	OUTPUT
Н	L
L	Н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
DB or PW pac	kage 0.5 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.4			٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.5	٧
VĮ	Input voltage		0		VCC	٧
٧o	Output voltage		0		VCC	٧
ЮН	H High-level output current				-6	mA
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T _A = -4	85°C	UNIT		
PARAMETER	1531 00	NUTTONS	v _{cc} ‡	MIN TYP MAX		MAX	UNIT	
Vou	VI = VIL,	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.5			٧	
Voн	V _I = GND,	I _{OH} = – 6 mA	3 V	2.4			v	
Voi	VI = VIH,	I _{OL} = 100 μA	MIN to MAX			0.5	٧	
V _{OL}	VI = VCC,	I _{OL} = 6 mA	3 V			0.4	· ·	
l _l	V _I = V _{CC} or GND		3.6 V			±1	μА	
lcc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			20	μА	
ΔlCC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,				500	μА	
Ci	V _I = V _{CC} or GND		3.3 V		7		pF	

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER FROM (INPUT)	FROM	FROM TO		3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII	
t _{pd}	Α	Υ		6	14		18	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

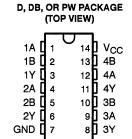
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS			
Cpd	Power dissipation capacitance per inverter	$C_L = 50 pF$,	f = 10 MHz	7	pF	

SN74LV08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

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- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{QLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV08 performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

The SN74LV08 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV08 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

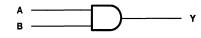
INP	JTS	OUTPUT
Α	В	Υ
Н	Н	Н
L	Χ	L
×	L	L

logic symbol†

1A & 3 2 1B 4 2A 6 5 2B 9 ЗА 8 10 3B 12 4A 11 13 4B

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	1.25 W
DB or DW package	0.5 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
Vj	Input voltage		0		VCC	V
٧o	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mΑ
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} ‡	MIN TY	P MAX	UNIT
Vou	lOH = -100 μA	MIN to MAX	V _{CC} -0.2		V
VOH [*]	l _{OH} = -6 mA	3 V	2.4		V
Vai	l _{OL} = 100 μA	MIN to MAX		0.2	v
VOL	I _{OL} = 6 mA	3 V		0.4	V
Ч	V _I = V _{CC} or GND	3.6 V		±1	μA
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μA
ΔlCC	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} = 0.6 \text{ V}$ Other inputs at V_{CC} or GND	/,		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.	5	pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

SN74LV08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

	PARAMETER FROM (INPUT) (OL	METER FROM		Vcc =	3.3 V ±	0.3 V	VCC =	2.7 V	UNIT
		(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII	
	tpd	A	Y		10	18		23	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

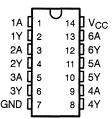
	PARAMETER		TEST CONDITIONS		
Cpd	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	24	pF

HEX SCHMITT-TRIGGER INVERTER

SCLS187 - FEBRUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D, DB,	OR	PW	PACKAGE
	(TOI	٧I	EW)



description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

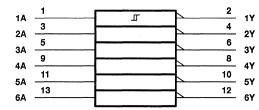
The SN74LV14 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT
Α	T
Н	L
L	Н

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2.4			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.4	V
VI	Input voltage		0		VCC	٧
Vo	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN	TYP MAX	UNIT	
		2.7 V	1	2		
V _{T+}	Positive-going threshold	3 V	1.2	2.2	V	
		3.6 V	1.5	2.4		
		2.7 V	0.4	1.4		
V _T _	Negative-going threshold	3 V	0.6	1.5	٧	
		3.6 V	0.8	1.8		
		2.7 V	0.3	1.1		
ΔV _T	Hysteresis (V _{T+} – V _{T-})	3 V	0.4	1.2	V	
		3.6 V	0.4	1.2		
Vou	$I_{OH} = -100 \mu A$	MIN to MAX	V _{CC} -0.2	2	V	
VOH	$I_{OH} = -6 \text{ mA}$	3 V	2.4		٧	
Vol	I _{OL} = 100 μA	MIN to MAX		0.2] _v	
VOL	IOL = 6 mA	3 V		0.4	V	
=	V _I = V _{CC} or GND	3.6 V		±1	μΑ	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
C _i	V _I = V _{CC} or GND	3.3 V		2.5	pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONII
t _{pd}	A	Y		13	30		36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
Cpd	Power dissipation capacitance per inverter	C _L = 50 pF,	f = 10 MHz	22	pF

QUADRUPLE 2-INPUT POSITIVE-OR GA

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- **EPIC™** (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF,
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D,	DB,	OR	PW	PΑ	CKA	GE
		MΩ	P VI	FW	`	

1A	d₁	U 14	Ъ	Vcc
1B		13	þ	4B
1Y		12	2	4A
2A		11		4Y
2B	[] 5	10	þ	3B
2Y		ç		ЗА
GND	7	8	P	3Y

description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV32 performs the Boolean functions Y = A + B or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

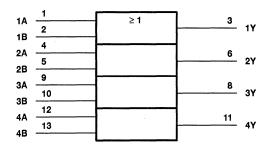
The SN74LV32 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV32 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT		
Α	В	Y		
Н	Х	Н		
Х	Н	Н		
L	L	L		

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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SN74LV32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	
DB or PW packa	ge 0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

		,	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
V _{JL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
٧ı	Input voltage		0		VCC	٧
٧o	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
lol	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} ‡	MIN TYP	MAX	UNIT	
V-:	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		v	
VOH	$I_{OH} = -6 \text{ mA}$	3 V	2.4		ľ	
	I _{OL} = 100 μA	MIN to MAX		0.2	0.2 0.4	
VOL	I _{OL} = 6 mA	3 V		0.4		
ΙΙ	V _I = V _{CC} or GND	3.6 V		±1	μА	
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА	
Ci	V _I = V _{CC} or GND	3.3 V	2.5	5	pF	

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

SN74LV32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	Vcc =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PANAMETER	(INPUT)	(OUTPUT) MIN TYP MAX		MIN	MAX	UNIT		
^t pd	Α	Y		8	17		22	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	23	pF

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- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D,	DB,	OR PW PACKAGE	
		(TOP VIEW)	

	_		
1CLR		U ₁₄	V _{CC} 2CLR
1D [13	2CLR
1CLK [2D
1PRE] 2CLK
	5	10	2PRE
		9] 2Q
GND [7	8] 2 <u>Q</u>

description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74LV74 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV74 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INP	UTS		OUTPUTS		
PRE	CLR	CLK	D	Q	Q	
L	Н	Х	Х	Н	L	
Н	L	X	Х	L	н	
L	L	Х	Χ	нt	н†	
Н	Н	1	Н	Н	L	
Н	Н	1	L	L	н	
Н	Н	L	Х	Q ₀	\overline{Q}_0	

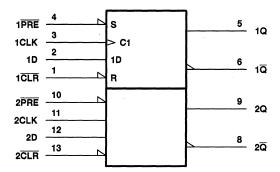
[†] This configuration is nonstable; that is, it will not persist when PRE or CLR returns to its inactive (high) level.

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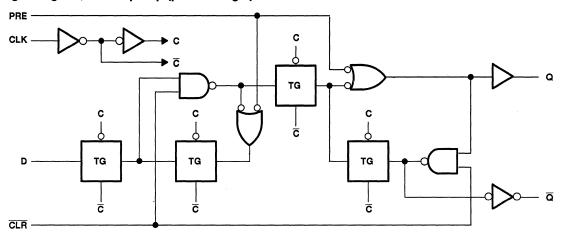
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logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 \
Input voltage range, V _I (see Note 1)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$ ±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package
DB or PW package 0.5 W
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		VCC	V
۷o	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	DITIONS	v _{cc} ‡	MIN	TYP	MAX	UNIT
V	I _{OH} = -100 μA		MIN to MAX	VCC-0.	2		V
VOH	I _{OH} = -6 mA	I _{OH} = – 6 mA			2.4		
Voi	I _{OL} = 100 μA	MIN to MAX			0.2	ν	
VOL	IOL = 6 mA	3 V			0.4	V	
l _l	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μА
ΔlCC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} - 0.6 V,				500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	24	0	19	MHz
	Pulse duration	PRE or CLR low	20		25		
t _w	Pulse duration	CLK high or low	20		25		ns
	Octor time to four OUT	Data	13		16		
t _{su}	Setup time before CLK↑	PRE or CLR inactive	8		10		ns
th	Hold time, data after CLK↑		3		3		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM TO (OUTPUT)	то	V _{CC} =	$V_{CC} \approx 3.3 \text{ V} \pm 0.3 \text{ V}$			V _{CC} = 2.7 V	
		(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
fmax			24	100		19		MHz
^t pd	PRE or CLR	QorQ		16	34		43	ns
	CLK	Q or Q		15	28		35	113

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

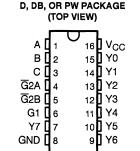
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CO	TYP	UNIT	
C _{pd} Power dissipation capacitance per flip-flop	$C_L = 50 pF$,	f = 10 MHz	32	pF

SN74LV138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LV138 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV138 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

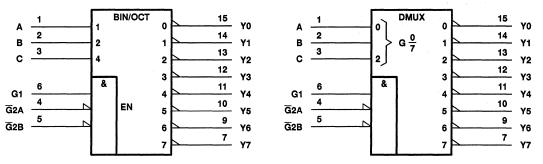
ENA	BLE INF	PUTS	SEL	ECT INF	UTS				OUT	PUTS			
G1	G2A	G2B	O	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y 7
Х	Н	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
Х	X	Н	Х	Χ	Χ	Н	Н	Н	Н	Н	н	Н	Н
L	X	X	Х	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	L	Н	н	Н	Н	н	Н	н
Н	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	L	Н	Н	L	Н	Н	н	Н	н
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	н	L	L	Н	Н	н	Н	L	Н	н	н
Н	L	L	Н	L	Н	Н	Н	н	Н	Н	L	Н	Н
Н	L	L	Н	Н	L	Н	H	Н	Н	Н	Н	L	Н
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

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TEXAS INSTRUMENTS

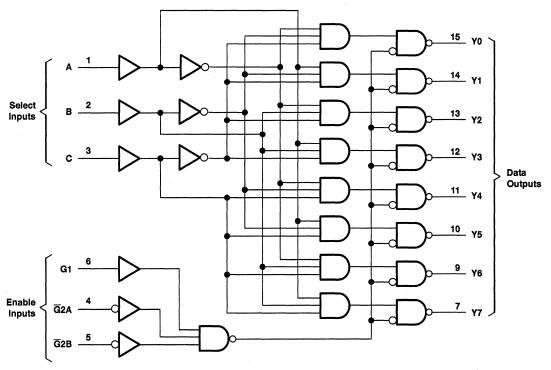
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logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Our also walks are usually V	0.5344 4.034
Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	
DB package	0.55 W
	0.5 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
V _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	ļ		8.0	٧
٧ _I	Input voltage		0		VCC	٧
٧o	Output voltage		0		٧cc	V
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONE	DITIONS	V _{CC} ‡	MIN	TYP	MAX	UNIT
V	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	!		v
VOH	I _{OH} = -6 mA		3 V	2.4			V
Va.	I _{OL} = 100 μA		MIN to MAX			0.2 _V	
VOL	IOL = 6 mA		3 V			0.4	V
l _l	V _I = V _{CC} or GND		3.6 V			±1	μΑ
lcc	V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μΑ
ΔlCC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,				500	μА
Ci	VI = VCC or GND		3.3 V		2.5		рF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LV138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM TO		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
.	A, B or C	v		14	29		36	no.
^T pd	Enable			16	33		41	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per channel	C _L = 50 pF,	f = 10 MHz	47	pF

SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

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 EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process

- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)									
	П	U	ጌ						
ΑL	1	14	٩Ų	V_{CC}					
В [2	13	3 []	Q_H					
Q_A [3	12	2[]	$Q_{\mathbf{G}}$					
Q _B [4	1	ıD	QF					
Q _C [5	10	0	Q_{E}					
Q _D [6	9	9]	CLR					
GND [7	1	3 []	CLK					

description

This 8-bit parallel-out serial shift register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV164 features AND-gated serial (A and B) inputs and an asynchronous clear (CLR) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN74LV164 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV164 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS					UTPUT	S	
CLR	CLK	Α	В	QA	$Q_{B}\dots Q_{H}$		
L	X	Х	Х	L	L	L	
Н	L	Χ	Χ	Q _{A0}	Q_{B0}	Q_{H0}	
Н	1	Н	Н	Н	Q_{An}	Q_{Gn}	
Н	1	L	Χ	L	Q_{An}	QGn	
Н	1	X	L	L	Q_{An}	Q_{Gn}	

 $\rm Q_{AO},\,Q_{BO},\,Q_{HO}$ = the level of $\rm Q_{A},\,Q_{B},\,or\,Q_{H},\,respectively,$ before the indicated steady-state inputs conditions were established.

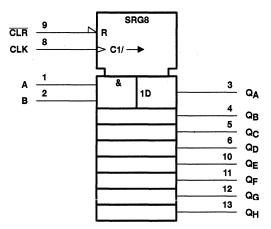
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a 1-bit shift.

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TEXAS INSTRUMENTS

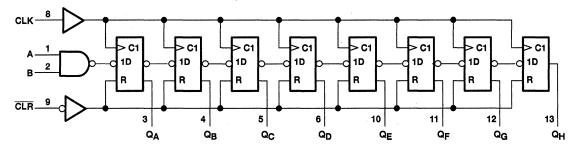
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logic symbol†



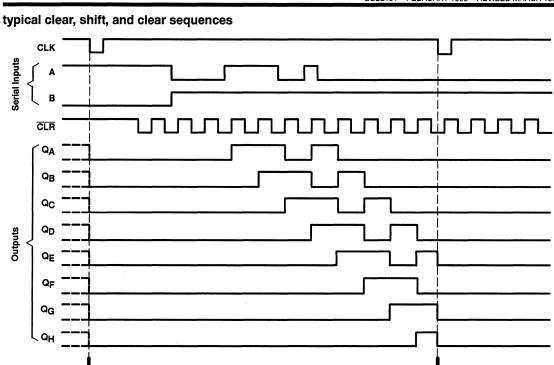
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Clear



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})
Continuous output current, I _O (V _O = 0 to V _{CC}) ±25 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package
DB or PW package 0.5 W
Storage temperature range –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. This value is limited to 4.6 V maximum.

Clear

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		Vcc	٧
٧o	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN	TYP	MAX	UNIT
Vou	lOH = -100 μA	MIN to MAX	V _{CC} -0.2			v
VOH	VOH		2.4			V
V	I _{OL} = 100 μA				0.2	V
VOL	I _{OL} = 6 mA	3 V			0.4	_ v
11	V _I = V _{CC} or GND	3.6 V			±1	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			. 20	μА
ΔlCC	$V_{CC} = 3 \ V \ to \ 3.6 \ V,$ One input at $V_{CC} - 0.6 \ Other$ inputs at V_{CC} or GND	V,			500	μА
Ci	VI = VCC or GND	3.3 V		2.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	3.3 V 3 V V _{CC} = 2.7 V		UNIT	
		•	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	24	0	19	MHz
. D.J	Pulse duration	CLR low	20		25		no
t _w	ruise duration	CLK high or low	20		25		ns
	Out of the before OUT	Data	13		16		
t _{su}	Setup time before CLK↑ CLR inactive		11		14		ns
th	Hold time, data after CLK↑		5		5		ns

SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SCLS191 - FEBRUARY 1993 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
fmax			24	75		19		MHz
t _{pd}	CLK	Q		16	29		36	ns
tPHL	CLR	Q		16	29		36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

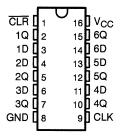
	PARAMETER		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance	$C_L = 50 pF$,	f = 10 MHz	74	pF

SN74LV174 HEX D-TYPE FLIP-FLOP WITH CLEAR

SCLS192 - FEBRUARY 1993 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This hex D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV174 is a monolithic positive-edge-triggered flip-flop with a direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV174 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV174 is characterized for operation from -40°C to 85°C.

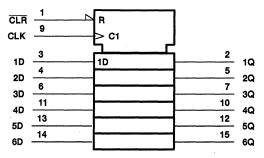
FUNCTION TABLE

	INPUTS	OUTPUT	
CLR	CLK	D	Q
L	Х	Х	L
н	1	Н	н
Н	1	L	L
н	L	Х	Q ₀

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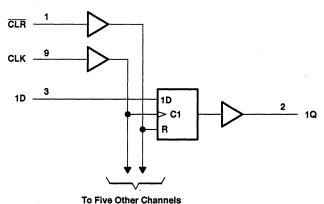
TEXAS INSTRUMENTS

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D packag	
DB packa	ge 0.55 W
PW packa	age 0.5 W
Storage temperature range	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
Vį	Input voltage		0		VCC	V
Vo	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	v _{cc} †	MIN	TYP	MAX	UNIT
Val	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	2		V
VOH	I _{OH} = -6 mA		3 V	2.4			V
Vo	I _{OL} = 100 μA		MIN to MAX			0.2	٧
VOL	I _{OL} = 6 mA		3 V			0.4	٧
lj .	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μΑ
ΔICC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} - 0.6 V,				500	μΑ
Ci	VI = VCC or GND		3.3 V		2.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX			
fclock	Clock frequency		0	24	0	19	MHz		
	Pulse duration	CLR low	20		25		no		
t _w	Pulse duration	CLK high or low	20		25		ns		
	Out a Para la face OLIG	Data	13		16		no		
^t su	Setup time before CLK↑ CLR inactive		5		5		ns		
th	Hold time, data after CLK↑	-	5		5		ns		

SN74LV174 **HEX D-TYPE FLIP-FLOP** WITH CLEAR

SCLS192 - FEBRUARY 1993 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM TO		V _{CC} = 3.3 V ± 0.3 V		0.3 V	V _{CC} = 2.7 V		UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	וואט
fmax			24	80		19		MHz
• .	CLR	0		12	26		33	no
^t pd	CLK	1		13	33	-	41	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per flip-flop	$C_L = 50 pF$,	f = 10 MHz	24	pF

SN74LV240 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS193 - FEBRUARY 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	10E 1 20 V _{CC} 1A1 2 19 20E 2Y4 3 18 1Y1 1A2 4 17 2A4 2Y3 5 16 1Y2 1A3 6 15 2A3 2Y2 7 14 1Y3
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages 	1A4 [] 8 13 [] 2A2 2Y1 [] 9 12 [] 1Y4 GND [[10 11]] 2A1

description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV240 is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74LV240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

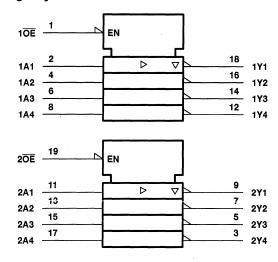
The SN74LV240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	L
L	L	н
Н	Χ	Z

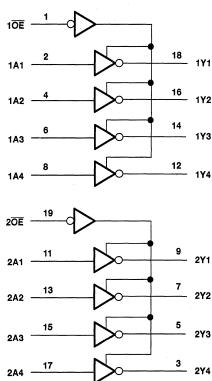
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$ ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})
Continuous current through V _{CC} or GND
Maximum power dissipation at TA = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range—65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



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recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
٧ _I	Input voltage		0		Vcc	V
٧o	Output voltage		0		Vcc	V
lон	High-level output current				-8	mA
loL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP	MAX	UNIT
Vali	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
VOH	$I_{OH} = -8 \text{ mA}$	3 V	2.4		V
Voi	I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL	I _{OL} = 8 mA	3 V		0.4	\ \ \
l _l	VI = VCC or GND	3.6 V		±1	μА
loz	VO = VCC or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μA
ΔlCC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	VI = VCC or GND	3.3 V	3		pF
Co	V _O = V _{CC} or GND	3.3 V	8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONII
t _{pd}	A	Υ .		10	21		26	ns
t _{en}	ŌĒ	Y		15	28		35	ns
^t dis	ŌĒ	Υ		17	27		33	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CO	ONDITIONS	TYP	UNIT
Cnd Power dissipation capacitance per buffer/driver		Outputs enabled	C. 50 pE	f = 10 MHz	45	nE
Cpd Power dissipation capacitance per bu	rower dissipation capacitatice per butter/driver	Outputs disabled	C _L = 50 pF, f =	T = 10 WIT12	2.5	pF

SN74LV244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS194 - FEBRUARY 1993 - REVISED MARCH 1994

•	EPIC ™	(Enhanced-Performance	Implanted
	CMOS)	2-μ Process	

- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

10E [ſ	U	20	vcc
1A1 [2		19	20E
2Y4 [3		18	1Y1
1A2 [4			2A4
2Y3 [5		16	1Y2
1A3 [6			2A3
2Y2 [] 1Y3
1A4 [8		13	2A2
2Y1 [9		12] 1Y4
GND [10		11	2A1

description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74LV244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

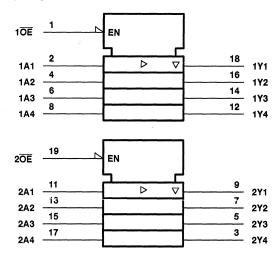
The SN74LV244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

Ì	INP	JTS	OUTPUT
	ŌĒ	Α	Y
	L	Н	Н
	L	L	L
	Н	X	Z

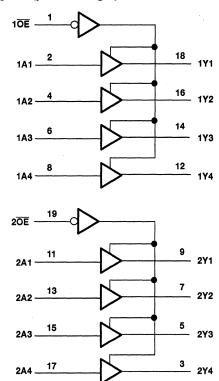
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.



recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
Vi	Input voltage		0		VCC	٧
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COMPLICANS	19 V .+		to 85°C	UNIT
PANAMEIEN	TEST CONDITIONS	vcct	MIN TY	P MAX	UNII
Val	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
VOH	$I_{OH} = -8 \text{ mA}$	3 V	2.4		V .
Va	I _{OL} = 100 μA	MIN to MAX		0.2	V
V _{OL}	IOL = 8 mA	3 V		0.4)
11	V _I = V _{CC} or GND	3.6 V		±1	μА
loz	V _O = V _{CC} or GND	3.6 V		±5	μА
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ
ΔICC	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V		3	pF
Co	VO = VCC or GND	3.3 V		8	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	ТО	V _{CC} = 3.3 V ± 0.3 V			V _{CC} =	UNIT	
PANAMETEN		(INPUT) (OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
t _{pd}	Α	Y		10	19		24	ns
t _{en}	ŌĒ	Υ		14	26		33	ns
^t dis	ŌĒ	Y		15	26		32	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CO	TYP	UNIT
C _{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	C _I = 50 pF,	f = 10 MHz	40	pF
	Power dissipation capacitance per buller/driver	Outputs disabled	CL = 50 pr,	1 = 10 IVII 12	4

SN74LV245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCLS075B - JANUARY 1991 - REVISED MARCH 1994

- EPIC ™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

	_		-	1
DIR [U	20] v _{cc}
A1 [2		19	ĪŒ
A2 [18] B1
АЗ [17	B2
A4 [16] B3
A5 [6		15] B4
A6 [7		14] B5
A7 [8		13] B6
A8 [9		12	B7
GND [10		11] B8

description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74LV245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

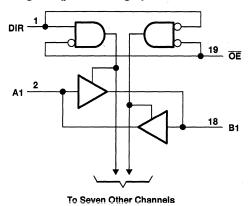
INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

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logic symbol†

ŌĒ 3EN1[BA] 3EN2[AB] 18 2∇ 17 **B2 B3** 15 **B4** 14 Α5 **B**5 13 **B6** 8 12 **B7** 11 **B8 8**A

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input voltage range, V _I (I/O ports) (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at T _A = 55°C (in still air) (see No	te 3): DB package 0.55 W
	DW package 1.6 W
	PW package 0.7 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	МОМ	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
VI	Input voltage		0		Vcc	٧
VO	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		50	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN TY	MAX	UNIT
Vou		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
VOH		I _{OH} = -8 mA	3 V	2.4		V
Vai		I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL		I _{OL} = 8 mA	3 V		0.4	V
Ц		V _I = V _{CC} or GND	3.6 V		±1	μА
loz‡		VO = VCC or GND	3.6 V		±5	μА
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	2.5	5	pF
Cio	A or B ports	VO = VCC or GND	3.3 V		7	рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
t _{pd}	A or B	B or A		8	16		20	ns
t _{en}	ŌĒ	A or B		13	23		29	ns
^t dis	ŌĒ	A or B		14	25		31	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS			UNIT
C _{pd} Power dissipation capacitance per transceiver	Outputs enabled	Cı = 50 pF.	f = 10 MHz	36	pF
	Outputs disabled	CL = 50 pr,	1 = 10 WiF12	4	þ

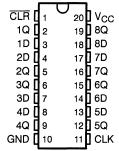
[‡] For I/O ports, the parameter IOZ includes the input leakage current.

SN74LV273 OCTAL D-TYPE FLIP-FLOP WITH CLIFAR

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- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV273 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT
CLR	CLK	D	Q
L	Х	Х	L
Н	1	Н	Н
Н	1	L	L
Н	L	Х	Q ₀

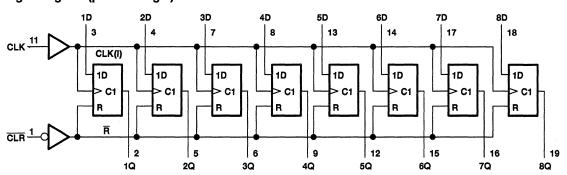
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logic symbol†

CLR CLK	1	R > C1		
1D 2D 3D 4D 5D 6D 7D 8D	3 4 7 8 13 14 17	1D	2 5 6 9 12 15 16	1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
30				Ju

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V_1 (see Note 1)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$ ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) \pm 25 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
Vį	Input voltage		0		Vcc	٧
۷o	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	့

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN	TYP MAX	UNIT	
Vou	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		\ \ \	
Voн	$I_{OH} = -6 \text{ mA}$	3 V	2.4		l '	
Vol	I _{OL} = 100 μA	MIN to MAX		0.2	V	
VOL	I _{OL} = 6 mA	3 V		0.4	l '	
lį	V _I = V _{CC} or GND	3.6 V		±1	μА	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА	
Δl _{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} = 0.0$. Other inputs at V_{CC} or GND	6 V,		500	μА	
C _i	V _I = V _{CC} or GND	3.3 V		2.5	pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX 19	
fclock	Clock frequency		0	24	0	19	MHz
A Dulas dunation	Pulse duration	CLR low	20		25		200
tw	Pulse duration	CLK high or low	20		25		ns
	0.1 - 1 - 1 - 1 - 1 - 1	Data	16		20		
t _{su}	Setup time before CLK↑	CLR inactive	5		5		ns
th	Hold time, data after CLK↑		5		5		ns

SN74LV273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то		$V_{CC} = 3.3 V \pm 0.3 V$		V _{CC} = 2.7 V		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
fmax				90		19		MHz
^t pd	CLK	Q		12	25		31	ns
t _{PHL}	CLR	Q		13	26		33	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
Cpd	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 10 MHz	32	pF

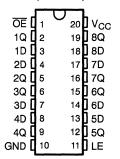
SN74LV373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS196 - FEBRUARY 1993 - REVISED MARCH 1994

 EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process

- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV373 is characterized for operation from -40°C to 85°C.

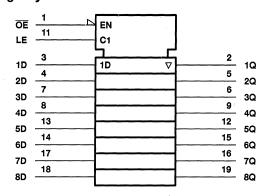
FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	Χ	Х	z

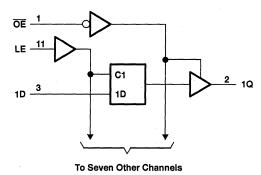
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TEXAS INSTRUMENTS

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Output voltage range, V_O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$ ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I_O ($V_O = 0$ to V_{CC})
Continuous current through V _{CC} or GND ±70 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range ——65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	٧
Vį	Input voltage		0		VCC	٧
VO	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	ŝ

NOTE 4: Unused or floating inputs must be held high or low.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT
V	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
VOH	$I_{OH} = -6 \text{ mA}$	3 V	2.4		, v
Vai	I _{OL} = 100 μA	MIN to MAX		0.2	v
VOL	IOL = 6 mA	3 V		0.4	V
Ц	VI = VCC or GND	3.6 V		±1	μА
loz	V _O = V _{CC} or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} - 0.6 \text{ V},$ Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.5		pF
Co	V _O = V _{CC} or GND	3.3 V	7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high		20		25		ns
t _{su}	Setup time, data before LE↓	High or low	10		13		ns
th	Hold time, data after LE↓	High or low	10		10		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} = 3.3 V	± 0.3 V	V _{CC} = 2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN TY	MAX	MIN MAX	Civil
	D	_	1	25	31	
^t pd	LE	ď	14	29	36	ns
t _{en}	ŌĒ	Q	18	29	36	ns
t _{dis}	ŌĒ	Q	18	29	36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST C	ONDITIONS	TYP	UNIT
C .	Outputs enabled		C _I = 50 pF,	f = 10 MHz	47	pE.
□Cpd	Power dissipation capacitance per latch	Outputs disabled	GL = 50 pr,	I = IO MINZ	29	p⊦

SN74LV374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB,	DW,	OR	PW	PΑ	CKA	GE
	- (TOP	VIE	W)		

OE [1	\bigcup_{20}] v _{cc}
1Q [2	19] 8Q
1D [3	18] 8D
2D [4	17] 7D
2Q [5	16] 7Q
3Q [6	15] 6Q
3D [7	14] 6D
4D [8	13] 5D
4Q [9	12] 5Q
GND [10	11	CLK

description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable (\overline{OE}) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV374 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	X	Q ₀
н	Х	Х	Z

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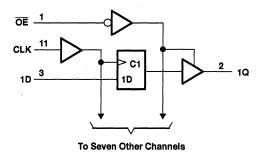


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logic symbol†

OE CLK C1 1D 1Q 1D 5 4 2Q 6 3D 3Q 8 9 4Q 4D 12 13 5Q 5D 15 14 6Q 6D 17 16 7D 7Q 19 18 8Q 8D

logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} $$ –0.5 V to 4.6 \
Input voltage range, V _I (see Note 1)
Output voltage range, V $_{ m O}$ (see Notes 1 and 2) $$
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, IO (VO = 0 to VCC)
Continuous current through V _{CC} or GND
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range—65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

SN74LV374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS197 - FEBRUARY 1993 - REVISED MARCH 1994

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
٧ _I	Input voltage		0		Vcc	V
٧o	Output voltage		0		Vcc	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δv	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP	MAX	UNIT
Vou	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
Voн	$I_{OH} = -6 \text{ mA}$	3 V	2.4		V
Voi	I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL	I _{OL} = 6 mA	3 V		0.4	٧
lj	V _I = V _{CC} or GND	3.6 V		±1	μА
loz	VO = VCC or GND	3.6 V		±5	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.5		рF
Со	$V_O = V_{CC}$ or GND	3.3 V	7		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	24	0	19	MHz
t _w	Pulse duration	CLK high or low	20		25		ns
t _{su}	Setup time before CLK↑	High or low	13		16		ns
th	Hold time, data after CLK↑		5		5		ns

SN74LV374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS197 - FEBRUARY 1993 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
f _{max}			24	75		19		MHz
^t pd	CLK	Q		14	30		38	ns
t _{en}	ŌĒ	Q		15	29		36	ns
^t dis	ŌĒ	Q		15	29		36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

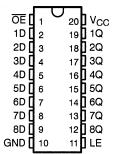
PARAMETER			TEST CO	ONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per flip-flop		Outputs enabled	C _I = 50 pF, f = 10 MHz		52	ρF
		Outputs disabled	CL = 50 pr,	pr, 1 = 10 MHz	34	Pi

SN74LV573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS198 - FEBRUARY 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV573 is characterized for operation from -40°C to 85°C.

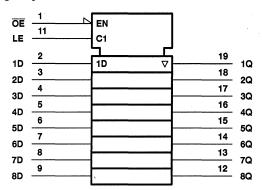
FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
OE	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	Χ	Х	Z

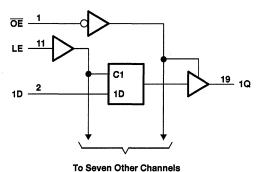
EPIC is a trademark of Texas Instruments Incorporated.

SCLS198 - FEBRUARY 1993 - REVISED MARCH 1994

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	. −0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	V to V_{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	V to V_{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
۷ _I	Input voltage		0		VCC	V
Vo	Output voltage		0		VCC	V
ЮН	High-level output current				-8	mA
loL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	v _{cc} †	MIN	TYP	MAX	UNIT
Voн	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		V
VOH	I _{OH} = -6 mA		3 V	2.4			V
Voi	I _{OL} = 100 μA		MIN to MAX			0.2 0.4 ±1	V
VOL	I _{OL} = 6 mA		3 V			0.4	V
l	$V_I = V_{CC}$ or GND		3.6 V			±1	μА
loz	$V_O = V_{CC}$ or GND		3.6 V			±5	μА
Icc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			20	μА
ΔlCC	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,				500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF
Co	VO = VCC or GND	,	3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 3.3 V ± 0.3 V		C = 3.3 V - 0.3 V V _{CC} = 2.7 V		UNIT
			MIN	MAX			
t _W	Pulse duration	LE high	20		25		ns
t _{su}	Setup time before LE↓	Data	10		13		ns
th	Hold time, data after LE↓		8		8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	то	V _{CC} = 3.3 V	± 0.3 V	V _{CC} = 2.7 V	UNIT
FANAMETER	(INPUT)	INPUT) (OUTPUT)	MIN TYP	MAX	MIN MAX	רוואט []
	D	0	11	29	36	ns
·ba	^t pd LE Q	15	30	38	1 115	
t _{en}	ŌĒ	Q	13	26	33	ns
^t dis	ŌĒ	Q	15	32	39	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

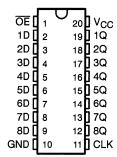
	PARAMETER		TEST C	ONDITIONS	TYP	UNIT
O . Davies discinsting association and lately	Outputs enabled	C ₁ = 50 pF, f = 10 MHz		30	pF	
Cpd	Power dissipation capacitance per latch	Outputs disabled	GE = 50 pF,	7 = 10 WH 12	14	Pi

SN74LV574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS199 - MARCH 1993 - REVISED MARCH 1994

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV574 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Χ	Q ₀
Н	Χ	Х	Z

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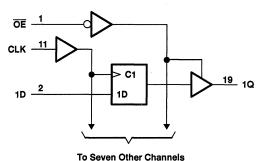
TEXAS INSTRUMENTS

SCLS199 - MARCH 1993 - REVISED MARCH 1994

logic symbol†

ŌE ΕN CLK > C1 19 1D 1D 1Q 18 2Q 2D 4 17 3D 3Q 5 16 4D 4Q 6 15 5D 5Q 7 14 6D 6Q 8 13 7D 7Q 9 12 8D 8Q

logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB pack	kage 0.6 W
DW pac	kage 1.6 W
PW pac	kage 0.7 W
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
Vį	Input voltage		0		νcc	٧
Vo	Output voltage		0		٧cc	٧
ЮН	High-level output current				-8	mA
loL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.



SN74LV574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS199 - MARCH 1993 - REVISED MARCH 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP MAX	UNIT
Vou	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	V
Voн	$I_{OH} = -8 \text{ mA}$	3 V	2.4	7
Voi	I _{OL} = 100 μA	MIN to MAX	0.2	2 V
VOL	I _{OL} = 8 mA	3 V	0.4	Π <u>΄</u>
1	VI = VCC or GND	3.6 V	±.	μА
loz	V _O = V _{CC} or GND	3.6 V	±	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20	μA
ΔICC	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		500	Αц
Ci	VI = VCC or GND	3.3 V	2.5	pF
Co	VO = VCC or GND	3.3 V	7	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			VCC =	V _{CC} = 3.3 V ± 0.3 V		3.3 V V		
			MIN MAX MIN MAX					
fclock	Clock frequency		0	24	0	19	MHz	
t _W	Pulse duration	CLK high or low	20		25		ns	
t _{su}	tsu Setup time before CLK↑ High or low		13		16		ns	
th	Hold time, data after CLK↑		5		5		ns	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM	FROM TO (OUTPUT)	Vcc=	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)		MIN	TYP	MAX	MIN	MAX	UNII
fmax			24	70		19		MHz
t _{pd}	CLK	Q		14	30		38	ns
t _{en}	ŌĒ	Q		13	27		34	ns
^t dis	ŌĒ	Q		15	29		36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT	
<u> </u>	Power dissipation capacitance per flip-flop	Outputs enabled	C ₁ = 50 pF.	f = 10 MHz	40	pF
Cpd	rower dissipation capacitance per hip-hop	Outputs disabled	OL = 50 pr,	1 = 10 101112	22	рі

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CBT BUS SWITCHES AND 5-V/3-V TRANSLATORS

Features

- Low propagation delay 5-V to 3-V translation
- Near-zero propagation delay
- Low $(4 \Omega 6 \Omega)$ on resistance (r_{on})
- Reduced (6 pF–8 pF) input capacitance (C_i)
- SOIC, EIAJ SSOP, and TSSOP packaging

Benefits

- Isolates 3.3-V components from 5-V signals
- Facilitates high-performance bus connections and exchanges
- Minimizes bus parasitics
- Easily configurated for mixed mode applications (see application note, section 12)
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

SN74CBT3244 8-BIT CROSSBAR SWITCH

SCDS001A - NOVEMBER 1992 - REVISED MARCH 1994

11 2A1

•	Functionally	Equivalent to	QS3244
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- Standard '244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

20 VCC 10E 1A1 🛛 2 19 1 2 OE 18[] 1Y1 2Y4 **3** 1A2 🛮 4 17 2A4 16 1Y2 2Y3 🛮 5 1A3 🛮 6 15 2A3 14 1 1Y3 2Y2 🛮 7 13 2A2 1A4 🛮 8 2Y1 **[]** 9 12 1 1Y4

GND 10

DB, DW, OR PW PACKAGE (TOP VIEW)

description

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on resistance of the switch allows connections to be made with minimal propagation delay.

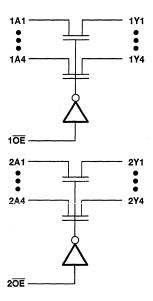
The device is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port Y, or visa versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3244 is characterized for operation from 0°C to 70 °C.

FUNCTION TABLE

INP	UTS	INPUT/OUTPUTS		
10E	2OE	1A,1Y	2A, 2Y	
L	L	1A= 1Y	2A = 2Y	
L	Н	1A=1Y	Z	
Н	L	z	2A = 2Y	
Н	Н	z	Z	

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to 6 V
Continuous channel current	128 mA
Clamp current, $I_K(V_{I/O} < 0)$	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2	
	DW package 1.6 W
	PW package 0.7 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
VCC	Supply voltage	4.75	5.25	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	0	70	°C



^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	ONS	MIN	TYPT	MAX	UNIT	
٧ _{IK}		$V_{CC} = 4.75 V$,	lj = –18 mA				-1.2	٧
1		$V_{CC} = 5.25 \text{ V},$	V _I = 5.25 V to GND				±5	μΑ
los		$V_{CC} = 4.75 V$,	$V_{I(A)} = 0$,	V _{I(Y)} = 4.75 V		250		mA
Icc		$V_{CC} = 5.25 \text{ V},$	l _O = 0,	V _I = V _{CC} or GND			50	μА
∆lcc [‡]	Control pins	$V_{CC} = 5.25 \text{ V},$	One input at 3.4 V,	Other inputs at VCC or GND			3.5	mA
Ci	Control pins	V _I = 3 V or 0				3		pF
C _{io(OFF}	=)	$V_0 = 3 \text{ V or } 0,$	OE = VCC			6		pF
			V ₁ = 0,	lj = 64 mA		5	7	
r _{on} §		V _{CC} = 4.75 V	V ₁ = 0,	lį = 30 mA		5	7	Ω
			$V_1 = 2.4 V$	lj = 15 mA		10	15	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pd} ¶				0.25	ns
t _{en}	ŌĒ	A or Y	1	8.9	ns
^t dis	ŌĒ	A or Y	1	7.4	ns

This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

[§] Measured by the voltage drop between the A and the Y pins at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or Y) pins.

SCDS002A - NOVEMBER 1992 - REVISED MARCH 1994

- Functionally Equivalent to QS3245Standard '245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

	•		•	
0E [1	U	20	v _{cc}
A1 [2		19	OE.
A2 🛭	3		18] B1
АЗ [17] B2
A4 🛭	5		16] B3
A5 [6		15] B4
A6 [7		14	B 5
A7 [13] B6
A8 [9		12] B7
GND [10		11	1 B8

DB, DW, OR PW PACKAGE (TOP VIEW)

description

The SN74CBT3245 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on resistance of the switch allows connections to be made without adding propagation delay.

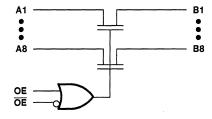
The device is organized as one 8-bit switch bank with dual output-enable (OE and \overline{OE}) inputs. When \overline{OE} is low or OE is high, the switch is on and port A is connected to port B. When \overline{OE} is high and OE is low, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

	INP	UTS	INPUT/ OUTPUTS
	OE OE		A, B
	Х	L	A = B
	. Н	X	A = B
١	L	Н	Z

logic diagram



SCDS002A - NOVEMBER 1992 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Continuous channel current	
Input clamp current, I _{IK} (V _{I/O} < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DB	package 0.6 W
	/ package 1.6 W
PW	/ package 0.7 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.25	V
VIH	High-level control input voltage	2		٧
V _{IL}	Low-level control input voltage		0.8	٧
TA	Operating free-air temperature	0	- 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION	SNC	MIN	TYP‡	MAX	UNIT
VIK		V _{CC} = 4.75 V,	l _l = –18 mA				-1.2	٧
11		$V_{CC} = 5.25 \text{ V},$	V _I = 5.25 V or GND				±5	μА
los		V _{CC} = 4.75 V,	$V_{I(A)} = 0$,	V _{I(B)} = 4.75 V		250		mA
Icc		V _{CC} = 5.25 V,	IO = 0,	VI = VCC or GND			50	μА
ΔICC§	Control pins	V _{CC} = 5.25 V,	One input at 3.4 V,	Other inputs at VCC or GND			3.5	mA
Ci	Control pins	V _I = 3 V or 0				3		pF
C _{io(OFF}	-)	$V_O = 3 \text{ V or } 0,$	OE = V _{CC}			6		рF
			V _I = 0,	i _l = 64 mA		5	7	
ron¶		V _{CC} = 4.75 V	V _I = 0,	l _j = 30 mA		5	7	Ω
			V _I = 2.4 V,	l _l = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.



^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	דואט
t _{pd} †	A or B	B or A		0.25	ns
^t en	OE or OE	A or B	1	9.1	ns
^t dis	OE or OE	A or B	1	8.7	ns

[†] This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

SN74CBT3383 10-BIT BUS-EXCHANGE SWITCH

SCDS003A - NOVEMBER 1992 - REVISED MARCH 1994

 Functionally Equivalent to QS3383 and QS3L383 	DB, DW, OR PW PACKAGE (TOP VIEW)
 5-Ω Switch Connection Between Two Ports 	BE (1 24) V _{CC}
 TTL-Compatible Input and Output Levels 	C1 2 23 D5
Package Options Include Plastic	A1 🛛 3 22 🕽 B5
Small-Outline (DW), Shrink Small-Outline	B1 [] 4 21 [] A5
(DB), and Thin Shrink Small-Outline (PW)	D1 🛛 5 20 🖟 C5
Packages	C2 [] 6 19 [] D4
	A2 🛛 7 18 🕽 B4
description	B2 [] 8 17 [] A4
The SN74CBT3383 provides ten bits of	D2 [] 9 16 [] C4
high-speed TTL-compatible bus switching or	C3 🛛 10 15 🗍 D3
exchanging. The low on resistance of the switch	A3 🛛 11 14 🗍 B3
allows connections to be made without adding	GND [12 13 BX

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the AB and CD pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when BE is low.

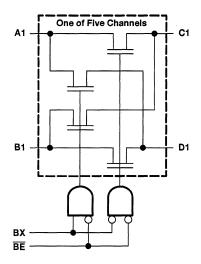
The SN74CBT3383 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

BE	вх	A1-A5	B1-B5
L	L	C1-C5	D1-D5
L	Н	D1 - D5	C1 -C5
Н	Х	Z	Z

logic diagram

propagation delay.





SN74CBT3383 10-BIT BUS-EXCHANGE SWITCH

SCDS003A - NOVEMBER 1992 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to	17 V
Input voltage range, V _I (see Note 1)	–0.5 V to) 6 V
Continuous channel current		3 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)) mA
Maximum power dissipation at T _A = 55° (in still air) (see Note 2)		
, , , , , , , , , , , , , , , , , , , ,	DW package 1.	.6 W
	PW package 0	.7 W
Storage temperature range		50°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
Vcc	Supply voltage	4.75	5.25	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	AMETER TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
VIK		$V_{CC} = 4.75 \text{ V},$	l _l ≈ −18 mA				-1.2	٧
ΙĮ		$V_{CC} = 5.25 \text{ V},$	V _I = 5.25 V or GND				±5	μА
los		V _{CC} ≈ 4.75 V,	$V_{I(A)} = 0,$	V _{I(B)} = 4.75 V		250		mA
Icc		$V_{CC} = 5.25 \text{ V},$	l _O = 0,	VI = VCC or GND			50	μА
ΔICC§	Control pins	$V_{CC} = 5.25 \text{ V},$	One input at 3.4 V,	Other inputs at VCC or GND	1		2.5	mA
Ci	Control pins	V _I = 3 V or 0				3		pF
C _{io(OFF}	-)	$V_O = 3 \text{ V or } 0,$	OE = V _{CC}			6		pF
		$V_{CC} = 4.75 \text{ V},$	V ₁ = 0,	lj = 64 mA		5	7	
ron¶		$V_{CC} = 4.75 \text{ V},$	V _I = 0,	I _I = 30 mA		5	7	Ω
		$V_{CC} = 4.75 \text{ V},$	V _I = 2.4 V,	lj ≈ 15 mA		10	15	

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

Measured by the voltage drop between the A and the B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

SN74CBT3383 10-BIT BUS-EXCHANGE SWITCH

SCDS003A - NOVEMBER 1992 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pd} †				0.25	ns
t _{BX}	BX	A, B, C, or D	1	9.2	ns
t _{en}	BE	A or B	1	8.6	ns
^t dis	BE	A or B	1	7.5	ns

[†] This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical On resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

SN74CBT3384 10-BIT CROSSBAR SWITCH

SCDS004A - NOVEMBER 1992 - REVISED APRIL 1994

 Functionally Equivalent to QS3384 and QS3L384 	DB, DW, OR PW PACKAGE (TOP VIEW)
 5-Ω Switch Connection Between Two Ports 	OE1 1 24 VCC
 TTL-Compatible Input and Output Levels 	B1 [] 2 23 [] B10
Package Options Include Plastic	A1 🚺 3 22 🗍 A10
Small-Outline (DW), Shrink Small-Outline	A2 🛛 4 21 🗍 A9
(DB), and Thin Shrink Small-Outline (PW)	B2 🛛 5 20 🗍 B9
Packages	B3 [] 6 19 [] B8
	A3 🛛 7 18 🖸 A8
description	A4 🛛 8 17 🖺 A7
The SN74CBT3384 provides ten bits of	B4 🛛 9 16 🖸 B7
high-speed TTL-compatible bus switching. The	B5 🛛 10 15 🖺 B6
low on resistance of the switch allows connections	A5 🛛 11 14 🖺 A6
to be made without adding propagation delay.	GND 12 13 OE2

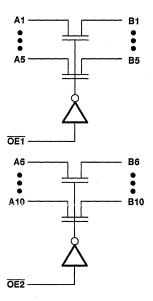
The device is organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3384 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OE1	OE2	B1 – B5	B6-B10
L	L	A1 – A5	A6-A10
L	н	A1 – A5	Z
Н	L	Z	A6-A10
Н	Н	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
input voltage range, V _I (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _{I/O} < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): D	B package 0.6 W
	W package 1.6 W
P	W package 0.7 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
VCC	Supply voltage	4.75	5.25	٧
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	٧
TA	Operating free-air temperature	0	70	°C



SCDS004A - NOVEMBER 1992 - REVISED APRIL 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYPT	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	i _l = –18 mA				-1.2	٧
l _l		V _{CC} = 5.25 V,	V _I = 5.25 V or GND				±5	μА
los		V _{CC} = 4.75 V,	$V_{I(A)} = 0$,	V _{I(B)} = 4.75 V		250		mA
lcc		V _{CC} = 5.5 V,	lO = 0,	V _I = V _{CC} or GND			50	μА
ΔICC [‡]	Control pins	$V_{CC} = 5.25 \text{ V},$	One input at 3.4 V,	Other inputs at VCC or GND			2.5	mA
Ci	Control pins	V _I = 3 V or 0				3		pF
Cio(OFF)		$V_O = 3 \text{ V or } 0,$	OE = V _{CC}			6		pF
r _{on} §		V _{CC} = 4.75 V	V _I = 0,	I _I = 64 mA		5	7	Ω
			V ₁ = 0,	I _I = 30 mA		5	7	
			V _I = 2.4 V,	l _j = 15 mA		10	15	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
^t pd [¶]	A or B	B or A		0.25	ns
t _{en}	ŌĒ	A or B	1	8.5	ns
^t dis	ŌĒ	A or B	1	8.5	ns

This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

[§] Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

SN74CBT6800 10-BIT CROSSBAR SWITCH WITH PRECHARGED OUTPUTS FOR LIVE INSERTION

SCDS005A - MARCH 1993 - REVISED MARCH 1994

- 5-Ω Switch Connection Between Two Ports
- Near-Zero Propagation Delay
- TTL-Compatible Input and Output Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages

description

The SN74CBT6800 provides ten bits of highspeed TTL-compatible bus switches. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

DW OR PW PACKAGE (TOP VIEW)

			1
ON (11	O 24	D v _{cc}
A1 [] 2	23] B1
A2	3	22] B2
АЗ [4	21	B 3
A4	5	20] B4
A5 [6	19] B5
A6 [7	18] B6
A7 [8	17] B7
A8	9	16] B8
A9 [] 10	15] B9
A10] 11	14	B10
GND [12	13	🛚 BIASV

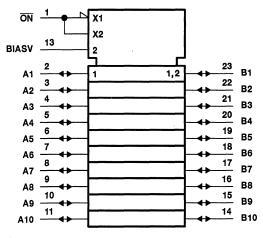
The SN74CBT6800 is organized as one 10-bit switch bank with a single enable (\overline{ON}) input. When \overline{ON} is low, the switch is on and port A is connected to port B. When \overline{ON} is high, the switch between port A and port B is open and the B port is precharged to the BIASV voltage through the equivalent of a 10-k Ω resistor.

The SN74CBT6800 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

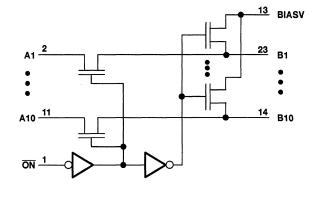
	ON	B1-B10	FUNCTION
i	L	A1-A10	Connect
	Н	BIASV	Precharge

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



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SN74CBT6800 10-BIT CROSSBAR SWITCH WITH PRECHARGED OUTPUTS FOR LIVE INSERTION

SCDS005A - MARCH 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Bias voltage range, BIASV	0.5 V to 6 V
Input voltage range, V _I (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Current into any pin, IO	128 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 2): DW package	1.7 W
PW package	0.7 W
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	٧
BIASV	Supply voltage	0	Vcc	V
VIH	High-level input voltage	2		٧
VIL	Low-level input voltage		0.8	V
TA	Operating free-air temperature	-40	85	ů

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
VIK	V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	٧
1.	$V_{CC} = 0$,	V _I = 5.5 V				10	
11	$V_{CC} = 5.5 \text{ V},$	V _I = 5.5 V or GND				±1	μA
Ю	V _{CC} = 4.5 V,	BIASV = 2.4 V,	V _O = 0	0.25			mA
los	V _{CC} = 4.5 V,	$V_{I(A)} = 0$,	V _{I(B)} = 4.5 V	100			mA
ICC	V _{CC} = 5.5 V,	I _O = 0,	VI = VCC or GND			1	mA
ΔICC§	$V_{CC} = 3.6 \text{ V},$	One input at 2.7 V,	Other inputs at VCC or GND			0.2	mA
C _i Control pins	V _I ≈ 3 V or 0				4		pF
C _{o(ON)}	$V_0 = 3 \text{ V or } 0,$	Switch on			8		рF
C _{o(OFF)}	V _O = 3 V or 0,	Switch off			6		pF
-	V 45V	V _I = 0,	l _l = 64 mA			6	Ω
ron [¶]	VCC = 4.5 V	V _I = 2.4 V,	l _l = 15 mA			12	22
10	V _{CC} = 4.5 V,	BIASV = 2.4 V,	V _O = 0	0.25			mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance (ron) is determined by the lower of the voltages of the two (A or B) pins.

SN74CBT6800 **10-BIT CROSSBAR SWITCH** WITH PRECHARGED OUTPUTS FOR LIVE INSERTION

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = -40°C to 85°C	T _A = 0°C to 70°C		UNIT
			MIN MAX	MIN	MAX	
t _{PLH} †	A or B	B or A			0.25	ns
t _{PHL} †					0.25	
tPZH [‡]	ŌN	A or B		1.5	7.5	ns
tpZL§				1.5	7.5	115
t _{PHZ} ‡	ŌN	A or B		1.5	6.5	ns
tpLZ§	- ON			1.5	6.5	110

This parameter is characterized but not tested. This propagation delay is due to the RC time constant of the on-state resistance of the switch and the load capacitance.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



[‡]BIASV = GND \$BIASV = 3 V

SN74CBT16209 18-BIT BUS-EXCHANGE SWITCH

SCDS006A - NOVEMBER 1992 - REVISED MARCH 1994

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74CBT16209 provides 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device operates as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) pins.

The SN74CBT16209 is characterized for operation from -40°C to 85°C.

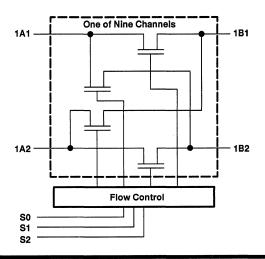
FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	Н	B1	z	A1 to B1
L	Н	L	B2	Z	A1 to B2
L	Н	Н	z	B1	A2 to B1
Н	L	L	z	B2	A2 to B2
Н	L	Н	z	Z	Disconnect
Н	Н	L	B1	B2	A1 to B1, A2 to B2
н	Н	н	B2	B1	A1 to B2, A2 to B1

DGG OR DL PACKAGE (TOP VIEW)

	1	U		
S0 []1		48] S1
1A1 [2		47] S2
1A2 [46] 1B1
GND [4		45	1B2
2A1 [5		44	2B1
2A2 [6		43	2B2
Vcc [17		42] GND
3A1 [8		41	3B1
3A2	9		40	3B2
GND [10		39	GND
4A1 [11		38	4B1
4A2 [12		37	4B2
5A1 [13		36	5B1
5A2 [14		35	5B2
GND [15		34	GND
6A1 [16		33] 6B1
6A2 [17		32] 6B2
7A1 [18		31] 7B1
7A2 [19		30	7B2
GND [20		29	GND
8A1 [21		28] 8B1
8A2 [22		27	8B2
9A1 [23		26	9B1
9A2 [24		25	9B2

logic diagram



PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



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SN74CBT16209 18-BIT BUS-EXCHANGE SWITCH

SCDS006A - NOVEMBER 1992 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V	to 7 V
Input voltage range, V _I (see Note 1)	to 6 V
Current into any pin, Io	
Input clamp current, $I_{ K }(V_1 < 0)$	50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 2): DGG package).85 W
DL package	1.2 W
Storage temperature range –65°C to	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	ν
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	٧
TA	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	l _l = –18 mA				-1.2	٧
1.		$V_{CC} = 0$,	V _I = 5.5 V				10	
1		V _{CC} = 5.5 V,	V _I = 5.5 V or GND				±1	μА
los		V _{CC} = 4.5 V,	$V_{i}(A) = 0,$	V _I (B) = 4.5 V	100			mA
I _{CC} §		V _{CC} = 5.5 V,	l _O = 0,	VI = VCC or GND			100	μА
ΔlCC		V _{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V _{CC} or GND			0.2	mA
Ci	Control pins	V _I = 3 V or 0				4		рF
C _{io(ON)}		$V_{O} = 3 \text{ V or } 0,$	OE = GND			8		pF
C _{io(OFF}	;)	$V_O = 3 \text{ V or } 0,$	OE = VCC			6		pF
ron¶		V _{CC} = 4.5 V	V _I = 0,	lj = 64 mA			6	Ω
		VCC = 4.5 V	V _I = 2.4 V,	i _I = 15 mA			12	32

All typical values are at V_{CC} = 5 V, T_A = 25°C.

\$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.



The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

SCDS006A - NOVEMBER 1992 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM	TO	T _A = -40 to 85°C		T _A = 0° to 70°C		UNIT
	(INPUT)	(OUTPUT)	MIN N	XAN	MIN	MAX	
t _{PLH} †	A or B	B or A			_	0.25	
t _{PHL} †		BOLA				0.25	ns
t _{PLH}	S0, S1, S2	A or B			1.5	7.5	ns
tPHL		A 01 B			1.5	7.5	115
^t PZH	S0, S1, S2	A or B			1.5	7.5	ns
^t PZL	50, 51, 52				1.5	7.5	110
t _{PHZ}	S0, S1, S2	A or B			1.5	6.5	ne
^t PLZ	30, 31, 32	AOFB			1.5	6.5	ns

[†] This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



SN74CBT16212 **24-BIT BUS-EXCHANGE SWITCH**

SCDS007A - NOVEMBER 1992 - REVISED MARCH 1994

55 S2

DGG OR DL PACKAGE (TOP VIEW)

1A1 🛮 2

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0-S2) pins.

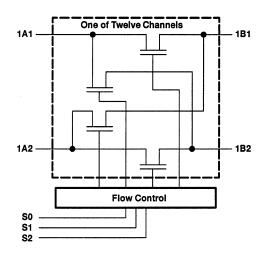
The SN74CBT16212 is characterized operation from -40°C to 85°C.

FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	Н	B1	z	A1 to B1
L	н	L	B2	Z	A1 to B2
L	Н	Н	Z	B1	A2 to B1
Н	L	L	z	B2	A2 to B2
Н	L	Н	Z	Z	Disconnect
н	н	L	B1	B2	A1 to B1, A2 to B2
н	н	н	B2	B1	A1 to B2, A2 to B1

1A2]з	54] 1B1
2A1	4] 1B2
2A2 [5		2B1
3A1 [51	2B2
3A2 [7	50	3B1
GND[8	49	GND
4A1 [9	48]3B2
4A2 [] 4B1
5A1 [11	46] 4B2
5A2 [12	45]5B1
6A1 [13	44]5B2
6A2 [14	43] 6B1
7A1 [15	42] 6B2
7A2 []7B1
v _{cc} [17	40]7B2
8A1 [18	39	8B1
GND [19	38	GND
8A2 [20	37] 8B2
9A1 [21	36]9B1
9A2 [22	35] 9B2
10A1 [23	34] 10B1
10A2	24	33] 10B2
11A1 [32] 11B1
11A2 [] 11B2
12A1 [27	30] 12B1
12A2 [28	29] 12B2

logic diagram



INSTRUMENTS

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SN74CBT16212 24-BIT BUS-EXCHANGE SWITCH

SCDS007A - NOVEMBER 1992 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Current into any pin, IO	
Input clamp current, I _{IK} (V _I < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note	
	 1.4 W
Storage temperature range	 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
Vcc	Supply voltage	4	5.5	V
VIH	High-level input voltage	2		,V
VIL	Low-level input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK	V _{CC} = 4.5 V,	lj = -18 mA				-1.2	٧
I.	$V_{CC} = 0$,	V _I = 5.5 V				10	
Ц	$V_{CC} = 5.5 \text{ V},$	V _I = 5.5 V or GND	V _I = 5.5 V or GND			±1	μА
los	V _{CC} = 4.5 V,	$V_{ }(A) = 0,$	V _I (B) = 4.5 V	100			mΑ
I _{CC} §	V _{CC} = 5.5 V,	l _O = 0,	VI = VCC or GND			100	μА
ΔICC	V _{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at VCC or GND			0.2	mΑ
C _i Control pins	V _I = 3 V or 0				4		pF
C _{io(ON)}	$V_{O} = 3 \text{ V or } 0,$	OE = GND			8		pF
C _{io(OFF)}	$V_{O} = 3 \text{ V or } 0,$	OE = VCC			6		pF
ron¶	V00 - 45 V	V _I = 0,	lj = 64 mA			6	Ω
on "	V _{CC} = 4.5 V	V _I = 2.4 V,	l _l = 15 mA			12	52

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note.

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

SN74CBT16212 24-BIT BUS-EXCHANGE SWITCH

SCDS007A - NOVEMBER 1992 - REVISED MARCH 1994

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		T _A = -40° to 85°C		T _A = 0° to 70°C	
	(114701)	(001701)	MIN	MAX	MIN	MAX	
t _{PLH} †	A or B	B or A				0.25	
t _{PHL} †	AOIB	BOLA				0.25	ns
^t PLH	S0, S1, S2	A or B			1.5	7.5	
^t PHL	30, 31, 32	A OI B			1.5	7.5	ns
^t PZH	S0, S1, S2	A or B			1.5	7.5	ns
tPZL	30, 31, 32	AOIB			1.5	7.5	113
^t PHZ	S0, S1, S2	A or B			1.5	6.5	ns
tPLZ	30, 31, 32	7010			1.5	6.5	110

[†] This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



SN74CBT16214 3-TO-1 BUS-SELECT SWITCH

SCDS008 - MAY 1993 - REVISED MARCH 1994

- 5-Ω Switch Connection Between Two Ports
- Zero Propagation Delay
- TTL-Compatible Input and Output Levels
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

The SN74CBT16214 provide 12 bits of highspeed TTL-compatible bus switching between three separate ports. The low on resistance of the switch allows connections to be made without adding propagation delay.

The SN74CBT16214 operates as a 12-bit bus switch via the data-select (S0-S2) pins.

The SN74CBT16214 is characterized for operation from –40°C to 85°C.

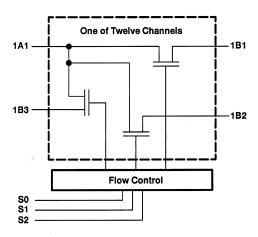
FUNCTION TABLE

S2	S1	S0	A1	FUNCTION
L	L	L	Z	Disconnect
L	L	Н	B1	A1 to B1
L	Н	L	B2	A1 to B2
L	н	Н	z	Disconnect
Н	L	L	Z	Disconnect
Н	L	Н	В3	A1 to B3
Н	н	L	B1	A1 to B1
Н	Н	Н	B2	A1 to B2

DGG OR DL PACKAGE (TOP VIEW)

S0[1	U]S1
1A1[56] S2
1B3			55	1B1
2A1			54	1B2
2B3			50	2B1
3A1 [51	2B2
3B3[50	3B1
GND [49	GND
4A1 [48	3B2
4B3	10		47	4B1
5A1 [11] 4B2
5B3[12			5B1
6A1[13		44	5B2
6B3[14			6B1
7A1[42	6B2
7B3[16]7B1
v_{CC} [17		40]7B2
8A1 [18			8B1
GND [19			[]GND
8B3 [8B2
9A1 [21			9B1
9В3 🛚	22			9B2
0A1 [23] 10B1
овз [24			10B2
11A1 🛚				11B1
11B3 [26			11B2
2A1 [12B1
2B3 L	28		29] 12B2

logic diagram





SCDS008 - MAY 1993 - REVISED MARCH 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to 6 V
Current into any pin, IO	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DGG package	1 W
DL package	1.4 W
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	٧
VIH	High-level input voltage	2		٧
VIL	Low-level input voltage		0.8	٧
TA	Operating free-air temperature	-40	85	ô

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TYP‡	MAX	UNIT
VIK	V _{CC} = 4.5 V,	l _l = –18 mA				-1.2	٧
ı.	$V_{CC} = 0$,	V _I = 5.5 V				10	
1	V _{CC} = 5.5 V,	V _I = 5.5 V or GND				±1	μА
los	V _{CC} = 4.5 V,	$V_{I}(A) = 0,$	V _I (B) = 4.5 V	100			mA
lcc	V _{CC} = 5.5 V,	I _O = 0,	VI = VCC or GND			100	μÄ
ΔICC§	V _{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V _{CC} or GND			0.2	mA
C _i Control pins	V _I = 3 V or 0				4		pF
Cio(ON)	$V_{O} = 3 \text{ V or } 0,$	OE = GND			10		рF
C _{io(OFF)}	V _O = 3 V or 0,	OE = V _{CC}			6		рF
. 1	V 45V	V _I = 0,	$V_{\parallel} = 0$, $I_{\parallel} = 48 \text{ mA}$			6	Ω
ron [¶]	V _{CC} = 4.5 V	V _I = 2.4 V,	lj = 15 mA		-	12	5.2

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

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Mixing It Up With 3.3 Volts

Ken Ristow Steve Perna Advanced System Logic – Semiconductor Group



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Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others will offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of $1.2 \, \mu m$, and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3-V operation.

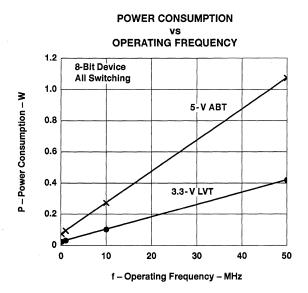


Figure 1. 3-V to 5-V Power vs Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as laptop computers, automotive and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups which can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged but the spread actually runs from about 3.3 V up to 3.9 V. For now the unregulated battery market demands low-voltage products which are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices will slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V, with volume requirements not beginning until the '94-'95 time frame. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC} . This limits input voltages to $V_{CC} + 0.5$ V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices which support this mode must be designed for maximum input voltages of 5.5 V without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL} , which are ratios of V_{CC} . Low-voltage TTL (LVTTL) utilizes the standard-TTL input levels of 0.8 and 2 V as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

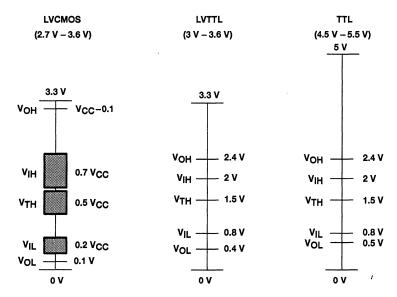


Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices, and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7- to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of: $V_{OH} = 2 \text{ V}$ at $I_{OH} = -32 \text{ mA}$ $V_{OL} = 0.55 \text{ V}$ at $I_{OL} = 64 \text{ mA}$

Rail-to-rail switching for driving CMOS

Maximum supply currents of:

 $I_{CC(L)} = 15 \text{ mA}$ $I_{CC(H)} = 250 \text{ }\mu\text{A}$ $I_{CC(Z)} = 250 \text{ }\mu\text{A}$

Propagation delays of: $t_{pd} < 4.6 \text{ ns}$ t_{pd} (LE to Q) < 5.1 ns t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages: 48- and 56-pin SSOP for LVT Widebus™
20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with $V_{CC} = 2.7$ to 3.6 V, the inputs can withstand 5.5 V even when $V_{CC} = 0$ V. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

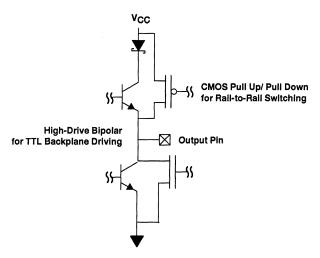


Figure 3. Simplified LVT Output Structure

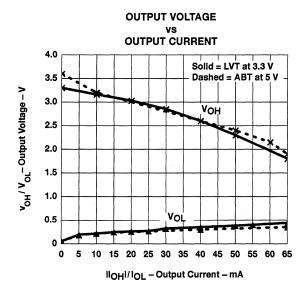


Figure 4. ABT vs LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, $\pm 100~\mu$ A, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately $\pm 500~\mu$ A, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load, and does not affect the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.

Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

Mark McClear Advanced System Logic – Semiconductor Group



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Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

- 1. Split-rail or dual 3.3-V and 5-V V_{CC} devices.
- 2. Completely 5-V tolerant, pure 3.3-V V_{CC} components.

This paper deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and data-path voltage translators, but the following precautions are usually recommended:

- Dual-V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even
 damage to the parts in the event that one V_{CC} rail ramps faster than the other. These stringent requirements
 are often difficult to meet from a system timing standpoint, and offer little flexibility for partial system power
 down or other advanced power-saving design techniques.
- Simply because the part has a 5-V V_{CC} pin does not necessarily guarantee that the part will actually switch
 all the way to the 5-V rail. Switching all the way to 5 V is one way to reduce the power consumption in 5-V
 memories or other pure 5-V CMOS circuits which are driven by a level-shifter device (this paper will
 demonstrate others as well).

A quick check of the data sheet for the product in question will reveal if the part drives all the way to the 5-V rail. If the output high voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs will typically drive only to around 3.6 V.

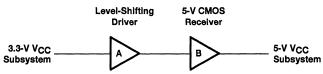
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices mentioned above. From a single V_{CC} source they avoid the power-sequencing problems of the split rails, and are also offered in a number of functions, bit widths, and storage options. The one potential drawback of the single- V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail . . . but is this really a drawback?

The Misconception About ∆I_{CC}

The component selection of a level shifter impacts two major aspects of total system power dissipation:

- The impact that the V_{OH} level of the driving part (A in Figure 1) has on the power dissipation of the receiving device (B in Figure 1), commonly known as ΔI_{CC}, and
- 2. The power of the device itself.



Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

 ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B in Figure 1) due to the V_{OH} level of the driving device (A in Figure 1). Put another way, one would correctly expect that a TTL-compatible 5-V CMOS product would have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from zero to V_{CC} .

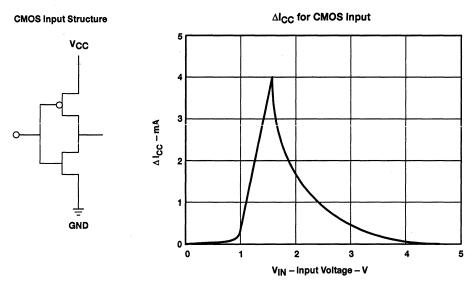


Figure 2. Basic CMOS Input Structure and Typical ∆I_{CC} Current

Note that as expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V.

Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

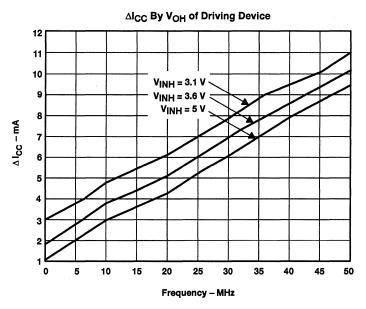


Figure 3. △I_{CC} – 16-Bit Device

Here we see that ΔI_{CC} is in fact 2 to 3 mA higher for the case where V_{OH} is only 3.1 V than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might be tempted to conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the system power impact of the driving device.

Figure 4 shows the V_{OH} of two devices; the FCT164245 split-rail device from Integrated Device Technologies, and the LVT16245A from Texas Instruments.

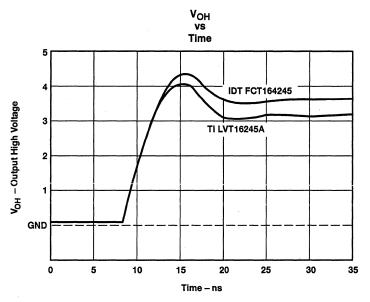


Figure 4. VOH of FCT164245 and 'LVT16245A

From the above, you would correctly conclude that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total system power dissipation that selection of a level-shifter device has from system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI LVT16245A, and the worst-case ΔI_{CC} (V_{OH} = 3.1 V) graphed on the same vertical scale.

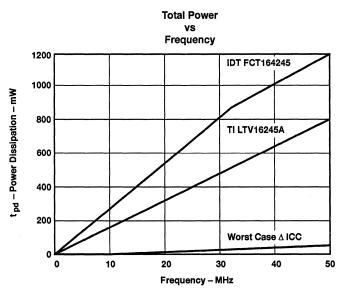


Figure 5. Total System Power Dissipation Impact

From this we can see that even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} will be more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's Low-Voltage Technology (LVT) product line mentioned above offer a parametric specification call I_{OFF} , which guarantees that the output pins of the parts will remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT part from dragging down the bus of an active part in the system, and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating (and causing damage to the devices on the bus). Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the TVT16245A (and others) from TI have a circuit feature called a *bus-hold cell* (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and, of course, power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

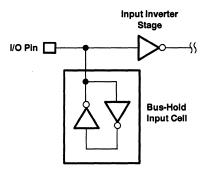


Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Texas Instruments Crossbar Switches (CBT)

Ramzi Ammar Advanced System Logic – Semiconductor Group



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What Are Texas Instruments Crossbar Switches (CBT)?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an N-channel MOS transistor driven by a CMOS gate. When enabled, the N-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on resistance of approximately $5\,\Omega$ and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at $\approx 1\,V$ less than the gate potential regardless of the level at the input pin. This is one of the N-channel transistor characteristics (see Figures 1 and 2). Note the $\approx 1\,V$ difference between the gate (V_{CC}) and the source (V_{O}) at any point on the graph.

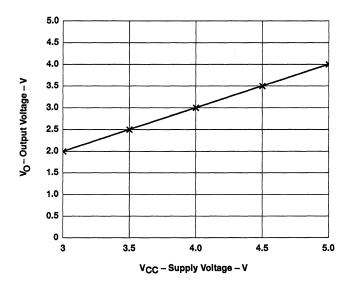


Figure 1. Output Voltage vs Supply Voltage

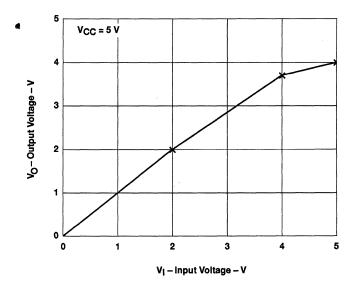


Figure 2. Output Voltage vs Input Voltage

The on-state resistance r_{on} increases gradually with V_I until V_I approaches $V_{CC}-1$ V, where r_{on} rapidly increases clamping V_O at $V_{CC}-1$ V (see Figure 3). Also, by the nature of the N-channel transistor design, the input and output pins are fully isolated when the transistor is off. Leakage and capacitance is to ground and not between input and output which minimizes feedthrough when the transistor is off.

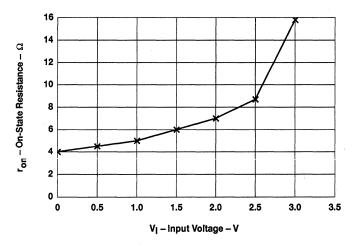
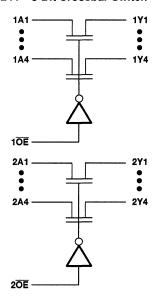


Figure 3. On-State Resistance vs Input Voltage

What Does Texas Instruments Offer in the CBT Family?

The following CBT switches offered by Texas Instruments are shown in this application report. This helps designers understand and identify areas where these devices are useful.

SN74CBT3244 - 8-Bit Crossbar Switch

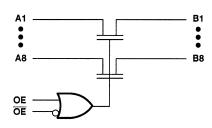


DB, DW, OR PW PACKAGE (TOP VIEW) 20 VCC 10E [19 20E 1A1 🗓 18 1Y1 2Y4 🛛 3 17 2A4 1A2 🛮 4 16]] 1Y2 2Y3 🛛 5 15 2A3 1A3 🛮 6 2Y2 🛛 7 14 1 1Y3 13 2A2 1A4 🛮 8 2Y1 **1**9 12 1Y4 GND [10 11 2A1

FUNCTION TABLE

INP	UTS	INPUT/C	UTPUTS
1OE	2OE	1A,1Y	2A, 2Y
L	L	1A= 1Y	2A = 2Y
L	Н	1A=1Y	Z
Н	L	z	2A = 2Y
Н	Н	z	Z

SN74CBT3245 - 8-Bit Crossbar Switch



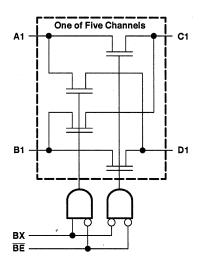
DB, DW, OR PW PACKAGE (TOP VIEW)

OE	1	U	20	v _{cc}
A1 [2		19] Œ
A2 🛚	3		18	B1
АЗ 🛚	4		17] B2
A4 🛚	5		16] B3
A5 🛚	6		15] B4
A6 🛚	7		14] B5
A7 🛚	8		13] B6
A8 🛚	9		12	B7
GND [10		11] B8

FUNCTION TABLE

INP	UTS	INPUT/ OUTPUTS
OE	ŌĒ	A, B
Χ	L	A = B
Н	X	A = B
L	Н	Z

SN74CBT3383 - 10-Bit Bus-Exchange Switch



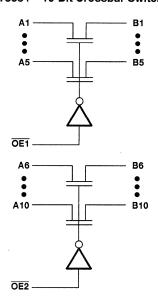
DB, DW, OR PW PACKAGE (TOP VIEW)

			L
BE	Q 1	O 24	D v _{cc}
C1	2	23	D5
A1	[] 3	22	B 5
B1	[] 4	21] A5
D1	[] 5	20	C5
C2	6	19] D4
A2	Q 7	18] B4
B2		17] A4
D2	9	16	C4
СЗ		15] D3
АЗ	[] 11	14] B3
GND	12	13] BX

FUNCTION TABLE

BE	вх	A1 – A5	B1-B5
L	L	C1-C5	D1-D5
L	Н.	D1 – D5	C1 -C5
Н	Х	Z	Z

SN74CBT3384 - 10-Bit Crossbar Switch

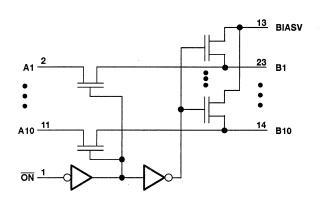


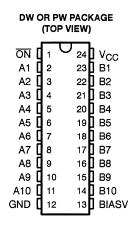
DB, DW, OR PW PACKAGE (TOP VIEW) 24 VCC OE1 В1 П 23 B10 Α1 **[**] 3 22 A10 A2 🛮 4 21 A9 B2 🛛 5 20 B9 вз [19 B8 6 АЗ [7 18 A8 A4 **Π** 8 17 A7 B4 🛮 9 16 B7 B5 🛮 10 15 B6 A5 🛮 11 14 🛮 A6 13 OE2 GND [] 12

FUNCTION TABLE

OE1	OE2	B1 – B5	B6-B10
L	L	A1 – A5	A6-A10
L	Н	A1 – A5	Z
н	L	Z	A6-A10
н	Н	Z	z

SN74CBT6800 - 10-Bit Crossbar Switch With Precharged Outputs for Live Insertion

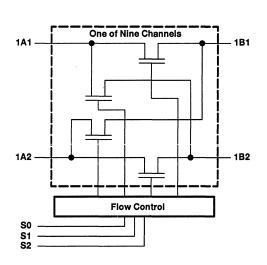




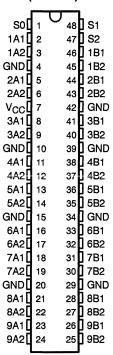
FUNCTION TABLE

ON	B1-B10	FUNCTION
L	A1-A10	Connect
Н	BIAS V	Precharge

SN74CBT16209 - 18-Bit Bus-Exchange Switch



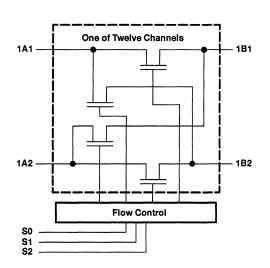
DGG OR DL PACKAGE (TOP VIEW)



FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
, L	L	L	Z	Z	Disconnect
L	L	Н	B1	Z	A1 to B1
L	Н	L	B2	Z	A1 to B2
L	Н	Н	z	B1	A2 to B1
Н	L	L	z	B2	A2 to B2
Н	L	Н	Z	Z	Disconnect
Н	н	L	B1	B2	A1 to B1, A2 to B2
Н	н	Н	B2	B1	A1 to B2, A2 to B1

SN74CBT16212 - 24-Bit Bus-Exchange Switch



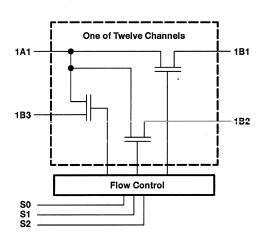
DGG OR DL PACKAGE (TOP VIEW)

	•		•	
	$\boldsymbol{\Gamma}$	U		L
S0	_			S1
1A1			55] S2
1A2]1B1
2A1] 1B2
2A2]2B1
3A1	6		51	2B2
3A2]3B1
GND			49]GND
4A1	9]3B2
4A2] 4B1
5A1				3 4B2
5A2]5B1
6A1	13]5B2
6A2	14		43]6B1
7A1 7A2	15		42] 6B2
7A2	16		41	781
vcc l	17		40] 7B2
8A1	18]8B1
GND]GND
8A2]8B2
9A1		:	36	9B1
9A2]9B2
0A1	23	;	34]10B1
0A2] 10B2
11A1	25]11B1
11A2				11B2
2A1] 12B1
2A2	28	:	29] 12B2
		_	_	

FUNCTION TABLE

. 511011011 171212						
S2	S1	S0	A1	A2	FUNCTION	
L	L	L	Z	Z	Disconnect	
L	L	Н	B1	z	A1 to B1	
L	н	L	B2	z	A1 to B2	
L	н	н	z	B1	A2 to B1	
Н	L	L	z	B2	A2 to B2	
Н	L	Н	z	z	Disconnect	
Н	н	L	B1	B2	A1 to B1, A2 to B2	
н	н	н	B2	B1	A1 to B2, A2 to B1	

SN74CBT16214 - 3-to-1 Bus-Select Switch



DGG OR DL PACKAGE (TOP VIEW)

	(. 0.	• • • •	- •••,	
en F	[U		h _e
S0[56]S1
1A1[55	S2
1B3[54	1B1
2A1 [53	1B2
2B3[52	2B1
3A1 [51	2B2
3B3 [50	3B1
GND [49	GND
4A1 [48	3B2
4B3			47] 4B1
5A1 [46	4B2
5B3 [45]5B1
6A1 [5B2
6B3 []6B1
7A1 [15]6B2
7B3[41]7B1
V _{CC} [17		40]7B2
8A1 [18] 8B1
GND[19		38	GND
8B3[20		37] 8B2
9A1 [21		36] 9B1
9B3 [22			9B2
10A1 [23		34	10B1
10B3 [10B2
11A1 [11B1
11B3 [26		31] 11B2
12A1 [27			12B1
12B3	28			12B2
	Ъ			г

FUNCTION TABLE

S2	S1	S0	A1	FUNCTION
L	L	L	Z	Disconnect
L	L	Н	B1	A1 to B1
L	н	L	B2	A1 to B2
L	н	Н	Z	Disconnect
Н	L	L	Z	Disconnect
Н	L	Н	В3	A1 to B3
Н	н	L	B1	A1 to B1
Н	Н	Н	B2	A1 to B2

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices can also provide bidirectional 5-V to 3-V translation with no added propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes the gate to drop to 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_{OC} to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

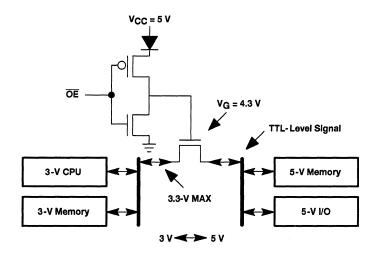


Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems where signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices can also replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on resistance and without the reliability problem that relays provide.

Bus Switches Convert TTL Logic to Hot-Card Insertion Capability

This application is used mostly in systems that require hot-card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and can not be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., that do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first followed by the signal pins then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance can not be achieved using CMOS logic since it contains P-channel transistors that provide an inherent diode between the I/O pins and V_{CC} that is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground leaving the bus disturbed.

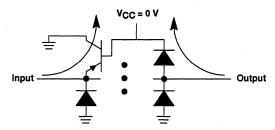


Figure 5. ACL Direction of Current Flow When $V_{CC} = 0 \text{ V}$

Another issue to consider is that, when V_{CC} is ramping but still below the device operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error will not occur.

There are two solutions to this problem. One is to use Texas Instruments BCT or ABT families, since both guarantee the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down .

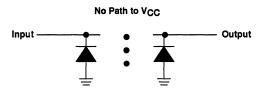


Figure 6. No ABT Current Flow When V_{CC} = 0 V

The second solution is to use the Texas Instruments crossbar technology (CBT) family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot-card insertion. It has a built-in channel pullup tied to a bias voltage (BIAS V) that is provided to ensure power up such that the buses are not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

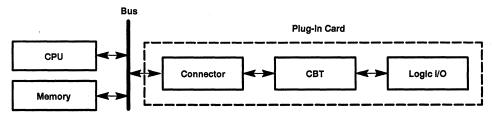
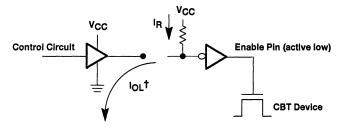


Figure 7. Hot-Card Insertion Application



 † I_{OL} > I_R, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple N-channel transistors, they are capable of providing several important bus functions, such as hot-card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

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LVT Family Characteristics

Ken Ristow Advanced System Logic – Semiconductor Group



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Introduction

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures which support live insertion

Standard TTL output drives of:

 $V_{OH} = 2 \text{ V at } I_{OH} = -32 \text{ mA}$

 $V_{OL} = 0.55 \text{ V}$ at $I_{OL} = 64 \text{ mA}$

Rail-to-rail switching for driving CMOS

Maximum supply currents of:

 $I_{CCL} \le 15 \text{ mA}$

 $I_{CCH} \le 200 \,\mu\text{A}$

 $I_{\text{CCZ}} \leq 200~\mu\text{A}$

Propagation delays of:

 $t_{pd} < 4.6 \text{ ns}$

 t_{pd} (LE to Q) < 5.1 ns

 t_{pd} (CLK to Q) < 6.3 ns

Surface mount packaging support including fine-pitch packages:

48-/56-pin SSOP and TSSOP for LVT Widebus™

20-/24-pin SOIC and TSSOP for standard LVT

LVT Input/Output Characteristics

Figure 1 shows a simplified LVT output and illustrates the mixed-mode-signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), and provide the dc drive needed for existing 5-V backplanes. This allows for a simple solution to reduce system power via the migration to 3.3-V operation.

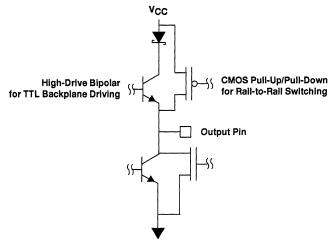


Figure 1. Simplified LVT Output Structure

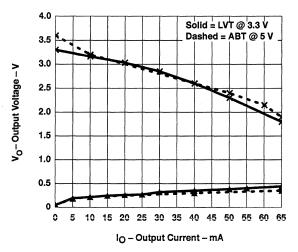


Figure 2. ABT vs LVT Output-Drive Comparison

Not only can LVT devices operate as 3-V to 5-V level translators by supporting input or I/O voltages of 5.5 V with $V_{CC} = 2.7 \text{ V}$ to 3.6 V, the inputs can withstand 5.5 V even when $V_{CC} = 0 \text{ V}$. This allows for the devices to be used under partial system power-down applications or those which require live insertion.

Bus Hold

Many times, devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, $\pm 100 \,\mu\text{A}$, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately $\pm 500 \,\mu\text{A}$, to toggle the state of the input. This current is trivial when compared to the tens of mA of current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live-insertion or partial-power applications, while providing for low-input leakage currents. The outputs are capable of driving today's 5-V backplanes, with a considerable reduction in device power consumption, as well as being packaged in state-of-the-art fine-pitch surface-mount packages.

'LVT244 Characteristics

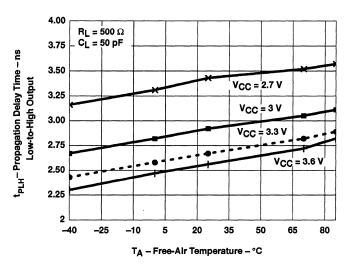


Figure 3. Propagation Delay vs Free-Air Temperature

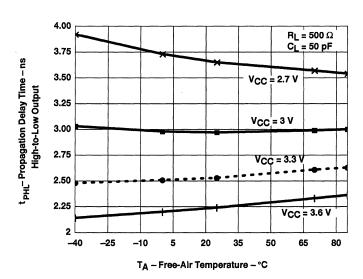


Figure 4. Propagation Delay vs Free-Air Temperature

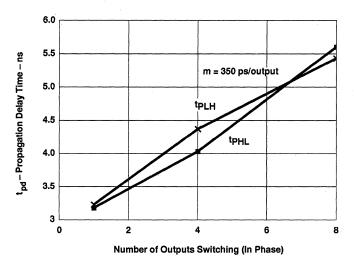


Figure 5. Propagation Delay vs Outputs Switching

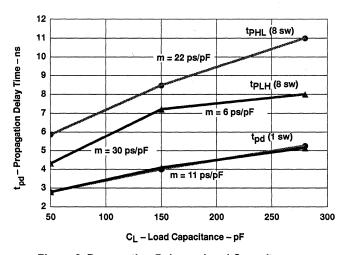


Figure 6. Propagation Delay vs Load Capacitance

'LVT244 Typical dc Characteristics

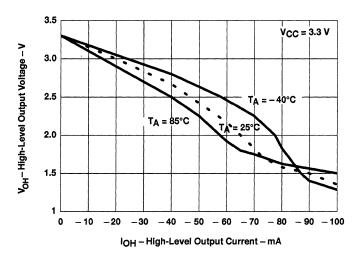


Figure 7. High-Level Output Voltage vs High-Level Output Current

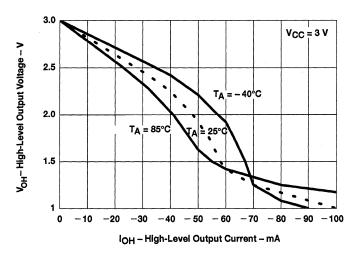


Figure 8. High-Level Output Voltage vs High-Level Output Current

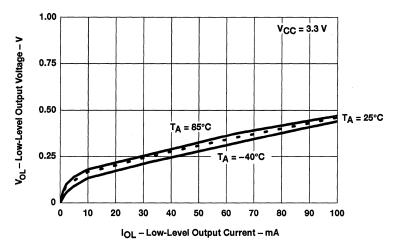


Figure 9. Low-Level Output Voltage vs Low-Level Output Current

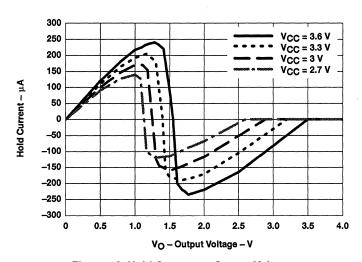


Figure 10. Hold Current vs Output Voltage

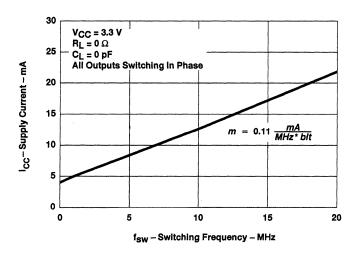
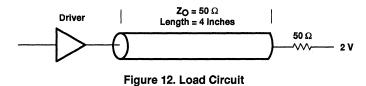


Figure 11. Supply Current vs Switching Frequency

Unloaded tr and tf Rates

The circuit shown below was used to measure the unloaded transition rates of the output.



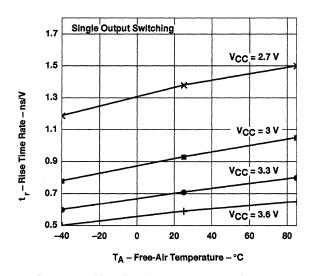


Figure 13. Rise Time Rate vs Free-Air Temperature

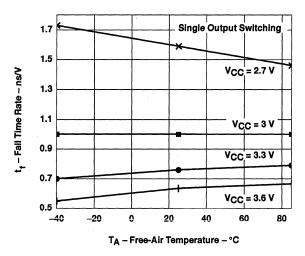


Figure 14. Fall Time Rate vs Free-Air Temperature

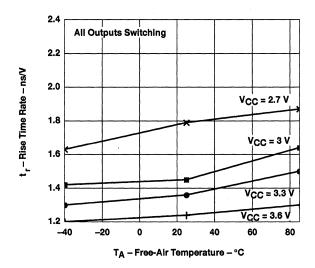


Figure 15. Rise Time Rate vs Free-Air Temperature

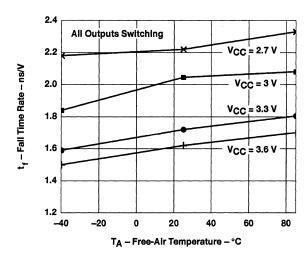


Figure 16. Fall Time Rate vs Free-Air Temperature

'LVT646 Characteristics

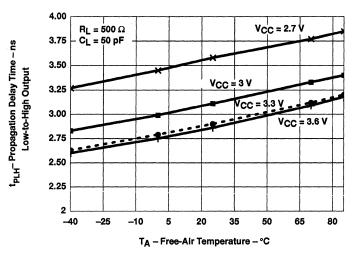


Figure 17. Thru-Mode Propagation Delay vs Free-Air Temperature

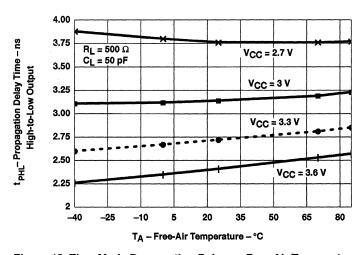


Figure 18. Thru-Mode Propagation Delay vs Free-Air Temperature

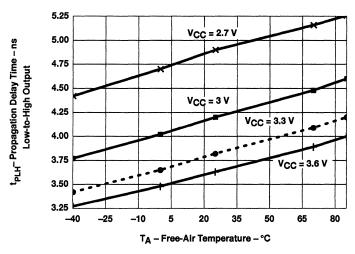


Figure 19. Clock-to-Q Propagation Delay vs Free-Air Temperature

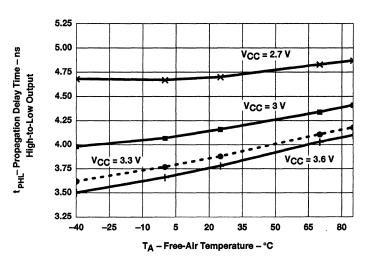


Figure 20. Clock-to-Q Propagation Delay vs Free-Air Temperature

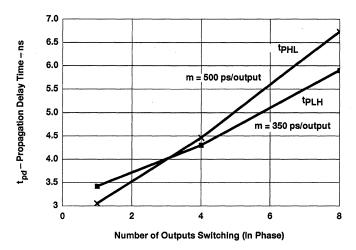


Figure 21. Propagation Delay vs Outputs Switching

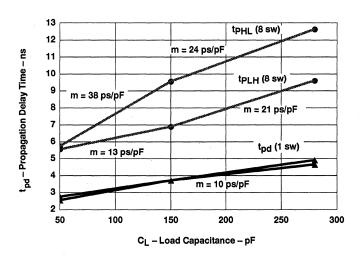
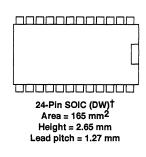
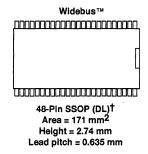
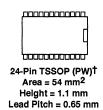


Figure 22. Propagation Delay vs Load Capacitance

Packaging Options









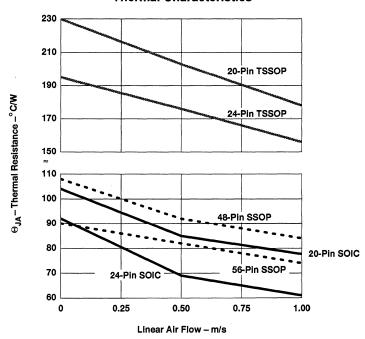
Area = 108 mm²

Height = 1.1 mm

Lead Pitch = 0.5 mm

†TI package designators

Thermal Characteristics



Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated.

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Mechanical Data 4

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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a three-part type number as explained in the following example.

Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN = Standard prefix
SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN SIX TO TWELVE CHARACTERS

Examples: 74LV00
74LVT244
74ALVC16244

Package -

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package
DB, DL = plastic shrink small-outline package
DGG, PW = plastic thin shrink small-outline package

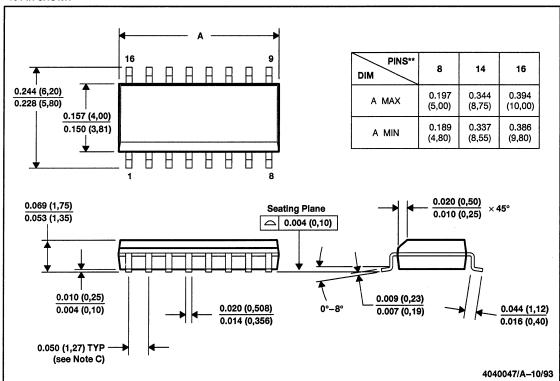
FK = leadless ceramic chip carrier
HV = ceramic quad flat package
J, JT = dual-in-line package
PM = plastic quad flat package
WD = ceramic flat package

(from pin-connection diagram on individual data sheet)

D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16 PIN SHOWN

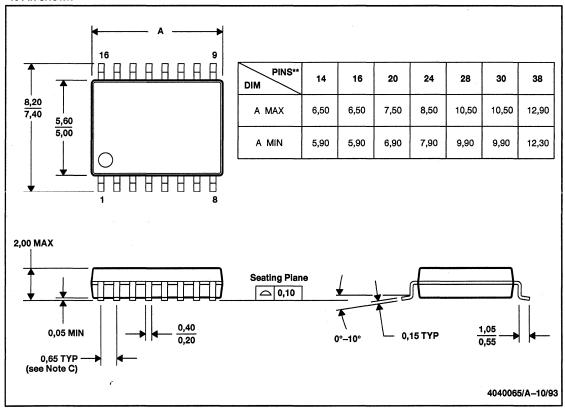


- B. This drawing is subject to change without notice.
- C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
- D. Body dimensions do not include mold flash or protrusion.
- E. Mold protrusion shall not exceed 0.006 (0,15).

DB/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

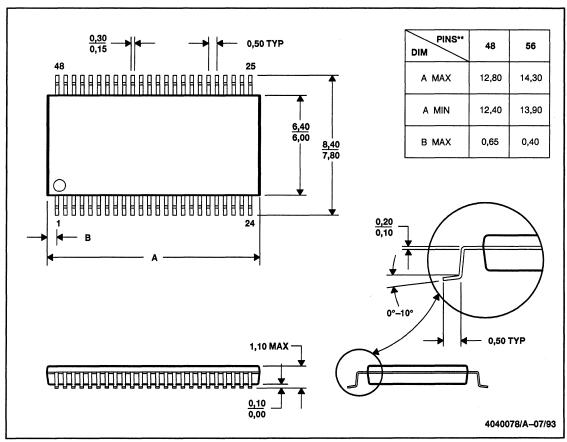
C. Leads are within 0,127 radius of true position at maximum material condition.

D. Body dimensions do not include mold flash or protrusion.

E. Mold protrusion shall not exceed 0.006 (0,15).

DGG/R-PDSO-G**

300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE



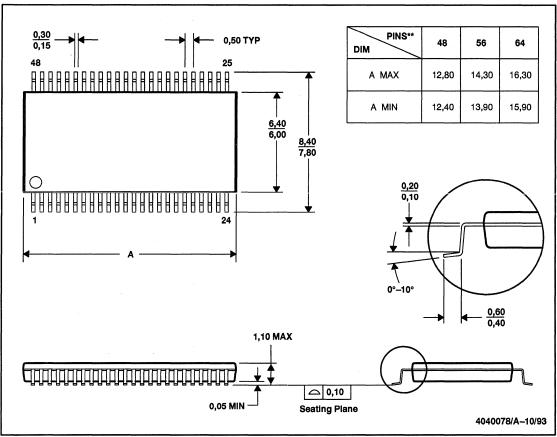
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions include mold flash or protrusion.

DGG/R-PDSO-G** **48 PIN SHOWN**

THIN SHRINK SMALL-OUTLINE PACKAGE



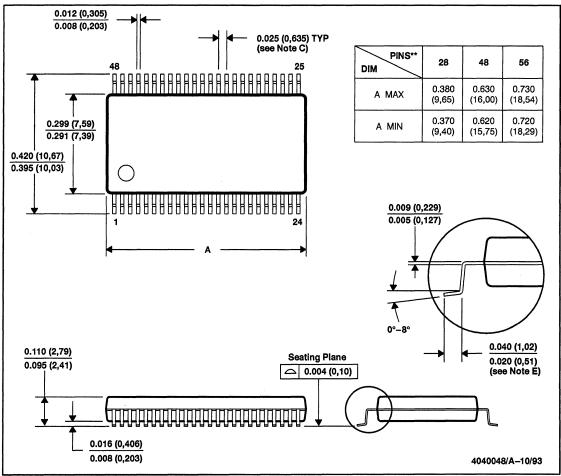
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.C. Body dimensions include mold flash or protrusion.

DL/R-PDSO-G**

PLASTIC SHRINK SMALL-OUTLINE PACKAGE

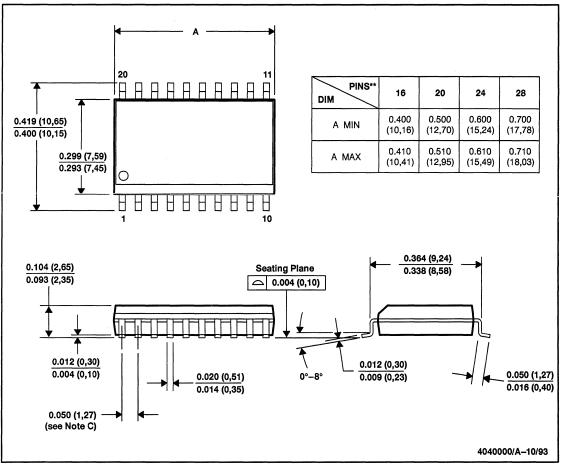
48 PIN SHOWN



- B. This drawing is subject to change without notice.
- C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
- D. Body dimensions do not include mold flash or protrusion, which does not exceed 0.006 (0,15).
- E. Foot length measured from lead top to point 0.010 (0.2,54) above seating plane.

DW/R-PDSO-G** 20 PIN SHOWN

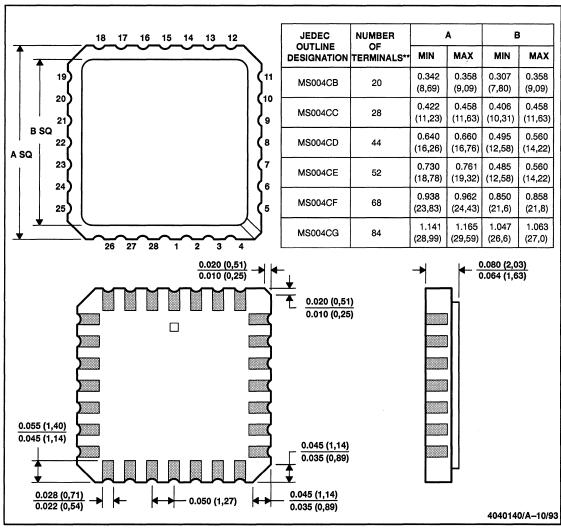
PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
 - D. Body dimensions do not include mold flash or protrusion.
 - E. Mold protrusion shall not exceed 0.006 (0,15).

FK/S-CQCC-N** 28 TERMINAL SHOWN

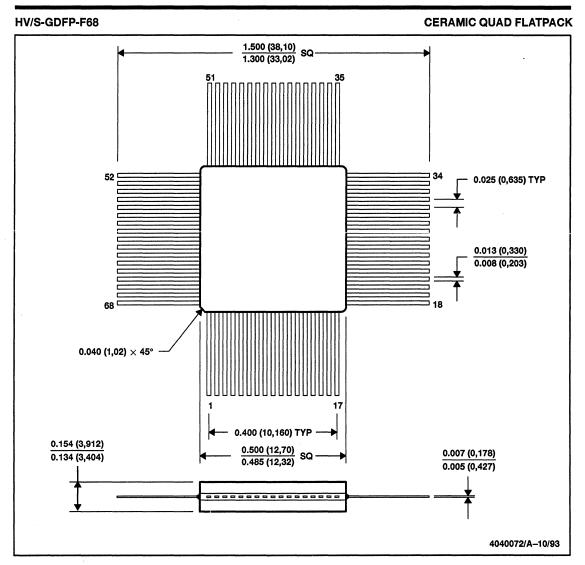
LEADLESS CERAMIC CHIP CARRIER PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Three-layer ceramic base with a metal lid and braze seal.
- D. FK package terminal assignments conform to JEDEC Standards 1, 2, and 11.
- E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.





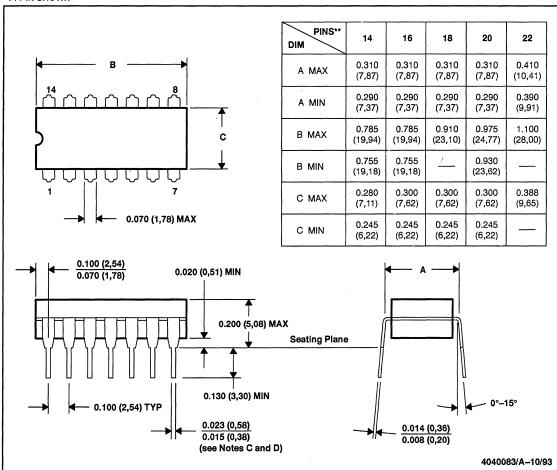
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN

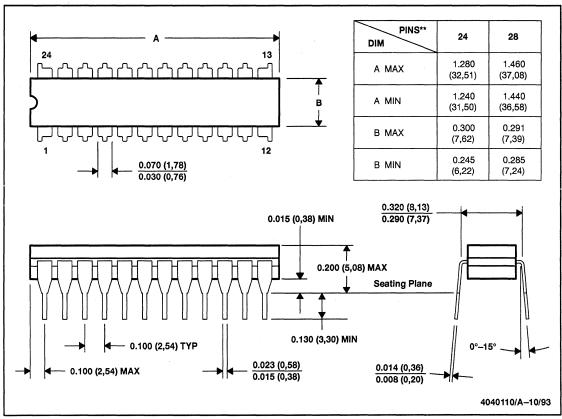


- B. This drawing is subject to change without notice.
- C. This dimension does not apply for solder-dipped leads.
- D. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

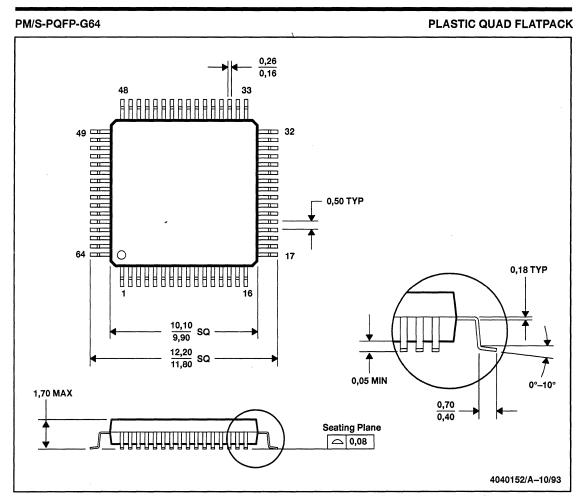
JT/R-GDIP-T**

24 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE



- B. This drawing is subject to change without notice.
- C. This package is glass sealed.



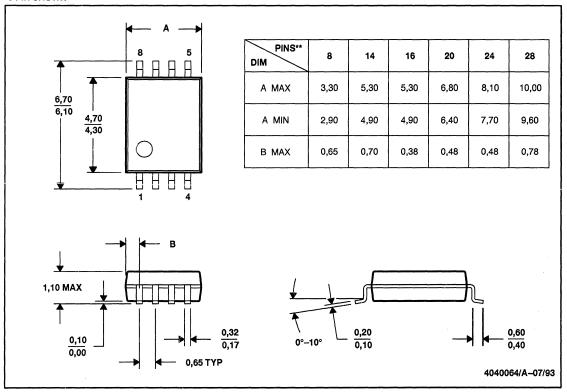
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

PW/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

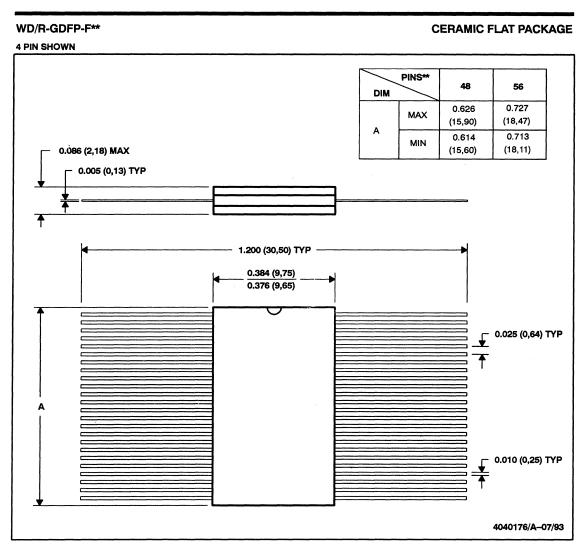
8 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Drawing source: SCJ Package Handbook, 1990



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

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