TEXAS INSTRUMENTS

Low-Voltage Logic

LV, LVC, LVT, LVTZ, ALVC, CBT, and GTL Families

Data Book

Data Book

Low-Voltage Logic

1994

1994

Advanced System Logic Products

Low-Voltage Logic Data Book

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INTRODUCTION

The 3.3-V era has arrived! The combination of continuous advancement in semiconductor wafer fabrication technologies and the proliferation of battery-powered computing devices has changed the system design methodologies of the past, and indeed our entire industry. This new era will bring an entirely new set of possibilities for computing and hand-held instruments. Products that will run faster, consume less power, and use fewer total system components than ever before. Products that will be smaller and lighter, yet maintain interface compatibility with existing industry standard bus architectures. Products that will in turn bring on the next era in the computer industry.

Welcome to the 1994 Texas Instruments Low-Voltage Logic Data Book. A single family of 3.3-V logic products could not possibly cover the diverse needs of all of the end equipment segments. Products ranging from hand-held point-of-sale terminals, notebook and laptop personal computers, low-power environmentally conscious desktop computers and peripherals, and high-performance RISC and CISC workstation platforms will all share the need for low-voltage technology, but will each have radically different price, performance, and feature requirements for the logic they will employ. As a response to these diverse needs, Texas Instruments has developed four independent logic families:

Low-Voltage HCMOS (LV)
Low-Voltage CMOS (LVC)
Low-Voltage Technology (LVT)
Advanced Low-Voltage CMOS (ALVC)

These products span four generations of CMOS and BiCMOS process technologies and years of fine-pitch packaging and innovative circuit developments to deliver a set of products for each of these end-equipment segments. In addition to popular octal and Widebus™ bus-interface circuits, two of the families also include SSI and MSI logic functions to help streamline design and facilitate time to market. Voltage translators are also provided to bridge the gap between the 5-V and 3.3-V worlds as well as the CBT family of ultra high-speed bus switches which can be easily adapted to these mixed 3.3-V/5-V environments. Designers of high-speed backplane applications will have great interest in the GTL family of transceivers.

Some of the information in this data book is in product preview form. For more information on these products including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments field sales representative, authorized distributor, or call our Advanced Logic hotline at (214) 997-5202.

We hope you will agree that Texas Instruments has developed the most complete line of low-voltage logic products in the industry. We also hope that these products will meet your system and design needs.

PRODUCT STAGE STATEMENTS

Product stage statements are used on Texas Instruments data sheets to indicate the development stage(s) of the product(s) specified in the data sheets.

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ALPHANUMERIC INDEX

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i Input capacitance

The internal capacitance at an input of the device

C_o Output capacitance

The internal capacitance at an output of the device

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

I_{CEX} Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V_O = 5.5 V.

$I_{I(hold)}$ Input hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state.

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input.

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input.

I_{off} Input/output power-off leakage current

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V

I_{OH} High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} Low-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

$I_{OZPU/PD}$ Off-state (high-impedance-state) output current (of a 3-state output)

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

t_a Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c Clock cycle time

Clock cycle time is $1/f_{max}$.

t_{dis} Disable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} Enable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

t_h Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

t_{PLH} Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

*Current out of a terminal is given as a negative value.

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{IT+} **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}.

V_{IT-} **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

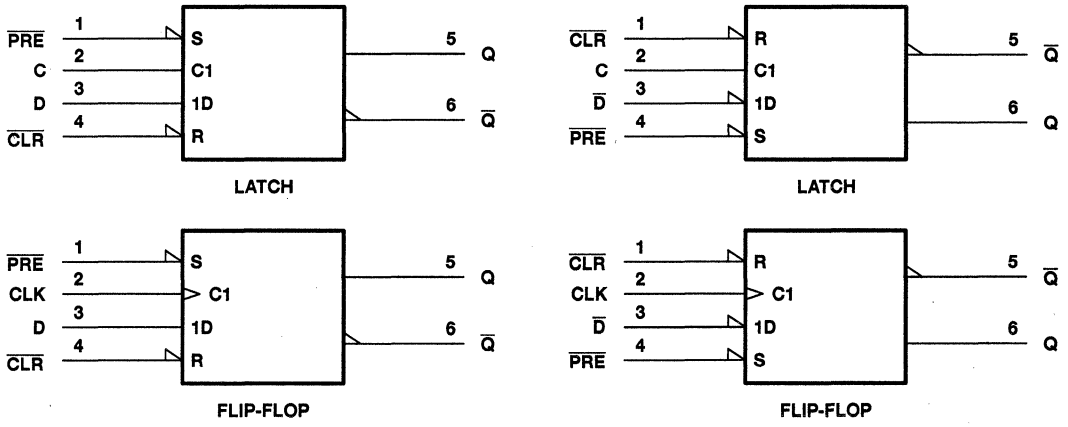
The function table functional tests do not reflect all possible combinations or sequential modes.

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow. Figures 2, 3, 4, and 5 are derating curves for the DB package.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the LVL family. In general, the junction temperature for any device can be calculated using using the following equation.

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device (see Section 15, package thermal considerations)
T_A = free-air temperature

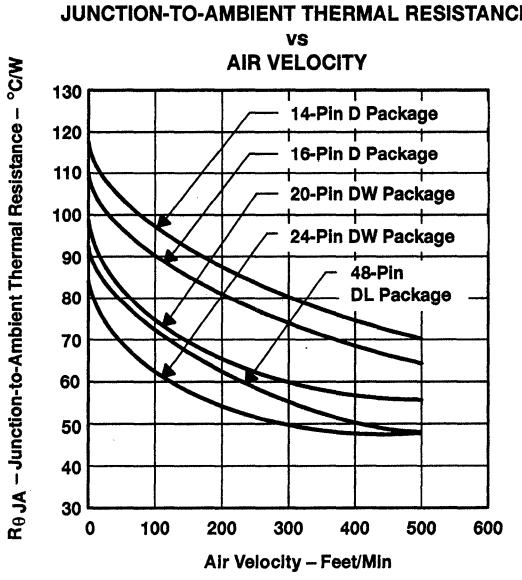


Figure 1

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

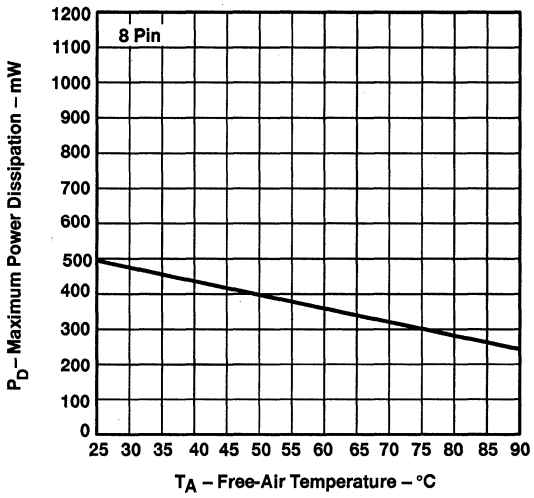


Figure 2

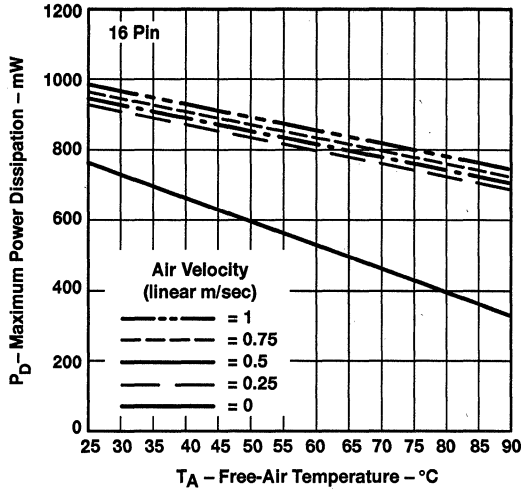


Figure 3

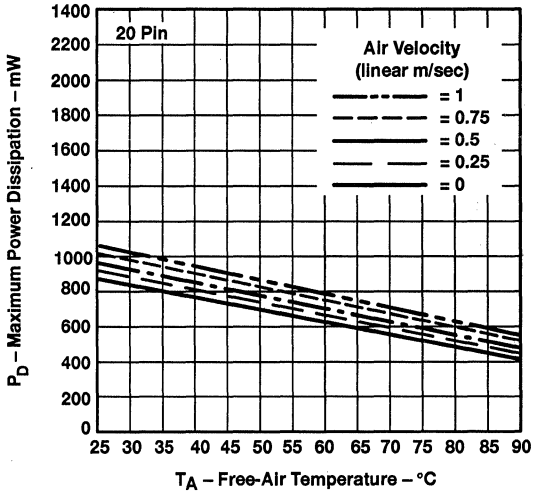


Figure 4

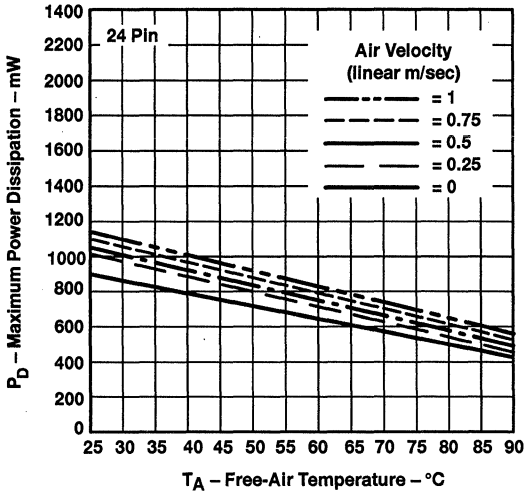


Figure 5

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type and list all available or planned options of that function. The technology columns identify the appropriate family and a particular data book where more information can be found. The applicable literature number, composed of either seven or eight alphanumeric characters, can be found at the lower right-hand corner on the back cover of each publication.

List of additional Advanced System Logic data books:

ABT Devices†	Advanced BiCMOS Technology	SCBD002A
AC and ACT Devices	Advanced CMOS Logic Data Book	SCAD001C
Advanced Logic Devices	Advanced Logic and Bus-Interface Data Book	SCYD001
ALS and AS Devices†	ALS/AS Logic Data Book	SDAD001B
ATM and SONET Devices†	ATM and SONET Product Information	SDNS023
BCT Devices	BiCMOS Bus-Interface Logic Data Book	SCBD001B
CDC Devices	Clock-Distribution Circuits Data Book	SCAD004
F Devices	F Logic (SN54/74F) Data Book	SDFD001B
FIFO Devices†	High-Performance FIFO Memories Data Book	SCAD003A
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
SCOPE™ Devices†	SCOPE™ Product Information	SSYV001
SPICE I/O Models	Advanced Bus Interface SPICE I/O Models	SCBD004
Std TTL, LS, and S Devices	TTL Logic Data Book	SDLD001A

† Updated data book planned for this technology.

Contents

Contents (Continued)

GATES

Positive-NAND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
8-Input		'30	✔	✔	✔								
		'11030						✔	✔				
13-Input		'133	✔			✔							
Dual 2-Input		'8003	✔										
Dual 4-Input		'20	✔	✔	✔	✔							
		'40	✔										
		'11020						✔	✔				
Triple 3-Input		'10	✔	✔	✔	✔							+
		'1010	✔										
		'11010						✔	✔				
Quad 2-Input		'00	✔	✔	✔	✔	✔					✔	+
		'11000						✔	✔				
		'37	✔										
	OC	'38	✔		✔								
		'132				✔							
		'11132						✔	✔				
		'1000		✔									
Hex 2-Input		'804	✔	✔									
Quad 2-Input	OC	'01	✔			✔							
		'03	✔			✔							

Positive-AND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-Input	OC	'09	✔			✔							
		'7001				✔							
Dual 4-Input		'21	✔	✔	✔	✔							
		'11021						✔	✔				
Triple 3-Input		'11	✔	✔	✔	✔							
		'11011						✔	✔				
Quad 2-Input		'08	✔	✔	✔	✔	✔					✔	+
		'1008		✔									
		'11008						✔	✔				
Hex 2-Input		'808		✔									

✔ Product available in technology indicated
+ New product planned in technology indicated

GATES

Positive-OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Triple 3-Input		'4075				✔							
Quad 2-Input		'32	✔	✔	✔	✔	✔					✔	+
		'1032		✔									
		'11032						✔	✔				
		'7032				✔							
Hex 2-Input		'832	✔	✔		✔							
Dual 5-Input		'260			✔								
Triple 3-Input		'27	✔	✔	✔	✔							
		'11027						✔	✔				
Quad 2-Input		'02	✔	✔	✔	✔	✔					✔	+
	OC	'33	✔										
		'7002				✔							
		'11002						✔	✔				
Hex 2-Input		'805	✔	✔		✔							

OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs		'86	✔	✔	✔	✔							+
		'11086						✔	✔				
Quad 2-Input Exclusive-OR Gates	OC	'136	✔										
Quad 2-Input Exclusive-NOR Gates	OD	'266				✔							
		'810	✔										
	OC	'811	✔										

AND-OR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 2-Wide 2-Input, 3-Input		'51			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Hex Inverters		'04	✔	✔	✔	✔	✔					✔	+
		'U04				✔						✔	+
		'11004						✔	✔				
	OC	'05	✔			✔							
		'14				✔						✔	+
		'11014						✔	✔				
		'1004	✔	✔									
		'1005	✔										
Hex Noninverters		'11034						✔	✔				
	OC	'35	✔										
		'1034	✔	✔									
	OC	'1035	✔										

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Quad Buffers/Drivers	3S	'125			✔	✔	✔			✔	✔	✔		+	
		'126			✔	✔				✔	✔			+	
Noninverting Hex Buffers/Drivers	3S	'365				✔									
		'367				✔									
Inverting Hex Buffers/Drivers	3S	'368				✔									
Noninverting Octal Buffers/Drivers	3S	'241	✔	✔	✔	✔	✔			✔	✔			+	
		'11241						✔	✔						
		'25241									+				
		'244	✔	✔	✔	✔	✔			✔	✔		✔	+	
		'244A										✔			
		'11244						✔	✔						
		'1244	✔												
		'25244								✔	+				
		'541	✔		✔	✔	✔			✔	✔			+	
	OC	'757		✔						✔					
		'760	✔	✔						✔					
		'25760								+					
Inverting Octal Buffers/Drivers	3S	'240	✔	✔	✔	✔	✔			✔	✔	✔	✔	+	
		'11240						✔	✔						
		'1240	✔												
		'25240								✔					
		'466	✔												
		'540	✔			✔	✔			✔	✔			+	
	OC	'756	✔	✔						✔					
		'763	✔	✔											
Inverting and Noninverting Octal Buffers/Drivers	3S	'230		✔											
	OC	'762		✔											
Triple 4-Input OR/NOR Drivers		'11802							✔						
Noninverting 10-Bit Buffers/Drivers	3S	'827									✔			✔	
		'11827						✔	✔						
		'29827	✔							✔					
Inverting 10-Bit Buffers/Drivers	3S	'828									+			+	
		'11828						✔	✔						
		'29828	✔							✔					
Noninverting 16-Bit Buffers/Drivers	3S	'16241							✔		✔			+	
		'16244						✔	✔		✔			+	+
		'16244A										✔			
		'16541							✔		✔			+	

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers (Continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY											
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Inverting 16-Bit Buffers/Drivers	3S	'16240						✔	✔		✔			+	+
		'16540							✔		✔				
Noninverting 18-Bit Buffers/Drivers	3S	'16825							✔		✔				+
Inverting 18-Bit Buffers/Drivers	3S	'16826									+				
Noninverting 20-Bit Buffers/Drivers	3S	'16827							✔		✔				+
Inverting 20-Bit Buffers/Drivers	3S	'16828									+				+
Octal Buffers/Drivers With Input Pullup Resistors		'746	✔												

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY							
			AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	3S	'16500					✔			+
		'16500B				✔				
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	3S	'16501				✔	✔		+	+
		'16600				✔				+
		'16601				✔				+
Noninverting 36-Bit Universal Bus Transceivers (UBT™)	3S	'32501				✔				
Noninverting 16-Bit Tri-Port Universal Bus Exchangers (UBE™)	3S	'32316				✔				
Noninverting 18-Bit Tri-Port Universal Bus Exchangers (UBE™)	3S	'32318				✔				
18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port	3S	'162500				✔				
		'162501				✔				
		'162600				+				
		'162601				✔				
SCOPE™ 18-Bit Universal Bus Transceivers (UBT™)	3S	'18502				✔	+			
SCOPE™ 20-Bit Universal Bus Transceivers (UBT™)	3S	'18504				✔	+			

✔ Product available in technology indicated
\+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting Quad Transceivers	3S	'243	✔		✔										
Inverting Quad Transceivers	OC	'758	✔												
	3S	'242			✔										
Noninverting Octal Transceivers	3S	'245	✔	✔	✔	✔	✔			✔	✔		✔	+	
		'245A										✔			
		'1245	✔												
		'11245						✔	✔						
		'25245								✔	✔				
		'645	✔	✔		✔	✔								
		'1645	✔												
	OC	'621	✔		✔										
		'641	✔	✔											
	OC/3S	'639	✔	✔											
Inverting Octal Transceivers	3S	'620	✔							✔	✔				
		'623	✔	✔	✔	✔	✔			✔	✔				
		'11623							✔						
		'640	✔	✔		✔				✔	✔				
		'1640	✔												
		'11640							✔						
	OC	'642	✔												
		'25642								✔					
	OC/3S	'638	✔	✔											
Noninverting 9-Bit Transceivers	3S	'863									✔			+	
		'29863	✔							✔					
Inverting 9-Bit Transceivers	3S	'29864								✔					
Noninverting 10-Bit Transceivers	3S	'861									+				
		'29861								✔					
Inverting 10-Bit Transceivers	3S	'29862								✔					
Noninverting 16-Bit Transceivers	3S	'16245						✔	✔		✔			+	+
		'16245A									✔	✔			
		'16623						✔	✔		✔				
Inverting 16-Bit Transceivers	3S	'16640						✔	✔		✔				
		'16620						✔	✔		+				
Noninverting 18-Bit Transceivers	3S	'16863							✔		✔				
Inverting 18-Bit Transceivers	3S	'16864									+				

✔ Product available in technology indicated
+ New product planned in technology indicated

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BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers (Continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 20-Bit Transceivers	3S	'16861							✔		+				
Inverting 20-Bit Transceivers	3S	'16862									+				
Noninverting Octal Registered Transceivers	3S	'11470							✔						
		'543			✔					✔	✔	✔		+	
		'11543							✔						
		'646	✔	✔		✔	✔			✔	✔	✔		+	
		'646A									✔				
		'11646						✔	✔						
		'652	✔	✔		✔	✔			✔	✔	✔		+	
		'11652						✔	✔						
		'2952								✔	+	✔		+	
		'2952A									✔				
	OC/3S	'653	✔												
		'654	✔												
Inverting Octal Registered Transceivers	3S	'544								✔	+			+	
		'11544							✔						
		'648	✔	✔						✔	+				
		'11648							✔						
		'651	✔	✔						✔	✔				
		'2953								✔	+				
Noninverting 16-Bit Registered Transceivers	3S	'16470							✔		✔				
		'16543						✔	✔		✔	✔		+	+
		'16646						✔	✔		✔	✔		+	+
		'16652						✔	✔		✔	+		+	+
		'16952							✔		✔	✔		+	+
Inverting 16-Bit Registered Transceivers	3S	'16471									+				
		'16544							✔		+			+	
		'16648							✔		+				
		'16651							✔		+				
		'16953									+				

✔ Product available in technology indicated
\+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers (Continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit Registered Transceivers	3S	'16472						✔							
		'16474							✔						
		'16500									✔	✔		+	+
		'16501									✔	+		+	+
		'16600									✔				+
		'16601									✔				+
Inverting 18-Bit Registered Transceivers	3S	'16475							✔						
Noninverting 36-Bit Transceivers	3S	'32245									+				
Noninverting 36-Bit Registered Transceivers	3S	'32501									✔				
		'32543									✔				
8-/9-Bit Bus Transceivers With Parity Checkers/ Generators	3S	'657			✔					✔	+				
		'659					✔								
		'833									+				
		'834									+				
		'853									+				
		'854									+				
		'899								✔					
	3S/OC	'29833	✔							✔					
		'29834								✔					
		'29853	✔							✔					
		'29854	✔							✔					
Dual 8-/9-Bit Bus Transceivers With Parity Checkers/ Generators	3S	'16833							✔		✔				
		'16657							✔		✔				
		'16853									✔				
Universal Transceivers/Port Controllers	3S	'856		✔											
Noninverting 16-Bit Tri-Port Registered Bus Exchangers	3S	'32316									✔				
Noninverting 18-Bit Tri-Port Registered Bus Exchangers	3S	'32318									✔				

✔ Product available in technology indicated
\+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

MOS Memory Drivers/Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY											
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LVC	ALVC
Octal Transceivers With Series Resistors on Output	3S	'2623		✔										
Octal Buffers/Drivers With Series Resistors on Output	3S	'2240	✔							✔	✔			
		'2241								✔	✔			
		'2244								✔	✔			
		'2541	✔											
Octal Transceivers With Series Resistors on B Port	3S	'2245								✔	+			
Octal Latches With Series Resistors on Output	3S	'2574								+				
10-Bit Buffers/Drivers With Series Resistors	3S	'2827								✔				
		'2828								✔				
11-Bit Buffers/Drivers With Series Resistors	3S	'2410								✔				
		'2411								+				
		'5400									✔			
		'5401									✔			
12-Bit Buffers/Drivers With Series Resistors	3S	'5402									✔			
		'5403									✔			
16-Bit Buffers/Drivers With Series Resistors	3S	'162240									+			
		'162244									✔	+	+	+
16-Bit Transceivers With Series Resistors	3S	'162245									✔	+	+	+
18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port	3S	'162500									+			
		'162501									+			+
		'162600									+			
		'162601									✔			+
12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port	3S	'162260									✔			

✔ Product available in technology indicated
+ New product planned in technology indicated

TESTABILITY BUS-INTERFACE CIRCUITS

JTAG/IEEE 1149.1 Testability Circuits

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY							
				F	HC	HCT	AC	ACT	BCT	ABT	LVT
Buffers/Drivers	8	3S	'8240A						✔		
			'8244A						✔		
Transceivers	8	3S	'8245							✔	
			'8245A						✔		
	18	3S	'18245							✔	+
Transparent Latches	8	3S	'8373A						✔		
Flip-Flops	8	3S	'8374A						✔		
Registered Transceivers	8	3S	'8543							✔	
			'8646							✔	
			'8652							✔	
			'8952							✔	
	18	3S	'18502							✔	+
			'18646							✔	
			'18652							+	
	20	3S	'18504							✔	+
Test Bus Controllers		3S	'8990					✔			
Digital Bus Monitors		3S	'8994					✔			
Scan Path Linkers With Identification Buses	4	3S	'8997					✔			
	8	3S	'8999					✔			

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Flip-Flops

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Dual J-K Edge Triggered		'73				✔									
		'76				✔									
		'109	✔	✔	✔	✔									
		'11109						✔	✔						
		'112	✔		✔	✔								+	
		'11112						✔	✔						
		'113	✔			✔									
		'114	✔												
Dual D-Type		'74	✔	✔	✔	✔	✔						✔	+	
		'11074						✔	✔						
Dual D-Type With 2-Input NAND/NOR Gates		'7074				✔									
		'7075				✔									
		'7076				✔									
Dual 4-Bit D-Type Edge Triggered	3S	'874	✔	✔											
		'11874							✔						
		'876	✔	✔											
		'879	✔	✔											
Quad D-Type		'173				✔									
		'175	✔	✔	✔	✔									
		'11175						✔	✔						
Hex D-Type		'174	✔	✔	✔	✔							✔		
		'11174						✔	✔						
		'378			✔	✔									
Octal D-Type True Data	3S	'374	✔	✔	✔	✔	✔			✔	✔		+	+	
		'11374						✔	✔						
		'574	✔	✔	✔	✔	✔			✔	✔	✔	+	+	
Octal D-Type True Data With Clear		'273	✔			✔	✔				✔	✔	+		
		'11273						✔	✔						
	3S	'575	✔	✔											
		'874	✔	✔											
Octal D-Type True Data With Clock Enable		'377			✔	✔	✔				✔				
		'11377						✔	✔						
Octal D-Type Inverting	3S	'534	✔	✔		✔				✔	✔				
		'11534						✔	✔						
		'564	✔												
		'576	✔	✔											
		'29826								✔					

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Flip-Flops (Continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Octal Dual-Ranked True Data	3S	'4374		✔											
Octal Inverting With Clear	3S	'577	✔												
		'879	✔	✔											
Octal Inverting With Preset	3S	'876	✔	✔											
Octal True Data	3S	'825		✔											
		'11825							✔						
		'29825								✔					
9-Bit True Data	3S	'823		✔							✔			+	
		'29823	✔							✔					
9-Bit Inverting	3S	'824		✔											
		'29824	✔												
10-Bit True Data	3S	'821		✔							✔			+	
		'1821		✔											
		'11821							✔						
		'29821	✔							✔					
10-Bit Inverting	3S	'29822								✔					
16-Bit D-Type True Data With Clock Enable		'16377									+				
16-Bit Noninverting	3S	'16374						✔	✔		✔	✔		+	+
16-Bit Inverting	3S	'16534									+				
18-Bit Noninverting	3S	'16823							✔		✔				+
20-Bit Noninverting	3S	'16821							✔		✔				+

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Latches

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY												
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Bistable	4		'75				✔									
			'375				✔									
D-Type Edge Triggered Inverting and Noninverting	8		'996	✔												
D-Type Transparent Readback Latch, True	8	3S	'990	✔												
	9	3S	'992	✔												
	10	3S	'994	✔												
D-Type Transparent With Clear, True Outputs	8	3S	'666	✔												
D-Type Transparent With Clear, Inverting Outputs	8	3S	'667	✔												
D-Type Transparent True	8	3S	'373	✔	✔	✔	✔	✔			✔	✔		+	+	
			'11373						✔	✔						
			'573	✔	✔	✔	✔	✔			✔	✔	✔	+	+	
	16	3S	'16373						✔	✔		✔	✔		+	+
			'16373A									✔				
	32	3S	'32373									+				
D-Type Dual 4-Bit Transparent True	8	3S	'873	✔	✔											
			'11873						✔							
D-Type Transparent Inverting	8	3S	'533	✔	✔						✔	✔				
			'11533						✔	✔						
			'563	✔			✔									
			'580	✔	✔											
	16	3S	'16533									+				
Dual 4-Bit Transparent Inverting	8	3S	'880	✔	✔											
2-Input Multiplexed	8	3S	'604				✔									
Addressable	8	2S	'259	✔			✔									
		Q	'4724				✔									

✔ Product available in technology indicated
\+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Latches (Continued)

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY												
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
D-Type True Inputs	8	3S	'845	✔												
			'29845	✔												
	9	3S	'843	✔	✔							✔			+	
			'1843		✔											
			'29843								✔					
	10	3S	'841	✔	✔							+			+	
			'29841	✔							✔					
	18	3S	'16843									+				+
	20	3S	'16841							✔		✔				+
D-Type Inverting Inputs	8	3S	'846	✔												
			'29846								✔					
	9	3S	'29844								✔					
	10	3S	'842	✔	✔											
			'29842	✔												

✔ Product available in technology indicated
+ New product planned in technology indicated

REGISTERS

Shift Registers

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	LV
Parallel In, Parallel Out, Bidirectional	4		'194		✔							
			'11194						✔	✔		
	8		'299	✔		✔						
			'323	✔								
Parallel In, Parallel Out	4		'195		✔							
Serial In, Parallel Out	8		'164	✔			✔					+
Parallel In, Serial Out	8		'165	✔			✔					
			'166	✔			✔					
Serial In, Parallel Out With Output Latches	8	3S	'594				✔					
			'595				✔					
Parallel Out	10		'11898						✔	✔		
Noninverting	8	3S	'299	✔								
	9	3S	'29823	✔								

Register Files

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 16 Word × 4 Bits	3S	'870	✔								
		'871		✔							

✔ Product available in technology indicated
+ New product planned in technology indicated

COUNTERS

Synchronous Counters – Positive Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
4-Bit Decade Up/Down	Sync	'568	✔							
4-Bit Binary	Sync	'161	✔	✔	✔	✔				
		'163	✔	✔	✔	✔				
		'561	✔							
4-Bit Binary Up/Down	Sync	'169	✔	✔	✔					
		'569	✔							
		'8169	✔							
	Async	'191	✔			✔				
		'11191						✔	✔	
		'193	✔			✔				
8-Bit Up/Down	Sync Clear	'869	✔	✔						
	Async Clear	'867	✔	✔						
		'11867							✔	
Divide-by-10	Sync	'4017				✔				

Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Dual 4-Bit Binary	None	'393				✔				
12-Bit Binary	Sync	'4040				✔				
14-Bit Binary	Sync	'4020				✔				
		'4060				✔				
		'4061				✔				

8-Bit Binary Counters With Registers

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Parallel Register Outputs	3S	'590				✔				
		'11590						✔	✔	
Parallel Register Inputs	3S	'11593						✔	✔	

✔ Product available in technology indicated
+ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-to-1		'157	✔	✔	✔	✔	✔						+
		'11157						✔	✔				
		'158	✔	✔	✔	✔							
		'11158						✔	✔				
		'298		✔									
	3S	'257	✔	✔	✔	✔	✔						+
		'11257						✔	✔				
		'258	✔	✔	✔	✔							
		'11258							✔				
Dual 4-to-1		'153	✔	✔	✔	✔							
		'11153						✔	✔				
		'352	✔										
	3S	'253	✔	✔	✔	✔							
		'11253						✔	✔				
		'353		✔									
		'11353							✔				
Hex 2-to-1 Universal Multiplexer	3S	'857	✔										
8-to-1		'151	✔	✔	✔	✔							
		'11151						✔	✔				
	3S	'251	✔		✔	✔							
		'11251						✔					
		'354				✔							
16-to-1	3S	'250		✔									
		'850		✔									
		'851		✔									
Full BCD		'147				✔							
Cascadable Octal		'148				✔							

✔ Product available in technology indicated
+ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Decoders/Demultiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Dual 2-to-4		'239				✔							
Dual 2-to-4		'139	✔			✔	✔						+
		'11139						✔	✔				
	OC	'156	✔										
3-to-8		'138	✔	✔	✔	✔	✔					✔	+
		'11138						✔	✔				
		'238					✔						
		'11238						✔	✔				
3-to-8 With Address Registers		'131		✔									
		'137	✔			✔							+
3-to-8 With Address Latches		'237				✔							
4-to-10 BCD-to-Decimal		'42				✔							
4-to-16		'154				✔							
4-to-16 With Address Latches		'4514				✔							
		'4515				✔							
Dual 2-to-4 for Battery Backed-Up Memories		'2414								✔			

Shifters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Shifter	3S	'350			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

DESCRIPTION								TYPE	TECHNOLOGY							
INPUT	P=Q	$\overline{P=Q}$	P>Q	$\overline{P>Q}$	P<Q	OUTPUT	ENABLE		ALS	AS	F	HC	HCT	AC	ACT	BCT
8-Bit With 20-kΩ Pullup	Yes	No	No	No	No	OC	Yes	'518	✔							
	No	Yes	No	No	No	2S	Yes	'520	✔		✔					
								'11520						✔	✔	
	No	Yes	No	No	No	OC	Yes	'522	✔							
	No	Yes	No	Yes	No	2S	No	'682				✔				
8-Bit Standard	Yes	No	No	No	No	OC	Yes	'519	✔							
	No	Yes	No	No	No	2S	Yes	'521	✔		✔					
								'11521						✔	✔	
	No	Yes	No	Yes	No	2S	No	'684				✔				
	No	Yes	No	No	No	2S	Yes	'688	✔			✔				
8-Bit Latched P	No	No	Yes	No	Yes	2S	Yes	'885		✔						
8-Bit Latched P and Q	Yes	No	Yes	No	Yes	L	Yes	'866		✔						

Address Comparators

DESCRIPTION	OUTPUT ENABLE	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16-Bit to 4-Bit	Yes	'677	✔								
12-Bit to 4-Bit	Yes	'679	✔								

Parity Generators/Checkers

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Odd/Even	9	'280	✔	✔	✔	✔					
		'11280						✔	✔		
		'286		✔							
		'11286						✔	✔		

✔ Product available in technology indicated
+ New product planned in technology indicated

BUS SWITCHES AND 5-V/3-V VOLTAGE TRANSLATORS

Crossbar Technology (CBT)

DESCRIPTION	TYPE	TECHNOLOGY
		CBT
Dual 4-Bit With '244 Pinout	'3244	✔
8-Bit With '245 Pinout	'3245	✔
10-Bit Bus Exchanger	'3383	✔
Dual 5-Bit	'3384	✔
10-Bit With Precharged Outputs for Live Insertion	'6800	+
18-Bit Bus Exchanger	'16209	+
24-Bit Bus Exchanger	'16212	+
12-Bit 3-to-1 Bus Select	'16214	+

ARITHMETIC CIRCUITS

Parallel Binary Adders

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit		'283			✔	✔					

Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Arithmetic Logic Units: Function Generator		'181		✔							
		'11181							✔		
		'881		✔							
4-Bit Arithmetic Logic Units With Ripple Carry		'382			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

FIFO MEMORIES

First-In, First-Out Memories (FIFOs)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY										
SIZE	TYPE†			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16 Words × 4 Bits	U	3S	'232B			✔								
16 Words × 5 Bits	U	3S	'225		✔									
			'229B			✔								
			'233B			✔								
32 Words × 9 Bits	B	3S	'2238			✔								
64 Words × 4 Bits	U	3S	'234			✔								
			'236			✔								
64 Words × 5 Bits	U	3S	'235			✔								
64 Words × 8 Bits	U	3S	'2232A			✔								
64 Words × 9 Bits	U	3S	'2233A			✔								
64 Words × 18 Bits	U, C	3S	'7813									✔		
	U	3S	'7814									✔		
64 Words × 36 Bits	B, C	3S	'3612											✔
			'3614											✔
	U, C	3S	'3611											+
			'3613											✔
Dual 64 × 1	C	3S	'2226									✔		
			'2227									✔		
Dual 256 × 1	C	3S	'2228									✔		
			'2229									✔		
256 Words × 9 Bits	U	3S	'7200									✔		
256 Words × 18 Bits	U, C	3S	'7805									✔		
	U	3S	'7806									✔		
256 × 36 × 2 Bits	B, C	3S	'3622									+		
512 Words × 9 Bits	U	3S	'7201									✔		
	U, S	3S	'72211									✔		
512 Words × 18 Bits	U, C	3S	'7803									✔		
	U	3S	'7804									✔		
	B, C	3S	'7819											✔
	B	3S	'7820											✔
512 Words × 32 Bits	B, C	3S	'3638									✔		
512 Words × 36 Bits	U, C	3S	'3631									+		
	B, C	3S	'3632									✔		

†U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
+ New product planned in technology indicated

FIFO MEMORIES

First-In, First-Out Memories (FIFOs) (Continued)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY										
SIZE	TYPE†			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
1K Words × 9 Bits	B	3S	'2235									✔		
			'2236									✔		
	U	3S	'7202									✔		
	U, S	3S	'72221									✔		
1K Words × 18 Bits	U, C	3S	'7801									✔		
			'7811									✔		
			'7881									+		
	U	3S	'7802									✔		
1K Words × 36 Bits	U, C	3S	'3641									+		
1K × 36 × 2 Bits	B, C	3S	'3642									+		
2K Words × 9 Bits	U, C	3S	'7807									✔		
	U	3S	'7203									✔		
			'7808									✔		
	U, S	3S	'72231									✔		
2K Words × 18 Bits	U, C	3S	'7882									+		
2K Words × 36 Bits	U, C	3S	'3651									+		
4K Words × 9 Bits	U	3S	'7204									✔		
	U, S	3S	'72241									✔		
4K Words × 18 Bits	U, C	3S	'7884									+		

† U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
\+ New product planned in technology indicated

CLOCK-DISTRIBUTION CIRCUITS

Clock-Distribution Circuits (CDC)

DESCRIPTION	TYPE	TECHNOLOGY								
		ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
3.3-V Hex Inverting Clock Drivers/Buffers	'203						✔			
Hex Inverting Clock Drivers/Buffers	'204						✔			
Dual 1-to-4 Clock Drivers/Buffers	'208							✔		
	'209						✔			
Octal Divide-by-2 Clock Drivers (6 inverting, 2 noninverting)	'303		✔							
Octal Divide-by-2 Clock Drivers (8 noninverting)	'305		✔							
Octal Divide-by-2 Clock Drivers (4 inverting, 4 noninverting)	'304		✔							
1-to-6 Clock Drivers	'328									✔
	'328A									+
	'329									✔
	'329A									✔
1-to-6 Clock Drivers With Output Enable	'391									✔
	'392									✔
1-to-8 Clock Drivers	'340									✔
	'341									✔
1-to-8, Divide-by-2 Clock Drivers	'337									✔
	'339									✔
Phase-Locked Loop 1-to-12 Clock Drivers	'582									+
	'586									+
	'2586									+

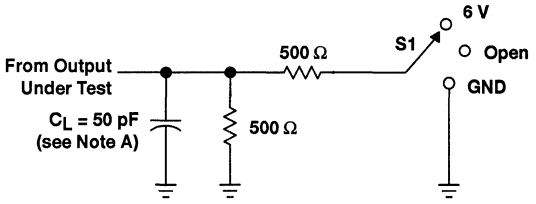
✔ Product available in technology indicated
\+ New product planned in technology indicated

ECL TRANSLATORS

ECL-to-TTL or TTL-to-ECL Translators

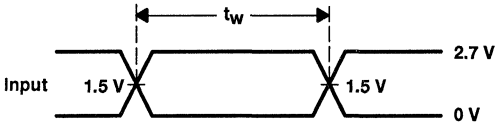
DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE
Octal Bus Driver, Inverting	ECL-to-TTL	3S	10KHT5540
	TTL-to-ECL	OE	10KHT5542
Octal Bus Driver, Noninverting	ECL-to-TTL	3S	10KHT5541
	TTL-to-ECL	OE	10KHT5543
			100KT5543
Octal D-Type Latch, True	ECL-to-TTL	3S	10KHT5573
			100KT5573
Octal D-Type Flip-Flop, True	ECL-to-TTL	3S	10KHT5574
	TTL-to-ECL	OE	10KHT5578
			100KT5578

LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR LVC, LVT, LVTZ, AND ALVC DEVICES

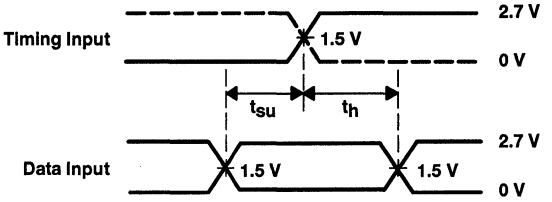


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

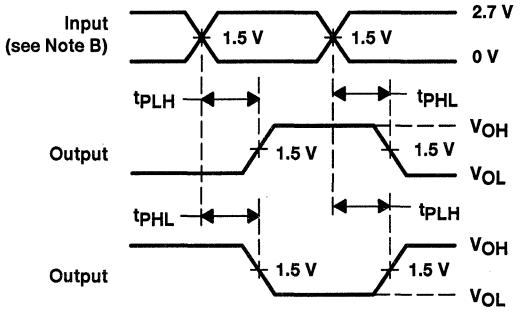
LOAD CIRCUIT FOR OUTPUTS



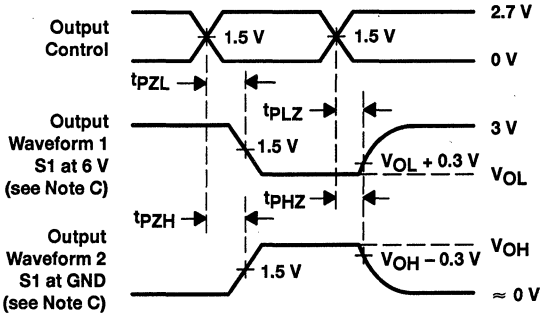
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



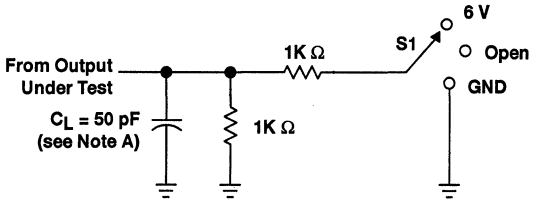
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

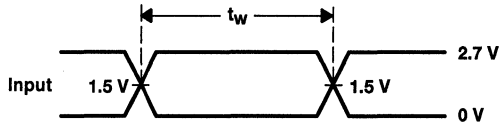
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR LV MSI AND OCTAL DEVICES

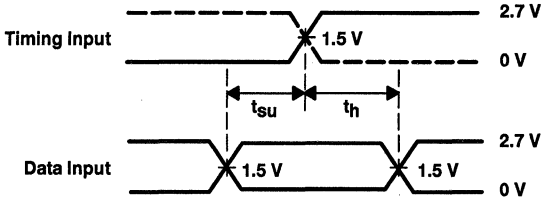


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

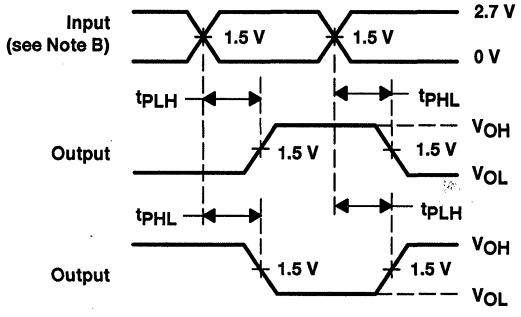
LOAD CIRCUIT FOR OUTPUTS



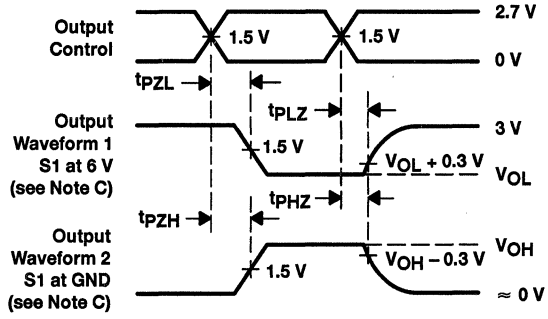
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



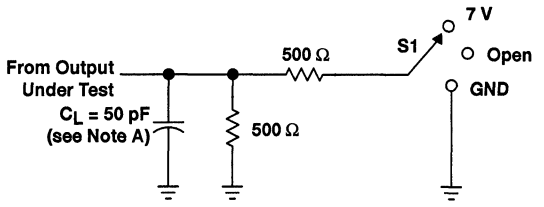
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

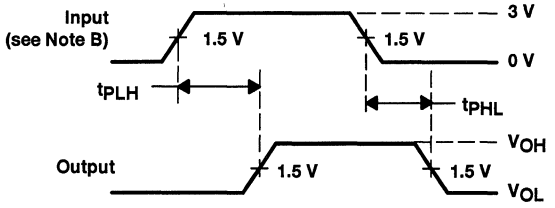
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR CBT DEVICES

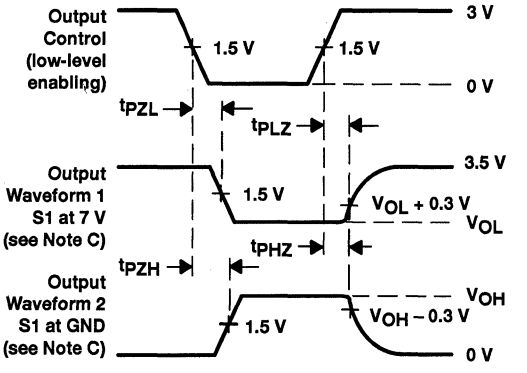


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



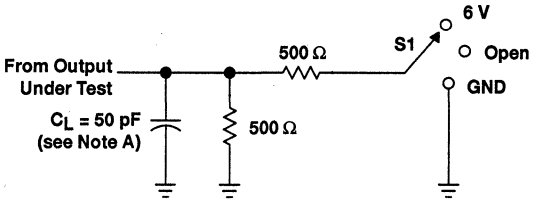
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



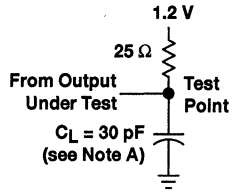
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS FOR GTL DEVICES

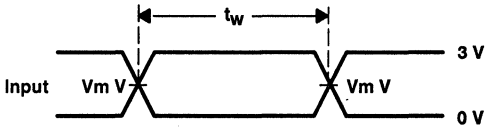


LOAD CIRCUIT FOR A OUTPUTS

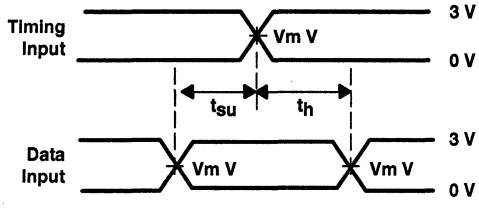


LOAD CIRCUIT FOR B OUTPUTS

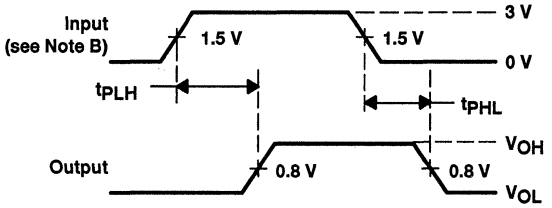
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



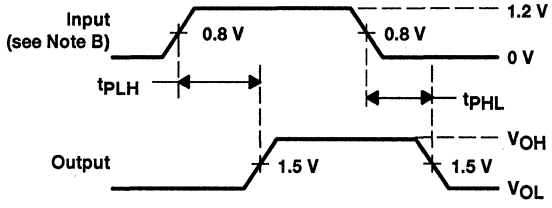
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



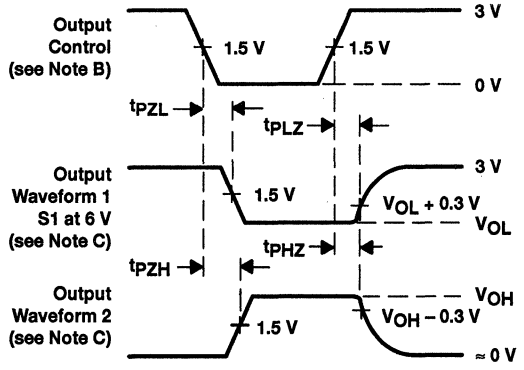
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

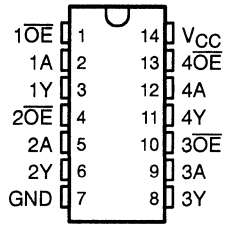
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

LVT OCTALS

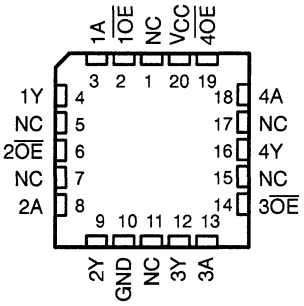
Features	Benefits
• State-of-the-art 0.8-μ EPIC-IIB™ BiCMOS process	• Propagation delays as fast as 4 ns maximum for improved performance
• No input-diode clamp to V_{CC}	• Interfaces directly to industry standard buses and 5-V integrated circuits
• Fully compatible (input and output) with 5-V systems	• Supports live insertion
• –32-mA/64-mA drive current	• Drives large loads, buses, or memory arrays
• Low standby current (190 μA)	• Extends battery life
• Bus-hold cell on data inputs and I/O pins	• Eliminates passive pullup resistors on local buses
• SOIC, EIAJ SSOP, and TSSOP packaging	• Saves board space and weight; TSSOP compatible with PCMCIA standards
• TI has established two worldwide alternate sources	• Standardization that comes from a common product approach

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

SN54LVT125 . . . J PACKAGE
SN74LVT125 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($\overline{OE}$) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

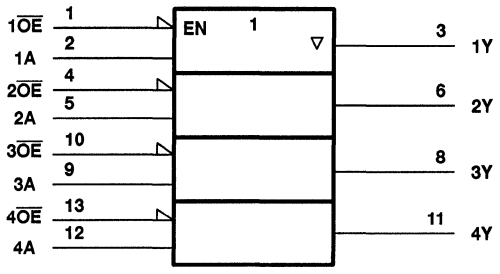
The SN74LVT125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

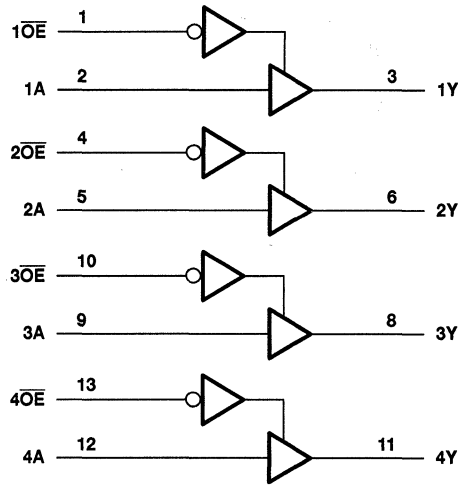
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT125 ..... 96 mA
SN74LVT125 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT125 ..... 48 mA
SN74LVT125 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT125		SN74LVT125		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT125			SN74LVT125			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		4.5	7		4.5	7	
			Outputs disabled		0.12	0.19		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

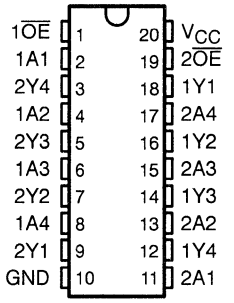
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT125				SN74LVT125					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	4.2		4.7	1	2.7	4		4.5	ns
t_{PHL}			1	4.1		5.1	1	2.9	3.9		4.9	
t_{PZH}	$\overline{OE}$	Y	1	4.9		6.2	1	3.4	4.7		6	ns
t_{PZL}			1.1	4.9		6.7	1.1	3.4	4.7		6.5	
t_{PHZ}	$\overline{OE}$	Y	1.8	5.3		5.9	1.8	3.7	5.1		5.7	ns
t_{PLZ}			1.3	4.7		4.2	1.3	2.6	4.5		4	

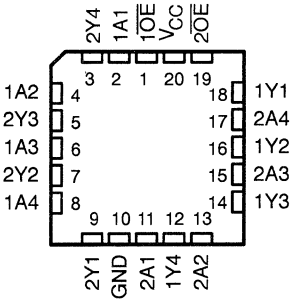
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVT240 . . . J PACKAGE
SN74LVT240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT240 is organized as two 4-bit buffer/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

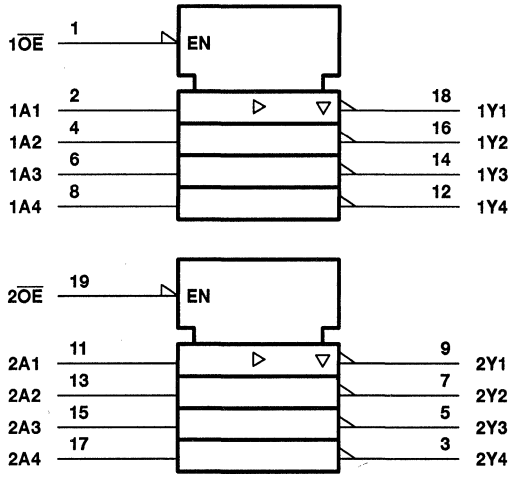
The SN74LVT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

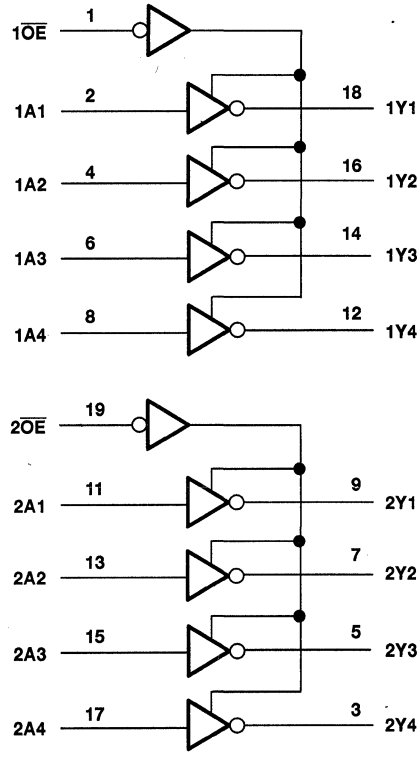
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT240 ..... 96 mA
SN74LVT240 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT240 ..... 48 mA
SN74LVT240 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT240		SN74LVT240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT240			SN74LVT240			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = − 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V	A inputs	−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−5			−5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		8.6	12		8.6	12	
			Outputs disabled		0.12	0.19		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

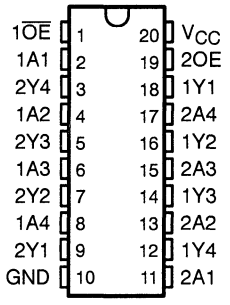
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT240				SN74LVT240					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	4.2		5.2	1	2.9	4.1		5.2	ns
t_{PHL}			1.3	3.7		4.1	1.3	2.5	3.5		4	
t_{PZH}	$\overline{OE}$	Y	1.2	4.7		5.7	1.2	3.2	4.6		5.6	ns
t_{PZL}			1.5	4.8		5.9	1.4	3.5	4.7		5.8	
t_{PHZ}	$\overline{OE}$	Y	2	5.3		5.7	2	3.6	5.2		5.5	ns
t_{PLZ}			1.9	4.6		4.6	1.9	3.2	4.4		4.4	

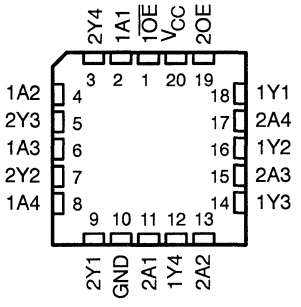
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVT241 . . . J PACKAGE
SN74LVT241 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT241 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT241 is organized as two 4-bit line drivers with separate output-enable ($1\overline{OE}$, 2OE) inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT241 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT241 is characterized for operation from –40°C to 85°C.

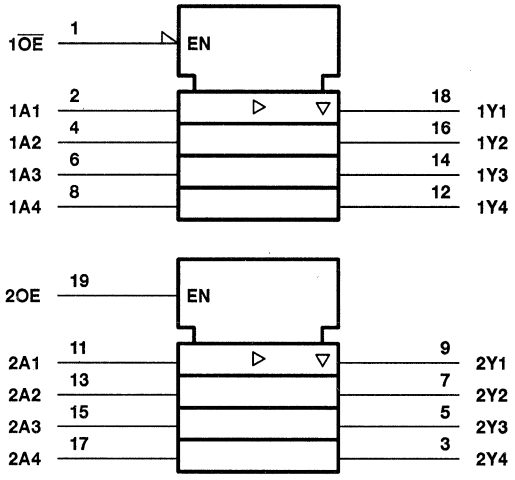
PRODUCT PREVIEW

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

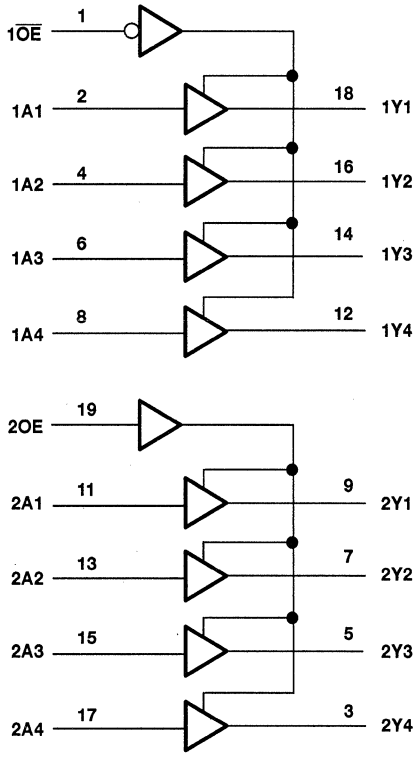
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT241 ..... 96 mA
SN74LVT241 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT241 ..... 48 mA
SN74LVT241 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT241		SN74LVT241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

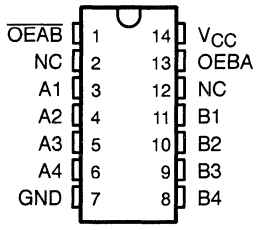
PARAMETER	TEST CONDITIONS			SN54LVT241			SN74LVT241			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.19	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

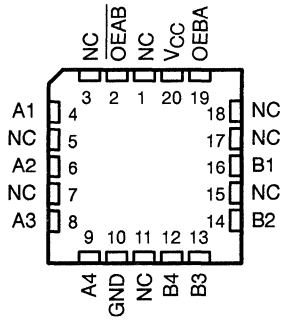
PRODUCT PREVIEW

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVT243 . . . J PACKAGE
SN74LVT243 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVT243 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT243 is designed for asynchronous communications between data buses. The control-function implementation allows for maximum flexibility in timing. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable (OEBA and $\overline{OEAB}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous enabling of OEBA and $\overline{OEAB}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (eight in all) remain at their states. The 4-bit codes appearing on the two sets of buses will be identical for the 'LVT243.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT243 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

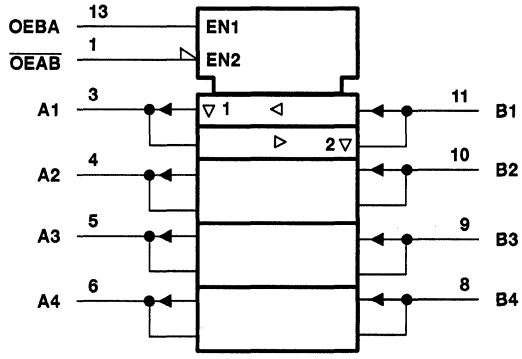
The SN54LVT243 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT243 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

FUNCTION TABLE

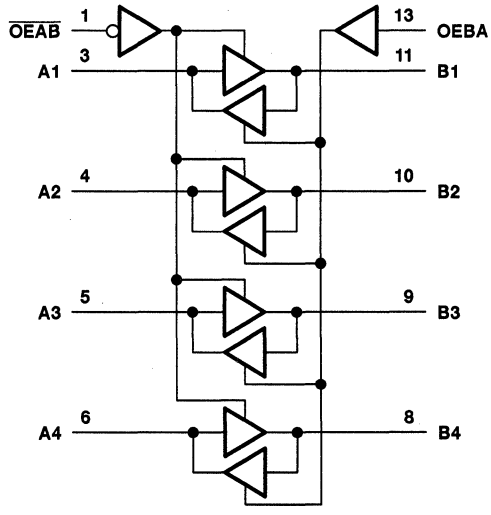
INPUTS		FUNCTION
$\overline{OEAB}$	OEBA	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT243 ..... 96 mA
SN74LVT243 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT243 ..... 48 mA
SN74LVT243 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT243		SN74LVT243		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

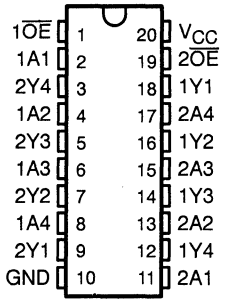
PARAMETER	TEST CONDITIONS			SN54LVT243			SN74LVT243			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V	Control pins			10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			100			20	
		V_I = V_{CC}	A or B ports§			5			5	
		V_I = 0	A or B ports§			–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V	A or B ports	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.5		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0									pF
C_{io}	V_O = 3 V or 0									pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

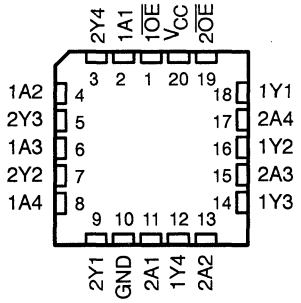
PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flatpacks (W), and Ceramic DIPS (J)

SN54LVT244 . . . J OR W PACKAGE
SN74LVT244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT244 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

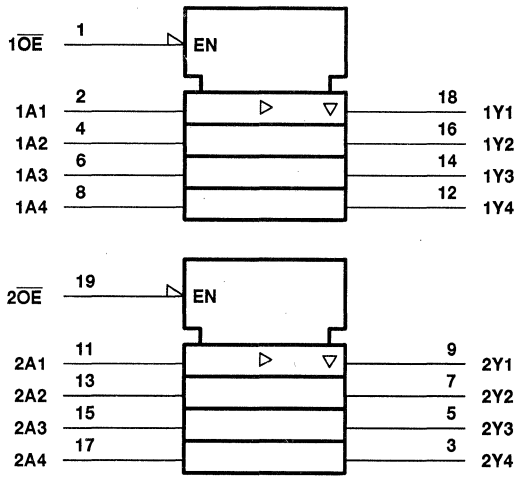
The SN74LVT244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

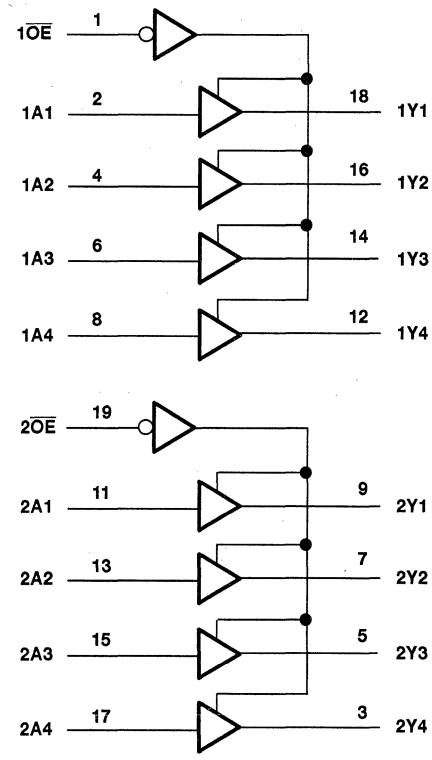
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT244 ..... 96 mA
SN74LVT244 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT244 ..... 48 mA
SN74LVT244 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT244		SN74LVT244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT244			SN74LVT244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				50			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V,	V_I = 0.8 V	A inputs	75			75			µA
	V_{CC} = 3 V,	V_I = 2 V	A inputs	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.39		0.12	0.19	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.39		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

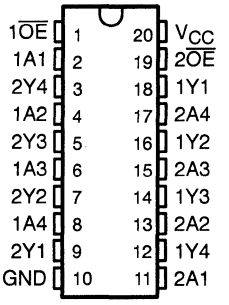
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT244				SN74LVT244					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.7		5.2	1	2.5	4.3		5	ns
t_{PHL}			0.5	4.4		5.4	1	2.5	4.2		5.2	
t_{PZH}	$\overline{OE}$	Y	0.8	5.4		6.5	1	2.7	5.2		6.3	ns
t_{PZL}			0.8	5.4		7.6	1.1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	6.2		6.9	2.1	3.9	5.6		6.3	ns
t_{PLZ}			1.2	5.5		6	1.8	3.2	5.1		5.6	

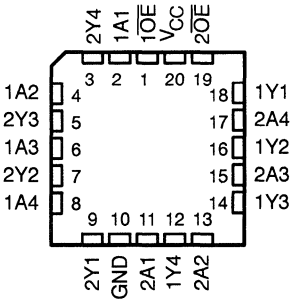
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVT244A . . . J PACKAGE
SN74LVT244A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT244A . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

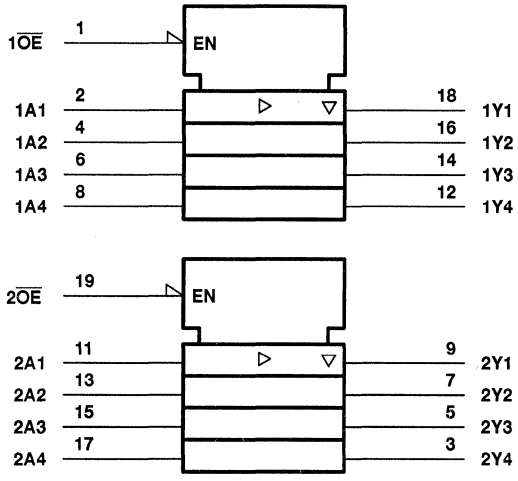
The SN74LVT244A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

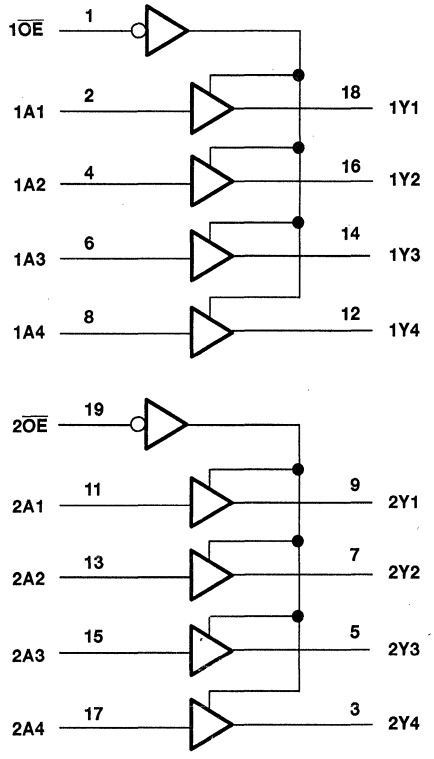
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT244A ..... 96 mA
SN74LVT244A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT244A ..... 48 mA
SN74LVT244A ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT244A		SN74LVT244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT244A			SN74LVT244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.19	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

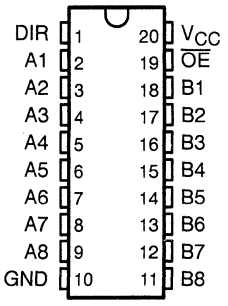
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT244A				SN74LVT244A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.7		5.2	1	2.5	4.1		5	ns
t_{PHL}			0.5	4.4		5.4	1	2.5	4.1		5.2	
t_{PZH}	$\overline{OE}$	Y	0.8	5.4		6.5	1	2.7	5.2		6.3	ns
t_{PZL}			0.8	5.4		7.6	1.1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	6.2		6.9	1.9	3.9	5.6		6.3	ns
t_{PLZ}			1.2	5.5		6	1.8	3.2	5.1		5.6	

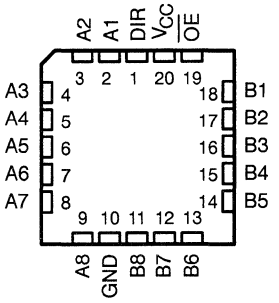
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Ceramic Chip Carriers (FK) and DIPs (J)**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN54LVT245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

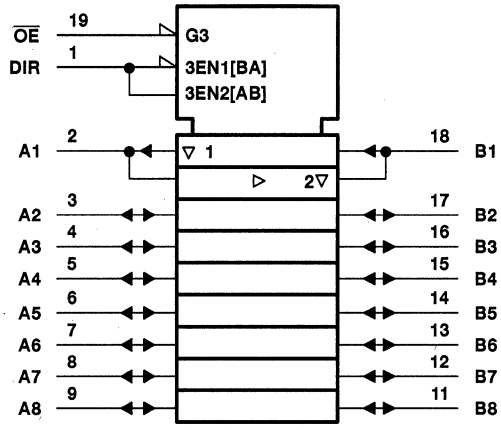
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVT245 is characterized for operation over the full military temperature range of −55°C to 125°C.

FUNCTION TABLE

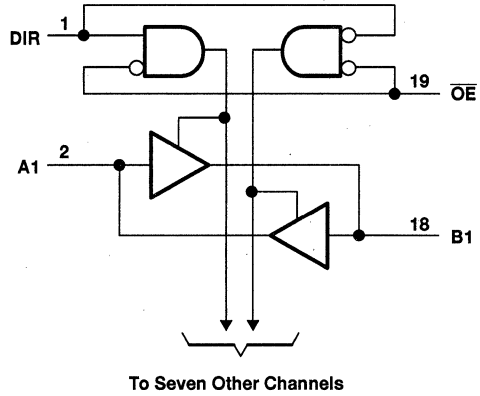
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 96 mA
Current into any output in the high state, I_O (see Note 2) ..... 48 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		−55	125	°C

NOTE 3: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 24 mA				0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4	
		I_{OL} = 32 mA				0.5	
		I_{OL} = 48 mA				0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			100	
		V_I = V_{CC}				5	
		V_I = 0				–10	
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			µA
		V_I = 2 V		–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.39	mA
			Outputs low		8.8	14	
			Outputs disabled		0.13	0.39	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.3	mA
C_i	V_I = 3 V or 0				4		pF
C_{io}	V_O = 3 V or 0				10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

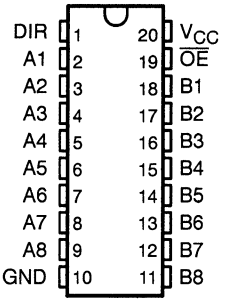
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	4.4		5.2	ns
t_{PHL}			0.5	4.2		4.8	
t_{PZH}	$\overline{OE}$	A or B	0.8	5.9		7.3	ns
t_{PZL}			1	5.9		7.2	
t_{PHZ}	$\overline{OE}$	A or B	1.5	6.5		7.2	ns
t_{PLZ}			1.5	6.1		6.5	

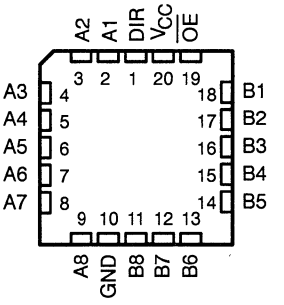
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVT245A . . . J PACKAGE
SN74LVT245A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT245A . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

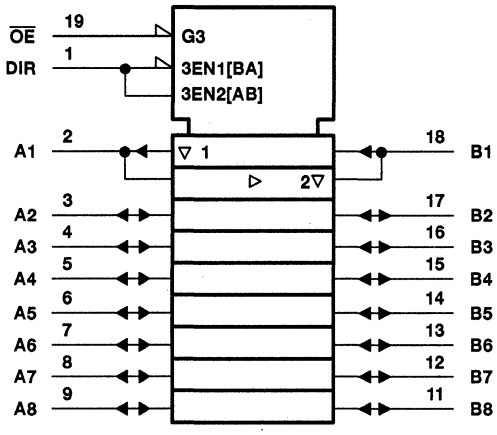
The SN74LVT245A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT245A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT245A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

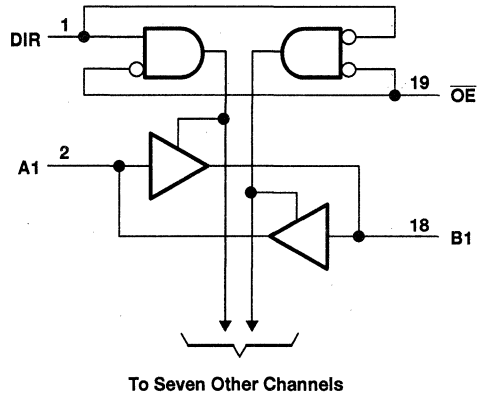
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT245A ..... 96 mA
SN74LVT245A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT245A ..... 48 mA
SN74LVT245A ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT245A		SN74LVT245A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT245A			SN74LVT245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			100			20	
		V_I = V_{CC}				5			5	
		V_I = 0				–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.5		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				10			10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

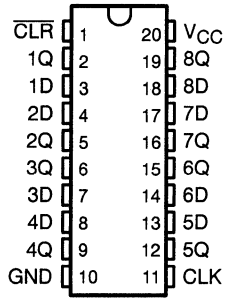
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT245A				SN74LVT245A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4.6		5.3	1	2.5	4		5.2	ns
t_{PHL}			1	4.1		5.7	1	2.5	4		5.5	
t_{PZH}	$\overline{OE}$	A or B	1.1	6.1		7.2	1.1	3.3	5.9		7.1	ns
t_{PZL}			1.5	6.6		8	1.5	3.8	6.5		7.9	
t_{PHZ}	$\overline{OE}$	A or B	2.2	6.2		7	2.2	4.3	5.9		6.5	ns
t_{PLZ}			2	6.3		5.9	2	3.9	5.5		5.6	

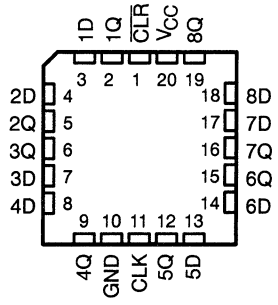
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Buffered Clock and Direct Clear Inputs**
- **Individual Data Input to Each Flip-Flop**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVT273 . . . J PACKAGE
SN74LVT273 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT273 . . . FK PACKAGE
(TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

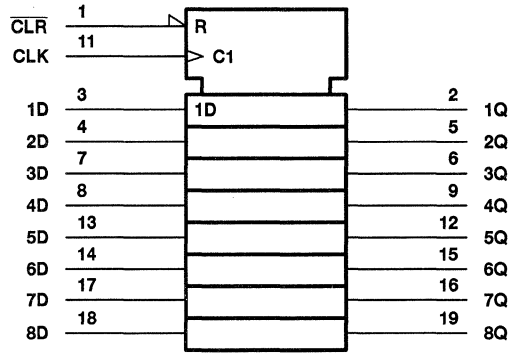
The SN74LVT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

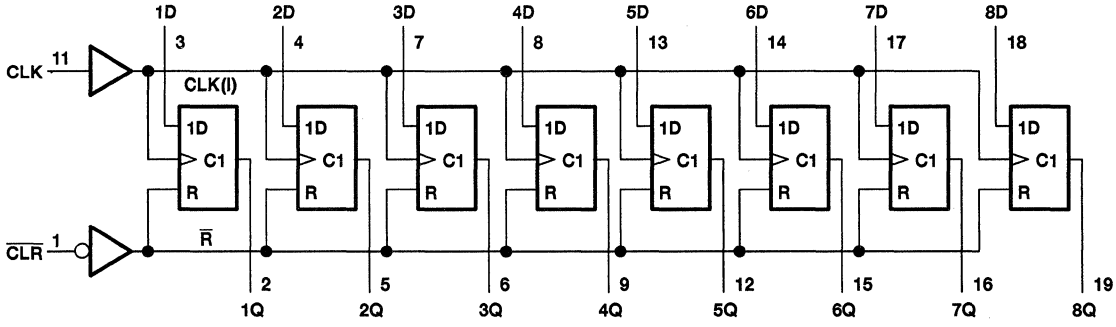
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT273 ..... 96 mA
SN74LVT273 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT273 ..... 48 mA
SN74LVT273 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

		SN54LVT273		SN74LVT273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT273			SN74LVT273			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				–5			–5	
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		8.6	12		8.6	12	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0							4		pF
C_o	V_O = 3 V or 0							8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT273				SN74LVT273				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						0	150			MHz
t_w	Pulse duration						3.3		3.3		ns
t_{su}	Setup time before CLK↑	Data high or low					2.3		2.7		ns
		$\overline{CLR}$ high					2.7		3.2		
t_h	Hold time after CLK↑	Data high or low					0		0		ns

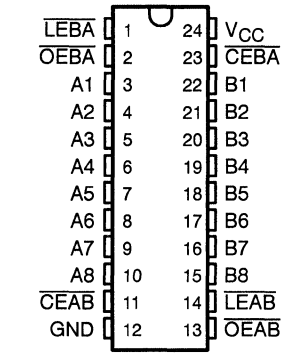
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT273				SN74LVT273					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}							150					MHz
t_{PLH}	CLK	Any Q					1.7	3.5	5.5		6.3	ns
t_{PHL}							1.9	3.5	5.5		5.9	
t_{PHL}	$\overline{CLR}$	Any Q					1.3	3.2	5.1		6.2	ns

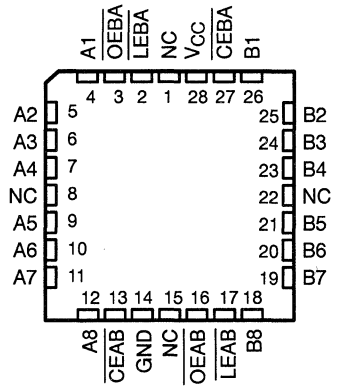
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (JT)**

SN54LVT543 . . . JT PACKAGE
SN74LVT543 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

description (continued)

The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

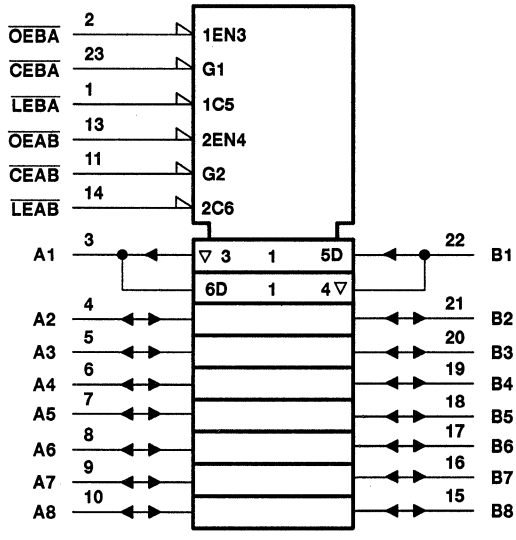
The SN54LVT543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

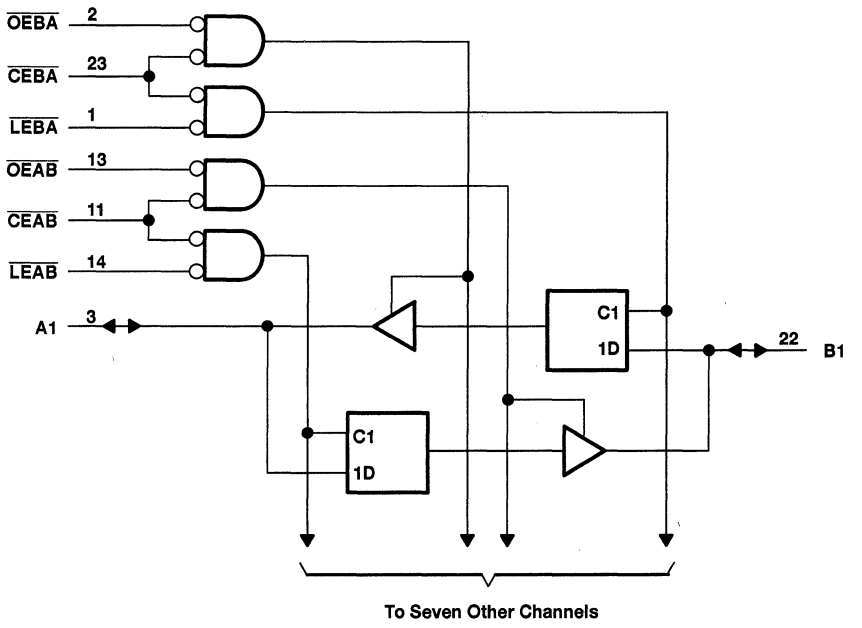
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT543 ..... 96 mA
SN74LVT543 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT543 ..... 48 mA
SN74LVT543 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT543		SN74LVT543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT543			SN74LVT543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				−10			−10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.8	12		8.8	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54LVT543				SN74LVT543				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$	High	0		0		0		0		ns
			Low	0.8		1.1		0.8		1.1		
		Data before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$	High	0		0		0		0		
			Low	0.9		1.2		0.9		1.2		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$		1.7		1.7		1.7		1.7		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$		1.8		1.8		1.8		1.8		

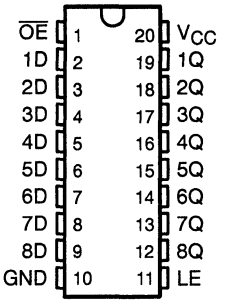
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT543				SN74LVT543					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4.9		5.7	1	2.9	4.7		5.5	ns
t_{PHL}			1	4.8		6	1	3.3	4.6		5.8	
t_{PLH}	$\overline{LE}$	A or B	1	6.1		7.5	1	4	5.9		7.3	ns
t_{PHL}			1	5.9		7.5	1	4.1	5.7		7.3	
t_{PZH}	$\overline{OE}$	A or B	1	6		7.8	1	4.1	5.8		7.6	ns
t_{PZL}			1.1	6.6		8.4	1.1	4.5	6.4		8.2	
t_{PHZ}	$\overline{OE}$	A or B	2.4	6.7		7.3	2.4	4.8	6.5		7.1	ns
t_{PLZ}			2	6		6.1	2	4	5.8		5.9	
t_{PZH}	$\overline{CE}$	A or B	1	6.2		7.8	1	4.2	6		7.6	ns
t_{PZL}			1.4	6.9		8.5	1.4	4.7	6.7		8.3	
t_{PHZ}	$\overline{CE}$	A or B	2.3	6.6		7.3	2.3	4.7	6.4		7.1	ns
t_{PLZ}			2	5.6		5.8	2	3.8	5.4		5.6	

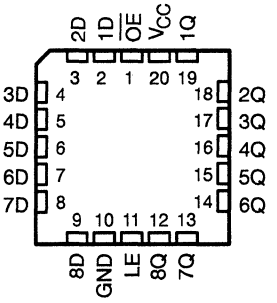
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flatpacks (W), and DIPS (J)

SN54LVT573 . . . J OR W PACKAGE
SN74LVT573 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT573 . . . FK PACKAGE
(TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

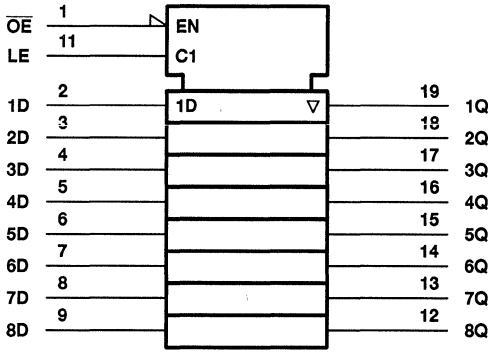
The SN74LVT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

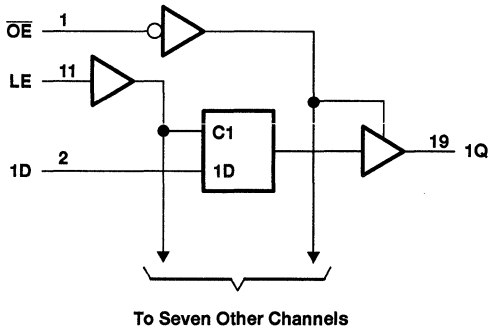
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT573 ..... 96 mA
SN74LVT573 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT573 ..... 48 mA
SN74LVT573 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT573		SN74LVT573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT573			SN74LVT573			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				50			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data inputs			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
I_{IH}	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.39		0.13	0.19	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.13	0.39		0.13	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT573				SN74LVT573				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High or low	1		0.9		0.7		0.6		ns
t_h	Hold time, data after LE↓	High or low	1.8		2		1.6		1.8		ns

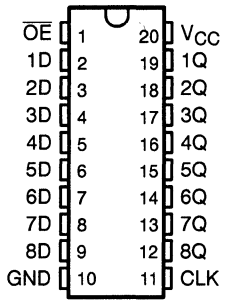
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT573				SN74LVT573					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q	0.5	4.7		4.9	1	2.5	4.2		4.7	ns
t_{PHL}			0.5	4.9		5.4	1	2.7	4.3		5.2	
t_{PLH}	LE	Q	1	6		6.9	1.6	3.5	5.6		6.3	ns
t_{PHL}			1.4	6.9		7.6	2.5	4.3	6.5		7.2	
t_{PZH}	$\overline{OE}$	Q	0.5	5.3		6.4	1	2.8	5.1		6.2	ns
t_{PZL}			0.7	5.7		7.2	1.3	3.3	5.5		6.6	
t_{PHZ}	$\overline{OE}$	Q	1.2	5.9		6.9	2	3.7	5.7		6.7	ns
t_{PLZ}			1	5.4		5.5	1.5	3	4.6		5.1	

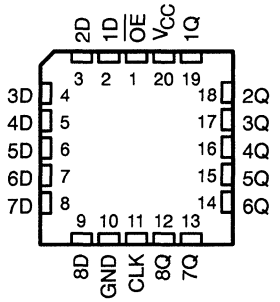
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flatpacks (W), and DIPS (J)

SN54LVT574 . . . J OR W PACKAGE
SN74LVT574 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT574 . . . FK PACKAGE
(TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{OE}$) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

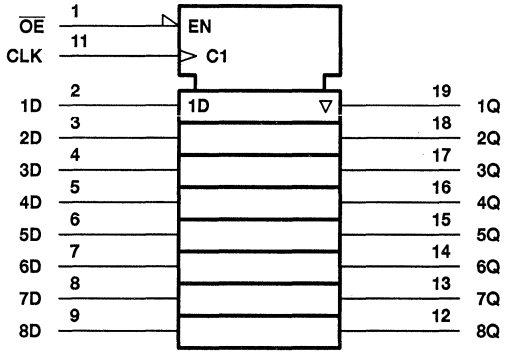
The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT574 is characterized for operation from –40°C to 85°C.

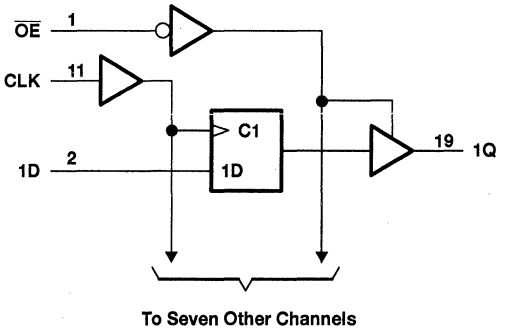
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT574 ..... 96 mA
SN74LVT574 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT574 ..... 48 mA
SN74LVT574 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT574		SN74LVT574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT574			SN74LVT574			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = −24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				50			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data inputs			1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.39		0.13	0.19	mA
			Outputs low		8.7	14		8.7	12	
			Outputs disabled		0.13	0.39		0.13	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT574				SN74LVT574				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	High or low	2		2.4		2		2.4		ns
t_h	Hold time, data after CLK↑	High or low	0.9		0.9		0.3		0		ns

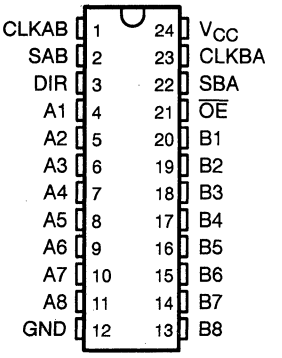
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT574				SN74LVT574					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	CLK	Q	1	5.9		6.6	1.7	3.6	5.4		6.2	ns
t_{PHL}			1	6.1		6.8	2.4	4.3	5.9		6.6	
t_{PZH}	$\overline{OE}$	Q	0.5	5.9		7.1	1	2.9	4.8		5.9	ns
t_{PZL}			0.5	5.3		6.4	1.3	3.4	5.1		6.2	
t_{PHZ}	$\overline{OE}$	Q	0.7	5.9		6.6	1.9	4	5.5		5.9	ns
t_{PLZ}			0.5	5.1		5.1	1.7	3.2	4.5		4.5	

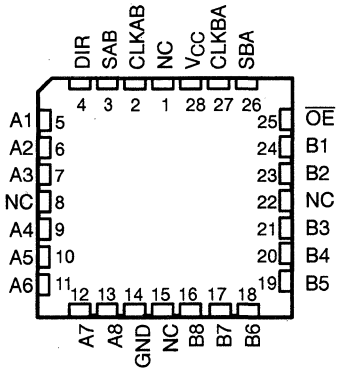
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Flatpacks (W), and DIPS (JT)

SN54LVT646 . . . JT OR W PACKAGE
SN74LVT646 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

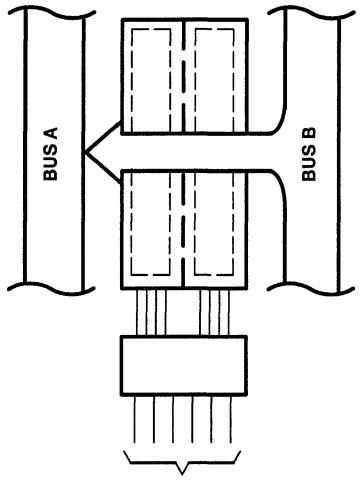
The SN74LVT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

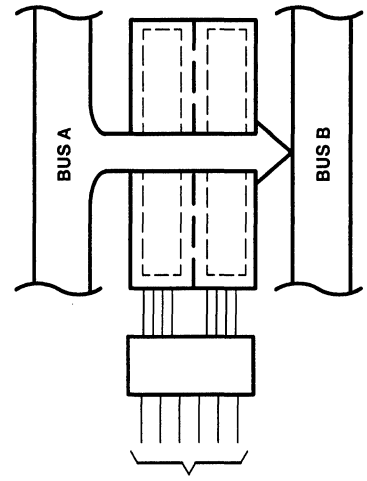
INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



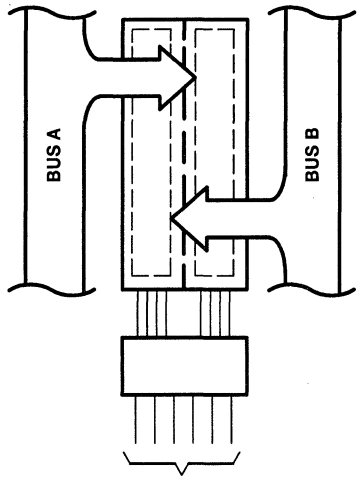
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



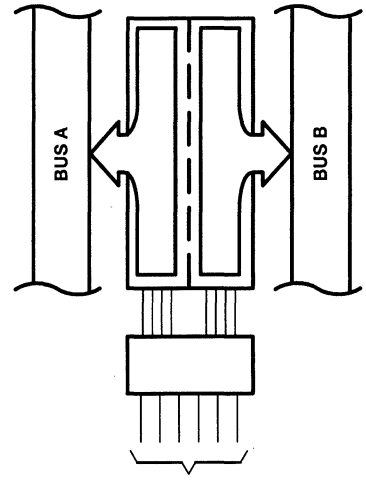
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



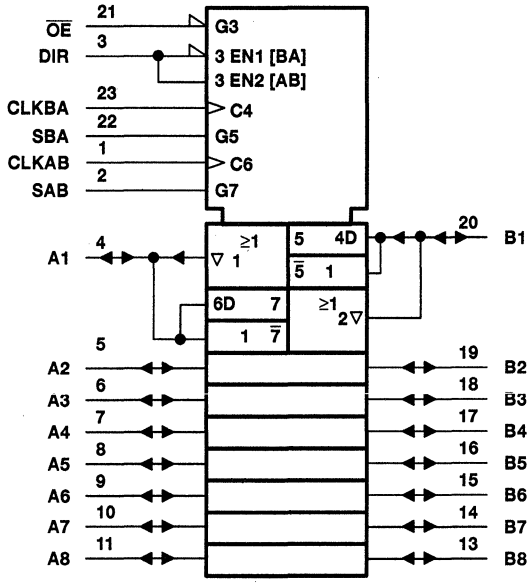
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

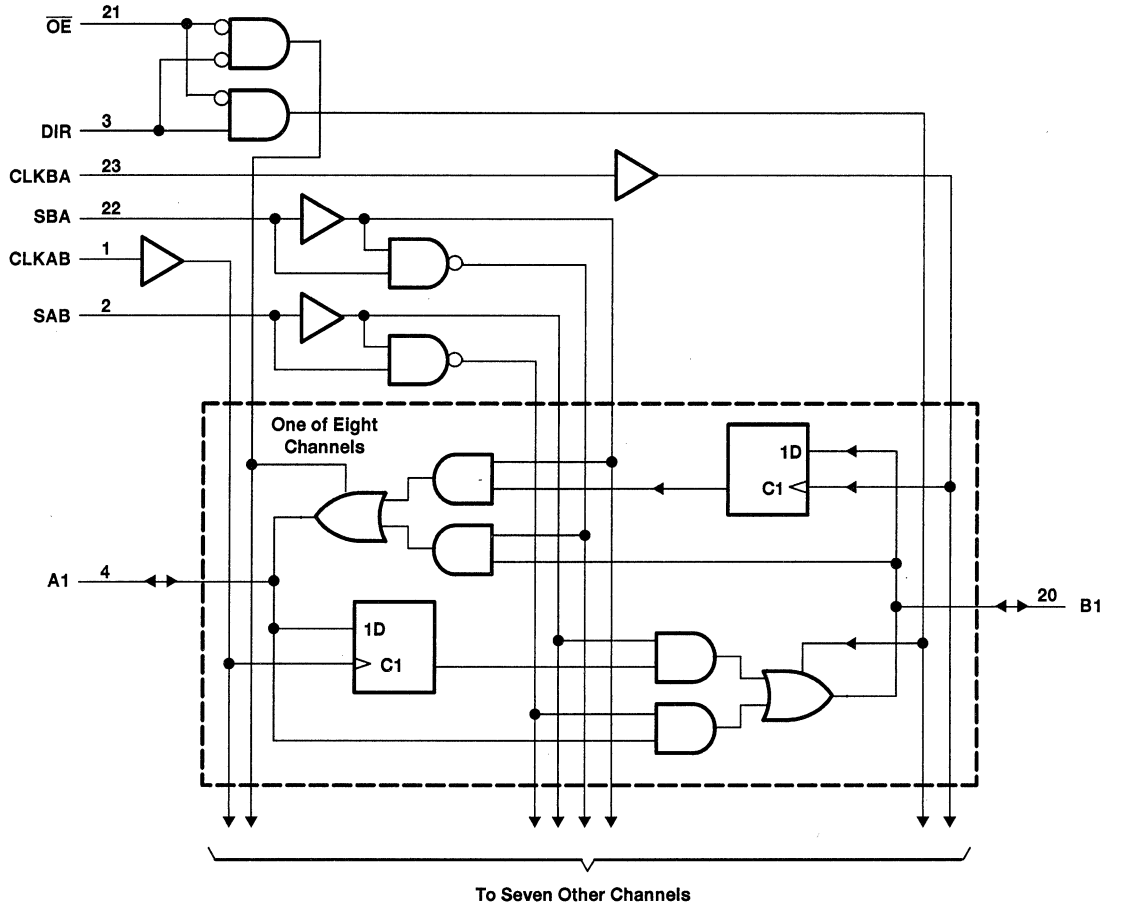
Pin numbers shown are for the DB, DW, JT, PW, and W packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT646 ..... 96 mA
SN74LVT646 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT646 ..... 48 mA
SN74LVT646 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT646		SN74LVT646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT646			SN74LVT646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			100			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.39		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.39		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT646				SN74LVT646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	High	1.5		1.5		1.3		1.3		ns
		Low	2.5		3.0		2		2.4		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑		0.9		0.9		0.4		0.4		ns

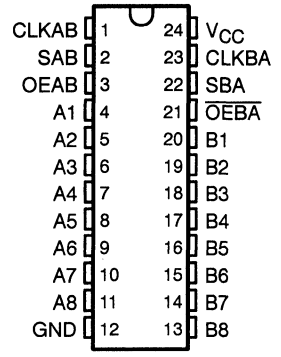
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT646				SN74LVT646					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			150				150					MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.2	5.9		6.9	1.8	3.8	5.7		6.7	ns
t_{PHL}			1.2	5.9		6.6	2.1	3.8	5.7		6.4	
t_{PLH}	A or B	B or A	0.8	4.9		5.6	1.3	2.8	4.7		5.4	ns
t_{PHL}			0.6	4.8		5.5	1	2.7	4.6		5.3	
t_{PLH}	SBA or SAB†	A or B	1	6.4		7.4	1.4	3.7	6.2		7.2	ns
t_{PHL}			1	6.4		7	1.4	3.8	6.2		6.8	
t_{PZH}	$\overline{OE}$	A or B	0.6	6		7.4	1	3	5.8		7.2	ns
t_{PZL}			0.6	6.2		7.5	1	3.2	6		7.3	
t_{PHZ}	$\overline{OE}$	A or B	1.4	6.7		7.1	2.3	4.3	6.5		6.9	ns
t_{PLZ}			1.4	6.4		6.5	2.2	3.8	5.8		5.9	
t_{PZH}	DIR	A or B	0.6	6.7		7.7	1	3.4	6.5		7.5	ns
t_{PZL}			0.8	6.5		7.3	1.2	3.4	6.3		7.1	
t_{PHZ}	DIR	A or B	0.8	7.4		8.3	1.7	4.1	7.2		8.1	ns
t_{PLZ}			1	6.7		7	1.5	3.5	5.8		6.3	

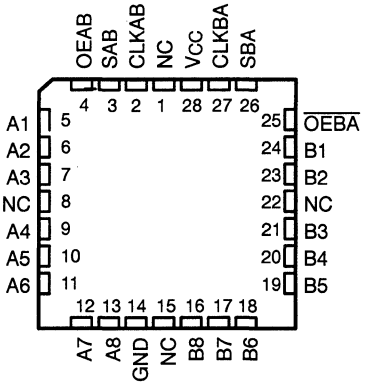
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (JT)**

SN54LVT652 . . . JT PACKAGE
SN74LVT652 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

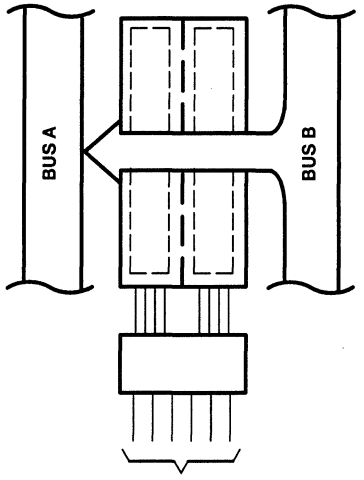
The SN74LVT652 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

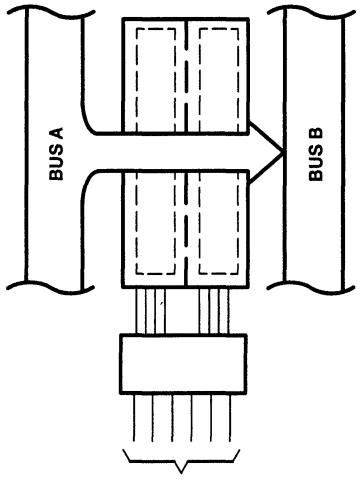
INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



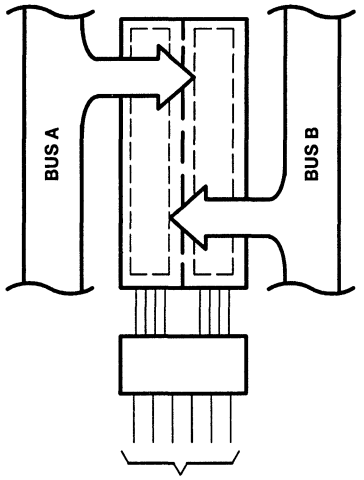
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



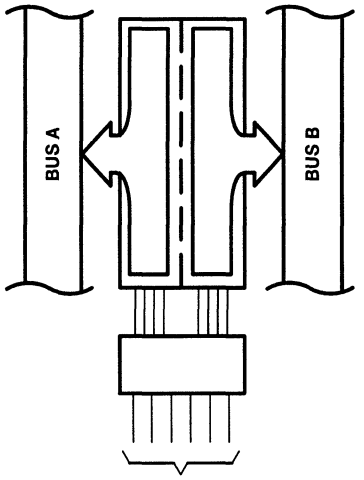
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



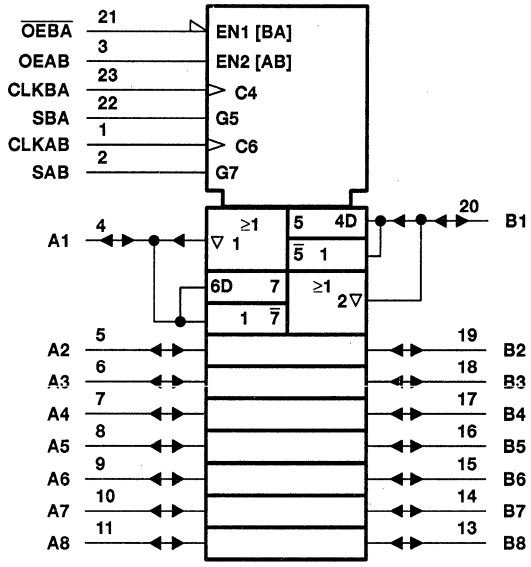
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

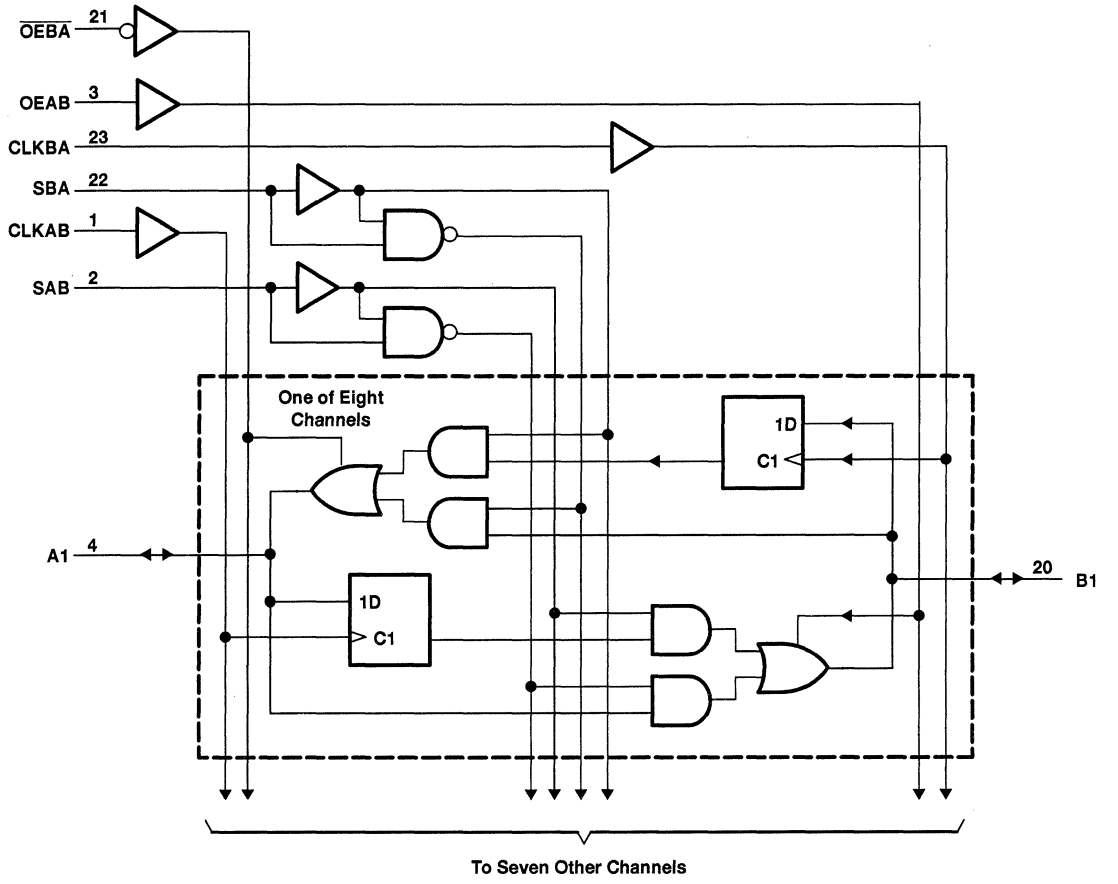
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT652 ..... 96 mA
SN74LVT652 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT652 ..... 48 mA
SN74LVT652 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT652		SN74LVT652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT652 MIN	SN54LVT652 TYP†	SN54LVT652 MAX	SN74LVT652 MIN	SN74LVT652 TYP†	SN74LVT652 MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				−10			−10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.8	12		8.8	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT652				SN74LVT652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low						3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high					1.2		1.2		ns
		Data low					2		2.5		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑						0.5		0.5		ns

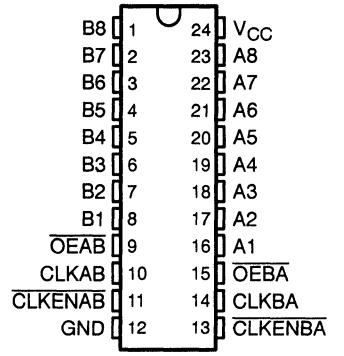
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT652				SN74LVT652					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}							150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B					1.8	3.7	6		6.9	ns
t_{PHL}							2	3.7	5.7		6.4	
t_{PLH}	A or B	B or A					1.2	2.8	4.7		5.5	ns
t_{PHL}							1	2.6	4.6		5.3	
t_{PLH}	SBA or SAB‡	A or B					1.4	3.7	6.4		7.6	ns
t_{PHL}							1.4	4	6.2		6.8	
t_{PZH}	$\overline{OEBA}$	A					1	2.9	5.8		7.2	ns
t_{PZL}							1	3	6		7.3	
t_{PHZ}	$\overline{OEBA}$	A					2.2	3.9	6.5		6.9	ns
t_{PLZ}							1.8	3.2	5.8		5.9	
t_{PZH}	OEAB	B					1	3.3	6.5		7.5	ns
t_{PZL}							1.2	3.4	6.3		7.1	
t_{PHZ}	OEAB	B					1.7	4.5	7.2		8.1	ns
t_{PLZ}							1.5	3.8	5.8		6.3	

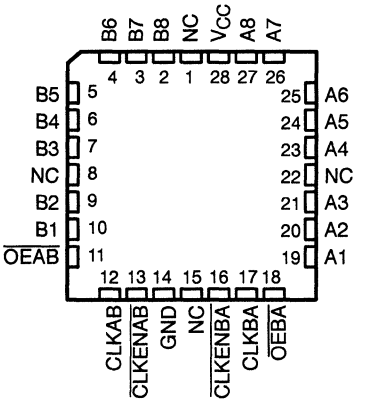
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and and Ceramic DIPs (JT)**

SN54LVT2952 . . . JT PACKAGE
SN74LVT2952 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

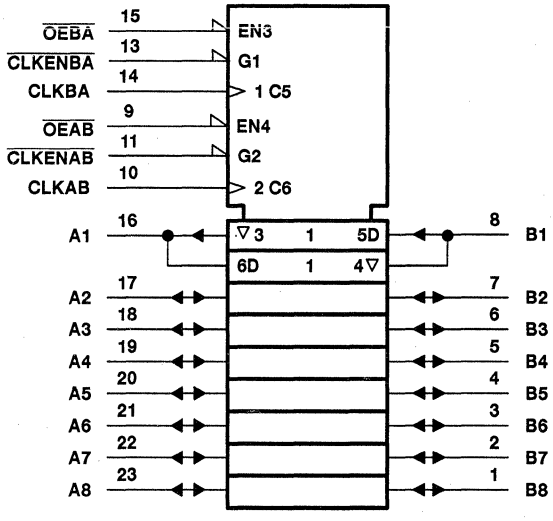
The SN54LVT2952 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT2952 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

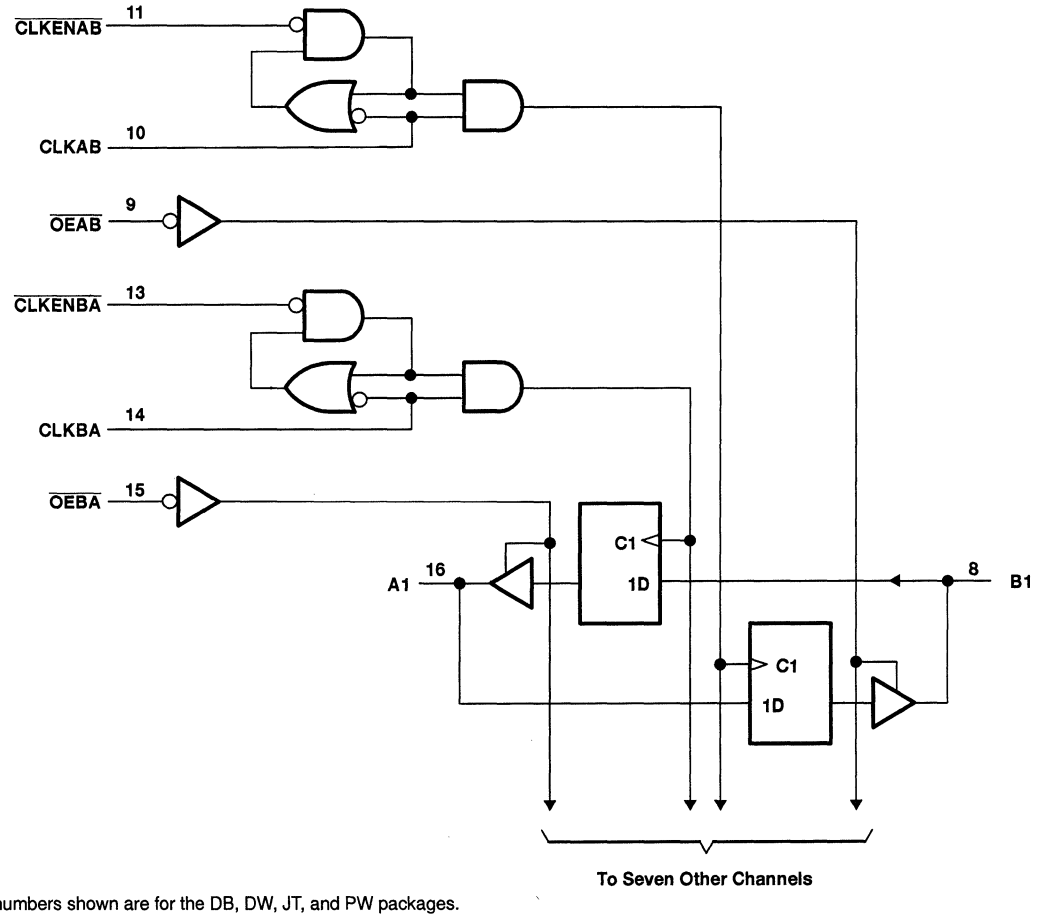
† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT2952 ..... 96 mA
SN74LVT2952 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT2952 ..... 48 mA
SN74LVT2952 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT2952		SN74LVT2952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT2952			SN74LVT2952			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.19		0.13	0.19	mA
			Outputs low		8.8	12		8.8	12	
			Outputs disabled		0.13	0.19		0.13	0.19	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4.5			4.5		pF
C_{io}	V_O = 3 V or 0				11.5			11.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirement over recommended operating free-air temperature range (unless otherwise noted)

				SN54LVT2952				SN74LVT2952				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency								150		150	MHz
t_w	Pulse duration		CLK high					3.3		3.3		ns
			CLK low					3.3		3.3		
t_{su}	Setup time before CLK↑	A or B	High	2.6		2.9		2.5		2.8		ns
			Low	2.6		3.1		2.5		3		
		$\overline{CE}$	High	0.9		0.8		0.9		0.8		
			Low	2.5		2.7		2.4		2.7		
t_h	Hold time after CLK↑	A or B		1.5		0.7		1.5		0.7		ns
		$\overline{CE}$		2.6		2.6		2.5		2.6		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT2952				SN74LVT2952					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}							150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.3	6.4	2.7	7.4	1.3	3.6	6.1	2.7	7.1	ns
t_{PHL}			1.8	6.1	2.7	7	1.8	3.7	6	2.7	6.9	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1	6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	ns
t_{PZL}			1.1	6.6	2.9	8.2	1.2	3.2	6.5	2.9	8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1	7	2.7	7.6	1	4.1	6.3	2.7	6.9	ns
t_{PLZ}			1.6	5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

LVTZ OCTALS

Features

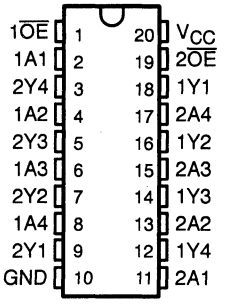
- Power-up 3-state between 0 V and 1.5 V without an external pullup resistor or voltage supervisor is assured
- Mixed-mode circuitry
- Expanded V_{CC} range from 2.7 V to 3.6 V
- Bus-hold circuitry
- Power-on-demand active feedback circuitry
- SOIC, EIAJ SSOP, and TSSOP packaging

Benefits

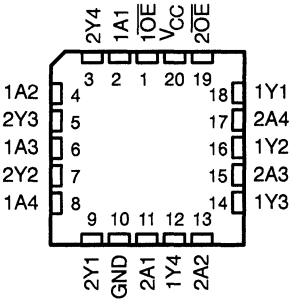
- Prevents loading and bus contention when V_{CC} is ramping during power up
- 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized or scaled CMOS
- Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
- AC performance optimized for both regulated supply and unregulated battery operation
- Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
- Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
- Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **High-Impedance State During Power Up and Power Down**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVTZ240 . . . J PACKAGE
SN74LVTZ240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTZ240 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

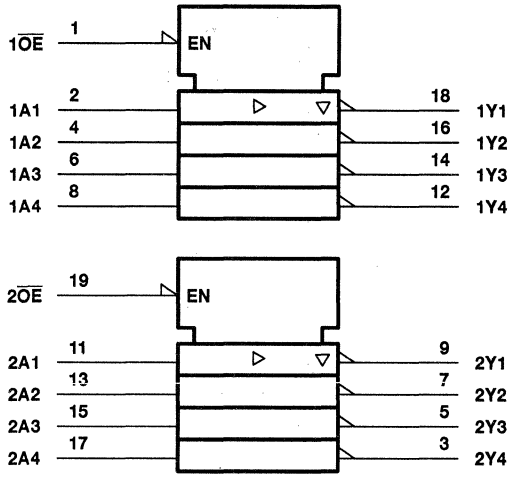
The SN74LVTZ240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTZ240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

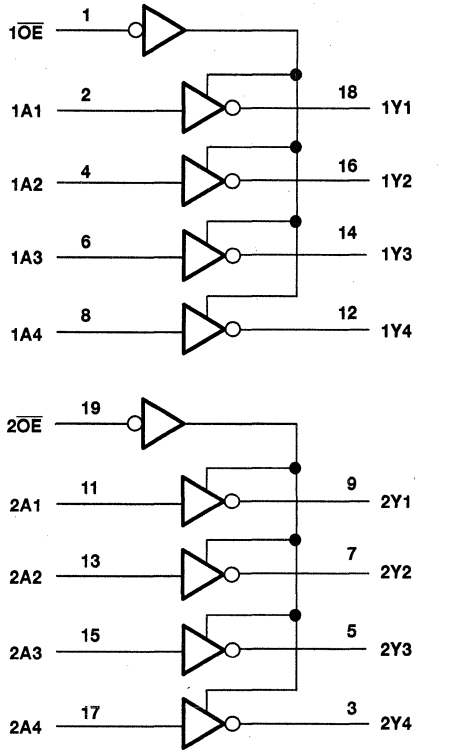
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTZ240 ..... 96 mA
SN74LVTZ240 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTZ240 ..... 48 mA
SN74LVTZ240 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			SN54LVTZ240		SN74LVTZ240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTZ240			SN74LVTZ240			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 0 to 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0 V,	V_I or V_O = 0 to 4.5 V							±100	µA
I_{OZPU}¶	V_{CC} = 0 V to 1.5,	V_O = 0.5 to 3 V,	$\overline{OE}$ = X						±50	µA
I_{OZPD}¶	V_{CC} = 1.5 V to 0,	V_O = 0.5 to 3 V,	$\overline{OE}$ = X						±50	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−5			−5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.225	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.225	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ This parameter is guaranteed by characterization.

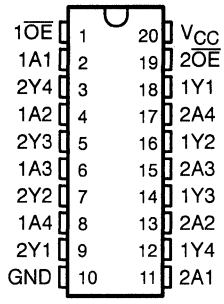
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ240				SN74LVTZ240				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A	Y	1	4.5		5.4	1	2.5	4.3	5.2	ns
t_{PHL}			1	4.5		5.2	1	2.5	4.3	5	
t_{PZH}	$\overline{OE}$	Y	1	5.4		6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1	5.4		7.4	1	3.1	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	2	5.8		6.5	2	3.9	5.6	6.3	ns
t_{PLZ}			1.6	5.3		5.8	1.6	3.2	5.1	5.6	

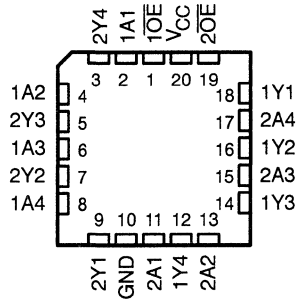
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **High-Impedance State During Power Up and Power Down**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVTZ244 . . . J PACKAGE
SN74LVTZ244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTZ244 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

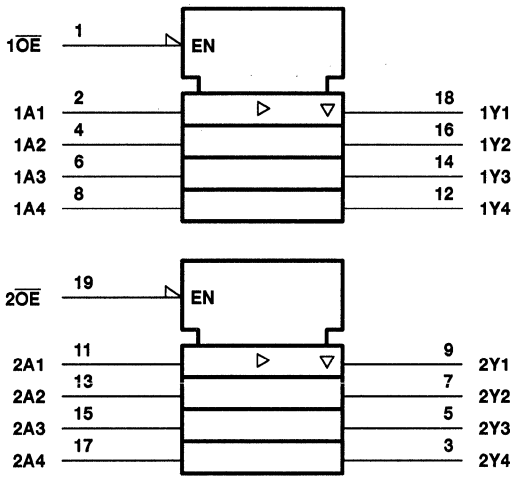
The SN74LVTZ244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTZ244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

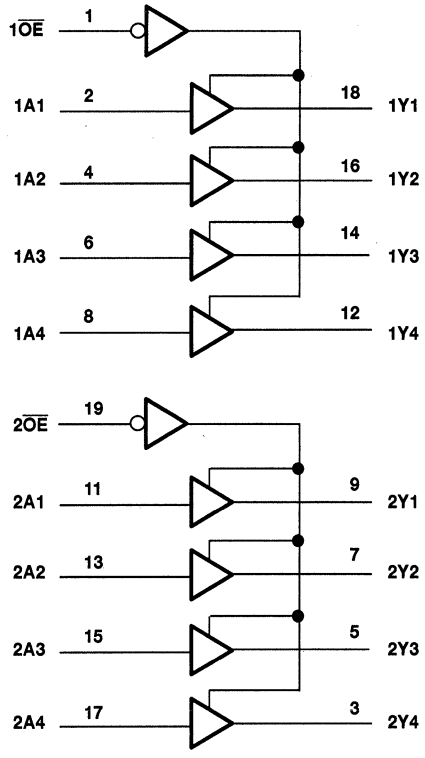
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTZ244 ..... 96 mA
SN74LVTZ244 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTZ244 ..... 48 mA
SN74LVTZ244 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			SN54LVTZ244		SN74LVTZ244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTZ244			SN74LVTZ244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 0 to 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0 V,	V_I or V_O = 0 to 4.5 V							±100	µA
I_{OZPU}¶	V_{CC} = 0 V to 1.5,	V_O = 0.5 to 3 V,	$\overline{OE}$ = X						±50	µA
I_{OZPD}¶	V_{CC} = 1.5 V to 0,	V_O = 0.5 to 3 V,	$\overline{OE}$ = X						±50	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.225	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.225	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ This parameter is guaranteed by characterization.

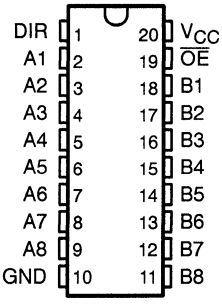
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ244				SN74LVTZ244				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A	Y	1	4.7		5.2	1	2.5	4.1	5	ns
t_{PHL}			1	4.4		5.4	1	2.5	4.1	5.2	
t_{PZH}	$\overline{OE}$	Y	1	5.4		6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1.1	5.4		7.6	1.1	3.1	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	1.9	6.2		6.9	1.9	3.9	5.6	6.3	ns
t_{PLZ}			1.8	5.5		6	1.8	3.2	5.1	5.6	

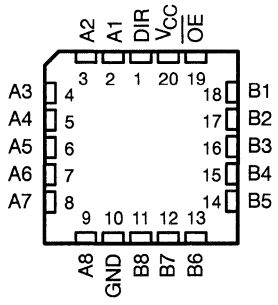
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **High-Impedance State During Power Up and Power Down**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**

SN54LVTZ245 . . . J PACKAGE
SN74LVTZ245 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTZ245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

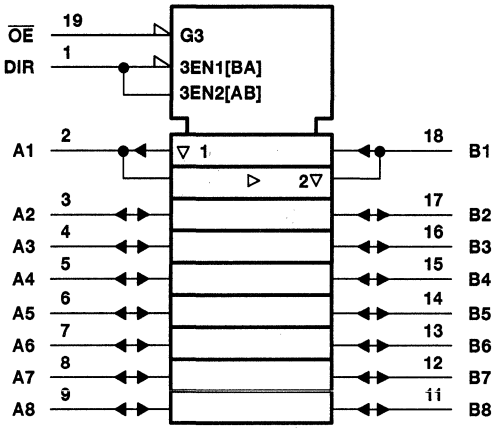
The SN74LVTZ245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVTZ245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

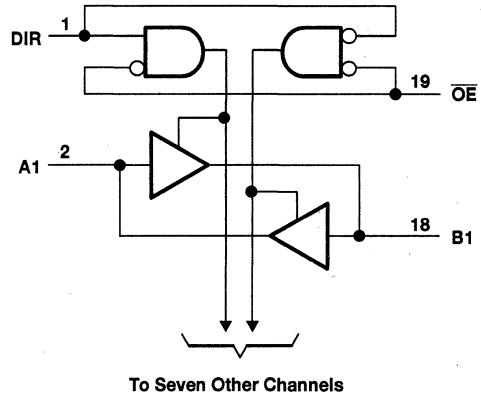
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTZ245 ..... 96 mA
SN74LVTZ245 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTZ245 ..... 48 mA
SN74LVTZ245 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			SN54LVTZ245		SN74LVTZ245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTZ245			SN74LVTZ245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			100			20	
		V_I = V_{CC}				5			5	
		V_I = 0				−10			−10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
I_{OZPU}¶	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = X						±50	µA
I_{OZPD}¶	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = X						±50	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.13	0.5		0.13	0.19	mA
			Outputs low		8.8	14		8.8	12	
			Outputs disabled		0.13	0.5		0.13	0.19	
ΔI_{CC}#	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				10			10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This parameter is guaranteed by characterization.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ245				SN74LVTZ245				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A or B	B or A	1	4.6		5.3	1	2.5	4	5.2	ns
t_{PHL}			1	4.1		5.7	1	2.5	4	5.5	
t_{PZH}	$\overline{OE}$	A or B	1.1	6.1		7.2	1.1	3.3	5.9	7.1	ns
t_{PZL}			1.5	6.6		8	1.5	3.8	6.5	7.9	
t_{PHZ}	$\overline{OE}$	A or B	2.2	6.2		7	2.2	4.3	5.9	6.5	ns
t_{PLZ}			2	6.3		5.9	2	3.9	5.5	5.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

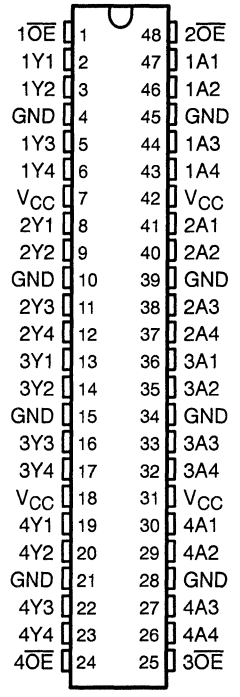
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

LVT Widebus™

Features	Benefits
• State-of-the-art 0.8-μ EPIC-IIB™ BiCMOS process	• Propagation delays as fast as 4.1 ns maximum for improved performance
• No input-diode clamp to V_{CC}	• Interfaces directly to industry standard buses and 5-V integrated circuits
• Fully compatible (input and output) with 5-V systems	• Supports live insertion
• –32-mA/64-mA drive current	• Drives large loads, buses, or memory arrays
• Low standby current (90 μA–190 μA)	• Extends battery life
• Bus-hold cell on data inputs and I/O pins	• Eliminates passive pullup resistors on local buses
• 2.7-V to 3.6-V V_{CC} range	• Fully characterized for unregulated battery operation
• JEDEC SSOP Widebus™ and EIAJ TSSOP Shrink Widebus™ packaging	• Saves board space and weight; TSSOP compatible with PCMCIA standards
• TI has established alternate sources	• Standardization that comes from a common product approach

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162240 . . . WD PACKAGE
SN74LVT162240 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162240 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

The SN74LVT162240 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

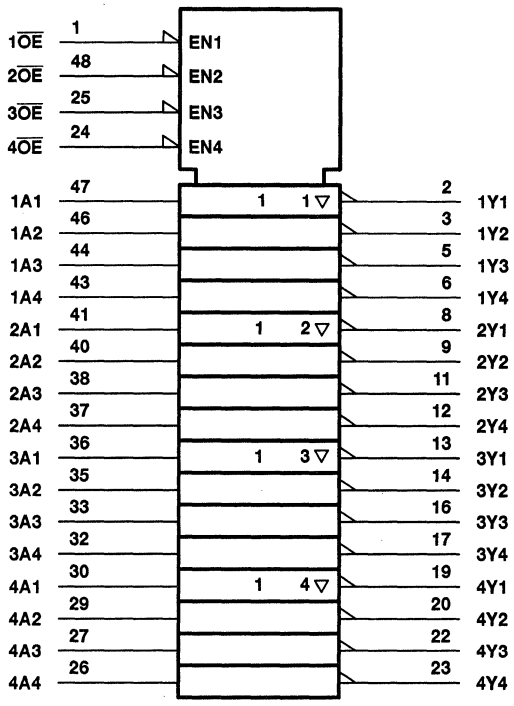
The SN54LVT162240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

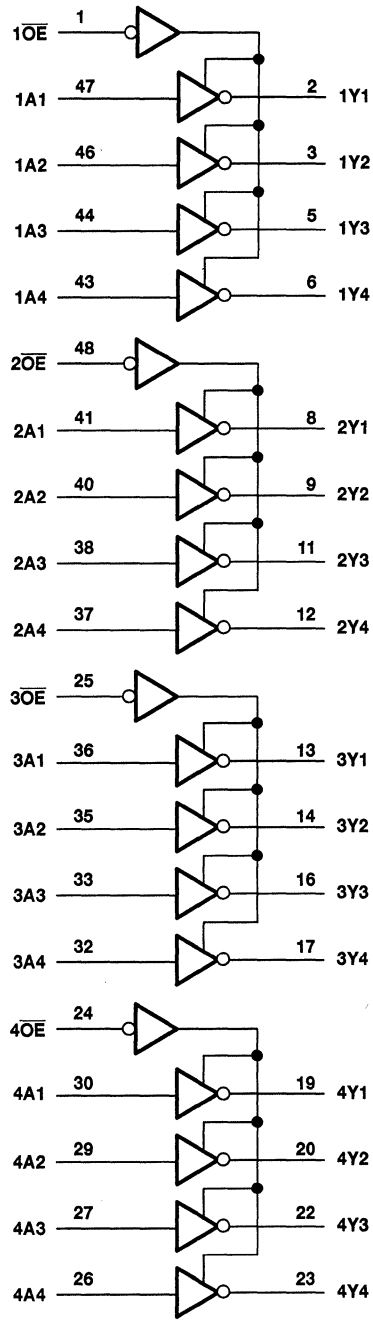
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LVT162240		SN74LVT162240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT162240		SN74LVT162240		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = – 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10		10	μA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	
		V_I = V_{CC}	Data pins		1		1	
		V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		μA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	μA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
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- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
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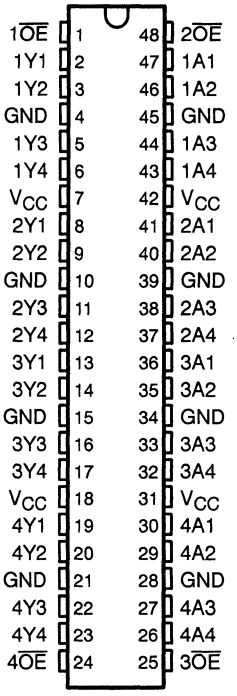
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16244A . . . WD PACKAGE
SN74LVT16244A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16244A is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

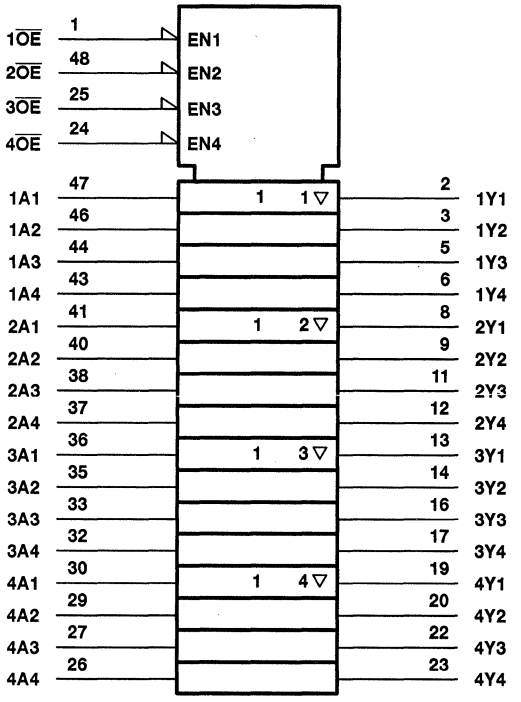
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16244A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16244A is characterized for operation from –40°C to 85°C.

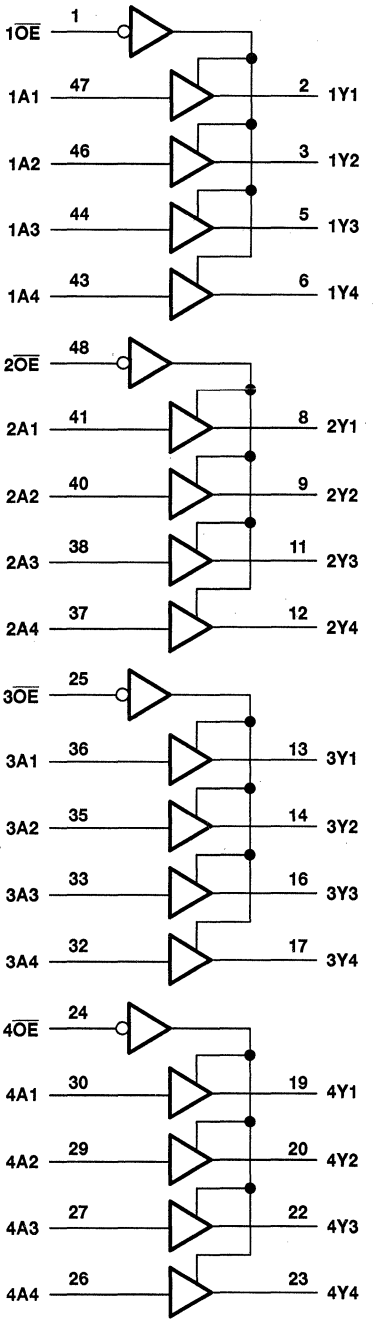
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16244A ..... 96 mA
SN74LVT16244A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16244A ..... 48 mA
SN74LVT16244A ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16244A		SN74LVT16244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16244A		SN74LVT16244A			UNIT
				MIN	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2					
		I_{OH} = –32 mA				2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
		I_{OL} = 24 mA			0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
		I_{OL} = 32 mA			0.5			0.5	
		I_{OL} = 48 mA			0.55				
		I_{OL} = 64 mA						0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins		±1			±1	
		V_I = V_{CC}	Data pins		1			1	
		V_I = 0			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75			µA
		V_I = 2 V		–75		–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.09			0.09	mA
			Outputs low		5			5	
			Outputs disabled		0.09			0.09	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2			0.2	mA
C_i	V_I = 3 V or 0						4		pF
C_o	V_O = 3 V or 0						10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

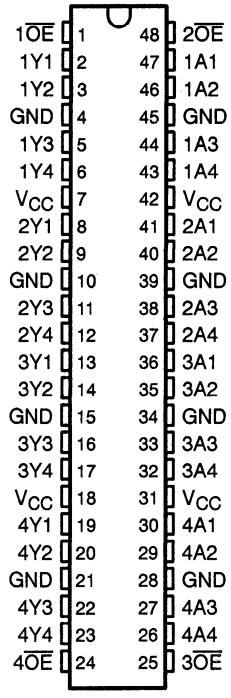
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16244A				SN74LVT16244A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1	4.2		5.1	1	2.3	4.1		5	ns
t_{PHL}			1	4.2		5.3	1	2.3	4.1		5.2	
t_{PZH}	$\overline{OE}$	Y	1	5.3		6.4	1	2.6	5.2		6.3	ns
t_{PZL}			1	5.3		6.8	1	2.6	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	2.1	5.9		6.4	2.2	3.9	5.7		6.3	ns
t_{PLZ}			1.9	5.3		5.7	2	3.7	5.1		5.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162244 . . . WD PACKAGE
SN74LVT162244 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162244 is a 16-bit buffer and line driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

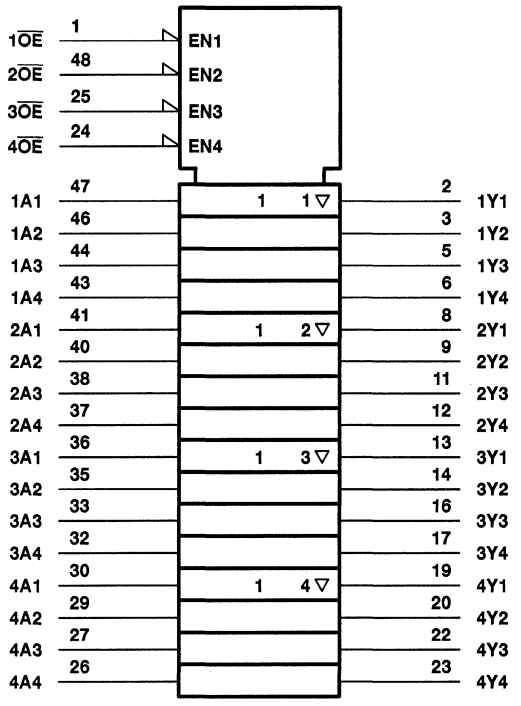
The SN74LVT162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

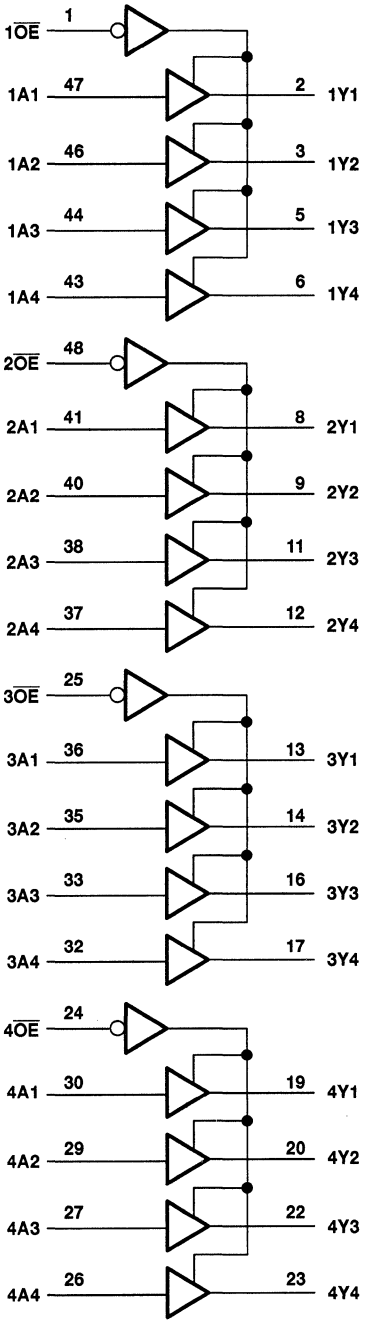
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LVT162244		SN74LVT162244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT162244			SN74LVT162244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA		2			2			V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA				0.8			0.8	V
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−5			−5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.19			0.09	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.09	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				10			10		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

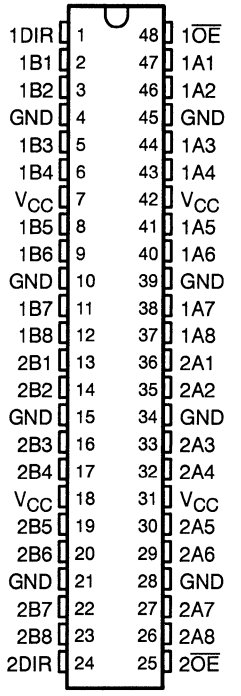
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162244				SN74LVT162244				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1.4	5.2		6.1	1.4	3.2	4.9		5.8	ns
t_{PHL}			1.1	5.1		6.3	1.1	3.1	5		6.1	
t_{PZH}	$\overline{OE}$	Y	1	6.6		7.3	1	4.7	6.4		7.1	ns
t_{PZL}			1.4	5.7		7.4	1.4	3.4	5.6		7.3	
t_{PHZ}	$\overline{OE}$	Y	2.6	6.9		7.6	2.6	4.5	6.6		7.3	ns
t_{PLZ}			2.6	6.1		6.8	2.6	3.6	5.8		6.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16245A . . . WD PACKAGE
SN74LVT16245A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16245A is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16245A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

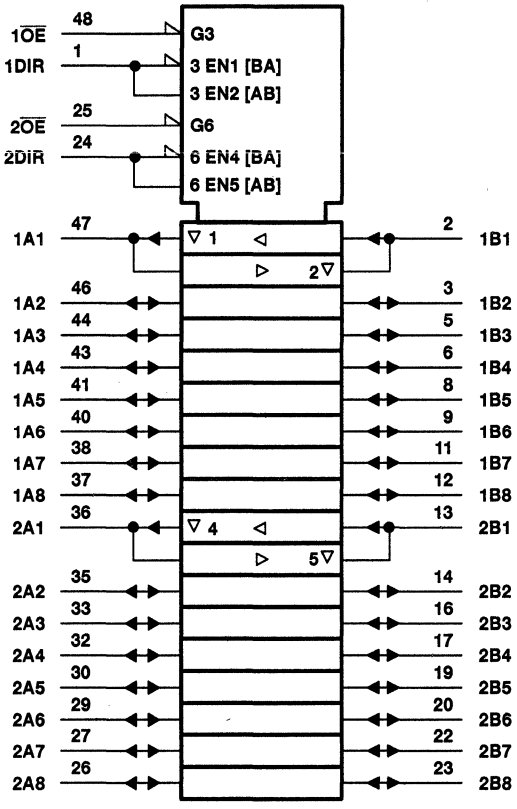
The SN54LVT16245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16245A is characterized for operation from –40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each 8-bit section)

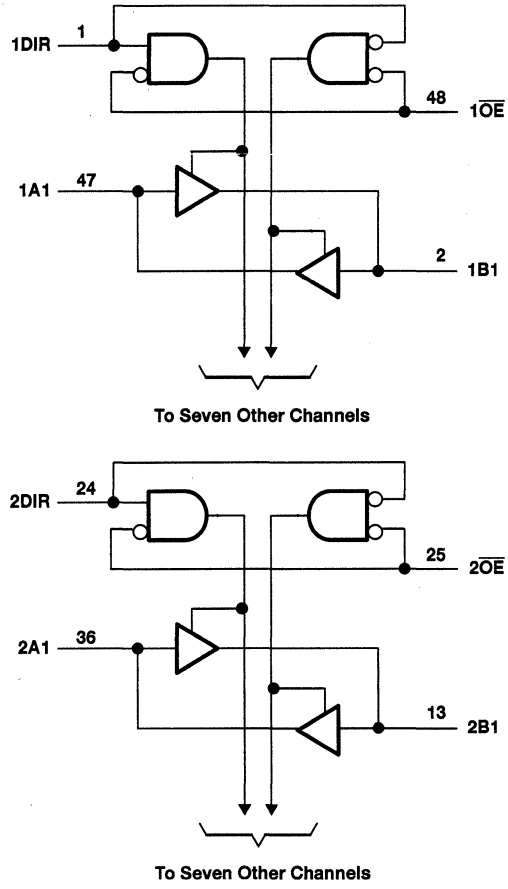
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16245A ..... 96 mA
SN74LVT16245A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16245A ..... 48 mA
SN74LVT16245A ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16245A		SN74LVT16245A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16245A			SN74LVT16245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = −24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.09			0.09	mA
			Outputs low			5			5	
			Outputs disabled			0.09			0.09	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

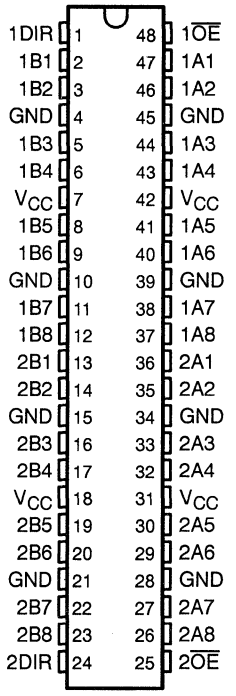
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16245A				SN74LVT16245A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A or B	B or A					1	2.4	4.1		5	ns
t_{PHL}							1	2.3	4.1		5.2	
t_{PZH}	$\overline{OE}$	A or B					1	3	5.3		6.3	ns
t_{PZL}							1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	A or B					2.7	4.6	6.4		7.2	ns
t_{PLZ}							2.6	4.3	5.8		6.1	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT162245 . . . WD PACKAGE
SN74LVT162245 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

description (continued)

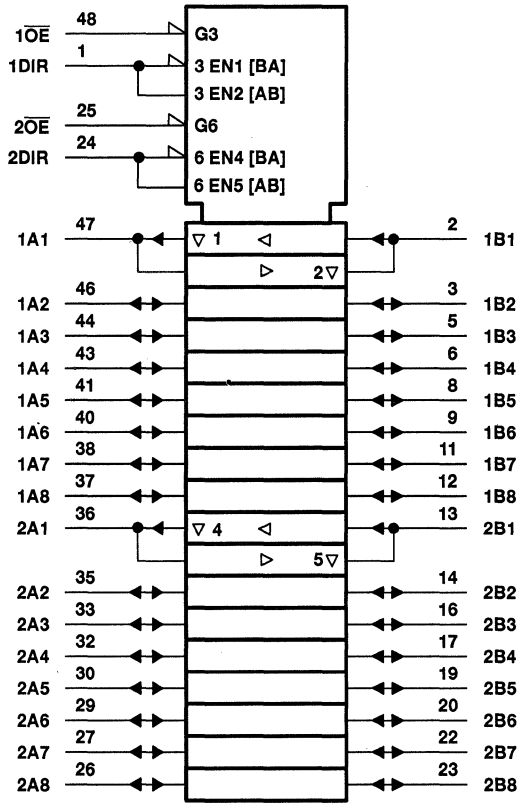
The SN74LVT162245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

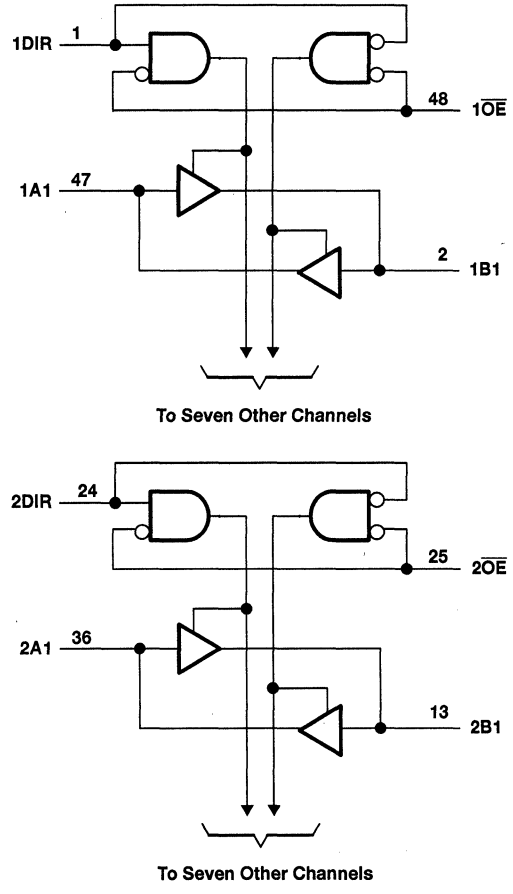
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT162245 (except A port) ..... 96 mA
SN74LVT162245 (except A port) ..... 128 mA
A port ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT162245 (B port) ..... 48 mA
SN74LVT162245 (B port) ..... 64 mA
A port ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT162245		SN74LVT162245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	B port		−24		−32	mA
		A port		−12		−12	
I_{OL}	Low-level output current	A port		12		12	mA
		B port		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

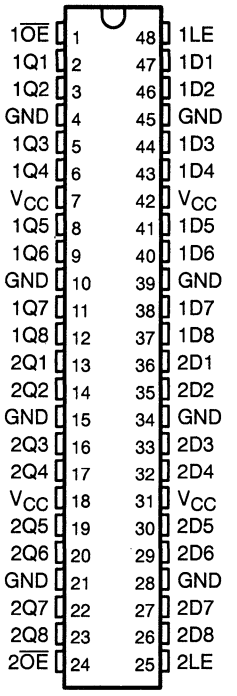
PARAMETER	TEST CONDITIONS			SN54LVT162245		SN74LVT162245		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = – 12 mA	A port	2		2		V
	V_{CC} = MIN to MAX†,	I_{OH} = –100 µA		V_{CC}–0.2		V_{CC}–0.2		
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V	I_{OH} = – 24 mA		2				
		I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 12 mA	A port		0.8		0.8	V
		I_{OL} = 100 µA	B port		0.2		0.2	
		I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA			0.4		0.4	
		I_{OL} = 32 mA			0.5		0.5	
		I_{OL} = 48 mA			0.55			
		I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX†,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports‡		20		20	
		V_I = V_{CC}			5		5	
		V_I = 0			–10		–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Unused pins at V_{CC} or GND
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16373 . . . WD PACKAGE
SN74LVT16373 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

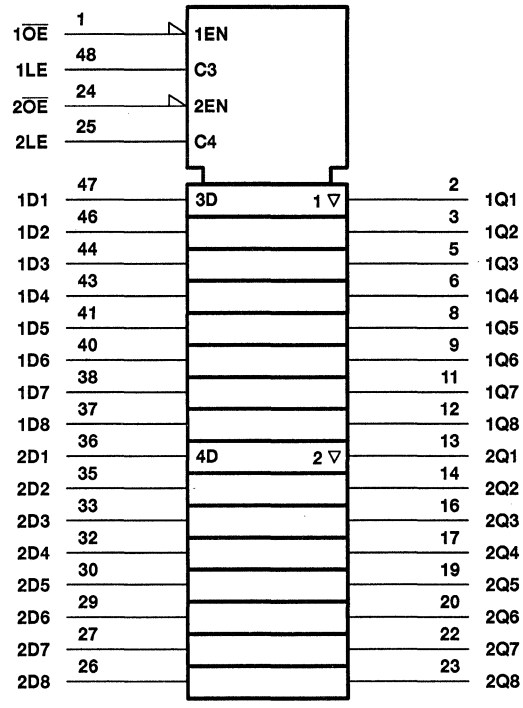
The SN74LVT16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

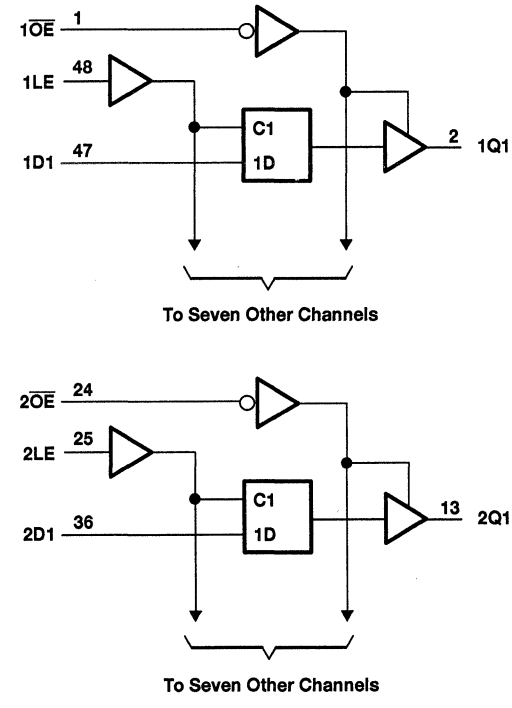
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16373 ..... 96 mA
SN74LVT16373 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16373 ..... 48 mA
SN74LVT16373 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16373		SN74LVT16373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16373			SN74LVT16373			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.09			0.09	mA
			Outputs low			5			5	
			Outputs disabled			0.09			0.09	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				5			5		pF
C_o	V_O = 3 V or 0				9.5			9.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54LVT16373				SN74LVT16373				UNIT
		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	0.5		0.5		0.5		0.5		ns
t_h	Hold time, data after LE↓	1.8		2		1.8		2		ns

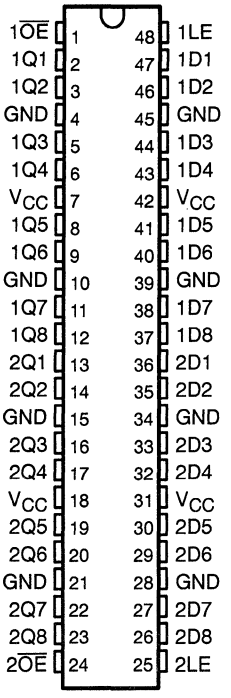
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16373				SN74LVT16373				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	D	Q	1.3	5.1		5.8	1.3	2.7	5	5.7	ns
t_{PHL}			1.4	5		5.8	1.4	2.9	4.9	5.7	
t_{PLH}	LE	Q	2.1	7		7.5	2.1	3.6	6	6.8	ns
t_{PHL}			3	8.1		9.4	3	4.7	6.9	8.8	
t_{PZH}	$\overline{OE}$	Q	1	5.6		6.4	1	2.9	5.3	6.3	ns
t_{PZL}			1.3	5.3		6	1.3	3	5.1	5.9	
t_{PHZ}	$\overline{OE}$	Q	2.7	7.2		8.2	2.7	4.3	6.8	7.6	ns
t_{PLZ}			2.6	6.1		6.2	2.6	4	5.8	5.9	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162373 . . . WD PACKAGE
SN74LVT162373 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162373 is a 16-bit transparent D-type latch with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

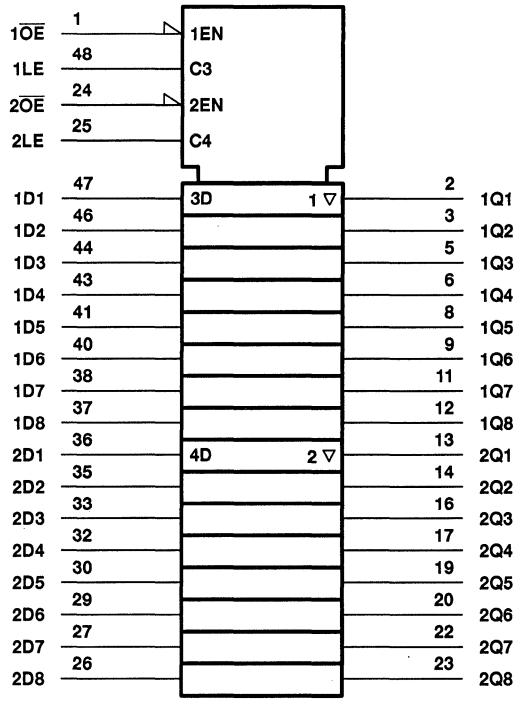
The SN54LVT162373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

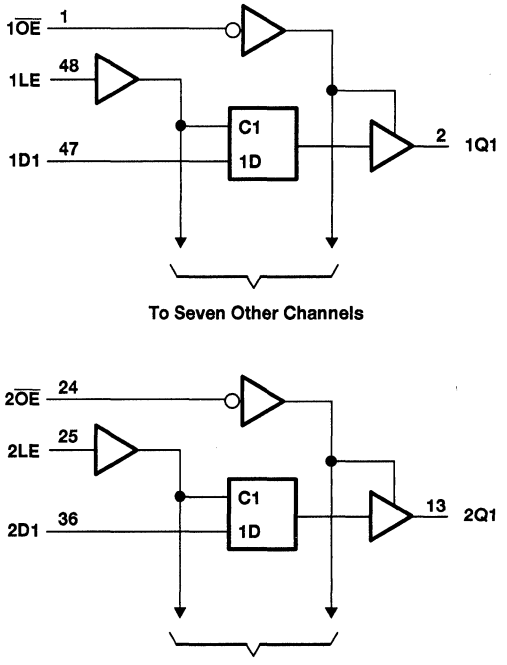
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LVT162373		SN74LVT162373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–12		–12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

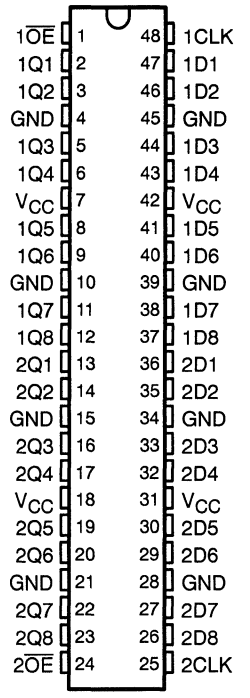
PARAMETER	TEST CONDITIONS			SN54LVT162373		SN74LVT162373		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = – 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX†,	V_I = 5.5 V			10		10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins		±1		±1	
		V_I = V_{CC}	Data pins		1		1	
		V_I = 0			–5		–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}‡	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16374 . . . WD PACKAGE
SN74LVT16374 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

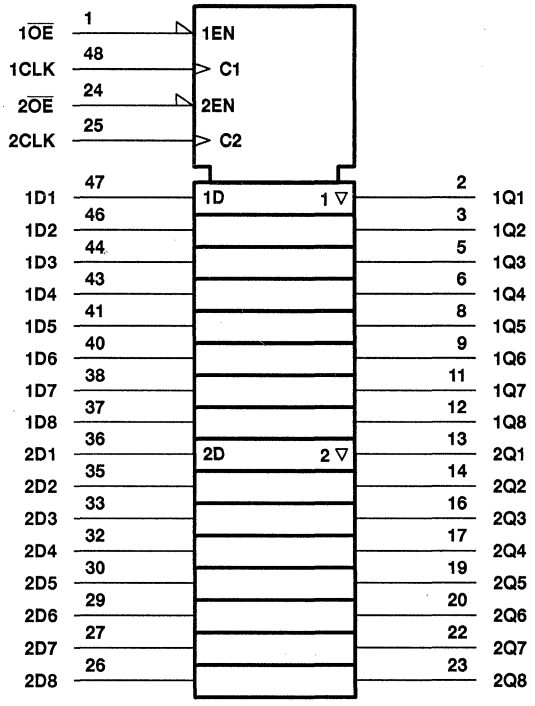
The SN74LVT16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

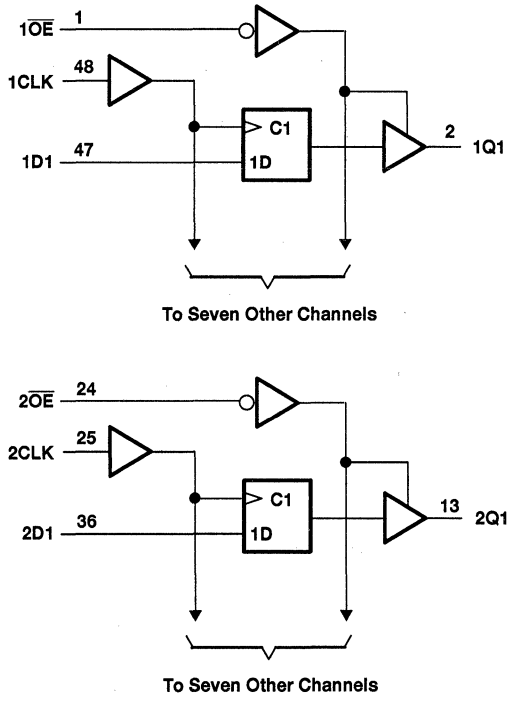
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16374 ..... 96 mA
SN74LVT16374 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16374 ..... 48 mA
SN74LVT16374 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16374		SN74LVT16374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16374			SN74LVT16374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	
		V_I = V_{CC}	Data pins			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.1			0.1	mA
			Outputs low			5			5	
			Outputs disabled			0.1			0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				5			5		pF
C_o	V_O = 3 V or 0				9.5			9.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16374				SN74LVT16374				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	High or low	2.2		2.6		2.2		2.6		ns
t_h	Hold time, data after CLK↑	High or low	0.6		0		0.6		0		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

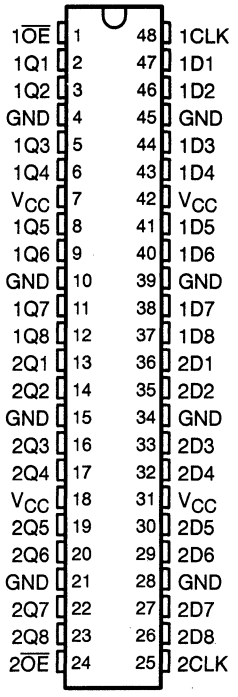
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16374				SN74LVT16374					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	CLK	Q	1.9	6.6		7.4	1.9	3.6	6.3		7	ns
t_{PHL}			2.3	6.9		7.5	2.3	4.1	6.6		7.2	
t_{PZH}	$\overline{OE}$	Q	1	5.6		6.4	1	2.7	5.3		6.3	ns
t_{PZL}			1.3	5.3		6	1.3	2.8	5.1		5.9	
t_{PHZ}	$\overline{OE}$	Q	2.7	7.2		8.2	2.7	4.3	6.8		7.6	ns
t_{PLZ}			2.6	6.1		8.2	2.6	3.9	5.8		5.9	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings**

SN54LVT162374 . . . WD PACKAGE
SN74LVT162374 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT162374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT162374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

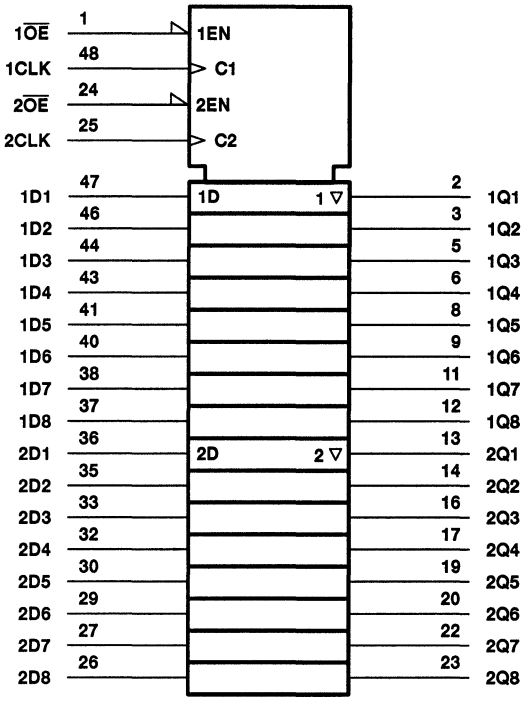
The SN54LVT162374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

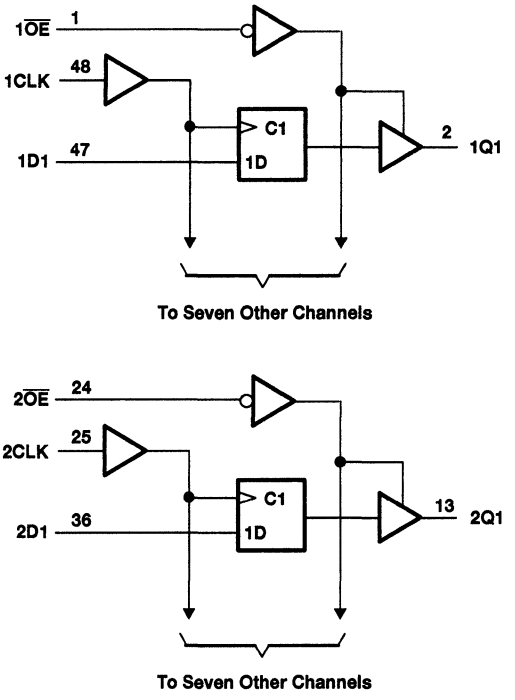
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O ..... 30 mA
Current into any output in the high state, I_O (see Note 2) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LVT162374		SN74LVT162374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

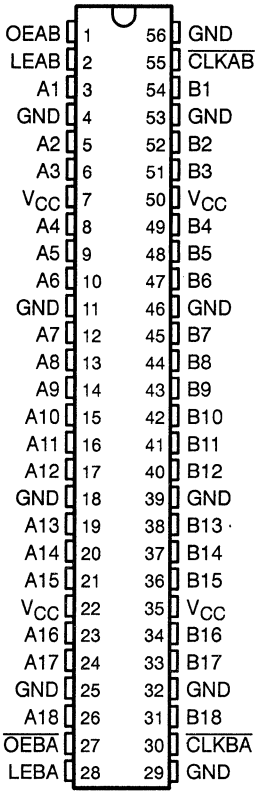
PARAMETER	TEST CONDITIONS			SN54LVT162374		SN74LVT162374		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = − 12 mA		2		2		V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8		0.8	V
I_I	V_{CC} = 0 or MAX†,	V_I = 5.5 V			10		10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins		±1		±1	
		V_I = V_{CC}	Data pins		1		1	
		V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		µA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−1		−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.19		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.1	
ΔI_{CC}‡	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16500 . . . WD PACKAGE
SN74LVT16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16500 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

Widebus and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

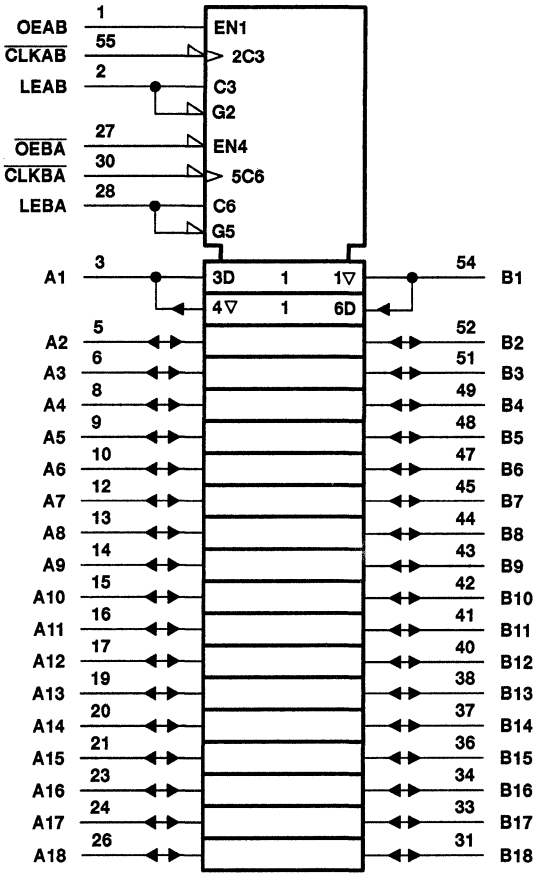
The SN54LVT16500 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16500 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

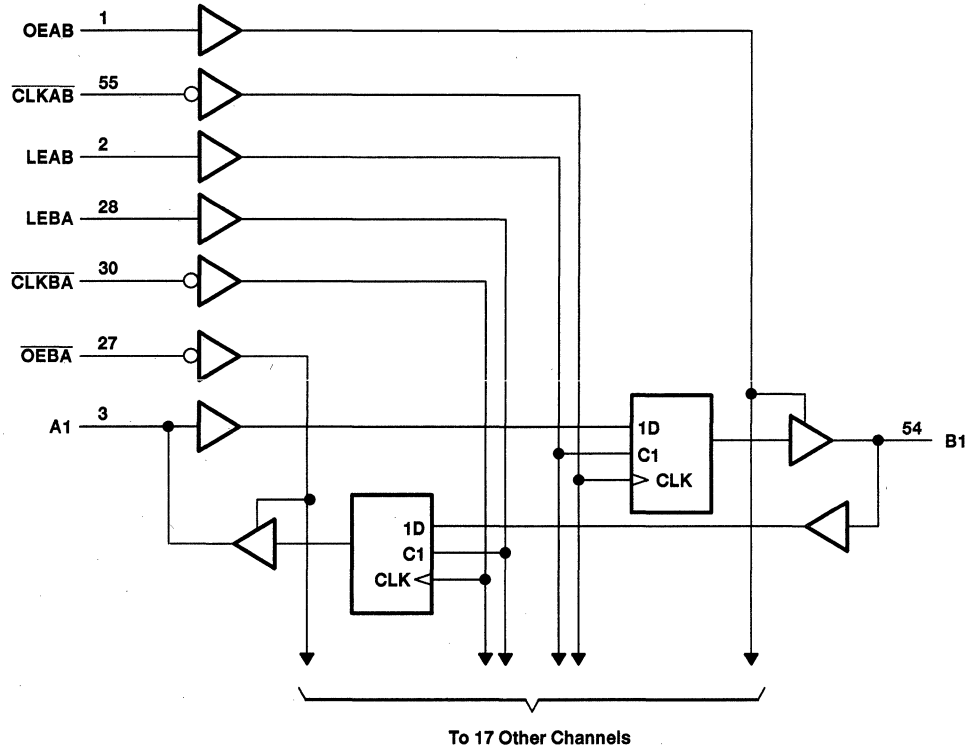
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16500 ..... 96 mA
SN74LVT16500 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16500 ..... 48 mA
SN74LVT16500 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16500		SN74LVT16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16500			SN74LVT16500			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				3.5			3.5		pF
C_{io}	V_O = 3 V or 0				12			12		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16500				SN74LVT16500				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	125	0	150	0	125	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		$\overline{CLK}$ high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before $\overline{CLKAB}\downarrow$	1.8		1.1		1.8		1.1		ns
		B before $\overline{CLKBA}\downarrow$	1.9		1.2		1.9		1.2		
		A or B before LE↓, $\overline{CLK}$ high	2.2		1.3		2.2		1.3		
		A or B before LE↓, $\overline{CLK}$ low	2.7		1.9		2.7		1.9		
t_h	Hold time	A or B after $\overline{CLK}\downarrow$	1.2		1.2		1.2		1.2		ns
		A or B after LE↓	0.9		1.1		0.9		1.1		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16500				SN74LVT16500					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		125		150			125		MHz
t_{PLH}	B or A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns
t_{PHL}			1.6	6		7.8	1.6	3.2	5.9		7.7	
t_{PLH}	LEBA or LEAB	A or B	2.3	7.3		8.9	2.3	4	7		8.5	ns
t_{PHL}			2.7	8.2		9.8	2.7	4.3	7.9		9.7	
t_{PLH}	$\overline{CLKBA}$ or $\overline{CLKAB}$	A or B	2	7.4		8.8	2	4.1	7		8.3	ns
t_{PHL}			2.4	8.1		10	2.4	4.4	7.9		9.9	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.2		6.1	1.2	3	5		5.9	ns
t_{PZL}			1.5	5.9		7	1.5	3	5.8		6.9	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	ns
t_{PLZ}			2.8	7.3		7.7	2.8	4.7	6.7		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

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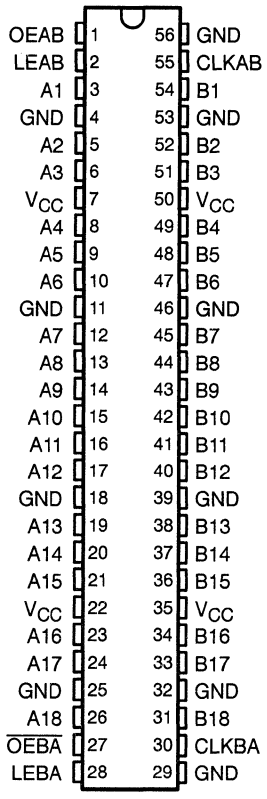
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16501 . . . WD PACKAGE
SN74LVT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16501 is an 18-bit universal bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{OEBA}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16501 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

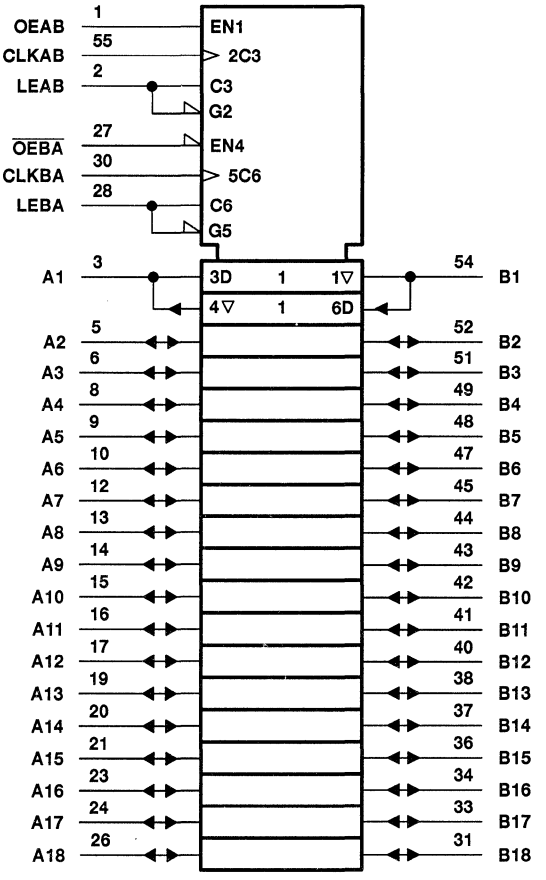
INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

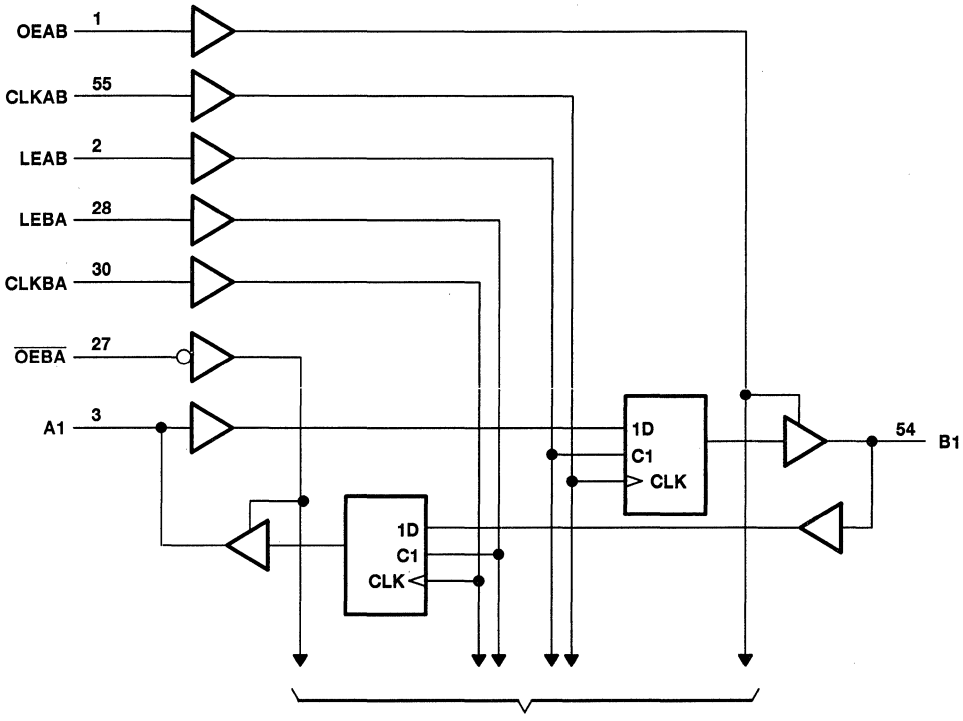
§ Output level before the indicated steady-state input conditions were established.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16501 ..... 96 mA
SN74LVT16501 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16501 ..... 48 mA
SN74LVT16501 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16501		SN74LVT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16501			SN74LVT16501			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				3.5			3.5		pF
C_{io}	V_O = 3 V or 0				12			12		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16501				SN74LVT16501				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	125	0	150	0	125	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before CLKAB↑	1.6		2.1		1.6		2.1		ns
		B before CLKBA↑	1.6		2.1		1.6		2.1		
		A or B before LE↓, CLK high	2.6		1.9		2.6		1.9		
		A or B before LE↓, CLK low	2		1.3		2		1.3		
t_h	Hold time	A or B after CLK↑	2		2.1		2		2.1		ns
		A or B after LE↓	0.9		1.2		0.9		1.2		

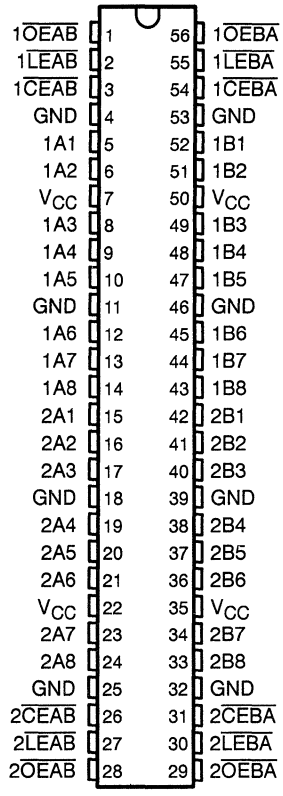
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16501				SN74LVT16501				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		125		150		125		MHz
t_{PLH}	B or A	A or B	1.7	5.4		5.8	1.7	5.4		6.8	ns
t_{PHL}			1.6	6		7.8	1.6	5.9		7.7	
t_{PLH}	LEBA or LEAB	A or B	2.3	6.6		7.6	2.3	7		8.5	ns
t_{PHL}			2.7	8.2		9.8	2.7	7.9		9.7	
t_{PLH}	CLKBA or CLKAB	A or B	2.5	6.9		7.9	2.5	7.9		9.2	ns
t_{PHL}			3.5	9.4		10.7	3.5	8.9		10.4	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.1		6.1	1.2	5		5.9	ns
t_{PZL}			1.5	5.9		7	1.5	5.8		6.9	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	2.7	7.5		8.5	2.7	7.4		8.3	ns
t_{PLZ}			2.8	6.8		7.5	2.8	6.7		7.2	

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16543 . . . WD PACKAGE
SN74LVT16543 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16543 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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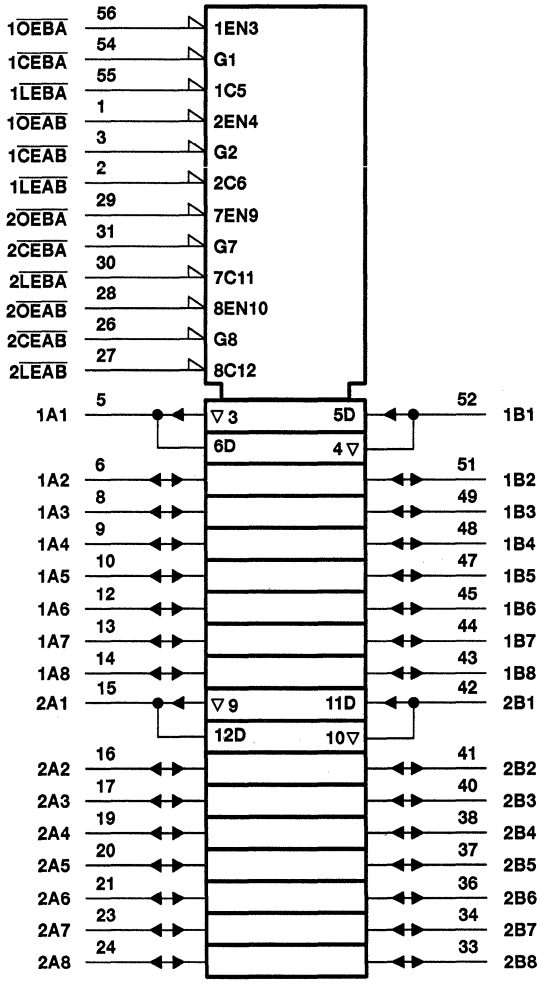
description (continued)

The SN74LVT16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

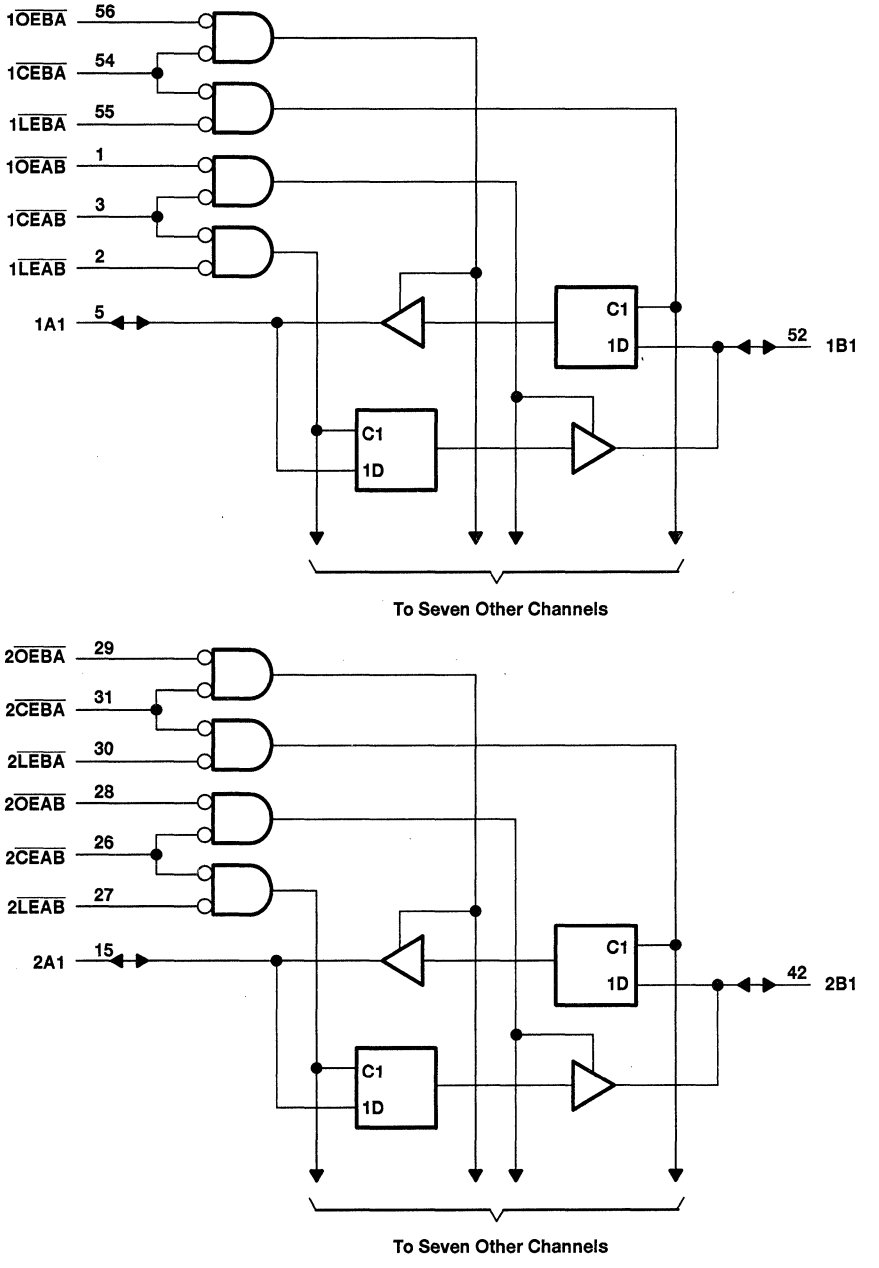
The SN54LVT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16543 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE† (each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16543 ..... 96 mA
SN74LVT16543 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16543 ..... 48 mA
SN74LVT16543 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16543		SN74LVT16543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16543			SN74LVT16543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				13			13		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54LVT16543				SN74LVT16543				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	High	0.8		0.5		0.8		0.5		ns
			Low	1.5		1.9		1.5		1.9		
		Data before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	High	0.7		0.4		0.7		0.4		ns
			Low	1.6		1.9		1.6		1.9		
t_h	Hold time	Data after $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	High	0.8		0		0.8		0		ns
			Low	1.2		1.3		1.2		1.3		
		Data after $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	High	0.8		0		0.8		0		ns
			Low	1.3		1.4		1.3		1.4		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

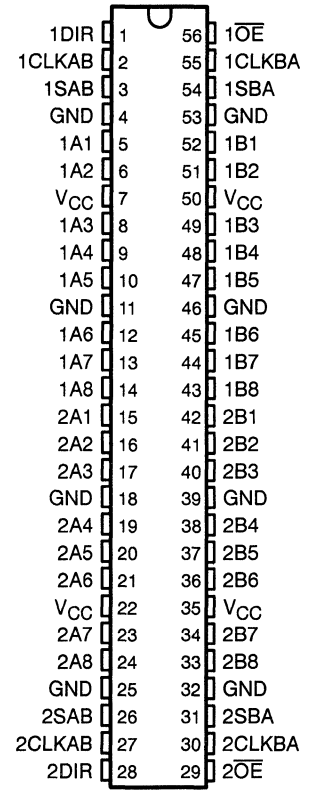
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16543				SN74LVT16543					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.4	4.5		5	1.4	2.7	4.6		5.5	ns
t_{PHL}			1.3	4.5		5.3	1.3	2.9	4.6		5.8	
t_{PLH}	$\overline{LE}$	A or B	1.3	6.8		8.5	1.7	3.7	6.3		8.1	ns
t_{PHL}			1.5	6.5		8.3	1.9	3.7	6		7.8	
t_{PZH}	$\overline{OE}$	A or B	1.4	5.7		7.3	1.5	3.3	5.8		7.6	ns
t_{PZL}			1.6	5.6		7.4	1.6	3.3	6.2		8.2	
t_{PHZ}	$\overline{OE}$	A or B	2	6.1		6.6	2	4.1	6.5		7.1	ns
t_{PLZ}			2.7	5.2		5.4	2.7	3.9	5.8		5.9	
t_{PZH}	$\overline{CE}$	A or B	1.4	5.5		6.7	1.5	3.3	6		7.6	ns
t_{PZL}			1.6	5.5		6.7	1.7	3.3	6.4		8.3	
t_{PHZ}	$\overline{CE}$	A or B	2	6.2		6.6	2	4.1	6.4		7.1	ns
t_{PLZ}			2.6	5.3		5.5	2.6	4	5.4		5.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16646 . . . WD PACKAGE
SN74LVT16646 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16646 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

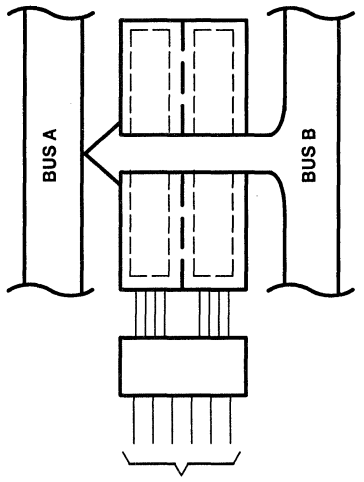
The SN74LVT16646 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

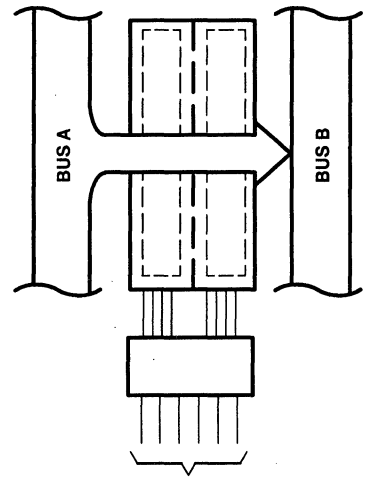
INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



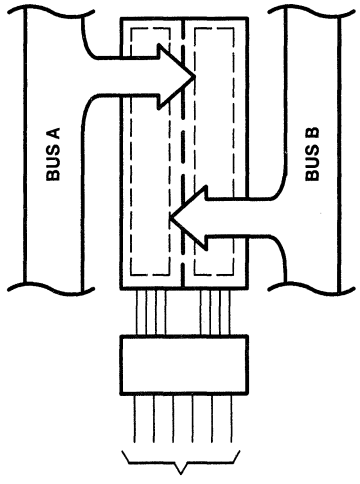
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



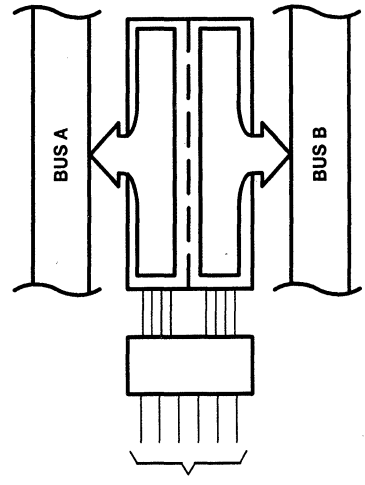
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

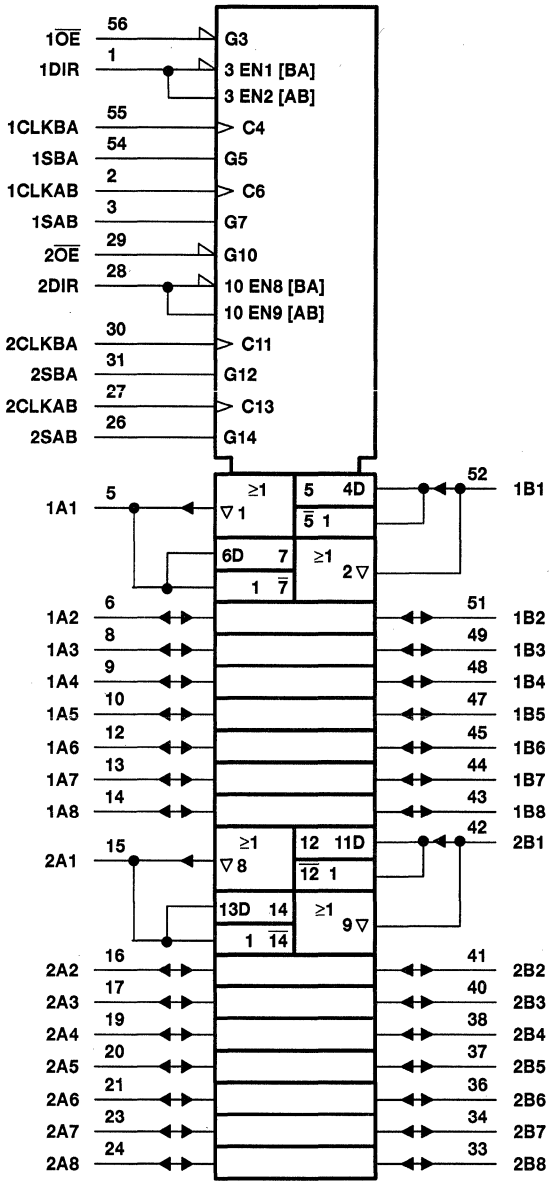


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

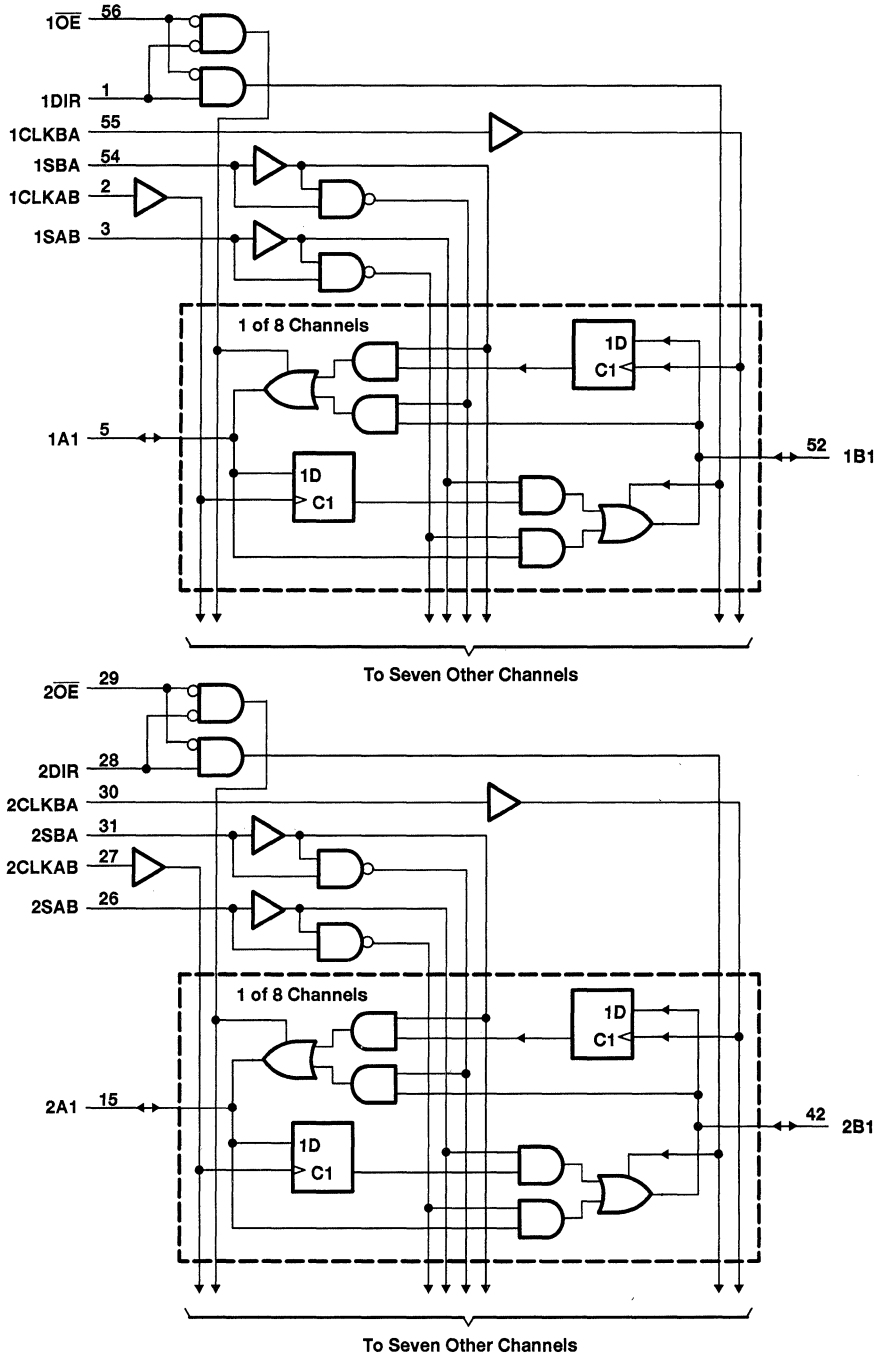
Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16646 ..... 96 mA
SN74LVT16646 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16646 ..... 48 mA
SN74LVT16646 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16646		SN74LVT16646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16646			SN74LVT16646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				5			5	
		V_I = 0				–10			–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				3.5			3.5		pF
C_{io}	V_O = 3 V or 0				12			12		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16646				SN74LVT16646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.3		1.4		1.3		1.4		ns
		Data low	2.4		3		2.4		3		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5		0		0.5		0		ns
		Data low	0.6		0.5		0.5		0.5		

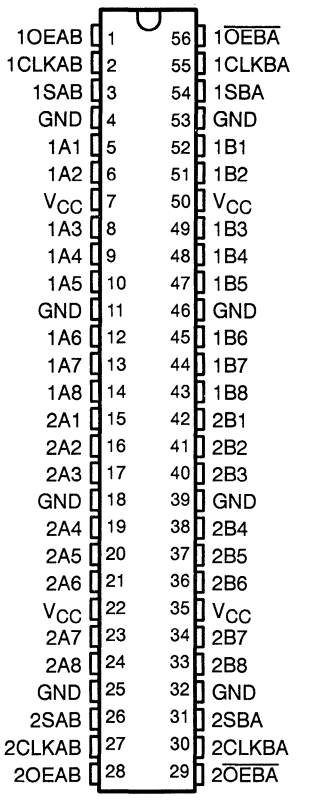
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16646				SN74LVT16646					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150				150					MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.8	6		6.9	1.8	3.8	5.7		6.7	ns
t_{PHL}			2.1	5.9		6.6	2.1	3.9	5.7		6.5	
t_{PLH}	A or B	B or A	1.3	4.9		5.6	1.3	3	4.7		5.4	ns
t_{PHL}			1	4.8		5.8	1	3.1	4.7		5.6	
t_{PLH}	SBA or SAB‡	A or B	1.4	6.4		7.4	1.4	4	6.2		7.2	ns
t_{PHL}			1.4	6.4		7.4	1.4	4.3	6.2		7.2	
t_{PZH}	$\overline{OE}$	A or B	1	5.7		7.4	1	3	5.4		6.4	ns
t_{PZL}			1	6.5		7.5	1	3.1	5.6		6.5	
t_{PHZ}	$\overline{OE}$	A or B	2.3	6.7		7.1	2.3	4.6	6.5		6.9	ns
t_{PLZ}			2.2	6		6.5	2.2	4.5	5.8		5.9	
t_{PZH}	DIR	A or B	1	5.9		7.7	1	3.3	5.7		6.7	ns
t_{PZL}			1.2	5.9		7.3	1.2	3.5	5.8		6.7	
t_{PHZ}	DIR	A or B	1.7	7.3		8.5	1.7	4.7	7.2		8.3	ns
t_{PLZ}			1.5	7.8		7.4	1.5	4.9	6.6		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16652 . . . WD PACKAGE
SN74LVT16652 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT16652 is a 16-bit bus transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

Widebus is a trademark of Texas Instruments Incorporated.

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

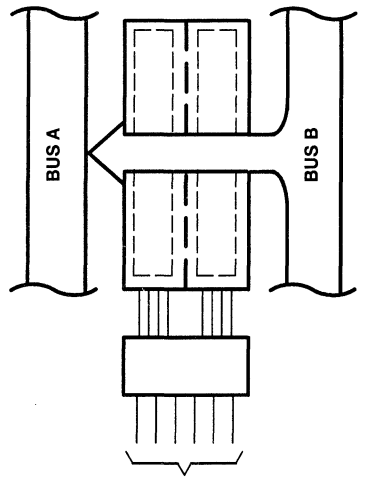
The SN54LVT16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

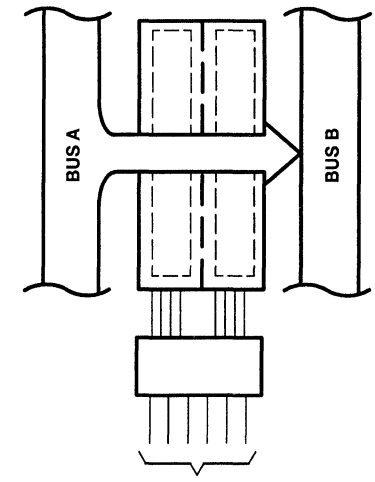
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



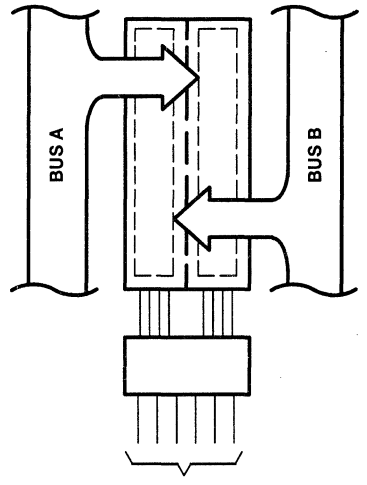
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



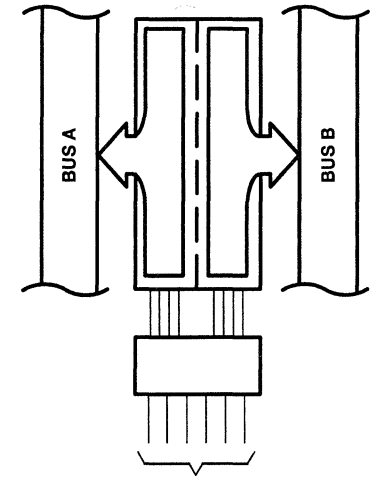
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



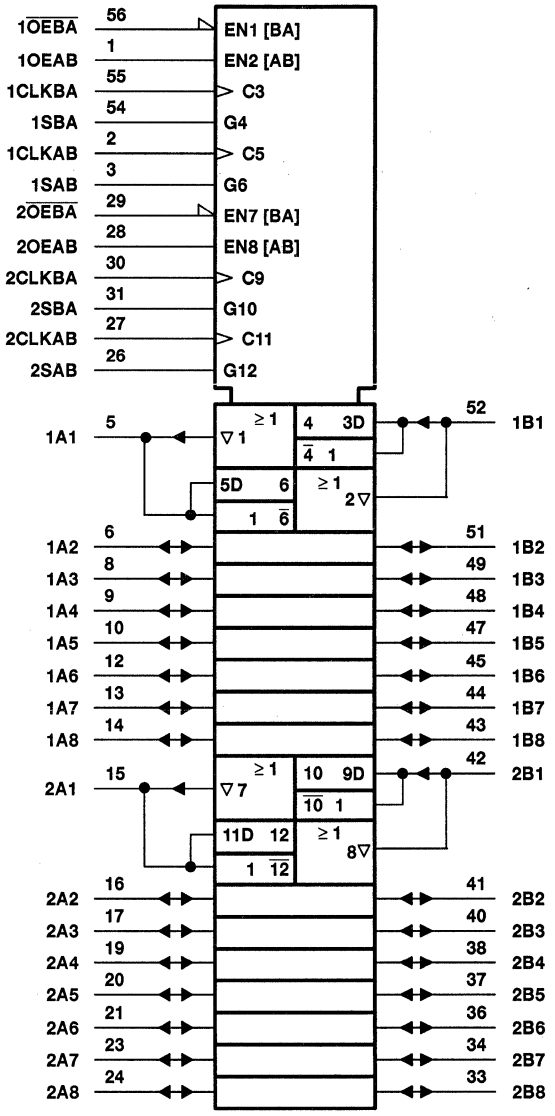
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

PRODUCT PREVIEW

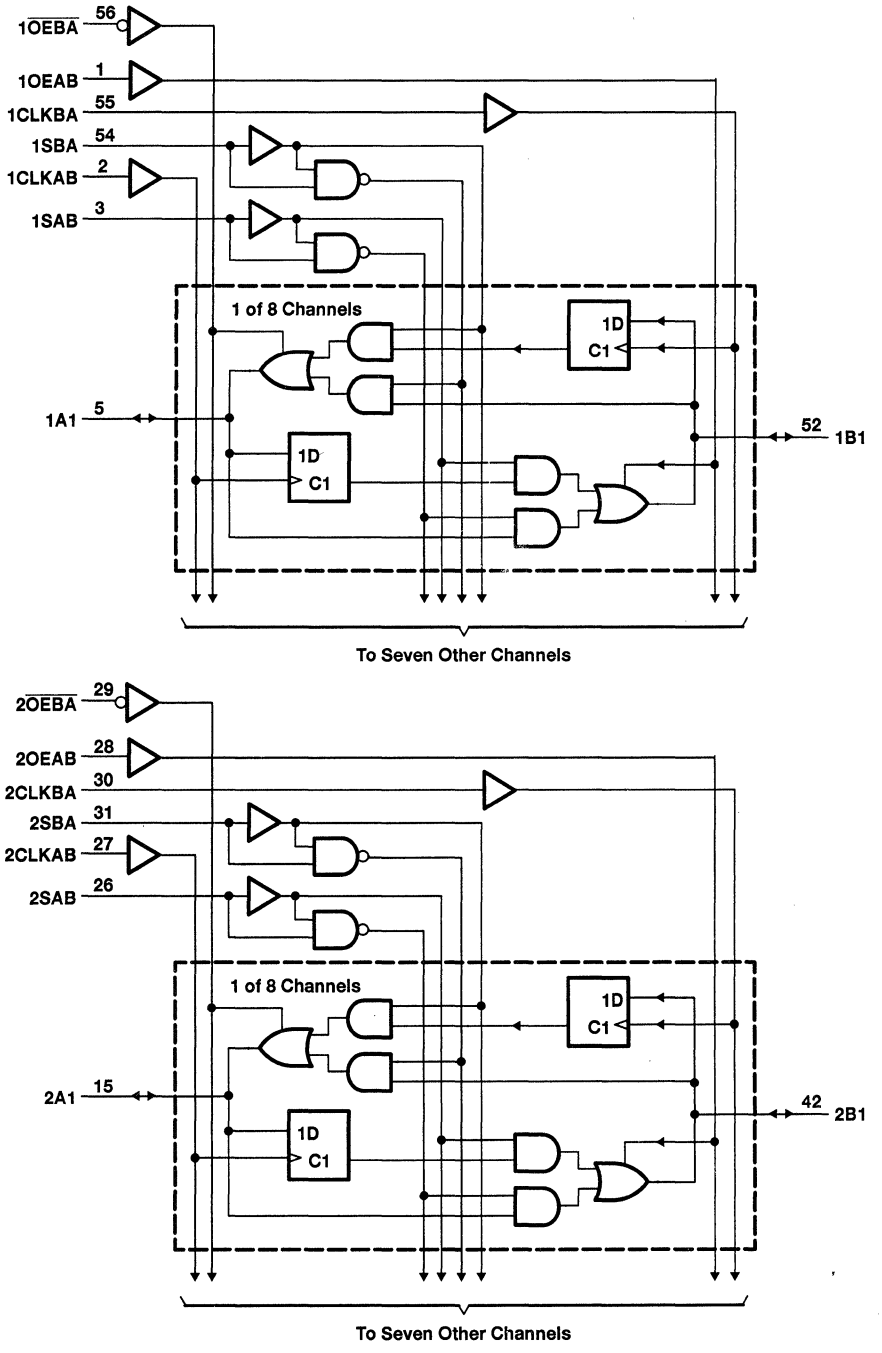
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16652 ..... 96 mA
SN74LVT16652 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16652 ..... 48 mA
SN74LVT16652 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16652		SN74LVT16652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

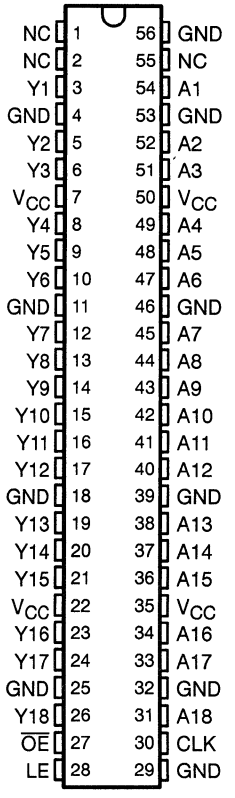
PARAMETER	TEST CONDITIONS			SN54LVT16652		SN74LVT16652		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA			–1.2		–1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = –100 µA		V_{CC}–0.2				V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4		2.4		
	V_{CC} = 3 V	I_{OH} = – 24 mA		2				
		I_{OH} = –32 mA				2		
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2		0.2	V
		I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA			0.4		0.4	
		I_{OL} = 32 mA			0.5		0.5	
		I_{OL} = 48 mA			0.55			
		I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins		±1		±1	µA
	V_{CC} = 0 or MAX†,	V_I = 5.5 V			10		10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports‡		20		20	
		V_I = V_{CC}			5		5	
		V_I = 0			–10		–10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75		75		µA
		V_I = 2 V		–75		–75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			–1		–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_{io}	V_O = 3 V or 0							pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Unused pins at V_{CC} or GND
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings**

SN54LVT16835 . . . WD PACKAGE
SN74LVT16835 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16835 is an 18-bit universal bus driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of the clock. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16835 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16835 is characterized for operation from −40°C to 85°C.

PRODUCT PREVIEW

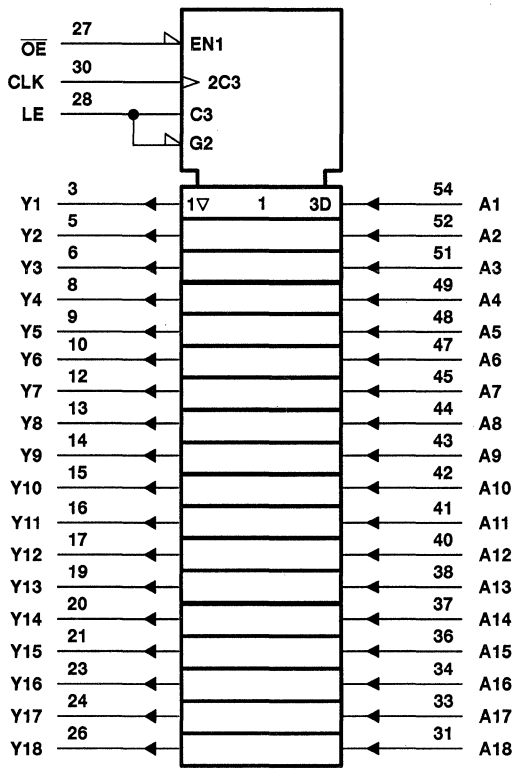
Widebus is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0†
L	L	L	X	Y_0‡

† Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low.
‡ Output level before the indicated steady-state input conditions were established.

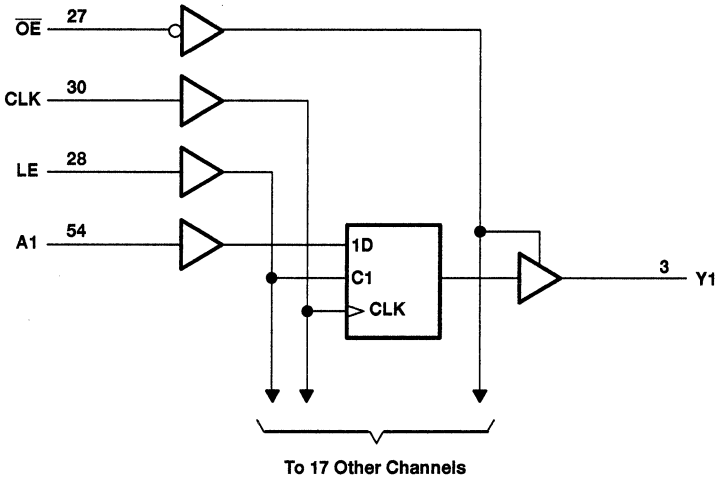
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16835 ..... 96 mA
SN74LVT16835 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16835 ..... 48 mA
SN74LVT16835 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			SN54LVT16835		SN74LVT16835		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

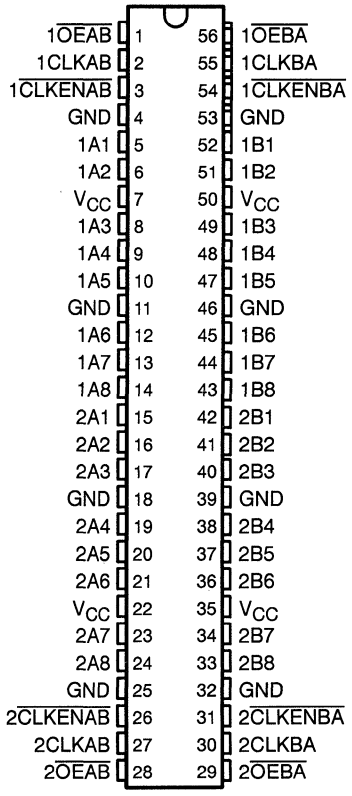
PARAMETER	TEST CONDITIONS			SN54LVT16835		SN74LVT16835		UNIT
				MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA			−1.2		−1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = −100 µA		V_{CC}−0.2		V_{CC}−0.2		V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4		2.4		
	V_{CC} = 3 V	I_{OH} = − 24 mA		2				
		I_{OH} = −32 mA				2		
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2		0.2	V
		I_{OL} = 24 mA			0.5		0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA			0.4		0.4	
		I_{OL} = 32 mA			0.5		0.5	
		I_{OL} = 48 mA			0.55			
		I_{OL} = 64 mA					0.55	
I_I	V_{CC} = 0 or MAX†,	V_I = 5.5 V			10		10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins		±1		±1	
		V_I = V_{CC}	A inputs‡		1		1	
		V_I = 5.5 V			20		20	
		V_I = 0			−5		−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V					±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75		75		µA
		V_I = 2 V		−75		−75		
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			1		1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V			−1		−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.1		0.1	mA
			Outputs low		5		5	
			Outputs disabled		0.1		0.1	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			0.2		0.2	mA
C_i	V_I = 3 V or 0							pF
C_o	V_O = 3 V or 0							pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Unused pins at V_{CC} or GND
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Supports Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT16952 . . . WD PACKAGE
SN74LVT16952 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVT16952 is a 16-bit registered transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

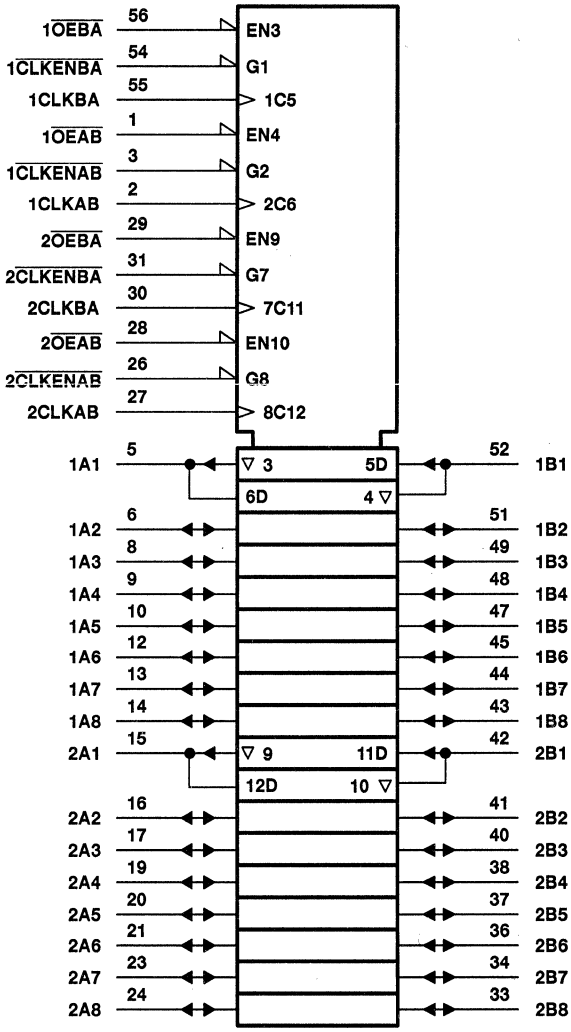
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16952 is characterized for operation from –40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



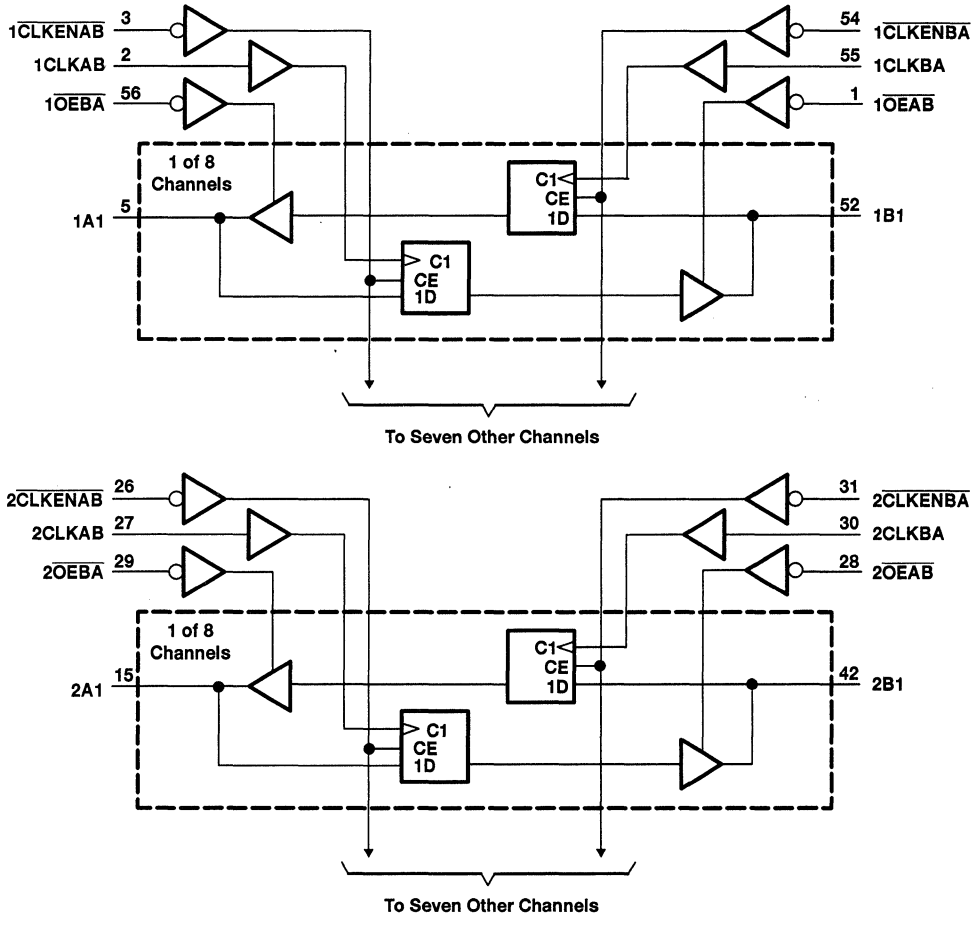
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B_0‡
X	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16952 ..... 96 mA
SN74LVT16952 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16952 ..... 48 mA
SN74LVT16952 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			SN54LVT16952		SN74LVT16952		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16952			SN74LVT16952			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				13			13		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54LVT16952				SN74LVT16952				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration	CLKEN high	3.3		3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK high or low	2.1		2.9		2.1		2.9		ns
		$\overline{CLKEN}$ before CLK, data high or low	1.2		1.6		1.2		1.6		
t_h	Hold time	Data after CLK high or low	0.7		0.7		0.7		0.7		ns
		$\overline{CLKEN}$ after CLK, data high or low	1.4		1.5		1.4		1.5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16952				SN74LVT16952					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		150		150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2	5.4		6.1	2	3.4	5.8		7.1	ns
t_{PHL}			2	5.4		5.7	2	3.4	5.8		6.9	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1	4.7		5.8	1	2.7	5.6		6.7	ns
t_{PZL}			1.2	4.6		5.5	1.2	2.7	6.5		8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.3	5.7		6.1	2.3	3.9	6.3		6.9	ns
t_{PLZ}			2.2	5.2		5.3	2.2	3.9	5.1		5.3	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

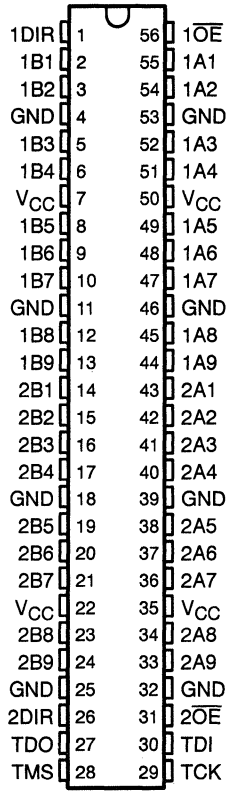
LVT JTAG/IEEE 1149.1

Features	Benefits
• Compatibility with IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) and boundary-scan architecture	• Facilitate testing of complex circuit board assemblies via a 4-wire test access port • No system throughput or cycle time penalty for boundary-scan implementation
• EPIC-IIB™ BiCMOS process with special low-voltage enhancements	• 3.3-V logic family with equivalent drive performance of 5-V ABT logic family – not just a recharacterized, scaled CMOS
• Expanded V_{CC} range from 2.7 V to 3.6 V	• Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation • Functional equivalents to standard ABT devices offer system and test designers flexible integration options
• EIAJ TSSOP, JEDEC SSOP, and EIAJ TQFP fine-pitch surface-mount packaging	• Save valuable board space
• Bus-hold circuitry	• Reduce component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
• 18-bit and 20-bit UBT™ architectures	• Advanced integration, as one UBT™ can replace nearly all common bus-interface logic
• Additional SCOPE™ instructions available such as: – Parallel Signature Analysis (PSA) – Pseudo-Random Pattern Generation (PRPG)	• Built-in self-test feature allows easy upgrade for advanced JTAG test applications
• Test-mode or normal-mode operation	• IEEE Standard 1149.1-1990 protocol can be bypassed for applications not requiring boundary scan
• Members of the Texas Instruments SCOPE™ family of testability products	• Compatible with complete line of system-level test products including controllers, bus monitors, scan path linkers, scan path selectors, application-specific products, and very large-scale integration products
• TI has established an alternate source	• Standardization that comes from a common product approach

Information regarding the tap control state diagram, signal descriptions, and other related JTAG/IEEE 1149.1 information for the 'LVT18245, 'LVT18502, 'LVT182502, 'LVT18504, 'LVT182504, 'LVT18640, 'LVT18646, 'LVT182646, 'LVT18652, and 'LVT182652 is similar to that for the 'ABT18245. Therefore, this information will only be provided in the data sheet for the 'ABT18245 in section 9 of the 1993 ABT data book. Please contact your local TI sales representative for further information.

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18245 . . . WD PACKAGE
SN74LVT18245 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54LVT18245 and SN74LVT18245 scan test devices with 18-bit bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit noninverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

SCOPE and Widebus are trademarks of Texas Instruments Incorporated.

description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT18245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

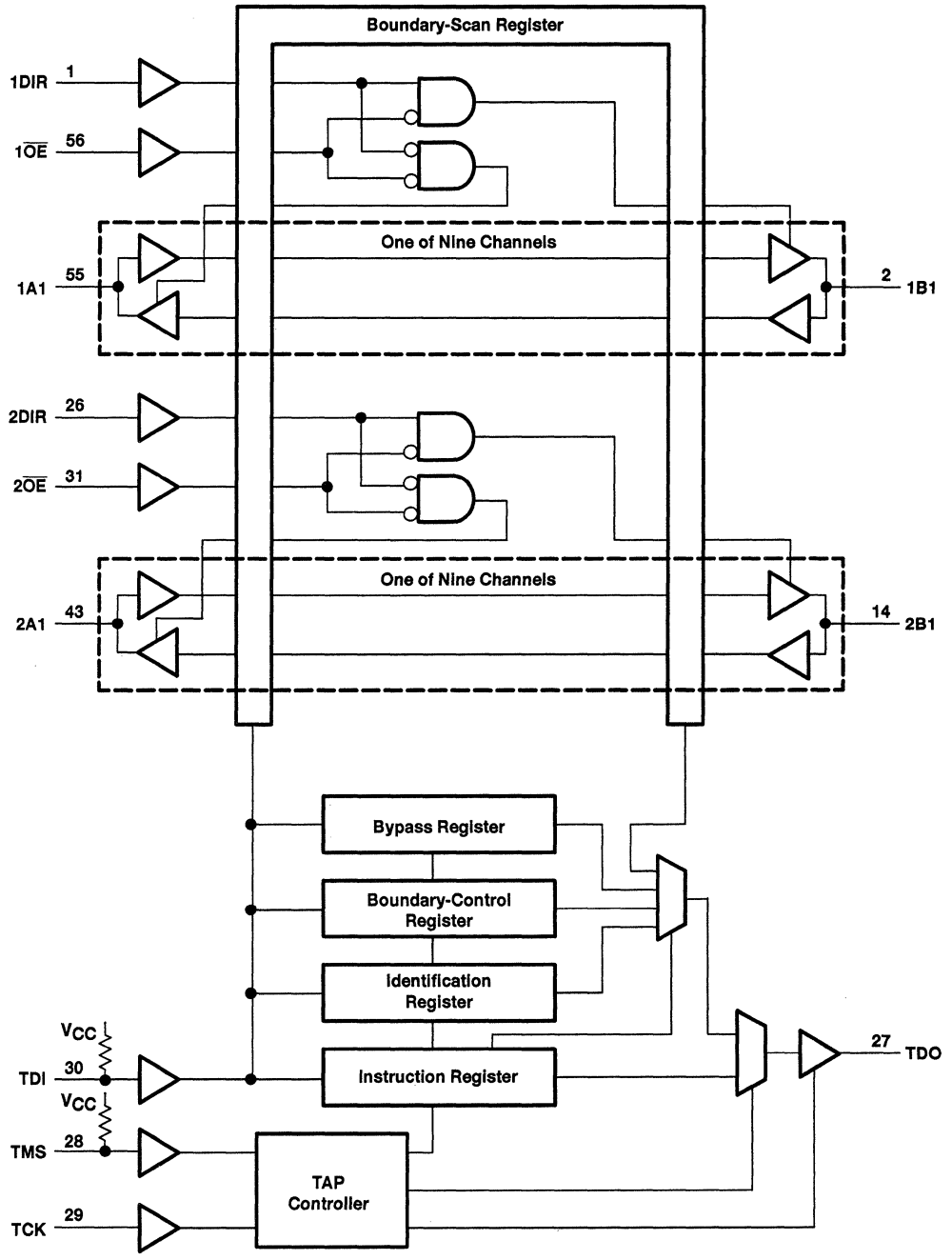
The SN54LVT18245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
GND	Ground
$1\overline{OE}$, $2\overline{OE}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ..... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18245 ..... 96 mA
SN74LVT18245 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18245 ..... 48 mA
SN74LVT18245 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT18245		SN74LVT18245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			SN54LVT18245			SN74LVT18245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	DIR, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				–100			–100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

			SN54LVT18245				SN74LVT18245				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, DIR, or $\overline{OE}$ before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, DIR, or $\overline{OE}$ after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.
4. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18245				SN74LVT18245				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A					1.5	6.5			ns
t_{PHL}							1.5	6.5			
t_{PZH}	$\overline{OE}$	B or A					3	9			ns
t_{PZL}							3	9			
t_{PHZ}	$\overline{OE}$	B or A					3	9.5			ns
t_{PLZ}							3	9.5			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

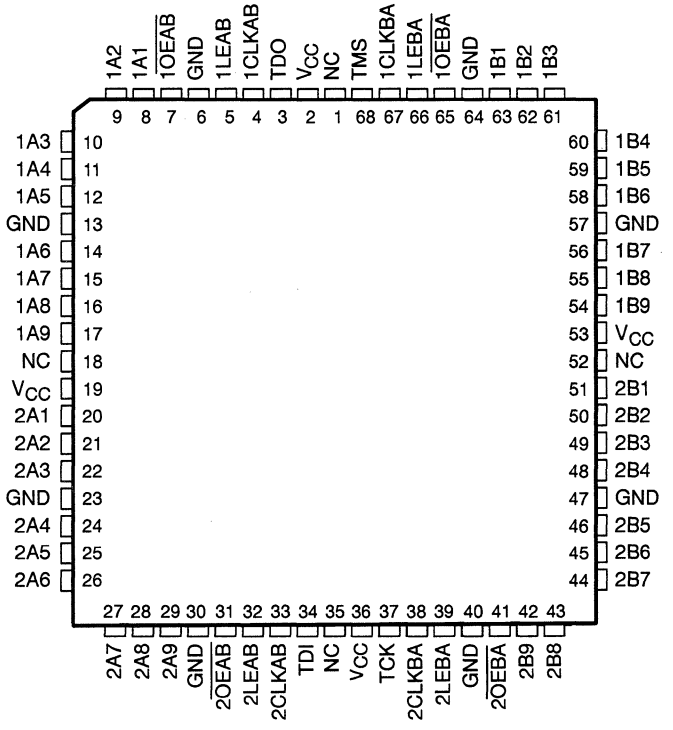
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18245				SN74LVT18245				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK↓						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.
4. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182502 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18502, SN54LVT182502 . . . HV PACKAGE
(TOP VIEW)



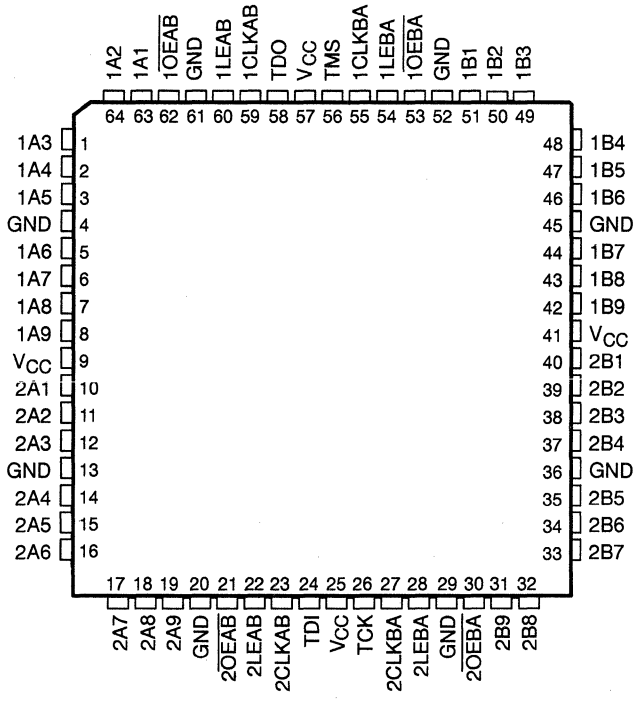
NC – No internal connection

SCOPE, Widebus, and UBT are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

SN74LVT18502, SN74LVT182502 . . . PM PACKAGE
(TOP VIEW)



description

The 'LVT18502 and 'LVT182502 scan test devices with 18-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

PRODUCT PREVIEW

description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182502, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18502 and SN54LVT182502 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT18502 and SN74LVT182502 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

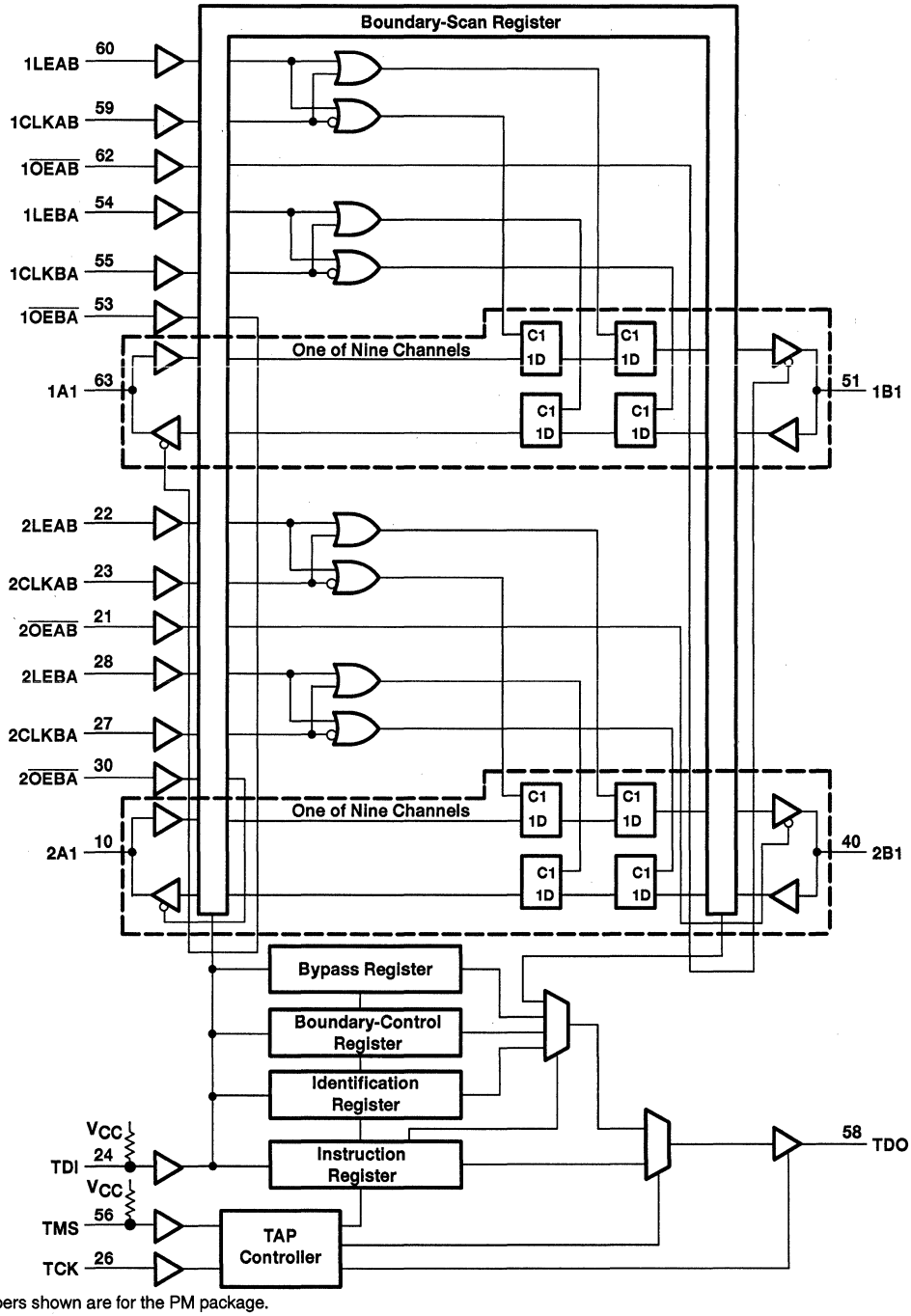
INPUTS				OUTPUT
$\overline{OEAB}$	LEAB	CLKAB	A	B
L	L	L	X	B_0‡
L	L	↑	L	L
L	L	↑	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
1LEAB, 1LEBA, 2LEAB, 2LEBA	Normal-function latch enables. See function table for normal-mode logic.
$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18502 ..... 96 mA
SN54LVT182502 (A port or TDO) ..... 96 mA
SN54LVT182502 (B port) ..... 30 mA
SN74LVT18502 ..... 128 mA
SN74LVT182502 (A port or TDO) ..... 128 mA
SN74LVT182502 (B port) ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18502 ..... 48 mA
SN54LVT182502 (A port or TDO) ..... 48 mA
SN54LVT182502 (B port) ..... 30 mA
SN74LVT18502 ..... 64 mA
SN74LVT182502 (A port or TDO) ..... 64 mA
SN74LVT182502 (B port) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): PM package (see Note 3) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. A 75-mil trace length was used to calculate Θ_{JA}.

recommended operating conditions

			SN54LVT18502		SN74LVT18502		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT18502			SN74LVT18502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LVT18502				SN74LVT18502				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA						0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low						5				ns
		LEAB or LEBA high						5				
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑						5				ns
		A before LEAB↓ or B before LEBA↓	CLK high					5				
			CLK low					5				
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑						0				ns
		A after LEAB↓ or B after LEBA↓						2				

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT18502				SN74LVT18502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502				SN74LVT18502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	7			ns
t_{PHL}							2	7			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	8.5			ns
t_{PHL}							2.5	8.5			
t_{PLH}	LEAB or LEBA	B or A					2.5	9			ns
t_{PHL}							2.5	9			
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2	10			ns
t_{PZL}							2	10			
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2.5	9			ns
t_{PLZ}							2.5	9			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18502				SN74LVT18502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT182502		SN74LVT182502		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port, TDO		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port, TDO		24		32	mA
		B port		12		12	
I_{OL}†	Low-level output current	A port, TDO		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT182502			SN74LVT182502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	A port, TDO	V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
		I_{OH} = − 12 mA	B port	2			2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA	A port, TDO			0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
		I_{OL} = 12 mA	B port			0.8			0.8	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			20			20	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LVT182502			SN74LVT182502			UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
				MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100		MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					5			ns
		LEAB or LEBA high					5			
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5			ns
		A before LEAB↓ or B before LEBA↓	CLK high				5			
			CLK low				5			
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0			ns
		A after LEAB↓ or B after LEBA↓					2			

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT182502			SN74LVT182502			UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
			MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
f_{clock}	Clock frequency	TCK				0	25		MHz
t_w	Pulse duration	TCK high or low				20			ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑				8			ns
		TDI before TCK↑				8			
		TMS before TCK↑				6			
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑				1			ns
		TDI after TCK↑				1			
		TMS after TCK↑				1			
t_d	Delay time	Power up to TCK↑				50			ns
t_r	Rise time	V_{CC} power up				1			µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182502				SN74LVT182502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	8			ns
t_{PHL}							2	8			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			ns
t_{PHL}							2.5	9.5			
t_{PLH}	LEAB or LEBA	B or A					2.5	10			ns
t_{PHL}							2.5	10			
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2	11			ns
t_{PZL}							2	11			
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2.5	9			ns
t_{PLZ}							2.5	9			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

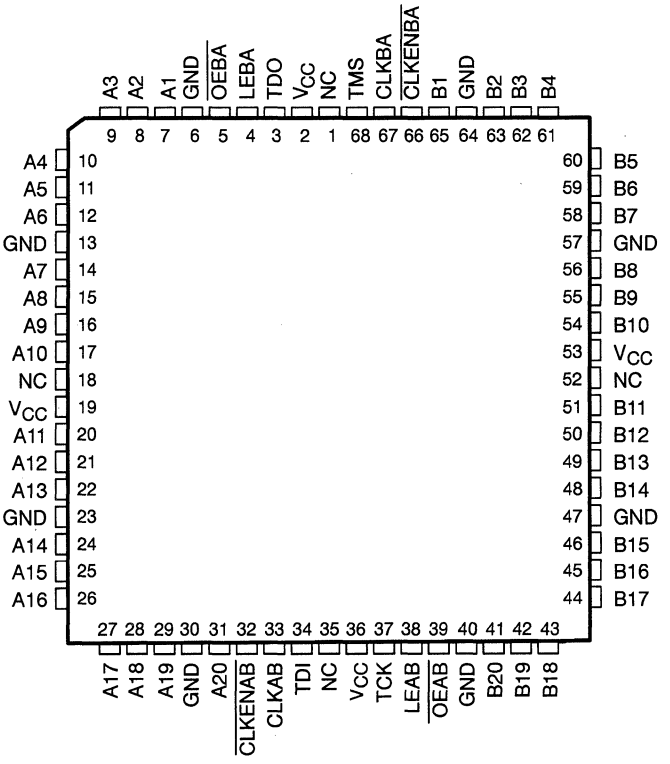
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182502				SN74LVT182502				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	25			ns
t_{PHL}							3	25			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	25			ns
t_{PZL}							3	25			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	25			ns
t_{PLZ}							3	25			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182504 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18504, SN54LVT182504 . . . HV PACKAGE
(TOP VIEW)

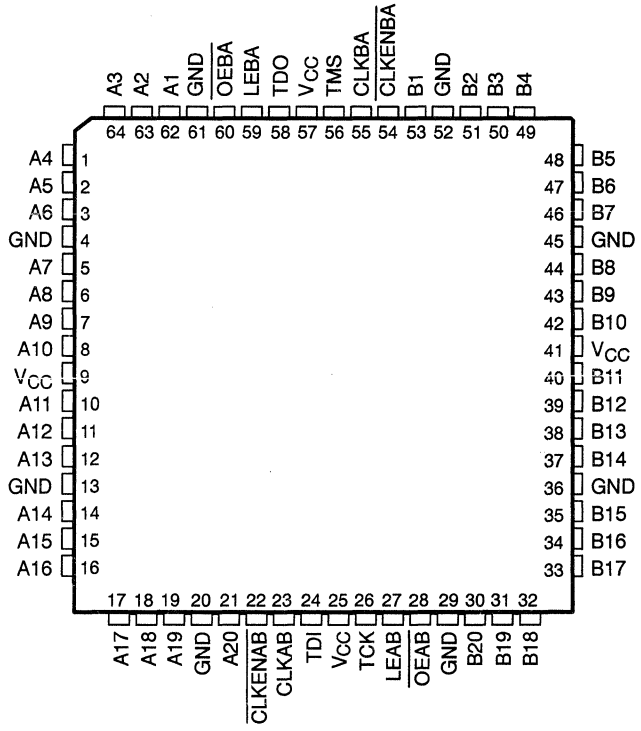


NC – No internal connection

SCOPE, Widebus, and UBT are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW

SN74LVT18504, SN74LVT182504 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT18504 and 'LVT182504 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

description (continued)

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182504, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN54LVT18504 and SN54LVT182504 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT18504 and SN74LVT182504 are characterized for operation from −40°C to 85°C.

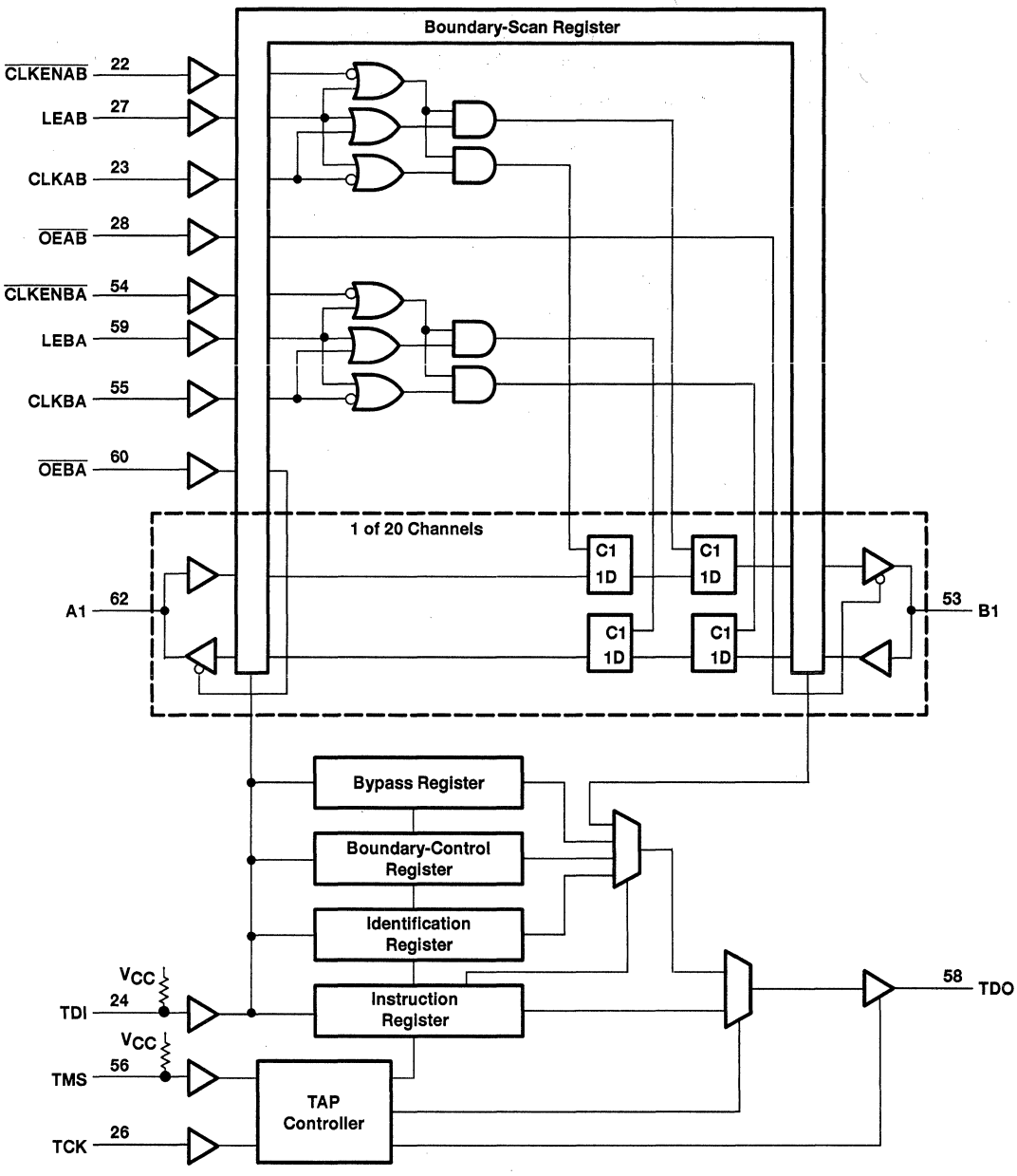
FUNCTION TABLE†
(normal mode, each register)

INPUTS					OUTPUT
$\overline{OEAB}$	LEAB	$\overline{CLKENAB}$	CLKAB	A	B
L	L	L	L	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B_0‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

TERMINAL NAME	DESCRIPTION
A1–A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1–B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
$\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18504 ..... 96 mA
SN54LVT182504 (A port or TDO) ..... 96 mA
SN54LVT182504 (B port) ..... 30 mA
SN74LVT18504 ..... 128 mA
SN74LVT182504 (A port or TDO) ..... 128 mA
SN74LVT182504 (B port) ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18504 ..... 48 mA
SN54LVT182504 (A port or TDO) ..... 48 mA
SN54LVT182504 (B port) ..... 30 mA
SN74LVT18504 ..... 64 mA
SN74LVT182504 (A port or TDO) ..... 64 mA
SN74LVT182504 (B port) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): PM package (see Note 3) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. A 75-mil trace length was used to calculate Θ_{JA}.

recommended operating conditions

			SN54LVT18504		SN74LVT18504		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT18504			SN74LVT18504			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = −24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, $\overline{CLKEN}$, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LVT18504				SN74LVT18504				UNIT
				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA						0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low						5				ns
		LEAB or LEBA	CLK high or low					5				
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑						5				ns
		A before LEAB↓ or B before LEBA↓	CLK high					5				
			CLK low					5				
		$\overline{CLKEN}$ before CLK↑						5				
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑						0				ns
		A after LEAB↓ or B after LEBA↓						2				
		$\overline{CLKEN}$ after CLK↑						0				

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT18504				SN74LVT18504				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18504				SN74LVT18504				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	7			ns
t_{PHL}							2	7			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	8.5			ns
t_{PHL}							2.5	8.5			
t_{PLH}	LEAB or LEBA	B or A					2.5	9			ns
t_{PHL}							2.5	9			
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2	10			ns
t_{PZL}							2	10			
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2.5	9			ns
t_{PLZ}							2.5	9			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18504				SN74LVT18504				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT182504		SN74LVT182504		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port, TDO		−24		−32	mA
		B port		−12		−12	
I_{OL}	Low-level output current	A port, TDO		24		32	mA
		B port		12		12	
I_{OL}†	Low-level output current	A port, TDO		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT182504			SN74LVT182504			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA	A port, TDO	V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
		I_{OH} = – 12 mA	B port	2			2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA	A port, TDO			0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
		I_{OL} = 12 mA	B port			0.8			0.8	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, $\overline{CLKEN}$, LE, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				–100			–100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			20			20	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

				SN54LVT182504		SN74LVT182504		UNIT
				V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA				0 100		MHz
t_w	Pulse duration	CLKAB or CLKBA high or low				5		ns
		LEAB or LEBA	CLK high or low			5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑				5		ns
		A before LEAB↓ or B before LEBA↓	CLK high			5		
			CLK low			5		
		$\overline{CLKEN}$ before CLK↑				5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑				0		ns
		A after LEAB↓ or B after LEBA↓				2		
		$\overline{CLKEN}$ after CLK↑				0		

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT182504		SN74LVT182504		UNIT
			V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 2.7 V	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f_{clock}	Clock frequency	TCK			0 25		MHz
t_w	Pulse duration	TCK high or low			20		ns
t_{su}	Setup time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ before TCK↑			8		ns
		TDI before TCK↑			8		
		TMS before TCK↑			6		
t_h	Hold time	A, B, CLK, $\overline{CLKEN}$, LE, or $\overline{OE}$ after TCK↑			1		ns
		TDI after TCK↑			1		
		TMS after TCK↑			1		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182504				SN74LVT182504				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	8			ns
t_{PHL}							2	8			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			ns
t_{PHL}							2.5	9.5			
t_{PLH}	LEAB or LEBA	B or A					2.5	10			ns
t_{PHL}							2.5	10			
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2	11			ns
t_{PZL}							2	11			
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A					2.5	9			ns
t_{PLZ}							2.5	9			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

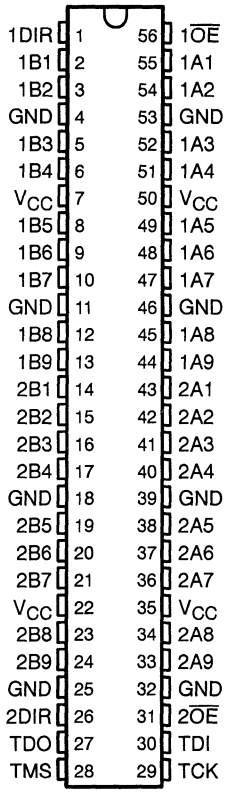
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182504				SN74LVT182504				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	25			ns
t_{PHL}							3	25			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	25			ns
t_{PZL}							3	25			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	25			ns
t_{PLZ}							3	25			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18640 . . . WD PACKAGE
SN74LVT18640 . . . DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The SN54LVT18640 and SN74LVT18640 scan test devices with 18-bit inverting bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit inverting bus transceivers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers.

Data flow is controlled by the direction-control (DIR) and output-enable ($\overline{OE}$) inputs. Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at DIR. The output-enable ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

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description (continued)

In the test mode, the normal operation of the SCOPE™ bus transceivers is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT18640 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

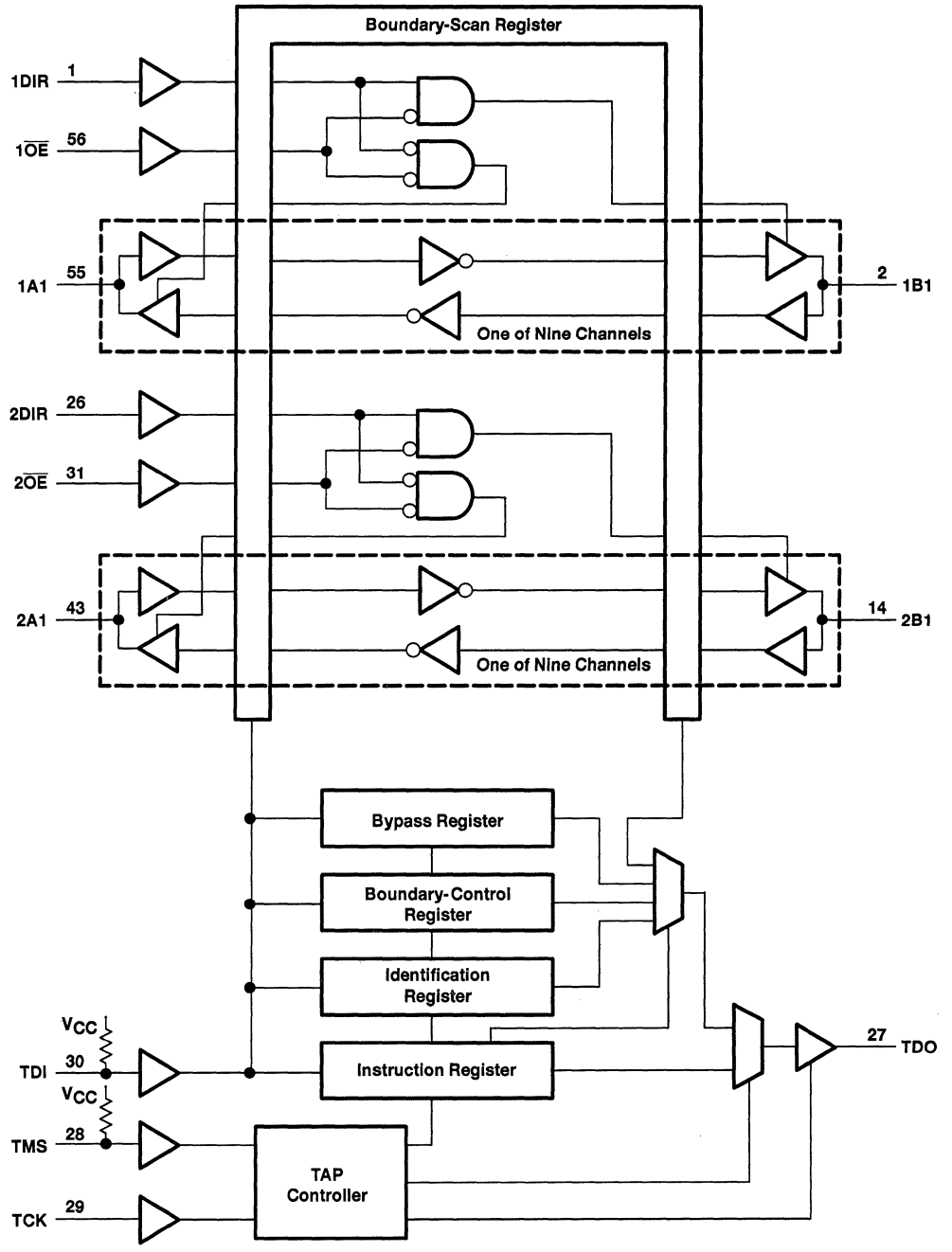
The SN54LVT18640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT18640 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

PRODUCT PREVIEW

functional block diagram



Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
GND	Ground
$1\overline{OE}$, $2\overline{OE}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18640 ..... 96 mA
SN74LVT18640 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18640 ..... 48 mA
SN74LVT18640 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT18640		SN74LVT18640		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS			SN54LVT18640			SN74LVT18640			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	DIR, $\overline{OE}$, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

			SN54LVT18640				SN74LVT18640				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, DIR, or $\overline{OE}$ before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, DIR, or $\overline{OE}$ after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.
4. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18640				SN74LVT18640				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A					1.5	7			ns
t_{PHL}							1.5	7			
t_{PZH}	$\overline{OE}$	B or A					3	9			ns
t_{PZL}							3	9			
t_{PHZ}	$\overline{OE}$	B or A					3	9.5			ns
t_{PLZ}							3	9.5			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 3 and 4)

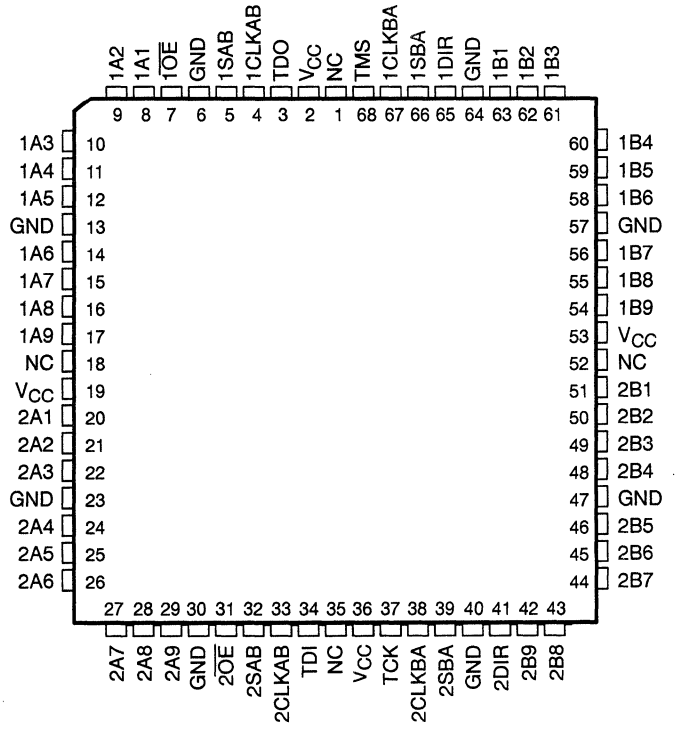
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18640				SN74LVT18640				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK↓						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 3. Product preview specifications are design goals only and are subject to change without notice.
4. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182646 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18646, SN54LVT182646 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

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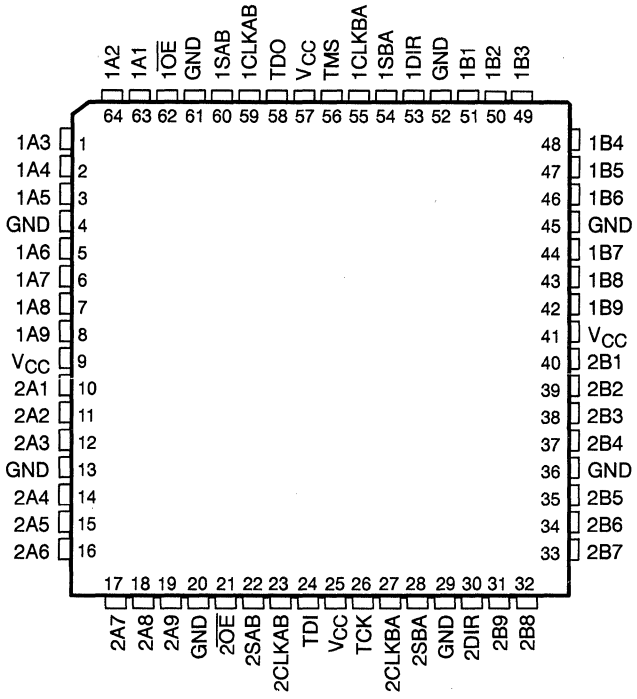
PRODUCT PREVIEW

SN74LVT18646, SN74LVT182646 . . . PM PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'LVT18646 and 'LVT182646 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

description (continued)

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT18646 and 'LVT182646.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182646, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

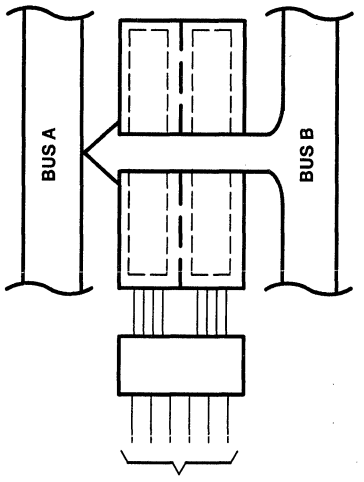
The SN54LVT18646 and SN54LVT182646 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT18646 and SN74LVT182646 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	X	X	H	Output	Input disabled	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	X	X	H	X	Input disabled	Output	Stored A data to B bus

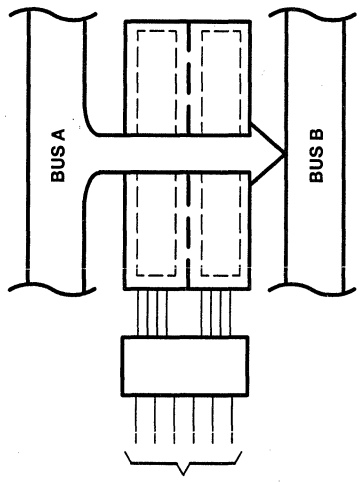
† The data output functions can be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW



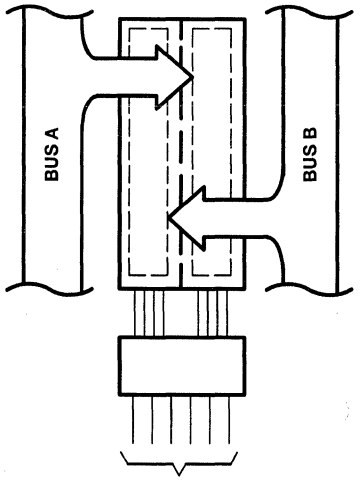
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



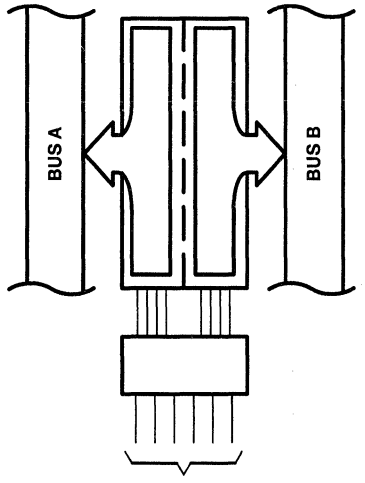
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

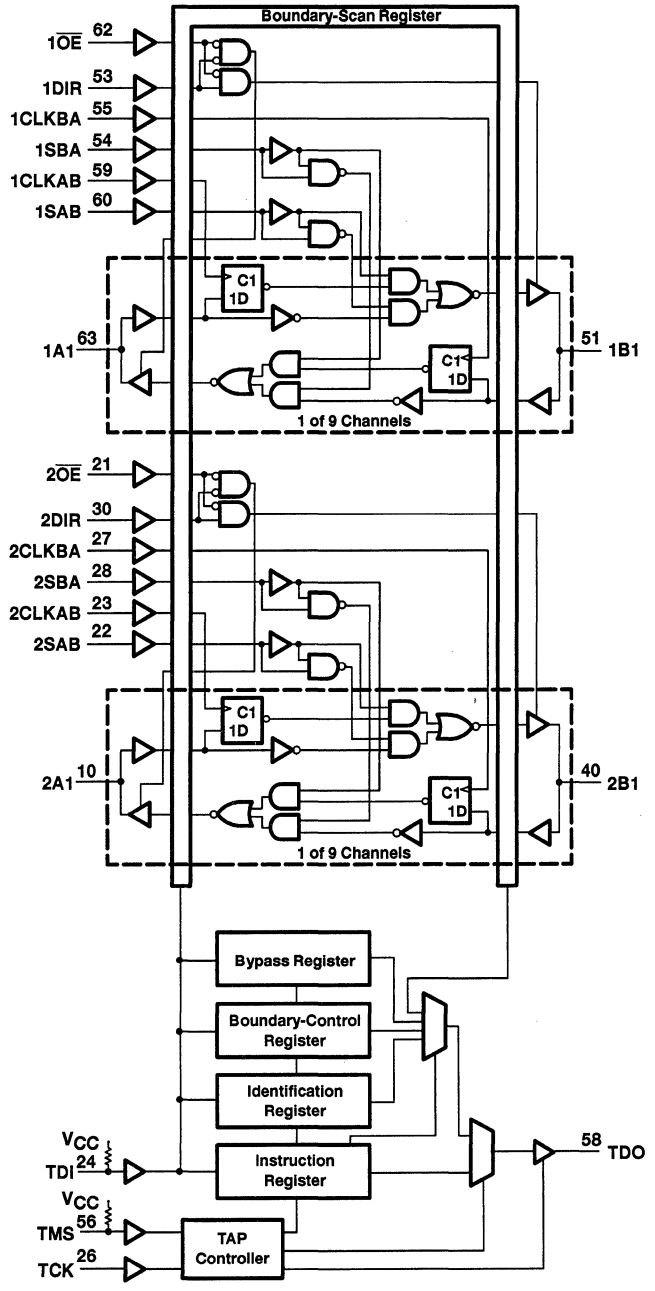


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	H
L	H	X	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
1DIR, 2DIR	Normal-function direction controls. See function table for normal-mode logic.
GND	Ground
$1\overline{OE}$, $2\overline{OE}$	Normal-function output enables. See function table for normal-mode logic.
1SAB, 1SBA, 2SAB, 2SBA	Normal-function select controls. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18646 ..... 96 mA
SN54LVT182646 (A port or TDO) ..... 96 mA
SN54LVT182646 (B port) ..... 30 mA
SN74LVT18646 ..... 128 mA
SN74LVT182646 (A port or TDO) ..... 128 mA
SN74LVT182646 (B port) ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18646 ..... 48 mA
SN54LVT182646 (A port or TDO) ..... 48 mA
SN54LVT182646 (B port) ..... 30 mA
SN74LVT18646 ..... 64 mA
SN74LVT182646 (A port or TDO) ..... 64 mA
SN74LVT182646 (B port) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): PM package (see Note 3) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. A 75-mil trace length was used to calculate Θ_{JA}.

recommended operating conditions

			SN54LVT18646		SN74LVT18646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT18646			SN74LVT18646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, DIR, $\overline{OE}$, S, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				–100			–100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			SN54LVT18646				SN74LVT18646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					5				ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT18646				SN74LVT18646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$ or S before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, DIR, $\overline{OE}$ or S after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18646				SN74LVT18646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	7			ns
t_{PHL}							2	7			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	8.5			ns
t_{PHL}							2.5	8.5			
t_{PLH}	SAB or SBA	B or A					2	9			ns
t_{PHL}							2	9			
t_{PZH}	DIR	B or A					2	10			ns
t_{PZL}							2	10			
t_{PZH}	$\overline{OE}$	B or A					2	10			ns
t_{PZL}							2	10			
t_{PHZ}	DIR	B or A					3	12			ns
t_{PLZ}							3	12			
t_{PHZ}	$\overline{OE}$	B or A					2	11			ns
t_{PLZ}							2	11			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18646				SN74LVT18646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT182646		SN74LVT182646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port, TDO		–24		–32	mA
		B port		–12		–12	
I_{OL}	Low-level output current	A port, TDO		24		32	mA
		B port		12		12	
I_{OL}†	Low-level output current	A port, TDO		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT182646			SN74LVT182646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	A port, TDO	V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = −8 mA	A port, TDO	2.4			2.4			V
	V_{CC} = 3 V	I_{OH} = −24 mA	A port, TDO	2						V
		I_{OH} = −32 mA	A port, TDO				2			V
		I_{OH} = −12 mA	B port	2			2			V
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA	A port, TDO			0.2			0.2	V
		I_{OL} = 24 mA	A port, TDO			0.5			0.5	V
	V_{CC} = 3 V	I_{OL} = 16 mA	A port, TDO			0.4			0.4	V
		I_{OL} = 32 mA	A port, TDO			0.5			0.5	V
		I_{OL} = 48 mA	A port, TDO			0.55				V
		I_{OL} = 64 mA	A port, TDO						0.55	V
		I_{OL} = 12 mA	B port			0.8			0.8	V
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, DIR, $\overline{OE}$, S, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V	CLK, DIR, $\overline{OE}$, S, TCK			10			10	µA
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	µA
		V_I = V_{CC}	TDI, TMS			1			1	µA
		V_I = 0	TDI, TMS			−100			−100	µA
		V_I = 5.5 V	A or B ports§			20			20	µA
		V_I = V_{CC}	A or B ports§			1			1	µA
		V_I = 0	A or B ports§			−5			−5	µA
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V	A or B ports	−75			−75			µA
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			20			20	mA
			Outputs disabled			2			2	mA
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			SN54LVT182646				SN74LVT182646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					5				ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT182646				SN74LVT182646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$ or S before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, DIR, $\overline{OE}$ or S after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182646				SN74LVT182646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	8			ns
t_{PHL}							2	8			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			ns
t_{PHL}							2.5	9.5			
t_{PLH}	SAB or SBA	B or A					2	10			ns
t_{PHL}							2	10			
t_{PZH}	DIR	B or A					2	11			ns
t_{PZL}							2	11			
t_{PZH}	$\overline{OE}$	B or A					2	11			ns
t_{PZL}							2	11			
t_{PHZ}	DIR	B or A					3	12			ns
t_{PLZ}							3	12			
t_{PHZ}	$\overline{OE}$	B or A					2	11			ns
t_{PLZ}							2	11			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

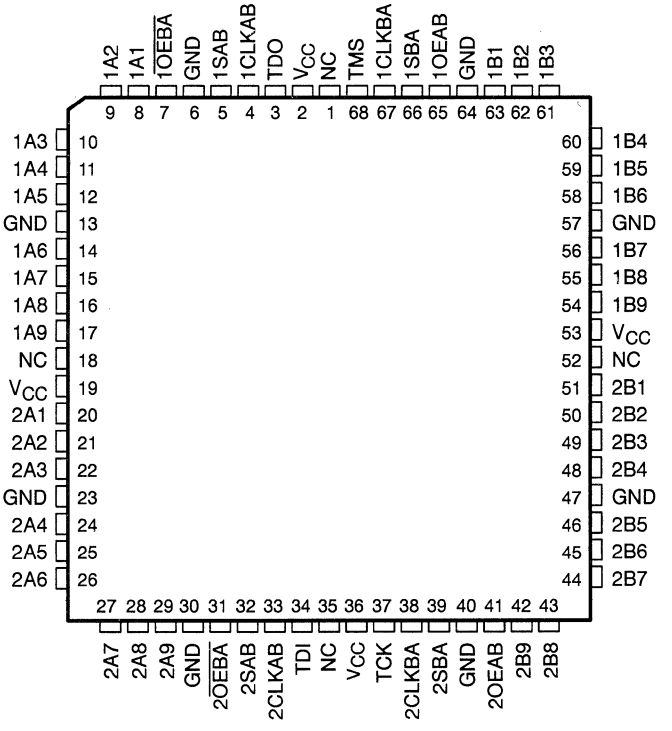
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182646				SN74LVT182646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	25			ns
t_{PHL}							3	25			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	25			ns
t_{PZL}							3	25			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	25			ns
t_{PLZ}							3	25			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- Members of the Texas Instruments *SCOPE*™ Family of Testability Products
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Include D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- B-Port Outputs of 'LVT182652 Devices Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- *SCOPE*™ Instruction Set
  - IEEE Standard 1149.1-1990 Required Instructions and Optional CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs
  - Pseudo-Random Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes
- Packaged in 64-Pin Plastic Thin Quad Flat (PM) Packages Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacings

SN54LVT18652, SN54LVT182652 . . . HV PACKAGE
(TOP VIEW)



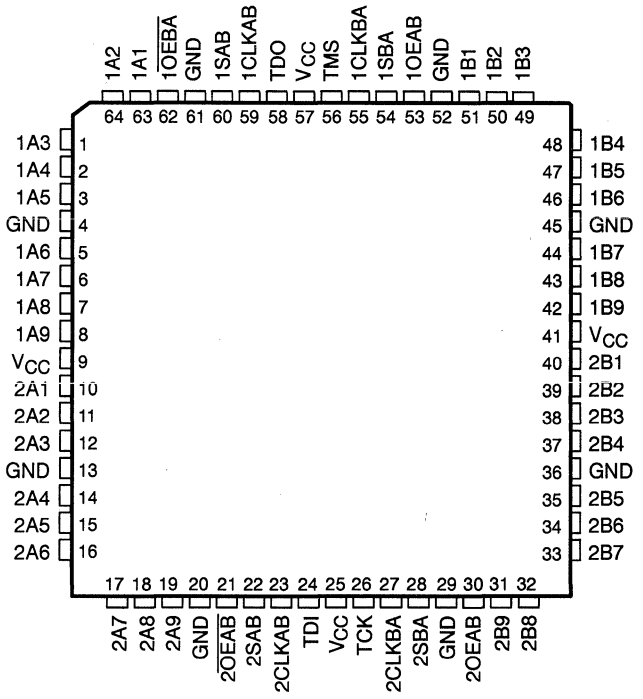
NC – No internal connection

SCOPE and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

SN74LVT18652, SN74LVT182652 . . . PM PACKAGE
(TOP VIEW)



description

The 'LVT18652 and 'LVT182652 scan test devices with 18-bit bus transceivers and registers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, these devices are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, these devices are 18-bit bus transceivers and registers that allow for multiplexed transmission of data directly from the input bus or from the internal registers. They can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and $\overline{\text{OEBA}}$) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state.

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description (continued)

Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and $\overline{\text{OEBA}}$ inputs. Since the $\overline{\text{OEBA}}$ input is active-low, the A outputs are active when $\overline{\text{OEBA}}$ is low and are in the high-impedance state when $\overline{\text{OEBA}}$ is high. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT18652 and 'LVT182652.

In the test mode, the normal operation of the SCOPE™ bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs of 'LVT182652, which are designed to source or sink up to 12 mA, include 25-Ω series resistors to reduce overshoot and undershoot.

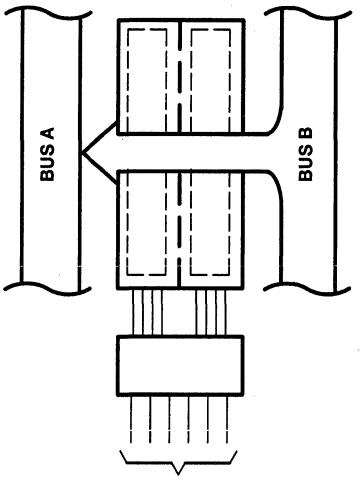
The SN54LVT18652 and SN54LVT182652 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT18652 and SN74LVT182652 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A9	B1 THRU B9	
L	H	L	L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified†	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified†	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	X	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	X	X	H	X	Input	Output	Stored A data to B bus
H	L	X	X	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

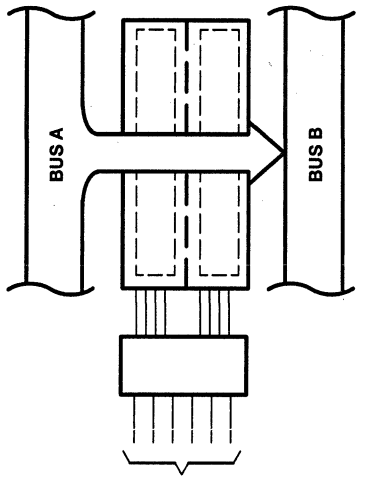
† The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

PRODUCT PREVIEW



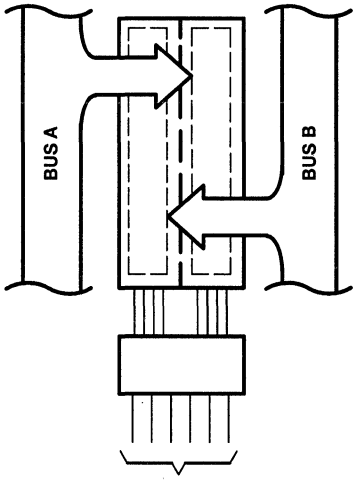
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



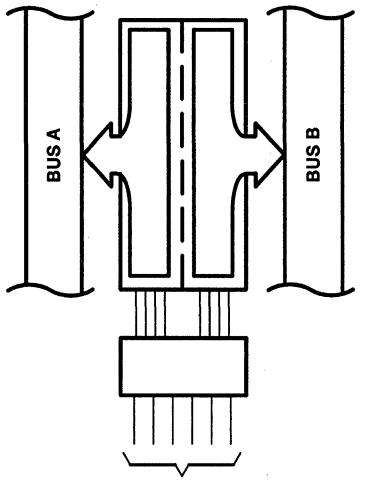
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

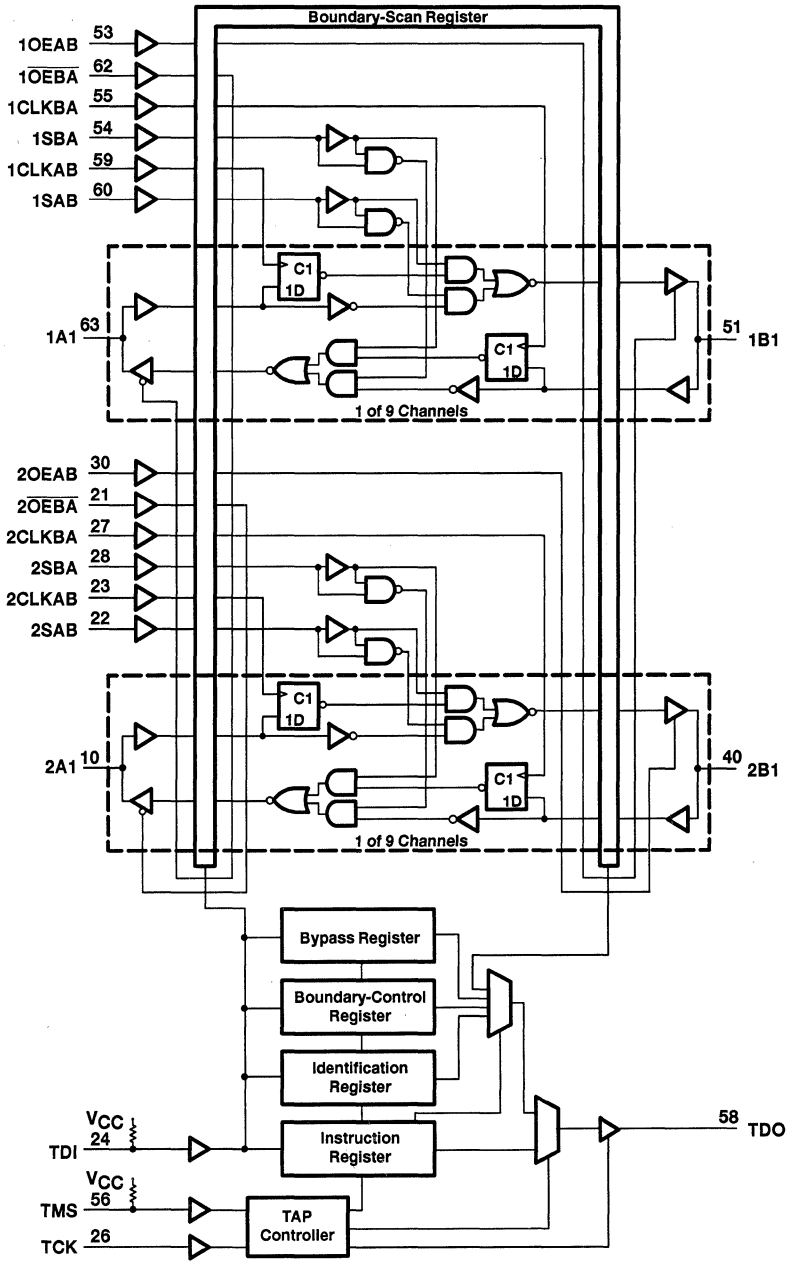


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	X	X	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

functional block diagram



Pin numbers shown are for the PM package.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	DESCRIPTION
1A1–1A9, 2A1–2A9	Normal-function A-bus I/O ports. See function table for normal-mode logic.
1B1–1B9, 2B1–2B9	Normal-function B-bus I/O ports. See function table for normal-mode logic.
1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
GND	Ground
1OEAB, 2OEAB	Normal-function active-high output enables. See function table for normal-mode logic.
$1\overline{OEBA}$, $2\overline{OEBA}$	Normal-function active-low output enables. See function table for normal-mode logic.
1SAB, 1SBA, 2SAB, 2SBA	Normal-function select controls. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT18652 ..... 96 mA
SN54LVT182652 (A port or TDO) ..... 96 mA
SN54LVT182652 (B port) ..... 30 mA
SN74LVT18652 ..... 128 mA
SN74LVT182652 (A port or TDO) ..... 128 mA
SN74LVT182652 (B port) ..... 30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT18652 ..... 48 mA
SN54LVT182652 (A port or TDO) ..... 48 mA
SN54LVT182652 (B port) ..... 30 mA
SN74LVT18652 ..... 64 mA
SN74LVT182652 (A port or TDO) ..... 64 mA
SN74LVT182652 (B port) ..... 30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): PM package (see Note 3) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.
3. A 75-mil trace length was used to calculate Θ_{JA}.

recommended operating conditions

			SN54LVT18652		SN74LVT18652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}‡	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT18652			SN74LVT18652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, OEAB, $\overline{OEBA}$, S, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				−100			−100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			15			15	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			SN54LVT18652				SN74LVT18652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					5				ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT18652				SN74LVT18652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, OEAB, $\overline{OEBA}$ or S before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, OEAB, $\overline{OEBA}$ or S after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18652				SN74LVT18652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	7			ns
t_{PHL}							2	7			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	8.5			ns
t_{PHL}							2.5	8.5			
t_{PLH}	SAB or SBA	B or A					2	9			ns
t_{PHL}							2	9			
t_{PZH}	OEAB or $\overline{OEBA}$	B or A					2	10			ns
t_{PZL}							2	10			
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A					1.5	11			ns
t_{PLZ}							1.5	11			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT18652				SN74LVT18652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	22			ns
t_{PHL}							3	22			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	22			ns
t_{PZL}							3	22			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	22			ns
t_{PLZ}							3	22			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

recommended operating conditions

			SN54LVT182652		SN74LVT182652		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port, TDO		–24		–32	mA
		B port		–12		–12	
I_{OL}	Low-level output current	A port, TDO		24		32	mA
		B port		12		12	
I_{OL}†	Low-level output current	A port, TDO		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			SN54LVT182652 MIN	SN54LVT182652 TYP†	SN54LVT182652 MAX	SN74LVT182652 MIN	SN74LVT182652 TYP†	SN74LVT182652 MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA	A port, TDO	V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = –32 mA					2			
		I_{OH} = – 12 mA	B port	2			2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA	A port, TDO			0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
		I_{OL} = 12 mA	B port			0.8			0.8	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	CLK, OEAB, $\overline{OEBA}$, S, TCK			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	TDI, TMS			50			50	
		V_I = V_{CC}				1			1	
		V_I = 0				–100			–100	
		V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			2			2	mA
			Outputs low			20			20	
			Outputs disabled			2			2	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				11			11		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
NOTE 4: Product preview specifications are design goals only and are subject to change without notice.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

			SN54LVT182652				SN74LVT182652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLKAB or CLKBA					0	100			MHz
t_w	Pulse duration	CLKAB or CLKBA high or low					5				ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑					5				ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑					0				ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

			SN54LVT182652				SN74LVT182652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK					0	25			MHz
t_w	Pulse duration	TCK high or low					20				ns
t_{su}	Setup time	A, B, CLK, OEAB, $\overline{OEBA}$ or S before TCK↑					8				ns
		TDI before TCK↑					8				
		TMS before TCK↑					6				
t_h	Hold time	A, B, CLK, OEAB, $\overline{OEBA}$ or S after TCK↑					1				ns
		TDI after TCK↑					1				
		TMS after TCK↑					1				
t_d	Delay time	Power up to TCK↑					50				ns
t_r	Rise time	V_{CC} power up					1				µs

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182652				SN74LVT182652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA						100				MHz
t_{PLH}	A or B	B or A					2	8			ns
t_{PHL}							2	8			
t_{PLH}	CLKAB or CLKBA	B or A					2.5	9.5			ns
t_{PHL}							2.5	9.5			
t_{PLH}	SAB or SBA	B or A					2	10			ns
t_{PHL}							2	10			
t_{PZH}	OEAB or $\overline{OEBA}$	B or A					2	11			ns
t_{PZL}							2	11			
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A					1.5	11			ns
t_{PLZ}							1.5	11			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT182652				SN74LVT182652				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK						25				MHz
t_{PLH}	TCK↓	A or B					3	25			ns
t_{PHL}							3	25			
t_{PLH}	TCK↓	TDO					2	12			ns
t_{PHL}							2	12			
t_{PZH}	TCK↓	A or B					3	25			ns
t_{PZL}							3	25			
t_{PZH}	TCK↓	TDO					2	12			ns
t_{PZL}							2	12			
t_{PHZ}	TCK↓	A or B					3	25			ns
t_{PLZ}							3	25			
t_{PHZ}	TCK↓	TDO					2	15			ns
t_{PLZ}							2	15			

NOTES: 4. Product preview specifications are design goals only and are subject to change without notice.
5. Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

GTL TRANSCEIVERS AND BACKPLANE DRIVERS

Features	Benefits
• High-speed GTL/TTL translating	• 3.3-V logic family with equivalent speed and drive performance of 5-V ABT logic family – not just a recharacterized or scaled CMOS
• Output edge-rate control (OEC™) options	• Complete input and output compatibility with 5-V signals combined with a pure 3.3-V internal supply signal – provides bidirectional 3-V to 5-V translation
• EPIC-IIB™ BiCMOS process with special low-voltage enhancements	• Reduces component count by eliminating need for external pullup or pulldown resistors on I/O pins configured as inputs left unused or floating
• Mixed-mode signal operations on A port	• Reduces disabled static power consumption (I_{CCZ}) to as little as 0.1 mA for power-conscious portable and battery-powered equipment
• Bus-hold circuitry	• 16- and 18-bit densities for flexible integration
• Power-on-demand active feedback circuitry	• Space-saving and height-saving surface-mount package options, pin compatible with existing 5-V families for easy conversion
• Widebus™ and UBT™ architectures	• Ideal for high-speed bus applications
• JEDEC SSOP (Widebus™) and EIAJ TSSOP (Shrink Widebus™) packaging	• Standardization that comes from a common product approach

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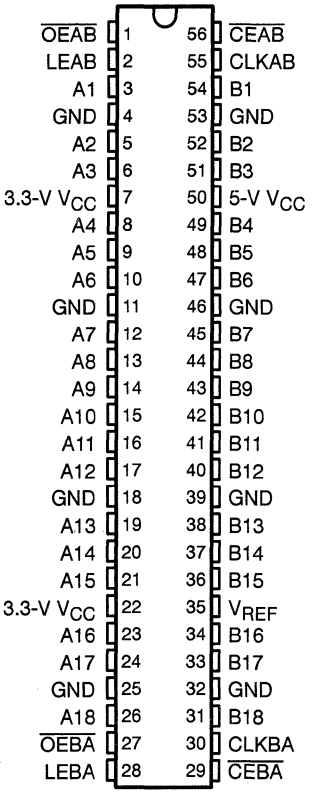
- **Translates Between GTL Signal Levels and LVCMOS, LVTTL, or 5-V TTL Signal Levels**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **State-of-the-Art BiCMOS Design for Low-Static Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16611 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

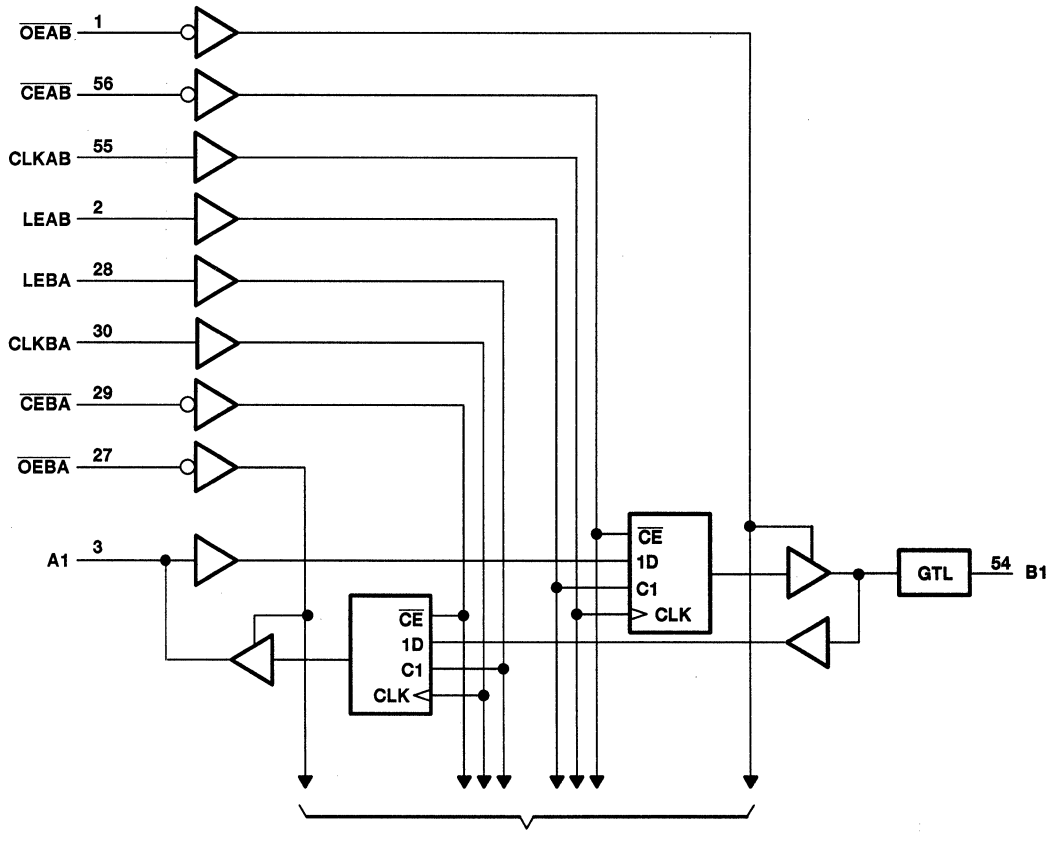
Widebus and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS					OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0‡	
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.
§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3-V V_{CC} ..... −0.5 V to 4.6 V
Supply voltage range, 5-V V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ..... −0.5 V to 7 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	
V_{REF}	Supply voltage			0.8		V
V_I	Input voltage	B port			V_{CC}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} +50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} −50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A port			−32	mA
I_{OL}	Low-level output current	A port‡			64	mA
		B port			40	
T_A	Operating free-air temperature		0		70	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = −18 mA			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC} − 0.2			V
		V_{CC} = 3.15 V	I_{OH} = − 8 mA	2.4			
			I_{OH} = − 32 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B port	V_{CC} = 3.15 V,	I_{OL} = 40 mA			0.4	
I_I	Control pins	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10	µA
	A port§	V_{CC} = 3.45 V	V_I = 5.5 V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			−5	
	B port	V_{CC} = 3.45 V	V_I = V_{CC}			5	
			V_I = 0			−5	
I_{off}	A port	V_{CC} = 0	V_I or V_O = 0 to 4.5 V			100	µA
	B port		V_I or V_O = 0 to 1.2 V			100	
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	−75			
I_{OZH}	A port	V_{CC} = 3.45 V	V_O = 3 V			1	µA
	B port		V_O = 1.2 V			10	
I_{OZL}	A port	V_{CC} = 3.45 V	V_O = 0.5 V			−1	µA
	B port		V_O = 0.4 V			−10	
I_{CC}	A port to B port	V_{CC} = 3.45 V, V_I = V_{CC} or GND	I_O = 0,				mA
	B port to A port						
	Outputs disabled						
ΔI_{CC}¶		V_{CC} = 3.45 V, A or control inputs at V_{CC} or GND	One input at 2.7 V,			1	mA
C_i	Control pins	V_I = 3.15 V or 0			4		pF
C_{io}	A port	V_O = 3.15 V or 0			10		pF
C_{io}	B port	Per IEEE1194.0-1991				5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	LEAB or LEBA high			ns
		CLKAB or CLKBA high or low			
t_{su}	Setup time	A before CLKAB↑	1.5		ns
		B before CLKAB↑	3		
		A before LEAB↓	0.5		
		B before LEBA↓	1.5		
		$\overline{CEAB}$ before CLKAB↑			
		$\overline{CEBA}$ before CLKBA↑			
		$\overline{CEAB}$ before LEAB↓			
		$\overline{CEBA}$ before LEBA↓			
t_h	Hold time	A after CLKAB↑	1		ns
		B after CLKAB↑	0		
		A after LEAB↓	2.5		
		B after LEBA↓	2		
		$\overline{CEAB}$ after CLKAB↑			
		$\overline{CEBA}$ after CLKBA↑			
		$\overline{CEAB}$ after LEAB↓			
		$\overline{CEBA}$ after LEBA↓			

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Note 3)

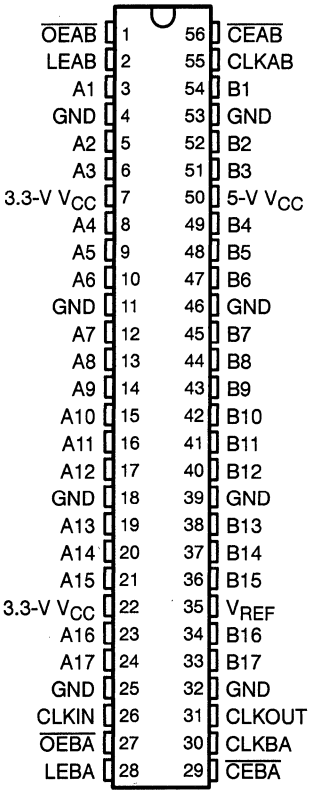
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	A	B			3.2	ns
t_{PHL}					3.2	
t_{PLH}	LEAB	B			4	ns
t_{PHL}					4	
t_{PLH}	CLKAB	B			4.3	ns
t_{PHL}					4.3	
t_{PLH}	$\overline{OEAB}$	B			4.5	ns
t_{PHL}					4.5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.7		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.6		ns
t_{PLH}	B	A			5.7	ns
t_{PHL}					4	
t_{PLH}	LEBA	A			5	ns
t_{PHL}					3.8	
t_{PLH}	CLKBA	A			5.2	ns
t_{PHL}					4.6	
t_{EN}	$\overline{OEBA}$	A			6	ns
t_{DIS}					6	

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- **Translates Between GTL Signal Levels and LVCMOS, LVTTL, or 5-V TTL Signal Levels**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation on A Port (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **State-of-the-Art BiCMOS Design for Low-Static Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 17-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. It provides for a copy of CLKAB at GTL logic levels (CLKOUT). It also provides a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the chip-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16615 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

Widebus and UBT are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS					OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H or L	X	B_0‡	
L	L	L	H or L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

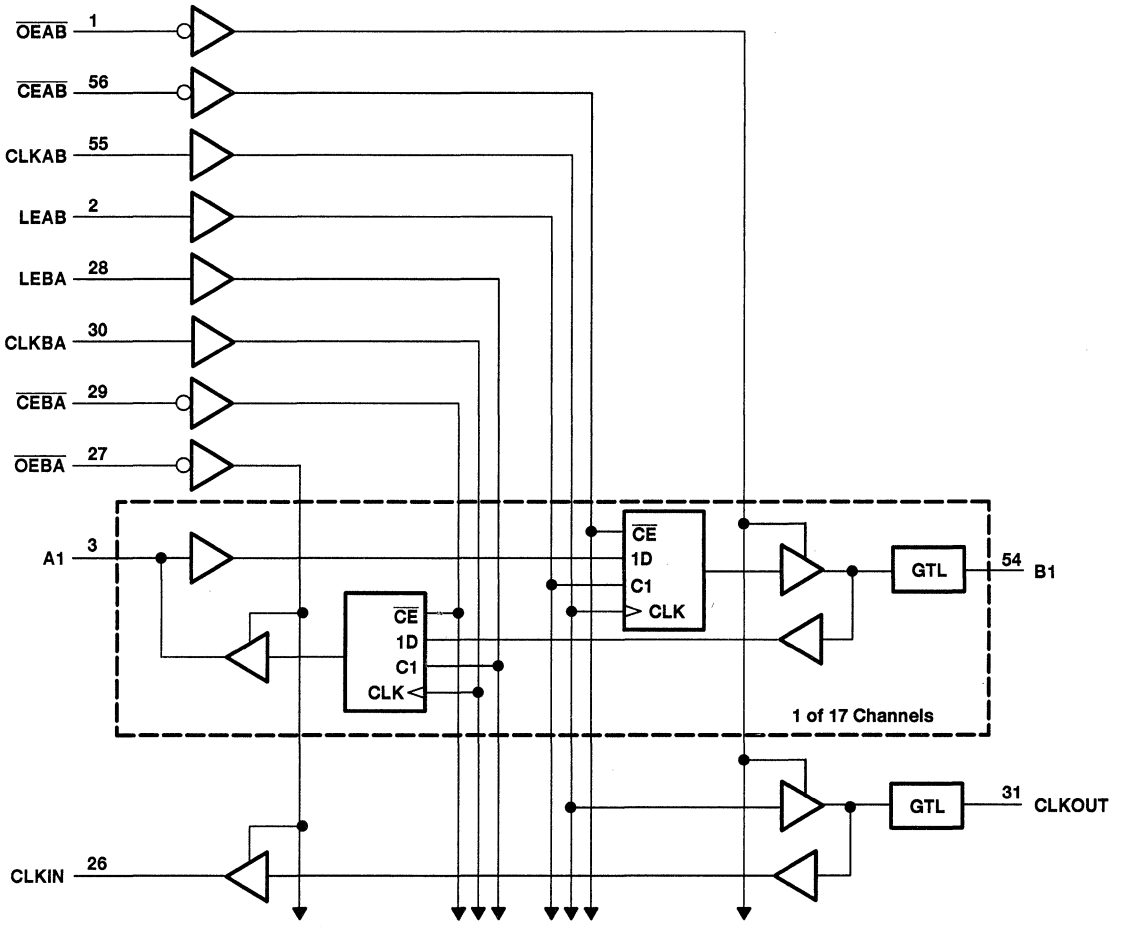
† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, 3.3 V, V_{CC} ..... −0.5 V to 4.6 V
Supply voltage range, 5 V, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

PRODUCT PREVIEW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	
V_{REF}	Supply voltage			0.8		V
V_I	Input voltage	B port			V_{CC}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF} − 50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A port			−32	mA
I_{OL}	Low-level output current	A port‡			64	mA
		B port			40	
T_A	Operating free-air temperature		0		70	°C

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = −18 mA			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC} − 0.2			V
		V_{CC} = 3.15 V	I_{OH} = − 8 mA	2.4			
			I_{OH} = − 32 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	V
			I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B port	V_{CC} = 3.15 V,	I_{OL} = 40 mA			0.4	
I_I	Control pins	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10	µA
	A port§	V_{CC} = 3.45 V	V_I = 5.5 V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			−5	
	B port	V_{CC} = 3.45 V	V_I = V_{CC}			5	
			V_I = 0			−5	
I_{off}	A port	V_{CC} = 0	V_I or V_O = 0 to 4.5 V			100	µA
	B port		V_I or V_O = 0 to 1.2 V			100	
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	−75			
I_{OZH}	A port	V_{CC} = 3.45 V	V_O = 3 V			1	µA
	B port		V_O = 1.2 V			10	
	CLKIN		V_O = 3 V			5	
I_{OZL}	A port	V_{CC} = 3.45 V	V_O = 0.5 V			−1	µA
	B port		V_O = 0.4 V			−10	
	CLKIN		V_O = 0.5 V			−5	
I_{CC}	A port to B port	V_{CC} = 3.45 V, V_I = V_{CC} or GND	I_O = 0,				mA
	B port to A port						
	Outputs disabled						
ΔI_{CC}¶		V_{CC} = 3.45 V, A or control inputs at V_{CC} or GND	One input at 2.7 V,			1	mA
C_i	Control pins	V_I = 3.15 V or 0			4		pF
C_{io}	A port	V_O = 3.15 V or 0			10		pF
C_{io}	B port	Per IEEE1194.0-1991				5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW

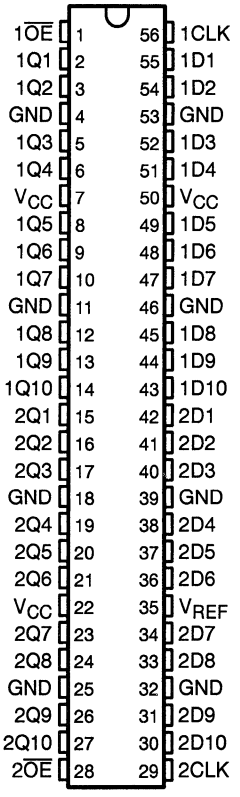
timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	150	MHz
t_w	Pulse duration	LEAB or LEBA high			ns
		CLKAB or CLKBA high or low			
t_{su}	Setup time	A before CLKAB↑	1.5		ns
		B before CLKAB↑	3		
		A before LEAB↓	0.5		
		B before LEBA↓	1.5		
		$\overline{CEAB}$ before CLKAB↑			
		$\overline{CEBA}$ before CLKBA↑			
		$\overline{CEAB}$ before LEAB↓			
		$\overline{CEBA}$ before LEBA↓			
t_h	Hold time	A after CLKAB↑	1		ns
		B after CLKAB↑	0		
		A after LEAB↓	2.5		
		B after LEBA↓	2		
		$\overline{CEAB}$ after CLKAB↑			
		$\overline{CEBA}$ after CLKBA↑			
		$\overline{CEAB}$ after LEAB↓			
		$\overline{CEBA}$ after LEBA↓			

PRODUCT PREVIEW

- ***EPIC-IIB*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Provides GTL Signals Levels on Both Inputs and Outputs**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74GTL16921 has 20 single-bit flip-flops which are designed to provide terminated GTL logic levels.

The device can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. The SN74GTL16921 provides true data at the Q outputs on the positive transition of the clock (CLK) input.

The output-enable ($\overline{OE}$) input can be used to place the outputs in a high state. The output-enable input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74GTL16921 is characterized for operation from 0°C to 70°C.

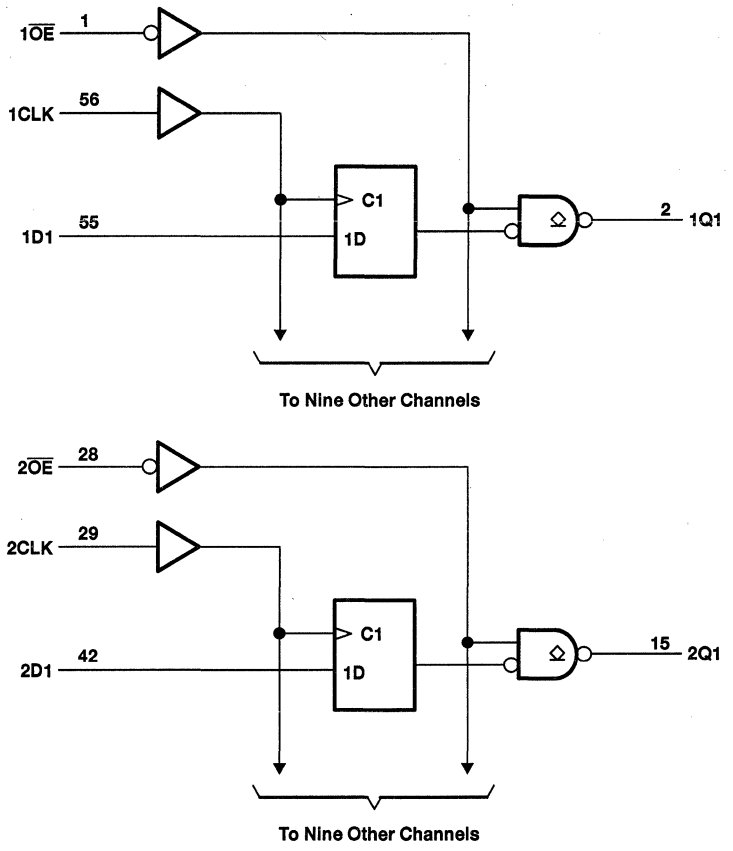
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

EPIC-IIB and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 4.6 V
Current into any output in the low state, I_O	80 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > 0$)	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package	1 W
DL package	1.4 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		3.6	V
V_{REF}	Supply voltage	2/3 V_{CC} – 2%	0.8	2/3 V_{CC} + 2%	V
V_I	Input voltage	0		V_{CC}	V
V_{OH}	High-level output voltage			3.6	V
V_{IH}	High-level input voltage	V_{REF} +50 mV			V
V_{IL}	Low-level input voltage			V_{REF} – 50 mV	V
I_{IK}	Input clamp current			–18	mA
I_{OL}	Low-level output current			40	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA			–1.2	V
V_{OL}		V_{CC} = 3 V,	I_{OL} = 40 mA			0.4	V
I_I		V_{CC} = 3 V	V_I = V_{CC}			5	µA
			V_I = 0			–5	
I_{OH}		V_{CC} = 3 V,	V_{OH} = 3.6 V				µA
I_{CC}	Outputs high	V_{CC} = 3 V,	I_O = 0,				mA
	Outputs low	V_I = V_{CC} or GND					
C_i		Per IEEE1194.0-1991			4		pF
C_o		Per IEEE1194.0-1991			6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW

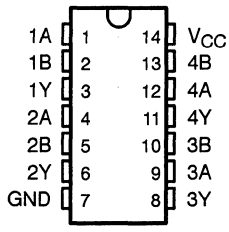
LVC MSI AND OCTALS

Features	Benefits
• 0.8-μ EPIC-II™ CMOS process	• High-performance propagation delays as fast as 6.5 ns
• No input-diode clamp to V_{CC}	• Saves power, extends battery life
• Very low standby current (20 μA)	
• –24-mA/24-mA drive current	• Drives transmission lines down to 50 Ω
• 2.7-V to 3.6-V V_{CC} range	• Fully characterized for unregulated battery operation
• SOIC, EIAJ SSOP, and TSSOP packaging	• Saves board space and weight; TSSOP compatible with PCMCIA standards
• TI has established two worldwide alternate sources	• Standardization that comes from a common product approach

SCAS279 – JANUARY 1993 – REVISED MARCH 1994

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

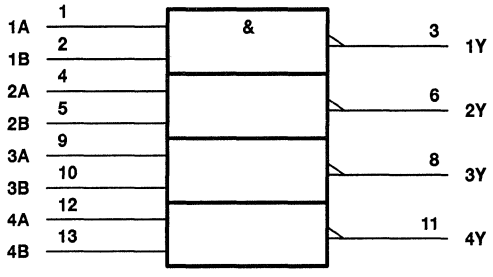
The SN74LVC00 performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74LVC00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

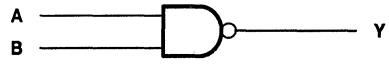
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

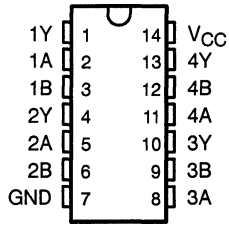
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

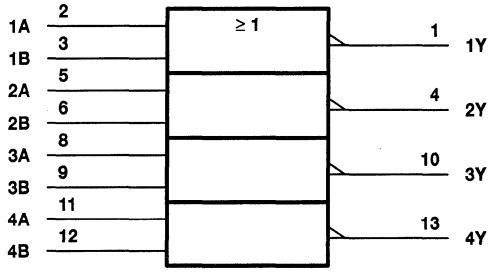
The SN74LVC02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN74LVC02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

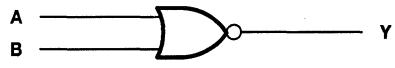
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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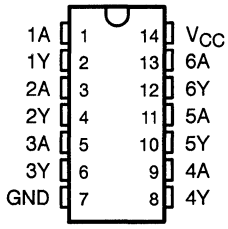
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

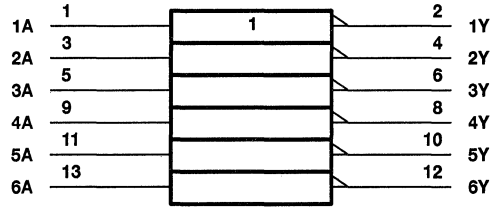
The SN74LVC04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74LVC04 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = −24 mA		3 V	2			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.6		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	1.5	3.8	6		7	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF,	f = 10 MHz	24	pF

PRODUCT PREVIEW

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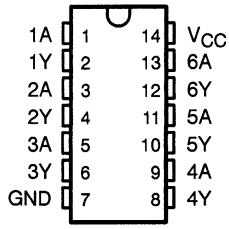
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

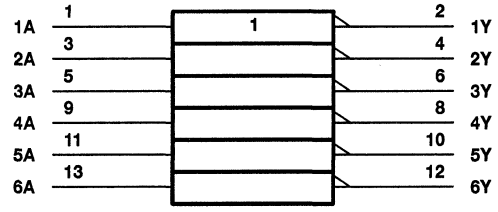
The SN74LVCU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \overline{A}$.

The SN74LVCU04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

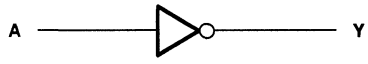
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = − 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = − 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

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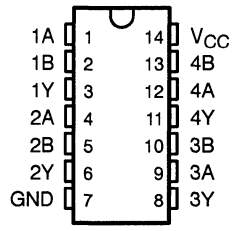
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

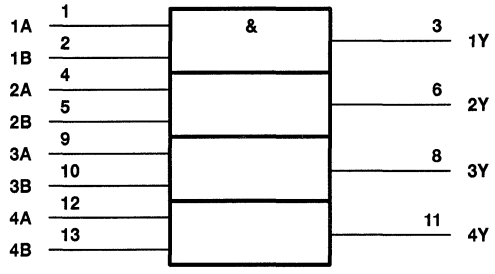
The SN74LVC08 performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74LVC08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

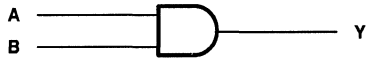
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

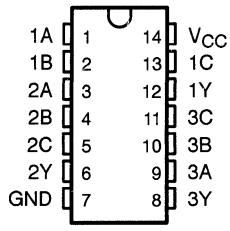
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This triple 3-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

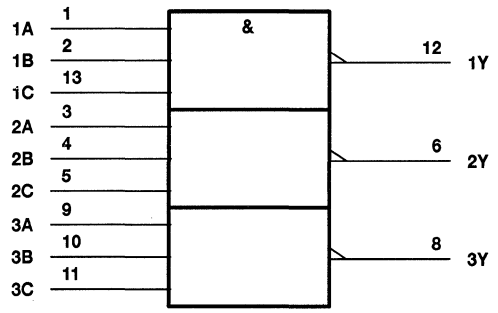
The SN74LVC10 performs the Boolean functions $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN74LVC10 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

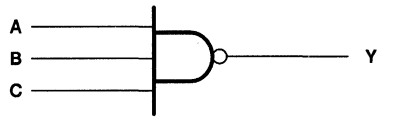
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

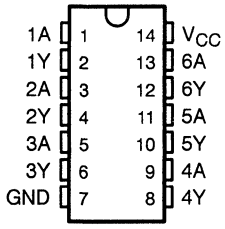
PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

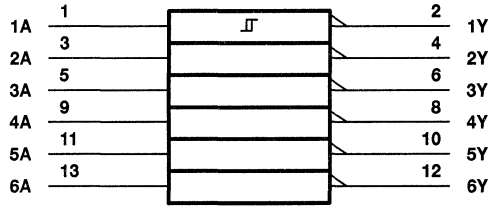
The SN74LVC14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74LVC14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

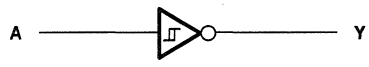
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

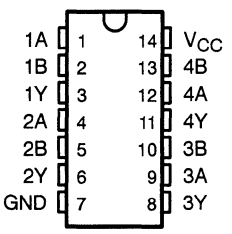
PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

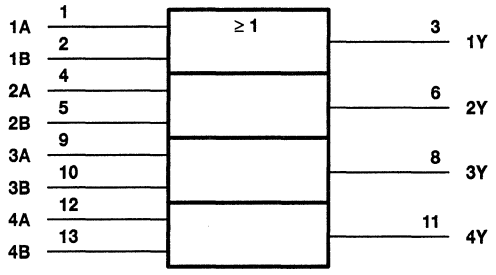
The SN74LVC32 performs the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

The SN74LVC32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

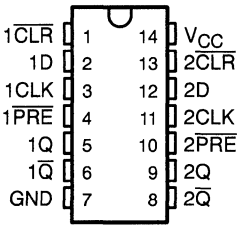
PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

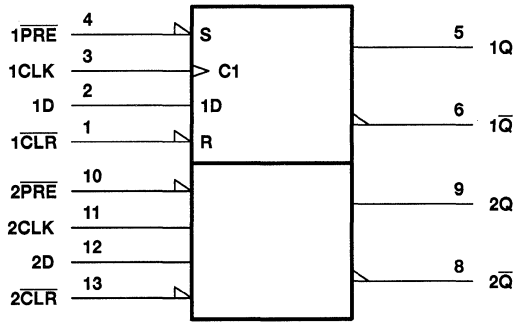
The SN74LVC74 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

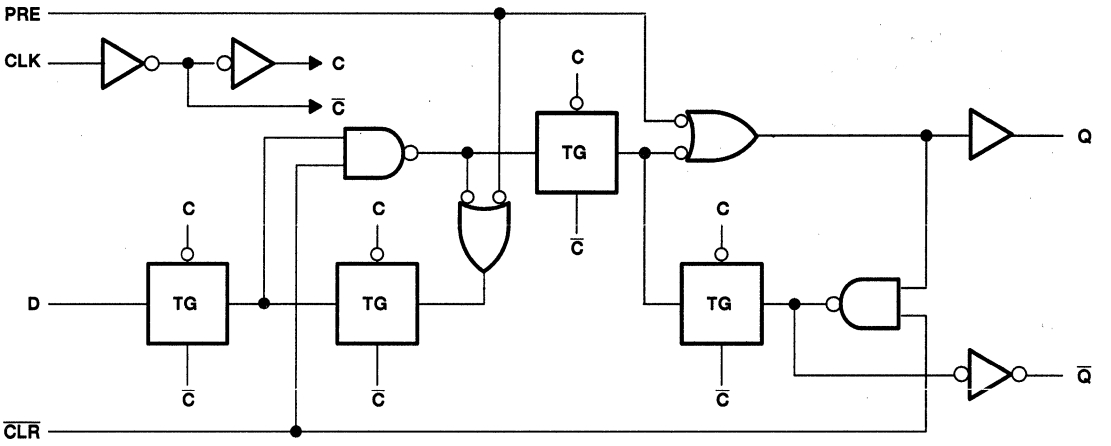
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = – 24 mA		3 V	2			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		5		ns
		CLK high or low	5		6		
t_{su}	Setup time before CLK↑	Data	3		4		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		3		
t_h	Hold time, data after CLK↑		1		2		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			150			150		MHz
t_{pd}	CLK	Q or $\overline{Q}$	1.5	3.5	9.2		10.2	ns
	$\overline{PRE}$ or $\overline{CLR}$		1.5	3.7	10.5		11.5	

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

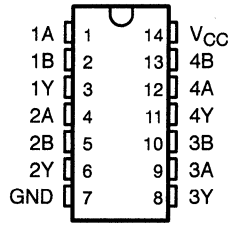
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF,	f = 10 MHz	27	pF

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC86 performs the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

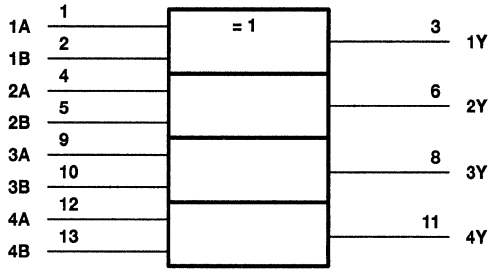
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN74LVC86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

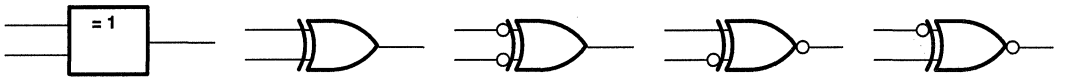
PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

exclusive-OR logic

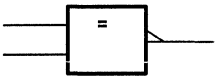
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR



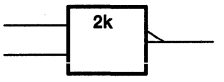
These are five equivalent exclusive-OR symbols valid for an 'LVC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



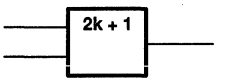
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I	−0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

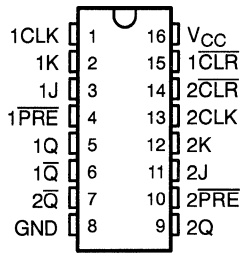
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = − 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = − 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual negative-edge-triggered J-K flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. The SN74LVC112 can perform as a toggle flip-flop by tying J and K high.

The SN74LVC112 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration may not meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

PRODUCT PREVIEW

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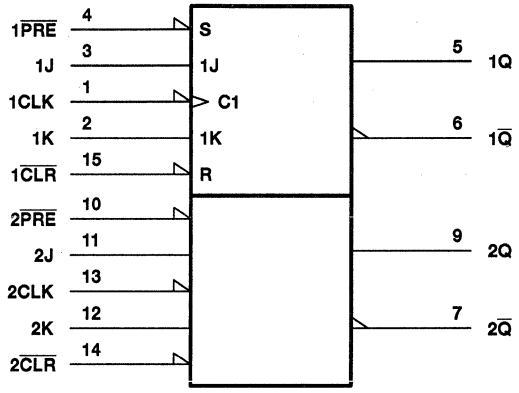
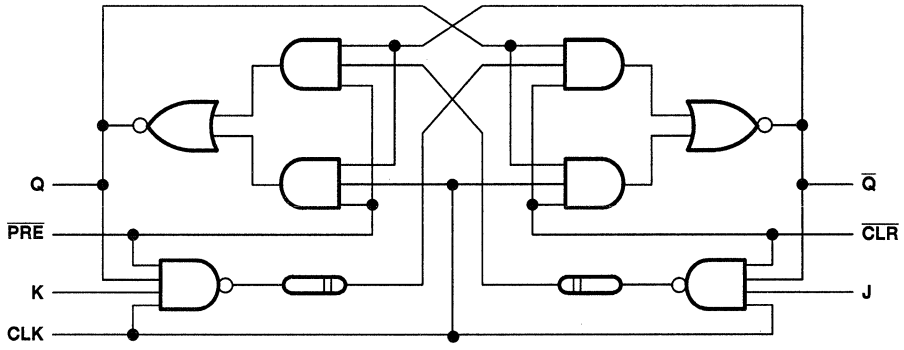
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

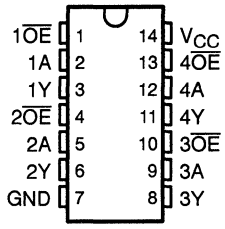
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

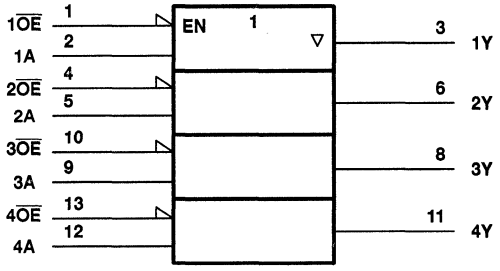
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVC125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

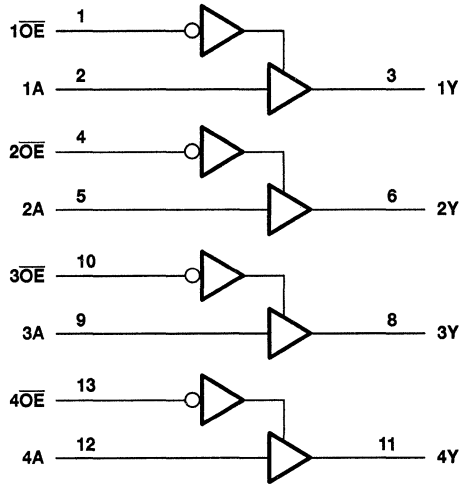
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

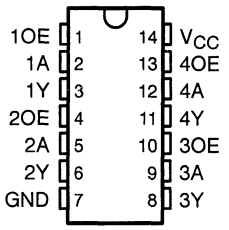
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC126 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

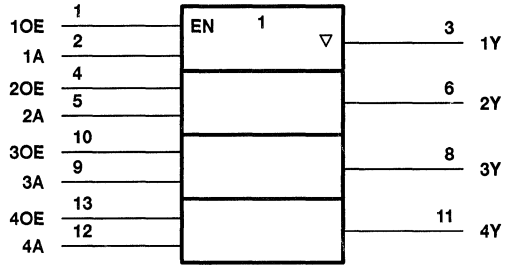
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVC126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

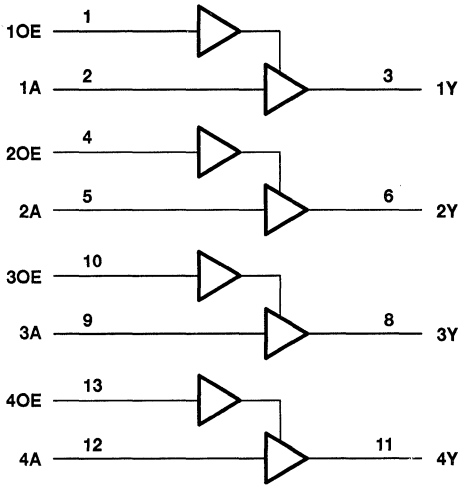
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

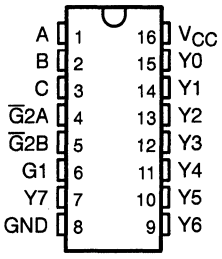
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer with latches on three address inputs is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC137 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch-enable ($\overline{G}$2A) input is low, the SN74LVC137 acts as a decoder/demultiplexer. when $\overline{G}$2A transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored provided $\overline{G}$2A remains high. The output-enable (G1 and $\overline{G}$2B) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high is G1 is low or $\overline{G}$2 is high.

The SN74LVC137 is characterized for operation from –40°C to 85°C.

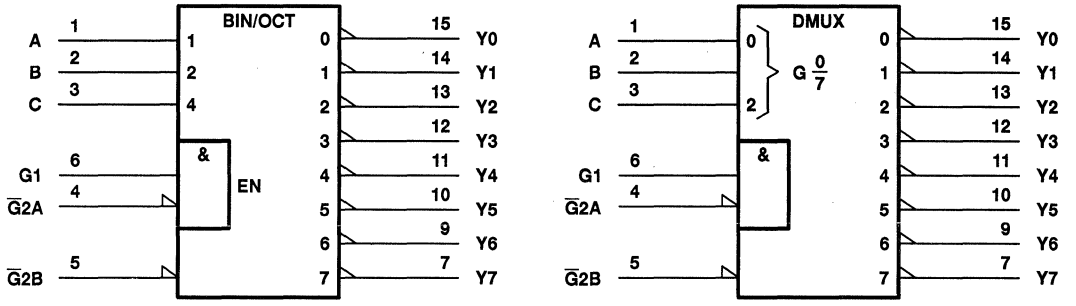
FUNCTION TABLE

LATCH ENABLE	OUTPUT-ENABLE		SELECT INPUTS			OUTPUTS							
$\overline{G}$2A	G1	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address = L; all other outputs = H							

PRODUCT PREVIEW

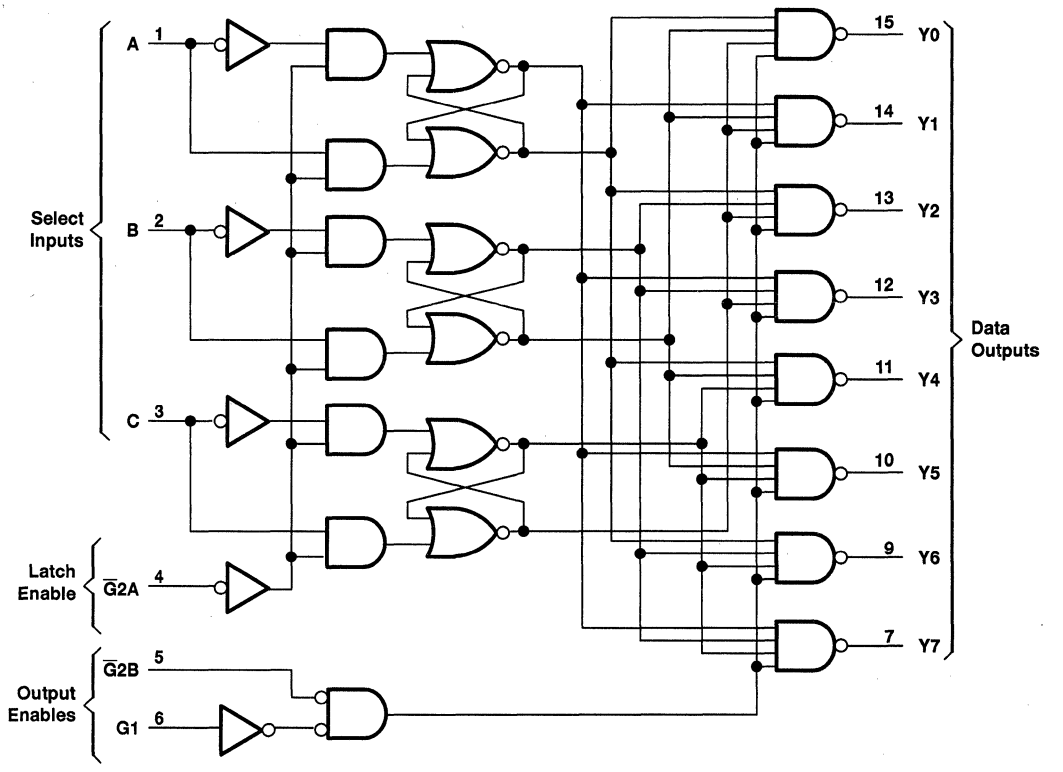
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

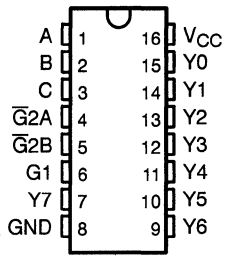
† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SCAS291 – MARCH 1993 – REVISED MARCH 1994

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LVC138 is characterized for operation from –40°C to 85°C.

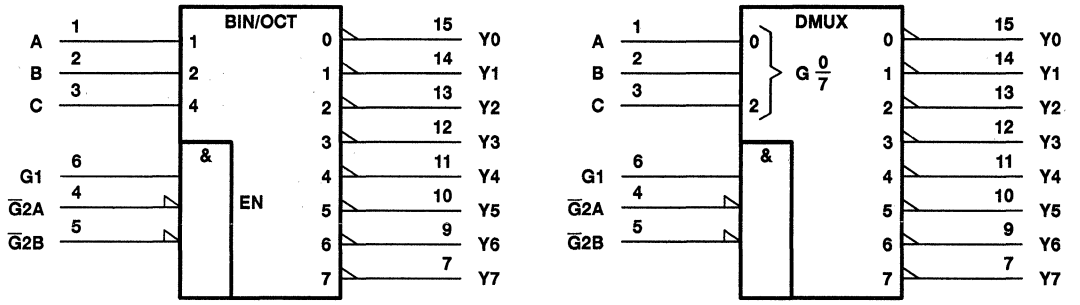
FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

PRODUCT PREVIEW

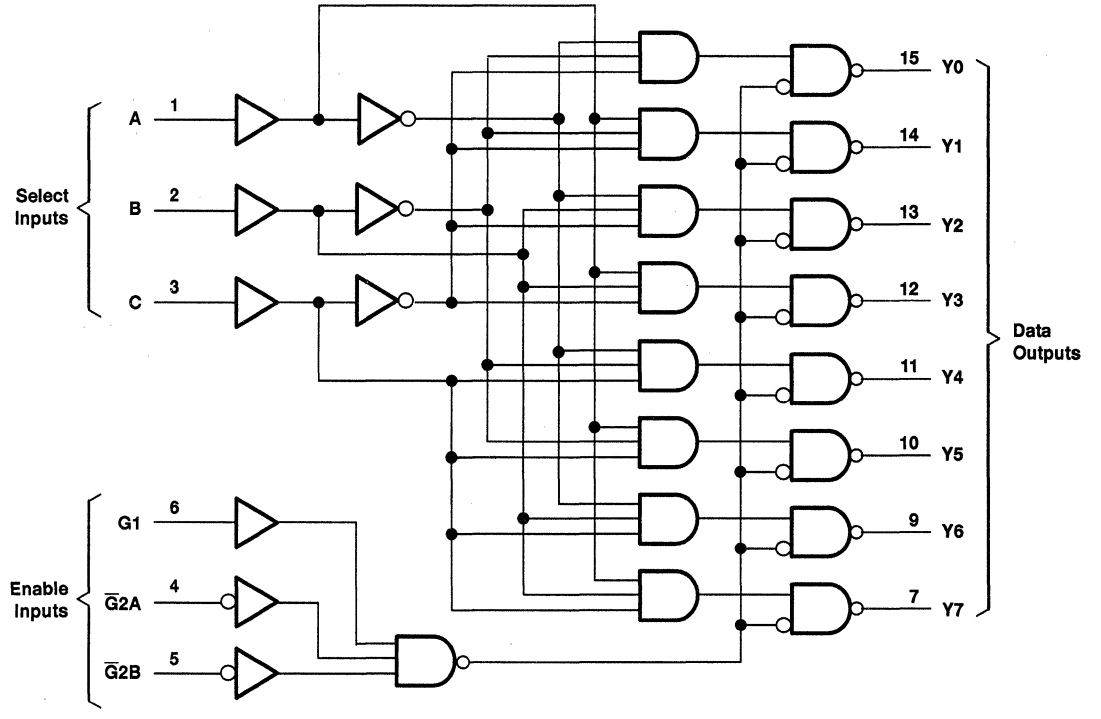
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

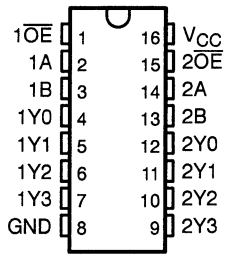
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} – 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual 2-line to 4-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC139 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

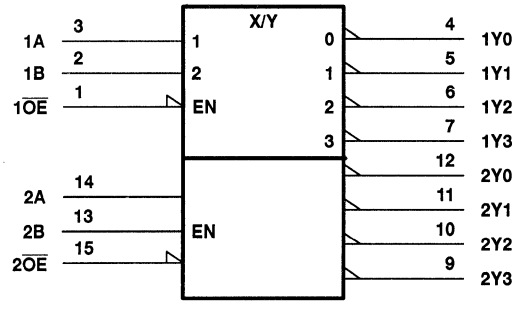
The device comprised of two individual 2-line to 4-line decoders in a single package. The active-low output-enable ($\overline{OE}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

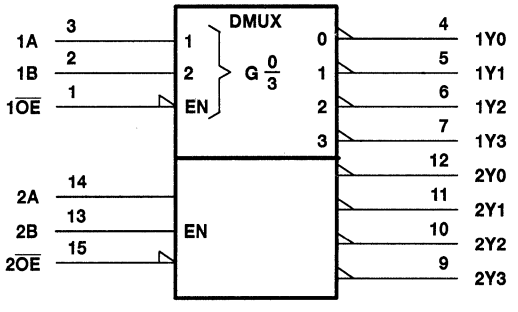
The SN74LVC139 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols (alternatives)†

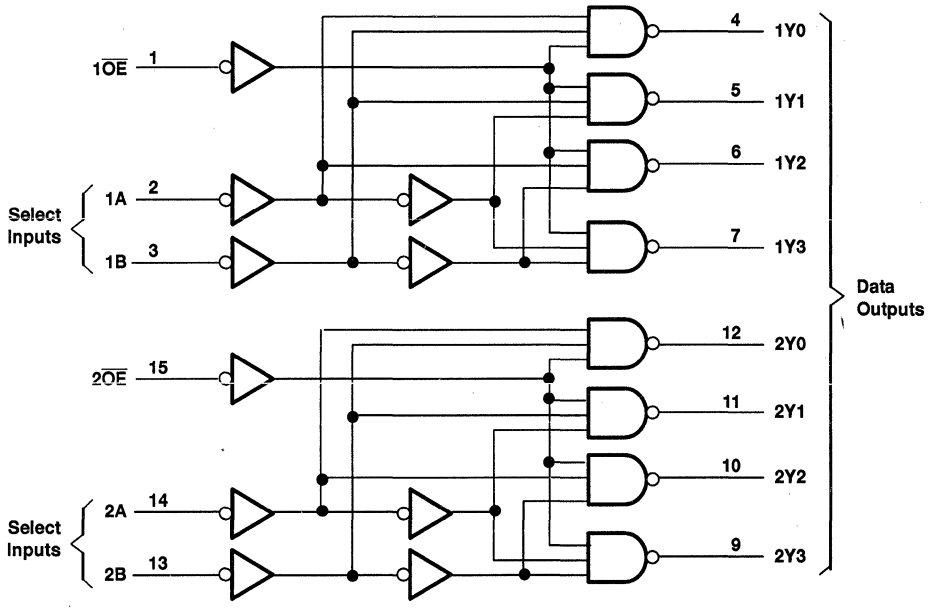




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
EPIC is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

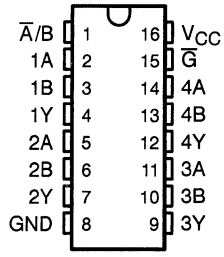
† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

SCAS292 – JANUARY 1993 – REVISED MARCH 1994

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC157 features a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

The SN74LVC157 is characterized for operation from –40°C to 85°C.

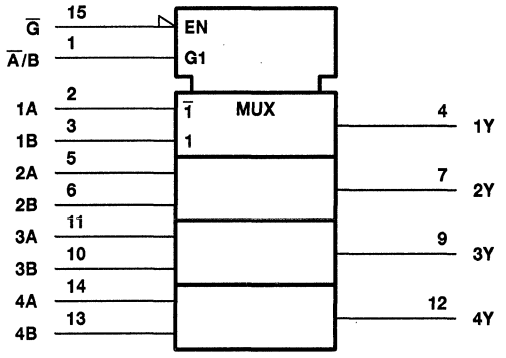
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

PRODUCT PREVIEW

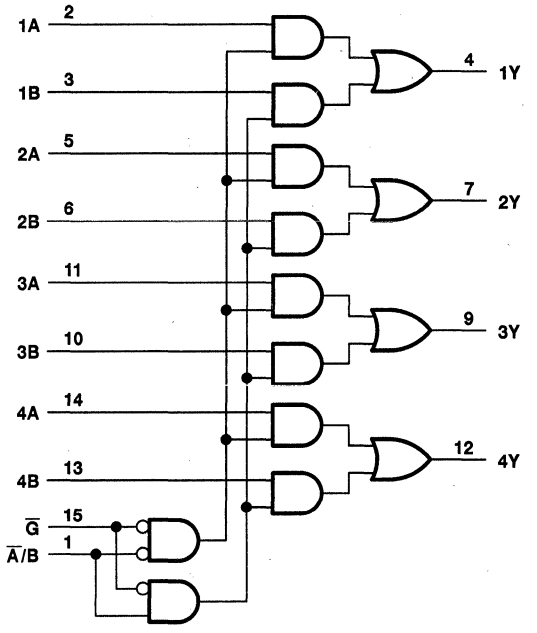
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

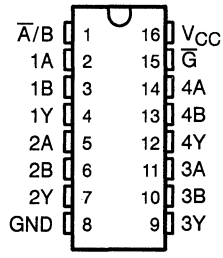
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V			
I_I	$V_I = V_{CC}$ or GND		3.6 V			μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V			μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				μA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC158 features a direct strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The SN74LVC158 provides inverted data.

The SN74LVC158 is characterized for operation from –40°C to 85°C.

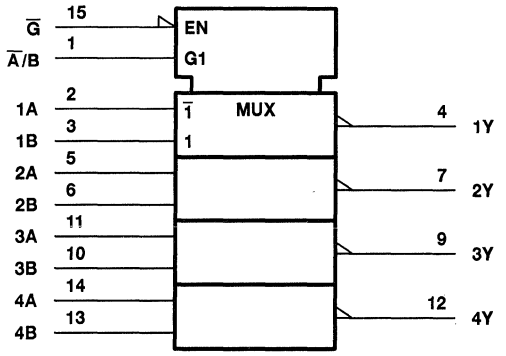
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

PRODUCT PREVIEW

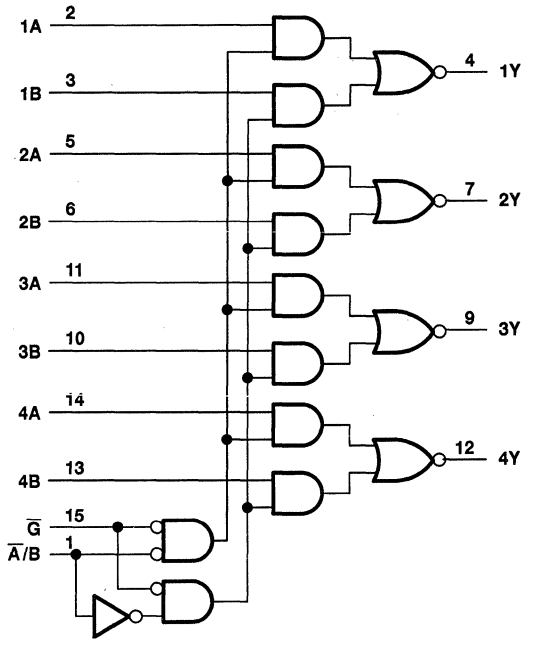
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

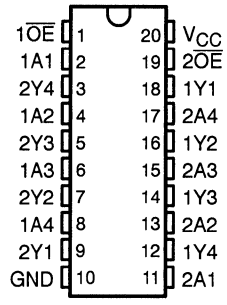
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = − 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = − 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V			
I_I	$V_I = V_{CC}$ or GND		3.6 V			µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V			µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LVC240 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74LVC240 is characterized for operation from –40°C to 85°C.

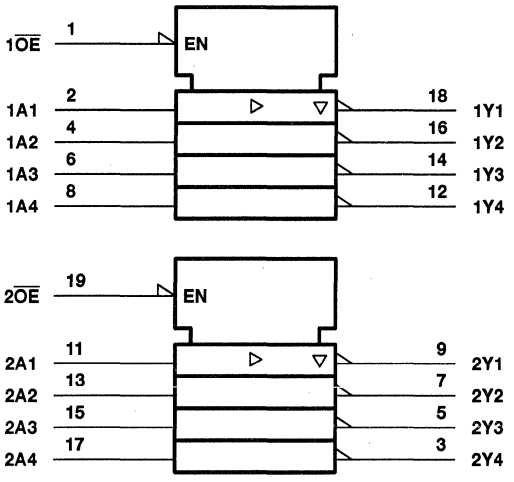
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

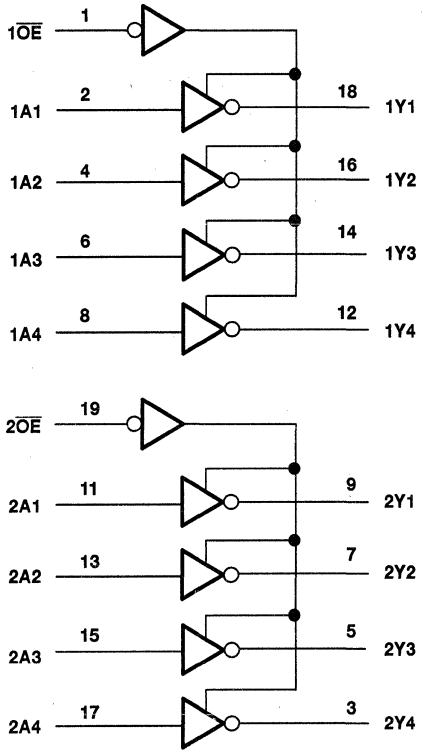
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

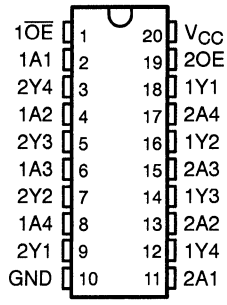
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'LVC240 and 'LVC244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{OE}$ (active-low output-enable) inputs, and complementary OE and $\overline{OE}$ inputs.

The SN74LVC241 is organized as two 4-bit line drivers with separate output-enable ($1\overline{OE}$, 2OE) inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVC241 is characterized for operation from –40°C to 85°C.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

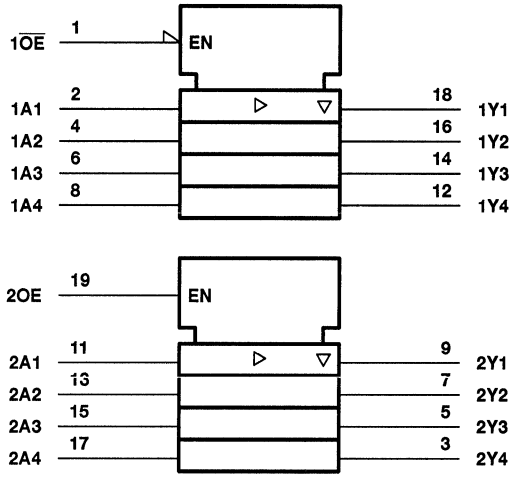
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

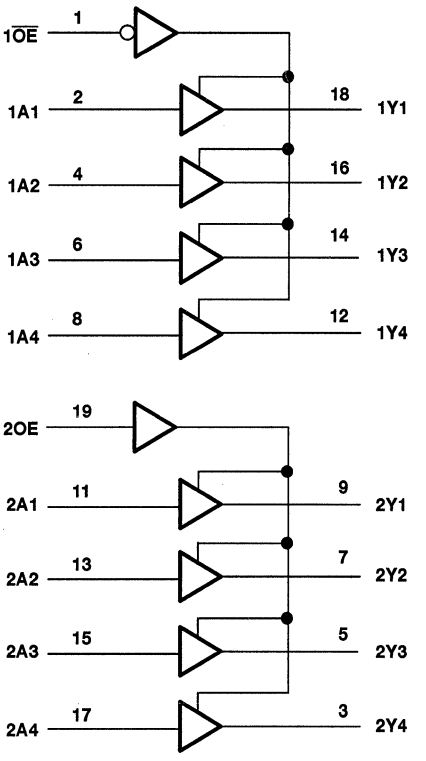
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

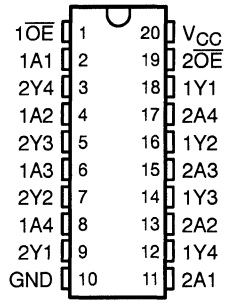
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC244 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74LVC244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

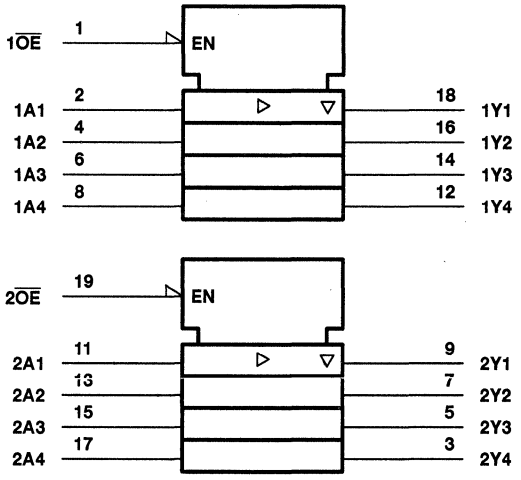
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

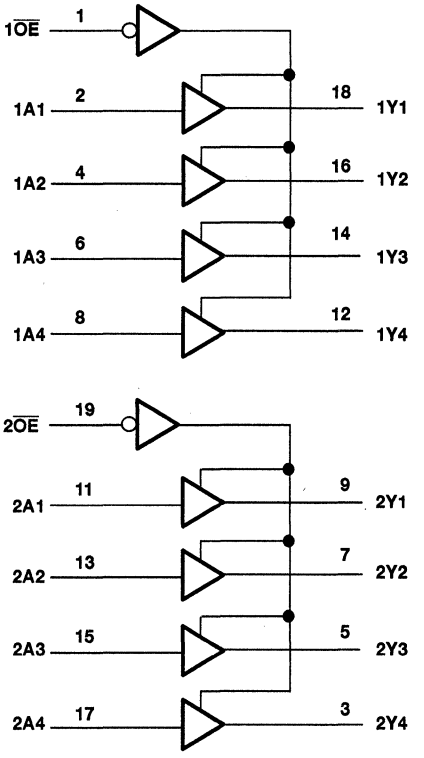
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = − 12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = − 24 mA		3 V	2			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	μA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	V_I = V_{CC} or GND		3.3 V		3		pF
C_o	V_O = V_{CC} or GND		3.3 V		3.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.5	7		8	ns
t_{en}	$\overline{OE}$	Y	1.5	8		9.2	ns
t_{dis}	$\overline{OE}$	Y	1.5	7.5		8.5	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

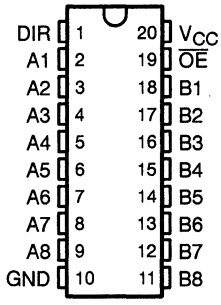
PRODUCT PREVIEW

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF, f = 10 MHz	20	pF
		Outputs disabled		2	

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

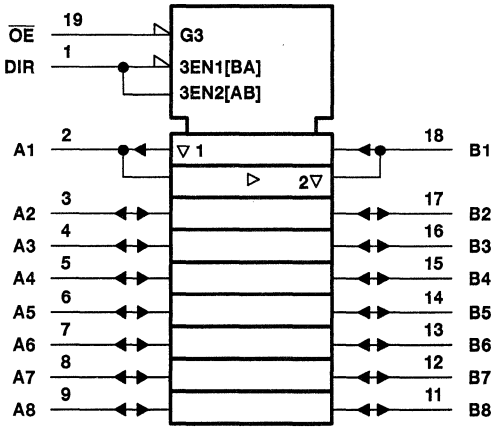
The SN74LVC245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

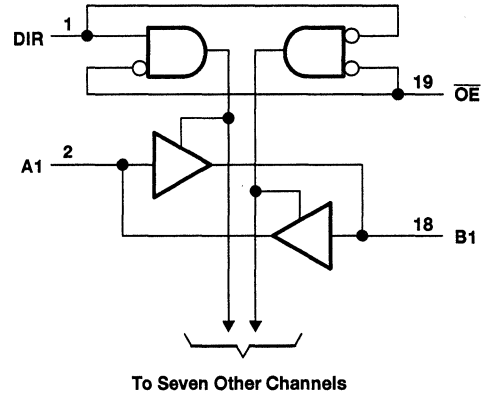
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{OH}		I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
		I_{OH} = −12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = −24 mA		3 V	2			
V_{OL}		I_{OL} = 100 µA		MIN to MAX			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		4		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	7		8	ns
t_{en}	$\overline{OE}$	A or B	1.5	9		10	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8		9	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

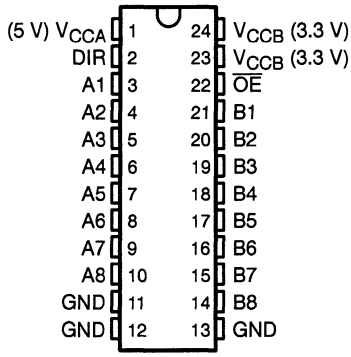
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 10 MHz	25	pF
		Outputs disabled		2	

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} which is set at 3.3 V, and A port has V_{CCA} which is set to operate at 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice-versa.

The SN74LVC4245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The pinout of the SN74LVC4245 allows the designer to switch to a normal all 3.3-V or all 5-V 20-pin '245 device without relaying out the board. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245 to achieve the conventional '245 layout.

The SN74LVC4245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

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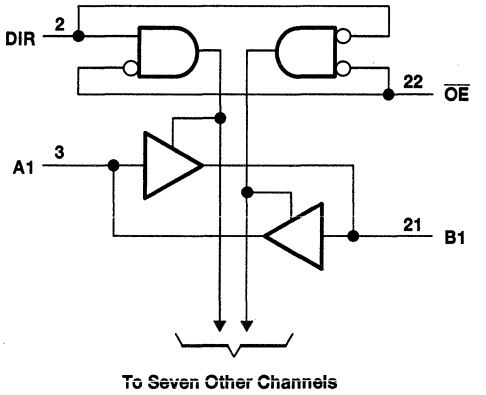
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5 V (unless otherwise noted)†

Supply voltage range, V_{CCA} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CCA} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CCA} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CCA}$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CCA}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CCA}) ..... ±50 mA
Continuous current through V_{CCA} or GND ..... ±100 mA

NOTE 1: This value is limited to 6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 3.3 V (unless otherwise noted)†

Supply voltage range, V_{CCB} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 2) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 2) ..... −0.5 V to V_{CCB} + 0.5 V
Output voltage range, V_O (see Note 2) ..... −0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CCB}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CCB}) ..... ±50 mA
Continuous current through V_{CCB} or GND ..... ±100 mA

NOTE 2: This value is limited to 4.6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5 V or for V_{CCB} at 3.3 V (unless otherwise noted)†

Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions for V_{CCA} at 5 V (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CCA}	V
V_O	Output voltage	0		V_{CCA}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

recommended operating conditions for V_{CCB} at 3.3 V (see Note 3)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CCB}	V
V_O	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		−12	mA
		V_{CCB} = 3 V		−24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused of floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		4.5 V	4.3		V
				5.5 V	5.3		
		I_{OH} = −24 mA		4.5 V	3.7		
				5.5 V	4.7		
V_{OL}		I_{OL} = 100 μA		4.5 V		0.2	V
				5.5 V		0.2	
		I_{OL} = 24 mA		4.5 V		0.55	
				5.5 V		0.55	
I_I	Control pins	V_I = V_{CCA} or GND		5.5 V		5	μA
I_{OZ}†	A or B ports	V_O = V_{CCA} or GND		5.5 V			μA
I_{CC}		V_I = V_{CCA} or GND,	I_O = 0	5.5 V			μA
ΔI_{CC}‡		One input at 3.4 V,	Other inputs at V_{CCA} or GND				μA
C_i	Control inputs	V_I = V_{CCA} or GND		5 V			pF
C_{io}	A or B ports	V_O = V_{CCA} or GND		5 V			pF

electrical characteristics over recommended operating free-air temperature range for V_{CCB} = 3.3 V (unless otherwise noted)

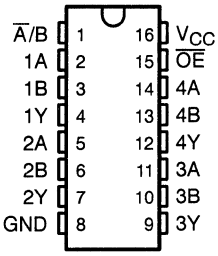
PARAMETER		TEST CONDITIONS		V_{CCB}§	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Control pins	V_I = V_{CCB} or GND		3.6 V		5	μA
I_{OZ}†		V_O = V_{CCB} or GND		3.6 V			μA
I_{CC}		V_I = V_{CCB} or GND,	I_O = 0	3.6 V			μA
ΔI_{CC}‡		V_{CCB} = 3 V to 3.6 V, Other inputs at V_{CCB} or GND	One input at V_{CCB} − 0.6 V,				μA
C_i	Control inputs	V_I = V_{CCB} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CCB} or GND		3.3 V			pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CCB}.
§ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

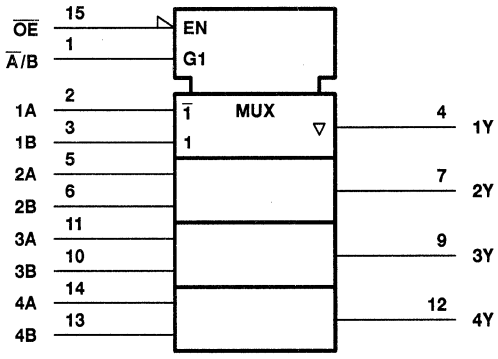
The SN74LVC257 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output enable ($\overline{OE}$) input is at a high logic level.

The SN74LVC257 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	A/B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic symbol†



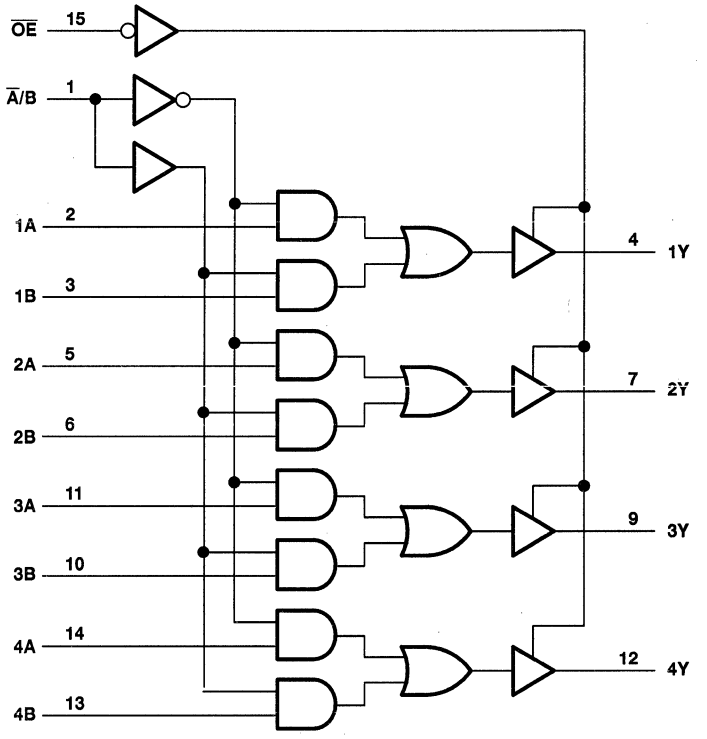
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

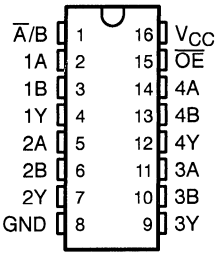
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

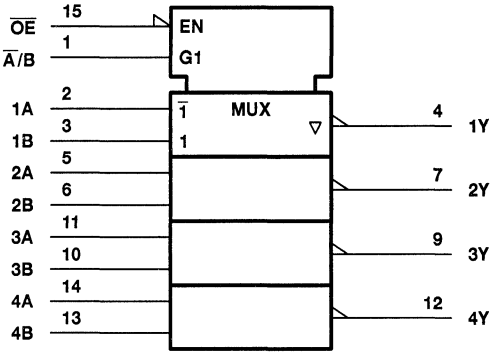
The SN74LVC258 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output enable ($\overline{OE}$) input is at a high logic level.

The SN74LVC258 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic symbol†



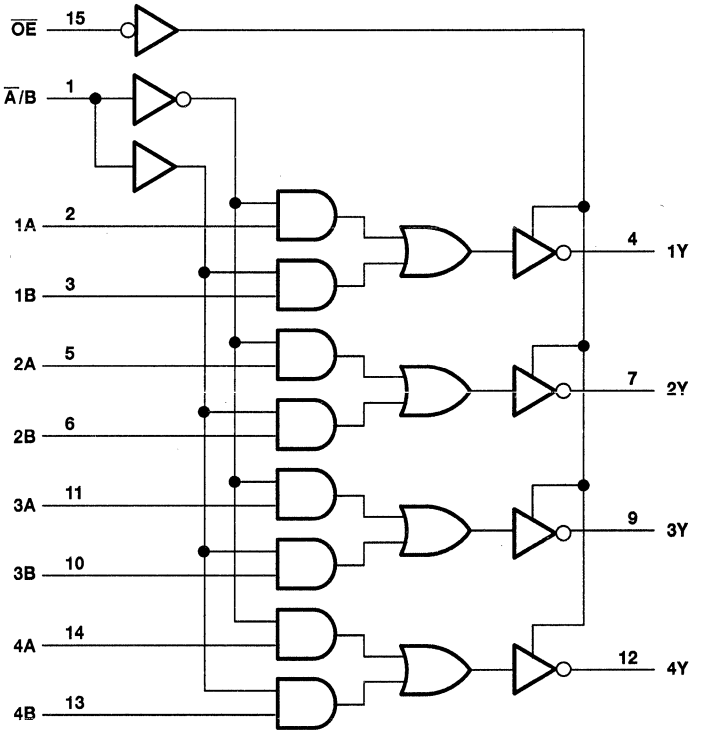
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

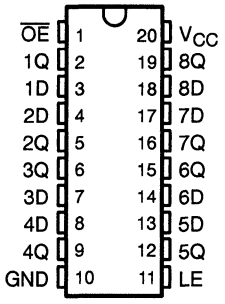
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC373 is characterized for operation from –40°C to 85°C.

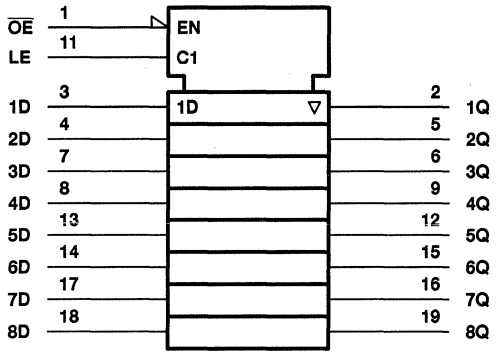
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

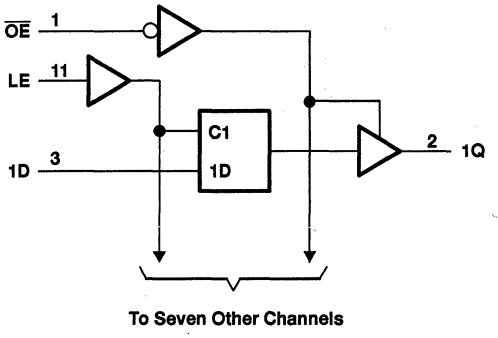
PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I	−0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

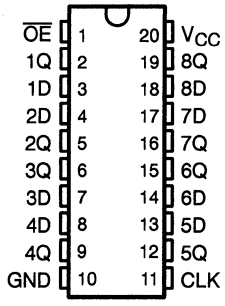
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC374 is characterized for operation from –40°C to 85°C.

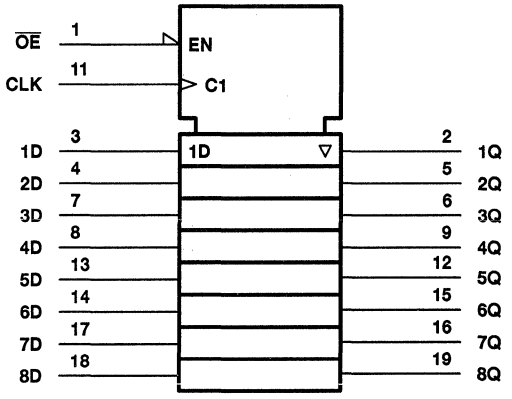
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

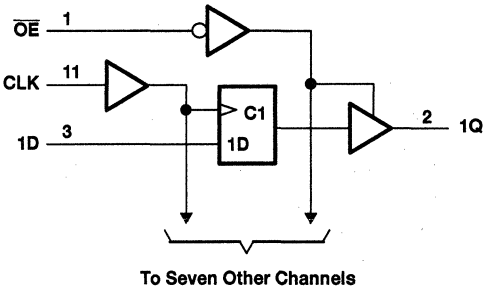
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

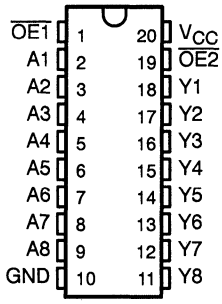
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC540 is ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package that facilitate printed-circuit-board layout.

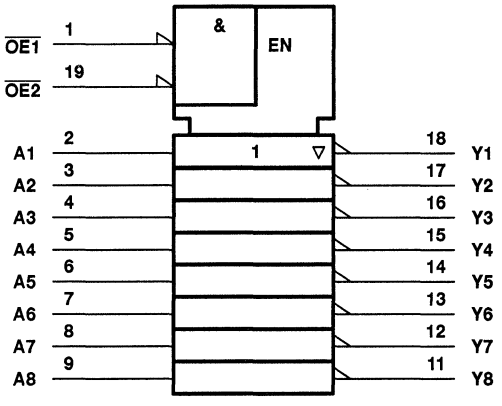
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN74LVC540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

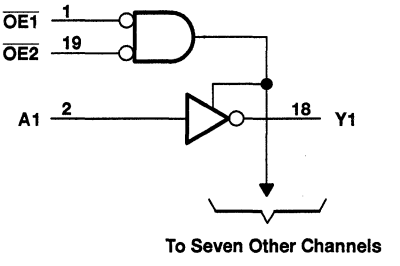
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

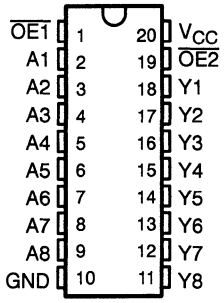
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC541 is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

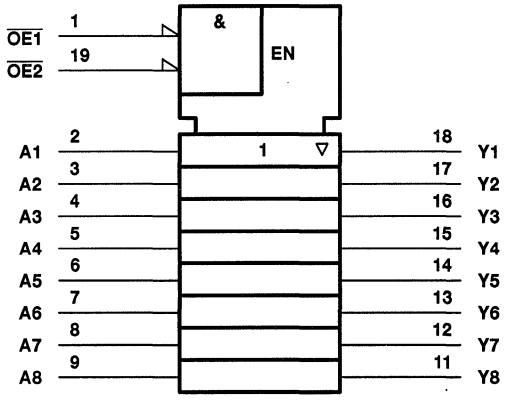
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

The SN74LVC541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

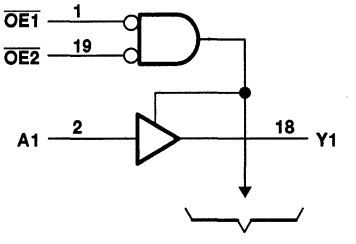
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

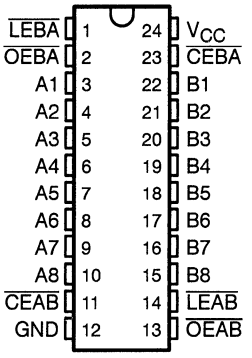
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The SN74LVC543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

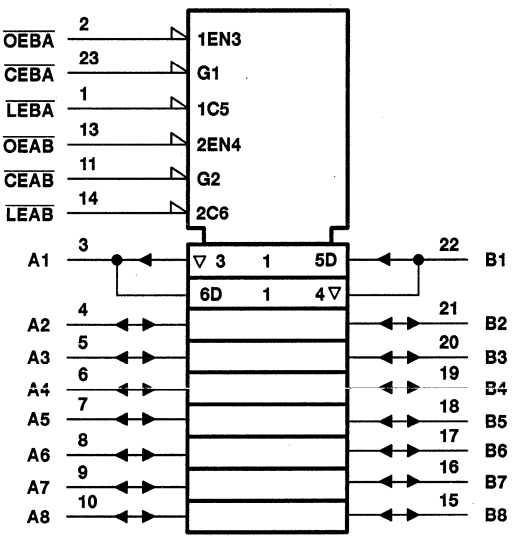
INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

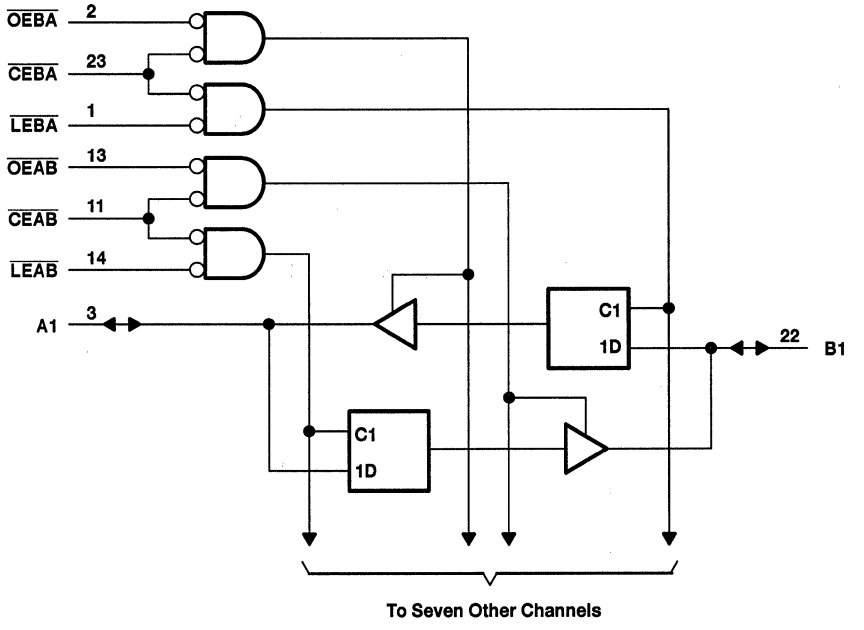
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
		I_{OH} = −12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = −24 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		MIN to MAX			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	μA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		4.3		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration		4		4		ns
t_{su}	Setup time	Data before $\overline{LE}$↑ or $\overline{CE}$↑	1.5		1.5		ns
t_h	Hold time	Data after $\overline{LE}$↑ or $\overline{CE}$↑	2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP§	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	4	8		9	ns
	$\overline{LE}$		1.5	4.4	9.5		10.5	
t_{en}	$\overline{OE}$	A or B	1.5	3.9	8.5		9.5	ns
	$\overline{CE}$		1.5	4.1	9		10	
t_{dis}	$\overline{OE}$	A or B	1.5	4.7	8.5		9.5	ns
	$\overline{CE}$		1.5	4.8	9		10	

§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

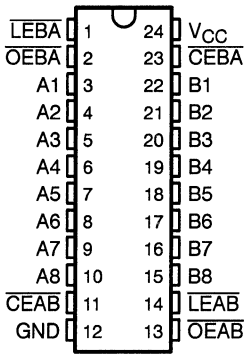
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	20	pF
		Outputs disabled		10	

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC544 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the inverted data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to GND through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC544 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

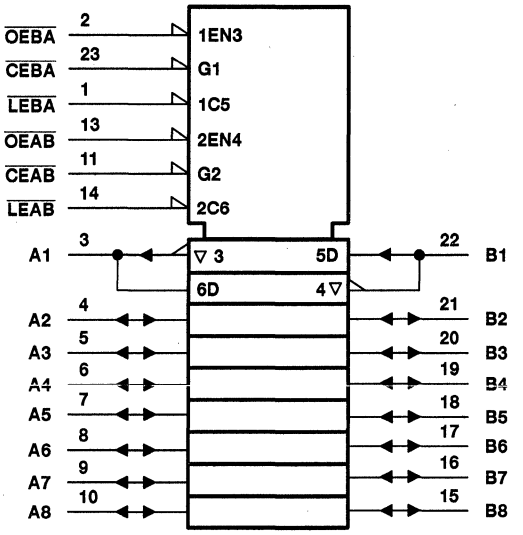
INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	H
L	L	L	H	L

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

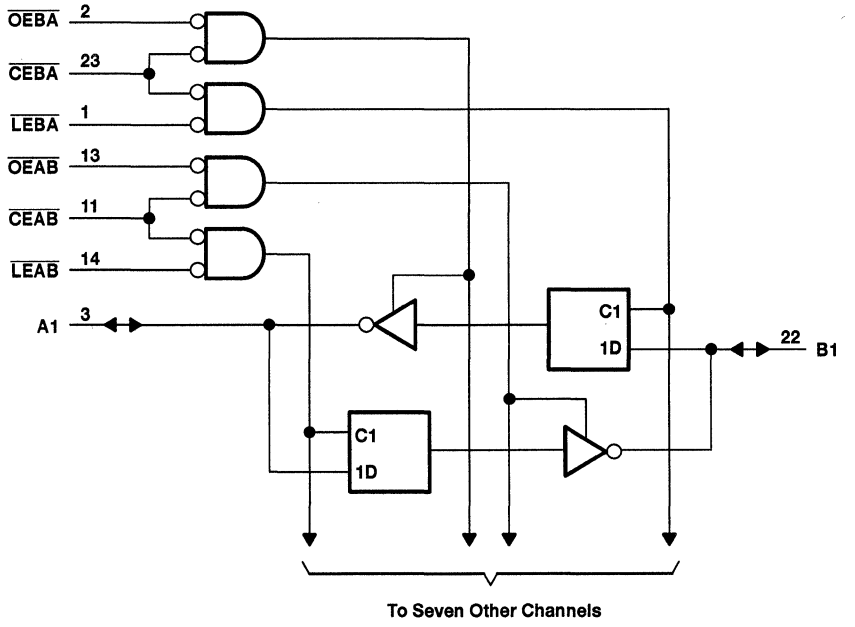
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

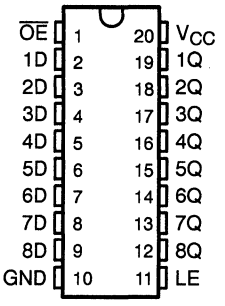
PARAMETER		TEST CONDITIONS	V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}		I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 µA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V		±5	µA
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		20	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

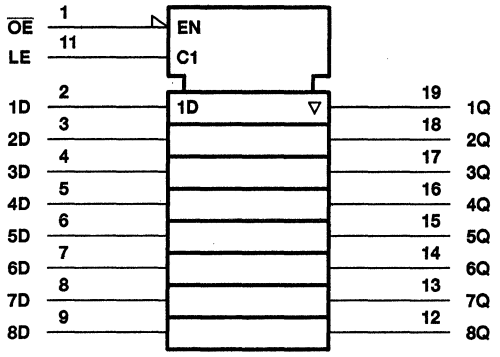
The SN74LVC573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

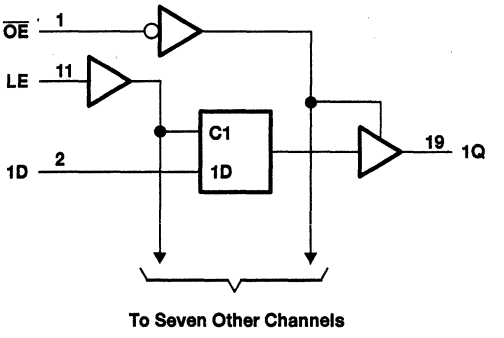
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

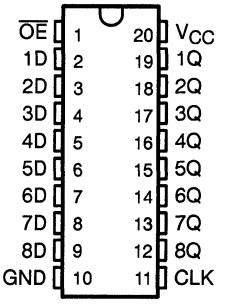
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC574 is characterized for operation from –40°C to 85°C.

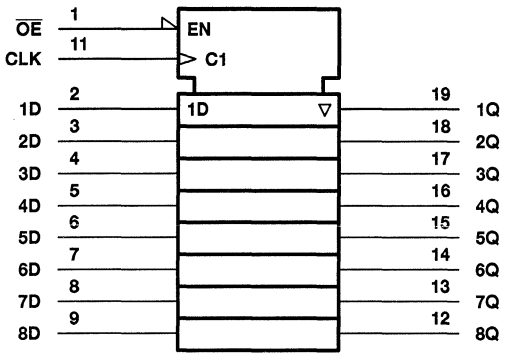
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

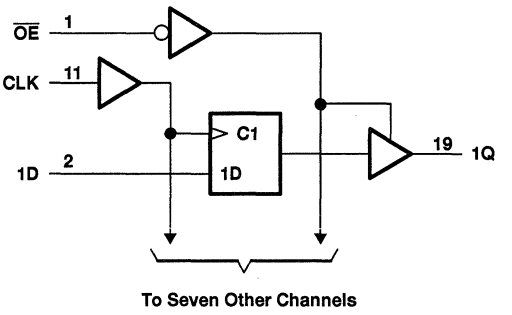
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
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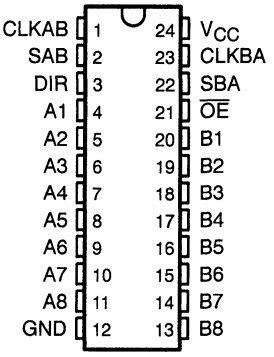
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74LVC646 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW

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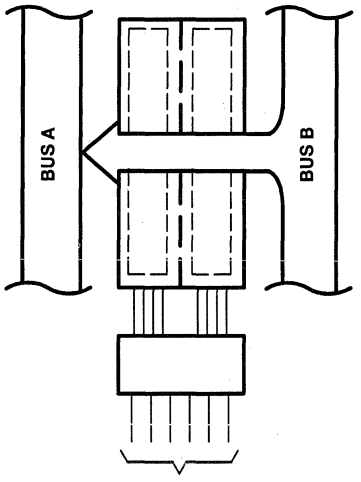
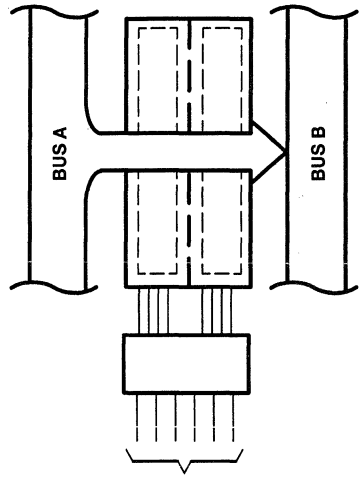


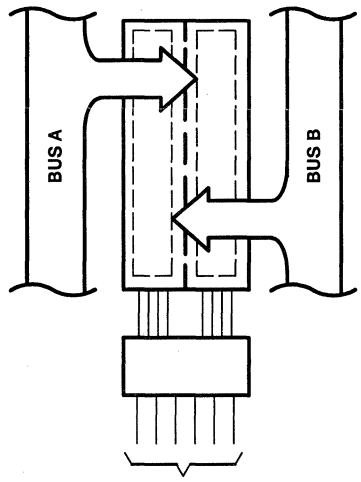
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



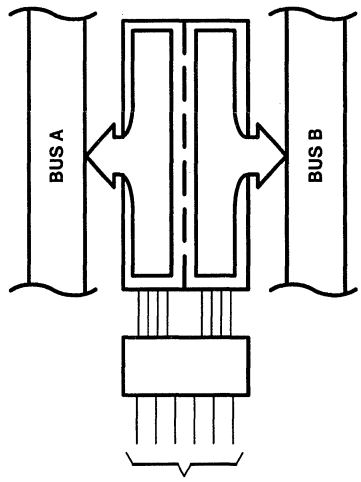
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B

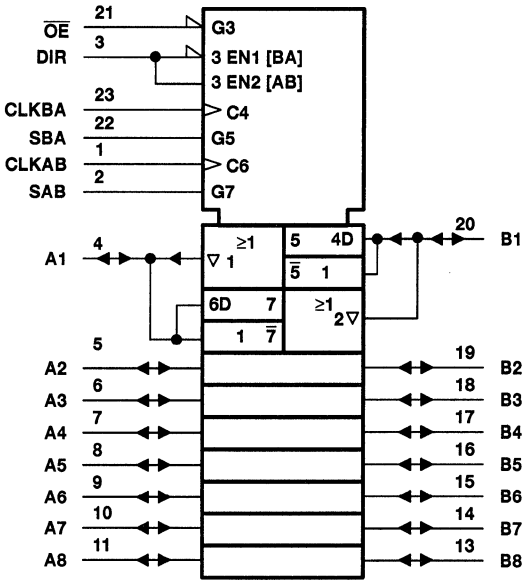


21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

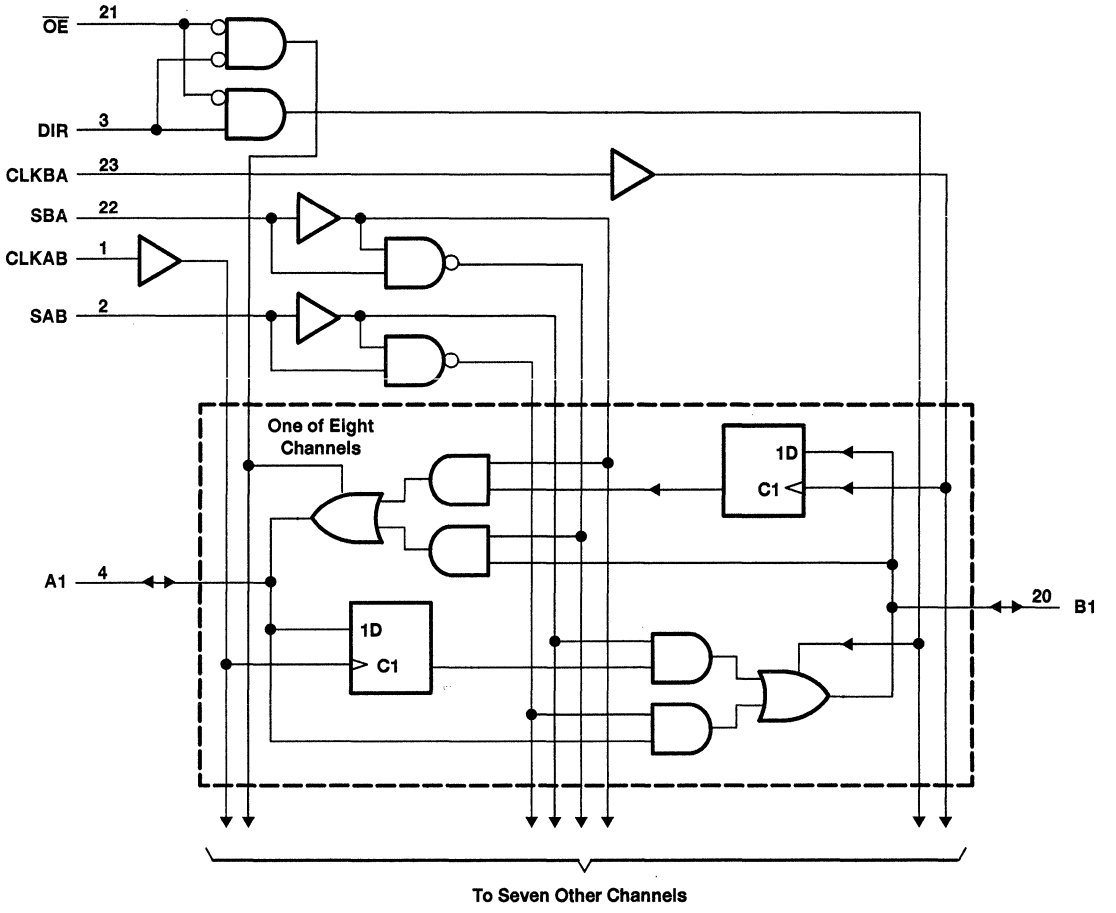
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
					MIN	MAX	
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
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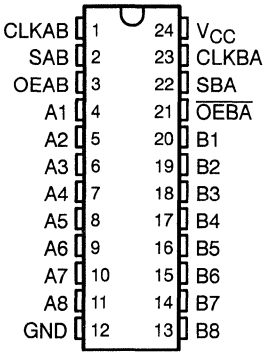
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

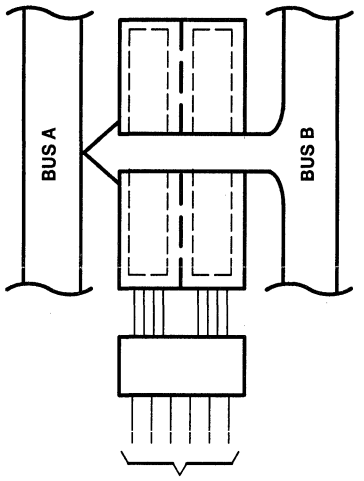
The SN74LVC652 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

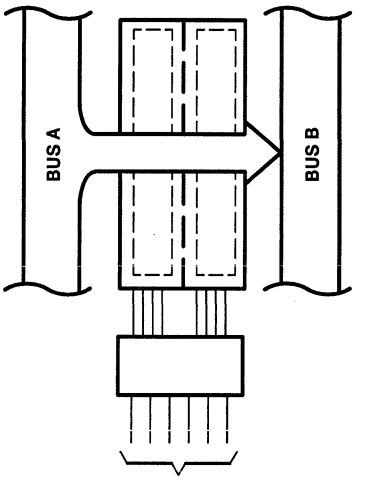
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

EPIC is a trademark of Texas Instruments Incorporated.



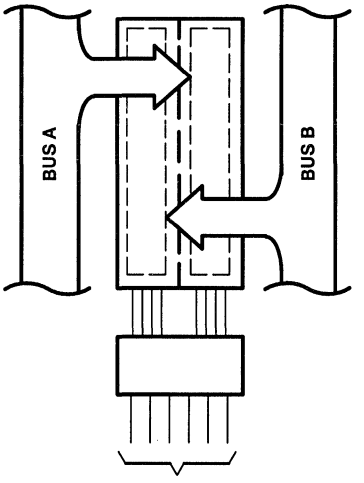
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



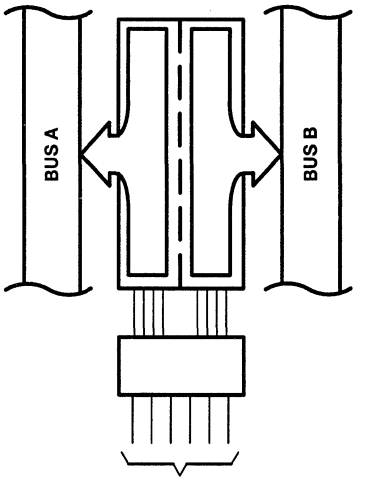
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B, OR A AND B

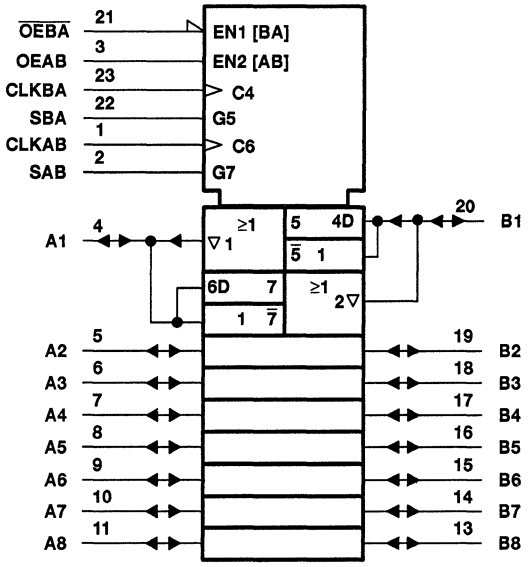


3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

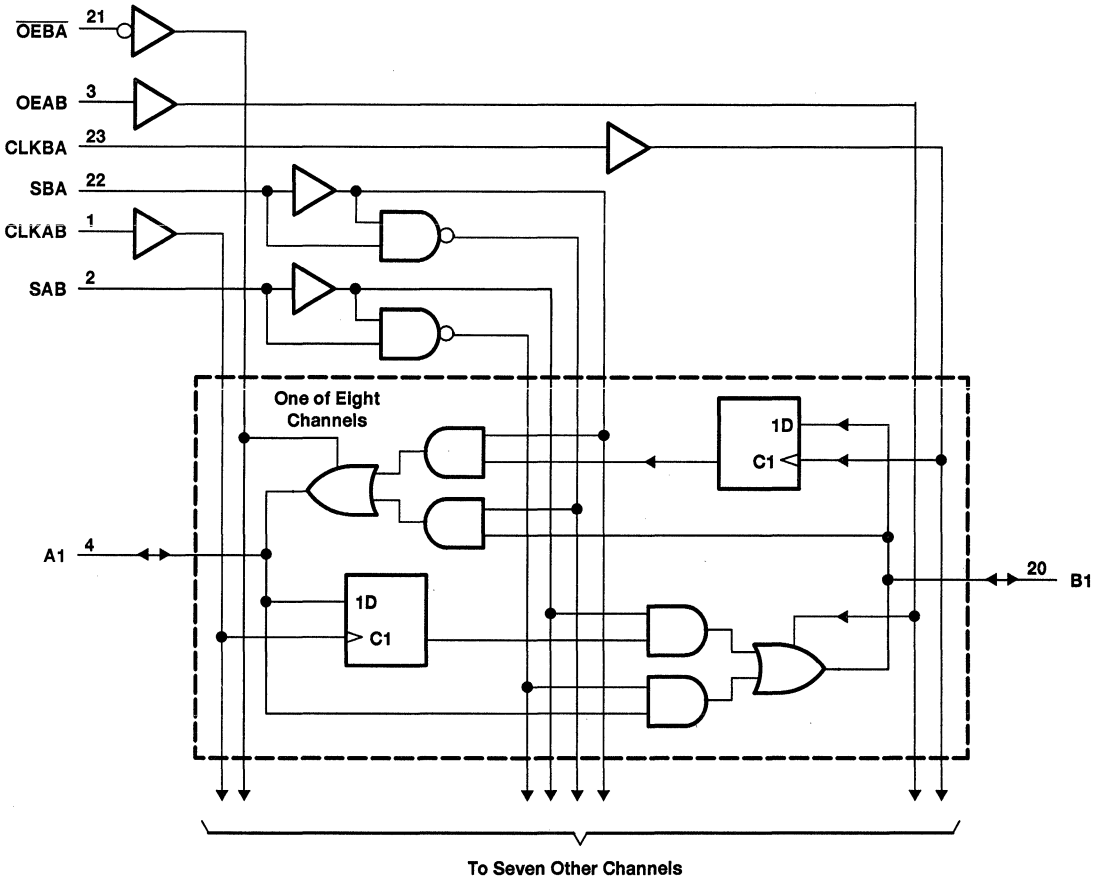
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

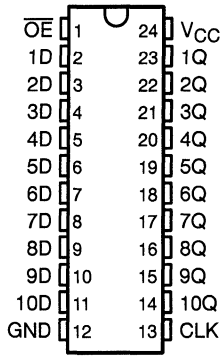
PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
					MIN	MAX	
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = – 12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = – 24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	µA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC821 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC821 is characterized for operation from –40°C to 85°C.

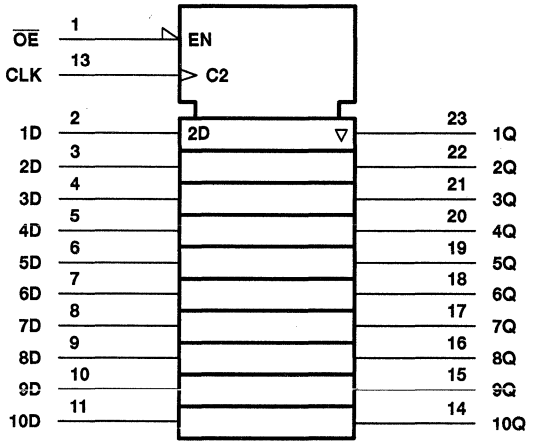
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

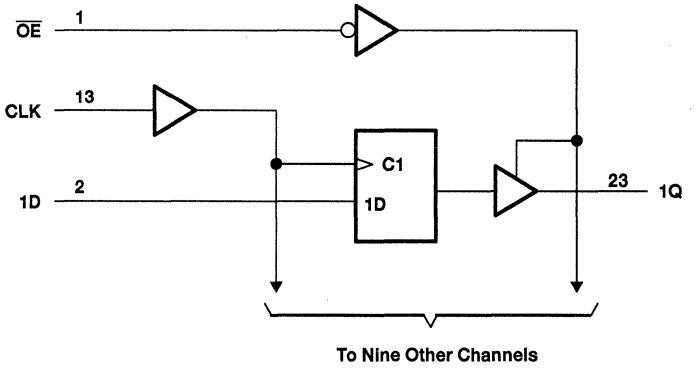
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

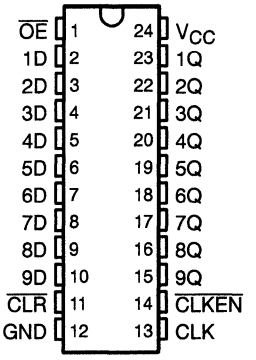
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	μA
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	μA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC823 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The SN74LVC823 has noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC823 is characterized for operation from –40°C to 85°C.

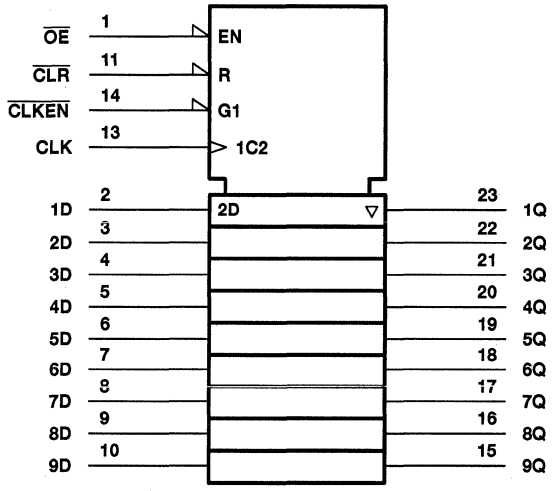
FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

PRODUCT PREVIEW

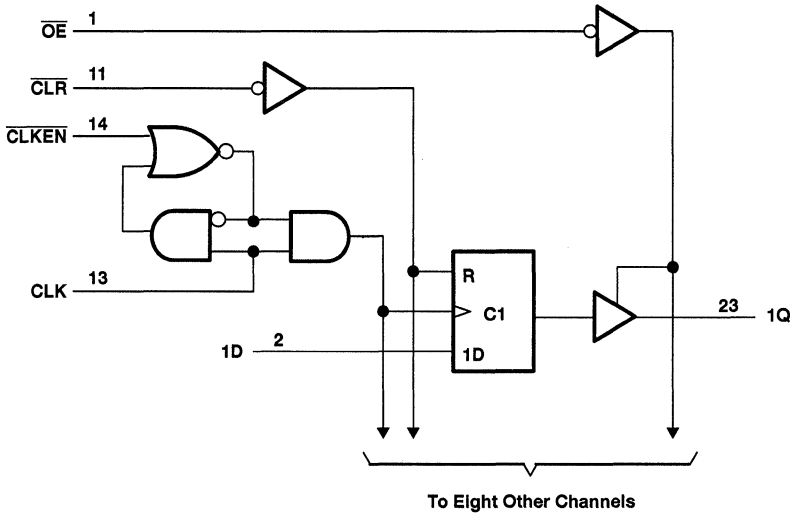
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

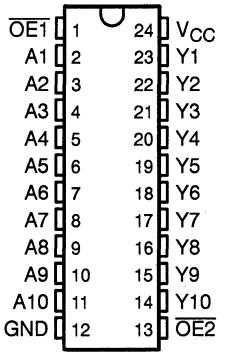
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit buffer/bus driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC827 provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC827 provides true data at its outputs.

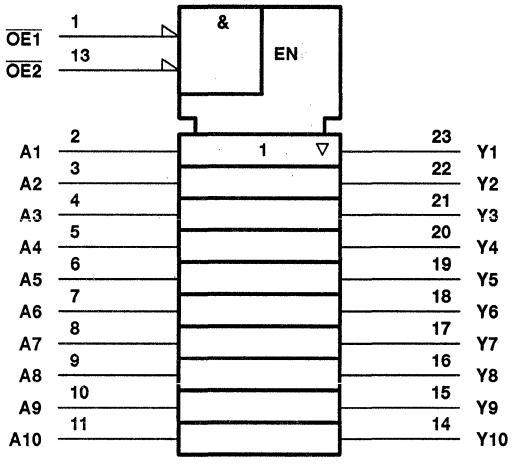
The SN74LVC827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

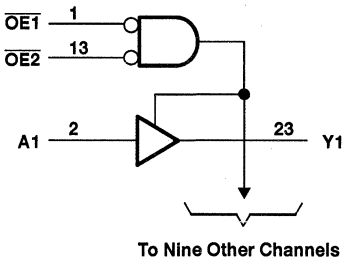
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I	−0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = – 24 mA		3 V	2			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	μA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	μA
C_i	V_I = V_{CC} or GND		3.3 V		7.5		pF
C_o	V_O = V_{CC} or GND		3.3 V		8.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	UNIT
			MIN	TYP	MAX	MAX	
t_{pd}	A	Y	1.5	3.5	7	8	ns
t_{en}	$\overline{OE}$	Y	1.5	4.3	9	11	ns
t_{dis}	$\overline{OE}$	Y	1.5	4	8	9	ns

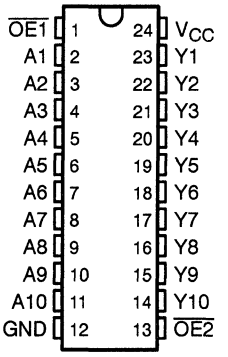
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF,	f = 10 MHz	25	pF
		Outputs disabled			2.5	

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit buffer/bus driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC828 provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state. The SN74LVC828 provides inverting data at its outputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC828 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

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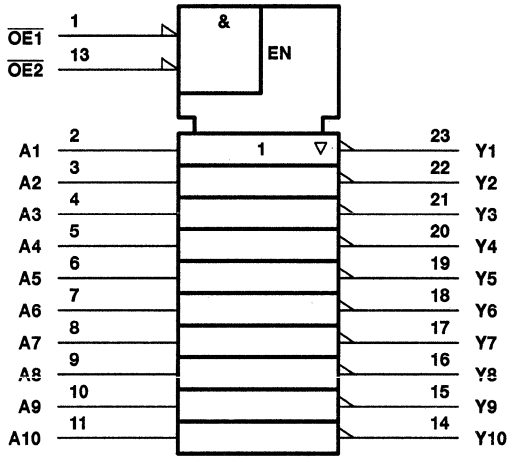
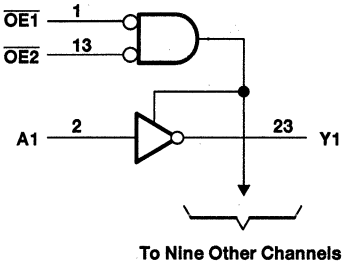
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I	−0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

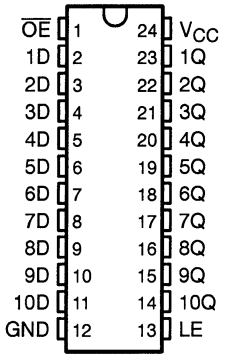
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = − 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = − 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC841 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC841 is characterized for operation from –40°C to 85°C.

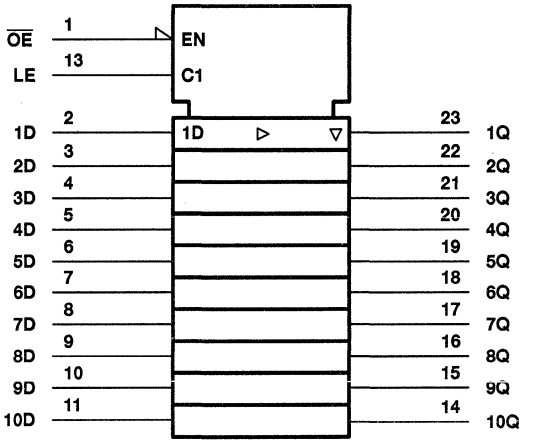
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

PRODUCT PREVIEW

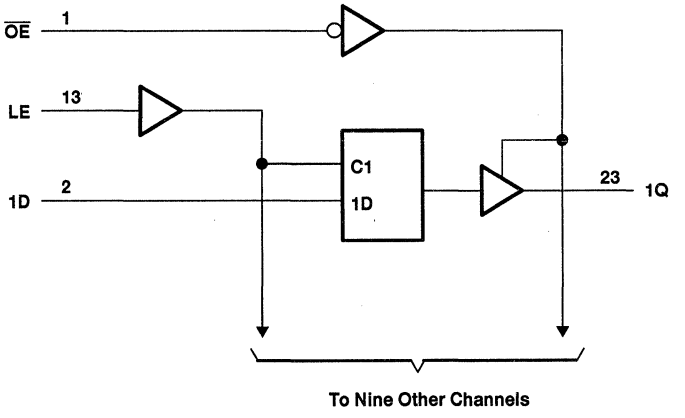
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

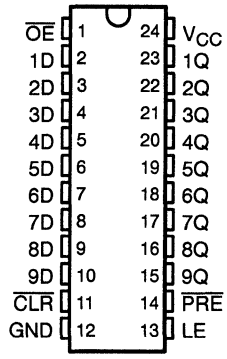
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
	I_{OH} = −12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = −24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC843 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC843 is characterized for operation from –40°C to 85°C.

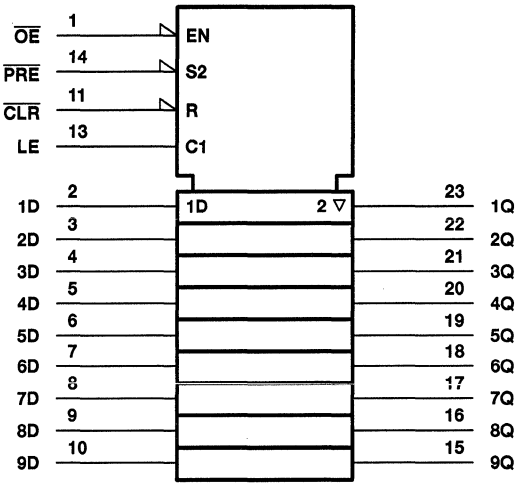
FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

PRODUCT PREVIEW

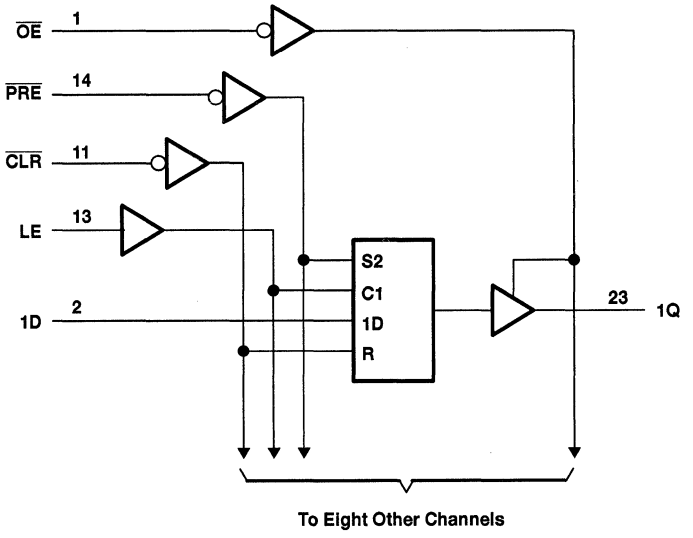
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

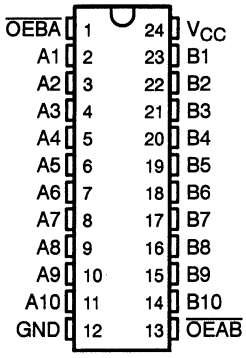
PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = – 12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = – 24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 10-bit bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC861 is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC861 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

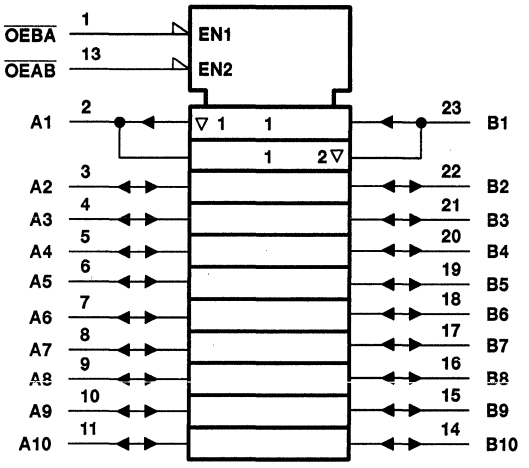
INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Isolation
L	L	Latch A and B (A = B)

PRODUCT PREVIEW

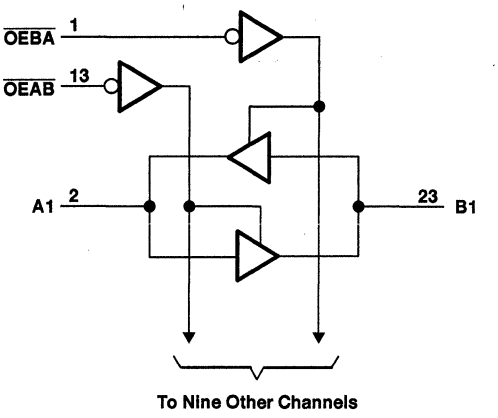
EPIC is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

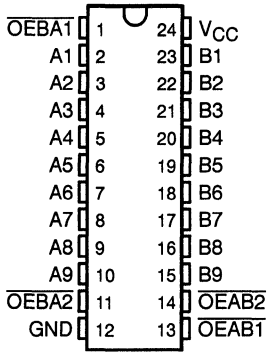
PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = −40°C to 85°C		UNIT
					MIN	MAX	
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = − 12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = − 24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This 9-bit bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC863 is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC863 is characterized for operation from –40°C to 85°C.

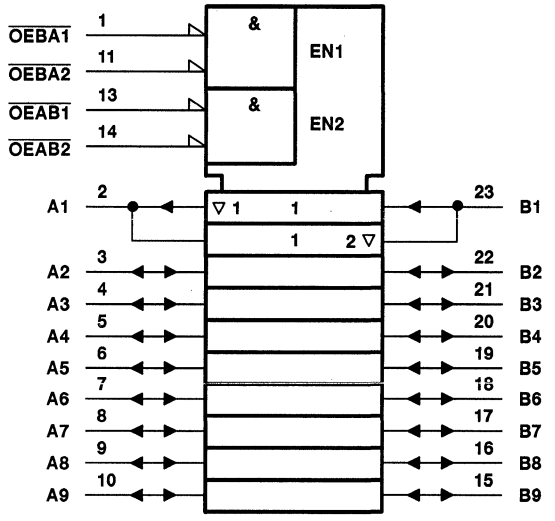
FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

PRODUCT PREVIEW

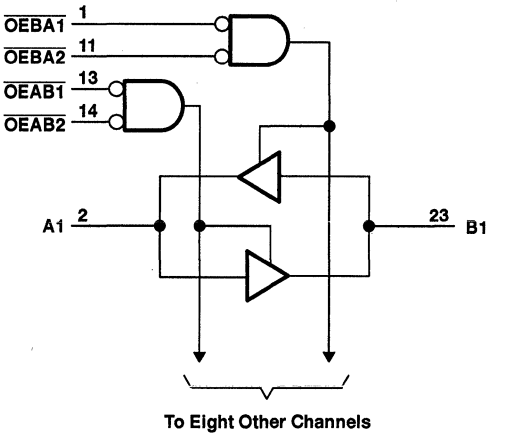
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

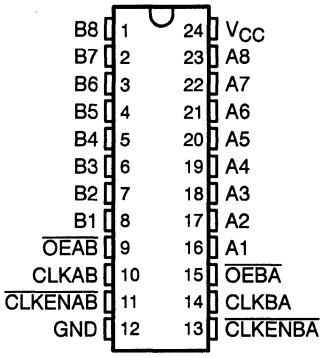
PARAMETER		TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C		UNIT
					MIN	MAX	
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = – 12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = – 24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	µA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		20	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

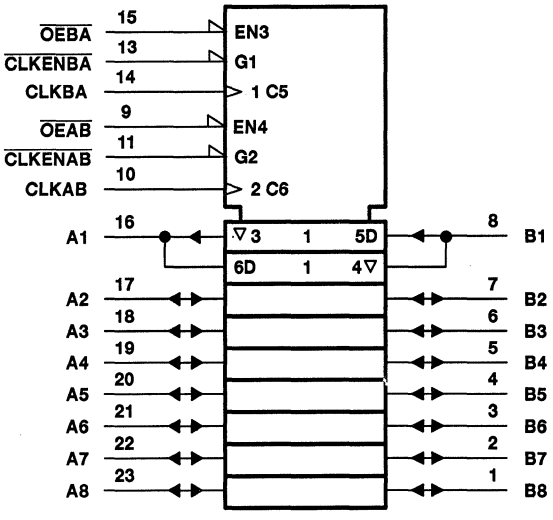
The SN74LVC2952 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B_0‡
X	H or L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

logic symbol§

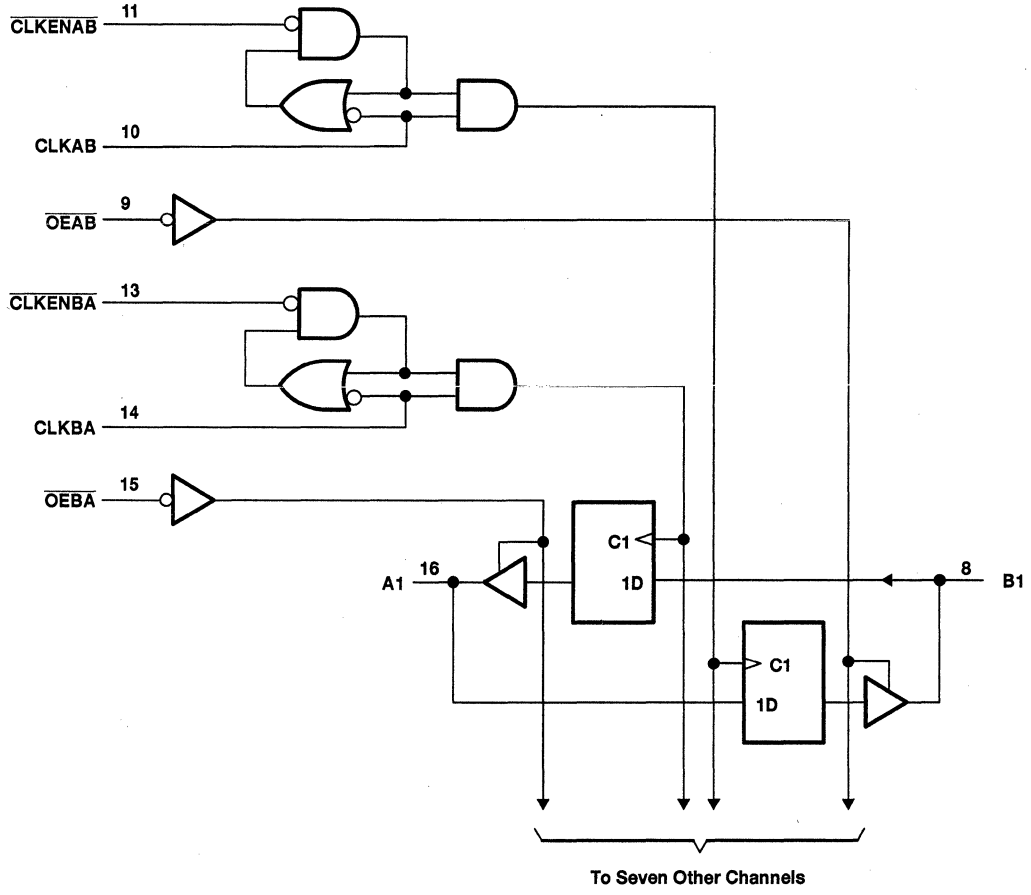


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.65 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	T_A = −40°C to 85°C		UNIT
				MIN	MAX	
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		V_I = V_{CC} or GND	3.6 V		±5	μA
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		20	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			500	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

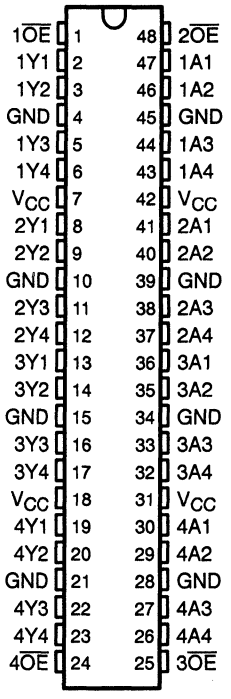
PRODUCT PREVIEW

LVC Widebus™

Features	Benefits
• 0.8-μ EPIC-II™ CMOS process	• High-performance propagation delays as fast as 6.5 ns
• Bus-hold cell on data inputs and I/Os	• Saves power, extends battery life
• Very low standby current (40 μA)	• Eliminates passive pullup resistors
• –24-mA/24-mA drive current	• Drives transmission lines down to 50 Ω
• 2.7-V to 3.6-V V_{CC} range	• Fully characterized for unregulated battery operation
• JEDEC SSOP Widebus™ and EIAJ TSSOP Shrink Widebus™ packaging	• Saves board space and weight; TSSOP compatible with PCMCIA standards
• TI has established two worldwide alternate sources	• Standardization that comes from a common product approach

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16240 is characterized for operation from –40°C to 85°C.

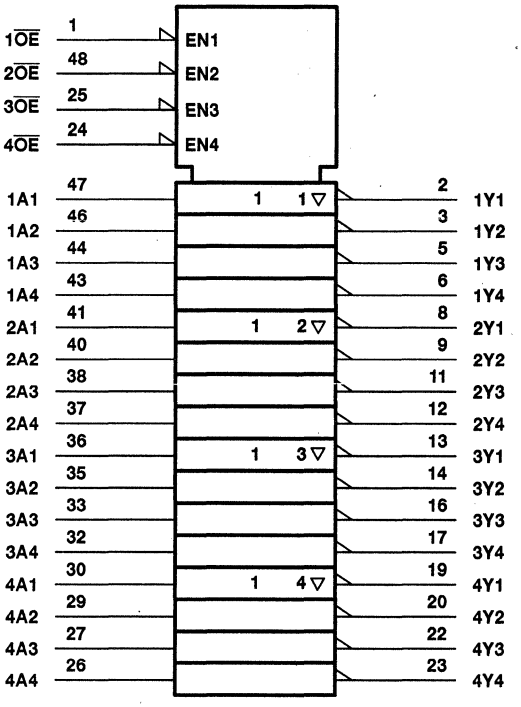
FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

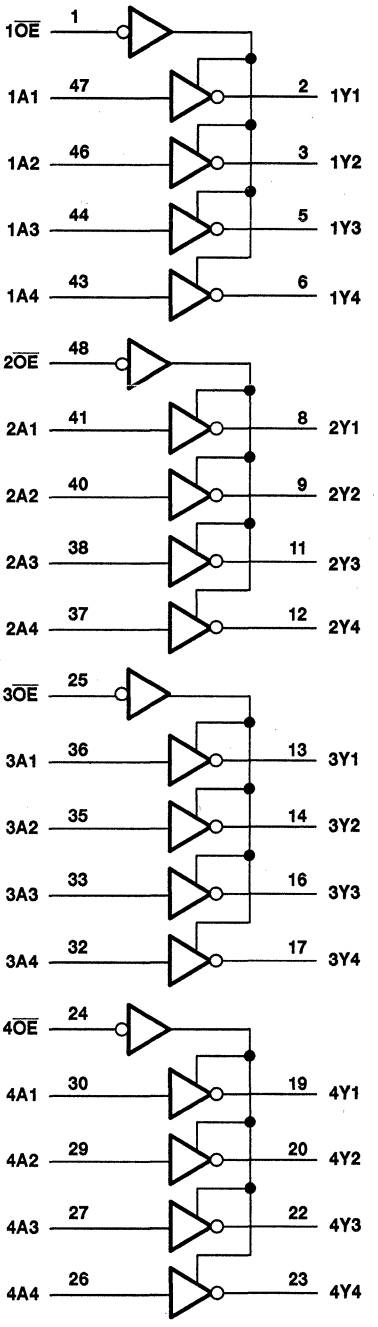
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

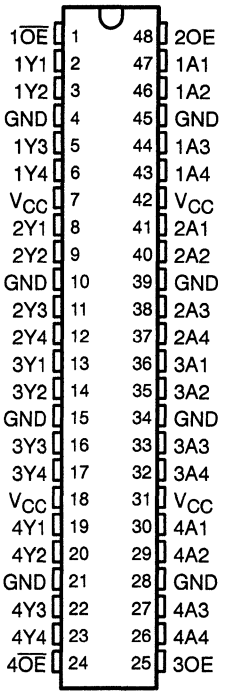
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 µA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		V_I = V_{CC} or GND	3.6 V		±5	µA
$I_{I(hold)}$	Data pins	V_I = 0.8 V	3 V	75		µA
		V_I = 2 V		–75		
I_{OZ}		V_O = V_{CC} or GND	3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	µA
C_i		V_I = V_{CC} or GND	3.3 V			pF
C_o		V_O = V_{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16241 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

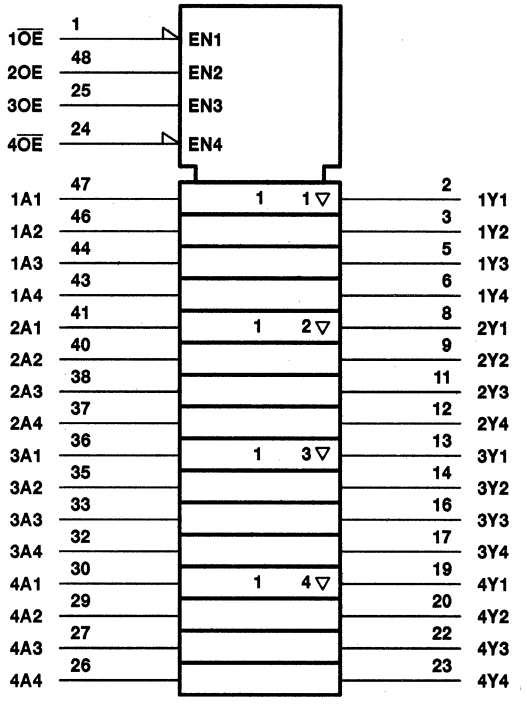
PRODUCT PREVIEW

FUNCTION TABLES

INPUTS		OUTPUTS
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

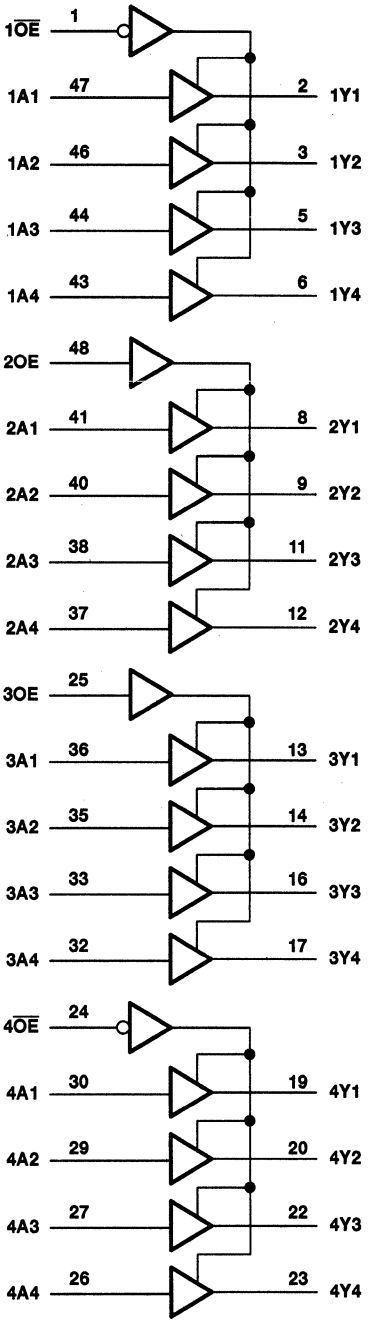
INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

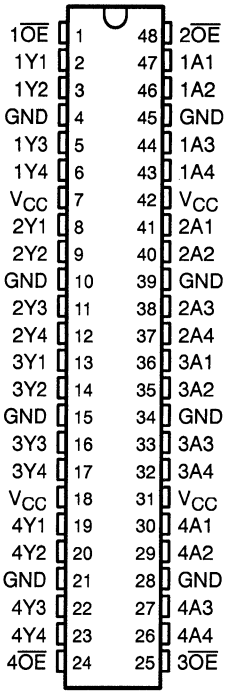
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			–75		
I_{OZ}		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i		V_I = V_{CC} or GND		3.3 V			pF
C_o		V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

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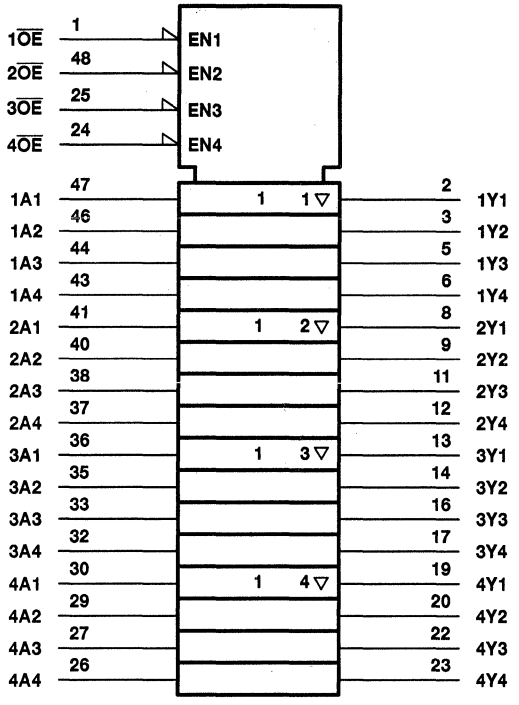
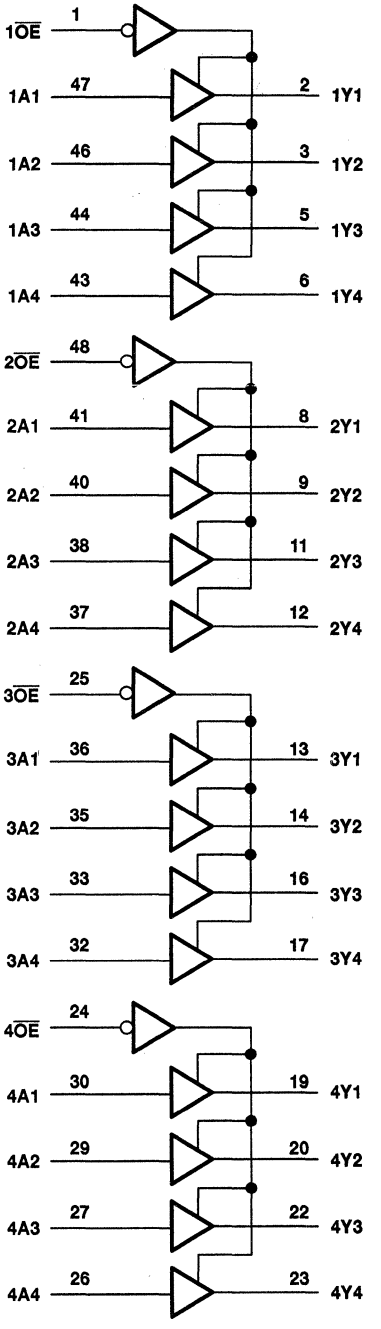
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

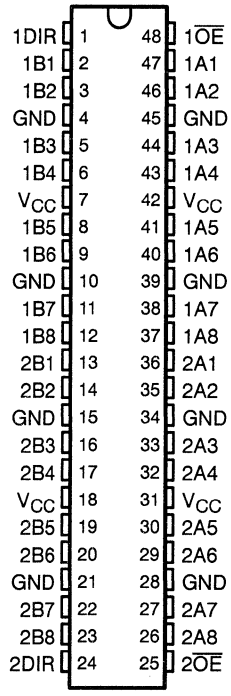
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			–75		
I_{OZ}		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i		V_I = V_{CC} or GND		3.3 V			pF
C_o		V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

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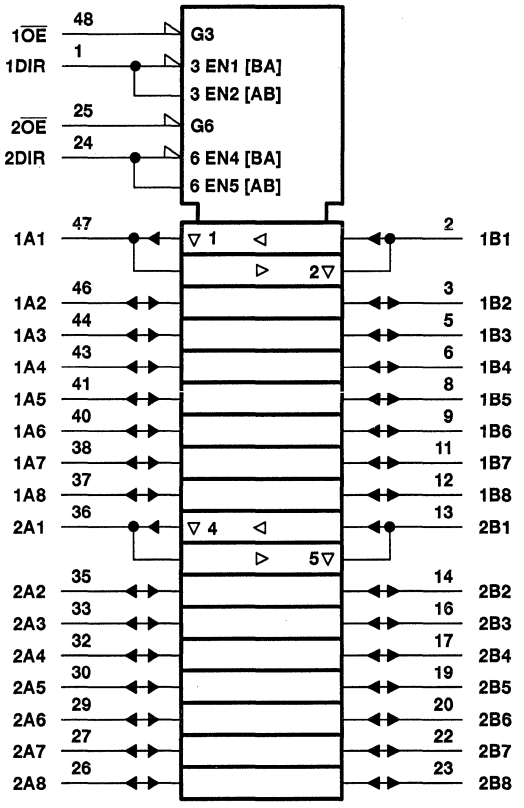
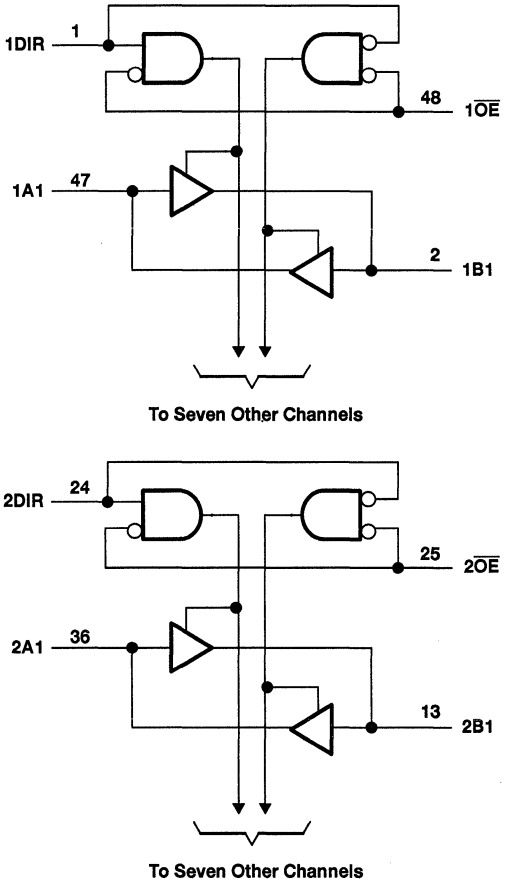
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

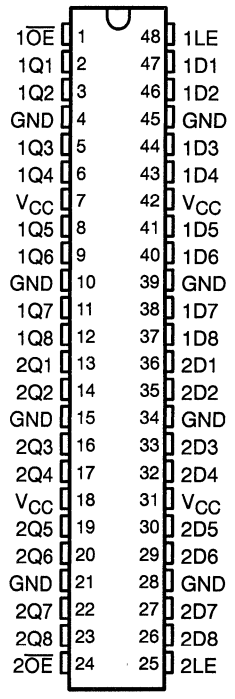
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	Control pins	$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

description

This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16373 is characterized for operation from –40°C to 85°C.

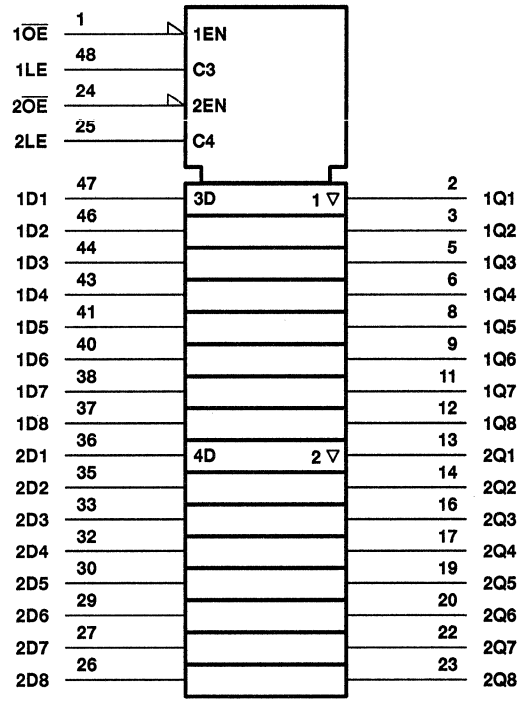
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 8-bit section)

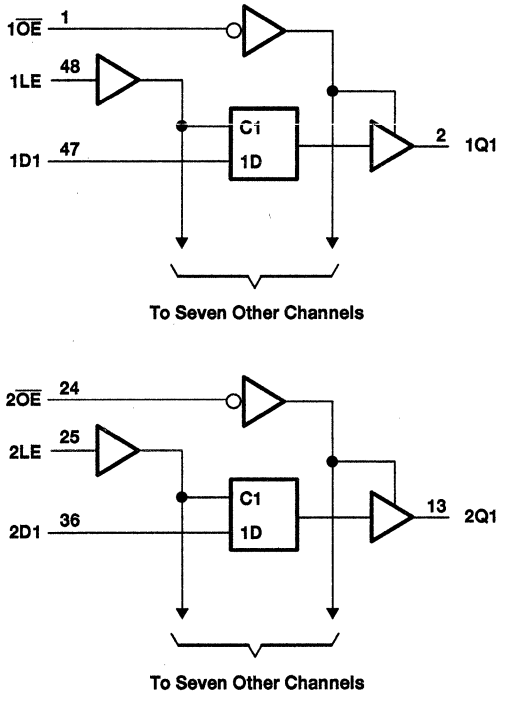
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

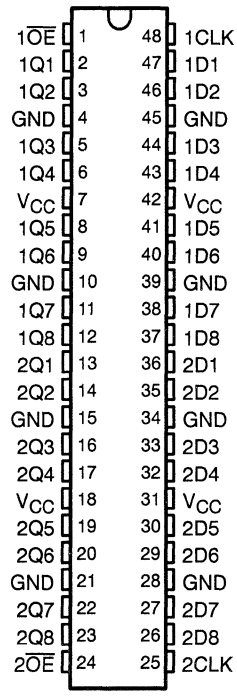
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	µA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		µA
		V_I = 2 V			–75		
I_{OZ}		V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i		V_I = V_{CC} or GND		3.3 V			pF
C_o		V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16374 is characterized for operation from –40°C to 85°C.

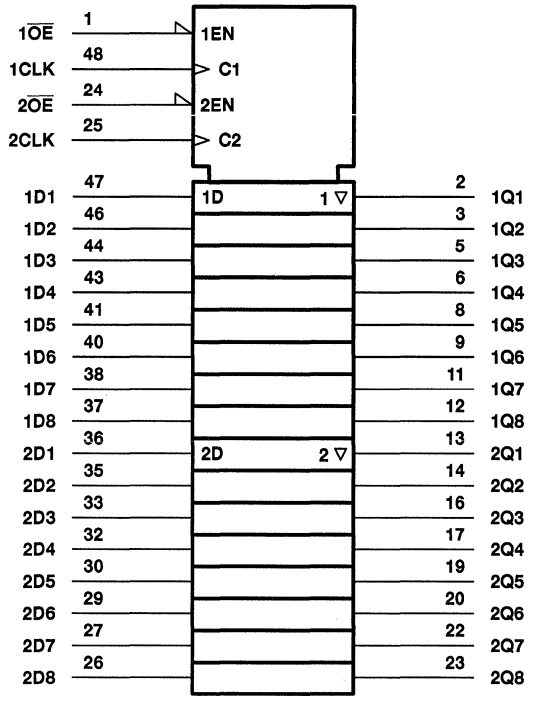
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

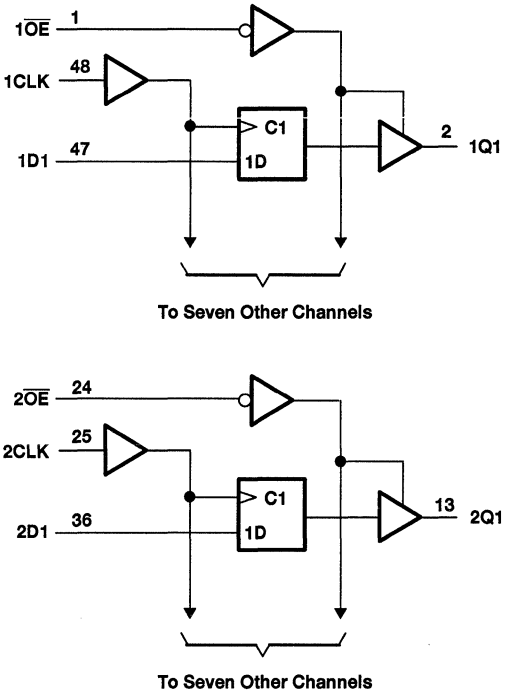
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

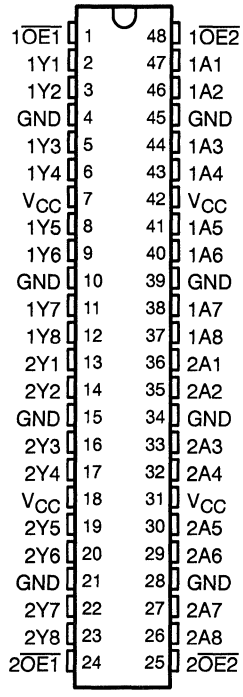
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		$V_I = V_{CC}$ or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			–75		
I_{OZ}		$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i		$V_I = V_{CC}$ or GND		3.3 V			pF
C_o		$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16540 provides a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN74LVC16540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

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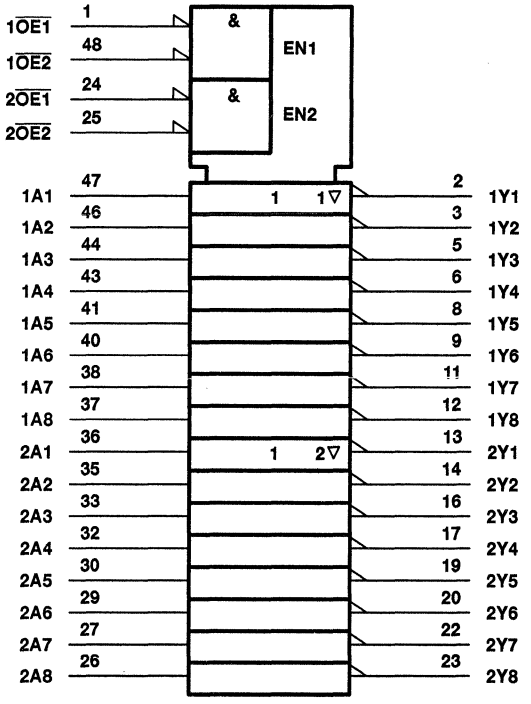
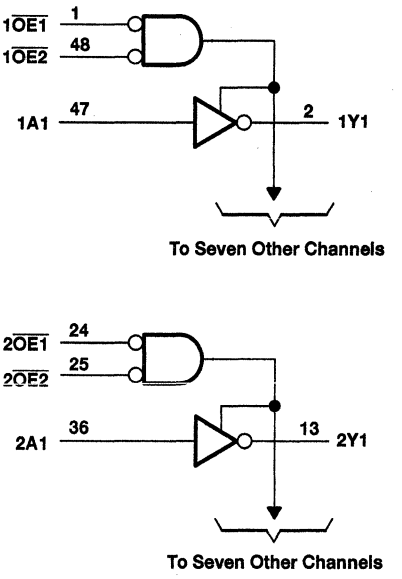
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

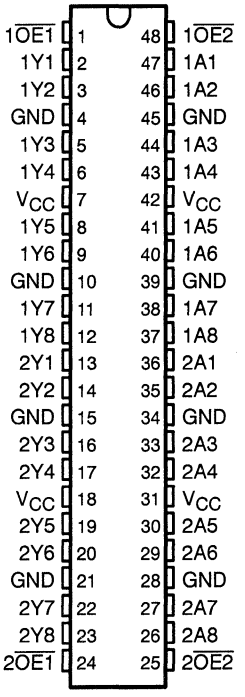
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			–75		
I_{OZ}		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	μA
C_i		V_I = V_{CC} or GND		3.3 V			pF
C_o		V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC16541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN74LVC16541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

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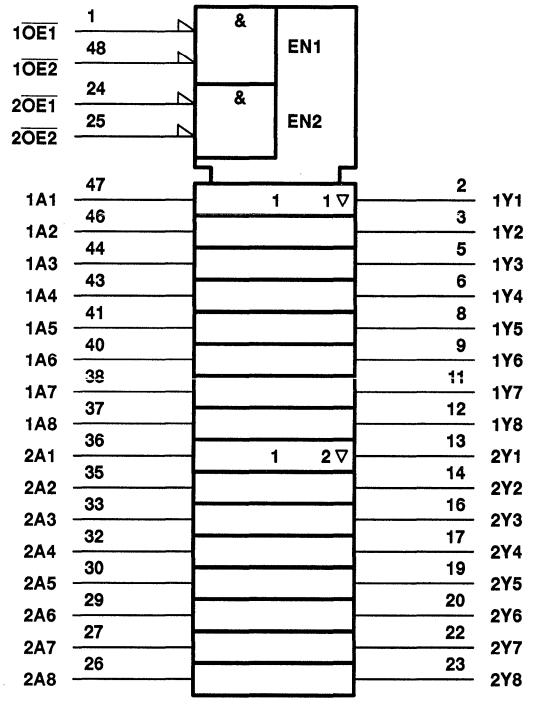
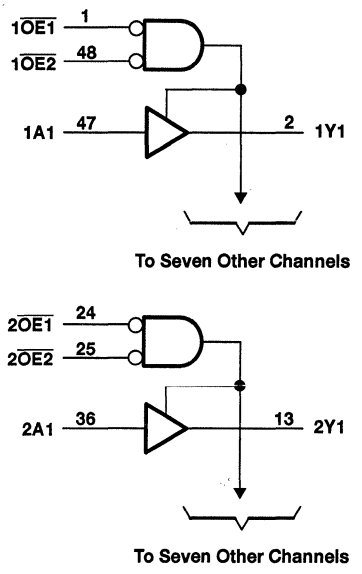
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

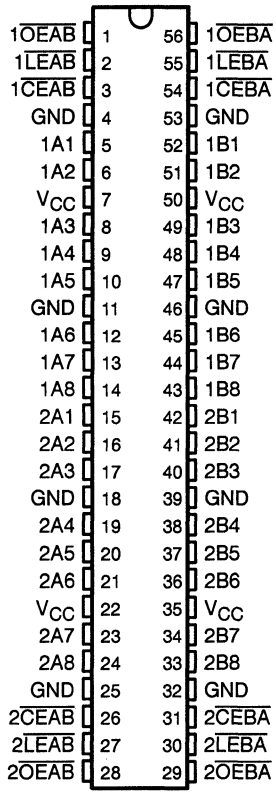
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		−75		
I_{OZ}		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			500	μA
C_i		$V_I = V_{CC}$ or GND	3.3 V			pF
C_o		$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit registered transceiver is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16543 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(each 8-bit section)

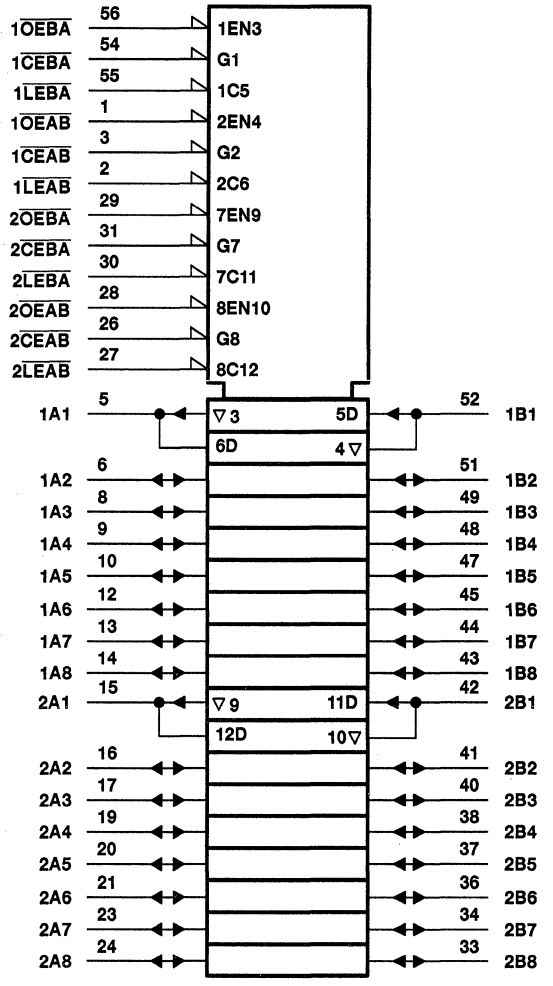
INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW

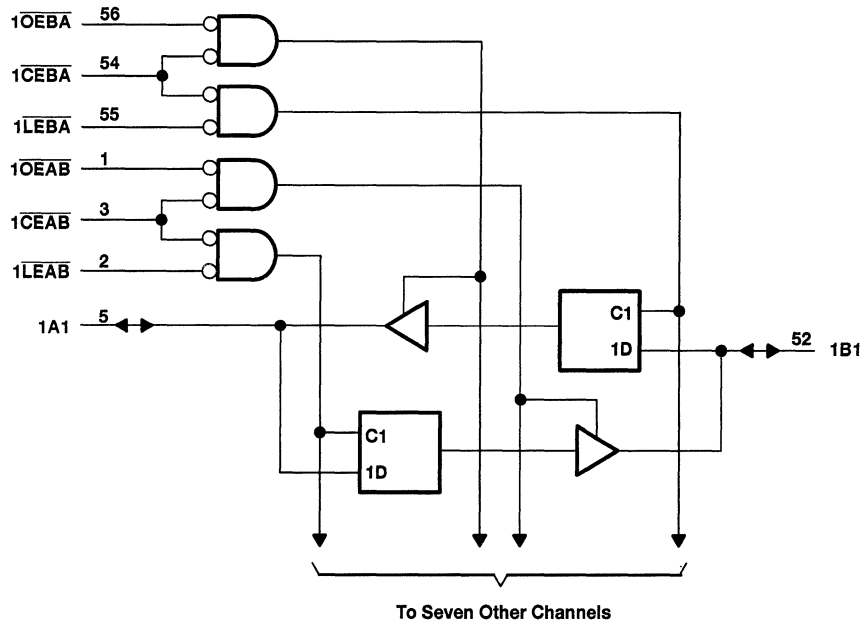
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

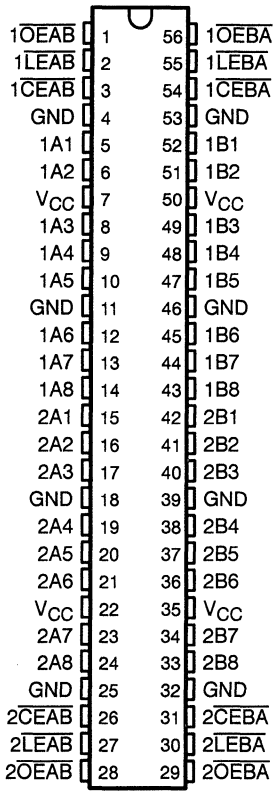
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Control inputs	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
$I_{I(hold)}$	A or B ports	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			−75		
I_{OZ}‡		$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit registered transceiver is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16544 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16544 is characterized for operation from –40°C to 85°C.

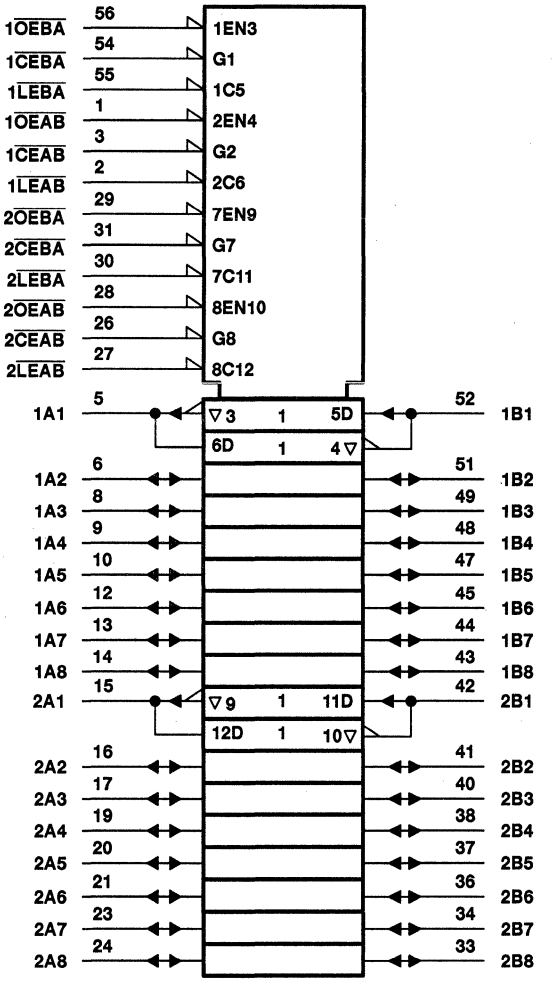
FUNCTION TABLE†
(each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	H
L	L	L	H	L

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

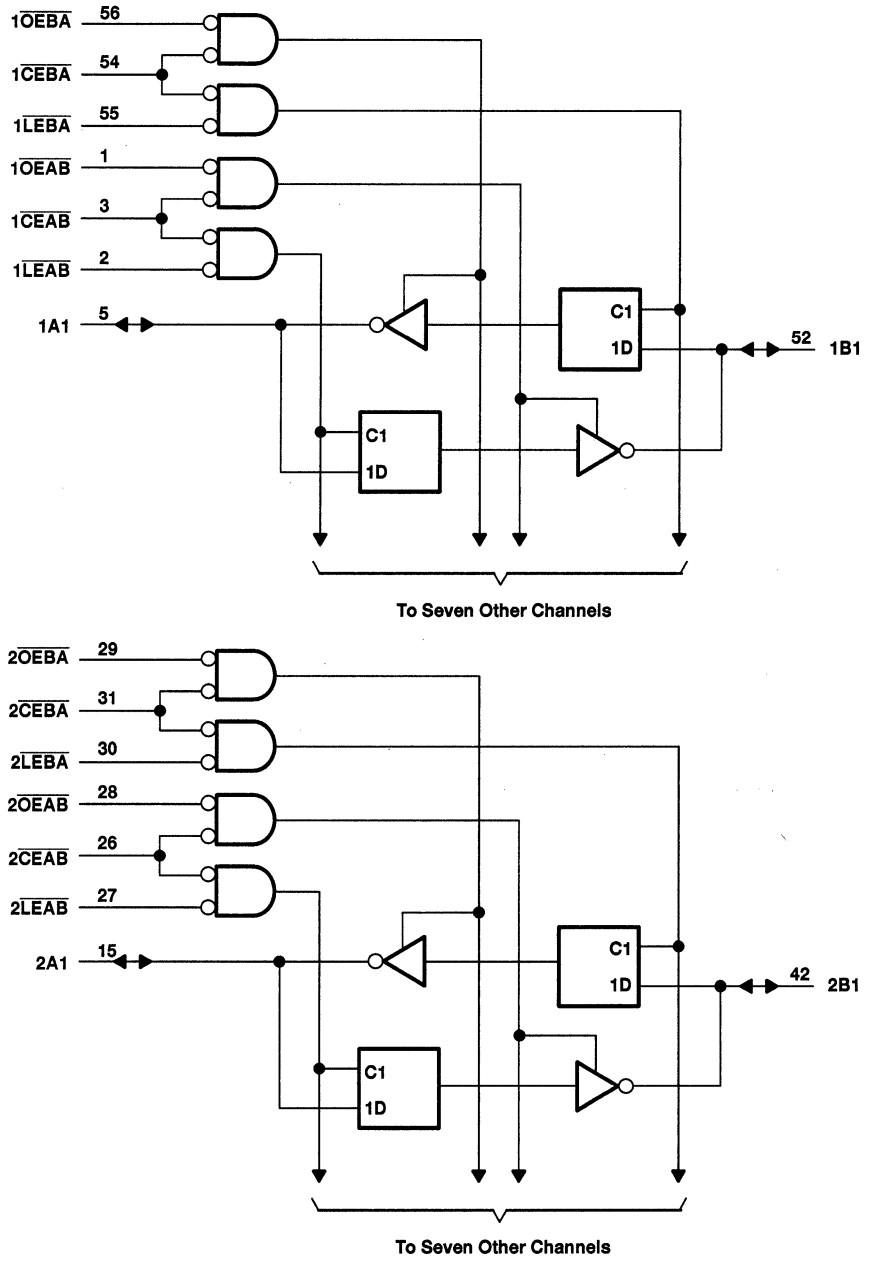
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

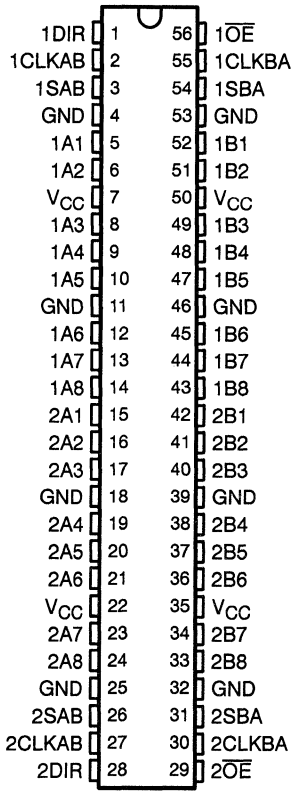
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	Control inputs	$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	A or B ports	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		−75		
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit bus transceiver and register is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

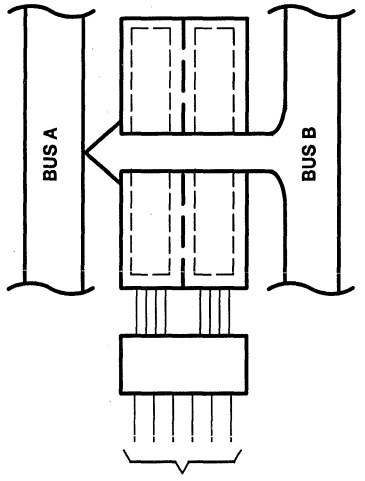
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16646 is characterized for operation from –40°C to 85°C.

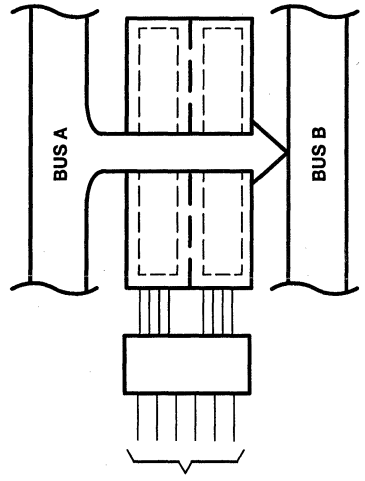
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW



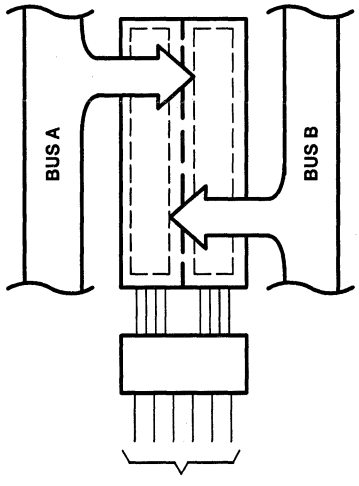
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



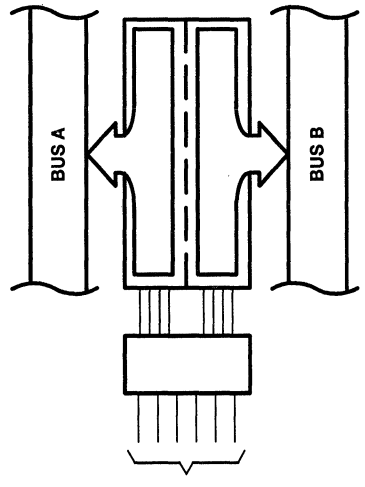
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

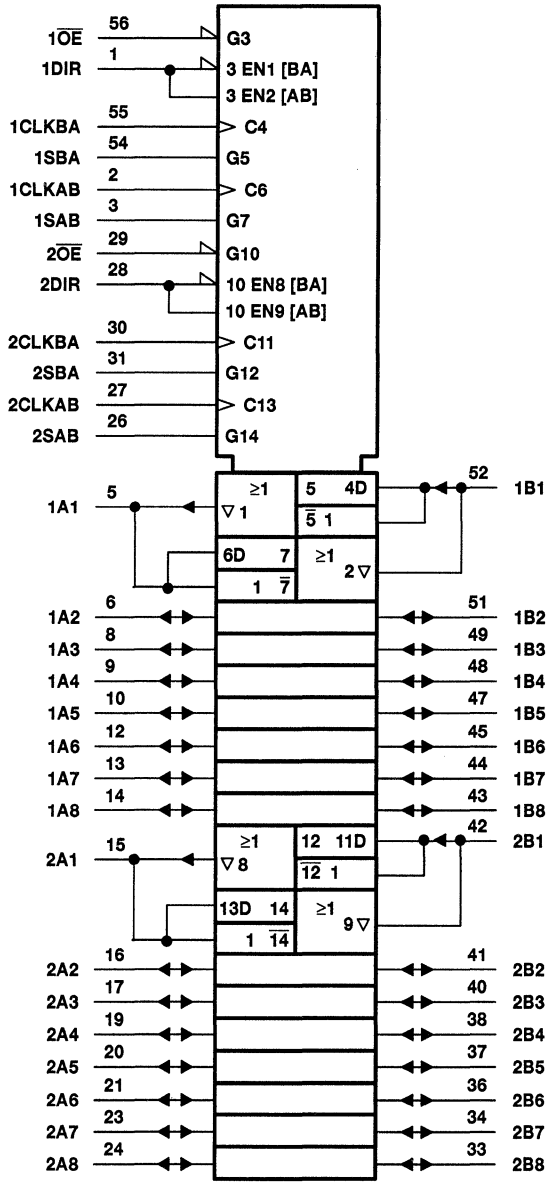


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

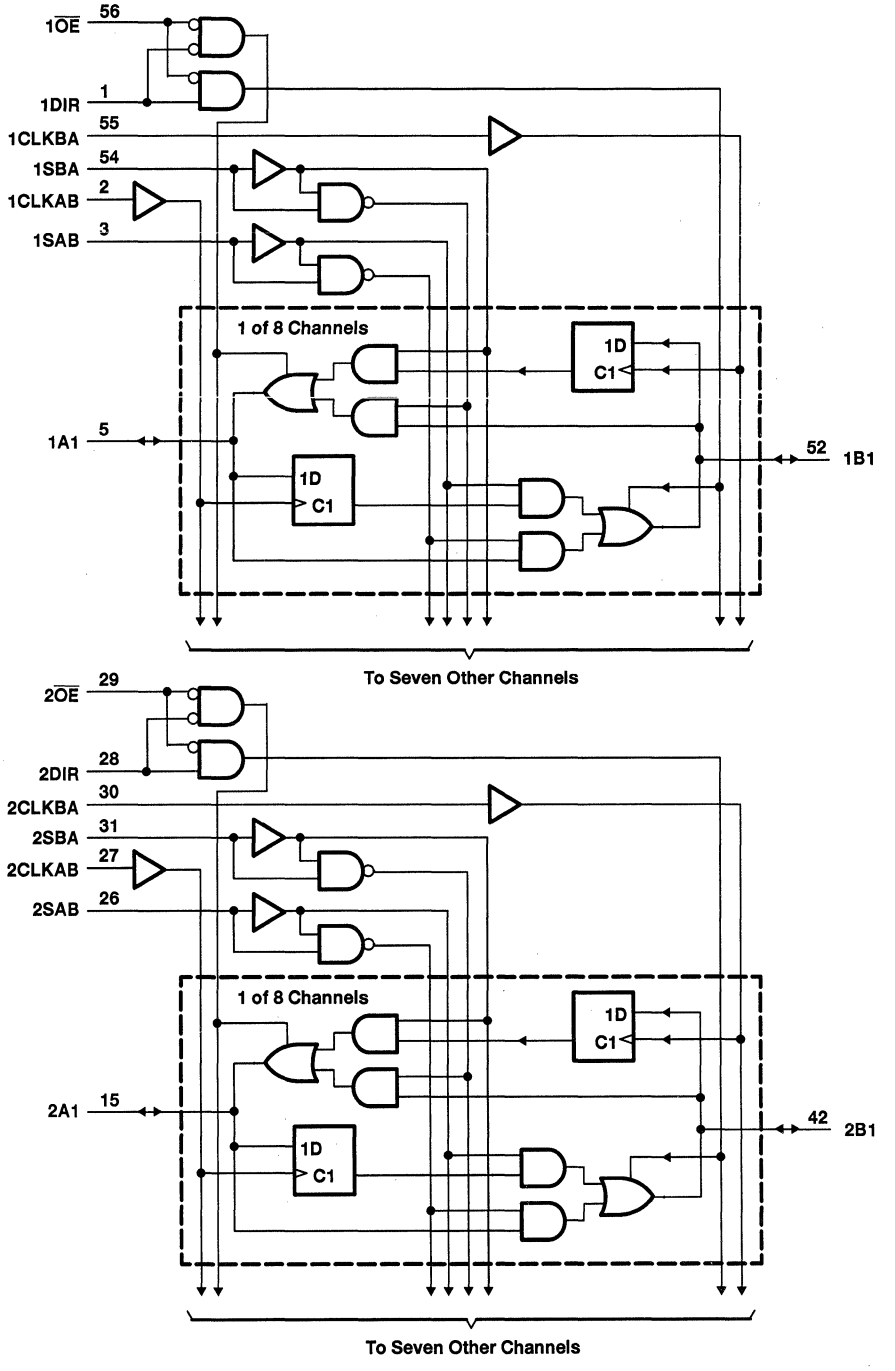
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

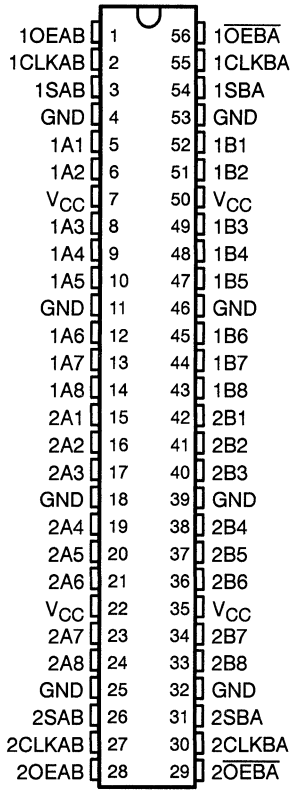
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Control inputs	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	A or B ports	V_I = 0.8 V		3 V	75		µA
		V_I = 2 V			–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit bus transceiver and register is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16652.

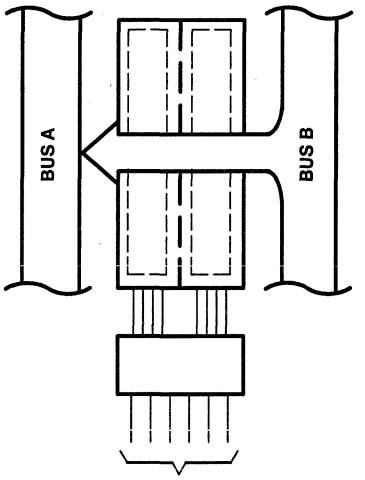
Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16652 is characterized for operation from –40°C to 85°C.

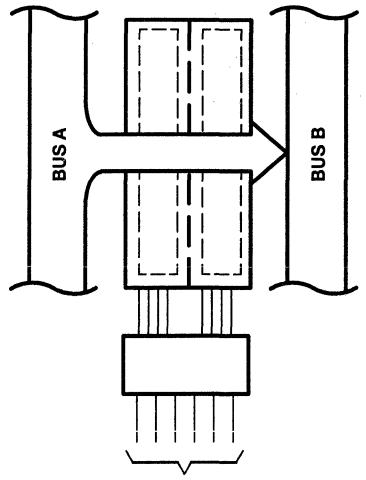
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



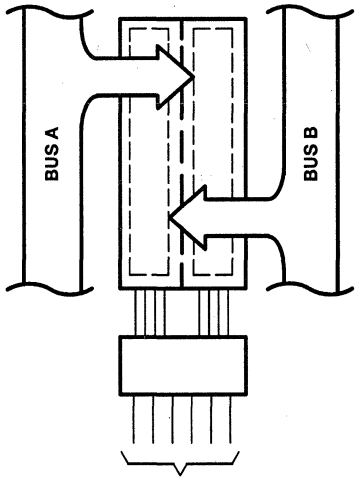
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



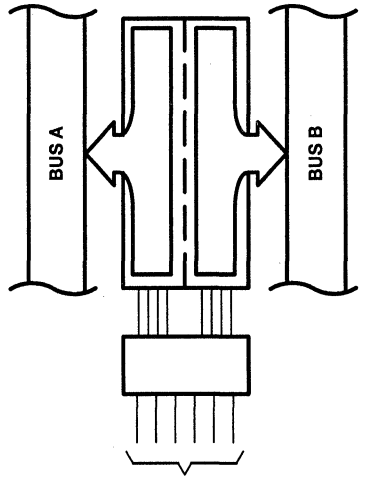
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

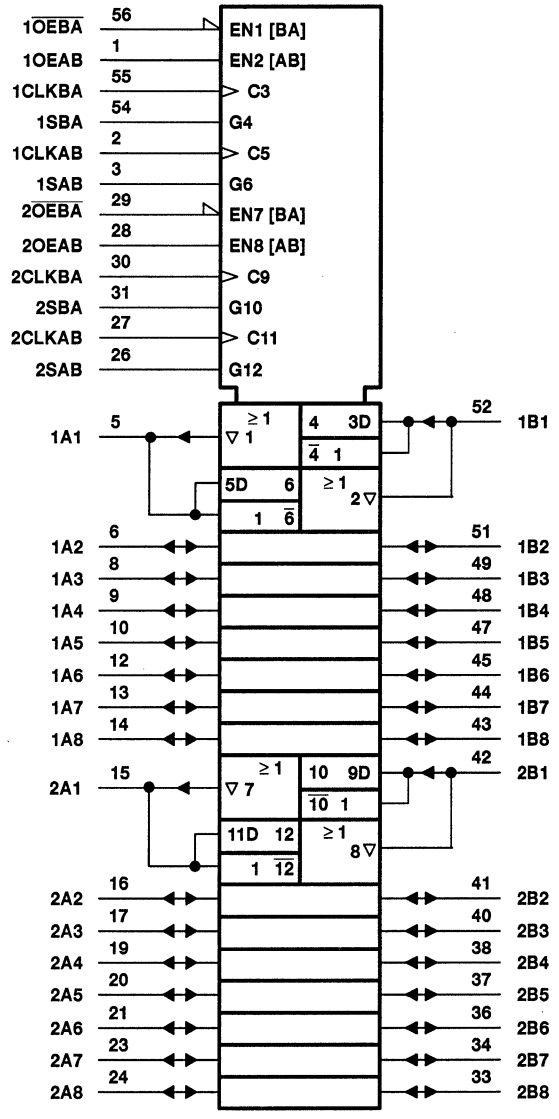


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

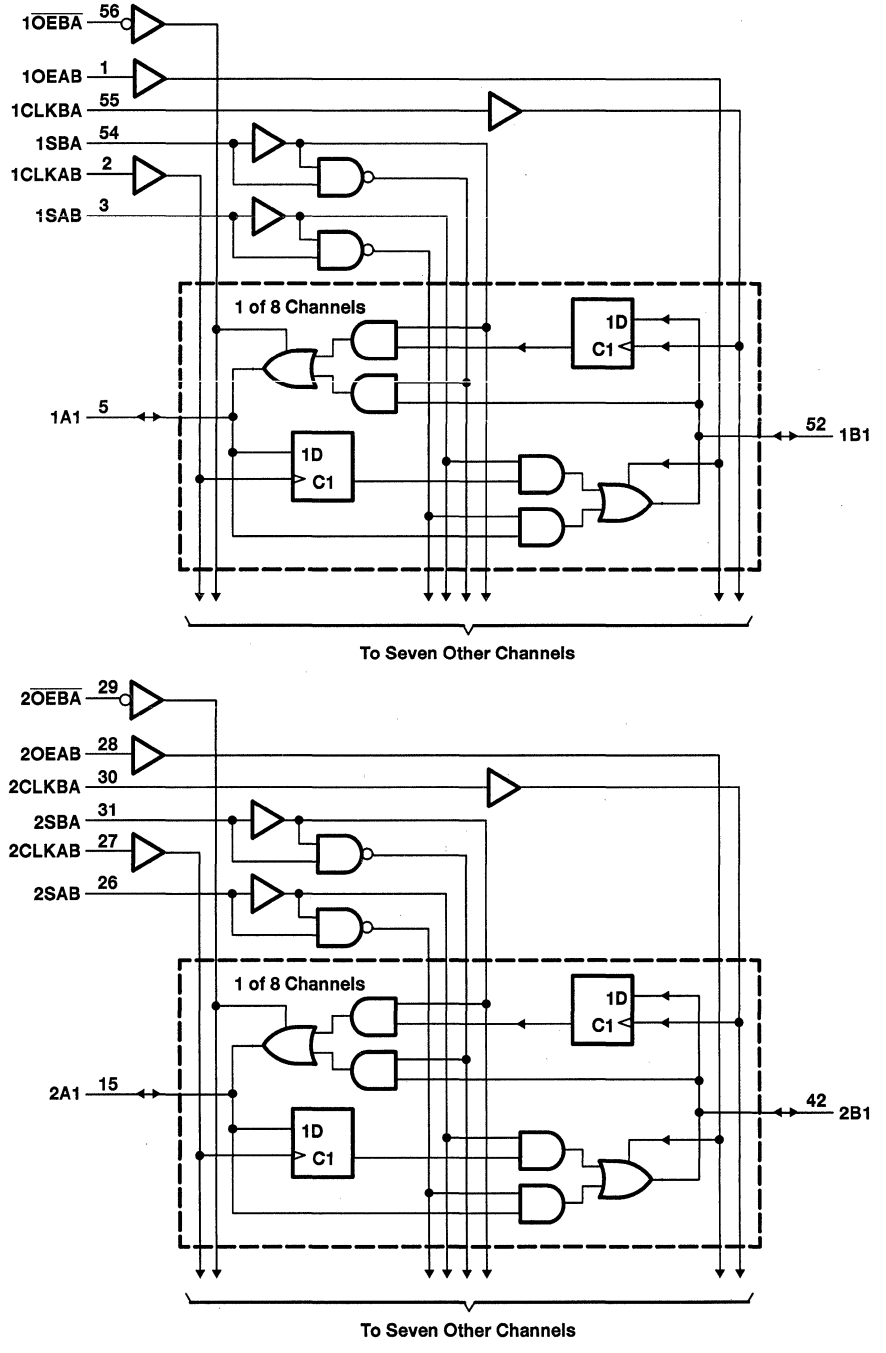
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

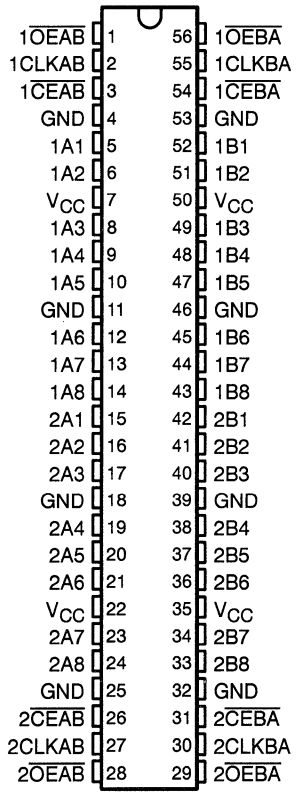
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 µA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 µA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	Control inputs	V_I = V_{CC} or GND	3.6 V		±5	µA
$I_{I(hold)}$	A or B ports	V_I = 0.8 V	3 V	75		µA
		V_I = 2 V		−75		
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			500	µA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit registered transceiver is designed for low-voltage (3.3 V) V_{CC} operation.

The SN74LVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CEAB}$ or $\overline{CEBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16952 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B_0‡
X	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

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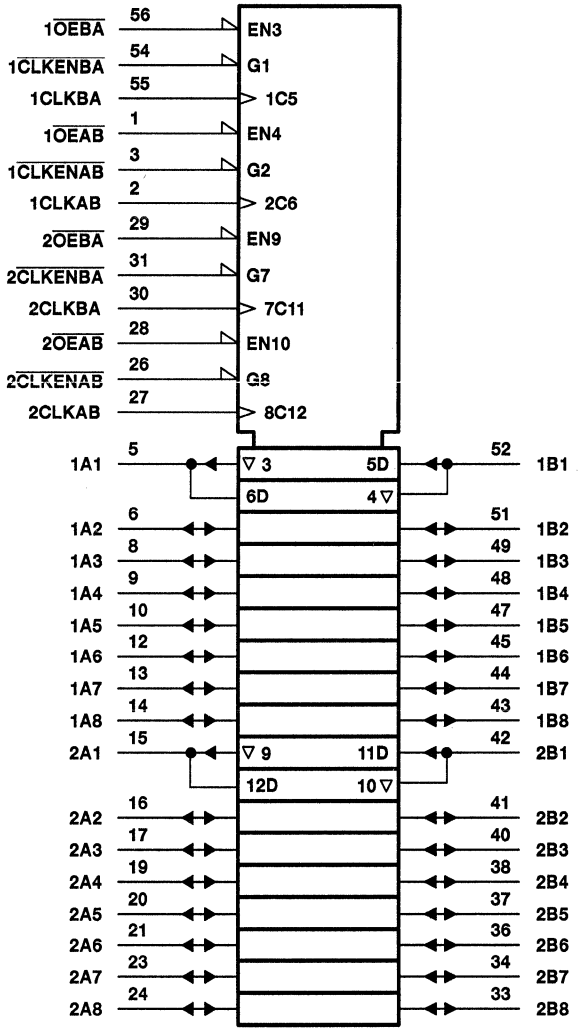
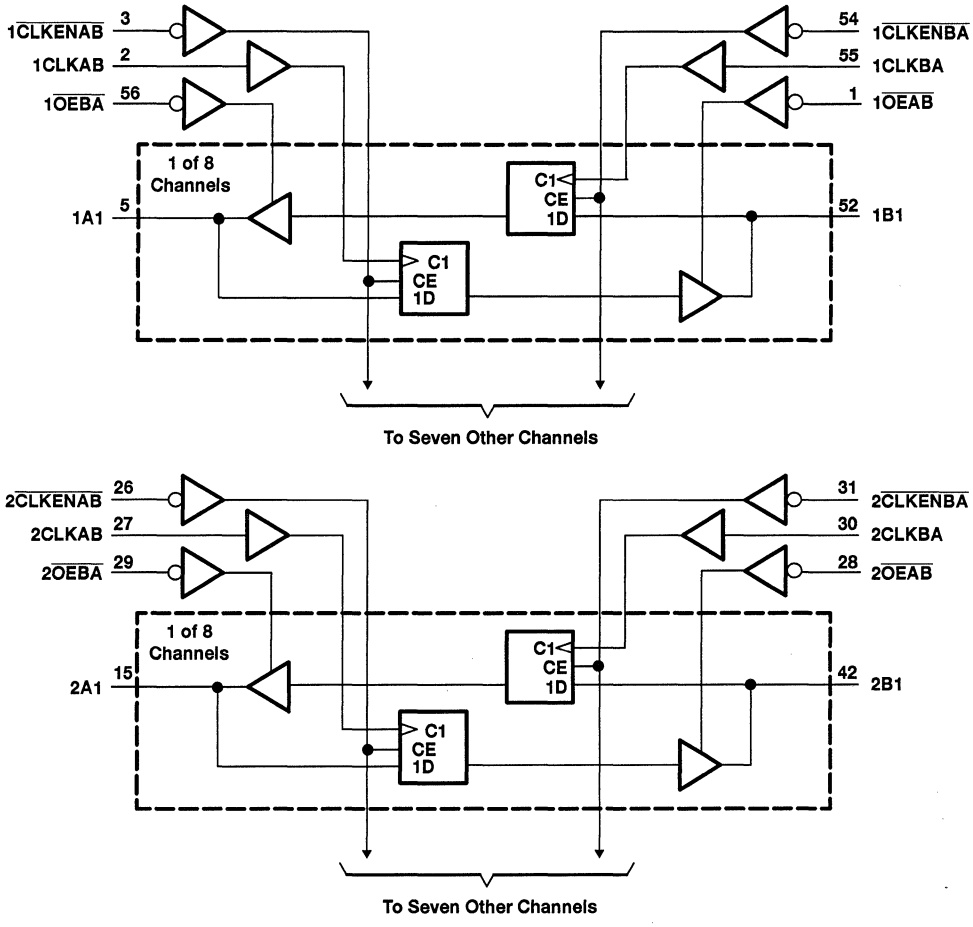
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating control pins must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Control inputs	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	A or B ports	V_I = 0.8 V		3 V	75		µA
		V_I = 2 V			–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			500	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

ALVC Widebus™

Features

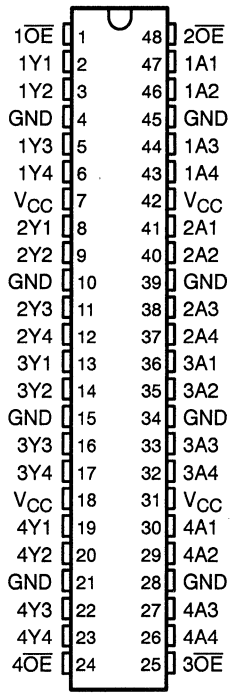
- State-of-the-art 0.6-μ EPIC-III™ CMOS process
- No input-diode clamp to V_{CC}
- Low standby current (20 μA)
- –24-mA/24-mA drive current
- 2.7-V to 3.6-V V_{CC} range
- JEDEC SSOP Widebus™ and EIAJ TSSOP Shrink Widebus™ packaging

Benefits

- Propagation delays as fast as 4 ns maximum for improved performance
- Saves power, extends battery life
- Drives transmission lines down to 50 Ω
- Fully characterized for unregulated battery operation
- Saves board space and weight; TSSOP compatible with PCMCIA standards

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The SN74ALVC16240 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16240 is characterized for operation from –40°C to 85°C.

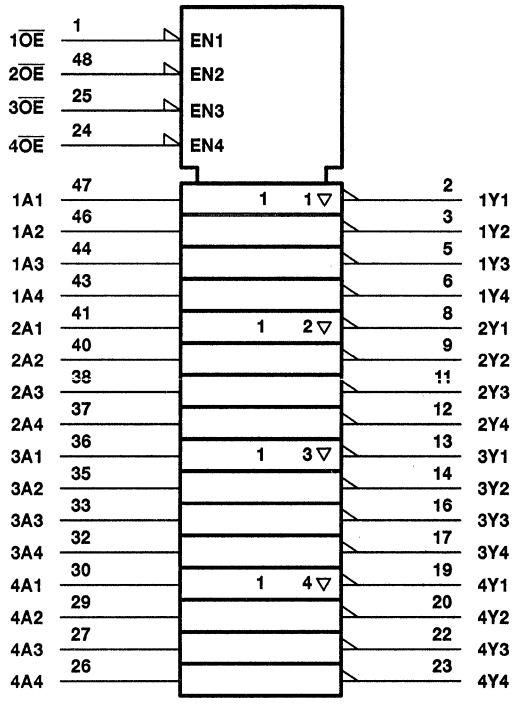
FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

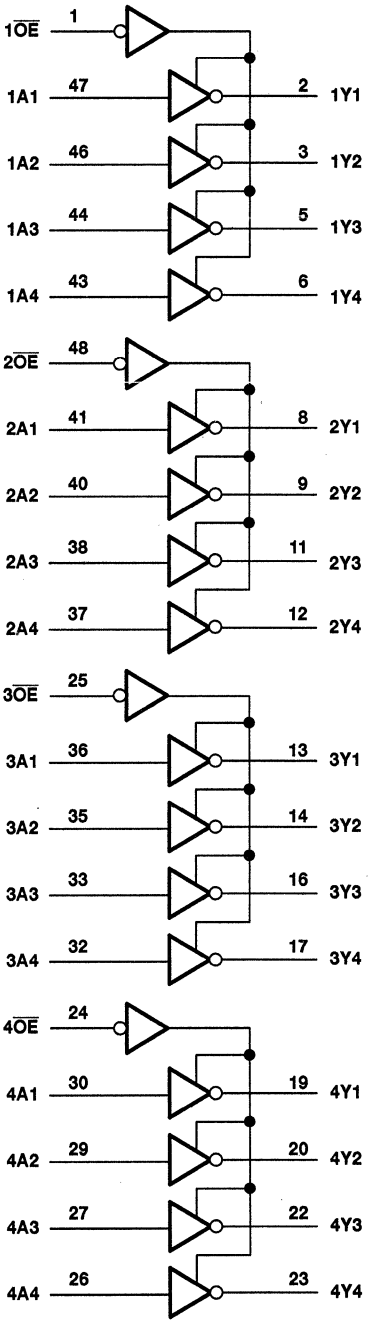
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

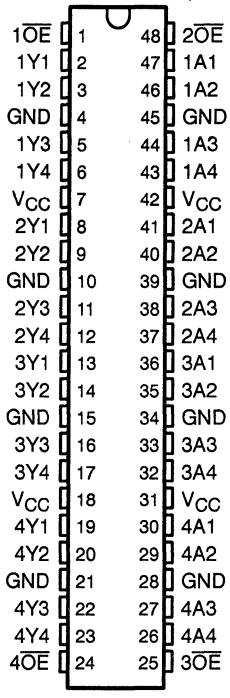
PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		µA
	V_I = 2 V			–75		
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16244 is characterized for operation from –40°C to 85°C.

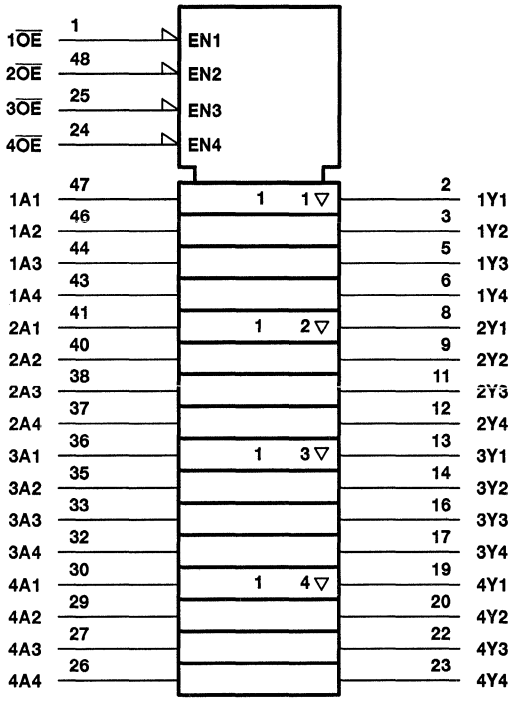
FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

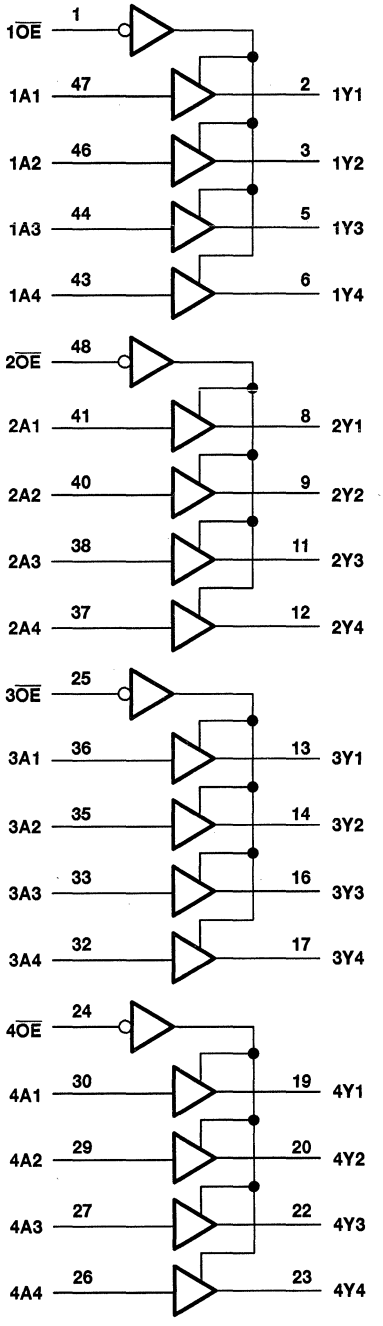
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL}		I_{OL} = 100 µA		MIN to MAX			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Inputs	V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75			µA
		V_I = 2 V			–75			
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				750	µA
C_i		V_I = V_{CC} or GND		3.3 V		3.5		pF
C_o		V_O = V_{CC} or GND		3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	1	2.2	3.6		4	ns
t_{en}	$\overline{OE}$	Y	1	2.7	5		6	ns
t_{dis}	$\overline{OE}$	Y	1	2.9	5		5.2	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

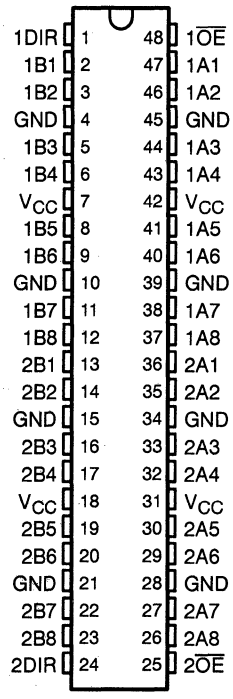
operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bit	Outputs enabled	C_L = 50 pF, f = 10 MHz	16	pF
		Outputs disabled		5	

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16245 is characterized for operation from –40°C to 85°C.

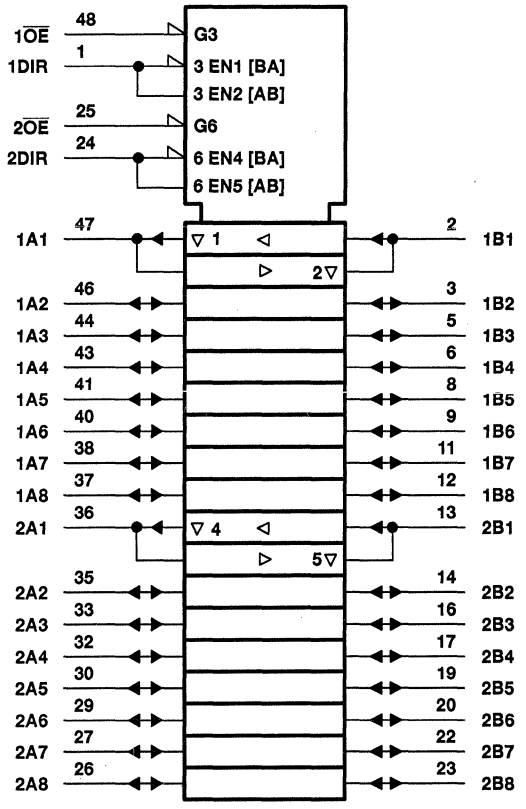
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

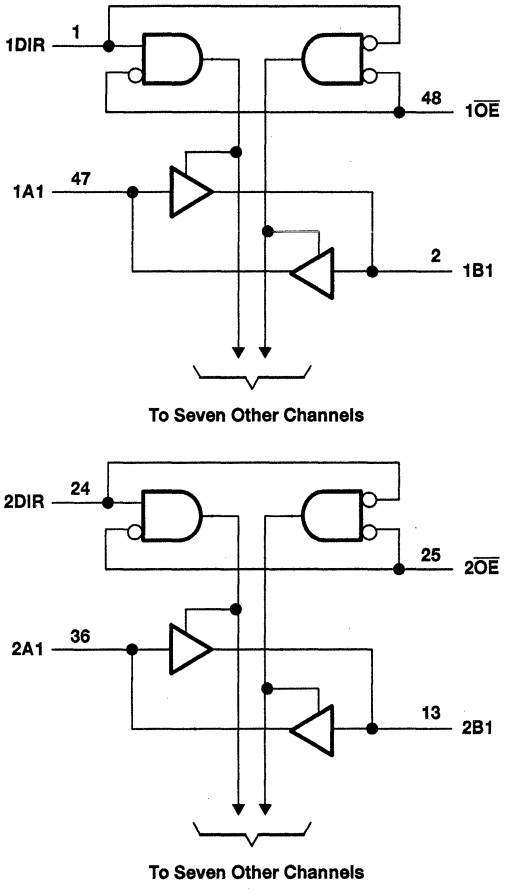
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2			V
		I_{OH} = −12 mA	2.7 V	2.2			
			3 V	2.4			
		I_{OH} = −24 mA	3 V	2			
V_{OL}		I_{OL} = 100 μA	MIN to MAX			0.2	V
		I_{OL} = 12 mA	2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
I_I	Control pins	V_I = V_{CC} or GND	3.6 V			±5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75			μA
		V_I = 2 V		−75			
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				750	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		3.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1	2.2	3.6		4	ns
t_{en}	$\overline{OE}$	B or A	1	2.7	5		6	ns
t_{dis}	$\overline{OE}$	B or A	1	2.9	5		5.2	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

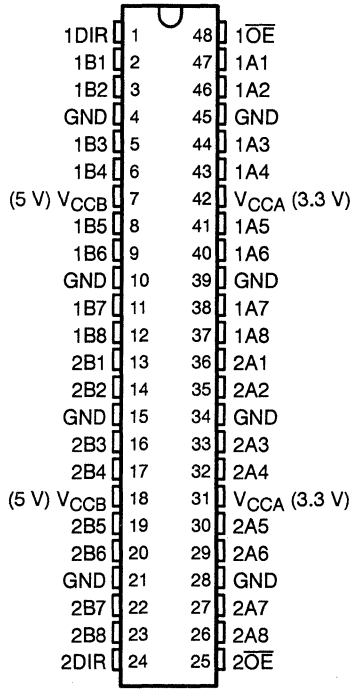
operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bit	Outputs enabled	C_L = 50 pF, f = 10 MHz	28	pF
		Outputs disabled		4	

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Inputs Are TTL-Voltage Compatible**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} which is set at 5 V, and A port has V_{CCA} which is set to operate at 3.3 V. This allows for translation from a 3.3-V to a 5-V environment and vice-versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

The SN74ALVC164245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC164245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

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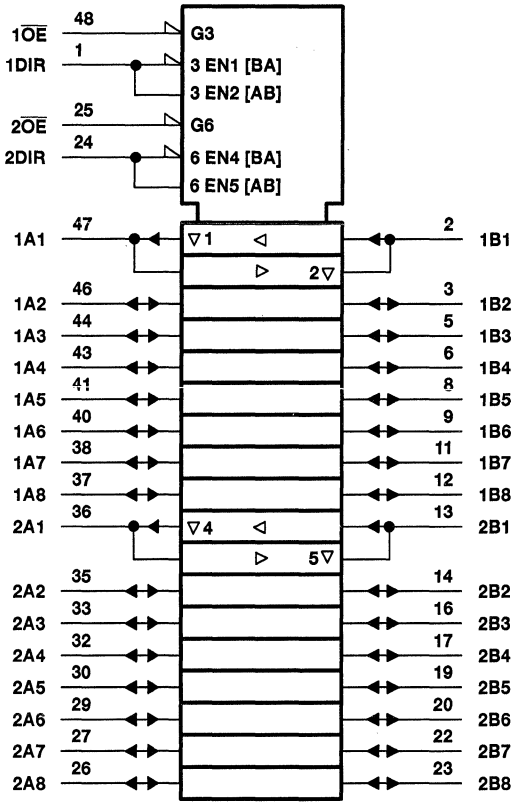
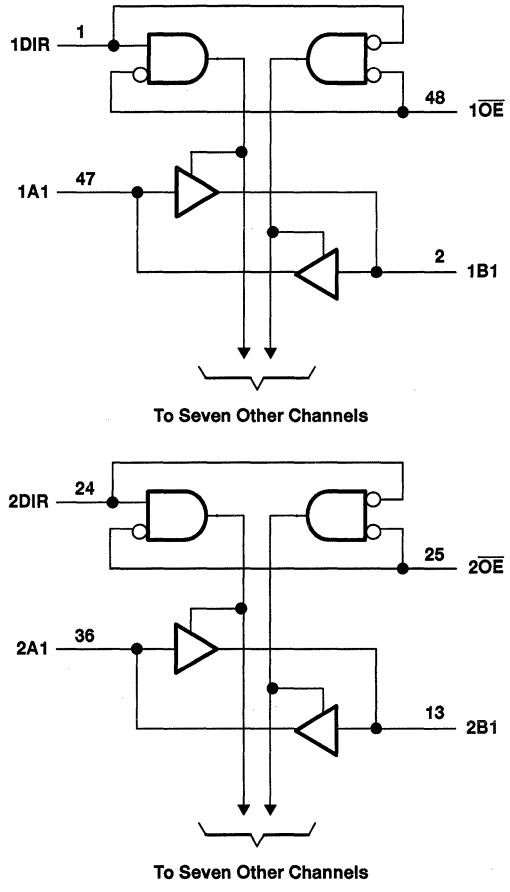
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V (unless otherwise noted)†

Supply voltage range, V_{CCB}	−0.5 V to 6 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CCB} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CCB}$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CCB}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CCB})	±50 mA
Continuous current through V_{CCB} or GND	±100 mA

NOTE 1: This value is limited to 6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCA} at 3.3 V (unless otherwise noted)†

Supply voltage range, V_{CCA}	−0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 2)	−0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Note 2)	−0.5 V to V_{CCA} + 0.5 V
Output voltage range, V_O (see Note 2)	−0.5 V to V_{CCA} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CCA}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CCA})	±50 mA
Continuous current through V_{CCA} or GND	±100 mA

NOTE 2: This value is limited to 4.6 V maximum.

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V or for V_{CCA} at 3.3 V (unless otherwise noted)†

Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions for V_{CCB} at 5 V

		MIN	NOM	MAX	UNIT
V_{CCB}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CCB}	V
V_O	Output voltage	0		V_{CCB}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

recommended operating conditions for V_{CCA} at 3.3 V

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCA} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CCA}	V
V_O	Output voltage		0	V_{CCA}	V
I_{OH}	High-level output current	V_{CCA} = 2.7 V		−12	mA
		V_{CCA} = 3 V		−24	
I_{OL}	Low-level output current	V_{CCA} = 2.7 V		12	mA
		V_{CCA} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range for V_{CCB} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCB}	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	4.5 V	4.3		V
			5.5 V	5.3		
		I_{OH} = −24 mA	4.5 V	3.7		
			5.5 V	4.7		
V_{OL}		I_{OL} = 100 μA	4.5 V		0.2	V
			5.5 V		0.2	
		I_{OL} = 24 mA	4.5 V		0.55	
			5.5 V		0.55	
I_I	Control pins	$V_I = V_{CCB}$ or GND	5.5 V		5	μA
I_{OZ}†	A or B ports	$V_O = V_{CCB}$ or GND	5.5 V			μA
I_{CC}		$V_I = V_{CCB}$ or GND, I_O = 0	5.5 V			μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CCB} or GND				μA
C_i	Control inputs	$V_I = V_{CCB}$ or GND	5 V			pF
C_{io}	A or B ports	$V_O = V_{CCB}$ or GND	5 V			pF

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	Control pins	$V_I = V_{CCA}$ or GND	3.6 V		5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		−75		
I_{OZ}‡		$V_O = V_{CCA}$ or GND	3.6 V			μA
I_{CC}		$V_I = V_{CCA}$ or GND, I_O = 0	3.6 V			μA
ΔI_{CC}§		V_{CCA} = 3 V to 3.6 V, One input at V_{CCA} − 0.6 V, Other inputs at V_{CCA} or GND				μA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CCA}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CCB}.

PRODUCT PREVIEW

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- **Member of the Texas Instruments *Widebus*™ Family**
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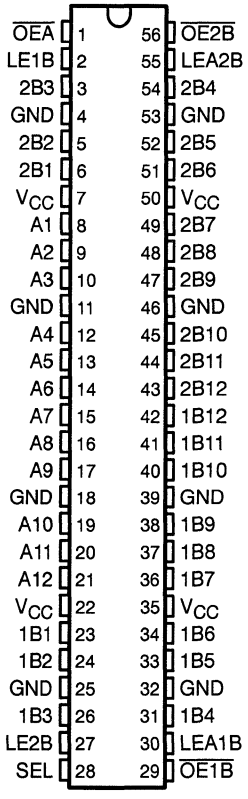
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16260 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16260 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Function Tables

B TO A ($\overline{OEB}$ = H)

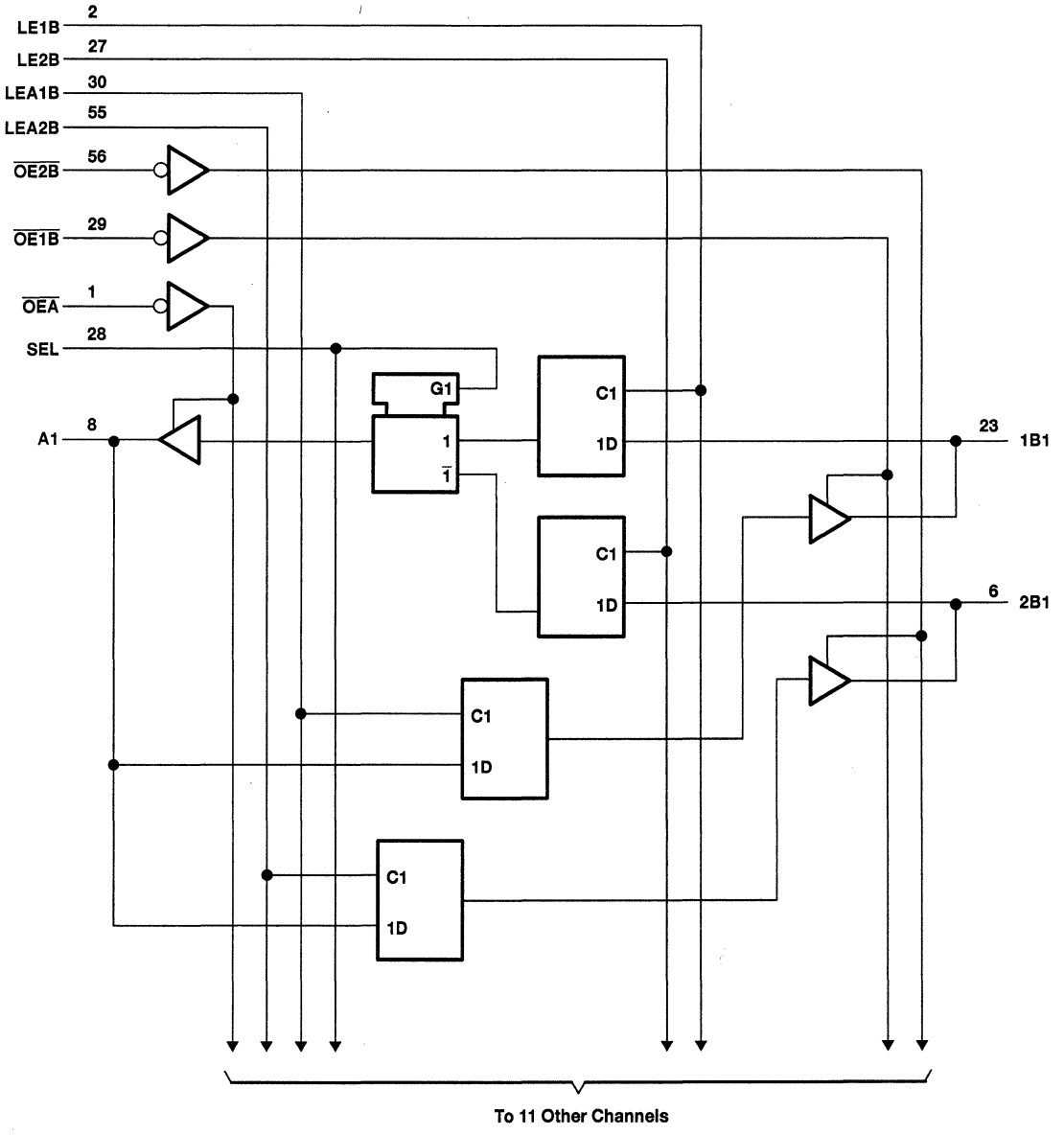
INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0
X	X	X	X	X	H	Z

A TO B ($\overline{OEA}$ = H)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Inputs	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			–75		
I_{OZ}		$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	μA
C_i		$V_I = V_{CC}$ or GND		3.3 V			pF
C_o		$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

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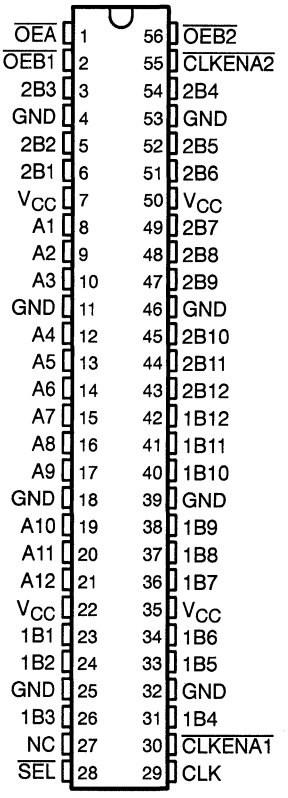
- **Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16269 is a 12-bit to 24-bit registered bus exchanger, which is intended for applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between sync DRAMs and high-speed microprocessors. The SN74ALVC16269 is designed specifically for low-voltage (3.3 V) V_{CC} operation.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{\text{CLKENA}}$ inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data will be valid on the bus. The control pins are registered so that all transactions are synchronous with the clock. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, $\overline{\text{OEB2}}$).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

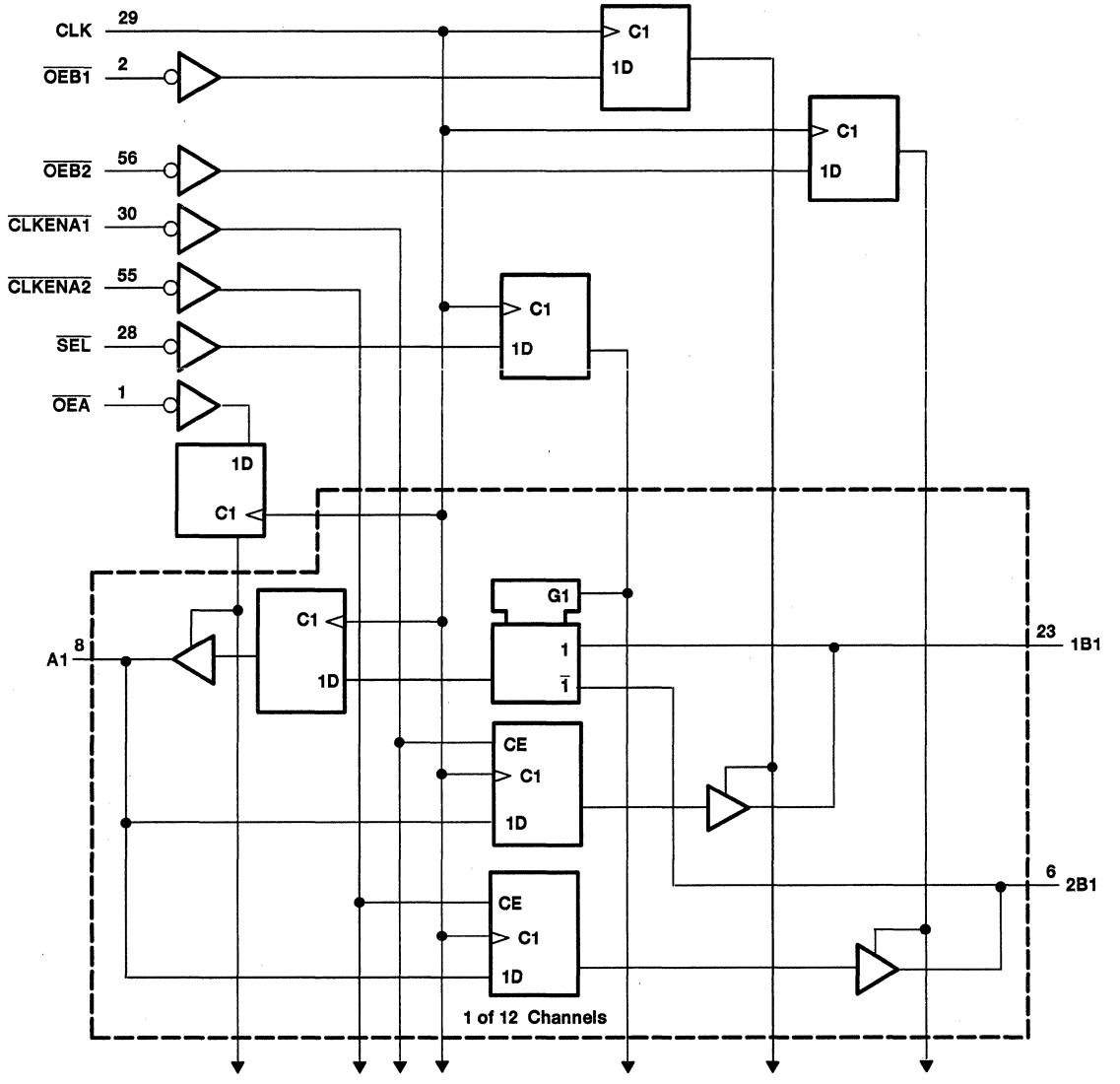
The SN74ALVC16269 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16269 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



Function Tables

OUTPUT-ENABLE TABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

B-TO-A STORAGE TABLE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
X	H	X	X	A_0†
X	L	X	X	A_0†
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Inputs	V_I = V_{CC} or GND		3.6 V		±5	µA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		µA
		V_I = 2 V			−75		
I_{OZ}		V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	µA
C_i		V_I = V_{CC} or GND		3.3 V			pF
C_{io}		V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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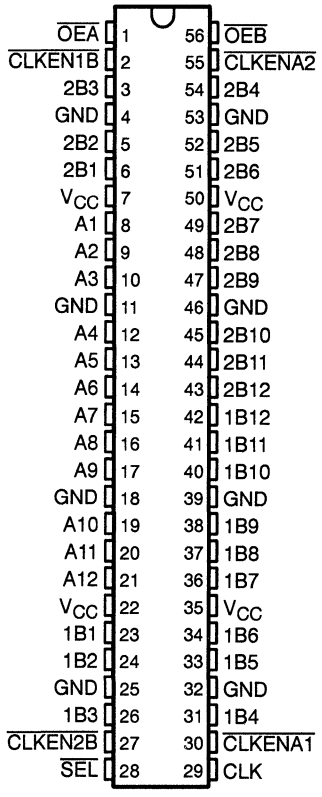
DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16270 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

The device provides for synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{\text{CLKEN}}$ inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the $\overline{\text{CLKENA}}$ inputs allow two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$). These control pins are registered so that bus direction changes are synchronous with the clock.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

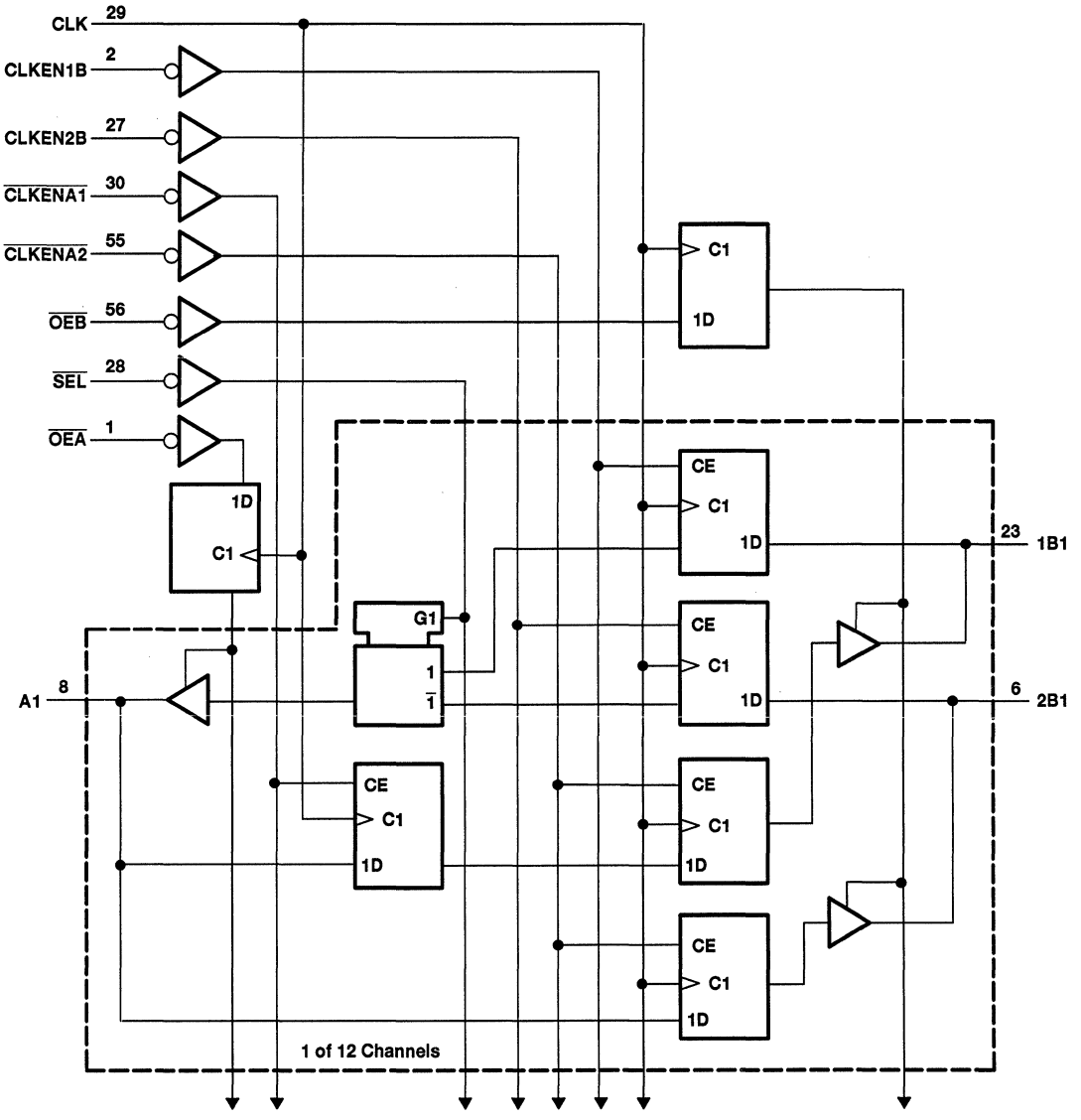
The SN74ALVC16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16270 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



Function Tables

OUTPUT-ENABLE TABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L[1]	X
L	X	↑	H	H[1]	X
X	L	↑	L	X	L
X	L	↑	H	X	H

[1] Two CLK edges are needed to propagate data.

B-TO-A STORAGE TABLE ($\overline{OEA}$ = L)

INPUTS						OUTPUT
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	A
H	X	X	H	X	X	A_0†
X	H	X	L	X	X	A_0†
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

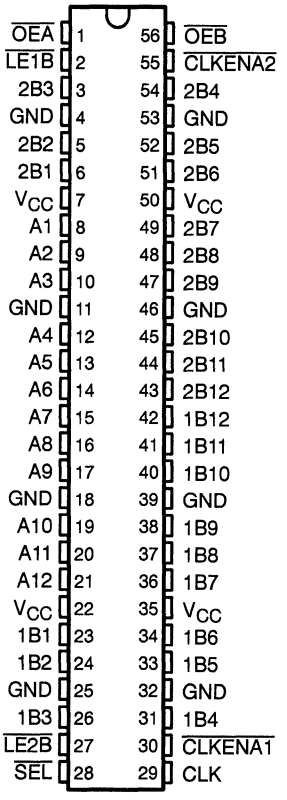
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Inputs	V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			−75		
I_{OZ}		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	μA
C_i		V_I = V_{CC} or GND		3.3 V			pF
C_{io}		V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16271 is a 12-bit to 24-bit bus exchanger, which is intended for applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. It is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the $\overline{\text{CLKENA}}$ inputs are low. Proper control of these inputs allow two sequential 12-bit words to be presented as a 24-bit word on the B port.

Transparent latches in the B to A path allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{\text{LE}}$) inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

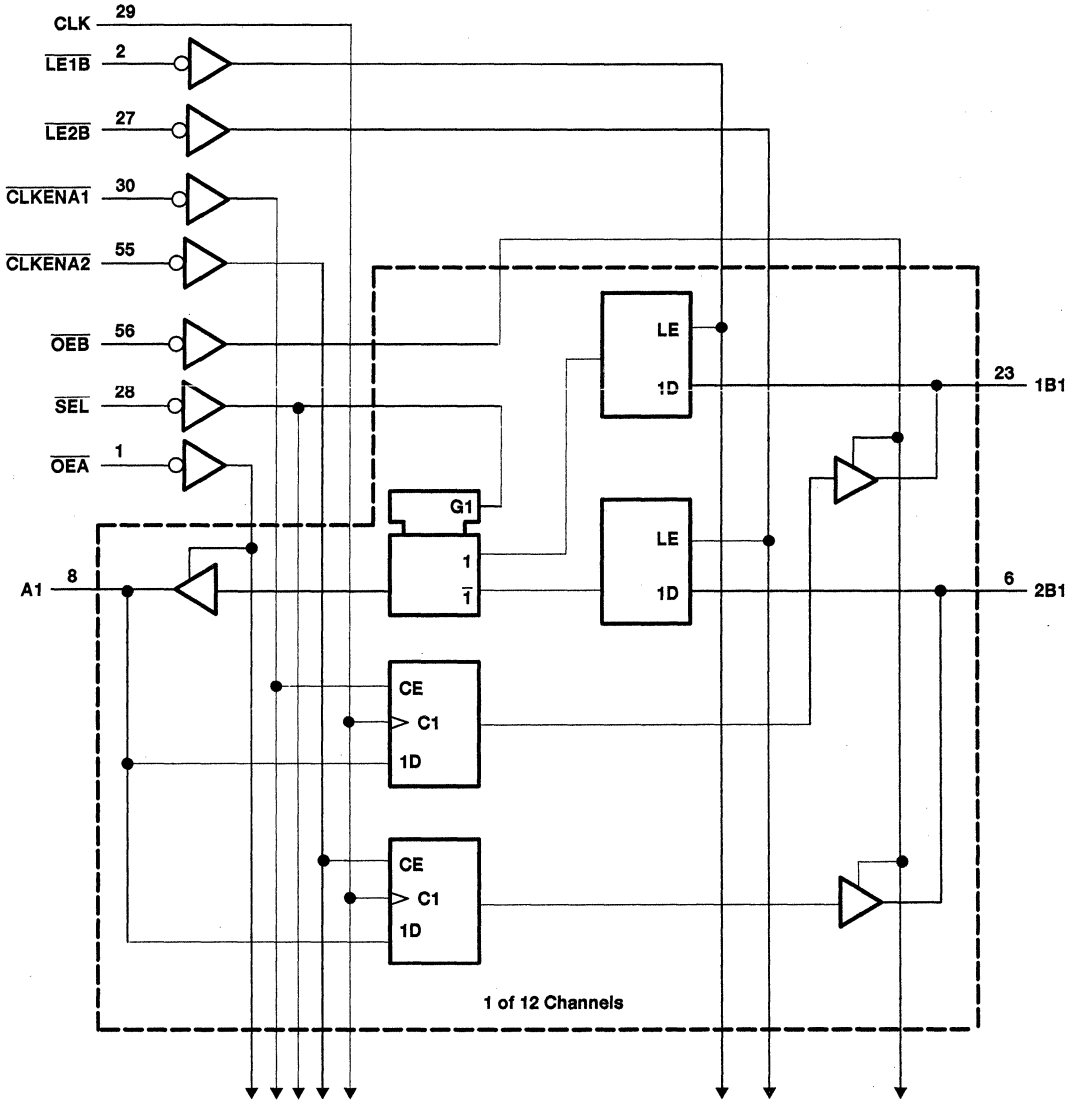
The SN74ALVC16271 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16271 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



Function Tables

OUTPUT-ENABLE TABLE

INPUTS		OUTPUTS	
$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	A_0	H

B-TO-A STORAGE TABLE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
$\overline{LE}$	$\overline{SEL}$	1B	2B	A
H	X	X	X	A_0†
H	X	X	X	A_0†
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Inputs	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		µA
		V_I = 2 V			−75		
I_{OZ}		$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	µA
C_i		$V_I = V_{CC}$ or GND		3.3 V			pF
C_{io}		$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
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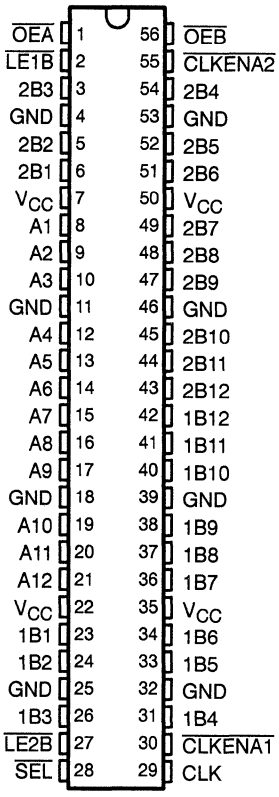
- **Typical V_{OHV} (Output V_{CC} Overshoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16272 is a 12-bit to 24-bit bus exchanger, which is intended for applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. It is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors. It is designed specifically for low-voltage (3.3 V) V_{CC} operation.

Data from the A inputs is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the $\overline{\text{CLKENA}}$ inputs are low. A two-stage pipeline is provided in each of the A to 1B and A to 2B paths to serve as a shallow write buffer.

Transparent latches are provided in the B to A path to allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{\text{LE}}$) inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16272 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16272 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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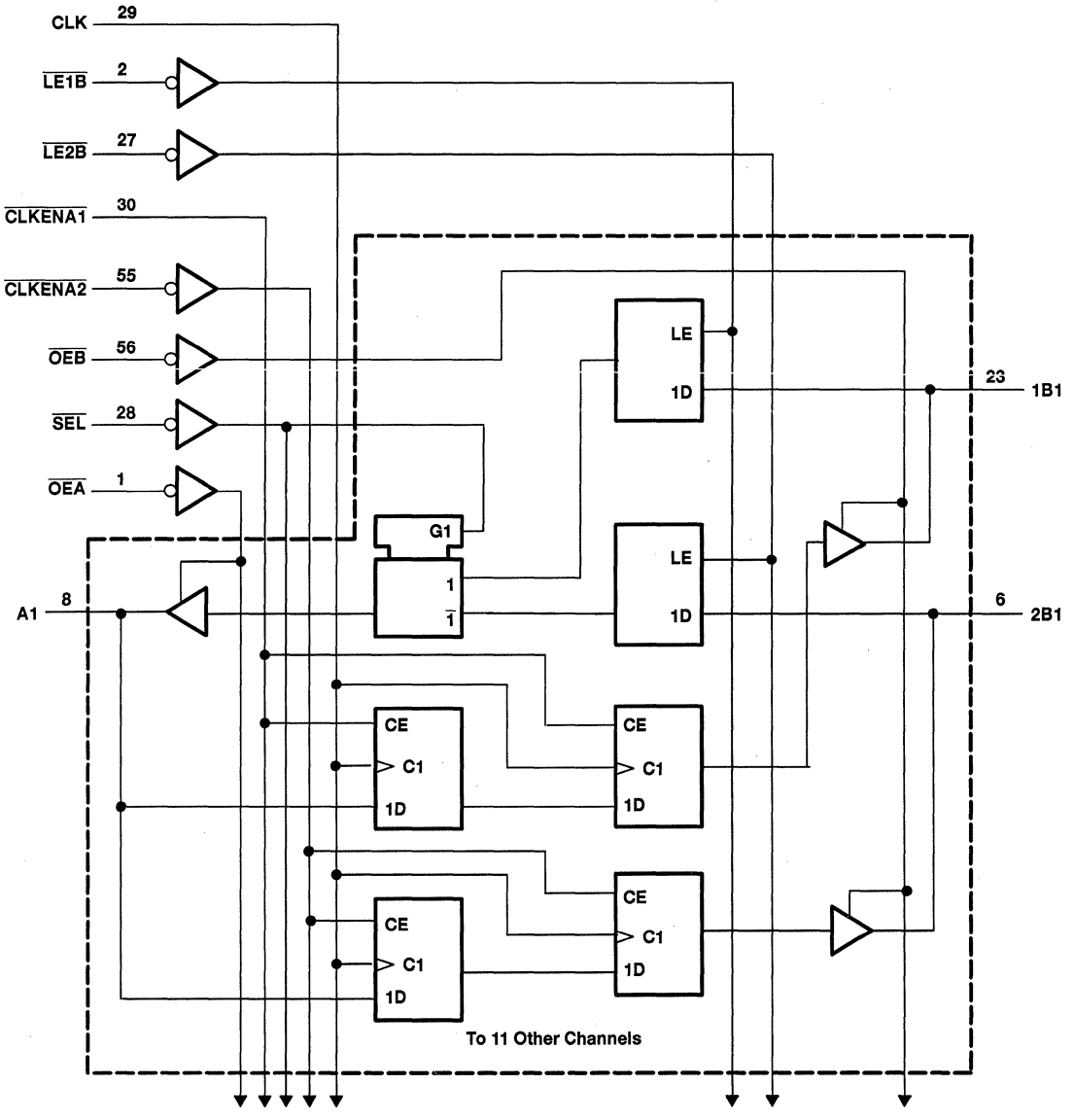
logic diagram (positive logic)



Function Tables

OUTPUT-ENABLE TABLE

INPUTS		OUTPUTS	
$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE TABLE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L[1]	X
L	X	↑	H	H[1]	X
X	L	↑	L	X	L
X	L	↑	H	A_0	H

[1] Two CLK edges are needed to propagate data.

B-TO-A STORAGE TABLE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
$\overline{LE}$	$\overline{SEL}$	1B	2B	A
H	X	X	X	A_0‡
H	X	X	X	A_0‡
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

† Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The input and output positive voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

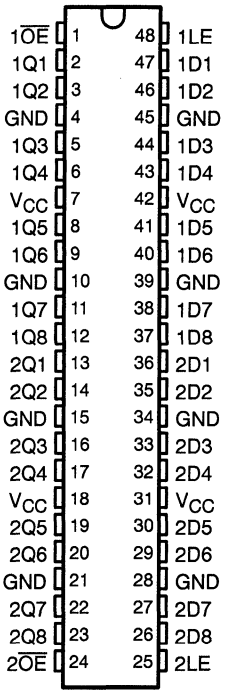
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I	Inputs	$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data pins	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		−75		
I_{OZ}		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			750	μA
C_i		$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}		$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16373 is characterized for operation from –40°C to 85°C.

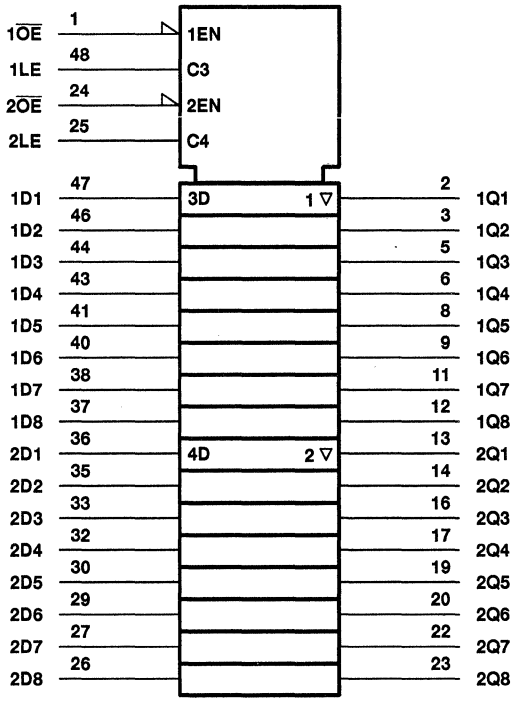
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 8-bit section)

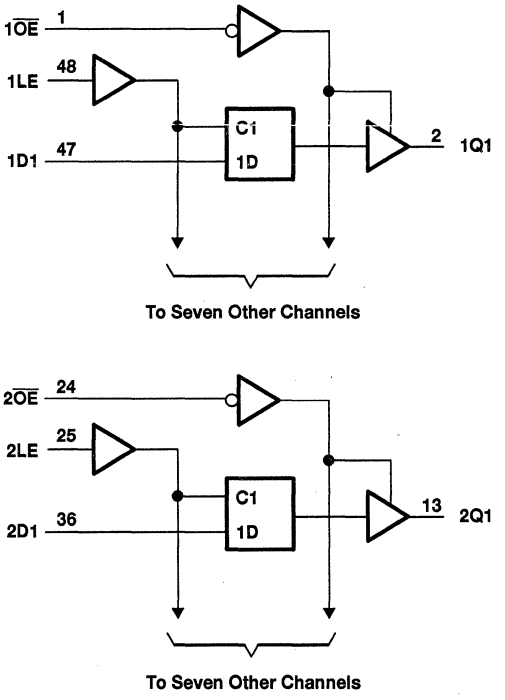
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		µA
	V_I = 2 V			–75		
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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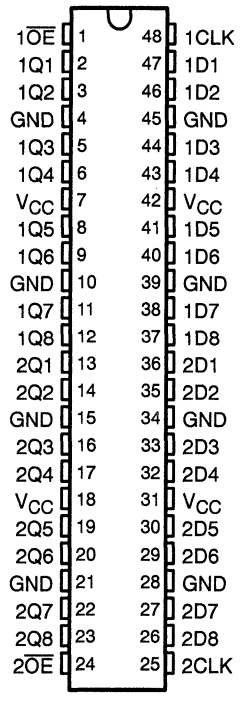
DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16374 is characterized for operation from –40°C to 85°C.

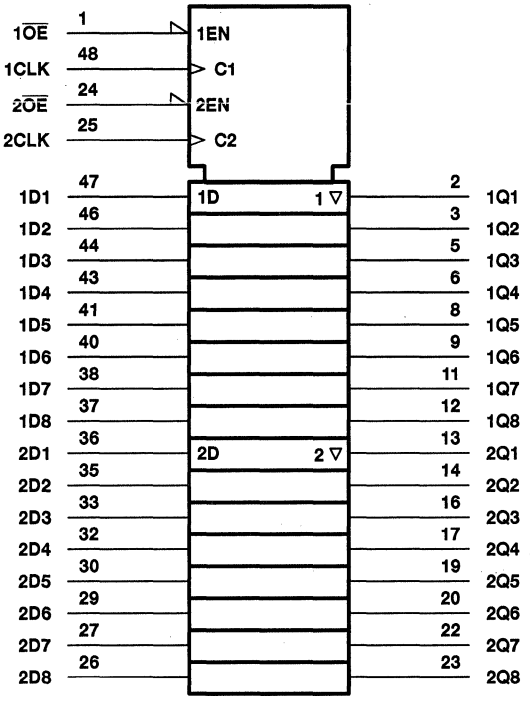
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

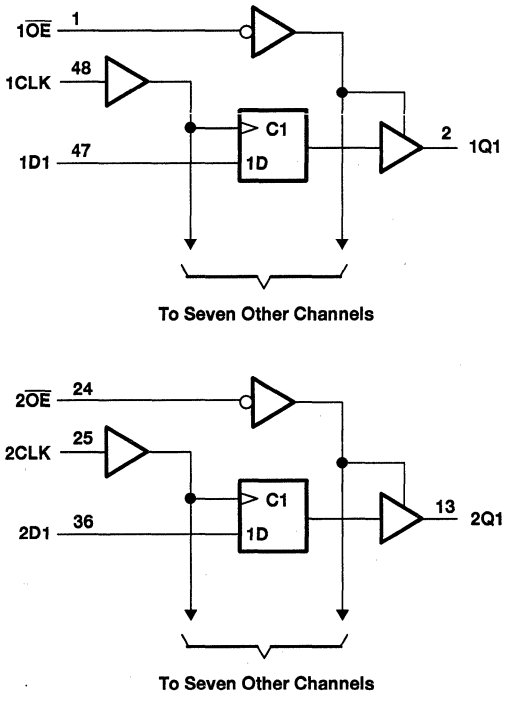
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

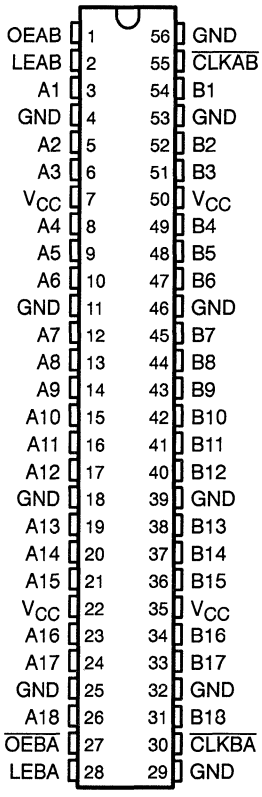
PARAMETER	TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA	2.7 V	2.2		
		3 V	2.4		
	I_{OH} = –24 mA	3 V	2		
V_{OL}	I_{OL} = 100 µA	MIN to MAX		0.2	V
	I_{OL} = 12 mA	2.7 V		0.4	
	I_{OL} = 24 mA	3 V		0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V		±5	µA
$I_{I(hold)}$	V_I = 0.8 V	3 V	75		µA
	V_I = 2 V		–75		
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V			pF
C_o	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active high, and $\overline{OEBA}$ is active low).

The SN74ALVC16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16500 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	$\overline{\text{CLKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

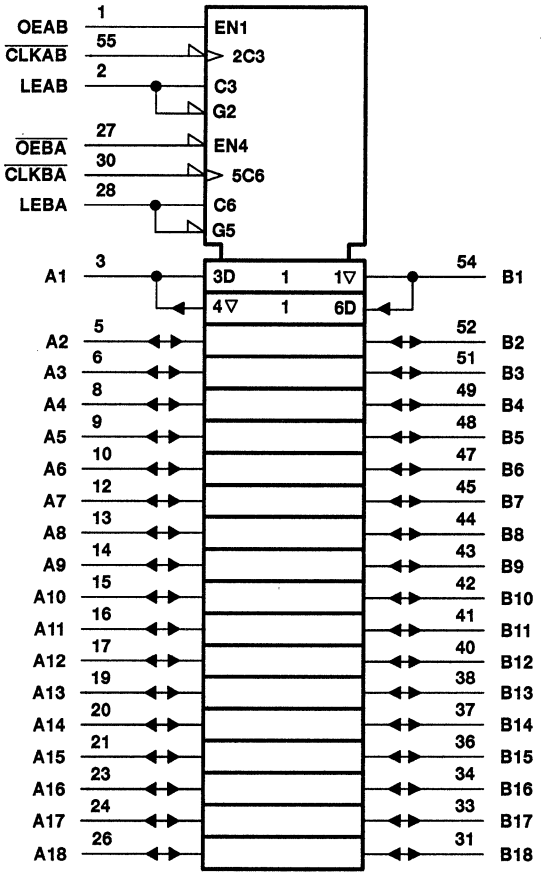
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

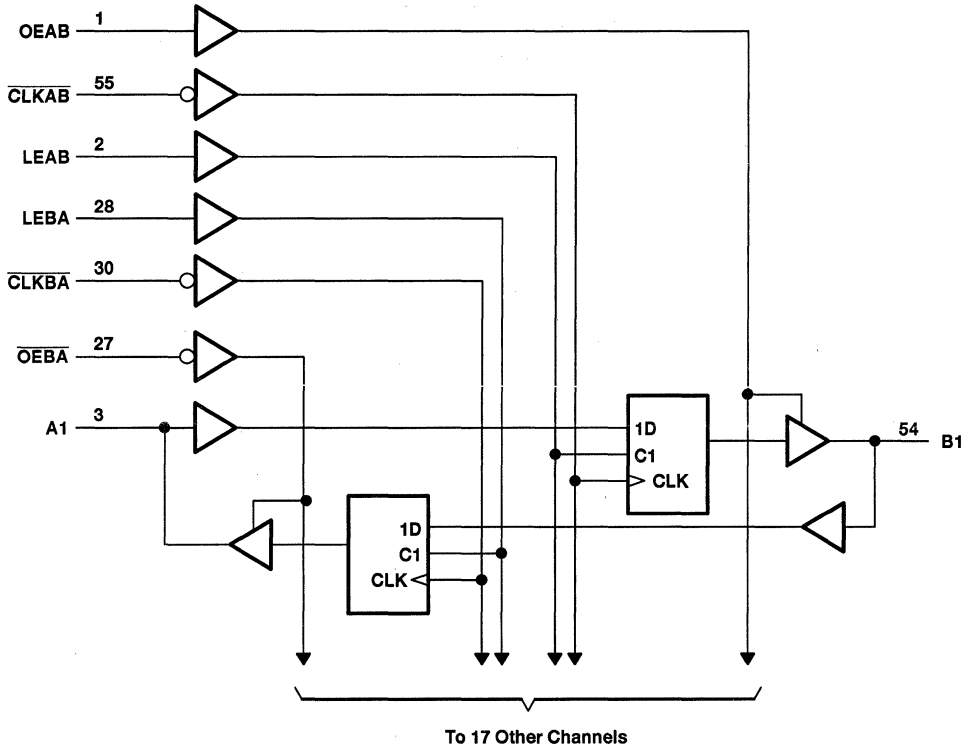
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

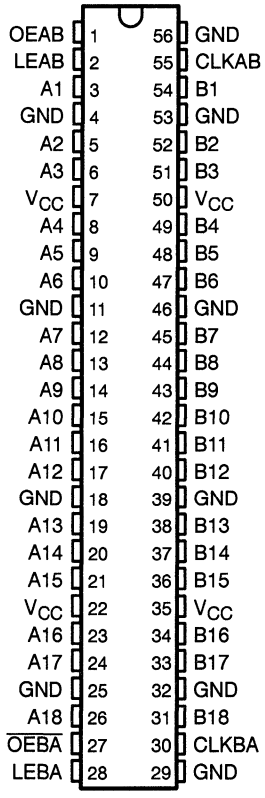
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			−75		
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and $\overline{\text{OEBA}}$ is active low).

The SN74ALVC16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16501 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

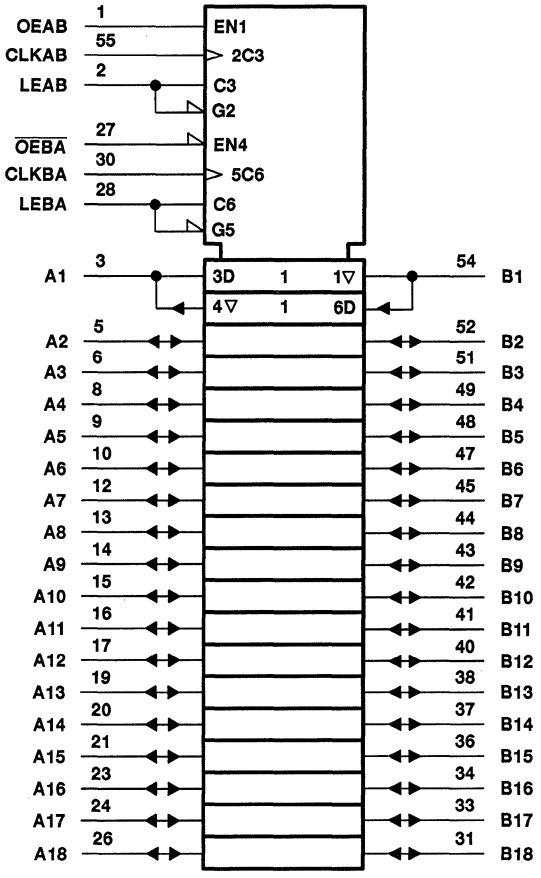
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

PRODUCT PREVIEW

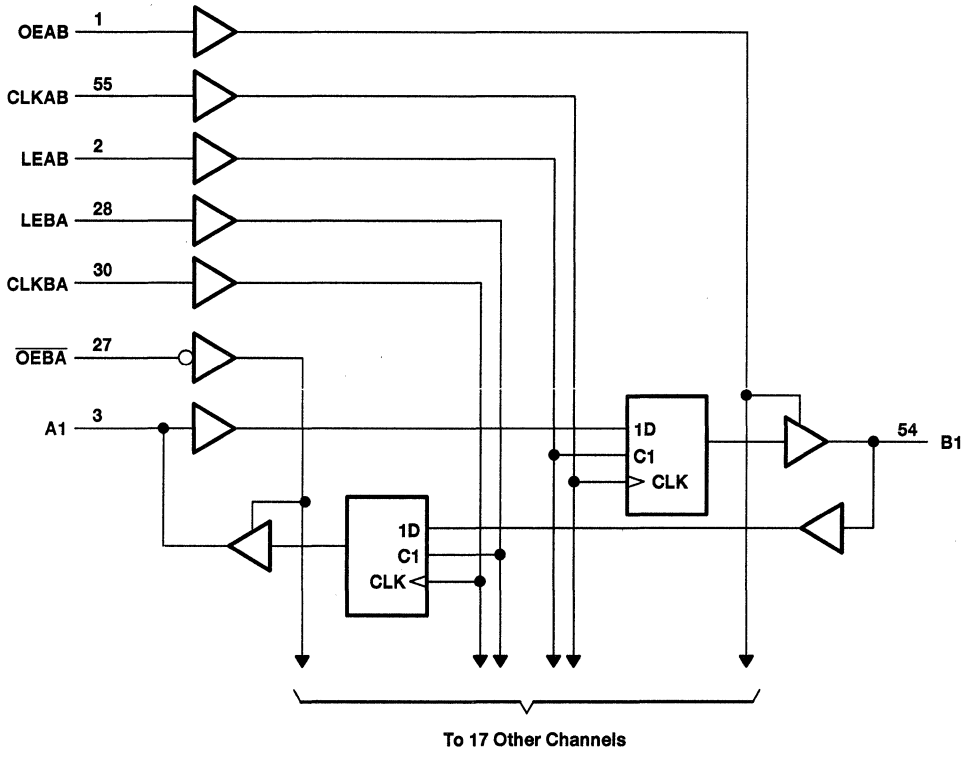
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		V_I = V_{CC} or GND		3.6 V		±5	μA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
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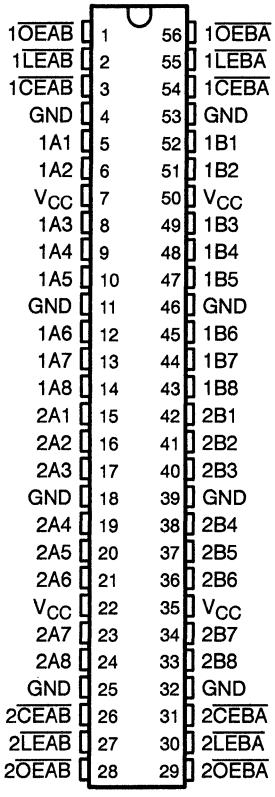
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

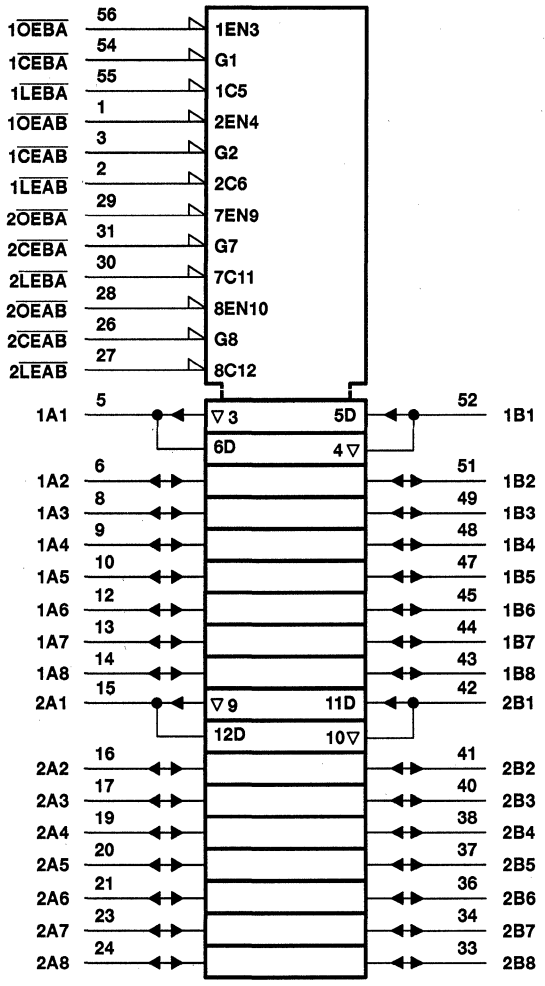
The SN74ALVC16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16543 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

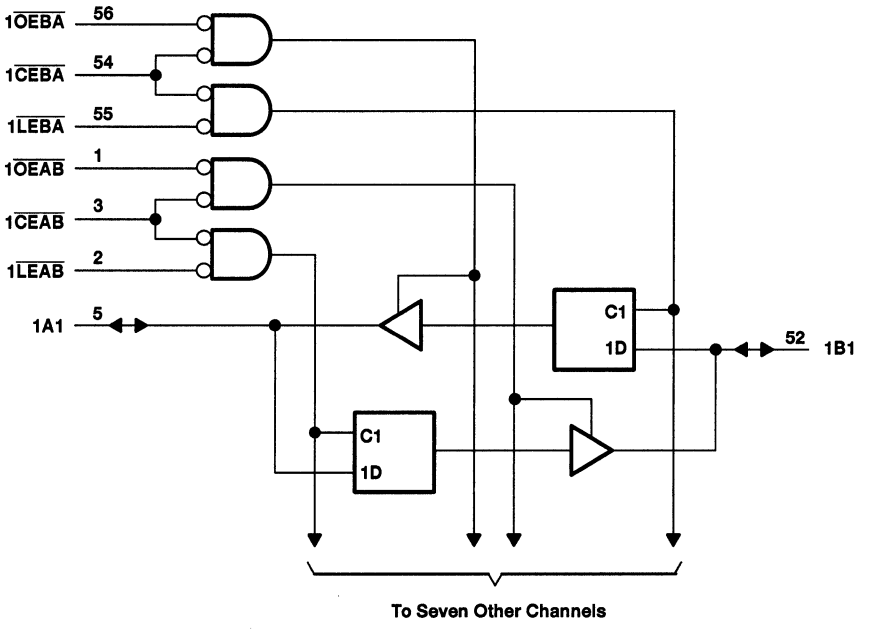
logic symbol†

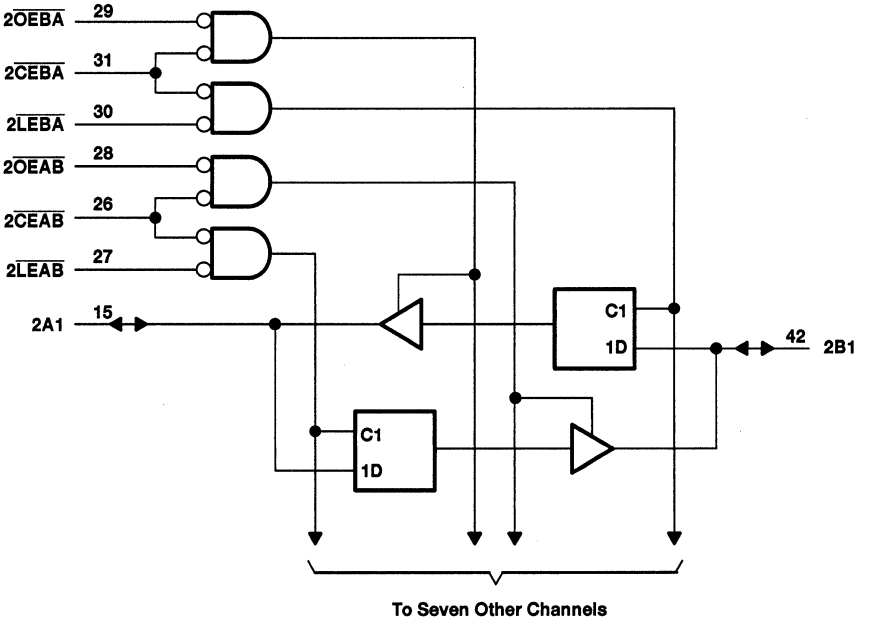


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)





PRODUCT PREVIEW

FUNCTION TABLE† (each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

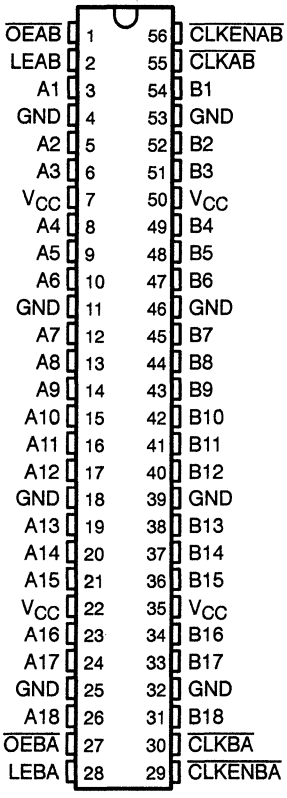
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		V_I = V_{CC} or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		−75		
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			750	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CLKENBA}$.

The SN74ALVC16600 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16600 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

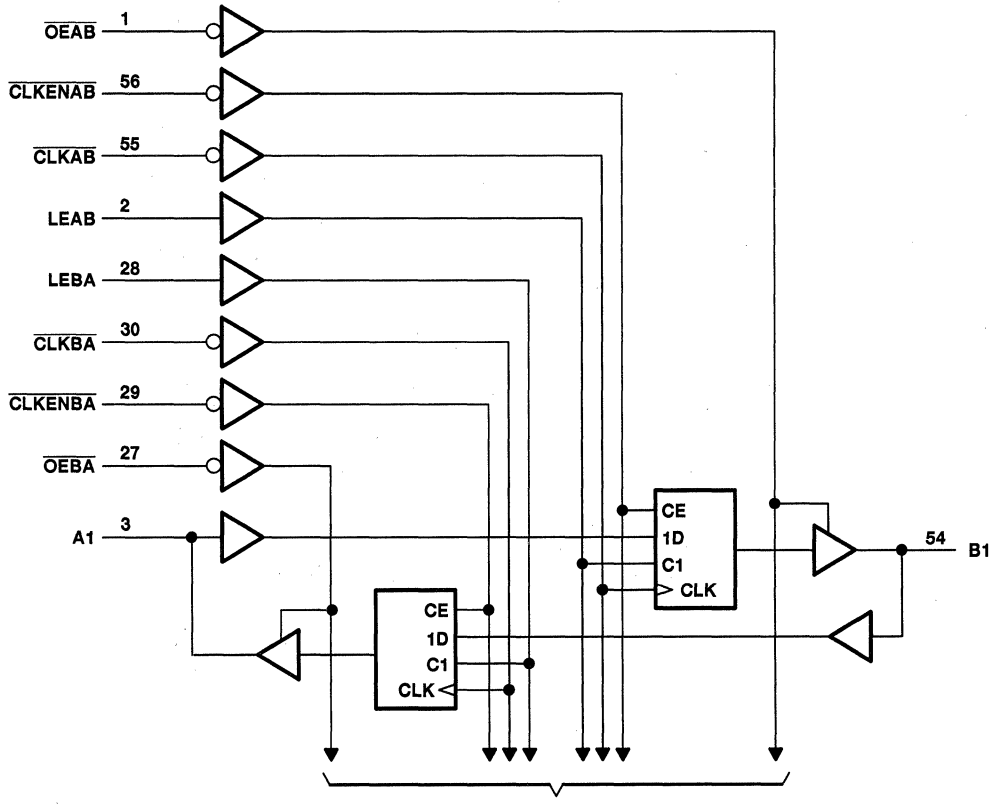
FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	$\overline{CLKAB}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B_0‡
L	L	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CLKENBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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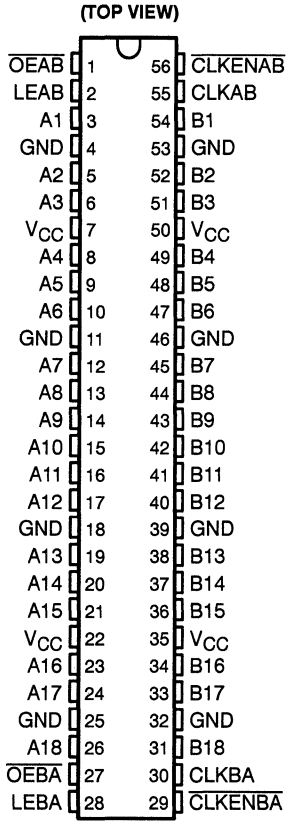
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

The SN74ALVC16601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16601 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

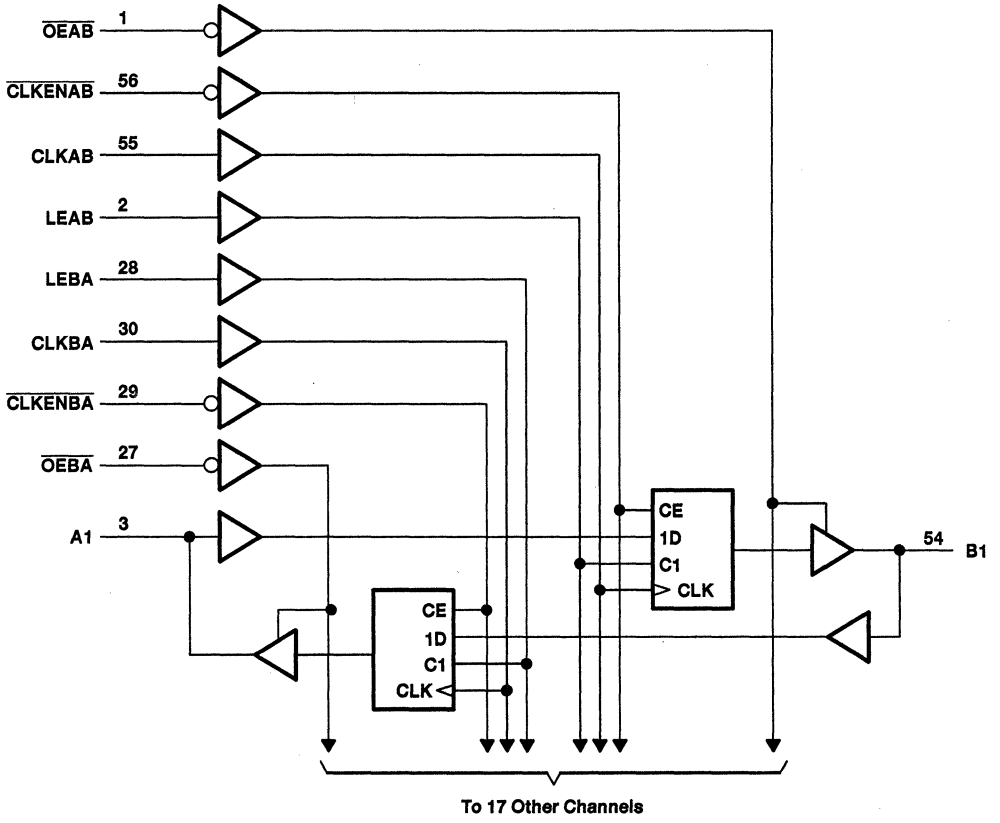
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

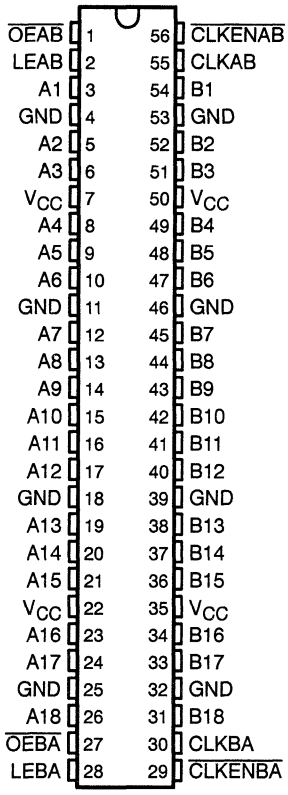
PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = −24 mA		3 V	2		
V_{OL}		I_{OL} = 100 μA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I		$V_I = V_{CC}$ or GND		3.6 V		±5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V		3 V	75		μA
		V_I = 2 V			−75		
I_{OZ}‡		$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,			750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on All I/O Pins**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

The B-port outputs, include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74ALVC162601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC162601 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

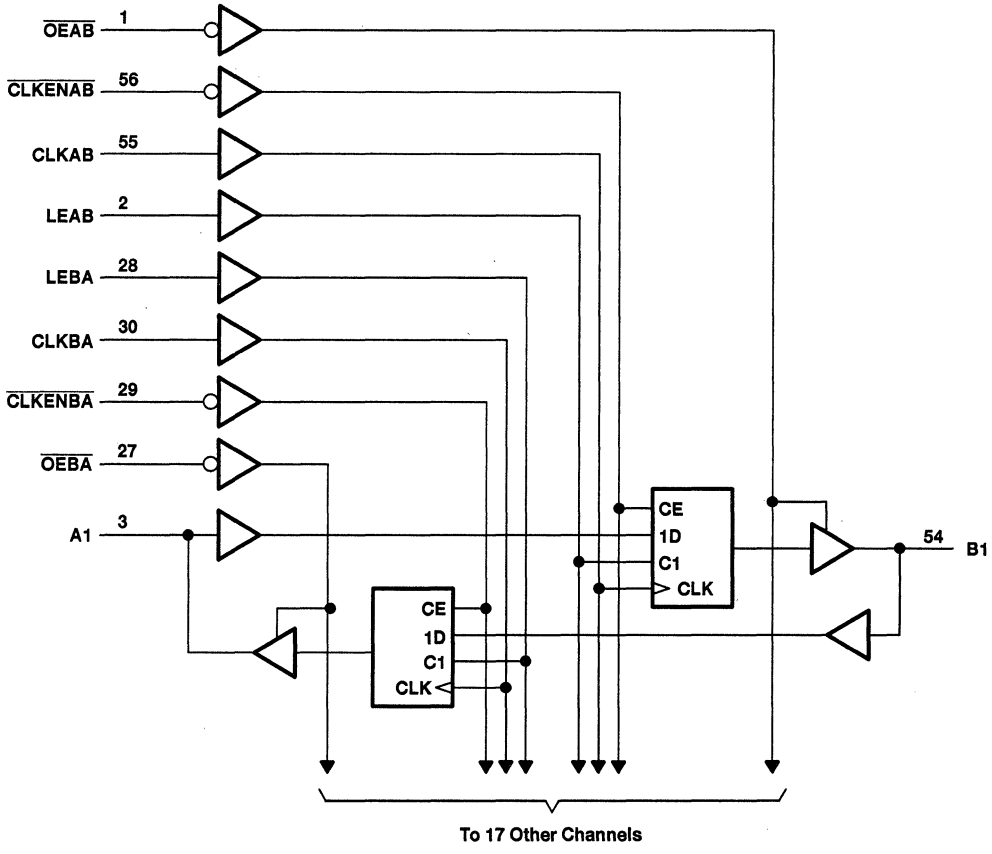
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V			mA
		V_{CC} = 3 V			
I_{OL}	Low-level output current	V_{CC} = 2.7 V			mA
		V_{CC} = 3 V			
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

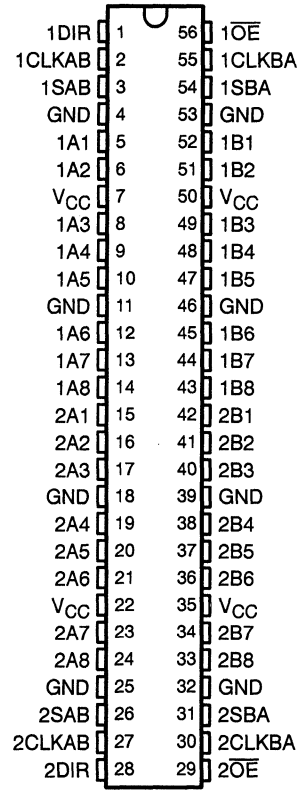
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = – 100 μA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = – 4 mA	2.7 V	2.4		
		I_{OH} = –6 mA	3 V	2.4		
		I_{OH} = TBD		2		
V_{OL}		I_{OL} =100 μA	MIN to MAX		0.2	V
		I_{OL} = 4 mA	2.7 V		0.4	
		I_{OL} = 6 mA	3 V		0.4	
		I_{OH} = TBD			0.8	
I_I		V_I = V_{CC} or GND	3.6 V		±5	μA
$I_{I(hold)}$		V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		–75		
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V		±10	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V			pF
C_{io}	A or B ports	V_O = V_{CC} or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVC16646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

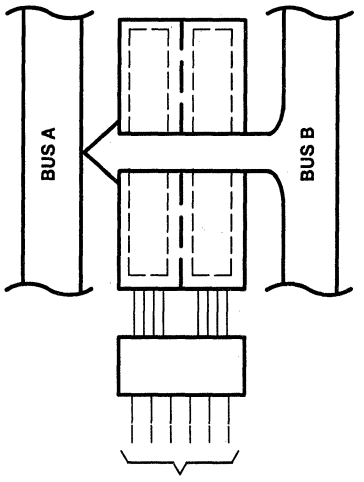
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN74ALVC16646 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16646 is characterized for operation from –40°C to 85°C.

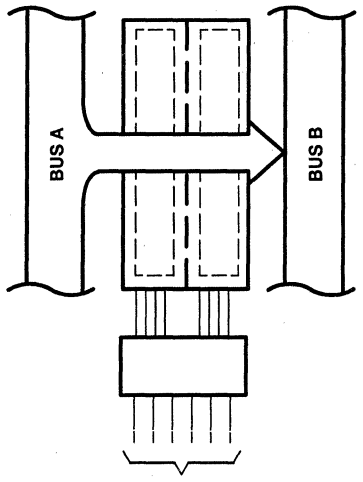
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



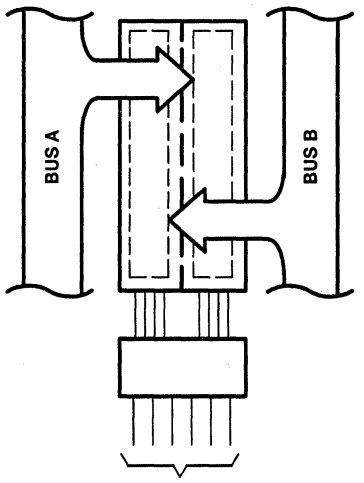
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



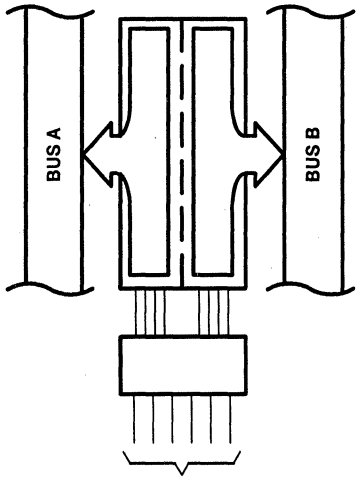
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

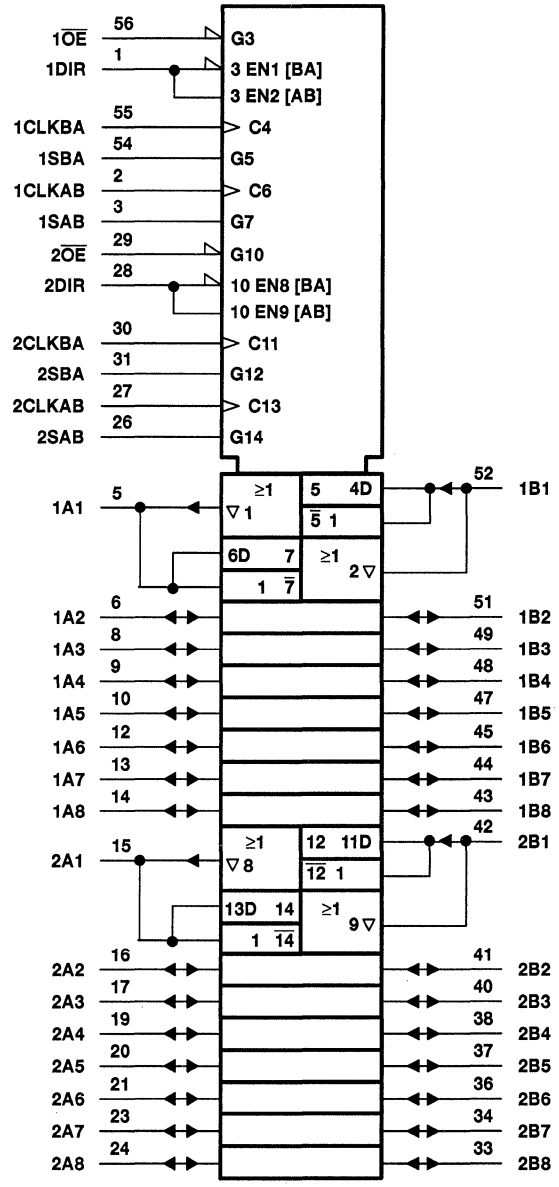


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

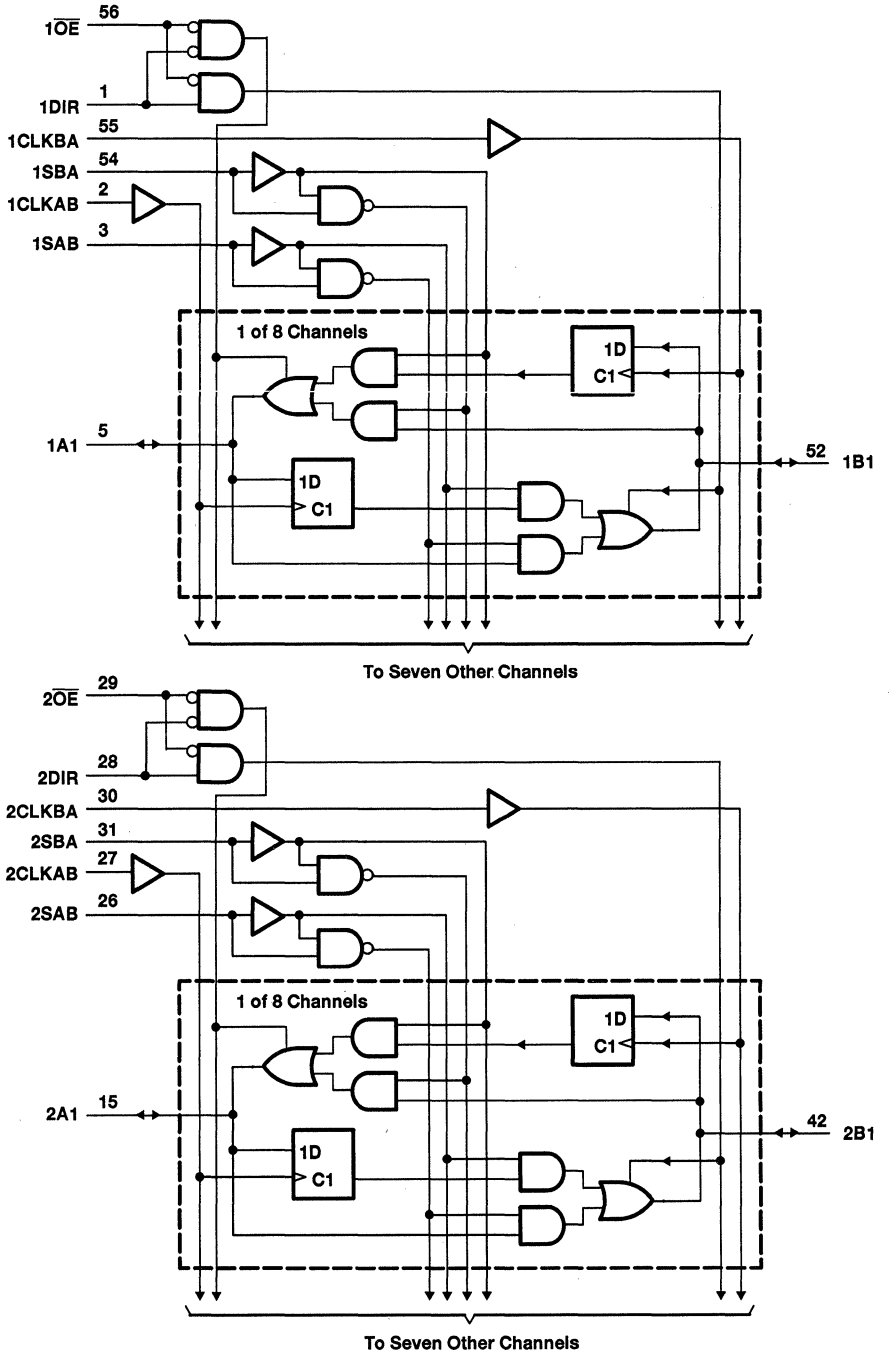
Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

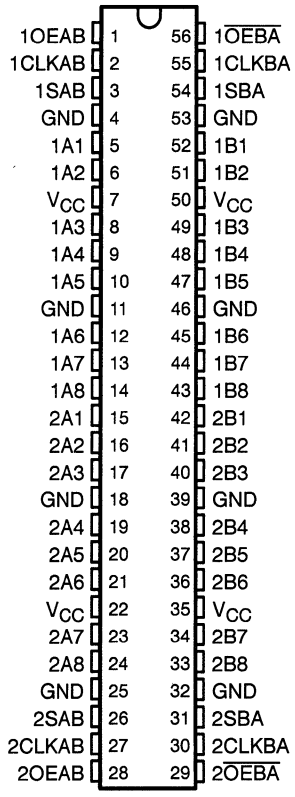
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 µA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V		±5	µA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		µA
		V_I = 2 V		–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVC16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

The SN74ALVC16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16652 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

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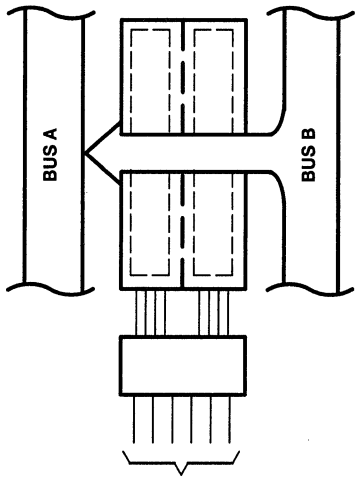
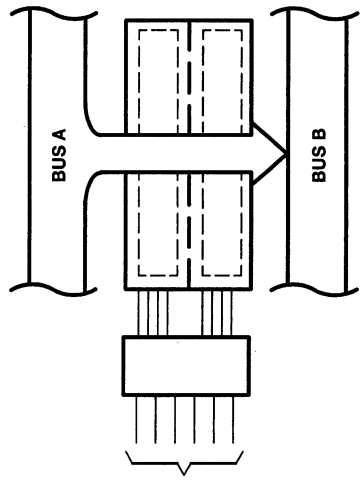


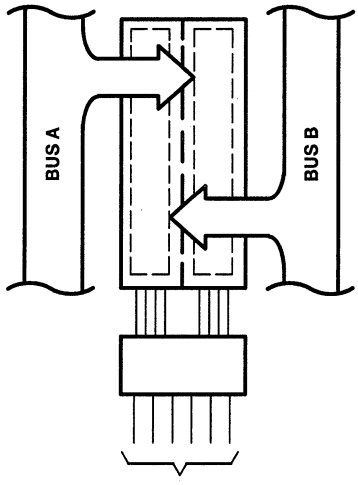
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



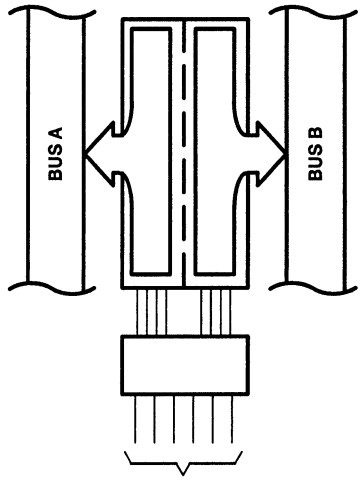
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

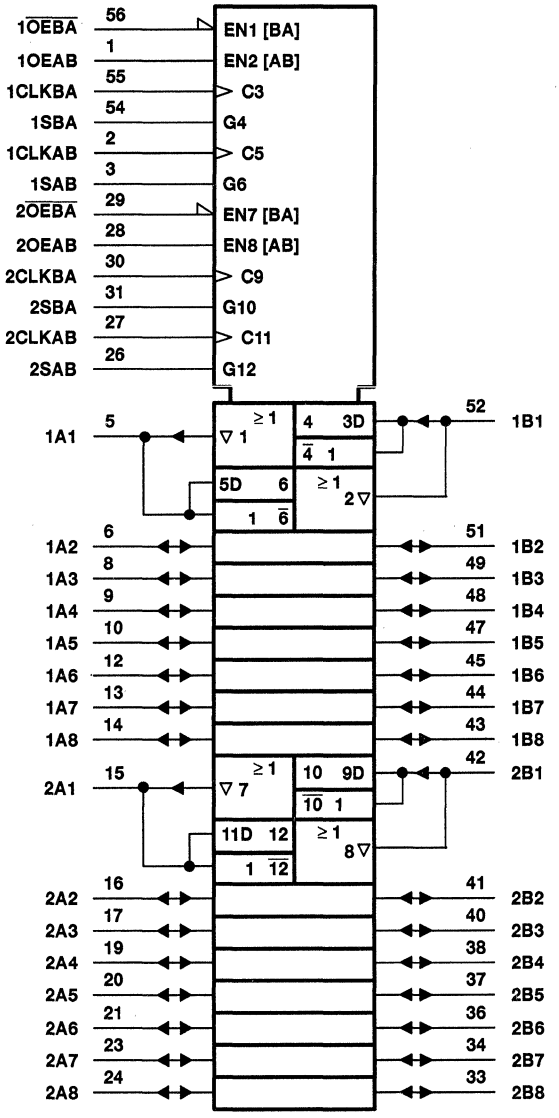


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

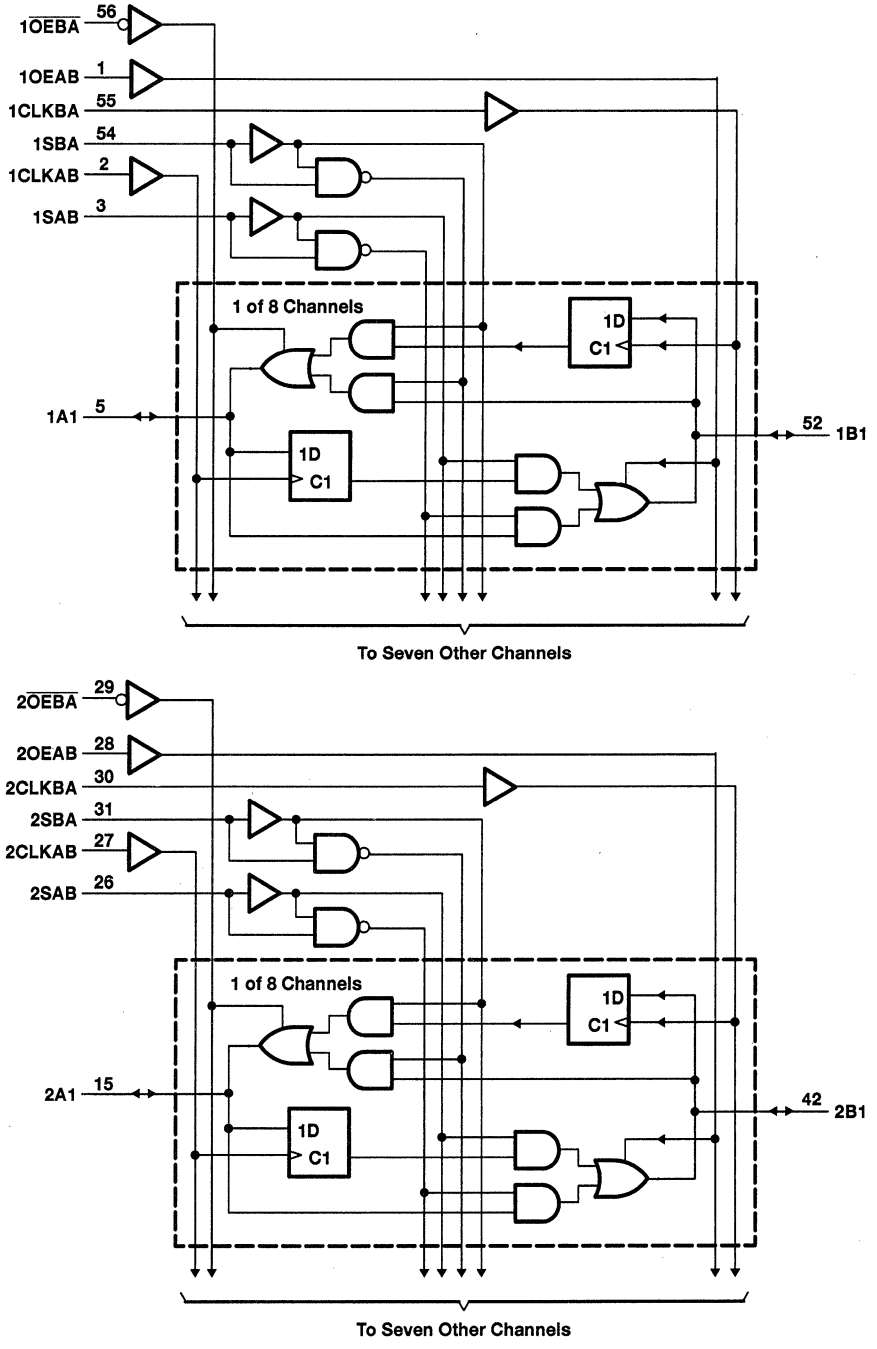
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

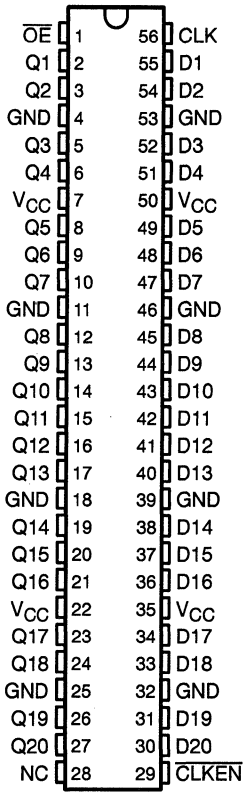
PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2		V
		I_{OH} = −12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = −24 mA	3 V	2		
V_{OL}		I_{OL} = 100 μA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V		±5	μA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		μA
		V_I = 2 V		−75		
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND			750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The SN74ALVC16721's twenty flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs, provided that the clock-enable ($\overline{CLKEN}$) input is low. If $\overline{CLKEN}$ is high, no data is stored.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16721 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16721 is characterized for operation from –40°C to 85°C.

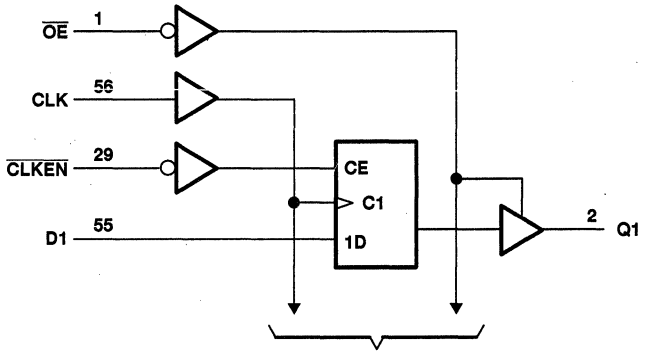
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	Q
L	H	X	H	Q_0
L	L	↑	H	H
L	L	↑	L	L
L	L	L	X	Q_0
H	X	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = −24 mA		3 V	2			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75			μA
	V_I = 2 V			−75			
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				750	μA
C_i	V_I = V_{CC} or GND		3.3 V		4		pF
C_o	V_O = V_{CC} or GND		3.3 V		6		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 3.3 V ± 0.15 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low									ns
t_{su}	Setup time	Data before CLK↑	High or low	3						ns
		$\overline{CLKEN}$ before CLK↑	High or low	3						
t_h	Hold time	Data after CLK↑	High or low	0						ns
		$\overline{CLKEN}$ after CLK↑	High or low	0						

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

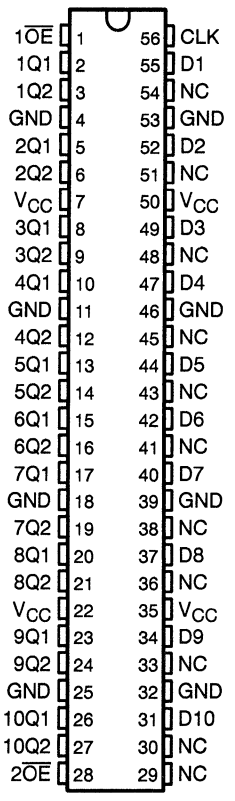
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{PLH}	CLK	Q		4		4.5			ns
t_{PHL}				4		4.5			
t_{PZH}	$\overline{OE}$	Q		5		5.7			ns
t_{PZL}				5		5.7			
t_{PHZ}	$\overline{OE}$	Q		4.5		4.5			ns
t_{PLZ}				4.5		4.5			

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 10-bit flip-flop is designed specifically for low-voltage 3.3-V V_{CC} operation.

The flip-flops of the SN74ALVC16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16820 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

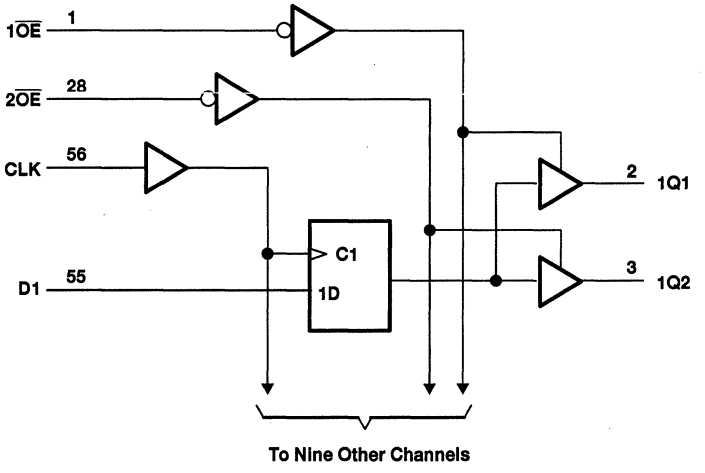
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}_n$†	CLK	D	Q_n†
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

† n = 1, 2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = −24 mA		3 V	2			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75			μA
	V_I = 2 V			−75			
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				750	μA
C_i	V_I = V_{CC} or GND		3.3 V		4		pF
C_o	V_O = V_{CC} or GND		3.3 V		6		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.15 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low								ns
t_{su}	Setup time, data before CLK↑	High or low	0.8		1				ns
t_h	Hold time, data after CLK↑	High or low	2		2				ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

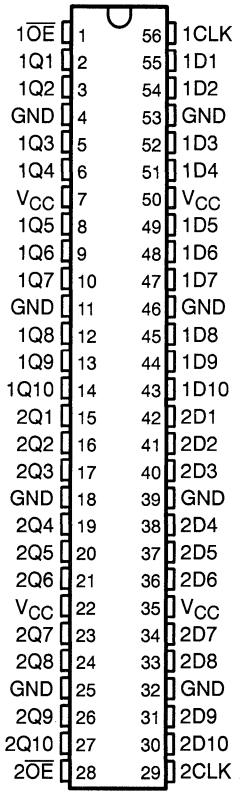
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{PLH}	CLK	Q		4		4.5			ns
t_{PHL}				4		4.5			
t_{PZH}	$\overline{OE}$	Q		5		5.7			ns
t_{PZL}				5		5.7			
t_{PHZ}	$\overline{OE}$	Q		4.5		4.5			ns
t_{PLZ}				4.5		4.5			

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit bus-interface flip-flop is designed specifically for low-voltage (3.3 V) V_{CC} operation.

The SN74ALVC16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The twenty flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16821 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16821 is characterized for operation from –40°C to 85°C.

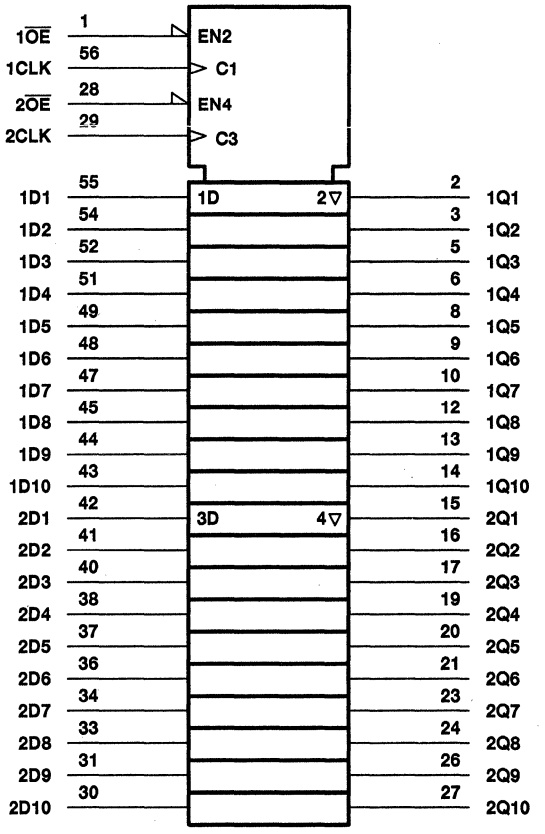
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 10-bit flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

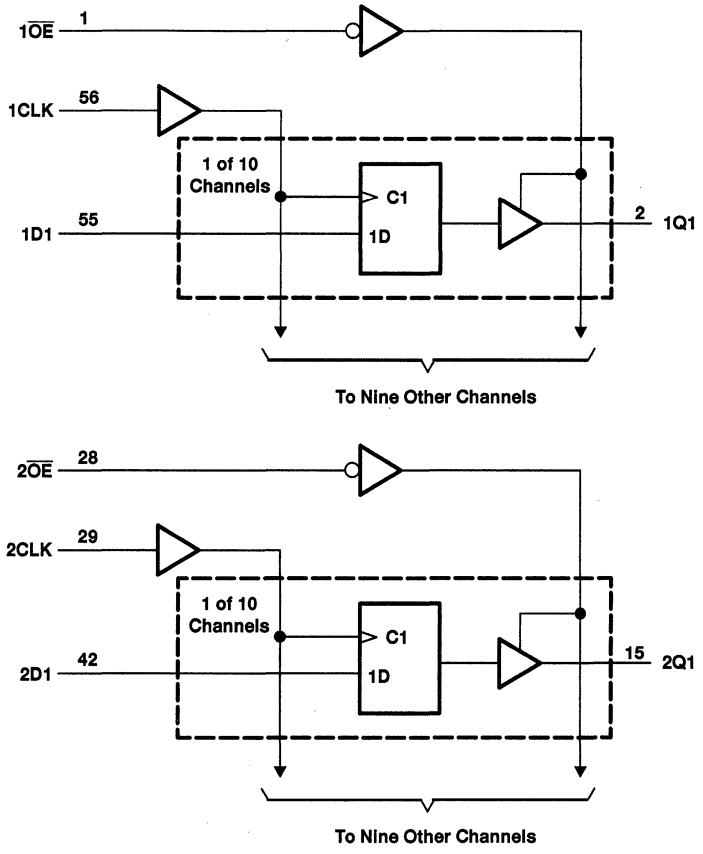
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = –12 mA		2.7 V	2.2			
			3 V	2.4			
	I_{OH} = –24 mA		3 V	2			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		2.7 V			0.4	
	I_{OL} = 24 mA		3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75			µA
	V_I = 2 V			–75			
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				750	µA
C_i	V_I = V_{CC} or GND		3.3 V		4		pF
C_o	V_O = V_{CC} or GND		3.3 V		6		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.15 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low								ns
t_{su}	Setup time, data before CLK↑	High or low	3						ns
t_h	Hold time, data after CLK↑	High or low	0						ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{PLH}	CLK	Q		4		4.5			ns
t_{PHL}				4		4.5			
t_{PZH}	$\overline{OE}$	Q		5		5.7			ns
t_{PZL}				5		5.7			
t_{PHZ}	$\overline{OE}$	Q		4.5		4.5			ns
t_{PLZ}				4.5		4.5			

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
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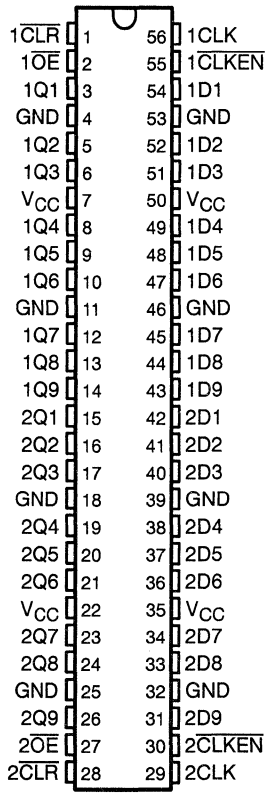
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVC16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16823 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16823 is characterized for operation from –40°C to 85°C.

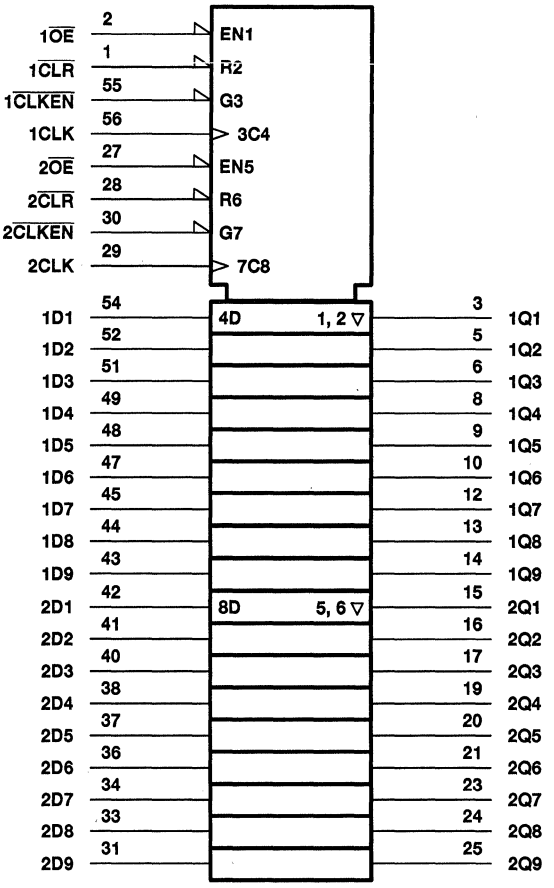
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 9-bit flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

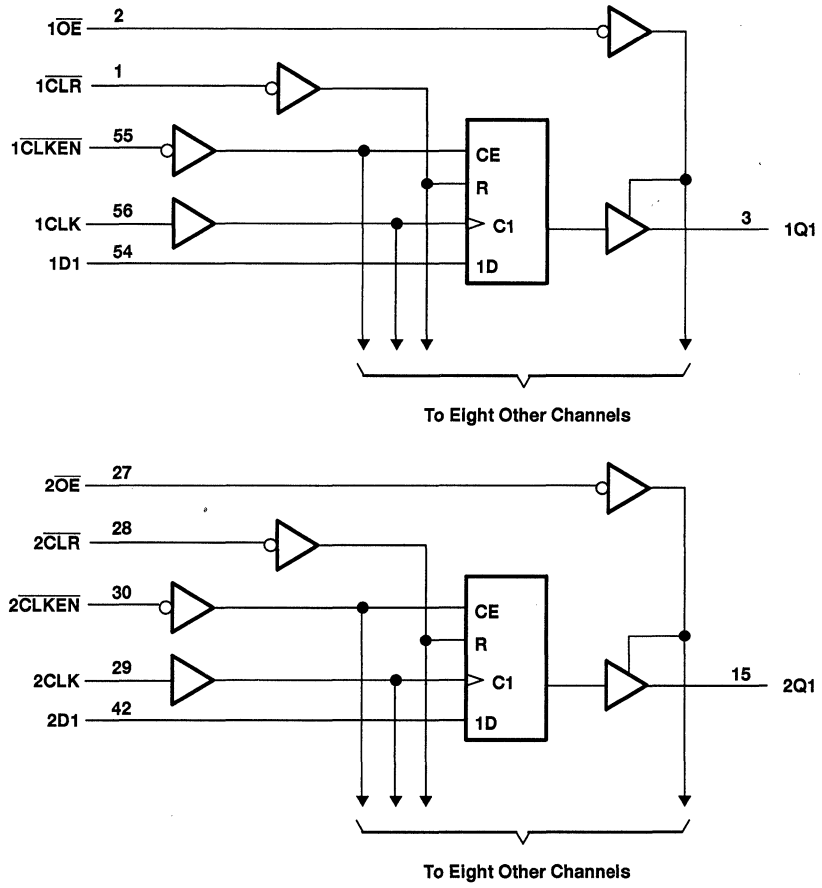
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	μA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		μA
	V_I = 2 V			–75		
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	μA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

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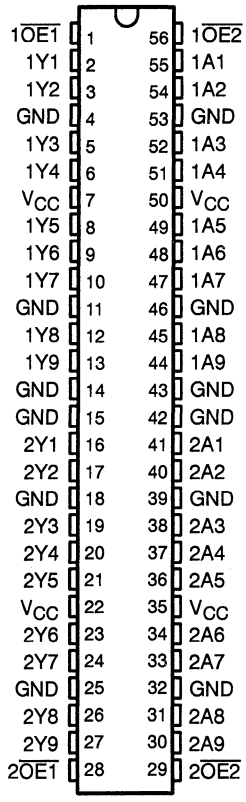
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVC16825 is an 18-bit buffer and line driver designed for 2.7-V to 3.6-V V_{CC} operation. It will improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16825 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16825 is characterized for operation from –40°C to 85°C.

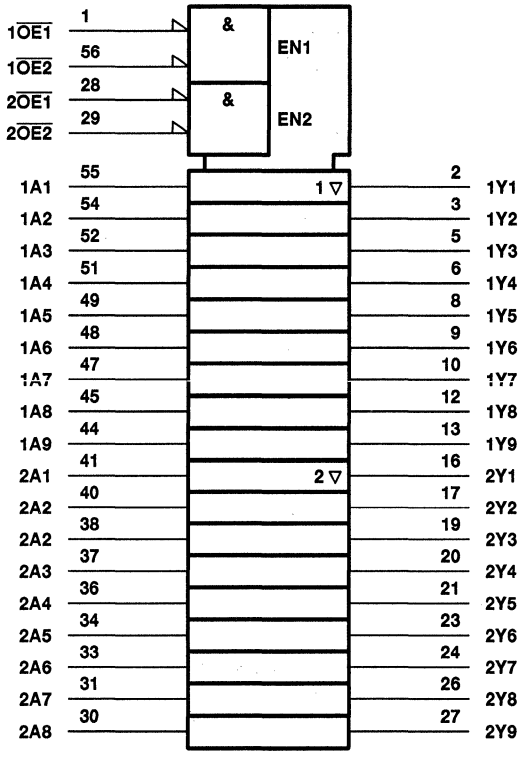
FUNCTION TABLE
(each 9-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

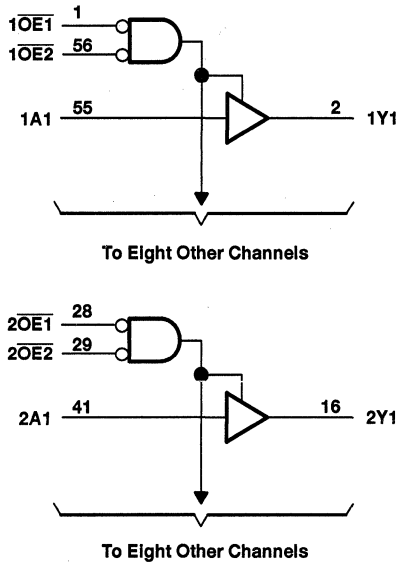
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		–12	mA
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	5	ns/V
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA		2.7 V	2.2		
				3 V	2.4		
		I_{OH} = –24 mA		3 V	2		
V_{OL}		I_{OL} = 100 µA		MIN to MAX		0.2	V
		I_{OL} = 12 mA		2.7 V		0.4	
		I_{OL} = 24 mA		3 V		0.55	
I_I	Control pins	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	Data pins	V_I = 0.8 V		3 V	75		µA
		V_I = 2 V			–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	µA
C_i		$V_I = V_{CC}$ or GND		3.3 V			pF
C_o		$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

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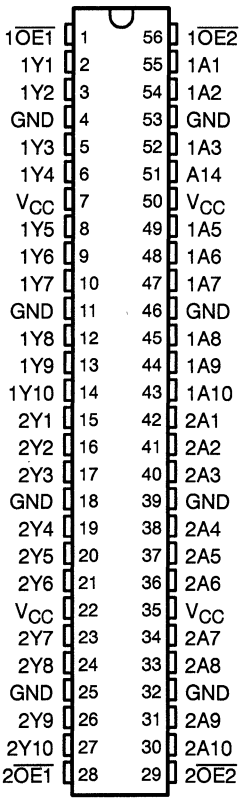
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit noninverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC16827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16827 is characterized for operation from –40°C to 85°C.

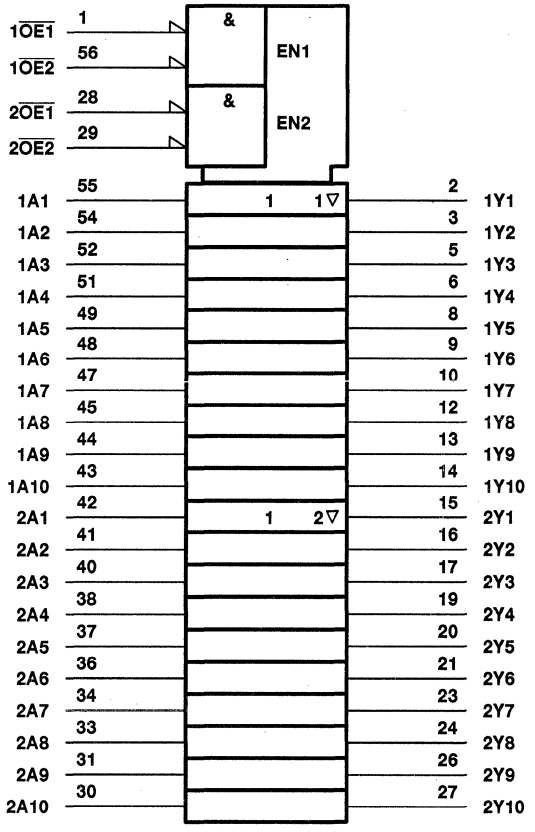
FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

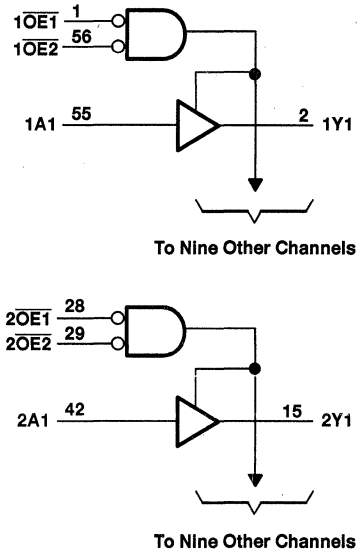
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

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NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	V_I = V_{CC} or GND		3.6 V		±5	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		µA
	V_I = 2 V			–75		
I_{OZ}	V_O = V_{CC} or GND		3.6 V		±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	µA
C_i	V_I = V_{CC} or GND		3.3 V			pF
C_o	V_O = V_{CC} or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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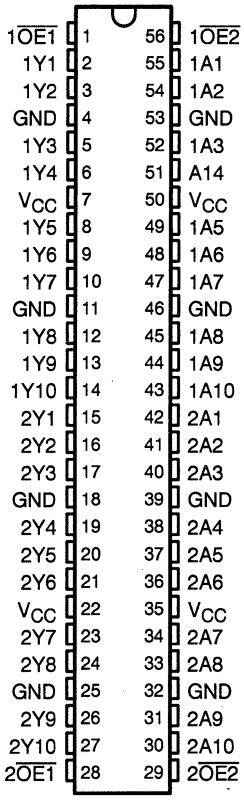
DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit inverting buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16828 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The SN74ALVC16828 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16828 is characterized for operation from –40°C to 85°C.

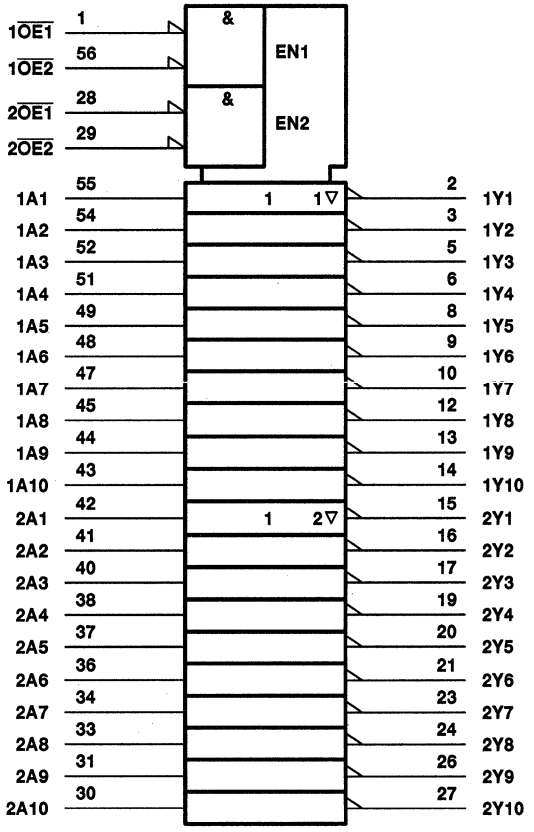
FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

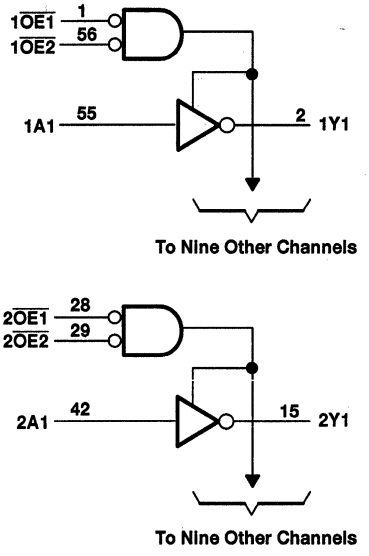
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

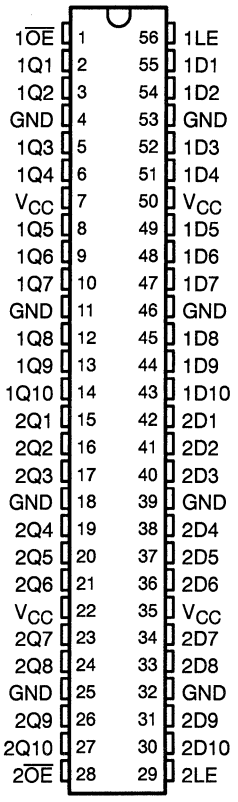
PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		µA
	V_I = 2 V			–75		
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVC16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74ALVC16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16841 is characterized for operation from –40°C to 85°C.

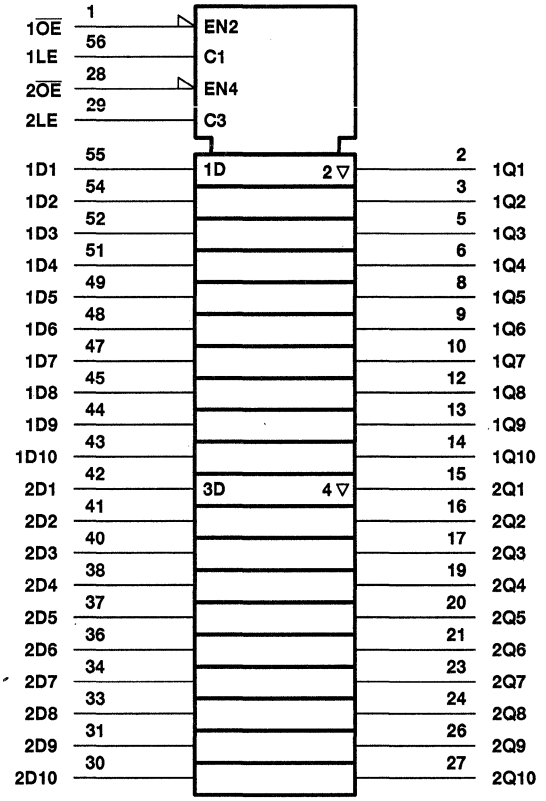
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 10-bit latch)

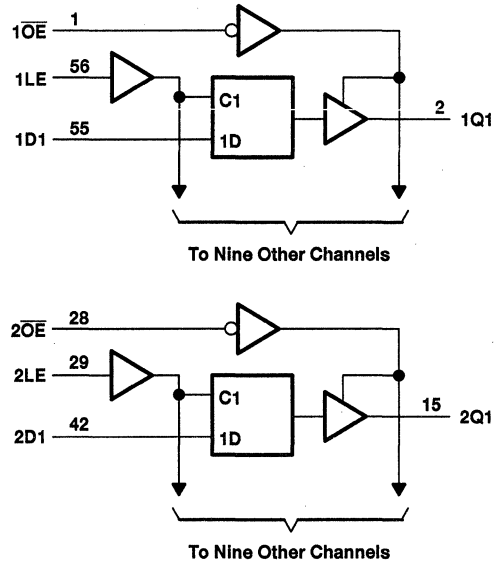
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 µA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	µA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		µA
	V_I = 2 V			–75		
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
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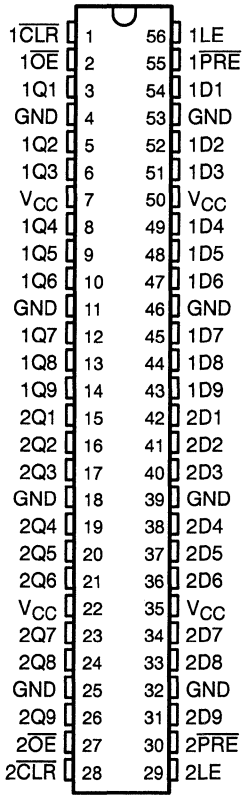
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVC16843 can be used as two 9-bit latches or one 18-bit latch. The eighteen latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

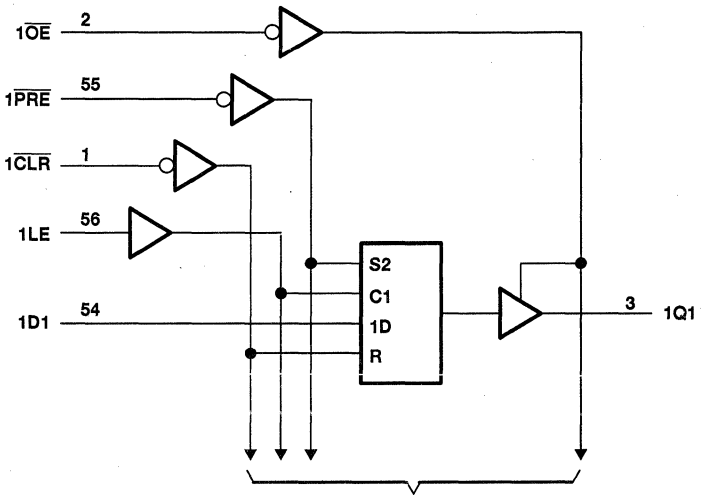
The SN74ALVC16843 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

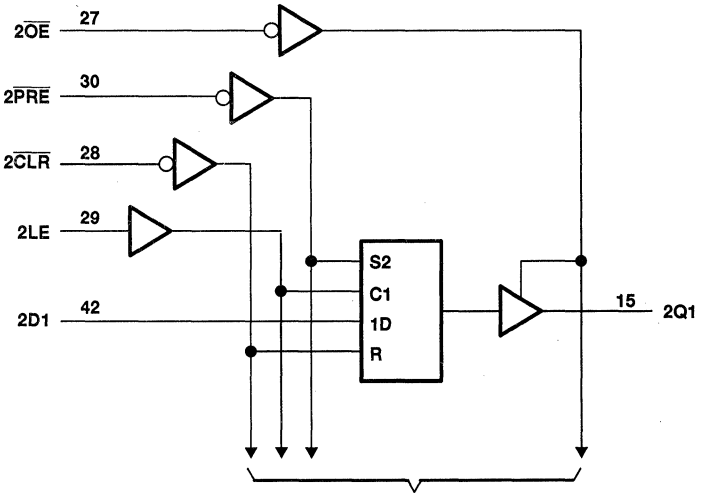
The SN74ALVC16843 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)





PRODUCT PREVIEW

FUNCTION TABLE
(each 9-bit latch)

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2		V
	I_{OH} = –12 mA		2.7 V	2.2		
			3 V	2.4		
	I_{OH} = –24 mA		3 V	2		
V_{OL}	I_{OL} = 100 μA		MIN to MAX		0.2	V
	I_{OL} = 12 mA		2.7 V		0.4	
	I_{OL} = 24 mA		3 V		0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V		±5	μA
$I_{I(hold)}$	V_I = 0.8 V		3 V	75		μA
	V_I = 2 V			–75		
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V		±10	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V		40	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,			750	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V			pF
C_o	$V_O = V_{CC}$ or GND		3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
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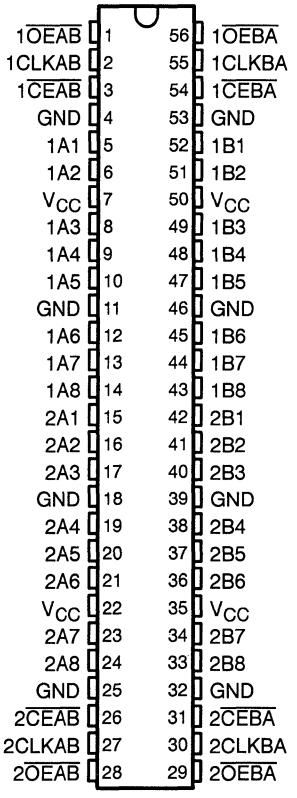
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CEAB}$ or $\overline{CEBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port.

The SN74ALVC16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16952 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B_0‡
X	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

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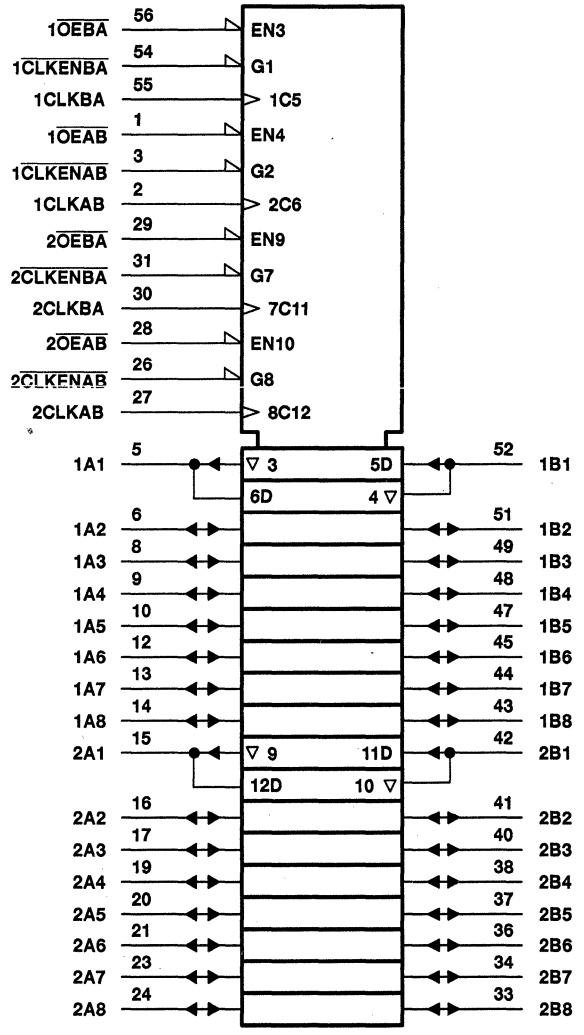
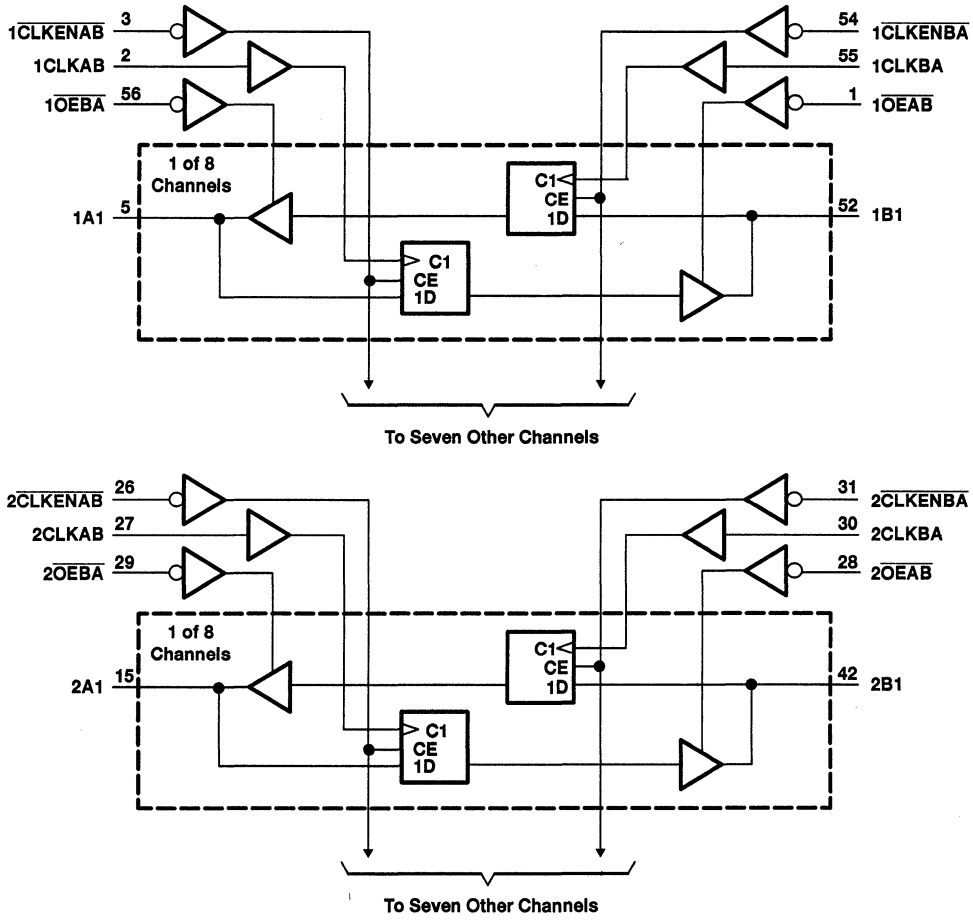
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

PRODUCT PREVIEW

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	MIN	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2		V
		I_{OH} = –12 mA	2.7 V	2.2		
			3 V	2.4		
		I_{OH} = –24 mA	3 V	2		
V_{OL}		I_{OL} = 100 µA	MIN to MAX		0.2	V
		I_{OL} = 12 mA	2.7 V		0.4	
		I_{OL} = 24 mA	3 V		0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V		±5	µA
$I_{I(hold)}$	Data I/Os	V_I = 0.8 V	3 V	75		µA
		V_I = 2 V		–75		
I_{OZ}‡		$V_O = V_{CC}$ or GND	3.6 V		±10	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V		40	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			750	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V			pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

LV MSI AND OCTALS

Features	Benefits
• 2-μ EPIC™ CMOS process	• Medium price/performance designs
• Low standby current (20 μA)	• Saves power, extends battery life
• –8-mA/8-mA drive current	• 5-V HCMOS upgrades
• 2.7-V to 3.6-V V_{CC} range	• Fully characterized for unregulated battery operation
• SOIC, EIAJ SSOP, and TSSOP packaging	• Saves board space and weight; TSSOP compatible with PCMCIA standards
• TI has established alternate sources	• Standardization that comes from a common product approach

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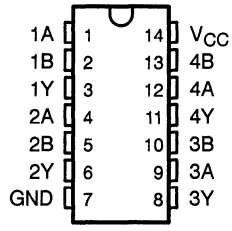
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV00 performs the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

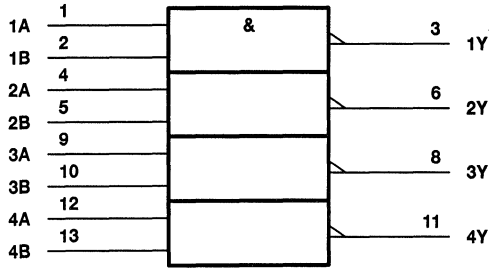
The SN74LV00 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		9	18		23	ns

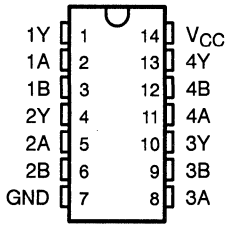
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 10 MHz	23	pF

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

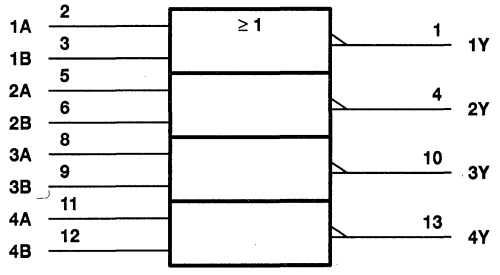
The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

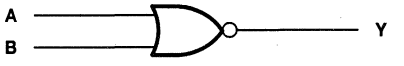
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		9	16		20	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

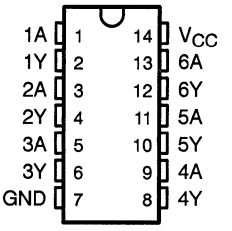
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 10 MHz	16	pF

SCLS184 – FEBRUARY 1993 – REVISED MARCH 1994

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

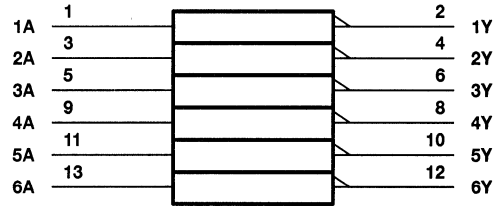
The SN74LV04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

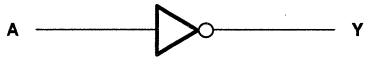
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	15		19	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

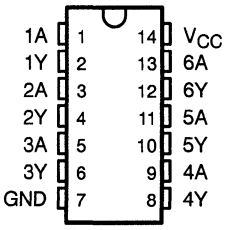
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 10 MHz	18	pF

SCLS185 – FEBRUARY 1993 – REVISED MARCH 1994

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \overline{A}$.

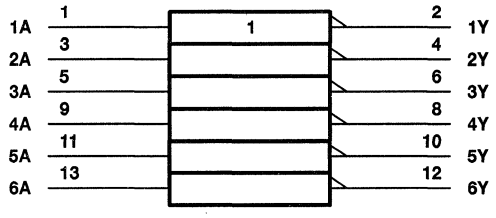
The SN74LVU04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVU04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

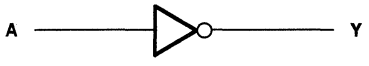
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2.4			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	T_A = −40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	$V_I = V_{IL}$,	I_{OH} = −100 µA	MIN to MAX	V_{CC}−0.5			V
	V_I = GND,	I_{OH} = −6 mA	3 V	2.4			
V_{OL}	$V_I = V_{IH}$,	I_{OL} = 100 µA	MIN to MAX			0.5	V
	$V_I = V_{CC}$,	I_{OL} = 6 mA	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		7		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		6	14		18	ns

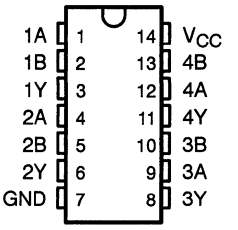
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 10 MHz	7	pF

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV08 performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

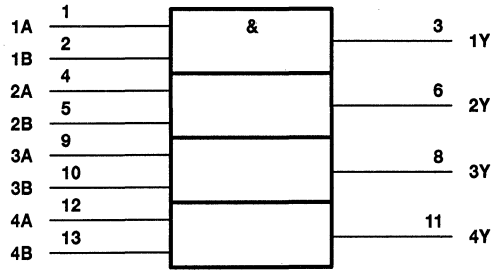
The SN74LV08 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or DW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		10	18		23	ns

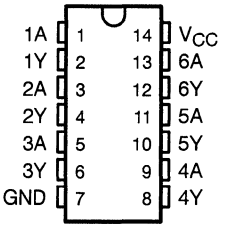
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 10 MHz	24	pF

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

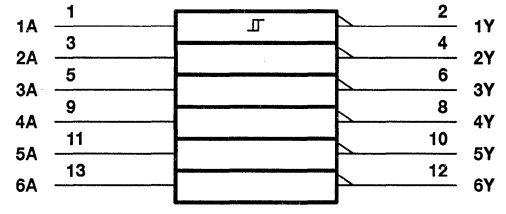
The SN74LV14 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

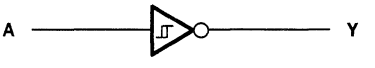
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2.4			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.4	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going threshold	2.7 V	1		2	V
		3 V	1.2		2.2	
		3.6 V	1.5		2.4	
V_{T-}	Negative-going threshold	2.7 V	0.4		1.4	V
		3 V	0.6		1.5	
		3.6 V	0.8		1.8	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	2.7 V	0.3		1.1	V
		3 V	0.4		1.2	
		3.6 V	0.4		1.2	
V_{OH}	$I_{OH} = -100$ μA	MIN to MAX	$V_{CC}-0.2$			V
	$I_{OH} = -6$ mA	3 V	2.4			
V_{OL}	$I_{OL} = 100$ μA	MIN to MAX			0.2	V
	$I_{OL} = 6$ mA	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND	3.6 V			±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		13	30		36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 10 MHz	22	pF

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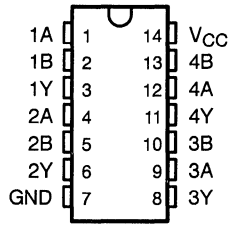
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV32 performs the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

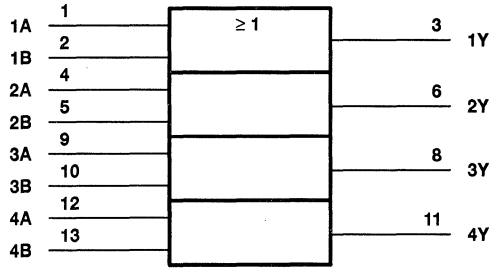
The SN74LV32 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = − 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		8	17		22	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 10 MHz	23	pF

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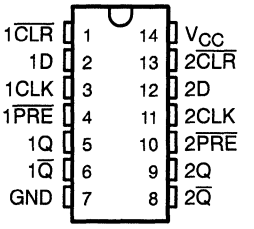
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74LV74 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV74 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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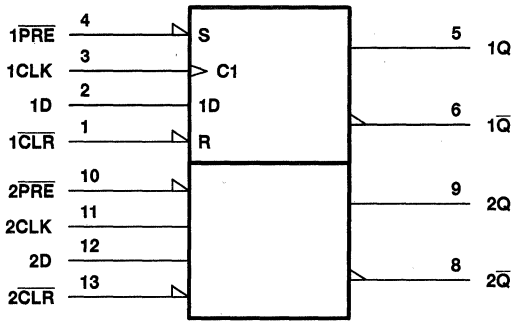
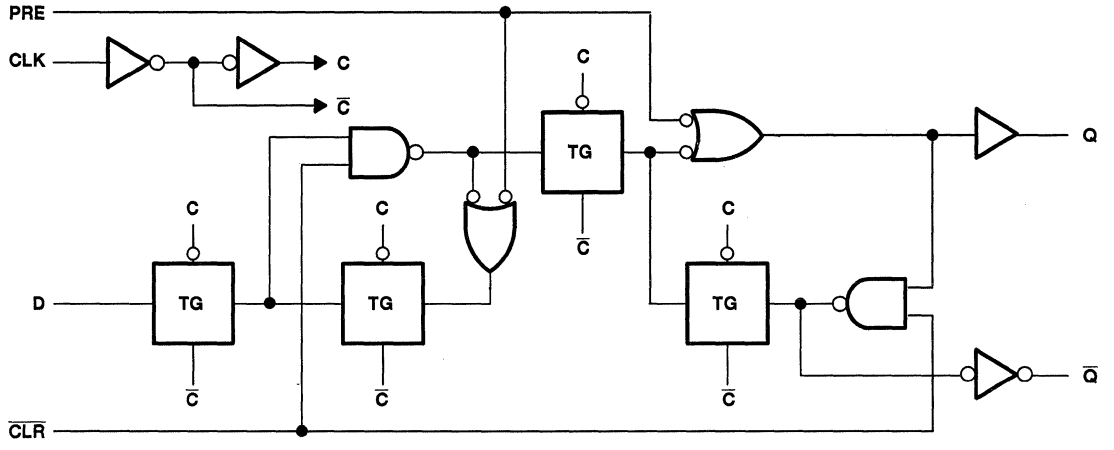
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	20		25		ns
		CLK high or low	20		25		
t_{su}	Setup time before CLK↑	Data	13		16		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	8		10		
t_h	Hold time, data after CLK↑		3		3		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	100		19		MHz
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		16	34		43	ns
	CLK			15	28		35	

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF,	f = 10 MHz	32	pF

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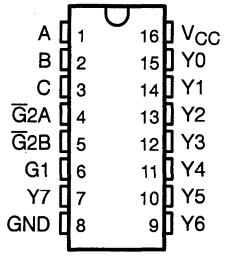
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LV138 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV138 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

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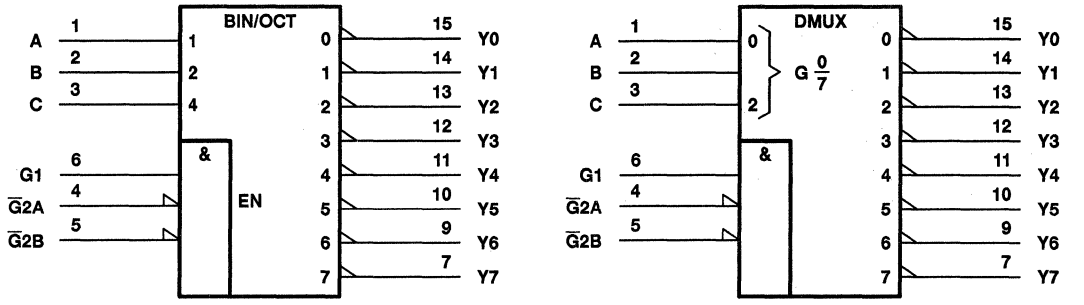
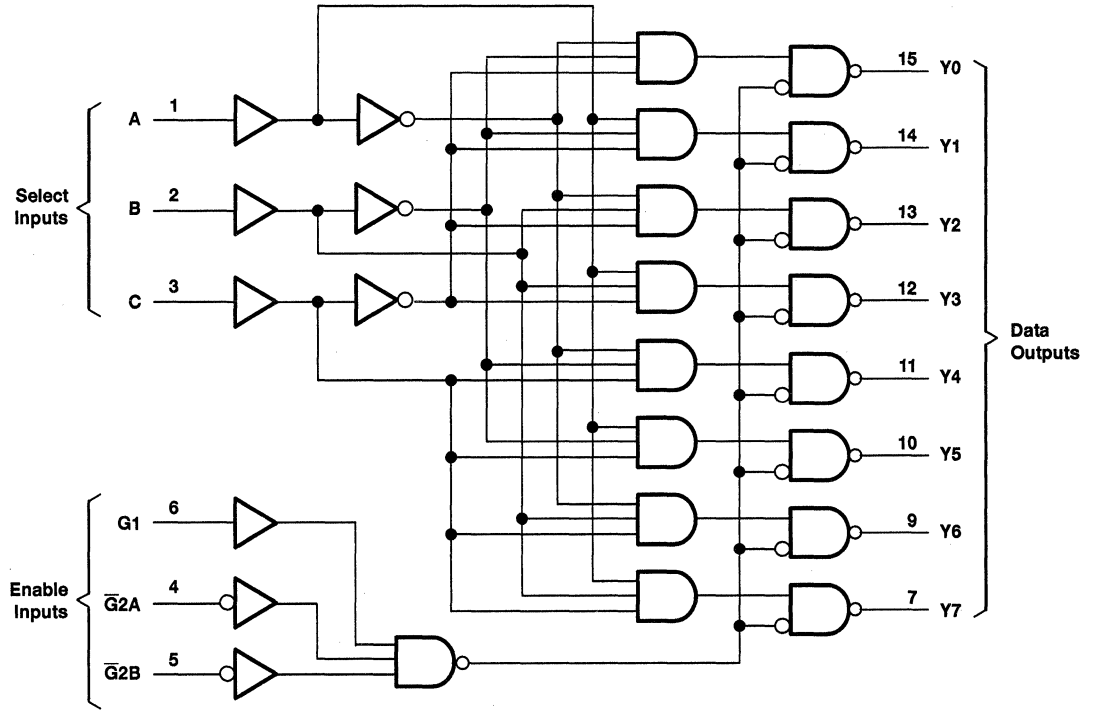
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = −6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B or C	Y		14	29		36	ns
	Enable			16	33		41	

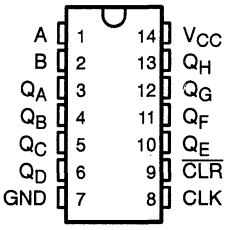
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per channel	C_L = 50 pF,	f = 10 MHz	47	pF

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 8-bit parallel-out serial shift register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV164 features AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{CLR}$) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN74LV164 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV164 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

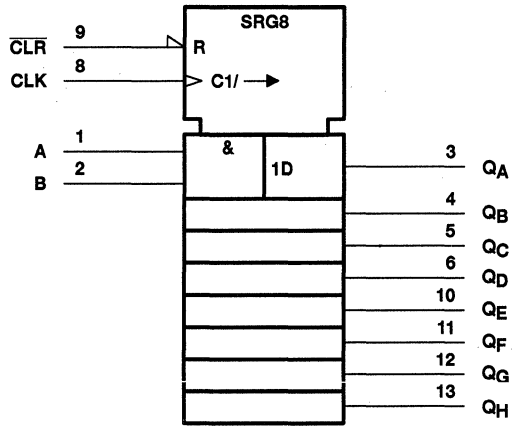
INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	$Q_B \ldots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state inputs conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a 1-bit shift.

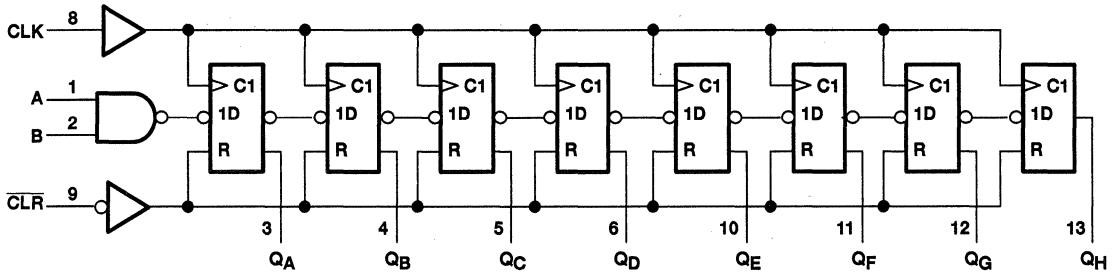
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

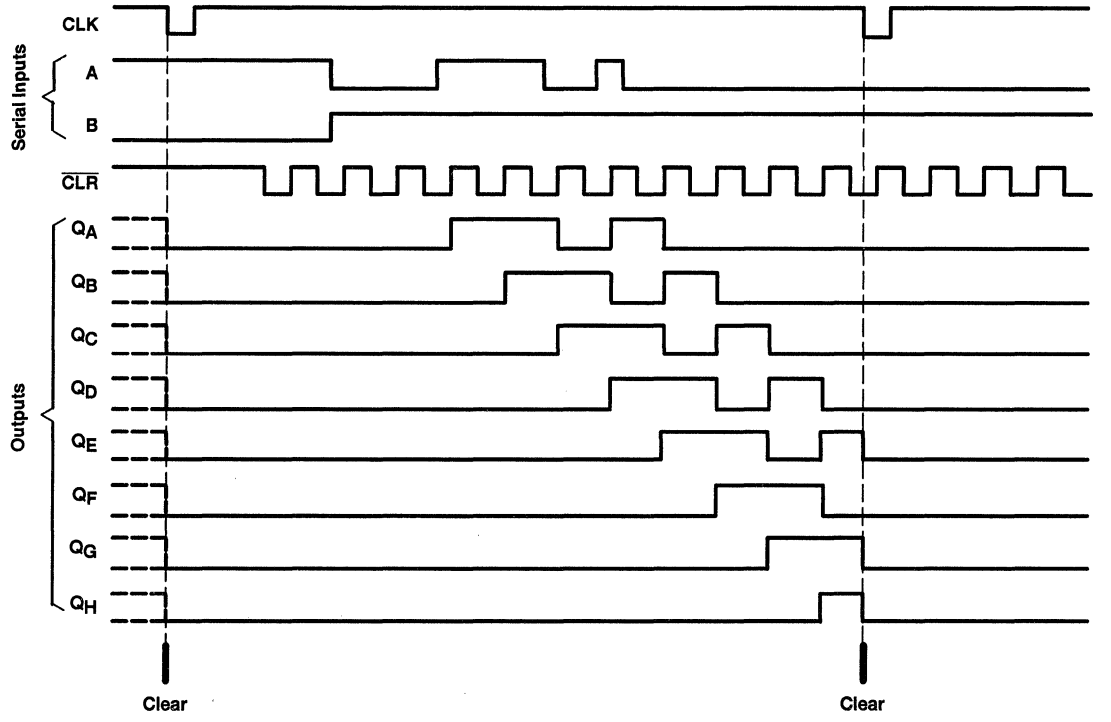


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = − 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	$\overline{CLR}$ low	20		25		ns
		CLK high or low	20		25		
t_{su}	Setup time before CLK↑	Data	13		16		ns
		$\overline{CLR}$ inactive	11		14		
t_h	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	75		19		MHz
t_{pd}	CLK	Q		16	29		36	ns
t_{PHL}	$\overline{CLR}$	Q		16	29		36	ns

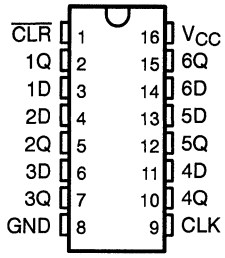
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	74	pF

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This hex D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV174 is a monolithic positive-edge-triggered flip-flop with a direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV174 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

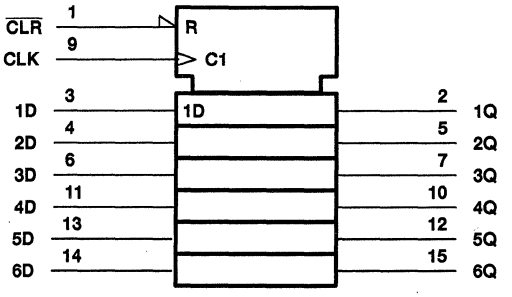
The SN74LV174 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

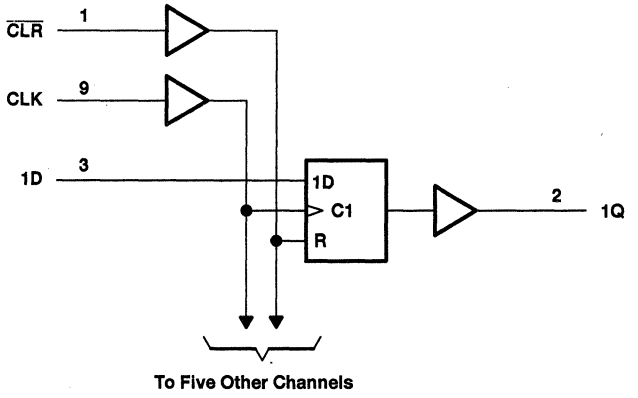
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = − 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	$\overline{CLR}$ low	20		25		ns
		CLK high or low	20		25		
t_{su}	Setup time before CLK↑	Data	13		16		ns
		$\overline{CLR}$ inactive	5		5		
t_h	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	80		19		MHz
t_{pd}	$\overline{CLR}$	Q		12	26		33	ns
	CLK			13	33		41	

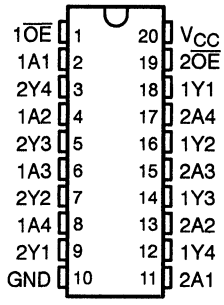
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 10 MHz	24	pF

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV240 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74LV240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

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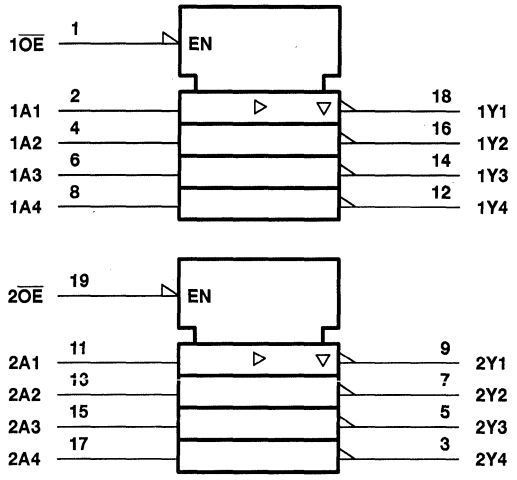
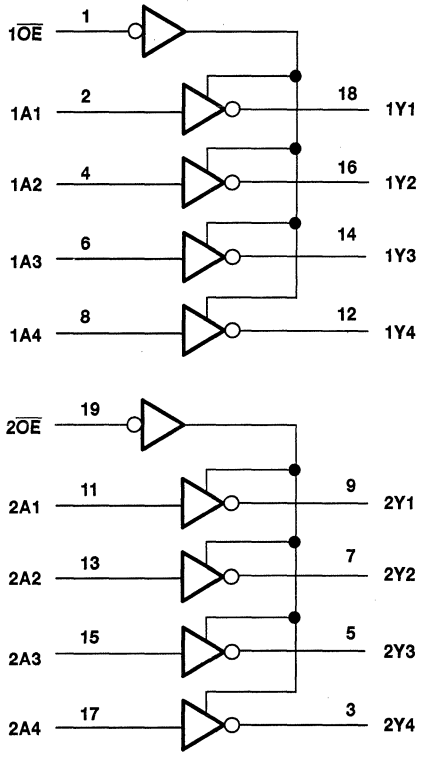
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 8 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 8 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	μA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	μA
C_i	V_I = V_{CC} or GND		3.3 V		3		pF
C_o	V_O = V_{CC} or GND		3.3 V		8		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		10	21		26	ns
t_{en}	$\overline{OE}$	Y		15	28		35	ns
t_{dis}	$\overline{OE}$	Y		17	27		33	ns

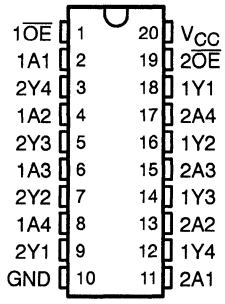
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF, f = 10 MHz	45	pF
		Outputs disabled		2.5	

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV244 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74LV244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

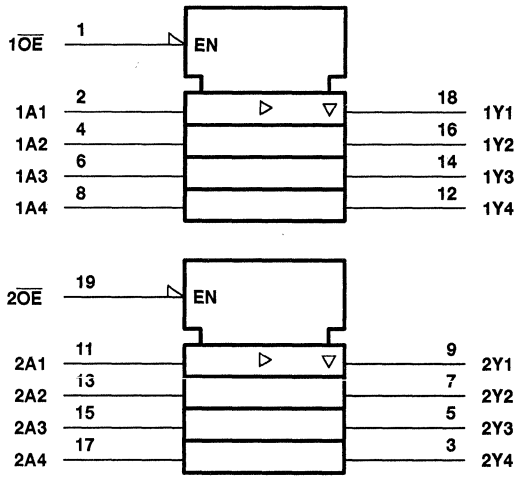
The SN74LV244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

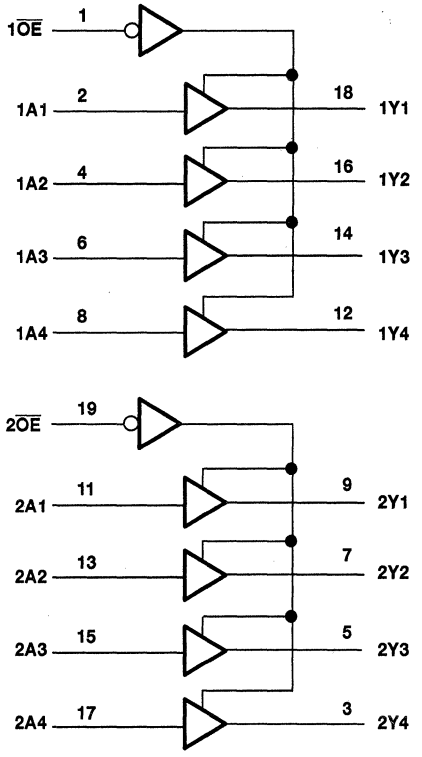
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	T_A = –40°C to 85°C			UNIT
				MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 8 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 8 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		3		pF
C_o	V_O = V_{CC} or GND		3.3 V		8		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		10	19		24	ns
t_{en}	$\overline{OE}$	Y		14	26		33	ns
t_{dis}	$\overline{OE}$	Y		15	26		32	ns

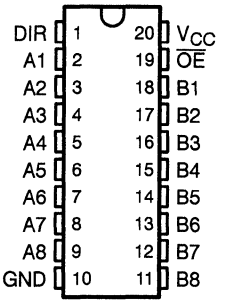
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF, f = 10 MHz	40	pF
		Outputs disabled		4	

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LV245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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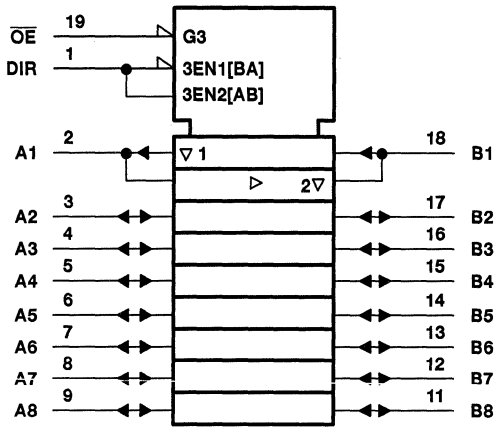
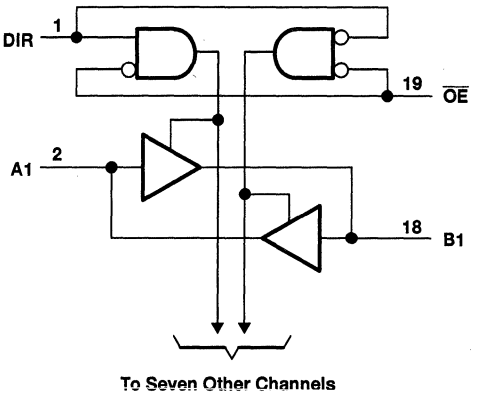
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.55 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		50	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 4: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V
		I_{OH} = – 8 mA		3 V	2.4			
V_{OL}		I_{OL} = 100 μA		MIN to MAX			0.2	V
		I_{OL} = 8 mA		3 V			0.4	
I_I		V_I = V_{CC} or GND		3.6 V			±1	μA
I_{OZ}‡		V_O = V_{CC} or GND		3.6 V			±5	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		2.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		7		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	B or A		8	16		20	ns
t_{en}	$\overline{OE}$	A or B		13	23		29	ns
t_{dis}	$\overline{OE}$	A or B		14	25		31	ns

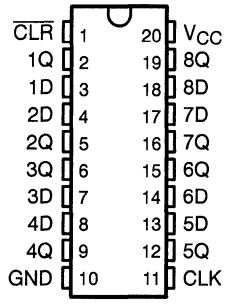
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 10 MHz	36	pF
		Outputs disabled		4	

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV273 is a positive-edge-triggered flip-flop with a direct clear input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

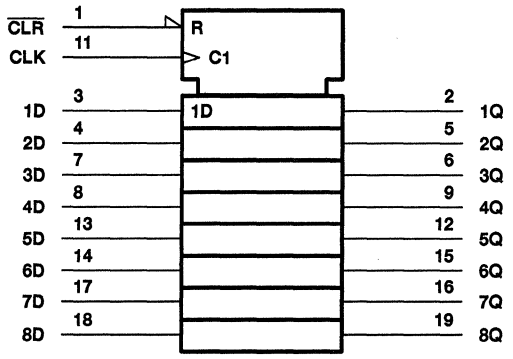
The SN74LV273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

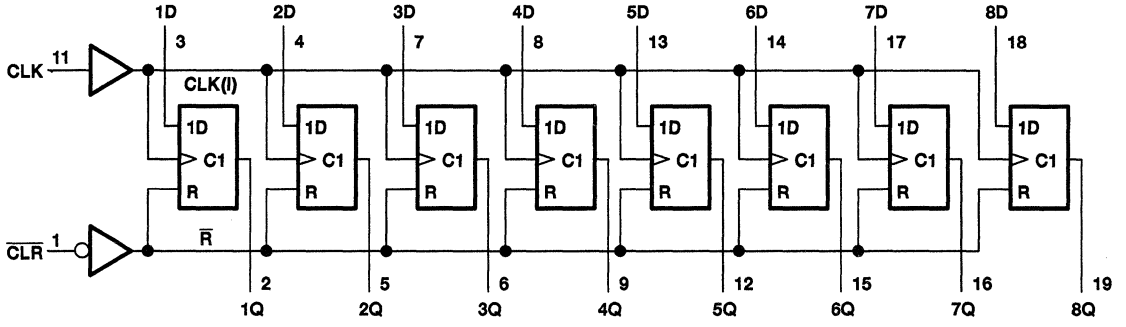
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−6	mA
I_{OL}	Low-level output current				6	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = − 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	$\overline{CLR}$ low	20		25		ns
		CLK high or low	20		25		
t_{su}	Setup time before CLK↑	Data	16		20		ns
		$\overline{CLR}$ inactive	5		5		
t_h	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}				90		19		MHz
t_{pd}	CLK	Q		12	25		31	ns
t_{PHL}	$\overline{CLR}$	Q		13	26		33	ns

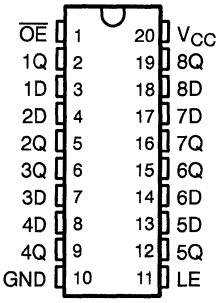
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 10 MHz	32	pF

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

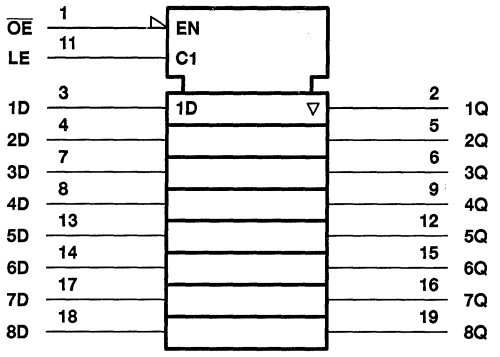
The SN74LV373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

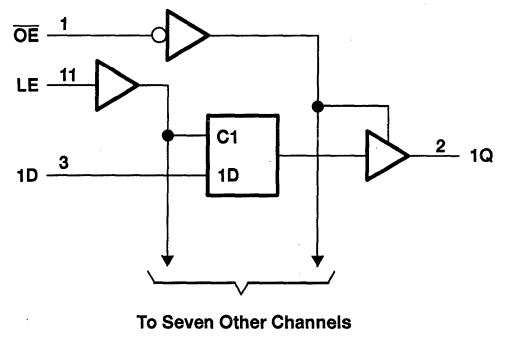
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF
C_o	V_O = V_{CC} or GND		3.3 V		7		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		20		25		ns
t_{su}	Setup time, data before LE↓	High or low	10		13		ns
t_h	Hold time, data after LE↓	High or low	10		10		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q		11	25		31	ns
	LE			15	29		36	
t_{en}	$\overline{OE}$	Q		15	29		36	ns
t_{dis}	$\overline{OE}$	Q		15	29		36	ns

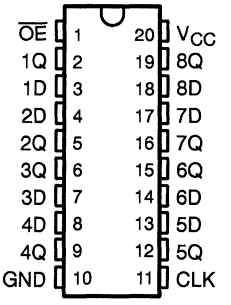
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 10 MHz	47	pF
		Outputs disabled		29	

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{OE}$) input does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

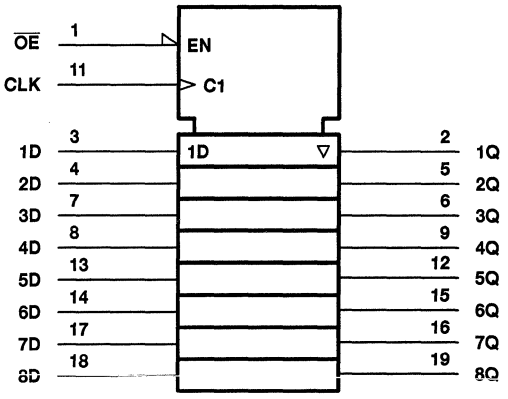
The SN74LV374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

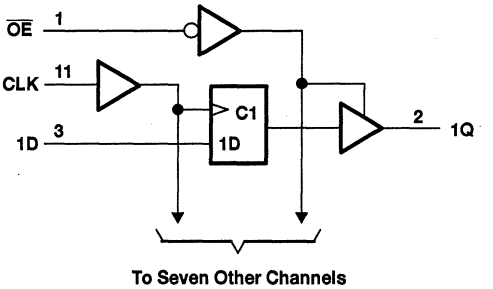
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −100 μA		MIN to MAX	V_{CC}−0.2			V
	I_{OH} = − 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND		3.6 V			±5	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	3.6 V			20	μA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		7		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	CLK high or low	20		25		ns
t_{su}	Setup time before CLK↑	High or low	13		16		ns
t_h	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	75		19		MHz
t_{pd}	CLK	Q		14	30		38	ns
t_{en}	$\overline{OE}$	Q		15	29		36	ns
t_{dis}	$\overline{OE}$	Q		15	29		36	ns

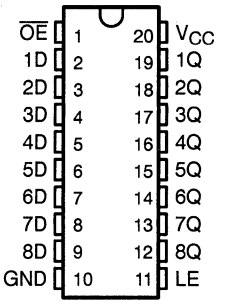
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 10 MHz	52	pF
		Outputs disabled		34	

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

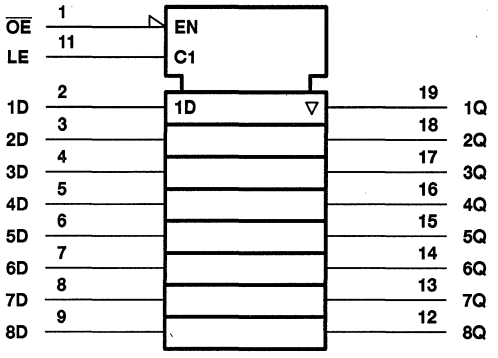
The SN74LV573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

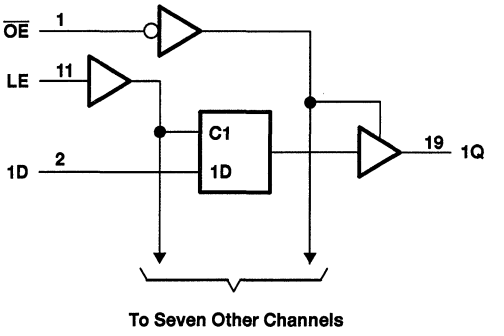
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 6 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF
C_o	V_O = V_{CC} or GND		3.3 V		7		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	LE high	20		25		ns
t_{su}	Setup time before LE↓	Data	10		13		ns
t_h	Hold time, data after LE↓		8		8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q		11	29		36	ns
	LE			15	30		38	
t_{en}	$\overline{OE}$	Q		13	26		33	ns
t_{dis}	$\overline{OE}$	Q		15	32		39	ns

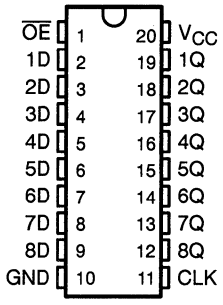
NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 10 MHz	30	pF
		Outputs disabled		14	

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

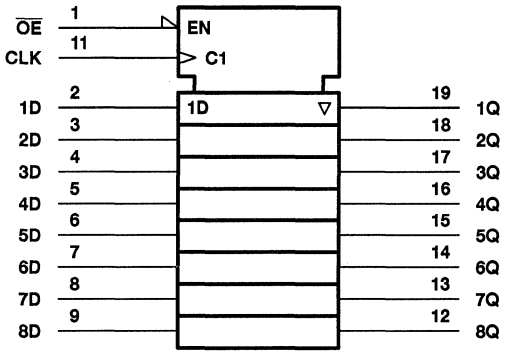
The SN74LV574 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

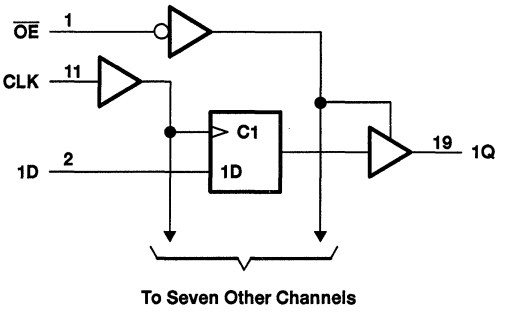
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current				−8	mA
I_{OL}	Low-level output current				8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 4: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = – 8 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 8 mA		3 V			0.4	
I_I	V_I = V_{CC} or GND		3.6 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND		3.6 V			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5		pF
C_o	V_O = V_{CC} or GND		3.3 V		7		pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	24	0	19	MHz
t_w	Pulse duration	CLK high or low	20		25		ns
t_{su}	Setup time before CLK↑	High or low	13		16		ns
t_h	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			24	70		19		MHz
t_{pd}	CLK	Q		14	30		38	ns
t_{en}	$\overline{OE}$	Q		13	27		34	ns
t_{dis}	$\overline{OE}$	Q		15	29		36	ns

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 10 MHz	40	pF
		Outputs disabled		22	

CBT BUS SWITCHES AND 5-V/3-V TRANSLATORS

Features

- Low propagation delay 5-V to 3-V translation
- Near-zero propagation delay
- Low (4 Ω–6 Ω) on resistance (r_{on})
- Reduced (6 pF–8 pF) input capacitance (C_i)
- SOIC, EIAJ SSOP, and TSSOP packaging

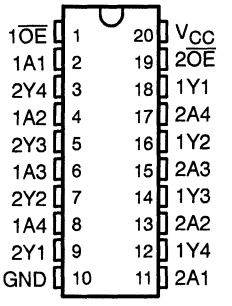
Benefits

- Isolates 3.3-V components from 5-V signals
- Facilitates high-performance bus connections and exchanges
- Minimizes bus parasitics
- Easily configurated for mixed mode applications (see application note, section 12)
- Saves board space and weight; TSSOP compatible with PCMCIA standards
- Standardization that comes from a common product approach

SCDS001A – NOVEMBER 1992 – REVISED MARCH 1994

- **Functionally Equivalent to QS3244**
- **Standard '244-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on resistance of the switch allows connections to be made with minimal propagation delay.

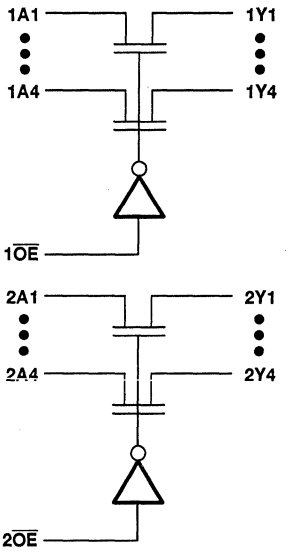
The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and data can flow from port A to port Y, or visa versa. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3244 is characterized for operation from 0°C to 70 °C.

FUNCTION TABLE

INPUTS		INPUT/OUTPUTS	
$1\overline{OE}$	$2\overline{OE}$	1A, 1Y	2A, 2Y
L	L	1A = 1Y	2A = 2Y
L	H	1A = 1Y	Z
H	L	Z	2A = 2Y
H	H	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Continuous channel current ..... 128 mA
Clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.25 V,	V_I = 5.25 V to GND				±5	μA
I_{OS}		V_{CC} = 4.75 V,	$V_{I(A)}$ = 0,	$V_{I(Y)}$ = 4.75 V		250		mA
I_{CC}		V_{CC} = 5.25 V,	I_O = 0,	V_I = V_{CC} or GND			50	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.25 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4.75 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the Y pins at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or Y) pins.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

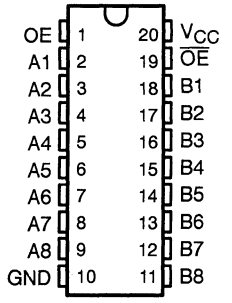
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶				0.25	ns
t_{en}	$\overline{OE}$	A or Y	1	8.9	ns
t_{dis}	$\overline{OE}$	A or Y	1	7.4	ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

SCDS002A – NOVEMBER 1992 – REVISED MARCH 1994

- **Functionally Equivalent to QS3245**
- **Standard '245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3245 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on resistance of the switch allows connections to be made without adding propagation delay.

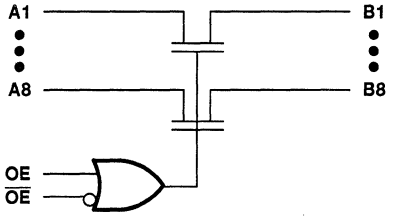
The device is organized as one 8-bit switch bank with dual output-enable (OE and $\overline{OE}$) inputs. When $\overline{OE}$ is low or OE is high, the switch is on and port A is connected to port B. When $\overline{OE}$ is high and OE is low, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		INPUT/ OUTPUTS
OE	$\overline{OE}$	A, B
X	L	A = B
H	X	A = B
L	H	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.25 V,	V_I = 5.25 V or GND				±5	μA
I_{OS}		V_{CC} = 4.75 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.75 V		250		mA
I_{CC}		V_{CC} = 5.25 V,	I_O = 0,	V_I = V_{CC} or GND			50	μA
ΔI_{CC}§	Control pins	V_{CC} = 5.25 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.75 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

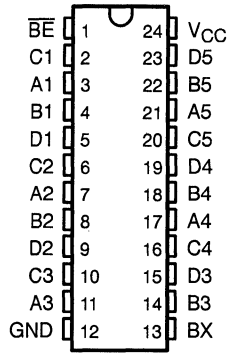
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$ or OE	A or B	1	9.1	ns
t_{dis}	$\overline{OE}$ or OE	A or B	1	8.7	ns

† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

- **Functionally Equivalent to QS3383 and QS3L383**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3383 provides ten bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

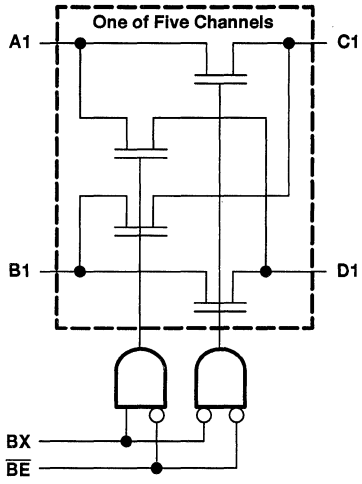
The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the AB and CD pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when $\overline{BE}$ is low.

The SN74CBT3383 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

$\overline{BE}$	BX	A1–A5	B1–B5
L	L	C1–C5	D1–D5
L	H	D1–D5	C1–C5
H	X	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 6 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.25 V,	V_I = 5.25 V or GND				±5	µA
I_{OS}		V_{CC} = 4.75 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.75 V		250		mA
I_{CC}		V_{CC} = 5.25 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}§	Control pins	V_{CC} = 5.25 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.75 V,	V_I = 0,	I_I = 64 mA		5	7	Ω
		V_{CC} = 4.75 V,	V_I = 0,	I_I = 30 mA		5	7	
		V_{CC} = 4.75 V,	V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and the B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†				0.25	ns
t_{BX}	BX	A, B, C, or D	1	9.2	ns
t_{en}	$\overline{BE}$	A or B	1	8.6	ns
t_{dis}	$\overline{BE}$	A or B	1	7.5	ns

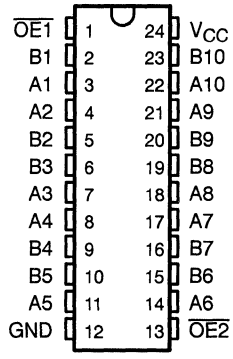
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical On resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

SCDS004A – NOVEMBER 1992 – REVISED APRIL 1994

- **Functionally Equivalent to QS3384 and QS3L384**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3384 provides ten bits of high-speed TTL-compatible bus switching. The low on resistance of the switch allows connections to be made without adding propagation delay.

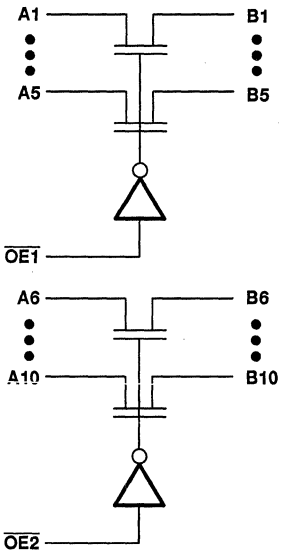
The device is organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3384 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

$\overline{OE1}$	$\overline{OE2}$	B1–B5	B6–B10
L	L	A1–A5	A6–A10
L	H	A1–A5	Z
H	L	Z	A6–A10
H	H	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.25 V,	V_I = 5.25 V or GND				±5	μA
I_{OS}		V_{CC} = 4.75 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.75 V		250		mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.25 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4.75 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

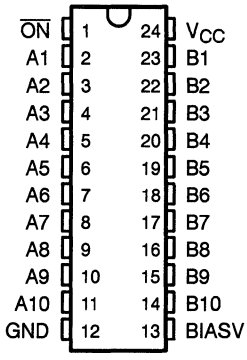
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.5	ns
t_{dis}	$\overline{OE}$	A or B	1	8.5	ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

- 5-Ω Switch Connection Between Two Ports
- Near-Zero Propagation Delay
- TTL-Compatible Input and Output Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Small-Outline (DW) and Thin Shrink Small-Outline (PW) Packages

DW OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT6800 provides ten bits of high-speed TTL-compatible bus switches. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

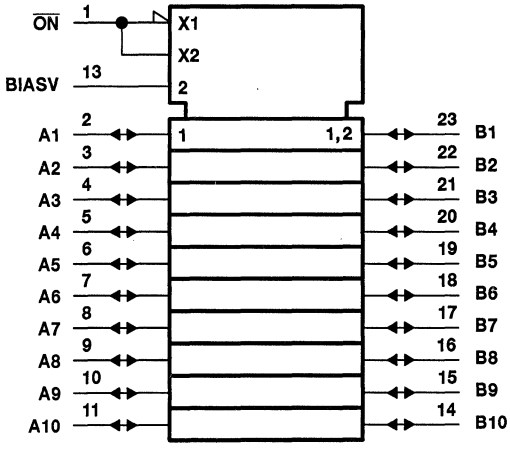
The SN74CBT6800 is organized as one 10-bit switch bank with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open and the B port is precharged to the BIASV voltage through the equivalent of a 10-kΩ resistor.

The SN74CBT6800 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

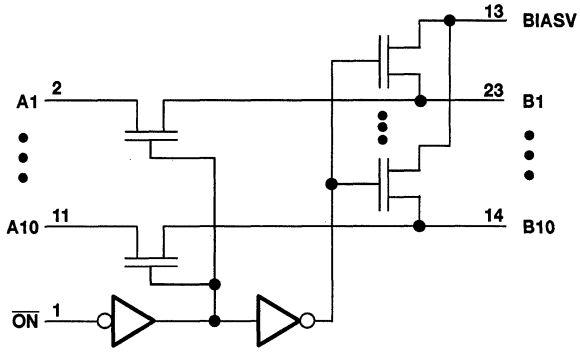
$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIASV	Precharge

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Bias voltage range, BIASV ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
BIASV	Supply voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O = 0	0.25			mA
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}§		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA			6	Ω
			V_I = 2.4 V,	I_I = 15 mA			12	
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O = 0	0.25			mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C to 85°C		T_A = 0°C to 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}†	A or B	B or A				0.25	ns
t_{PHL}†						0.25	
t_{PZH}‡	$\overline{ON}$	A or B			1.5	7.5	ns
t_{PZL}§					1.5	7.5	
t_{PHZ}‡	$\overline{ON}$	A or B			1.5	6.5	ns
t_{PLZ}§					1.5	6.5	

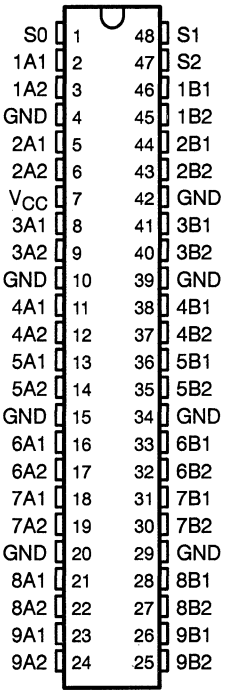
† This parameter is characterized but not tested. This propagation delay is due to the RC time constant of the on-state resistance of the switch and the load capacitance.
‡ BIASV = GND
§ BIASV = 3 V
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

SCDS006A – NOVEMBER 1992 – REVISED MARCH 1994

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74CBT16209 provides 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

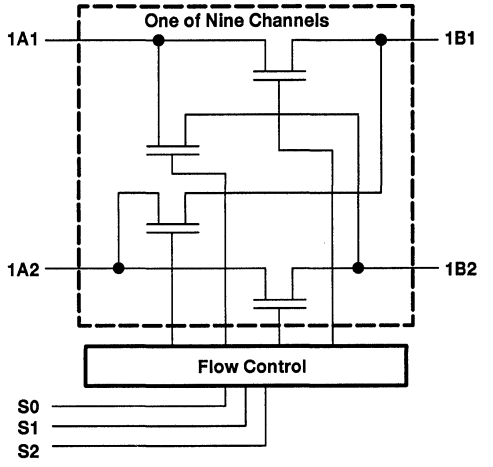
The device operates as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) pins.

The SN74CBT16209 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

logic diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	V_I(A) = 0,	V_I(B) = 4.5 V	100			mA
I_{CC}§		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			100	µA
ΔI_{CC}		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(ON)}$		V_O = 3 V or 0,	$\overline{OE}$ = GND			8		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA			6	Ω
			V_I = 2.4 V,	I_I = 15 mA			12	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = –40° to 85°C		T_A = 0° to 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}†	A or B	B or A				0.25	ns
t_{PHL}†						0.25	
t_{PLH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PHL}					1.5	7.5	
t_{PZH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	S0, S1, S2	A or B			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

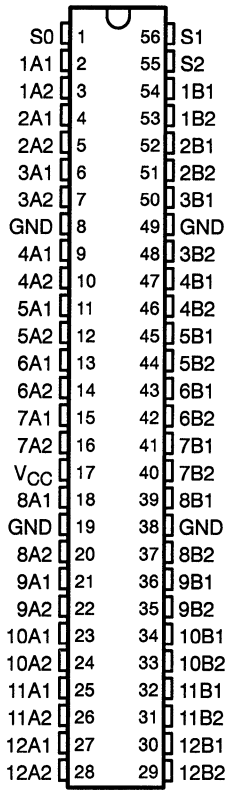
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

SCDS007A – NOVEMBER 1992 – REVISED MARCH 1994

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on resistance of the switch allows connections to be made without adding propagation delay.

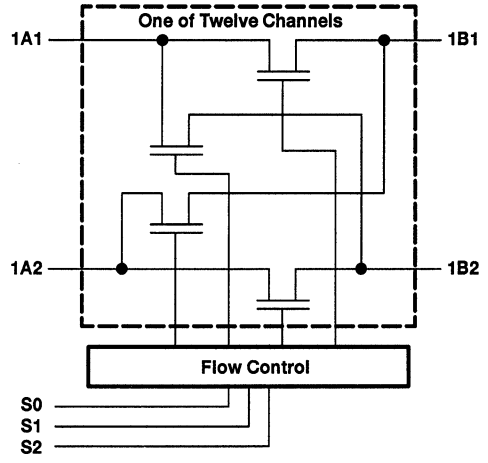
The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) pins.

The SN74CBT16212 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

logic diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	V_I(A) = 0,	V_I(B) = 4.5 V	100			mA
I_{CC}§		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			100	µA
ΔI_{CC}		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(ON)}$		V_O = 3 V or 0,	$\overline{OE}$ = GND			8		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA			6	Ω
			V_I = 2.4 V,	I_I = 15 mA			12	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40° to 85°C		T_A = 0° to 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}†	A or B	B or A				0.25	ns
t_{PHL}†						0.25	
t_{PLH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PHL}					1.5	7.5	
t_{PZH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	S0, S1, S2	A or B			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on resistance of the switch and a load capacitance of 50 pF.

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW

SCDS008 – MAY 1993 – REVISED MARCH 1994

- **5-Ω Switch Connection Between Two Ports**
- **Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

The SN74CBT16214 provide 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low on resistance of the switch allows connections to be made without adding propagation delay.

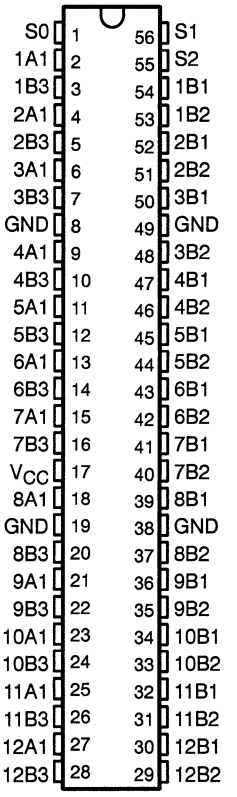
The SN74CBT16214 operates as a 12-bit bus switch via the data-select (S0–S2) pins.

The SN74CBT16214 is characterized for operation from –40°C to 85°C.

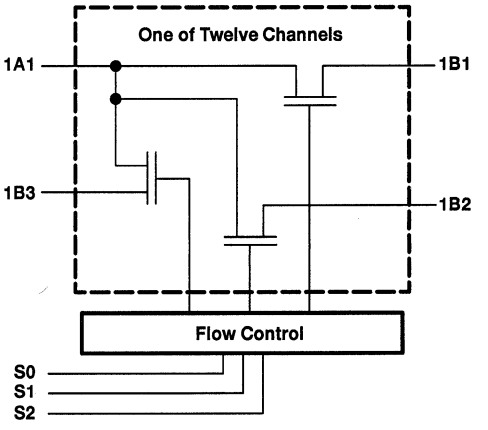
FUNCTION TABLE

S2	S1	S0	A1	FUNCTION
L	L	L	Z	Disconnect
L	L	H	B1	A1 to B1
L	H	L	B2	A1 to B2
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A1 to B3
H	H	L	B1	A1 to B1
H	H	H	B2	A1 to B2

DGG OR DL PACKAGE
(TOP VIEW)



logic diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	V_I(A) = 0,	V_I(B) = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			100	µA
ΔI_{CC}§		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(ON)}$		V_O = 3 V or 0,	$\overline{OE}$ = GND			10		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0,	I_I = 48 mA			6	Ω
			V_I = 2.4 V,	I_I = 15 mA			12	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On resistance is determined by the lower of the voltages of the two (A or B) pins.

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Mixing It Up With 3.3 Volts

Ken Ristow
Steve Perna
Advanced System Logic – Semiconductor Group

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Printed in the U.S.A.

Contents

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Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others will offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of 1.2 μm, and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3-V operation.

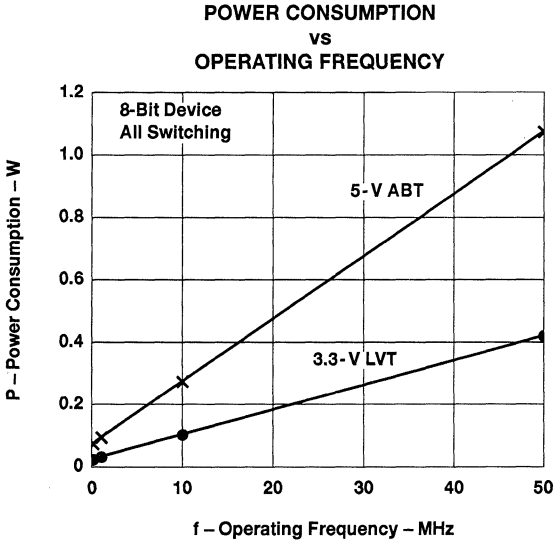

Figure 1. 3-V to 5-V Power vs Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as laptop computers, automotive and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups which can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged but the spread actually runs from about 3.3 V up to 3.9 V. For now the unregulated battery market demands low-voltage products which are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices will slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V, with volume requirements not beginning until the '94–'95 time frame. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC}. This limits input voltages to V_{CC} + 0.5 V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices which support this mode must be designed for maximum input voltages of 5.5 V without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL}, which are ratios of V_{CC}. Low-voltage TTL (LVTTL) utilizes the standard-TTL input levels of 0.8 and 2 V as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

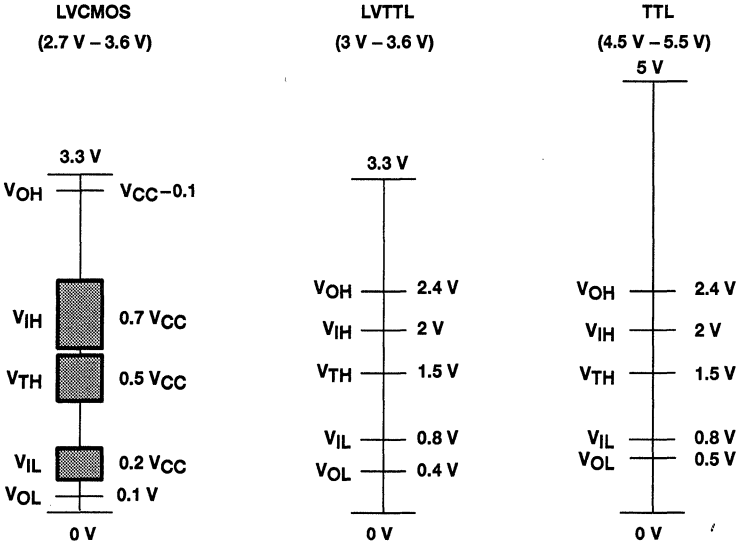

Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices, and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7- to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = –32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CC(L)}$ = 15 mA
$I_{CC(H)}$ = 250 µA
$I_{CC(Z)}$ = 250 µA

Propagation delays of:
t_{pd} < 4.6 ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48- and 56-pin SSOP for LVT Widebus™
20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

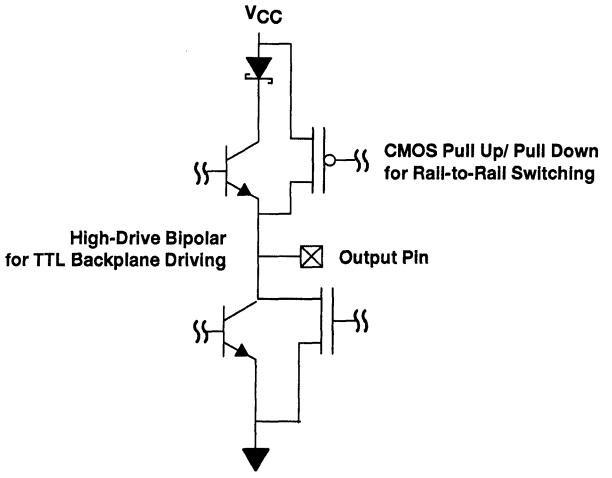

Figure 3. Simplified LVT Output Structure

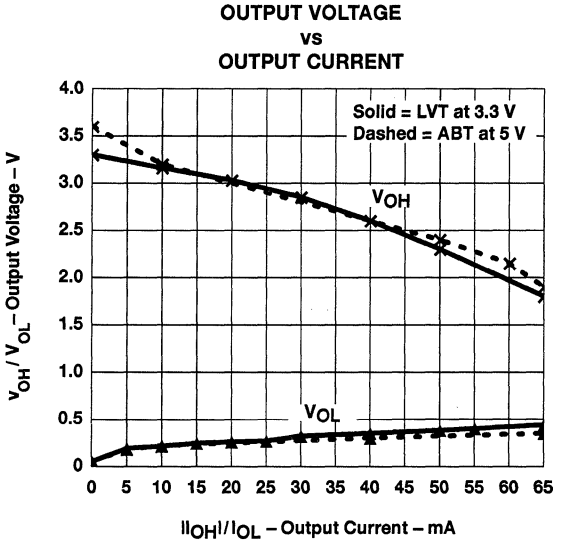

Figure 4. ABT vs LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ±100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ±500 μA, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load, and does not affect the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.

Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

Mark McClear
Advanced System Logic – Semiconductor Group

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Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

1. *Split-rail* or dual 3.3-V and 5-V V_{CC} devices.
2. Completely 5-V tolerant, pure 3.3-V V_{CC} components.

This paper deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and data-path voltage translators, but the following precautions are usually recommended:

1. Dual-V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to the parts in the event that one V_{CC} rail ramps faster than the other. These stringent requirements are often difficult to meet from a system timing standpoint, and offer little flexibility for partial system power down or other advanced power-saving design techniques.
2. Simply because the part has a 5-V V_{CC} pin does not necessarily guarantee that the part will actually switch all the way to the 5-V rail. Switching all the way to 5 V is one way to reduce the power consumption in 5-V memories or other pure 5-V CMOS circuits which are driven by a level-shifter device (this paper will demonstrate others as well).

A quick check of the data sheet for the product in question will reveal if the part drives all the way to the 5-V rail. If the output high voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs will typically drive only to around 3.6 V.

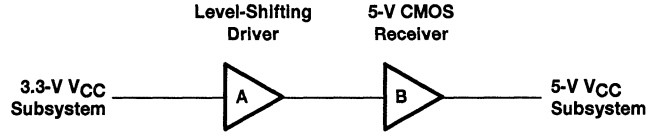
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices mentioned above. From a single V_{CC} source they avoid the power-sequencing problems of the split rails, and are also offered in a number of functions, bit widths, and storage options. The one potential drawback of the single-V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail . . . but is this really a drawback?

The Misconception About ΔI_{CC}

The component selection of a level shifter impacts two major aspects of total system power dissipation:

1. The impact that the V_{OH} level of the driving part (A in Figure 1) has on the power dissipation of the receiving device (B in Figure 1), commonly known as ΔI_{CC}, and
2. The power of the device itself.



Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B in Figure 1) due to the V_{OH} level of the driving device (A in Figure 1). Put another way, one would correctly expect that a TTL-compatible 5-V CMOS product would have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from zero to V_{CC}.

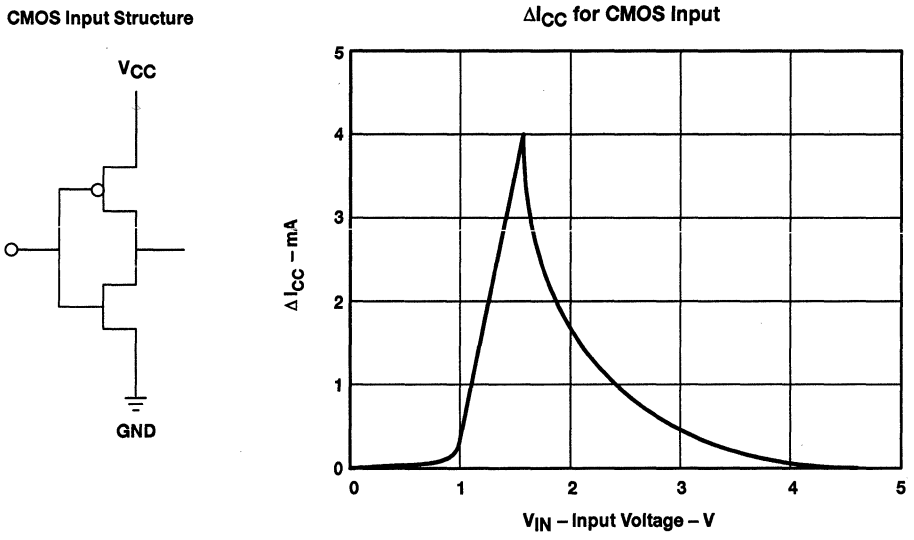


Figure 2. Basic CMOS Input Structure and Typical ΔI_{CC} Current

Note that as expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V.

Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

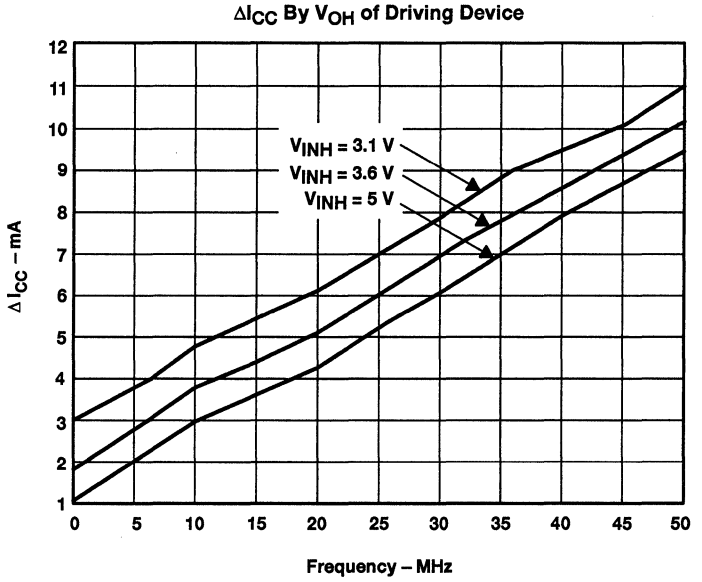


Figure 3. ΔI_{CC} – 16-Bit Device

Here we see that ΔI_{CC} is in fact 2 to 3 mA higher for the case where V_{OH} is only 3.1 V than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might be tempted to conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the system power impact of the driving device.

Figure 4 shows the V_{OH} of two devices; the FCT164245 split-rail device from Integrated Device Technologies, and the 'LVT16245A from Texas Instruments.

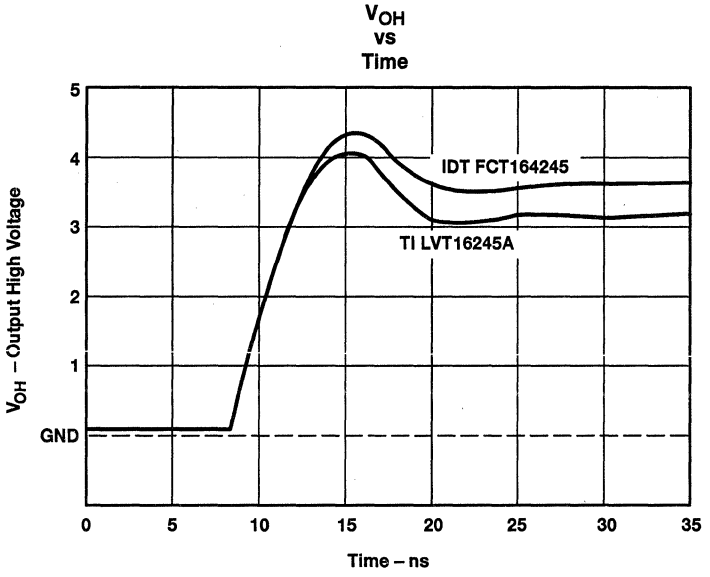


Figure 4. V_{OH} of FCT164245 and 'LVT16245A

From the above, you would correctly conclude that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total system power dissipation that selection of a level-shifter device has from system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI 'LVT16245A, and the worst-case ΔI_{CC} (V_{OH} = 3.1 V) graphed on the same vertical scale.

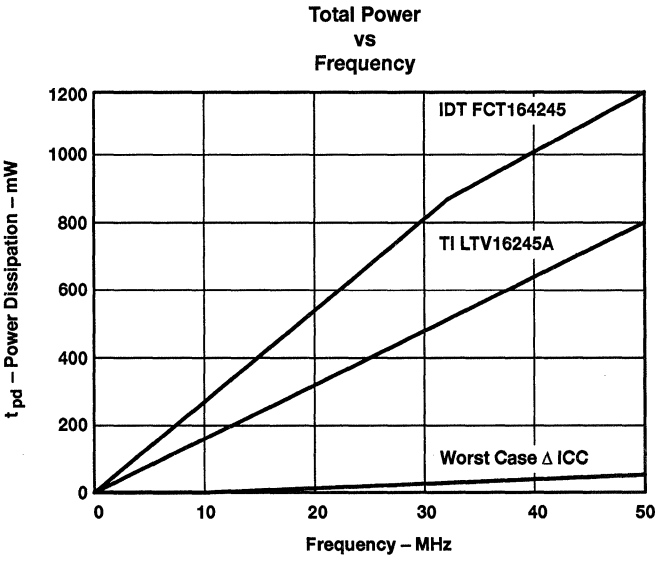


Figure 5. Total System Power Dissipation Impact

From this we can see that even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} will be more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as *partial power down*. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's Low-Voltage Technology (LVT) product line mentioned above offer a parametric specification call I_{OFF}, which guarantees that the output pins of the parts will remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT part from dragging down the bus of an active part in the system, and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating (and causing damage to the devices on the bus). Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the 'LVT16245A (and others) from TI have a circuit feature called a *bus-hold cell* (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and, of course, power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

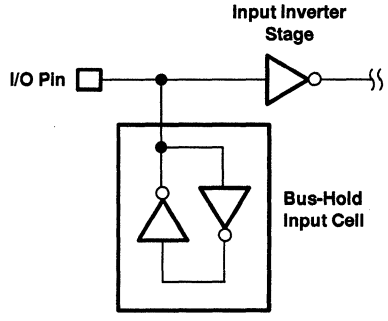


Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Texas Instruments Crossbar Switches (CBT)

Ramzi Ammar
Advanced System Logic – Semiconductor Group

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What Are Texas Instruments Crossbar Switches (CBT)?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an N-channel MOS transistor driven by a CMOS gate. When enabled, the N-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on resistance of approximately 5 Ω and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at ≈ 1 V less than the gate potential regardless of the level at the input pin. This is one of the N-channel transistor characteristics (see Figures 1 and 2). Note the ≈ 1 V difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.

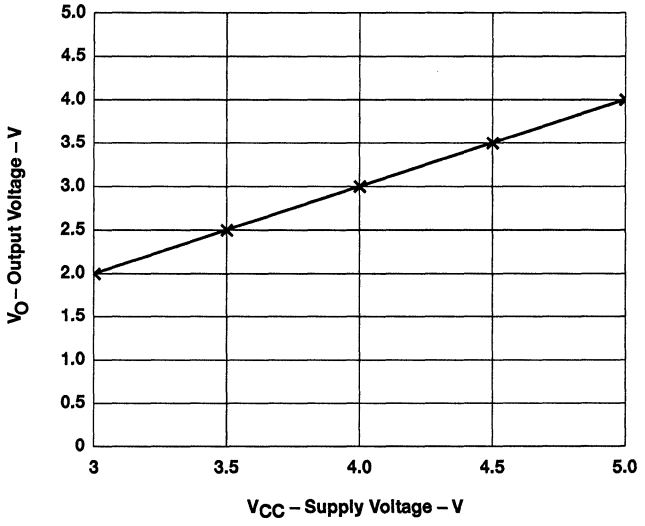


Figure 1. Output Voltage vs Supply Voltage

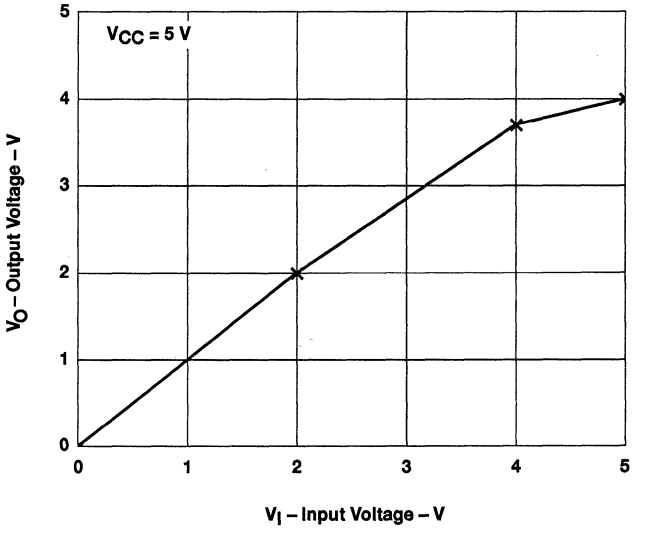


Figure 2. Output Voltage vs Input Voltage

The on-state resistance r_{on} increases gradually with V_I until V_I approaches $V_{CC} - 1$ V, where r_{on} rapidly increases clamping V_O at $V_{CC} - 1$ V (see Figure 3). Also, by the nature of the N-channel transistor design, the input and output pins are fully isolated when the transistor is off. Leakage and capacitance is to ground and not between input and output which minimizes feedthrough when the transistor is off.

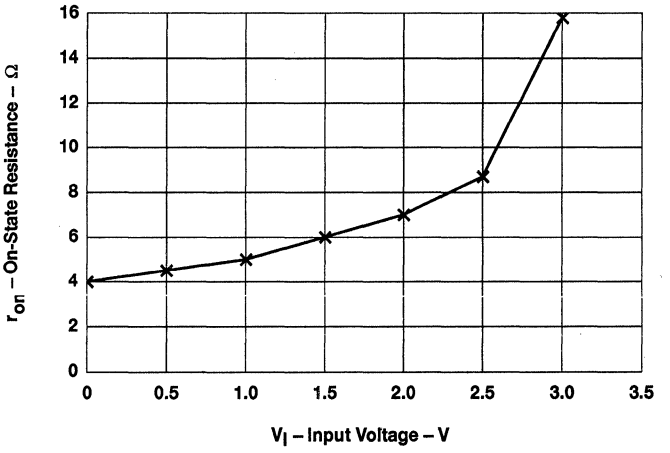
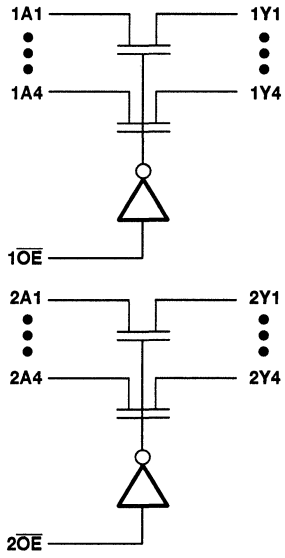


Figure 3. On-State Resistance vs Input Voltage

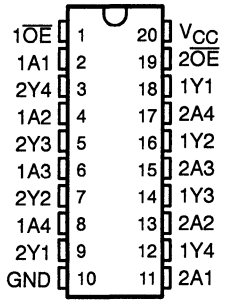
What Does Texas Instruments Offer in the CBT Family?

The following CBT switches offered by Texas Instruments are shown in this application report. This helps designers understand and identify areas where these devices are useful.

SN74CBT3244 – 8-Bit Crossbar Switch



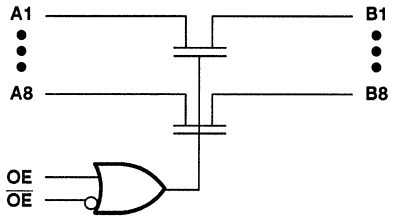
DB, DW, OR PW PACKAGE
(TOP VIEW)



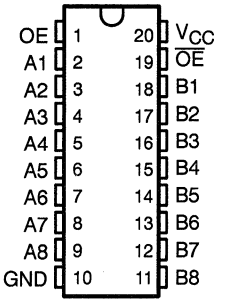
FUNCTION TABLE

INPUTS		INPUT/OUTPUTS	
1OE	2OE	1A, 1Y	2A, 2Y
L	L	1A= 1Y	2A= 2Y
L	H	1A= 1Y	Z
H	L	Z	2A = 2Y
H	H	Z	Z

SN74CBT3245 – 8-Bit Crossbar Switch



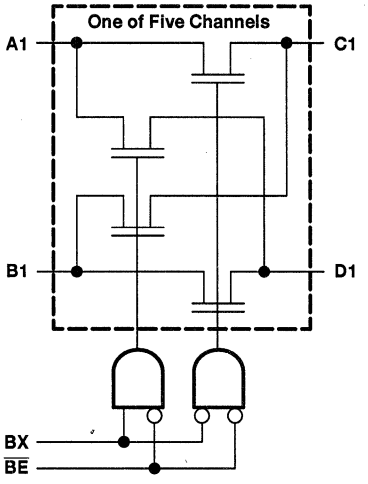
DB, DW, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		INPUT/ OUTPUTS
OE	$\overline{OE}$	A, B
X	L	A = B
H	X	A = B
L	H	Z

SN74CBT3383 – 10-Bit Bus-Exchange Switch



DB, DW, OR PW PACKAGE
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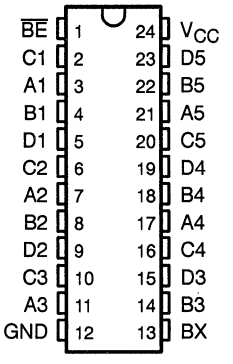
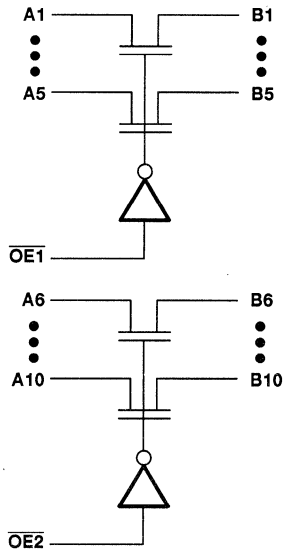


FUNCTION TABLE

$\overline{BE}$	BX	A1–A5	B1–B5
L	L	C1–C5	D1–D5
L	H	D1–D5	C1–C5
H	X	Z	Z

SN74CBT3384 – 10-Bit Crossbar Switch



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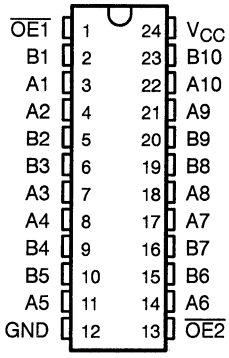
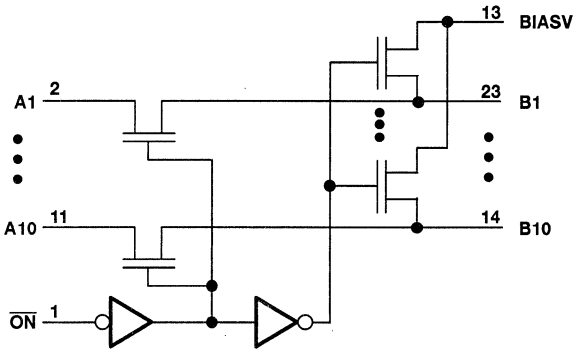
(TOP VIEW)



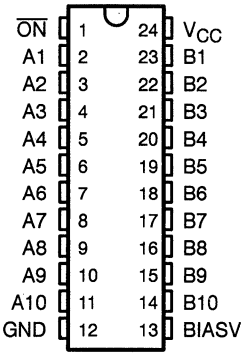
FUNCTION TABLE

$\overline{OE1}$	$\overline{OE2}$	B1–B5	B6–B10
L	L	A1–A5	A6–A10
L	H	A1–A5	Z
H	L	Z	A6–A10
H	H	Z	Z

SN74CBT6800 – 10-Bit Crossbar Switch With Precharged Outputs for Live Insertion



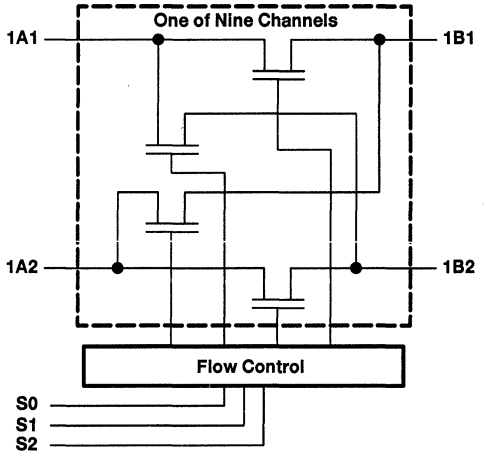
DW OR PW PACKAGE
(TOP VIEW)



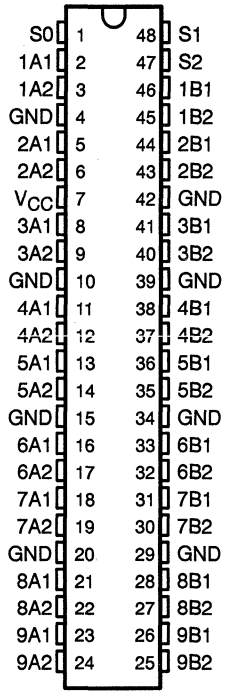
FUNCTION TABLE

$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIAS V	Precharge

SN74CBT16209 – 18-Bit Bus-Exchange Switch



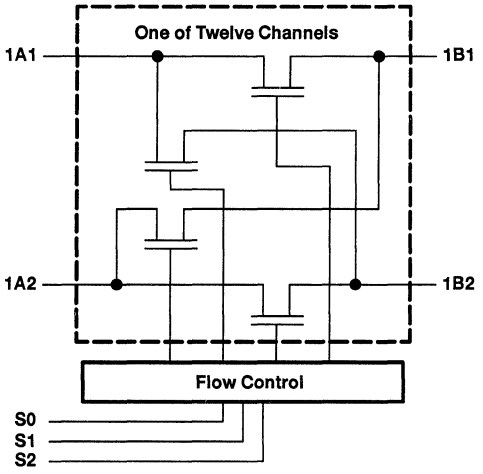
DGG OR DL PACKAGE
(TOP VIEW)



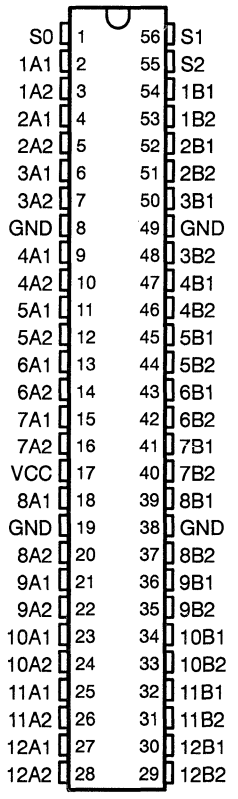
FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

SN74CBT16212 – 24-Bit Bus-Exchange Switch



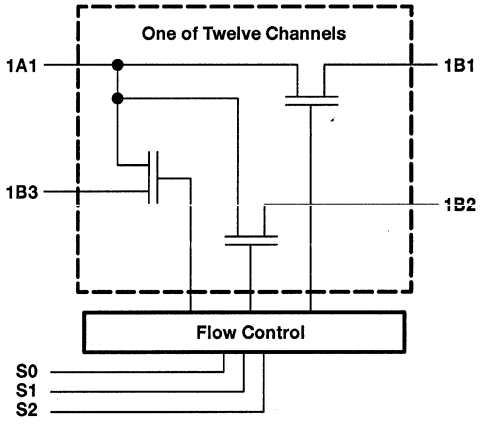
DGG OR DL PACKAGE
(TOP VIEW)



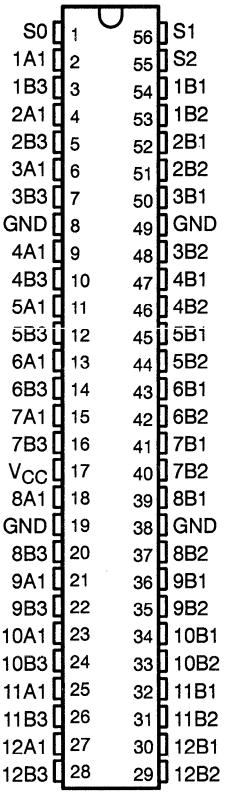
FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

SN74CBT16214 – 3-to-1 Bus-Select Switch



DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

S2	S1	S0	A1	FUNCTION
L	L	L	Z	Disconnect
L	L	H	B1	A1 to B1
L	H	L	B2	A1 to B2
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A1 to B3
H	H	L	B1	A1 to B1
H	H	H	B2	A1 to B2

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices can also provide bidirectional 5-V to 3-V translation with no added propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes the gate to drop to 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_O to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

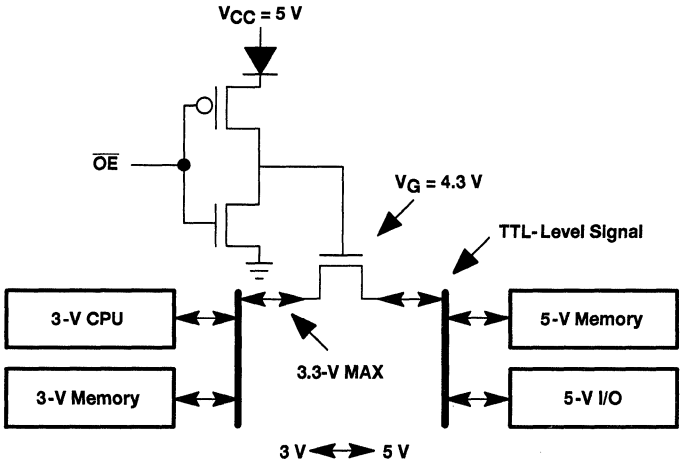


Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems where signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices can also replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on resistance and without the reliability problem that relays provide.

Bus Switches Convert TTL Logic to Hot-Card Insertion Capability

This application is used mostly in systems that require hot-card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and can not be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., that do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first followed by the signal pins then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance can not be achieved using CMOS logic since it contains P-channel transistors that provide an inherent diode between the I/O pins and V_{CC} that is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground leaving the bus disturbed.

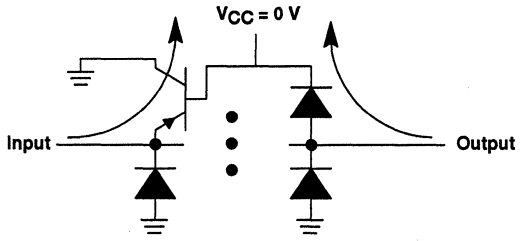


Figure 5. ACL Direction of Current Flow When V_{CC} = 0 V

Another issue to consider is that, when V_{CC} is ramping but still below the device operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error will not occur.

There are two solutions to this problem. One is to use Texas Instruments BCT or ABT families, since both guarantee the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down .

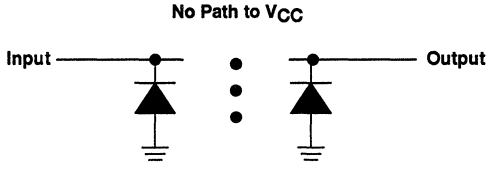


Figure 6. No ABT Current Flow When V_{CC} = 0 V

The second solution is to use the Texas Instruments crossbar technology (CBT) family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot-card insertion. It has a built-in channel pullup tied to a bias voltage (BIAS V) that is provided to ensure power up such that the buses are not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

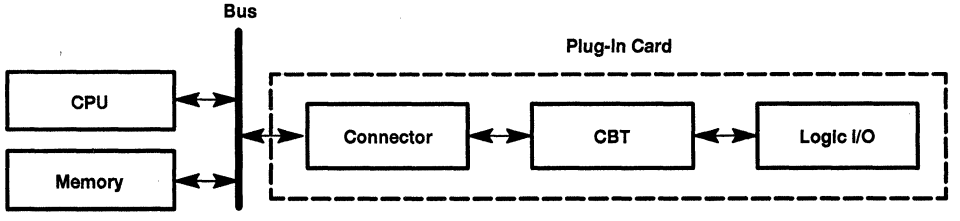
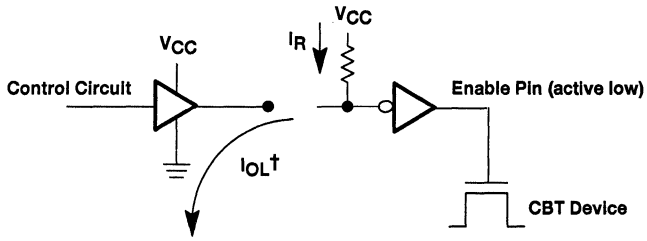


Figure 7. Hot-Card Insertion Application



† $I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple N-channel transistors, they are capable of providing several important bus functions, such as hot-card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

Characterization Information 13

LVT Family Characteristics

Ken Ristow
Advanced System Logic – Semiconductor Group

TEXAS INSTRUMENTS

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Printed in the U.S.A.

Introduction

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed-mode operation. The LVT series of parts rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures which support live insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = −32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CCL} \leq 15$ mA
$I_{CCH} \leq 200$ µA
$I_{CCZ} \leq 200$ µA

Propagation delays of:
$t_{pd} < 4.6$ ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface mount packaging support including fine-pitch packages:
48-/56-pin SSOP and TSSOP for LVT Widebus™
20-/24-pin SOIC and TSSOP for standard LVT

LVT Input/Output Characteristics

Figure 1 shows a simplified LVT output and illustrates the mixed-mode-signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), and provide the dc drive needed for existing 5-V backplanes. This allows for a simple solution to reduce system power via the migration to 3.3-V operation.

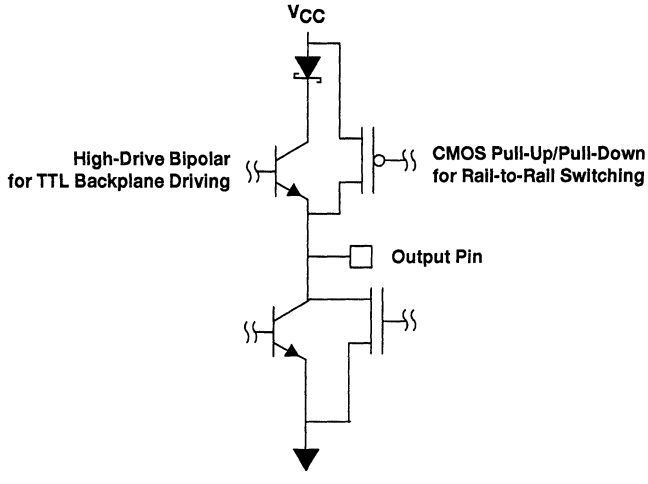


Figure 1. Simplified LVT Output Structure

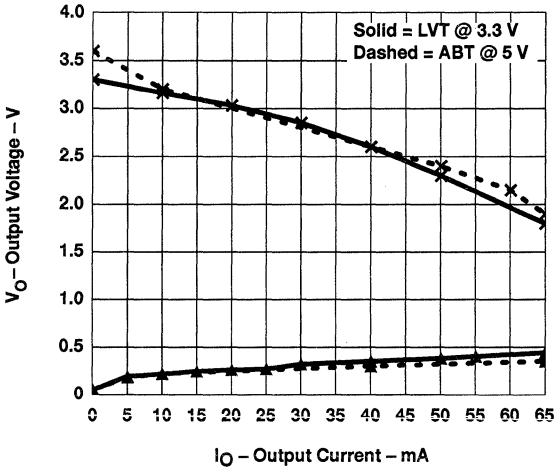


Figure 2. ABT vs LVT Output-Drive Comparison

Not only can LVT devices operate as 3-V to 5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 V to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or those which require live insertion.

Bus Hold

Many times, devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ±100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ±500 μA, to toggle the state of the input. This current is trivial when compared to the tens of mA of current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live-insertion or partial-power applications, while providing for low-input leakage currents. The outputs are capable of driving today's 5-V backplanes, with a considerable reduction in device power consumption, as well as being packaged in state-of-the-art fine-pitch surface-mount packages.

'LVT244 Characteristics

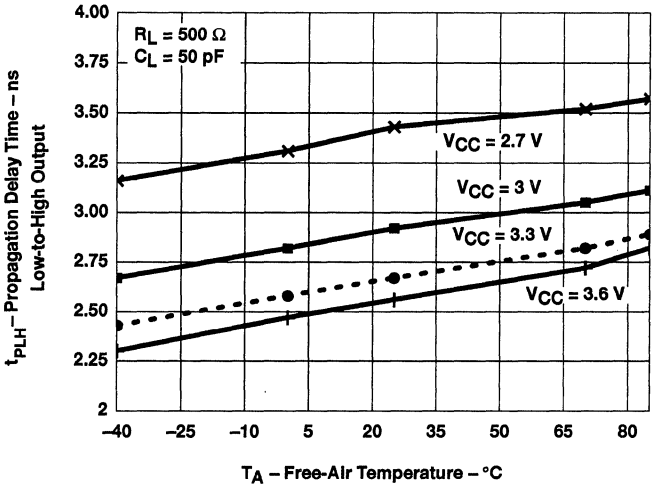


Figure 3. Propagation Delay vs Free-Air Temperature

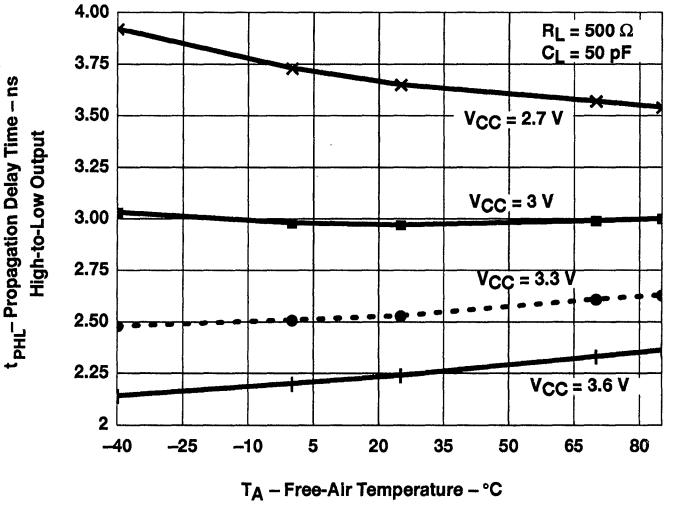


Figure 4. Propagation Delay vs Free-Air Temperature

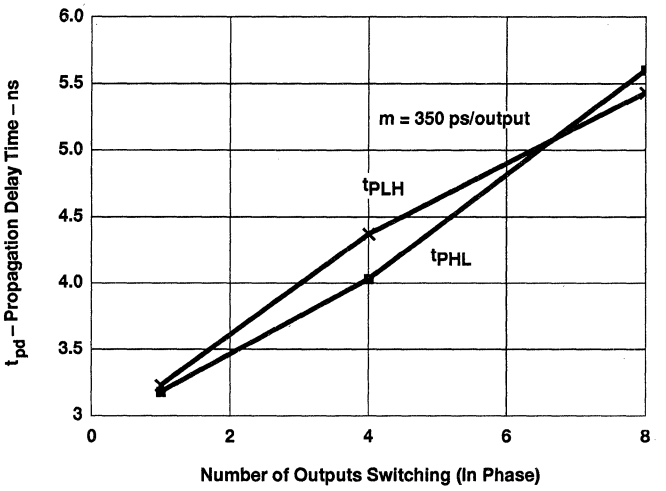


Figure 5. Propagation Delay vs Outputs Switching

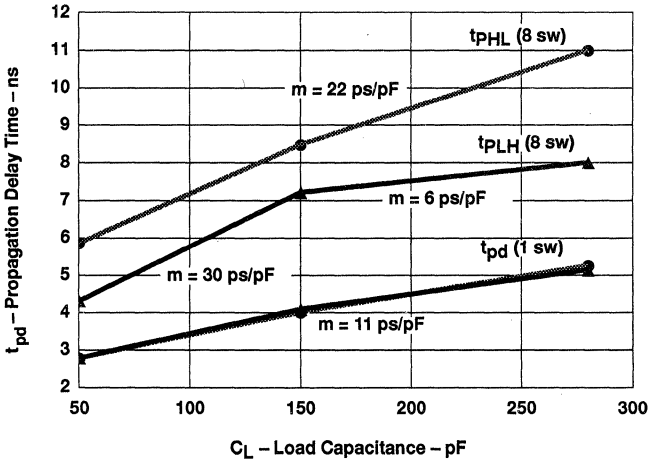


Figure 6. Propagation Delay vs Load Capacitance

'LVT244 Typical dc Characteristics

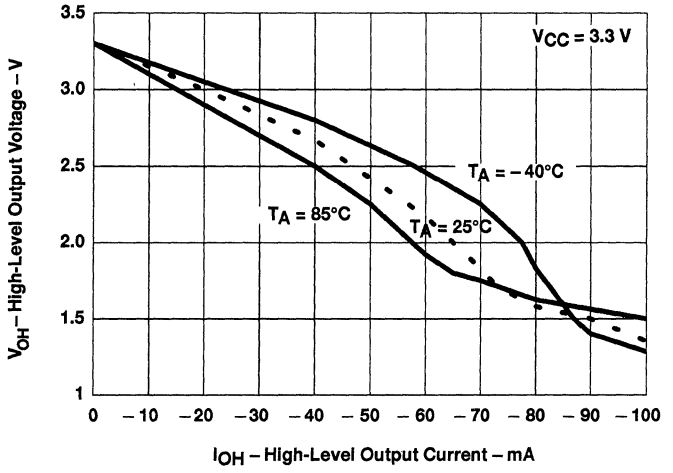


Figure 7. High-Level Output Voltage vs High-Level Output Current

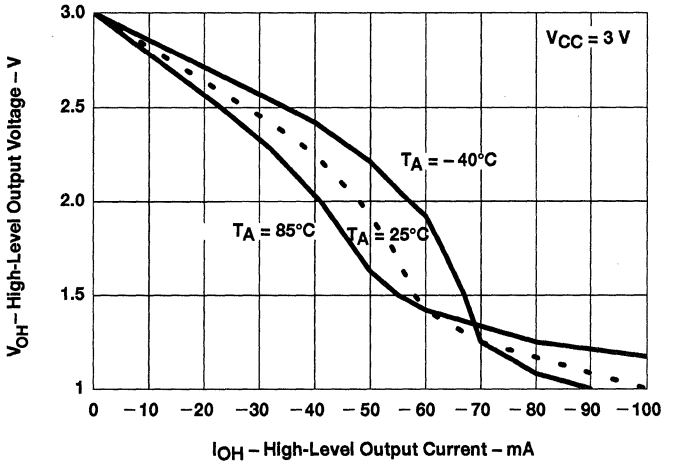


Figure 8. High-Level Output Voltage vs High-Level Output Current

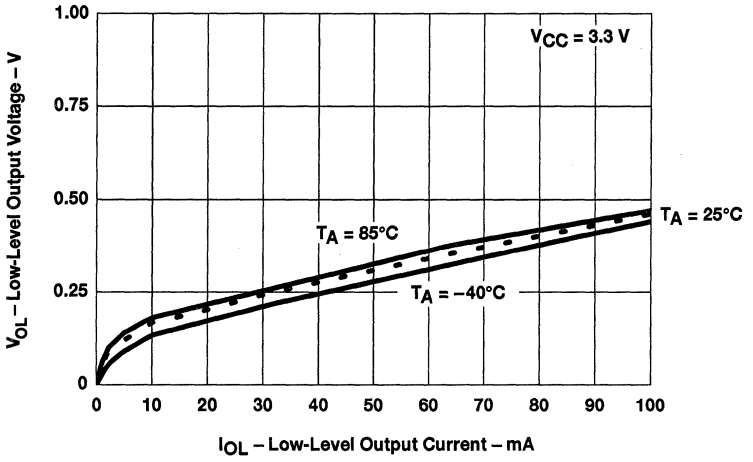


Figure 9. Low-Level Output Voltage vs Low-Level Output Current

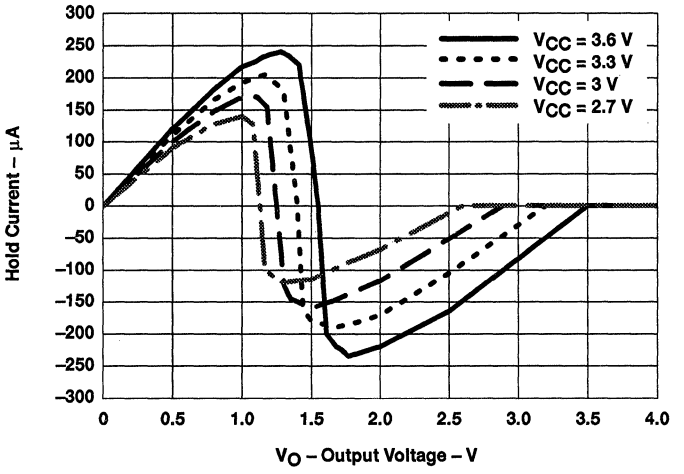


Figure 10. Hold Current vs Output Voltage

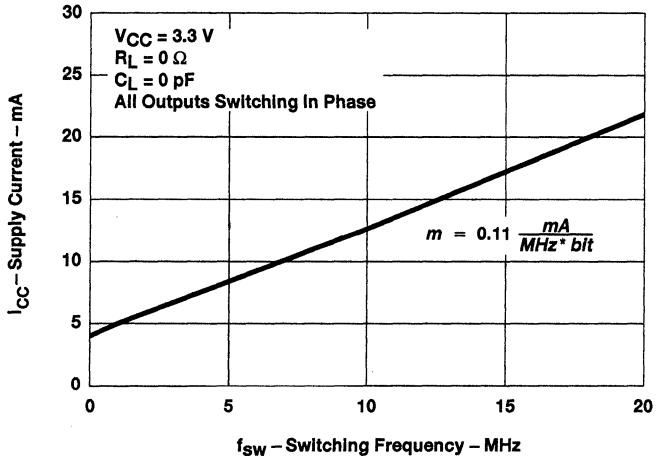


Figure 11. Supply Current vs Switching Frequency

Unloaded t_r and t_f Rates

The circuit shown below was used to measure the unloaded transition rates of the output.

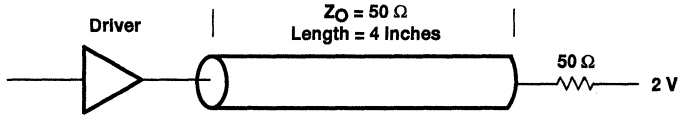


Figure 12. Load Circuit

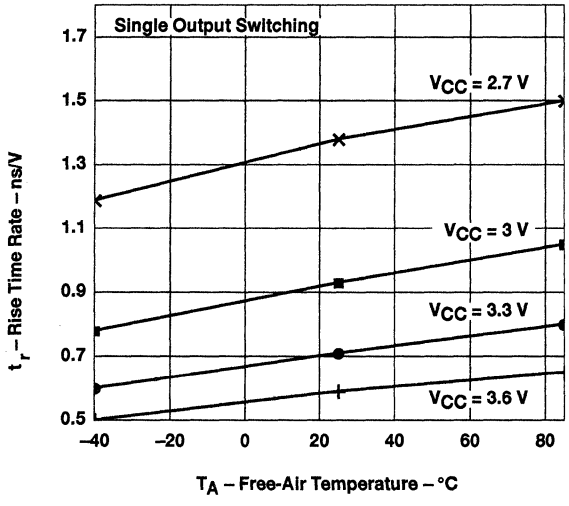


Figure 13. Rise Time Rate vs Free-Air Temperature

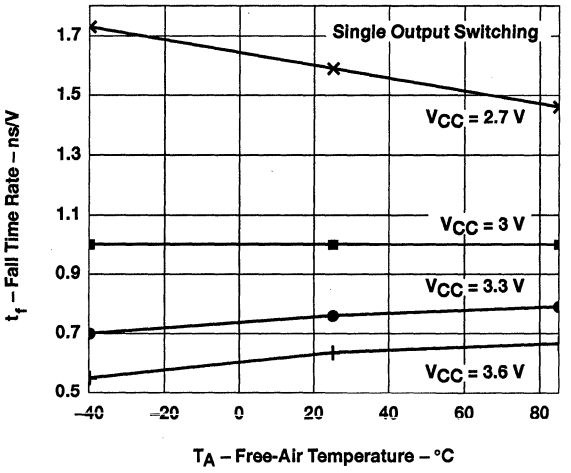


Figure 14. Fall Time Rate vs Free-Air Temperature

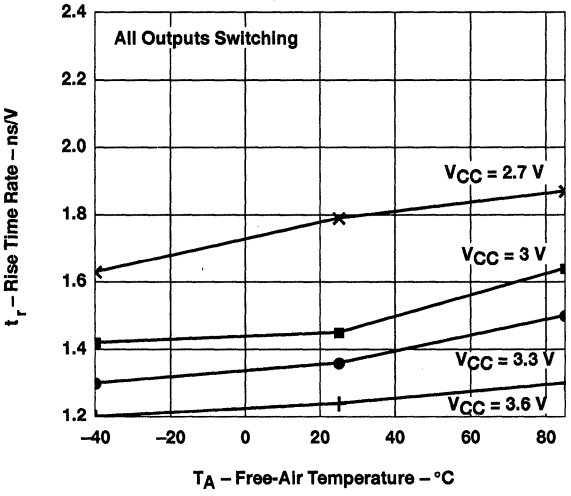


Figure 15. Rise Time Rate vs Free-Air Temperature

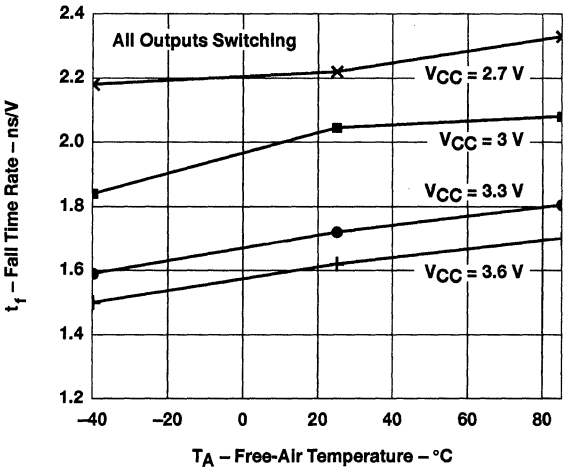


Figure 16. Fall Time Rate vs Free-Air Temperature

'LVT646 Characteristics

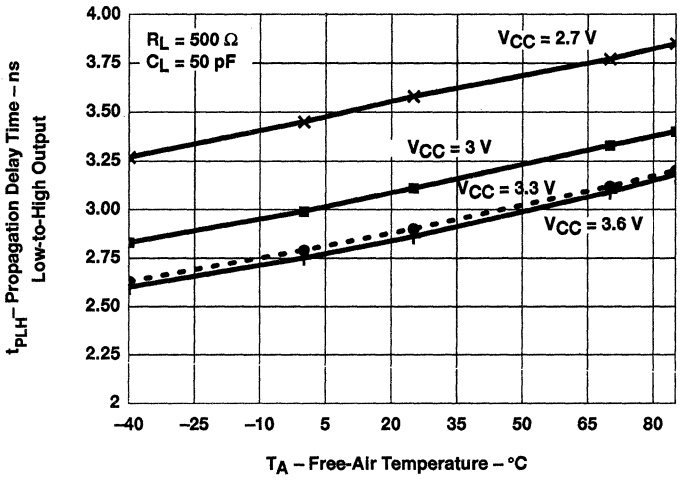


Figure 17. Thru-Mode Propagation Delay vs Free-Air Temperature

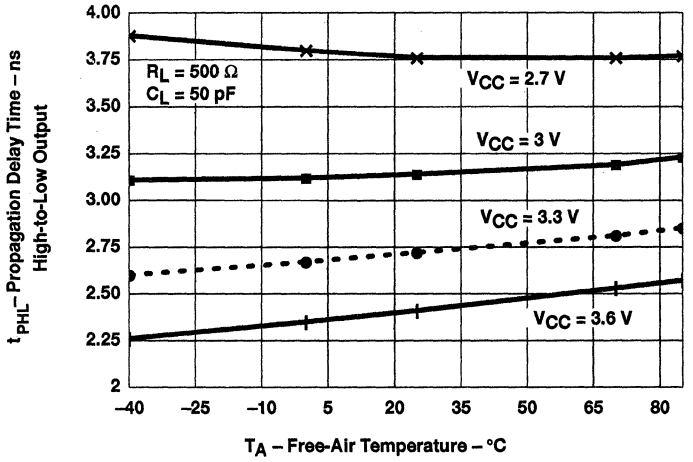


Figure 18. Thru-Mode Propagation Delay vs Free-Air Temperature

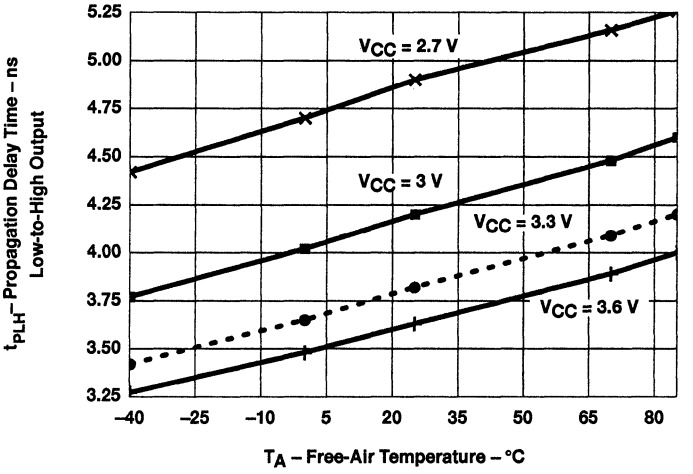


Figure 19. Clock-to-Q Propagation Delay vs Free-Air Temperature

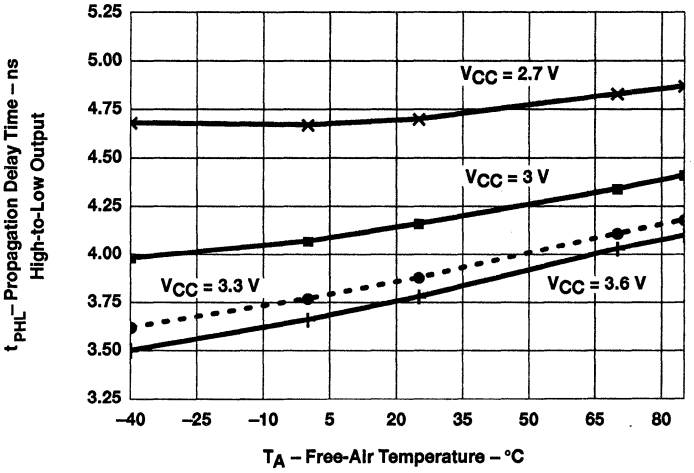


Figure 20. Clock-to-Q Propagation Delay vs Free-Air Temperature

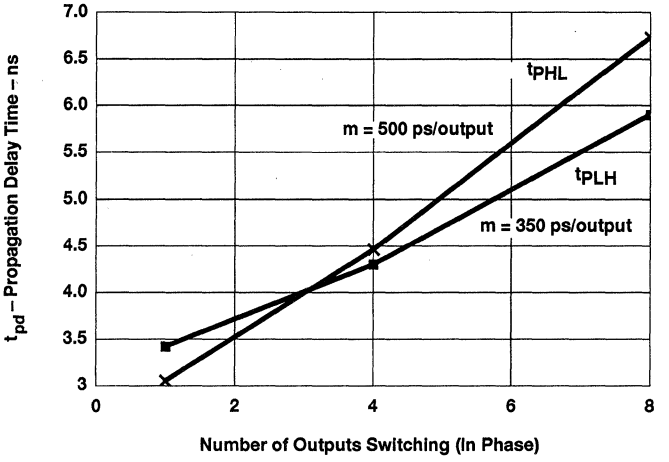


Figure 21. Propagation Delay vs Outputs Switching

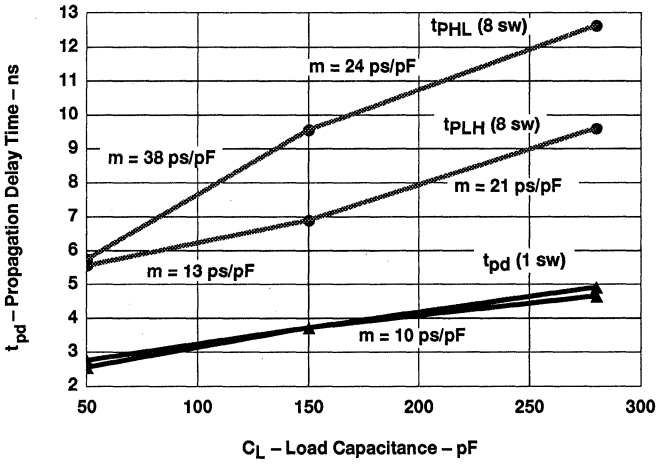
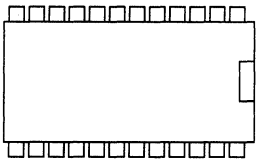


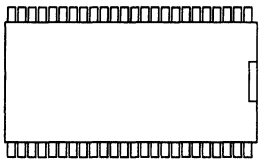
Figure 22. Propagation Delay vs Load Capacitance

Packaging Options

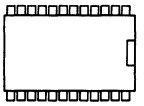


24-Pin SOIC (DW)†
Area = 165 mm^2
Height = 2.65 mm
Lead pitch = 1.27 mm

Widebus™

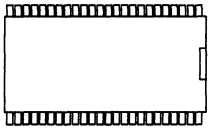


48-Pin SSOP (DL)†
Area = 171 mm^2
Height = 2.74 mm
Lead pitch = 0.635 mm



24-Pin TSSOP (PW)†
Area = 54 mm^2
Height = 1.1 mm
Lead Pitch = 0.65 mm

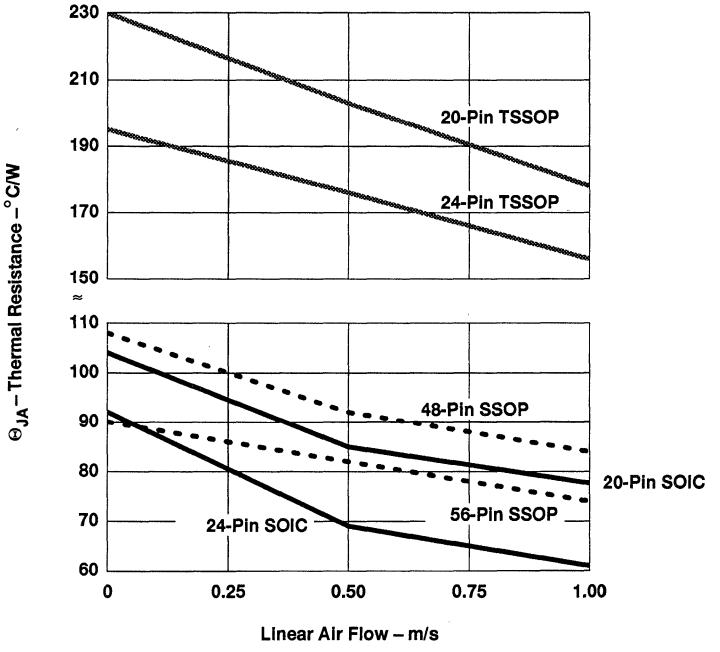
Shrink Widebus™



48-Pin TSSOP (DGG)†
Area = 108 mm^2
Height = 1.1 mm
Lead Pitch = 0.5 mm

† TI package designators

Thermal Characteristics

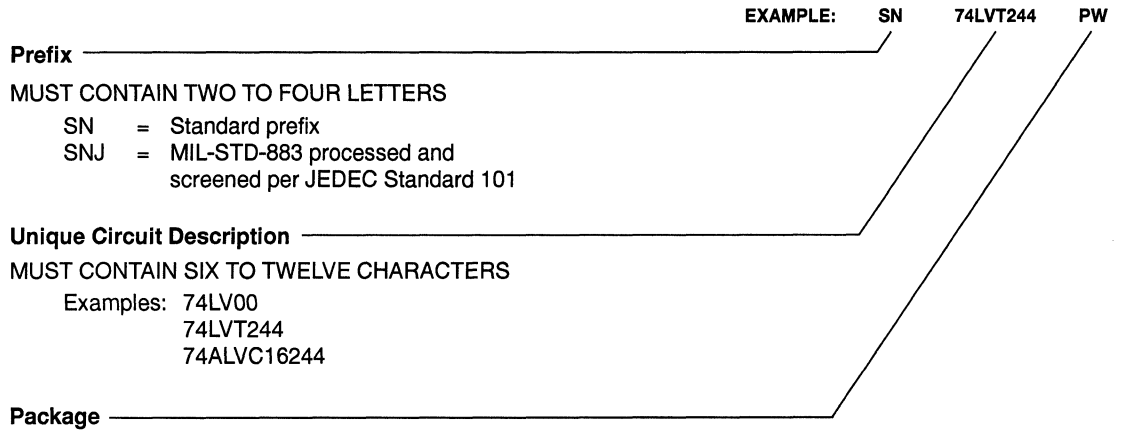


Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated.

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

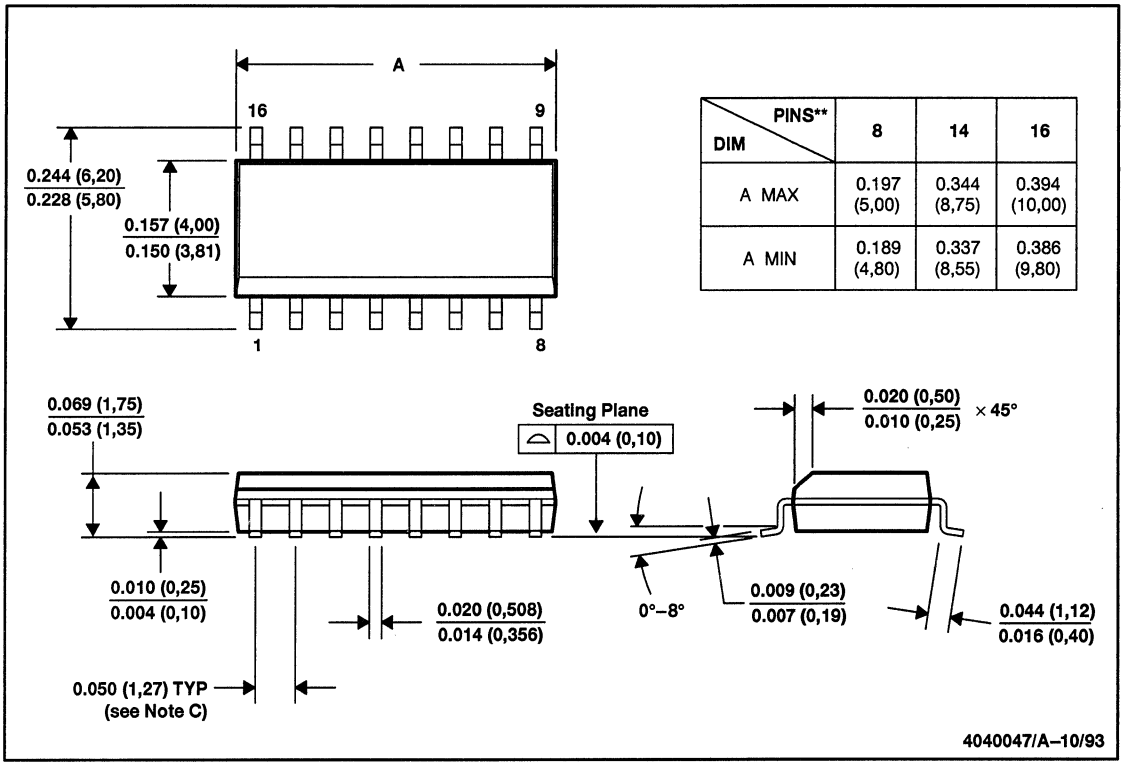
Factory orders for circuits described in this catalog should include a three-part type number as explained in the following example.



D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16 PIN SHOWN



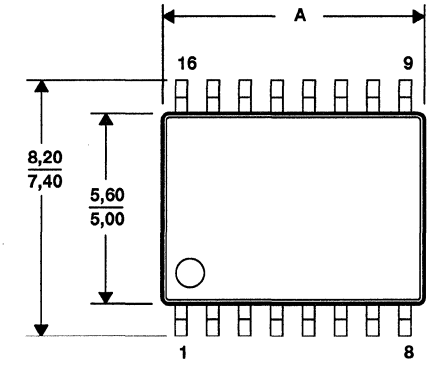
DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

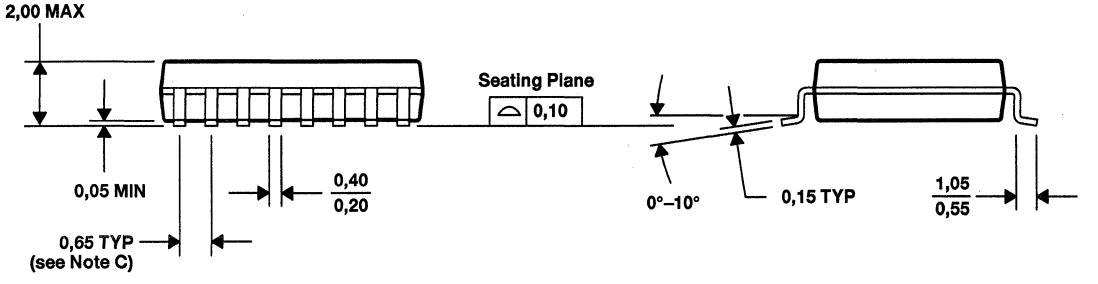
DB/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



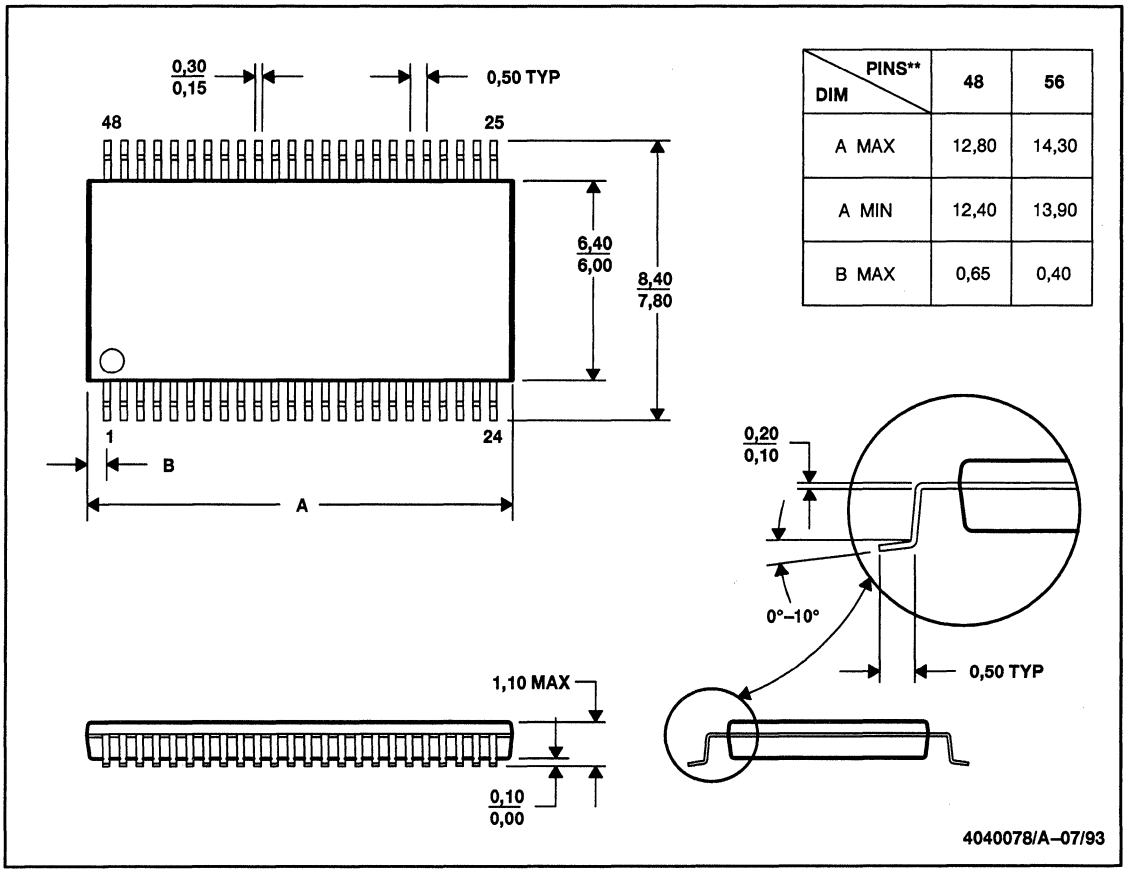
DIM \ PINS**	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30



4040065/A–10/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

DGG/R-PDSO-G** **300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE**

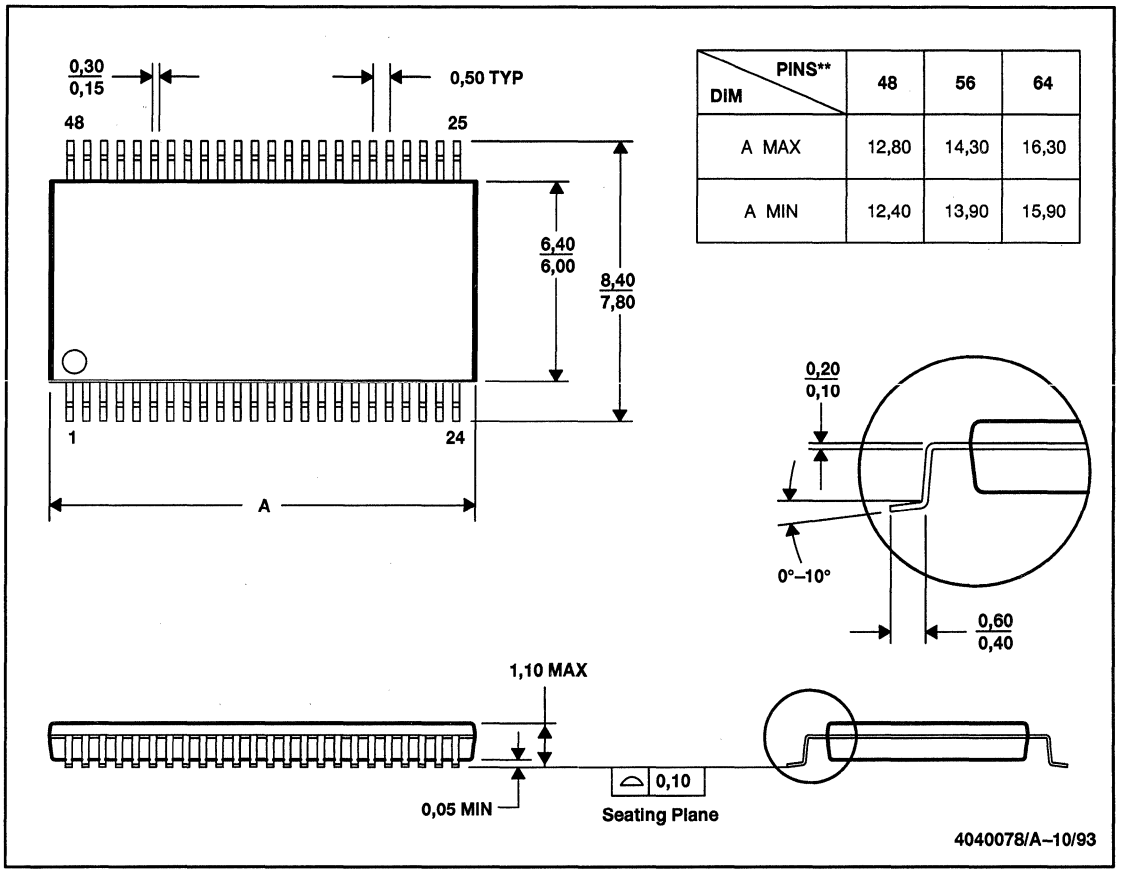


DIM \ PINS**	48	56
A MAX	12,80	14,30
A MIN	12,40	13,90
B MAX	0,65	0,40

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

DGG/R-PDSO-G**
48 PIN SHOWN

THIN SHRINK SMALL-OUTLINE PACKAGE



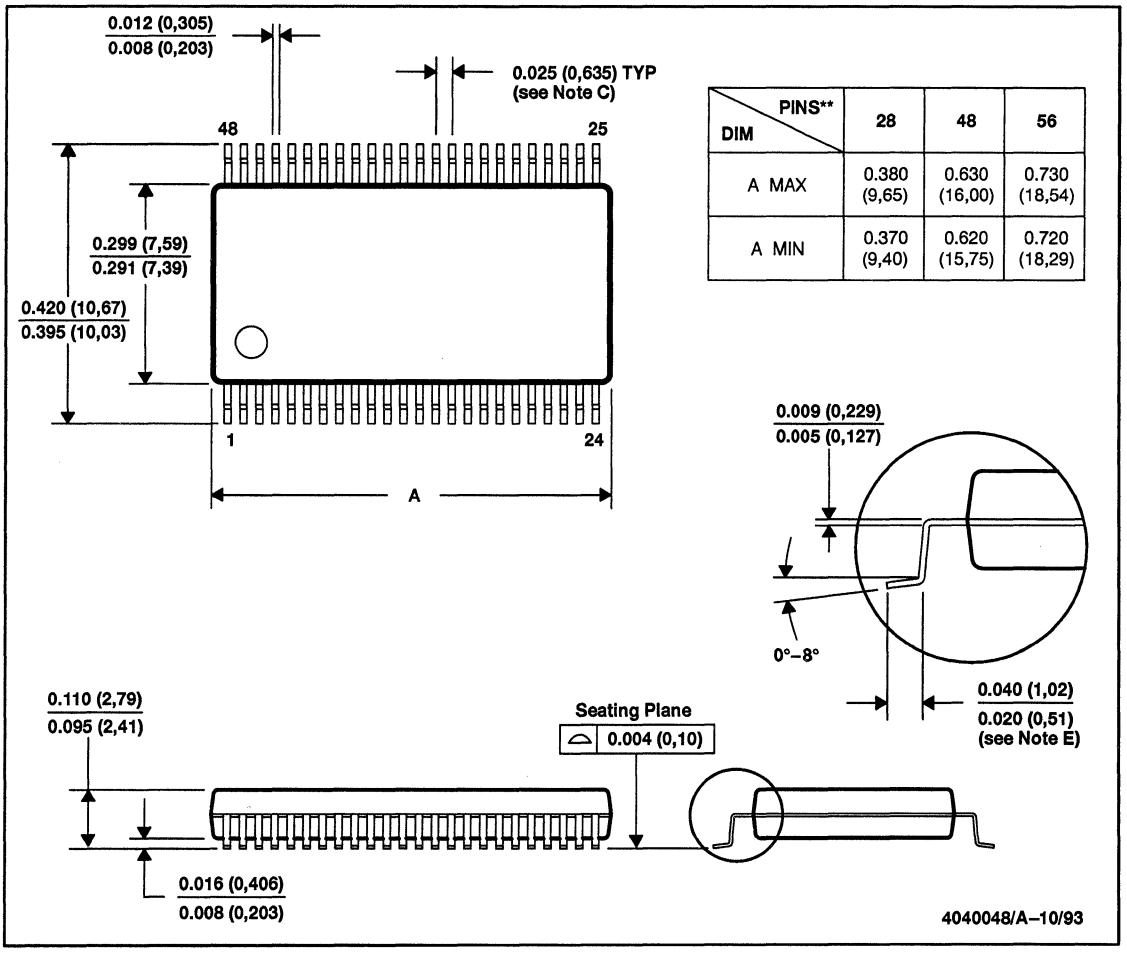
DIM \ PINS**	48	56	64
A MAX	12,80	14,30	16,30
A MIN	12,40	13,90	15,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

DL/R-PDSO-G**

PLASTIC SHRINK SMALL-OUTLINE PACKAGE

48 PIN SHOWN

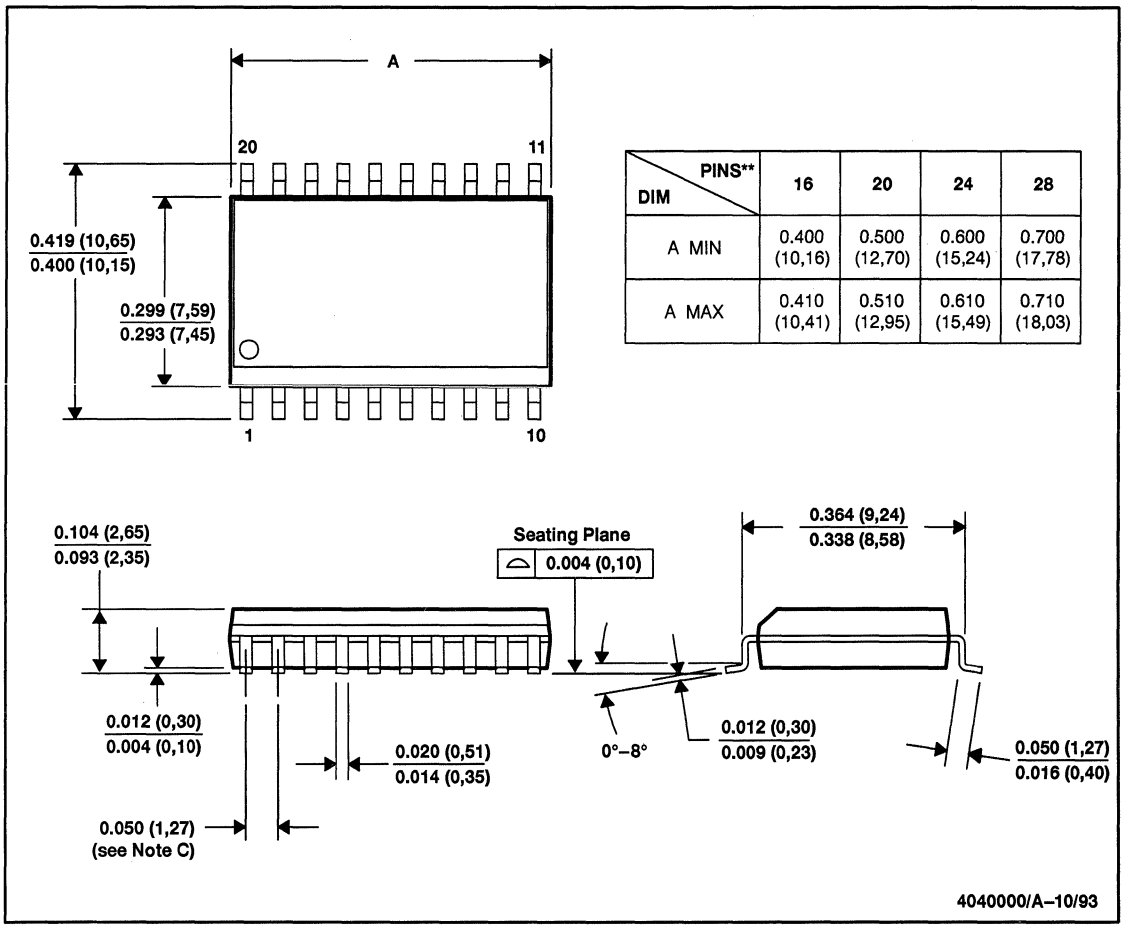


DIM \ PINS**	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion, which does not exceed 0.006 (0,15).
E. Foot length measured from lead top to point 0.010 (0.2,54) above seating plane.

DW/R-PDSO-G**
20 PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

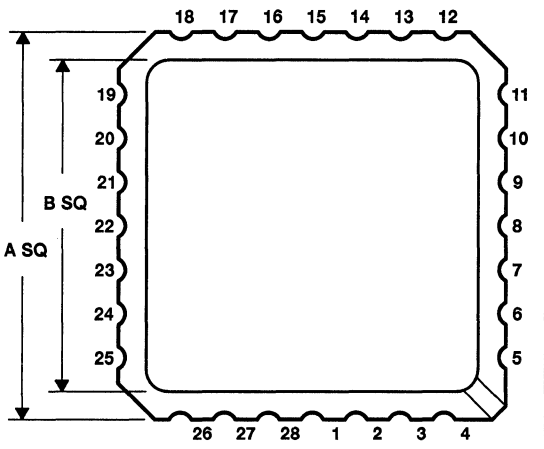


DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

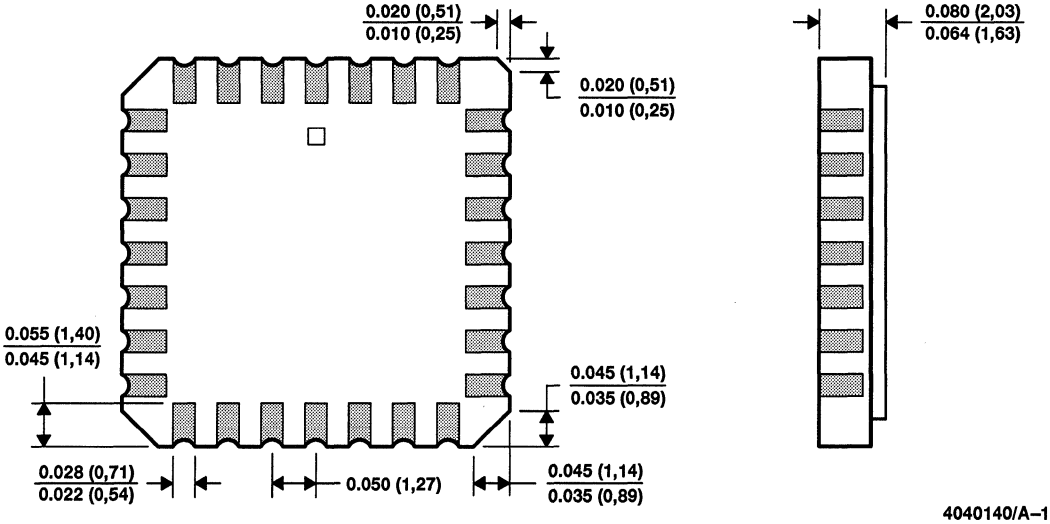
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).

FK/S-CQCC-N**
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER PACKAGE



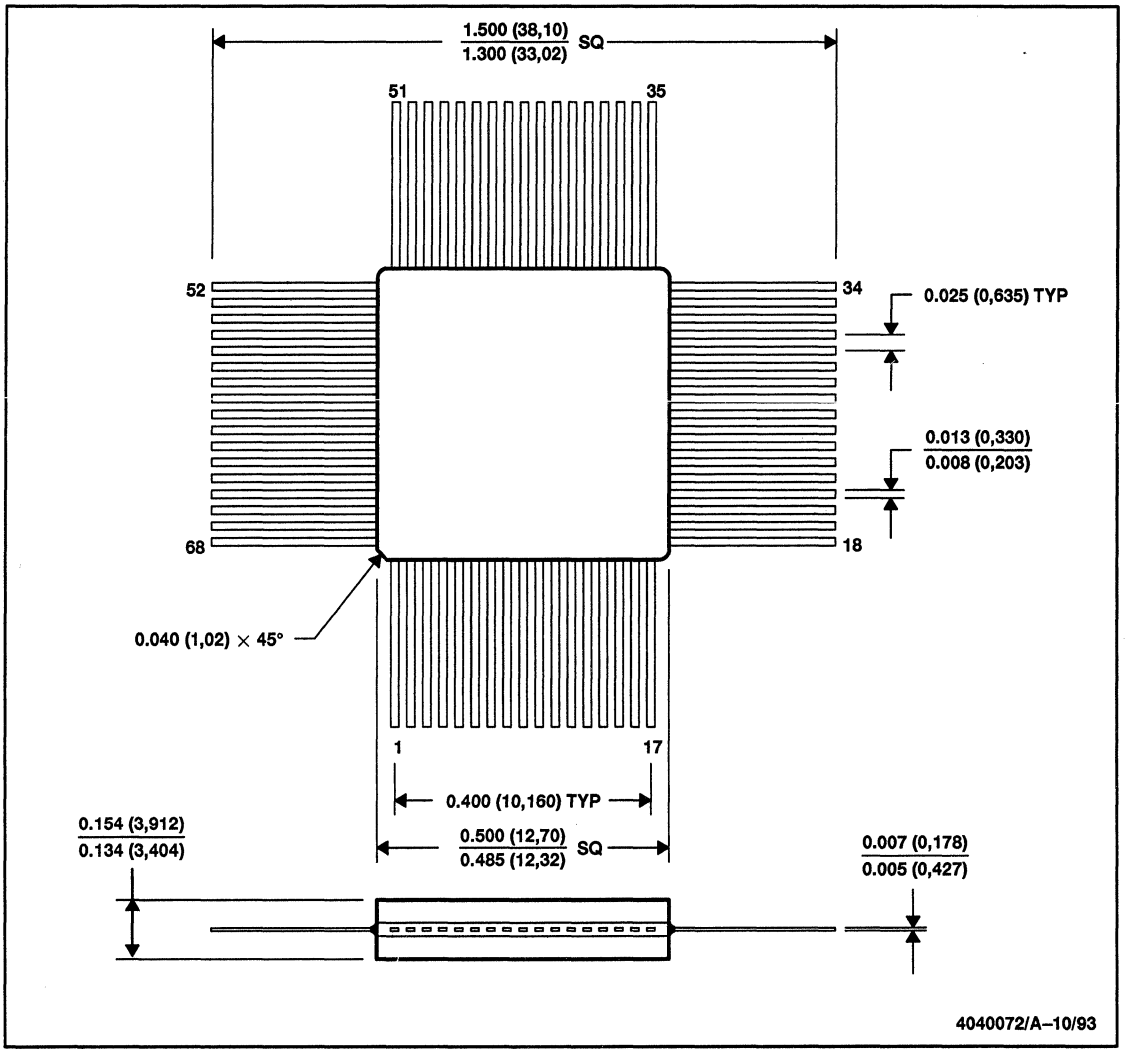
JEDEC OUTLINE DESIGNATION	NUMBER OF TERMINALS**	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
MS004CE	52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
MS004CF	68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
MS004CG	84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Three-layer ceramic base with a metal lid and braze seal.
D. FK package terminal assignments conform to JEDEC Standards 1, 2, and 11.
E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.

HV/S-GDFP-F68 **CERAMIC QUAD FLATPACK**

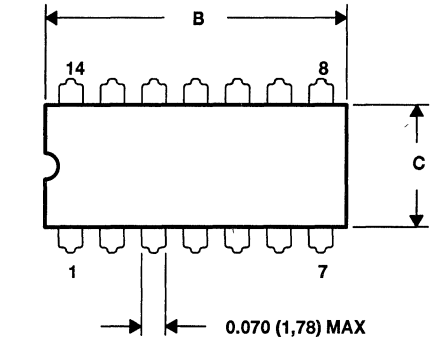


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

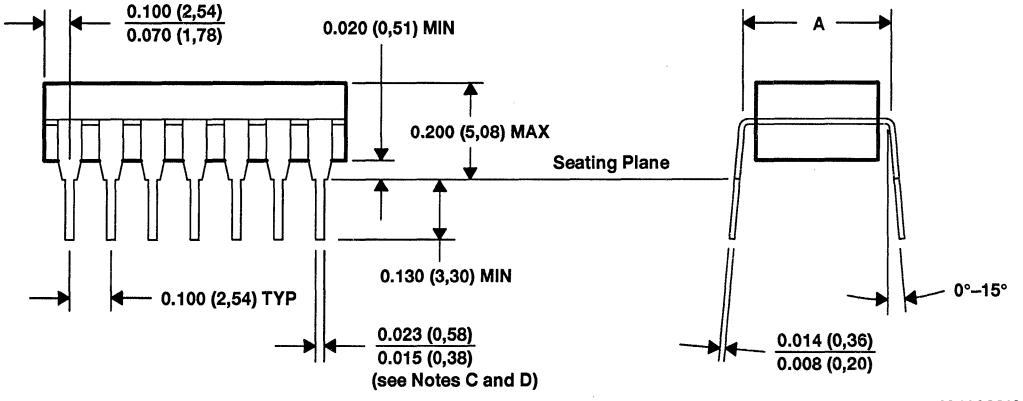
J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



DIM \ PINS**	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



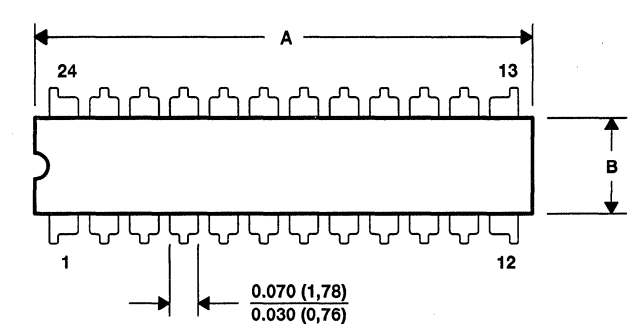
4040083/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This dimension does not apply for solder-dipped leads.
D. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

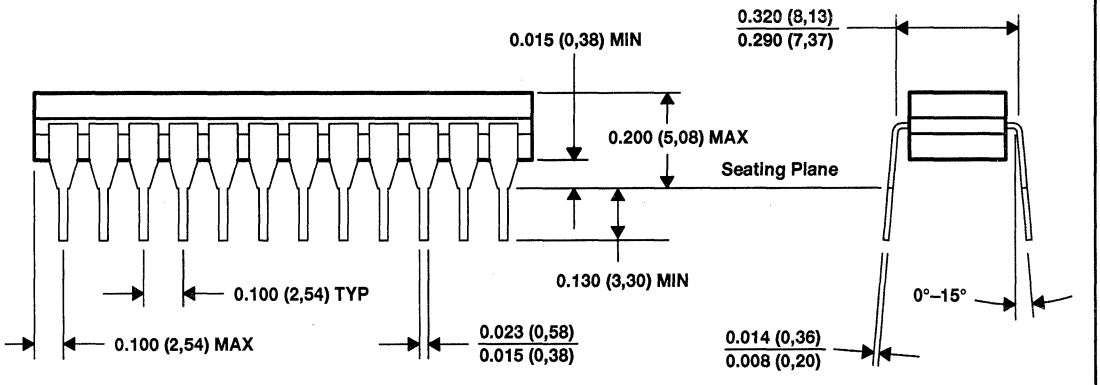
JT/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



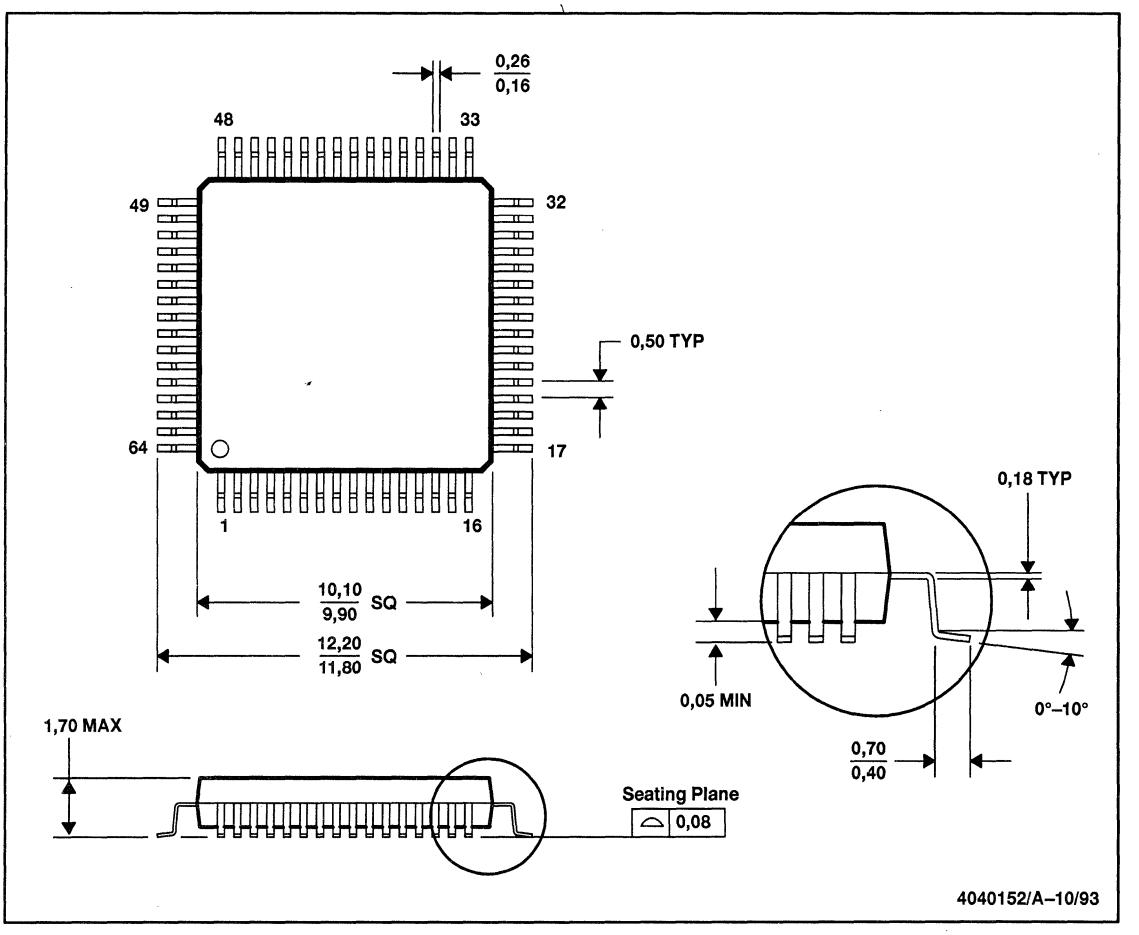
DIM \ PINS**	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)



4040110/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is glass sealed.

PM/S-PQFP-G64 **PLASTIC QUAD FLATPACK**

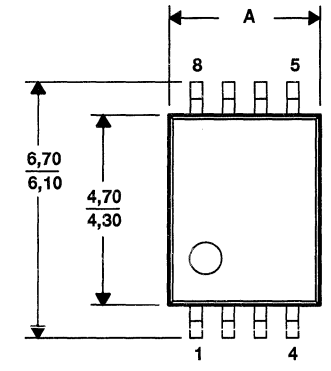


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

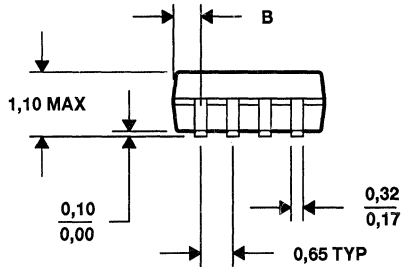
PW/R-PDSO-G**

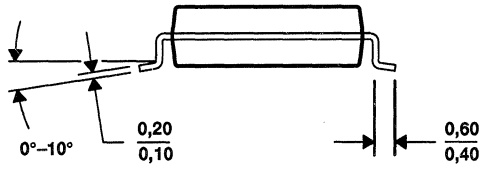
PLASTIC SMALL-OUTLINE PACKAGE

8 PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
B MAX	0,65	0,70	0,38	0,48	0,48	0,78





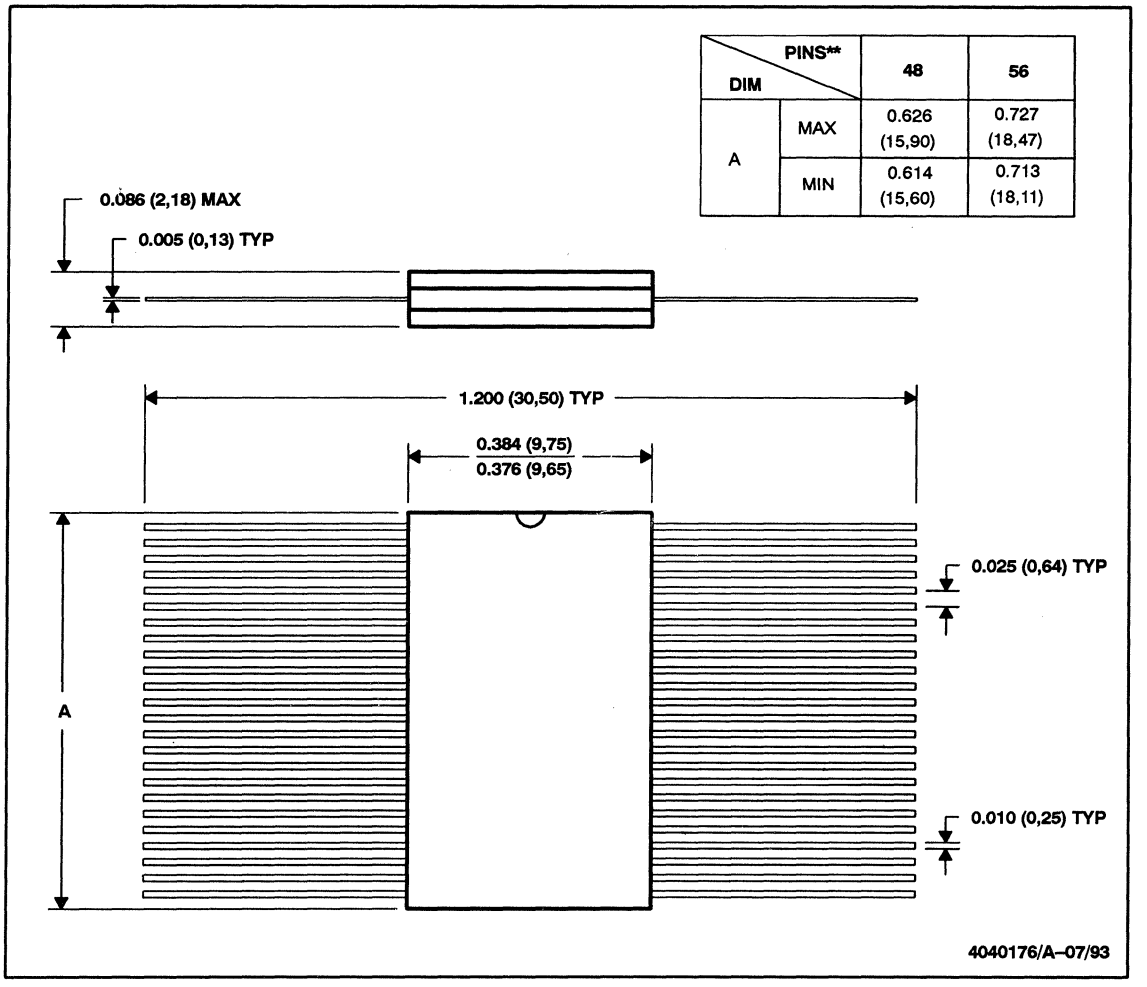
4040064/A–07/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package Handbook, 1990

WD/R-GDFP-F**

CERAMIC FLAT PACKAGE

4 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

NOTES

NOTES

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