Texas Instruments

Supplement to the Linear Circuits

3-V Family

Data Book

1995

Linear Products

Data Book

Supplement to the Linear Circuits
3-V Family

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3-V Family

TEXAS INSTRUMENTS

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INTRODUCTION

Texas Instruments offers the industry's first dedicated family of linear integrated circuits (ICs) that are specifically designed, characterized, and tested for operation at 3.3 V or less. This supplement to the 3-V data book includes a pulse-width-modulation control circuit, operational amplifiers a p-channel MOSFET, power distribution switches, voltage regulators, a driver/receiver, a universal asynchronous receiver transmitter, audio processors, light-to-frequency converters, and optical sensors.

While this manual offers information only on the 3-V analog devices available now from Texas Instruments, complete technical data for upcoming 3-V devices or any other TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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pulse-width-modulation control circuit

DEVICE	V_{CC} (V)		T_A (°C)		$V_{I(FB)}$ (mV)	V_O (V)	I_O (mA)	R_t (kΩ)	f_{OSC} (kHz)	DESCRIPTION
	MIN	MAX	MIN	MAX	MAX	MAX	MAX	MAX	MAX	
TL5001C	3.6	40	−20	85	1.5	50	20	250	400	Pulse-width-modulation (PWM) control circuit
TL5001I	3.6	40	−40	85	1.5	50	20	250	400	Pulse-width-modulation (PWM) control circuit

operational amplifiers

DEVICE	V_{CC} (V)		V_{IO} (mV)	I_{DD} (μA)	CMRR (dB)	V_n (nV/√Hz)	SR (V/μs)	GBW (MHz)	DESCRIPTION
	MIN	MAX	MAX	MAX	TYP	TYP	TYP	TYP	
TLV2252	2.7	8	1.5	125	75	19	0.1	0.187	Dual, low noise, micropower, rail-to-rail
TLV2252A	2.7	8	0.85	125	77	19	0.1	0.187	Dual, precision, low noise, micropower, rail-to-rail
TLV2254	2.7	8	1.5	250	75	19	0.1	0.187	Quad, low noise, micropower, rail-to-rail
TLV2254A	2.7	8	0.85	250	77	19	0.1	0.187	Quad, precision, low noise, micropower, rail-to-rail

p-channel MOSFETs

DEVICE	V_{DS} (V)	$r_{DS(on)}$ (V_{GS} = −10 V) Ω	$r_{DS(on)}$ (V_{GS} = −4.5 V) Ω	$r_{DS(on)}$ (V_{GS} = −2.7 V) Ω	I_D (A)	DESCRIPTION
	MAX	TYP	TYP	TYP	MAX	
TPS1120	−15	0.18	0.291	0.606	±1.17	Dual p-channel enhancement-mode MOSFET

power-distribution switches

DEVICE	RECOMMENDED CONTINUOUS LOAD CURRENT (A)	SHORT-CIRCUIT OUTPUT CURRENT LIMIT T_A 25°C (A)	$V_{I(IN)}$ (V)		DESCRIPTION
	MAX	TYP	MIN	MAX	
TPS2010	0.2	0.4	−0.3	7	Power-distribution switch with thermal protection
TPS2011	0.6	1.2	−0.3	7	Power-distribution switch with thermal protection
TPS2012	1	2	−0.3	7	Power-distribution switch with thermal protection
TPS2013	1.5	2.6	−0.3	7	Power-distribution switch with thermal protection

voltage regulators

DEVICE	V_O (V)	I_O (mA)	I_O (mA)	DROPOUT VOLTAGE (mV)	TOLERANCE (±%)	DESCRIPTION
	TYP	MAX	TYP	MAX		
TPS7101Q	—	500	2	—	2	Programmable from 1.2 V to 9.75 V
TPS7133Q	3.3	500	2	400	2	Fixed 3.3 V, low dropout
TPS7148Q	4.85	500	2	250	2	Fixed 4.85 V, low dropout
TPS7150Q	5	500	2	230	2	Fixed 5 V, low dropout

drivers/receivers

DEVICE	APPLICATION	BUS I/O	DRIVERS/RECEIVERS PER PACKAGE	DESCRIPTION
SN75LV4735A	EIA/TIA Standard RS-232-E	Single ended	3/5	Multichannel RS232 line driver/receiver

UARTs

DEVICE	FUNCTION	DEVICE TYPE	DESCRIPTION
TL16PC564A	Single ACE Plus PCMCIA Interface Logic With FIFO	TL16C450 Mode at Reset With Selectable Normal TL16C500 Mode	PCMCIA UART

audio processors

DEVICE	V_{CC} (V)		I_O (mA)	I_O (mA)	COMPANDED MODE	LINEAR MODE	DESCRIPTION
	MIN	MAX	MAX	TYP			
TLV320AC36	2.7	5	7.5	6.2	8-bit word (μ-Law)	16-bit word	3-V voice-band audio processor
TLV320AC37	2.7	5	7.5	6.2	8-bit word (A-Law)	16-bit word	3-V voice-band audio processor

light-to-frequency converters

DEVICE	V_{DD} (V)		I_{DD} (μA)	NONLINEARITY ERROR at 100 kHz (%F.S.)	ABSOLUTE-OUTPUT-FREQUENCY TOLERANCES (±%)	DESCRIPTION
	MIN	MAX	MAX	TYP		
TSL230	2.7	6	3	0.2	20	Programmable light-to-frequency converter
TSL230A	2.7	6	3	0.2	10	Programmable light-to-frequency converter
TSL230B	2.7	6	3	0.2	5	Programmable light-to-frequency converter
TSL235	2.7	6	3	0.2	—	Light-to-frequency converter

optical sensors

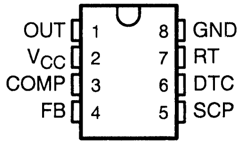
DEVICE	V_{DD} (V)		I_{DD} (μA)	N_e at $\lambda = 880$ nm [mV(μW/cm^2)]	DARK (OFFSET) VOLTAGE at $T_A = 25°C$ and $V_{DD} = 5$ V (mV)	DESCRIPTION
	MIN	MAX	TYP	TYP	MAX	
TSL250	3	9	900	80	10	Light-to-voltage optical sensor
TSL251	3	9	900	45	10	Light-to-voltage optical sensor
TSL252	3	9	900	7	10	Light-to-voltage optical sensor
TSL260	3	9	900	42	10	IR light-to-voltage optical sensor
TSL261	3	9	900	23	10	IR light-to-voltage optical sensor
TSL262	3	9	900	3.8	10	IR light-to-voltage optical sensor

TL5001C, TL5001I
PULSE-WIDTH-MODULATION CONTROL CIRCUIT

SLVS084B – APRIL 1994 – REVISED JANUARY 1995

- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 40 kHz to 400 kHz**
- **Variable Dead Time Provides Control Over Total Range**

D OR P PACKAGE
(TOP VIEW)



description

The TL5001 incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001 contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

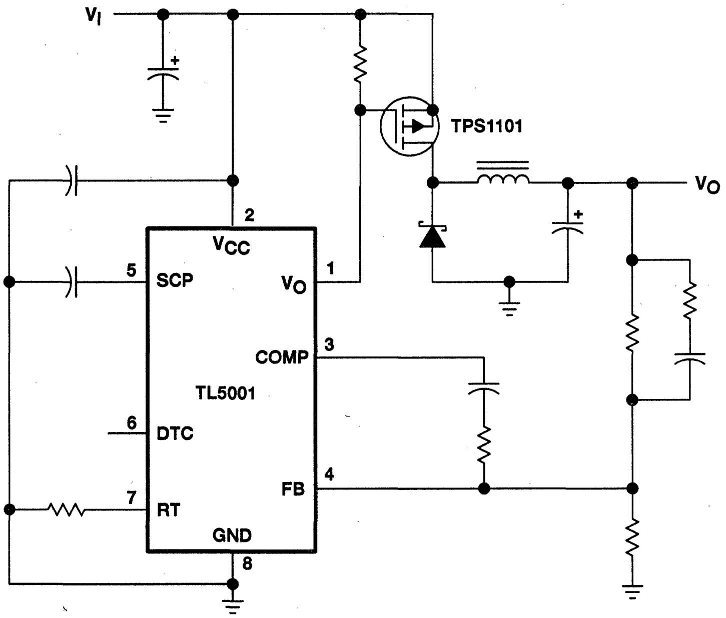
The TL5001C is characterized for operation from −20°C to 85°C. The TL5001I is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

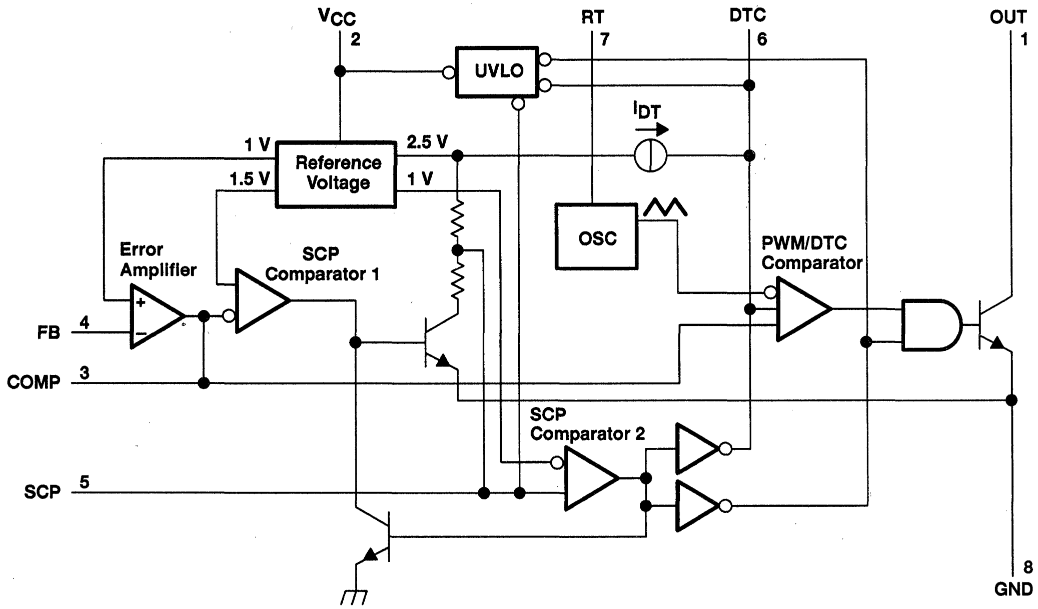
T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
−20°C to 85°C	TL5001CD	TL5001CP
−40°C to 85°C	TL5001ID	TL5001IP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR).

schematic for typical application



functional block diagram



detailed description

voltage reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001 and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input. The 1-V reference remains within 2% of nominal over the operating temperature range.

error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$V_O = (1 + R1/R2)\ (1\ V)$

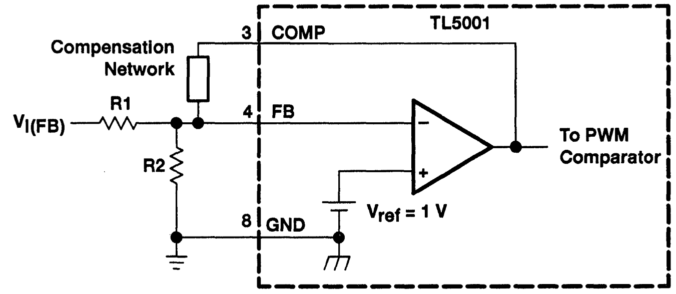


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45-µA, the total dc load resistance should be 100 kΩ or more.

oscillator/PWM

The oscillator frequency can be set between 40 kHz and 400 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown as Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off when the triangular wave is greater than the lesser of the two inputs.

dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100 percent, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0 percent when V_{DT} is 0.7 V or less and 100 percent when V_{DT} is 1.3 V or greater. Because the triangle-wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{max} and V_{min} are the maximum and minimum oscillator levels):

$$R_{DT} = \left(R_t + 1250\right)\left[D\left(V_{max} - V_{min}\right) + V_{min}\right]$$

where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT}\left(1-e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

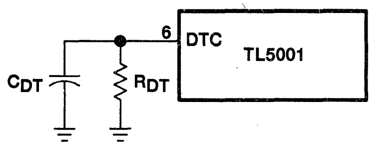


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5001 remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch when the supply voltage drops too low (approximately 3 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL5001 includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns the TL5001 output transistor off.

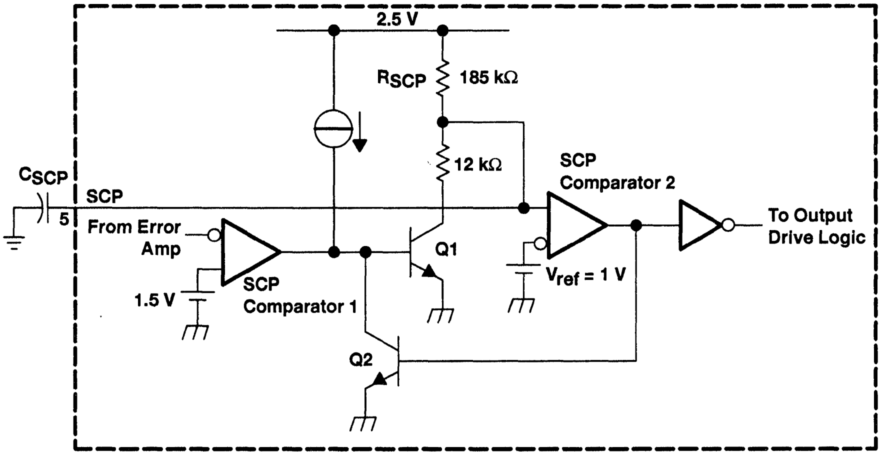


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (C_{SCP}) connected between the SCP terminal and ground towards 2.5 V through a 185-kΩ resistor (R_{SCP}). The circuit begins charging from an initial voltage of about 185 mV and times out when the capacitor voltage reaches 1 V and the output of SCP comparator 2 goes high, turns Q2 on, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5-0.185)\left(1-e^{-t/\tau}\right) + 0.185$$

where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period, t_{SCP}, occurs when $V_{SCP} = 1$ V. Solving for C_{SCP} yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

where

t is in seconds, C in µF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001 is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 41 V
Amplifier input voltage, $V_{I(FB)}$ .... 20 V
Output voltage, V_O, OUT .... 51 V
Output current, I_O, OUT .... 21 mA
Output peak current, $I_{O(peak)}$, OUT .... 100 mA
Continuous total power dissipation .... See Dissipation Rating Table
Operating ambient temperature range, T_A: TL5001C .... –20°C to 85°C
TL5001I .... –40°C to 85°C
Storage temperature range .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	40	V
Amplifier input voltage, $V_{I(FB)}$		0	1.5	V
Output voltage, V_O, OUT			50	V
Output current, I_O, OUT			20	mA
COMP source current			45	µA
COMP dc load resistance		100		kΩ
Oscillator timing resistor, R_t		15	250	kΩ
Oscillator frequency, f_{osc}		40	400	kHz
Operating ambient temperature, T_A	TL5001C	–20	85	°C
	TL5001I	–40	85	

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 6$ V, $f_{osc} = 100$ kHz (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Output voltage	COMP connected to FB	0.95	1	1.05	V
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output voltage change with temperature	T_A = –20°C to 25°C (TL5001C)	–10	–1	10	mV/V
	T_A = –40°C to 25°C (TL5001I)	–10	–1	10	
	T_A = 25°C to 85°C	–10	–2	10	

‡ All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

undervoltage lockout

PARAMETER	MIN	TYP†	MAX	UNIT
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis	100	200		mV

short-circuit protection

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SCP threshold voltage	T_A = 25°C	0.95	1	1.05	V
SCP voltage, latched	No pullup	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120	mV
Timing resistance			185		kΩ
SCP comparator 1 threshold voltage			1.5		V

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	R_t = 100 kΩ		97		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature	T_A = −20°C to 25°C	−4	−0.4	4	kHz
	T_A = 25°C to 85°C	−4	−0.2	4	
Voltage at RT			1		V

dead-time control

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output (source) current		$0.9 \times I_{RT}$‡		$1.1 \times I_{RT}$	µA
Input threshold voltage	Duty cycle = 0%	0.5	0.7		V
	Duty cycle = 100%		1.3	1.5	

error amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input voltage		V_{CC} = 3.6 V to 40 V	0		1.5	V
Input bias current				−160	−500	nA
Output voltage swing	Positive		1.5	2.3		V
	Negative			0.3	0.4	V
Open-loop voltage amplification				80		dB
Unity-gain bandwidth				1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V	100	600		µA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V	−45	−90		µA

† All typical values are at T_A = 25°C.
‡ Output source current at RT

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

output

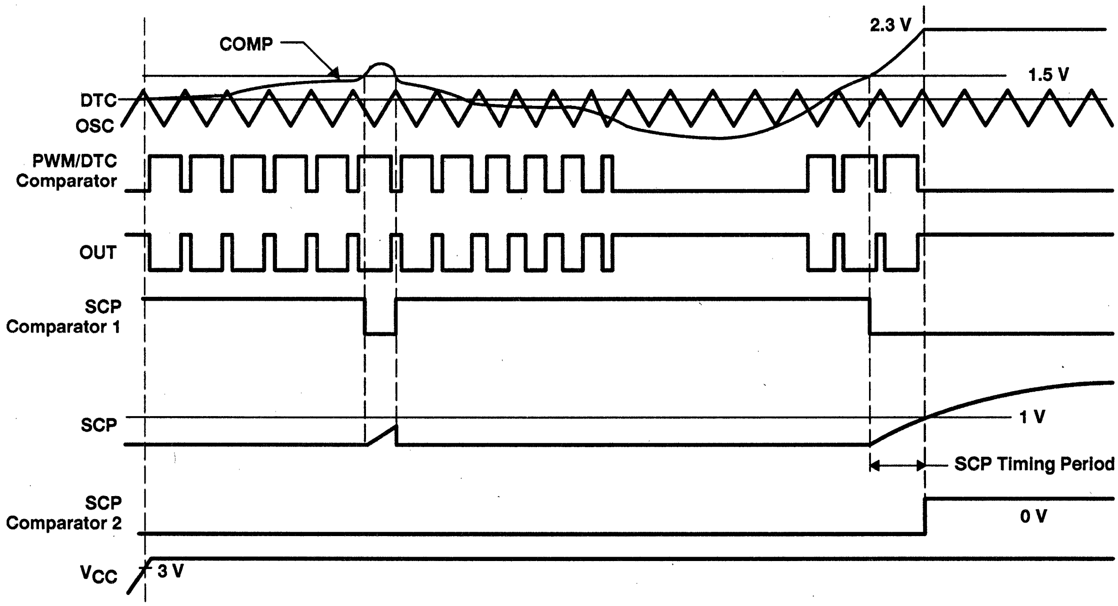
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output saturation voltage	I_O = 10 mA		1.5	2	V
Off-state current	V_O = 50 V, V_{CC} = 0			10	μA
	V_O = 50 V			10	
Short-circuit output current	V_O = 6 V		40		mA

total device

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Off state			1	1.5	mA
Average supply current		R_t = 100 kΩ		1.1	2.1	mA

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

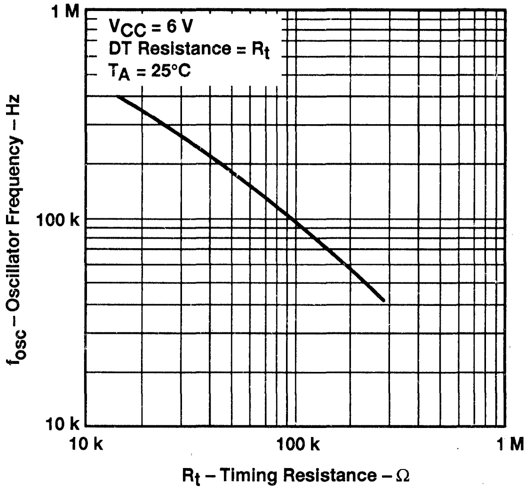


Figure 5

OSCILLATION FREQUENCY
vs
AMBIENT TEMPERATURE

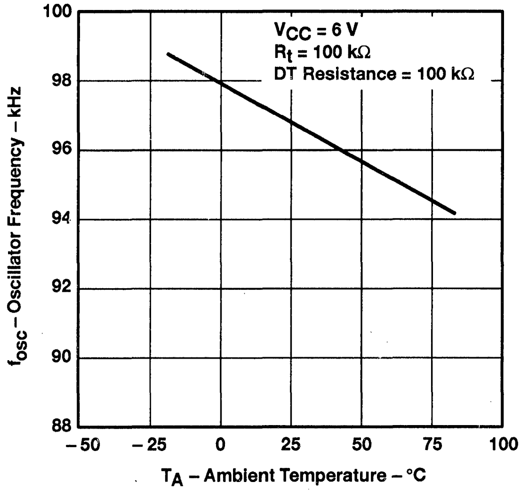


Figure 6

REFERENCE OUTPUT VOLTAGE
vs
POWER SUPPLY VOLTAGE

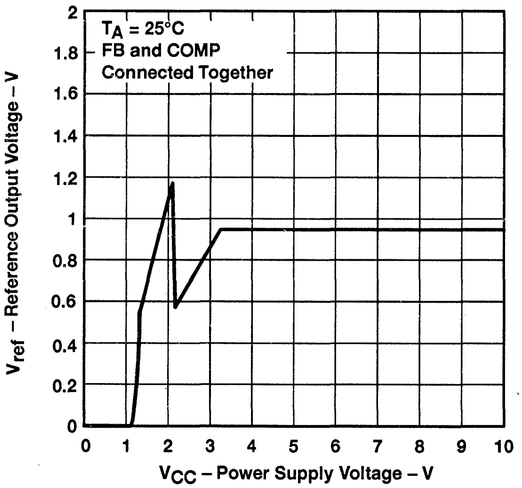


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION
vs
AMBIENT TEMPERATURE

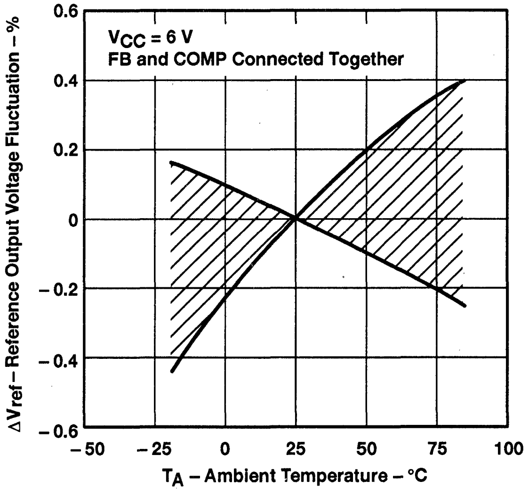


Figure 8

TYPICAL CHARACTERISTICS

**AVERAGE STANDBY CURRENT
vs
POWER SUPPLY VOLTAGE**

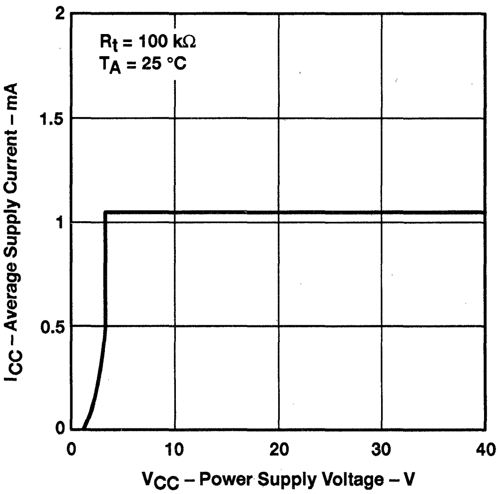


Figure 9

**AVERAGE SUPPLY CURRENT
vs
AMBIENT TEMPERATURE**

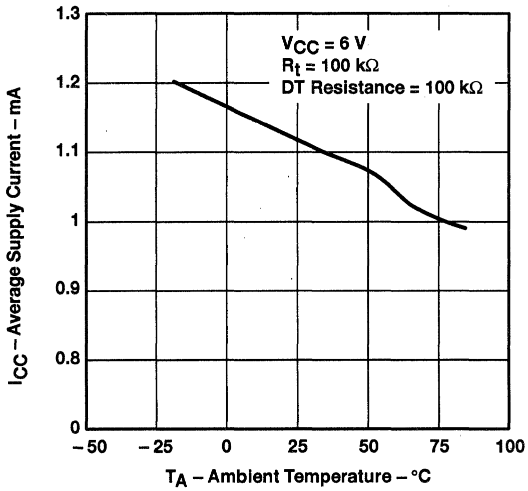


Figure 10

**PWM TRIANGLE WAVE AMPLITUDE VOLTAGE
vs
OSCILLATOR FREQUENCY**

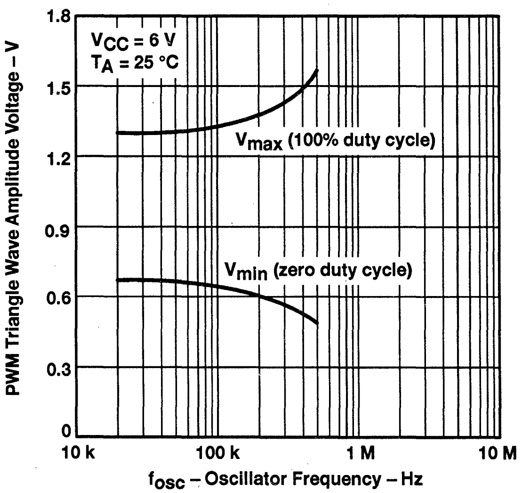


Figure 11

**ERROR AMPLIFIER OUTPUT VOLTAGE
vs
OUTPUT SINK CURRENT**

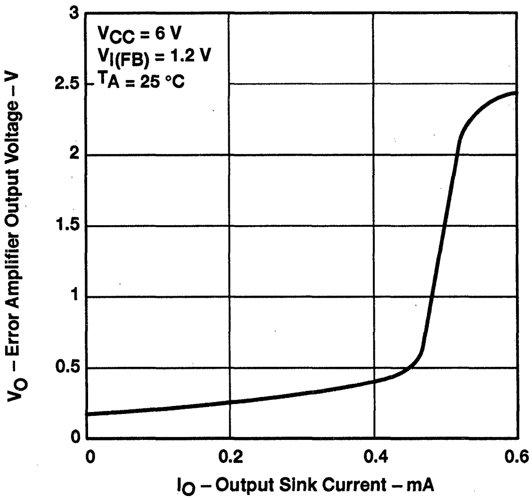


Figure 12

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

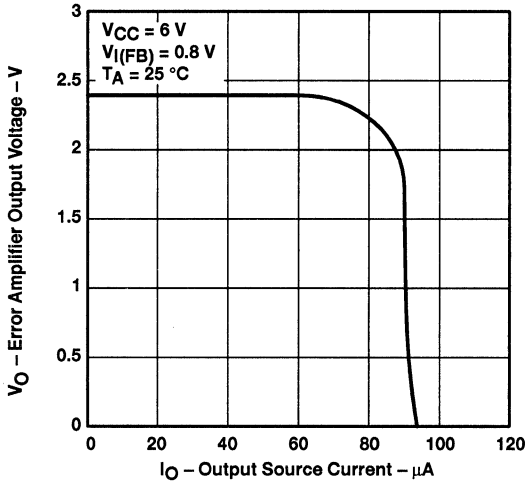


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

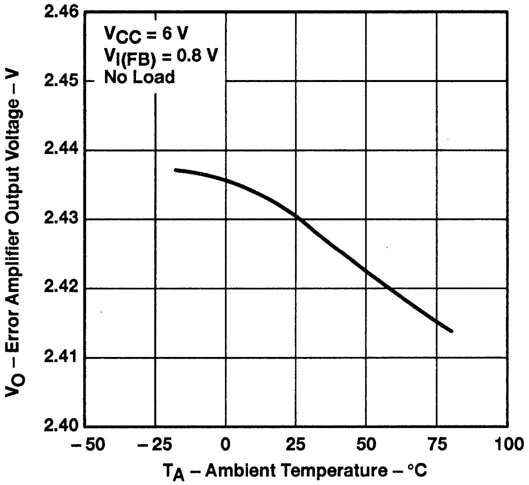


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

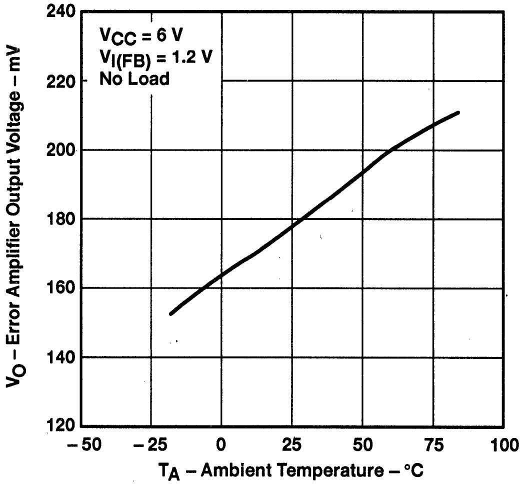


Figure 15

ERROR AMPLIFIER CLOSED-LOOP GAIN AND PHASE SHIFT vs OSCILLATOR FREQUENCY

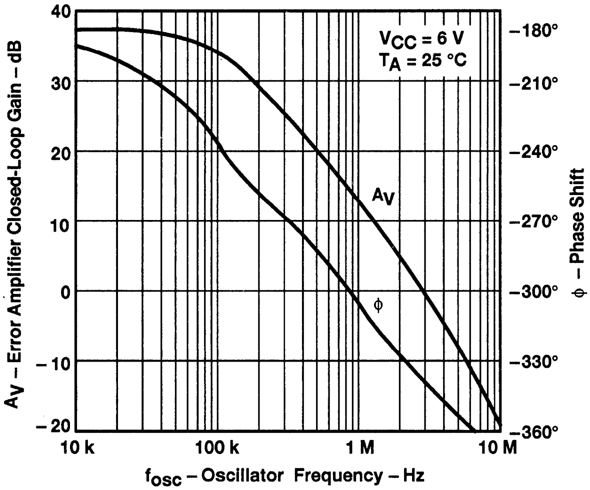


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT DUTY CYCLE vs DTC VOLTAGE

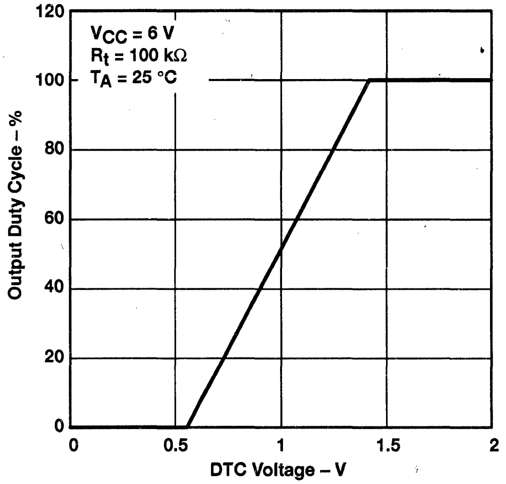


Figure 17

PROTECTION ENABLE TIME vs PROTECTION ENABLE CAPACITANCE

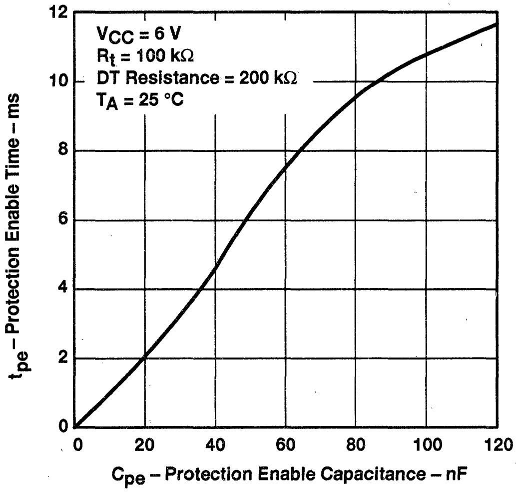


Figure 18

DTC OUTPUT CURRENT vs RT OUTPUT CURRENT

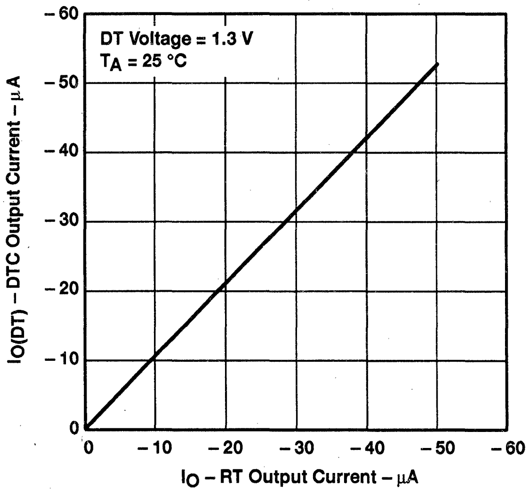


Figure 19

COLLECTOR SATURATION VOLTAGE vs OUTPUT SINK CURRENT

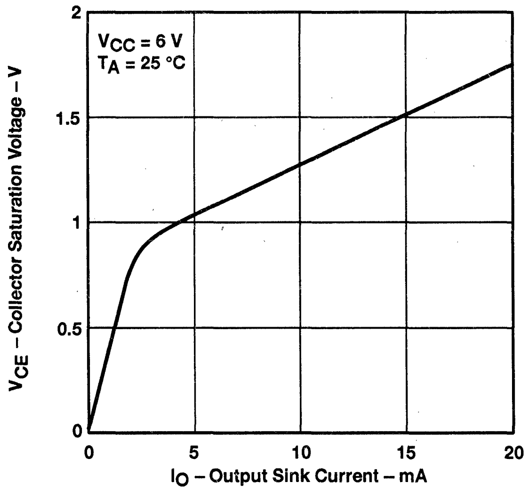
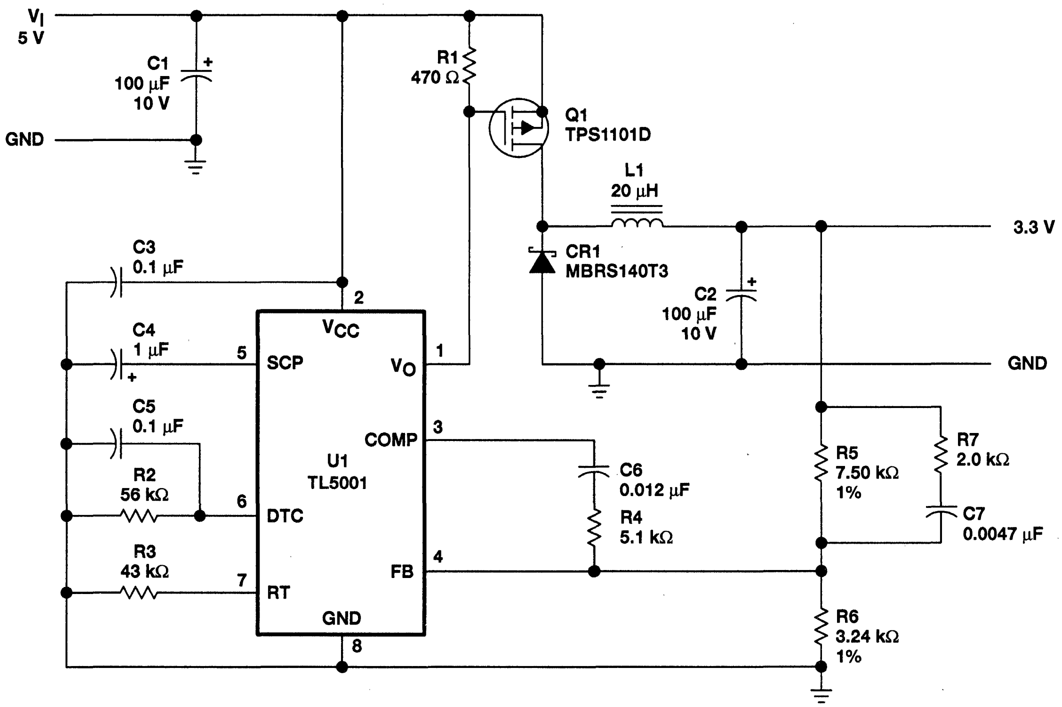


Figure 20

APPLICATION INFORMATION



NOTES: A. Frequency = 200 kHz
B. Duty cycle = 90% max
C. Soft-start time constant (TC) = 5.6 ms
D. SCP TC = 70 ms

Partial Bill of Materials:

U1	TL5001D	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T5O-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

Figure 21. Step-Down Converter

- Output Swing Includes Both Supply Rails
- Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Very Low Power . . . 34 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage 850 μV Max at T_A = 25°C
- Wide Supply Voltage Range 2.7 V to 8 V
- Macromodel Included

description

The TLV2252 and TLV2252A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μ-power dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2252 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 34 μA (typical) of supply current per amplifier, the TLV2252 family can achieve input offset voltage levels as low as 850 μV, outperforming existing CMOS amplifiers. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

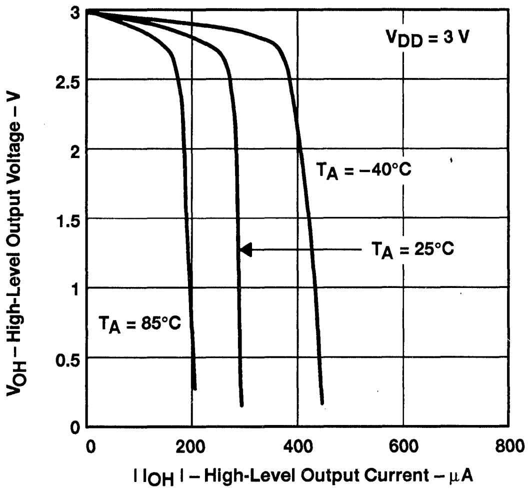


Figure 1

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	850 μV 1500 μV	TLV2252AID TLV2252ID	TLV2252AIP TLV2252IP	TLV2252AIPWLE —	TLV2252Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2252IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

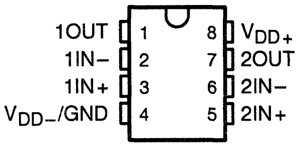
Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

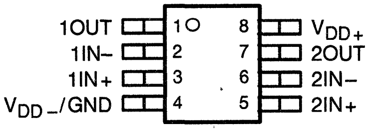
The TLV2252 and TLV2252A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features combined with its temperature performance make the TLV2252 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR P PACKAGE
(TOP VIEW)



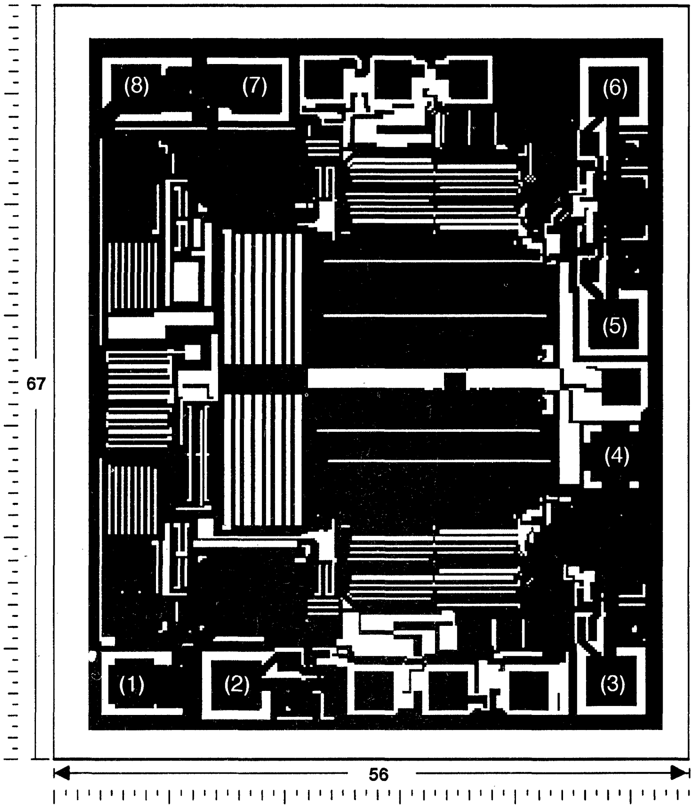
PW PACKAGE
(TOP VIEW)

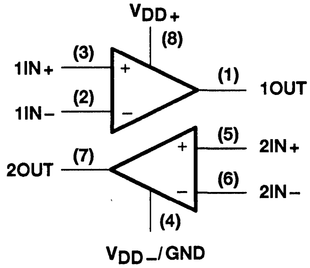


TLV2252Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2252. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

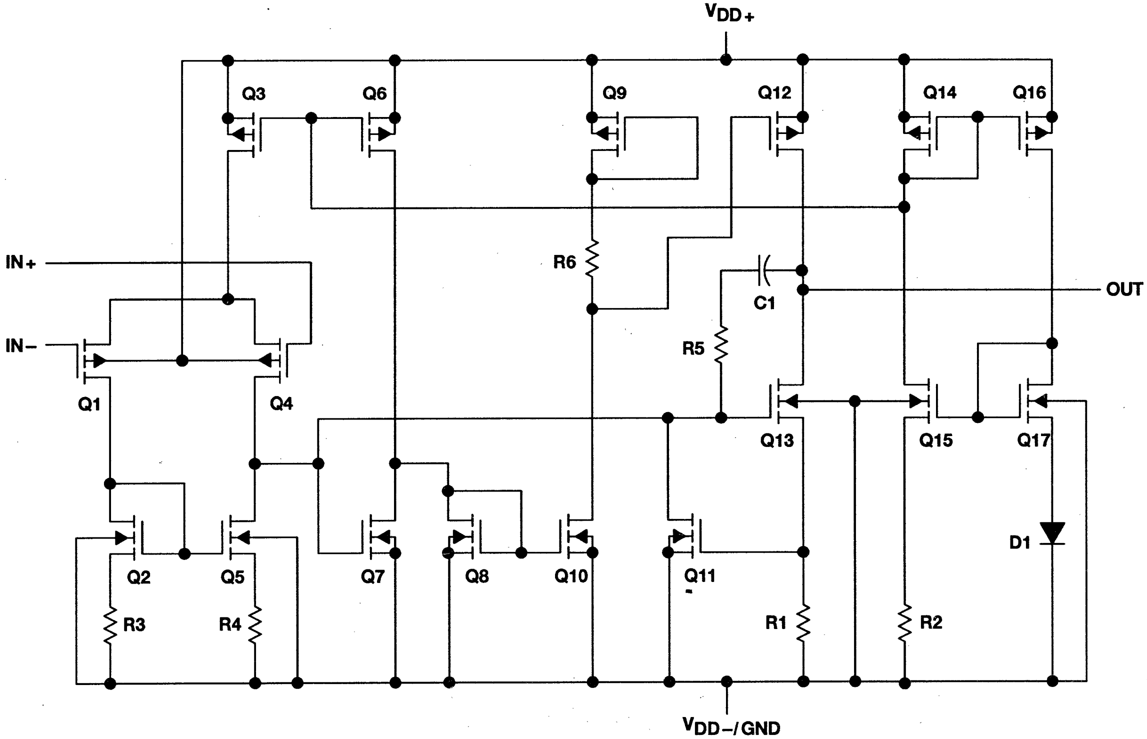
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	30
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	−0.3 V to V_{DD}
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} −1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.3	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252			TLV2252A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm1.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\|V_{IO}\| \le 5$ mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$		25°C		2.98			2.98		V
		$I_{OH} = -75\ \mu A$		25°C	2.9			2.9			
				Full range	2.8			2.8			
		$I_{OH} = -150\ \mu A$		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	$V_{IC} = 1.5$ V, $I_{OL} = 50\ \mu A$		25°C		10			10		mV
		$V_{IC} = 1.5$ V, $I_{OL} = 500\ \mu A$		25°C		100			100		
				Full range			150			150	
		$V_{IC} = 1.5$ V, $I_{OL} = 1$ mA		25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 1.5$ V, $V_O = 1$ V to 2 V	$R_L = 100\ k\Omega$‡	25°C	100	250		100	250		V/mV
				Full range	10			10			
			$R_L = 1\ M\Omega$‡	25°C		800			800		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$		25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V, $V_O = 1.5$ V, $R_S = 50\ \Omega$		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 8 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current	$V_O = 1.5$ V, No load		25°C		68	125		68	125	μA
				Full range			125			125	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2252			TLV2252A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.07	0.1		0.07	0.1		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		35			35		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2252 MIN	TLV2252 TYP	TLV2252 MAX	TLV2252A MIN	TLV2252A TYP	TLV2252A MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
			Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert$ ≤5 mV, R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.98			4.98		V
		I_{OH} = −75 μA	25°C	4.9	4.94		4.9	4.94		
			Full range	4.8			4.8			
		I_{OH} = −150 μA	25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
			Full range	10			10			
		R_L = 1 MΩ‡	25°C		1700			1700		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		70	125		70	125	μA
			Full range			125			125	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2252			TLV2252A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2252Y MIN	TLV2252Y TYP	TLV2252Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm1.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$		200	1500	μV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert \le 5$ mV,	$R_S = 50\ \Omega$	0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -20$ μA			2.98		V
		$I_{OH} = -150$ μA		2.8	2.85		
V_{OL}	Low-level output voltage	$V_{IC} = 0$,	$I_{OL} = 50$ μA		10		V
		$V_{IC} = 0$,	$I_{OL} = 500$ μA		100	125	
		$V_{IC} = 0$,	$I_{OL} = 1$ mA		200	250	
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 2 V	$R_L = 100\ k\Omega$†	100	225		V/mV
			$R_L = 1\ M\Omega$†		800		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	$A_V = 10$		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V,	$V_O = 0$, $R_S = 50\ \Omega$	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 8 V,	$V_{IC} = 0$, No load	80	100		dB
I_{DD}	Supply current	$V_O = 0$,	No load		68	125	μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2252Y MIN	TLV2252Y TYP	TLV2252Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$		200	1500	µV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	$R_S = 50\ \Omega$	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA			4.98		V
		$I_{OH} = -75$ µA		4.9	4.94		
		$I_{OH} = -150$ µA		4.8	4.88		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ µA		0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA		0.09	0.15	
		$V_{IC} = 2.5$ V,	$I_{OL} = 1$ mA		0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 100$ kΩ†	100	350		V/mV
			$R_L = 1$ MΩ†		1700		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	$A_V = 10$		200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V,	$V_O = 2.5$ V, $R_S = 50\ \Omega$	70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V, No load	$V_{IC} = V_{DD}/2$,	80	95		dB
I_{DD}	Supply current	$V_O = 2.5$ V,	No load		70	125	µA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2252
INPUT OFFSET VOLTAGE

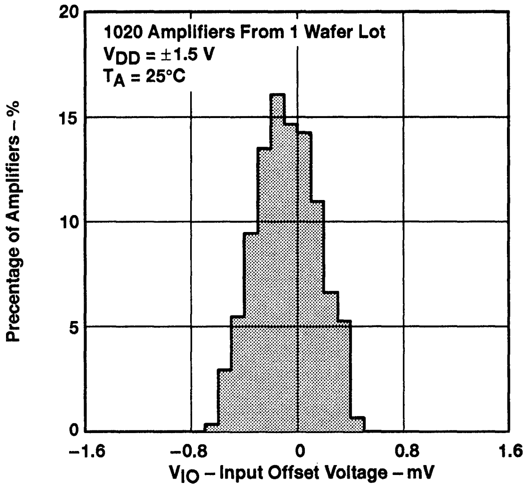


Figure 2

DISTRIBUTION OF TLV2252
INPUT OFFSET VOLTAGE

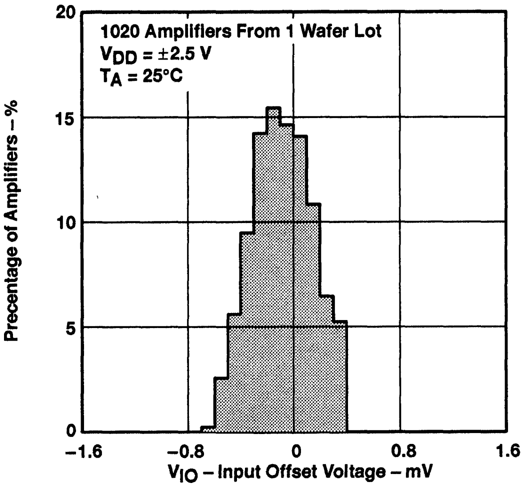


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

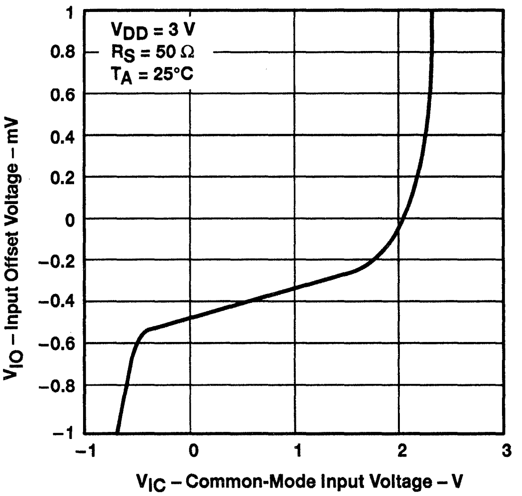


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

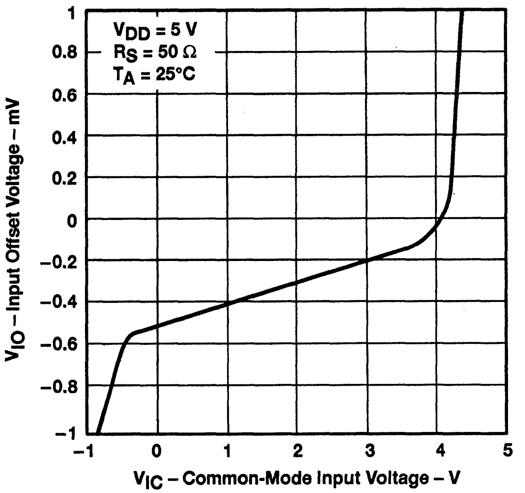


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2252 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

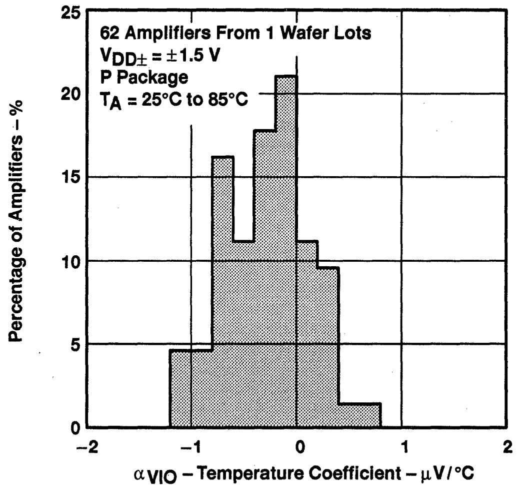


Figure 6

DISTRIBUTION OF TLV2252 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

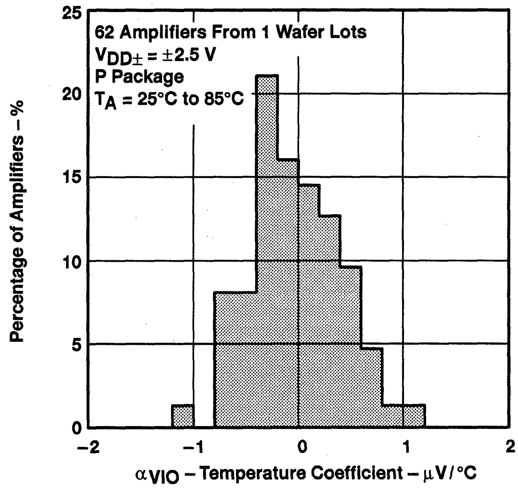


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

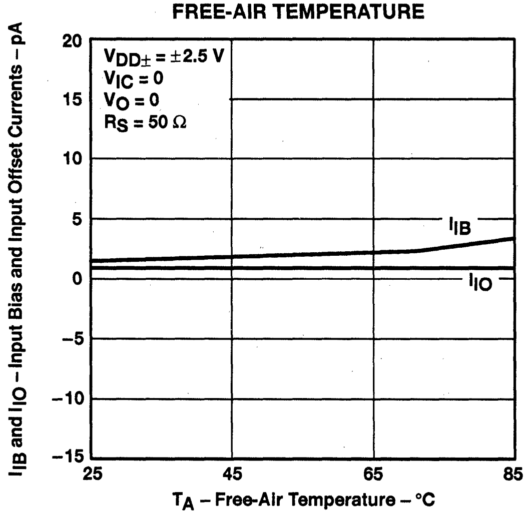


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

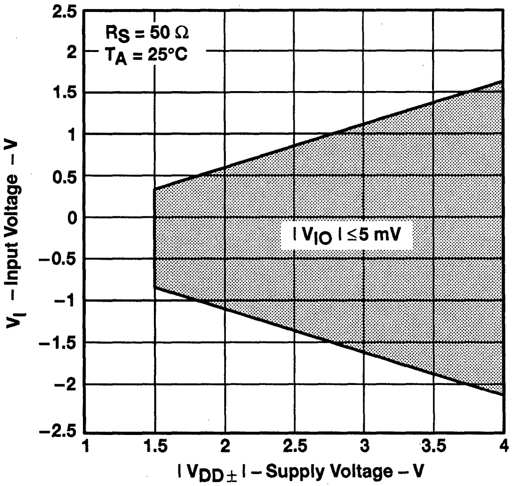


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

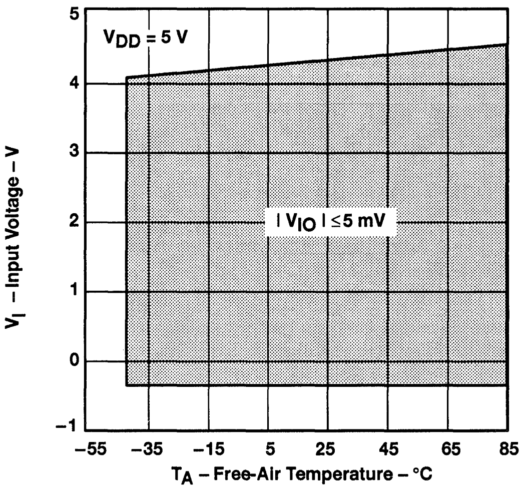


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

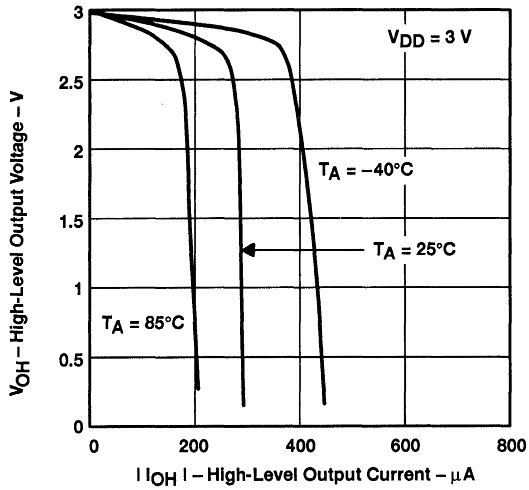


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

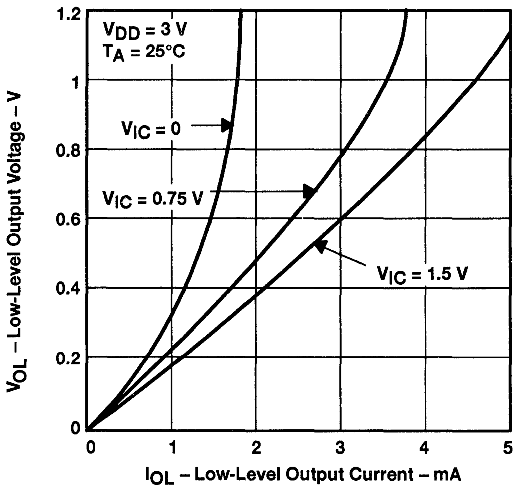


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

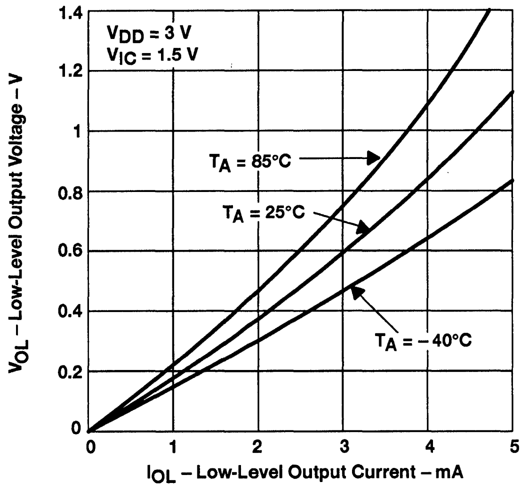


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

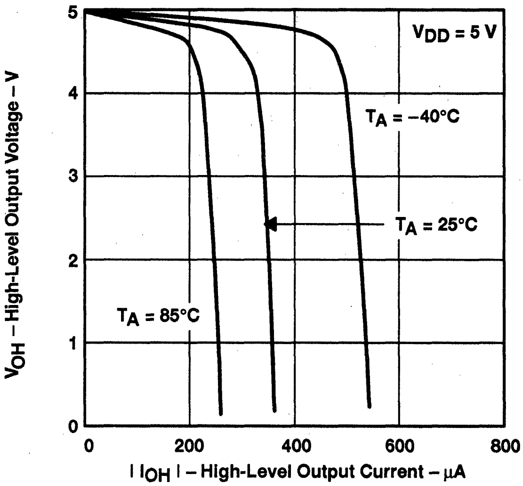


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

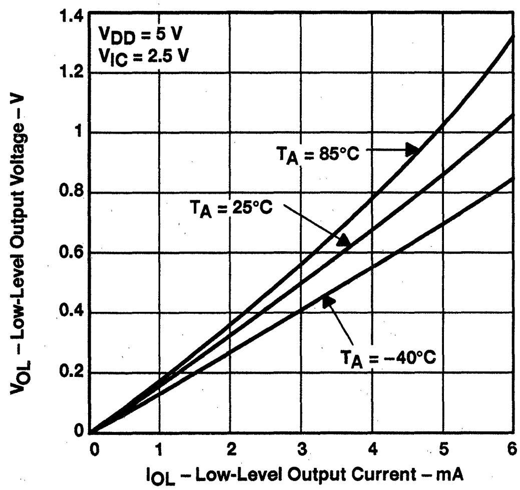


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

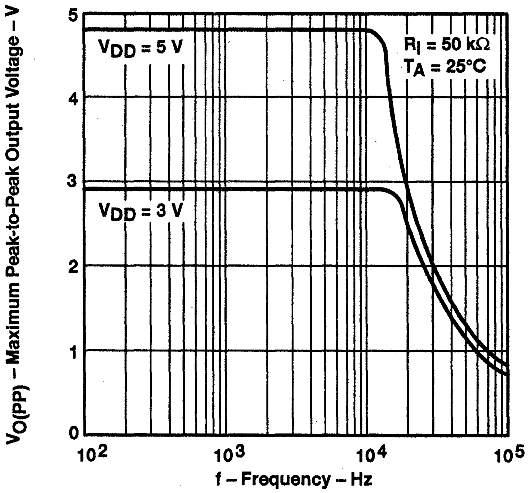


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

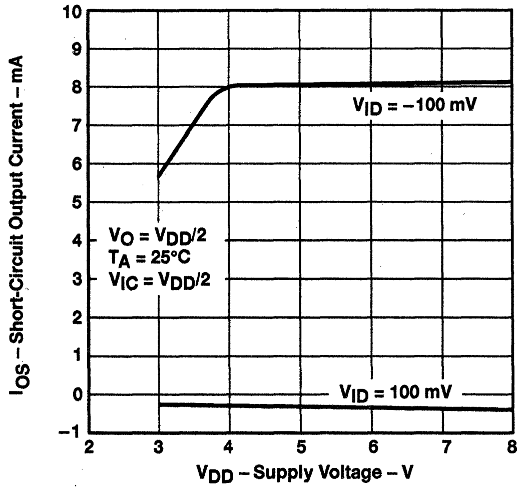


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

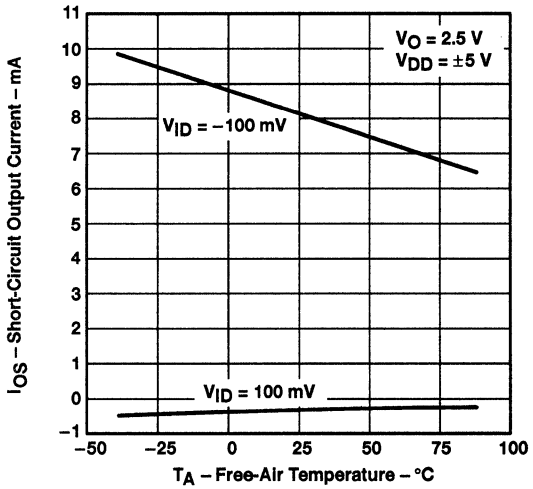


Figure 18

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

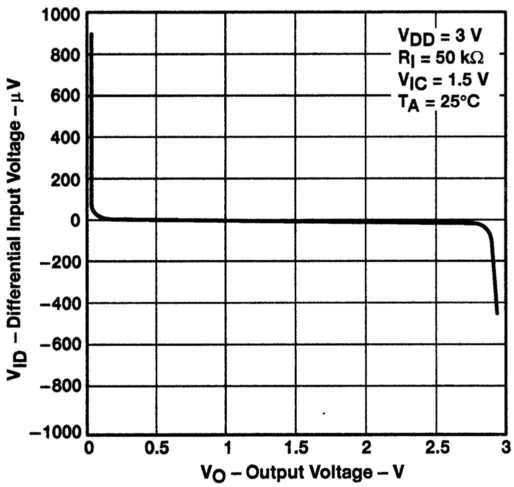


Figure 19

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

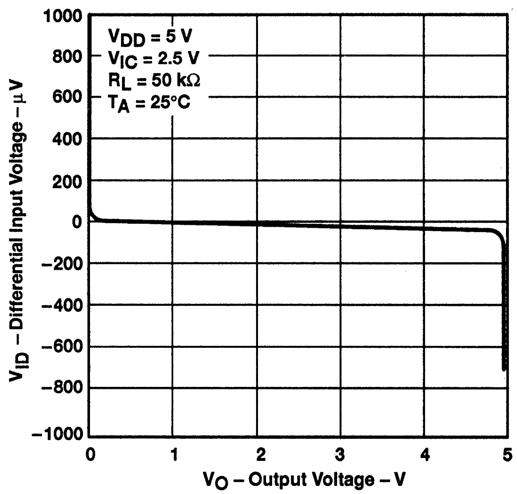


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

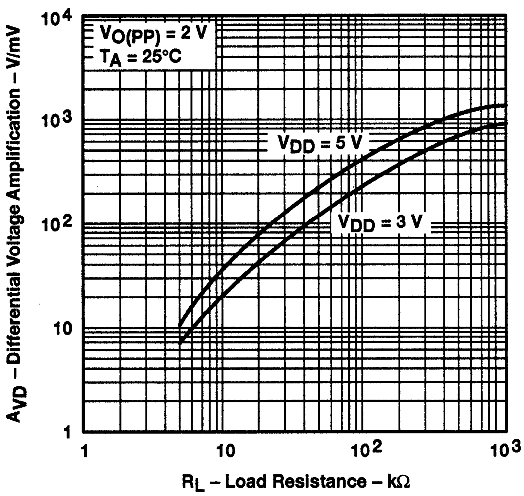


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

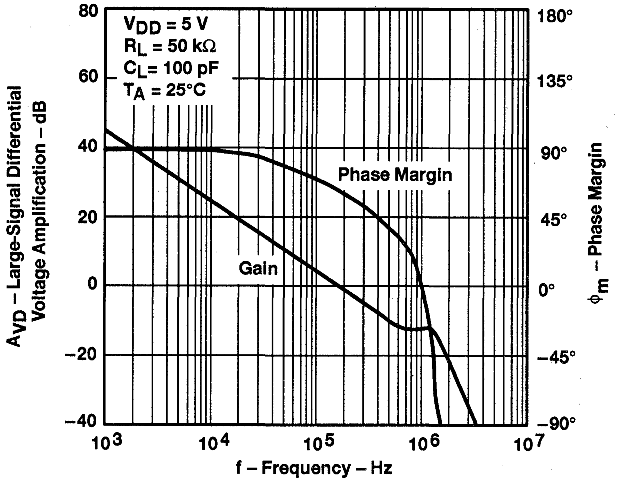


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

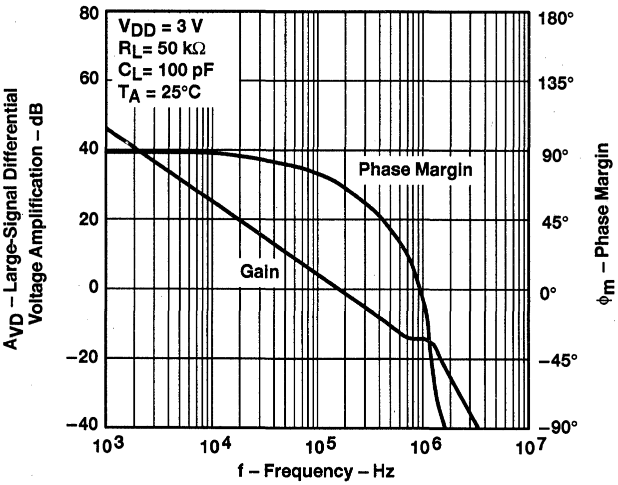


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

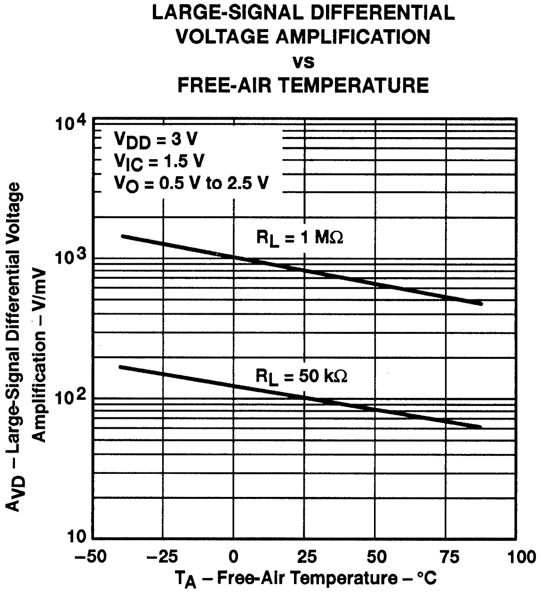


Figure 24

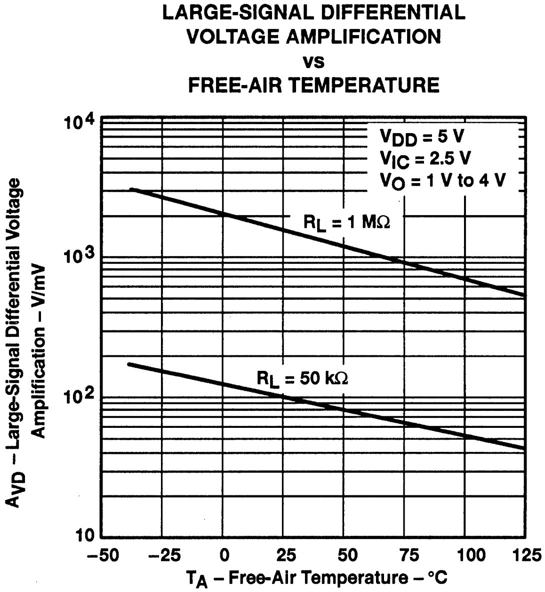


Figure 25

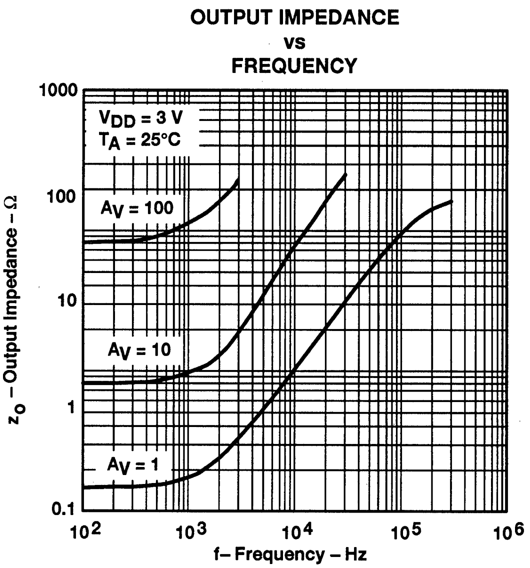


Figure 26

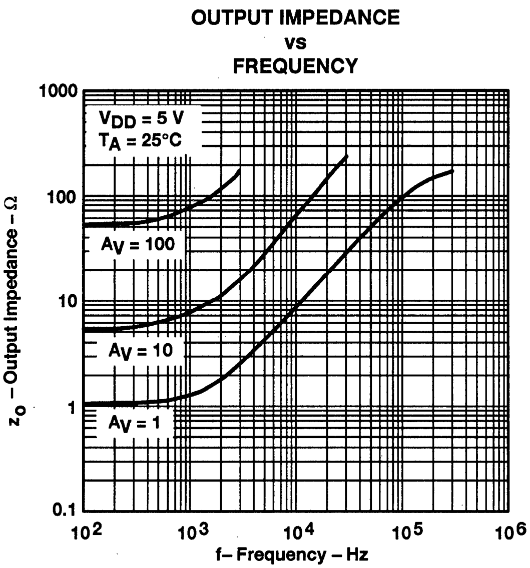


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO vs FREQUENCY

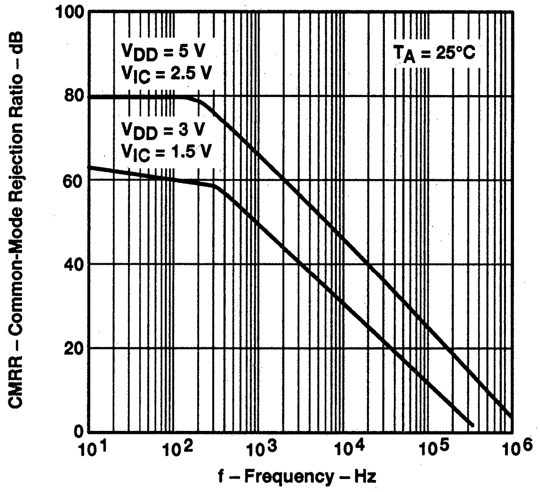


Figure 28

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

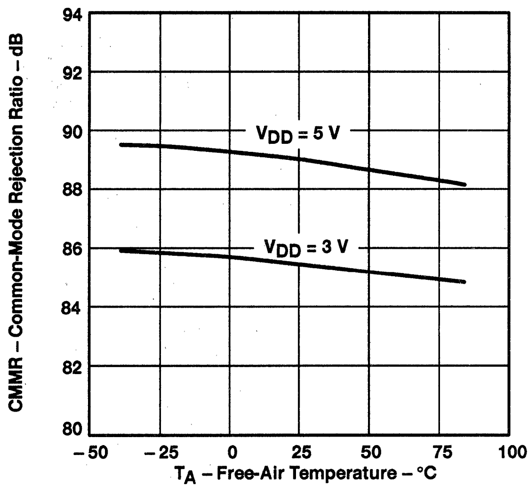


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

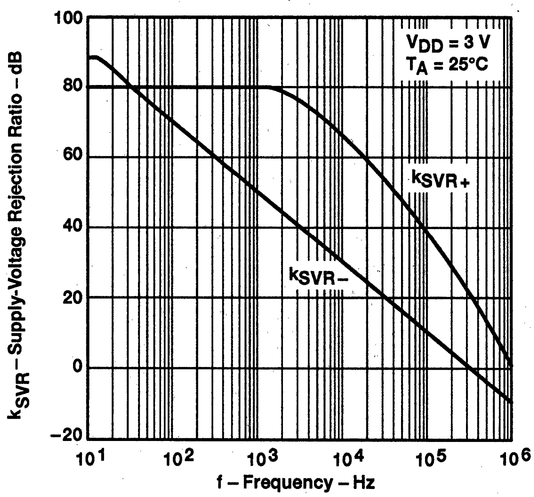


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

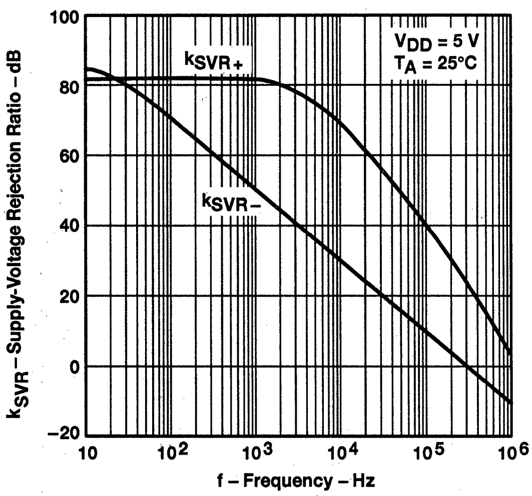


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

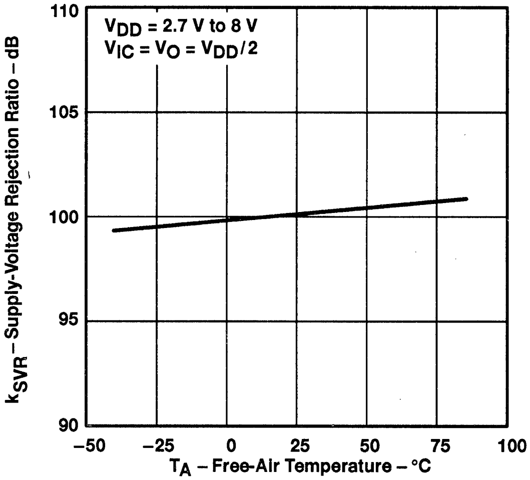


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

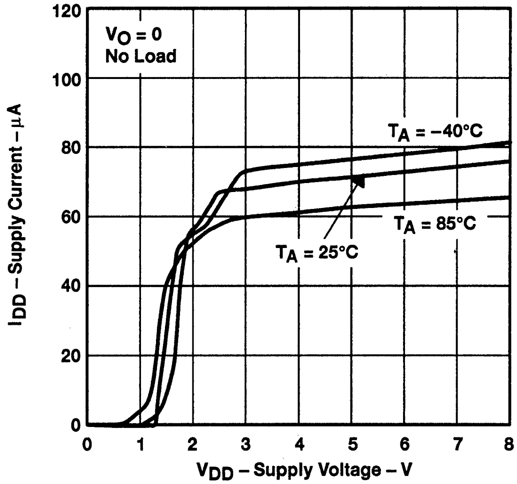


Figure 33

SLEW RATE
vs
LOAD CAPACITANCE

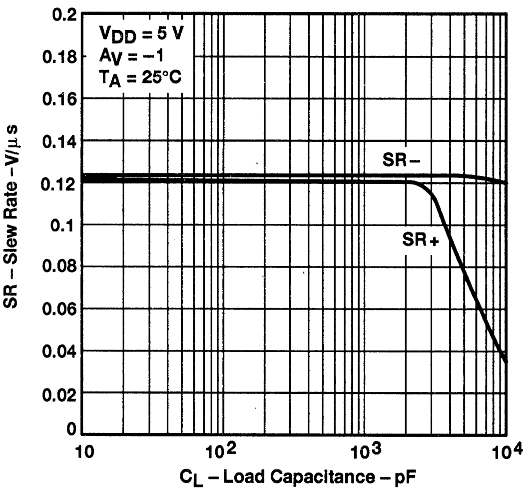


Figure 34

SLEW RATE
vs
FREE-AIR TEMPERATURE

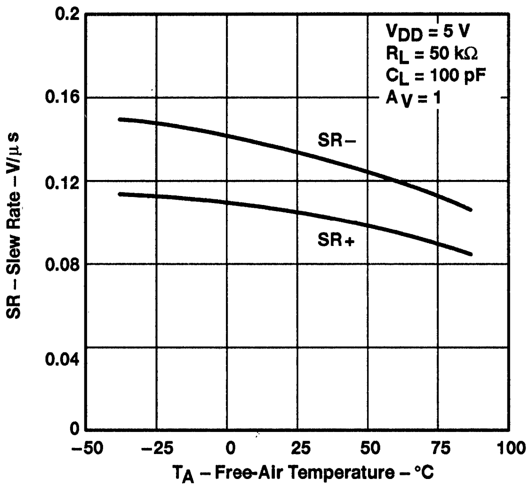


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

INVERTING LARGE-SIGNAL PULSE RESPONSE

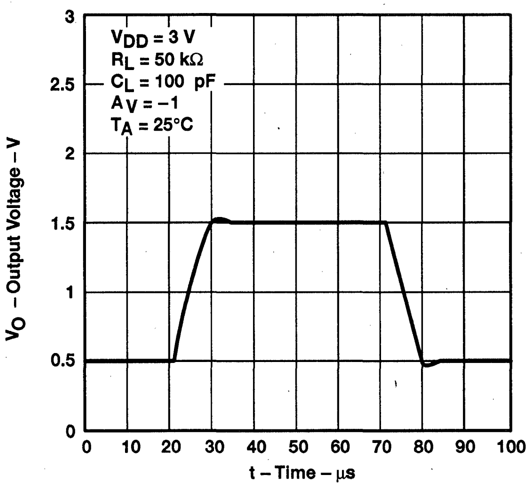


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

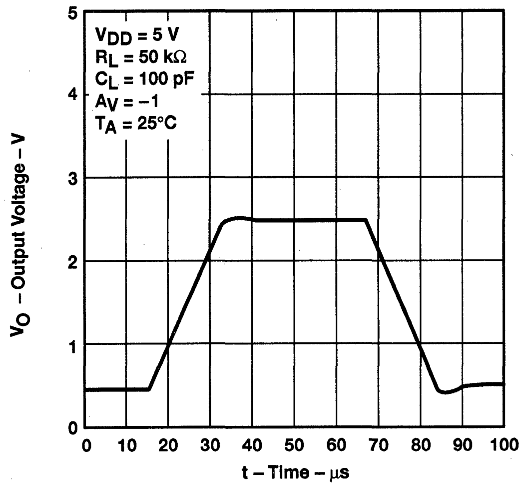


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

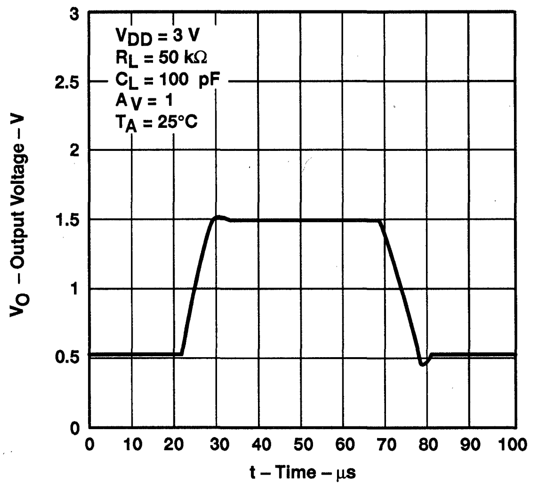


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

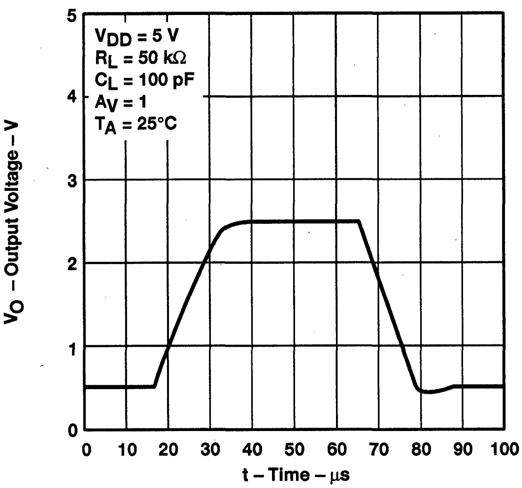


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL PULSE RESPONSE

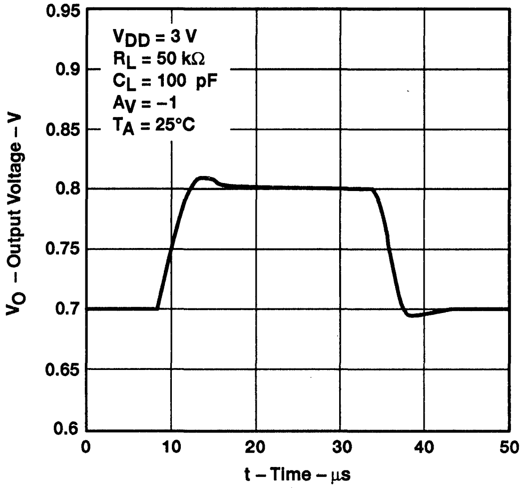


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE

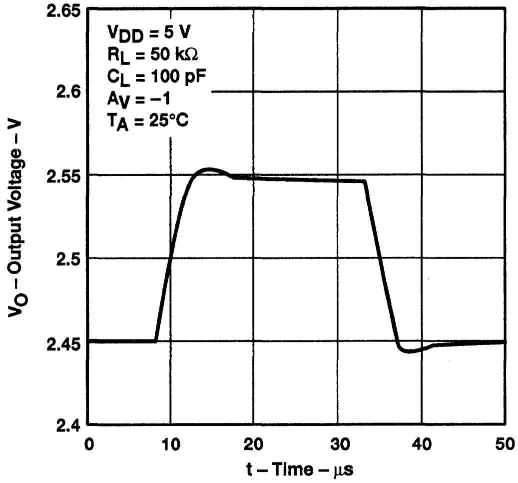


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

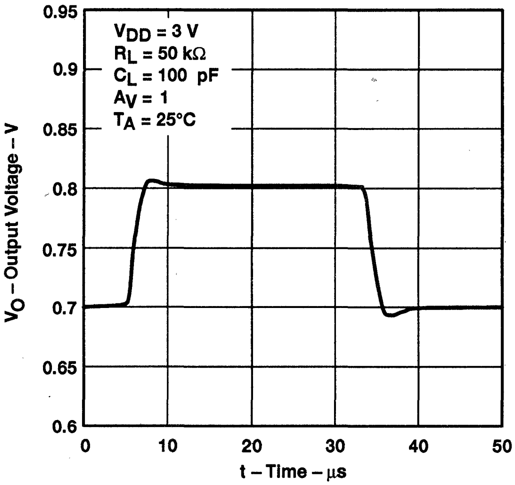


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

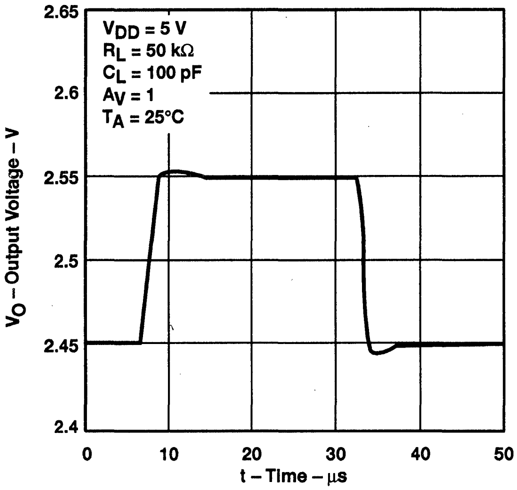


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

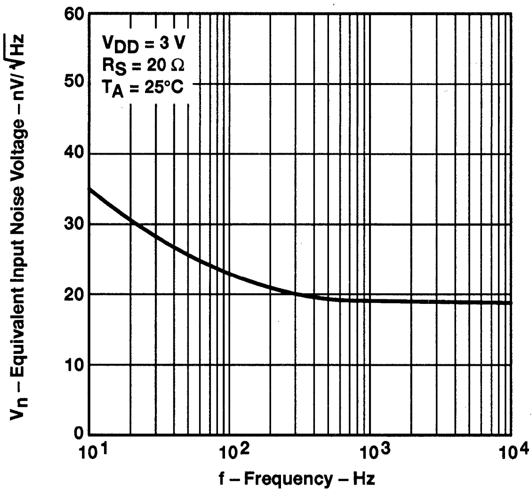


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

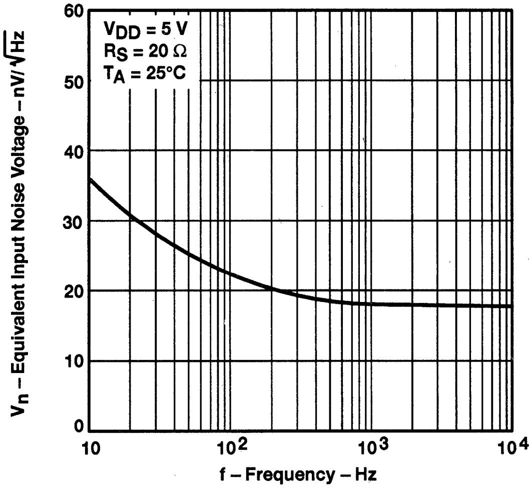


Figure 45

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

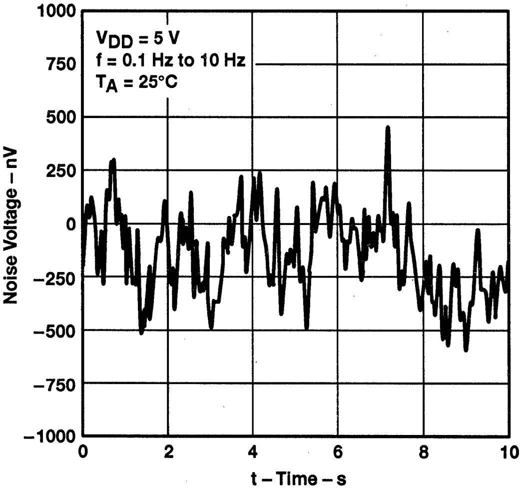


Figure 46

INTEGRATED NOISE VOLTAGE vs FREQUENCY

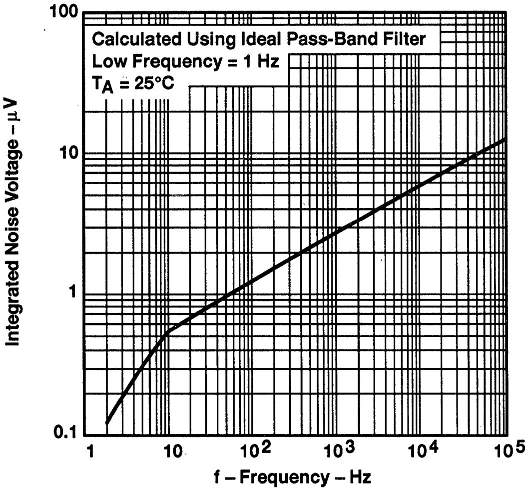


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

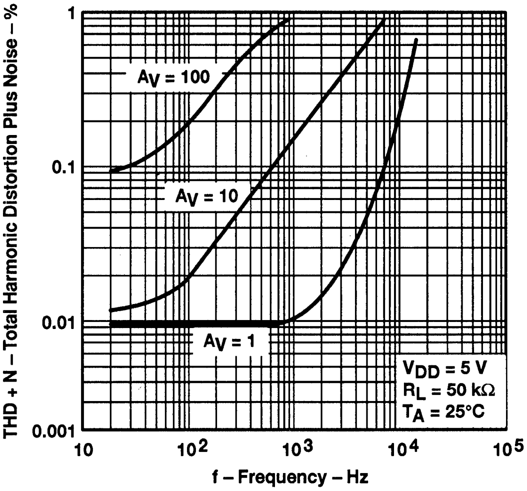


Figure 48

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

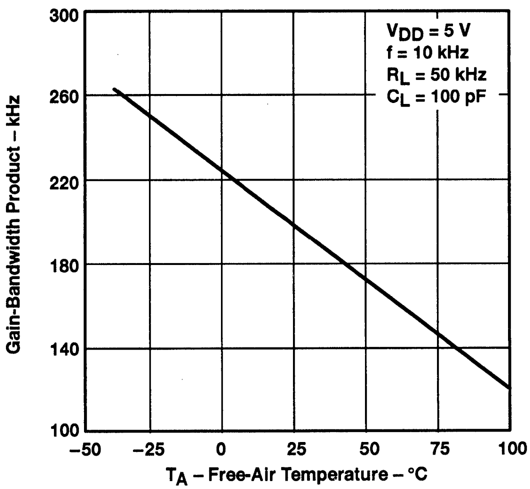


Figure 49

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

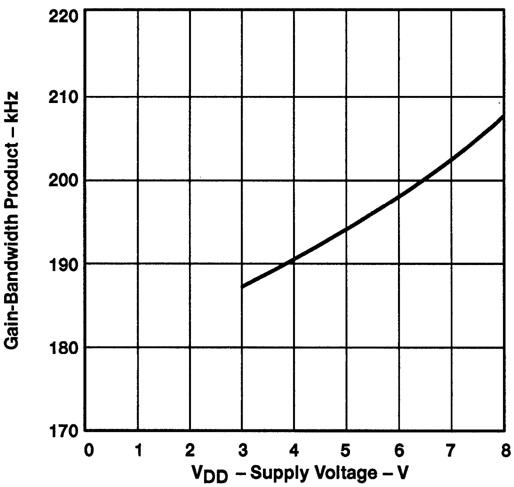


Figure 50

PHASE MARGIN vs LOAD CAPACITANCE

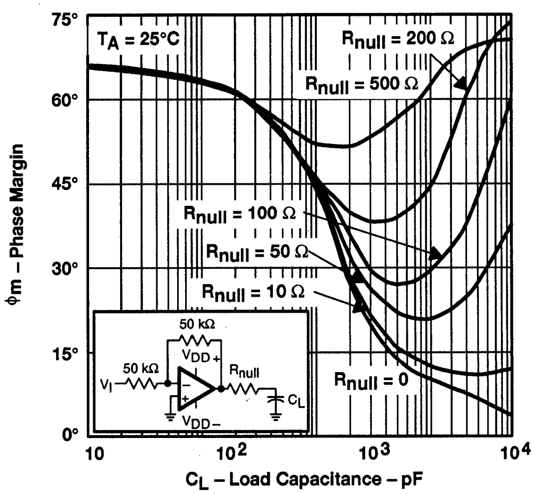


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN vs LOAD CAPACITANCE

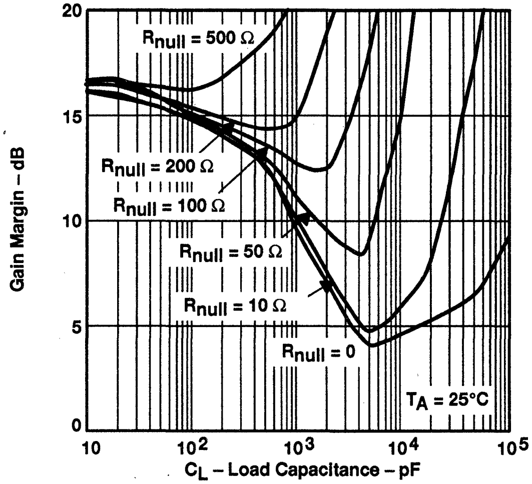


Figure 52

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

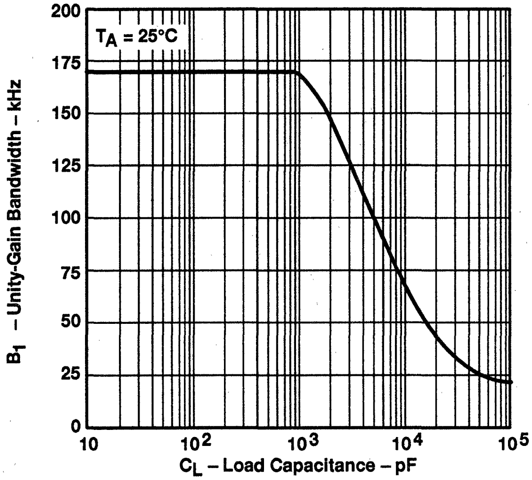
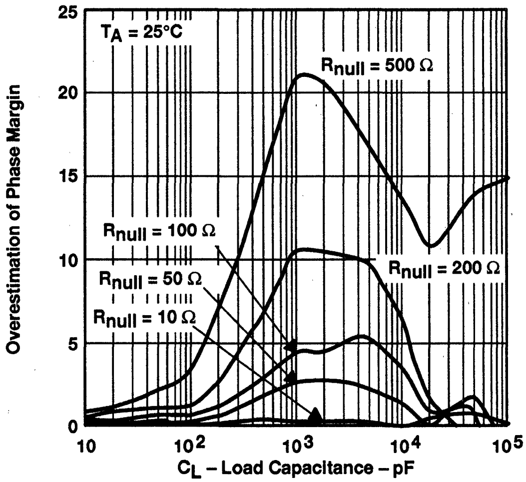


Figure 53

OVERESTIMATION OF PHASE MARGIN† vs LOAD CAPACITANCE



† See application information

Figure 54

APPLICATION INFORMATION

driving large capacitive loads

The TLV2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \qquad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 55, with equation (1) enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

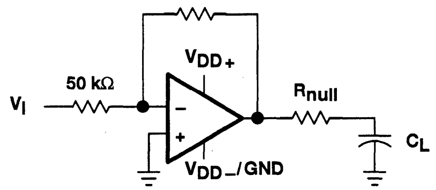


Figure 55. Series-Resistance Circuit

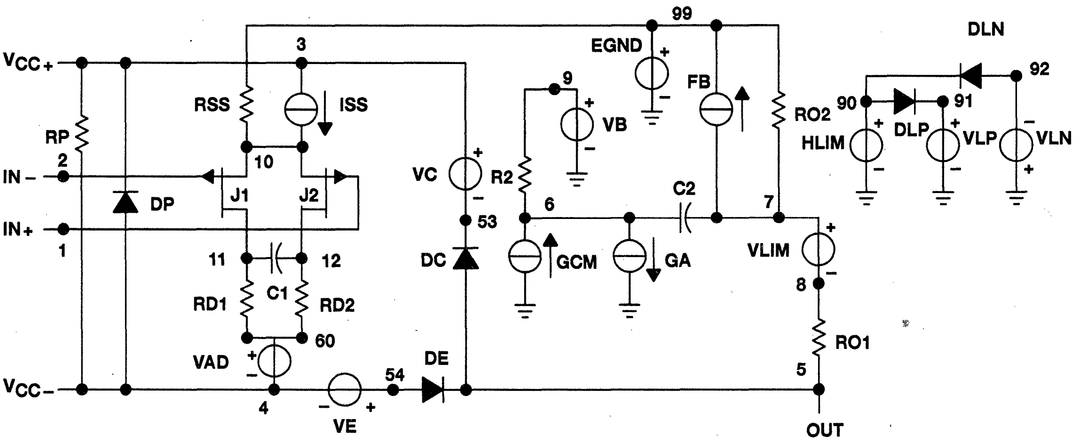
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 56 are generated using the TLV2252 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLC2252 1 2 3 4 5
    C1     11    12    6.369E-12
    C2     6     7     25.00E-12
    DC     5     53    DX
    DE     54    5     DX
    DLP    90    91    DX
    DLN    92    90    DX
    DP     4     3     DX
    EGND   99    0     POLY (2) (3,0) (4,0) 0 .5 .5
    FB     7     99    POLY (5) VB VC VE VLP
    + VLN 0 57.62E6 –60E6 60E6 60E6 –60E6
    GA     6     0     11    12 26.86E–6
    GCM    0     6     10    99 2.686E–9
    ISS    3     10    DC 3.1E–6
    HLIM   90    0     VLIM 1K
    J1     11    2     10 JX
    J2     12    1     10 JX
    R2     6     9     100.0E3
    RD1    60    11    37.23E3
    RD2    60    12    37.23E3
    R01    8     5     84
    R02    7     99    84
    RP     3     4     71.43E3
    RSS    10    99    64.52E6
    VAD    60    4     –.5
    VB     9     0     DC 0
    VC     3     53    DC .605
    VE     54    4     DC .605
    VLIM   7     8     DC 0
    VLP    91    0     DC –0.235
    VLN    0     92    DC 7.5
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=139E–6
+ VTO=–.05)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 850 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range 2.7 V to 8 V**
- **Macromodel Included**

description

The TLV2254 and TLV2254A are quad operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μ-power dissipation levels, the input noise-voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2254 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 35 μA (typical) of supply current per amplifier, the TLV2254 family can achieve input offset voltage levels as low as 850 μV outperforming existing CMOS amplifiers. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

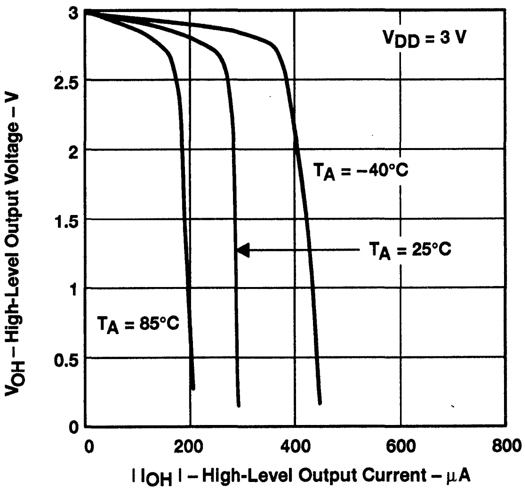


Figure 1

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
−40°C to 85°C	850 μV 1500 μV	TLV2254AID TLV2254ID	TLV2254AIN TLV2254IN	TLV2254AIPWLE —	TLV2254Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2254IDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

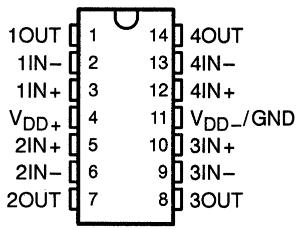
Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

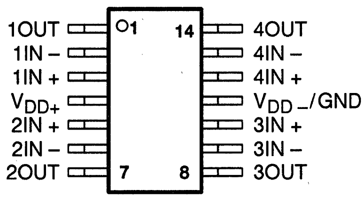
The TLV2254 and TLV2254A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power-dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to analog-to-digital converters (ADCs). All of these features, combined with its temperature performance make the TLV2254 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR N PACKAGE
(TOP VIEW)



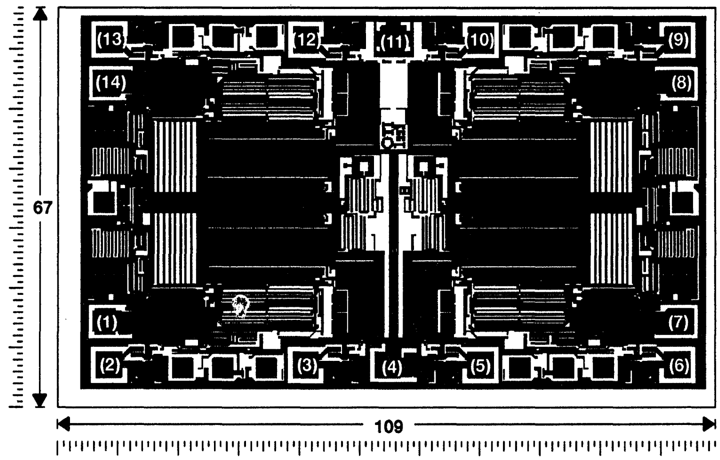
PW PACKAGE
(TOP VIEW)

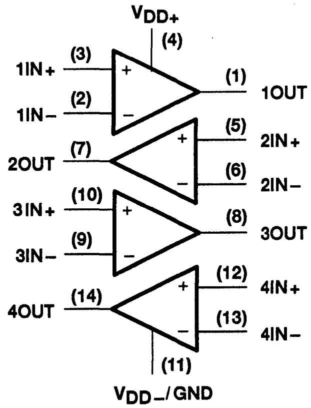


TLV2254Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2254. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

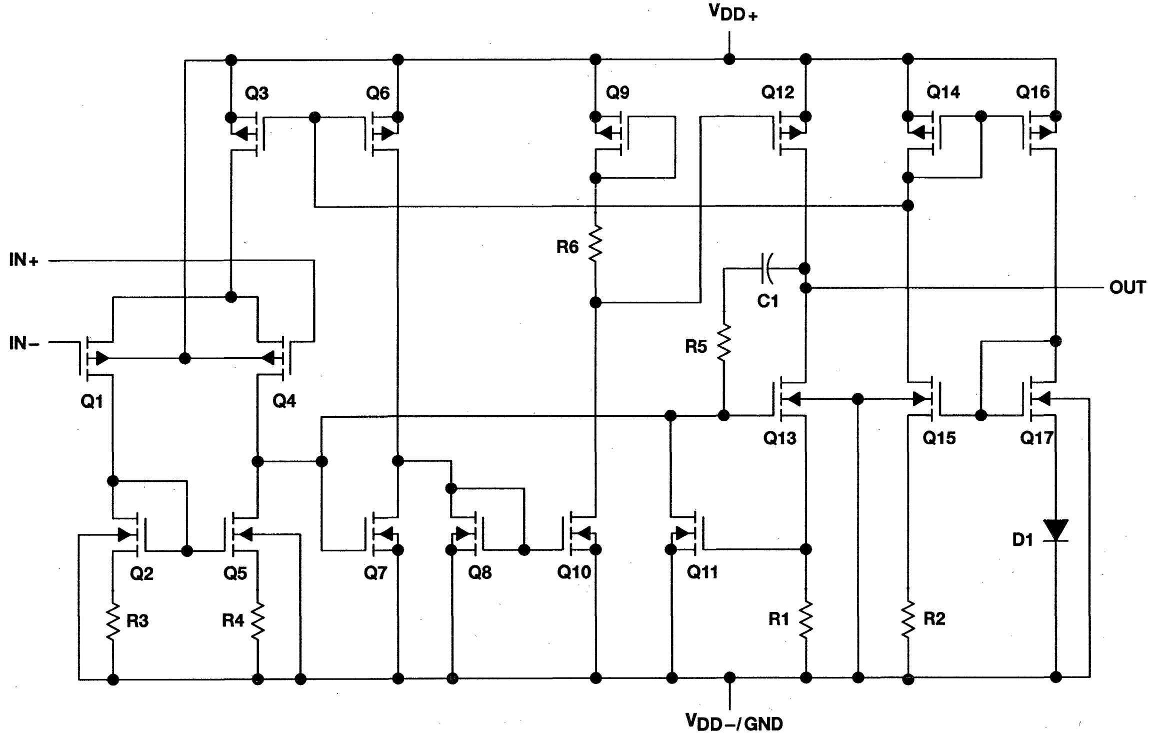
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	76
Diodes	18
Resistors	56
Capacitors	6

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 8 V
Differential input voltage, V_{ID} (see Note 2) .... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) .... $V_{DD-} - 0.3$ V to V_{DD+}
Input current, I_I (each input) .... ±5 mA
Output current, I_O .... ±50 mA
Total current into V_{DD+} .... ±50 mA
Total current out of V_{DD-} .... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A .... –40°C to 85°C
Storage temperature range .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	–40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254 MIN	TLV2254 TYP	TLV2254 MAX	TLV2254A MIN	TLV2254A TYP	TLV2254A MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO} \rvert$ ≤5 mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.98			2.98		V
		I_{OH} = −75 μA		25°C	2.9			2.9			
				Full range	2.8			2.8			
		I_{OH} = −150 μA		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 50 μA		25°C		10			10		mV
		V_{IC} = 1.5 V, I_{OL} = 500 μA		25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V, I_{OL} = 1 mA		25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 100 kΩ‡	25°C	100	225		100	225		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		800			800		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10		25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V, No load		25°C		135	250		135	250	μA
				Full range			250			250	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV2254			TLV2254A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.7 V to 1.7 V, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C	0.07	0.1		0.07	0.1		V/µs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		35			35		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6			0.6		µV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254 MIN	TLV2254 TYP	TLV2254 MAX	TLV2254A MIN	TLV2254A TYP	TLV2254A MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le 5$ mV, $R_S = 50\ \Omega$		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$		25°C		4.98			4.98		V
		$I_{OH} = -75\ \mu A$		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		$I_{OH} = -150\ \mu A$		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50\ \mu A$		25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500\ \mu A$		25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 1$ mA		25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 100\ k\Omega$‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			$R_L = 1\ M\Omega$‡	25°C		1700			1700		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$		25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5$ V, No load		25°C		140	250		140	250	µA
				Full range			250			250	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2254 MIN	TLV2254 TYP	TLV2254 MAX	TLV2254A MIN	TLV2254A TYP	TLV2254A MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 100 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2254Y MIN	TLV2254Y TYP	TLV2254Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω			200	1500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.98		V
		I_{OH} = −150 μA			2.8	2.85		
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 50 μA			10		mV
		V_{IC} = 0,	I_{OL} = 500 μA			100		
		V_{IC} = 0,	I_{OL} = 1 mA			200		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 100 kΩ†		100	225		V/mV
			R_L = 1 MΩ†			800		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load	80	100		dB
I_{DD}	Supply current (four amplifiers)	V_O = 0,	No load			135	250	μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2254Y MIN	TLV2254Y TYP	TLV2254Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω			200	1500	μV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	| V_{IO} | ≤ 5 mV, R_S = 50 Ω		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.98		V
		I_{OH} = −75 μA		4.9	4.94		
		I_{OH} = −150 μA		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA			0.09	0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA			0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ†	100	350		V/mV
			R_L = 1 MΩ†		1700		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load		80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load			140	250	μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

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TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2254
INPUT OFFSET VOLTAGE

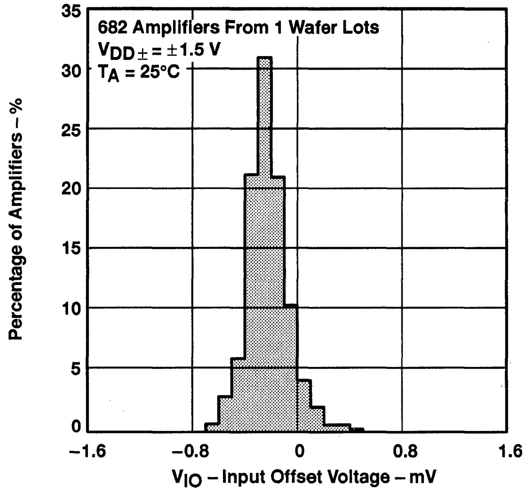


Figure 2

DISTRIBUTION OF TLV2254
INPUT OFFSET VOLTAGE

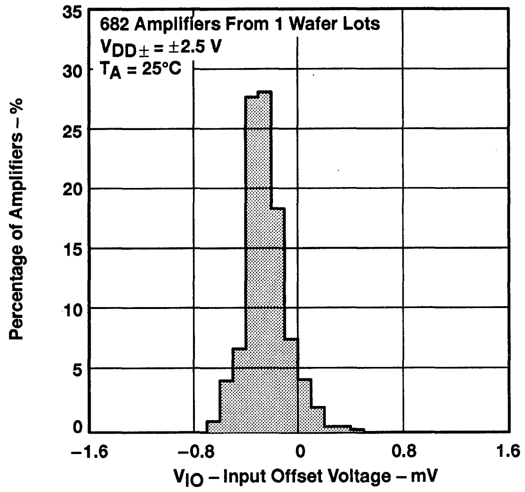


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

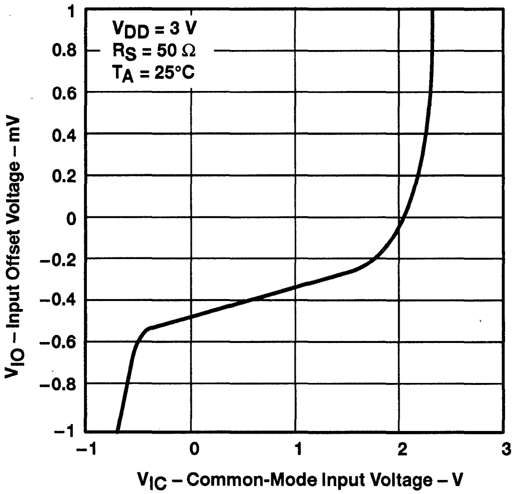


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

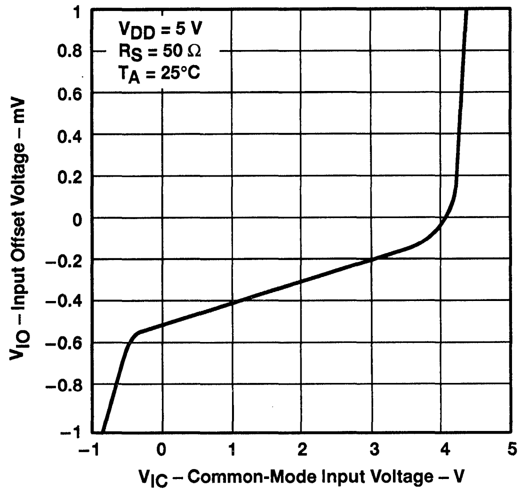


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2254 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

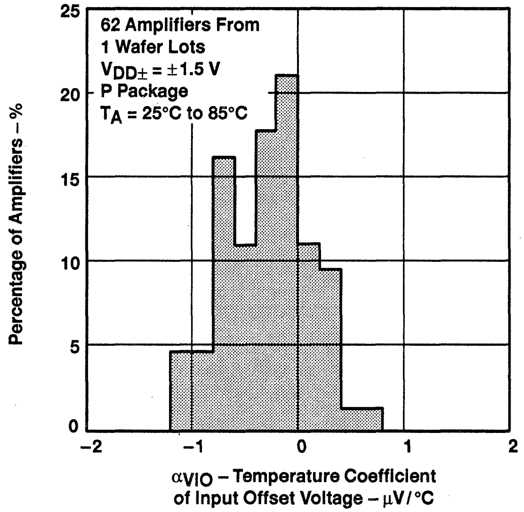


Figure 6

DISTRIBUTION OF TLV2254 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

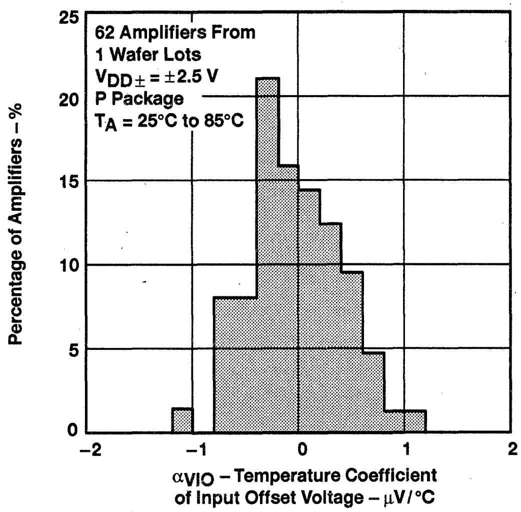


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

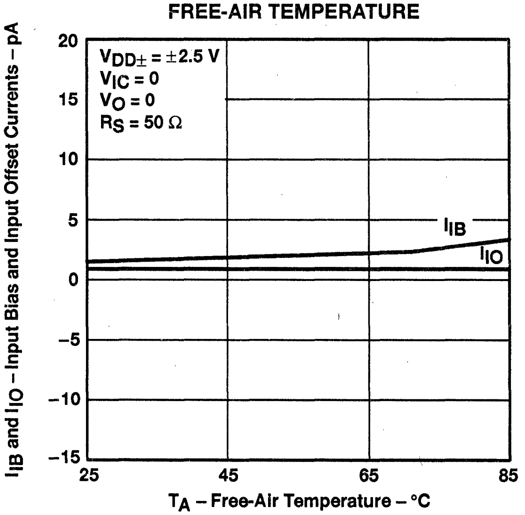


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

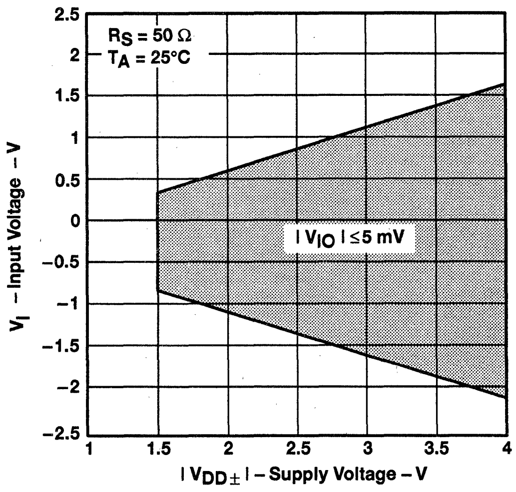


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

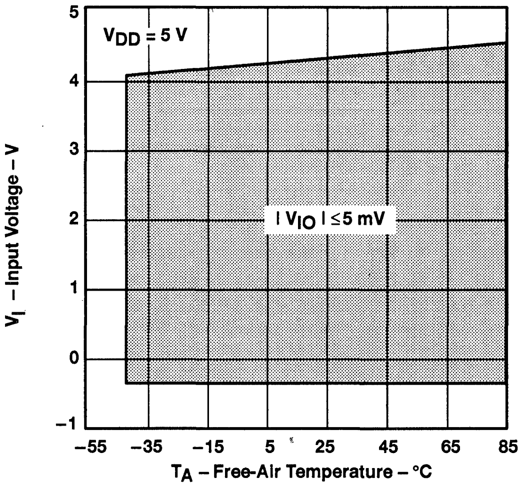


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

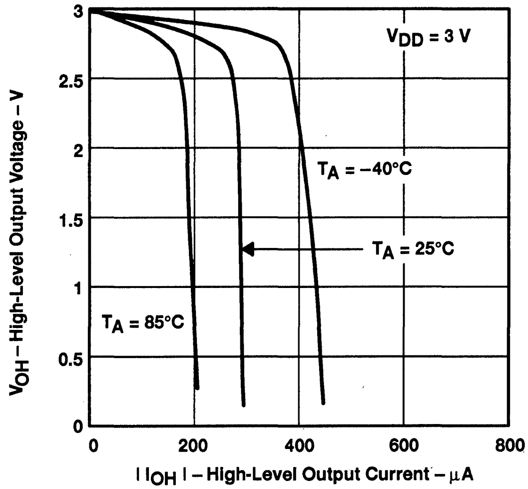


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

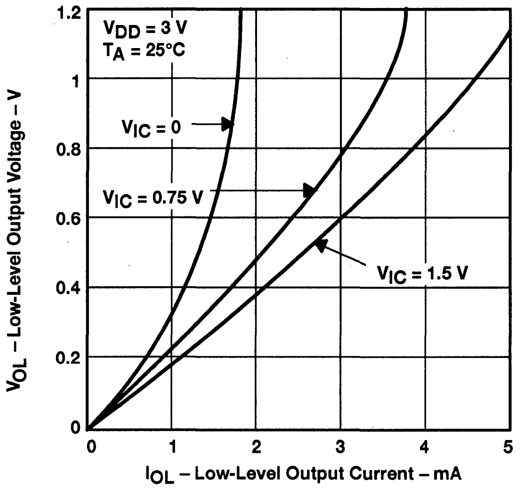


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

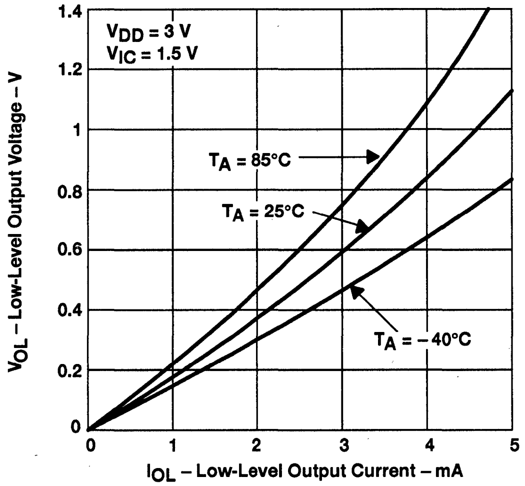


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

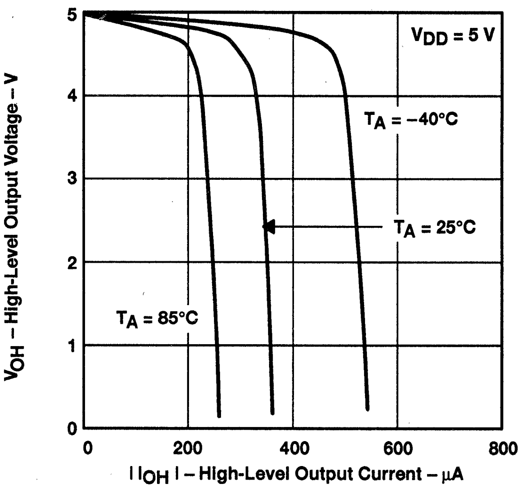


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

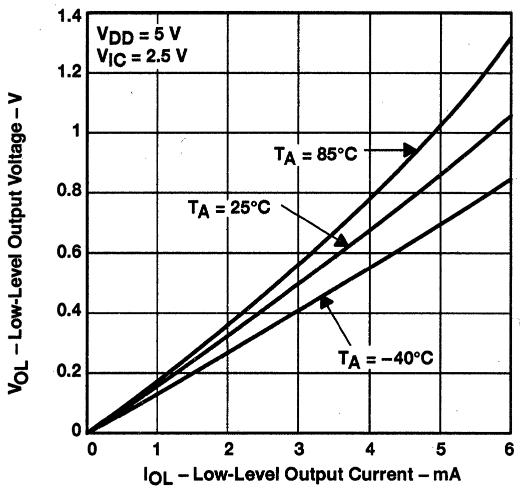


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

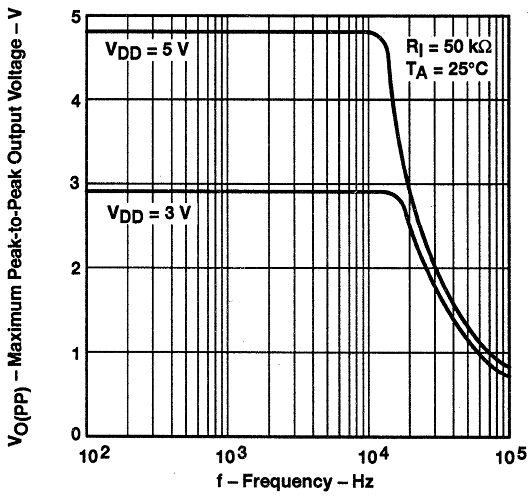


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

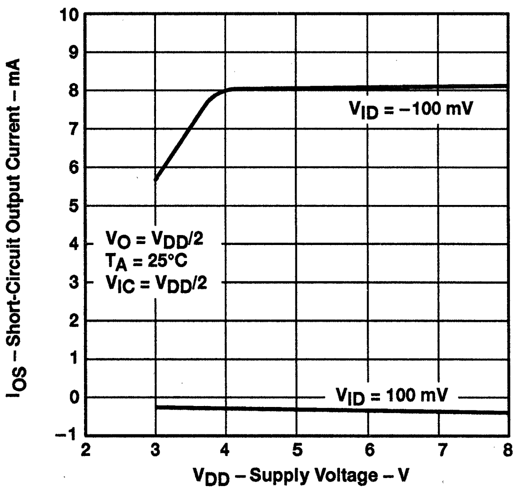


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

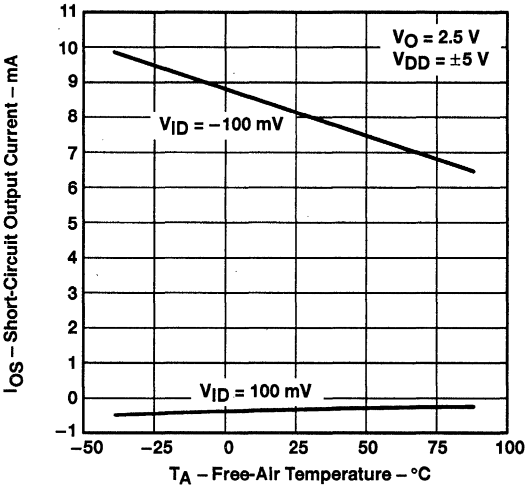


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

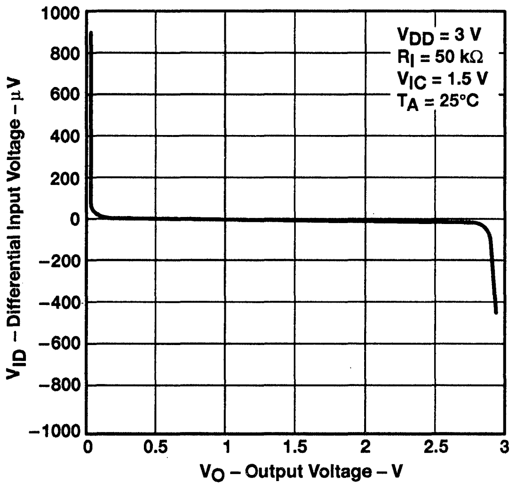


Figure 19

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

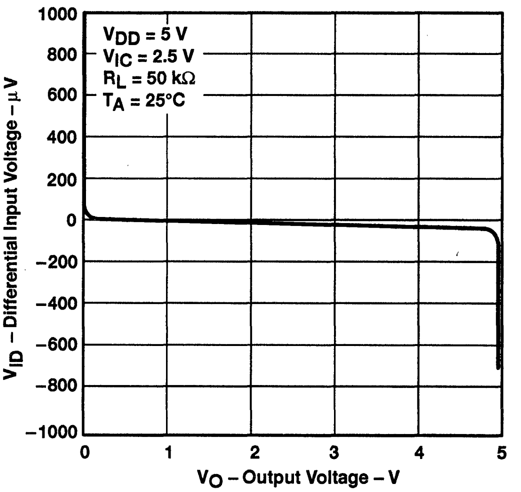


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

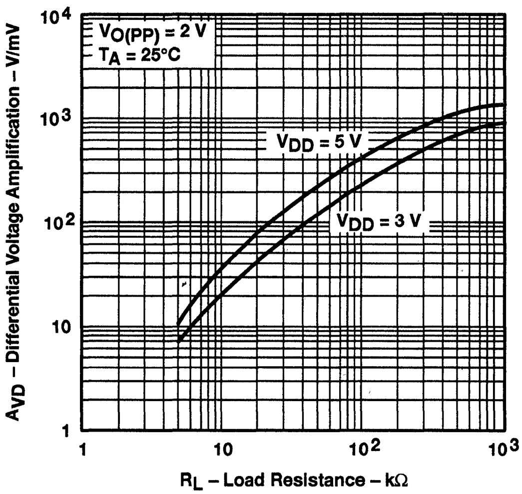


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

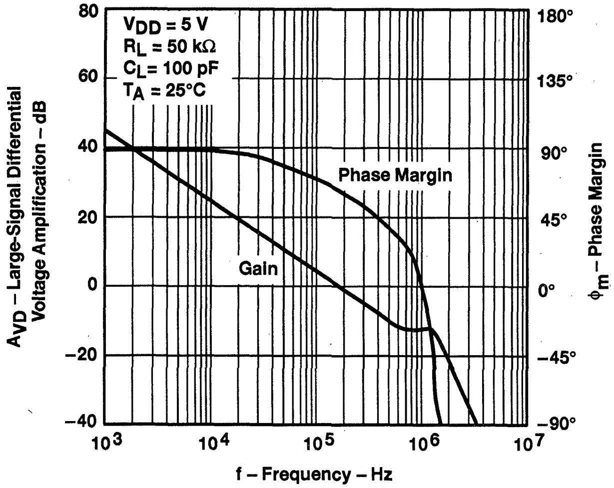


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

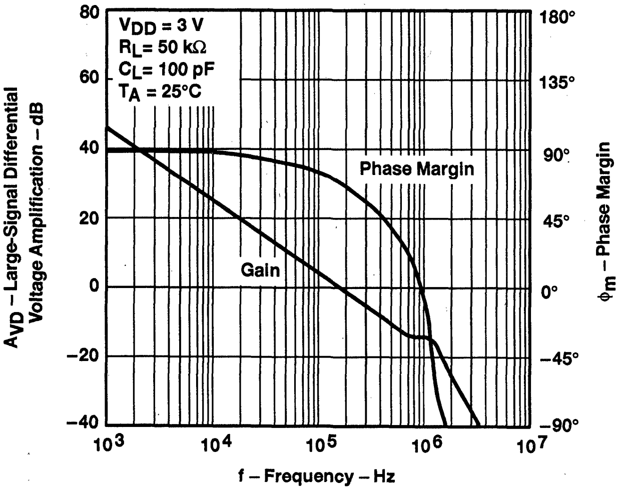


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

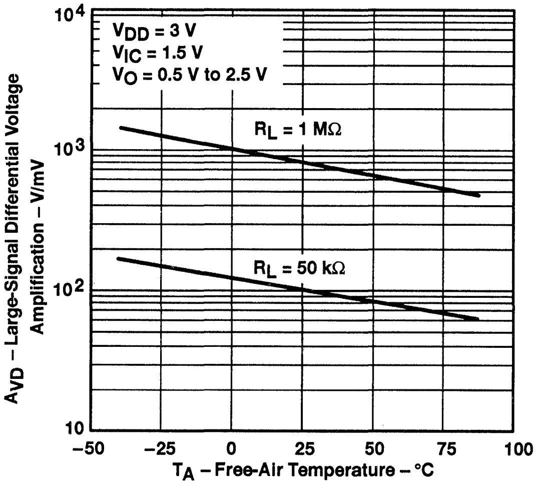


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

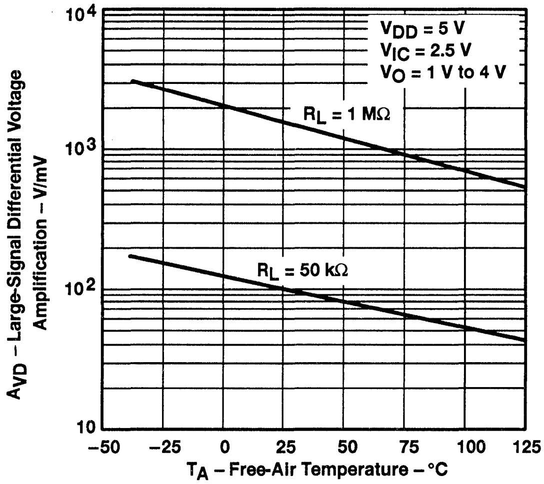


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

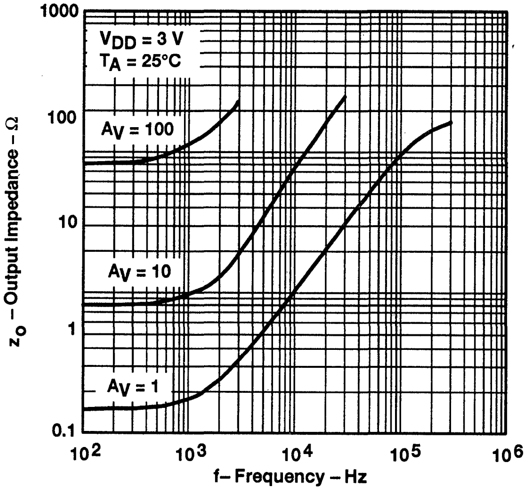


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

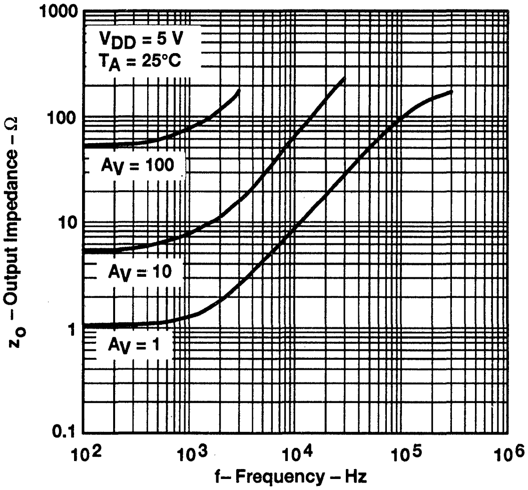


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO vs FREQUENCY

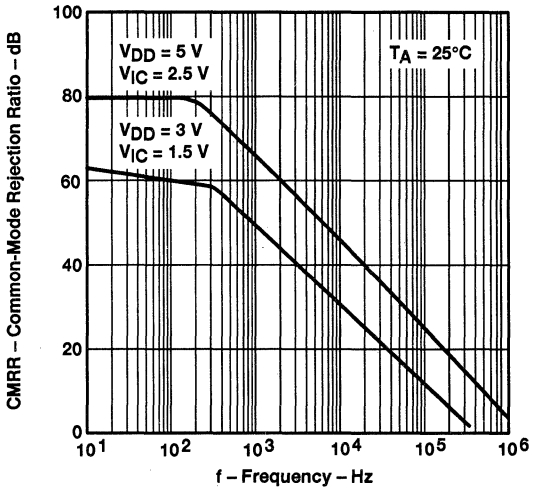


Figure 28

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

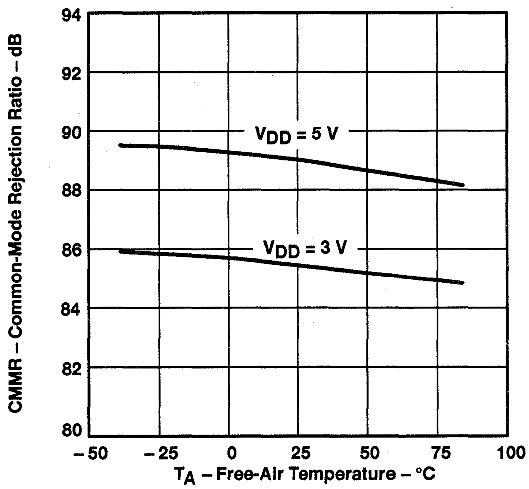


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

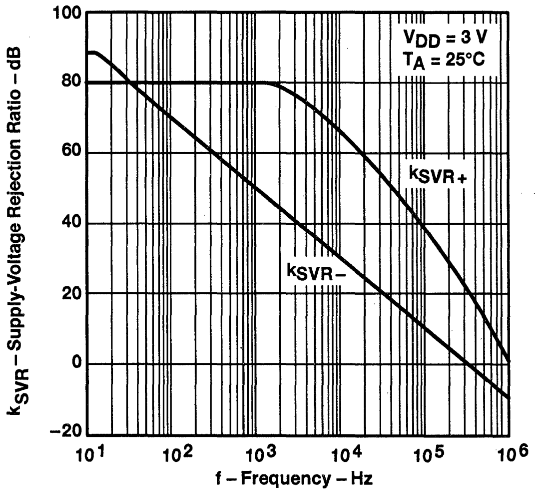


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

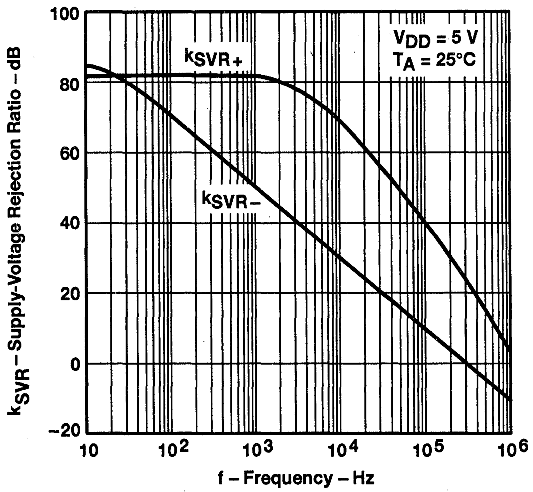


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

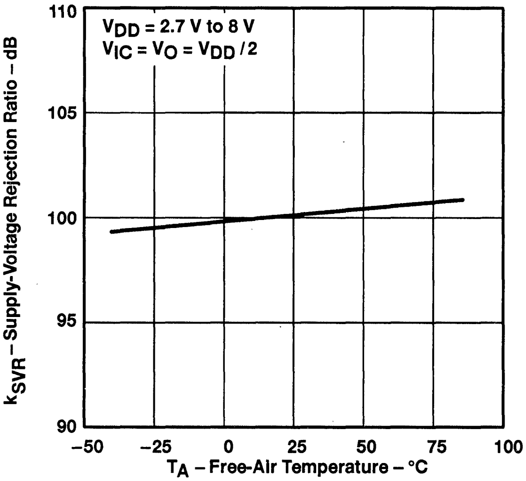


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

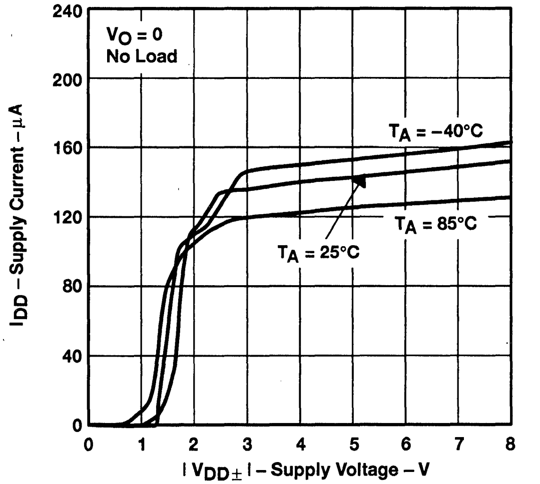


Figure 33

SLEW RATE
vs
LOAD CAPACITANCE

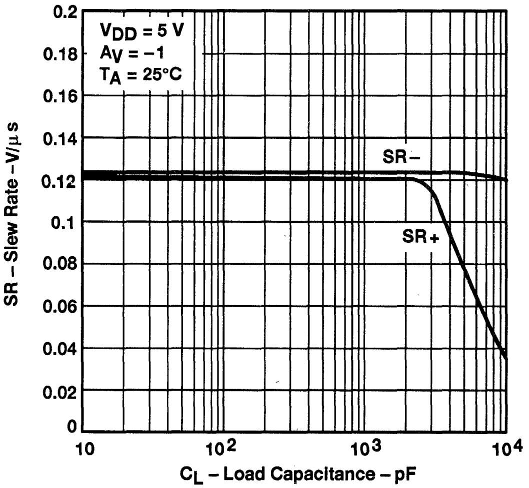


Figure 34

SLEW RATE
vs
FREE-AIR TEMPERATURE

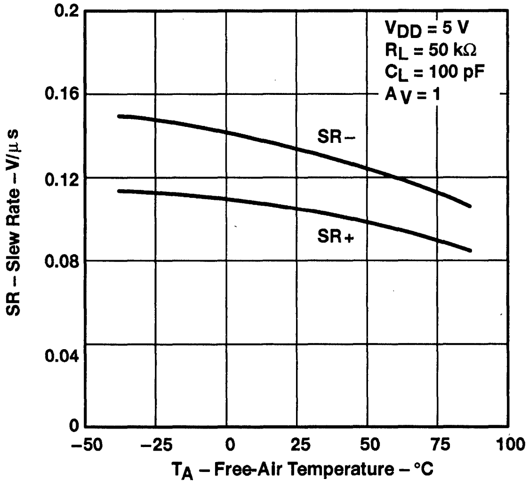


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

INVERTING LARGE-SIGNAL PULSE RESPONSE

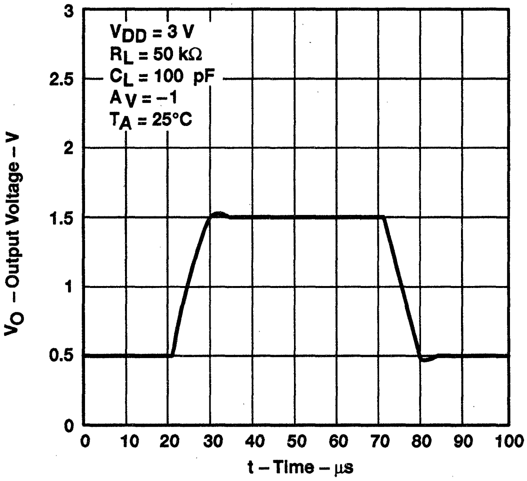


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

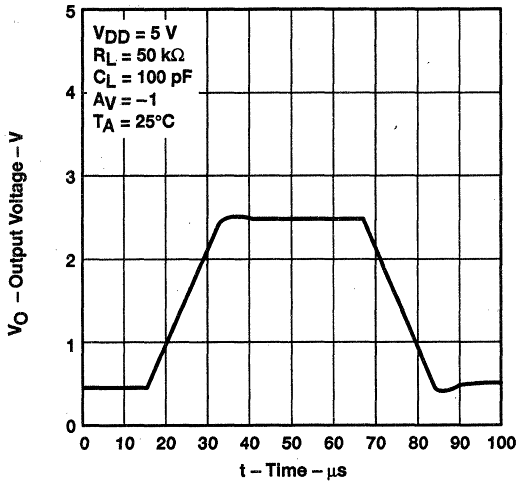


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

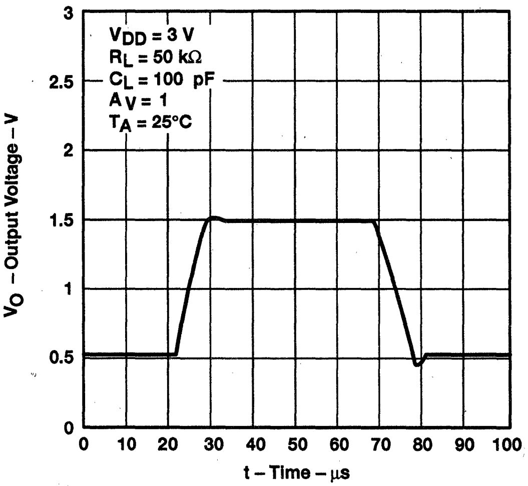


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

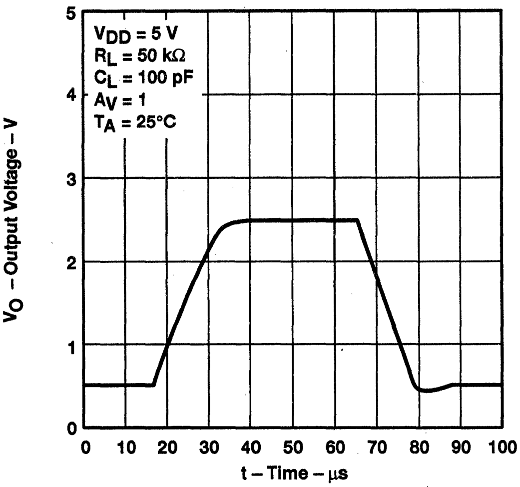


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL PULSE RESPONSE

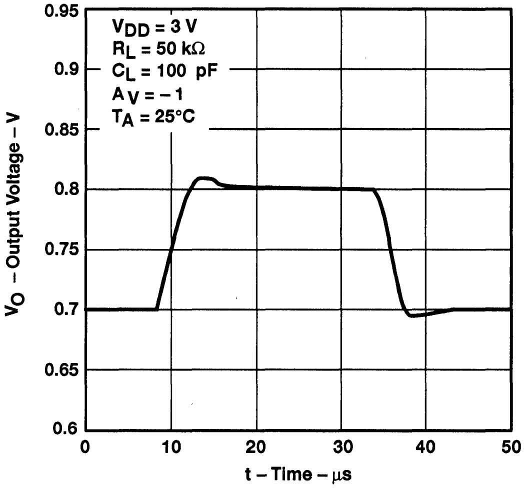


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE

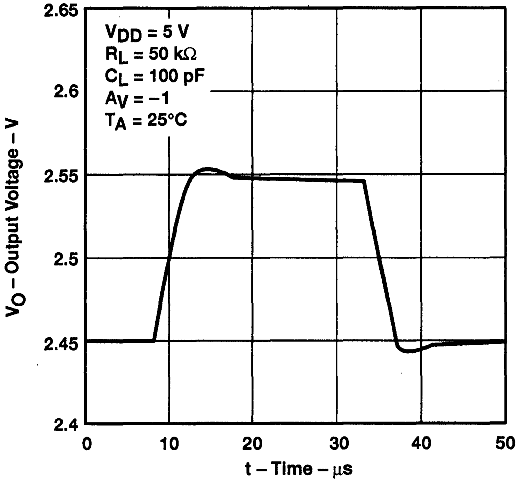


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

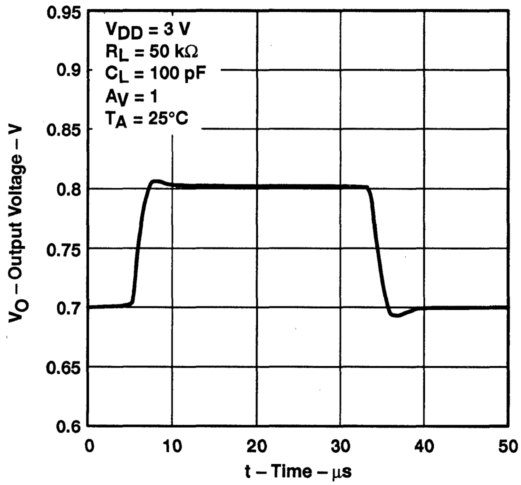


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

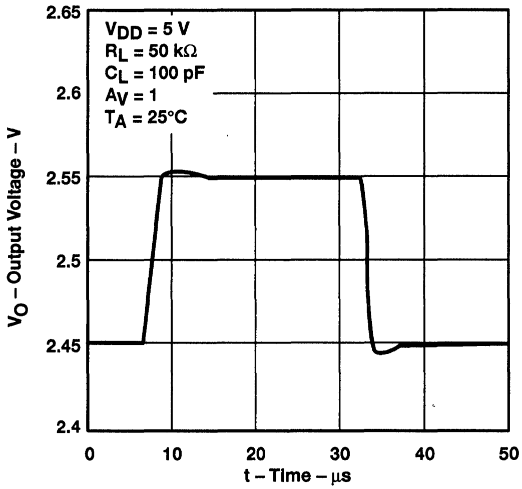


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

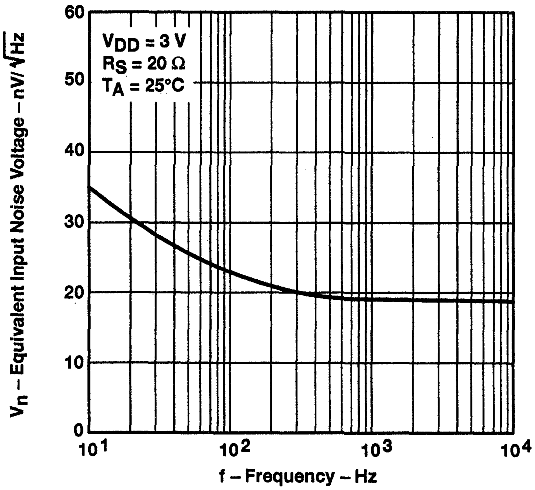


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

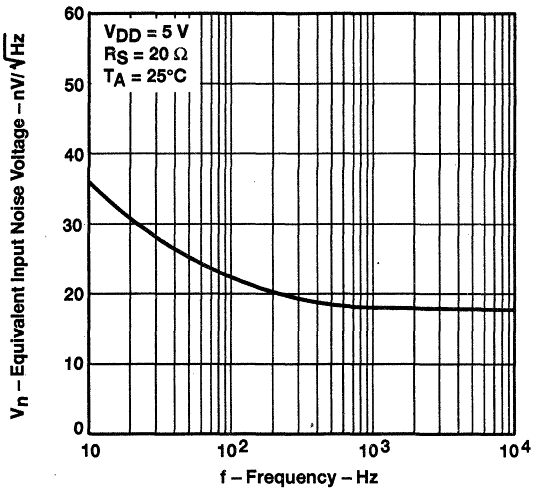


Figure 45

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

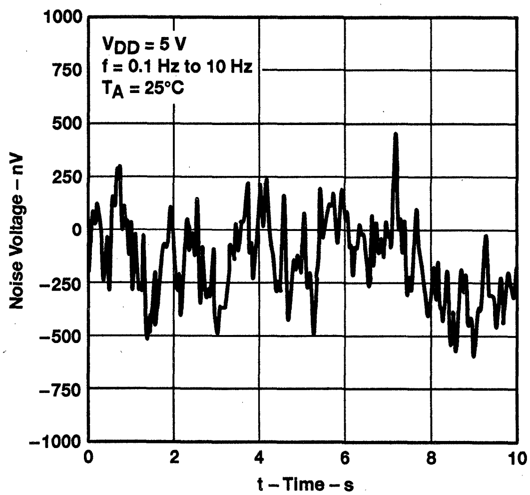


Figure 46

INTEGRATED NOISE VOLTAGE vs FREQUENCY

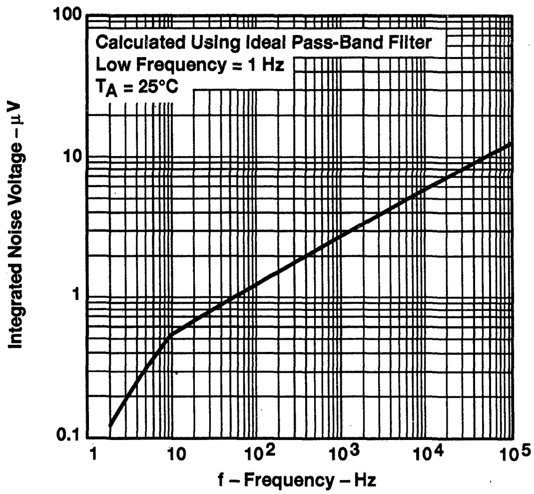


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY**

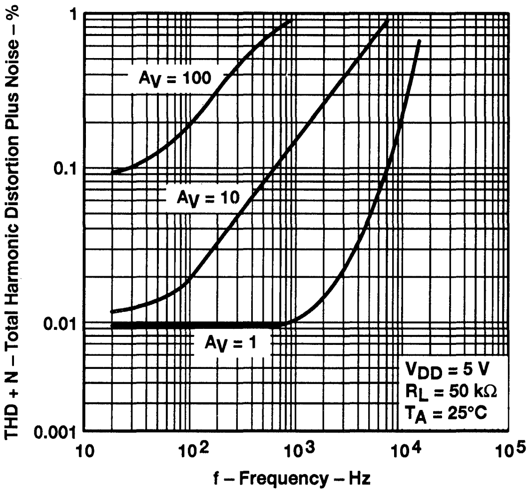


Figure 48

**GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE**

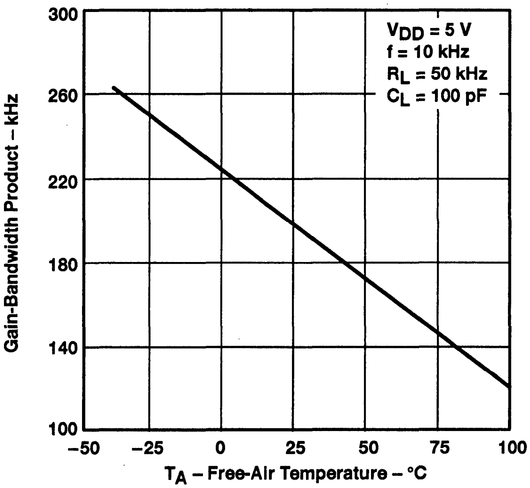


Figure 49

**GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE**

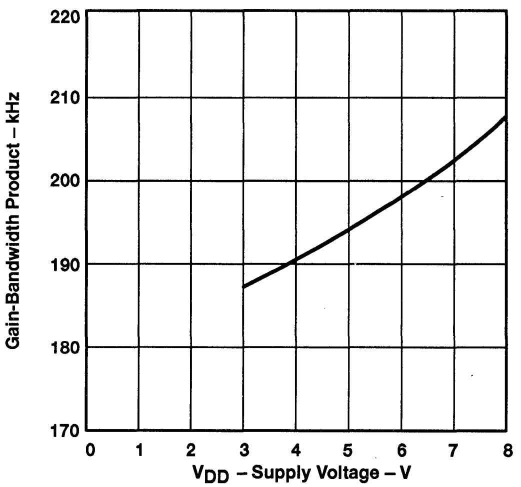


Figure 50

**PHASE MARGIN
vs
LOAD CAPACITANCE**

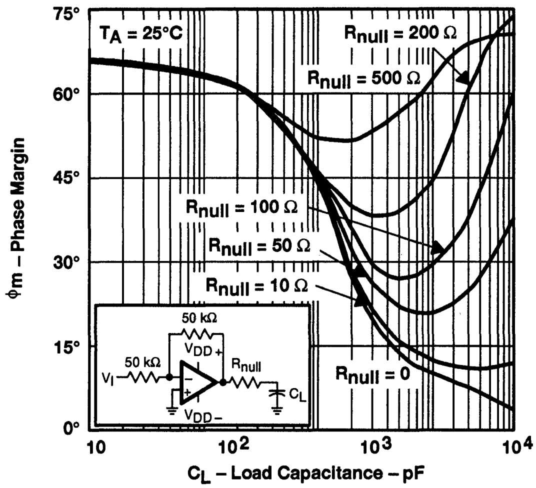


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

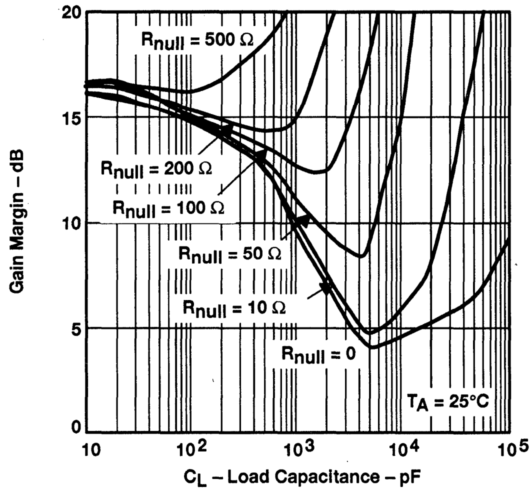


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

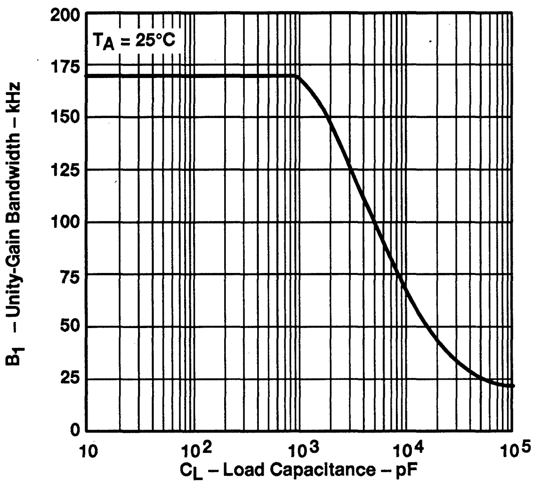
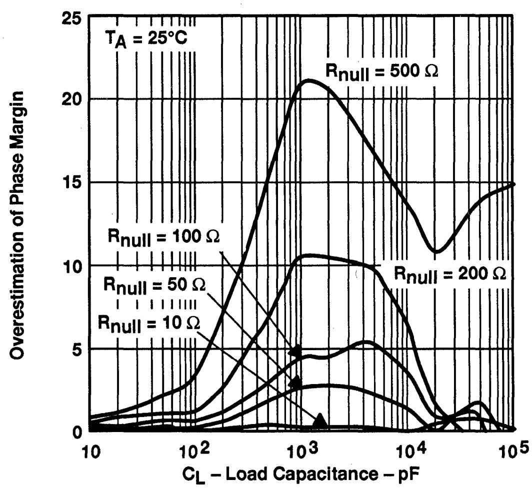


Figure 53

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 54

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

driving large capacitive loads

The TLV2254 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 54) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \quad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 55 with equation (1) enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

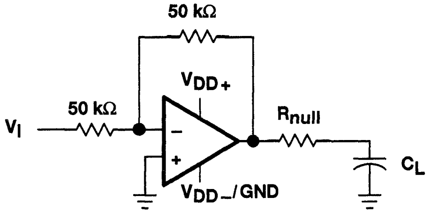


Figure 55. Series-Resistance Circuit

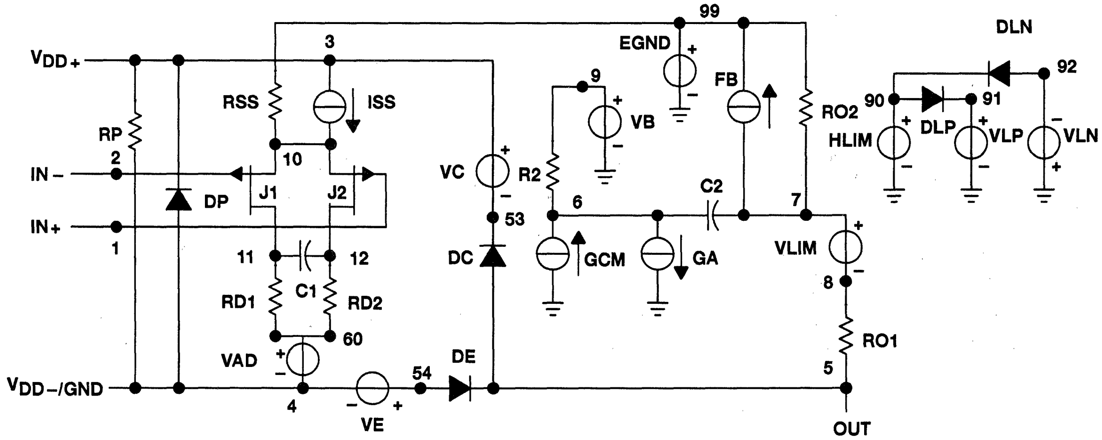
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 56 are generated using the TLV2254 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2254 1 2 3 4 5
C1     11   12   6.369E–12
C2     6    7    25.0E–12
DC     5    53   DX
DE     54   5    DX
DLP    90   91   DX
DLN    92   90   DX
DP     4    3    DX
EGND   99   0    POLY (2) (3,0) (4,0) 0 .5 .5
FB     7    99   POLY (5) VB VC VE VLP
+ VLN 0 57.62E6 –60E6 60E6 60E6 –60E6
GA     6    0    11   12 26.86E–6
GCM    0    6    10   99 2.686E–9
ISS    3    10   DC 3.1E–6
HLIM   90   0    VLIM 1K
J1     11   2    10 JX
J2     12   1    10 JX
R2     6    9    100.0E3
```

```
RD1    60   11   37.23E3
RD2    60   12   37.23E3
R01    8    5    84
R02    7    99   84
RP     3    4    71.43E3
RSS    10   99   64.52E6
VAD    60   4    –.5
VB     9    0    DC 0
VC     3    53   DC .605
VE     54   4    DC .605
VLIM   7    8    DC 0
VLP    91   0    DC –0.235
VLN    0    92   DC 7.5
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=139E–6
+ VTO=–0.05)
.ENDS
```

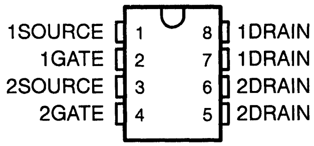
Figure 56. Boyle Macromodel and Subcircuit

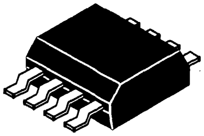
PSpice and *Parts* are trademarks of MicroSim Corporation.

SLVS080 – MARCH 1994

- Low $r_{DS(on)}$ . . . 0.18 Ω at V_{GS} = −10 V
- 3-V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- $V_{GS(th)}$ = −1.5 V Max
- ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015

D PACKAGE
(TOP VIEW)



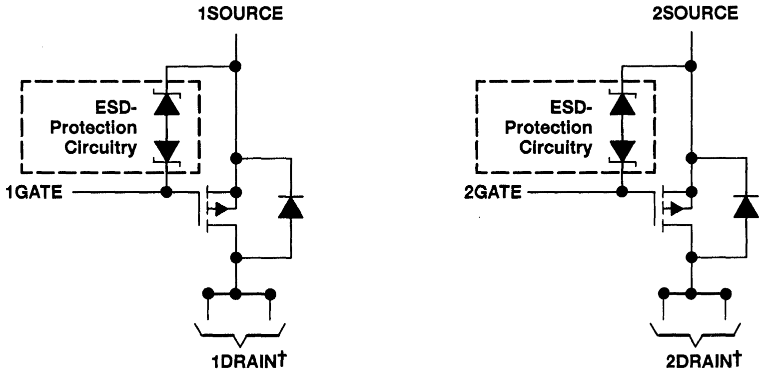


description

The TPS1120 incorporates two independent p-channel enhancement-mode MOSFETs that have been optimized, by means of the Texas Instruments LinBiCMOS™ process, for 3-V or 5-V power distribution in battery-powered systems. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 µA, the TPS1120 is the ideal high-side switch for low-voltage portable battery-management systems, where maximizing battery life is a primary concern. Because portable equipment is potentially subject to electrostatic discharge (ESD), the MOSFETs have built-in circuitry for 2-kV ESD protection. End equipment for the TPS1120 includes notebook computers, personal digital assistants (PDAs), cellular telephones, bar-code scanners, and PCMCIA cards. For existing designs, the TPS1120D has a pinout common with other p-channel MOSFETs in SOIC packages.

The TPS1120 is characterized for an operating junction temperature range, T_J, from −40°C to 150°C. The D package is available taped and reeled. When ordering, add an R suffix to the device-type number (e.g., TPS1120DR).

schematic



† For all applications, both drain pins for each device should be connected.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

absolute maximum ratings, each device, over operating free-air temperature (unless otherwise noted)†

				UNIT
Drain-to-source voltage, V_{DS}			−15	V
Gate-to-source voltage, V_{GS}			2 or −15	V
Continuous drain current, each device (T_J = 150°C), I_D	V_{GS} = −2.7 V	T_A = 25°C	±0.39	A
		T_A = 125°C	±0.21	
	V_{GS} = −3 V	T_A = 25°C	±0.5	
		T_A = 125°C	±0.25	
	V_{GS} = −4.5 V	T_A = 25°C	±0.74	
		T_A = 125°C	±0.34	
	V_{GS} = −10 V	T_A = 25°C	±1.17	
		T_A = 125°C	±0.53	
Pulse drain current, I_{DM}		T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S		T_A = 25°C	−1	A
Continuous total power dissipation		See Dissipation Rating Table		
Storage temperature range, T_{stg}			−55 to 150	°C
Operating junction temperature range, T_J			−40 to 150	°C
Operating free-air temperature range, T_A			−40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le$ 25°C POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	840 mW	6.71 mW/°C	536 mW	436 mW	168 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 149°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	$I_D = -250$ µA		−1	−1.25	−1.50	V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	$I_S = -1$ A,	$V_{GS} = 0$ V			−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V,	$V_{GS} = -12$ V				±100	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V,	$V_{GS} = 0$ V	T_J = 25°C			−0.5	µA
				T_J = 125°C			−10	
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -1.5$ A			180		mΩ
		$V_{GS} = -4.5$ V	$I_D = -0.5$ A			291	400	
		$V_{GS} = -3$ V	$I_D = -0.2$ A			476	700	
		$V_{GS} = -2.7$ V				606	850	
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V,	$I_D = -2$ A			2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q_g	Total gate charge	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -1$ A		5.45		nC
Q_{gs}	Gate-to-source charge			0.87		
Q_{gd}	Gate-to-drain charge			1.4		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_L = 10$ Ω, $I_D = -1$ A, $R_G = 6$ Ω, See Figures 1 and 2		4.5		ns
$t_{d(off)}$	Turn-off delay time			13		ns
t_r	Rise time			10		ns
t_f	Fall time			2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A, di/dt = 100 A/µs		16		

PARAMETER MEASUREMENT INFORMATION

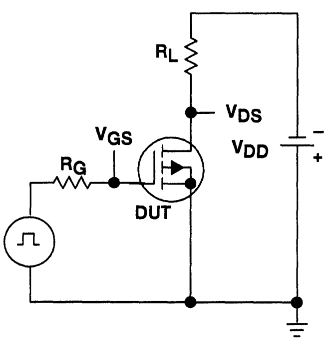


Figure 1. Switching-Time Test Circuit

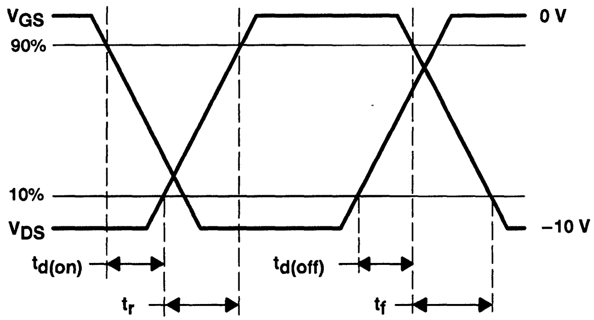


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

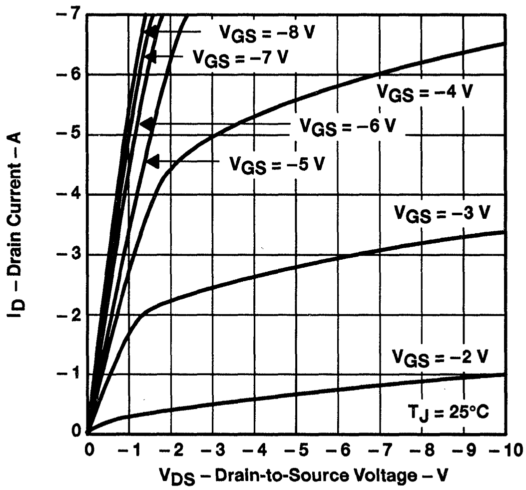


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

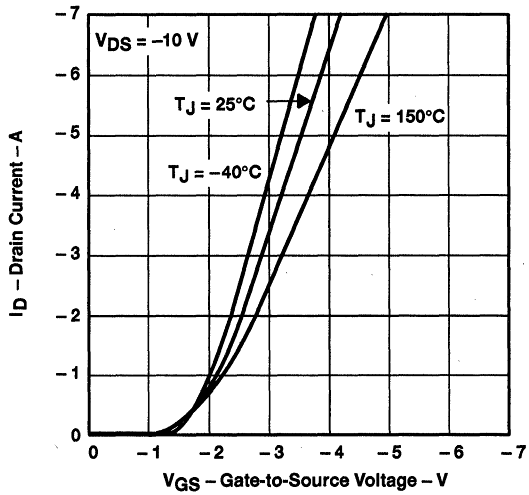


Figure 4

† All characteristics data applies for each independent MOSFET incorporated on the TPS1120.

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

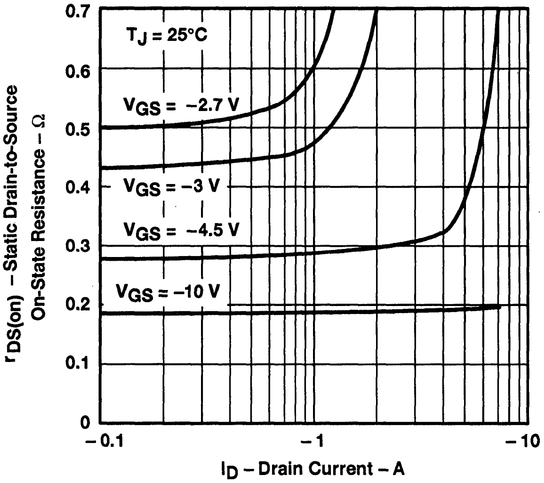
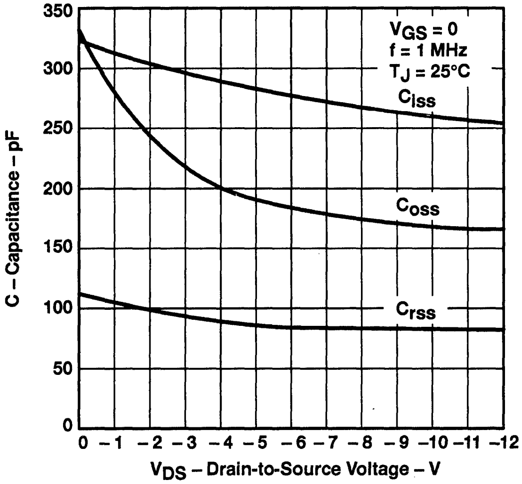


Figure 5

CAPACITANCE† vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

$$C_{rss} = C_{gd},\ C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

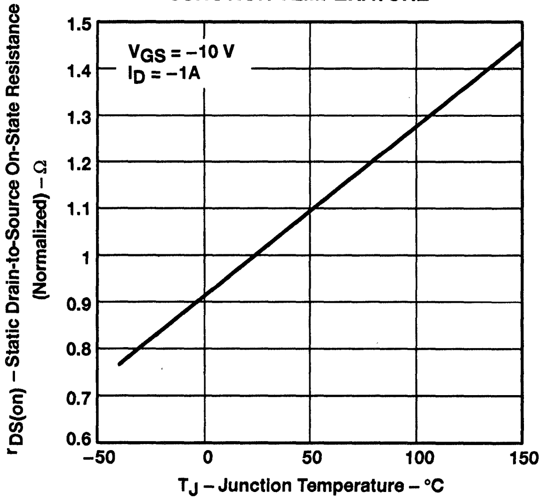


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

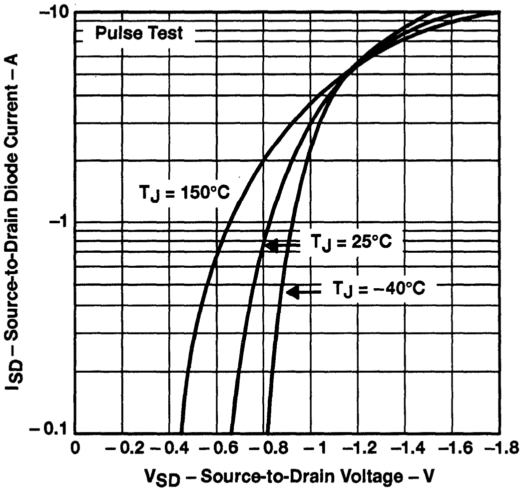


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

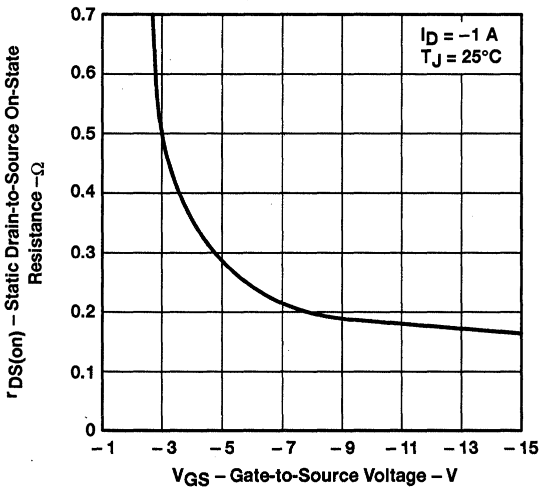


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

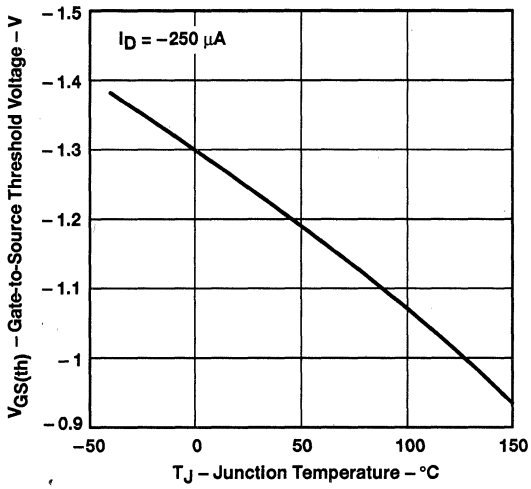


Figure 10

GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

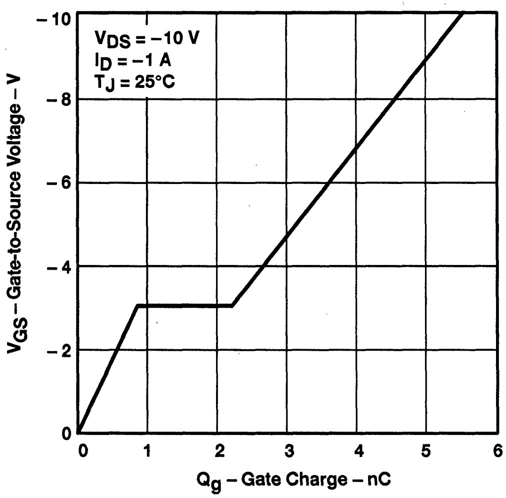


Figure 11

THERMAL INFORMATION

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

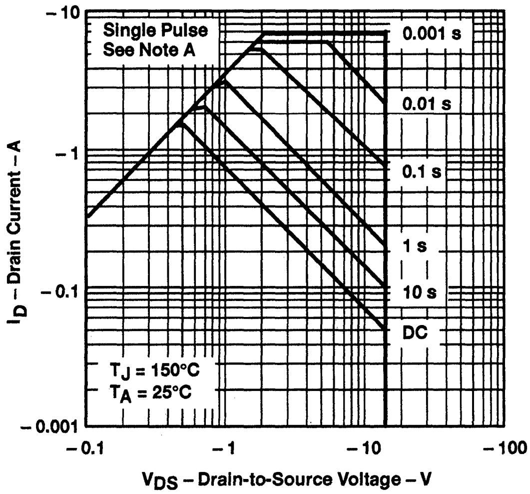


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION

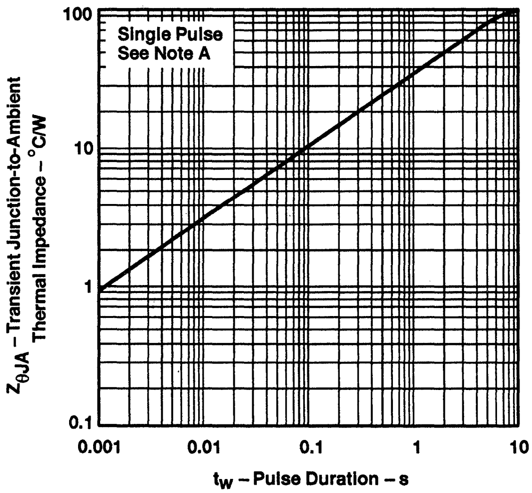


Figure 13

NOTE A: FR4-board-mounted only

THERMAL INFORMATION

The profile of the heat sinks used for thermal measurements is shown in Figure 14. Board type is FR4 with 1-oz copper and 1-oz tin/lead (63/37) plate. Use of vias or through-holes to enhance thermal conduction was avoided.

Figure 15 shows a family of $R_{\theta JA}$ curves. The $R_{\theta JA}$ was obtained for various areas of heat sinks while subject to air flow. Power remained fixed at 0.25 W per device or 0.50 W per package. This testing was done at 25°C.

As Figure 14 illustrates, there are two separated heat sinks for each package. Each heat sink is coupled to the lead that is internally tied to a single MOSFET source and is half the total area in Figure 15. For example, if the total area in Figure 15 is 4 cm², each heat sink is 2 cm².

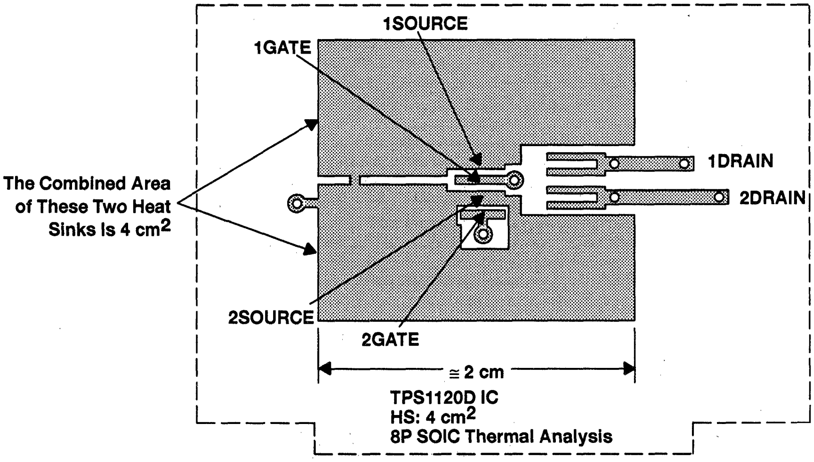


Figure 14. Profile of Heat Sinks

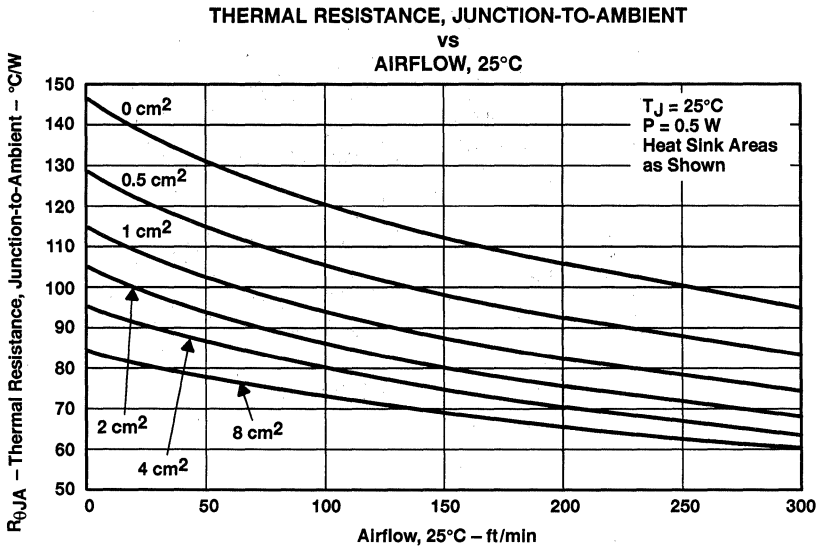


Figure 15

THERMAL INFORMATION

Figure 16 illustrates the thermally enhanced (SO) lead frame. Attaching the two MOSFET dies directly to the source pins allows maximum heat transfer into a power plane.

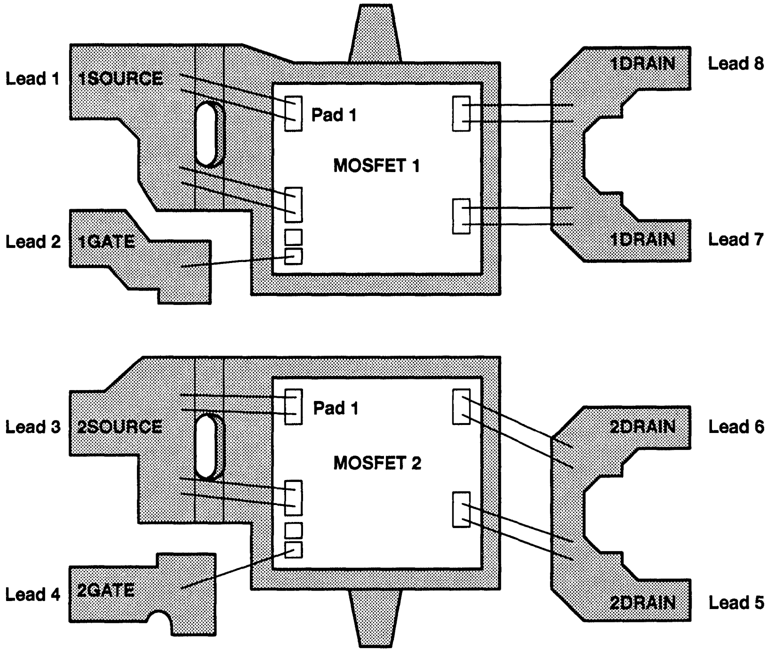


Figure 16. TPS1120 Dual MOSFET SO-8 Lead Frame

APPLICATION INFORMATION

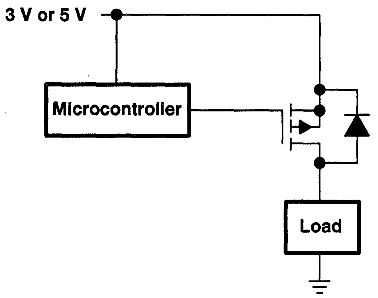


Figure 17. Notebook Load Management

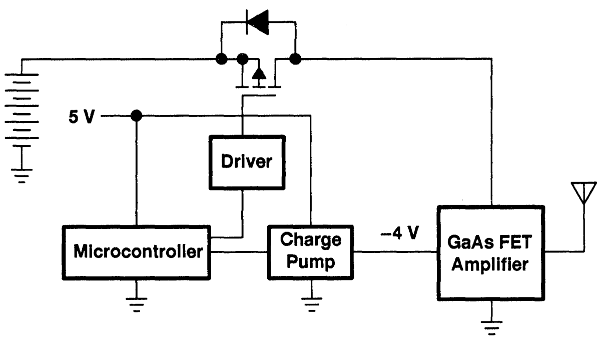
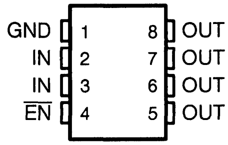


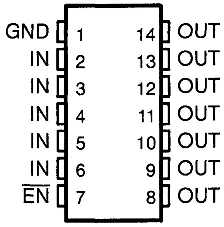
Figure 18. Cellular Phone Output Drive

- **95-mΩ Max (5.5-V Input) High-Side MOSFET Switch With Logic Compatible Enable Input**
- **Short-Circuit and Thermal Protection**
- **Typical Short-Circuit Current Limits: 0.4 A, TPS2010; 1.2 A, TPS2011; 2 A, TPS2012; 2.6 A, TPS2013**
- **Electrostatic-Discharge Protection, 12-kV Output, 6-kV All Other Terminals**
- **Controlled Rise and Fall Times to Limit Current Surges and Minimize EMI**
- **SOIC-8 Package Pin Compatible With the Popular Littlefoot™ Series When GND Is Connected**
- **2.7-V to 5.5-V Operating Range**
- **10-μA Maximum Standby Current**
- **Surface-Mount SOIC-8 and TSSOP-14 Packages**
- **–40°C to 125°C Operating Junction Temperature Range**

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TPS201x family of power-distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ N-channel MOSFET. Gate drive is provided by an internal driver and charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump operates at 100 kHz, requires no external components, and allows operation from supplies as low as 2.7 V. When the output load exceeds the current-limit threshold or a short circuit is present, the TPS201x limits the output current to a safe level by switching into a constant-current mode. Continuous heavy overloads and short circuits increase power dissipation in the switch and cause the junction temperature to rise. If the junction temperature reaches approximately 180°C, a thermal protection circuit shuts the switch off to prevent damage. Recovery from thermal shutdown is automatic once the device has cooled sufficiently.

The members of the TPS201x family differ only in short-circuit current threshold. The TPS2010 is designed to limit at 0.4-A load; the other members of the family limit at 1.2 A, 2 A, and 2.6 A (see the available options table). The TPS201x family is available in SOIC-8 and TSSOP-14 packages and operates over a junction temperature range of –40°C to 125°C. Versions in the SOIC-8 package are drop-in replacements for Siliconix's Littlefoot™ power PMOS switches, except that GND must be connected.

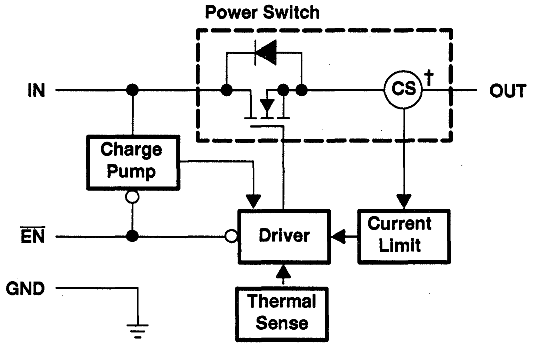
AVAILABLE OPTIONS

T_J	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT OUTPUT CURRENT LIMIT AT 25°C (A)	PACKAGE	
			SOIC (D)†	TSSOP (PW)‡
–40°C to 125°C	0.2	0.4	TPS2010D	TPS2010PWLE
	0.6	1.2	TPS2011D	TPS2011PWLE
	1	2	TPS2012D	TPS2012PWLE
	1.5	2.6	TPS2013D	TPS2013PWLE

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2010DR).
‡ The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2010PWLE).

Littlefoot is a trademark of Siliconix.

functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D	NO. PW		
$\overline{EN}$	4	7	I	Enable input. Logic low turns power switch on.
GND	1	1	I	Ground
IN	2, 3	2–6	I	Input voltage
OUT	5–8	8–14	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 95 mΩ ($V_{I(IN)}$ = 5.5 V), configured as a high-side switch.

charge pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{EN}$)

A logic high on the $\overline{EN}$ input turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

current sense

A sense FET is used to monitor the current supplied to the load. The sense FET is a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit is used to shut the power switch off if the junction temperature rises to approximately 180°C. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) .... –0.3 V to 7 V
Output voltage range, V_O (see Note 1) .... –0.3 V to $V_{I(IN)}$ +0.3 V
Input voltage range, V_I at $\overline{EN}$ .... –0.3 V to 7 V
Continuous output current, I_O .... internally limited
Continuous total power dissipation .... See Dissipation Rating Table
Operating virtual junction temperature range, T_J .... –40°C to 125°C
Storage temperature range .... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$		2.7	5.5	V
Input voltage, V_I at $\overline{EN}$		0	5.5	V
Continuous output current, I_O	TPS2010	0	0.2	A
	TPS2011	0	0.6	
	TPS2012	0	1	
	TPS2013	0	1.5	
Operating virtual junction temperature, T_J		–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
On-state resistance	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C		75	95	mΩ
	$V_{I(IN)}$ = 4.5 V,	T_J = 25°C		80	110	
	$V_{I(IN)}$ = 3 V,	T_J = 25°C		120	175	
	$V_{I(IN)}$ = 2.7 V,	T_J = 25°C		140	215	
Output leakage current	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.001	1	μA
		−40°C ≤ T_J ≤ 125°C			10	
Output rise time	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C, C_L = 1 μF		4		ms
	$V_{I(IN)}$ = 2.7 V,	T_J = 25°C, C_L = 1 μF		3.8		
Output fall time	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C, C_L = 1 μF		3.9		ms
	$V_{I(IN)}$ = 2.7 V,	T_J = 25°C, C_L = 1 μF		3.5		

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
	2.7 V ≤ $V_{I(IN)}$ < 4.5 V			0.4	
Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(IN)}$	−0.5		0.5	μA
Propagation (delay) time, low-to-high-level output	C_L = 1 μF			20	ms
Propagation (delay) time, high-to-low-level output	C_L = 1 μF			40	

current limit

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Short-circuit current	T_J = 25°C, $V_{I(IN)}$ = 5.5 V, OUT connected to GND, device enabled into short circuit	TPS2010	0.22	0.4	0.6	A
		TPS2011	0.66	1.2	1.8	
		TPS2012	1.1	2	3	
		TPS2013	1.65	2.6	4.5	

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply current, low-level output	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.015	1	μA
		−40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73	100	μA
		−40°C ≤ T_J ≤ 125°C			100	

PARAMETER MEASUREMENT INFORMATION

timing diagrams

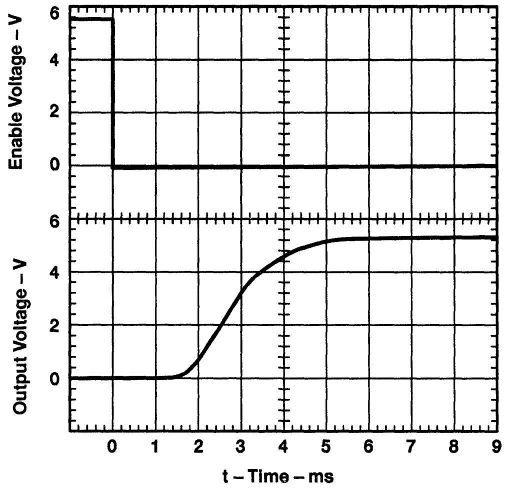


Figure 1. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 5.5 V

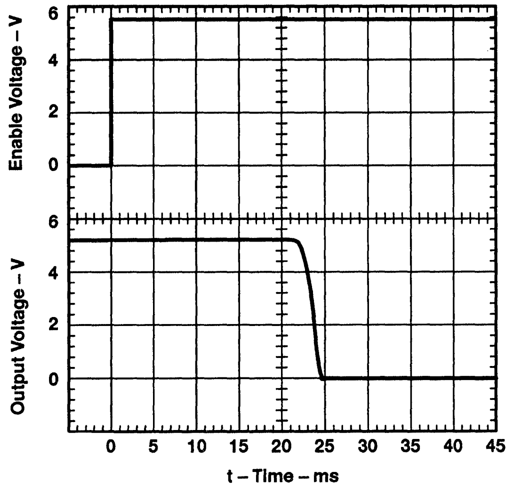


Figure 2. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 5.5 V

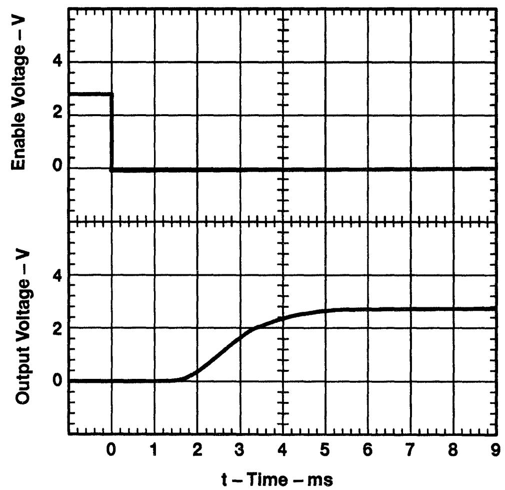


Figure 3. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 2.7 V

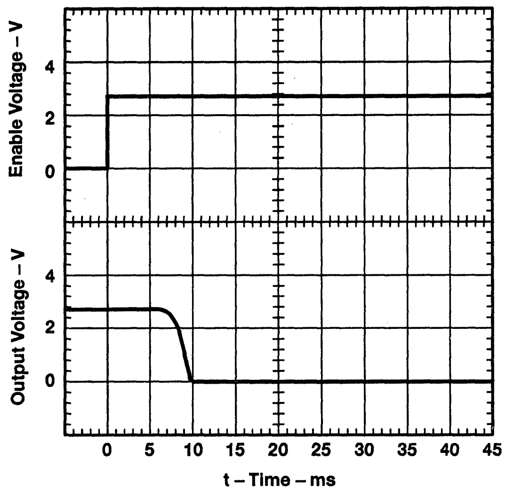


Figure 4. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 2.7 V

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)

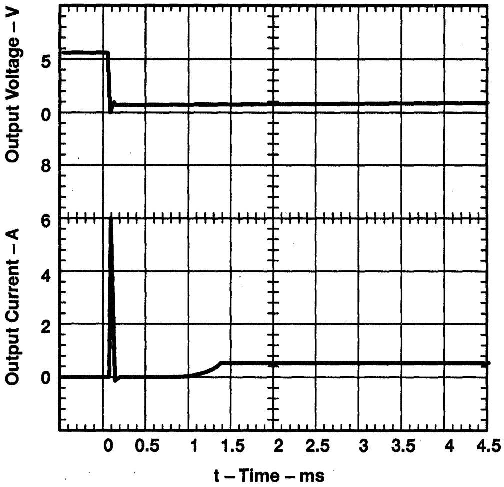


Figure 5. TPS2010, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

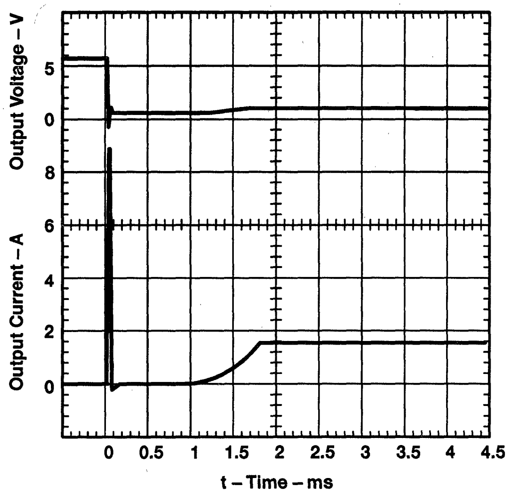


Figure 6. TPS2011, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

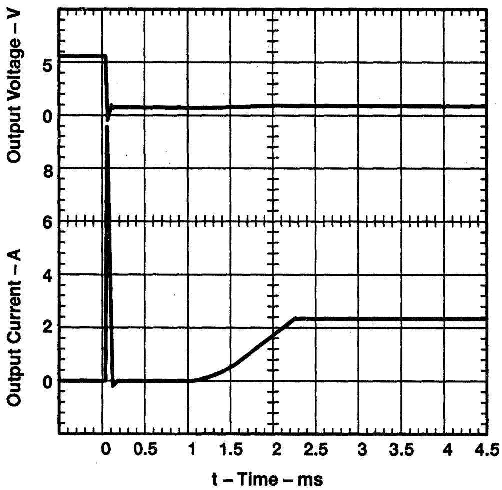


Figure 7. TPS2012, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

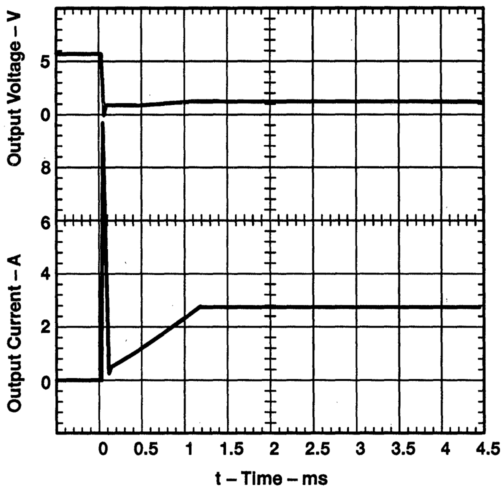


Figure 8. TPS2013 – Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)

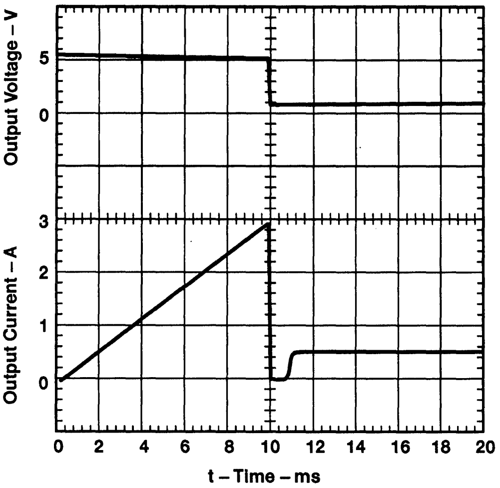


Figure 9. TPS2010 – Threshold Current, $V_{I(IN)}$ = 5.5 V

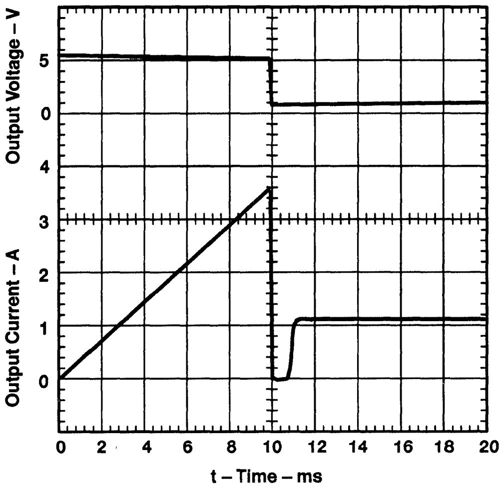


Figure 10. TPS2011 – Threshold Current, $V_{I(IN)}$ = 5.5 V

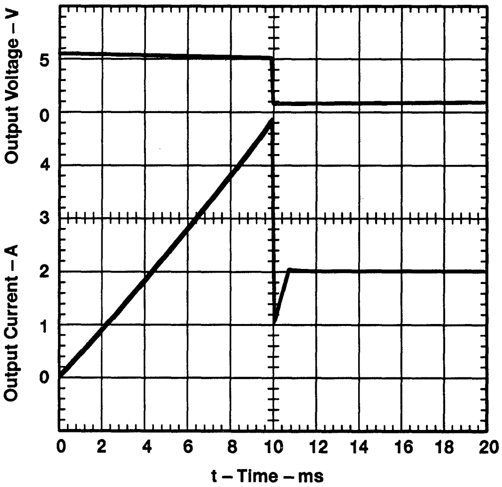


Figure 11. TPS2012 – Threshold Current, $V_{I(IN)}$ = 5.5 V

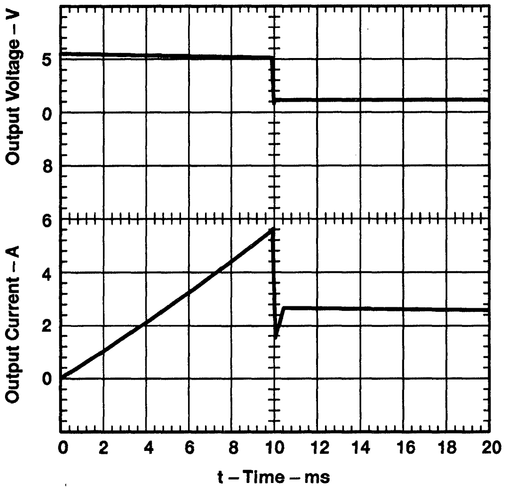


Figure 12. TPS2013 – Threshold Current, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

timing diagrams (continued)

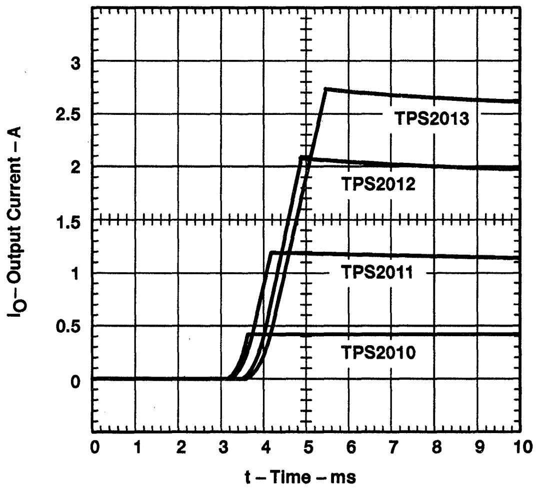
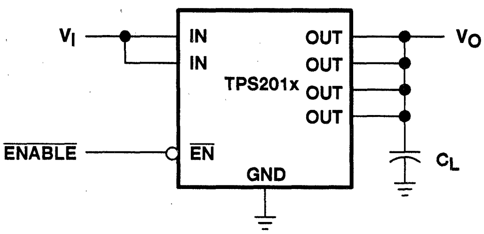
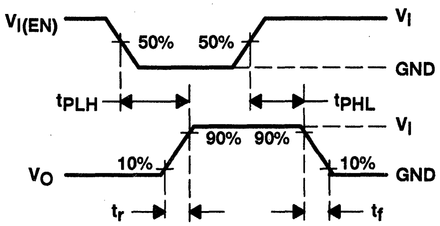


Figure 13. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 14. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TURN-ON DELAY vs INPUT VOLTAGE

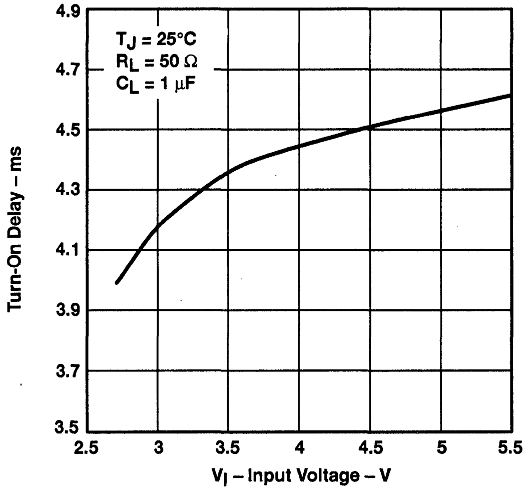


Figure 15

TURN-OFF DELAY vs INPUT VOLTAGE

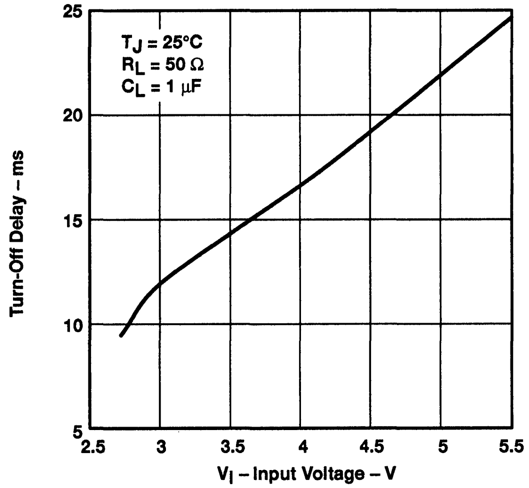


Figure 16

RISE TIME vs OUTPUT CURRENT

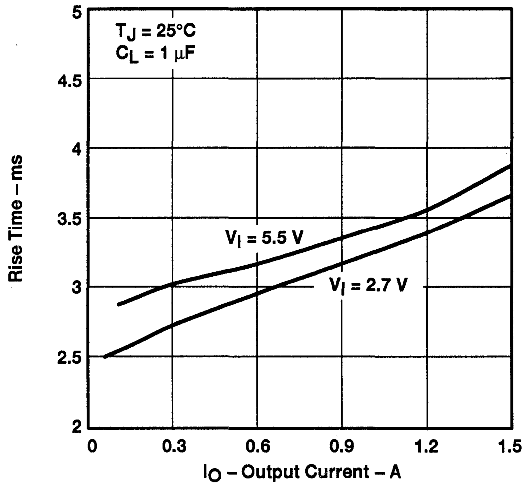


Figure 17

FALL TIME vs OUTPUT CURRENT

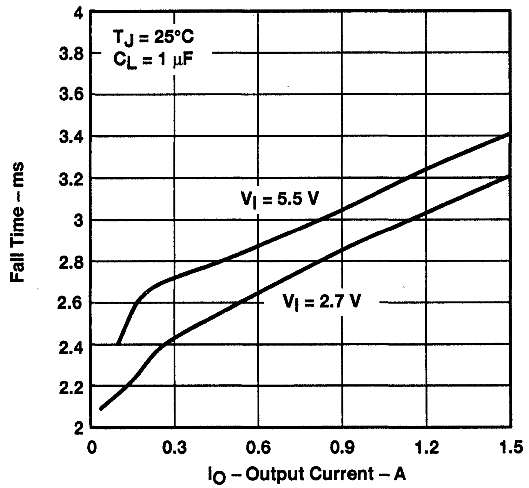


Figure 18

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

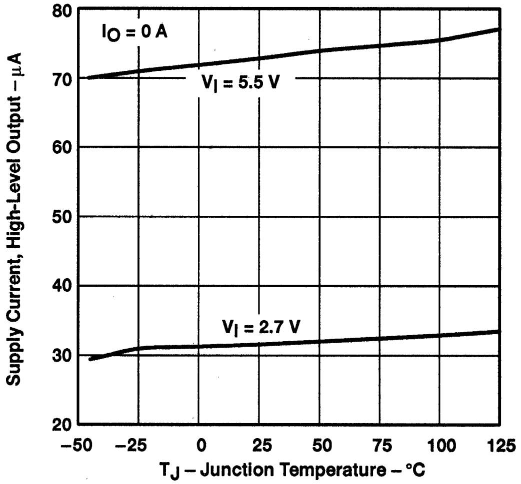


Figure 19

SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

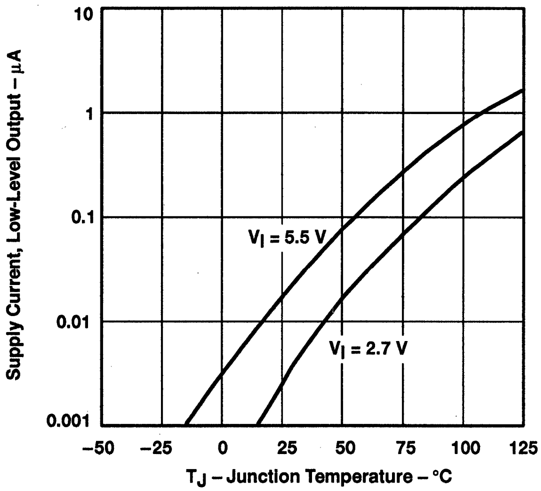


Figure 20

SUPPLY CURRENT, OUTPUT ENABLED vs INPUT VOLTAGE

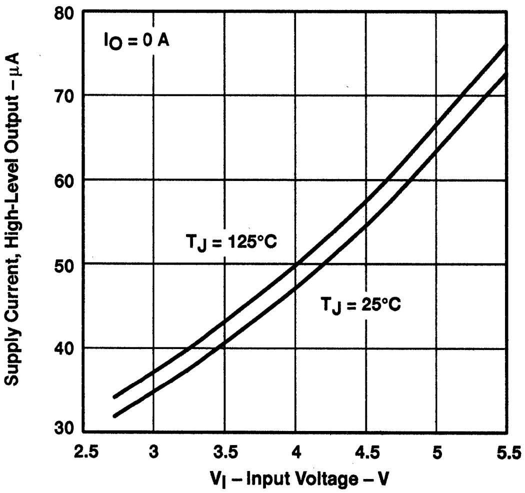


Figure 21

SUPPLY CURRENT, OUTPUT DISABLED vs INPUT VOLTAGE

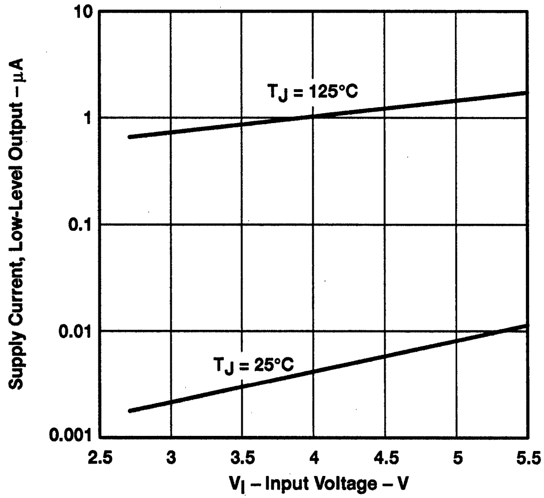


Figure 22

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

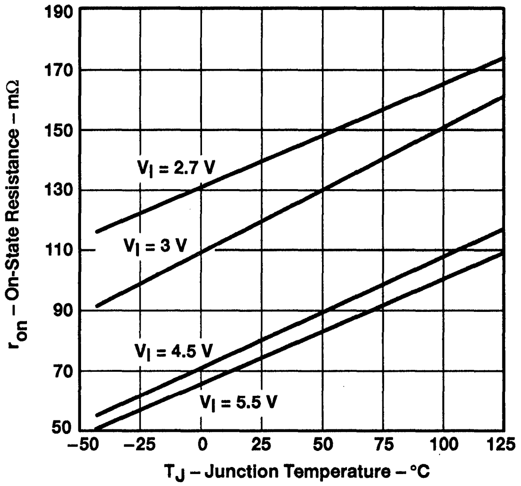


Figure 23

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

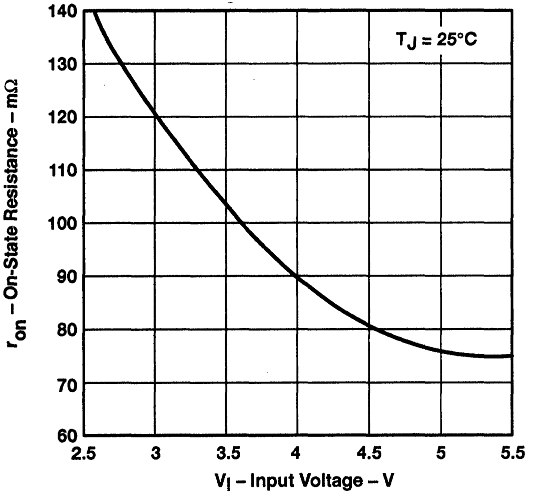


Figure 24

INPUT VOLTAGE TO OUTPUT VOLTAGE
vs
INPUT VOLTAGE

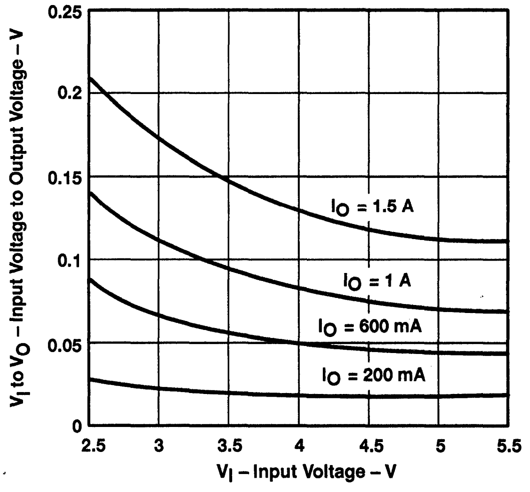


Figure 25

SHORT-CIRCUIT CURRENT
vs
INPUT VOLTAGE

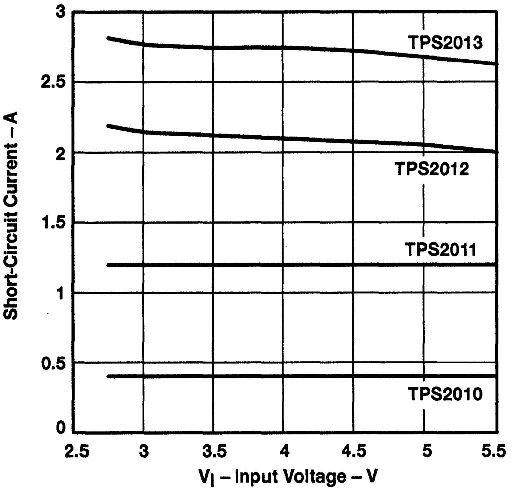


Figure 26

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

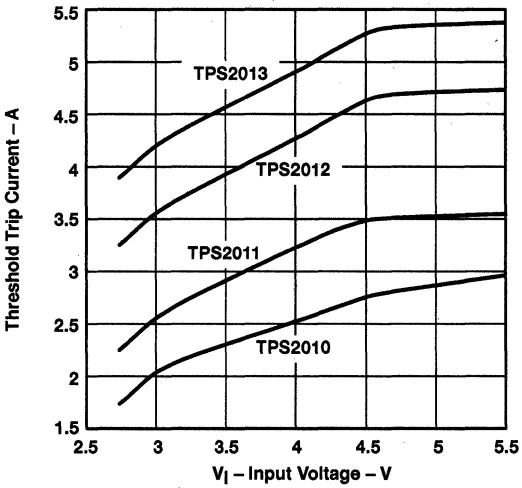


Figure 27

SHORT-CIRCUIT CURRENT vs JUNCTION TEMPERATURE

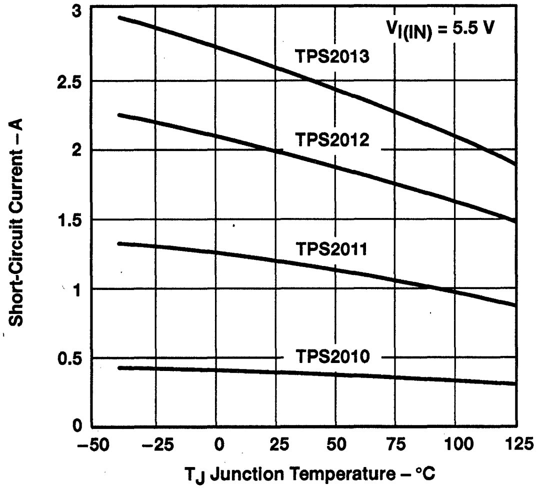


Figure 28

APPLICATION INFORMATION

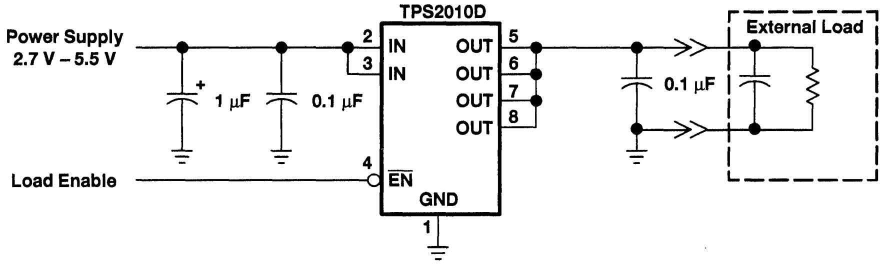


Figure 29. Typical Application

power supply considerations

The TPS201x family has multiple inputs and outputs, which must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.047-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduce the output voltage accordingly. Shutdown only occurs if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 30). The TPS201x senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 5, 6, 7, and 8). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 9, 10, 11, and 12). The TPS201x family is capable of delivering currents up to the current-limit threshold without damage. Once the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

overcurrent (continued)

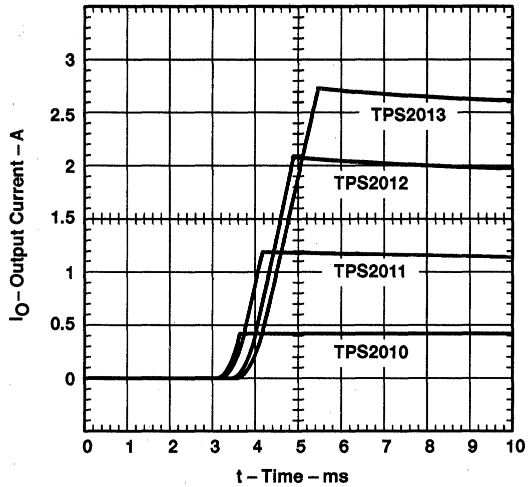


Figure 30. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V

power dissipation and junction temperature

The low on resistance of the N-channel MOSFET allows small surface-mount packages, such as SOIC or TSSOP to pass large currents. The thermal resistances of these packages is high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and and read r_{on} from Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, TSSOP = 179°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations is generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

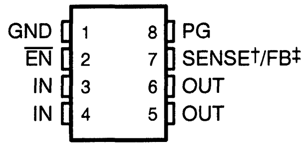
Thermal protection is provided to prevent damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201x into its constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or input power is removed.

ESD protection

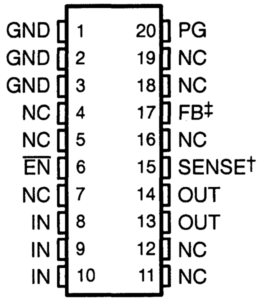
All TPS201x terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

- **Available in 5-V, 4.85-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Very Low-Dropout Voltage . . . Maximum of 32 mV at I_O = 100 mA (TPS7150)**
- **Very Low Quiescent Current – Independent of Load . . . 285 μA Typ**
- **Extremely Low Sleep-State Current 0.5 μA Max**
- **2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions**
- **Output Current Range of 0 mA to 500 mA**
- **TSSOP Package Option Offers Reduced Component Height for Critical Applications**
- **Power Good (PG) Status Output**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC – No internal connection
† SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
‡ FB – Adjustable version only (TPS7101)

description

The TPS71xx integrated circuits are a family of micropower low-dropout (LDO) voltage regulators. An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 32 mV at an output current of 100 mA for the TPS7150) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and remains independent of output loading (typically 285 μA over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. The LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at T_J = 25°C.

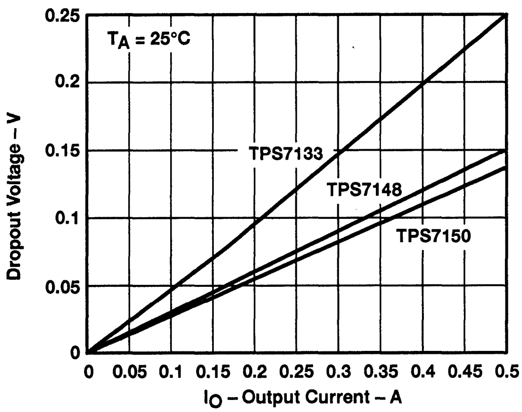


Figure 1. Dropout Voltage Versus Output Current

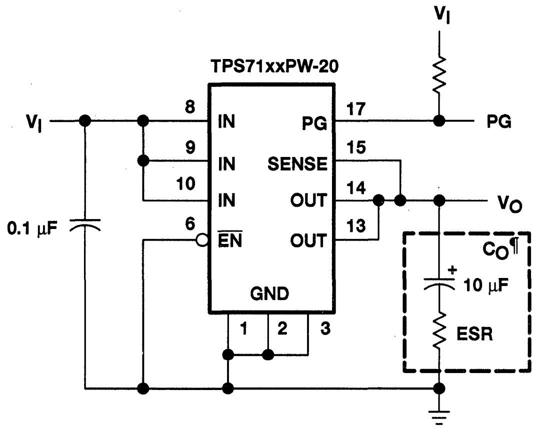
Power good (PG) reports low output voltage and can be used to implement a power-on reset or a low-battery indicator.

The TPS71xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS71xx family is available in PDIP (8 pin), SO (8 pin), and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

AVAILABLE OPTIONS

PART NUMBER	OUTPUT VOLTAGE			UNIT
	MIN	TYP	MAX	
TPS7150QPWLE†	4.9	5	5.1	V
TPS7150QD‡				
TPS7150QP				
TPS7148QPWLE†	4.75	4.85	4.95	V
TPS7148QD‡				
TPS7148QP				
TPS7133QPWLE†	3.23	3.3	3.37	V
TPS7133QD‡				
TPS7133QP				
TPS7101QPWLE†	Adjustable§ 1.2 V to 9.75 V			V
TPS7101QD‡				
TPS7101QP				

† The PW package is only available left-end taped and reeled.
‡ The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7150QDR).
§ The TPS7101Q is programmable using an external resistor divider (see application information).



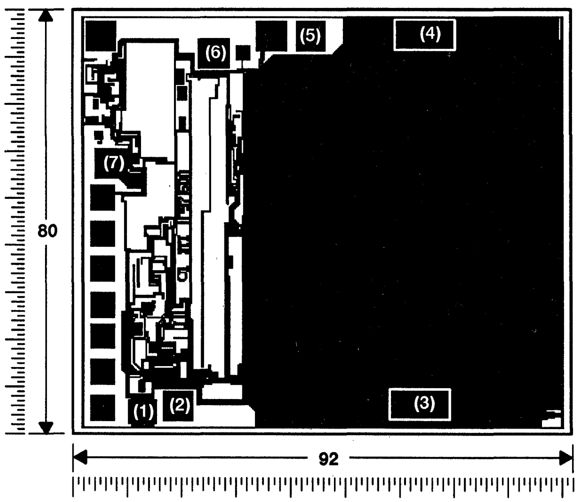
¶ Capacitor selection is nontrivial. See application information section for details.

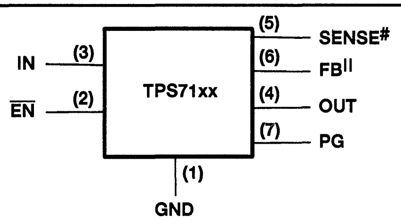
Figure 2. Typical Application Configuration

TPS71xx chip information

Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pad. Chips can be mounted with conductive epoxy or a gold-silicon preform. Contact factory for die sales.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

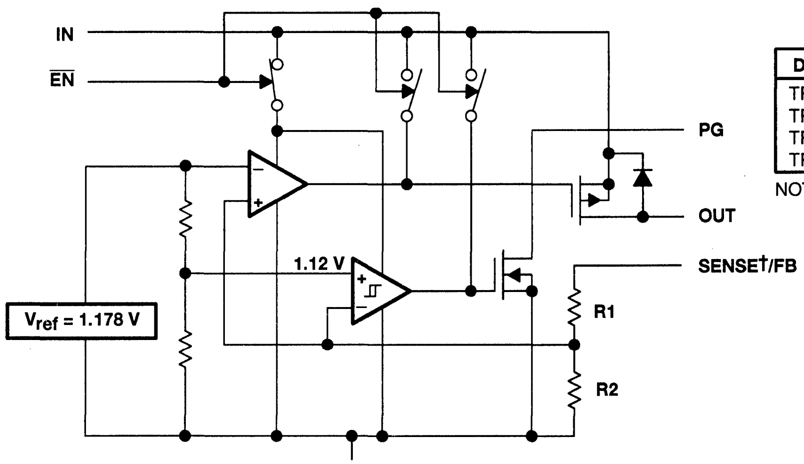
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

SENSE – Fixed voltage options only (TPS7133, TPS7148, and TPS7150)
|| FB – Adjustable version only (TPS7101)

NOTE: For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the applications information section of this data sheet.

functional block diagram



RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7101	0	∞	Ω
TPS7133	420	233	kΩ
TPS7148	726	233	kΩ
TPS7150	756	233	kΩ

NOTE: Resistors are nominal values only.

† For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range§, V_I, PG, SENSE, $\overline{EN}$ .... –0.3 to 10 V
Output current, I_O .... 2 A
Continuous total power dissipation .... See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J .... –55°C to 150°C
Storage temperature range .... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
§ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW¶	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 70°C POWER RATING	T_C = 125°C POWER RATING
D	2188 mW	17.5 mW/°C	1400 mW	438 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW¶	4025 mW	32.2 mW/°C	2576 mW	805 mW

¶ Refer to thermal information section for detailed power dissipation considerations when using the TSSOP package.

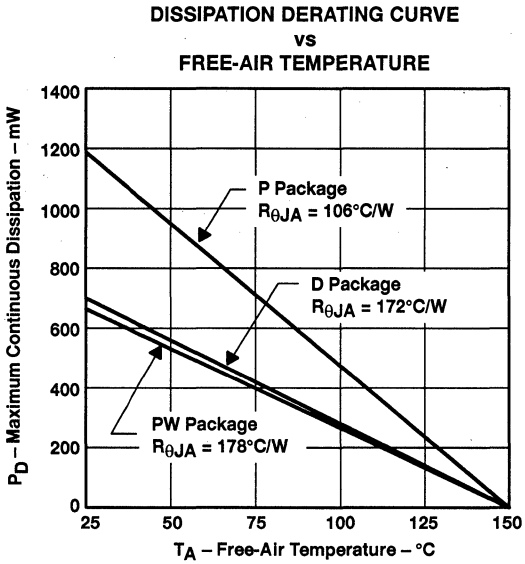


Figure 3

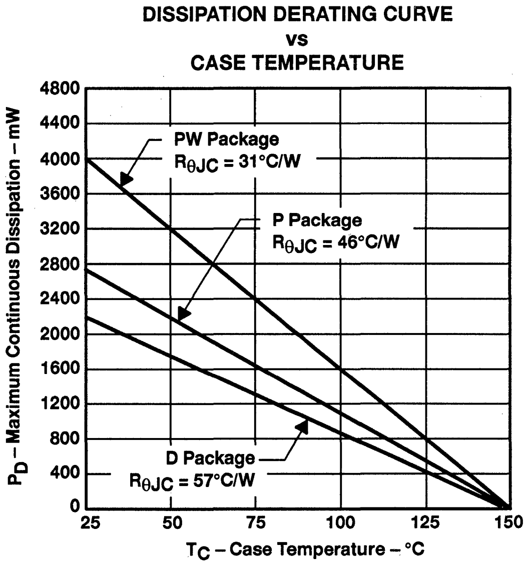


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7101Q	2.5	10	V
	TPS7133Q	3.77	10	
	TPS7148Q	5.2	10	
	TPS7150Q	5.33	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current range, I_O		0	500	mA
Operating virtual junction temperature range, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7101 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7101.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	T_J	MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 500 mA	25°C		285	350	µA
		−40°C to 125°C			460	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	µA
		−40°C to 125°C			2	
Output current limit	V_O = 0 V, V_I = 10 V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C			0.5	µA
		−40°C to 125°C			1	
PG leakage current	Normal operation, V_{PG} = 10 V	25°C		0.02	0.5	µA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5		0.5	µA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid PG	I_{PG} = 300 µA	25°C		1.06	1.5	V
		−40°C to 125°C			1.9	

† ESR refers to the equivalent resistance, including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7101Q electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Reference voltage (measured at FB with OUT connected to FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.178		V
	2.5 V ≤ V_I ≤ 10 V, See Note 1	5 mA ≤ I_O ≤ 500 mA,	–40°C to 125°C	1.143		1.213	V
Reference voltage temperature coefficient			–40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V,	50 µA ≤ I_O ≤ 150 mA	25°C		0.7	1	Ω
			–40°C to 125°C			1	
	V_I = 2.4 V,	150 mA ≤ I_O ≤ 500 mA	25°C		0.83	1.3	
			–40°C to 125°C			1.3	
	V_I = 2.9 V,	50 µA ≤ I_O ≤ 500 mA	25°C		0.52	0.85	
			–40°C to 125°C			0.85	
	V_I = 3.9 V,	50 µA ≤ I_O ≤ 500 mA	25°C		0.32		
	V_I = 5.9 V,	50 µA ≤ I_O ≤ 500 mA	25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, See Note 1	50 µA ≤ I_O ≤ 500 mA,	25°C			18	mV
			–40°C to 125°C			25	
Output regulation	I_O = 5 mA to 500 mA, See Note 1	2.5 V ≤ V_I ≤ 10 V,	25°C			14	mV
			–40°C to 125°C			25	
	I_O = 50 µA to 500 mA, See Note 1	2.5 V ≤ V_I ≤ 10 V,	25°C			22	mV
			–40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	48	59		dB
			–40°C to 125°C	44			
		I_O = 500 mA, See Note 1	25°C	45	54		
			–40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		95		µVrms
		C_O = 10 µF	25°C		89		
		C_O = 100 µF	25°C		74		
PG trip-threshold voltage§	V_{FB} voltage decreasing from above V_{PG}		–40°C to 125°C	0.92 × $V_{FB(nom)}$		0.98 × $V_{FB(nom)}$	V
PG hysteresis voltage§	Measured at V_{FB}		25°C		12		mV
PG output low voltage§	I_{PG} = 400 µA,	V_I = 2.13 V	25°C		0.1	0.4	V
			–40°C to 125°C			0.4	
FB input current			25°C	–10	0.1	10	nA
			–40°C to 125°C	–20		20	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 31) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

2. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figure 30.

TPS7133Q electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		0.02	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		47	60	
			−40°C to 125°C			80	
	I_O = 500 mA,	V_I = 3.23 V	25°C		235	300	
			−40°C to 125°C			400	
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 500 mA	V_I = 3.23 V,	25°C		0.47	0.6	Ω
			−40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			20	mV
			−40°C to 125°C			27	
Output regulation	I_O = 5 mA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	38	mV
			−40°C to 125°C			75	
	I_O = 50 µA to 500 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		30	60	mV
			−40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	43	54		dB
			−40°C to 125°C	40			
		I_O = 500 mA	25°C	39	49		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		274		µVrms
		C_O = 10 µF	25°C		228		
		C_O = 100 µF	25°C		159		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		35		mV
PG output low voltage	I_{PG} = 1 mA,	V_I = 2.8 V	25°C		0.22	0.4	V
			−40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7148Q electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.85 V,	I_O = 10 mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	–40°C to 125°C	4.75		4.95	
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V	25°C		0.08	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.75 V	25°C		30	37	
			–40°C to 125°C			54	
	I_O = 500 mA,	V_I = 4.75 V	25°C		150	180	
			–40°C to 125°C			250	
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 500 mA	V_I = 4.75 V,	25°C		0.32	0.35	Ω
			–40°C to 125°C			0.52	
Input regulation	V_I = 5.85 V to 10 V,	50 μA ≤ I_O ≤ 500 mA	25°C			27	mV
			–40°C to 125°C			37	
Output regulation	I_O = 5 mA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		12	42	mV
			–40°C to 125°C			80	
	I_O = 50 μA to 500 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		42	60	mV
			–40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	42	53		dB
			–40°C to 125°C	39			
		I_O = 500 mA	25°C	39	50		
			–40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 μF	25°C		410		μVrms
		C_O = 10 μF	25°C		328		
		C_O = 100 μF	25°C		212		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		–40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		50		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.12 V	25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7150Q electrical characteristics at I_O = 10 mA, V_I = 6 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF/ESR† = 1 Ω, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V,	I_O = 10 mA	25°C		5		V
	6 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 500 mA	−40°C to 125°C	4.9		5.1	
Dropout voltage	I_O = 10 mA,	V_I = 4.88 V	25°C		0.13	6	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.88 V	25°C		27	32	
			−40°C to 125°C			47	
	I_O = 500 µA,	V_I = 4.88 V	25°C		146	170	
			−40°C to 125°C			230	
Pass-element series resistance	(4.88 V − V_O)/I_O, I_O = 500 mA	V_I = 4.88 V.	25°C		0.29	0.32	Ω
			−40°C to 125°C			0.47	
Input regulation	V_I = 6 V to 10 V,	50 µA ≤ I_O ≤ 500 mA	25°C			25	mV
			−40°C to 125°C			32	
Output regulation	I_O = 5 mA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		30	45	mV
			−40°C to 125°C			86	
	I_O = 50 µA to 500 mA,	6 V ≤ V_I ≤ 10 V	25°C		45	65	mV
			−40°C to 125°C			140	
Ripple rejection	f = 120 Hz	I_O = 50 µA	25°C	45	55		dB
			−40°C to 125°C	40			
		I_O = 500 mA	25°C	42	52		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, ESR† = 1 Ω	C_O = 4.7 µF	25°C		430		µVrms
		C_O = 10 µF	25°C		345		
		C_O = 100 µF	25°C		220		
PG trip-threshold voltage	V_O voltage decreasing from above V_{PG}		−40°C to 125°C	0.92 × $V_{O(nom)}$		0.98 × $V_{O(nom)}$	V
PG hysteresis voltage			25°C		53		mV
PG output low voltage	I_{PG} = 1.2 mA,	V_I = 4.25 V	25°C		0.2	0.4	V
			−40°C to 125°C			0.4	

† ESR refers to the equivalent resistance including internal resistance and series resistance.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 5 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 6. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board (L × W × H = 3.2 inch × 3.2 inch × 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

Figure 7 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m · °C.

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature or 125°C.

This limit should then be applied to the internal power dissipated by the TPS71xx regulator. The equation for calculating total internal power dissipation of the TPS71xx is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS71xx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O$$

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where T_A = 55°C, airflow = 100 ft/min, copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 7, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{94°C/W} = 745 \text{ mW}$$

If the system implements a TPS7148 regulator where V_I = 6 V and I_O = 385 mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

THERMAL INFORMATION

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

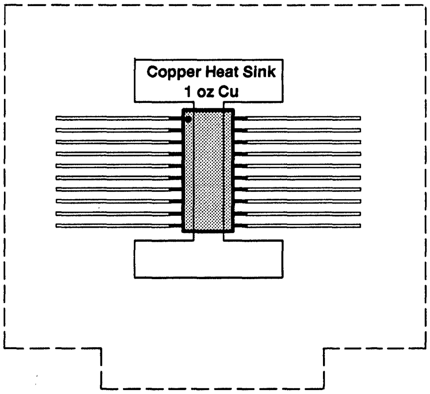


Figure 5. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

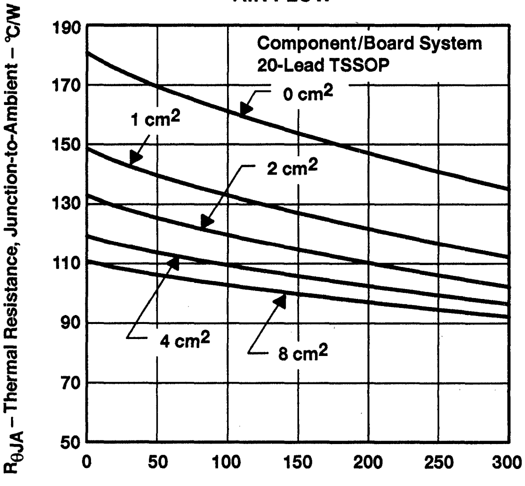


Figure 6

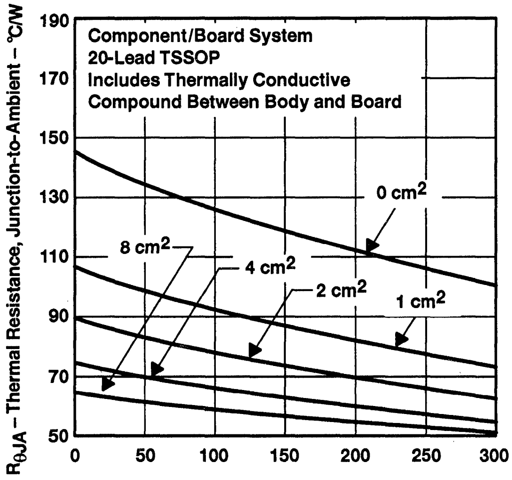


Figure 7

APPLICATION INFORMATION

The TPS71xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier-generation LDOs, while adding features such as a power-saving shutdown mode and a power-good indicator. The TPS71xx family includes three fixed-output voltage regulators: the TPS7133 (3.3 V), the TPS7148 (4.85 V), and the TPS7150 (5 V). The family also offers an adjustable device, the TPS7101 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS71xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that those devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS71xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS71xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS71xx quiescent current remains low even when the regulator drops out, eliminating both problems.

Included in the TPS71xx family is a 4.85-V regulator, the TPS7148. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within ± 2%, allows for operation within the low-end limit of 5-V systems specified to ± 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS71xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2 μA. If the shutdown feature is not used, $\overline{\text{EN}}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS71xx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE pin of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection if the TPS71xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS71xx family requires an output capacitor for stability. A low-ESR 10-μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 8). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-μF devices can be screened for ESR. Figures 39 through 46 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 μF), the output capacitance can be reduced to 4.7 μF, provided ESR is maintained between 0.7 and 2.5 Ω. Because minimum capacitor ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As show in the ESR graphs (Figures 39 through 46), minimum ESR is not a problem when using 10-μF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS71xx family. This information (along with the ESR graphs, Figures 39 through 46) is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)

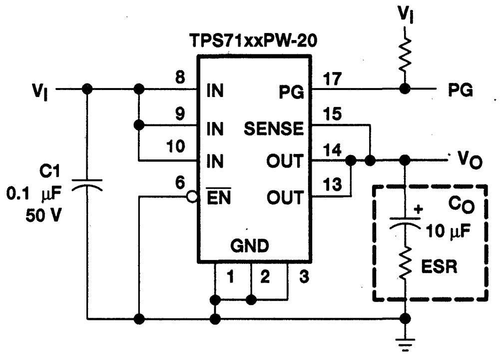


Figure 8. Typical Application Circuit

programming the TPS7101 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 9. The equation governing the output voltage is:

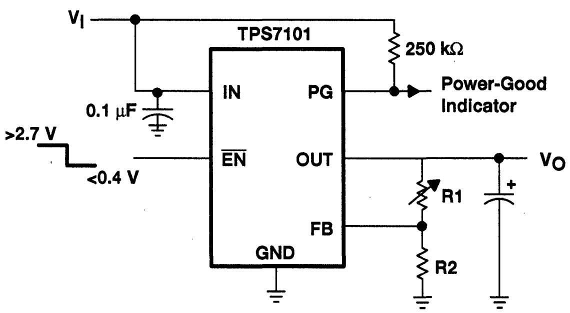
$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

V_{ref} = reference voltage, 1.178 V typ

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 9. TPS7101 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power-good indicator

The TPS71xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

regulator protection

The TPS71xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS71xx also features internal current limiting and thermal protection. During normal operation, the TPS71xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_Q	Quiescent current	vs Output current	10
		vs Input voltage	11
		vs Free-air temperature	12
V_{DO}	Dropout voltage	vs Output current	13
ΔV_{DO}	Change in dropout voltage	vs Free-air temperature	14
ΔV_O	Change in output voltage	vs Free-air temperature	15
V_O	Output voltage	vs Input voltage	16
ΔV_O	Change in output voltage	vs Input voltage	17
V_O	Output voltage	vs Output current	18
			19
			20
			21
	Ripple rejection	vs Frequency	22
			23
			24
			25
	Noise	vs Frequency	26
			27
			28
			29
$r_{DS(on)}$	Pass-element resistance	vs Input voltage	30
R	Divider resistance	vs Free-air temperature	31
$I_{I(SENSE)}$	SENSE current	vs Free-air temperature	32
	FB leakage current	vs Free-air temperature	33
V_I	Minimum input voltage for active-pass element	vs Free-air temperature	34
	Minimum input voltage for valid PG	vs Free-air temperature	35
$I_{I(EN)}$	Input current (EN)	vs Free-air temperature	36
	Output voltage response from Enable ($\overline{EN}$)		37
V_{PG}	Power-good (PG) voltage	vs Output voltage	38
	ESR total equivalent resistance	vs Output current	39
			40
	ESR total equivalent resistance	vs Ceramic capacitance	41
			42
	ESR total equivalent resistance	vs Output current	43
			44
	ESR total equivalent resistance	vs Ceramic capacitance	45
			46

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs OUTPUT CURRENT

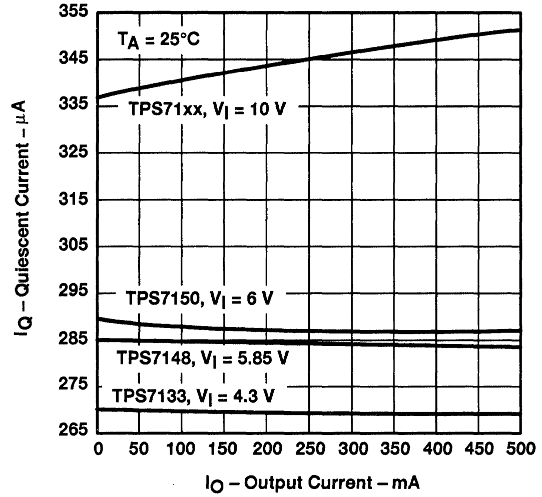


Figure 10

QUIESCENT CURRENT vs INPUT VOLTAGE

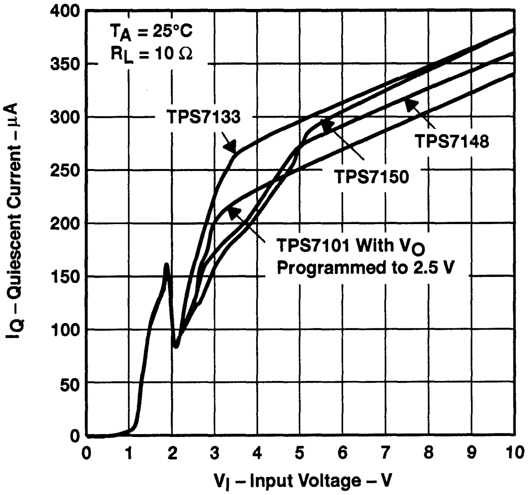


Figure 11

TPS7148Q QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

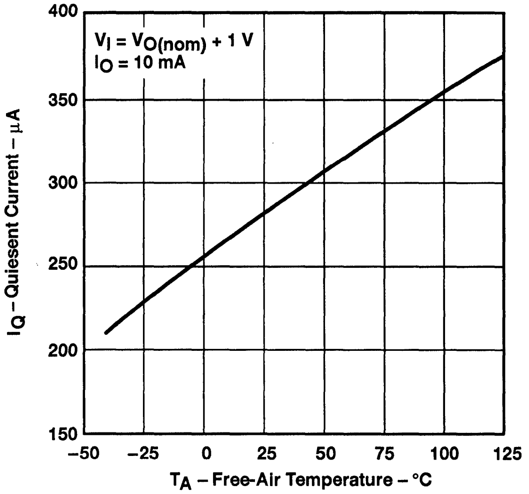


Figure 12

DROPOUT VOLTAGE vs OUTPUT CURRENT

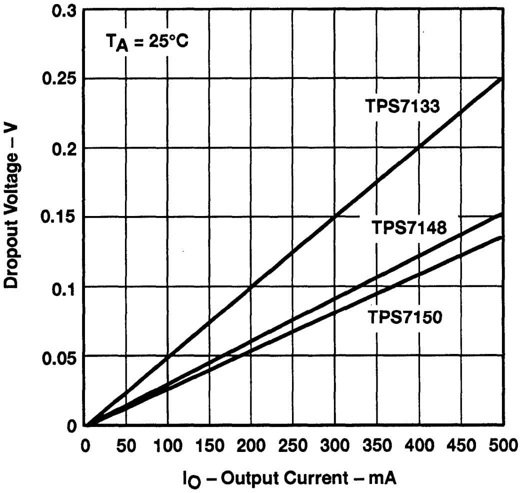


Figure 13

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

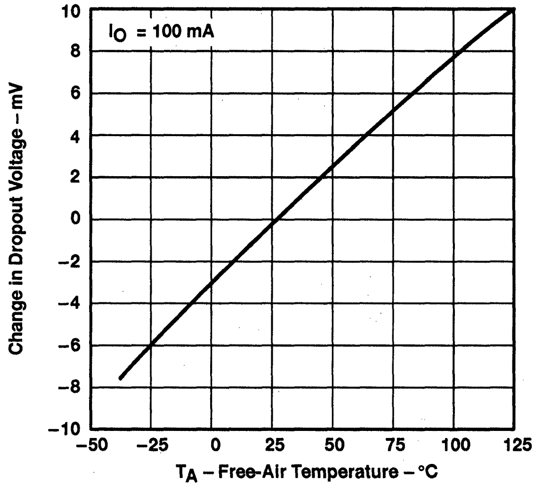


Figure 14

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

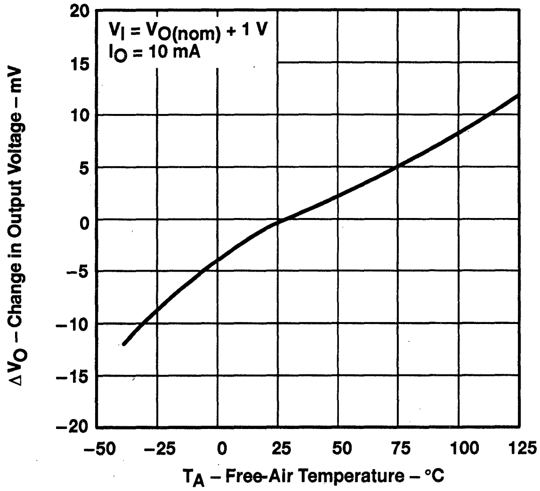


Figure 15

OUTPUT VOLTAGE vs INPUT VOLTAGE

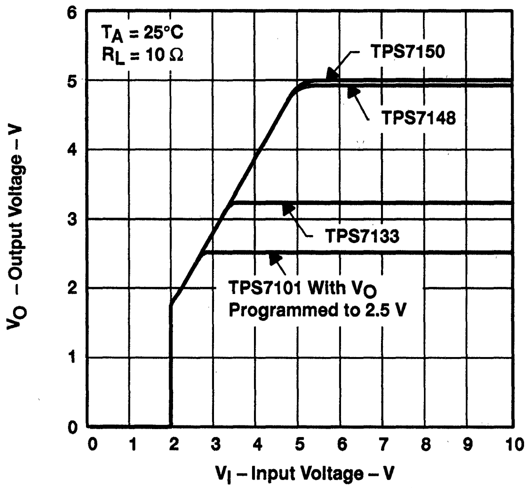


Figure 16

CHANGE IN OUTPUT VOLTAGE vs INPUT VOLTAGE

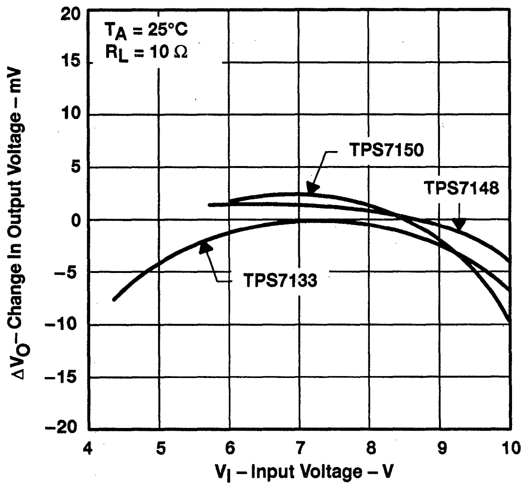


Figure 17

TYPICAL CHARACTERISTICS

TPS7101Q OUTPUT VOLTAGE vs OUTPUT CURRENT

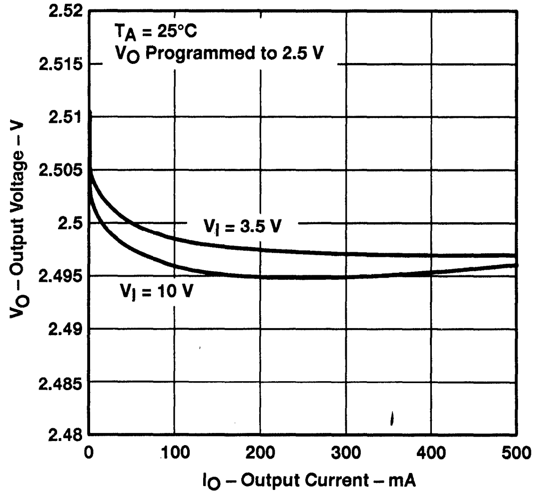


Figure 18

TPS7133Q OUTPUT VOLTAGE vs OUTPUT CURRENT

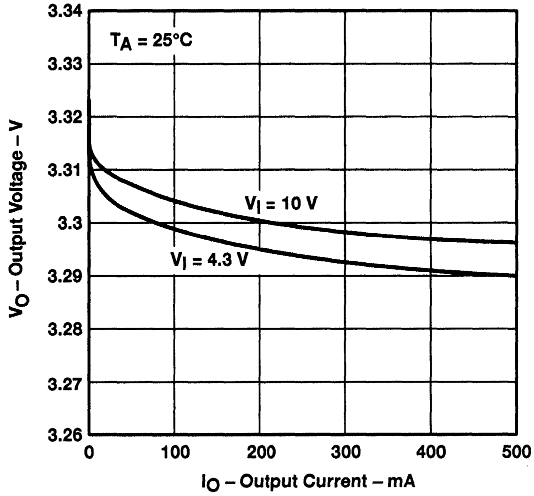


Figure 19

TPS7148Q OUTPUT VOLTAGE vs OUTPUT CURRENT

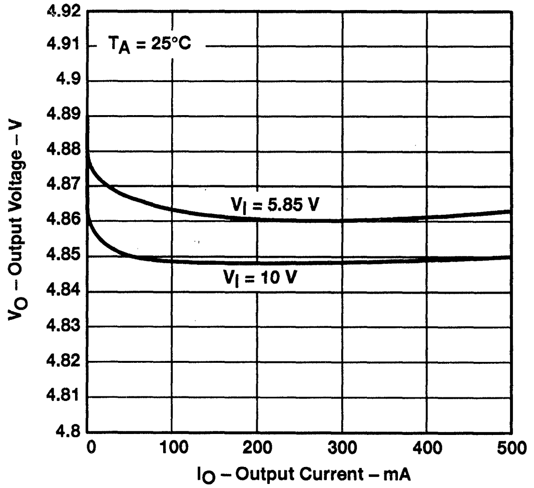


Figure 20

TPS7150Q OUTPUT VOLTAGE vs OUTPUT CURRENT

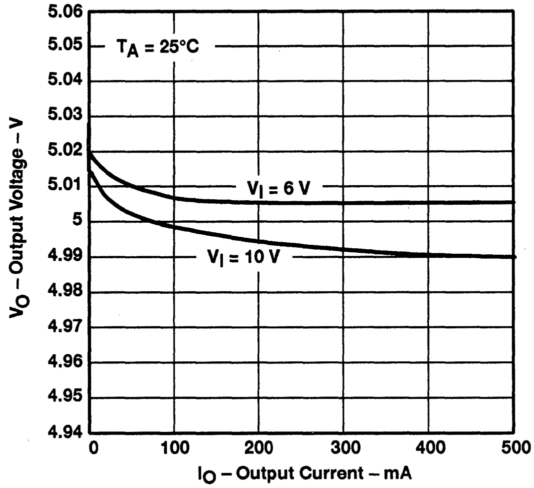


Figure 21

TYPICAL CHARACTERISTICS

TPS7101Q
RIPPLE REJECTION
vs
FREQUENCY

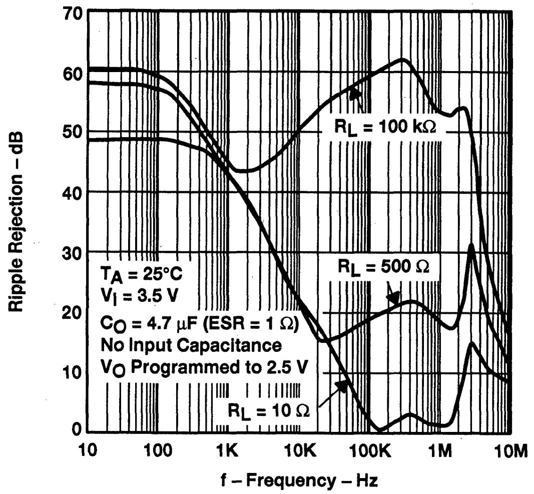


Figure 22

TPS7133Q
RIPPLE REJECTION
vs
FREQUENCY

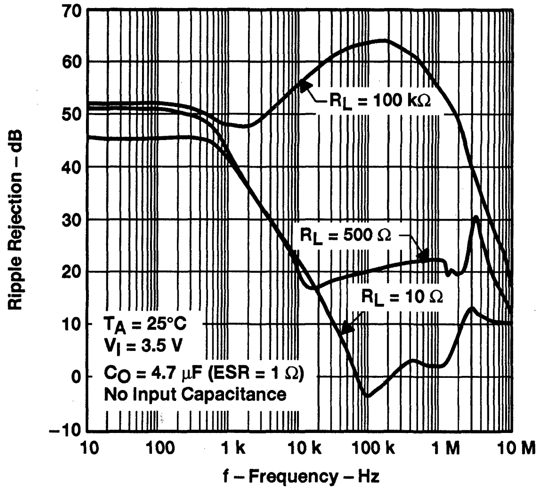


Figure 23

TPS7148Q
RIPPLE REJECTION
vs
FREQUENCY

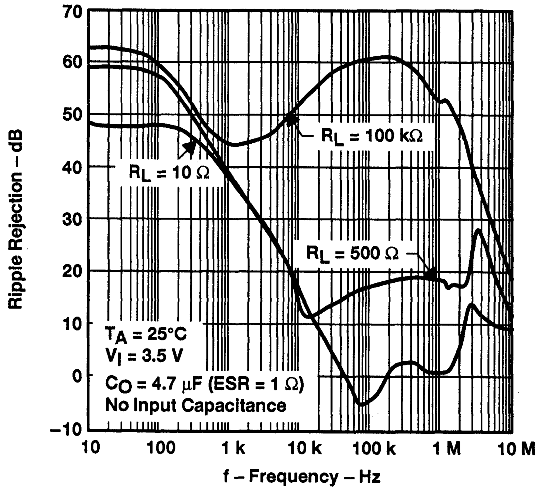


Figure 24

TPS7150Q
RIPPLE REJECTION
vs
FREQUENCY

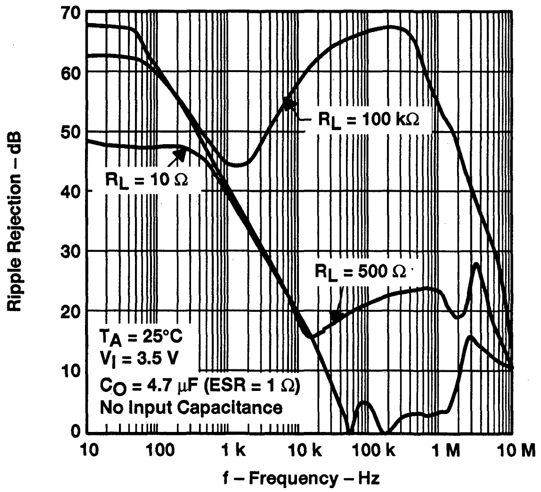


Figure 25

TYPICAL CHARACTERISTICS

**TPS7101Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

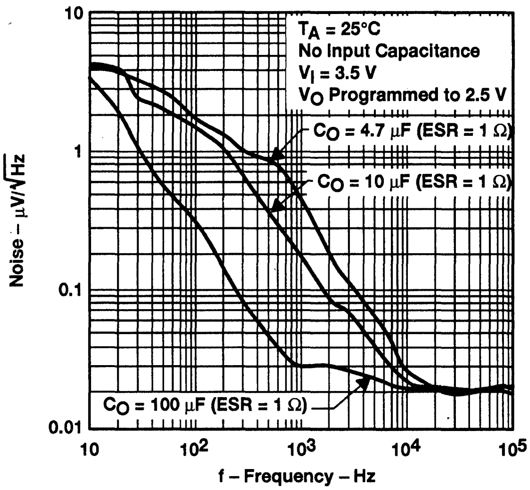


Figure 26

**TPS7133Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

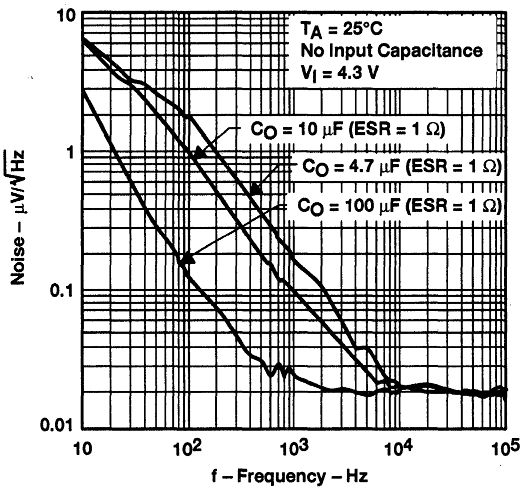


Figure 27

**TPS7148Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

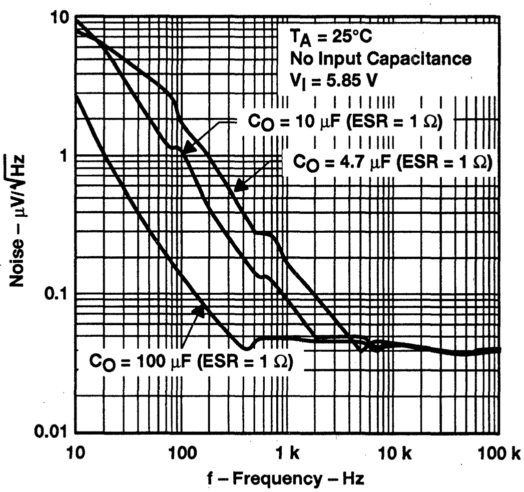


Figure 28

**TPS7150Q
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY**

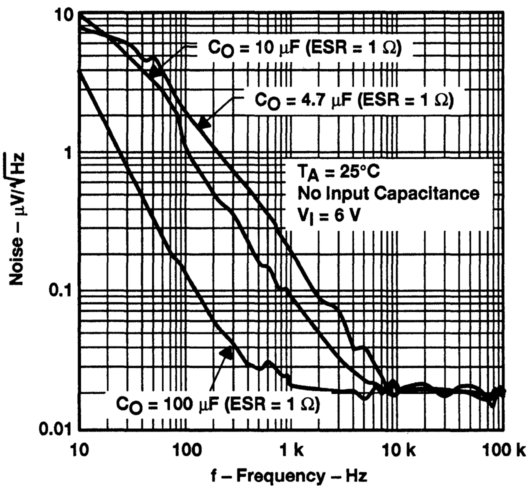


Figure 29

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

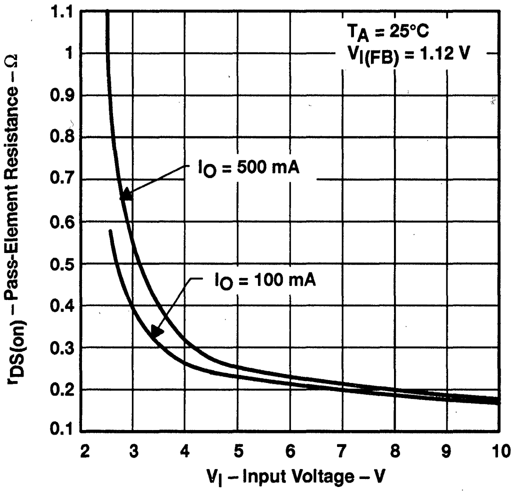


Figure 30

DIVIDER RESISTANCE vs FREE-AIR TEMPERATURE

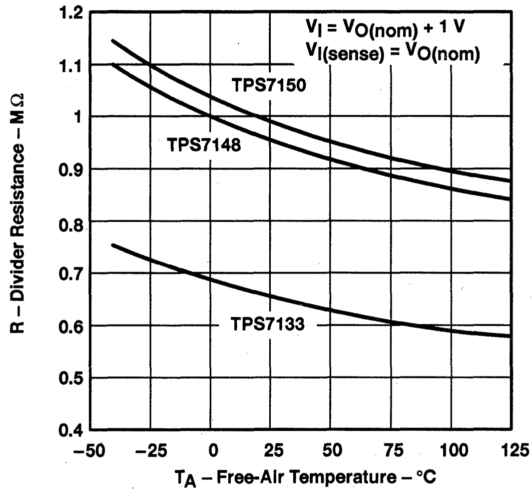


Figure 31

FIXED-OUTPUT VERSIONS SENSE PIN CURRENT vs FREE-AIR TEMPERATURE

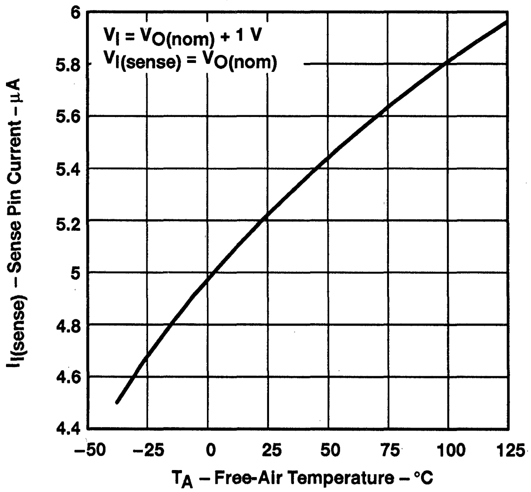


Figure 32

ADJUSTABLE VERSION FB LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

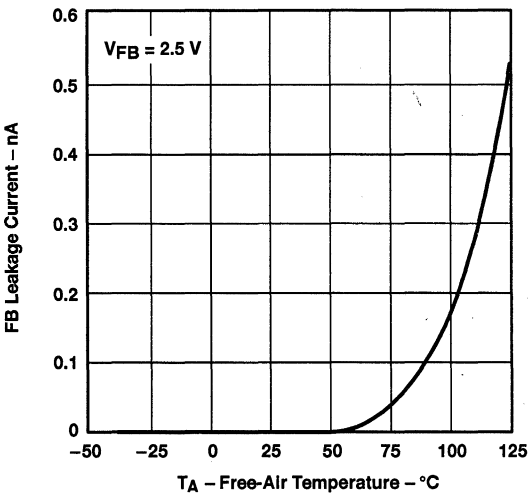


Figure 33

TYPICAL CHARACTERISTICS

MINIMUM INPUT VOLTAGE FOR ACTIVE PASS ELEMENT vs FREE-AIR TEMPERATURE

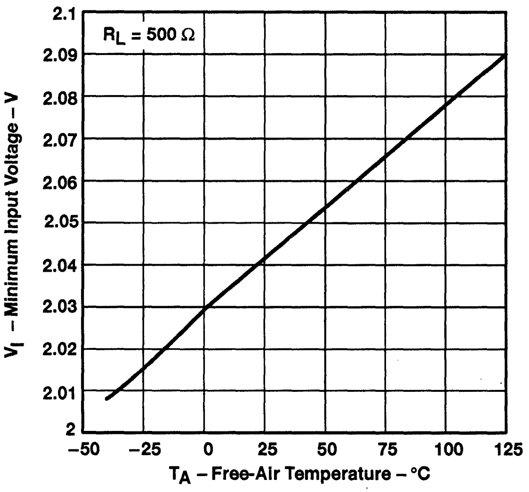


Figure 34

MINIMUM INPUT VOLTAGE FOR VALID POWER GOOD (PG) vs FREE-AIR TEMPERATURE

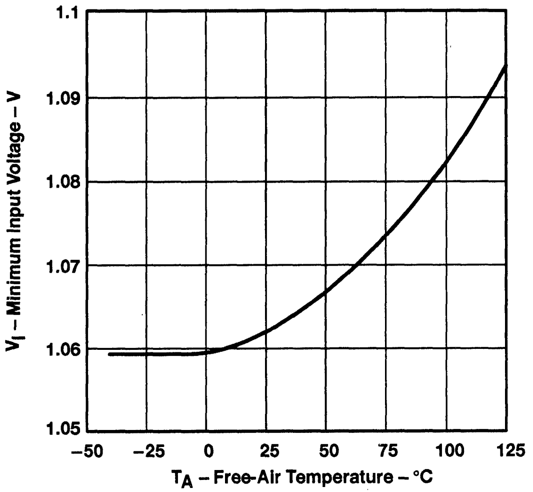


Figure 35

$\overline{EN}$ INPUT CURRENT vs FREE-AIR TEMPERATURE

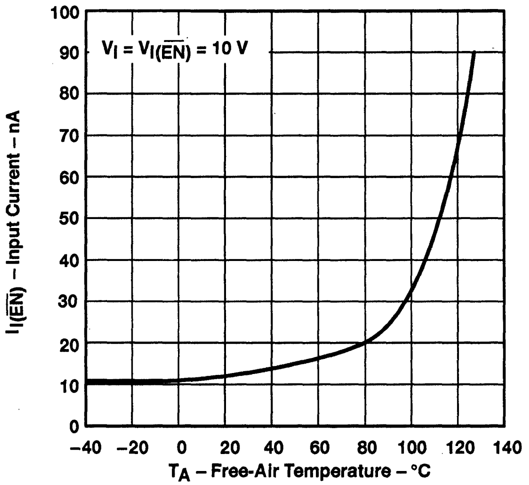


Figure 36

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE FROM ENABLE (EN)

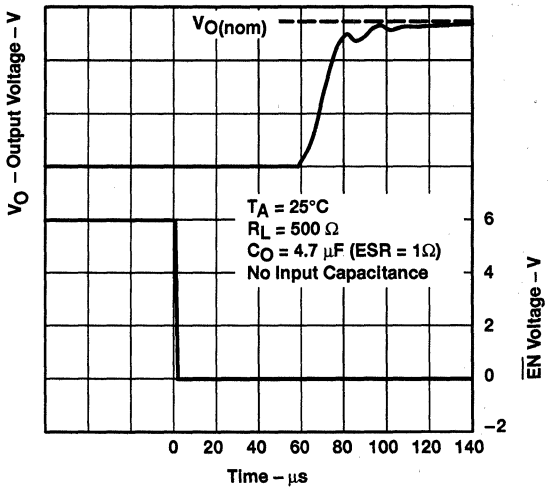


Figure 37

POWER-GOOD (PG) VOLTAGE vs OUTPUT VOLTAGE

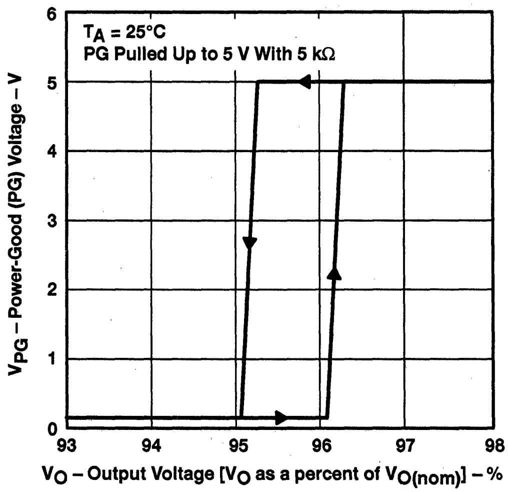


Figure 38

TYPICAL CHARACTERISTICS

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT**

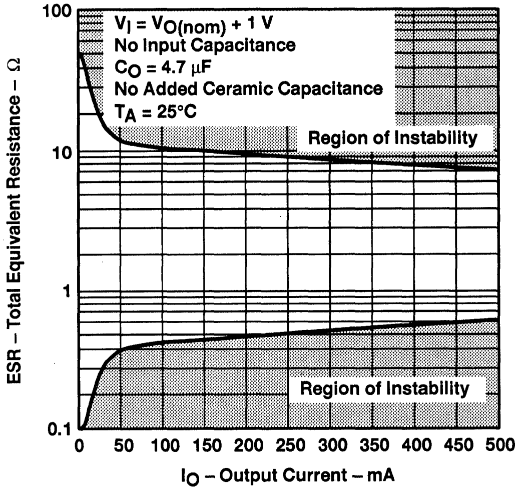


Figure 39

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
OUTPUT CURRENT**

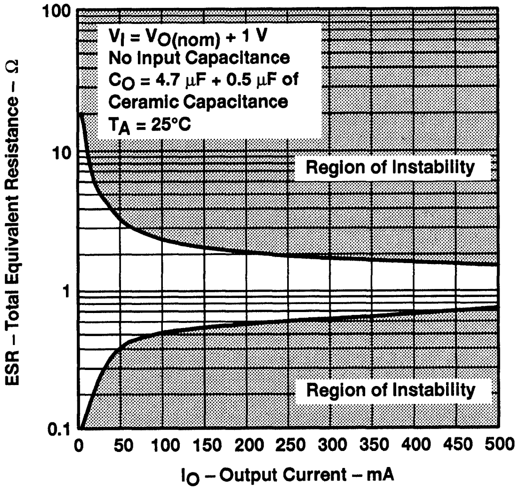


Figure 40

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE**

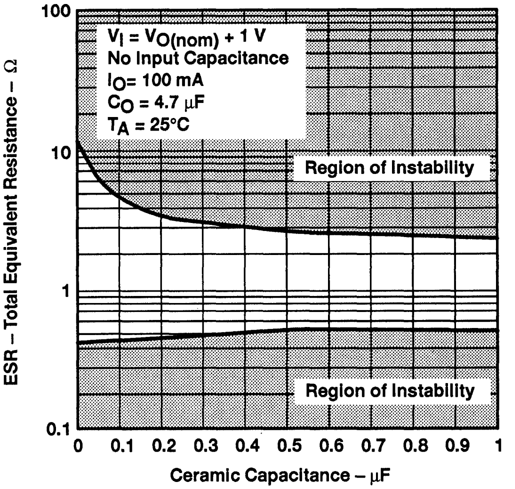


Figure 41

**TYPICAL REGIONS OF STABILITY
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE**

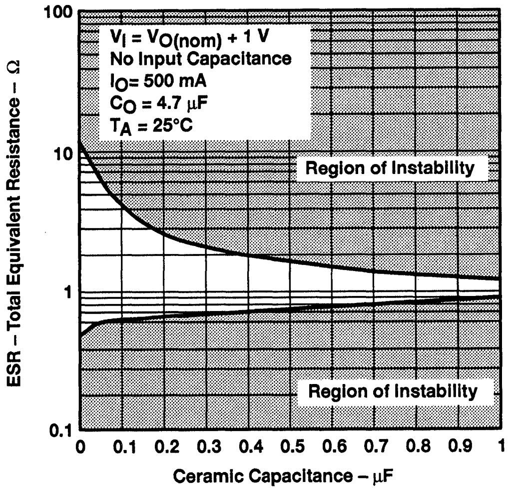


Figure 42

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

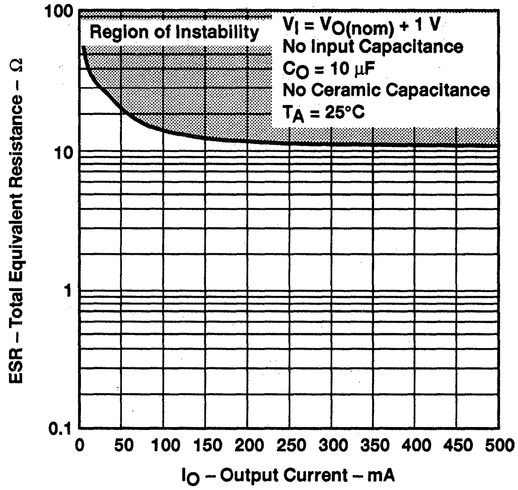


Figure 43

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
OUTPUT CURRENT

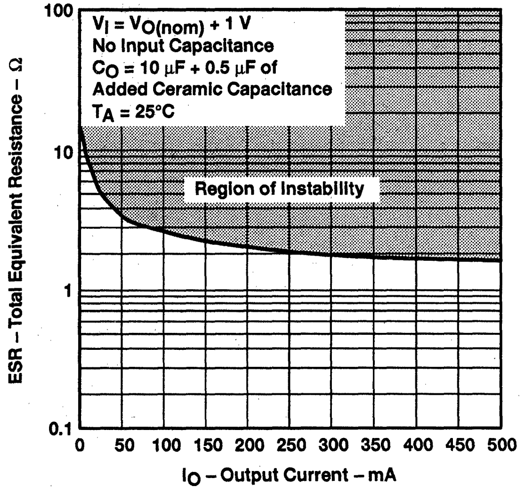


Figure 44

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

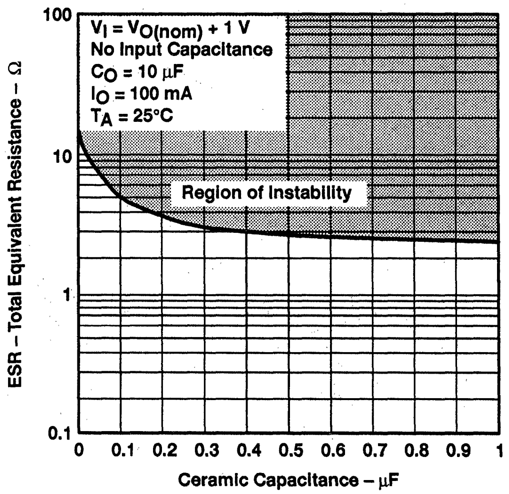


Figure 45

TYPICAL REGIONS OF STABILITY†
TOTAL ESR
vs
ADDED CERAMIC CAPACITANCE

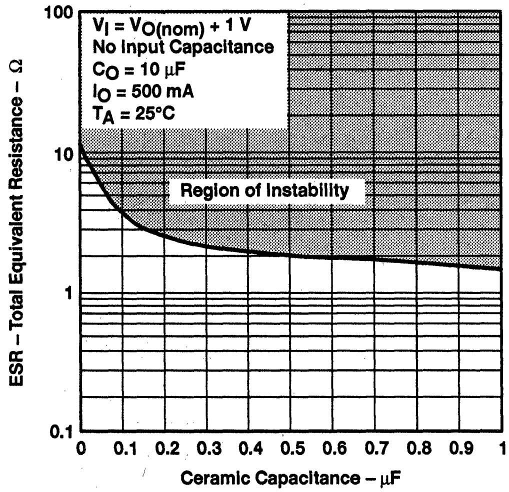
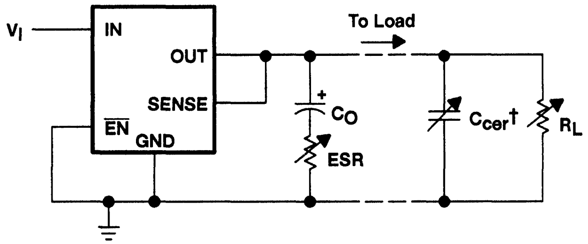


Figure 46

† ESR values below 0.1 Ω are not recommended.

TYPICAL CHARACTERISTICS

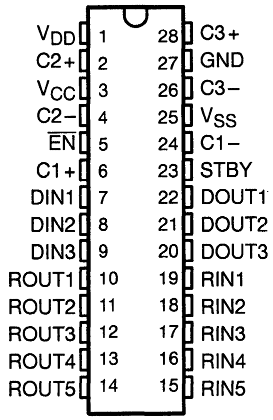


† Ceramic capacitor

Figure 47. Test Circuit for Typical Regions of Stability (Figures 39 through 46)

- **Single-Chip and Single-Supply Interface for IBM PC/AT Serial Port**
- **Three Drivers and Five Receivers Meet or Exceed the Requirements of EIA/TIA-232-E and ITU v.11 Standards**
- **Operates With 3.3-V or 5-V Supplies**
- **One Receiver Remains Active During Standby (Wake-Up Mode)**
- **Designed to Operate at 128 kbits Over a 3-m Cable**
- **Low Standby Current . . . 5 μA Max**
- **ESD Protection on RS-232 Pins Meets or Exceeds 4 kV (HBM) and 1.5 kV (HBM) on All Pins Per MIL-STD-883C, Method 3015**
- **External Capacitors . . . 0.1 μF**
  (V_{CC} = 3.3 V Five External Capacitors)
  (V_{CC} = 5 V Four External Capacitors)
- **Packaged in Shrink Small-Outline Package With 25-Mil Terminal Pitch and Maximum 2-mm Height (SSOP)**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Pin Compatible With the SN75LV4735**
- **Applications**
  EIA/TIA-232 Interface
  Battery-Powered Systems, PDAs
  Notebook, Laptop, and Palmtop PCs
  External Modems and Hand-Held Terminals

DB PACKAGE†
(TOP VIEW)



† The DB package is only available in left-ended tape and reel (order part number SN75LV4737ADBLE).

description

The SN75LV4737A‡ consists of three line drivers, five line receivers, and a charge-pump circuit. It provides the electrical interface between an asynchronous communication controller and the serial-port connector and meets the requirements of EIA/TIA-232-E. This combination of drivers and receivers matches those needed for the typical serial port used in an IBM PC/AT or compatibles. The charge pump and five small external capacitors allow operation from a single 3.3-V supply and four capacitors for operation from a 5-V supply.

The device has flexible control options for power management when the serial port is inactive. A common disable for all of the drivers and receivers is provided with the active-high STBY input. The active-low $\overline{EN}$ input is an enable for one receiver to implement a wake-up feature for the serial port. All the logic inputs can accept signals from controllers operating from a 5-V supply even though the SN75LV4737A is operating from 3.3 V.

The SN75LV4737A is characterized for operation over the temperature range of 0°C to 70°C.

‡ Patent-pending design

Function Tables

EACH DRIVER

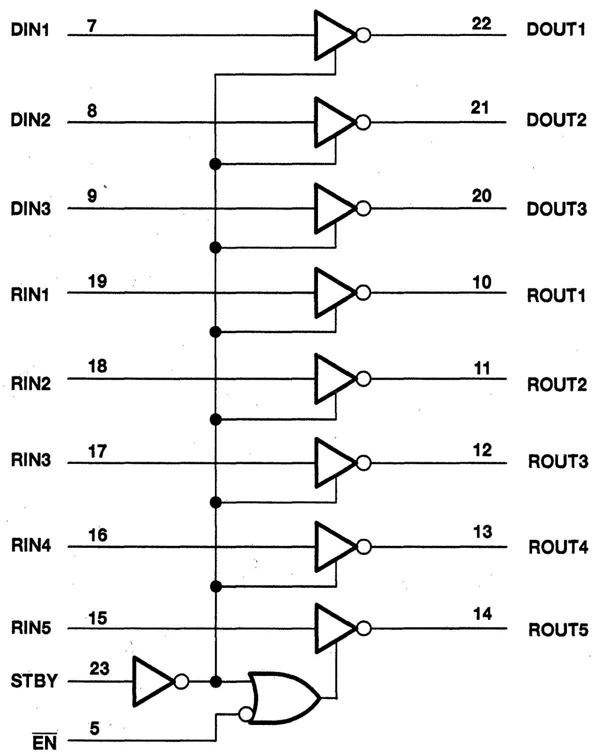
INPUTS		OUTPUTS
DIN	STBY	DOUT
X	H	Z
L	L	H
H	L	L
Open	L	L

EACH RECEIVER

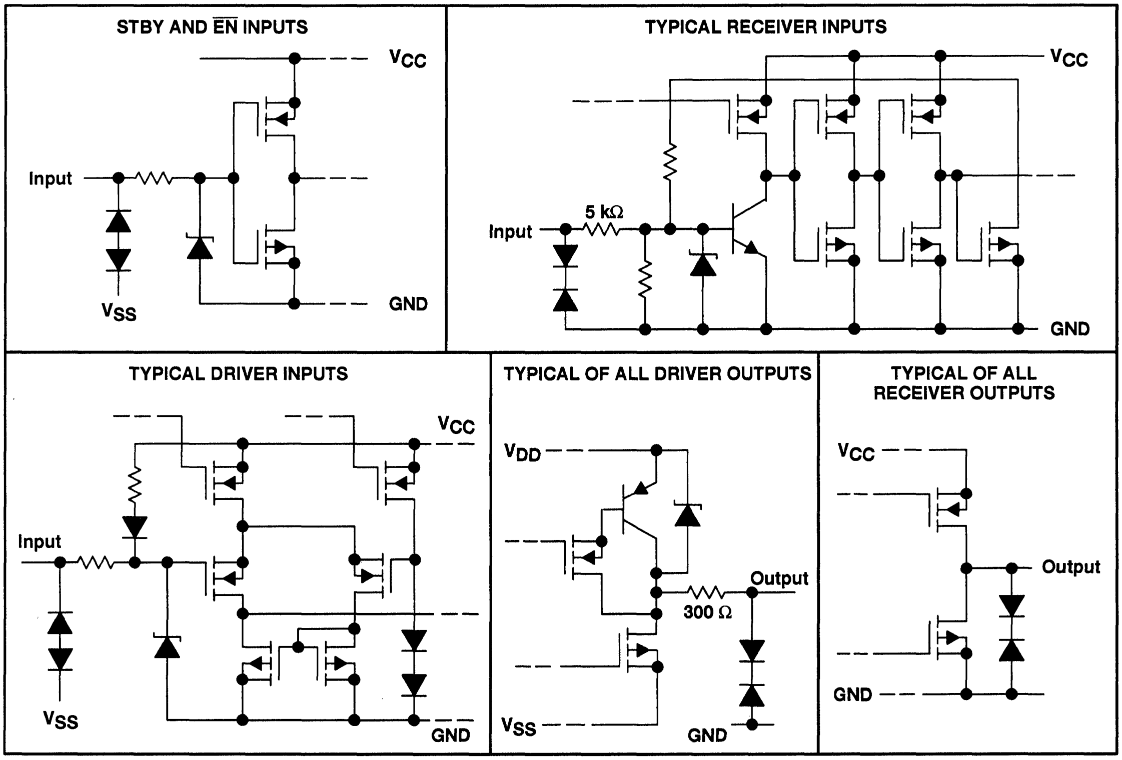
INPUTS				OUTPUTS	
STBY	$\overline{EN}$	RIN5	RIN1 – RIN4	ROUT5	ROUT1 – ROUT4
H	H	X	X	Z	Z
H	L	H	X	L	Z
H	L	L	X	H	Z
L	X	L	L	H	H
L	X	H	H	L	L

H = high level, Low = low level, X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Positive output supply voltage, V_{DD} (see Note 1)	15 V
Negative output supply voltage, V_{SS}	−15 V
Input voltage range, V_I: Driver	−3 V to 7 V
Receiver	−30 V to 30 V
Output voltage range, V_O: Driver	V_{SS} – 0.3 V to V_{DD} + 0.3 V
Receiver	−0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	668 mW	5.3 mW/°C	430 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage	V_{CC} = 3.3 V		3	3.3	3.6	V
	V_{CC} = 5 V		4.5	5	5.5	V
Driver high-level input voltage, V_{IH}	V_{CC} = 3.3 V	DIN, $\overline{EN}$, STBY	2			V
	V_{CC} = 5 V	DIN	2			
		$\overline{EN}$, STBY	2.5			
Driver low-level input voltage, V_{IL}	DIN, $\overline{EN}$, STBY				0.8	V
Receiver input voltage, V_I					±30	V
External capacitor	3.3-V operation (C1, C2, C3, C4, C5), 5-V operation (C1, C3, C4, C5), See Note 2 and Figures 6 and 7		0.1			µF
Operating free-air temperature, T_A			0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 6 and 7)

PARAMETER		TEST CONDITIONS		V_{CC} = 3.3 V MIN	TYP†	MAX	V_{CC} = 5 V MIN	TYP†	MAX	UNIT
V_{DD}	Positive supply voltage	No load		8	10		7	8.7		V
V_{SS}	Negative supply voltage	No load			−9.5	−7		−8	−6	V
I_I	Input current ($\overline{EN}$, STBY)	See Notes 3 and 4				±2			±2	µA
I_{CC}	Supply current	No load, Inputs open	STBY at GND, $\overline{EN}$ at V_{CC} or GND	8.4	10	18	10	12	20.7	mA
	Supply current (standby mode) (see Note 3)		$\overline{EN}$, STBY at V_{CC}			5			5	µA
	Supply current (wake-up mode) (see Note 4)		$\overline{EN}$ at GND, STBY at V_{CC}			10			10	µA

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.

NOTES: 2. C2 is only needed for 3.3-V operation.
3. When STBY mode is not used, STBY must be taken low.
4. When wake-up mode is not used, $\overline{EN}$ must be taken high.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ		5.5	7		V
V_{OL}	Low-level output voltage	R_L = 3 kΩ			−6	−5	V
I_{IH}	High-level input current	$V_I = V_{CC}$				1	μA
I_{IL}	Low-level input current	V_I at GND				−10	μA
I_{OS}	Short-circuit output current (see Note 5)	V_{CC} = 3.6 V,	V_O = 0 V		±15	±40	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_o	Output resistance	$V_{CC} = V_{DD} = V_{SS}$ = 0 V,	V_O = ±2 V	300	500		Ω

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 3 kΩ to 7 kΩ, See Figure 1	3.3 V	100	500	850	ns
			5 V	100	500	850	ns
t_{PHL}	Propagation delay time, high- to low-level output		3.3 V	100	500	850	ns
			5 V	100	500	850	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		1	5	ms
t_{PZL}	Output enable time to low level				3	7	ms
t_{PHZ}	Output disable time from high level	C_L = 50 pF, R_L = 3 kΩ to 7 kΩ, See Figure 2	3.3 V		0.9	3	μs
			5 V		0.6	3	
t_{PLZ}	Output disable time from low level		3.3 V		0.5	3	
			5 V		0.3	3	
SR	Slew rate	C_L = 50 pF, See Figure 1	R_L = 3 kΩ to 7 kΩ,	4		30	V/μs
SR(tr)	Slew rate, transition region	C_L = 2500 pF, See Figure 3	R_L = 3 kΩ to 7 kΩ,	3		30	V/μs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.

NOTE 5: Short-circuit durations should be controlled to prohibit exceeding the device absolute power dissipation ratings and not more than one output should be shorted at a time.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

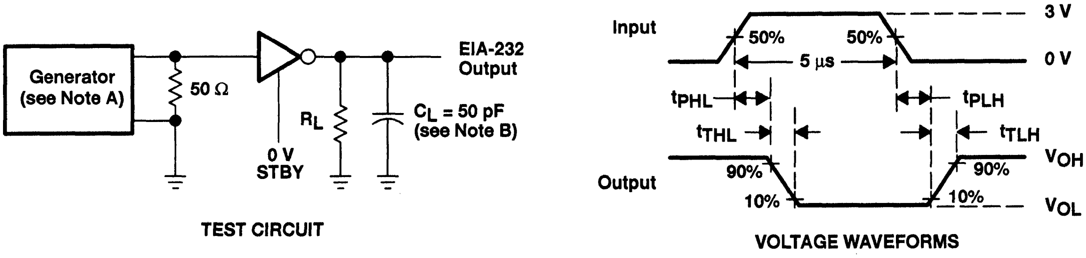
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	3.3 V	2.4	3		V
			5 V	3.5	5		V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA			0.2	0.4	V
V_{T+}	Positive-going input threshold voltage				2.2	2.6	V
V_{T-}	Negative-going input threshold voltage			0.6	1		V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5	1.2	1.8	V
r_i	Input resistance	$V_I = \pm 3$ V to ± 25 V		3	5	7	kΩ

† All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V and $T_A = 25°C$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF, $R_L = 3$ kΩ to GND

PARAMETER		TEST CONDITIONS	$V_{CC} = 3.3$ V			$V_{CC} = 5$ V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 4	10	70	200	10	70	200	ns
t_{PHL}	Propagation delay time, high- to low-level output		10	60	200	10	55	200	ns
t_{PLH}	Propagation delay time, low- to high-level output (wake-up mode)			40	200		40	200	µs
t_{PHL}	Propagation delay time, high- to low-level output (wake-up mode)			90	500		70	500	ns
t_{PZH}	Output enable time to high level	See Figure 5		3	10		1.2	10	µs
t_{PZL}	Output enable time to low level			100	250		60	250	ns
t_{PHZ}	Output disable time from high level		100	200	600	100	150	600	ns
t_{PLZ}	Output disable time from low level			130	250		60	250	ns

PARAMETER MEASUREMENT INFORMATION



$$SR = \frac{0.8\ V(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\ V(V_{OL} - V_{OH})}{t_{THL}}$$

Figure 1. Driver Propagation Delay Times and Slew Rate (5-µs input)

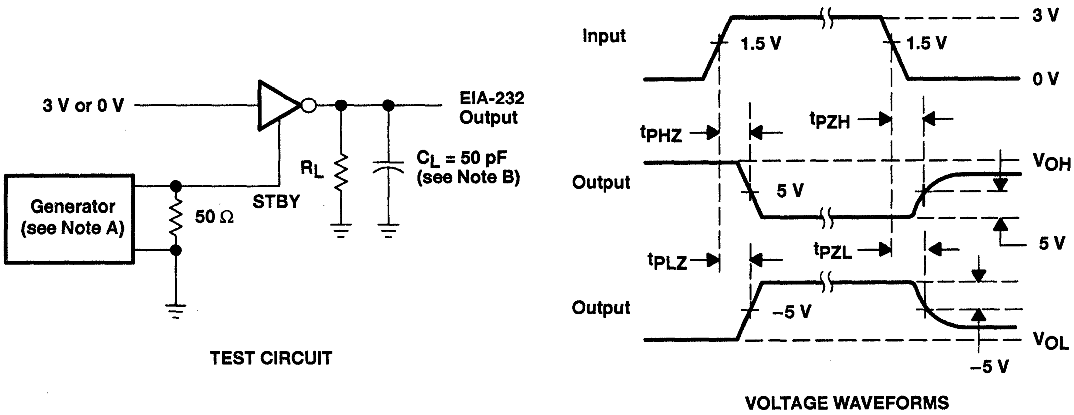
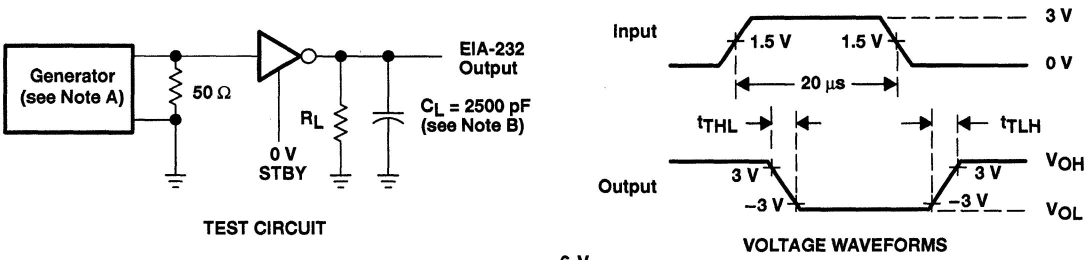


Figure 2. Driver Enable and Disable Test Times



$$SR = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

Figure 3. Driver Transition Times and Slew Rate (20-µs input)

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

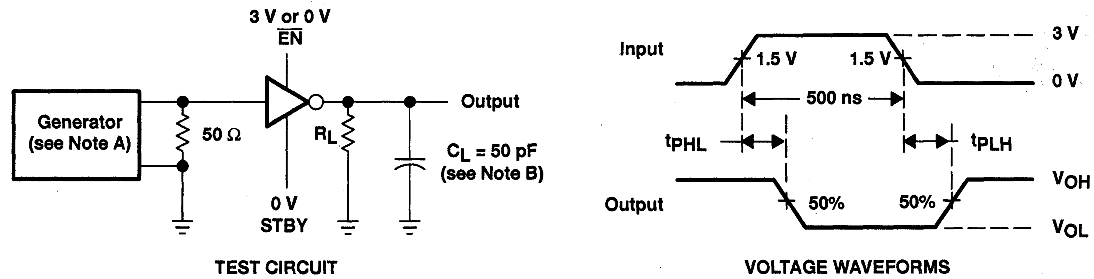


Figure 4. Receiver Propagation Delay Times

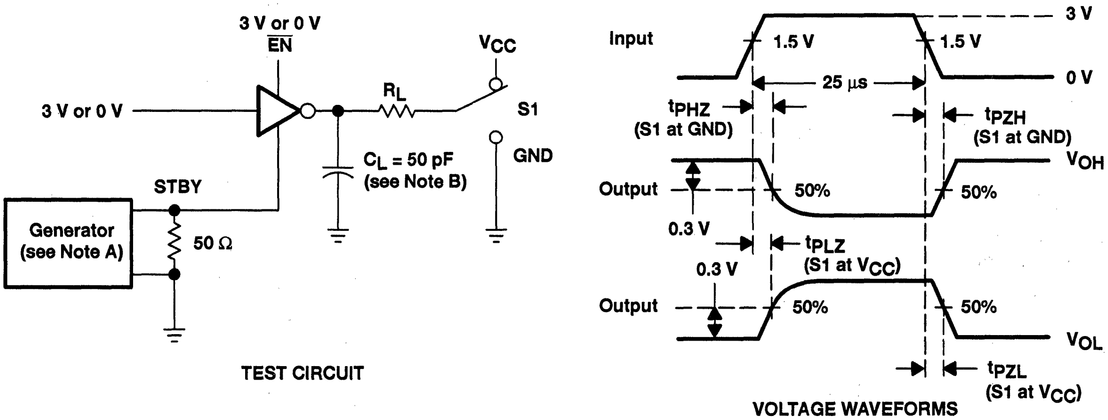
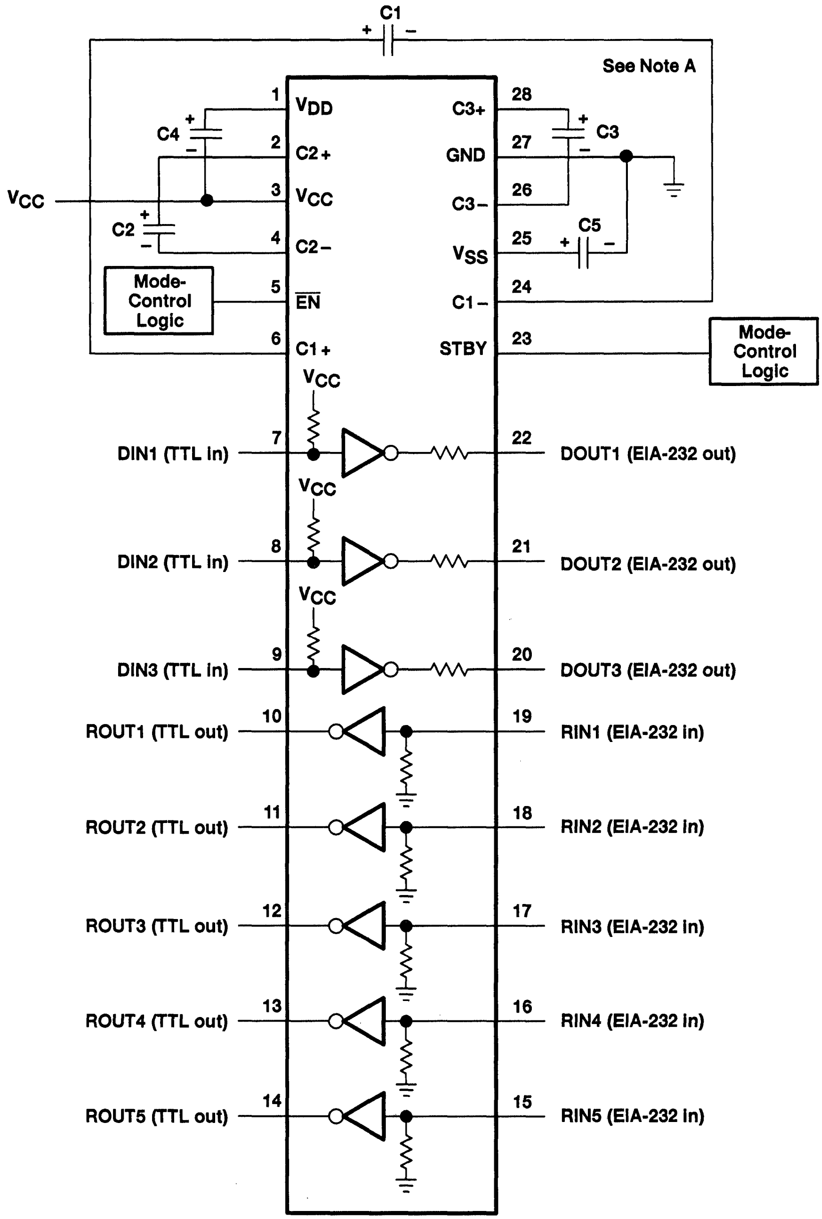


Figure 5. Receiver Enable and Disable Times

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
B. C_L includes probe and jig capacitance.

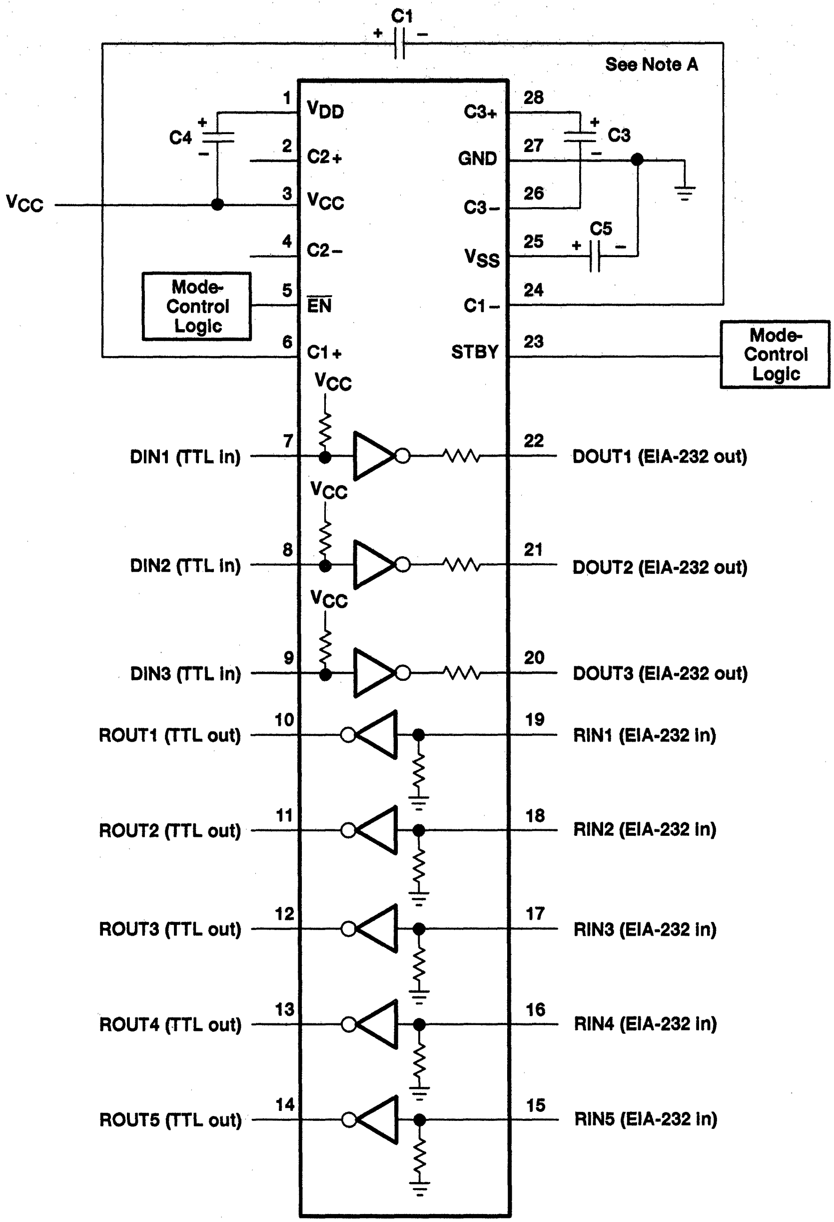
APPLICATION INFORMATION



NOTE A: C1 = C2 = C3 = C4 = C5 = 0.1 μF

Figure 6. Typical 3.3-V Operating Circuit

APPLICATION INFORMATION



NOTE A: C2 is not used.
C1 = C3 = C4 = C5 = 0.1 μF

Figure 7. Typical 5-V Operating Circuit

- **Integrated Asynchronous Communications Element Compatible With PCMCIA PC Card Standard Release 2.01**
- **Consists of a Single TL16C550 ACE Plus PCMCIA Interface Logic**
- **Provides Common I-Bus/Z-Bus Microcontroller Inputs for Most Intel and Zilog Subsystems**
- **Fully Programmable 256-Byte Card Information Structure and 8-Byte Card Configuration Register**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop and Parity) to or From Serial Data Stream**
- **Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts**
- **Selectable Serial-Bypass Mode Provides Subsystem With Direct Parallel Access to the FIFOs**
- **Fully Programmable Serial-Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud-Rate Generation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions**
- **Provides TL16C450 Mode at Reset Plus Selectable Normal TL16C550 Operation or Extended 64-Byte FIFO Mode**
- **Selectable Auto-$\overline{\text{RTS}}$ Mode Deactivates $\overline{\text{RTS}}$ at 14 Bytes in 550 Mode and at 56 Bytes in Extended 550 Mode**
- **Selectable Auto-$\overline{\text{CTS}}$ Mode Deactivates Serial Transfers When $\overline{\text{CTS}}$ is Inactive**

description

The TL16PC564A† is designed to provide all the functions necessary for a Personal Computer Memory Card International Association (PCMCIA) universal asynchronous receiver transmitter (UART) subsystem interface. This interface provides a serial-to-parallel conversion for data to and from a modem coder-decoder/digital signal processor (CODEC/DSP) function to a PCMCIA parallel data-port format. A computer central processing unit (CPU), through a PCMCIA host controller, can read the status of the asynchronous communications element (ACE) interface at any point in the operation. Reported status information includes the type of transfer operation in process, the status of the operation, and any error conditions encountered.

Attribute memory consists of a 256-byte card information structure (CIS) and eight 8-byte card configuration registers (CCR). The CIS, implemented with a dual-port random-access memory (DPRAM), is available to both the host CPU and subsystem (modem), as are the CCRs. This DPRAM is used in place of the electrically erasable programmable read-only memory (EEPROM) normally used for the CIS. At power up, attribute memory is initialized by the subsystem.

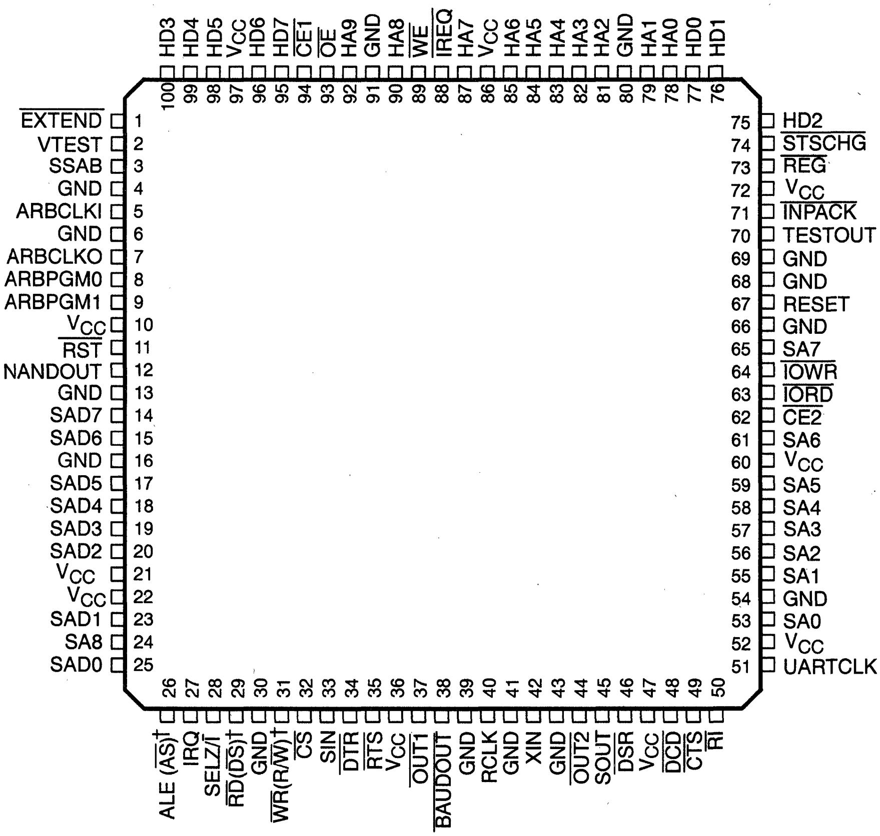
The TL16PC564A uses a TL16C550 ACE-type core with an expanded 64 × 11 receiver first-in-first-out (FIFO) memory and a 64 × 8 transmitter FIFO memory. The receiver trigger logic flags have been adjusted in order to take full advantage of the increased capacity when in the extended mode. In addition, eight of the UART registers have been mapped into the subsystem (modem) memory space as read-only registers. This allows the subsystem to read UART status information.

A subsystem-selectable serial-bypass mode has been implemented to allow the subsystem to bypass the serial portion of the UART and write directly to the receiver FIFO and read directly from the transmitter FIFO. Interrupt operation is not affected in this mode.

The TL16PC564A is packaged in a 100-pin thin quad flat package (PZ).

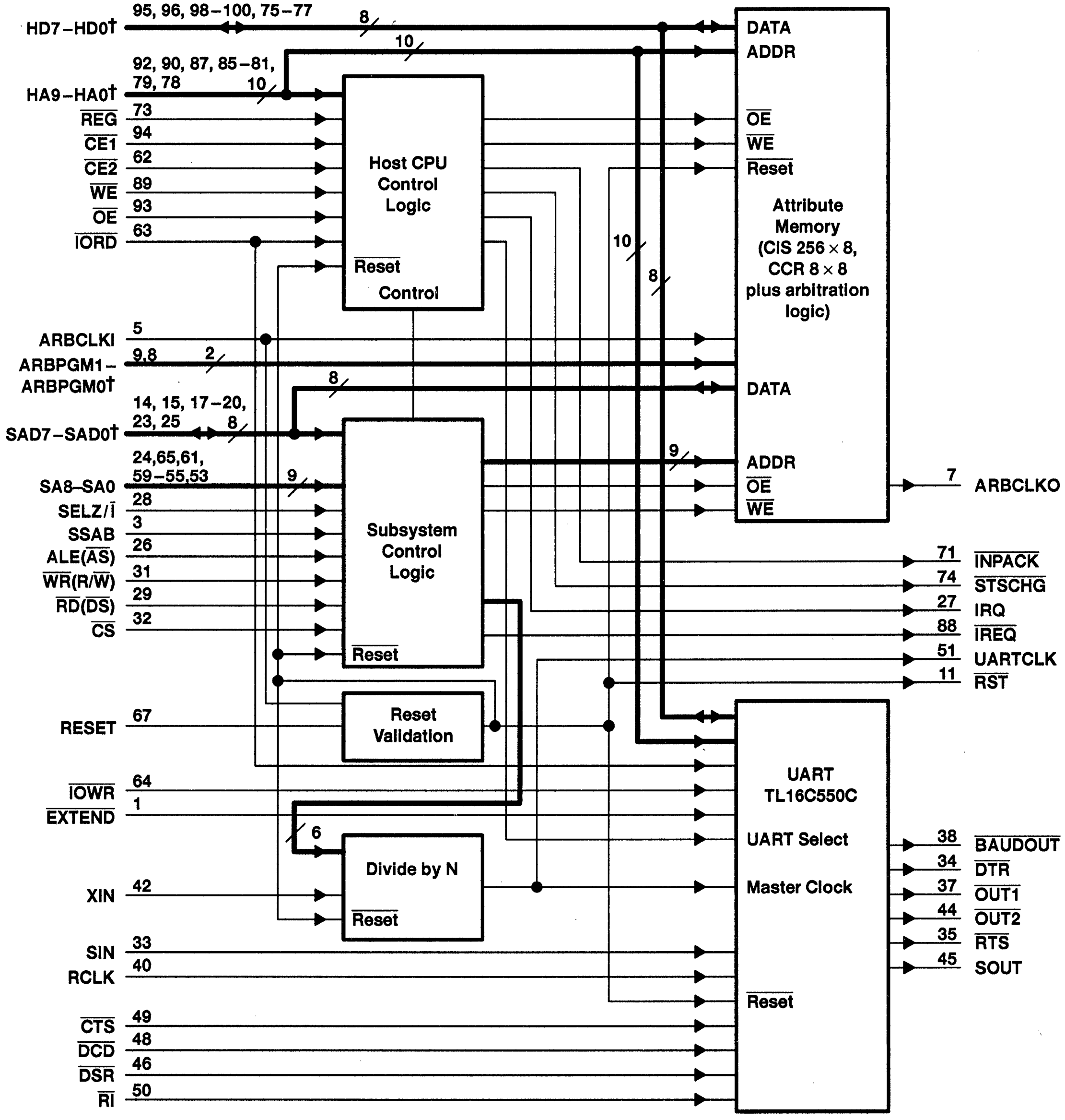
† Patent pending

PZ PACKAGE
(TOP VIEW)



† The terminal names not enclosed in parentheses correspond to an Intel microcontroller signal, and the terminal names enclosed in parentheses correspond to a Zilog microcontroller signal.

block diagram



† Bit 0 is the least significant bit.

Terminal Functions

TERMINAL		INTER-FACE†	I/O	DESCRIPTION
NAME	NO.			
ALE ($\overline{AS}$)	26	S	I	Address-latch enable/address strobe. ALE($\overline{AS}$) is an address-latch enable in the Intel mode and an address strobe in the Zilog mode. ALE ($\overline{AS}$) is active high for an Intel subsystem and active low for a Zilog subsystem.
ARBCLKO	7	M	O	Arbitration clock output. ARBCLKO is equal to the input on ARBCLKI divided by the binary-coded divisor input on ARBPGM (1 – 0).
ARBCLKI	5	M	I	Arbitration clock input. ARBCLKI is the base clock used in arbitration for the attribute memory DRAM and the reset validation circuitry.
ARBPGM0 ARBPGM1	8 9	M	I	Arbitration clock divisor program. These two bits are used to set the divisor for ARBCLKI. Divide by 1, 2, 4, and 8 are available.
$\overline{BAUDOUT}$	38	U	O	Baud output. $\overline{BAUDOUT}$ is an active-low 16× signal for the transmitter section of the UART. The clock rate is established by the reference clock (UARTCLK) frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
$\overline{CE1}$ $\overline{CE2}$	94 62	H	I	Card enable 1 and card enable 2 are active-low signals. $\overline{CE1}$ enables even-numbered address bytes, and $\overline{CE2}$ enables odd-numbered address bytes. A multiplexing scheme based on HA0, $\overline{CE1}$, and $\overline{CE2}$ allows an 8-bit host to access all data on HD0 through HD7 if desired. These signals have internal pullup resistors.
$\overline{CS}$	32	S	I	Chip-select. $\overline{CS}$ is the active-low chip select from the Zilog or Intel microcontroller.
$\overline{CTS}$	49	U	I	Clear to send. $\overline{CTS}$ is an active-low modem-status signal whose condition can be checked by reading bit 4 (CTS) of the modem-status register (MSR). Bit 0 (delta clear to send) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem-status interrupt is enabled when $\overline{CTS}$ changes states, an interrupt is generated.
DCD	48	U	I	Data-carrier detect. $\overline{DCD}$ is an active-low modem-status signal whose condition can be checked by reading bit 7 (DCD) of the MSR. Bit 3 (delta data-carrier detect) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem-status interrupt is enabled when $\overline{DCD}$ changes states, an interrupt is generated.
$\overline{DSR}$	46	U	I	Data-set ready. $\overline{DSR}$ is an active-low modem-status signal whose condition can be checked by reading bit 5 (DSR) of the MSR. Bit 1 (delta data-set ready) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem-status interrupt is enabled when $\overline{DSR}$ changes states, an interrupt is generated.
$\overline{DTR}$	34	U	O	Data terminal ready. $\overline{DSD}$ is an active-low signal. When active, $\overline{DTR}$ informs the modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit 0 of the modem-control register (MCR) to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a reset, doing a loop-mode operation, or resetting bit 0 (DTR) of the MCR.
$\overline{EXTEND}$	1	U	I	FIFO extend. When $\overline{EXTEND}$ is high, the UART is configured as a standard TL16C550 with 16-byte transmit and receive FIFOs. When $\overline{EXTEND}$ is low and FIFO control register (FCR) bit 5 is high, the FIFOs are extended to 64 bytes and the receiver-interrupt trigger levels adjust accordingly. $\overline{EXTEND}$ low in conjunction with FIFO-control register (FCR) bit 4 set high enables the auto-$\overline{RTS}$ function.
GND	4, 6, 13, 16, 30, 39, 41, 43, 54, 66, 68, 69, 80, 91	M		Common ground
HA0 HA1 HA2 HA3 HA4 HA5 HA6 HA7 HA8 HA9	78 79 81 82 83 84 85 87 90 92	H	I	The 10-bit address bus is used to address the attribute memory (bits 1 – 8) and to address the internal UART as either PCMCIA I/O (bits 0 – 2) or as a standard COM port (bits 0 – 9).

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

Terminal Functions (Continued)

TERMINAL NAME	NO.	INTERFACE†	I/O	DESCRIPTION
HD0 HD1 HD2 HD3 HD4 HD5 HD6 HD7	77 76 75 100 99 98 96 95	H	I/O	The 8-bit bidirectional data bus is used to transfer data to and from the attribute memory and the internal UART.
$\overline{INPACK}$	71	H	O	Input port acknowledge. $\overline{INPACK}$ is an active-low output signal that is asserted when the card responds to an I/O read cycle at the address on the HA bus.
$\overline{IORD}$	63	H	I	I/O read strobe. $\overline{IORD}$ is an active-low input signal activated to read data from the card's I/O space. The $\overline{REG}$ signal and at least one of the card enable inputs ($\overline{CE1}$, $\overline{CE2}$) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.
$\overline{IOWR}$	64	H	I	I/O write strobe. $\overline{IORW}$ is an active-low input signal activated to write data to the card's I/O space. The $\overline{REG}$ signal and at least one of the card enable inputs ($\overline{CE1}$, $\overline{CE2}$) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.
$\overline{IREQ}$	88	H	O	Interrupt request. $\overline{IREQ}$ is an active-low output signal asserted by the card to indicate to the host CPU that a card device requires host software service. This signal doubles as READY/BUSY during power-up initialization.
IRQ	27	S	O	Interrupt request. This active-high IRQ to the subsystem indicates a host CPU write to attribute memory has occurred.
NANDOUT	12	M	O	This is a production test output.
$\overline{OE}$	93	H	I	Output enable. $\overline{OE}$ is an active-low input signal used to gate memory read data from the card. This signal has an internal pullup resistor.
$\overline{OUT1}$ $\overline{OUT2}$	37 44	U	O	Output 1 and output 2 are active-low signals. $\overline{OUT1}$ and $\overline{OUT2}$ are user-defined output terminals that are set to their active state by setting respective MCR bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) state as a result of a reset, doing loop-mode operation, or by resetting bit 2 (OUT1) or bit 3 (OUT2) of the MCR. This signal has an open-drain outputs.
RCLK	40	U	I	Receiver clock. RCLK is the 16×-baud-rate clock input for the receiver section of the UART.
$\overline{RD}$($\overline{DS}$)	29	S	I	Read enable or data strobe input. $\overline{RD}$($\overline{DS}$) is the active-low read enable in the Intel mode and the active-low data strobe in the Zilog mode.
$\overline{REG}$	73	H	I	Attribute memory select. This active-low input signal is generated by the host CPU and accesses attribute memory ($\overline{OE}$ and $\overline{WE}$ active) and I/O space ($\overline{IORD}$ or $\overline{IOWR}$ active). PCMCIA common memory access is excluded. This signal has an internal pullup resistor and hysteresis on the input buffer.
RESET	67	H	I	Reset. RESET is an active-high input that serves as the master reset for the device. RESET clears the UART, placing the card in an unconfigured state. This signal has an internal pullup resistor.
$\overline{RI}$	50	U	I	Ring indicator. $\overline{RI}$ is an active-low modem-status signal whose condition can be checked by reading bit 6 (RI) of the MSR. The trailing-edge ring indicator (TERI) bit 2 of the MSR indicates that $\overline{RI}$ has transitioned from a low to a high state since the last read from the MSR. If the modem-status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RST}$	11	M	O	This is the qualified active-low reset signal. $\overline{RST}$ has a fail-safe open-drain output.
$\overline{RTS}$	35	U	O	Request to send is an active-low signal. When active, $\overline{RTS}$ informs the modem of the data set that the UART is ready to receive data. $\overline{RTS}$ is set to its active state by setting the RTS modem-control register bit and is set to its inactive (high) state either as a result of a reset, doing loop-mode operation, or by resetting bit 1 (RTS) of the MCR.

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	INTERFACE†	I/O	DESCRIPTION
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7	53 55 56 57 58 59 61 65	S	I	When SSAB is high, this is the subsystem address bus and SAD (7–0) is the subsystem data bus. When SSAB is low, this bus is not used and SAD(7–0) is the subsystem multiplexed address/data bus.
SA8	24	S	I	Address bit 8 is bit 8 of the subsystem address bus.
SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7	25 23 20 19 18 17 15 14	S	I/O	Subsystem address/data 7–0. This is a multiplexed bidirectional address/data bus to the attribute-memory DPRAM and CCRs when SSAB is low. This becomes a bidirectional data bus when SSAB is high.
SELZ/$\overline{\text{I}}$	28	S	I	Select Zilog or Intel mode. SELZ/$\overline{\text{I}}$ is used to select between a Zilog-like or Intel-like microcontroller. 1 = Zilog, 0 = Intel.
SIN	33	U	I	Serial data input. SIN moves information from the communication line or modem to the TL16PC564A UART receiver circuits. Data on the serial bus is disabled when operating in the loop mode.
SOUT	45	U	O	Serial out. SOUT is the composite serial data output to a connected communication device. SOUT is set to the marking (logic 1) state as a result of a reset.
SSAB	3	S	I	Separate subsystem address bus. SSAB is used to select between a multiplexed address/data bus subsystem interface (SSAB = 0) and a subsystem interface with separate address and data buses (SSAB = 1). This signal has an internal pulldown resistor.
$\overline{\text{STSCHG}}$	74	H	O	Status change. $\overline{\text{STSCHG}}$ is an optional active-low output signal used to alert the host that a subsystem write to attribute memory has occurred. This signal has an open-drain output.
TESTOUT	70	M	O	This is a production test output.
UARTCLK	51	M	O	UART clock. UARTCLK is a clock output whose frequency is determined by the frequency on XIN and the divisor value on the PGMCLK register.
V_{CC}	10,21,22,36, 47,52,60, 72,86,97	M		3.3-V or 5-V supply voltage
VTEST	2	M	I	VTEST is an active-high production test input with an internal pulldown resistor. It can be left open or tied to ground.
$\overline{\text{WE}}$	89	H	I	Write enable. $\overline{\text{WE}}$ is an active-low input signal used for strobing attribute-memory write data into the card. This signal has an internal pullup resistor
$\overline{\text{WR}}$(R/$\overline{\text{W}}$)	31	S	I	Write or read/write enable. $\overline{\text{WR}}$(R/$\overline{\text{W}}$) is the active-low write enable in the Intel mode and read/$\overline{\text{write}}$ in the Zilog mode.
XIN	42	M	I	Crystal input. XIN is a clock input divided internally based on the PGMCLK register value, then used as the primary UART clock input.

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

detailed description

reset-validation circuit

A reset-validation circuit has been implemented to qualify the active-high RESET input. At power up, the level on the $\overline{RST}$ output is unknown. Whenever RESET is stable for at least 8 ARBCLKIs, $\overline{RST}$ reflects the inverted state of that stable value of RESET. Any changes on RESET must be valid for eight ARBCLKI clocks before the change is reflected on $\overline{RST}$. This eight-clock filter provides needed hysteresis on the master reset input. $\overline{RST}$ is driven by a low-noise, open-drain, fail-safe output buffer.

host CPU memory map

The host CPU attribute memory space is mapped as follows:

Host CPU Address Bits 9–1 (HA0 = 0)	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The host CPU I/O space is mapped as follows:

	Address Mode (hex)				
Normal Mode	**COM1**	**COM2**	**COM3**	**COM4**	**I/O Space**
0 (DLAB = 0)†	3F8	2F8	3E8	2E8	UART receiver buffer register (RBR) – read only
0 (DLAB = 0)†	3F8	2F8	3E8	2E8	UART transmitter holding register (THR) – write only
0 (DLAB = 1)†	3F8	2F8	3E8	2E8	UART divisor latch LSB (DLL)
1 (DLAB = 0)†	3F9	2F9	3E9	2E9	UART interrupt-enable register (IER)
1 (DLAB = 1)†	3F9	2F9	3E9	2E9	UART divisor latch MSB (DLM)
2	3FA	2FA	3EA	2EA	UART interrupt-identification register (IIR) – read only
2	3FA	2FA	3EA	2EA	UART FIFO control register (FCR) – write only
3	3FB	2FB	3EB	2EB	UART line-control register (LCR)
4	3FC	2FC	3EC	2EC	UART modem-control register (MCR) – bit 5 read only
5	3FD	2FD	3ED	2ED	UART line-status register (LSR)
6	3FE	2FE	3EE	2EE	UART modem-status rgister (MSR)
7	3FF	2FF	3EF	2EF	UART scratch register (SCR)

† DLAB is bit 7 of the line-control register (LCR).

subsystem memory map

The subsystem attribute memory space is mapped as follows:

Subsystem Address Bits 8–0	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

subsystem memory map (continued)

The subsystem control space is mapped as follows:

Subsystem Address Bits 8–0	Control Space
272	Control Register
288	PGMCLK Register (write only)

The subsystem UART space is mapped as follows:

Subsystem Address Bits 8–0	UART Space
304	UART MCR bit 5 (write only)
304	UART DLL (read only)
305	UART IER (read only)
306	UART FCR (read only)
307	UART LCR (read only)
308	UART MCR (read only)
309	UART LSR (read only)
310	UART MSR (read only)
311	UART DLM (read only)
320	UART transmitter FIFO (read only)†
320	UART receiver FIFO (write only)†

† Only when serial bypass mode is enabled

host CPU/attribute-memory interface

The host CPU/attribute-memory interface is comprised of one port of the internal DPRAM, the eight CCRs, and necessary control circuitry. Signals HA0 and $\overline{\text{CE1}}$ are gated together internally so that the output of the gate is low when both signals have been asserted by the host CPU. This output is combined with $\overline{\text{REG}}$ and the decoded address, HA(9–1), to provide the chip enable for the DPRAM and CCRs. This composite chip enable in combination with $\overline{\text{WE}}$ or $\overline{\text{OE}}$ allows writes and reads to the DPRAM and CCRs.

subsystem/attribute-memory interface

The subsystem/attribute-memory interface is comprised of the second port of the internal DPRAM, the eight CCRs, and necessary control circuitry. When in multiplexed mode (SSAB = 0), the combination of signals SELZ/$\overline{\text{I}}$ and ALE($\overline{\text{AS}}$) allows either a positive-pulse Intel or a negative-pulse Zilog address latch-enable strobe to latch the address on SA8 and SAD(7–0). When in the Zilog mode (SELZ/$\overline{\text{I}}$ high), the combination of read/write [$\overline{\text{WR}}$(R/$\overline{\text{W}}$)], data strobe [$\overline{\text{RD}}$($\overline{\text{DS}}$)], and decoded address allows ZBUS access. When in the Intel configuration (SELZ/$\overline{\text{I}}$ low), the combination of read [$\overline{\text{RD}}$($\overline{\text{DS}}$)], write [$\overline{\text{WR}}$(R/$\overline{\text{W}}$)], and decoded address allows IBUS access.

When in nonmultiplexed mode (SSAB = 1), SA(7–0) become the lower-order address bits, SAD(7–0) are strictly the bidirectional data bus, and ALE($\overline{\text{AS}}$) is nonfunctional. All other interface signals function the same.

SSAB	SELZ/$\overline{\text{I}}$	$\overline{\text{RD}}$($\overline{\text{DS}}$)	$\overline{\text{WR}}$(R/$\overline{\text{W}}$)	Address	Operation
0	0	0	1	SA8, SAD(7–0)	Intel read
0	0	1	0	SA8, SAD(7–0)	Intel write
0	1	0	1	SA8, SAD(7–0)	Zilog read
0	1	0	0	SA8, SAD(7–0)	Zilog write
1	0	0	1	SA(8–0)	Intel read
1	0	1	0	SA(8–0)	Intel write
1	1	0	1	SA(8–0)	Zilog read
1	1	0	0	SA(8–0)	Zilog write

attribute-memory arbitration

Arbitration for the attribute memory is necessary whenever there is simultaneous access to the same DPRAM or CCR address for the conditions of:

- Host CPU read and subsystem write
- Host CPU write and subsystem read
- Host CPU write and subsystem write

If arbitration were not provided, attribute-memory data would be corrupted and invalid data read due to uncontrolled access to the same DPRAM or CCR address.

The arbitration control circuitry synchronizes the asynchronous accesses of the host CPU and subsystem to the DPRAM and CCR and controls the access based on the pending host CPU and subsystem attribute-memory operation. The synchronizing and control circuitry needs a clock called the arbitration clock. The external clock (ARBCLKI) goes through a programmable divider and can be divided by one, two, four, or eight to generate a clock frequency within an allowed range for the arbitration logic to work correctly. The output of this frequency divider is named ARBCLKO. The programmable divider bits are defined as follows:

ARBPGM1	ARBPGM0	INTERNAL ARITRATION CLOCK
L	L	ARBCLKI/1
L	H	ARBCLKI/2
H	L	ARBCLKI/4
H	H	ARBCLKI/8

The upper period limit of ARBCLKO is N/6, where N (ns) is the shortest of the two attribute-memory accesses, host CPU or subsystem. The lower period limit of ARBCLKO is based on the DPRAM specifications at the supply voltage used:

5 V = 14-ns clock cycle (71 MHz)
3.3 V = 26-ns clock cycle (38.5 MHz)

For any arbitration condition, attribute-memory access is controlled to ensure valid data is read for a port that is doing a read operation and valid data is written for a port that is doing a write operation. When both the host CPU and subsystem are performing simultaneous write operations to the same address, the host CPU is allowed to write and the subsystem write is ignored.

host CPU/subsystem handshake

Two signals are provided for handshaking between the host CPU and the subsystem. The active-high IRQ signifies to the subsystem that the host CPU has written data into attribute memory. The subsystem can clear IRQ by writing a one to bit 6 of the subsystem control register. The active-low $\overline{\text{STSCHG}}$ signifies to the host CPU that the subsystem has written data to attribute memory provided bit 2 of the subsystem control register ($\overline{\text{STSCHG}}$ enable) is high. The host CPU can clear $\overline{\text{STSCHG}}$ by reading any location in attribute memory. The control of these signals is synchronized to ARBCLKO to ensure there are no false assertions/deassertions.

There is additional arbitration performed for instances of simultaneous assertion/deasseration of IRQ or $\overline{\text{STSCHG}}$. If a subsystem write and host CPU read occur simultaneously, $\overline{\text{STSCHG}}$ may be briefly deasserted prior to being asserted, but the write ultimately wins arbitration. If the host CPU read occurs more than one-half an arbitration clock after the subsystem write, $\overline{\text{STSCHG}}$ is deasserted. IRQ is arbitrated in a similar fashion.

host CPU/UART interface

The UART select is derived from either host CPU address information or logic levels on $\overline{CE1}$, $\overline{CE2}$ and $\overline{REG}$. In the address mode, host CPU address bits HA9, HA7, HA6, HA5, and HA3 are combined with conditional derivatives of HA4 and HA8 to select the UART (HA4 and HA8 are used to select COM ports 1–4 based on settings in the subsystem control register). $\overline{CE1}$ and $\overline{CE2}$ are combined such that either of these two signals in combination with $\overline{REG}$ enable the UART in the event that these signals are present. In the event that $\overline{CE1}$ or $\overline{CE2}$ are not present, the UART must be accessed in the address mode previously described. The UART select in conjunction with $\overline{IORD}$ and $\overline{IOWR}$ allows host CPU accesses to the UART. Host CPU address bits HA2–HA0 are decoded to select which UART register is to be accessed.

All UART registers remain intact with the exception of the FIFO control register (FCR) and the modem-control register (MCR). The FCR (host CPU write-only address 2) bits 4 and 5 in conjunction with $\overline{EXTEND}$ control $\overline{RTS}$ operation and FIFO depth as follows:

BIT 5	BIT 4	$\overline{EXTEND}$	RTS OPERATION	FIFO DEPTH
X	X	H	Normal	16 bytes
0	0	L	Normal	16 bytes
0	1	L	Auto	16 bytes
1	0	L	Normal	64 bytes
1	1	L	Auto	64 bytes

FCR bit 5 high and $\overline{EXTEND}$ low redefine the receiver FIFO trigger levels set by FCR bits 6 and 7 as follows:

BIT 7	BIT 6	TRIGGER LEVEL
0	0	1
0	1	16
1	0	32
1	1	56

The MCR (host CPU address 4) bit 5 is read only. This bit is controlled by the subsystem to enable (high) the auto-$\overline{CTS}$ mode of operation

subsystem/UART interface

The UART provides a serial-communications channel to the subsystem with enhanced $\overline{RTS}$ control (see auto-$\overline{RTS}$ description). This channel is capable of operating at 115 kbps and is the main communications channel to the subsystem (refer to the TL16C550 specification for the detailed description of the serial-communications channel).

Many of the UART registers have been mapped into the subsystems memory space as read only. In addition, MCR bit 5 (subsystem address 130 hex) is controlled by the subsystem to enable (High) auto-$\overline{CTS}$. The subsystem can read the MCR at address 134 hex. When reading the FCR (subsystem address 132 hex), bits 1 and 2 are always high, and bits 4 and 5 are low only when $\overline{EXTEND}$ is low and the host CPU has set them high (64-byte FIFOs and auto-$\overline{RTS}$ enabled) (refer to the subsystem memory map).

subsystem control register

The subsystem control register is an 8-bit register located at subsystem address 110 (hex). This register is programmed based on host CPU configuration information and has a default selection of COM2 after a valid reset. The bit definitions are as follows (0 = lsb):

Bits 0 and 1 define which host COM port the UART is connected to when the chip is in the address mode. COM2 is the default (power-up) condition.

BIT 1	BIT 0	COM PORT
0	0	COM1
1	0	COM2
0	1	COM3
1	1	COM4

Bit 2 is a host CPU interrupt-enable bit. When this bit is set, any subsystem attribute-memory write cycle causes $\overline{STSCHG}$ to be asserted. This bit is cleared after a valid reset.

Bit 3 enables or disables address-mode selection as described in the host CPU/UART interface description. This bit is cleared (disabling the address mode) after a valid reset.

Bits 4 and 5 together ensure adherence to PCMCIA power-up requirements. At power up, the card must operate as a memory card and all host CPU I/O operations must be disabled. $\overline{IREQ}$, which doubles as the host CPU READY/$\overline{BUSY}$ line, powers up low, indicating that the memory card is busy. Once the subsystem initializes attribute memory, the subsystem sets bit 4 to indicate that the memory card is ready. Then bit 5 is reset, changing the configuration from a memory card to an I/O card, enabling host CPU UART accesses. $\overline{IREQ}$ now becomes the host CPU interrupt-request line.

BIT 5	BIT 4	CONFIGURATION
1	0	Memory card, I/O operation (UART) disabled; $\overline{IREQ}$ is low, indicating card is busy (power-up and reset condition)
1	1	Memory card, I/O operation (UART) disabled; $\overline{IREQ}$ is high, indicating card is ready
0	X	I/O card, I/O operation (UART) enabled; $\overline{IREQ}$ now functions as the host CPU interrupt-request line

Bit 6 is a self-clearing bit that resets the subsystem IRQ signal. Writing a one to this location clears the IRQ interrupt.

Bit 7 enables or disables serial-bypass mode as described in the subsystem serial-bypass-mode description. This bit is cleared (disabling serial-bypass mode) after a valid reset.

subsystem PGMCLK register/divide-by-n circuit

The subsystem PGMCLK register is a 6-bit write-only register located at address 120 hex and is used to select the divisor of the divide-by-n-and-a-half circuitry. Any write to this register generates a reset to the UART and the divide-by-n circuitry.

The divide-by-n circuitry allows for a divisor from 0 to 31.5 in 0.5 increments (PGMCLK0 is the half bit). The divided clock output is used to drive the UART clock input and can be seen on UARTCLK. The UART requires a clock with a minimum high pulse duration of 50 ns and a minimum low pulse duration of 50 ns (10-MHz maximum operating frequency). A programmed divisor between 2 and 7.5 drives the UART clock low for one XIN clock cycle for integer divisors and one-and-a-half XIN clock cycles for integer-plus-a-half divisors. A programmed divisor of eight or greater drives the UART clock low for four XIN clock cycles for integer divisors and four-and-a-half XIN clock cycles for integer-plus-a-half divisors. Based on the above parameters, the acceptable XIN/divisor combinations can be derived. The precision of the programmable clock generator for integer-plus-a-half divisors depends on the closeness to a 50% duty cycle for the XIN input clock.

subsystem PGMCLK register/divide-by-n circuit (continued)

PGMCLK(0–5) VALUE (HEX)	RESULT
0 (0)	No clock (driven high)
0.5 (1)	Divide-by-1
1 (2)	Divide-by-1
1.5 (3)	Divide-by-1
2 (4) to 31.5 (3F)	Divide-by-2 to divide-by-31.5

subsystem serial-bypass mode

The optional serial-bypass mode is implemented to allow a high-throughput path to/from the host CPU. When this mode is enabled and subsystem control register bit 7 is high, the serial portion of the UART is bypassed and the subsystem has direct parallel access to the receiver FIFO (write address 140 hex) and the transmitter FIFO (read address 140 hex). All host CPU interrupts operate normally except for receiver parity, framing, and breaking interrupts.

auto-$\overline{\text{CTS}}$ operation

The optional auto-$\overline{\text{CTS}}$ operation is implemented so that the host CPU cannot overflow the modem receive buffer. Auto-$\overline{\text{CTS}}$ operation is enabled when the subsystem sets MCR (subsystem address 130 hex) bit 5 high. When enabled, deactivating $\overline{\text{CTS}}$ (high) halts the transmitter section of the UART after it completes the current transfer. Once $\overline{\text{CTS}}$ is reactivated (low) by the modem, transfers resume. Interrupt operation is not affected by enabling auto-$\overline{\text{CTS}}$.

auto-$\overline{\text{RTS}}$ operation

The optional auto-$\overline{\text{RTS}}$ operation is implemented so that the subsystem cannot overflow the receiver FIFO. Auto-$\overline{\text{RTS}}$ operation is enabled when FCR bit 4 is high and $\overline{\text{EXTEND}}$ is low and operates independently from the trigger-level circuitry. In the 16-byte FIFO mode, the RTS bit in the modem-control register (bit 1) clears when 14 characters are in the receive FIFO. This action causes $\overline{\text{RTS}}$ to go high (inactive). In the 64-byte FIFO mode, the MCR RTS bit clears when 56 characters are in the receiver FIFO. Interrupt operation is not affected and operates the same way in either auto-$\overline{\text{RTS}}$ or nonauto-$\overline{\text{RTS}}$ mode. If enabled, a receive-data-available interrupt occurs after the trigger level is reached. The MCR RTS bit must then be set by the host CPU after the receiver FIFO has been read.

power consumption

The TL16PC564A has low power consumption under the following conditions:

- 32-MHz signal on XIN
- Divide-by-n is set to give a 1.8432-MHz UARTCLK signal
- Nominal data
- V_{CC} = 5 V

The current (I_{CC}) and power consumption are 18 mA (typical) and 90 mW (typical), respectively. These current and power figures fluctuate with changes in the above conditions.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} .... –0.5 V to 6 V
Input voltage range, V_I (standard) .... –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (fail safe) .... –0.5 V to 6.5 V
Output voltage range, V_O (standard) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (fail safe) .... –0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2) .... ±20 mA
Operating free-air operating temperature range, T_A .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies for external input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail-safe pins.
2. Applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe pins.

recommended operating conditions

low voltage (3.3 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage (CMOS), V_{IH} (see Note 1)		0.7 V_{CC}			V
Low-level input voltage (CMOS), V_{IL} (see Note 1)				0.3 V_{CC}	V
Output voltage, V_O (see Note 2)		0		V_{CC}	V
High-level output current, I_{OH}	All outputs except $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, $\overline{OUT2}$ (see Note 4)			1.8	mA
Low-level output current, I_{OL}	All outputs except $\overline{RST}$			3.2	mA
	$\overline{RST}$			6.4	
Input transition time, t_t		0		25	ns
Operating free-air temperature range, T_A		0	25	70	°C
Junction temperature range, T_J (see Note 3)		0	25	115	°C

standard voltage (5 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage (CMOS), V_{IH}		0.7 V_{CC}			V
Low-level input voltage (CMOS), V_{IL}				0.2 V_{CC}	V
Output voltage, V_O (see Note 2)		0		V_{CC}	V
High-level output current, I_{OH}	All outputs except $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, $\overline{OUT2}$ (see Note 4)			4	mA
Low-level output current, I_{OL}	All outputs except $\overline{RST}$			4	mA
	$\overline{RST}$			8	
Input transition time, t_t		0		25	ns
Operating free-air temperature range, T_A		0	25	70	°C
Junction temperature range, T_J (see Note 3)		0	25	115	°C

NOTES: 1. Meets TTL levels, V_{IH}min = 2 V and V_{IL}max = 0.8 V on nonhysteresis inputs
2. Applies for external output buffers
3. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.
4. $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, and $\overline{OUT2}$ are open-drain outputs, so I_{OH} does not apply.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

low voltage (3.3 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{CC}-0.55$		V
V_{OL}	Low-level output voltage	I_{OL} = rated		0.5	V
V_{IT+}	Positive-going input threshold voltage (see Note 5)			0.7 V_{CC}	V
V_{IT-}	Negative-going input threshold voltage (see Note 5)		0.3 V_{CC}		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$) (see Note 5)		0.1 V_{CC}	0.3 V_{CC}	V
I_{OZ}	3-state-output high-impedance current (see Note 6)	$V_I = V_{CC}$ or GND		±10	µA
I_{IL}	Low-level input current (see Note 7)	V_I = GND		−1	µA
I_{IH}	High-level input current (see Note 8)	$V_I = V_{CC}$		1	µA

standard voltage (5 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{CC}-0.8$		V
V_{OL}	Low-level output voltage	I_{OL} = rated		0.5	V
V_{IT+}	Positive-going input threshold voltage (see Note 5)			0.7 V_{CC}	V
V_{IT-}	Negative-going input threshold voltage (see Note 5)		0.2 V_{CC}		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$) (see Note 5)		0.1 V_{CC}	0.3 V_{CC}	V
I_{OZ}	3-state-output high-impedance current (see Note 6)	$V_I = V_{CC}$ or GND		±10	µA
I_{IL}	Low-level input current (see Note 7)	V_I = GND		−1	µA
I_{IH}	High-level input current (see Note 8)	$V_I = V_{CC}$		1	µA

NOTES: 5. Applies for external input and bidirectional buffers with hysteresis
6. The 3-state or open-drain output must be in the high-impedance state.
7. Specifications only apply with pullup terminator turned off
8. Specifications only apply with pulldown terminator turned off

XIN timing requirements over recommended operating free-air temperature range (see Figure 1)

		TEST CONDITIONS	MIN	MAX	UNIT
	Input frequency	V_{CC} = 3.3 V		50	MHz
		V_{CC} = 5 V		60	
t_{c1}	Cycle time, XIN	V_{CC} = 3.3 V	20		ns
		V_{CC} = 5 V	16.7		
t_{w1}	Pulse duration, XIN clock high	V_{CC} = 3.3 V	10		ns
		V_{CC} = 5 V	8		
t_{w2}	Pulse duration, XIN clock low	V_{CC} = 3.3 V	10		ns
		V_{CC} = 5 V	8		

clock switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time, XIN↑ to UARTCLK↑	V_{CC} = 3.3 V		14	ns
		V_{CC} = 5 V		8	
t_{d2}	Delay time, XIN↓ to UARTCLK↓	V_{CC} = 3.3 V		16	ns
		V_{CC} = 5 V		10	
t_{d3}	Delay time, XIN↑ to UARTCLK↓	V_{CC} = 3.3 V		19.8	ns
		V_{CC} = 5 V		13	
t_{d4}	Delay time, XIN↑ to UARTCLK↑	V_{CC} = 3.3 V		20.6	ns
		V_{CC} = 5 V		13.5	
t_{d5}	Delay time, XIN↓ to UARTCLK↑	V_{CC} = 3.3 V		21	ns
		V_{CC} = 5 V		13.8	

host CPU I/O read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 9)

		MIN	MAX	UNIT
t_{h1}	Hold time, HA(9–0) valid after $\overline{\text{IORD}}$↑	20		ns
t_{h2}	Hold time, $\overline{\text{REG}}$↑ valid after $\overline{\text{IORD}}$↑	0		ns
t_{w4}	Pulse duration, $\overline{\text{IORD}}$ low	165		ns
t_{su1}	Setup time, HA(9–0) valid before $\overline{\text{IORD}}$↓	70		ns
t_{su2}	Setup time, $\overline{\text{CEx}}$↓ before $\overline{\text{IORD}}$↓	5		ns
t_{h3}	Hold time, $\overline{\text{CEx}}$↑ after $\overline{\text{IORD}}$↑	20		ns
t_{h4}	Hold time, HD(7–0) valid after $\overline{\text{IORD}}$↑	0		ns
t_{su3}	Setup time, $\overline{\text{REG}}$↓ before $\overline{\text{IORD}}$↓	5		ns
t_{d6}	Delay time, HD(7–0) valid after $\overline{\text{IORD}}$↓		100	ns

host CPU I/O read-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 9)

PARAMETER		MIN	MAX	UNIT
t_{d7}	Delay time, $\overline{\text{INPACK}}$↓ after $\overline{\text{IORD}}$↓		45	ns
t_{d8}	Delay time, $\overline{\text{INPACK}}$↑ after $\overline{\text{IORD}}$↑		45	ns

NOTE 9: The maximum load on $\overline{\text{INPACK}}$ is one LSTTL with 50-pF total load. All timing is measured in nanoseconds.

host CPU I/O write-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 3)

		MIN	MAX	UNIT
t_{su4}	Setup time, HD(7–0) valid before $\overline{IOWR}$↓	60		ns
t_{h5}	Hold time, HA(9–0) valid after $\overline{IOWR}$↑	20		ns
t_{w6}	Pulse duration, $\overline{IOWR}$ low	165		ns
t_{su5}	Setup time, HA(9–0) valid before $\overline{IOWR}$↓	70		ns
t_{h6}	Hold time, $\overline{REG}$↑ after $\overline{IOWR}$↑	0		ns
t_{su6}	Setup time, $\overline{CEx}$↓ before $\overline{IOWR}$↓	5		ns
t_{h7}	Hold time, $\overline{CEx}$↑ after $\overline{IOWR}$↑	20		ns
t_{su7}	Setup time, $\overline{REG}$↓ before $\overline{IOWR}$↓	5		ns
t_{h8}	Hold time, HD(7–0) valid after $\overline{IOWR}$↑	30		ns

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time, $\overline{SOUT}$↓ after $\overline{IOWR}$↑		8	24	Baud cycles
t_{d10}	Delay time, $\overline{IREQ}$↓ after $\overline{SOUT}$↓		8	8	Baud cycles
t_{d11}	Delay time, $\overline{IREQ}$↓ after $\overline{IOWR}$↑		16	32	Baud cycles
t_{d12}	Delay time, $\overline{IREQ}$↑ after $\overline{IOWR}$↑	C_L = 100 pF		140	ns
t_{d13}	Delay time, $\overline{IREQ}$↑ after $\overline{IORD}$↑	C_L = 100 pF		140	ns

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay time, sample CLK↑ after RCLK↑			100	ns
t_{d15}	Delay time, $\overline{IREQ}$↓ after SIN↓			1	RCLK cycles
t_{d16}	Delay time, $\overline{IREQ}$↑ after $\overline{IORD}$↑	C_L = 100 pF		150	ns

modem-control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 6)

PARAMETER		MIN	MAX	UNIT
t_{d17}	Delay time, $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$, $\overline{OUT2}$ ↓ or ↑ after $\overline{IOWR}$↑		50	ns
t_{d18}	Delay time, $\overline{IREQ}$↓ after $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$↓		30	ns
t_{d19}	Delay time, $\overline{IREQ}$↑ after $\overline{IORD}$↑		35	ns
t_{d20}	Delay time, $\overline{IREQ}$↓ after $\overline{RI}$↑		30	ns

host CPU attribute-memory write-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figures 7 and 8)

		MIN	MAX	UNIT
t_{c2}	Write cycle time, HA(9–0)	250		ns
t_{w8}	Pulse duration, $\overline{WE}$ low	150		ns
t_{su8}	Setup time, $\overline{CE}$x↓ before $\overline{WE}$↑	180		ns
t_{su9}	Setup time, HA(9–0) before $\overline{WE}$↑ (see Note 10)	180		ns
t_{su10}	Setup time, HA(9–0) before $\overline{WE}$↓ and $\overline{CE}$x↓(see Note 10)	30		ns
t_{su11}	Setup time, $\overline{OE}$↑ before $\overline{WE}$↓	10		ns
t_{h9}	Hold time, HD(7–0) after $\overline{WE}$↑	30		ns
t_{rec1}	Recovery time, HA(9–0) after $\overline{WE}$↑	30		ns
t_{su12}	Setup time, HD(7–0) before $\overline{WE}$↑	80		ns
t_{h10}	Hold time, $\overline{OE}$↓ after $\overline{WE}$↑	10		ns
t_{su13}	Setup time, $\overline{CE}$x↓ before $\overline{WE}$↓	0		ns
t_{h11}	Hold time, $\overline{CE}$x↑ after $\overline{WE}$↑	20		ns

NOTE 10: The $\overline{REG}$ signal timing is identical to address signal timing.

host CPU attribute-memory write-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 7)

PARAMETER		MIN	MAX	UNIT
t_{dis1}	Disable time, HD(7–0) after $\overline{WE}$↓		100	ns
t_{dis2}	Disable time, HD(7–0) after $\overline{OE}$↑		100	ns
t_{en1}	Enable time, HD(7–0) after $\overline{WE}$↑	5		ns
t_{en2}	Enable time, HD(7–0) after $\overline{OE}$↓	5		ns

host CPU attribute-memory read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

		MIN	MAX	UNIT
t_{c3}	Read cycle time	300		ns
t_{d22}	Delay time, HD(7–0) after HA(9–0)		300	ns
t_{d23}	Delay time, HD(7–0) after $\overline{CE}$x↓		300	ns
t_{d24}	Delay time, HD(7–0) after $\overline{OE}$↓		150	ns
t_{h12}	Hold time, HD(7–0) after HA(9–0)	0		ns
t_{su14}	Setup time, $\overline{CE}$x↓ before $\overline{OE}$↓	0		ns
t_{h13}	Hold time, HA(9–0) after $\overline{OE}$↑	20		ns
t_{su15}	Setup time, HA(9–0) before $\overline{OE}$↓	30		ns
t_{h14}	Hold time, $\overline{CE}$x↑ after $\overline{OE}$↑	20		ns

host CPU attribute-memory read-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

PARAMETER		MIN	MAX	UNIT
t_{dis3}	Disable time, HD(7–0) after $\overline{CE}$x↑		100	ns
t_{dis4}	Disable time, HD(7–0) after $\overline{OE}$↑		100	ns
t_{en3}	Enable time, HD(7–0) after $\overline{CE}$x↓	5		ns
t_{en4}	Enable time, HD(7–0) after $\overline{OE}$↓	5		ns

subsystem Intel-mode timing requirements (32 MHz) (see Figure 10)

INTEL SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
t_{LHLL}	t_{w11}	Pulse duration, ALE high	48		ns
t_{AVLL}	t_{su16}	Setup time, SA8, SAD(7–0) valid to ALE low	21		ns
t_{PLLL}	t_{d25}	Delay time, $\overline{CS}$ low to ALE low	21		ns
t_{LLAX}	t_{h15}	Hold time, SA8, SAD(7–0) valid after ALE↓	21		ns
t_{LLWL}	t_{d26}	Delay time, ALE low to $\overline{WR}$ low	16		ns
t_{LLRL}	t_{d27}	Delay time, ALE low to $\overline{RD}$ low	16		ns
t_{WHLH}	t_{d28}	Delay time, $\overline{WR}$ high to ALE high	21		ns
t_{AFRL}	t_{d29}	Delay time, SA8, SAD(7–0) in high-impedance state to $\overline{RD}$ low	0		ns
t_{RLRH}	t_{w12}	Pulse duration, $\overline{RD}$ low	120		ns
t_{WLWH}	t_{w13}	Pulse duration, $\overline{WR}$ low	120		ns
t_{RHAX}	t_{d30}	Delay time, $\overline{RD}$ high to SA8, SAD(7–0) active	48		ns
t_{WHDX}	t_{h16}	Hold time, SA8, SAD(7–0) valid after $\overline{WR}$ high	48		ns
t_{WHPH}	t_{d31}	Delay time, $\overline{WR}$ high to $\overline{CS}$ high	21		ns
t_{RHPH}	t_{d32}	Delay time, $\overline{RD}$ high to $\overline{CS}$ high	21		ns
t_{PHPL}	t_{w14}	Pulse duration, $\overline{CS}$ high	21		ns

subsystem Zilog-mode timing requirements (20 MHz) (see Figure 11)

ZILOG SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
$t_{dA(AS)}$	t_{su17}	Setup time, SA8 and SAD(7–0) valid before $\overline{AS}$ high	20		ns
$t_{dAS(A)}$	t_{d33}	Delay time, $\overline{AS}$ high to SA8 and SAD(7–0) invalid	35		ns
$t_{dAS(DR)}$	t_{d34}	Delay time, $\overline{AS}$ high to data in on SAD(7–0)		150	ns
t_{wAS}	t_{w15}	Pulse duration, $\overline{AS}$ low	35		ns
$t_{dA(DS)}$	t_{d35}	Delay time, SA8 and SAD(7–0) invalid to $\overline{DS}$ low	0		ns
$t_{wDS(read)}$	t_{w16}	Pulse duration, $\overline{DS}$ low (read)	125		ns
$t_{wDS(write)}$	t_{w17}	Pulse duration, $\overline{DS}$ low (write)	65		ns
$t_{dDS(DR)}$	t_{d36}	Delay time, $\overline{DS}$ low to data in valid		80	ns
$t_{hDS(DR)}$	t_{h17}	Hold time, $\overline{DS}$ high to data in invalid	0		ns
$t_{dDS(A)}$	t_{h18}	Hold time, $\overline{DS}$ high to data out invalid	20		ns
$t_{dDS(AS)}$	t_{d37}	Delay time, $\overline{DS}$ high to $\overline{AS}$ low	30		ns
$t_{dDO(DS)}$	t_{d38}	Delay time, SAD(7–0) (write data from µP) valid to $\overline{DS}$ low	10		ns
$t_{dRW(AS)}$	t_{d39}	Delay time, R/$\overline{W}$ active to AS high	20		ns

subsystem Intel nonmultiplexed timing requirements (see Figure 12)

		MIN	MAX	UNIT
t_{su18}	Setup time, SA(8–0), $\overline{CS}$ valid to $\overline{RD}$, $\overline{WR}$↓	30		ns
t_{w18}	Pulse duration, $\overline{RD}$ low	120		ns
t_{w19}	Pulse duration, $\overline{WR}$ low	120		ns
t_{su19}	Setup time, SAD(7–0) valid to $\overline{WR}$↑	50		ns
t_{en4}	Enable time, $\overline{RD}$↓ to SAD(7–0) driving	5		ns
t_{d40}	Delay time, $\overline{RD}$↓ to SAD(7–0) valid		105	ns
t_{h19}	Hold time, SA(8–0), $\overline{CS}$ valid after $\overline{RD}$, $\overline{WR}$↑	30		ns
t_{h20}	Hold time, SAD(7–0) valid after $\overline{WR}$↑	30		ns
t_{dis3}	Disable time, $\overline{RD}$↑ to SAD(7–0) high impedance	5	15	ns

subsystem Zilog nonmultiplexed timing requirments (see Figure 13)

		MIN	MAX	UNIT
t_{su20}	Setup time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid to $\overline{DS}$↓ (write)	90		ns
t_{su21}	Setup time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid to $\overline{DS}$↓ (read)	30		ns
t_{w20}	Pulse duration, $\overline{DS}$ low (write)	65		ns
t_{w21}	Pulse duration, $\overline{DS}$ low (read)	125		ns
t_{su22}	Setup time, SAD(7–0) valid to $\overline{DS}$↑	50		ns
t_{en5}	Enable time, $\overline{DS}$↓ to SAD(7–0) driving	5		ns
t_{d41}	Delay time, $\overline{DS}$↓ to SAD(7–0) valid		105	ns
t_{h21}	Hold time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid after $\overline{DS}$↑	30		ns
t_{h22}	Hold time, SAD(7–0), $\overline{CS}$, R/$\overline{W}$ valid after $\overline{DS}$↑	30		ns
t_{dis4}	Hold time, $\overline{DS}$↑ to SAD(7–0) high impedance	5	15	ns

ARBCLK switching characteristics over recommended operating free-air temperature range (see Figure 14)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{c4}	Cycle time, internal arbitration clock (ARBCLKI ÷ ARBPGM)	V_{CC} = 3.3 V	26	Note 11	ns
		V_{CC} = 5 V	14	Note 11	
t_{c5}	Cycle time, arbitration clock	V_{CC} = 3.3 V	26		ns
		V_{CC} = 5 V	14		
t_{d42}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷1)	V_{CC} = 3.3 V		13	ns
		V_{CC} = 5 V		7.3	
t_{d43}	Delay time, ARBCLKI↓ to ARBCLK0↓ (÷1)	V_{CC} = 3.3 V		15.5	ns
		V_{CC} = 5 V		10	
t_{d44}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷2)	V_{CC} = 3.3 V		15.3	ns
		V_{CC} = 5 V		8.8	
t_{d45}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷2)	V_{CC} = 3.3 V		17.5	ns
		V_{CC} = 5 V		11	
t_{d46}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷4)	V_{CC} = 3.3 V		19.5	ns
		V_{CC} = 5 V		11.5	
t_{d47}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷4)	V_{CC} = 3.3 V		21.5	ns
		V_{CC} = 5 V		13.5	
t_{d48}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷8)	V_{CC} = 3.3 V		22.7	ns
		V_{CC} = 5 V		13.5	
t_{d49}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷8)	V_{CC} = 3.3 V		25	ns
		V_{CC} = 5 V		15.7	

NOTE 11: t_{c4} MAX = N/6, where N = shortest (in ns) of the two attribute-memory accesses, host CPU or subsystem.

reset timing requirements over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Figure 15)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{w22}	Pulse duration, RESET active		$8 \cdot t_{c5}$		ns
t_{w23}	Pulse duration, RESET inactive		$8 \cdot t_{c5}$		ns
t_{d50}	Delay time, ARBCLKI↑ to $\overline{RST}$ low	V_{CC} = 3.3 V		10.4	ns
		V_{CC} = 5 V		7.5	
t_{d51}	Delay time, ARBCLKI↑ to $\overline{RST}$ high impedance	V_{CC} = 3.3 V		13.9	ns
		V_{CC} = 5 V		9.7	

subsystem interrupt-request timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 16)

		MIN	MAX	UNIT
t_{d52}	Delay time, $\overline{WE}$↑ to IRQ↑ (see Note 11)	$2t_{c5}$	$3t_{c5}$	ARBCLKI cycles
t_{d53}	Delay time, SCR bit 6↑ to IRQ↓ (see Note 12)	t_{c5}	$2t_{c5}$	ARBCLKI cycles

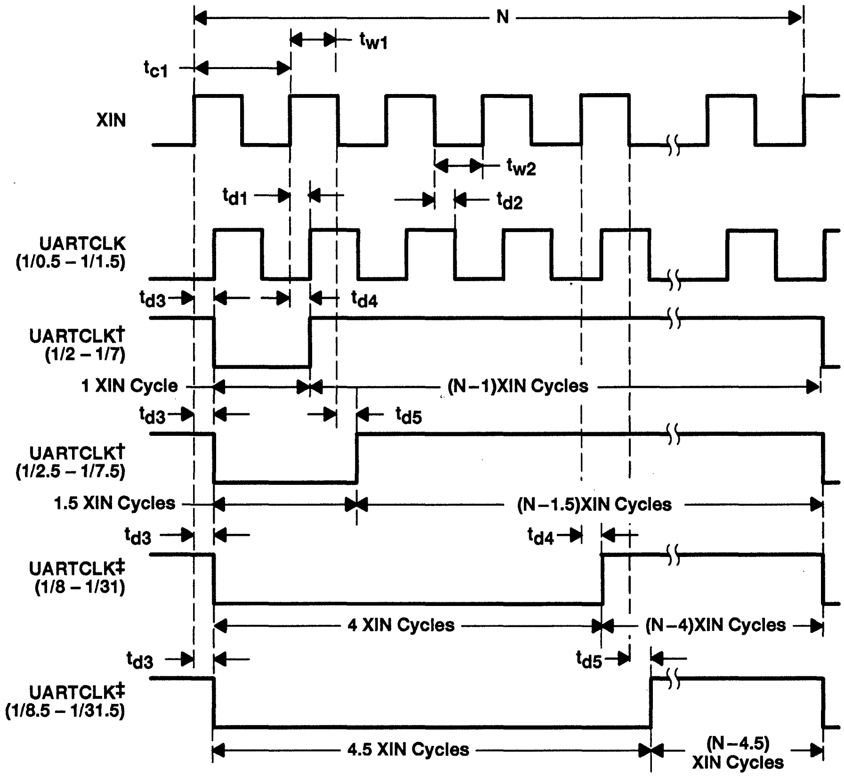
NOTES: 12. Synchronized to rising edge of ARBCLKI
13. Synchronized to falling edge of ARBCLKI

host CPU status change timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 17)

		MIN	MAX	UNIT
t_{d54}	Delay time, subsystem write↑ to $\overline{STSCHG}$↓ (see Note 12)	$2t_{c5}$	$3t_{c5}$	ARBCLKI cycles
t_{d55}	Delay time, $\overline{OE}$↓ to $\overline{STSCHG}$ high impedance (see Note 13)	t_{c5}	$2t_{c5}$	ARBCLKI cycles

NOTES: 12. Synchronized to rising edge of ARBCLKI
13. Synchronized to falling edge of ARBCLKI

PARAMETER MEASUREMENT INFORMATION

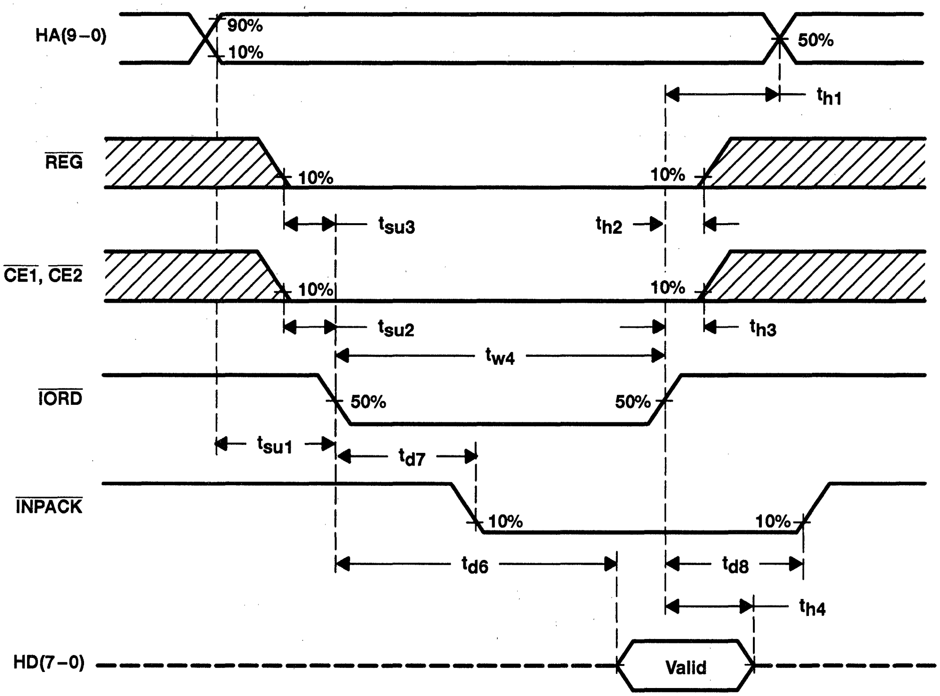


† The low portion of the UARTCLK cycle = 1 XIN cycle for PGMCLK integer values of 2 to 7 and 1.5 XIN cycles for PGMCLK noninteger values 2.5 to 7.5.

‡ The low portion of the UARTCLK cycle = 4 XIN cycles for PGMCLK integer values of 8 to 31 and 4.5 XIN cycles for PGMCLK noninteger values 8.5 to 31.5.

Figure 1. XIN Clock Timing Waveforms

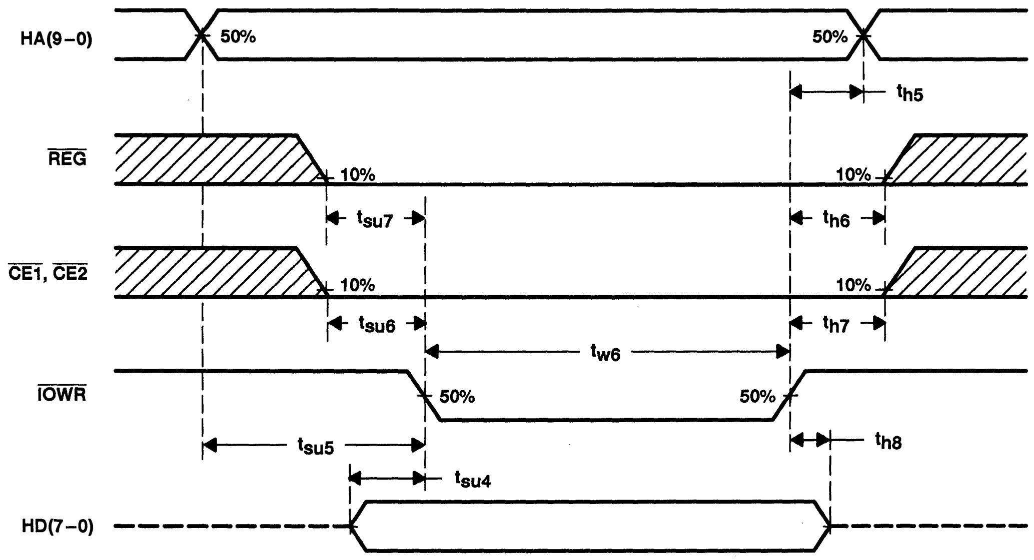
PARAMETER MEASUREMENT INFORMATION



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 2. Host CPU I/O Read Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 3. Host CPU I/O Write Timing Waveforms

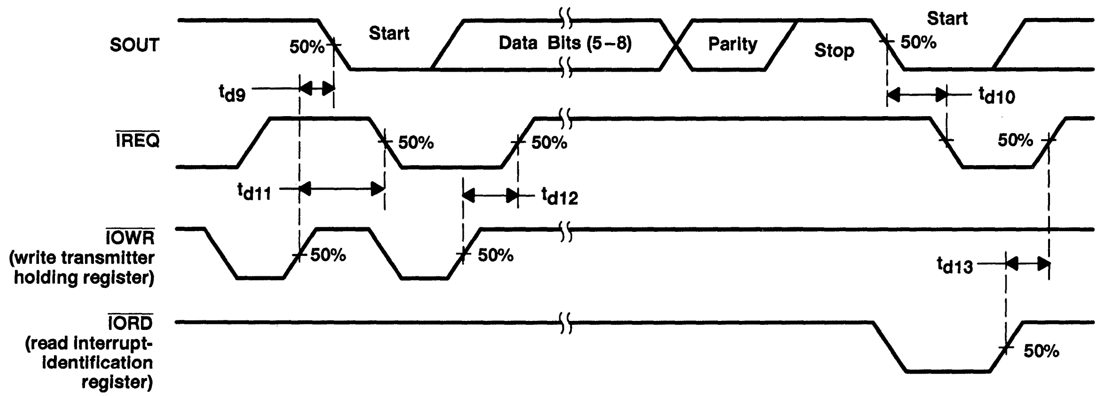


Figure 4. Transmitter Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

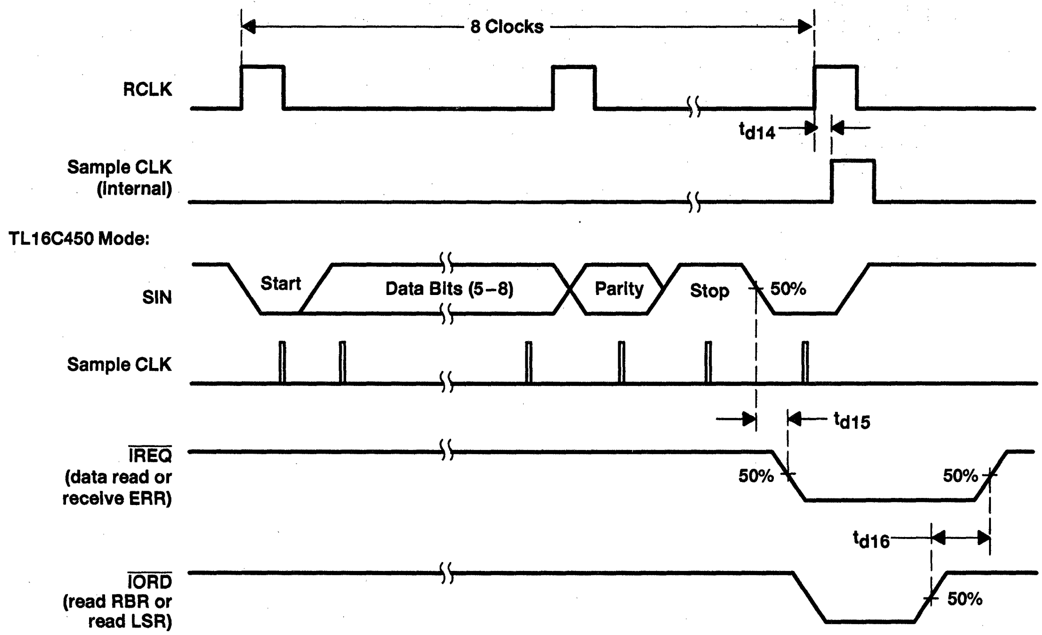


Figure 5. Receiver Timing Waveforms

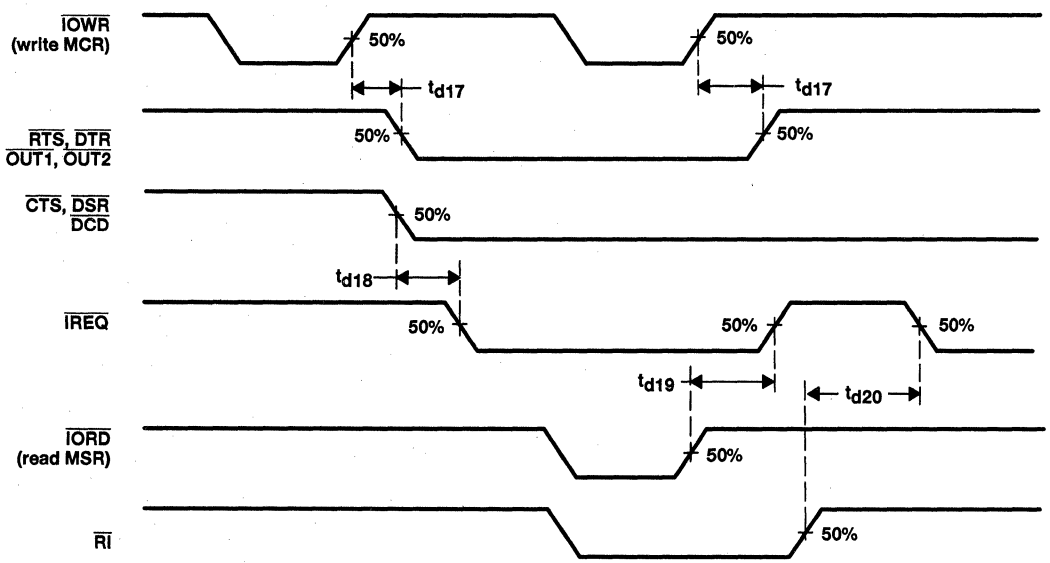
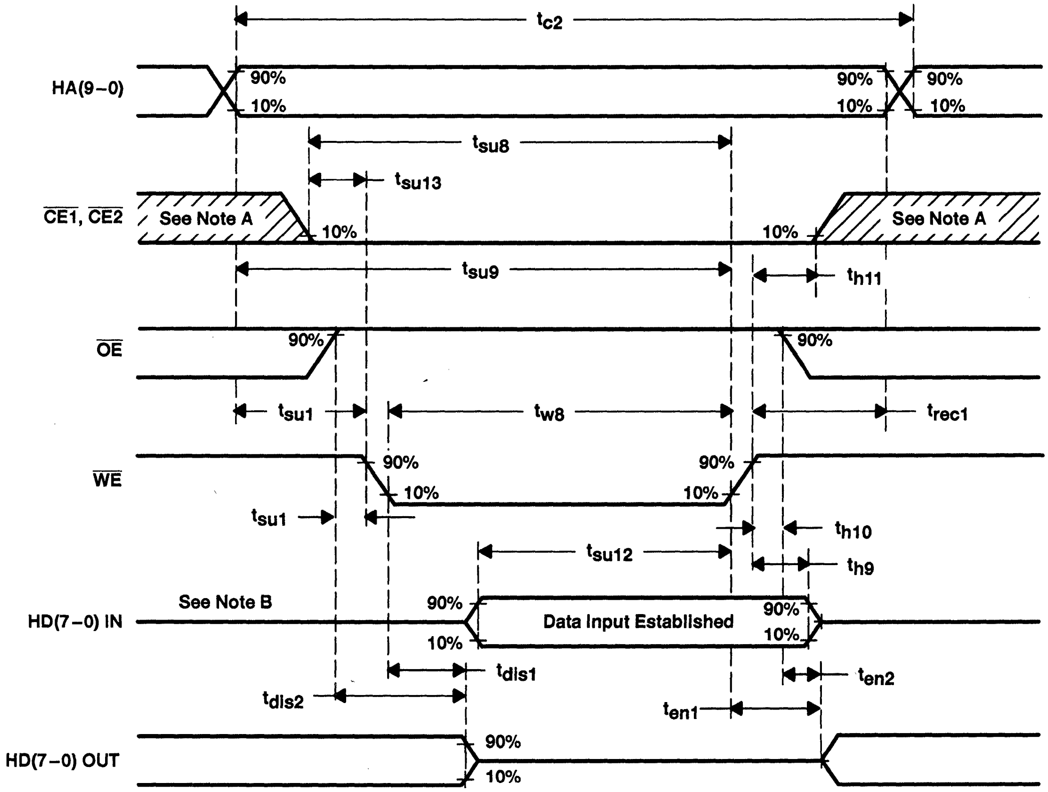


Figure 6. Modem-Control Timing Waveforms

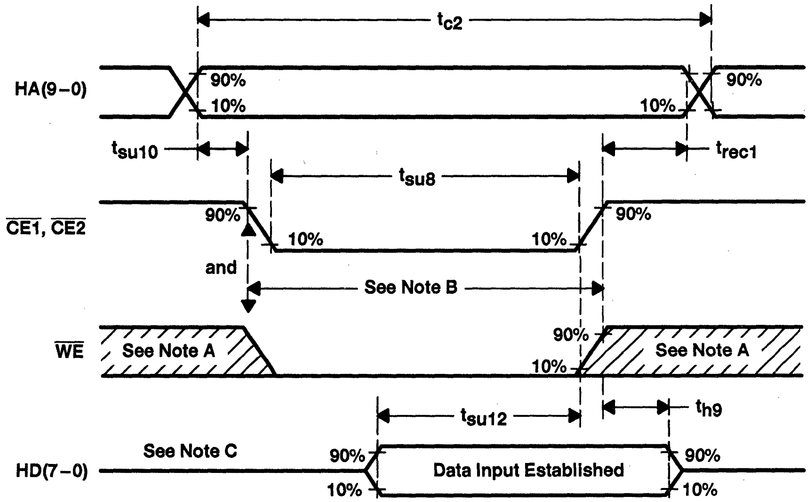
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The hatched portion may be either high or low.
B. When the data I/O terminal is in the output state, no signals shall be applied to HD(7–0) by the system.

Figure 7. Host CPU Attribute-Memory Write Timing Waveforms ($\overline{\text{WE}}$ Control)

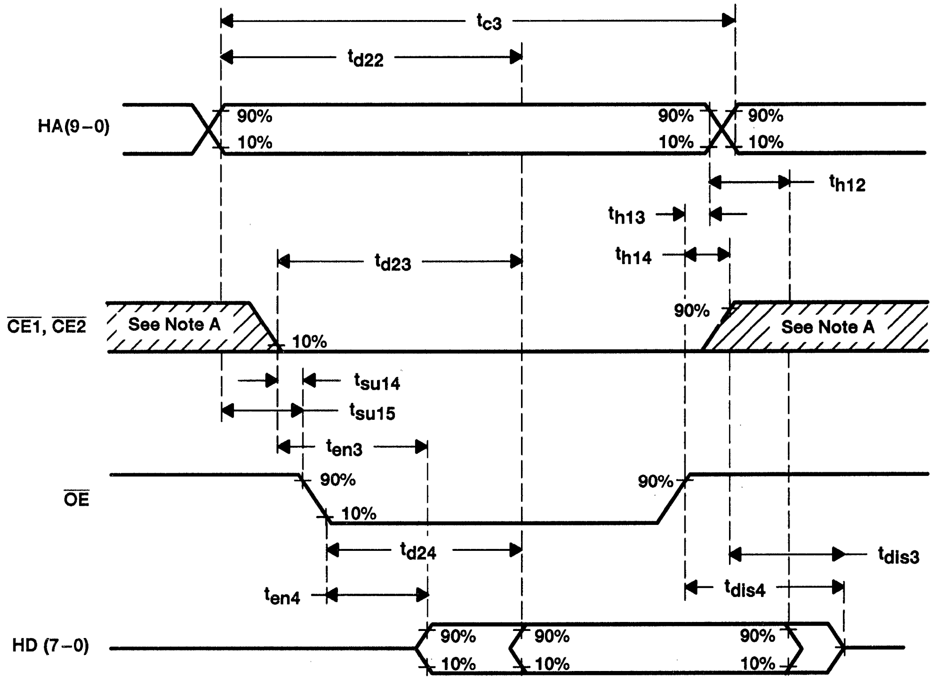
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The hatched portion may be either high (H) or low (L).
B. $\overline{\text{OE}}$ must be high (H).
C. When the data I/O terminal is in the output state, no signals shall be applied to HD(7–0) by the system.

Figure 8. Host CPU Attribute-Memory Write Timing Waveforms ($\overline{\text{CE}}$ Control)

PARAMETER MEASUREMENT INFORMATION



NOTE A: The shaded portion may be either high or low.

Figure 9. Host CPU Attribute-Memory Read Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

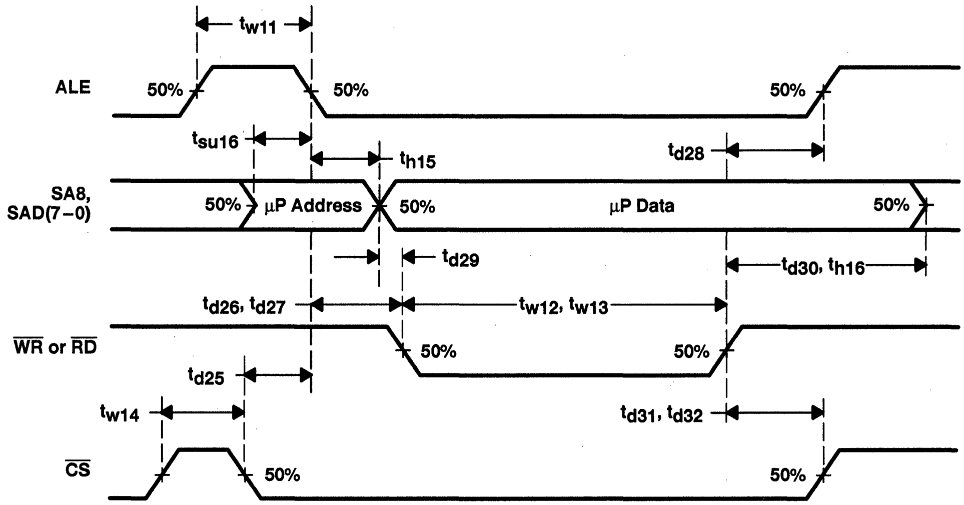


Figure 10. Subsystem Intel-Mode Timing Waveforms

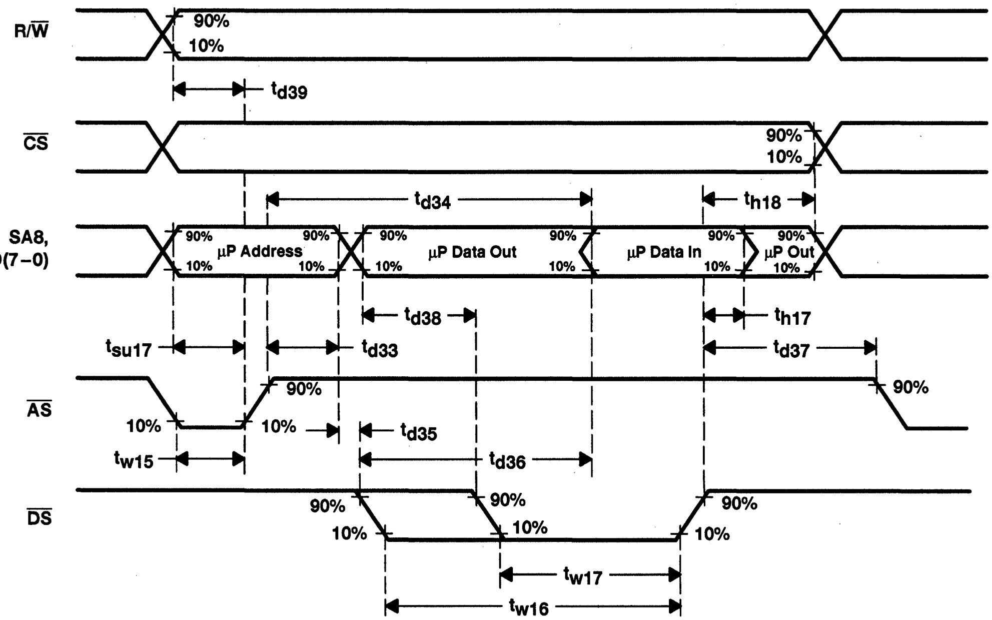


Figure 11. Subsystem Zilog-Mode Timing Waveforms

NOTE A: Figures 10 and 11 are from the microprocessor perspective, not from the UART perspective.

PARAMETER MEASUREMENT INFORMATION

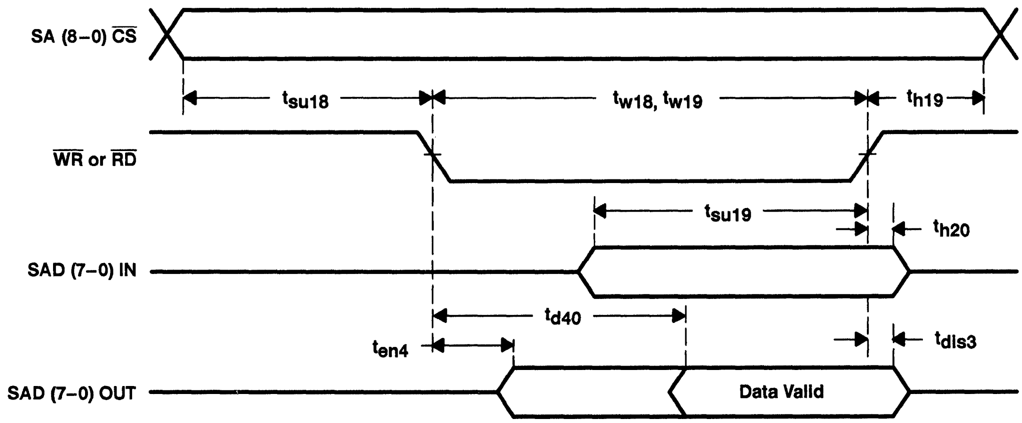


Figure 12. Subsystem Intel Nonmultiplexed Timing Waveforms

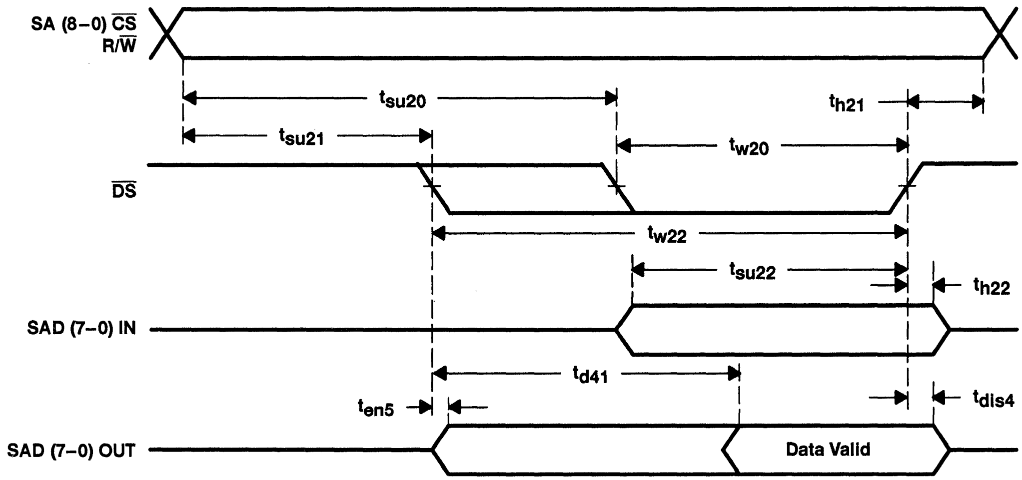


Figure 13. Subsystem Zilog Nonmultiplexed Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

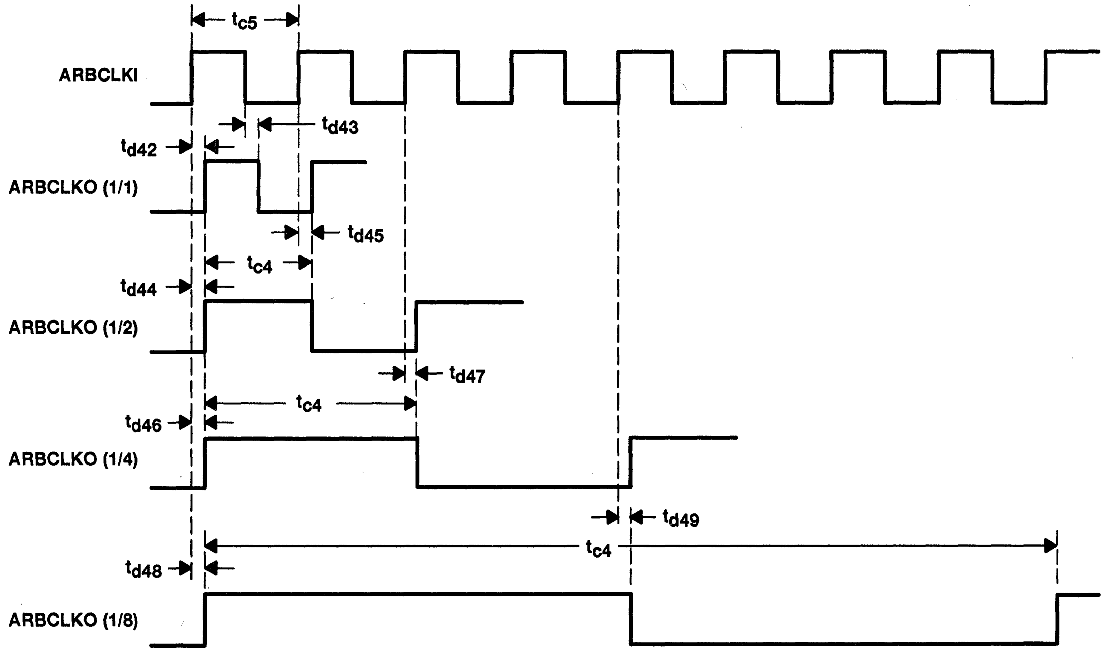


Figure 14. Arbitration-Clock Timing Waveforms

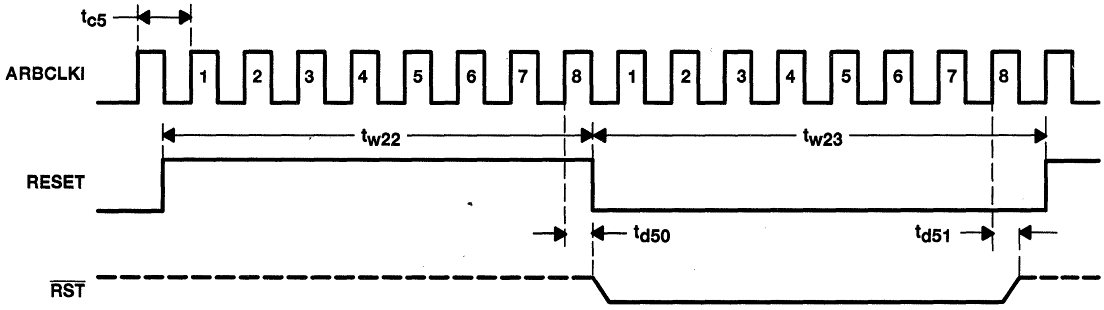


Figure 15. Reset Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

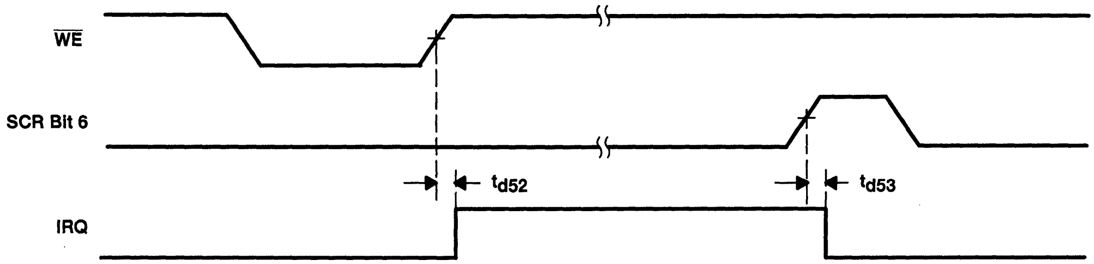


Figure 16. IRQ Timing Waveforms

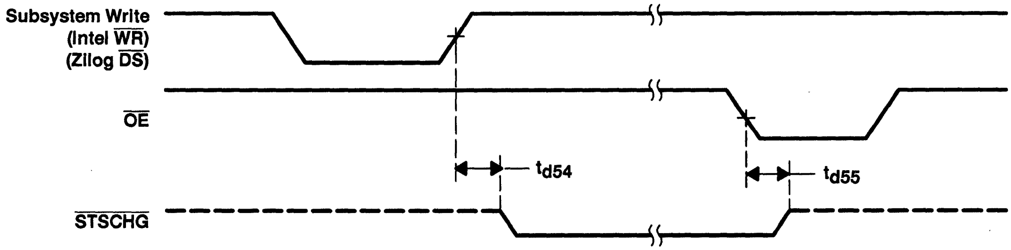


Figure 17. STSCHG Timing Waveforms

General Information 1

Linear and Mixed Signal 2

Computer and Computer Peripherals 3

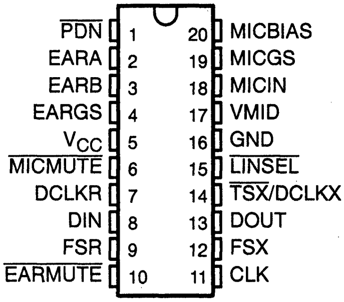
Telecommunications 4

Optoelectronics 5

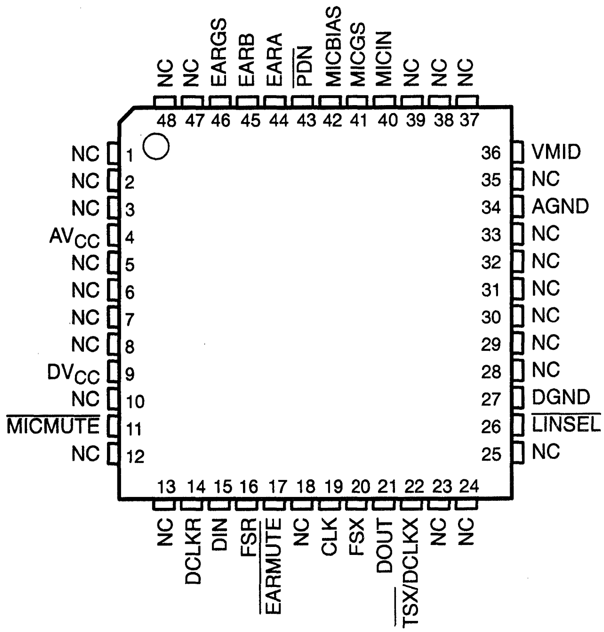
Mechanical Data 6

- **Single 3-V Operation**
- **Low Power Consumption:**
  Operating Mode . . . 20 mW Typ
  Standby Mode . . . 5 mW Typ
  Power-Down Mode . . . 2 mW Typ
- **Combined ADC, DAC, and Filters**
- **Electret Microphone Bias Reference Voltage Available**
- **Drives a Piezo Speaker Directly**
- **Compatible With All DSPs**
- **Selectable Between 8-Bit Companded and 13-Bit (Dynamic Range) Linear Conversion:**
  TLV320AC36 . . . μ-Law and Linear Modes
  TLV320AC37 . . . A-Law and Linear Modes
- **Programmable Volume Control in Linear Mode**
- **Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, DECT, GSM, and PCN Hand-Held Battery-Powered Telephones**

DW OR N PACKAGE
(TOP VIEW)



PT PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLV320AC36 and TLV320AC37 voice-band audio processor (VBAP™) integrated circuits are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band communications systems. Cellular telephone systems are targeted in particular; however, these integrated circuits can function in other systems including digital audio, telecommunications, and data acquisition.

These devices are pin selectable for either of two modes, providing data in two formats: companded and linear. When the device is in the companded mode, data is transmitted and received in eight-bit words. When the linear mode is selected, 13 bits of data are sent and received, padded with zeros to provide a 16-bit word.

Caution. These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description (continued)

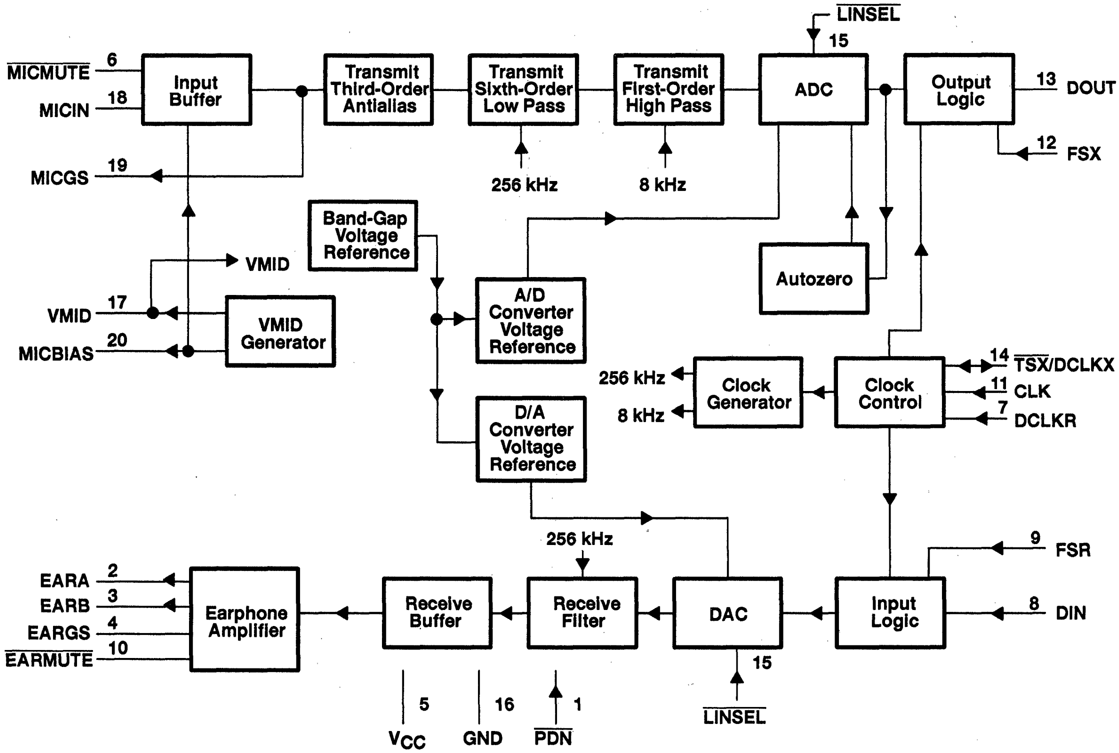
The transmit section is designed to interface directly with an electret microphone element. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then applied to the input of a compressing analog-to-digital converter (COADC) if companded mode is selected. Otherwise, the analog-to-digital converter performs a linear conversion.

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) if the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain and is designed to minimize static power dissipation.

A single on-chip high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages. An internal reference voltage equal to $V_{CC}/2$, VMID, is used to develop the mid-level virtual ground for all the amplifier circuits and the microphone bias circuit. Another reference voltage, MICBIAS, can be used to supply bias current for the microphone.

The TLV320AC3xC devices are characterized for operation from 0°C to 70°C. The TLV320AC3xI devices are characterized from −40°C to 85°C.

functional block diagram



Pin numbers shown are for the DW and N packages.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DW, N	PT		
AGND	—	34		Ground return for all internal analog circuits
AV_{CC}	—	4		3-V supply voltage for all internal analog circuits
CLK	11	19	I	In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input. In the variable-data-rate mode, CLK serves only as the master clock input.
DCLKR	7	14	I	Selects fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock.
DGND	—	27		Ground return for all internal digital circuits
DIN	8	15	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate.
DOUT	13	21	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate.
DV_{CC}	—	9		3-V supply voltage for all internal digital circuits
EARA	2	44	O	Earphone output. EARA forms a differential drive when used with the EARB signal.
EARB	3	45	O	Earphone output. EARB forms a differential drive when used with the EARA signal.
EARGS	4	46	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB. Minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an RC approach.
$\overline{\text{EARMUTE}}$	10	17	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone.
FSR	9	16	I	Frame-synchronization clock input for receive channel. In the variable-data-rate mode, FSR must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer.
FSX	12	20	I	Frame-synchronization clock input for transmit channel. FSX operates independently of, but in an analogous manner to, FSR. The transmit channel enters the standby state when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer.
GND	16	—		Ground return for all internal circuits
$\overline{\text{LINSEL}}$	15	26	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. Companding code on the 'AC36 is µ-law, and companding code on the 'AC37 is A-law.
MICBIAS	20	42	O	Bias voltage equal to VMID for the electret microphone
MICGS	19	41	O	Output of the internal microphone amplifier. MICGS is used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS.
MICIN	18	40	I	Electret microphone input to the internal microphone amplifier
$\overline{\text{MICMUTE}}$	6	11	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), zero code is transmitted.
$\overline{\text{PDN}}$	1	43	I	Power-down input. When low, the device powers down to reduce power consumption.
$\overline{\text{TSX}}$/DCLKX	14	22	I/O	Transmit time-slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input.
V_{CC}	5	—		3-V supply voltage for all internal circuits
VMID	17	36	O	$V_{CC}/2$ bias voltage reference. An external, low-leakage, high-frequency 1-µF capacitor should be connected to VMID for filtering.

general information

system reliability features

The device should be powered up and initialized as follows:

1. Apply GND
2. Apply V_{CC}
3. Connect all clocks
4. Apply TTL high to $\overline{PDN}$
5. Apply synchronizing pluses to FSX and/or FSR

Even though the VBAP is heavily protected against latch-up, it is still possible to cause it to latch-up under certain improper power conditions. To ensure that latch-up does not occur, a reverse-biased Schottky diode should be connected between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{TSX}$ are held in the high-impedance state for approximately four frames (500 μs) after power up (application of V_{CC}). After this delay, DOUT, $\overline{TSX}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{TSX}$ are placed in a high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{PDN}$. In the absence of a signal, $\overline{PDN}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 2 mW.

Three standby modes give the user the options of placing the entire device on standby, placing only the transmit channel on standby, or placing only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation (receive channel on standby), FSX is pulsing and FSR is held low. For receive-only operation (transmit section on standby), FSR is pulsing and FSX is held low. When the entire device is in standby mode, power consumption is reduced to 5 mW (see Table 1 for power-down and standby procedures).

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{PDN}$ = high, FSX = pulses, FSR = pulses	20 mW	Digital outputs active but not loaded
Power down	$\overline{PDN}$ = low, FSX/FSR = X/X	2 mW	$\overline{TSX}$ and DOUT in a high-impedance state
Entire device on standby	FSX = low, FSR = low, $\overline{PDN}$ = high	5 mW	$\overline{TSX}$ and DOUT in a high-impedance state
Only transmit on standby	FSX = low, FSR = pulses, $\overline{PDN}$ = high	10 mW	$\overline{TSX}$ and DOUT in a high-impedance state within 5 frames
Only receive on standby	FSR = low, FSX = pulses, $\overline{PDN}$ = high	10 mW	Digital outputs active but not loaded

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC} and uses the master clock (CLK), frame-synchronization clocks (FSX and FSR), and $\overline{TSX}$. FSX and FSR set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and sixteen bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX, respectively. This allows the data to be transferred into and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

To avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time-slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

conversion laws

The TLV320AC36 provides μ-law companding operation as specified by CCITT G.711 recommendation. The TLV320AC37 provides A-law companding operation as specified by CCITT G.711 recommendation. The linear mode of operation is the same for both the TLV320AC36 and the TLV320AC37, and uses a 13-bit 2s-complement format.

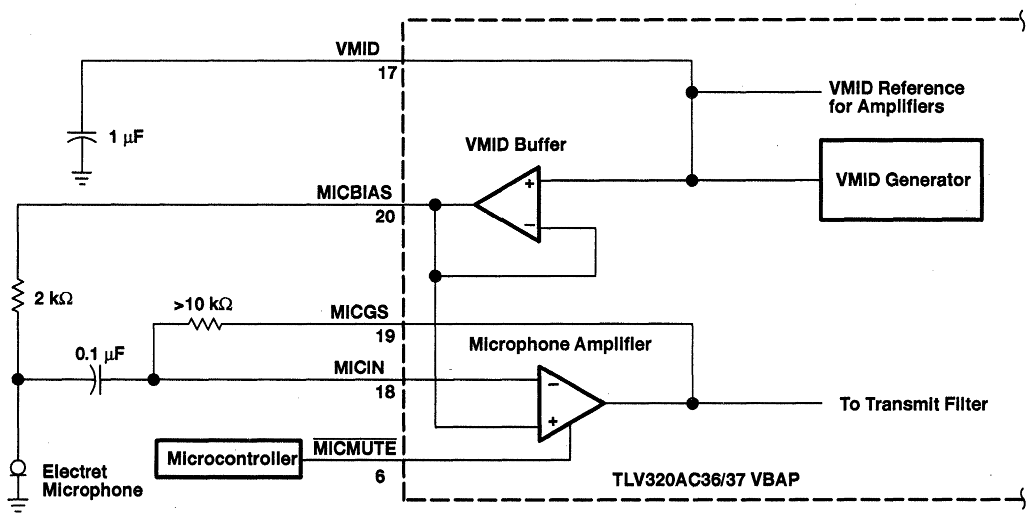
transmit operation

microphone input

The microphone input amplifier is specifically designed to interface to electret-type microphone elements as shown in Figure 1. The VMID buffer circuit provides a voltage (MICBIAS) equal to 1/2 V_{CC} as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network and applied to the amplifier inverting input (MICIN) to set the amplifier gain. VMID appears at a terminal to provide a place to filter the VMID voltage.

microphone mute function

The $\overline{\text{MICMUTE}}$ input causes the digital circuitry to transmit all zero code of DOUT.



Pin numbers shown are for the DW and N packages.

Figure 1. Typical Microphone Interface

transmit filter

A low-pass antialiasing filter section is included on the device and achieves 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode and all eight bits represent one audio data sample. The sign bit is the first bit transmitted. The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits are volume control in the receive direction (DIN) and zeros in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and on the last eight clock cycles in variable-data rate. In the linear mode, the serial data word is received at DIN on the first 13 clock cycles. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness and stop-band rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

The receive buffer contains the volume control.

earphone amplifier

The earphone amplifier has a balanced output to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

receive data format

In the companded mode, eight bits of data are received. The sign bit is the first bit received (see Table 2).

In the linear mode, 16 bits of data are received. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control in which the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps giving a maximum attenuation of 21 dB when all bits are 1s. The volume control bits are not latched into the VBAP and must be present in each received data word.

Table 2. Receive Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

relationship between data word and frame sync

Volume control and other control bits always follow the PCM data in time:

Companded Mode: **MSB (sign bit)** … **LSB**

CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0

Companded Data (CD7–CD0)

Linear Mode: **MSB (sign bit)** … **LSB**

LD12 LD11 LD10 LD9 LD8 LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0 V2 V1 V0

Linear Data (LD12–LD0) **Volume Control** (V2–V0)

Time ⟶

where:

CD7–CD0 = Data word when in companded mode
— = Unused bits in companded mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0
LD12–LD0 = Data word when in linear mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.3 V to 5.5 V
Output voltage range at DOUT, V_O .... −0.3 V to 5.5 V
Input voltage range at DIN, V_I .... −0.3 V to 5.5 V
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
I suffix .... −40°C to 85°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
PT	1075 mW	7.1 mW/°C	756 mW	649 mW

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)		2.7	5	V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}			0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)		600		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)			50	nF
Operating free-air temperature, T_A	TLV320AC36C, TLV320AC37C	0	70	°C
	TLV320AC36I, TLV320AC37I	−40	85	

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the following sequence should be followed when applying power:
(1) Connect to GND
(2) Connect V_{CC}
(3) Connect the input signals
When removing power, follow the preceding steps in reverse order.
3. Voltages at analog inputs and outputs and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		6.2	7.5	mA
	Power down	$\overline{PDN}$ is low for 500 μs			0.75	
	Standby–both	$\overline{PDN}$ is high with FSX and FSR missing for 500 μs			2	
	Standby – one	$\overline{PDN}$ is high with FSX and FSR missing for 500 μs			4.5	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = −3.2 mA, V_{CC} = 3 V	2.2	2.8		V
V_{OL}	Low-level output voltage	DOUT	I_{OL} = 3.2 mA, V_{CC} = 3 V		0.2	0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digital input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

microphone interface‡

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset channel voltage at MICIN to DOUT		V_I = 0 to 3 V			±5	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN§				1.5		MHz
C_i	Input capacitance at MICIN					5	pF
A_V	Large-signal voltage amplification at MICGS					10000	V/V
$I_{O(max)}$	Maximum output current	VMID				500	μA
		MICBIAS (source only)				1	mA

speaker interface‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{O(PP)}$	Peak-to-peak ac output voltage				3¶	Vp-p
	Output offset voltage at EARA, EARB (single ended)	Relative to GND			80	mVpk
I_{IL}	Input leakage current at EARGS	V_I = 0 to 4 V			±200	nA
$I_{O(max)}$	Maximum output current	R_L = 600 Ω			±2.5	mA
r_o	Output resistance at EARA, EARB			1		Ω
	Gain change	$\overline{EARMUTE}$ low, max level when muted	−64			dB

† All typical values are at V_{CC} = 3 V and T_A = 25°C.
‡ All parameters are measured between MICIN and GND (unless otherwise noted).
§ The frequency of the first pole is 100 Hz.
¶ 2.5 V_{p-p} when V_{CC} is 2.7 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

transmit gain and dynamic range, companded or linear mode, µ-law or A-law, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (see Note 7)	Companded mode selected, µ-law ('AC36)		0.614	Vrms
	Companded mode selected, A-law ('AC37)		0.616	
	Linear mode selected ('AC36 and 'AC37)		0.626	
Overload-signal level (MICIN at unity gain)	Companded mode selected, µ-law ('AC36)		2.5	Vp-p
	Companded mode selected, A-law ('AC37)		2.5	
	Linear mode selected ('AC36 and 'AC37)		2.5	
Absolute gain error	0-dB input signal		±1	dB
Gain error with input level relative to gain at −10 dB	MICIN to DOUT at 3 dBm0 to −40 dBm0		±0.5	dB
	MICIN to DOUT at −41 dBm0 to −50 dBm0		±1.5	
	MICIN to DOUT at −51 dBm0 to −55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

transmit filter transfer, µ-law, A-law, or linear mode selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	f_{MICIN} = 50 Hz	−10	0	dB
		f_{MICIN} = 200 Hz	−2.8	0	
		f_{MICIN} = 300 Hz to 3 kHz		±0.25	
		f_{MICIN} = 3.3 kHz	−0.55	0.2	
		f_{MICIN} = 3.4 kHz	−1	−0.1	
		f_{MICIN} = 4 kHz		−14	
		f_{MICIN} ≥4.6 kHz		−32	

transmit idle channel noise and distortion, companded mode, µ-law or A-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, psophometrically weighted	MICIN connected to MICGS through a 10-kΩ resistor		−72	dBop
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		10	dBrnCo
Transmit signal-to-distortion ratio with sine-wave input MICIN to DOUT	MICIN to DOUT at 0 dBm0 to −30 dBm0	36		dB
	MICIN to DOUT at −31 dBm0 to −40 dBm0	30		
	MICIN to DOUT at −41 dBm0 to −45 dBm0	20		
Intermodulation distortion, 2-tone CCITT method, composite power level −13 dBm0	CCITT G.712 (7.1), R2	48		dB
	CCITT G.712 (7.2), R3	48		

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. The reference-signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.
8. Transmit noise, linear mode: 200 µVrms is equivalent to –74 dB (referenced to device 0-dB level)

transmit idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		200	μVrms
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to −6 dBm0	48		dB
	MICIN to DOUT at −7 dBm0 to −12 dBm0	46		
	MICIN to DOUT at −13 dBm0 to −18 dBm0	40		
	MICIN to DOUT at −19 dBm0 to −24 dBm0	36		
	MICIN to DOUT at −25 dBm0 to −45 dBm0	24		

receive gain and dynamic range, companded or linear mode, μ-law or A-law, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level at analog output with unity gain (0 dB) (see Note 11)	Companded mode selected, μ-law ('AC36)		0.736	Vrms
	Companded mode selected, A-law ('AC37)		0.739	
	Linear mode selected ('AC36 and 'AC37)		0.751	
Overload-signal level, peak-to-peak	Companded mode selected, μ-law ('AC36)		3	Vp-p
	Companded mode selected, A-law ('AC37)		3	
	Linear mode selected ('AC36 and 'AC37)		3	
Absolute gain error	0-dB input signal		±1	dB
Gain error with output level relative to gain at −10 dBm0	DIN to EARA and EARB at 3 dBm0 to −40 dBm0		±0.5	dB
	DIN to EARA and EARB at −41 dBm0 to −50 dBm0		±1.5	
	DIN to EARA and EARB at −51 dBm0 to −55 dBm0		±2	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature, FSR = 8 kHz (see Note 9)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	DIN = 0 dBm0	f_{DIN} = < 200 Hz		0.25	dB
		f_{DIN} = 200 Hz	−0.5	0.25	
		f_{DIN} = 300 Hz to 3 kHz		±0.25	
		f_{DIN} = 3.3 kHz	−0.55	0.2	
		f_{DIN} = 3.4 kHz	−1	−0.1	
		f_{DIN} = 4 kHz		−14	
		f_{DIN} = > 4.6 kHz		−30	

NOTES: 6. The input amplifier is set for inverting unity gain.
8. Transmit noise, linear mode: 200 μVrms is equivalent to −74 dB (referenced to device 0-dB level)
9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

receive idle channel noise and distortion, companded mode, μ-law or A-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, psophometrically weighted	DIN = 11010101 (A-law)		–72	dBop
Receive noise, C-message weighted	DIN = 11111111 (μ-law)		8	dBrnCo
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –30 dBm0	36		dB
	DIN to EARA and EARB at –31 dBm0 to –40 dBm0	30		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	24		

NOTE 9: Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.

receive idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 9 and 12)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000		250	μVrms
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –5 dBm0	48		dB
	DIN to EARA and EARB at –6 dBm0 to –12 dBm0	46		
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	40		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	36		
	DIN to EARA and EARB at –25 dBm0 to –45 dBm0	25		
Intermodulation, 2-tone CCITT distortion method, composite power level –13 dBm0	CCITT G.712 (7.1), R2	48		dB
	CCITT G.712 (7.2), R3	48		

NOTES: 9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
12. Receive noise, linear mode: 200 μVrms is equivalent to –71 dB (referenced to device 0-dB level)

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply-voltage rejection, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply-voltage rejection, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit to receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	60			dB
Crosstalk attenuation, receive to transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	60			dB

† All typical values are at V_{CC} = 3 V, T_A = 25°C.

timing requirements

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 2, 3, 4, and 5)

		MIN	NOM‡	MAX	UNIT
t_t	Transition time, CLK and DCLK			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLK	45%	50%	55%	

‡ All nominal values are at V_{CC} = 3 V, T_A = 25°C.

transmit timing requirement over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	20	468	ns
$t_{h(FSX)}$	Hold time, FSX	20	468	ns

receive timing requirement over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	20	468	ns
$t_{h(FSR)}$	Hold time, FSR	20	468	ns
$t_{su(DIN)}$	Setup time, DIN	20		ns
$t_{h(DIN)}$	Hold time, DIN	20		ns

transmit timing requirement over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	40	$t_{c(DCLKX)}-40$	ns
$t_{h(FSX)}$	Hold time, FSX	35	$t_{c(DCLKX)}-35$	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	40		ns
$t_{h(FSR)}$	Hold time, FSR	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN	30		ns
$t_{h(DIN)}$	Hold time, DIN	30		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figures 2 and 3)

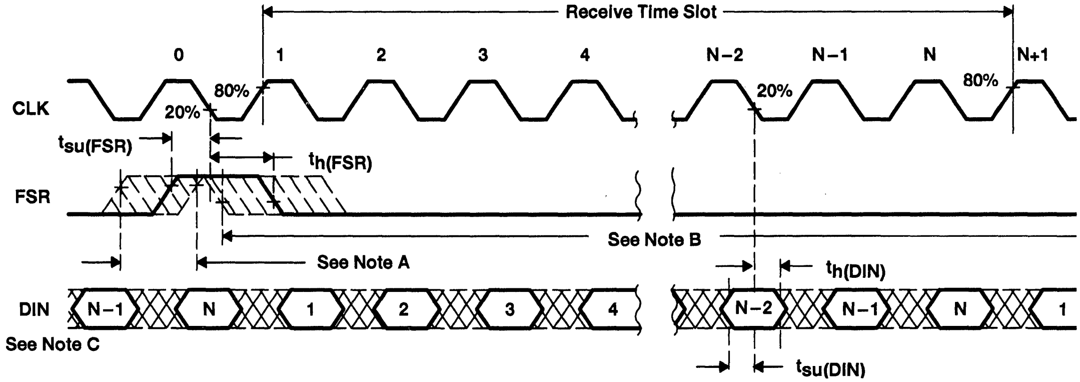
		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK blt 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to $\overline{TSX}$ inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figures 4 and 5)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

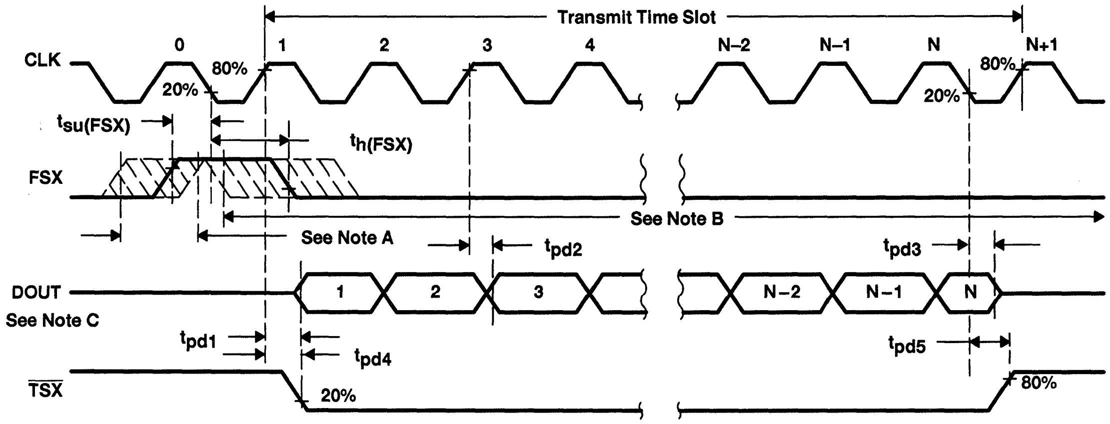
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

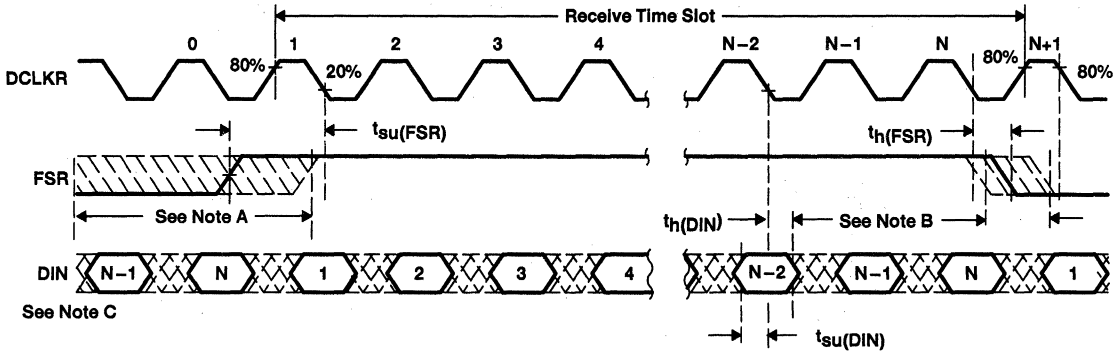
Figure 2. Fixed Data Rate, Receive-Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

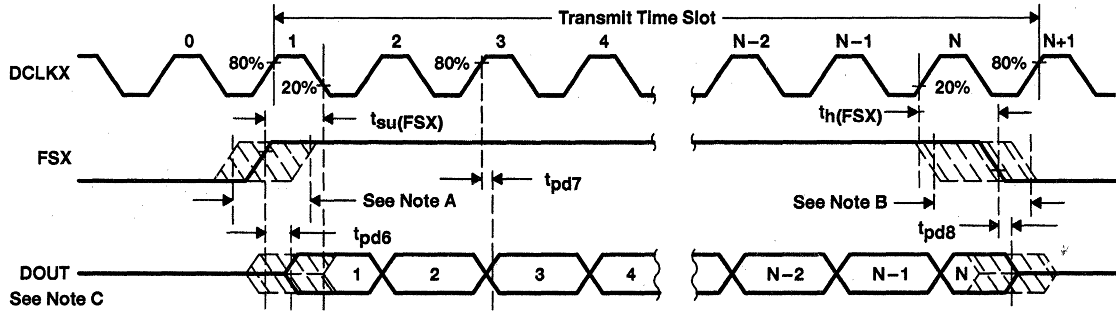
Figure 3. Fixed Data Rate, Transmit-Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 4. Variable Data Rate, Receive-Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 5. Variable Data Rate, Transmit-Side Timing Diagram

APPLICATION INFORMATION

output gain set design considerations (see Figure 6)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

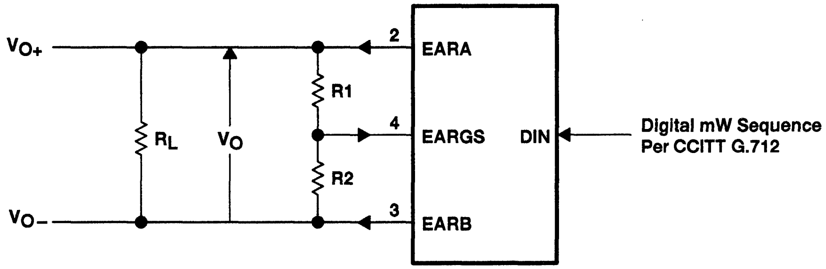
A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital mW output response (V_A = 1.001 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$



Pin numbers shown are for the DW and N package.

Figure 6. Gain-Setting Configuration

- **High-Resolution Conversion of Light Intensity to Frequency With No External Components**
- **Programmable Sensitivity and Full-Scale Output Frequency**
- **Communicates Directly With a Microcontroller**
- **Single-Supply Operation Down to 2.7 V, With Power-Down Feature**
- **Absolute Output Frequency Tolerance of ±5% (TSL230B)**
- **Nonlinearity Error Typically 0.2% at 100 kHz**
- **Stable 100 ppm/°C Temperature Coefficient**
- **Advanced LinCMOS™ Technology**

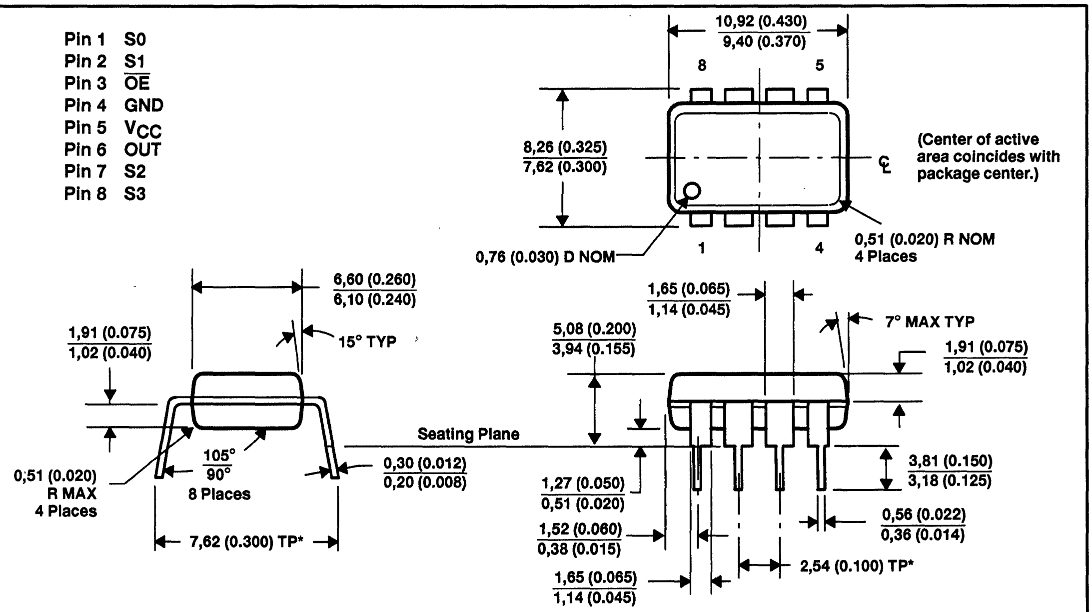
description

The TSL230, TSL230A, and TSL230B programmable light-to-frequency converters combine a configurable silicon photodiode and a current-to-frequency converter on single monolithic CMOS integrated circuits. The output can be either a pulse train or a square wave (50% duty cycle) with frequency directly proportional to light intensity. The sensitivity of the devices is selectable in three ranges, providing two decades of adjustment. The full-scale output frequency can be scaled by one of four preset values. All inputs and the output are TTL compatible, allowing direct two-way communication with a microcontroller for programming and output interface. An output enable ($\overline{OE}$) is provided that places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line. The devices are available with absolute-output-frequency tolerances of ±5% (TSL230B), ±10% (TSL230A), or ±20% (TSL230). Each circuit has been temperature compensated for the ultraviolet-to-visible-light range of 300 nm to 700 nm. The devices are characterized for operation over the temperature range of −25°C to 70°C.

mechanical data

The TSL230, TSL230A, and TSL230B are packaged in a clear plastic 8-pin dual-in-line package. The photodiode area is typically 1.36 mm^2 (0.0029 in^2) (S0 = S1 = H).

Pin 1	S0
Pin 2	S1
Pin 3	$\overline{OE}$
Pin 4	GND
Pin 5	V_{CC}
Pin 6	OUT
Pin 7	S2
Pin 8	S3



*True position when unit is installed.

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Terminal Functions

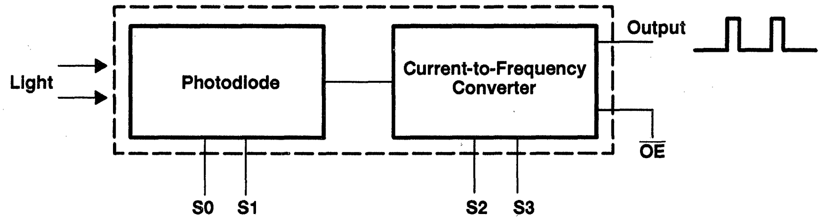
TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{OE}$	3	I	Enable for f_O (active low)
OUT	6	O	Scaled-frequency (f_O) output
S0, S1	1, 2	I	Sensitivity-select inputs
S2, S3	7, 8	I	f_O scaling-select inputs
V_{DD}	5		Supply voltage

Selectable Options

S1	S0	SENSITIVITY
L	L	Power Down
L	H	1×
H	L	10×
H	H	100×

S3	S2	f_O SCALING (divide-by)
L	L	1
L	H	2
H	L	10
H	H	100

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 6.5 V
Input voltage range, all inputs, V_I .... −0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A .... −25°C to 70°C
Storage temperature range .... −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	5	6	V
High-level input voltage, V_{IH}	V_{DD} = 4.5 V to 5.5 V	2		V_{DD}	V
Low-level input voltage, V_{IL}	V_{DD} = 4.5 V to 5.5 V	0		0.8	V
Operating free-air temperature range, T_A		−25		70	°C

electrical characteristics at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	4	4.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.17	0.26	V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				1	µA
I_{DD}	Supply current	Power-on mode		2	3	mA
		Power-down mode			10	µA
	Full-scale frequency†		1.1			MHz
	Temperature coefficient of output frequency	λ ≤ 700 nm, –25°C ≤ T_A ≤ 70°C		±100		ppm/°C
k_{SVS}	Supply voltage sensitivity	V_{DD} = 5 V ±10%		0.5		%/V

† Full-scale frequency is the maximum operating frequency of the device without saturation.

operating characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TSL230			TSL230A			TSL230B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	S0 = H, S1 = S2 = S3 = L, E_e = 130 mW/cm^2, λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0, S0 = H, S1 = S2 = S3 = L		0.1	10		0.1	10		0.1	10	Hz
		S1 = H, S0 = S2 = S3 = L, E_e = 13 mW/cm^2, λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0 S1 = H, S0 = S2 = S3 = L		0.13	10		0.13	10		0.13	10	Hz
		S0 = S1 = H, S2 = S3 = L, E_e = 1.3 mW/cm^2, λ_p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz
		E_e = 0, S0 = S1 = H, S2 = S3 = L		0.5	10		0.5	10		0.5	10	Hz
t_w	Output pulse duration	S2 = S3 = L	125		550	125		550	125		550	ns
		S2 or S3 = H		1/2f_O			1/2f_O			1/2f_O		s
	Nonlinearity‡	f_O = 0 MHz to 10 kHz		±0.1%			±0.1%			±0.1%		%F.S.
		f_O = 0 MHz to 100 kHz		±0.2%			±0.2%			±0.2%		%F.S.
		f_O = 0 MHz to 1 MHz		±0.5%			±0.5%			±0.5%		%F.S.
	Recovery from power down				100			100			100	µs
	Step response to full-scale step input		1 pulse of new frequency plus 1 µs									
	Response time to programming change		2 periods of new principal frequency plus 1 µs§									
	Response time to output enable ($\overline{OE}$)			50	150		50	150		50	150	ns

† Full-scale frequency is the maximum operating frequency of the device without saturation.
‡ Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.
§ Principal frequency is the internal oscillator frequency, equivalent to divide-by-1 output selection.

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY
vs
IRRADIANCE

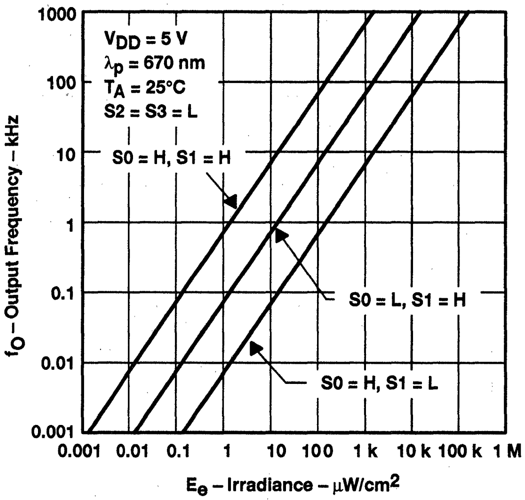


Figure 1

PHOTODIODE SPECTRAL RESPONSIVITY

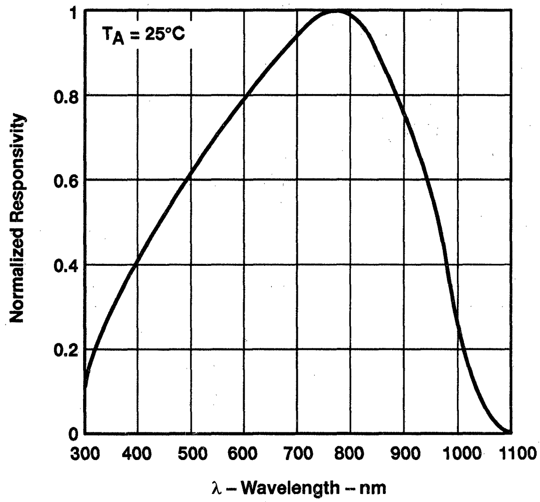


Figure 2

DARK FREQUENCY
vs
TEMPERATURE

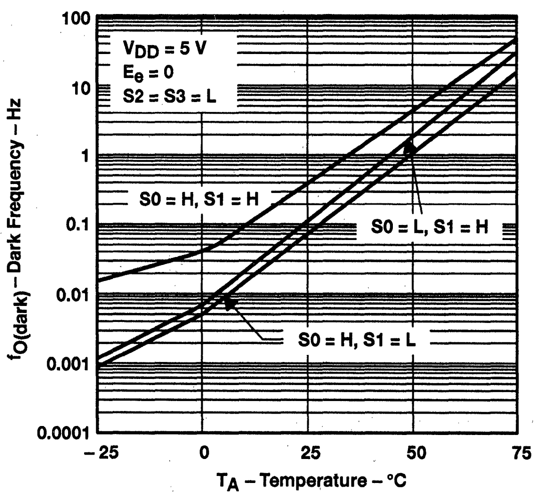


Figure 3

TEMPERATURE COEFFICIENT
OF OUTPUT FREQUENCY
vs
WAVELENGTH OF INCIDENT LIGHT

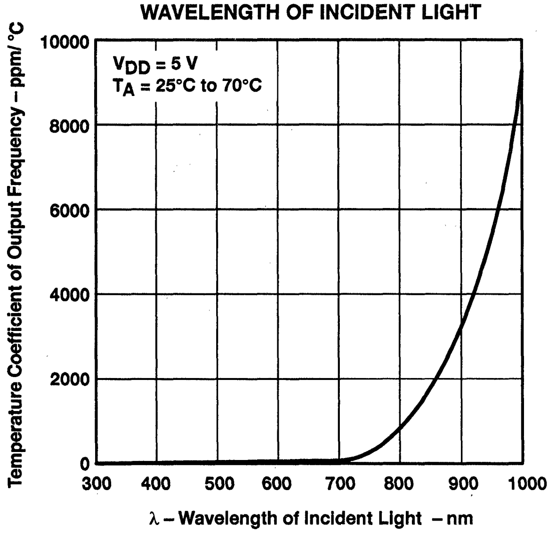


Figure 4

TYPICAL CHARACTERISTICS

**OUTPUT FREQUENCY
vs
SUPPLY VOLTAGE**

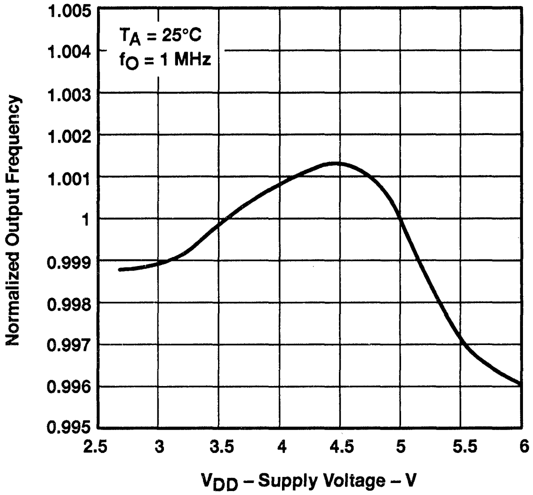


Figure 5

APPLICATION INFORMATION

power-supply considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-µF to 0.1-µF capacitor with short leads.

output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

sensitivity adjustment

Sensitivity is controlled by two logic inputs, S0 and S1. Sensitivity is adjusted using an electronic iris technique – effectively an aperture control – to change the response of the device to a given amount of light. The sensitivity can be set to one of three levels: 1x, 10x or 100x, providing two decades of adjustment. This allows the responsivity of the device to be optimized to a given light level while preserving the full-scale output-frequency range. Changing of sensitivity also changes the effective photodiode area by the same factor.

APPLICATION INFORMATION

output-frequency scaling

Output-frequency scaling is controlled by two logic inputs, S2 and S3. Scaling is accomplished on chip by internally connecting the pulse-train output of the converter to a series of frequency dividers. Divided outputs available are divide-by 2, 10, 100, and 1 (no division). Divided outputs are 50 percent-duty-cycle square waves while the direct output (divide-by 1) is a fixed-pulse-width pulse train. Because division of the output frequency is accomplished by counting pulses of the principal (divide-by 1) frequency, the final-output period represents an average of n (where n is 2, 10 or 100) periods of the principal frequency. The output-scaling-counter registers are cleared upon the next pulse of the principal frequency after any transition of the S0, S1, S2, S3, or OE lines. The output goes high upon the next subsequent pulse of the principal frequency, beginning a new valid period. This minimizes the time delay between a change on the input lines and the resulting new output period in the divided output modes. In contrast with the sensitivity adjust, use of the divided outputs lowers both the full-scale frequency and the dark frequency by the selected scale factor.

The frequency-scaling function allows the output range to be optimized for a variety of measurement techniques. The divide-by-1 or straight-through output can be used with a frequency counter, pulse accumulator, or high-speed timer (period measurement). The divided-down outputs may be used where only a slower frequency counter is available, such as a low-cost microcontroller, or where period measurement techniques are used. The divide-by-10 and divide-by-100 outputs provide lower frequency ranges for high resolution-period measurement.

measuring the frequency

The choice of interface and measurement technique depends on the desired resolution and data acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Using the divide-by-2 output, data can be collected at a rate of twice the output frequency or one data point every microsecond for full-scale output. Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. Output scaling can be used to increase the resolution for a given clock rate or to maximize resolution as the light input changes. Period measurement is used to measure rapidly varying light levels or to make a very fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration (the accumulation of pulses over a very long period of time) can be used to measure exposure, the amount of light present in an area over a given time period.

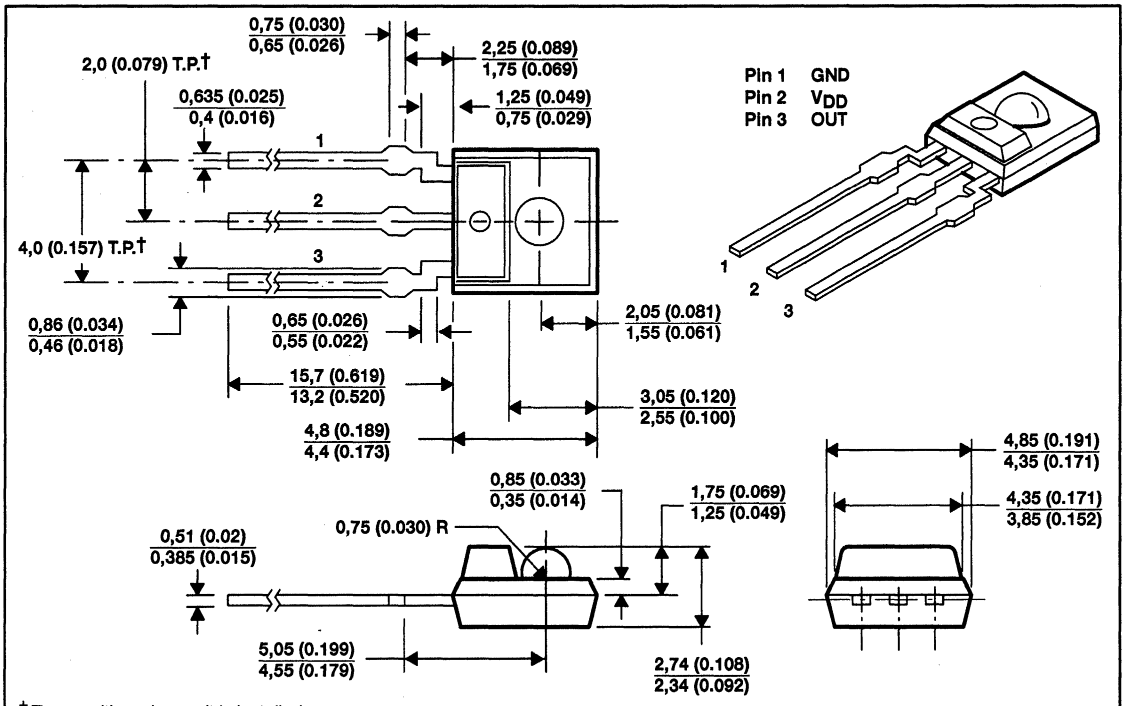
- **High-Resolution Conversion of Light Intensity to Frequency With No External Components**
- **Communicates Directly With a Microcontroller**
- **Compact Three-Leaded Clear-Plastic Package**
- **Single-Supply Operation Down to 2.7 V**
- **Nonlinearity Error Typically 0.2% at 100 kHz**
- **Stable 100 ppm/°C Temperature Coefficient**
- **Advanced LinCMOS™ Technology**

description

The TSL235 light-to-frequency converter combines a silicon photodiode and a current-to-frequency converter on a single monolithic CMOS integrated circuit. The output is a square wave (50% duty cycle) with frequency directly proportional to light intensity. Because it is TTL compatible, the output allows direct interface to a microcontroller or other logic circuitry. The device has been temperature compensated for the ultraviolet-to-visible light range of 300 nm to 700 nm and responds over the light range of 300 nm to 1100 nm. The TSL235 is characterized for operation over the temperature range of −25°C to 70°C.

mechanical data

The TSL235 is offered in a clear-plastic three-leaded package. The photodiode area is 1.36 mm^2 (0.0029 in^2).



† True position when unit is installed.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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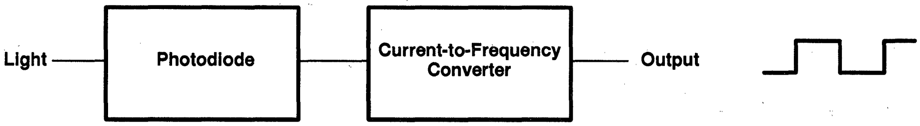
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 6.5 V
Operating free-air temperature range, T_A .... –25°C to 70°C
Storage temperature range .... –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	5	6	V
Operating free-air temperature range, T_A	–25		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA	4	4.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.17	0.26	V
I_{DD}	Supply current			2	3	mA
	Full-scale frequency‡		500			kHz
	Temperature coefficient of output frequency	$\lambda \le 700$ nm, $-25°C \le T_A \le 70°C$		±100		ppm/°C
k_{SVS}	Supply-voltage sensitivity	V_{DD} = 5 V ±10%		0.5		%/V

‡ Full-scale frequency is the maximum operating frequency of the device without saturation.

operating characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_O	Output frequency	E_e = 375 µW/cm^2, λ_p = 670 nm	200	250	300	kHz
		E_e = 0		0.25	10	Hz
	Nonlinearity§	f_O = 0 kHz to 10 kHz		±0.1%		%F.S.
		f_O = 0 kHz to 100 kHz		±0.2%		%F.S.
	Step response to full-scale step input			1 pulse of new frequency plus 1 µs		

‡ Full-scale frequency is the maximum operating frequency of the device without saturation.
§ Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY vs IRRADIANCE

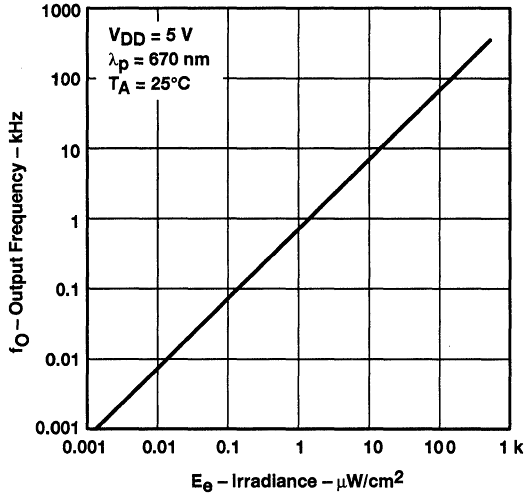


Figure 1

PHOTODIODE SPECTRAL RESPONSIVITY

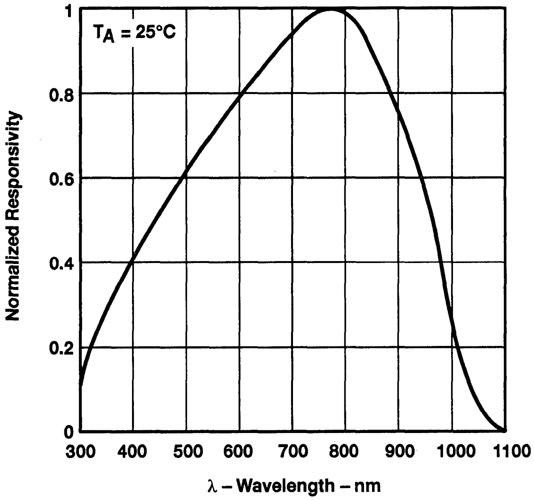


Figure 2

DARK FREQUENCY vs TEMPERATURE

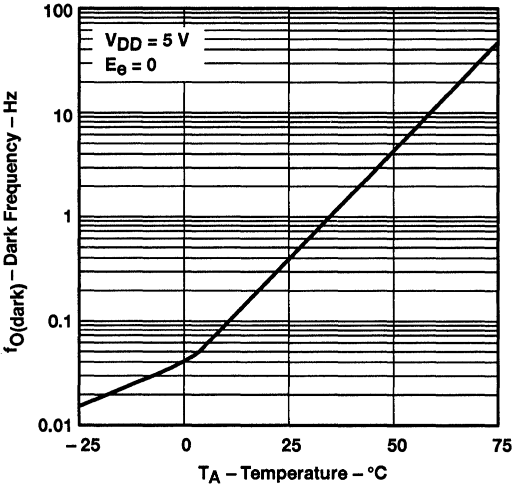


Figure 3

TEMPERATURE COEFFICIENT OF OUTPUT FREQUENCY vs WAVELENGTH OF INCIDENT LIGHT

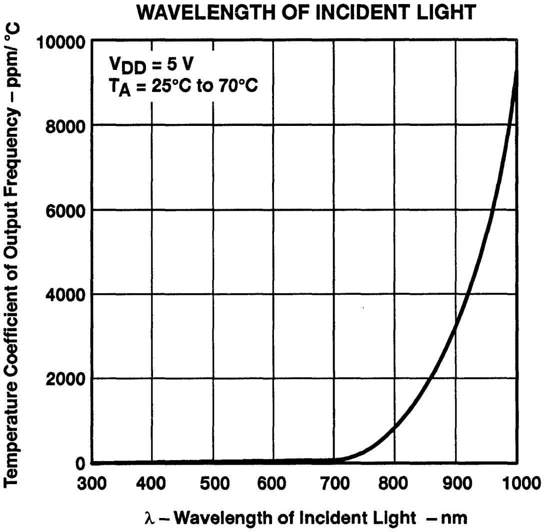


Figure 4

TYPICAL CHARACTERISTICS

OUTPUT FREQUENCY
vs
SUPPLY VOLTAGE

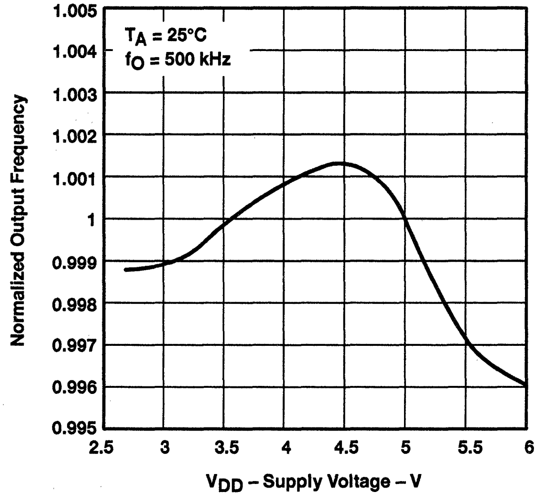


Figure 5

APPLICATION INFORMATION

power-supply considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01-μF to 0.1-μF capacitor with short leads (see Figure 6).

output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

measuring the frequency

The choice of interface and measurement technique depends on the desired resolution and data-acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. The technique is employed to measure rapidly varying light levels or to make a fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration, the accumulation of pulses over a very long period of time, can be used to measure exposure – the amount of light present in an area over a given time period.

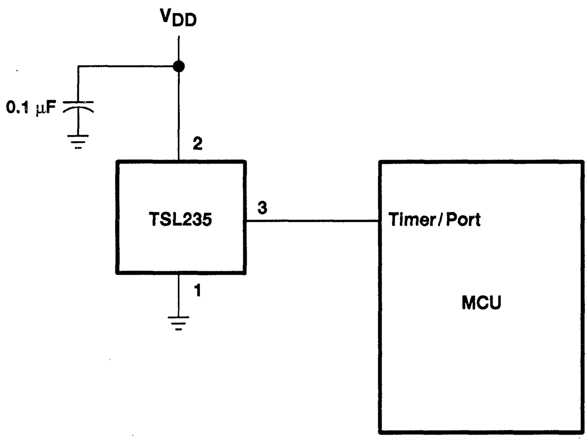


Figure 6. Typical TSL235 Interface to a Microcontroller

TSL250, TSL251, TSL252
LIGHT-TO-VOLTAGE OPTICAL SENSORS

SOES004B–D3732, AUGUST 1991– REVISED AUGUST 1992

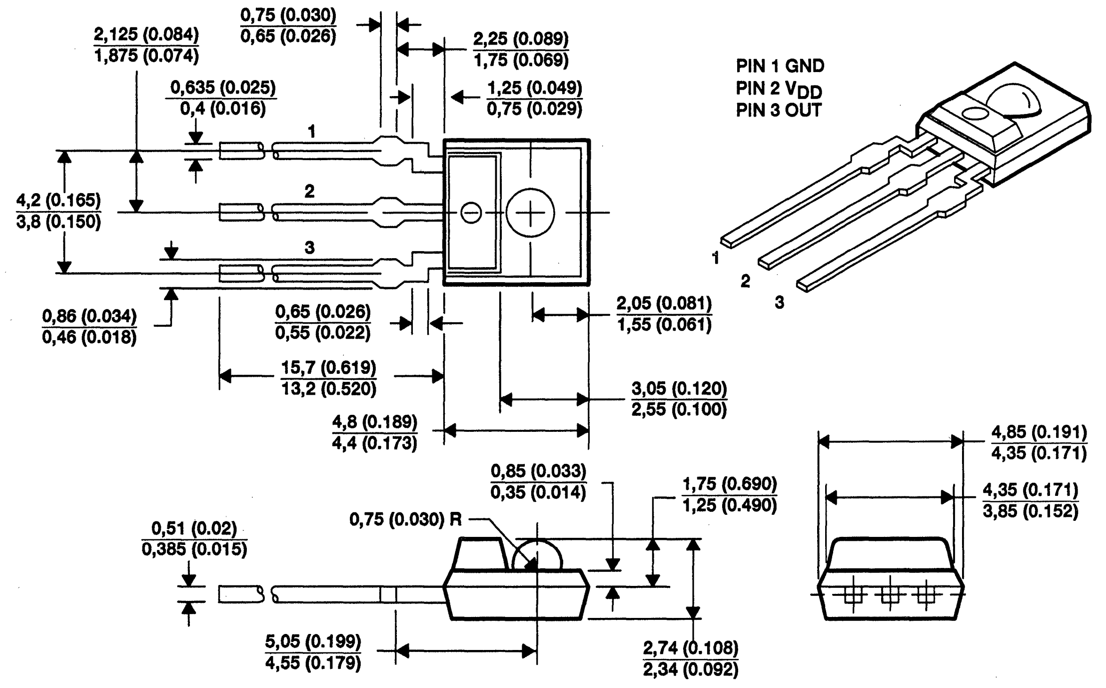
- **Monolithic Silicon IC Containing Photodiode, Operational Amplifier, and Feedback Components**
- **Converts Light Intensity to Output Voltage**
- **High Irradiance Responsivity Typically 80 mV/(μW/cm^2) at λ_p = 880 nm (TSL250)**
- **Compact Three-Leaded Clear Plastic Package**
- **Low Dark (Offset) Voltage . . . 10 mV Max at 25°C, V_{DD} = 5 V**
- **Single-Supply Operation**
- **Wide Supply Voltage Range . . . 3 V to 9 V**
- **Low Supply Current . . . 800 μA Typical at V_{DD} = 5 V**
- **Advanced LinCMOS™ Technology**

description

The TSL250, TSL251, and TSL252 are light-to-voltage optical sensors each combining a photodiode and a transimpedance amplifier (feedback resistor = 16 MΩ, 8 MΩ, and 2 MΩ, respectively) on a single monolithic IC. The output voltage is directly proportional to the light intensity (irradiance) on the photodiode. The TSL250, TSL251, and TSL252 utilize Texas Instruments silicon-gate LinCMOS™ technology, which provides good amplifier offset-voltage stability and low power consumption.

mechanical data

The photodiode/amplifier chip is packaged in a clear plastic three-leaded package. The integrated photodiode active area is typically 1,0 mm^2 (0.0016 in^2), 0.5 mm^2 (0.00078 in^2), and 0.26 mm^2 (0.0004 in^2) for the TSL250, TSL251, and TSL252, respectively.



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TEXAS INSTRUMENTS
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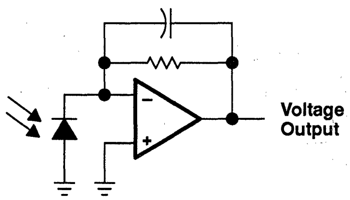
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) .... 10 V
Output current, I_O .... ±10 mA
Duration of short-circuit current at (or below) 25°C (see Note 2) .... 5 s
Operating free-air temperature range, T_A .... –25°C to 85°C
Storage temperature range .... –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 240°C

NOTES: 1. All voltages are with respect to GND.
2. Output may be shorted to either supply.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	9	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C, λp = 880 nm, R_L = 10 kΩ (unless otherwise noted) (see Note 3)

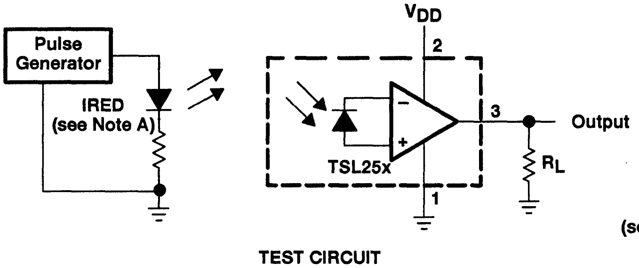
PARAMETER		TEST CONDITIONS	TSL250 MIN	TSL250 TYP	TSL250 MAX	TSL251 MIN	TSL251 TYP	TSL251 MAX	TSL252 MIN	TSL252 TYP	TSL252 MAX	UNIT
V_D	Dark voltage	E_e = 0		3	10		3	10		3	10	mV
V_{OM}	Maximum output	E_e = 2 mW/cm^2	3.1	3.5		3.1	3.5		3.1	3.5		V
V_O	Output voltage	E_e = 25 μW/cm^2	1	2	3							V
		E_e = 45 μW/cm^2				1	2	3				
		E_e = 285 μW/cm^2							1	2	3	
	Temperature coefficient of output voltage (V_O)	E_e = 25 μW/cm^2, T_A = 0°C to 70°C		±1								mV/°C
		E_e = 45 μW/cm^2, T_A = 0°C to 70°C					±1					
		E_e = 285 μW/cm^2, T_A = 0°C to 70°C								±1		
N_e	Irradiance responsivity	See Note 4		80			45			7		mV/(μW/cm^2)
I_{DD}	Supply current	E_e = 25 μW/cm^2		900	1600							μA
		E_e = 45 μW/cm^2					900	1600				
		E_e = 285 μW/cm^2								900	1600	

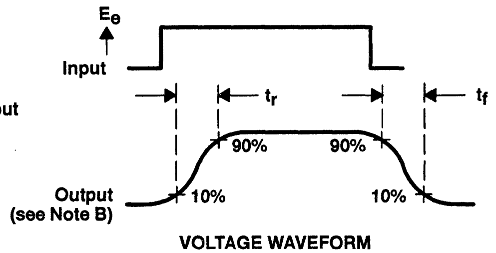
NOTES: 3. The input irradiance E_e is supplied by a GaAlAs infrared-emitting diode with λ_p = 880 nm.
4. Irradiance responsivity is characterized over the range V_O = 0.05 to 3 V.

operating characteristics at T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	TSL250 MIN	TSL250 TYP	TSL250 MAX	TSL251 MIN	TSL251 TYP	TSL251 MAX	TSL252 MIN	TSL252 TYP	TSL252 MAX	UNIT
t_r	Output pulse rise time	V_{DD} = 5 V, λ_p = 880 nm		360			90			7		µs
t_f	Output pulse fall time	V_{DD} = 5 V, λ_p = 880 nm		360			90			7		µs
V_n	Output noise voltage	V_{DD} = 5 V, f = 20 Hz		0.6			0.5			0.4		µV/√Hz

PARAMETER MEASUREMENT INFORMATION





NOTES: A. The input irradiance is supplied by a pulsed GaAlAs infrared-emitting diode with the following characteristics: λ_p = 880 nm, t_r < 1 µs, t_f < 1 µs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r < 100 ns, Z_i ≥ 1 MHz, C_i ≤ 20 pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

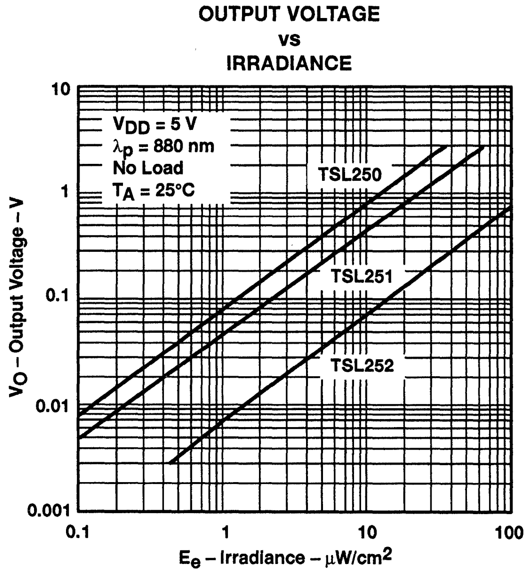


Figure 2

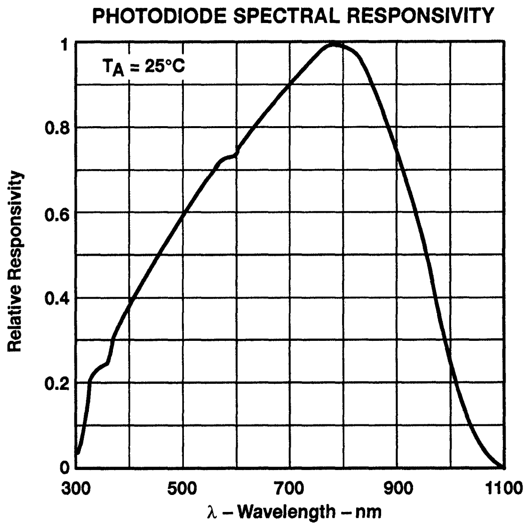


Figure 3

TYPICAL CHARACTERISTICS

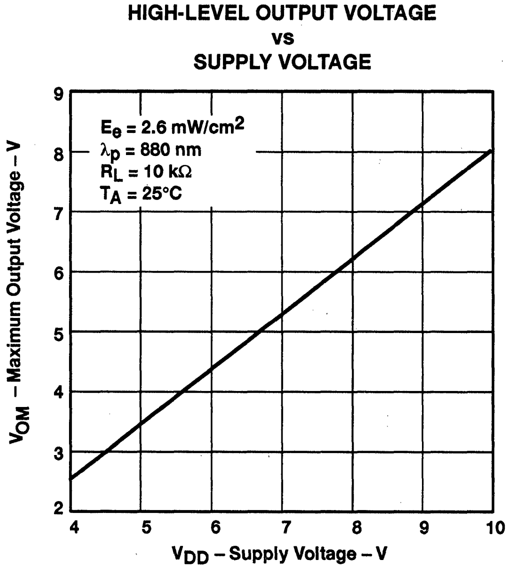


Figure 4

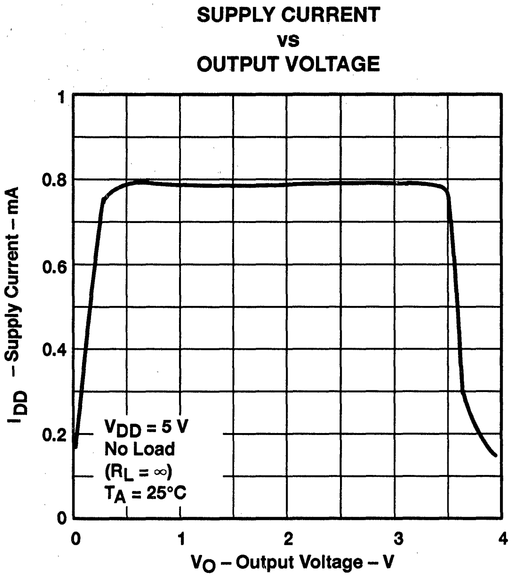


Figure 5

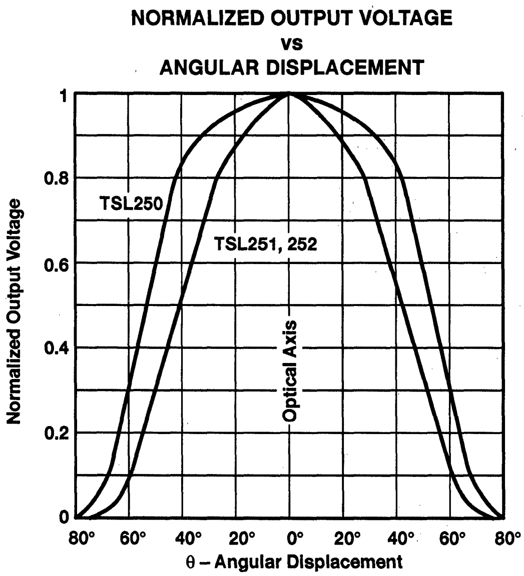


Figure 6

SOES008A – DECEMBER 1992 – REVISED FEBRUARY 1993

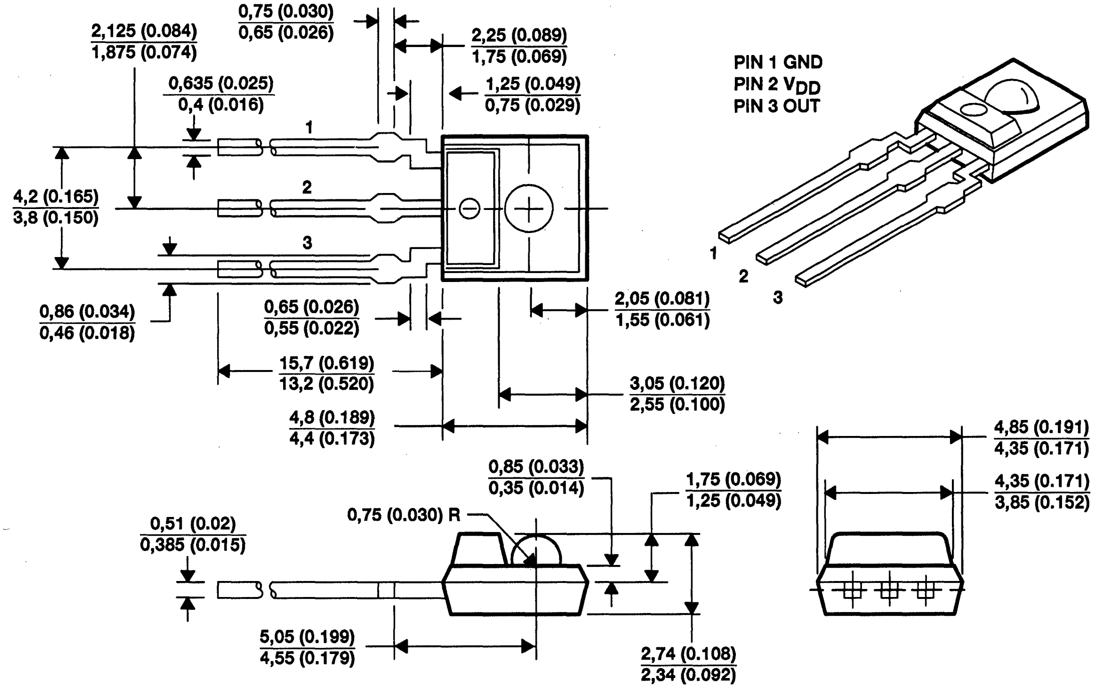
- **Integral Visible Light Cutoff Filter**
- **Monolithic Silicon IC Containing Photodiode, Operational Amplifier, and Feedback Components**
- **Converts Light Intensity to Output Voltage**
- **High Irradiance Responsivity Typically 42 mV/(μW/cm²) at λ_p = 940 nm (TSL260)**
- **Low Dark (Offset) Voltage . . . 10 mV Max at 25°C, V_{DD} = 5 V**
- **Single-Supply Operation**
- **Wide Supply Voltage Range . . . 3 V to 9 V**
- **Low Supply Current . . . 800 μA Typical at V_{DD} = 5 V**
- **Advanced LinCMOS™ Technology**

description

The TSL260, TSL261, and TSL262 are light-to-voltage optical sensors each combining a photodiode and a transimpedance amplifier (feedback resistor = 16 MΩ, 8 MΩ, and 2 MΩ, respectively) on a single monolithic integrated circuit. The output voltage is directly proportional to the infrared light intensity (irradiance) on the photodiode. The TSL260, TSL261, and TSL262 utilize Texas Instruments silicon-gate LinCMOS™ technology, which provides good amplifier offset-voltage stability and low power consumption.

mechanical data

The photodiode/amplifier chip is packaged in a black, infrared-transmissive plastic package. The integrated photodiode active area is typically 1,0 mm² (0.0016 in²), 0.5 mm² (0.00078 in²), and 0.26 mm² (0.0004 in²) for the TSL260, TSL261, and TSL262, respectively.



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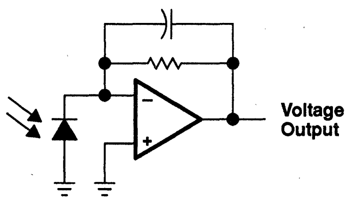
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) .... 10 V
Output current, I_O .... ±10 mA
Duration of short-circuit current at (or below) 25°C (see Note 2) .... 5 s
Operating free-air temperature range, T_A .... –25°C to 85°C
Storage temperature range .... –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 240°C

NOTES: 1. All voltages are with respect to GND.
2. Output may be shorted to either supply.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	9	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C, λp = 940 nm, R_L = 10 kΩ (unless otherwise noted) (see Note 3)

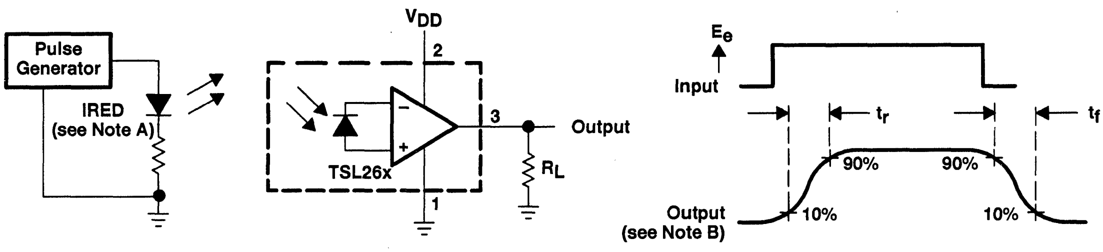
PARAMETER		TEST CONDITIONS	TSL260			TSL261			TSL262			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{DARK}	Dark voltage	E_e = 0		3	10		3	10		3	10	mV
V_{OM}	Maximum output	E_e = 2.6 mW/cm^2	3.1	3.5		3.1	3.5		3.1	3.5		V
V_O	Output voltage	E_e = 48 µW/cm^2	1	2	3							V
		E_e = 87 µW/cm^2				1	2	3				
		E_e = 525 µW/cm^2							1	2	3	
	Temperature coefficient of output voltage (V_O)	E_e = 48 µW/cm^2, T_A = 0°C to 70°C		±1								mV/°C
		E_e = 87 µW/cm^2, T_A = 0°C to 70°C					±1					
		E_e = 525 µW/cm^2, T_A = 0°C to 70°C								±1		
N_e	Irradiance responsivity	See Note 4		42			23			3.8		mV/(µW/cm^2)
I_{DD}	Supply current	E_e = 48 µW/cm^2, No load		900	1600							µA
		E_e = 87 µW/cm^2, No load					900	1600				
		E_e = 525 µW/cm^2, No load								900	1600	

NOTES: 3. The input irradiance E_e is supplied by a GaAs infrared-emitting diode with λ_p = 940 nm.
4. Irradiance responsivity is characterized over the range V_O = 0.05 to 3 V.

operating characteristics at T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS	TSL260			TSL261			TSL262			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Output pulse rise time	V_{DD} = 5 V, λ_p = 940 nm		360			90			7		µs
t_f	Output pulse fall time	V_{DD} = 5 V, λ_p = 940 nm		360			90			7		µs
V_n	Output noise voltage	V_{DD} = 5 V, f = 20 Hz		0.6			0.5			0.4		µV/√Hz

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORM

NOTES: A. The input irradiance is supplied by a pulsed GaAs infrared-emitting diode with the following characteristics: λ_p = 940 nm, t_r < 1 µs, t_f < 1 µs.

B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r < 100 ns, Z_i ≥ 1 MHz, C_i ≤ 20 pF.

Figure 1. Switching Times

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs IRRADIANCE

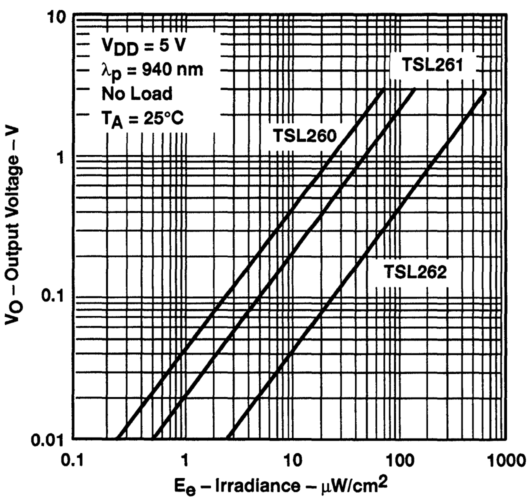


Figure 2

PHOTODIODE SPECTRAL RESPONSE

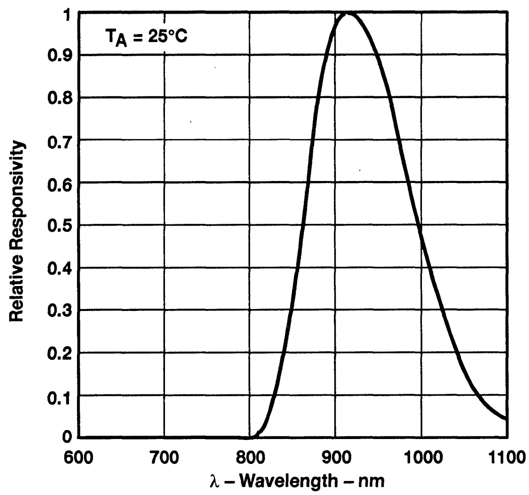


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

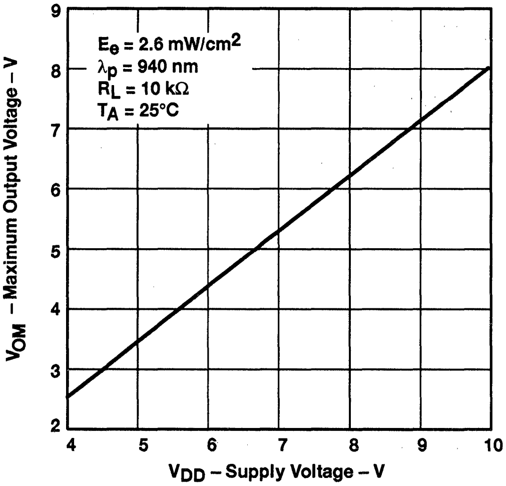


Figure 4

SUPPLY CURRENT
vs
OUTPUT VOLTAGE

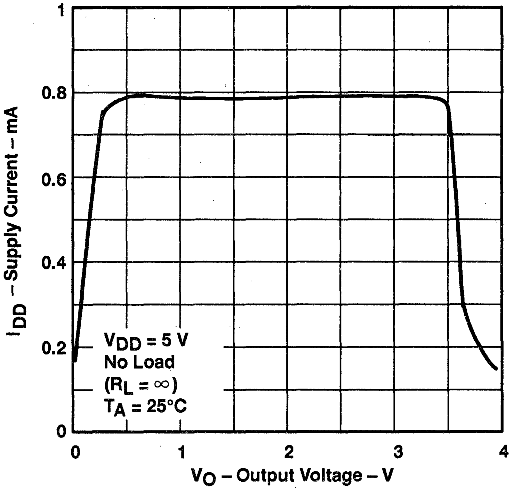


Figure 5

NORMALIZED OUTPUT VOLTAGE
vs
ANGULAR DISPLACEMENT

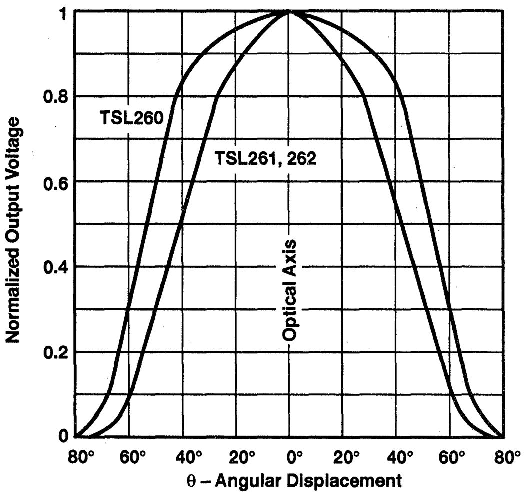
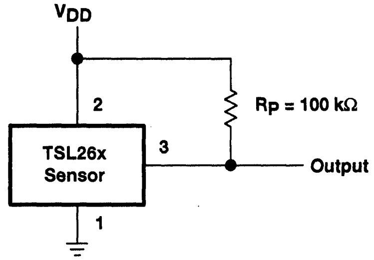


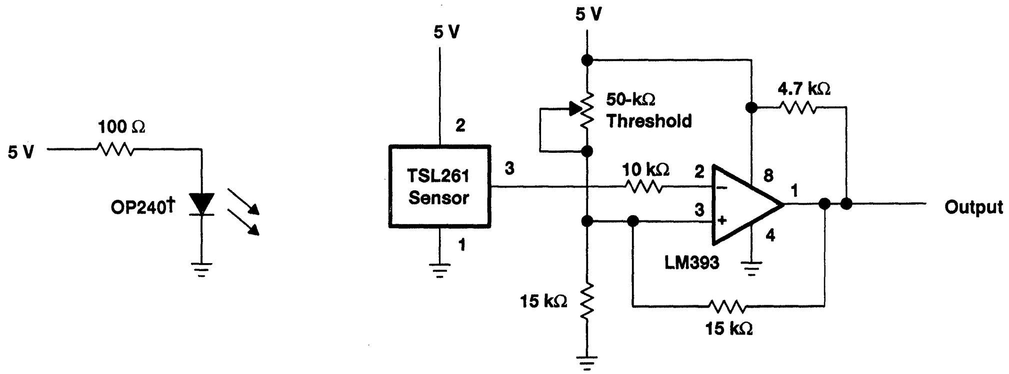
Figure 6

APPLICATION INFORMATION



NOTE A: Pullup resistor extends linear output range to near V_{DD} with minimal (several millivolts typical) effect on V_{DARK}; particularly useful at low V_{DD} (3 V to 5 V).

Figure 7. Pullup for Increased V_{OM}

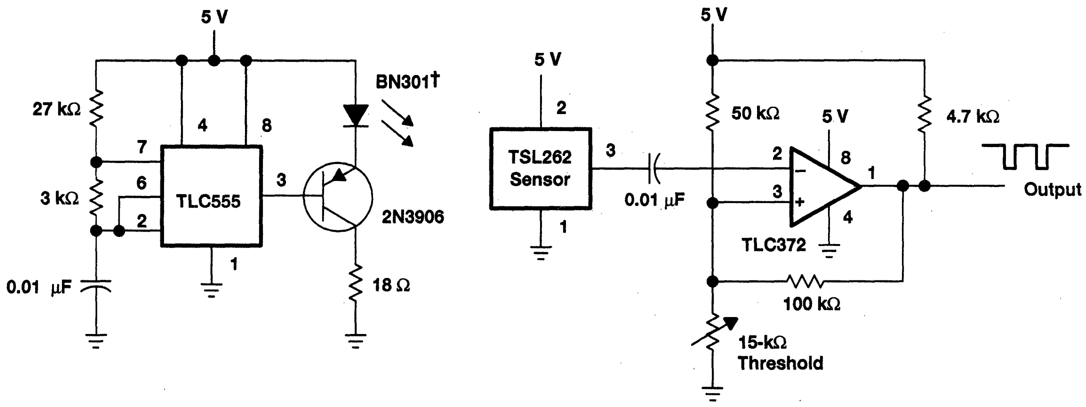


† OPTEK part number

NOTE A: Output goes high when beam is interrupted; working distance is several inches or less. Intended for use as optical-interrupter switch or reflective-object sensor.

Figure 8. Short-Range Optical Switch With Hysteresis

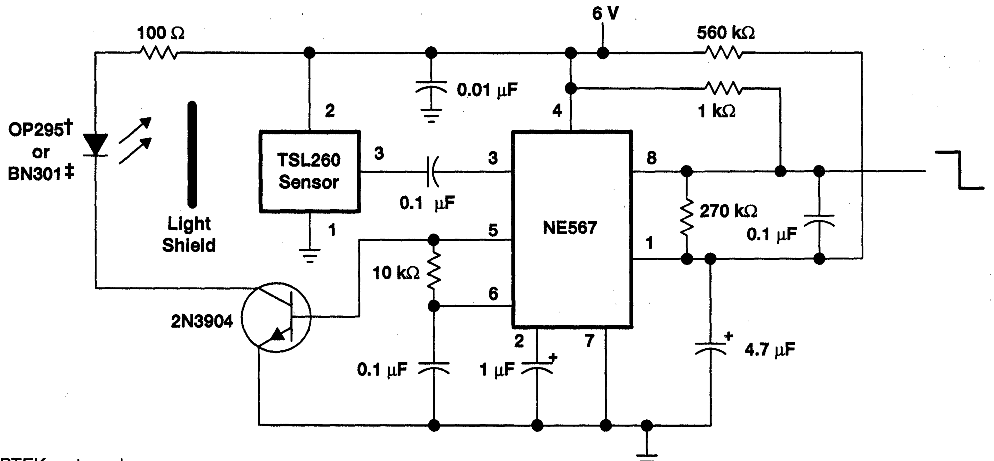
APPLICATION INFORMATION



† Stanley part number

NOTE A: Output pulses low until beam is interrupted. Useful range is 1 ft to 20 ft; can be extended with lenses. This configuration is suited for object detection, safety guards, security systems, and automatic doors.

Figure 9. Pulsed Optical-Beam Interrupter



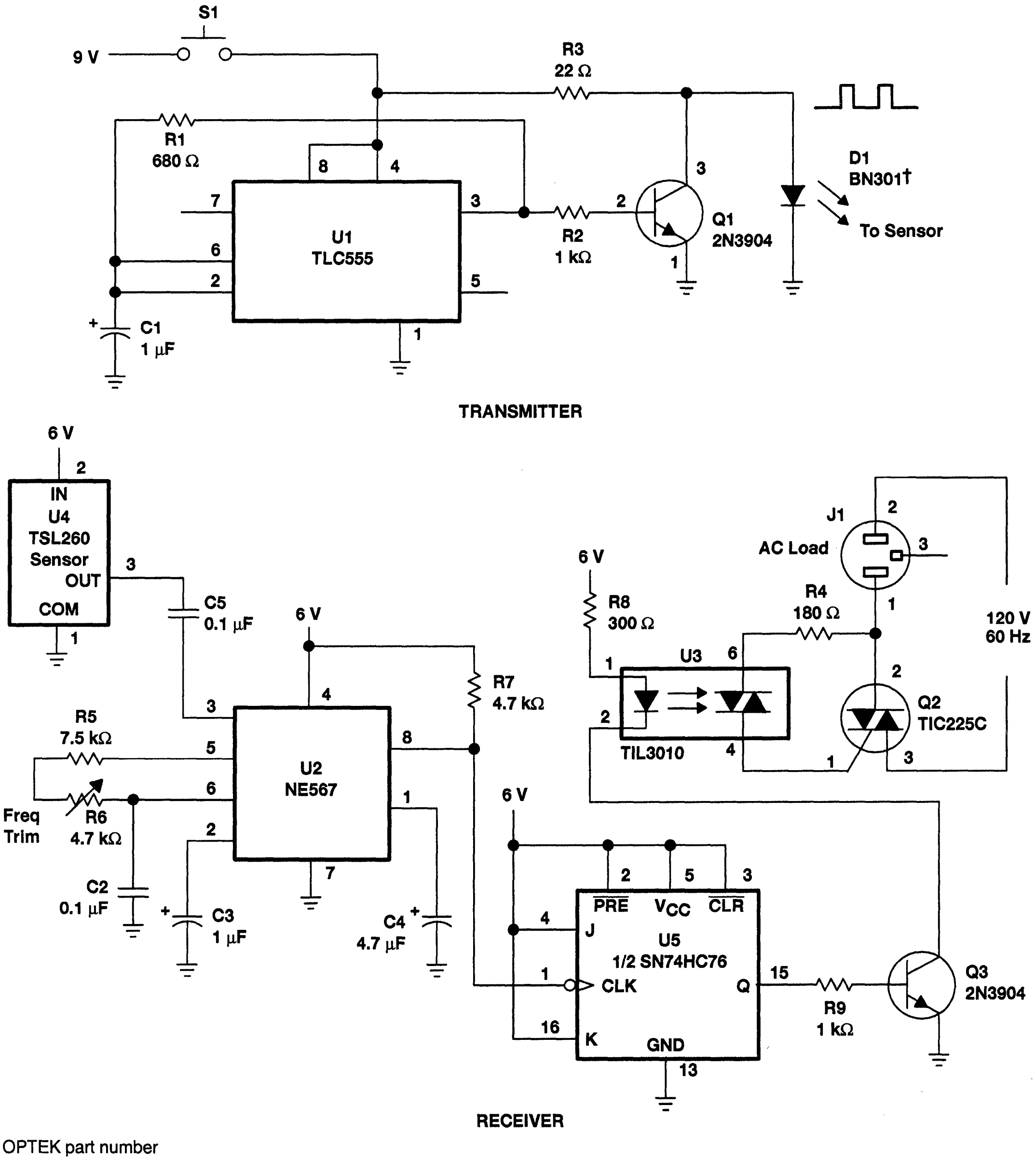
† OPTEK part number

‡ Stanley part number

NOTE A: Output goes low when light pulses from emitter are reflected back to sensor. Range is 6 in to 18 in depending upon object reflectance. Useful for automatic doors, annunciators, object avoidance in robotics, automatic faucets, and security systems.

Figure 10. Proximity Detector

APPLICATION INFORMATION

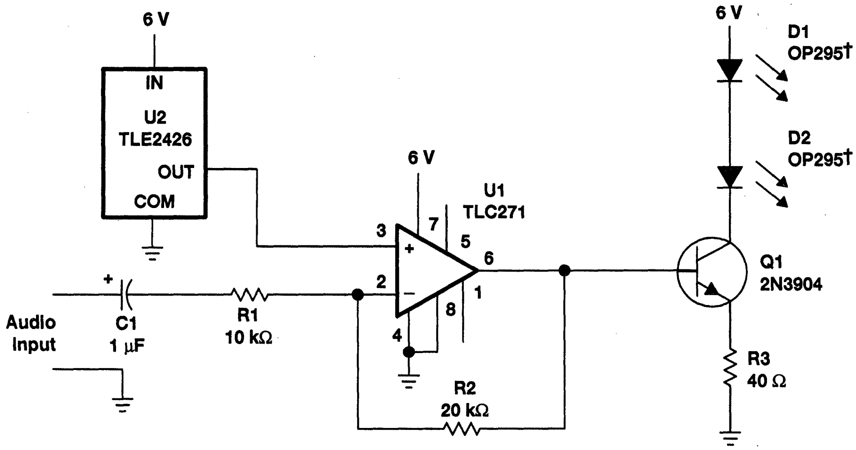


† OPTEK part number

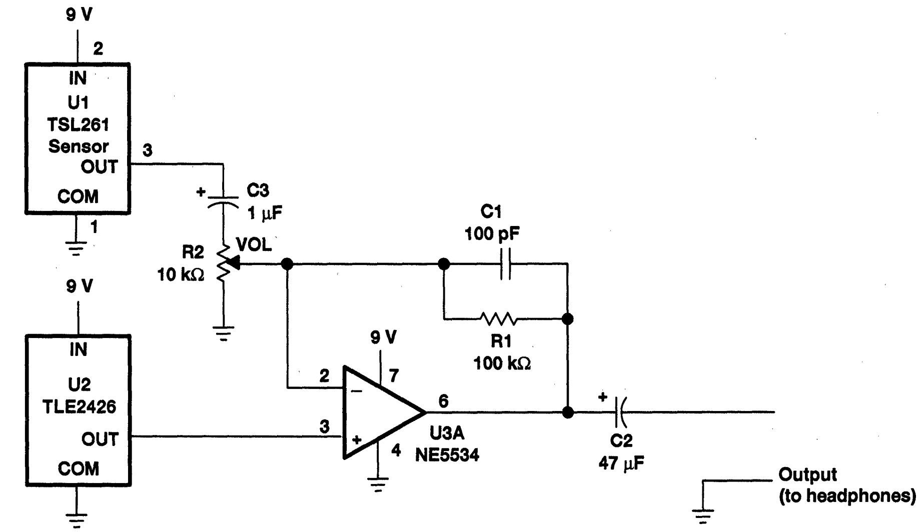
NOTE A: Single-channel remote control can be used to switch logic or light dc loads by way of U5 or ac loads by way of the optocoupler and triac as shown. Applications include ceiling fans, lamps, electric heaters, etc.

Figure 11. IR Remote Control

APPLICATION INFORMATION



TRANSMITTER



RECEIVER

† OPTEK part number

NOTE A: Simple transmission of audio signal over short distances (<10 ft). Applications include wireless headphones, wireless-telephone headset, and wireless-headset intercom.

Figure 12. IR Voice-Band Audio Link

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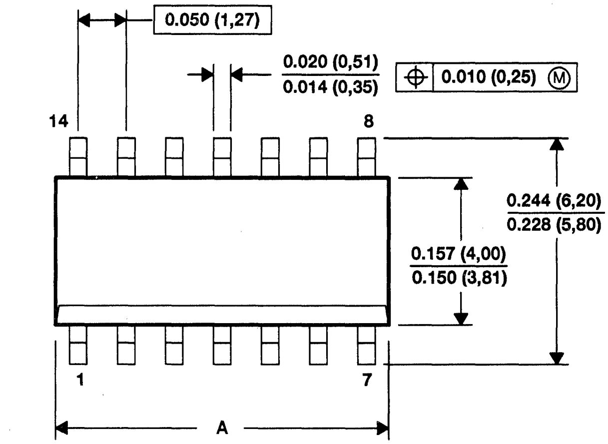
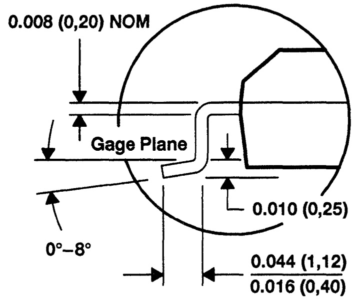
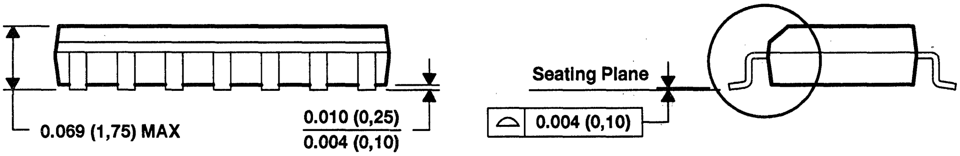
D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)





4040047/ B10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die-mount pad.
E. Falls within JEDEC MS-012

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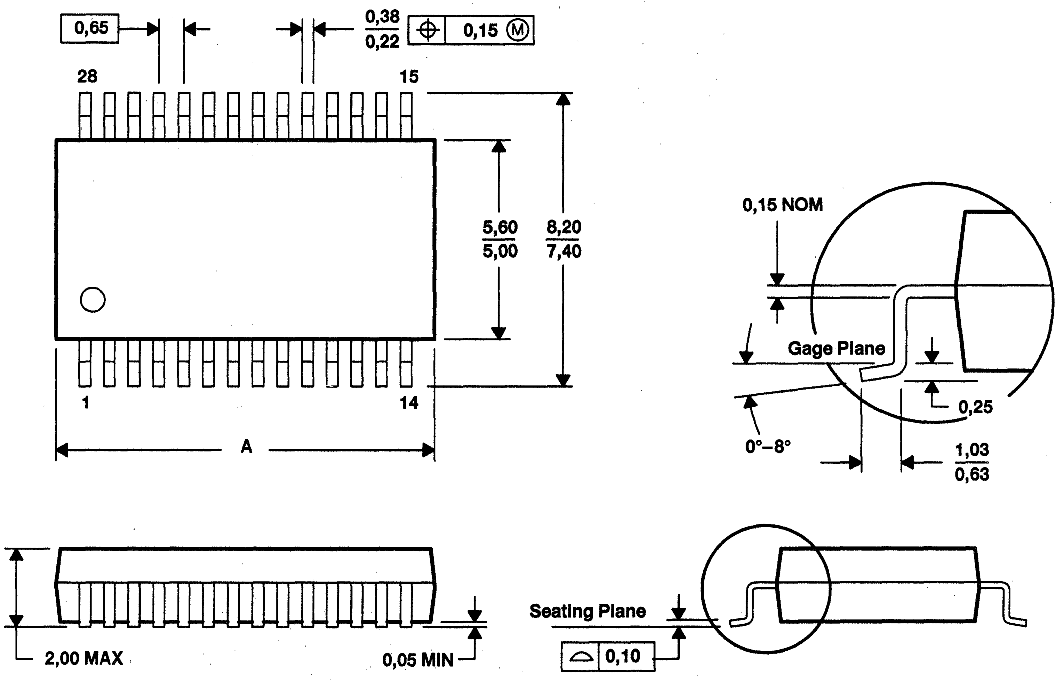
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
D. Falls within JEDEC MO-150

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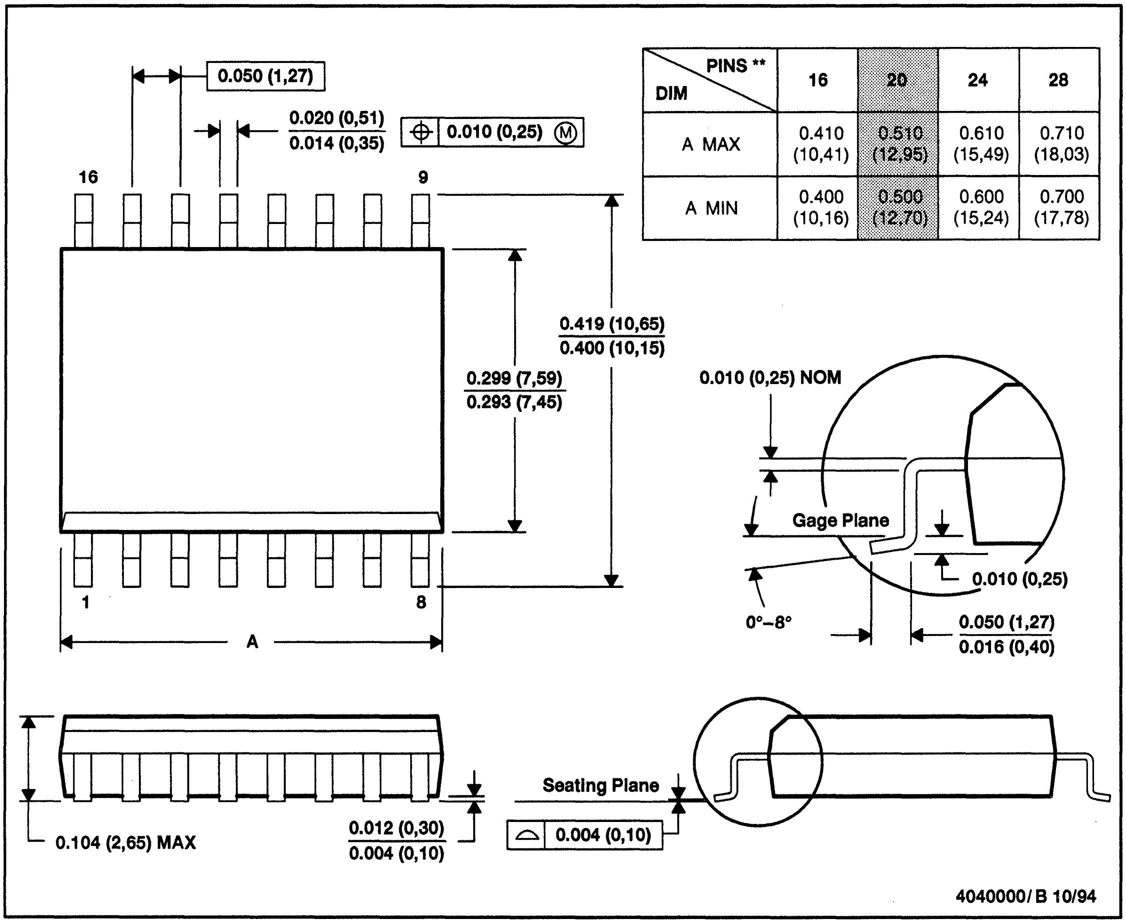
DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN

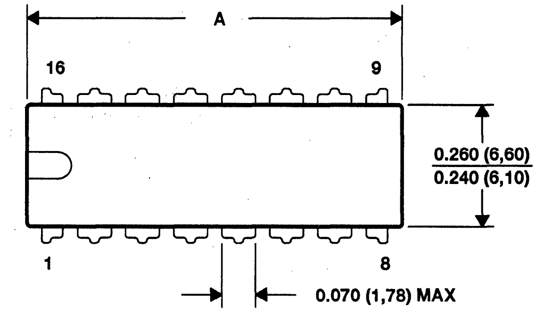


PINS ** / DIM	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

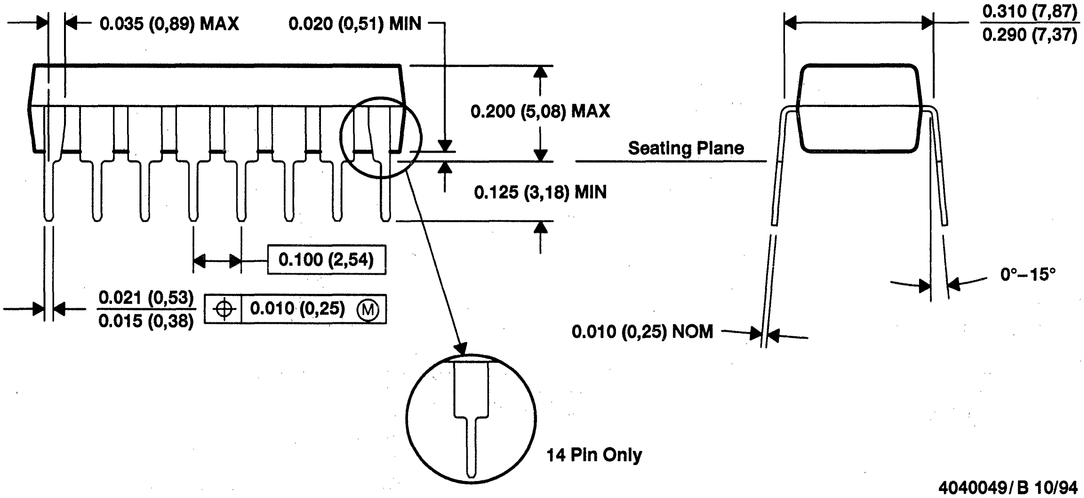
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



PINS ** / DIM	14	16	20
A MAX	0.780 (19,81)	0.775 (19,69)	0.975 (24,77)
A MIN	0.710 (18,03)	0.745 (18,92)	0.940 (23,88)



4040049/B 10/94

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter then MS-001)

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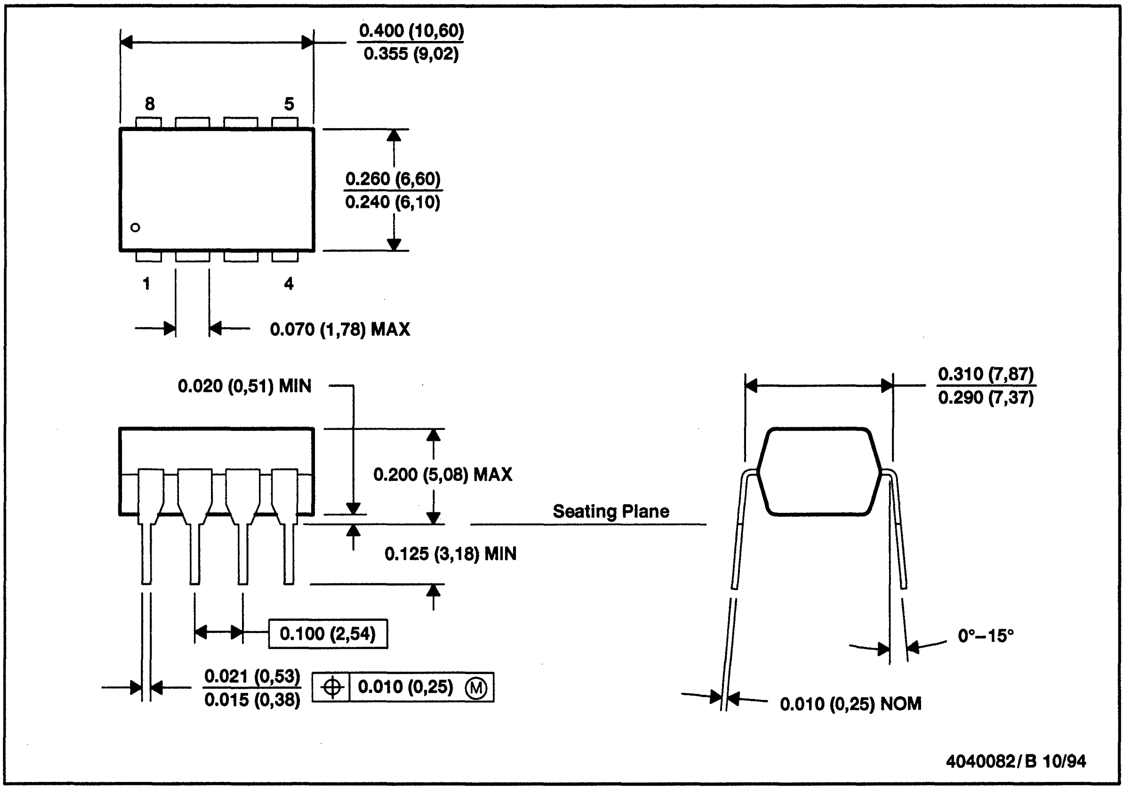
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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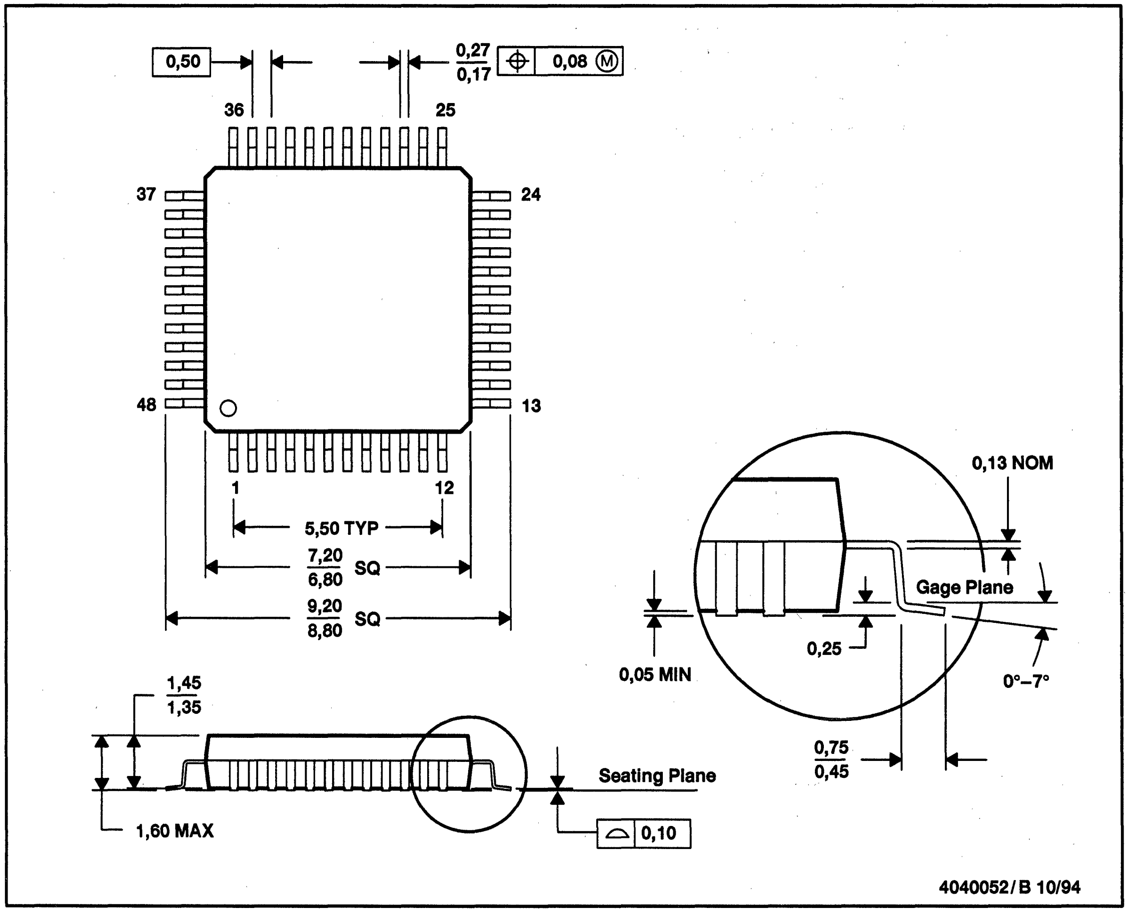
PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. Also may be a thermally enhanced plastic package with leads conected to the die pads

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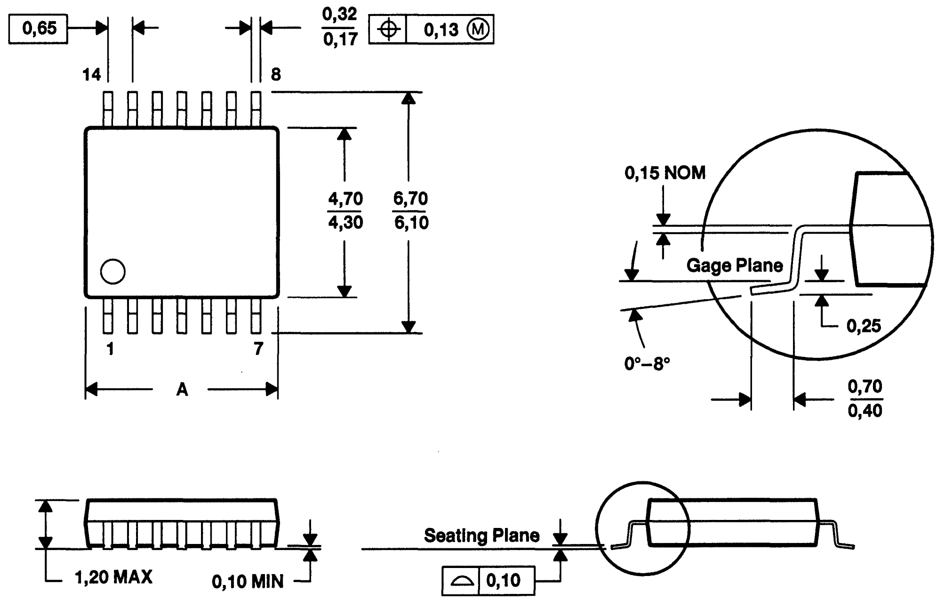
PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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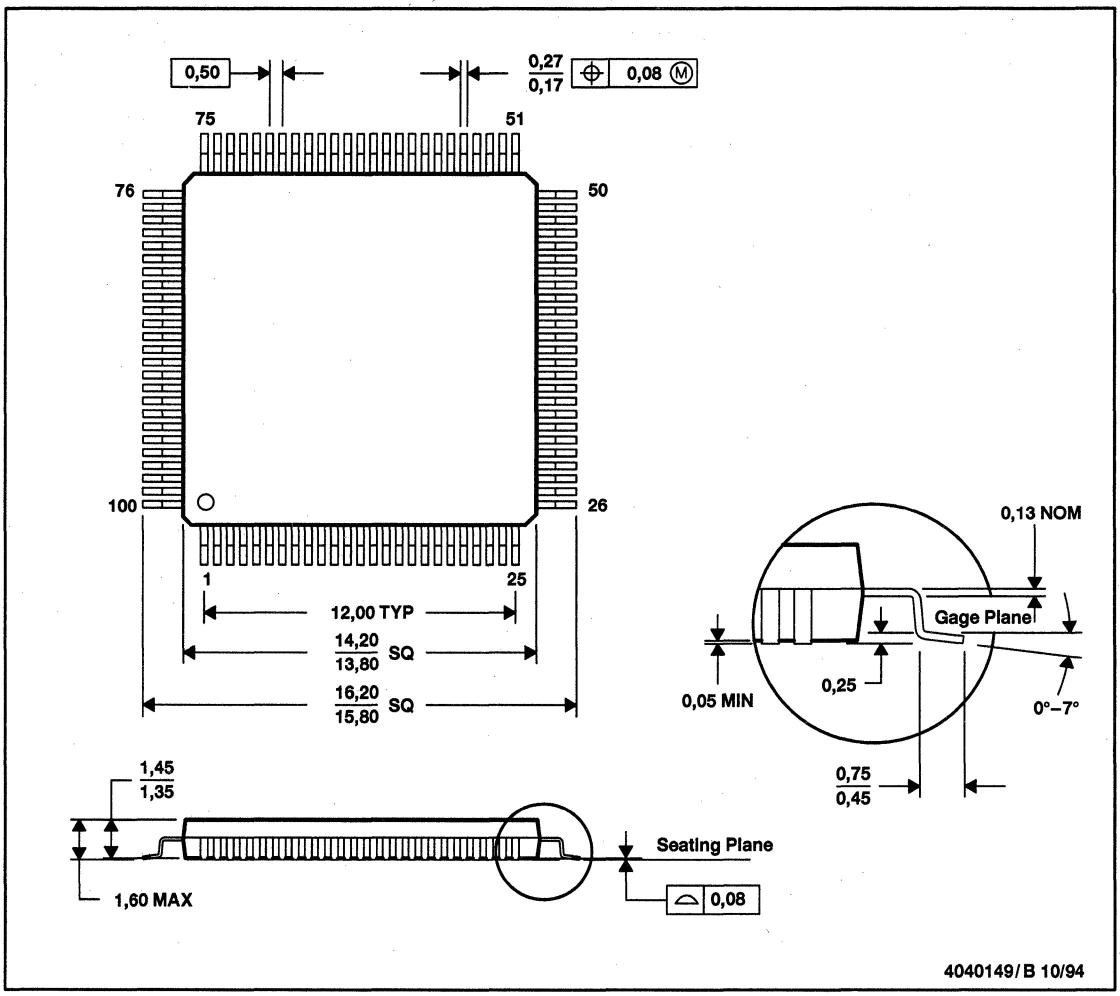
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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